國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

多晶鍺奈米線薄膜電晶體與無接面多晶矽奈米線場效電晶體製作與特性分析

A Study on the Fabrication and Characterization of Poly-Ge NWTFTs and Junctionless Poly-Si NWFETs

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中華民國九十九年十二月

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摘要

在本論文中，我們製作並研究兩種新穎的奈米線元件，多晶鍺奈米線薄膜電晶體(poly-Ge NWTFTs)與無接面多晶矽奈米線場效電晶體(JL poly-Si NWFETs)。多晶鍺奈米線薄膜電晶體採用一種先進的邊襯蝕刻技術形成奈米線，並利用固相結晶法(SPC)將非晶鍺轉換為多晶鍺。利用多閘極(multiple-gated)的結構，開關電流比可以增加至 10^4，次臨界擺幅可以改善至 0.64 V/dec。此外，我們也比較了具有獨立雙閘極(independent double-gated)的多晶鍺奈米線電晶體在各種模式操作時的特性。

無接面多晶矽奈米線場效電晶體(JL poly-Si NWFETs)利用一種簡單的方法，同時形成源/汲極與通道，且不需要離子佈植即可完成。在特性表現方面，無接面多晶矽奈米線場效電晶體擁有較佳的操作電流與更低的串連電阻。此外，增強型(IM)奈米線場效電晶體在特定操作條件下展現出低於 60m V/dec 的次臨界擺幅。

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Abstract

In this thesis, two kinds of nanowire devices, namely, poly-Ge nanowire thin film transistors (NWTFTs) and junctionless (JL) poly-Si nanowire field effect transistors (NWFETs) were fabricated and investigated. Poly-Ge NWTFTs were realized with a novel approach by adopting the sidewall spacer etching technique for NW channel formation. Solid phase crystallization (SPC) was utilized to transform amorphous Ge (α-Ge) to poly-Ge. By adopting multiple-gated structure, ON/OFF current ratio is increased to 10^4 and subthreshold swing (S.S.) is improved to 0.64V/dec. Besides, poly-Ge NWTFTs with independent double-gated (DG) configuration are characterized and compared. Each gate can be biased independently to manipulate the device.

JL poly-Si NWFETs were fabricated in a simplified manner duo to the fact that the source/drain (S/D) and channel was formed simultaneously without implantation. JL devices show better on-state performance and lower series resistance. On the other hand, the inversion mode (IM) NWFETs present ultra-low S.S. lower than 60mV/dec under specific operation conditions.

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劉禹伶
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Chapter 1

Introduction

1-1 Evolution of Nanowire Technology

In integrated circuit (IC) industry, it is well known that the size of transistors has to be scaled down continuously to achieve high operating speed and improved performance, thereby maintaining the benefit of products in each generation. The underlying principle for the downscaling of metal-oxide-semiconductor field-effect-transistor (MOSFET) is Moore's law [1-1]. In 1965, Gordon Moore observed that the number of transistors in a chip doubled every two years. As the feature size of transistor shrinks from deep sub-micrometer to nanometer scale, the conventional scaling methods of the semiconductor devices encounter increasing technological and fundamental challenges [1-2].

Recently, various novel devices based on nanostructures, such as nanowire, nano-ribbon, etc. have been widely proposed and investigated [1-3]. When a stripe-structured material with a diameter or feature size smaller than 100 nm, it is termed nanowire. Since nanowire has very tiny volume and large surface-to-volume ratio, transistors based on nanowire channel can possess better gate control capability compared to the conventional planar type MOSFETs [1-4]. In addition, nanowire channel can significantly restrain the short channel effects (SCEs) of transistors. By ingeniously designing the structure of nanowire devices, the leakage current can be effectively suppressed and therefore reducing the power consumption [1-5]. Owing to the aforementioned advantages, nanowires are feasible and promising for several applications in the future.

Based on the method of preparation, nanowires can be virtually separated into two classes, one is top-down, and the other is bottom-up [1-6]. In general, IC manufacturing utilizes the top-down approach, which fabricates devices and interconnects by standard IC processes such as photolithography, thin-film deposition, etching, and metallization [1-5]. These techniques are well developed and mature for mass production purpose. Nevertheless, directly defining the prerequisite nanowire patterns necessitates very expensive lithography equipments and advanced techniques such as deep-UV steppers, e-beam writers, or nano-imprint tools [1-7]. Although cheaper photolithographic processes (e.g., G-line and I-line steppers) are not capable of patterning nanowires directly, some helpful approaches like thermal flow [1-8], chemical shrink [1-9], and spacer patterning [1-10] have been proposed to help generate the nano-scale patterns using these conventional lithography tools. On the other hand, bottom-up approach is non-lithographic and the key techniques are chemical synthesis and self-assembly. In bottom-up method, the nanowires are synthesized through different chemical methods such as vapor–liquid–solid (VLS) [1-11], surface diffusion and epitaxy [1-12] [1-13], solution–liquid–solid (SLS), and oxide-assisted growth (OAG) [1-14]. Most commonly, nanowires are synthesized by using metal-catalyzed VLS method [1-15]. Although this method can be done under the premise of low cost, and the nanowire diameter defined during the growth or chemical synthesis process can be controlled with near-atomic-scale precision [1-16], it still faces repeatability, reliability and reproducibility problems. Moreover, metal contamination and electrodes alignment bring about significant obstructions.

1-2 Germanium Material Properties and Devices

As early as 1947, J. Bardeen, W. Brattain and W. Shockley developed the first transistor at Bell Laboratory by using germanium (Ge) as the device's substrate [1-17]. Recently, Ge has regained a considerable amount of interests in research due to its great potential as active channel materials for nano-scale CMOS transistors [1-18]. As shown in Table 1-I, Ge has several fascinating properties suitable for electronic devices. First, the electron and hole mobilities in crystalline Ge are much higher than that in crystal silicon (Si). This property enables Ge a good candidate as the channel material for high-speed devices and circuits. In comparison with Si, the mobility difference in magnitude between electrons and holes in Ge crystal is smaller; hence Ge has more advantages in design and fabrication of complementary metal-oxide-Semiconductor (CMOS) with a more symmetrical configuration. Secondly, Ge has lower melting and crystallization temperature as compared with Si. For example, the melting point of single crystal Ge is 937 ^{o}C, lower than that of Si (i.e., 1412 ^{o}C). Activation of the source/drain dopants can be done at a temperature as low as 400 ~ 500 ^{o}C [1-19]. These features allow Ge to be used in a variety of applications which demand low temperature processing. In addition, Ge also can be applied to non-silicon monolithic 3D integrated circuits (3D-ICs) [1-20].

However, applying Ge as device channel in MOSFETs has some daunting problems. Most higher-mobility materials have a much smaller band gap compared to Si and suffer from higher band-to-band-tunneling (BTBT) leakage, which may ultimately limit their scalability [1-21]. Moreover, unlike Si which can directly form high-quality oxide by high temperature thermal oxidation, the inferior quality of Ge-oxide makes it not suitable for gate insulator and isolation field oxide [1-22]

[1-23]. Fortunately, the recent advancement in the preparation of high-*k* dielectric enables the improvement in the characteristics of Ge MOSFETs [1-24] [1-25].

1-3 Overview of Multiple-gated Transistors

When the devices continue scaling down, precise control of critical structural parameters is a critical problem. For example, for single-gated fully depleted silicon-on-insulator (FDSOI) devices, the silicon body thickness must be about a third to a half of the gate length in order to retain good control over SCEs [1-26] [1-27]. However, high uniformity of the ultra-thin channel thickness is a basic requirement but very difficult to achieve. To relieve this concern, the adoption of multiple-gated field-effect transistor (MuGFET) structure [1-28] is most popularly taken into consideration. The MuGFET is a device with more than one side of the channel wrapped by the gate electrode. Double-gated FinFET, the thickness of the silicon channel (or the fin) between the two opposite gates is relaxed to approximate one or two-thirds of the physical gate length since each gate controls half the body thickness [1-29]. It means that the MuGFET has the ability to relax the physical and process limitations introduced with gate length scaling.

The double-gated FinFET, triple-gated, pi-gate, omega-gate and gate-all-around SOI devices all belong to the MuGFET architectures [1-30]. According to the ITRS roadmap [1-31], the excellent electrostatic control of these devices will be required for sub-25 nm gate lengths [1-32]. MuGFET devices realize some excellent virtues, such as great immunity against SCE, good gate controllability and near ideal subthreshold slope [1-33].

1-4 Overview of Junctionless MOSFET

A typical MOSFET involves the source-to-channel junction and the drain-to-channel junction. The junctions are called the PN junctions and consisted of ultra-sharp doping profile. For example, for a modern n-channel transistor, the source and drain are doped with n-type dopants at a concentration of 1×10^{20} atoms/cm^3 and the channel is of p-type doping at a concentration of 1×10^{18} atoms/cm^3 [1-34]. In very short-channel devices, the extraordinarily high doping concentration gradient imposes variation in diffusion of impurities over a distance of a few nanometers. This requires a very tight thermal budget which shrinks dramatically with device scaling.

Recently, junctionless (JL) MOSFET has been developed to cope with the above-mentioned issue [1-34][1-35][1-36]. Compared to conventional MOSFET, JL-MOSFET has no source or drain junctions because the doping type and doping concentration are the same in the channel, source and drain regions. Since the constraints in the formation of ultra-shallow junction in conventional CMOSFETs can be avoided, fabrication process of JL-MOSFET is greatly simplified.

The most important and critical part of this scheme is the conditions of the semiconductor layer (or channel layer). The channel layer must be thin enough so it can be fully depleted by the gate to turn off the device. Furthermore, the doping concentration should be high enough to provide low source/drain resistance and sufficient driving current when the device is turned on. According to the previous work in Ref. [1-36], JL-MOSFET with multiple-gated and ultra-thin channel structure could have nearly ideal subthreshold slope (~ 60 mV/dec) and limited leakage current. Moreover, it also shows less degradation in mobility with gate voltage and temperature than regular transistors.

1-5 Motivation

Our laboratory (Advanced Device Technology Lab) has proposed and developed a novel technique to fabricate poly-Si nanowire thin-film-transistor (NWTFT) [1-37]. The main advantage is that it does not require expensive equipment, and the fabrication is simple. The feature size of NWs is determined by the thickness of deposited film as well as adjusting the etching time in the NW channel defining step. Besides, NW channel, source and drain can be formed simultaneously and positioned accurately. The NWs are also free from metal contamination. Finally, our technique has good reproducibility and reliability.

One of the issues for the above NW device is the limited on-current due to the use of poly-Si. As described previously, Ge has many advantages, such as higher carrier mobility, lower melting and crystallization temperatures. These features make Ge a potential and promising channel material. Besides, the unique junctionless structure in JL-MOSFETs is also promising to promote the device characteristics. In this work we exploit the feasibility of using Ge or heavily doped poly-Si as the channel layer of the NW devices.

1-6 Thesis Organization

In this thesis, several types of NWTFTs equipped with different channel material were fabricated and characterized, including poly-Ge NWTFTs, n-channel poly-Si JL-NWFETs and IM-NWFETs. Devices with multiple-gated structure were also demonstrated and discussed in this study.

In the first chapter, we briefly introduce the evolution of nano devices and the Ge material. In Chapter 2, the process flows of poly-Ge NWTFT with different gated structure including side-gate, inverse-T-gate and inverse-T-double-gate (ITDG) are depicted. The electrical characteristics of fabricated devices are also shown and compared. In Chapter 3, junctionless (JL) poly-Si NWFET and inversion mode (IM) poly-Si NWFET were fabricated and analyzed. Finally, we summarize important conclusions achieved in this thesis, and some suggested future works in Chapter 4.

Table Captions

Table 1-I. Properties of Si and Ge [1-38].

Electrical property	Si	Ge
Mobility(bulk)		
Electron	1500 cm^2/V-s	3900 cm^2/V-s
Hole	450 cm^2/V-s	1900 cm^2/V-s
Band Gap(bulk)		
Direct		~0.8 eV
Indirect	~1.1 eV	~0.66 eV
Melting point *Tm* (°C)	1412°C	937°C

Chapter 2

Poly - Ge NWTFTs

2-1 Samples Preparation

In this section, we will firstly describe the ultrahigh-vacuum (UHV) Ge sputtering system, and then discuss the material properties of the sputtered Ge. For the purpose of fabricating Ge-NWTFT, some approaches for alleviating the difficulties met in device fabrication will also be described.

Sputter deposition is a physical vapor deposition method where thin films are deposited on substrates via vaporizing a material target. In general, sputter deposition takes place in a vacuum. In our fabrication, the base pressure in the UHV Ge sputtering system is 5×10^{-8} torr. Such a low base pressure would reduce the contamination level of impurities (e.g. O) in the deposited films. If the substrate has a non-planar topography, however, conformity of the deposited film is a concern. Since the sputter materials typically have a high sticking coefficient and approach the substrate with directions almost perpendicular to the substrate surface, protruding features block the sputter material from being deposited in some areas [2-1]. This phenomenon is called "shadowing", which may lead to poor step coverage (Fig. 2-1) [2-2].

According to our NWTFT fabrication method [2-3], the NW channel is supposed to be formed by side-wall spacer etching technique. This technique requires conformal thin-film deposition and decent step coverage to achieve NW spacer formation. In this thesis, however, the Ge channel film was deposited by UHV sputtering system, so the poor step coverage of Ge film could be a major issue for device fabrication and needs to be resolved.

In this experiment, we examined the uniformity of the Ge thin film. In order to form the spacer as NW channel in the etching step, a sufficiently thick α-Ge thin film must be deposited at the sidewalls of the side-gate. The cross-sectional scanning electron microscopic (SEM) images for samples with nominally deposited film thickness of 100 nm are shown in Fig. 2-2 (Fig. 2-2(a) for single side-gated structure and Fig. 2-2(b) for inverse-T-gated structure). It can be seen that the film thickness reduces as it crosses a step, indicating that the deposited thin film has a poor step coverage (marked by red circle). To address this issue, we tried to change the thickness of α-Ge deposition from 100 nm to 150 nm. In Fig. 2-3, we can see a better step coverage is resulted with such thicker film. Base on this result, thickness of 150 nm was chosen for α-Ge deposition in this study.

Moreover, in order to transform α-Ge into polycrystalline state for better crystal property, solid-phase crystallization (SPC) is employed as the recrystallization method. In the previous works [2-4], the sample preparation and recrystallization temperature of SPC process for poly-Ge were investigated and discussed. The transmission electron microscopy (TEM) image and diffraction pattern of the poly-Ge film annealed at 500 ^{o}C for 1 hour are shown in Fig. 2-4 and Fig. 2-5, respectively. From the TEM analysis, the grain size is about 5 nm, while the diffraction pattern shows that the Ge film has been transformed into poly-Ge, which is in agreement with the XRD profile. For this reason, in the device fabrication described below, the annealed condition was set to be 500 ^{o}C for 1 hour.

2-2 Device Structure, Fabrication and Measurement

2-2.1 Process Flow of Single Side-Gated and Inverse-T-Gated Poly-Ge NWTFTs

Top view of single side-gated device and inverse-T-gated device are given in Fig. 2-6. Figs. 2-7(a) to (f) show the stereograph and process flow of the proposed inverse-T-gated device. First, silicon wafers were capped with a 200 nm-thick thermal oxide layer. After depositing a 150 nm-thick *in situ* doped n^+ poly-Si (Fig. 2-7(a)), the inverse-T-gate was formed by applying twice the standard I-line lithography and dry etching steps (Figs. 2-7(b) and (c)). Then, 30 nm tetraethyl orthosilicate oxide (TEOS-SiO_2) was deposited by low-pressure chemical vapor deposition (LPCVD) as the gate dielectric. After standard cleaning, a 150 nm-thick α-Ge film was deposited on the SiO_2 through the UHV Ge sputtering system (Fig. 2-7(d)). Subsequently, source/drain (S/D) implant was performed by BF_2^+ implantation with a dose of 5×10^{15} cm^{-2} at 40 keV (Fig. 2-7(e)). After forming S/D photoresist patterns through I-line stepper, a reactive plasma etching step was employed to form the NW channels simultaneously with S/D definition. During the etching process, the two NW channels were precisely positioned abutting the upper stud of the inverted-T-gate in a self-aligned manner (Fig. 2-7(f)). Then, 30 nm PECVD TEOS oxide capping layer was deposited. Next, to transform the α-Ge layer into poly-Ge, a solid-phase crystallization (SPC) treatment was executed at 500 ^{o}C for 1 hour in N_2 ambient. Finally, all devices were then capped with a 220 nm-thick oxide passivation layer. Fabrication of single side-gated devices is basically the same as that of the inverse-T-gated device except the formation of the side-gate which employed only one time lithographic step for patterning.

2-2.2 Process Flow of Independent Double-Gated Poly-Ge NWTFTs

Top view of independent double-gated poly-Ge NWTFT is given in Fig. 2-8. The process flow and fabricated structure are similar to that described in 2-2.1. The only difference is the formation of an additional top gate after definition of the S/D and NW channels. The top gate was made up of a 300 nm-thick aluminum (Al) which was deposited by electron-beam evaporation system after the deposition of PECVD top gate oxide on the NW channels. Then Al top gate was defined by I-line lithography and patterned by dry etching (Fig. 2-9). Finally, a 220-nm-thick passivation layer was deposited.

2-2.3 Measurement Setup

The transfer characteristics and output characteristics of the fabricated devices in this thesis were measured by a Keithley 4200 semiconductor characterization system with Keithley Interactive Test Environment (KITE) software and HP4156 semiconductor parameter analyzer and Interactive Characterization Software (ICS) program. In all measurements, the temperature was controlled at a stable value by temperature regulated hot-chuck.

According to the I_D-V_G curve measured at V_D = -0.5 V, threshold voltage (V_{th}) and subthreshold swing (S.S.) could be extracted. The V_{th} is obtained by the constant current method and defined as the gate voltage (V_G) needed to achieve a specific drain current (I_D). The expression is as follows,

$$V_{th} = V_G @ I_D = \frac{W}{L} \times 10nA \qquad \text{(Eq. 2-1)}$$

where W and L are the channel width and length, respectively. S.S. is calculated from the subthreshold current in the weak inversion region, given by,

$$S.S. = \frac{\partial V_G}{\partial \left(\log I_D \right)} \qquad \text{(Eq. 2-2)}$$

Moreover, for the ON/OFF current ratio (I_{ON}/I_{OFF}), I_{ON} and I_{OFF} are determined from the I_D-V_G curves, where I_{ON} is chosen as the maximal I_D and I_{OFF} is the minimal one.

2-3 Electrical Characteristics of Poly-Ge NWTFTs

The cross-sectional SEM image of a poly-Ge NWTFT is shown in Fig. 2-10. The cross-sectional dimension of the poly-Ge NW is around 45 nm.

The transfer characteristics of poly-Ge NWTFTs with single side-gated and inverse-T-gated structure are given in Fig. 2-11. Channel length (L) = 0.4 μm in Fig. 2-11(a) and 0.7 μm in Fig. 2-11(b). Both the fabricated devices show decent transistor characteristics with ~2.5×10^2 ON/OFF current ratio for single side-gated device, and ~10^4 for inverse-T-gated split. In Fig. 2-11(a), the S.S. of single side-gated device is 1.36 V/dec, and for inverse-T-gated device it is 0.64 V/dec. The V_{th} of single side-gated device is -2.09 V, and for inverse-T-gated device it is -1.56 V. Apparently, the inverse-T-gated NW device exhibits better performance in terms of higher ON current and steeper subthreshold slope. This is mainly attributed to the fact that the inverse-T-gated NW device has larger gated area and thus possesses better gate control capability as compared to the single side-gated device. The output characteristics of single side-gated and inverse-T-gated poly-Ge NWTFTs are also shown and compared in Fig. 2-12. The results again show that the inverse-T-gated poly-Ge NWTFT exhibits better device performance.

Furthermore, the transfer characteristics of the poly-Ge NWTFT and the poly-Ge planar TFT are compared in Fig. 2-13. Channel width and length of two types of devices are shown in the figure. For poly-Ge NWTFT, the S.S. is 0.6 V/dec and the V_{th} is -1.80 V. For poly-Ge planar TFT, the S.S. is 0.9 V/dec and the V_{th} is -4.17 V. Obviously, the NW device shows better S.S., smaller V_{th} and reduced I_{min} in spite of the much shorter channel length (0.4 μm) over that of the planar one (10 μm).

2-4 Electrical Characteristics of Independent Double-gated Poly-Ge NWTFTs

2-4.1 Fundamental Electrical Characteristics

In Sec. 2-3, the devices characterized are with only one gate electrode that the gate bias can be applied to for device characterization. In this section, poly-Ge NWTFTs with independent double-gated (DG) configuration are characterized and compared. Each gate can be biased independently to manipulate the device. Such design allows more freedoms for device operation [2-5]. Three operation modes specified in Table 2-I are investigated, including two single-gated (i.e., SG-1 and

SG-2) and one double-gated (DG) modes. The SG modes, namely, the sweeping gate voltage is applied to one of the two gates (the driving gate), while the other gate is grounded during the measurement. For the DG mode, both the inverse-T gate and top gate electrodes are connected together and applied simultaneously with the sweeping voltage.

Typical transfer characteristics under SG and DG modes are shown in Fig. 2-14. Due to the stronger gate controllability over the NW channels, the DG mode exhibits significantly better performance as compared to the two SG modes, such as lower V_{th}, steeper S.S. and higher I_{ON}. Moreover, due to larger gated area, operating under SG-1 mode shows better performance than SG-2 mode. For SG modes, the remaining gate is grounded throughout the measurements, so the three curves have a common intersection point while the gate voltage is zero. Some representative electrical parameters are summarized in Table 2-II.

Output characteristics are shown in Fig. 2-15 and Fig. 2-16. In Fig. 2-15, devices are operated under DG-mode. In Figs. 2-16(a) and (b), the drain voltages are -6 V and -9 V respectively. The performance of DG mode clearly outperforms the others.

2-4.2 Threshold Voltage Modulation

In this measurement, the sweeping voltage is applied to the inverse-T-gate, while a fixed voltage varying from +2 V to -6 V in -2 V step is applied to the top-gate. Fig. 2-17 shows the transfer characteristics of the independent double-gated device with inverse-T-gate as the drive gate and the top gate as the V_{th} control gate. In Fig. 2-17, the ability of the top-gate bias in tuning the V_{th} can be observed. The dashed line represents the transfer characteristics under DG mode of operation. Obviously, the curve is shifted with the sweeping voltage, and the V_{th} could be flexibly controlled by the top-gate bias. The reason for this phenomenon is due to the tiny NW channels, in which the entire channel potential can be easily modulated by either inverse-T-gate or top-gate, leading to conspicuous gate-to-gate coupling effect.

Extracted V_{th} data is depicted in Fig. 2-18. Although the V_{th} from the transfer curves are not linearly modulated by the top-gate, the V_{th} shift clearly reveals this trend. The flexible V_{th} controllability of double-gated TFTs could be used to resolve the stand-by power consumption issues [2-5]. For instance, as the circuit is operated in stand-by mode, the V_{th} can be adjusted to a higher value to suppress the subthreshold leakage current and thus the power consumption. In contrast, an adequate driving current can be obtained in active mode by adjusting V_{th} to a lower value.

2-5 Brief Summary

We proposed a new field-effect transistor structure which utilizes poly-Ge nanowire (NW) as the channels. In comparison with single side-gated structure, inverse-T-gated achieved better performance in terms of higher ON/OFF current ratio and steeper subthreshold swing, owing to the fact that the inverse-T-gated NW device possesses better gate control capability as compared to the single side-gated device.

Besides, poly-Ge NWTFTs with independent double-gated (DG) configuration are characterized and compared. Each gate can be biased independently to manipulate the device.

In fact, the grain size of poly-Ge recrystallized by SPC method in our device is very small (< 5 nm). This means that many defects are contained in the channel layer or near the interface between poly-Ge channel and gate oxide, leading to performance degradation. Enhancement in film crystallinity is essential for boosting the device characteristics.

Table Captions

Table 2-I. Definition of three operation modes.

	DG mode	SG-1 mode	SG-2 mode
Inverse-T Gate	Driving Gate	Driving Gate	Grounded
Top Gate	Driving Gate	Grounded	Driving Gate

Table 2-II. Comparison of the electrical parameters among various modes of multiple-gated operations.

	SG-1	SG-2	DG
Vth (V)	-3.21	-4.45	-1.12
S.S. (V/dec)	1.34	2.01	0.74
I_{ON} (A)	6.59×10^{-8}	2.65×10^{-8}	1.61×10^{-7}

Chapter 3

Junctionless Poly-Si NWFETs

In this chapter, two types of devices with different channel doping techniques were fabricated, characterized, and compared. One of the two types of devices has no S/D junctions and is called “junctionless (JL)” [1-34]. Unlike conventional transistors which have extremely high doping concentration gradients at junction, the channel and S/D regions of the junctionless transistors are of the same doping type and concentration. On the other hand, we called the other type of devices with undoped channels as the “inversion mode (IM)” devices. Such kind of devices has conventional S/D structure and their on-current is conducted through an inversion channel formed between the source and drain.

The key to successfully operating a JL device is the ability to turn it off with gate bias. This implies the channel must be sufficiently thin and can be fully depleted to shut off the current conduction path in off state. To meet such requirement, we have fabricated gate-all-around (GAA) poly-Si JL NWFETs. IM devices were also fabricated and served as a bench mark for the JL device characterization.

3-1 Device Structure and Fabrication

3-1.1 Process Flow of Junctionless Poly-Si NWFETs

Fig. 3-1 shows the top and cross-sectional views of the JL poly-Si NWFET with GAA structure. It can be seen that the NW channels are surrounded by the gate. Figs. 3.2(a) ~ (h) show the major process steps of the devices. All devices in this work were fabricated on bare silicon substrates capped with a 200 nm-thick wet oxide. First, a 50 nm bottom nitride layer was deposited by low pressure chemical vapor deposition (LPVCD). Then a 30 nm TEOS oxide and a 30 nm dummy-nitride layer (hard mask layer) were deposited sequentially (Fig. 3-2(a)). After a standard I-line lithographic step, dummy nitride/TEOS stack was patterned by anisotropic reactive plasma etching (Fig. 3-2(b)). In this etching step, the etching time was carefully controlled because of low selectivity between nitride and TEOS. Diluted HF (DHF) etching was subsequently employed to laterally etch the TEOS oxide layer with a high selectivity to the top and underlying nitrides (Fig. 3-2(c)). The size of NW channels could be adjusted by controlling the etching time of TEOS oxide layer. Rectangular-shaped cavities were formed at the two sides of the dummy patterns after this step. The main split conditions of this work were the channel doping conditions. For JL poly-Si NWFETs, a 100 nm *in situ* phosphorus doped poly-Si was deposited by LPCVD at 550 ^{o}C under pressure of 600 mtorr using 15 sccm PH_3 and 0.49 slm SiH_4 (Fig. 3-2(d)). Note that, the cavities could be completely refilled due to the good conformability of LPCVD. After forming S/D photoresist patterns through an I-line stepper, an anisotropic reactive plasma etching step was employed to define the NW channels simultaneously with S/D regions (Fig. 3-2(e)). Note, the S/D and the channel were of the same doping type and concentration, so there were no junctions formed in such type of devices. Afterwards, wet etch steps were used to remove the nitride hardmask and dummy TEOS with hot H_3PO_4 and DHF, respectively. In order to form the suspend NW channels hanging between the S/D regions, the bottom nitride was fully wiped out by soaking in hot H_3PO_4 (Fig. 3-2(f)). Next, a 15 nm TEOS oxide layer was deposited as the gate dielectric (Fig. 3-2(g)) and a 150 nm TiN film which was sequentially deposited and patterned to serve as the gate electrode (Fig. 3-2(h)). So far, the GAA structure was accomplished. After depositing a 200 nm passivation oxide layer and opening contact holes, a standard metallization step was performed to complete the device fabrication.

3-1.2 Process Flow of Poly-Si NWFETs with Undoped Channel

All steps are the same as those described in Sec. 3-1.1 until the deposition of the channel material. After forming the cavities underneath the nitride hardmask, a 100 nm undoped amorphous-Si (α-Si) was deposited by LPCVD to serve as the channel material (Fig. 3-3(a)). Afterwards, an annealing step was performed at 600 ^{o}C in N_2 ambient for 24 hours to transform the α-Si into polycrystalline phase. Then by adopting a dry etching step with endpoint detection, the NW channels were formed snugly in the cavities (Fig. 3-3(b)). Subsequently, *in situ* phosphorus doped poly-Si was deposited by LPCVD at 550 $^{\circ}$C and 600 mtorr using 15 sccm PH_3 (Fig. 3-3(c)). Next, S/D photoresist patterns were generated through an I-line stepper, followed by an anisotropic dry etching step to define S/D (Fig. 3-3(d)). It should be noted that the devices whose S/D regions are formed by employing *in situ* doping technique show better performance than those formed by ion-implanted poly-Si [3-1]. Then, similarly, for forming GAA structure, nitride hardmask and dummy TEOS were removed by hot H_3PO_4 and DHF, respectively. Bottom nitride was also removed by hot H_3PO_4. The remaining steps were the same as those described in Sec. 3-1.1 until completion.

3-2 Measurement Setup

The methods for parameter extraction and measurement are basically the same as those presented in Sec. 2-2.3. Here, additional parameters which are not mentioned previously are defined as follows.

The on-current (I_{ON}) in the linear region ($V_G > V_{th}$, $V_G - V_{th} > V_D$) can be expressed as [1-38]

$$I_D = \frac{W}{L} C_{ox} \mu_{FE} (V_G - V_{th} - \frac{1}{2} V_D) V_D \qquad \text{(Eq. 3-1)}$$

where L is the channel length, W is the channel width, μ is the mobility, and C_{ox} is the gate capacitance per unit area.

The field-effect mobility is derived from I_D as function of V_G and described as

$$\mu_{FE} = \frac{L G_m}{W C_{ox} V_D} \qquad \text{(Eq. 3-2)}$$

where G_m is the transconductance extracted by the differentiation of Eq- 3-1 with V_G,

$$G_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D = const.} \qquad \text{(Eq. 3-3)}$$

3-3 Electrical Characteristics of JL and IM Poly-Si NWFETs

3-3.1 Fundamental Electrical Characteristics

For the conventional inversion-mode (IM) transistors, the source/drain (S/D) regions are of the opposite doping type to the channel. For example, n-channel devices are fabricated in the form of n^+-p-n^+ from source to drain (namely, both source and drain are n-type, while the channel region is p-type). In contrast, traditional n-channel accumulation-mode (AM) devices are formed with n^+-n-n^+ structure from source to drain. In the so-called junctionless (JL) transistors, the devices are effectively turned off through depleting the channel by gate electrostatic potential to increase the channel resistance in the off state. On the other hand, while the gate is biased in a positive voltage much larger than the threshold voltage for n-channel JL transistors, the majority carriers much higher than the background carrier concentration are accumulated in the channel, leading to a much lower resistance, thus effectively turning on the device [3-2]. The JL device we proposed belongs to the category of AM devices due to the fact that it is of the form n^+-n^+-n^+. Since traditional AM devices show a strong dependence of channel thickness on threshold voltage (V_{th}) and subthreshold swing (S.S.), AM devices with thick channel film (thicker than 20 nm, typically) suffer from severe short channel effects (SCEs). Based on the paper [3-3], the SCEs are kept at bay by decreasing the thickness of the channel layer. Therefore, in order to obtain better performances of JL devices, the thickness of NW channel should be very thin so that the NW channel can be depleted completely and turned off by the gate bias. The device cross section needs to be smaller as the channel doping concentration gets higher. The transmission electron microscopy (TEM) picture of a fabricated device is given in Fig. 3-4. The dimension of the proposed device is depicted in the figure.

Typical transfer characteristics of JL and IM transistors with different channel lengths at $V_D = 0.1$ V are shown in Figs. 3-5(a) and (b), respectively. The S.S. of the shortest channel length (0.4 μm) in JL device is 177 mV/dec. It illustrates the potential of JL transistors for nano-scale device applications. The ON/OFF current ratio extracted at $V_G = 3$ V and $V_G = -2$ V is larger than 1×10^7 at $V_D = 0.1$ V.

Typically, for the IM device, more and more electrons are attracted to the surface of Si NW in subthreshold region as the gate bias is increased from below to above threshold voltage. In this condition, the electrons in the channel are strongly influenced by the electric field. As the gate voltage further increases, the mobility of carriers in the channel is mainly swayed by surface scattering. Consequently, the on current above threshold doesn't increase linearly and the transconductance becomes worse as gate bias increases for IM devices. In contrast, the ionized donor impurities exist throughout the body of NW channel and form a normally conductive path in the JL devices. When the gate voltage is operated below threshold, depletion of electrons in the channel starts from the channel/oxide interface and the device is turned off by decreasing the gate bias to widen the depletion region. Before the device is completely shut off, the electrons conduct through the middle of the channel.

Fig. 3-6 shows the I_{ON} as a function of channel length for two types of devices. The I_{ON} is significantly improved in the JL devices over its IM counterparts. From the above discussion we can understand that I_{ON} in the JL devices is more uniformly distributed throughout the channel, rather than restricted to near the channel/oxide interface as in the IM devices [3-4]. This well explains the above difference. Table 3-I shows the mean value of I_{ON} of the two types of devices. The I_{ON} improvement ratio becomes larger as the channel length increases. In order to form gate-all-around (GAA) structure, the NW channels are suspended between the S/D regions before gate oxide deposition. Since the NW channel in our structure is very tiny, the NWs are hard to sustain the gravity as the channel lengths are long (say, 2 μm and 5 μm). For these long-channel devices, the central part of the channel collapses and contacts the bottom wafer surface. As a result, the devices become "omega gate" in the center part of the channel (Fig. 3-7(a) and (b)) after the gate oxide and electrode formation. According to the difference in conduction paths between JL and IM transistors mentioned above, the I_{ON} of the IM transistor is more susceptible to this phenomenon than JL device. As a result, ratio of the I_{ON} becomes larger as channel length is increased.

The output characteristics of JL and IM devices are shown in Fig. 3-8. The JL devices exhibit better performance than IM devices in both 0.4 μm- and 5μm-channel-length devices. For 0.4 μm-channel-length devices, the enhancement of saturation current is 255 % at $V_D = 4$ V and $V_G - V_{th} = 4$ V. The value increases to 361 % in the 5 μm-devices.

Fig. 3-9 shows V_{th} of JL and IM devices versus channel length at $V_D = 0.5$ V and 2 V. Obviously, the V_{th} of JL devices is smaller than that of IM devices. Since the JL devices are normally on, that is, they could conduct current at zero V_{GS}, so these devices are suitable for high-performance logic circuits as loads where a constant current load is desired [3-5]. Due to much improved gate controllability with the GAA configuration and ultra-thin channel body, the JL devices shows decent V_{th} roll-off characteristics at $V_D = 0.5$ V.

As the distance between the source and drain diminishes, the channel potential distribution under the gate is influenced by source to drain potential conspicuously. Namely, a high drain-to-source voltage brings about the barrier lowering effect along the conduction path. It leads to the reduction of V_{th}. The definition of drain induced barrier lowing (DIBL) is the reduction in V_{th} when the drain voltage is biased from 0.5 V to 2 V. Fig. 3-10 depicts the DIBL of JL and IM devices as a function of channel length. JL devices are more susceptible to DIBL and bulk punch-through. For JL transistors, since the operation is in accumulation mode, there is a depleted region between gate oxide and the conduction layer when the device is operated in the subthreshold region. This results in the larger effective oxide thickness (EOT) than IM devices, and thus the channel is less easily controlled by the gate field. The threshold voltage of the JL devices operating in saturation is more vulnerable to the drain bias. So the DIBL phenomenon is prominent in the JL devices. However, an anomalous phenomenon is observed that, for IM devices, the DIBL value is negative as the channel length is long. Possible origin for such finding will be addressed later.

The S.S. is defined as the inverse of the slope of the drain current in log scale versus gate voltage in the sub-threshold region. The S.S. of JL and IM transistors with various channel lengths are compared in Fig. 3-11 at $V_D = 0.5$ V and 2 V. It is worth noting that the trend of S.S. gets smaller as the channel length becomes shorter. This is, again, attributed to the deformation of long-channel suspended channels and formation of “omega gate” gate later on, as addressed in the discussion of Fig. 3-7. As the channel length is larger than 1 μm, it is hard to maintain the GAA configuration with the above issue. As a result, the S.S. is degraded.

Gate-induced drain leakage (GIDL) current is considered as a major drain leakage in off-state of the NW transistors, as has been identified in one previous study

[3-6]. The GIDL current is through the tunneling mechanism caused by band-to-band tunneling or trap-assisted band-to-band tunneling and occurs in the deep-depleted drain region overlapping with the gate. Typical drain currents and gate currents as a function of gate bias are plotted in Figs. 3-12(a) and (b) for JL and IM devices, respectively. In the figures, because the drain current is obviously lager than the gate current in the off-state regime, it could be ruled out that the leakage current is the electron tunneling current from the gate. Moreover, it can be seen that the JL device has much reduced GIDL current than the IM one.

3-3.2 Transconductance

The dependence of Gm on overdrive gate voltage for JL and IM transistors are recorded in Fig. 3-13 for devices with channel length of 0.4 μm and 5 μm. As expected, the transconductance of JL transistors is larger than that of the IM transistors, because the conduction of JL transistors is through the whole channel film rather than the channel surface. In Fig. 3-13 (a) for devices with L = 0.4 μm, the peak Gm value is 3.64×10^{-6} A/V in the JL device and 7.37×10^{-7} A/V in the IM device. It can be calculated that the value of JL device is 4.94 times larger than the IM counterpart. In Fig. 3-13 (b) for devices with L = 5 μm, the peak Gm value is 4.37×10^{-7} A/V in the JL device, 4.65 times larger than the value of 9.38×10^{-8} A/V in IM counterpart. Fig.3-14 shows the drain currents at $V_D = 0.5$ V and 2 V as a function of gate voltage while the channel length is 1μm. The Gm values extracted at $V_D = 0.5$ V are also plotted in the figure. Again, it can be found that the JL device has better performance of Gm. Fig.3-15 re-plots the data of Fig. 3-14 by expressing them as a function of gate over drive. It is interesting to see that the Gm is smaller for JL device in the subthreshold region, similar to that observed in Fig. 3-13(b) for device with L of 5 μm. As the gate overdrive is small, it is suspected that the conduction is mainly through the central portion of the doped channel film while a depletion region close to the channel surface exists for the JL device. In other words, the effective EOT of the JL device is larger than that of the IM one, explaining its smaller Gm in this region. However, as the gate voltage increases further, the width of depletion region gradually shrinks and eventually disappears. Then the device becomes accumulation mode and a sheet of electron layer would accumulate near the channel interface. As a result, the Gm rises quickly with increasing gate overdrive and far exceeds the peak Gm of the IM one. It should be noted that such phenomenon is not found in Fig. 3-13(a) for the devices with L of 0.4 μm. This might be related to the applied drain bias which exerts a non-negligible lateral electric field which would drift the electrons in the channel and increase the Gm of the JL device.

The field-effect mobility (peak value) of the two types of devices versus channel length are extracted from the Gm results and shown in Fig. 3-16. The current flowing in the channel surface for the IM device is more susceptible to scattering than the body current which conducts through the center of the channel, resulting in a degraded mobility in the IM devices [3-7]. However, it should also be noted that the JL devices' mobility values shown in the figure are actually overestimated since the Gm formula (Eq. 3-2) does not take the abundance of carriers contained in the heavily doped channel into account.

3-4 Series Resistance of JL and IM Poly-Si NWFETs

The parasitic series resistance of MOSFETs is another important issue as devices' scaling down continues. The R_{SD} is the parasitic resistance in series with the channel resistance and its major components include the S/D contact resistance, the S/D sheet resistance, and the spreading resistance at the transition points at junctions [3-8]. Some technological limitations such as the non-abrupt p-n junction profile of the source and drain are the factor of R_{SD} [3-9]. The spreading resistance caused by the lateral doping gradient is a key constituent contributing to the total parasitic resistance. For this reason, the technique of controlling the doping profile and specific contact resistance must be employed to overcome the parasitic limitation in the future [3-10]. In this section, the series resistances of JL and IM devices are analyzed. The total resistances were measured and the channel resistances are calculated.

The I-V characteristics of a NWFET operating in the linear region can be expressed as

$$I_{DS} = \mu_S C_{ox} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{th} - 0.5V_{DS}) V_{DS} \quad \text{(Eq. 3-4)}$$

From this expression, we can extract the total resistance, R_{tot}, with the following form:

$$R_{tot} = \frac{V_{DS}}{I_{DS}} = \frac{L_{eff}}{\mu_S C_{ox} W_{eff} (V_{GS} - V_T - 0.5V_{DS})} \quad \text{(Eq. 3-5)}$$

where V_{DS} is the drain bias and I_{DS} is the drain current. The total resistance can also be represented as

$$R_{tot} = \frac{V_{DS}}{I_{DS}} = L \times R_{ch} + R_{SD} \quad \text{(Eq. 3-6)}$$

where R_{ch} and R_{SD} are the intrinsic channel resistance per unit length (Ω/μm) and the S/D series resistance (Ω), respectively.

Fig. 3-17 shows and compares the measured total resistance of JL and IM devices as a function of physical gate length for different V_{DS} ranging from 0.1 to 0.3 V. The data were measured at $V_G – V_{th}$ of 4 V. The results indicate that the applied V_{DS} has negligible effect on the extracted resistance. From Eq. 3-6, the extrapolations of the curves to $L = 0$ yield the values of R_{SD}. The R_{SD} is reduced from 11.78 kΩ for IM devices to 0.71 kΩ for JL ones. This is a clear indication about the effect of eliminating the source/drain junctions in the JL devices. On the other hand, information of R_{ch} can be obtained from the slopes of the curves depicted in Fig. 3-17. Obviously, the extracted R_{ch} of the JL device is 108.9 kΩ/μm which is significantly smaller than 402.8 kΩ/μm extracted from the IM ones at $V_D = 0.2$ V.

3-5 Observation of Anomalously Low Subthreshold Swing

The subthreshold swing (S.S.) is defined as the inverse of the slope of the log(I_D)-vs.-V_G curve in the subthreshold region. It has a theoretical minimum value of S.S. = (k_BT/q) ln (10) which is 60 mV/dec at T = 300 K. To break this limit, at least two kinds of devices have been proposed and investigated. One is the tunneling FET which utilizes the band-to-band tunneling [3-11] to reduce the S.S.. However, it has a drawback that the on current is constrained. Another type of device is the IMOS which utilizes impact ionization to abruptly increase the drain current [3-12]. Nonetheless, with this mechanism, a high operating voltage is required. In these methods, the electronic transport is no longer purely thermionic.

In this thesis, we unintentionally found that the S.S. of GAA NWFETs with undoped channel can be lower than 60 mV/dec as specific measurement conditions were applied. One example is given in Fig. 3-18, in which the transfer characteristics of a device with L of 5 μm measured with various drain voltages are illustrated and compared. As can be seen in the figure, an increase in drain voltage tends to increase V_{th} and decrease the S.S.. The V_{th} and S.S. as the function of drain voltage are plotted in Fig. 3-19. It is interesting to see that the S.S. can be smaller than 60 mV/dec and the values are 31 and 53 mV/dec as V_D = 2.5 and 3 V, respectively. Here, we examine Fig. 3-18 again. The significant GIDL current is observed at the beginning of the sweeping at V_G = -1 V and increases with increasing drain voltage. Obviously the magnitude of the initial GIDL plays an important role in affecting the S.S.. It is well known that [3-13], in the poly-Si NW, GIDL is dominated by the trap-assisted band-to-band tunneling current and strongly related to the strength of electric field in the drain junction which is mainly dependent on V_{GD}. As V_D increases, more holes are generated and flow into the channel. During V_G sweeping, it is postulated that portion of the generated holes at the beginning would store in the channel and affect the operation, leading to the anomalously low S.S. Work is still in progress to identify the exact origin of this phenomenon.

Table Captions

Table 3-I. The mean values of I_{on} of JL and IM NWFETs and the current ratio. The data were extracted at $V_G - V_{th} = 4$ V and $V_D = 0.5$ V.

	0.4μm	**0.7μm**	**1μm**	**2μm**	**5μm**
I_{ON}(JL)	6.24×10^{-6}	4.81×10^{-6}	3.14×10^{-6}	2.38×10^{-6}	7.57×10^{-7}
I_{ON}(IM)	4.04×10^{-6}	2.96×10^{-6}	1.93×10^{-6}	9.51×10^{-7}	2.10×10^{-7}
I_{ON}(JL)/I_{ON}(IM)	1.54	1.63	1.63	2.50	3.60

Unit : Ampere (A)

Chapter 4

Conclusion and Future Work

4-1 Conclusion

In Chapter 2, we proposed new field-effect transistor structures which utilize poly-Ge nanowire (NW) as the channels. In this work, the NW channel definition was done with a novel sidewall spacer etching technique. Solid phase crystallization (SPC) was utilized to transform amorphous Ge (α-Ge) to poly-Ge. In comparison with single side-gated structure, the inverse-T-gated one achieved better performance in terms of higher ON/OFF current ratio and steeper subthreshold swing (S.S.).

Independent doubled-gated (DG) poly-Ge NWTFTs were fabricated and characterized. Each gate can be biased independently to manipulate the device. Such design allows more freedoms for device operation. The device which is operated under DG mode exhibits significantly better performance as compared to the two single-gated (SG) modes, such as lower V_{th}, steeper S.S. and higher I_{ON}.

In Chapter 3, poly-Si JL-NWFET and poly-Si IM-NWFET with gate-all-around (GAA) structure were fabricated and investigated. For the JL device, it shows superior ON/OFF current ratio, and better on-state performance. The series resistance of JL device is lower than IM device. It is attributed to the heavily doped S/D and the channel of JL device which were formed simultaneously with *in situ* doped poly-Si deposition. Elimination of the junctions between S/D and channel indeed helps reduce the series resistance.

Besides, poly-Si IM-NWFET shows an interesting property. Specifically, the S.S. of IM device with 5 μm channel length can be lower than 60 mV/dec if the operation conditions are appropriately chosen, and decent performance is observed in on state current. It is postulated to be related to the generation of the electron-hole pairs near the drain side as GIDL mechanism takes place. Nonetheless, more efforts are still needed to verify the exact cause of this phenomenon.

4-2 Future Work

For poly-Ge NWTFT, the recrystallization method we adopted was solid-phase crystallization (SPC). However, in our experiment, the grain size formed by SPC is too small (~ 5 nm). As a result, the merits of Ge are constrained by grain boundaries and defects. To address this issue, alternative recrystallization methods could be attempted, such as metal-induced crystallization (MIC), metal-induced lateral crystallization (MILC) and excimer laser annealing (ELA). The performance of poly-Ge devices is expected to be improved while the grain size is enlarged.

In fact, the etching time of α-Ge is hard to control. The dimensions of poly-Ge NW channel are not small enough, since the leakage of device is found to be large. Besides, poor quality of TEOS oxide is also a reason responsible for worse performance. Based on those reasons, refinement in etching step is a way to improve the performance. In addition, the gate dielectric could be replaced by high-*k* dielectric to reduce the equivalent oxide thickness and film properties.

For JL poly-Si NWFETs, the size of poly-Si NW channel can be controlled by tuning the etching time in the fabrication process, the characteristics of devices with various NW channel size is a topic worth being studied in the future. Besides, the material of gate dielectric can also be changed to high-*k* dielectrics to enhance gate controllability. Finally, the p-type JL poly-Si NWFET could be fabricated and compared with n-type counterpart.

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Chapter 1 Introduction

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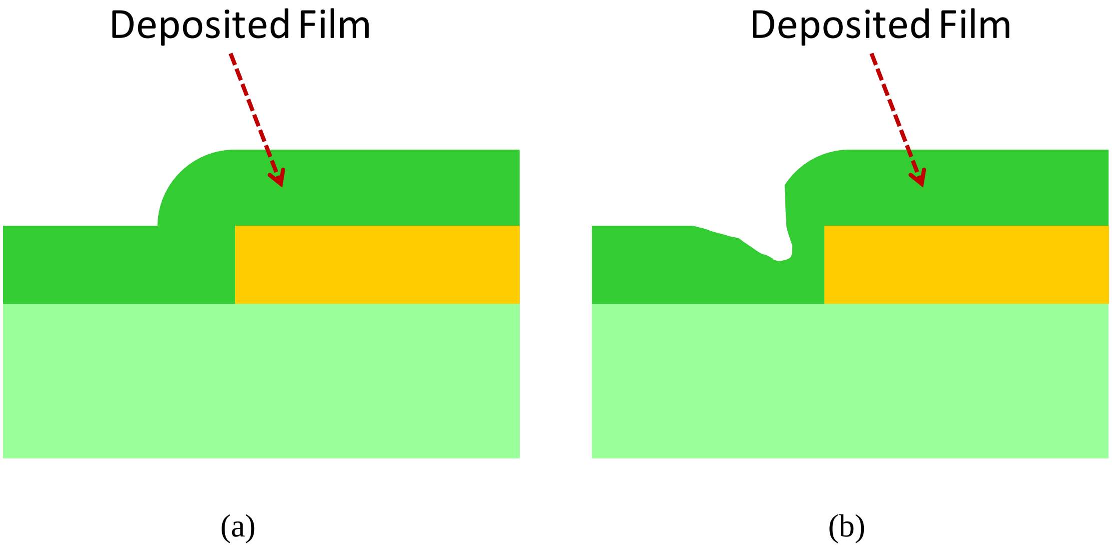
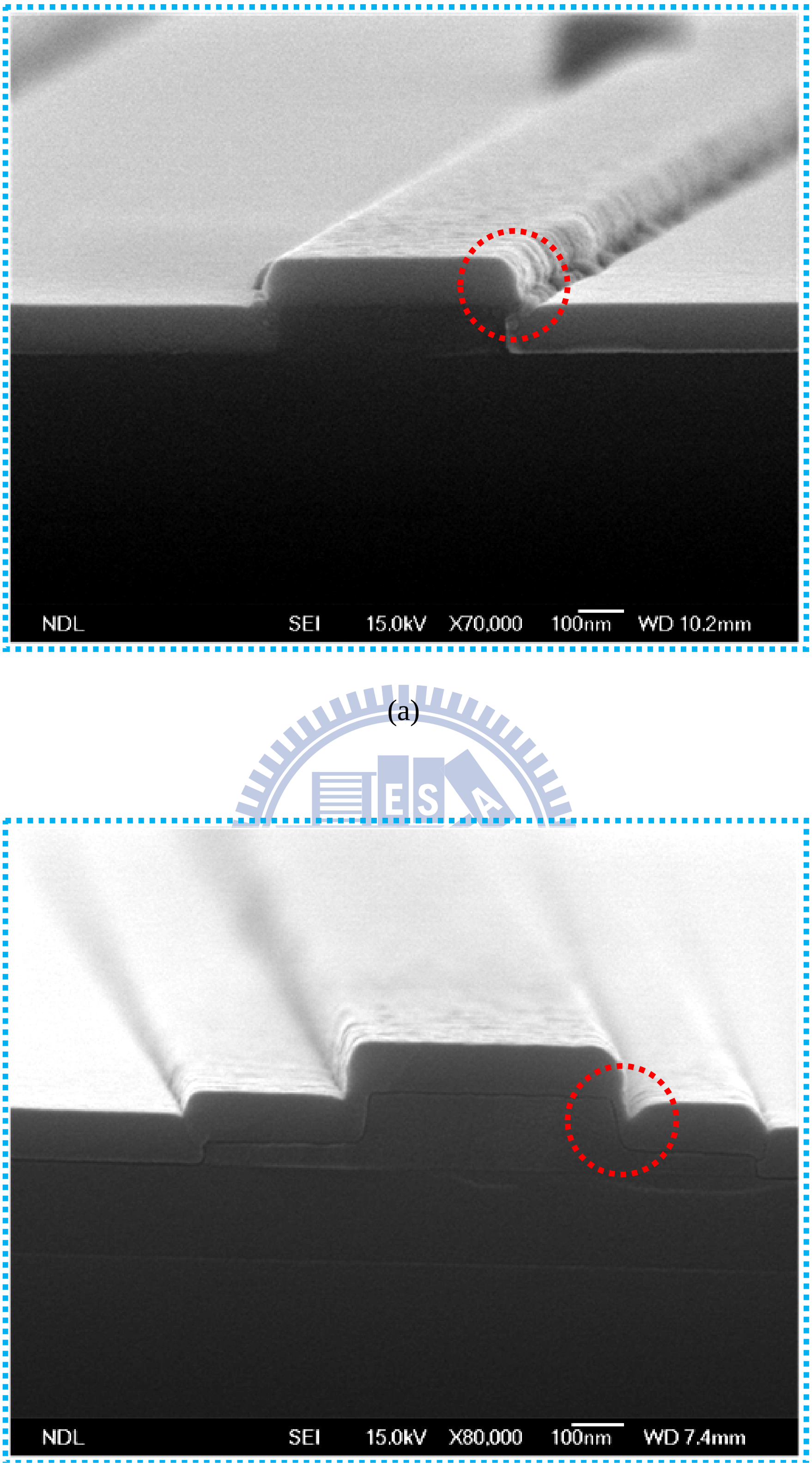


Fig. 2-1 Step coverage of deposited film over non-planar topography with (a) conformal and (b) non-conformal deposition.



(a)

(b)

Fig. 2-2 SEM images of 100 nm-thickness α-Ge thin films deposited on (a) the single side-gated structure and (b) inverse-T-gated structure.

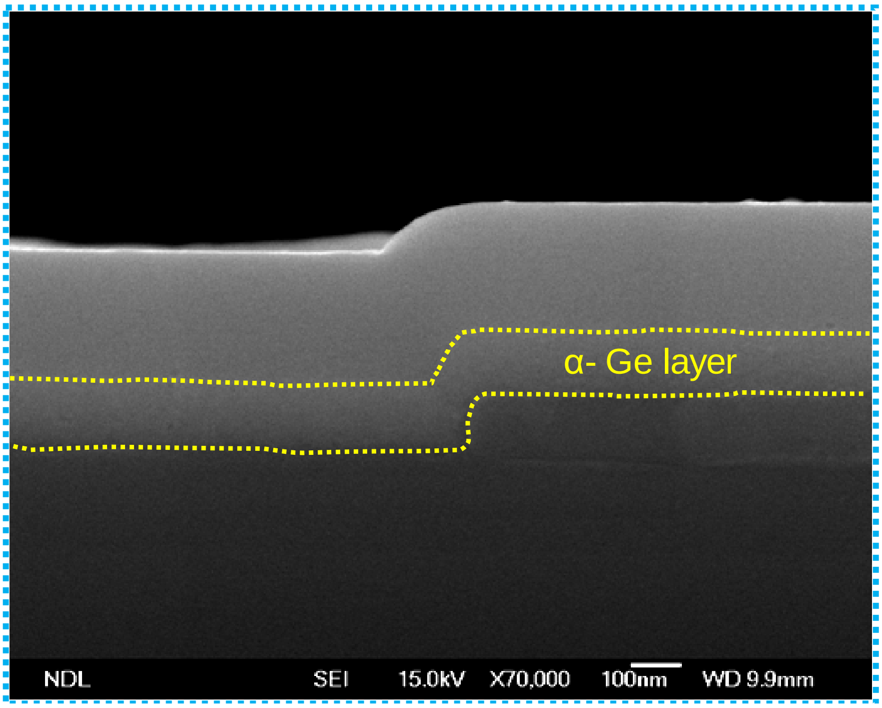


Fig. 2-3 SEM image of a 150 nm-thick α-Ge thin film deposited on the single side-gated structure.

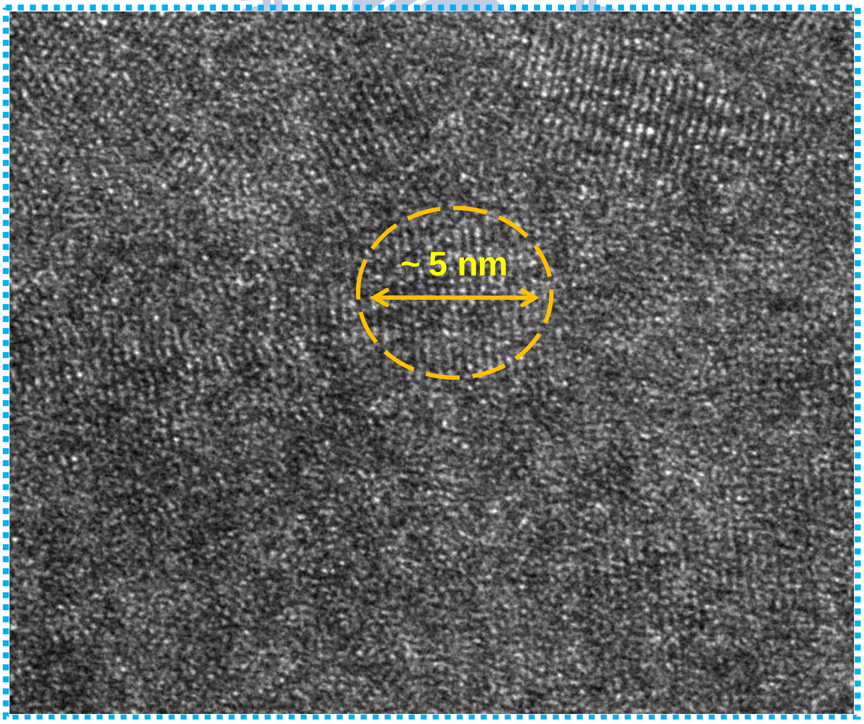


Fig. 2-4 TEM cross-sectional view of poly-Ge film annealed at 500 ^{o}C for 1 hour. The circled area in the image indicates the region of a grain.

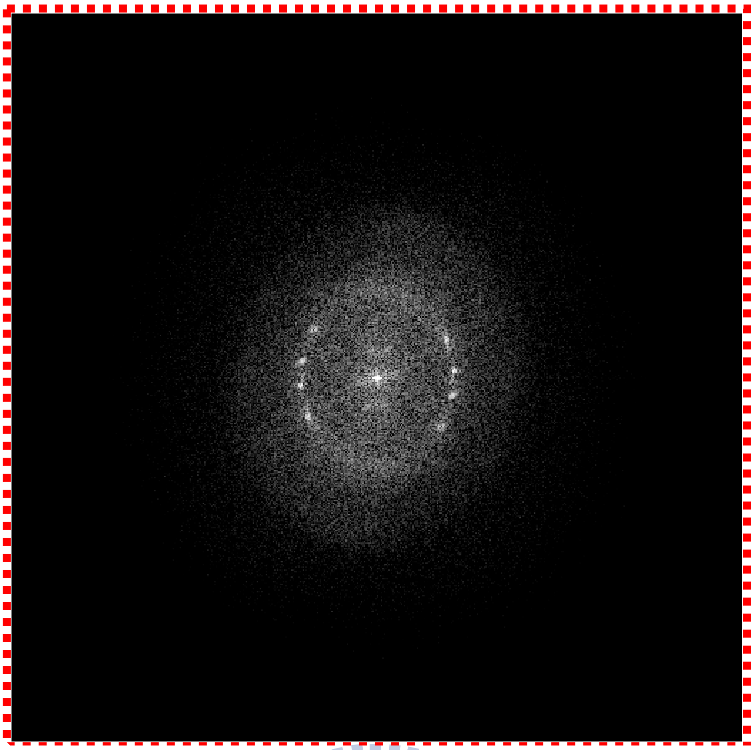
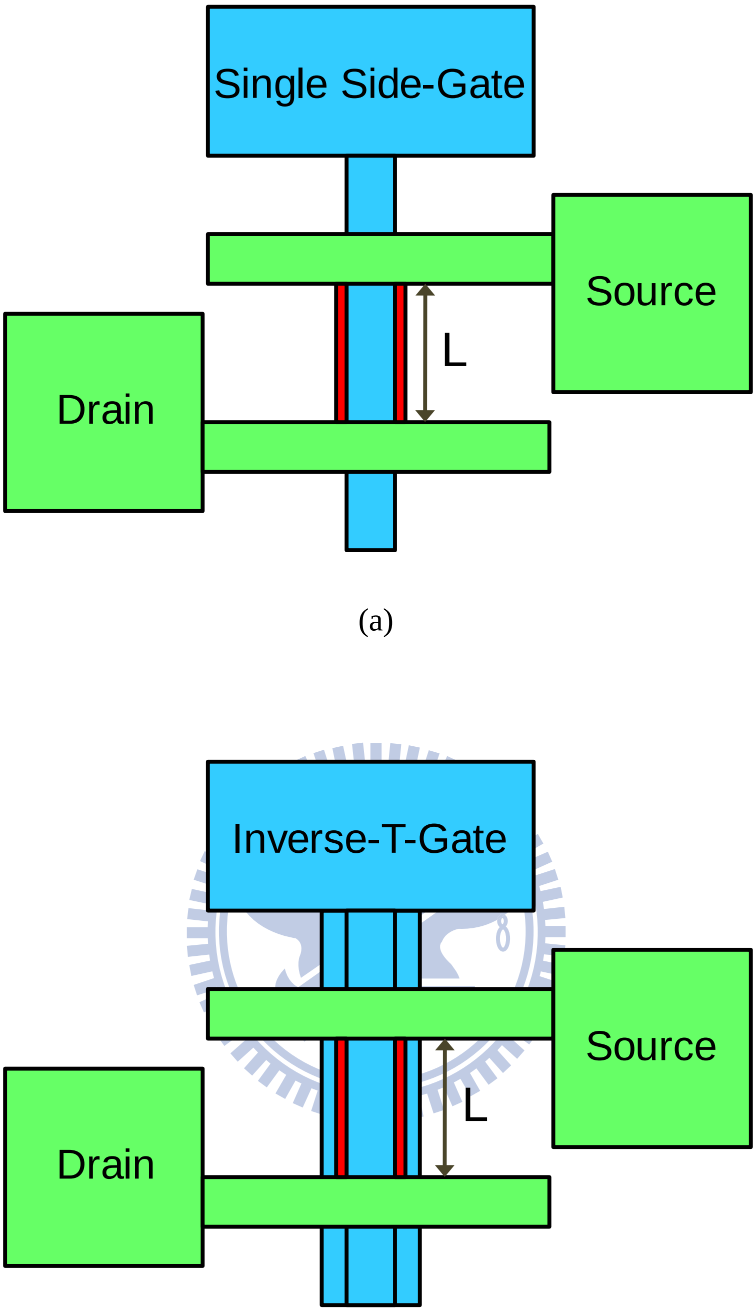


Fig. 2-5 Diffraction pattern of the poly-Ge film.



(a)

(b)

Fig. 2-6 Top views of (a) single side-gated (b) inverse-T-gated poly-Ge NWTFT.

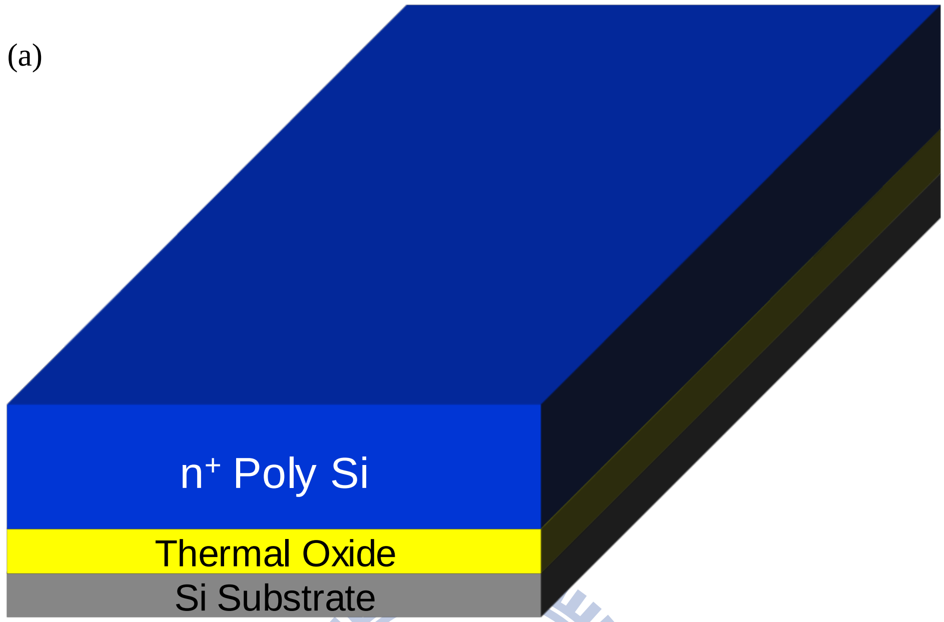


Fig. 2-7 (a) Deposition of *in situ* doped n^+ poly-Si on oxide-capped Si substrate.

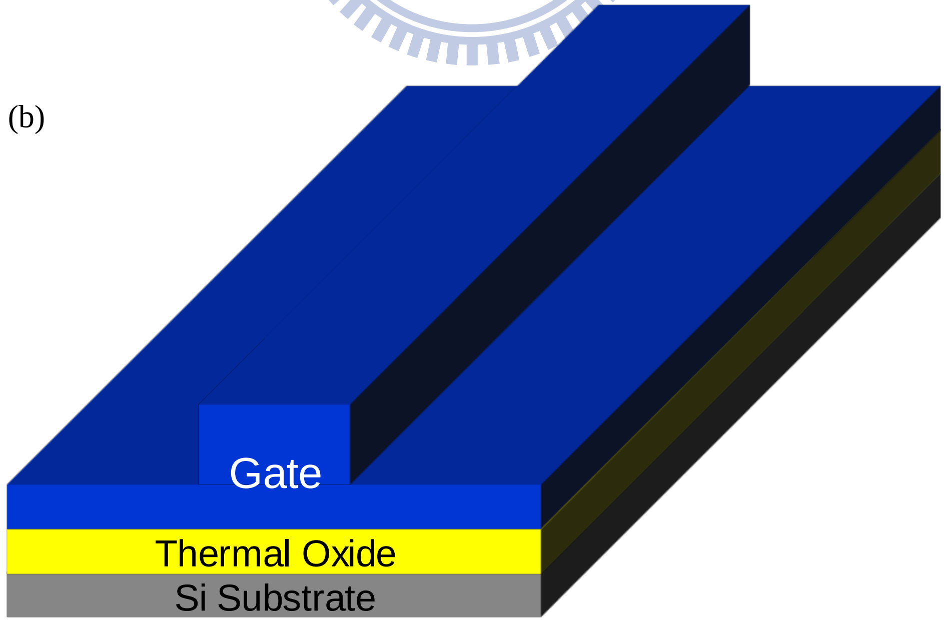


Fig. 2-7 (b) First gate definition by standard I-line lithography and subsequent dry etching steps.

(c)

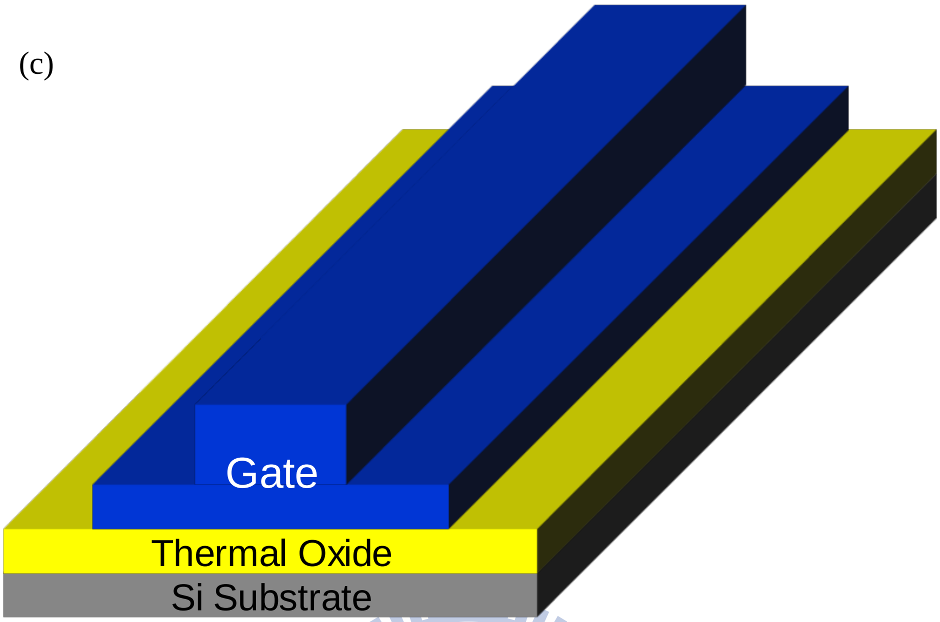


Fig. 2-7 (c) Second gate definition by standard I-line lithography and subsequent dry etching steps to form the inverse-T-gate.

(d)

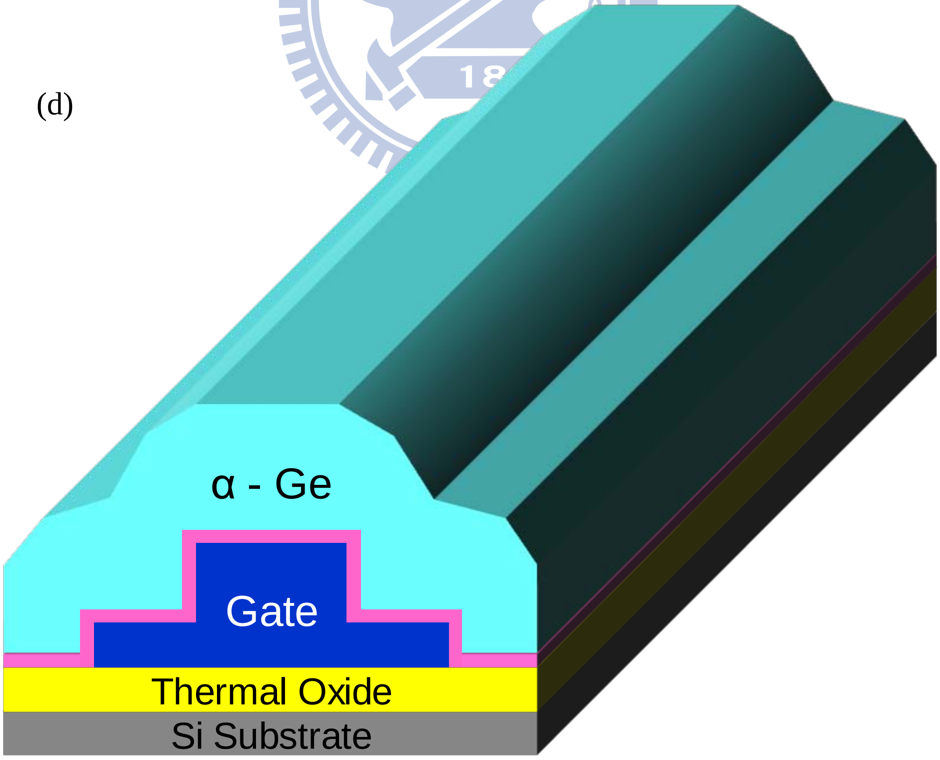


Fig. 2-7 (d) Deposition of gate oxide and α-Ge layers.

(e)

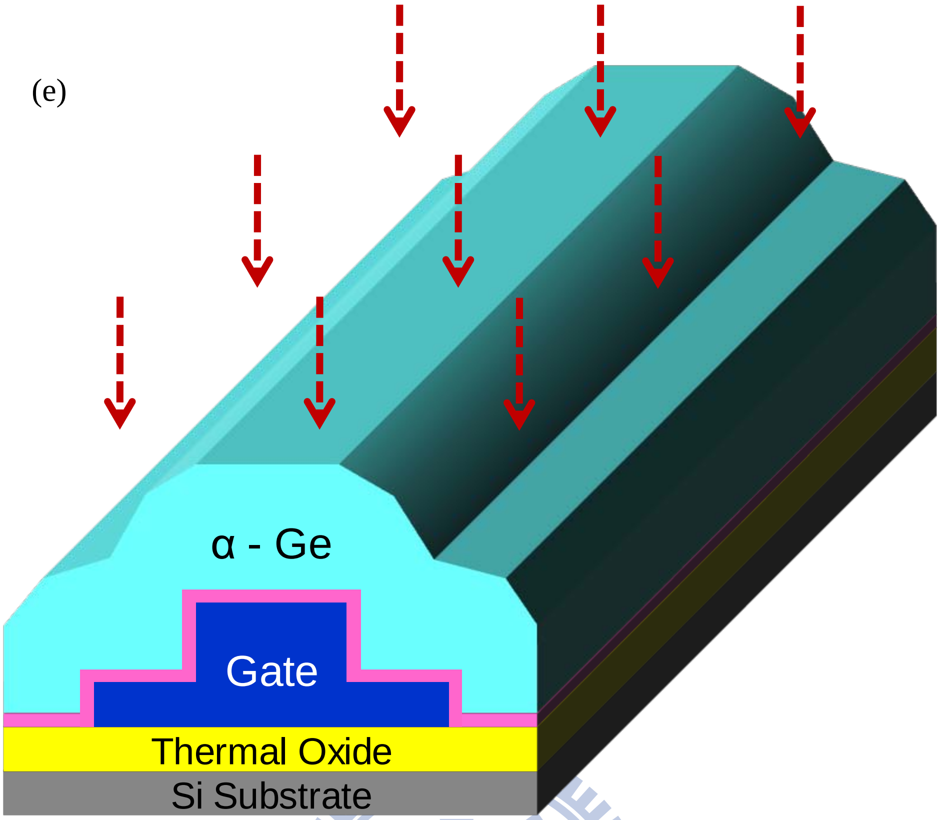


Fig. 2-7 (e) Source/drain ion implantation.

(f)

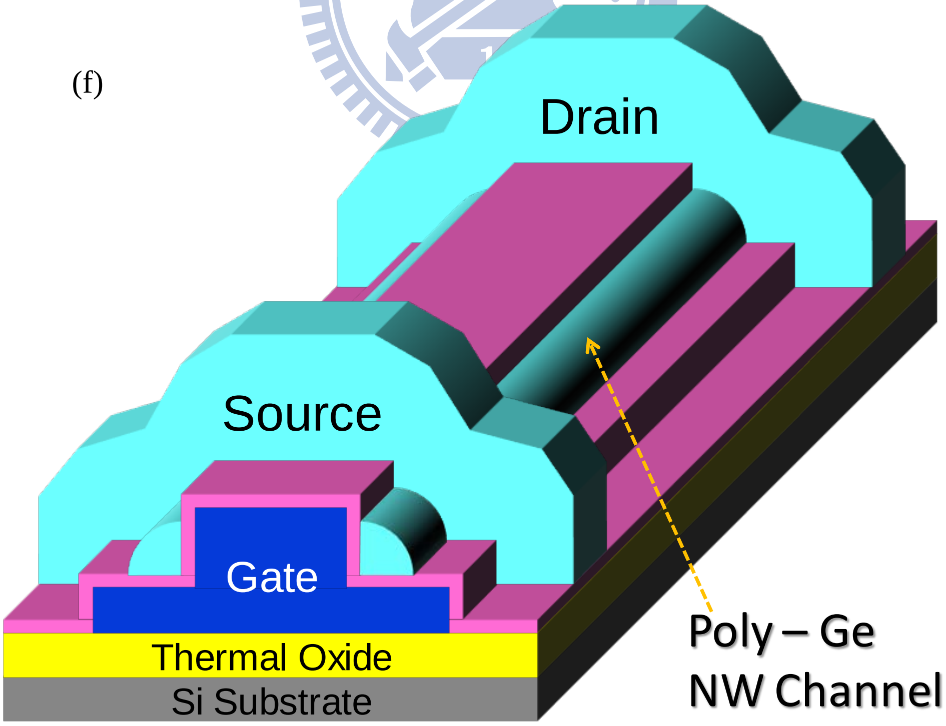


Fig. 2-7 (f) Definition of source/drain and formation of NW channel.

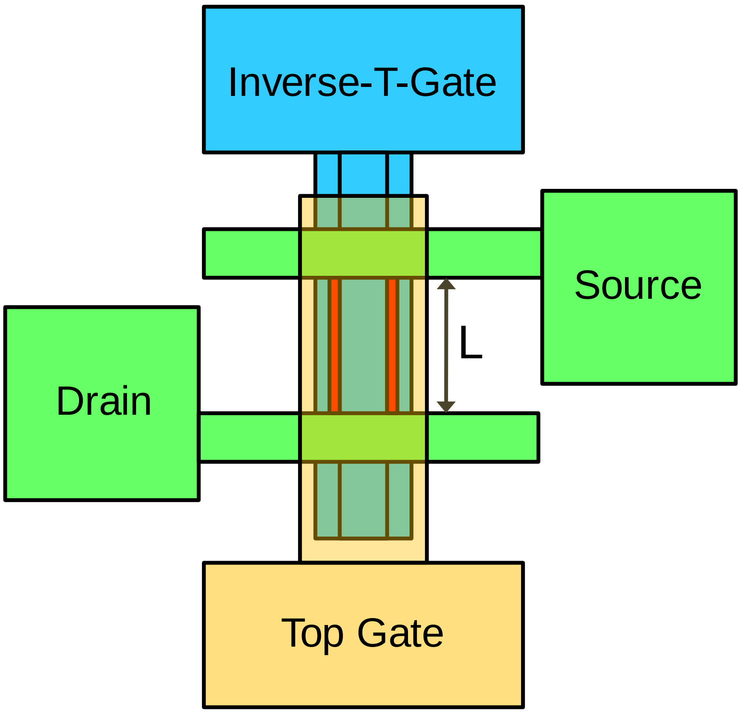


Fig. 2-8 Top view of independent double-gated poly-Ge NWTFT.

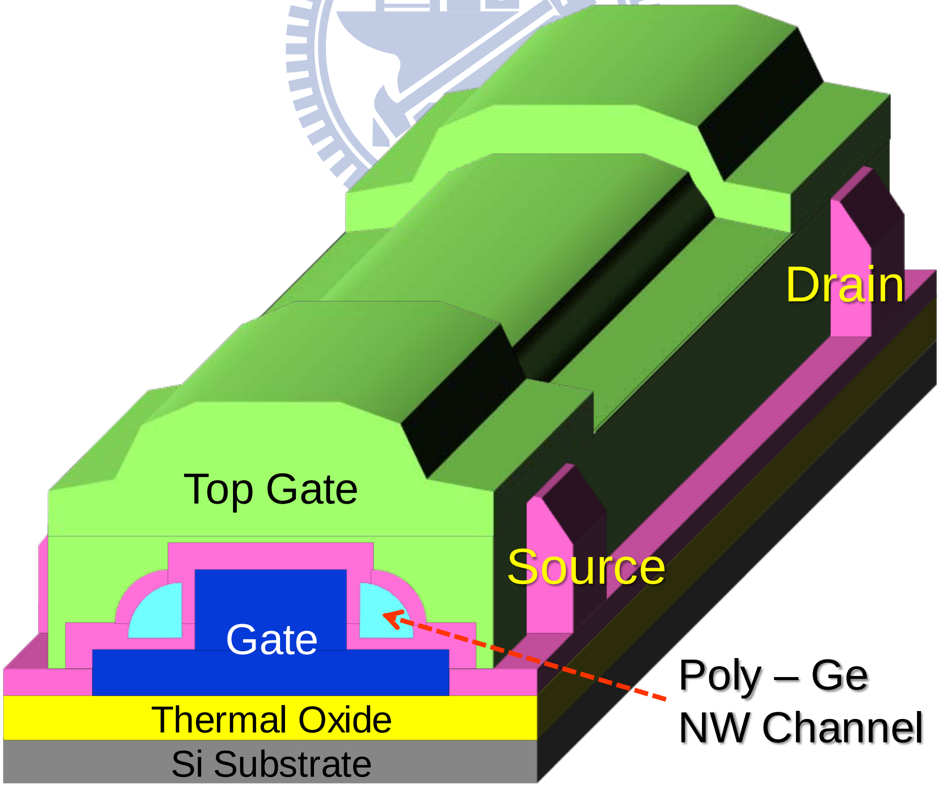


Fig. 2-9 Deposition of top gate oxide and formation of top gate.

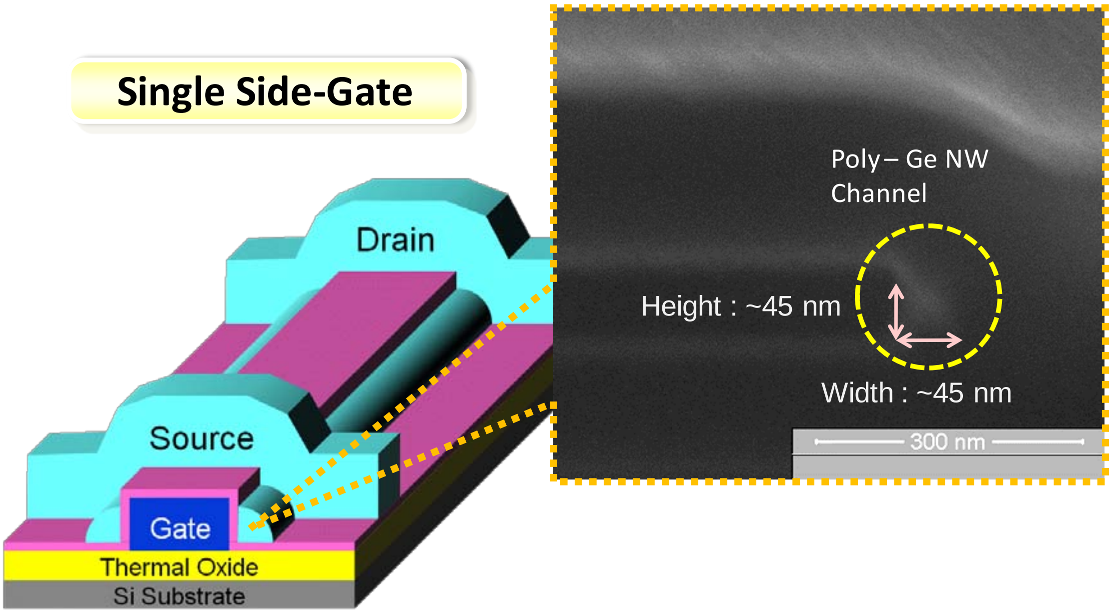
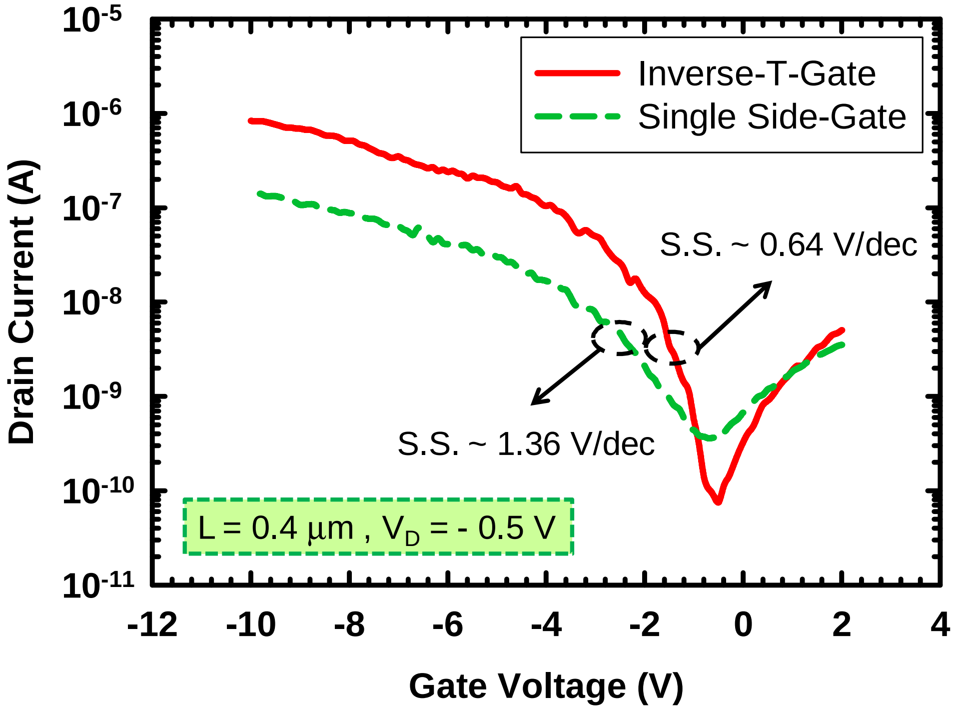
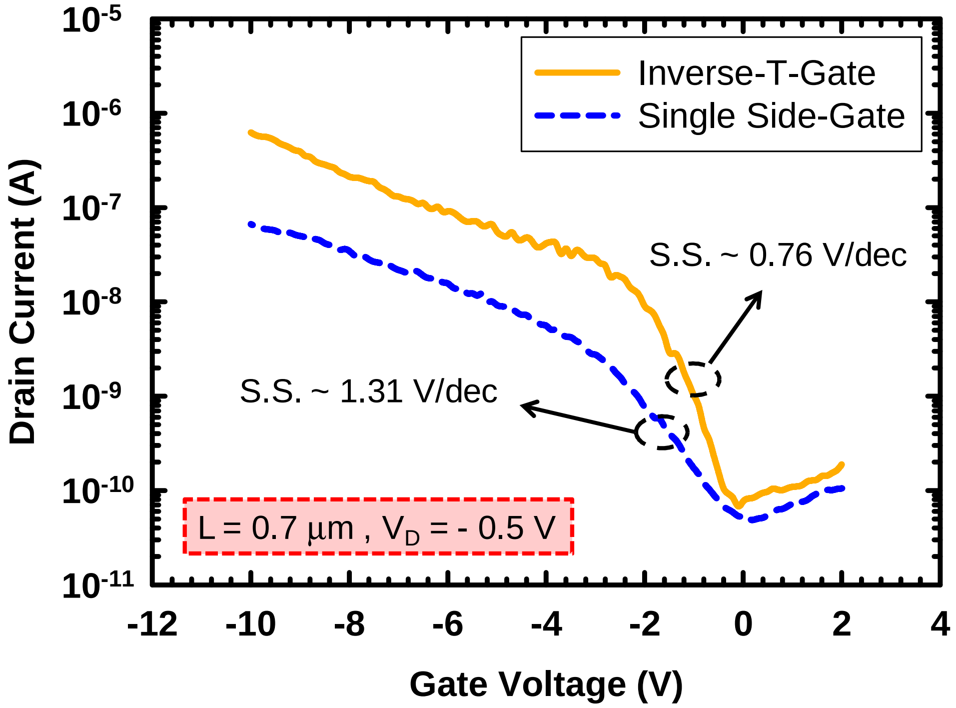


Fig. 2-10 SEM picture of a fabricated device. Both height and width of NW channel are 45 nm.



(a)



(b)

Fig. 2-11 Comparisons of transfer characteristics between inverse-T-gated and Single Side-Gated poly-Ge NWTFTs with channel length of (a) 0.4 and (b) 0.7 μm.

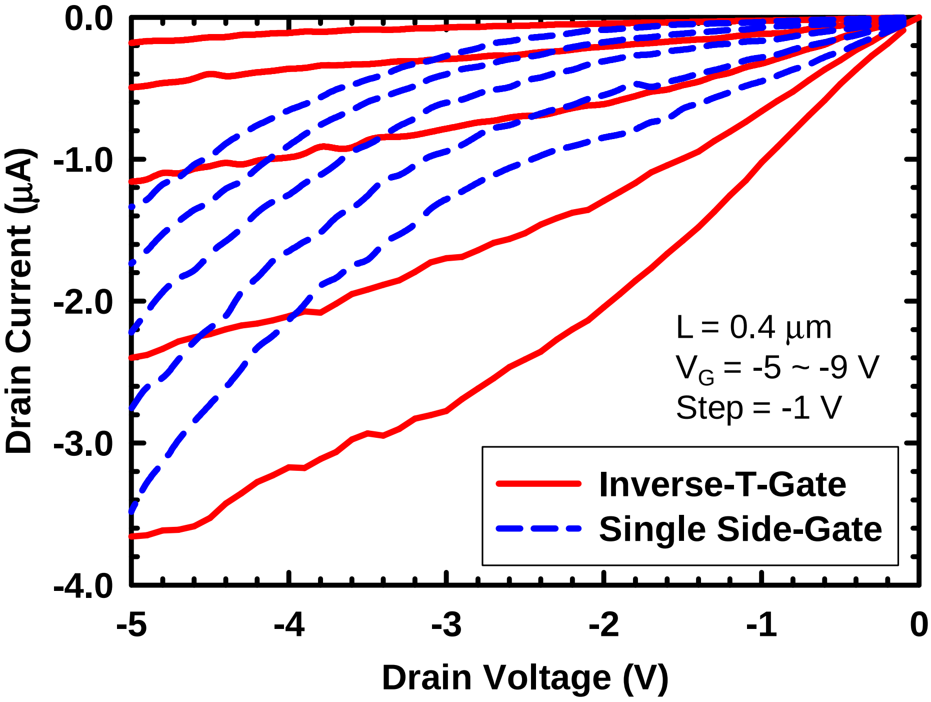


Fig. 2-12 Output characteristics of ITG and Single side- gated poly-Ge NWTFTs.

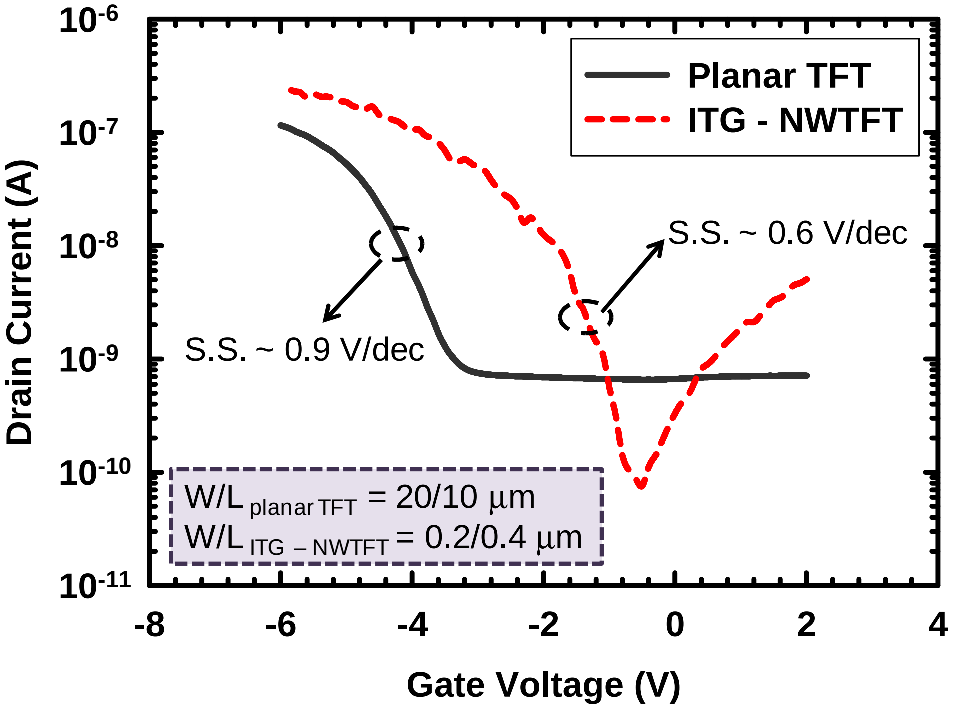


Fig. 2-13 Comparisons of transfer characteristics between poly-Ge planar TFT and poly-Ge NWTFT (ITG : inverse-T-gated).

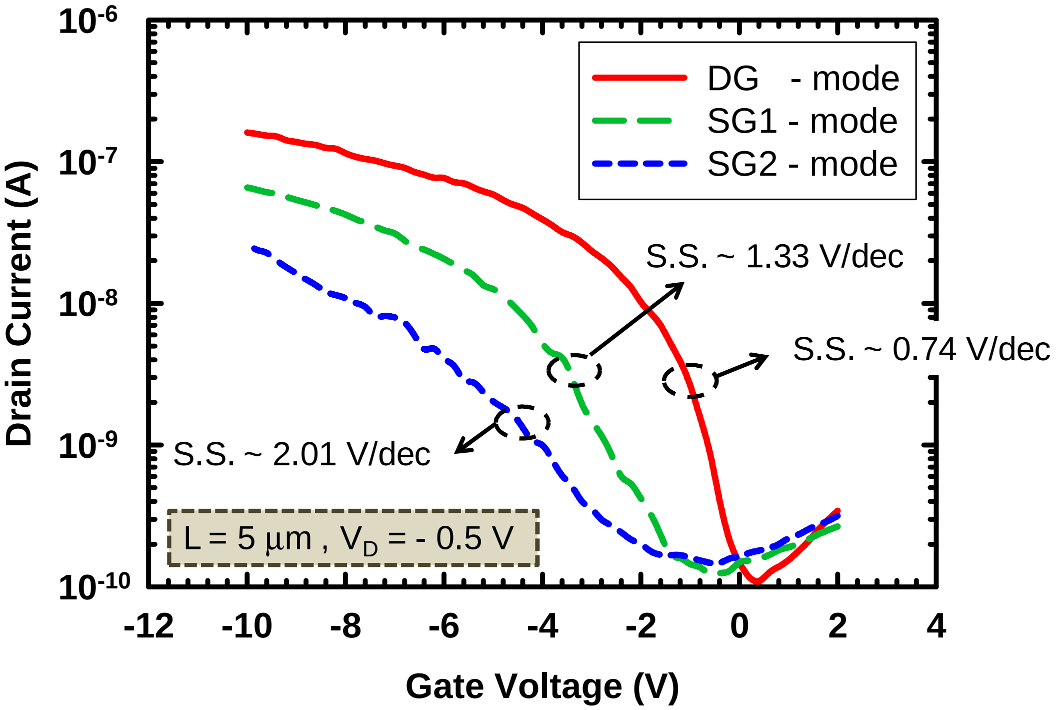


Fig. 2-14 Transfer characteristics of independent DG poly-Ge NWTFT operated in single-gated (SG) modes and double-gated (DG) mode.

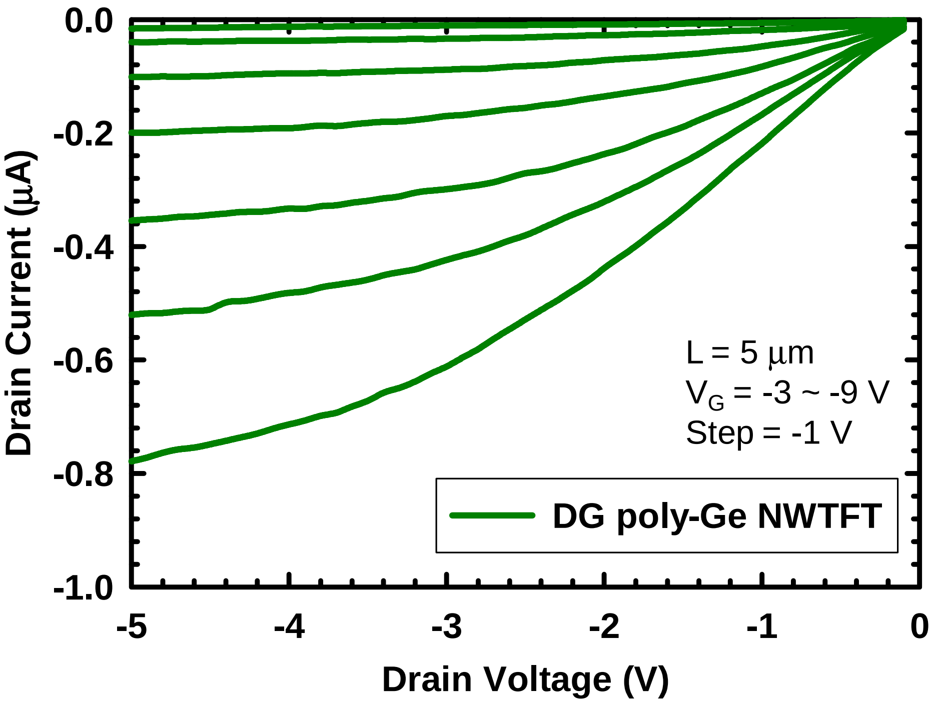
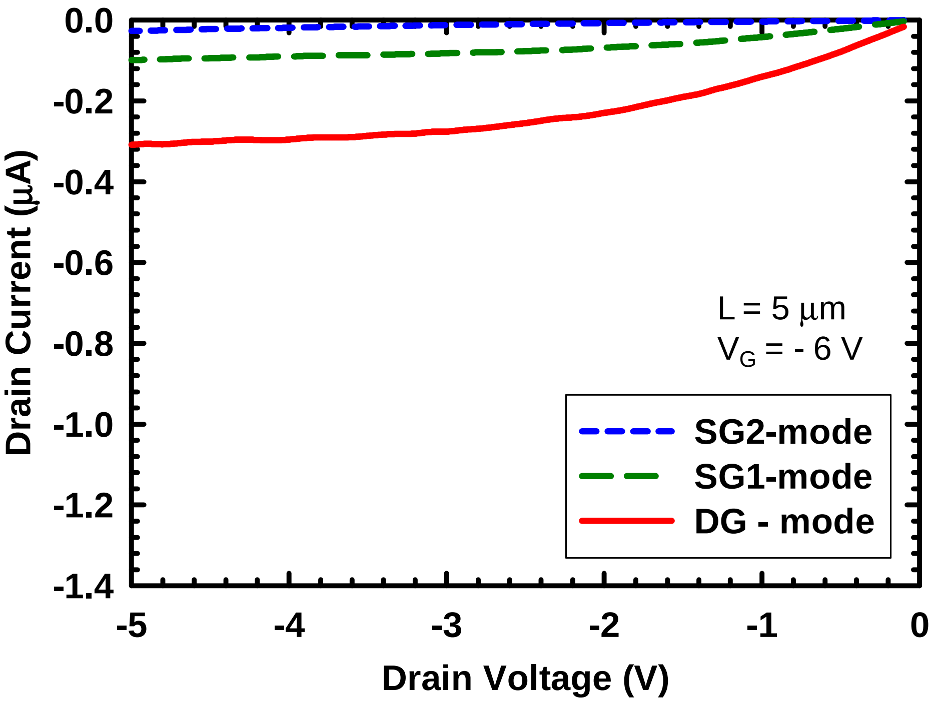
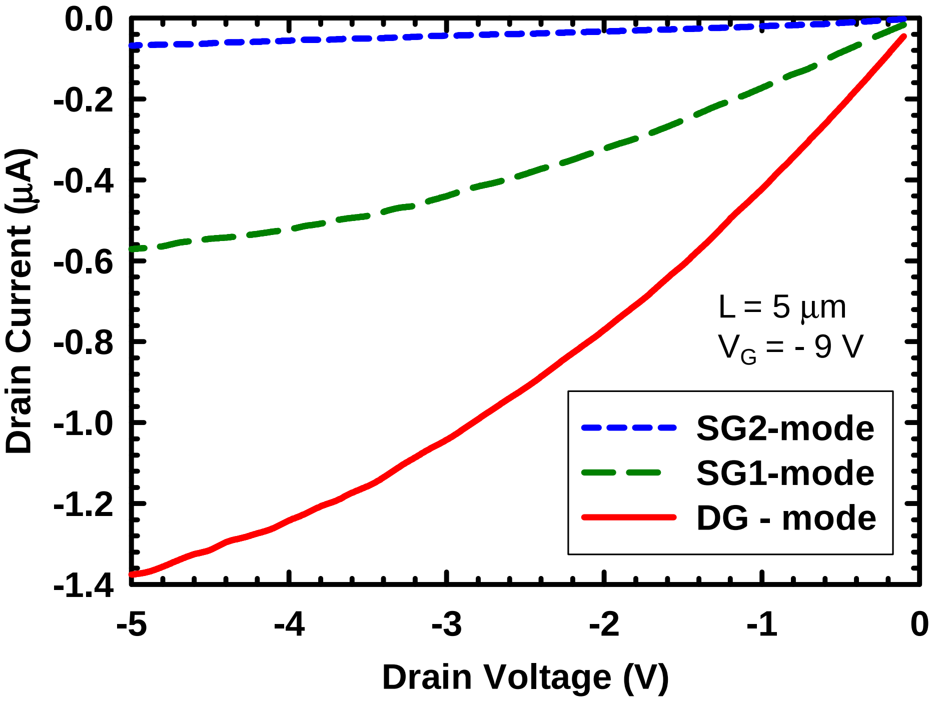


Fig. 2-15 Output characteristics of a device under DG mode.



(a)



(b)

Fig. 2-16 Comparisons of output characteristics between DG and SG modes of operations with gate voltage of (a) -6 V and (b) -9 V.

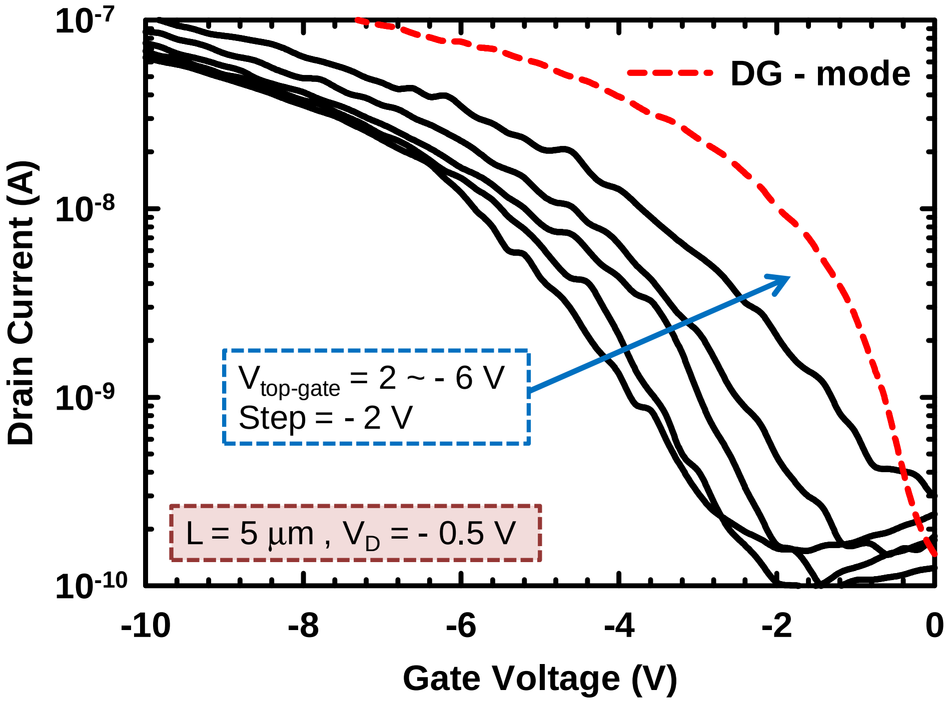


Fig. 2-17 Transfer characteristics of DG devices characterized by sweeping inverse-T gate voltage with top gate biased at various constant values.

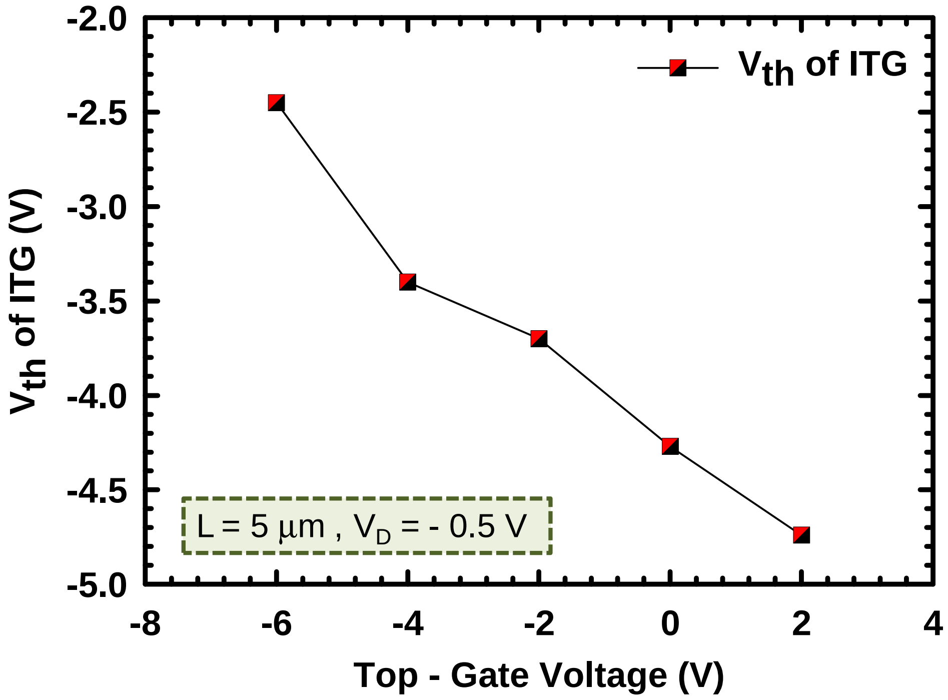
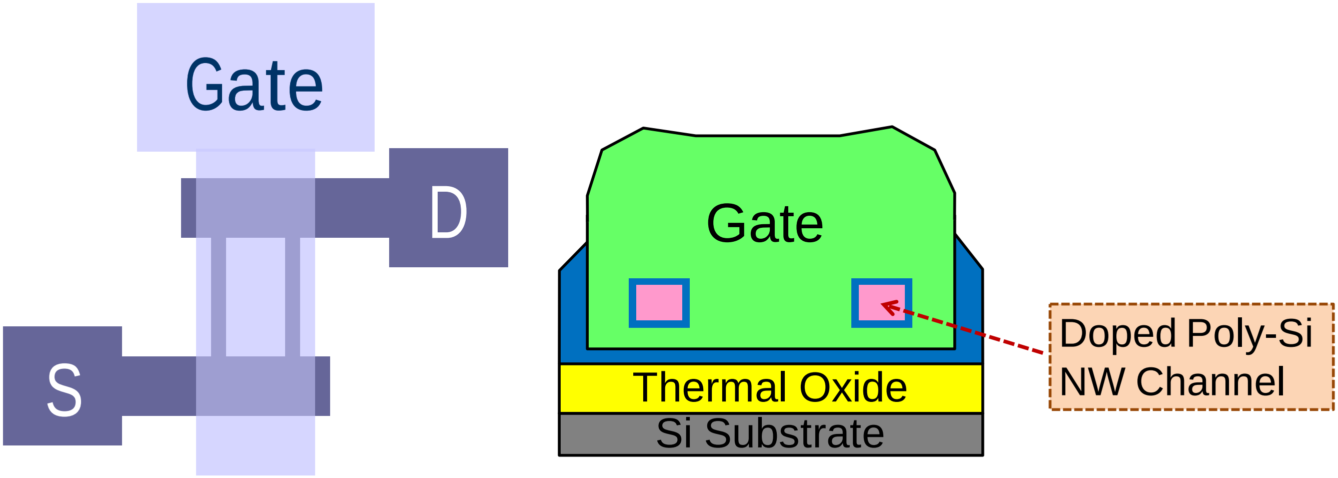


Fig. 2-18 Extracted V_{th} as a function of top-gate voltage (ITG : inverse-T-gated).



(a) (b)

Fig. 3-1 (a) Top view and (b) cross-sectional view of a JL poly-Si NWFET.

(a)

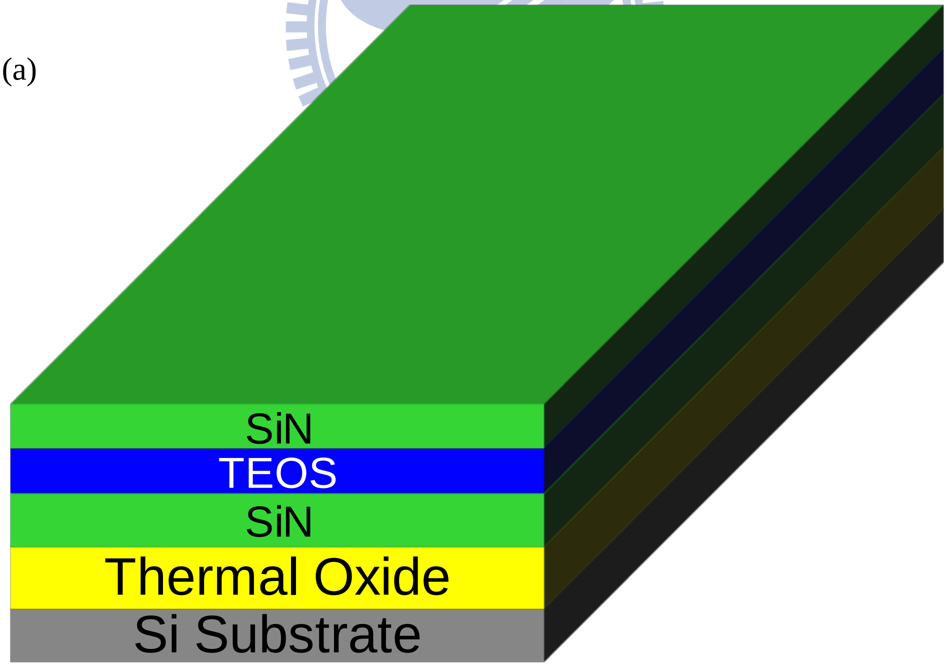


Fig. 3-2 Fabrication of the JL device. (a) Deposition of a bottom nitride/TEOS oxide/hardmask nitride stacked layer. The thicknesses were 50/30/30 nm, respectively.

(b)

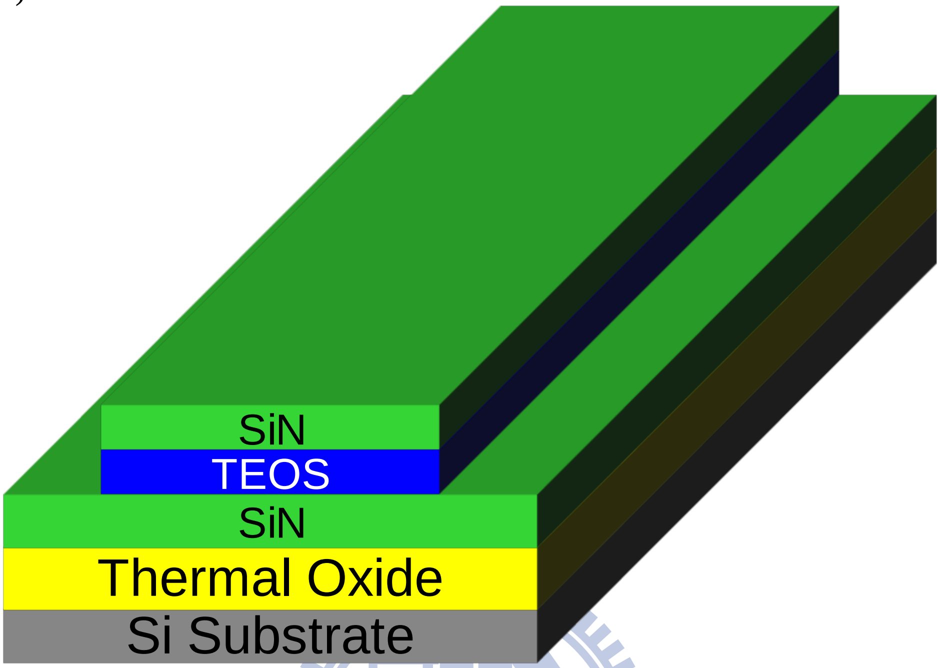


Fig. 3-2 (b) The hardmask nitride/TEOS oxide stack was defined by anisotropic reactive plasma etching.

(c)

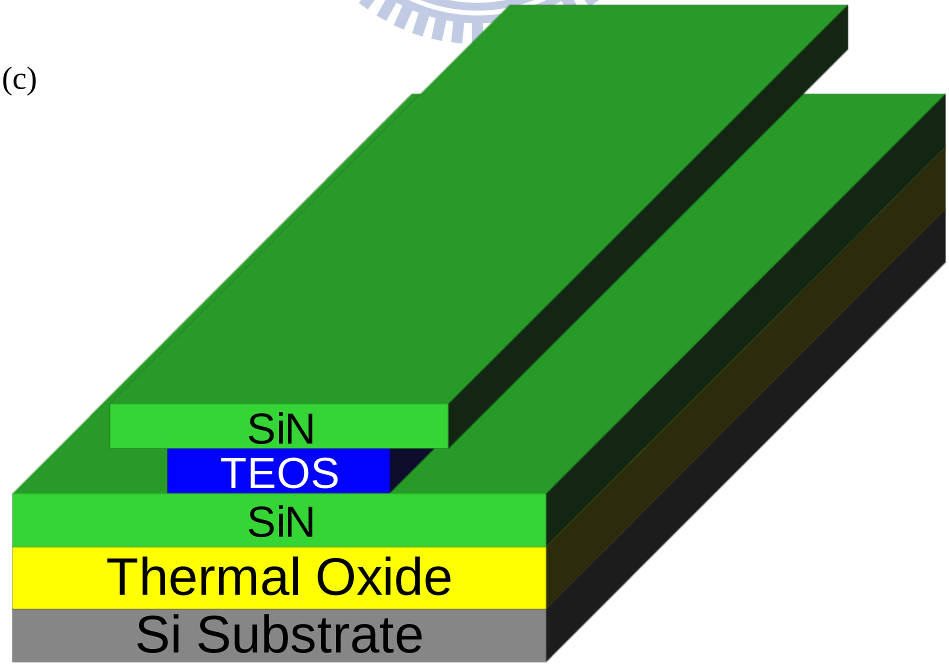


Fig. 3-2 (c) The formation of cavities by utilizing DHF lateral etching.

(d)

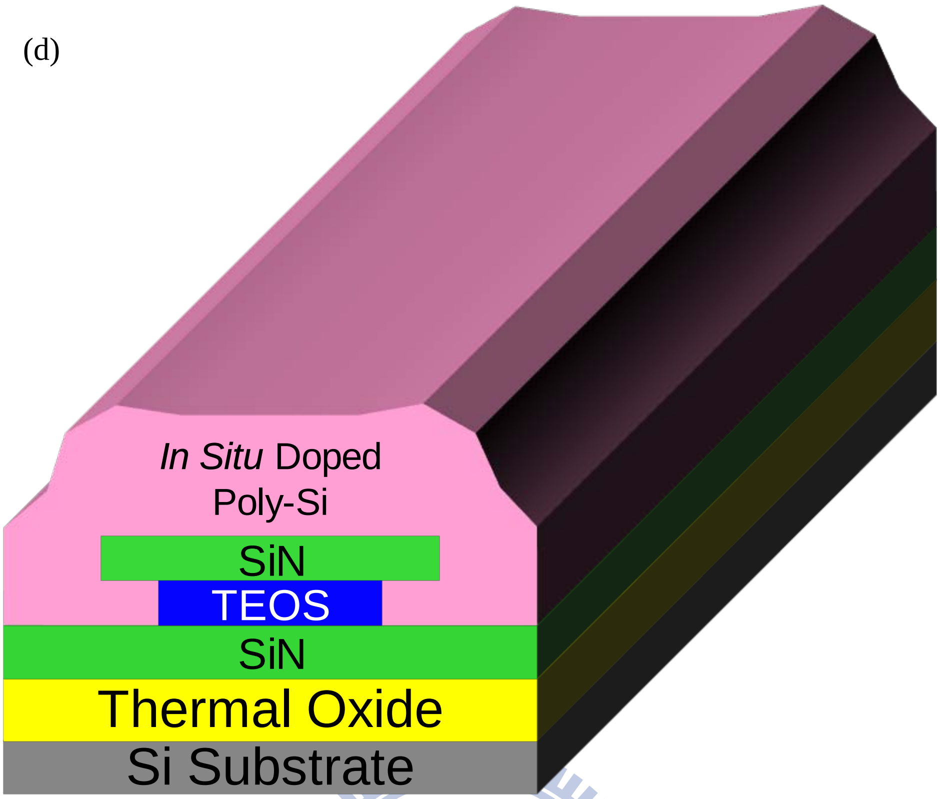


Fig. 3-2 (d) Deposition of *in situ* phosphorus doped poly-Si layer.

(e)

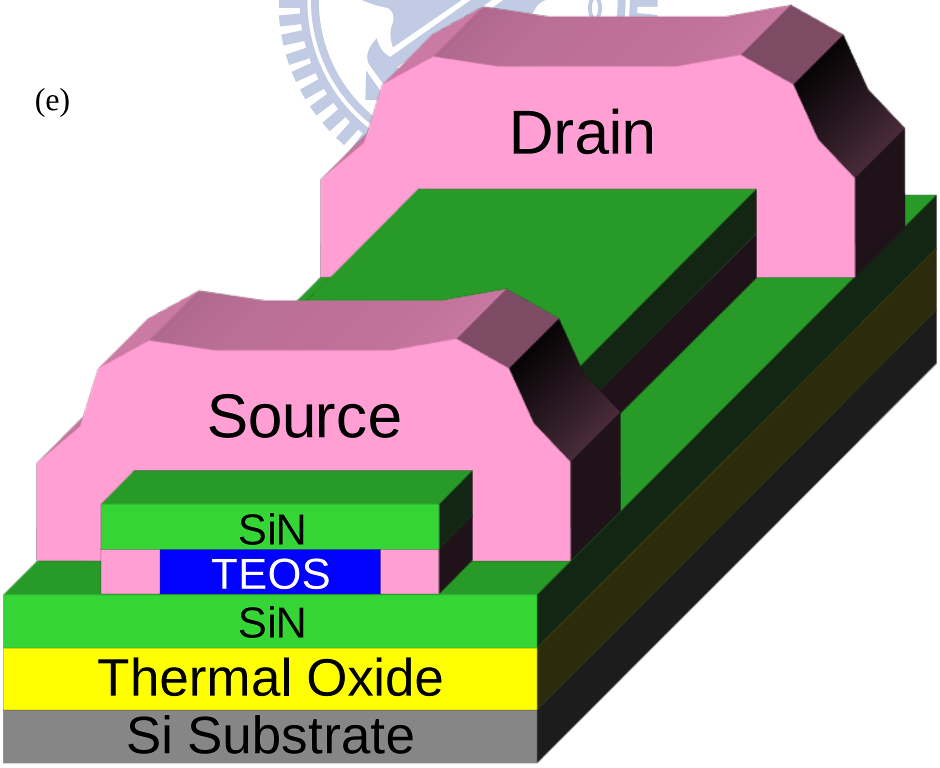


Fig. 3-2 (e) Definition of source/drain and formation of doped poly-Si NW channels.

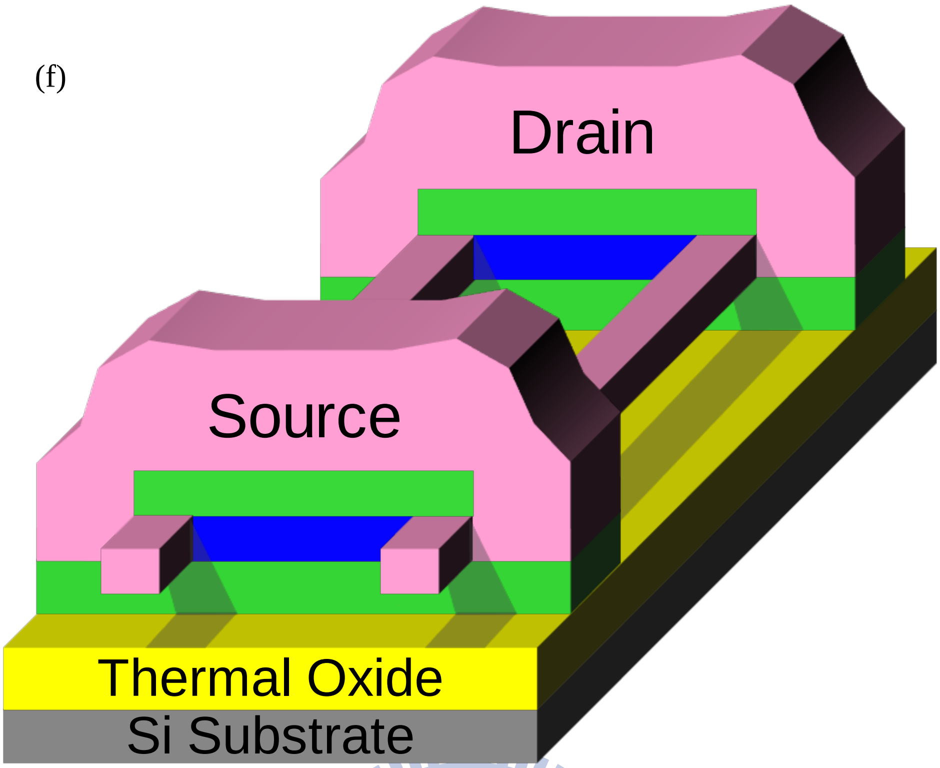


Fig. 3-2 (f) Removal of bottom nitride/TEOS oxide/hardmask nitride stacked layer. The NW channels are hanging between the S/D regions.

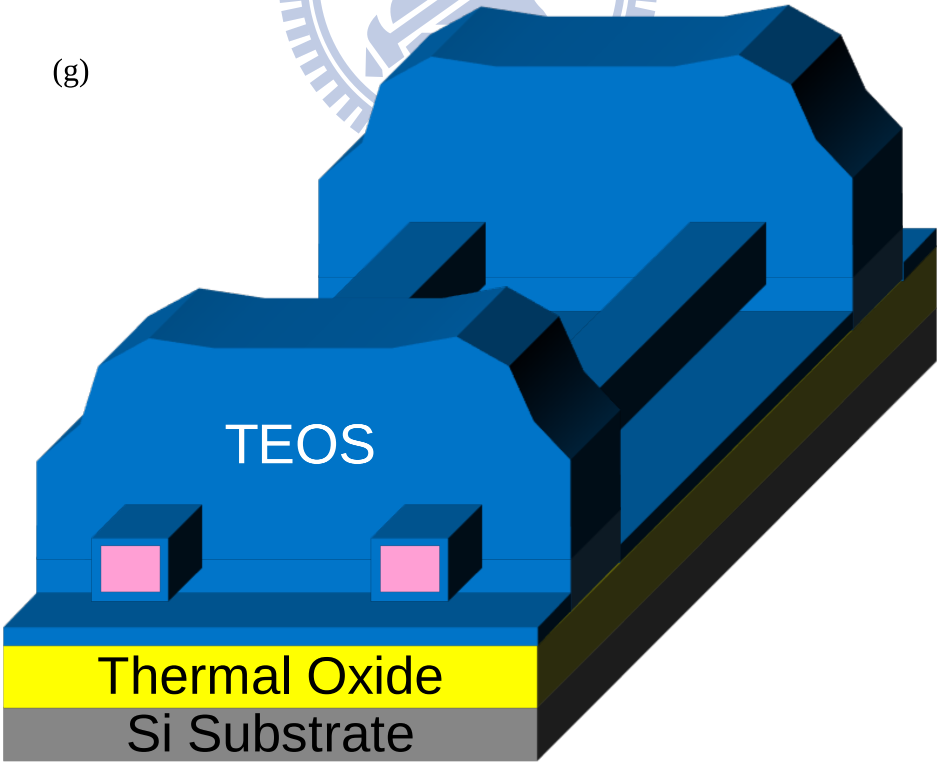


Fig. 3-2 (g) Deposition of a TEOS oxide layer as the gate dielectric.

(h)

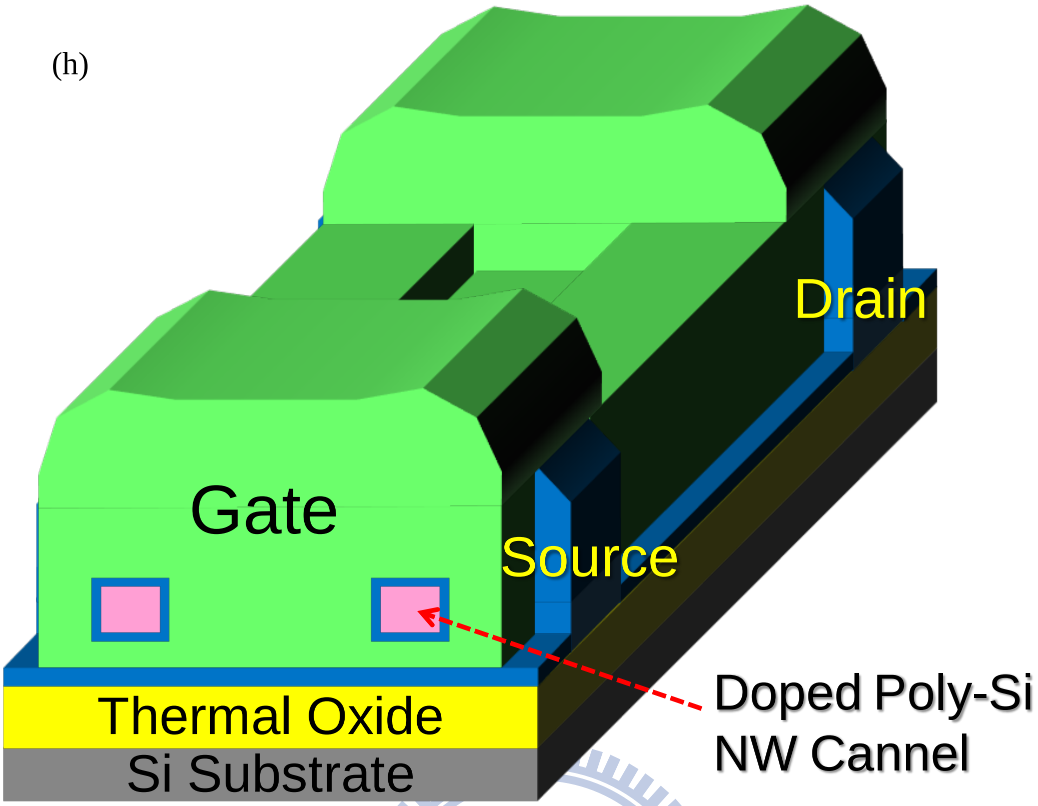


Fig. 3-2 (h) Deposition of a TiN film as the gate electrode.

(a)

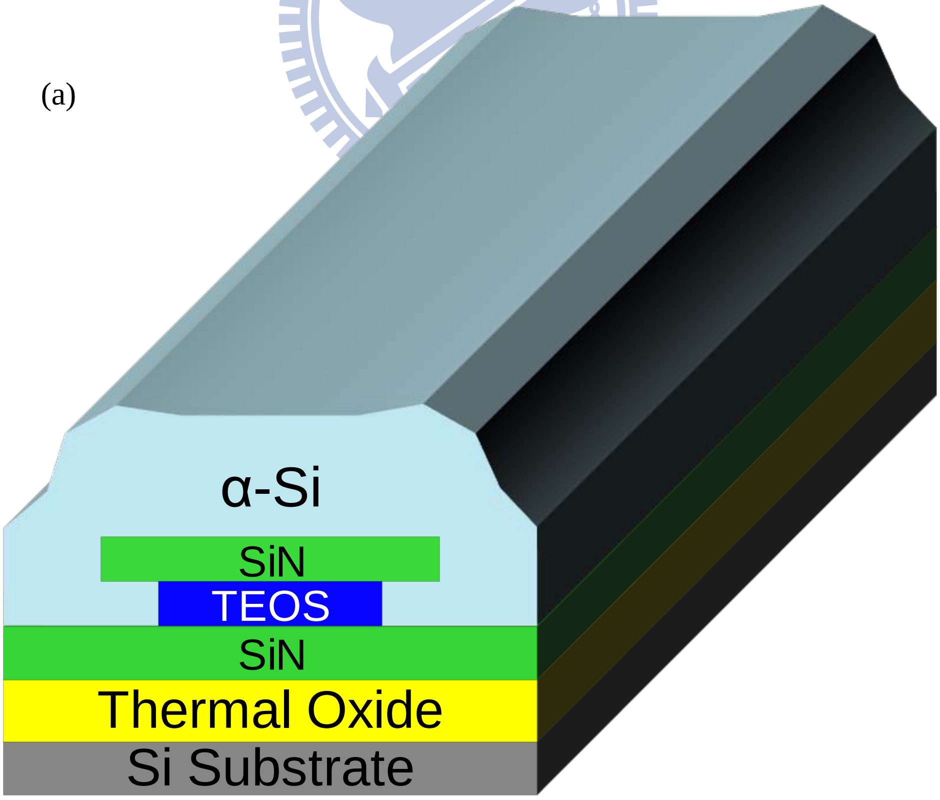


Fig. 3-3 Fabrication of the IM device. (a) 100 nm amorphous-Si layer deposition followed by 600^{o}C annealing at N_2 ambient for 24 HR (SPC).

(b)

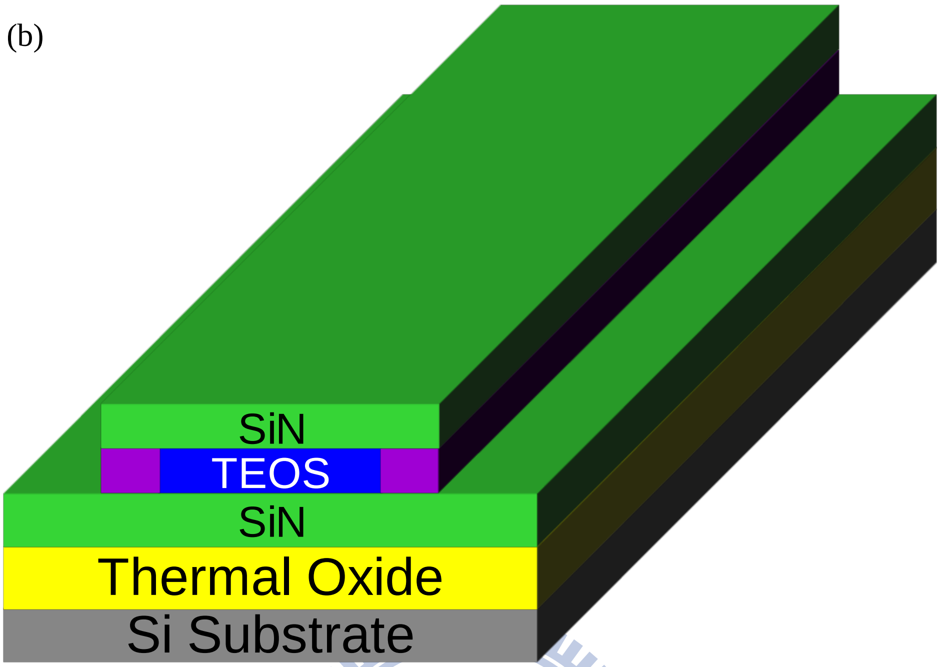


Fig. 3-3 (b) Dry etching to form NWs underneath the hard mask.

(c)

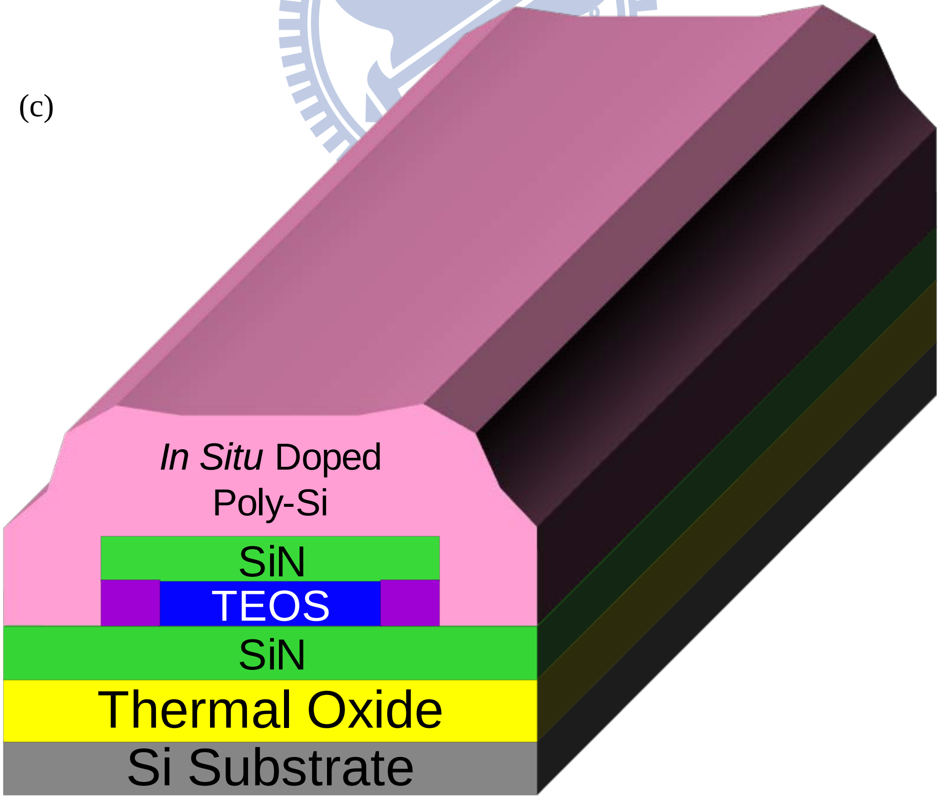


Fig. 3-3 (c) Deposition of 100 nm *in situ* phosphorus doped poly-Si layer.

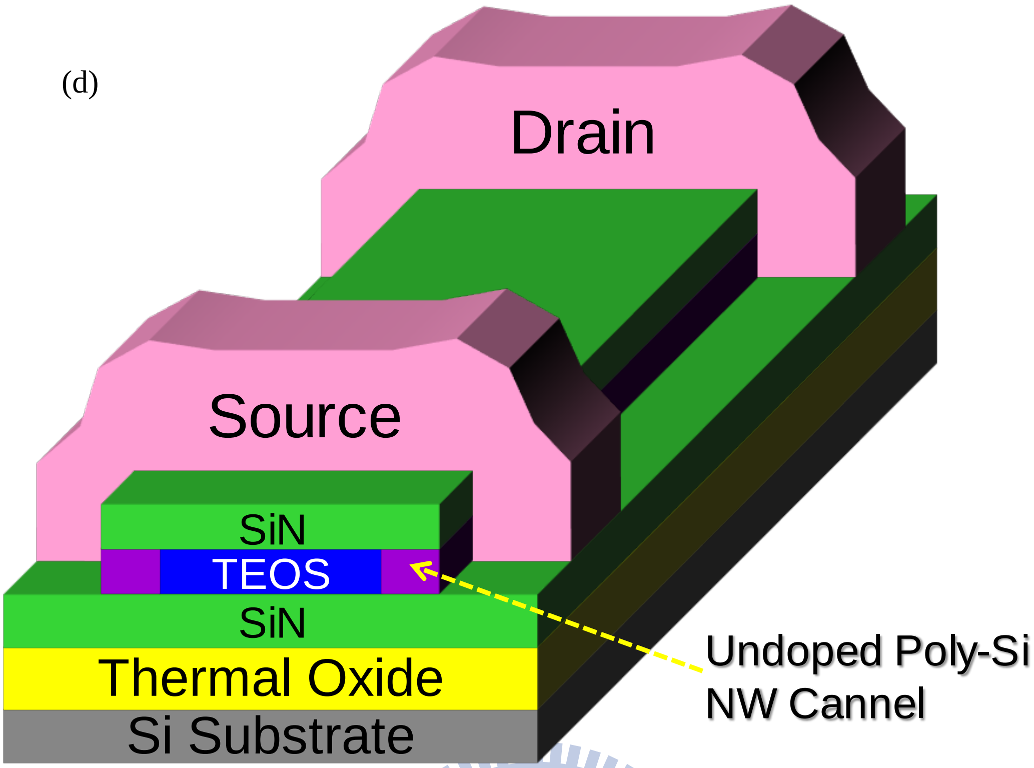


Fig. 3-3 (d) Definition of S/D regions by dry etching.

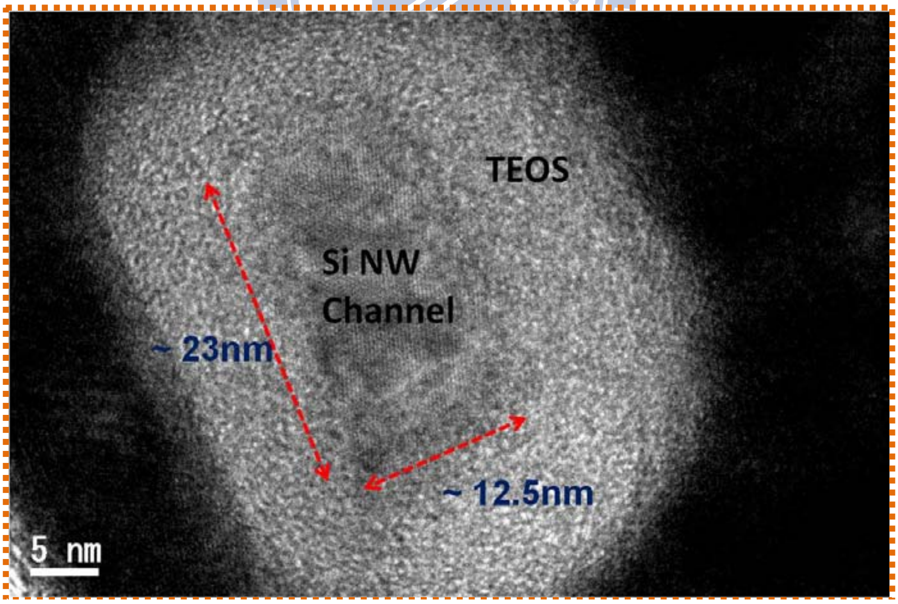
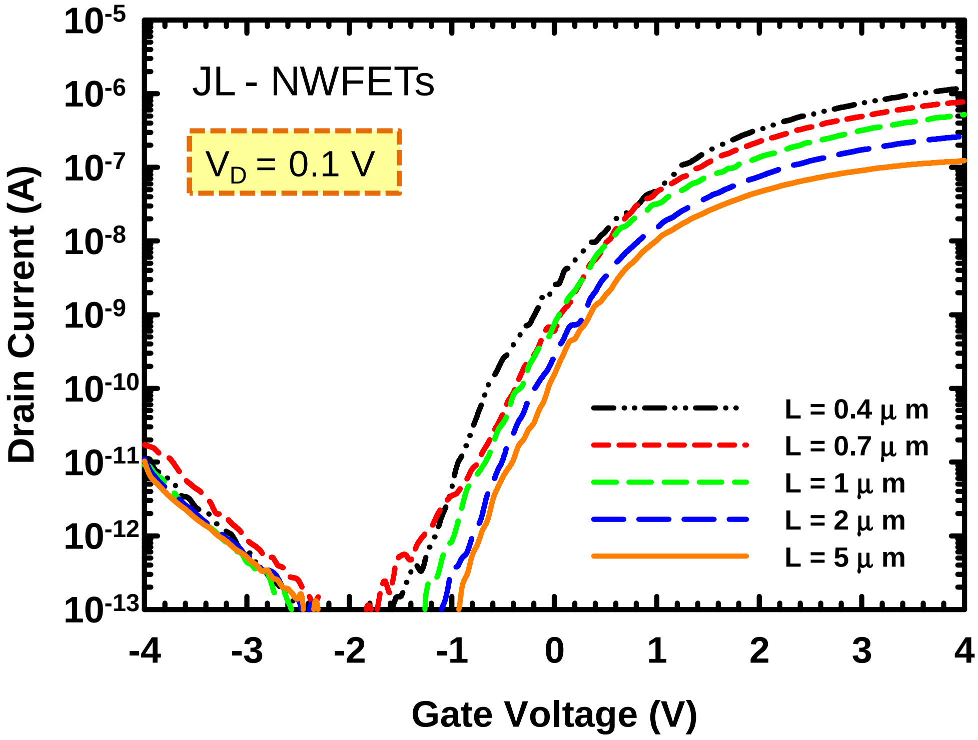
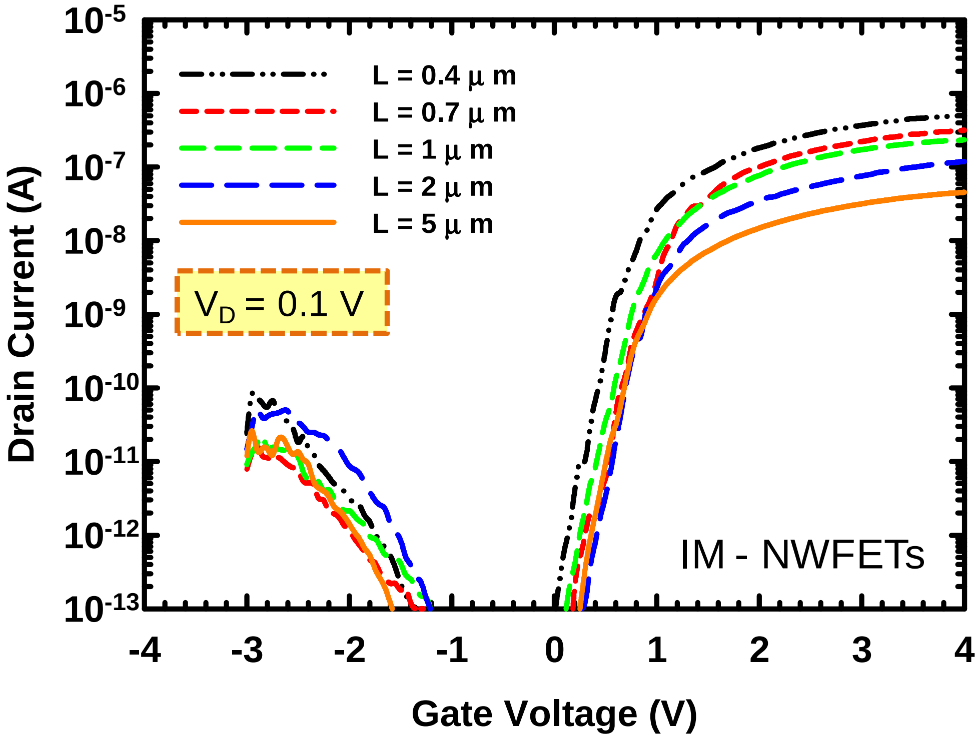


Fig. 3-4 Cross-sectional-view TEM picture of a JL-NWFET with GAA structure.



(a)



(b)

Fig. 3-5 Transfer characteristics of (a) JL-NWFETs and (b) IM-NWFETs at V_D = 0.1 V.

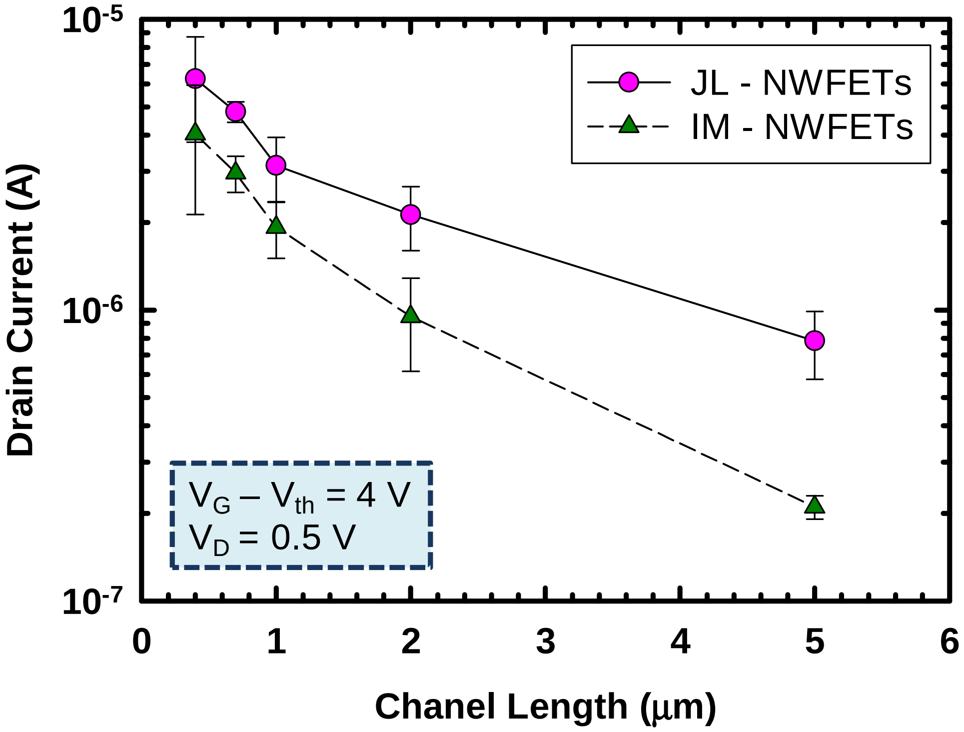
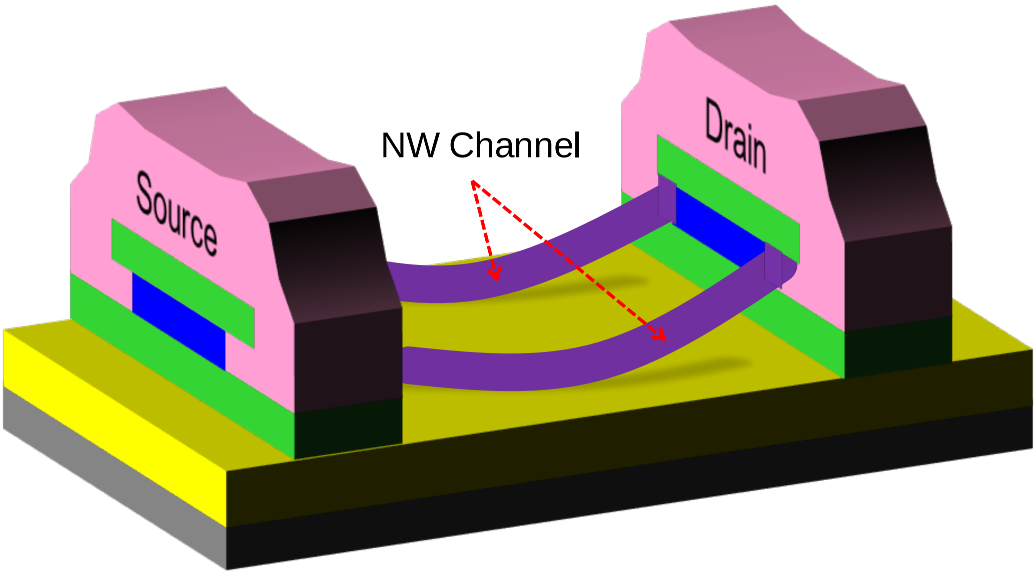
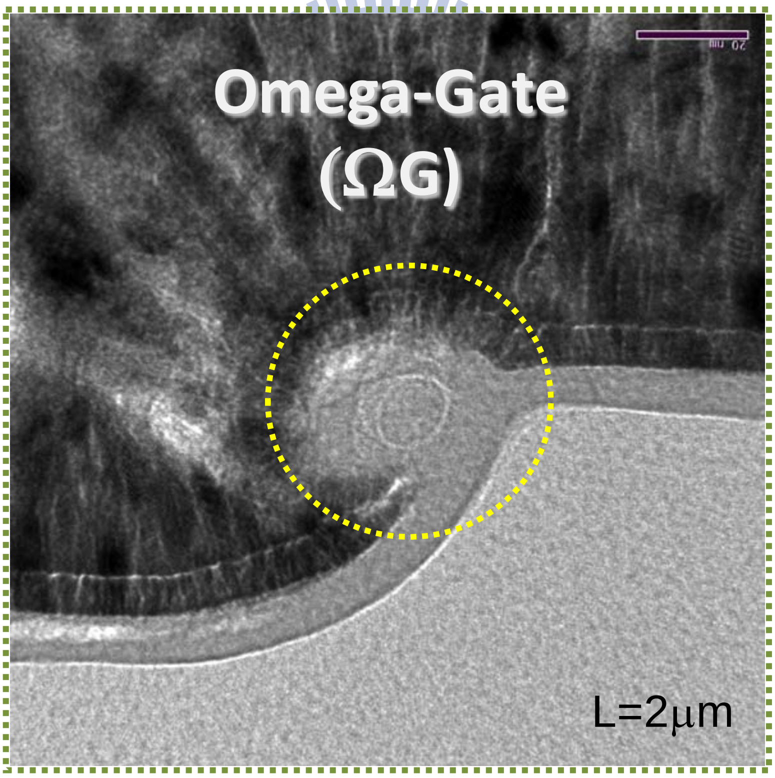


Fig. 3-6 Measured I_{ON} of JL and IM devices as a function of channel length.

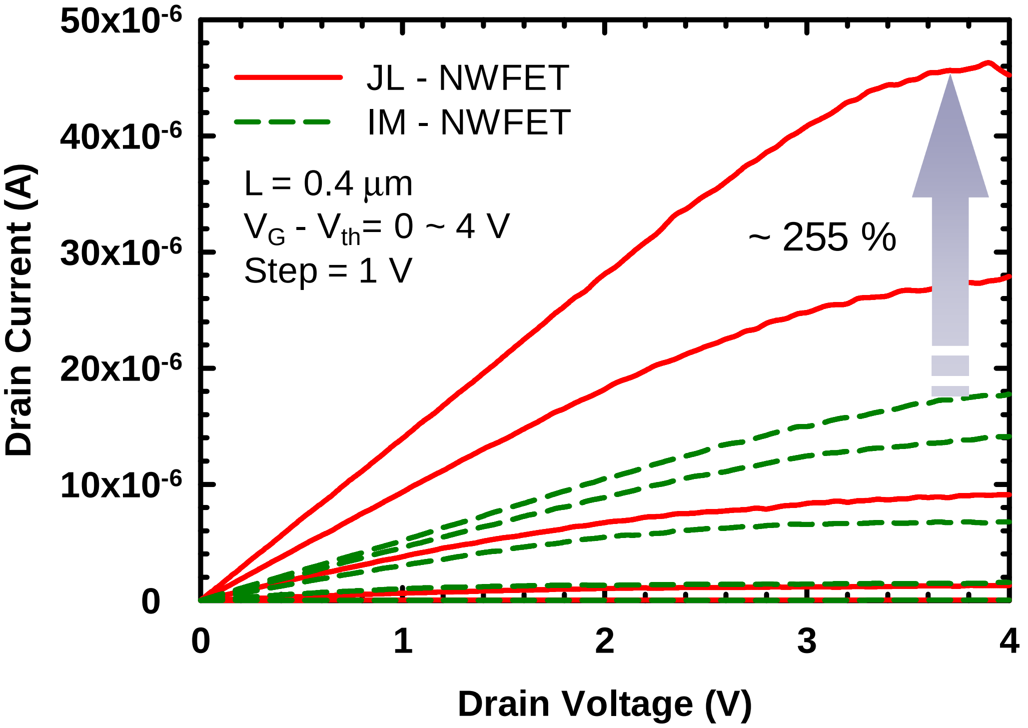


(a)

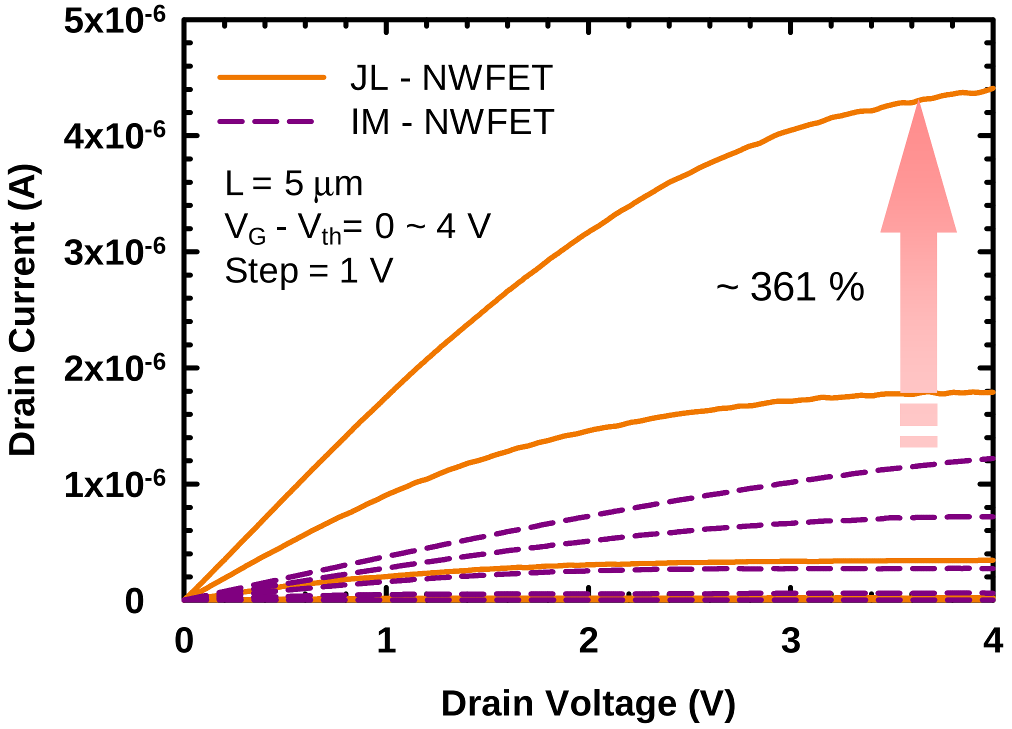


(b)

Fig. 3-7 (a) A schematic diagram illustrating the collapse of the suspended NW channels after the surrounding dielectrics were removed during fabrication as the channel length is larger than 1 μm. (b) TEM image of omega-gate.

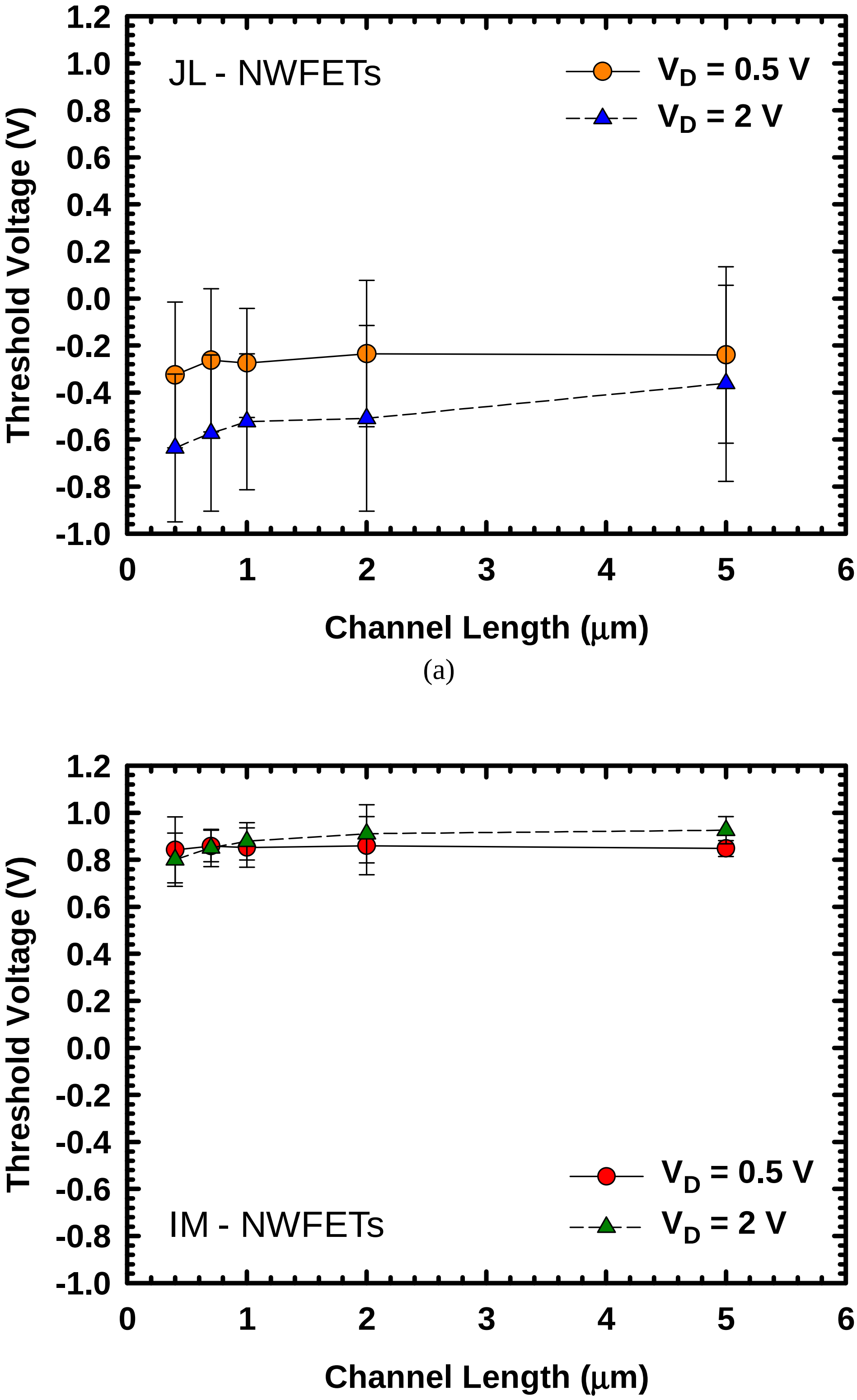


(a)



(b)

Fig. 3-8 Output characteristics of the JL and IM NWFETs with (a) L = 0.4 μm and (b) L = 5 μm.



(a)

(b)

Fig. 3-9 Threshold voltage as a function of channel length for (a) JL-NWFETs and (b) IM-NWFETs.

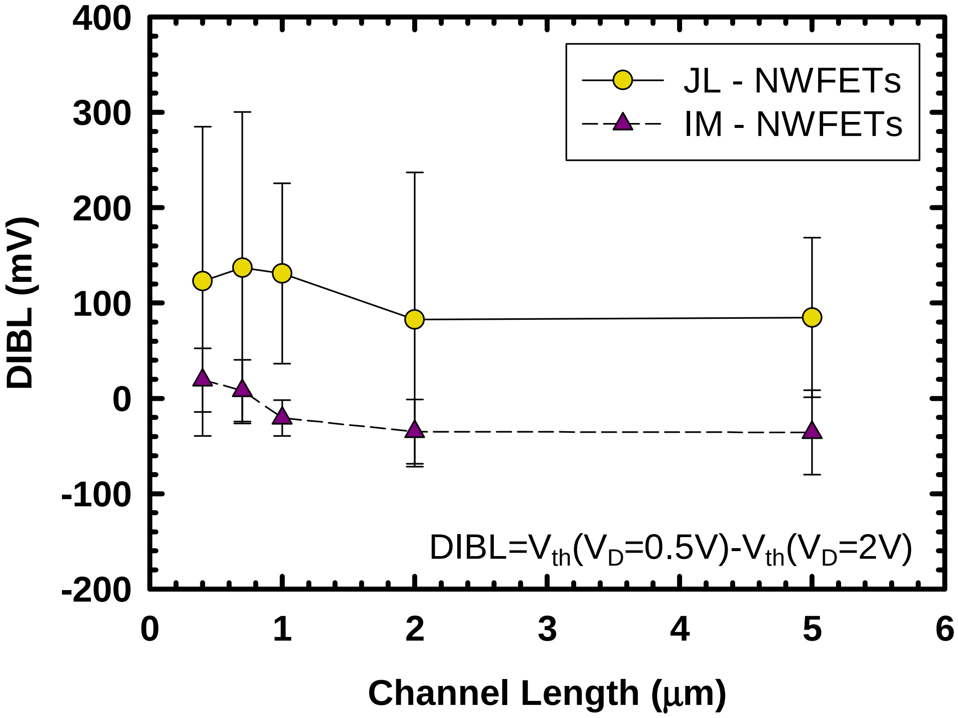
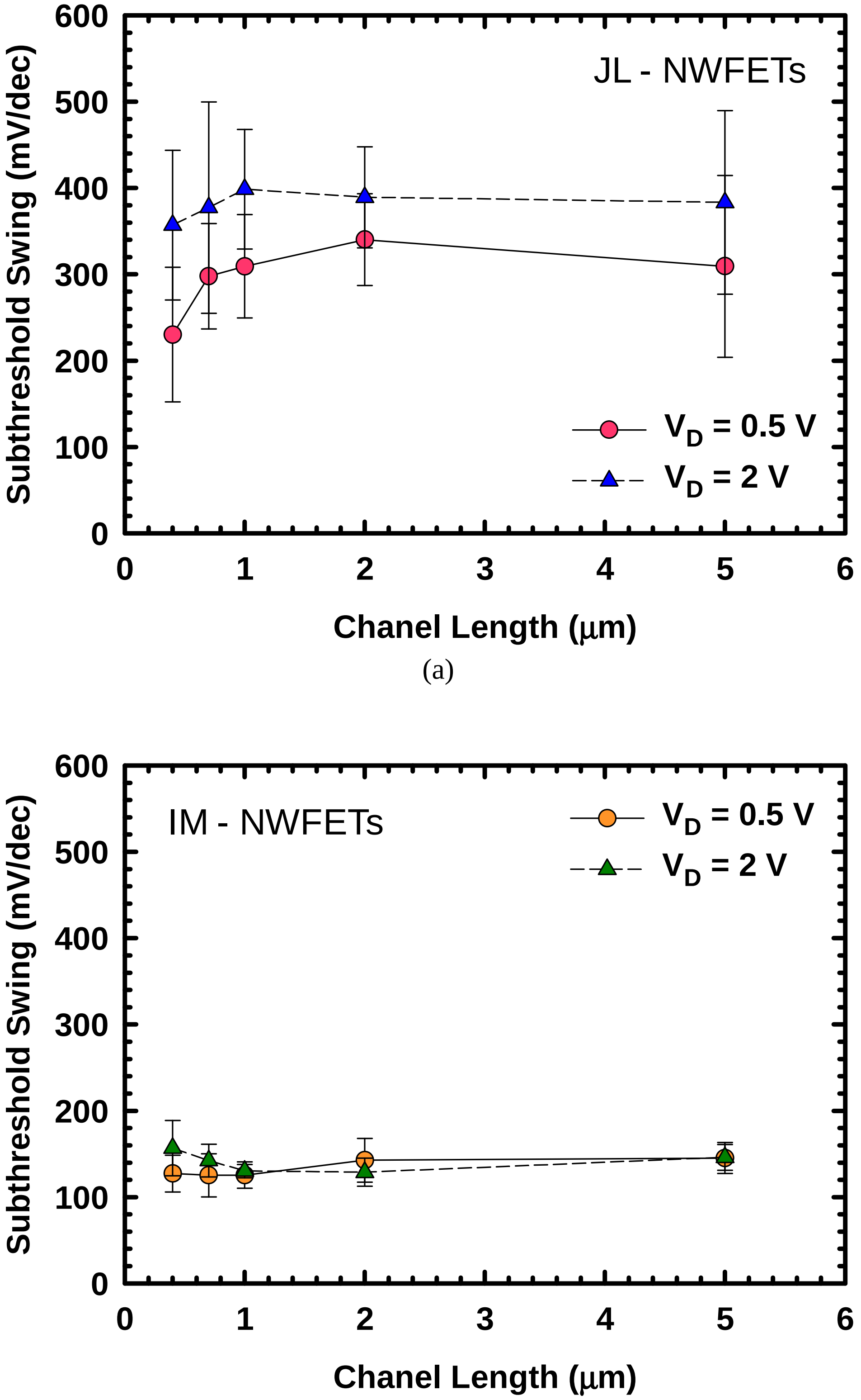


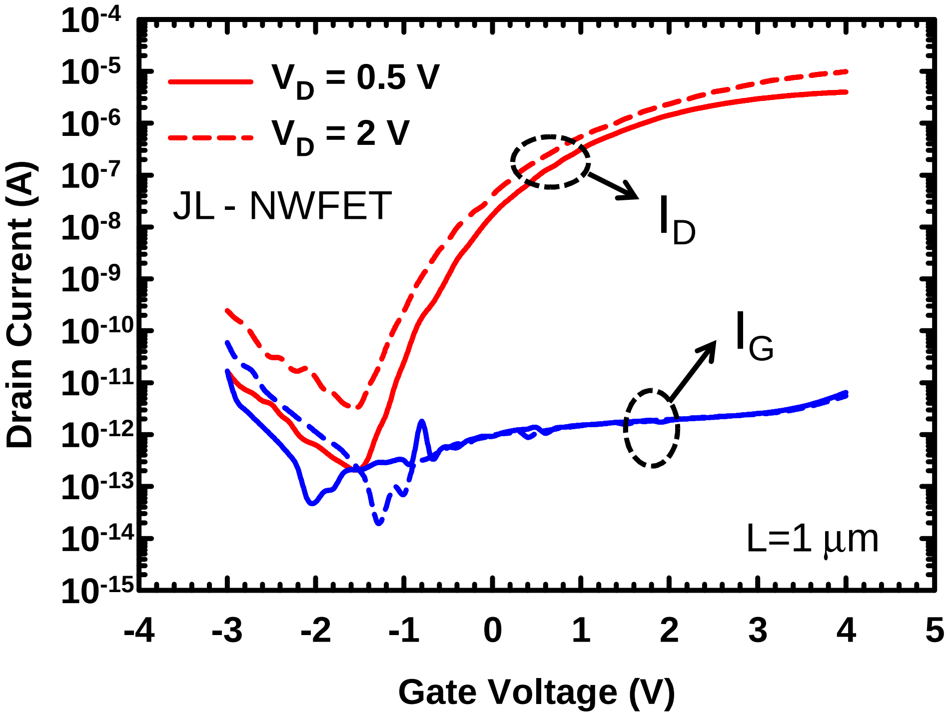
Fig. 3-10 Drain-induced barrier lowering (DIBL) for JL-NWFETs and IM-NWFETs as a function of channel length.



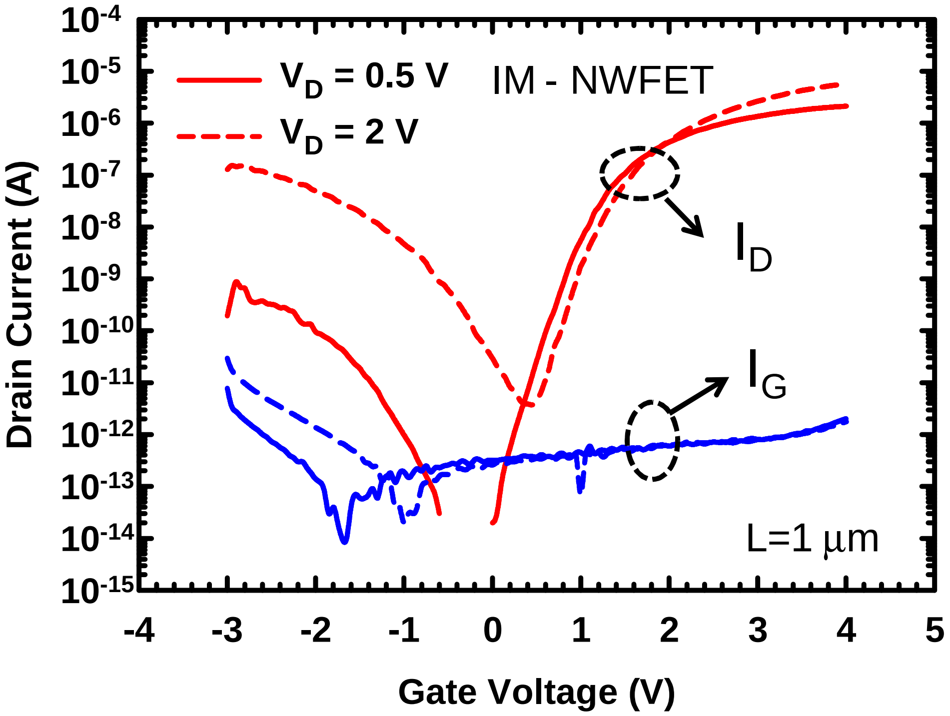
(a)

(b)

Fig. 3-11 The subthreshold swing of (a) JL-NWFETs and (b) IM-NWFETs as a function of channel length.

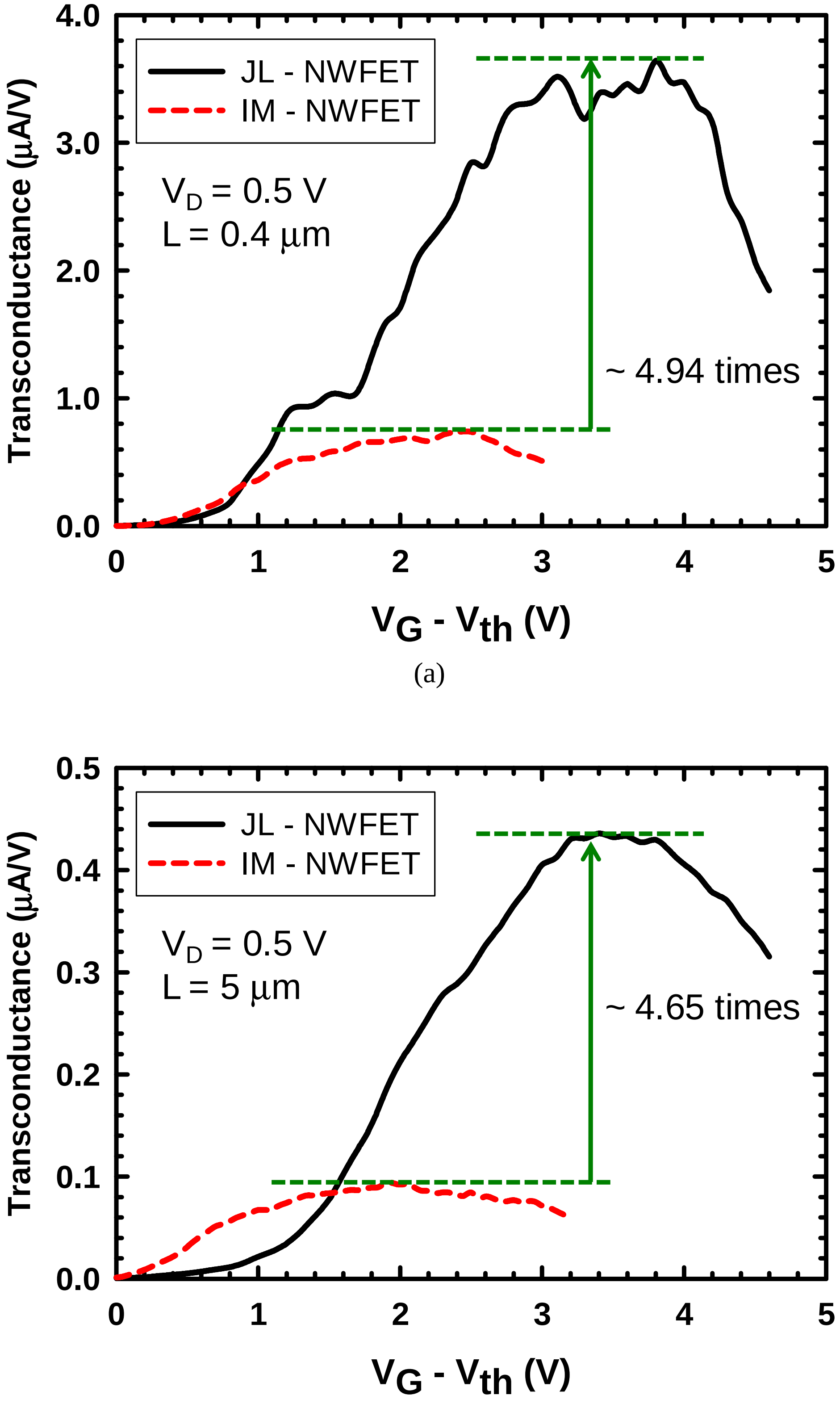


(a)



(b)

Fig. 3-12 Drain current and gate current versus gate voltage for (a) JL-NWFET and (b) IM-NWFET measured at V_D = 0.5 V and V_D = 2 V.



(a)

(b)

Fig. 3-13 The transconductance of devices as a function of gate overdrive voltage with (a) L = 0.4 μm and (b) L = 5 μm.

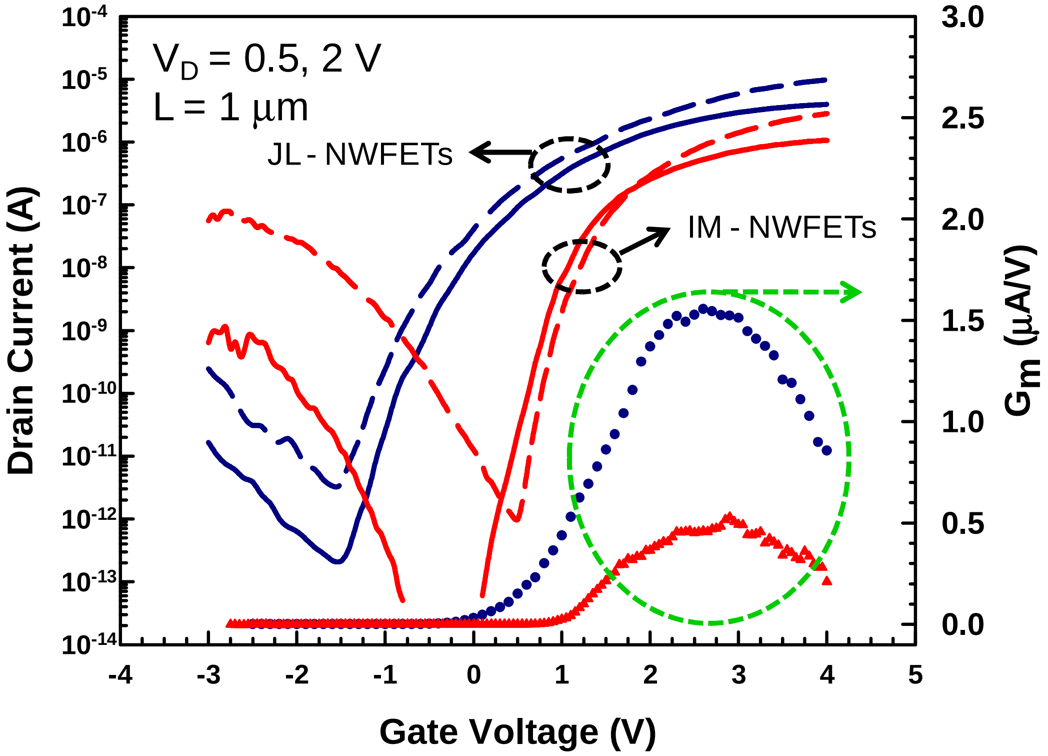


Fig. 3-14 Subthreshold characteristics and transconductance of JL-NWFET and IM-NWFET versus gate voltage.

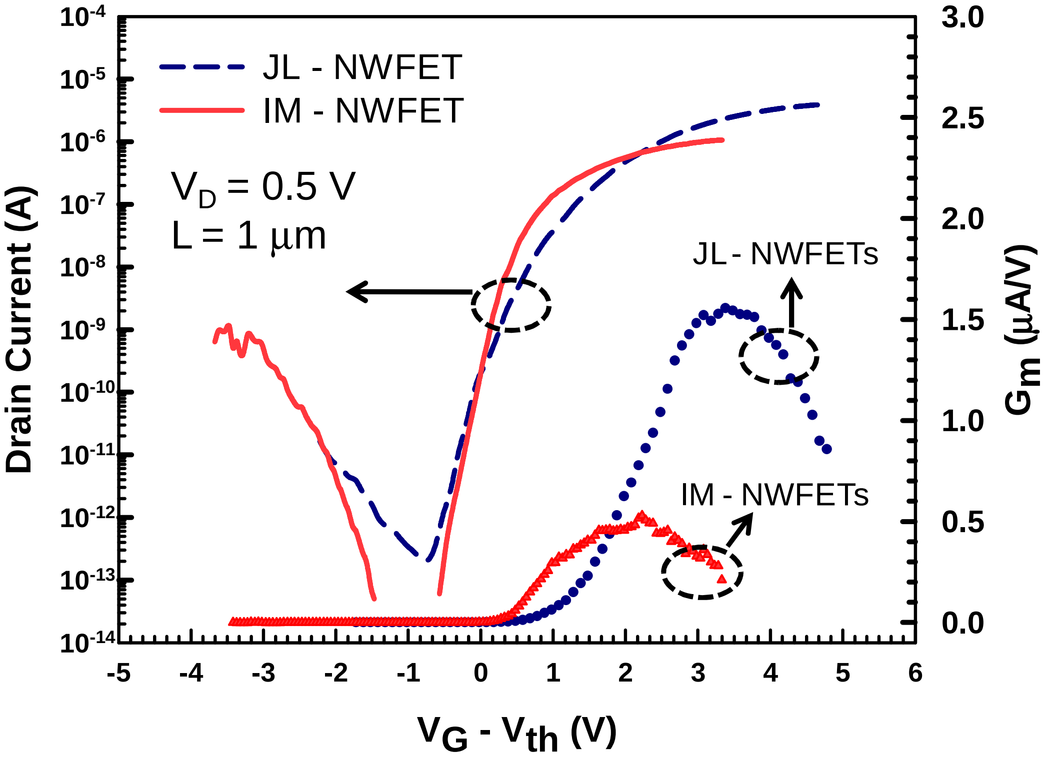


Fig. 3-15 Subthreshold characteristics and transconductance as a function of gate overdrive voltage.

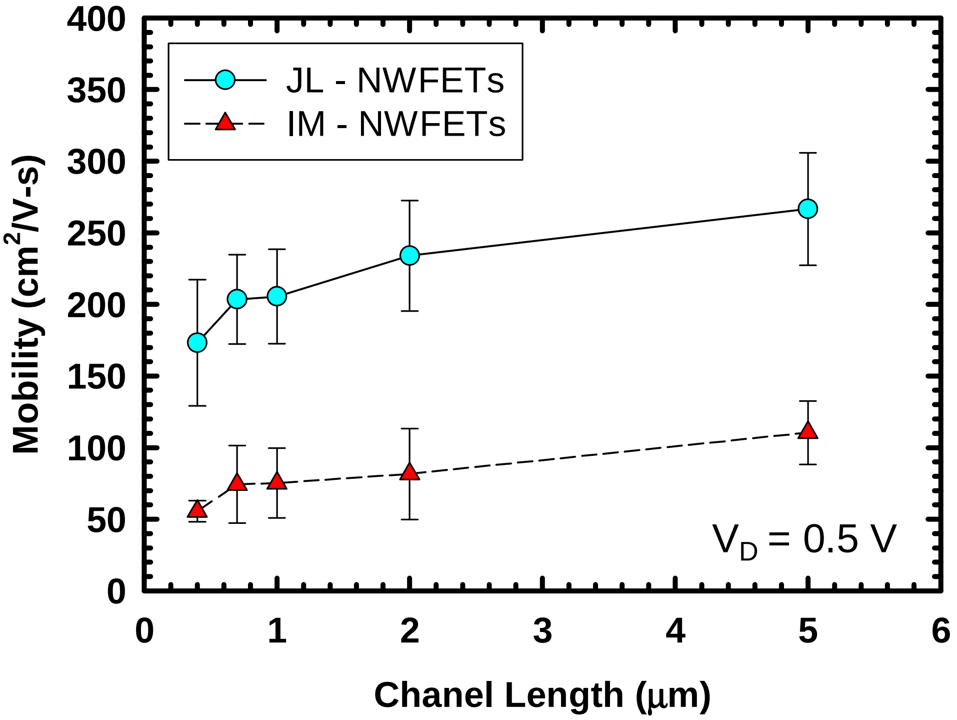


Fig. 3-16 Comparisons of field-effect mobility for JL-NWFETs and IM-NWFETs.

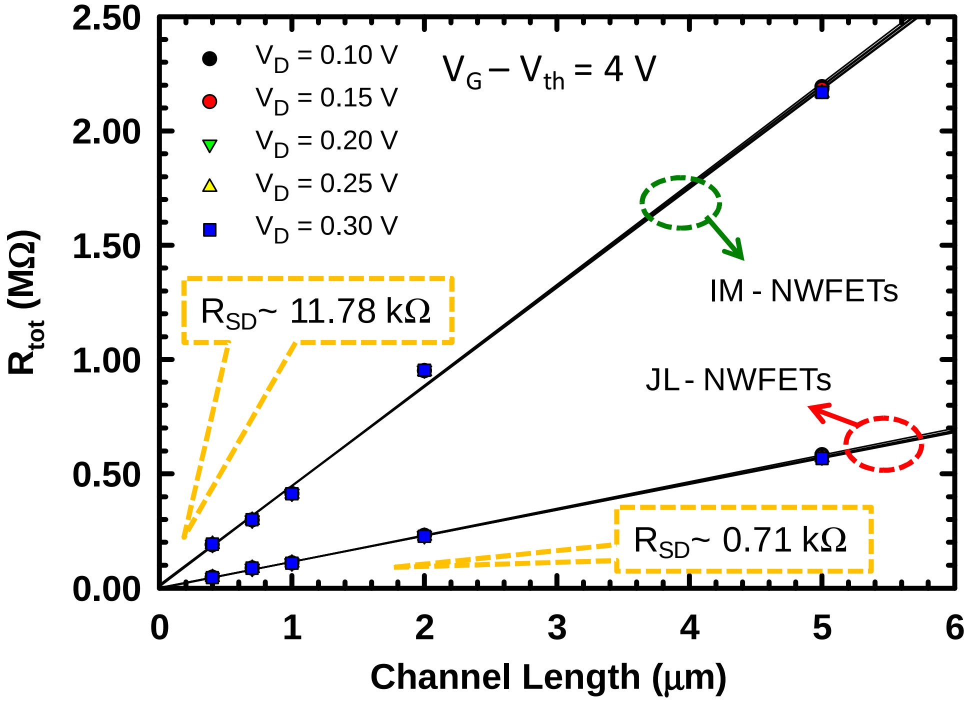


Fig. 3-17 Extraction of R_{tot} for JL-NWFETs and IM-NWFETs.

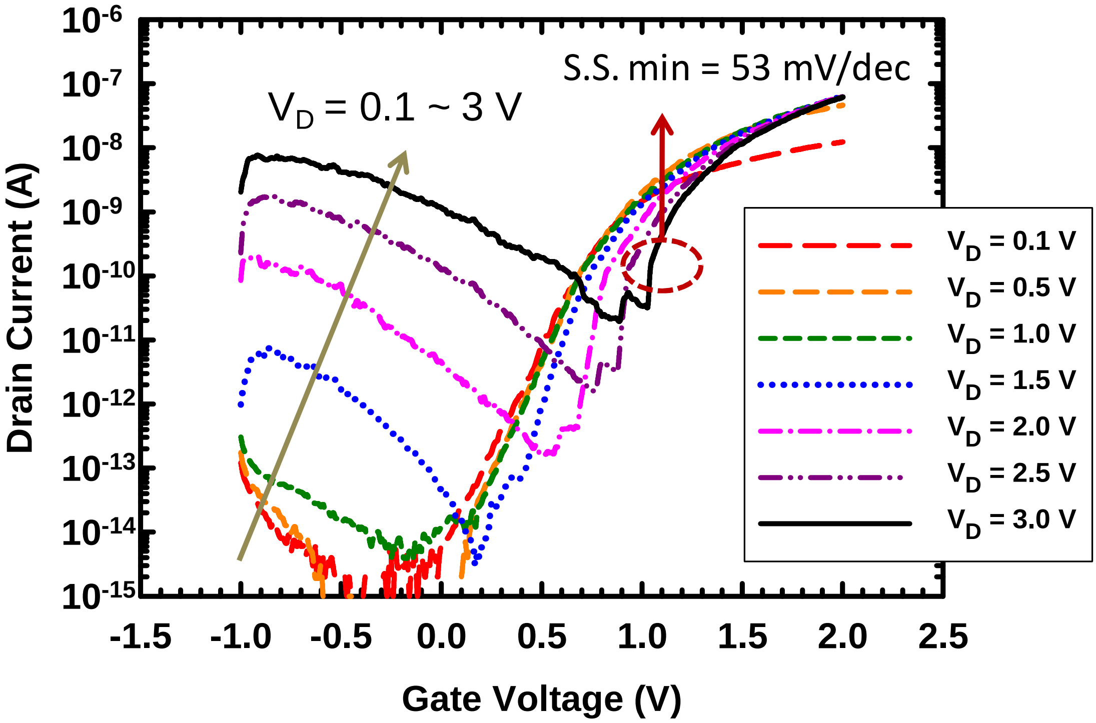


Fig. 3-18 Transfer characteristics with various drain voltages (L= 5 μm).

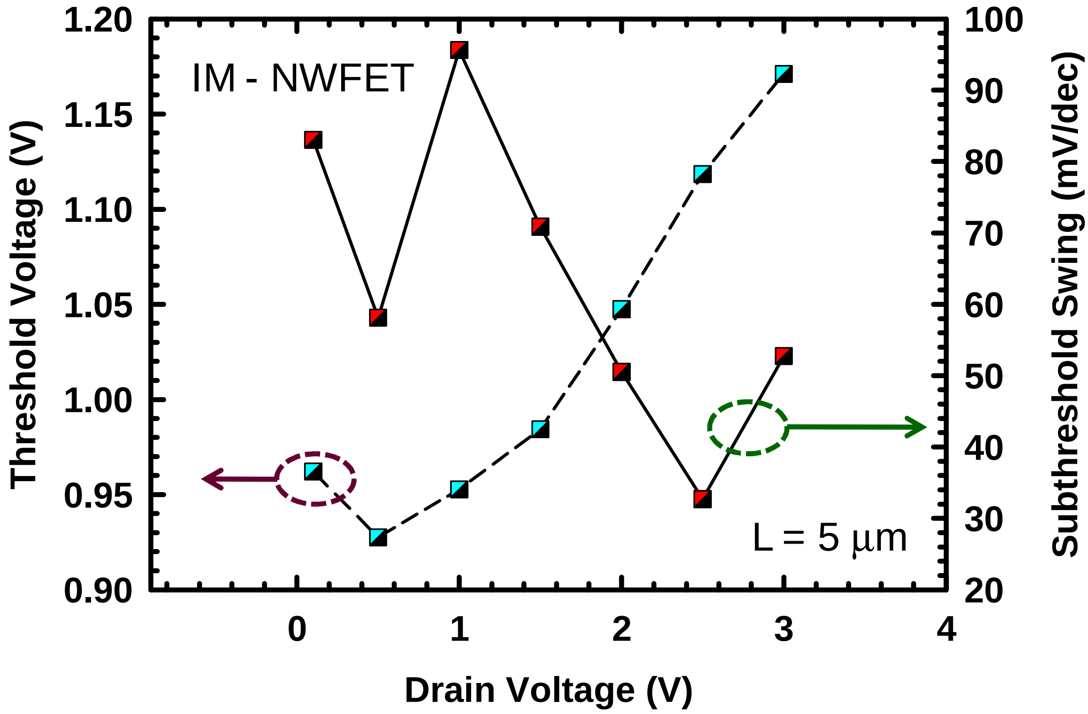


Fig. 3-19 Extracted V_{th} and S.S. from Fig. 3-18 as a function of drain voltage.

Publication List

[1] **Yu-Ling Liou**, Wei-Chen Chen, Horng-Chih Lin, and Tiao-Yuan Huang, "Fabrication and Characterization of Poly-Germanium Nanowire TFTs," *Int. Electron Devices and Materials Symp. (IEDMS)*, Nov. 2010.

[2] Chun-Jung Su, **Yu-Ling Liou**, Tzu-I Tsai, Horng-Chih Lin, Tien-Shen Chao, and Bing-Yue Tsui, "Fabrication and characterization of junctionless poly-Si nanowire devices with gate-all-around structure," submitted to *International Symposium on VLSI-TSA*, 2011.

[3] Chun-Jung Su, Tzu-I Tsai, **Yu-Ling Liou**, Zer-Ming Lin, Horng-Chih Lin, Tien-Sheng Chao, and Bing-Yue Tsui, "Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels," submitted to *IEEE Electron Device Lett.*.