國 立 交 通 大 學

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碩 士 論 文

原子層沉積氧化鋁閘極介電層之砷化鎵通道元件電性研究

A study on the electrical properties of GaAs channel devices with atomic-layer-deposited Al_2O_3 gate dielectric

研　究　生：何 宗 霖

指 導 教 授：簡 昭 欣 教授

中 華 民 國 九 十 九 年 十 月

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國 立 交 通 大 學

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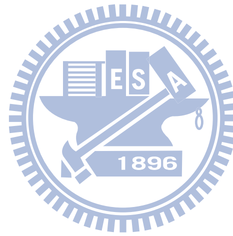
摘要

在此篇文獻中，我們已經最佳化表面處理使得砷化鎵的表面費米能階可成功到達反轉區，也將砷化鎵能隙中間的 D_{it} 值降低至 2E12cm^{-2}V^{-1}。首先，我們先探討利用原子層沉積氧化鋁做為閘極氧化層的電容電性，使用 Berlund 積分公式求出半導體表面費米能階與閘極電壓關係，並且比較不同 D_{it} 在砷化鎵能隙中分佈的萃取方式。其次，我們探討在沉積氧化鋁之前，利用三甲基鋁，還原基板表面的氧化物，其對砷化鎵電容特性的影響。雖然在電容的電性以及 XPS 分析上沒有發現明顯的改善，但是經過 TEM 照片的輔助，計算出閘極氧化層的介電值與等效氧化層厚度有明顯的改進。接著，我們探討不同表面晶向(100)與(111)A 的基板的電容特性。發現利用基板晶向為(111)A 的電容特性具有很大的改進，可以使表面費米能階成功到達反轉區，也將砷化鎵能隙中間的 D_{it} 值降低，我們推測改善是源自於基板表面結構不同所致。針對電容研究的情形，我們利用已經最佳化過後的表面處理去製作出砷化鎵場效應電晶體。

最後我們成功在半絕緣的基板上製作出原子層沉積氧化鋁高介電層之增強式砷化鎵N型場效電晶體。砷化鎵場效電晶體(寬度/長度 = 100 μm/50 μm)的載子遷移率峰值為 15 $cm^2V^{-1}s^{-1}$，而電晶體(寬度/長度 = 100 μm/5 μm)的電流開關比為 4.12E3。雖然成功製作出電晶體，不過元件特性尚未預期的好，我們推測是由於電晶體的源極與汲極的活化步驟的條件沒掌控好所導致。此外，我們也成功製作出通道為砷化銦鎵而源極與汲極為磊晶鍺異質接面的金半場效電晶體，並探討其元件特性。



A study on the electrical properties of GaAs channel devices with atomic-layer-deposited Al_2O_3 gate dielectric

Student：Tsung-Lin He **Advisor : Dr .Chao-Hsin Chien**

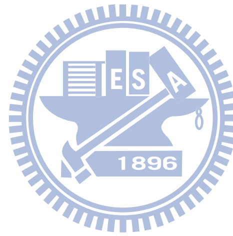
Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University

Abstract

In this thesis, we demonstrated that the Fermi level (E_F) of GaAs on the surface could be adjusted to the level of the inversion mode via optimizing the surface treatment. With the optimized treatment, the interface state density (D_{it}) in the middle of energy bandgap of GaAs could be significantly eliminated to a value of 2E12cm^{-2}V^{-1}. At first, we studied the electrical characteristics on GaAs MOS capacitor with Al_2O_3 gate dielectric formed by atomic-layer-deposition (ALD). We not only utilized Berglund's integration to obtain the relation between surface potential and gate voltage but also compared the D_{it} distribution within energy bandgap by the different extraction methods. Next, we studied the reduction of native oxides on GaAs substrates by trimethylaluminum (TMA) pretreatment before ALD of Al_2O_3 and examined the impact of the electrical characteristics on GaAs MOS capacitors. Although we did not observe anything different on electrical characteristics and XPS analysis,

we found the improvement in the value of *k* and effective oxide thickness after calculation with the TEM image. Then, we studied the electrical characteristics on GaAs MOS capacitors with the different surface orientation of substrates. There was improvement on GaAs MOS capacitors with (111)A surface orientation. The E_F of surface on GaAs could reach inversion region and the value of D_{it} in the middle of energy bandgap was decreased. We presumed that improvement was caused by the different structure of surface on substrate.

Finally, we fabricated E-mode GaAs n-MOSFET on semi-insulator substrate. The electronic mobility we extracted was 15 $cm^2V^{-1}S^{-1}$ and the on/off ratio was 4.12E3; the lower mobility and poor on/off ratio were due to the unsuccessful S/D activation. In addition, we also fabricated InGaAs channel MESFET with Ge S/D and studied electrical characteristics.



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於 新竹國立交通大學

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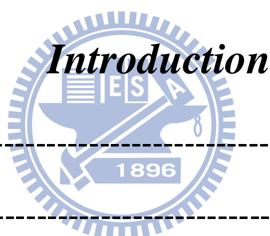

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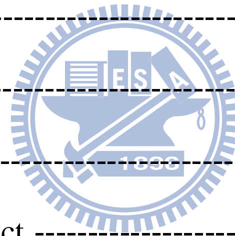

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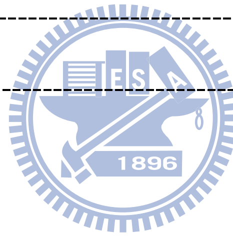

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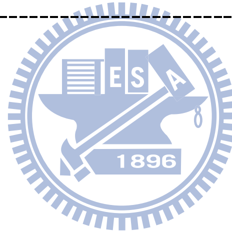

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Chapter 1

Introduction

1.1 General Background

Silicon-based complementary metal-oxide-semiconductor (CMOS) devices with traditional structures are approaching fundamental physical limits. R. Chau, Intel Corporation, had even demonstrated the scaling roadmap of the future in the progress of the Si metal-oxide-semiconductor field-effect transistor (MOSFET), as shown in **Fig. 1.1**. D. Lin, Interuniversity Microelectronics Center (IMEC vzw), reported that one of the several possible future high-performance CMOS architecture [1], as the scheme presented in **Fig. 1.2**. Because of the feature electronic products demand, CMOS devices is required not only high speed and high performance but also less power consumption. For the above requirements, novel device structures and materials must be investigated.

The advantage of Ⅲ-Ⅴ MOSFET over its Si counterpart has long been recognized because the electron mobility in Ⅲ-Ⅴ compound material is five or more times higher than that in Si. Therefore, Ⅲ-Ⅴ MOSFET have application in high-speed electronic devices, like microwave and digital, and its technology promises the advantages of low-power consumption and circuit simplicity.

Silicon-based technology with its devices of 32 nm gate length in production or the smaller in research and development, and with SiO_2 gate oxide thickness close to quantum

tunneling limit of 1.0 nm, has called for alternative high-*k* gate dielectrics. However, Coulomb scattering from charge trapping and the phonon issue related to high-*k* gate dielectric have resulted the degradation in channel mobility. The choices of applicable to gate dielectric on Ⅲ-Ⅴ compound semiconductor will be required the gate oxide does not react with the semiconductor, and the band offset of the gate oxide on the semiconductor substrate is requested to have over 1eV [2].

1.2 Motivation

Ⅲ-Ⅴ compound semiconductors have the advantages which high electron mobility, high breakdown field, low power consumption and rich band gap engineering [3-5]. Thus they are expected to out-perform silicon-based CMOS applications such as high-speed and low-power consumption devices. GaAs is of great importance for scientific understanding of Ⅲ-Ⅴ interfaces and GaAs MOS devices can be used as a sensitive test bed for all dielectric techniques. The treatment or passivation techniques developed on GaAs can naturally be applied to InGaAs or other Ⅲ-Ⅴ compound semiconductors [6].

The major challenge in developing Ⅲ-Ⅴ devices is large interface states density (D_{it}) associated with dielectric/Ⅲ-Ⅴ interface reduces the free carrier density available for transport and can lower the effective channel mobility. In the past few years, for the studies of the dielectric/Ⅲ-Ⅴ interface, especially the (In)GaAs substrate, the several studies have been devoted in intensively searching the high interface quality insulators and efficient passivation methods. Except for SiO_2 and Si_3N_4, $(Gd,Ga)_2O_3$ [7] and atomic-layer-deposited (ALD) Al_2O_3 [8], HfO_2 [9] high-k dielectrics are of particular interest; meanwhile, the sulfur chemical treatment[10], and Si and Ge [11] as the interfacial passivation layers are currently active approaches to protect the surface of III-V semiconductors prior to the dielectric deposition.

1.3 Organization of The Thesis

In **Chapter 2**, we exhibited the common electrical characteristics of MOS capacitors on GaAs substrate and calculated surface potential fluctuation. We also introduced the conductance methods to extract D_{it} distributions within energy bandgap to compare high-low frequency method.

In **Chapter 3**, we studied the reduction of native oxides on GaAs substrates before ALD of Al_2O_3. After trimethylaluminum (TMA) pluses, it is to suppress native oxides on GaAs surface. Subsequently, we deposited ALD-Al_2O_3 as gate dielectric to fabricate MOS capacitors and examined the impact of interface quality on the electrical characteristics; the capacitance-voltage (C−V) characteristics were studied. Besides, we also investigated the electrical properties on the different surface orientation of GaAs substrates. Two different GaAs substrates, p-type (111)A and p-type (100), were also fabricated MOS capacitors and studied the impact of the different surface orientation on the electrical characteristics.

In **Chapter 4**, we utilized the results in optimization of Al_2O_3/GaAs interface to fabricate the enhance-mode GaAs n-MOSFET on semi-insulating GaAs substrate and also fabricated MESFET on InGaAs structures grown by molecular beam epitaxy (MBE). We discussed their I_d-V_g and I_d-V_d electrical characteristics and determined the electronic mobility, source/drain resistance.

In **Chapter 5**, finally, we summarized the experimental results in the thesis and gave the conclusion and suggestions for future work.

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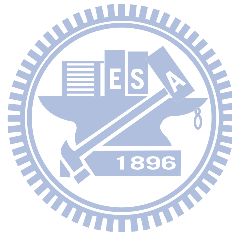


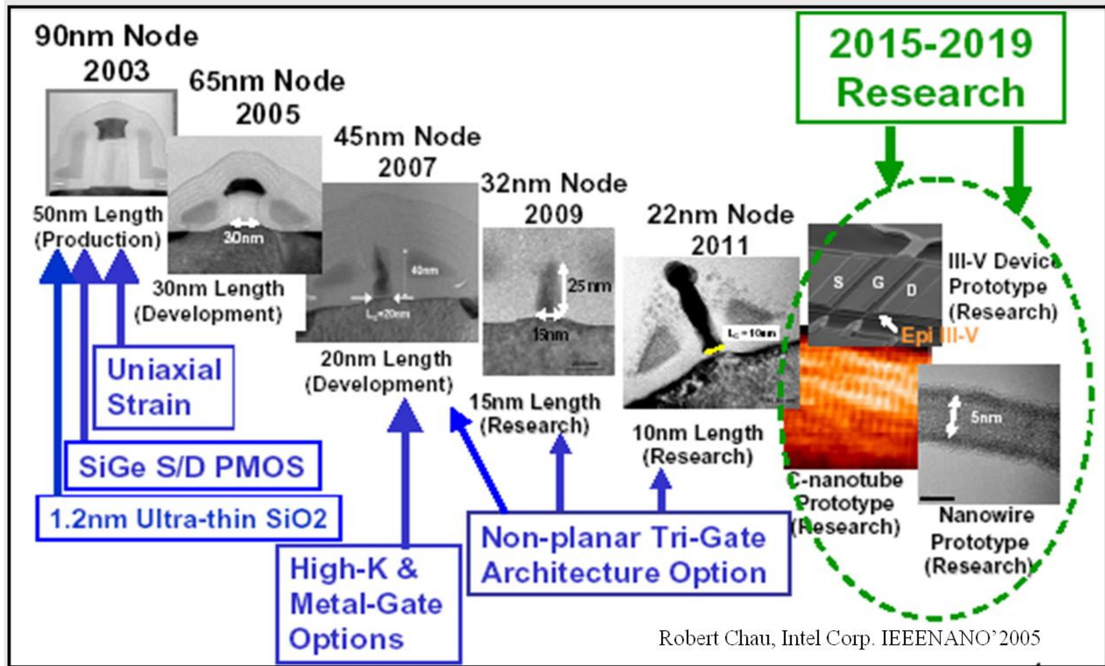


Fig. 1.1 Transistor scaling and research roadmap demonstrated by R. Chau, Intel Corp.

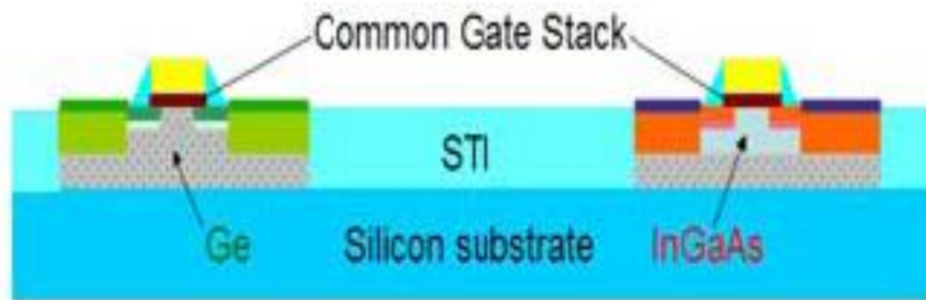
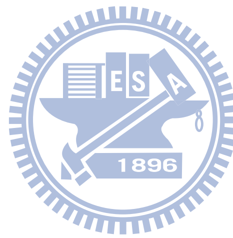


Fig. 1.2 One of the several possible future high-performance CMOS architecture by D. Lin, IMEC.



Chapter 2

Electrical characteristics of GaAs MOS capacitor with Al_2O_3 gate dielectric

2.1. Introduction

Electrical characteristics, such that capacitance-voltage (C-V) and conductance-voltage characteristics (G-V), are regularly used in research and development to understand important parameters of metal-oxide-semiconductor (MOS) capacitor which are like the flatband voltage (V_{FB}), fixed charge (Q_f), effective oxide thickness (EOT) and the quality of dielectric/Ⅲ-V interface. The C-V and G-V characteristics are the methods of choice to extensively study the interfacial characteristics because of the inherent sensitivity of the electrical measurements and the ease-of-use of the involved methods.

Interfacial characteristic is a crucial challenge for realizing Ⅲ-V MOS capacitor. Therefore, it is essential that the quality of interface is evaluated correctly. For example, poor interfacial quality can cause major distortions of the electrical characteristics and result in extensive misconstruction in the interface states density (D_{it}) or other perfunctory parameters extracted from these measurements. The energy bandgap of III-V materials also affect the conductance characteristics in several ways that do not have to be considered in Si-based devices. The correct interpretation of the used electrical characteristics therefore becomes of

paramount importance in III-V technology.

Thorough understanding of the electrical characteristics will give the proper extraction of the MOS capacitor parameters and of the D_{it} distribution within the energy bandgap. In this chapter, the understanding of the behavior of GaAs MOS capacitor with the D_{it} contribution is provided based on firmly established Si/SiO_2 MOS capacitor theory [1-4].

The conductance method, proposed by Nicollian Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [3]. D_{it} of 10^9 $cm^{-2}eV^{-1}$ and lower can be measured. It is also the most complete method, because it yields D_{it} in the depletion and weak inversion portion of the bandgap, the capture cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface traps capture and emission of carriers, is a measure of the interface trap density.

Fig.2.1(a) illustrates the simplified equivalent circuit of MOS capacitor appropriate for the conductance method. It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s, and the interface state capacitance C_{it}. The capture-emission of carriers by D_{it} is a losing process, represented by the resistance R_{it}. It is convenient to replace the circuit of **Fig. 2.1(a)** by **Fig. 2.1(b)**, where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.1}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.2}$$

where $C_{it} = q^2D_{it}$ and $\tau_{it} = R_{it}C_{it}$, the characteristic emission frequencies of trapped charge carriers, given by

$$\tau_{it} = \left[\upsilon_{th}\sigma_P N_A \exp(-q\varphi_s/kT)\right]^{-1} \tag{2.3}$$

The equations are for interface state with a single energy level in the energy bandgap.

Interface state at the dielectric/substrate interface, however, are continuously distributed in energy throughout the energy bandgap. Capture and emission occurs primarily by interface state located within a few kT/q nearby the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega}=\frac{qD_{it}}{2\omega\tau_{it}}\ln[1+(\omega\tau_{it})^2] \tag{2.4}$$

The conductance is measured as a function of the frequency and ploted as G_p/ω versus ω. G_p/ω has a maximum at $\omega \approx 2/\tau_{it}$ and at that maximum $D_{it} = 2.5G_p/q\omega$. Hence we could determine D_{it} from the G_p/ω versus ω and determine τ_{it} from ω at the peak conductance location on the ω-axis.

An approximate expression giving the interface state density in term of the measured maximum conductance is

$$D_{it}\approx\frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \tag{2.5}$$

Capacitance meters generally assume the device to consist of the parallel C_m-G_m combination in **Fig. 2.1(c)**. A circuit comparison of **Fig. 2.1(b)** to **Fig. 2.1(c)** gives G_p/ω in term of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega}=\frac{\omega G_m C_{ox}^2}{G_m^2+\omega^2(C_{ox}-C_m)^2} \tag{2.6}$$

In the addition, the device has series resistance which has so far been neglected. Series resistance is a common parasitic affecting C-V and G-V measurement of MOS capacitor. The series resistance is due to the resistance of the bulk semiconductor material and/or the gate electrode material, as well as the contact resistances. The more complete circuit is shown in **Fig. 2.1(d)** and G_t represents the tunnel conductance and r_s represents the series resistance. Therefore, **Eq. (2.6)** becomes [4]

$$\frac{G_p}{\omega}=\frac{\omega(G_c-G_t)C_{ox}^2}{G_c^2+\omega^2(C_{ox}-C_c)^2} \tag{2.7}$$

where

$$C_c = \frac{C_m}{(1-r_s G_m)^2 + (\omega r_s C_m)^2} \quad (2.8)$$

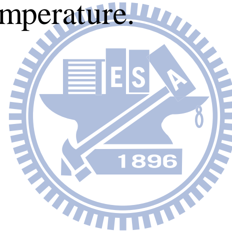
$$G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1} \quad (2.9)$$

C_m and G_m are the measured capacitance and conductance. The series resistance is determined by biasing the MOS capacitor into accumulation according to [6]

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \quad (2.10)$$

where G_{ma} and C_{ma} are the measured conductance and capacitance in accumulation.

From **Eq.(2.3)**, we assumed the capture cross section $\sigma = 1\times10^{-15}$ cm^2 and plotted the characteristic emission frequencies of trapped charge carriers in GaAs at the different temperature as a function of the position of the trap in the energy bandgap, as presented in **Fig. 2.2**. In order to get a good continuous distribution of D_{it} , we have to measure C-V curve with multi- frequency at the different temperature.



2.2 Sample Preparation

MOS capacitor sample was prepared on high Si-doped (p-type, ~ 5×10^{17} cm^{-3}) GaAs (100) substrates. At first, the GaAs was rinsed in the diluted HCl (HCl : H_2O = 1 : 3) solution for 3 min, followed by rinsed in deionized (D.I.) water for 5 min. Then, the GaAs was rinsed in the diluted NH_4OH (NH_4OH : H_2O = 1 : 10) solution for 10 min, followed by rinsed in D.I. water for 5 min. Third, the GaAs was rinsed in the $(NH_4)_2S$ solution for 10 min, followed by rinsed in D.I. water for 5 min. After surface cleaning, thermal desorbed native oxide on the surface of substrate at 350 ℃ for 10 min and then the Al_2O_3 gate dielectric was deposited by atonic-layer-deposition (ALD) at 250 ℃, followed by post deposition annealing (PDA) at 600 ℃ for 15 s in a N_2 ambient. Thermal evaporated 400 nm Al was patterned as gate electrodes through the lithography. Finally, Ti/Pt/Au (5 nm/30 nm/180 nm) was

deposited by e-beam evaporator as backside contact. The complete process flow was shown in **Fig. 2.3**. The electrical characteristics of Al/Al_2O_3/p-GaAs/TiPtAu MOS capacitors were measured using an HP4284 and HP4200, respectively.

2.3 Results and Discussion

2.3.1 Multi-Frequency C-V of GaAs MOS Capacitor

In the beginning, exhibiting the basic properties of the GaAs MOS capacitor, C-V curves, include different measurement temperatures at 25℃ and 125℃, as shown in **Fig. 2.4 (a)** and **(b)**, respectively. The frequency and temperature dependent C-V characteristic was observed obviously because of D_{it} contribution which is distributed within the energy bandgap [6]. Besides, the quasi-static C-V was also shown in **Fig. 2.5** and calculating the surface potential, ϕ_s, is a function of gate voltage. Berglund proposed [7]

$$\phi_s = \int_{V_{G1}}^{V_{G2}} \left(1 - C_{QSCV} / C_{ox} \right) dV_G + \Delta \qquad (2.11)$$

where C_{QSCV} is the quasi-static C-V curve as a function of gate voltage. Integration from $V_{G1} = V_{FB}$ makes $\triangle = 0$, because band bending is zero at faltband. Integration from V_{FB} to accumulation and from V_{FB} to inversion gives the surface potential across the energy bandgap range. **Fig. 2.6** illustrates the calculated result, surface potential versus gate voltage (ϕ_s-V_G).

Utilizing high-frequency C-V curve and quasi-static C-V to extract D_{it} as a function of gate voltage by high-low frequency method is described in **Eq. (2.12)** [8].

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{C_{QS}/C_{ox}}{1 - C_{QS}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \qquad (2.12)$$

where the value of C_{ox} is defined on accumulation of quasi-static C-V. After D_{it} extraction by high-low frequency method and x-axis conversion by surface potential as function of gate

voltage, result in D_{it} distribution within energy bandgap was displayed in **Fig. 2.7**.

2.3.2 Conductance Method Application of GaAs MOS Capacitor

Calculating the series resistance by **Eq. (2.10)** after measurement at 25℃. The result of series resistance extraction was shown in **Fig. 2.8**, and fitting the series resistance value, r_s = 122 Ω. Next, correction of C_c and G_c by **Eq. (2.8)** and **Eq. (2.9)**, respectively, and the plotting the G_p/ω versus frequency by using **Eq. (2.7)**. **Fig. 2.9 (a)** and **(b)** displayed G_p/ω as a function of frequency through the correction of series resistance and calculation by conductance method. As same as before, plotting the G_p/ω as a function of frequency curve which data was measured at 125℃ and the result was shown in **Fig. 2.9 (c)** and **(d)**. Finally, getting the peak of G_p/ω-frequency curve and determining the D_{it} by using **Eq. (2.5)**. **Fig. 2.10** illustrates the D_{it} distribution within energy bandgap as derived from measurement on GaAs MOS capacitor with ALD-Al_2O_3 gate dielectric.

2.3.3 Comparison of D_{it} Extraction

Fig. 2.11 presented the comparison of D_{it} extraction between high-low frequency method and conductance method on GaAs MOS capacitor with ALD-Al_2O_3 gate dielectric, and two D_{it} distributions from the different extraction methods have the same trends which indicate that the high value of D_{it} was close to mid-gap. The value of D_{it} from high-low frequency method is overestimated due to some detail; it may be the series resistance effect which has been neglected. Moreover, for high-frequency curve of high-low frequency method, the measurement must be sufficiently high to interface states do not respond, but for MOS capacitors with high D_{it} there will be some response due to interface traps. The conductance

method have the simplified but plentiful circuit model, combining multi-frequency C-V and elevated-temperature measurement enhance the sensitivity near mid-gap allowing the detection of trap energy levels [9].

2.4 Summary

After fabricating a MOS capacitor on GaAs substrates, we could have a standard operation process to extract the electrical characteristic of GaAs MOS capacitors with ALD-Al_2O_3 gate dielectric. At the first, we measured quasi-static C-V and the multi-frequencies of C-V at the different temperature conditions. Next, we calculated the surface potential as a function of gate voltage by Berglund's integration. We can realize the fluctuation of Fermi level (E_F) on the surface of GaAs substrate, and judge it weather reaches the inversion portion of the band gap or not. After D_{it} extraction by conductance method, we can accurately determine D_{it} distribution across the energy bandgap. Finally, utilizing the electrical characteristics of the GaAs MOS capacitor to decide the experimental condition is suitable in manufacture procedure of enhance-mode GaAs n-MOSFET.

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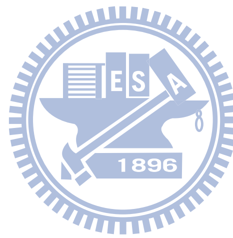


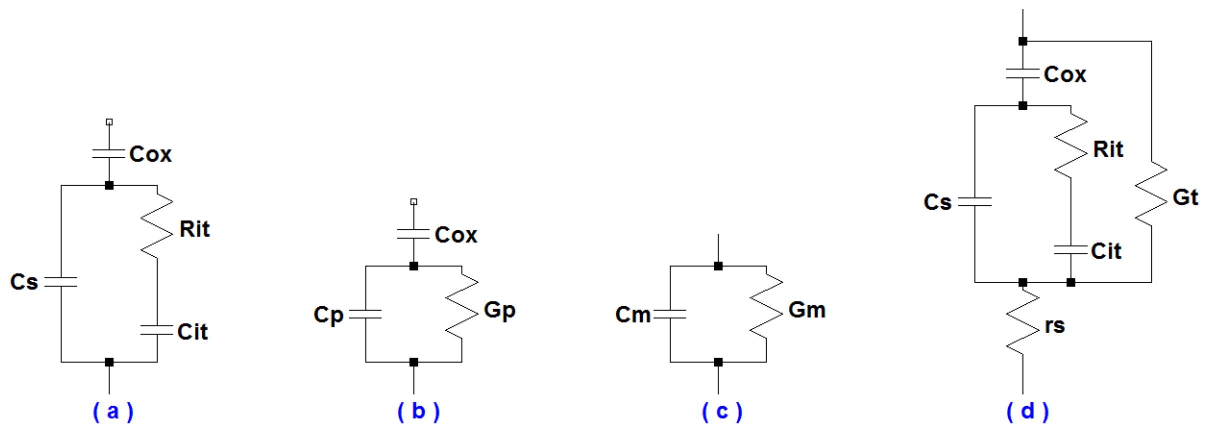


Fig. 2.1 Equivalent circuits for conductance measurements; (a) MOS capacitor, (b) simplified circuit, (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t.

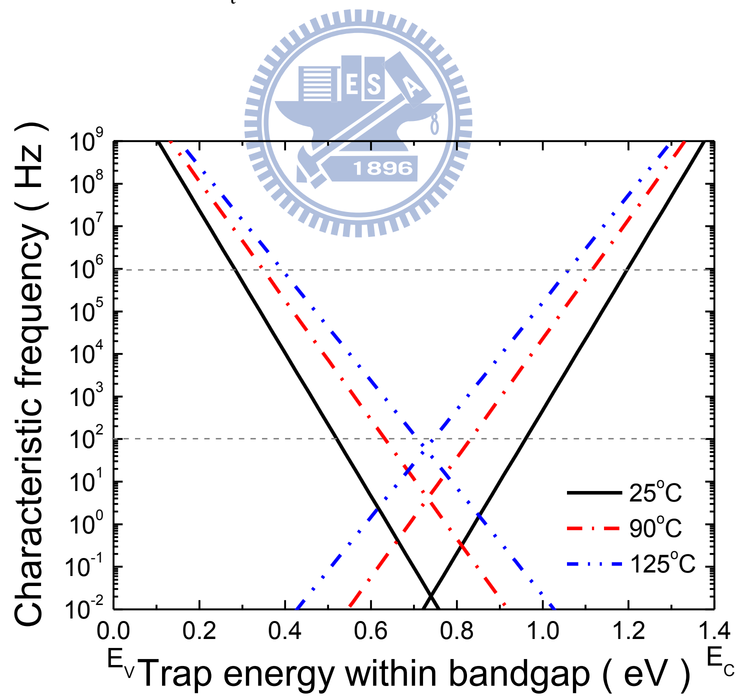


Fig. 2.2 Characteristic emission frequencies of trapped charge carriers in GaAs at the different temperatures.

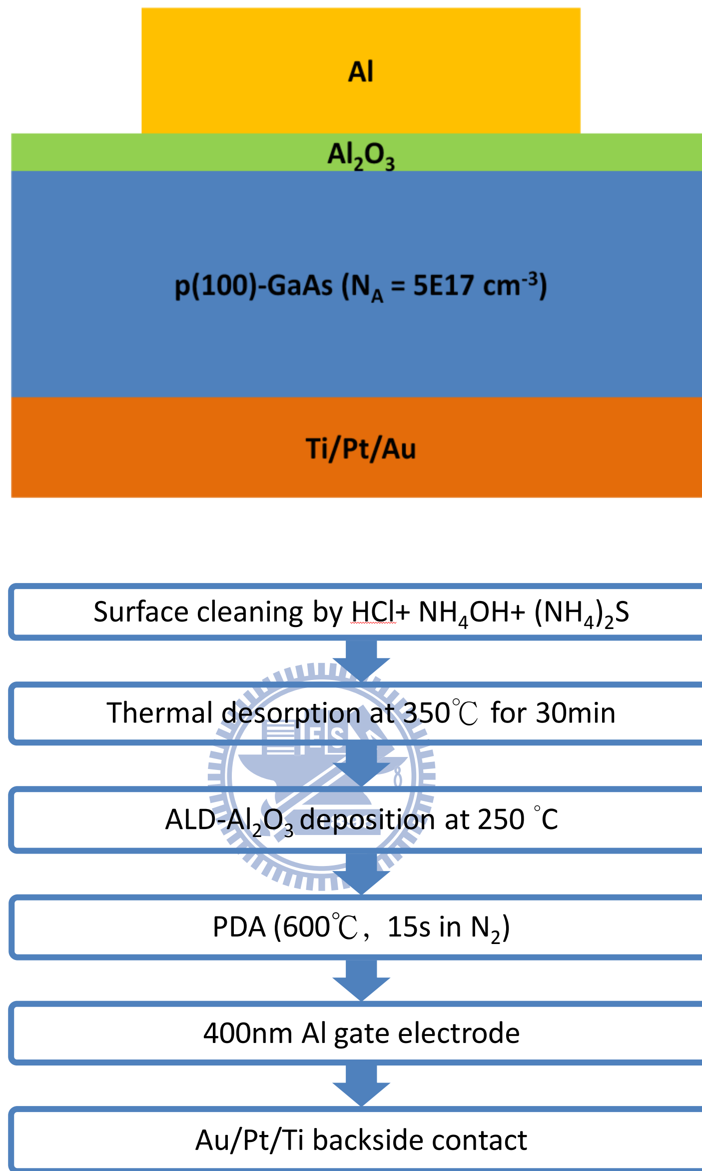


Fig. 2.3 The structure and process flow of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor.

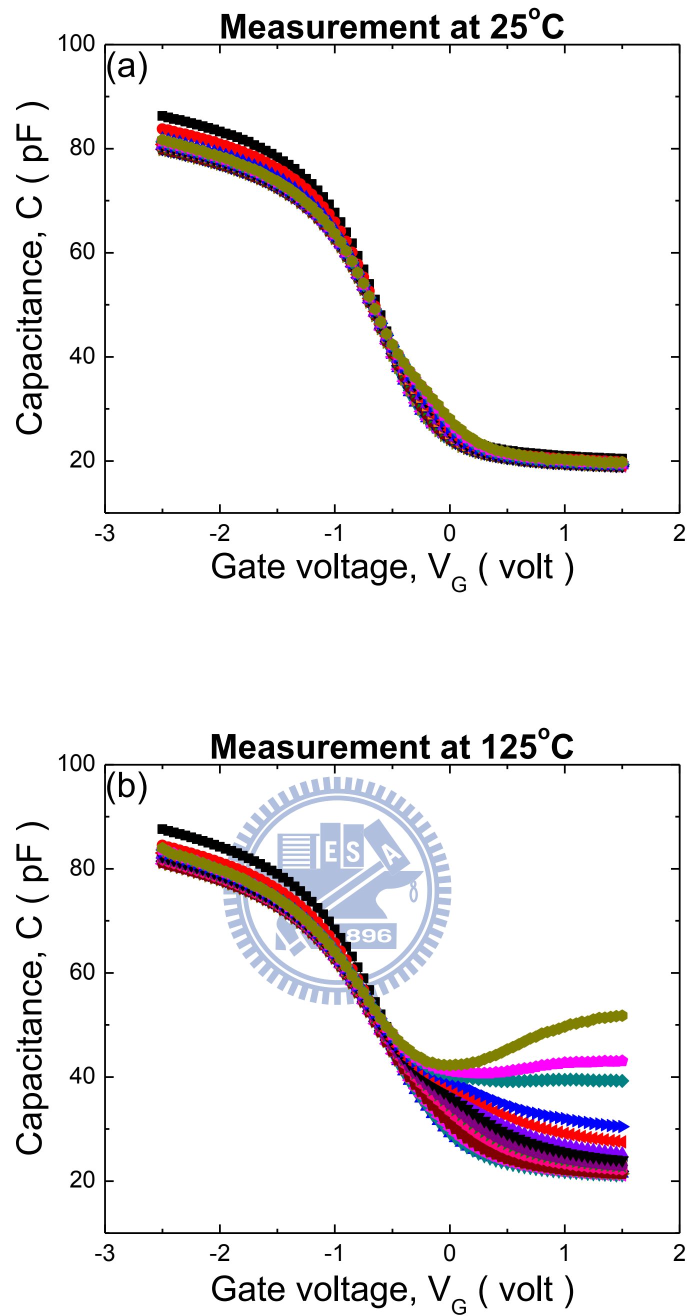


Fig. 2.4 Multi-frequency C-V curve of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor at (a) 25℃, (b) 125℃ measurement condition.

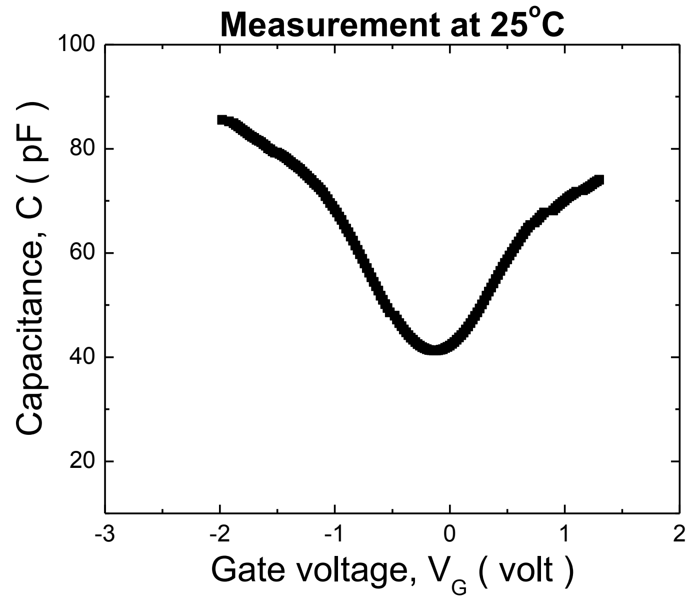


Fig. 2.5 Quasi-static C-V curve of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor.

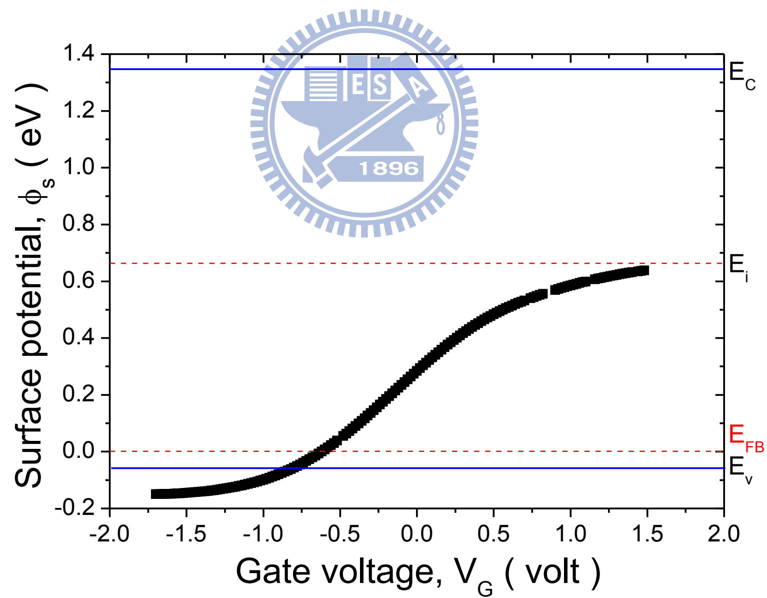


Fig. 2.6 Surface potential versus gate voltage of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor.

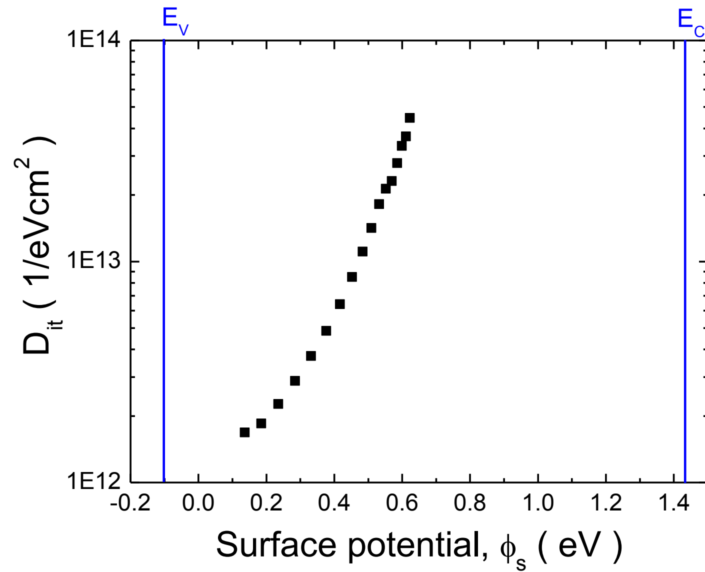


Fig. 2.7 D_{it} distribution by high-low frequency method of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor.

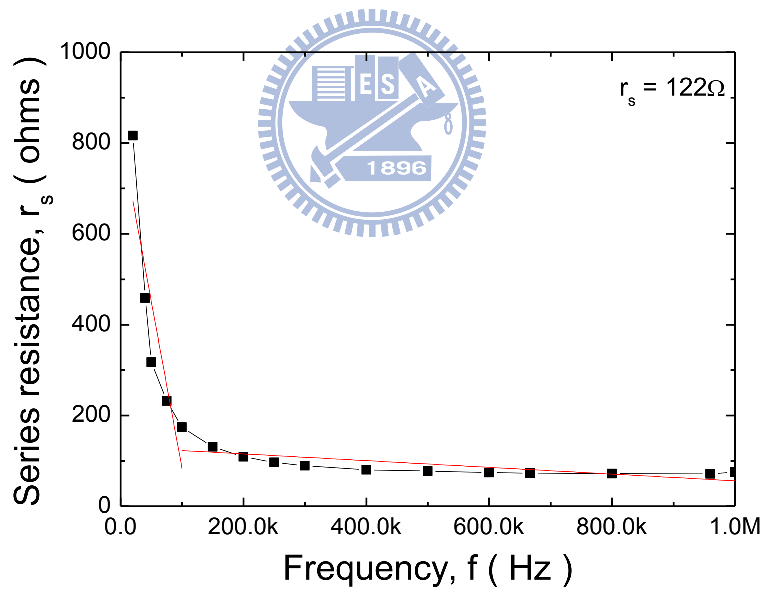


Fig. 2.8 Series resistance extraction of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor.

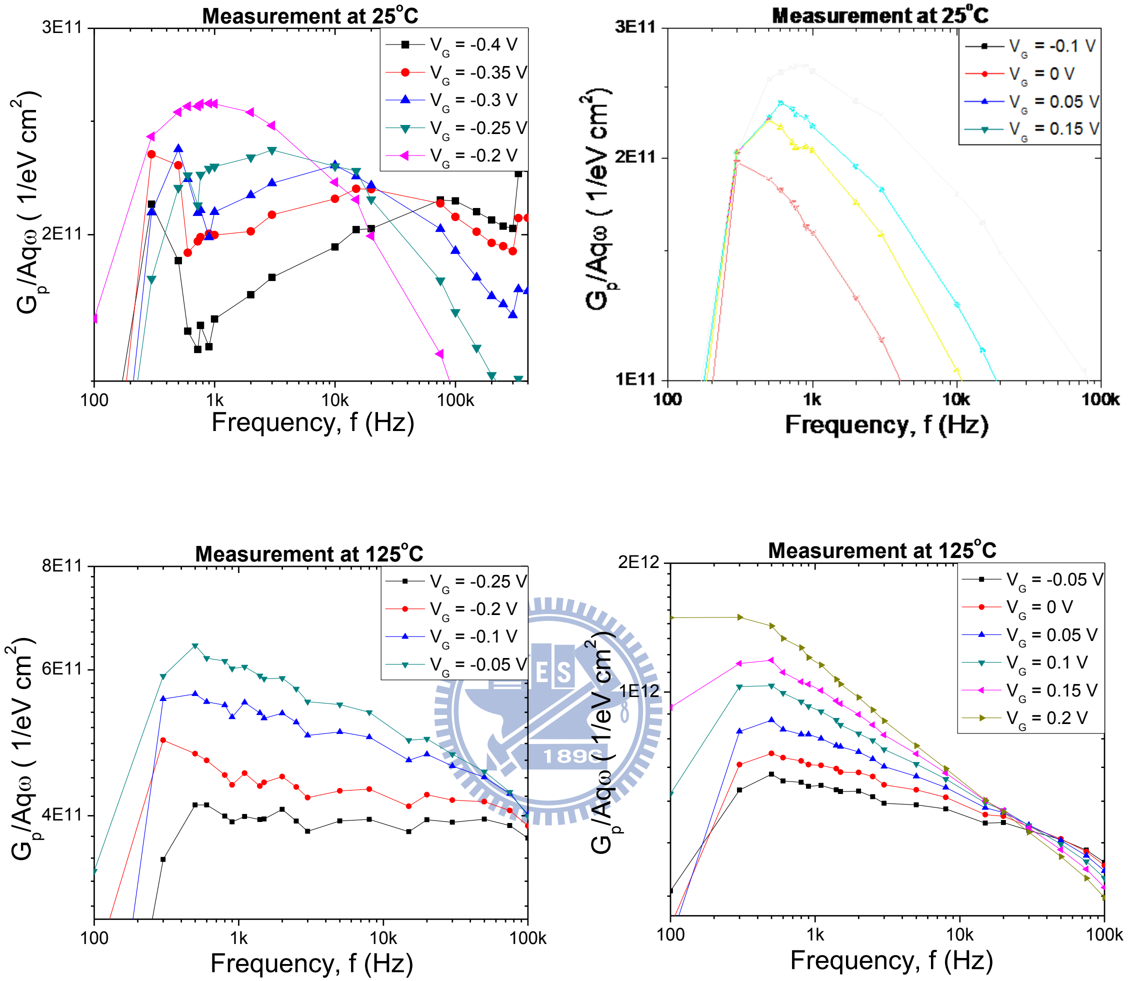


Fig. 2.9 G_p/ω as a function of frequency (a) and (b) at 25℃ measurement condition; (c) and (d) at 125℃ measurement condition.

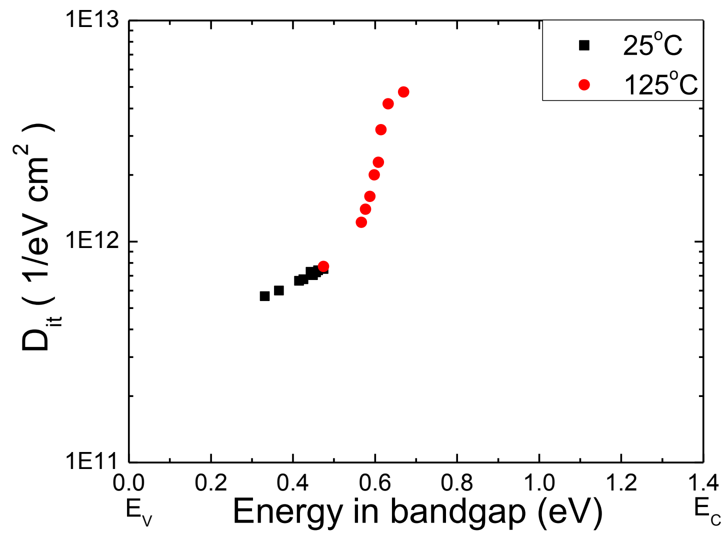


Fig. 2.10 D_{it} distribution by conductance methods of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitor.

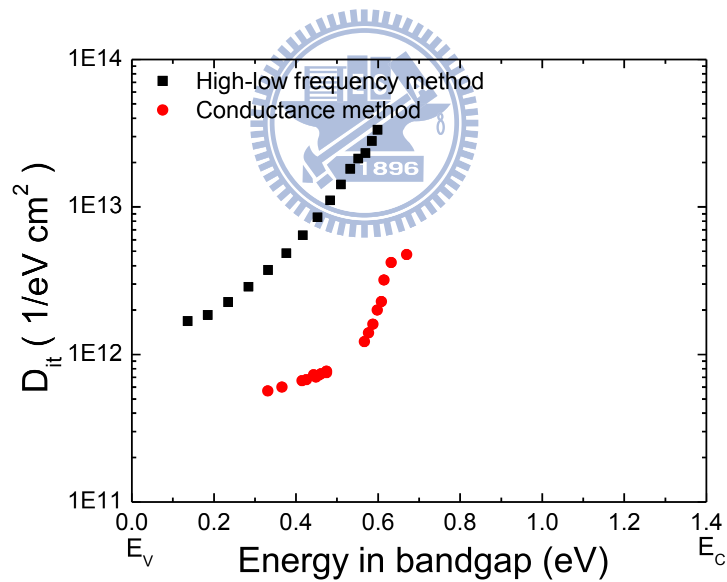


Fig. 2.11 Comparison of D_{it} extractions by high-low frequency method and conductance

Chapter 3

Optimization of Al_2O_3 /GaAs interface with MOS capacitor

3.1 Introduction

Today, in the semiconductor industry, Ⅲ-Ⅴ compound materials are used widely in such applications as optoelectronic devices, photodiodes, high-electron-mobility transistors (HEMTs), and other high-frequency devices. In order to obtain high-speed and low-power Ⅲ-Ⅴ metal-oxide-semiconductor (MOS) logic devices, a high quality interface between insulator and Ⅲ-Ⅴ is imperative. A large interface states density (D_{it}) within the Ⅲ-Ⅴ energy bandgap was caused by the native surface oxides is identified as a serious device challenge for Ⅲ-Ⅴ based devices [1-2]. Studies into competitive insulators on Ⅲ-Ⅴ compound semiconductors and efficient passivation methods have been performed for more than four decades; the poor quality of the insulator/substrate interface has been the prime obstacle hindering the realization of III-V MOS devices.

As mentioned in the chapter 1, GaAs is of great importance for scientific understanding of Ⅲ-Ⅴ compound material interfaces and GaAs MOS devices can be used as a sensitive test bed for all dielectric techniques. The treatment before insulator deposition or passivation layers between insulator and substrate techniques are developed on GaAs can naturally be applied to (In)GaAs or other Ⅲ-Ⅴ compound semiconductors [3]. Excluding SiO_2 and Si_3N_4 ,

$(Gd,Ga)_2O_3$, and HfO_2 high-*k* dielectrics are also potential candidates for use on Ⅲ-V compound substrates. One route of obtaining a native oxide-free interface that has attracted the attention of researchers is the “self-cleaning” [4-7]; in which the native oxides on GaAs get a reduction during the atomic layer deposition (ALD) of HfO_2 or Al_2O_3 due to ALD precursor chemistry, tetrakis(ethylmethylamino)hafnium (TEMAH, $Hf[N(C_2H_5)(CH_3)]_4$) and trimethylaluminum (TMA, $Al(CH_3)_3$), separately. The self-cleaning during the ALD and the using of ultra-thin Si or Ge interfacial passivation layers are both practical techniques for improving the interface between insulator and Ⅲ-V compound material. The pretreatment on GaAs by the ALD precursor prior to deposition of the gate dielectric has been reviewed comprehensively; the improvement in the device performance depends strongly on the ALD precursor pretreatment procedure. The in situ or ex situ deposition of several Si or Ge monolayers on GaAs can reduce the D_{it} to ca. 1×10^{10} –1×10^{11} cm^{-2} eV^{-1} [8-9]; this passivation technique has received renewed interest in recent years. Besides, the different crystalline surfaces of GaAs substrates were found that a much higher driving current on GaAs(111)A n-metal-oxide-semiconductor field-effect transistor (MOSFET). This experimental result conclusively demonstrated that Fermi-level (E_F) pinning is not an intrinsic property of GaAs, but is orientation dependent [10].

Subsequent thermal annealing can further improve the quality of insulator films deposited on GaAs [11]. Meanwhile, during high temperature processing it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides; these processes lead directly to electrical deterioration in GaAs MOS capacitors [12]. The impact of rapid thermal annealing (RTA) on the properties of various high-*k*/GaAs structures has been studied previously [13]. However, the correlations between these thermal reactions and the MOS performance have not been established in detail. In this study, we examined the electrical characteristics of

ALD-Al_2O_3 thin films deposited on an ALD precursor treated GaAs surface and then monitored the impact of postdeposition annealing (PDA) process. ALD is an ultrathin film deposition technique based on sequences of self-limiting surface reactions, which enables thickness control on the atomic scale. Unlike CVD, there is less need of reactant flux homogeneity, which gives large area capability, excellent conformality and reproducibility. Other advantages of ALD are the wide range of film materials available and high density. Also, lower deposition temperature can be used in order not to affect sensitive substrates.

The deposition mechanism of ALD is like chemical vapor deposition (CVD). We introduce the unique feature of the step-by-step deposition in ALD by using a general example of Al_2O_3 film deposition. It is well known that Al_2O_3 films can be grown by using alternating pulses of $Al(CH_3)_3$ (TMA, the aluminum precursor) and H_2O (the oxygen precursor) in the presence of N_2 carrier gas flow. Its mechanism procedures for one deposition cycle are illustrated in **Fig. 3.1**. At first, TMA is fed into the reactor and react with the OH bond on the GaAs substrate. Second, the reactor is purged with pure N_2 gas to clean out residual TMA. Third, H_2O is purged into the reactor and forms Al_2O_3 on surface. Finally, the reactor is purged with pure N_2 gas again to clean out residual H_2O.

3.2 Experimental Procedures

MOS capacitor structures were fabricated on high Si-doped (p-type, ~ 5×10^{17} cm^{-3}) GaAs substrates. At first, the sample was rinsed in the diluted HCl (HCl : H_2O = 1 : 3) solution for 3 min, followed by rinsed in deionized (D.I.) water for 5 min. Second, the sample was rinsed in the diluted NH_4OH (NH_4OH : H_2O = 1 : 10) solution for 10 min, followed by rinsed in D.I. water for 5 min. Third, the sample was rinsed in the $(NH_4)_2S$ solution for 10 min, followed by rinsed in D.I. water for 5 min. After surface cleaning, the sample was loading

into the ALD chamber, followed by surface pretreatment with TMA 20 cycles pulse at 250 ℃. Next, the Al_2O_3 gate dielectric was deposited at 250 ℃, followed by PDA at 600 ℃ for 15 s in an N_2 ambient. Thermal evaporated 400 nm Al was patterned as gate electrodes through the lithography. Finally, Ti/Pt/Au (5 nm/30 nm/180 nm) was deposited by e-beam evaporator as backside contact. The complete process flow was shown in **Fig. 3.2**, and **Tab. 3.1** shows experimental conditions. The electrical characteristics of Al/Al_2O_3/p-GaAs/TiPtAu MOS capacitors were measured using an HP4284 and HP4200, respectively.

Surface orientation	Surface pretreatment	ALD cycle	PDA
(100)	None	Al_2O_3 60 cycles at 250℃	As-deposited
			600℃ 15s in N_2
	TMA pulse 20 cycles at 250℃		As-deposited
			600℃ 15s in N_2
(100)	TMA pulse 20 cycles at 250℃	Al_2O_3 150 cycles at 250℃	As-deposited
			600℃ 15s in N_2
(111)A			As-deposited
			600℃ 15s in N_2

Tab. 3.1 The experimental condition of Si-doped (p-type, ~ 5×10^{17} cm^{-3}) GaAs MOS capacitors were in this study.

3.3 Results and Discussion

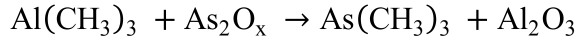
3.3.1 TMA Effect

Fig. 3.3 (a) and **(b)** presented the frequency-dependent capacitance-voltage (C-V) curves of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors with and without TMA pretreatment. According to Berglund's integration as mentioned in the chapter 2, calculating the relation of surface potential fluctuation and gate voltage, and the result of TMA effect was shown in **Fig. 3.4**. The two curves revealed that the surface potential cannot reach conductance band (E_c) edge just only saturated near mid-gap; illustrated that the surface potential are pinned at mid-gap and gate voltage cannot product inversion charge, electron. Besides, in **Fig. 3.5**, utilizing high-low frequency method to extract the D_{it} distribution and comparing the trend of distribution within energy bandgap. In the **Fig. 3.4**, finding that surface potential fluctuation saturated at 0.7 eV above valance band (E_v) of GaAs, and this was corresponding to the $D_{it} \gg 1\times10^{13}$ $eV^{-1}cm^{-2}$ in the **Fig. 3.5**.

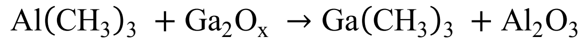
Fig. 3.6 displayed the respective As $2p_{3/2}$ photoemission spectra of Al_2O_3/GaAs interface with/without TMA pretreatment and after wet cleaning. As the figure represents, we cannot found clearly that native oxide, As_2O_3 and As_2O_5, change between with and without TMA pretreatment obviously. This result of XPS analysis may be caused by some reasons, (a) the majority of self-cleaning effect by ALD reactions of TMA occurs following the initial TMA pulse [14]; (b) the XPS spectra analyzer with a nonmonochromatic Mg $K\alpha$ x-ray source ($h\nu$=1253.6 eV), the energy source is too small that not finding the obvious reactions on the Al_2O_3/GaAs interface after additional 20-cycles TMA pulse.

Fig. 3.7 (a) and **(b)** represented the cross-section transmission electron microscopy (TEM) image of Al/Al_2O_3/GaAs MOS capacitors with and without TMA pretreatment,

respectively. The interlayer between Al_2O_3 and Al is native oxide which is product after ligand exchange mechanism. During ALD process, the $Al(CH_3)_3$ was purged into the deposition chamber, it would react with the native oxides, i.e., As_2O_x and Ga_2O_x, and formed volatile products of $As(CH_3)_3$ and $Ga(CH_3)_3$, as shown by the following reactions.



$$Al(CH_3)_3 + As_2O_x \rightarrow As(CH_3)_3 + Al_2O_3$$



$$Al(CH_3)_3 + Ga_2O_x \rightarrow Ga(CH_3)_3 + Al_2O_3$$

The volatile products can be purged away in the next process of N_2 purge. However, the volatility products may not be sufficiently high to be completely purged away by N_2 purge, the remainder would be oxidized again in the followed pulse of water vapor and caused the contamination of As_2O_x and Ga_2O_x in the top portion of Al_2O_3, as observed in the **Fig. 3.7**. Hence, the interlayer between Al_2O_3 and Al can cause that lowering the value of k of the gate dielectric and raising the value of effective oxide thickness (EOT). Comparing **Fig. 3.7 (a)** and **(b)**, the sample with TMA pretreatment has the larger value of k and the smaller value of EOT than the sample without TMA pretreatment.

3.3.2 PDA Effect

Fig. 3.8 presented the frequency-dependent C-V curves of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors with and without PDA. The sample with TMA pretreatment and PDA displayed a higher oxide capacitance accompanying a decreased C-V frequency dispersion, relative to as-deposited sample. **Fig. 3.9** and **Fig. 3.10** displayed the surface potential as function of gate voltage and D_{it} distribution within bandgap by high-low frequency method, respectively. These results were indicative of the slight abatement of the E_F pinning effect in the capacitor properties; in other words, modulation of the carrier manipulation was enhanced.

In **Fig. 3.11**, using the conductance method by **Eq. (2.5)** to **Eq. (2.10)** as mentioned in the chapter 2 to extract accurately the D_{it} distribution, and the sample with TMA pretreatment and PDA had the lower value of D_{it}. Although not finding any reaction after the XPS analysis, we suggest that these As oxides (As_2O_3 and As_2O_5) convert to Ga_2O_3 by thermal conversion through PDA at 600 ℃ for 15 s in N_2 ambient [15]. However, the electrical characteristics was improved, there was still very high value of D_{it} ($D_{it} \gg 1\times10^{13}$ $eV^{-1}cm^{-2}$) at about 0.7 eV above E_v of GaAs by the result of high-low frequency method.

3.3.3 Surface Orientation Effect

Now that, having the better result that the GaAs MOS capacitor with TMA pretreatment and PDA process. We will study the electrical characteristic on GaAs (100) and (111)A MOS capacitors– two different crystalline surfaces with ALD-Al_2O_3 gate dielectric.

Fig. 3.12 illustrated the frequency-dependent C-V curves of Al/Al_2O_3/p-GaAs (100) and (111)A/TiPtAu MOS capacitors. Apparently, we could observe the less C-V stretch out behavior with the hump emerged in depletion region for p-GaAs (111)A sample, indicating the existence of a large D_{it} at the dielectric/substrate interface for p-GaAs (100) MOS capacitor. Not only utilizing the Berglund's integration to calculate the surface potential fluctuation but also extracting D_{it} distribution by high-low frequency method as shown in **Fig. 3.13** and **Fig. 3.14**, respectively. As the figures represented, the surface potential fluctuation was improved very much and it could approach the conductance band, in other words, the E_F not be pinned at mid-gap as the same as the before. This result was also verified by high-low frequency method, the value of D_{it} is about 2×10^{12} $eV^{-1}cm^{-2}$ at mid-gap.

Since GaAs (111)A is a pure Ga polar surface in contrast to (100) Ga-As nonpolar surface, we presumed that the improvement of electrical characteristics is caused by the

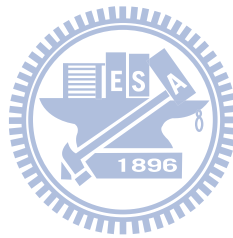
different surface structure. One, As-S chemical bonds were broken at a relatively low temperature, approximately 150-250 ℃, whereas adsorption of sulfur from the surface, through breaking Ga-S bonds occurs above 500 ℃. At 250 ℃ ALD process, only Ga-S bonds remained stable, whereas As-S bonds were possibly reduced into the metallic As. So that, we could avoid the more arsenic oxide formation, which is believed that As-O will lead to high interface state density locate at the lower half of energy bandgap within GaAs.

Two, these electrical characteristics of experimental results may be explained by the following proposed empirical model as illustrated in **Fig. 3.15**. The empirical model is based on the unified disorder induced gap state (DIGS) model proposed by Hasegawa and Ohno in 1986 [15], which explains the striking correlation between the energy location E_0 for the minimum interface state density at the insulator/semiconductor interface. The central concept is that there is an energy level called trap neutral level E_0 at the insulator/GaAs interface, above which the trap states are of acceptor type or electron traps and below which are of donor type or hole traps. It is also explained that the GaAs (111)A sample have the better electrical characteristics, including the ability of surface potential fluctuation and the lower value of D_{it} at mid-gap of GaAs.

3.4 Summary

In this chapter, we studied sequentially self-clean effect by additional TMA pulse before Al_2O_3 deposition, PDA effect and surface orientation of substrate effect by analyzing the electrical characteristics of GaAs MOS capacitors. Utilizing the extraction of electrical characteristics as mentioned in the chapter 2, we demonstrated that the gate dielectric obtains the larger value of *k* and the smaller value of EOT by additional TMA pulse. After PDA process, the electrical characteristic of GaAs MOS capacitor was improved. Finally, we

investigated GaAs (100) and (111)A surface orientation by MOS capacitors. GaAs (111)A had the best surface potential fluctuation and the lower value of D_{it} at mid-gap, we proposed the chemical reactions on the surface of substrate during ALD and cited DISG model from reference to explain the improvement of electrical characteristics.



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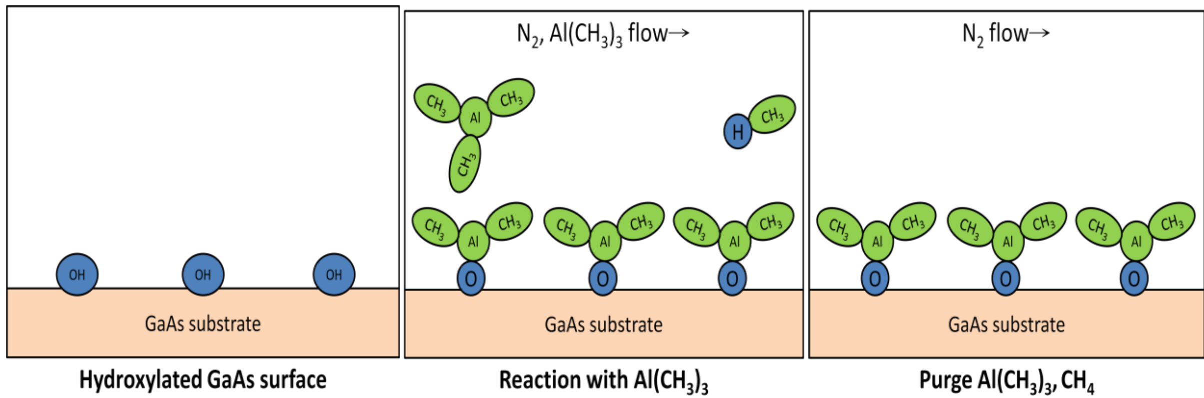
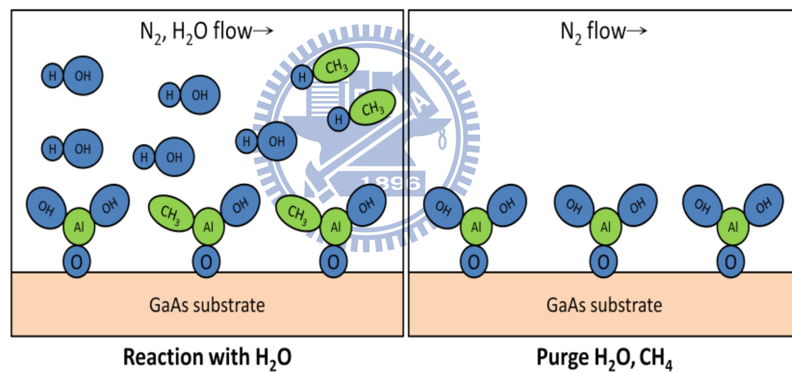




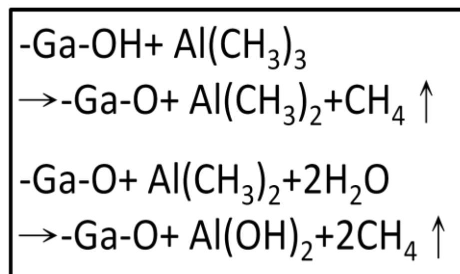


Fig. 3.1 Atomic layer deposition (ALD)-Al_2O_3 mechanism and chemical reaction.

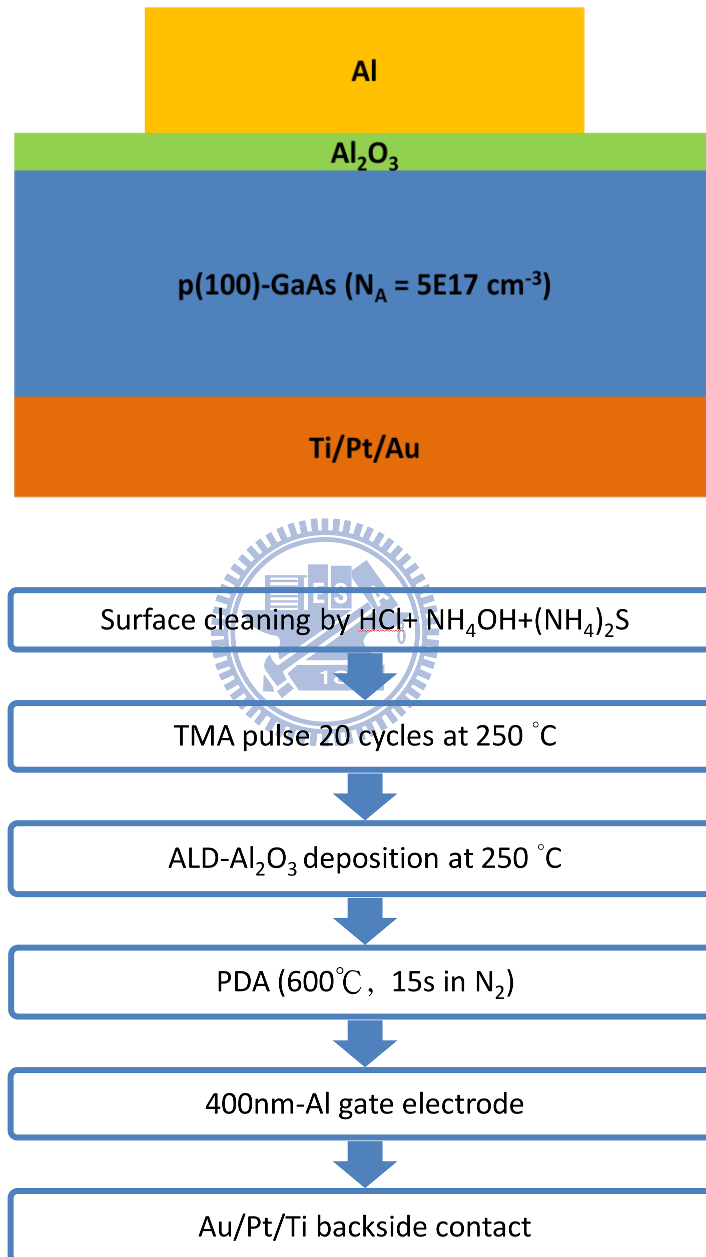


Fig. 3.2 The structure and process flow of Al/Al_2O_3/GaAs/TiPtAu MOS capacitor.

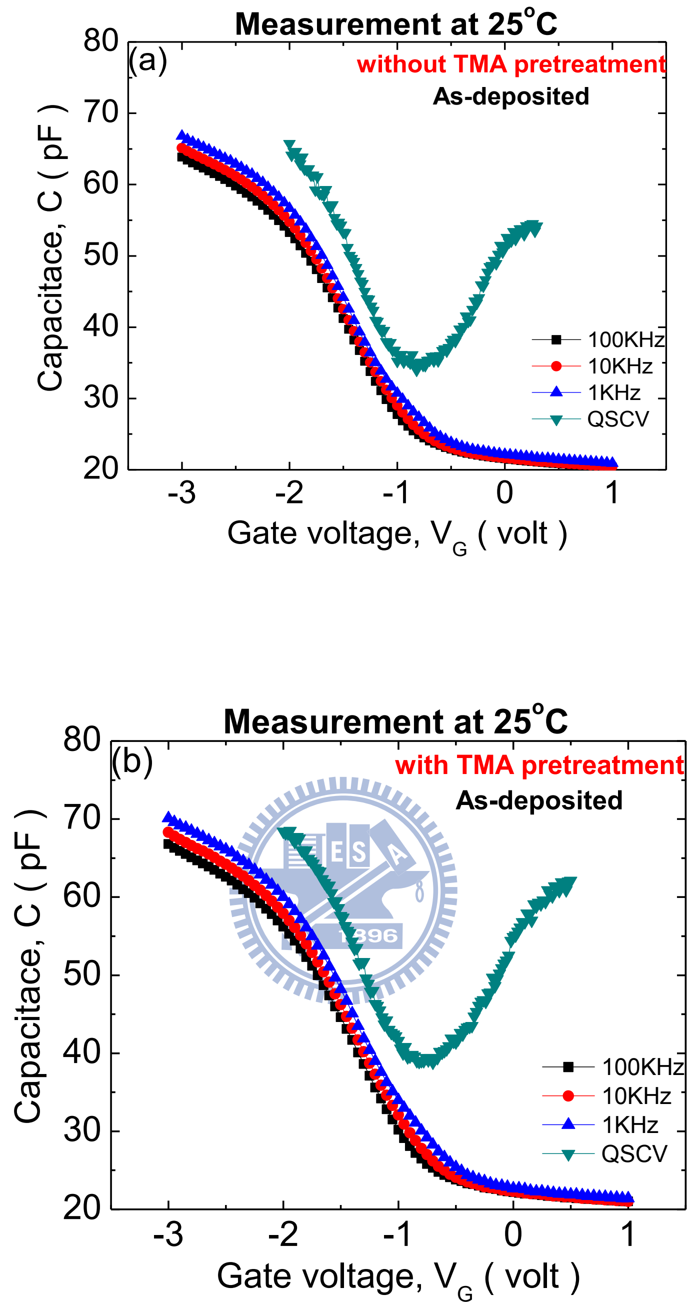


Fig. 3.3 Frequency-dependent C-V curves of Al/Al_2O_3/p(100)-GaAs/TiPtAu MOS capacitors. (a)without, (b)with TMA pretreatment.

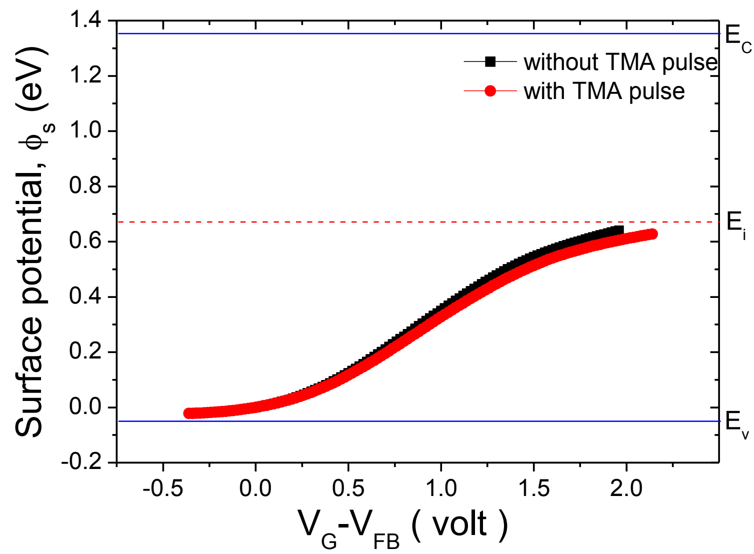


Fig. 3.4 Comparison of surface potential fluctuation of TMA effect of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors.

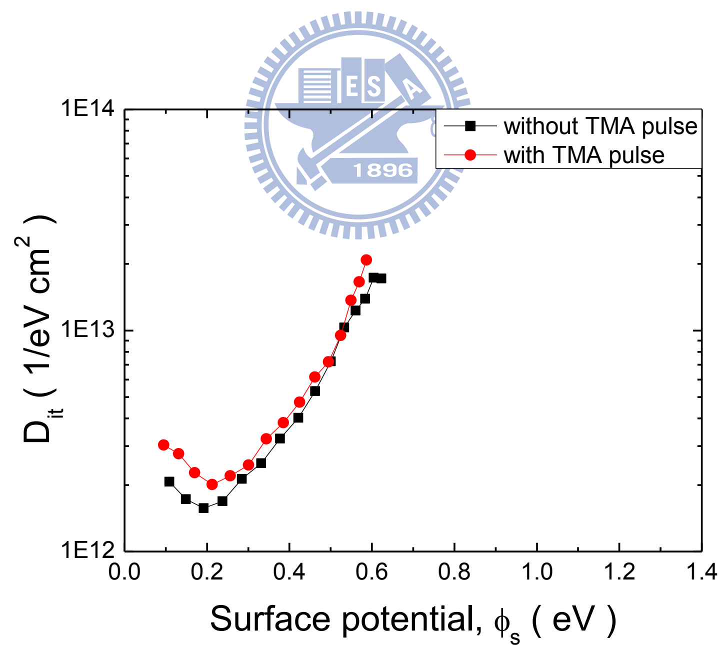


Fig. 3.5 Comparison of D_{it} distribution of TMA effect of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors.

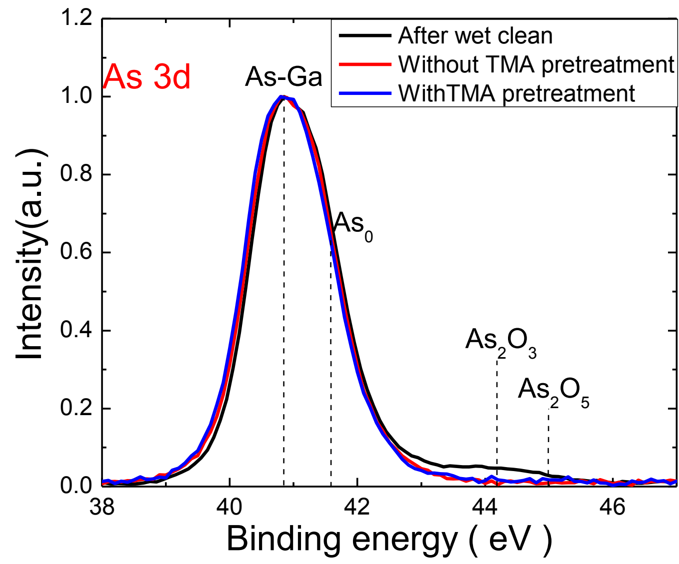
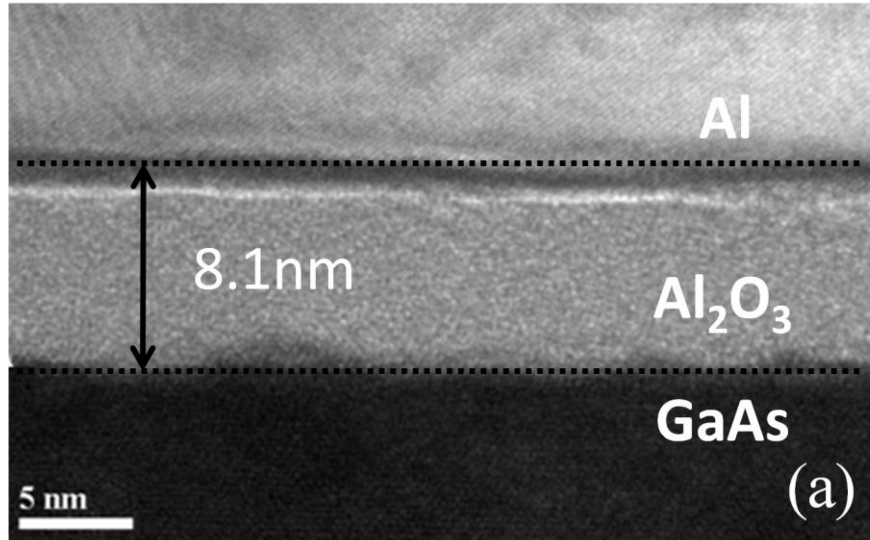


Fig. 3.6 As $2p_{3/2}$ XPS spectra of Al_2O_3/GaAs interface subjected to with and without TMA pulse.



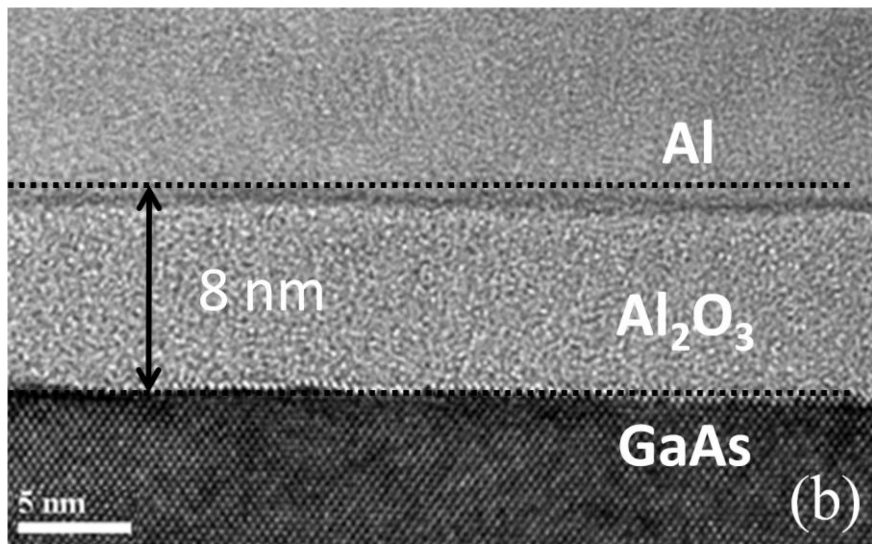


Fig. 3.7 The cross-section of TEM image of $Al/Al_2O_3/GaAs$: (a) without TMA pretreatment; (b) with TMA pretreatment.

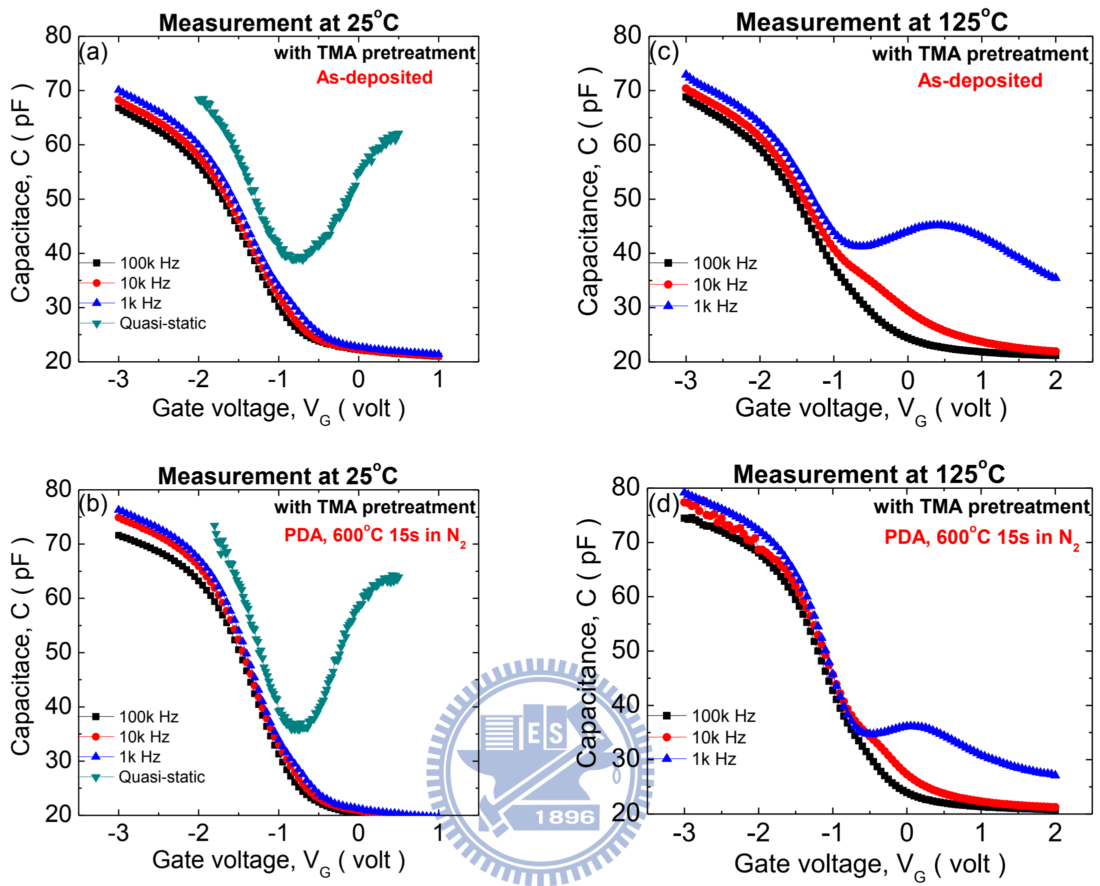


Fig. 3.8 Frequency-dependent C-V curves of Al/Al_2O_3/p(100)-GaAs/TiPtAu MOS capacitors at 25℃ and 125℃ measurement condition with TMA pretreatment, (a) and (c) as-deposited; (b) and (d) with PDA.

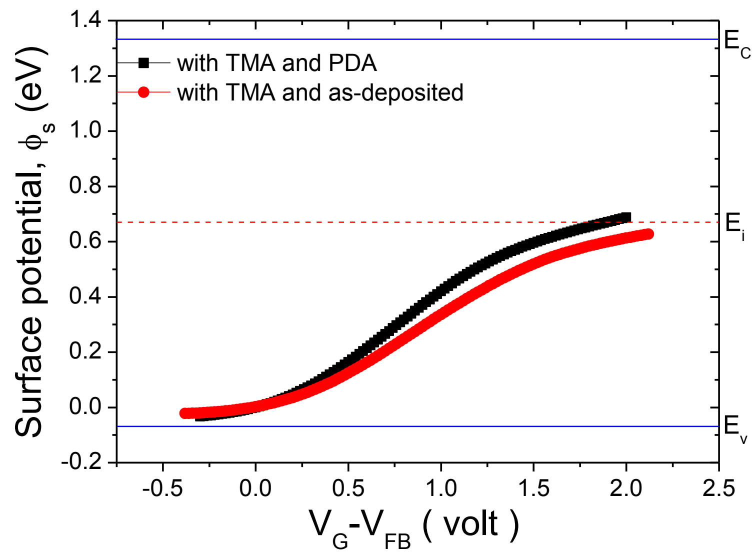


Fig. 3.9 Comparison of surface potential fluctuation of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors with and without PDA.

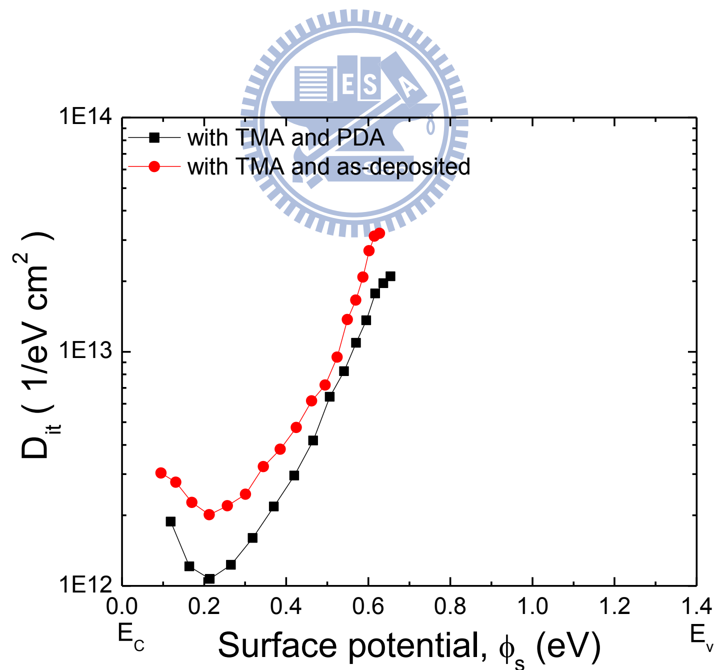


Fig. 3.10 Comparison of D_{it} distribution of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors with and without PDA.

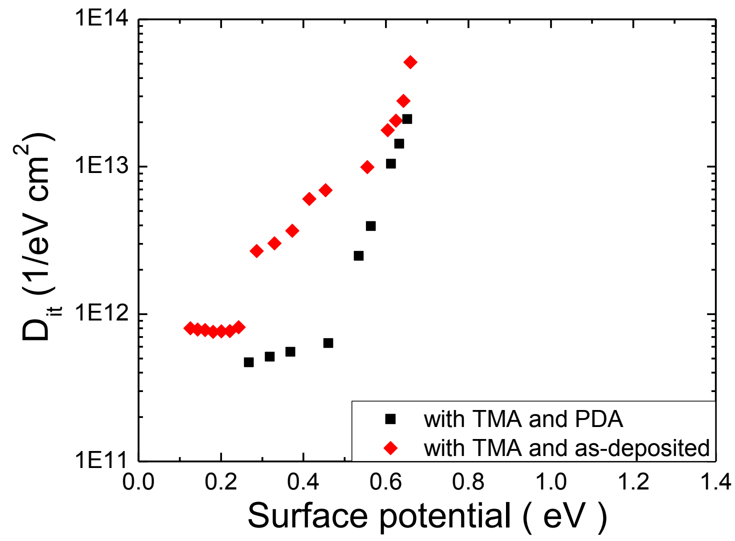


Fig. 3.11 Comparison of D_{it} distribution of Al/Al_2O_3/p-GaAs (100)/TiPtAu MOS capacitors with and without PDA.

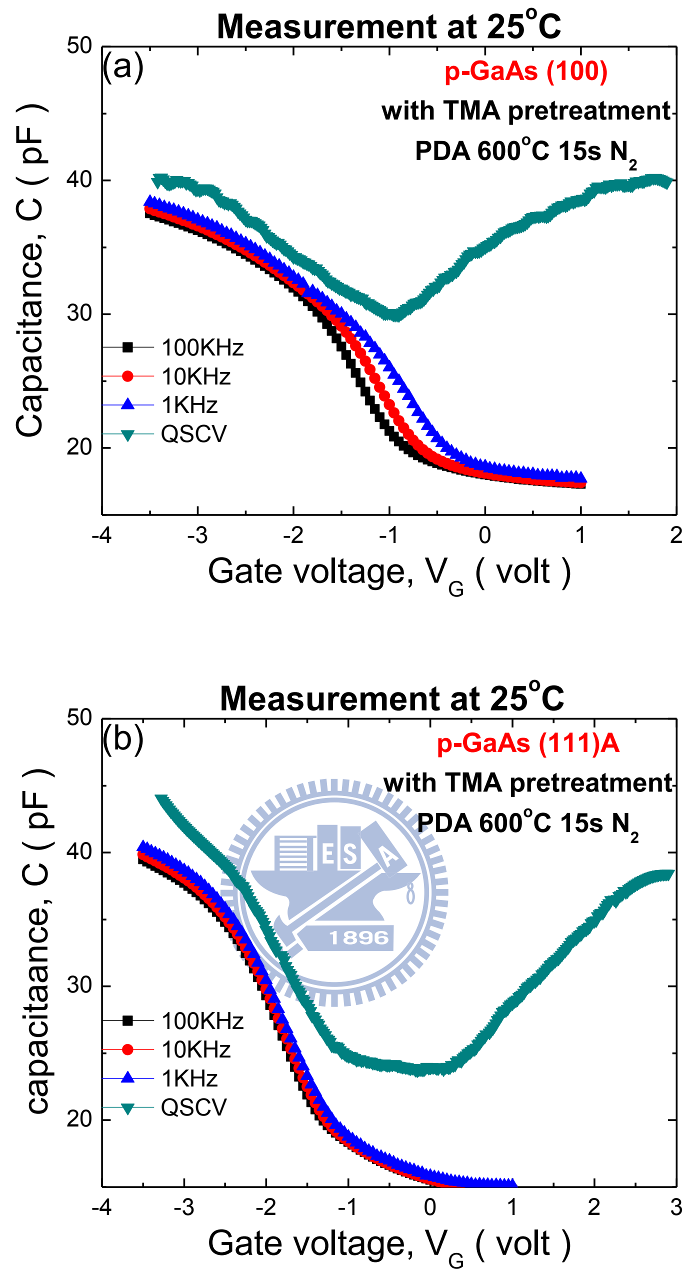


Fig. 3.12 C-V curves of Al/Al_2O_3/p-GaAs/TiPtAu MOS capacitors (a) (100), (b) (111)A surface orientation.

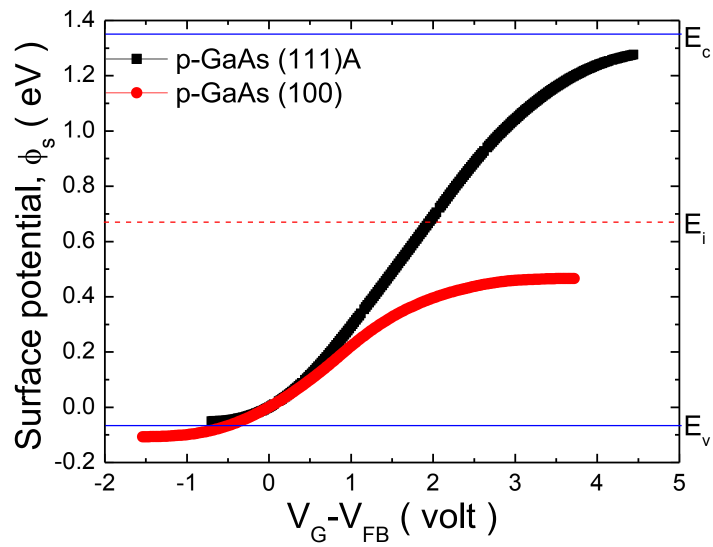


Fig. 3.13 Comparison of surface potential fluctuation of surface orientation effect of Al/ Al_2O_3/p-GaAs/TiPtAu MOS capacitors.

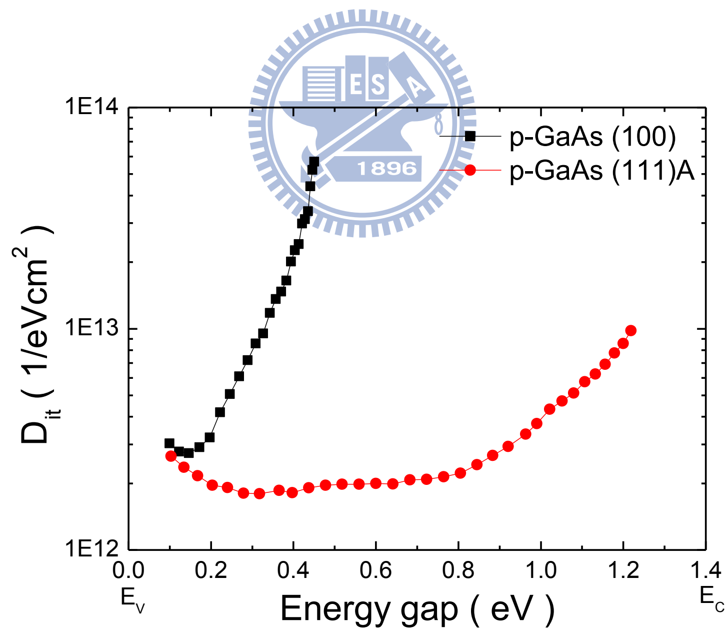


Fig. 3.14 Comparison of D_{it} distribution of surface orientation effect of Al/Al_2O_3/p-GaAs/ TiPtAu MOS capacitors.

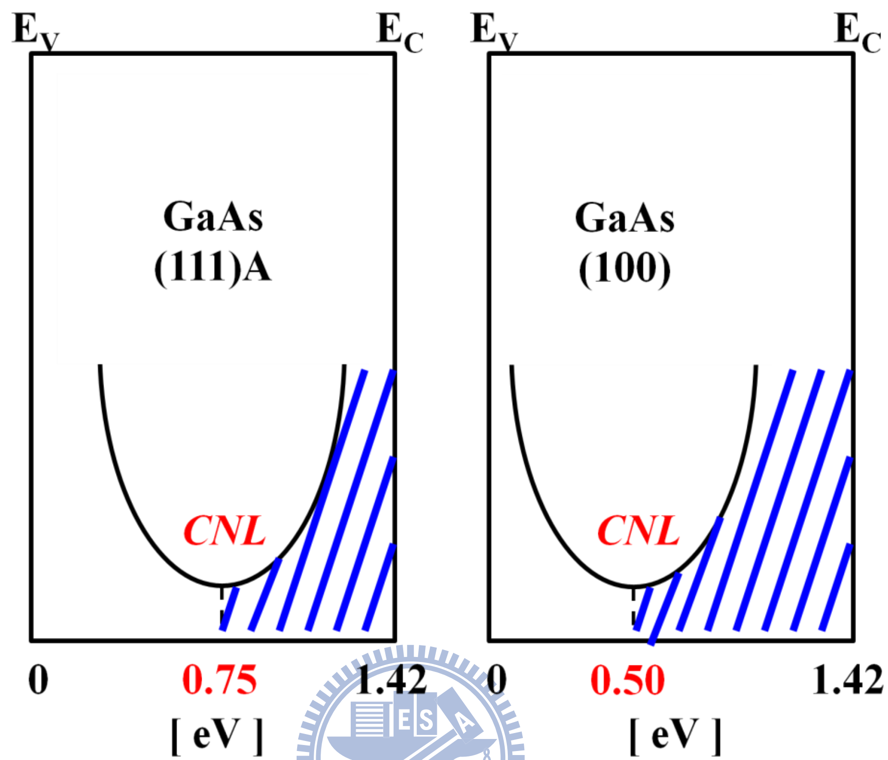


Fig. 3.15 Empirical model of GaAs (111)A and (100) surface. The minimum D_{it} and U-shape curvature depend on processing conditions, while the location of E_0 remains constant for each semiconductor with the same crystal face.

Chapter 4

Fabrications of GaAs MOSFET and InGaAs MESFET

4.1 Introduction

According to major silicon-based electronics industries including Intel Corp. [1-2], the Si complementary metal-oxide-semiconductor (CMOS) technology is rapidly approaching the ultimate scaling limit of physics, as demonstrated on the famous International Technology Roadmap for Semiconductors (ITRS) [3]. The high mobility semiconductor materials are resumed in MOSFET applications to obtain much higher device performance. In particular, Ge- and III-V-based channels featuring various prevailing gate dielectrics are promising structures to be used in place of conventional silicon MOSFETs.

Recently, superior high-*k*/Ge p-MOSFET characteristics have been reported [4-5], however, the fabrication of promising Ge n-MOSFETs remains challenging because of the resulting low electron mobility and the asymmetrical distribution of interface states, the Fermi level (E_F) pinning. On the other hand, the several promising n-MOSFET device characteristics based on (In)GaAs-based III-V channels have been continually demonstrated [6-8], and their performances even exceeded the strained-silicon transistors with the sub-micro gate length [9]. In fact, for obtaining the superior III-V device performance, it is essential to achieve the unpinned interface between dielectric and substrate. Up to now, this

issue is still of interest and more challenging for the dielectrics on (In)GaAs substrate, because of a larger energy difference between the charge neutrality level (E_{CNL}) and the conductance band edege (E_c) [10]. Various kinds of the treatment or passivation methods, such Si capping layer [11], silane-ammonia [12], and sulfur treatment [13], are adopted to eliminate the native oxides and other surface defects.

From several literatures, it was found that the deposition of Al_2O_3 dielectric on GaAs substrates during atomic layer deposition (ALD) could reduce the native oxide [14-16], decrease intermixing and lower interface states density (D_{it}). Hence, the characteristics of Al_2O_3 gate dielectrics by ALD system, on either GaAs channels or substrates are worth studying in more detail.

Nevertheless, III-V materials, in general, have the lower values of solid solubility of n-type dopants and the density of states (DOS), and these issues may be the problem in outperforming the silicon-based device characteristics of deep sub-100nm region [17]. For example, on GaAs substrate, the maximum silicon solubility and the DOS are merely 1×10^{19} and 4.7×10^{17} cm^{-3}, respectively, which are one and two orders of magnitude lower than silicon [18]. In consequence, these properties of III-V materials can contribute the more source/drain (S/D) resistance and hence suppress the maximum driving current. Therefore, we proposed a new structure of the III-V channel device having the IV S/D to solve these problems and hence enhance the current drive.

In this chapter, we succeeded to fabricate the enhancement-mode (E-mode) GaAs n-MOSFET with ALD- Al_2O_3 gate dielectrics on the GaAs (111)A substrate. Additionally, we also fabricated the common metal-semiconductor field effect transistor (MESFET) for control sample and epi-Ge S/D MESFET on InGaAs structures grown by molecular beam epitaxy (MBE) and discussed electrical characteristics of devices.

4.2 Experimental Procedures

4.2.1 Device Structure (MESFET)

For the n-channel (In)GaAs MESFET, we used different channel compositions to adjust driving current performance. The first channel layer is 90 nm n-GaAs with silicon-doped ($3\sim5 \times 10^{17}$ cm^{-3}), and for further improvement, there is a 10 nm n-$In_{0.2}Ga_{0.8}As$ channel layer on the top of n-GaAs channel. The 2.5 nm $In_{0.47}Ga_{0.51}P$ later is used as etching stop layer, followed by the heavily doped n^+-GaAs contact layer. The scheme was presented in **Fig. 4.1**.

Device structures were achieved by wet etching with $H_3PO_4 : H_2O_2 : H_2O = 1 : 1 : 160$ (the etching rate ~0.5 nm/s) and $HCl : H_2O = 1 : 3$ (the etching rate ~1.25 nm/s) for GaAs and $In_{0.47}Ga_{0.51}P$, respectively.

In MESFET fabrication, the first step is the mesa etching to semi-insulator GaAs substrate for the definition of active area region. Next, Ni/Ge/Au (30 nm/70 nm/180 nm) tri-layer metal was deposited by e-beam evaporator as S/D ohmic contact, followed by rapid thermal annealing (RTA) at 400℃ for 60s in N_2 ambient. And then, we used T-gate mask to achieve recess gate and etched by the solution as mentioned above. After gate recess, depositing Ti/Pt/Au (5 nm/30 nm/180 nm) as Schottky metal gate through lift-off process. The fully process flow was also shown in **Fig. 4.1**.

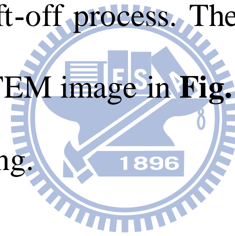
4.2.2 Device Structure (MESFET with Ge S/D)

In Ge-S/D MESFET fabrication, in the first step, depositing 400-nm SiO_2 as hard masker and etching of the recess S/D region by the solution as mentioned above. After surface cleaning, the growth of Ge was carried out by using a UHV/CVD system with a base pressure

of less than 5 × 10^{-8} Torr. After GaAs wafers were loaded into the growth chamber, the in-situ prebaking at 650℃ for 10 min in H_2 ambient was introduced. Then, the temperature was lowered to 550℃ for Ge growth with a constant GeH_4 flow rate. Throughout the entire growth process, the gas pressure in the growth chamber was kept at 30 mTorr.

Next, the S/D regions were implanted with phosphorus at doses of 5 × 10^{14} cm^{-2} and 1 × 10^{15} cm^{-2} at 50keV and 30keV, respectively. Subsequently, a SiO_2 capping layer was deposited by plasma-enhanced chemical vapor deposition (PECVD), and then, the sample was annealed in a N_2 ambient at 600 ℃ for 30 s by RTA.

The 500-nm Al metal was deposited as S/D contact, followed by forming gas annealing (FGA) at 400 ℃ 30 min. Finally, we used T-gate mask to achieve recess gate and etched by the solution as mentioned above. After gate recess, depositing Ti/Pt/Au (50 nm/70 nm/180 nm) as Schottky metal gate through lift-off process. The fully process flow of Ge-S/D MESFET was shown in **Fig. 4.2**. From the TEM image in **Fig. 4.3**, there was no dislocation at Ge/GaAs interface because of lattice matching.



4.2.3 Device Structure (MOSFET)

In E-mode GaAs n-MOSFET fabrication, using ALD and PECVD to deposit Al_2O_3 10 nm and SiO_2 420 nm as hard masker, and then, defining the S/D region for implantation Si and P at 50 keV of 1 × 10^{14} cm^{-2} and 60 keV of 1 × 10^{15} cm^{-2}, respectively. S/D activation was using RTA at 850℃ for 10 s in N_2 ambient with a SiO_2 capping layer. The SiO_2 was subsequently removed from the active area region, followed by cleaning by diluted HCl, diluted NH_4OH, $(NH_4)_2S$ solution. After surface cleaning, the sample was loaded into the ALD chamber, followed by surface pretreatment with TMA pulse 20 cycles. Next, the Al_2O_3 gate dielectric was deposited by ALD at 250 ℃, followed by postdeposition annealing (PDA)

at 600 ℃ for 15 s in an N_2 ambient. Thermal evaporated Al about 400 nm was patterned as T-gate electrodes through the lithography. After excavating the S/D contact holes, the tri-layer Ni/Ge/Au (30 nm/70 nm/180 nm) was deposited at the S/D region and patterned by lift-off process, followed by RTA at 400℃ for 60 s in an N_2 ambient to form ohmic contact. The fully process flow of GaAs n-MOSFET was shown in **Fig. 4.4**.

4.3 Results and Discussion

4.3.1 Electrical Characteristics of InGaAs MESFET

DC characteristics of InGaAs MESFETs were measured by HP4200 and HP4284, respectively. **Fig. 4.5** displayed electrical characteristic of the source to drain current with the different gate recess depth and extracting the contact resistance and sheet resistance by transfer length method (TLM) test structure. **Fig. 4.6** illustrated the total resistance measured from various contact spacings, and the test structure of TLM is shown in the inset. The total resistance between any two contacts is described from **Eq. (4.1)**

$$R_T = \frac{R_{sh} d}{Z} + 2R_c \approx \frac{R_{sh}}{Z}(d + L_T) \qquad (4.1)$$

Where R_T is total resistance between any two contacts, R_{sh} is sheet resistance, and R_c is contact resistance. Three parameters can be extracted from the plots. The slope △ (R_T)/△ (R_T) = R_{sh}/Z leads to the sheet resistance with the contact width Z independent measured. The intercept at d = 0 is R_T = 2 R_c giving the contact resistance. The intercept at R_c = 0 gives -d = $2L_T$, which leads to the specific contact resistivity with R_{sh} known from the slope of the plots by **Eq. (4.2)**.

$$L_T = \left(\frac{\rho_c}{R_{sh}}\right)^{\frac{1}{2}} \qquad (4.2)$$

After calculating, we listed the parameters of InGaAs MESFETs in **Tab. 4.1**. The sample with 19 nm recess depth is stopped on the contact layer, where the gate metal located, will result in the extra current path from source to drain.

Fig. 4.7 and **Fig. 4.8** illustrated the I_D-V_G transfer characteristic and I_D-V_D output characteristic of 8 μm gate length for InGaAs MESFET with different recess gate depth, respectively. We can observe the 20 nm recess depth stopped on $In_{0.48}Ga_{0.51}P$ layer has the higher ratio I_{on}/I_{off} than the others. The better ratio I_{on} (I_D at $V_G = 1$ V, $V_D = 1.5$ V)/I_{off} (I_D at $V_G = -0.75$ V, $V_D = 1.5$ V) of the device with gate metal contacted on $In_{0.48}Ga_{0.51}P$ layer is 5.9×10^4. We deduced the other devices which perform poor I_{on}/I_{off} ratio. According to the comparison of electrical characteristics above, using the recess gate structure of the better ratio I_{on}/I_{off} to fabricate the Ge-S/D InGaAs MESFET and discussed the electrical characteristics.

4.3.2 Electrical Characteristics of Ge-S/D InGaAs MESFET

Fig. 4.9 illustrated the total resistance measured from various contact spacings, and the TLM test structure is presented in the inset. After calculating, the R_{sh} is 1289 Ω/□, the R_c is 149 Ω, and the ρ_c is 1.93×10^{-3} Ω-cm^{-2}. Comparing with control sample which was analyzed above, the sample with Ge S/D has the poorer sheet resistance. The reason is probably that we did not exactly control the dose of implantation and time of S/D activation; it leaded to the more impurity in the S/D region. The issue of large specific contact resistivity of Al/n^+-Ge contact has been a challenge due to E_F pinned on metal/ n^+-Ge interface.

Fig. 4.10 illustrated the I_D-V_G transfer characteristic of InGaAs MESFET with Ge-S/D with 3 μm gate length, and the I_{on} (I_D at $V_G = 1$ V, $V_D = 1$ V)/I_{off} (I_D at $V_G = -1$ V, $V_D = 1$ V) ratio is 3.23×10^2; **Fig. 4.11** illustrated the I_D-V_D output characteristic of the same device, and

the maximum drain current was 12 μA/μm measured at $V_G = 0.5$ V, $V_D = 3$ V. We ascribed the device with Ge-S/D has the lower transfer and output characteristics due to the larger resistance parameters analyzed by TLM test structure.

4.3.3 Electrical Characteristics of E-mode GaAs n-MOSFET

Fig. 4.12 illustrated the I_D-V_G transfer characteristic of E-mode ALD-Al_2O_3/GaAs (111)A n-MOSFET with TMA 20-cycles-pulse pretreatment. The gate length of this device is 5 μm and the I_{on} (I_D at $V_G = 3V$, $V_D = 2V$)/I_{off} (I_D at $V_G = 0V$, $V_D = 2V$) ratio is 4.12×10^3; **Fig. 13.** showed the trans-characteristic in the linear and saturations. For device with the gate length/width of 5/100 μm, the value of V_{th} was 0.95 V which is extracted by linear extrapolation. The value of G_m at $V_D = 0.1$ V was 0.35 nS/μm.

In **Fig. 4.14**, the well saturation and pinch-off characteristics were presented in I_D-V_D curves as the function of the gate voltage (V_G) ranging from 0 to 3 V. It could be obtained that the maximum drain current was 9 nA/ μm measured at $V_G = 3$ V and $V_D = 4$ V.

Fig. 4.15 illustrated the gate-to-channel capacitance (C_{GC}) and inversion charge density (Q_{inv})by **Eq. (4.3)**

$$Q_{inv} = \int_{-\infty}^{V_G} C_{GC}(V_G)dV_G \tag{4.3}$$

and solving for the effective mobility (μ_{eff}) gives

$$\mu_{eff} = \frac{g_d L}{W Q_{inv}} \tag{4.4}$$

where the drain conductance (g_d) is defined as

$$g_d = \frac{\partial I_D}{\partial V_D} |_{V_G=constant} \tag{4.5}$$

Fig. 4.16 depicted the effective mobility extracted from the g_d at $V_G = 3$ V and the capacitance-voltage curve property under inversion region at 100 kHz in the **Fig. 4.15**.

4.4 Summary

In the chapter 4, firstly, we have grown superior III-V epi layer by using MBE system and also fabricated MESFET through the standard 3 mask processes. Secondly, we succeeded in demonstrating the MESFET with Ge-S/D through the 4 mask processes. Finally, we accompanied the experiences in Al_2O_3/GaAs capacitors to successively demonstrate the GaAs MOSFET on SI-substrate. We presented all the electrical performances and extracted device parameters for those GaAs FET with different device structures. By analyzing the $I_D - V_G$ and $I_D - V_D$ electrical characteristics, we also discussed those parameters such as V_{th} , S.S., and μ_{FE}.

For MESFET with Ge-S/D, however, we have the poorer DC characteristics than control sample. We have to overcome the large sheet resistance and specific contact resistivity, and apply this Ge-S/D application for GaAs MOSFET.

For E-mode GaAs MOSFET, we used ALD self-cleaning and different surface orientation to form a well dielectric/substrate interface. Although we successively demonstrate the GaAs MOSFET on semi-insulator substrate, the electrical characteristics were poor and it should be better to continue improving the output and transfer characteristics for realization of an acceptable transistor. We will further fabricate the E-mode GaAs MOSFET with other passivation methods on p-type and SI-substrates based on the experience in this chapter of the E-mode GaAs MOSFET.

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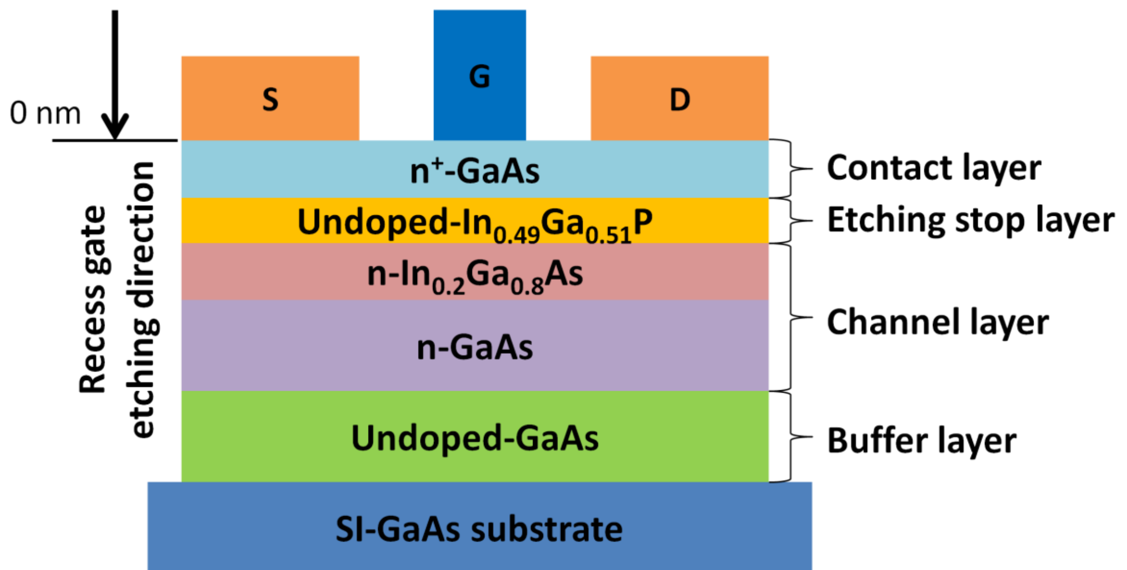


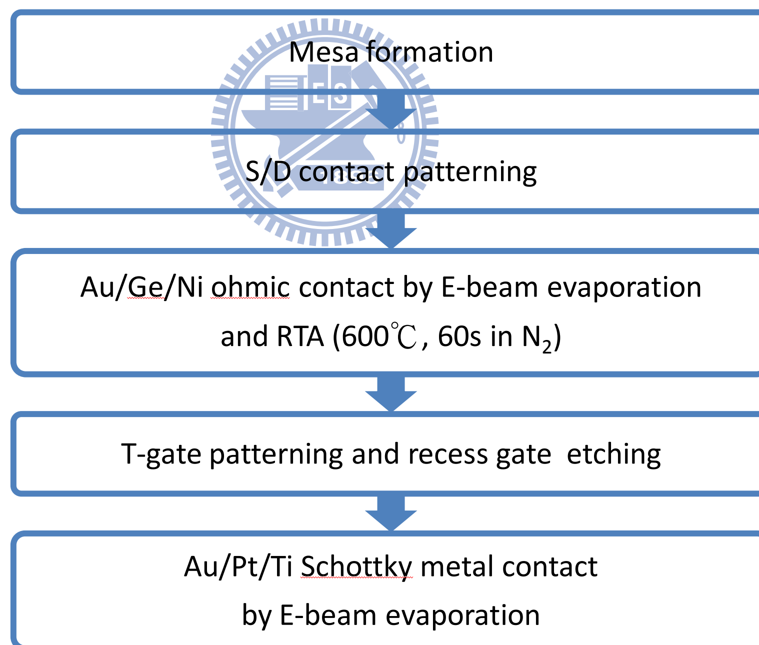


Fig. 4.1 The scheme of MBE InGaAs and the fabricated InGaAs MESFET process flow.

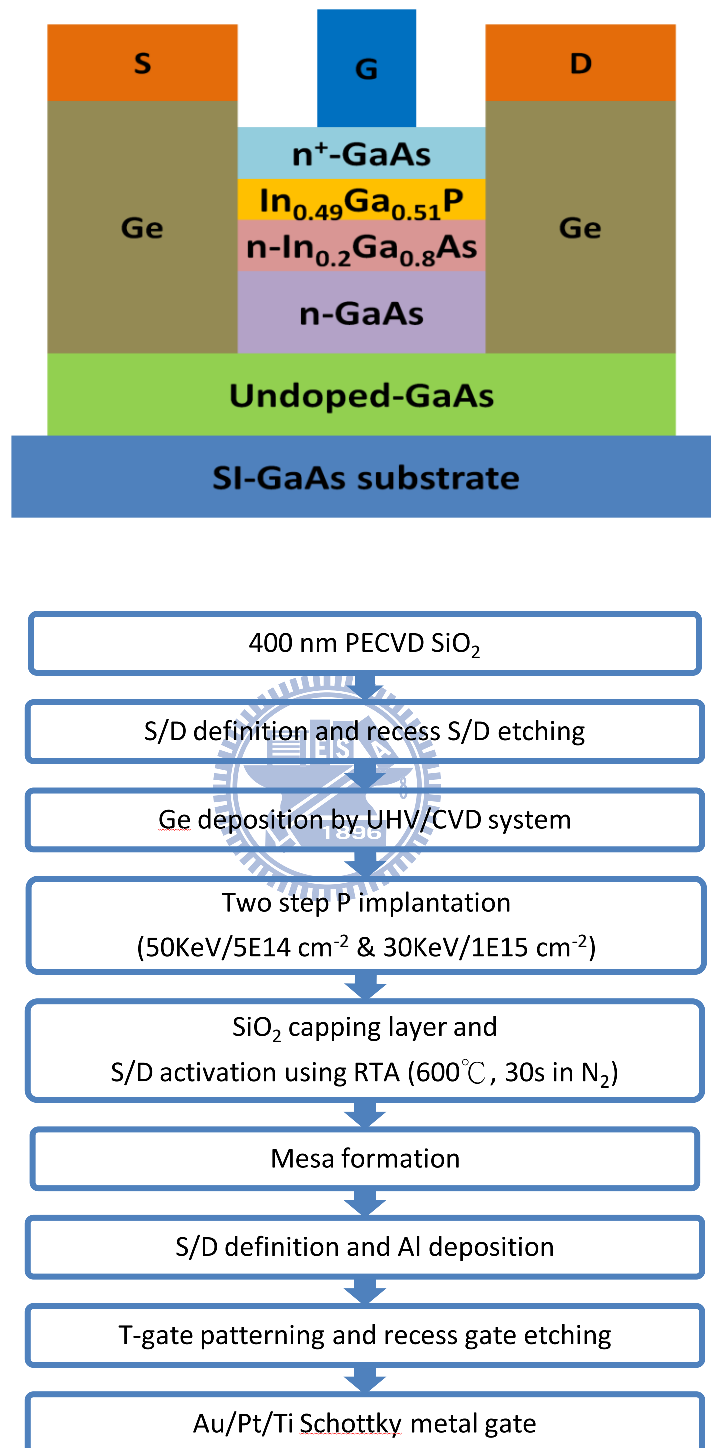


Fig. 4.2 The scheme and process flow of MESFET with Ge-S/D on InGaAs structure.

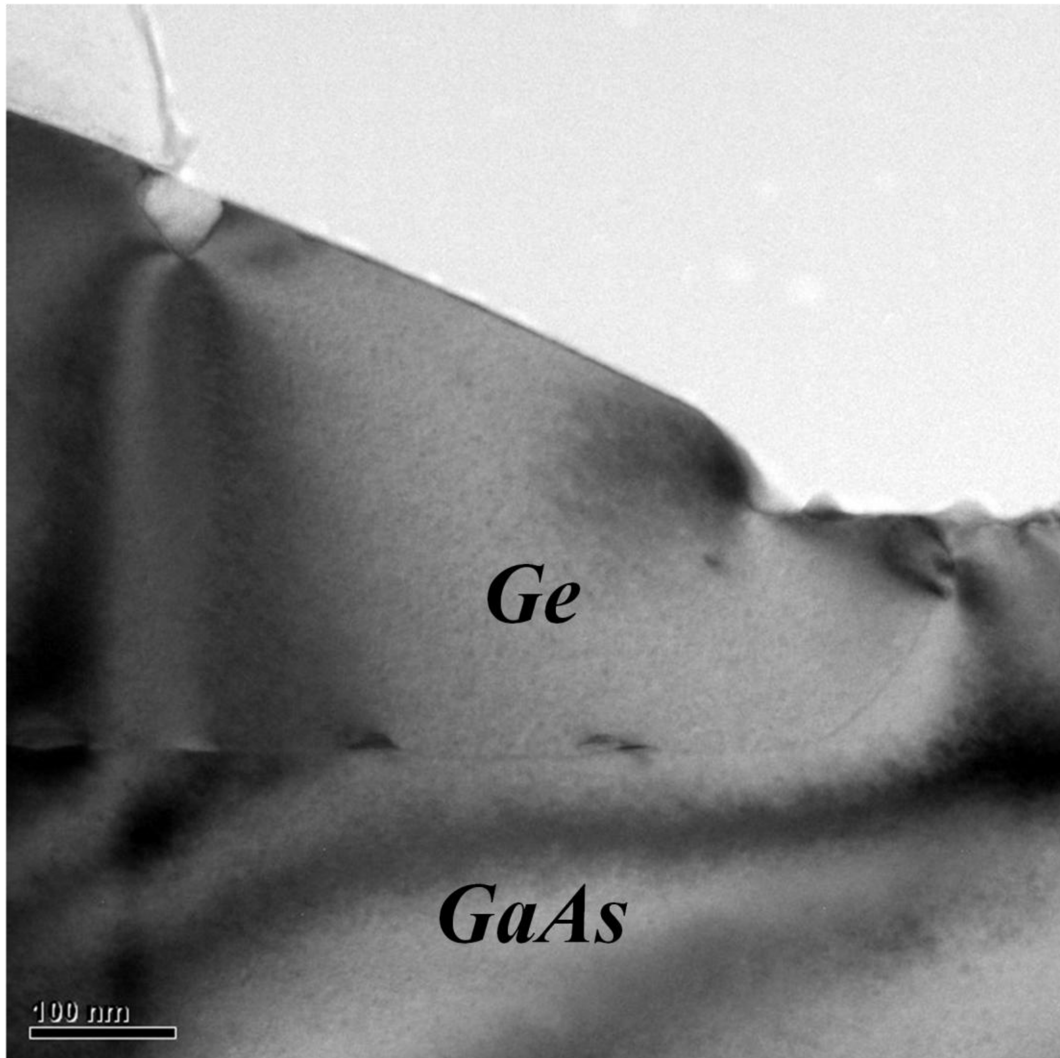
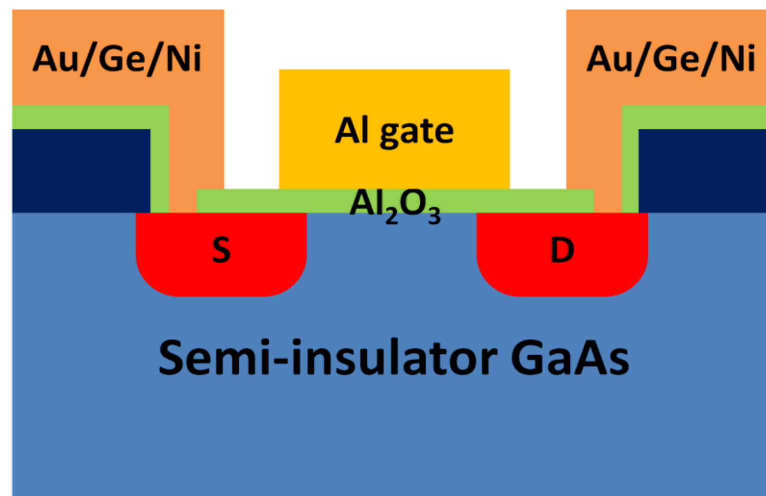


Fig. 4.3 The TEM image of Ge film which was grown by UHV/CVD system on semi-insulator GaAs substrate.



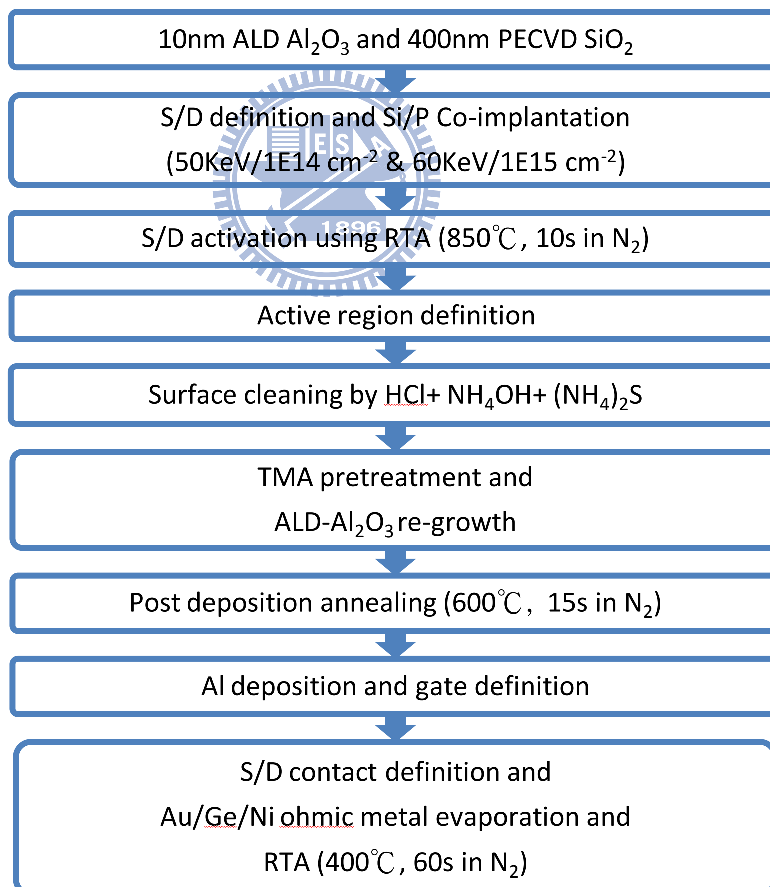


Fig. 4.4 The scheme and process flow of E-mode GaAs n-MOSFET on semi-insulator substrate.

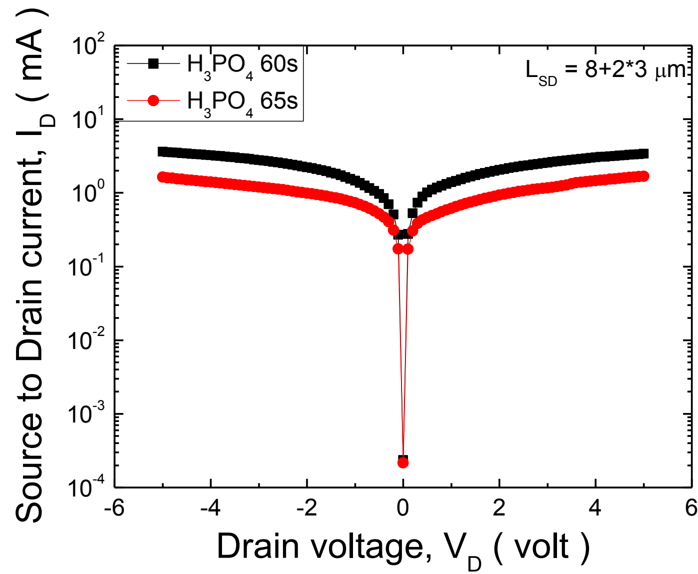


Fig. 4.5 Source to drain current with the different recess gate etching depth of GaAs MESFET.

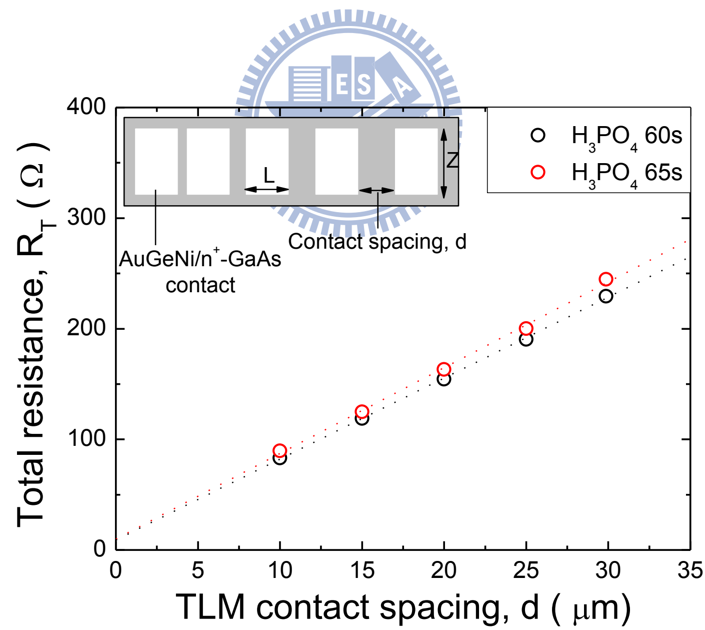


Fig. 4.6 Total resistance with the different recess gate etching depth of InGaAs MESFET and the inset is TLM test structure (L=50μm Z=100μm).

	Recess depth	Sheet resistance R_{sh} ($\Omega/\square$)	Contact resistance R_c (Ω)	Specific contact resistivity ρ_c (Ω-cm^{-2})
H_3PO_4 60 s	19 nm	731.85	3.66	1.83×10^{-6}
H_3PO_4 65 s	20 nm	774.54	3.87	1.91×10^{-6}

Tab. 4.1 The resistance parameters by transfer length method (TLM) test structure of InGaAs MESFET.

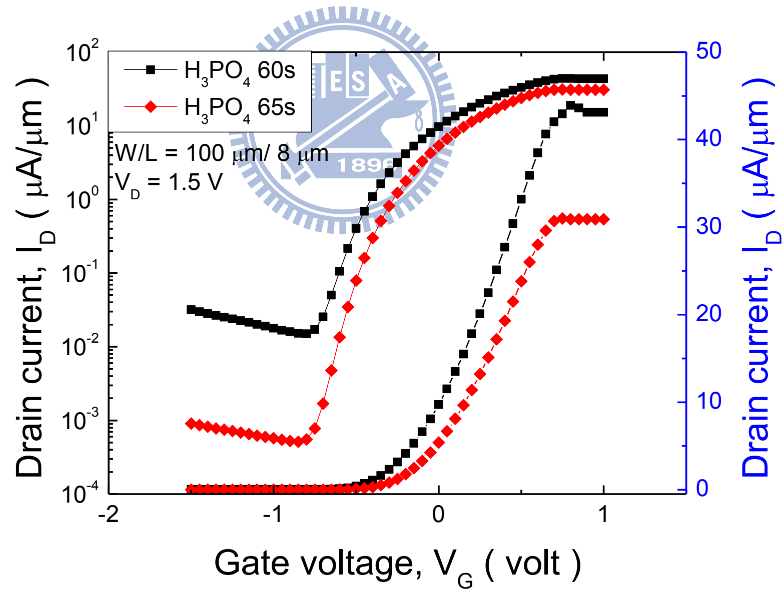


Fig. 4.7 Transfer characteristic for InGaAs MESFET with 8 µm gate length. The best I_{on}/I_{off}(@ V_{DS} = 1.5 V) is about 5.9×10^4.

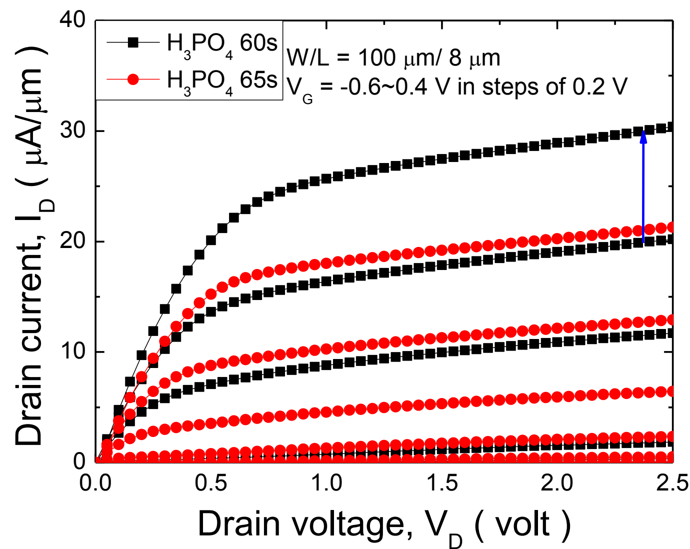


Fig. 4.8 Output characteristic (I_D-V_D) with different gate bias for InGaAs MESFET with 8 μm gate length.

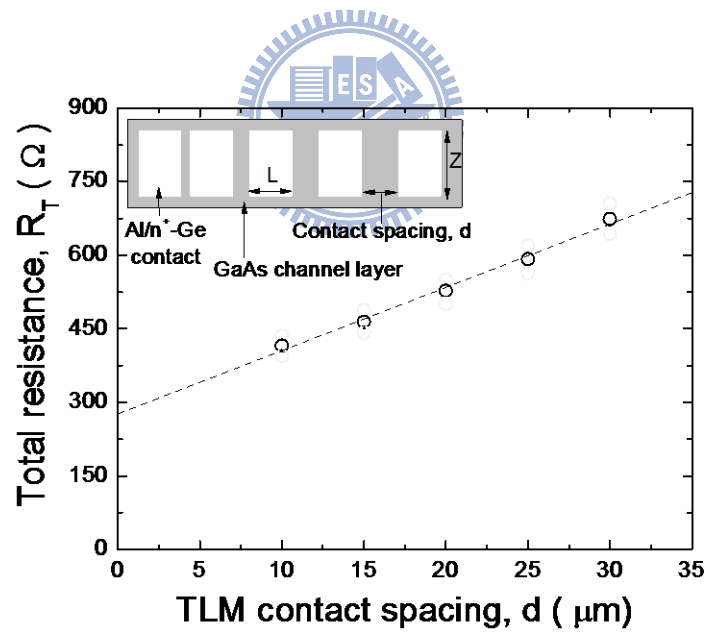


Fig. 4.9 Total resistance of InGaAs MESFET with Ge-S/D and the inset is TLM test structure (L=50μm Z=100μm).

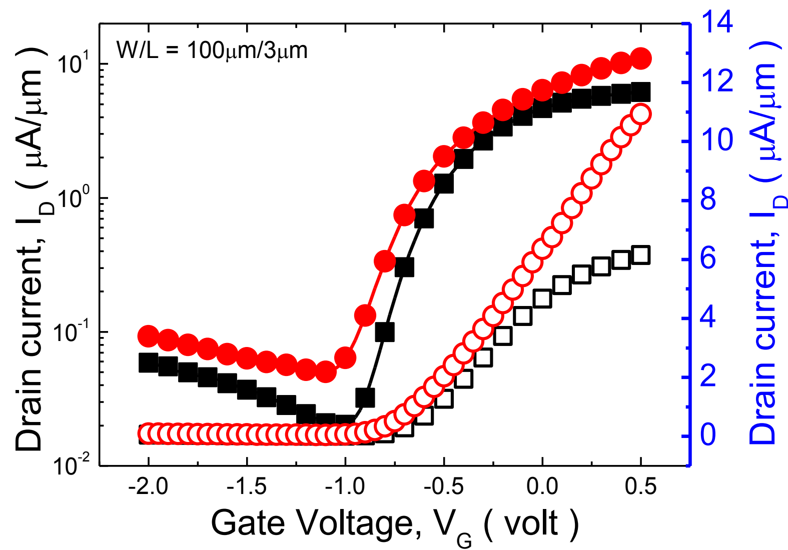


Fig. 4.10 Transfer characteristic for InGaAs MESFET with Ge-S/D with 3 μm gate length. The best I_{on}/I_{off} (@ V_{DS} = 1 V) is about 3.23×10^2.

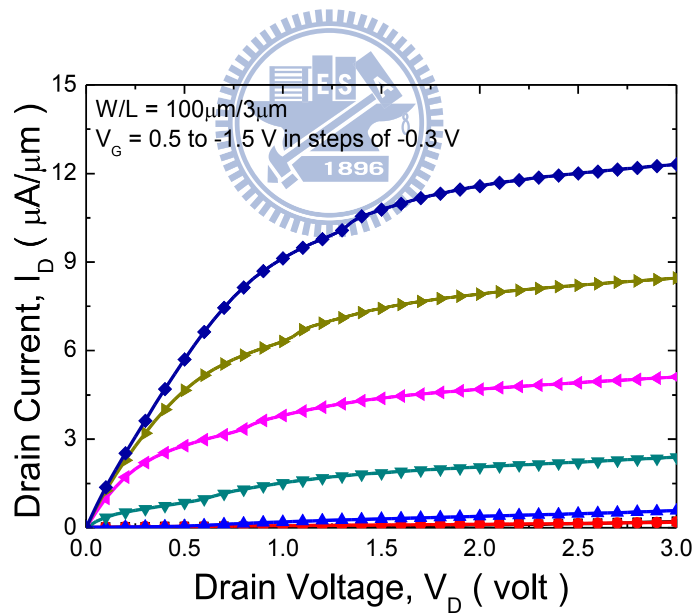


Fig. 4.11 Output characteristic (I_D-V_D) for for InGaAs MESFET with Ge-S/D with 3 μm gate length.

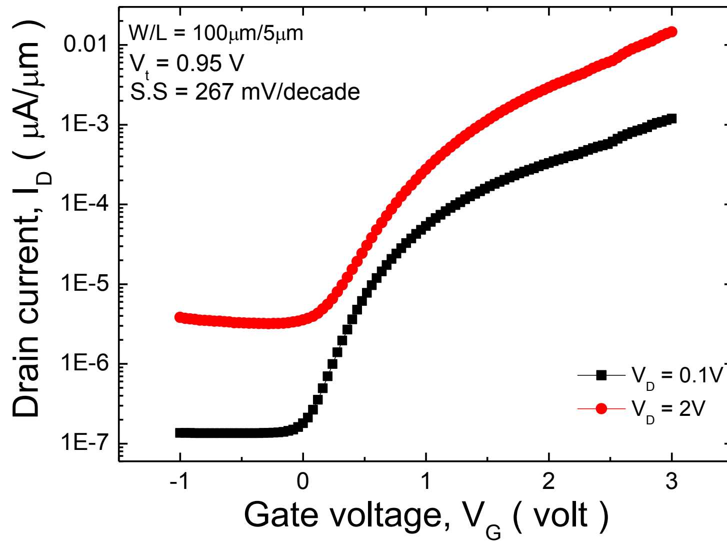


Fig. 4.12 Transfer characteristic of E-mode GaAs n-MOSFET with 5μm gate length. I_{on}/I_{off}(@ V_{DS}=2V) is about 4.12×10^3.

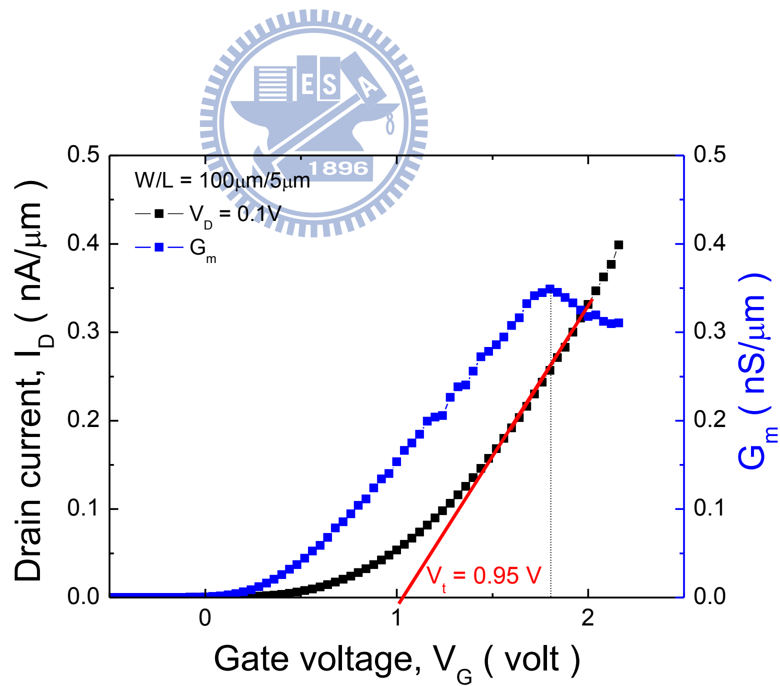


Fig. 4.13 Trans-characteristic (G_m) versus gate bias (V_G) of E-mode GaAs n-MOSFET with 5μm gate length. The peak G_m is 0.35 nS/μm.

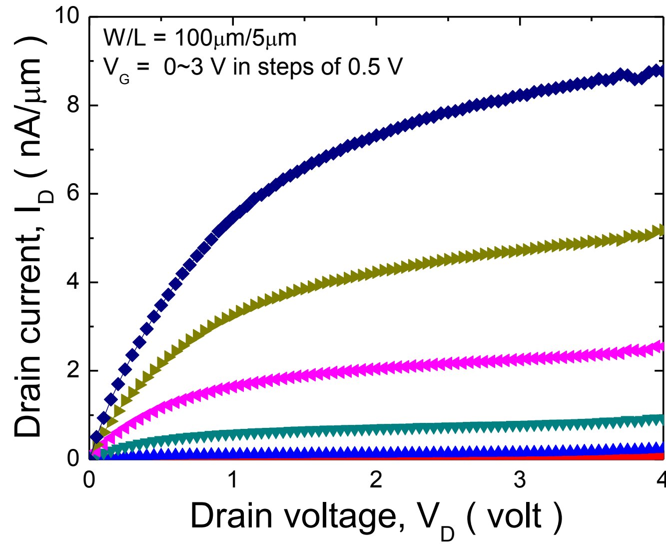


Fig. 4.14 Output characteristic (I_D-V_D) for E-mode GaAs n-MOSFET with 5μm gate length. The maximum drain current is 9 nA/μm.

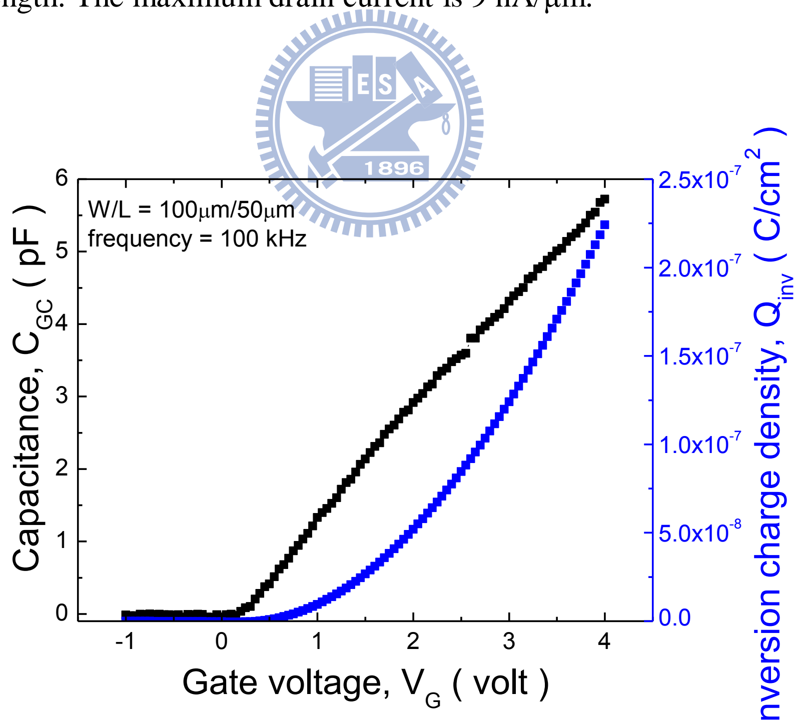


Fig. 4.15 The gate-to-channel capacitance and inversion charge density of E-mode GaAs n-MOSFET with 5μm gate length.

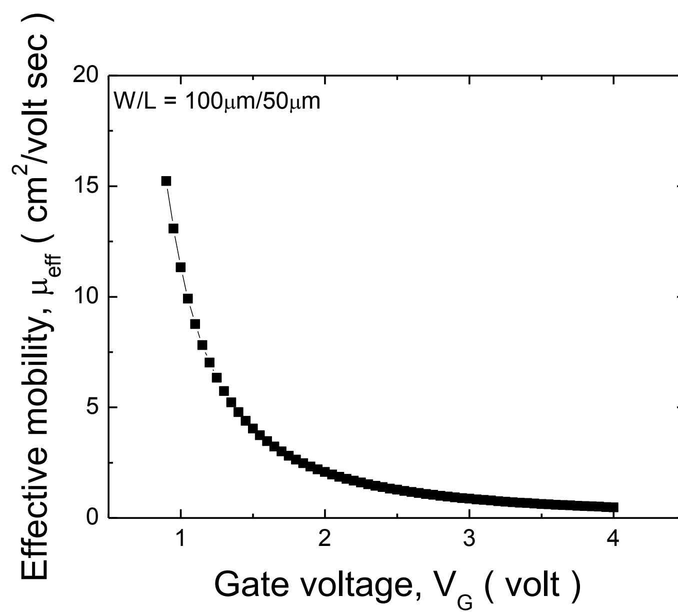
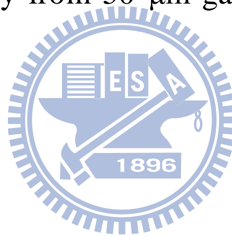


Fig. 4.16 The effective mobility from 50 μm gate length on E-mode GaAs n-MOSFET.



Chapter 5

Conclusion and Suggestions

5.1 Conclusion

In this thesis, firstly, we have studied the electrical characteristics of GaAs metal-oxide-semiconductor (MOS) capacitors with Al_2O_3 gate dielectric. Using the results of capacitance-voltage (C-V), including quasi-static C-V and multi-frequency C-V with the different temperature conditions, we established a process to determine the electrical characteristics which surface potential fluctuation and the distribution of interface states density (D_{it}) within energy bandgap.

Next, we have investigated sequentially self-clean by $Al(CH_3)_3$ (TMA, the aluminum precursor) during atomic layer deposition (ALD) and surface orientation of substrate effect by analyzing the electrical characteristics of GaAs MOS capacitors. We demonstrated the GaAs (111)A with TMA pretreatment had the best surface potential fluctuation and the lower value of D_{it} at mid-gap.

Accompanying above these experiences in ALD-Al_2O_3/GaAs MOS capacitors, we successively demonstrated the device characteristics of the enhance-mode (E-mode) n-metal-oxide-semiconductor field-effect transistor (MOSFET) with ALD-Al_2O_3 gate dielectrics on semi-insulator GaAs substrate. The peak mobility and on/off ratio reached as high as 15 cm^2/V*sec and >10^3, respectively, for the n-MOSFET (W/L = 100 μm/5 μm). In

addition, we also successively fabricated the InGaAs metal-semiconductor field-effect transistor (MESFET) with Ge-source/drain (S/D) and demonstrated the electrical characteristics. The maximum drain current and on/off ratio reached as high as 12 μA/μm and >10^2, respectively, for the InGaAs MESFET with Ge-S/D (W/L = 100 μm/3 μm).

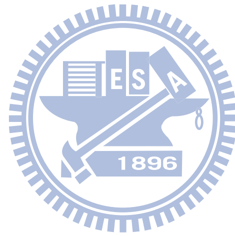
5.2 Suggestions

In terms of our experimental results and several reported studies, it is concluded that the value of D_{it} is still higher in the upper half of the energy bandgap of GaAs. The challenge is still to get the native oxide free in the interface between insulator and substrate. The other surface treatment before insulator deposition, including native reduction by hydrogen, Si or Ge interfacial passivation layers are both practical techniques for lowering the value of D_{it}.

Except for improving the performance of the E-mode GaAs n-MOSFET, the reliability characteristics of MOS capacitors with ALD-Al_2O_3 gate dielectric on GaAs substrates is also worth investigating. Accelerated life-test of MOS devices is conventionally performed by applying a constant gate voltage (CVS) or injecting a constant gate current (CCS) over a period of time to monitor the oxide degradation. Moreover, time to dielectric breakdown (TDDB) under constant-voltage stressing is considered a very important parameter in determining the reliability and integrity of gate oxide.

On the other hand, the performance of GaAs filed-effect transistor with Ge-S/D can be improved by inserting an insulator or dipole layer between metal and n^+-Ge. This is because that the epitaxial structure of the III-V channels MOSFET having the IV-group S/D is capable of solving the resistance problem and hence boosting the current drive capability. Such a nano-scale MOSFET integrates the advantages of III-V n-channel with higher electron mobility and thermal velocity, and the advantages of IV-group S/D with higher density of

states and solid solubility of n-type dopants. This structure is believed that these research topics in the heteroepitaxy technique and device fabrication are worthy of more detailed investigation.



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A study on the electrical properties of GaAs channel devices with atomic-layer-deposited Al_2O_3 gate dielectric