國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

具有加強轉換增益及雜訊相消機制的 V-band 四倍頻器

A V-band Frequency Quadrupler with Spur Cancellation and Conversion Gain Enhancement

研究生：任根生

指導教授：郭建男教授

中 華 民 國 一 百 年 九 月

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摘要

藉於操作在 V-band 頻段以達到高資料傳輸已是近來的趨勢，本論文主要是設計一個低消耗功率的四倍頻器以做為在 V-band 系統下的應用，如做為升頻混波器的本地震盪訊號等。此提出的四倍頻器為利用次諧波混合以增進其效能，包含詳盡的非線性分析與實驗結果，證明其能更有效率產生四倍頻信號。

在本論文中實現的晶片是使用 TSMC 90-nm CMOS 製程，輸入端的中心操作頻率為 12.5 GH,在 8 dBm 的基頻輸入功率下，輸出量得-20 dBm 的四倍頻訊號(包含 3 dB 的四相位產生器損耗以及 9.5 dB 的輸出級損耗)，功率消耗為 2.8mW，在輸出雜訊抑制上，基頻與二倍頻以及三倍頻諧波的抑制比分別是 53.5 dBc， 29.2 dBc 及 43 dBc，此外，在量測中也驗證我們提出的混頻架構可以在同樣的功率消耗下，比直接利用四階非線性特性產生四倍頻要高出 4 到 7 dB 的增益量。再者，整體直流功率消耗也控制在 3mW 以內，遠低於過去已提出的文獻。

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ABSTRACT

For the reason that the recent trend of high data-rate transmission operating at V-band, this thesis aims at the design of a low-power frequency quadrupler on the application of V-band system such as a local oscillator signal for the up-conversion mixer. Moreover, the frequency quadrupler we proposed is by use of sub-harmonic mixing to improve the efficacy. Through the nonlinear analysis in detail and experiment result, we can demonstrate a truth that the generation efficiency is enhanced.

The quadrupler circuit is designed and fabricated in TSMC 90nm CMOS technology. The input center frequency is 12.5 GHz. The measured output power level with an input signal of 8 dBm is -20 dBm(the date contains a loss of 3dB by differential-to-quadrature circuit and a loss of 9.5 dB due to the output buffer.), and the DC power consumption is 2.8mW. In respect of spurs rejection, the corresponding HRRs of f_0. 2 f_0, and 3 f_0 are 53.5, 29.2, and 43 dBc, respectively. In addition, the measure date also verify our proposed architecture get 4 to 7 dB higher than the merely direct generation from the forth-order derivative, which is in a fair comparison

of equal power consumption with each other. Moreover, the DC power consumption is merely 3mW, which is lower than prior works.

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Chapter 1

Introduction

1.1 Background and Motivation

Owing to the advances of wireless communication systems, the operation frequency moves from radio-frequency up to millimeter-wave. The development of millimeter-wave front-end has been prospering in recent research. In general, high-frequency circuits usually need devices with better properties such as SiGe BiCMOS technology. Now utilizing a low-cost and advanced CMOS process is a trend for the integration. Therefore, the circuit we proposed is implemented and fabricatd in tsmc 90-nm CMOS process provided by CIC. A frequency quadrupler with spurs rejection on V-band application such as a local oscillator signal has been designed mainly in this thesis.

Frequency multipliers are widely employed in communication system for providing high frequency signal from a low-noise and low-frequency oscillator. A frequency quadrupler with a frequency multiplication ratio of four is more difficult to realize because the four-order harmonic at 4 f_0 is far from the fundamental frequency and the nonlinear intermodulation product at this frequency is usually lower compared to those at 2 f_0, and 3 f_0. Existing frequency quadrupler are square-wave generators that have filtered output to select the forth-order harmonic at 4 f_0[1][2], this results in poor efficiency since most power is wasted in the undesired terms. For example, in reference[1], The concept is just through driving the strongly non-linear devices to get nonlinear harmonics then filtering out the undesired harmonics. Furthermore, a weak point is its poor spur harmonics rejection because of low quality of output filter

operating at high frequency, especially the spurs around the desired harmonic. Therefore, to achieve the further suppression of spur harmonics inevitably need additional filters.

In conclusion, we try to explore some great technique to efficiently generate this fourfold frequency, and then a method of exploiting the sub-harmonic mixing to enhance generation efficiency is proposed and analyzed. Besides, it shows great reduction in circuit complexity compared with other published works.

1.2 Thesis Organization

In Chapter 2, fundamentals about nonlinear circuit are introduced. Techniques and principles relating to the analysis of nonlinear system are also mentioned.

In Chapter 3, the detailed design and analysis of a frquency quadrupler with spurs rejection is described. We also introduce the Volterra series to analyze the nonlinear behavior.

In Chapter 4, chip implement and measurement result is demonstrated including harmonic response, phase noise, and the verification of efficacy by sub-harmonic mixing.

In Chapter 5, the conclusion and future work of the thesis are given.

Chapter 2

Harmonic Generation by Nonlinear Behavior

2.1 Linearity and Nonlinearity

A fundamental truth of electronic engineering is all electronic circuits are nonlinear. Generally, the linear assumption that underlies most modern circuit theory is practically nearly an approximation. Some circuits, such as small-signal amplifiers, are very weakly nonlinear, and are usually be regarded as linear in systems. However, in these circuits, nonlinear behavior are often crucial factors that degrade system performance and must be minimized. As to some circuits, such as frequency multipliers, exploit the nonlinearities in their circuit elements; these circuits would be hardly implement if nonlinearities did not exist. So the courses of these circuits are often desirable to maximize the effect of the nonlinearities, and even to maximize the effects of annoying linear phenomena. The difficulty of analyzing and designing such circuits is usually more severe than for linear circuits; it is the main subject.

Linear circuits are defined as those which can put the superposition principle into analyzing. Specifically, if excitations x_1 and x_2 are applied separately to a circuit having responses y_1 and y_2, respectively, the response to the excitation ax_1+bx_2 is ay_1+by_2, where a and b are arbitrary constants. This criterion can be applied to either circuits or systems. This definition implies that the response of a linear, time-invariant circuit of system includes only those frequencies present in the excitation waveforms. Thus, linear, time-invariant circuits do not generate new frequencies. As nonlinear circuits usually generate a remarkably large number of new frequency components, this criterion provides an important dividing line between linear and nonlinear

circuits.

Nonlinear circuits are often characterized as either strongly nonlinear or weakly nonlinear. Although these terms have no precise definitions, a good working distinction is that a weakly nonlinear circuit can be described with adequate accuracy by a Taylor series expansion of its nonlinear current/voltage (I/V), charge/voltage (C/V), or flux/current (Φ/I) characteristic around some bias current or voltage. This definition implies that the characteristic is continuous, has continuous derivatives, and for most practical purposes, does not require more than a few terms in its Taylor series. Virtually all transistors and passive components satisfy this definition if the excitation voltages are well within the component's normal operating ranges; that is, below saturation.

2.2 Harmonic Generation

2.2.1 Single-frequency Excitation

We will first describe the frequency spectrum at the output of the test circuit when it is excited with one sinusoidal source at a frequency ω_1. When the amplitude A_1 of the input signal is small enough, then the output spectrum of the circuit only contain one frequency component above the noise floor, this is to say, the response corresponding to the circuit's linear behavior. This is a signal at the same frequency of the input signal, called the fundamental frequency. The amplitude of this signal change proportionally with the input amplitude.

When the input amplitude increased, the output spectrum contains signals at the frequencies $2\omega_1$ and $3\omega_1$, and these signals called the second and third harmonics, originate from second- and third-order nonlinear circuit behavior. Respectively, as we shall see below. Harmonics higher than the third, caused by higher-order behavior,

come above the noise floor at even higher input amplitudes. It is seen that the amplitude of the *n*th harmonic increases with the *n*th power of the input amplitude: an increase of the input amplitude with 6dB yields an increase of the second harmonic at the output with 12dB, the third harmonic increases with 18dB and so on. At high input amplitudes, this is not true anymore. Then it is observed that the third-order nonlinear behavior also give rise to a component at the fundamental frequency which increases with the third power of the input amplitude. As a result, the fundamental response can increase faster than linear, which for an amplifier means that the gain slightly increase. In this case one speak about gain expansion. On the other hand, if the increase is less than linear because the sign of the third-order contribution is opposite to the sign of the linear response, then a gain compression is observed in the output. Similarly, forth-order behavior gives a contribution to the second harmonic and so on. This situation is depicted in Figure 2.1. Signals caused by nonlinear behavior of order higher than five are not shown in this figure. Also it must be noted that a component at 0Hz is found at the output. This DC shift is caused by second-order, forth-order, or in general, even-order nonlinear behavior.

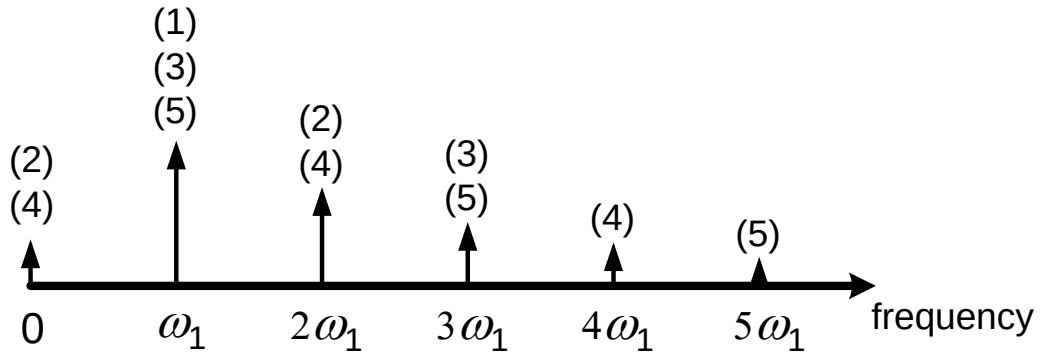


Figure 2.1 The differential harmonics at the output of an analog circuit excited by a sinusoidal signal at frequency ω_1. The numbers between brackets indicate the order of nonlinear behavior by which the signal is determined.

The nonlinear behavior as discussed above in a qualitative way can be clarified mathematically with a simple example. Assume that the relationship between the input signal $x(t)$ (which is either a current or a voltage) of a circuit and the output $y(t)$ is given by the following relationship

$$y(t) = K_1 \cdot x(t) + K_2 \cdot \left(x(t)\right)^2 + K_3 \cdot \left(x(t)\right)^3 + \ldots \tag{2.1}$$

When the input-output relationship is given explicitly by an analytic relationship

$$y(t) = f(x(t)) \tag{2.2}$$

Then the coefficients $K_1, K_2, K_3, \ldots$ can be identified with the coefficients of a Taylor series of f:

$$K_1 = \frac{df}{dx} \tag{2.3}$$

$$K_2 = \frac{1}{2} \cdot \frac{d^2 f}{dx^2} \tag{2.4}$$

$$K_3 = \frac{1}{6} \cdot \frac{d^3 f}{dx^3} \tag{2.5}$$

The coefficient K_1 describes the behavior of the linearized circuit. This behavior is often referred to as first-order behavior. The coefficients $K_2, K_3, \ldots$ are called second-order and third-order nonlinearity coefficients, respectively, in general, high-order nonlinearity coefficients.

Returning to our example, we assure that the input signal $x(t)$ has the form

$$x(t) = A\cos(\omega_1 t + \alpha_1) \tag{2.6}$$

Substituting this expression into equation (2.4) yields the output $y(t)$:

$$y(t) = AK_1 \cos(\omega_1 t + \alpha_1) + A^2 K_2 \left(\frac{1}{2} + \frac{1}{2}\cos(2\omega_1 t + 2\alpha_1)\right)$$
$$+ A^3 K_3 \left(\frac{3}{4}\cos(\omega_1 t + \alpha_1) + \frac{1}{4}\cos(3\omega_1 t + 3\alpha_1)\right) \tag{2.7}$$

It is seen that the second-order coefficient K_2 give rise to a signal at $2\omega_1$ and at 0Hz. Both signals are proportional to K_2 and to the square of the input amplitude A.

Therefore, these signals are denoted as second-order signals. And the third-order signals at the frequency $3\omega_1$ and at the fundamental frequency ω_1 are with the same reason. Assure K_3 has the same sign as K_1, in this case the third-order signal at the fundamental frequency as the same sign at the first-order signal. In other words, the amplitude of the fundamental signal has increased due to third-order behavior. This situation corresponds to expansion. If K_1 and K_3 have an opposite sign then we have compression.

2.2.1 Two-frequency Excitation

In the same way as in the previous section, the test circuit under consideration is now excited with two sinusoids $A_1\cos(\omega_1 t)$ and $A_2\cos(\omega_2 t)$, both applied at the same input port. When A_1 and A_2 are sufficiently low, the output spectrum contains two signals above the noise floor at the fundamental frequency ω_1 and ω_2 due to the circuit's linear behavior. Because in a linear circuit the superposition principle is valid, the two excitations don't produce any interfering signal. However, When A_1 and A_2 become larger, then, apart from the harmonics of ω_1 and ω_2, interfering signals grow above the noise floor at the frequency $\omega_1+\omega_2$, $|\omega_1-\omega_2|$, $2\omega_1+\omega_2$, $|2\omega_1-\omega_2|$, $\omega_1+2\omega_2$ and $|-\omega_1+2\omega_2|$. The signals at $|\omega_1 \pm \omega_2|$ are caused by second-order nonlinear behavior and are called second-order intermodulation products. They increase with the first power of both A_1 and A_2. The other signals come from third-order behavior and are denoted as third-order intermodulation products. The signals at $|\omega_1 \pm 2\omega_2|$ increase with the square of A_1 and with the first power of A_2, and so on.

For analog circuits such as amplifiers, the intermodulation products are usually unwanted. Therefore, they are denoted as intermodulation distortion. In communication circuits, these unwanted products are often denoted as spurious responses. Then consider again the test circuit with the input-output relationship given

by equation (2.1). When the input signal x(t) consists of two signals of equal amplitude and with a different frequency ω_1 and ω_2:

$$x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t) \tag{2.8}$$

Then the different responses are shown in Figure 2.2. It is assumed that the amplitude A is sufficiently low such that the circuit behaves in a weakly nonlinear way. The frequency w1 and w2 are have been given the value 2π*10 *MHz* and 2π*11 *MHz.* It is seen that harmonics of ω_1 and ω_2 are present at the output as well as intermodulation products.

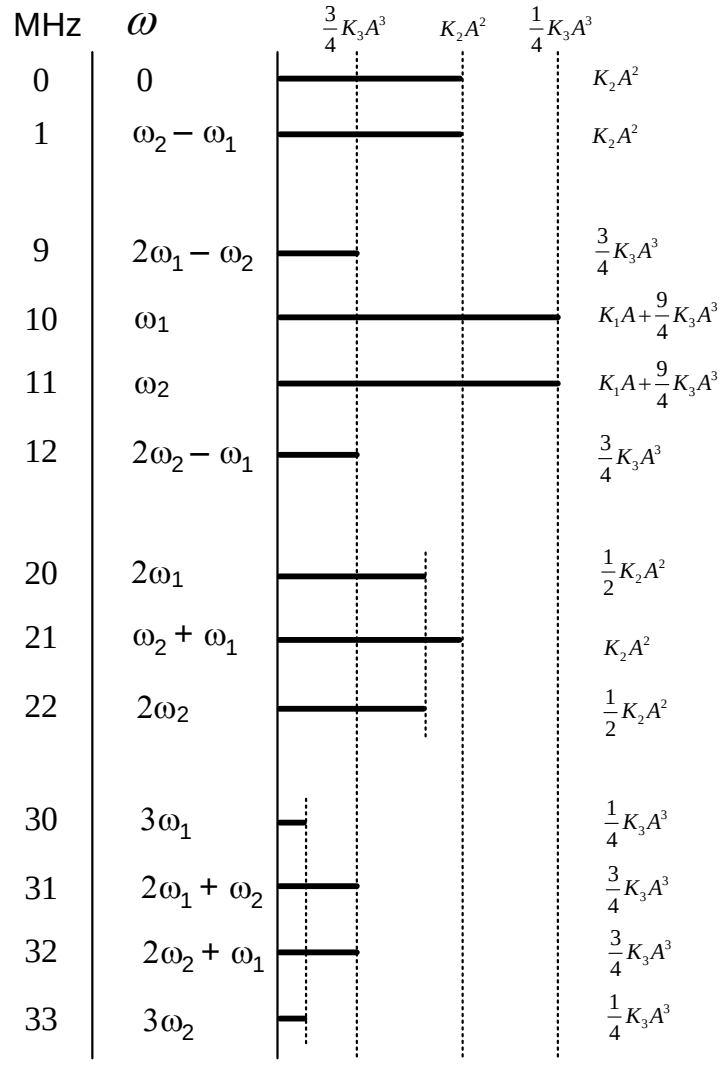


Figure 2.2: The different frequency components at the output of a weakly nonlinear circuit with the input-output relationship given by equation (2.1) to a combination of two sinusoidal signals with the same amplitude A. The frequency of the two input signals are 10 MHz and 11 MHz.

2.3 Description of Nonlinearities in Analog Integrated Circuits

prior to the analysis of nonlinear behavior of analog circuits, it is necessary to describe the nonlinear devices that are present in analog circuits. The devices most commonly used in silicon analog integrated circuits are transistors, resistors, capacitors and diodes. In circuit analysis the devices mentioned above are described using an equivalent circuit. This equivalent circuit can be as simple as one circuit element (e.g. one resistor), or it consist of several circuit elements (e.g. transistor). The elements of such equivalent circuit are nonlinear in general. The following circuit elements are used in analog integrated circuits as a part of the equivalent circuit of a device.

- A nonlinear conductance: the current through this element is an algebraic function of the voltage over the element.
- A nonlinear transconductance: the current through this element is an algebraic function of a voltage other than the voltage over the element.
- A nonlinear resistance: the voltage over this element is an algebraic function of the current through this element.
- A nonlinear transresistance: the voltage over this element is an algebraic function of a current different from the current through this element.
- A nonlinear capacitance: the charge on this element is an algebraic function of the voltage across the element.
- A nonlinear transcapacitance: the charge on this element is an algebraic function of the voltage across the element.

These circuit elements are referred to as basic nonlinearities, since they are the building elements for nonlinear equivalent circuits of devices such as transistor,

diodes, integrated resistors,... Nonlinear voltage-controlled voltage sources and current-controlled current sources are seldom used in equivalent circuits of devices in analog integrated circuits.

2.3.1 Power Series Description of Basic Nonlinearities

A power series description of a basic nonlinearity contains the derivatives of the output quantity (current or voltage) with respect to the controlling quantities. These derivatives are evaluated in the quiescent point. An accurate description of a nonlinear device in terms of power series requires that the different derivatives that are considered be accurate. These derivatives are a function of the controlling quantities and of the model parameters that describe the nonlinear device. The main nonlinearities in transistor are transconductances, then we look into the derivation of the nonlinear coefficients as following sections.

2.3.2 Nonlinear Transconductance

For a nonlinear transconductance, the current through the element $i_{OUT}(t)$, is a nonlinear function f of the controlling voltage $v_C(t)$ elsewhere in the circuit. This function can be expanded into a power series around the quiescent point $I_{OUT} = f(V_C)$:

$$i_{OUT}(t) = f(v_C(t)) = f(V_C + v_c(t))$$

$$= f(V_C) + \sum_{k=1}^{\infty} \frac{1}{k!} \frac{\partial^k f(v(t))}{\partial v^k}\bigg|_{v=V_C} \cdot v_c^k(t) \qquad (2.9)$$

In this equation $i_{OUT}(t)$ is the total value of the current, which is the sum of the DC and the AC current. The voltage $v_c(t)$ is the AC voltage that controls the conductance. The second term in equation (2.9) is a power series representing the AC part of the current. When the analysis of a circuit that contains a nonlinear conductance is limited to first- second- and third-order nonlinear behavior, then the power series in equation

(2.9) can be broken down after the third term.

Defining the following coefficients

$$g_1 = \left.\frac{\partial f(v)}{\partial v}\right|_{v=V_C} \tag{2.10}$$

$$K_{2,g_1} = \left.\frac{1}{2!}\cdot\frac{\partial^2 f(v)}{\partial v^2}\right|_{v=V_C} \tag{2.11}$$

$$K_{3,g_1} = \left.\frac{1}{3!}\cdot\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_C} \tag{2.12}$$

In which we omitted the time dependence for simplicity, and in general

$$K_{n,g_1} = \left.\frac{1}{n!}\cdot\frac{\partial^n f(v)}{\partial v^n}\right|_{v=V_C} \tag{2.13}$$

Leads to the expression of the AC current through the conductance

$$i_{OUT}(t) = g_1 \cdot v_c(t) + K_{2,g_1}\cdot v_c^2(t) + K_{3,g_1}\cdot v_c^3(t) + \ldots \tag{2.14}$$

In this expression, g_1 is the small-signal transconductance of the linearized circuit. The coefficients in the second and third term, $K_{2,g1}$ and $K_{3,g1}$ are respectively the second- and third-order nonlinearity coefficients that describe the nonlinear element. Similarly, the small-signal conductance is often referred to as the first-order coefficient. The subscript for K_2 and K_3 is the symbol that represents the linearized element, in this case g_1.

2.3.3 Two-dimensional Transconductance

A two-dimensional transconductance is an element the current of which is controlled by two different voltage. In other words, the current $i_{OUT}(t)$ is a function f of two voltages u_C and v_C, which can be expressed in terms of AC values using a two-dimensional power series expression around the quiescent point $I_{OUT}=f(U_C,V_C)$

$$i_{OUT}(t) = f\left(u_C(t), v_C(t)\right) = f\left(U_C + u_c(t), V_C + v_c(t)\right)$$

$$= f\left(U_C, V_C\right) + \sum_{m=1}^{\infty}\sum_{n=0}^{\infty}\left[\left.\frac{\partial^m f(u,v)}{\partial u^n \partial v^{m-n}}\right|_{\substack{u=U_C \\ v=V_C}} \cdot \frac{u_c^n(t)}{n!} \cdot \frac{v_c^{m-n}(t)}{(m-n)!}\right] \tag{2.15}$$

The AC part of the current corresponds to the second term of equation(2.15), which is a two-dimensional power series. This series can be split into three series i_1, i_2 and i_3, each corresponding to a part of the total AC current.

$$i_1 = g_1 \cdot u_c + K_{2,g_1} \cdot u_c^2 + K_{3,g_1} \cdot u_c^3 + \ldots \tag{2.16}$$

$$i_2 = g_2 \cdot v_c + K_{2,g_2} \cdot v_c^2 + K_{3,g_2} \cdot v_c^3 + \ldots \tag{2.17}$$

The time dependence of u_c and v_c has been omitted for simplicity. The third series, i_3, contains nothing but cross-terms, which are terms that contain a nonzero power of both u_c and v_c.

$$i_3 = K_{2,g_1\&g_2} \cdot u_c \cdot v_c + K_{3,2g_1\&g_2} \cdot u_c^2 \cdot v_c + K_{3,g_1\&2g_2} \cdot u_c \cdot v_c^2 \tag{2.18}$$

The meaning of the subscripts in the nonlinearity coefficients defined above is as follows. Suppose that the first-order derivative of the total current with respect to u and v are respectively g_1 and g_2. Then a coefficient like $K_{m,jg1\&(m-j)g2}$ with m and j positive integers and $m > j$ means

$$K_{m,jg_1\&(m-j)g_2} = \frac{\partial^m f(u,v)}{\partial u^j \partial v^{m-j}} \cdot \frac{1}{j!} \cdot \frac{1}{(m-j)!} \tag{2.19}$$

2.3.4 Three-dimensional Transconductance

A three-dimensional transconductance is a current source that is controlled by three voltage. In other words, the current is a function f of three voltage $u(t)$, $v(t)$, and $w(t)$. Using a power series expansion around the quiescent value of the current can be split into a quiescent part $I_{OUT} = f(U_C, V_C, W_C)$ and an AC part. This AC part is given by

$$i_{OUT}(t) = f(U_C, V_C, W_C) +$$

$$\sum_{k=1}^{\infty}\sum_{i=0}^{k}\sum_{j=0}^{k-i}\left[\left.\frac{\partial^k f(u,v,w)}{\partial u^i \partial v^j \partial w^{k-i-j}}\right|_{\substack{u=U_C \\ v=V_C \\ w=W_C}} \cdot \frac{u_c^i(t)}{i!} \cdot \frac{v_c^j(t)}{j!} \cdot \frac{w_c^{k-i-j}(t)}{(k-i-j)!}\right] \tag{2.20}$$

The AC current can be split into distinct parts, and this series implies the introduction of the following nonlinearity coefficients.

$$K_{m,j,k} = \frac{\partial^m f(u,v,w)}{\partial u^j \partial v^k \partial w^{m-j-k}} \cdot \frac{1}{j!} \cdot \frac{1}{k!} \cdot \frac{1}{(m-j-k)!} \tag{2.21}$$

2.3.5 Example: Drain Current of A MOS Transistor

The meaning of the newly defined coefficients is illustrated with a simple model for the drain current of an nMOS transistor in saturation. Taking into account bulk effect and Early effect, the drain current is given by

$$i_D = \frac{K_P}{2}\frac{W}{L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}) \tag{2.22}$$

with

$$V_T = V_{TO} + \gamma\left(\sqrt{v_{SB} + \phi} - \sqrt{\phi}\right) \tag{2.23}$$

The parameter λ, γ, and ϕ are the channel-length modulation factor, the body-effect coefficient and the surface inversion potential, respectively. The first derivatives of the current with respect to the controlling voltage v_{GS}, v_{BS}, and v_{DS} are the small-signal parameters g_m, g_{mb}, g_o. Then from above equations the AC current is given by:

$$
\begin{aligned}
i_d = {} & g_m \cdot v_{gs} + K_{2,g_m} \cdot v_{gs}^2 + K_{3,g_m} \cdot v_{gs}^3 + \ldots \\
& + g_o \cdot v_{ds} + K_{2,g_o} \cdot v_{ds}^2 + K_{3,g_o} \cdot v_{ds}^3 + \ldots \\
& + g_{mb} \cdot v_{bs} + K_{2,g_{mb}} \cdot v_{bs}^2 + K_{3,g_{mb}} \cdot v_{bs}^3 + \ldots \\
& + K_{2,g_m \& g_{mb}} \cdot v_{gs} \cdot v_{bs} + K_{3,2g_m \& g_{mb}} \cdot v_{gs}^2 \cdot v_{bs} + K_{3,g_m \& 2g_{mb}} \cdot v_{gs} \cdot v_{bs}^2 + \ldots \\
& + K_{2,g_m \& g_o} \cdot v_{gs} \cdot v_{ds} + K_{3,2g_m \& g_o} \cdot v_{gs}^2 \cdot v_{ds} + K_{3,g_m \& 2g_o} \cdot v_{gs} \cdot v_{ds}^2 + \ldots \\
& + K_{2,g_{mb} \& g_o} \cdot v_{bs} \cdot v_{ds} + K_{3,2g_{mb} \& g_o} \cdot v_{bs}^2 \cdot v_{ds} + K_{3,g_{mb} \& 2g_o} \cdot v_{sb} \cdot v_{ds}^2 + \ldots \\
& + K_{3,g_m \& g_{mb} \& g_o} \cdot v_{gs} \cdot v_{bs} \cdot v_{ds} + \ldots
\end{aligned}
\tag{2.24}
$$

In this equation, the first three line correspond to series that describe the dependence of the AC drain current on one single AC voltage. The following three lines represent the variation of the current when two voltages change at the same time. The last line describes the variation of the current with the three controlling voltages at the same of the three-dimensional drain current in general requires sixteen second- and third- order coefficients. Table 2.1 lists the expressions for the coefficients that describe the nonlinearity of the drain current according to equation 2.24, and only shows coefficients with respect to g_m.

g_m	K_{2,g_m}	K_{3,g_m}	$K_{2,g_m \& g_{mb}}$	$K_{2,g_m \& g_{mo}}$
$\frac{\partial i_D}{\partial v_{GS}}$	$\frac{1}{2} \cdot \frac{\partial^2 i_D}{\partial v_{GS}^2}$	$\frac{1}{6} \cdot \frac{\partial^3 i_D}{\partial v_{GS}^3}$	$\frac{\partial^2 i_D}{\partial v_{GS} \partial v_{BS}}$	$\frac{\partial^2 i_D}{\partial v_{GS} \partial v_{DS}}$
$K_{3,g_m \& 2g_{mb}}$	$K_{3,g_m \& 2g_o}$	$K_{3,2g_m \& g_{mb}}$	$K_{3,2g_m \& g_o}$	$K_{3,g_m \& g_{mb} \& g_o}$
$\frac{1}{2} \cdot \frac{\partial^3 i_D}{\partial v_{GS} \partial v_{BS}^2}$	$\frac{1}{2} \cdot \frac{\partial^3 i_D}{\partial v_{GS} \partial v_{DS}^2}$	$\frac{1}{2} \cdot \frac{\partial^3 i_D}{\partial v_{GS}^2 \partial v_{BS}}$	$\frac{1}{2} \cdot \frac{\partial^3 i_D}{\partial v_{GS}^2 \partial v_{DS}}$	$\frac{1}{6} \cdot \frac{\partial^3 i_D}{\partial v_{GS} \partial v_{BS} \partial v_{DS}}$

Table 2.1 Definition of the nonlinearity coefficients of the drain current of a nMOS transistor.

Chapter 3

A Frequency Quadrupler with Spur Harmonics Suppression

3.1 Introduction

Active frequency multipliers are utilized in numerous applications to efficiently provide a source of high frequency microwave energy. They are commonly used in communication systems to enable frequency translation of a signal from a low-noise and low-frequency oscillator to the required higher frequency band for the purpose of up/down conversion in transceivers.

In general, frequency quadrupler and higher order multipliers have not seen more prominence and detailed investigation than doublers and triplers, due to higher circuit complexity and lower achievable conversion gain and efficiency. Therefore, at first we inspect some published works about quadrupler.

Begin with the work pronounced by professor Huei Wang, proceedings of 2010 *EuMC* conference[1]. The circuit schematic is shown in figure 3.1. A single-stage V-band frequency quadrupler is proposed and manufactured in 0.25-μm SiGe BiCMOS technology. The maxima output power is -10 dBm with 11.7 mW dc power consumption. The concept is through driving the strongly non-linear devices to get nonlinear harmonics then filtering out the undesired harmonics. The conversion efficiency is poor by this approach. Another weak point is its poor spur-harmonic rejection of output signal because of low quality of output filter operating at high frequency, especially the spurs around the desired harmonic. In the design of frequency quadrupler, the third-order spur harmonic at frequency $3f_0$ is in particular

hard to suppress. The measured dates shown in figure 3.2 clearly shows the poor harmonic rejection, especially the spur at $3f_0$. Therefore, to achieve the further suppression of spur harmonics inevitably need additional filters. It is an inconvenient concern. According to the paper, the merit of the circuit is the 36% bandwidth from 52 to 75 GHz. In my opinion, it takes advantages of the strongly non-linear devices of SiGe BiCMOS technology, and by large input signal to make the output power achieve the saturation point in the frequency band.

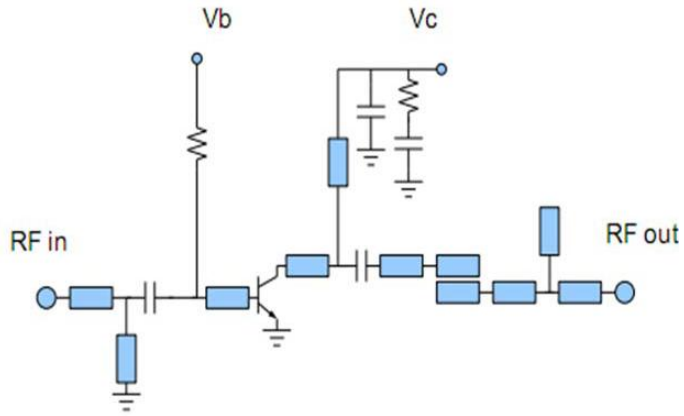


Figure 3.1 The quadrupler circuit schematic of reference[1].

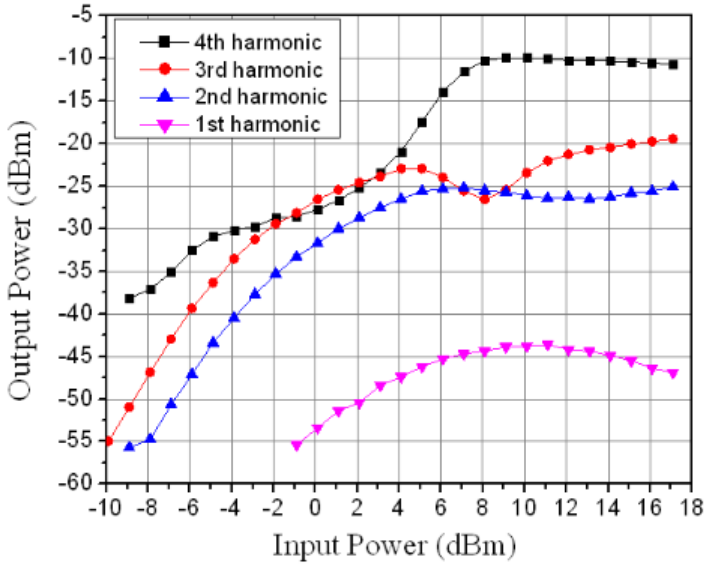


Figure 3.2 Measurement date of reference[1].

Next, the work pronounced by Infineon Technologies AG, proceedings of 2009 *EuMIC* conference[3]. This work is manufactured in a Silicon-Germanium production

technology, and the schematic is shown in figure 3.3. The DC consumption of this quadrupler is 43mW from 3.5 V supply voltage and RF output power is -5dBm at frequency 77GHz. From my point of view, it is a good work. The structure is using two doublers stacked one by one. Therefore, the cost is higher supply voltage for stacking, and the requirement of quadrature input signal for each Gibert mixer operation. So the circuit contains several TRLs for 90 degree phase shifting which increases the complexity of design and chip area, especially when operating in lower frequency application.

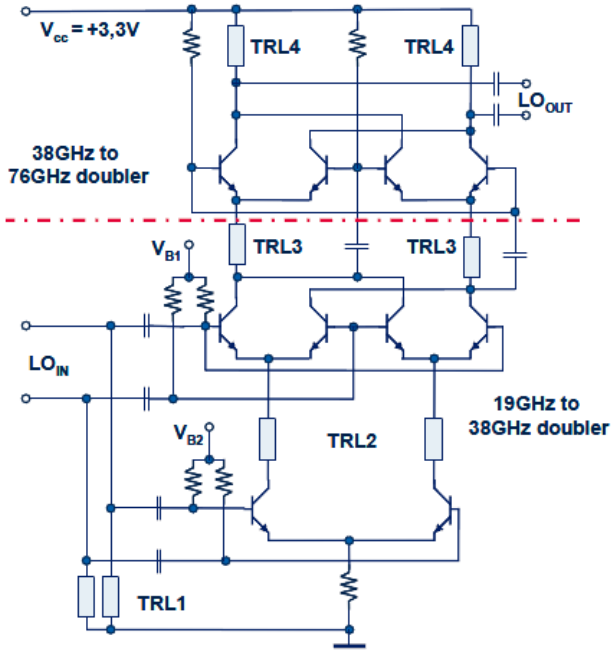


Figure 3.3 Stacked quadrupler of reference[3].

Next, the work pronounced by professor Euisik Yoon, proceedings of 2005 *TMTT*[2]. The schematic shown in figure 3.4 is manufactured in a 0.18- μm CMOS process. The DC consumption of the quadrupler is 106mW with 1.8V VDD and it has -18 dBm RF output power at frequency 40 GHz. Apparently, the focal point of this paper is not with an emphasis on the quadrupler. It merely contains four transistors biased at the maxima forth-order derivative of transconductance. The disadvantages

are high power consumption and low conversion efficiency. Although the design do not have any particularity, except for the linear superposition. It let us think of some possibilities that can upgrade the circuit.

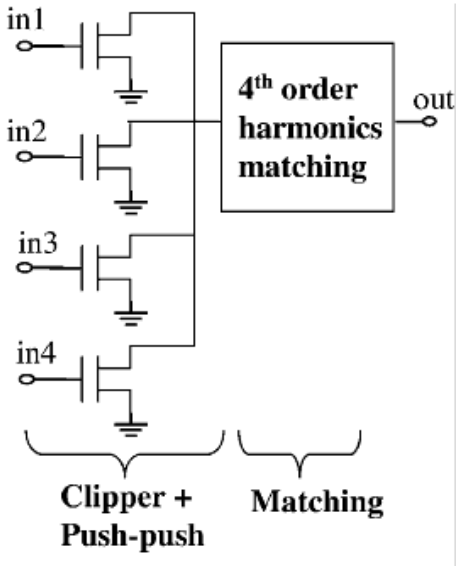


Figure 3.4 Quadrupler schematic of reference[2].

Finally, in this work, a new technique of generating the forth-order harmonic at $4f_0$ is proposed and analyzed. It improves the generating efficiency by not only direct generation, but also mixing generation. Applying this technique, frequency $4f_0$ can be generated under low power consumption and the circuit itself is uncomplicated compared with other published methods. Analytical equations were developed to approximate the numerically-converged results of CAD tools for optimization with paper and hand calculation. Detailed analyses were done to maximize the frequency $4f_0$ and suppress the undesired harmonics. According to the experimental results, the output power of proposed quadrupler is -20dBm (contained 9.5 dB loss of the output buffer) under only 4.5 mW dynamic power consumption with fundamental input power of +8 dBm. The proposed quadrupler is fabricated using TSMC 90-nm low-leakage CMOS technology for the verification of theoretical results.

In Section 3.2, the architecture of the proposed quadrupler is introduced preliminarily. The nonlinear analysis by Voterra series are presented in Section 3.3. The design procedure of the proposed quadrupler is illustrated in Section 3.4, including the design of quadrature all pass filter.

3.2 A Proposed Architecture of Frequency Quadrupler

In the last section we saw several types of methods to devise a quadrupler. Principally, you can find some issues which dominate the performances such as power consumption, harmonic rejection ratio(HRR), and conversion gain...etc. But however, a technique which can advance the performance in all aspects is nearly impossible. When a technique can improve some quality, a drawback maybe emerges at the same time. Consequently, ameliorating the drawback is the target for all designers. Return to the topic, in the beginning we should determine what features are our desires. Apart from low power consumption being a trend, perfect HRR is a significant criterion for multipliers. Because a multiplier with perfect HRR can avoid connecting superfluous filters after the output, especially when operating at high frequency. We have studied several examples of the quadruplers, and the best way to eliminate the spur harmonics is by cancellation instead of oppression. Some methods similar to filtering have difficulties handling the spurs adjacent to the desired harmonic. For the quadrupler the spur harmonics at $3f_0$ and $5f_0$ are hardly suppressed by filtering. But cancellation can thoroughly eliminate spurs. Consequently, to accomplice lower power consumption and great HRR, we take sub-harmonic mixers and quadrature input signals as the first step and the circuit is shown in figure 3.5; as we have known, the design is mainly due to biasing properly to maximize the forth-order derivative of transconductance (gm_4). In addition, the merit of this structure is perfect spur cancellation of responses

f_0, $2f_0$, and $3f_0$..., but the cost is the preparation of quadrature input signals. Furthermore, its conversion gain is poor, the direct generation for $4f_0$ is not powerful after all. On the whole, if we can maintain the merits of lower power consumption and perfect HRR, and then find a method to upgrade the output power of $4f_0$, the project will be worth doing.

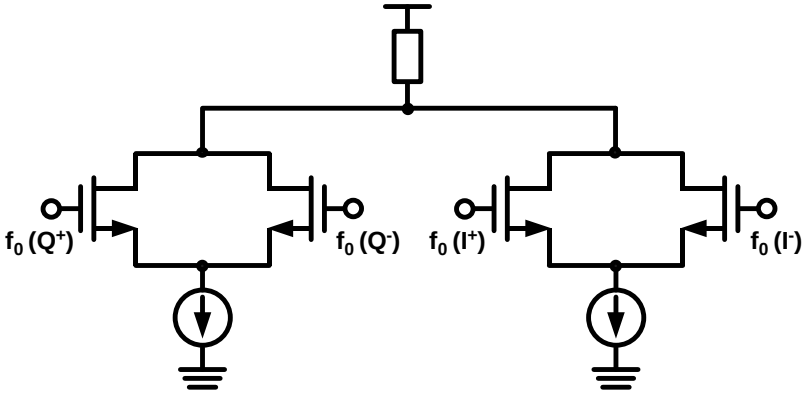


Figure 3.5 A typical quadrupler by way of direct generation.

The proposed architecture is shown in figure 3.6. Figure 3.6(a) describes the concept of the circuit in figure 3.5. The fundamental signal f_0 through nonlinear devices to directly generate the signal $4f_0$. Figure 3.6(b) shows an idea to upgrade the amount of $4f_0$, which start with the direct generation and then we add a way of sub-harmonic mixing. The idea of circuit implementation may be shown in figure 3.7. It clearly reveals that the current sinks now provide not only DC bias current, but also AC injection current at frequency $2f_0$. In other words, as far as possible no additional DC power are required to yield this AC injection current. However, the question is how much benefit we gained by this sub-harmonic mixing.

By way of some nonlinear analysis we can explain how it works theoretically. Such as Volterra series, which is a mathematic approach, can help us comprehend the nonlinear behavior in more detail. So the section 3.3 will discuss the solutions of Volterra series to analyze the circuit like as figure 3.7. On the other hand, if you have

understood the Volterra series more or if you merely intend to know the design methods, you can pass over the next section and move on to the section 3.4 directly. In Section 3.4 we will carry on the design procedure of the proposed quadrupler.

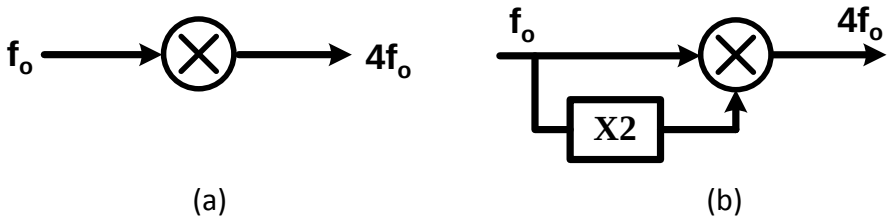


Figure 3.6 The architecture of proposed quadrupler.

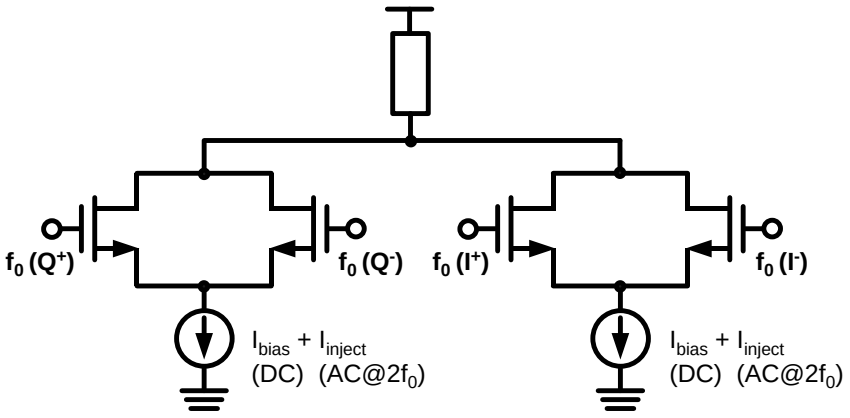


Figure 3.7 The concept of circuit implementation of the proposed quadripler.

3.3 Nonlinear Analysis of Sub-harmonic Mixing

In this section we study how to analyze the weakly nonlinear behavior of analog integrated circuit. When we use simulation tool to get the response of output harmonics, simulation results can not clearly present information of how the circuit works. As we all know, nonlinear behavior due to the physical structure is complicated. General simulation tools use BSIM4 model to consider and compute the

behavior of a MOS transistor. By this meticulous model we could get the precise simulation results, but it can not clearly tell us each contribution and how it generates. A mathematic approximately model such as Volterra series can help us get some information in more detail.

Volterra series describe the output response of a nonlinear system as the sum of the harmonics of a first-order operator, a second-order one, a third-order one, and so on. Every operator is describe either in the time domain or in the frequency domain with a kind of transfer function, called Volterra kernel. In principles, the method of Volterra series describing a nonlinear system is as like the way that Taylor series approximate an analytic function. The higher input amplitude, the more terms of series need to be taken into account in order to have precise representation of the system. For very high amplitude, the series diverges, just as Taylor series. The most difference between Taylor series and Volterra series is the ability to deal with a circuit with memory. Volterra series can analyze the memory circuit including the inductors and capacitors which retain phase information, but Taylor series can not. It deals with a memory-less circuit more properly.

For a one-port system, Volterra kernel can be computed to get the output response for any input signal. However, for multiple-port circuit, Volterra kernel become formation of tensors, so the calculation also become more arduous. Now a direct calculation method (DCM), a variant Volterra series approach, directly calculates the required response repeatedly so that it does not make use of tensors. The DCM calculate the nonlinear response at desired frequency directly, and if you want to obtain another response at other frequency, nearly calculate repeatedly. For mixer circuits, such as Gilbert mixer, they are two-port system with two inputs of signal RF and signal LO. Therefore, the DCM is more appropriate for the nonlinear analysis. The nonlinear analysis of the sub-harmonic mixer shown in figure 3.8 (not

including bias circuit) is implemented with DCM. As we have mentioned in the last section, this is a half-circuit of the proposed quadrupler. Figure 3.9 shows its equivalent circuit for nonlinear analysis. The circuit is excited by three different input ports, $v_{RF1}(t)$ and $v_{RF2}(t)$ which are differential signals in principle are at frequency ω_{RF}, and $i_{LO}(t)$ is at frequency ω_{LO}, respectively.

$$v_{RF1}(t) = \mathrm{Re}\left(V_{RF1}e^{j\omega_{RF}t}\right) \tag{3.1}$$

$$v_{RF2}(t) = \mathrm{Re}\left(V_{RF2}e^{j\omega_{RF}t}\right) \tag{3.2}$$

$$i_{LO}(t) = \mathrm{Re}\left(I_{LO}e^{j\omega_{LO}t}\right) \tag{3.3}$$

Under steady-state conditions, every node voltage $v_x(t)$ consists of harmonics and intermodulation of signal RF and signal LO as shown in equation (3.4).

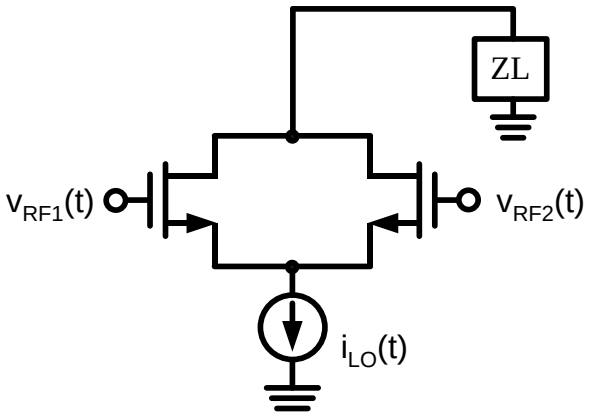


Figure 3.8 The sub-harmonic mixer, which is the half circuit of the proposed quadrupler with the differential-pair topology.

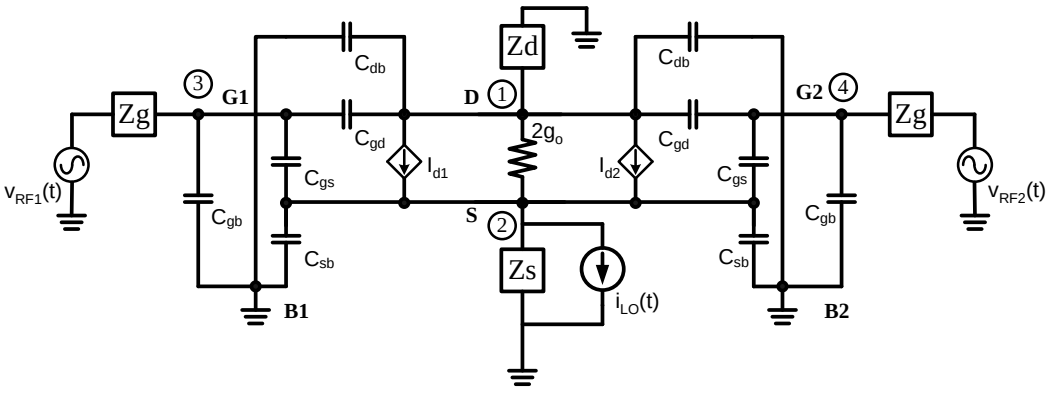


Figure 3.9 The equivalent circuit for nonlinear analysis.

$$v_x(t) = \mathrm{Re}\left(V_{x,10}e^{j\omega_{RF}t}\right) + \mathrm{Re}\left(V_{x,01}e^{j\omega_{LO}t}\right) + \mathrm{Re}\left(V_{x,20}e^{j2\omega_{RF}t}\right) + \mathrm{Re}\left(V_{x,11}e^{j(\omega_{RF}+\omega_{LO})t}\right) + \mathrm{Re}\left(V_{x,20}e^{j2\omega_{LO}t}\right) + \ldots\ldots$$
$$= \frac{1}{2}\sum_{m,n=-\infty}^{\infty} V_{x,mn}e^{j(m\omega_{RF}+n\omega_{LO})t} \qquad , x = 1,2,3,4 \tag{3.4}$$

where $v_{x,mn}$ denotes the voltage at the node x at frequency $m\omega_{RF}+n\omega_{LO}$. The first thing in this section is to explain the way to compute the complex phasor $V_{x,mn}$. We define the matrix $U(t)$ as the matrix of each node's voltage responses shown in equation (3.5) ,and this is not including parameters concerning negative frequency.

$$U(t) = \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \\ v_4(t) \end{bmatrix} = \begin{bmatrix} V_{1,10} & V_{1.01} \\ V_{2,10} & V_{2.01} \\ V_{3,10} & V_{3.01} \\ V_{4,10} & V_{4.01} \end{bmatrix} \begin{bmatrix} \frac{1}{2}e^{j\omega_{RF}t} \\ \frac{1}{2}e^{j\omega_{LO}t} \end{bmatrix} + \begin{bmatrix} V_{1,20} & V_{1,11} & V_{1,02} \\ V_{2,20} & V_{2,11} & V_{2,02} \\ V_{3,20} & V_{3,11} & V_{3,02} \\ V_{4,20} & V_{4,11} & V_{4,02} \end{bmatrix} \begin{bmatrix} \frac{1}{2}e^{j2\omega_{RF}t} \\ \frac{1}{2}e^{j(\omega_{LO}+\omega_{RF})t} \\ \frac{1}{2}e^{j2\omega_{LO}t} \end{bmatrix} + \ldots$$
$$= \begin{bmatrix} U_{10} & U_{01} \end{bmatrix} \begin{bmatrix} \frac{1}{2}e^{j\omega_{RF}t} \\ \frac{1}{2}e^{j\omega_{LO}t} \end{bmatrix} + \begin{bmatrix} U_{20} & U_{11} & U_{02} \end{bmatrix} \begin{bmatrix} \frac{1}{2}e^{j2\omega_{RF}t} \\ \frac{1}{2}e^{j(\omega_{LO}+\omega_{RF})t} \\ \frac{1}{2}e^{j2\omega_{LO}t} \end{bmatrix} + \ldots \tag{3.5}$$

The drain current is a function of v_{ds}, v_{ds}, and v_{bs} so that it can be expanded by a three-dimensional power series as be shown in equation (2.24), rewrite in equation (3.6) and high orders are omitted.

$$\begin{aligned} i_d = & \underbrace{g_m \cdot v_{gs} + g_{mb} \cdot v_{bs} + g_o \cdot v_{ds}}_{\text{First-order}} \\ & \underbrace{+ K_{2,g_m} \cdot v_{gs}^2 + K_{2,g_{mb}} \cdot v_{bs}^2 + K_{2,g_o} \cdot v_{ds}^2 + K_{2,g_m\&g_{mb}} \cdot v_{gs} \cdot v_{bs} + K_{2,g_m\&g_o} \cdot v_{gs} \cdot v_{ds} + K_{2,g_{mb}\&g_o} \cdot v_{bs} \cdot v_{ds}}_{\text{Second-order}} \\ & \underbrace{+ K_{3,g_m} \cdot v_{gs}^3 + K_{3,g_{mb}} \cdot v_{bs}^3 + K_{3,g_o} \cdot v_{ds}^3 + K_{3,2g_m\&g_{mb}} \cdot v_{gs}^2 \cdot v_{bs} + K_{3,2g_m\&g_o} \cdot v_{gs}^2 \cdot v_{ds}}_{} \\ & \underbrace{+ K_{3,g_m\&2g_{mb}} \cdot v_{gs} \cdot v_{bs}^2 + K_{3,g_m\&2g_o} \cdot v_{gs} \cdot v_{ds}^2 + K_{3,2g_{mb}\&g_o} \cdot v_{bs}^2 \cdot v_{ds} + K_{3,g_{mb}\&2g_o} \cdot v_{sb} \cdot v_{ds}^2}_{} \\ & \underbrace{+ K_{3,g_m\&g_{mb}\&g_o} \cdot v_{gs} \cdot v_{bs} \cdot v_{ds} + \ldots}_{\text{Third-order}} \end{aligned} \tag{3.6}$$

The nonlinear coefficients are defined as equation (2.13), (2.19) and (2.21) for one-, two-, and three- dimensional. Wright again in equation (3.7), (3.8), and (3.9)

$$K_{n,g_1} = \frac{1}{n!} \cdot \frac{\partial^n f(v)}{\partial v^n}\bigg|_{v=V_C} \tag{3.7}$$

$$K_{m,jg_1\&(m-j)g_2} = \frac{\partial^m f(u,v)}{\partial u^j \partial v^{m-j}} \cdot \frac{1}{j!} \cdot \frac{1}{(m-j)!} \tag{3.8}$$

$$K_{m,jg_1\&kg_2\&n(j-k\ g\ )_3} = \frac{\partial^m f(u,v,w)}{\partial u^j \partial v^k \partial w^{m-j-k}} \cdot \frac{1}{j!} \cdot \frac{1}{k!} \cdot \frac{1}{(m-j-k)!} \tag{3.9}$$

3.3.1 First-Order Response

First-order response is linear and can be obtained by Kirchoff's laws. Use the technique of superposition to get the individual response for frequency ω_{RF} and ω_{LO}. For instance, as we calculate the response to the inputs v_{RF1} and v_{RF2} which are at the same frequency ω_{RF}, set i_{LO} to be zero. The AC equivalent circuit is as same as figure 3.2 but i_{LO} taking off. Then make use of Kirchoff's current and voltage laws, we can get four equations at nodes marked ①, ②, ③, and ④, as follow.

① $$\begin{aligned} &sC_{gd}(v_3 - v_1) + sC_{gd}(v_4 - v_1) + 2sC_{db}(-v_1) = \\ &\quad g_m(v_3 - v_2) + g_m(v_4 - v_2) + 2g_{mb}(-v_2) + g_{ZL}v_1 + 2g_o(v_1 - v_2) \end{aligned} \tag{3.10}$$

② $$\begin{aligned} g_{ZS}v_2 = {} & g_m(v_3 - v_2) + g_m(v_4 - v_2) + 2g_{mb}(-v_2) + 2g_o(v_1 - v_2) + \\ & 2sC_{sb}(-v_2) + sC_{gs}(v_3 - v_2) + sC_{gs}(v_4 - v_2) \end{aligned} \tag{3.11}$$

③ $$g_{ZG}(v_{RF1} - v_3) = sC_{gb}v_3 + sC_{gs}(v_3 - v_2) + sC_{gd}(v_3 - v_1) \tag{3.12}$$

④ $$g_{ZG}(v_{RF2} - v_4) = sC_{gb}v_4 + sC_{gs}(v_4 - v_2) + sC_{gd}(v_4 - v_1) \tag{3.13}$$

Make a arrangement and transform the equation into a matrix, write down the matrix equation:

$$\begin{bmatrix} -2\left(sC_{gd}+sC_{db}+g_o\right)-g_{ZL} & 2\left(g_m+g_{mb}+g_o\right) & sC_{gd}-g_m & sC_{gd}-g_m \\ -2g_o & 2\left(g_m+g_{mb}+g_o+sC_{gs}+sC_{sb}\right)+g_{ZS} & -g_m-sC_{gs} & -g_m-sC_{gs} \\ -sC_{gd} & -sC_{gs} & sC_{gb}+sC_{gs}+g_{ZG}+sC_{gd} & 0 \\ -sC_{gd} & -sC_{gs} & 0 & sC_{gb}+sC_{gs}+g_{ZG}+sC_{gd} \end{bmatrix}$$

- $$\begin{bmatrix} v_{1,10} \\ v_{2,10} \\ v_{3,10} \\ v_{4,10} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ g_{ZG}v_{RF1} \\ g_{ZG}v_{RF2} \end{bmatrix} \qquad (3.14)$$

where $s = j\omega_{RF}$

Equation (3.14) can write in a general form:

$$Y\left(j\omega_{RF}\right)\cdot U_{10} = IN_{1,10} \qquad (3.15)$$

and

$$Y(s) = \begin{bmatrix} -2\left(sC_{gd}+sC_{db}+g_o\right)-g_{ZL} & 2\left(g_m+g_{mb}+g_o\right) & sC_{gd}-g_m & sC_{gd}-g_m \\ -2g_o & 2\left(g_m+g_{mb}+g_o+sC_{gs}+sC_{sb}\right)+g_{ZS} & -g_m-sC_{gs} & -g_m-sC_{gs} \\ -sC_{gd} & -sC_{gs} & sC_{gb}+sC_{gs}+g_{ZG}+sC_{gd} & 0 \\ -sC_{gd} & -sC_{gs} & 0 & sC_{gb}+sC_{gs}+g_{ZG}+sC_{gd} \end{bmatrix}$$

$$U_{10} = \begin{bmatrix} v_{1,10} \\ v_{2,10} \\ v_{3,10} \\ v_{4,10} \end{bmatrix} \quad \textit{and} \quad IN_{1,10} = \begin{bmatrix} 0 \\ 0 \\ g_{ZG}v_{RF1} \\ g_{ZG}v_{RF2} \end{bmatrix}$$

where $Y(s)$ is a transconductance matrix. U_{10} is a matrix of the voltage response, and $IN_{1,10}$ is a vector whose only nonzero components are terms in the network equations at frequency ω_{RF}. Then the linear response can be got by the inverse operation. In the same way, the first-order response to the input signal at other frequencies can be identified by the following equations:

$$U_{01} = \begin{bmatrix} v_{1,01} \\ v_{2,01} \\ v_{3,01} \\ v_{4,01} \end{bmatrix} = Y^{-1}\left(j\omega_{LO}\right)\cdot IN_{1,01} = Y^{-1}\left(j\omega_{LO}\right)\cdot \begin{bmatrix} 0 \\ i_{LO} \\ 0 \\ 0 \end{bmatrix} \qquad (3.16)$$

$$U_{-10}=\begin{bmatrix} v_{1,-10} \\ v_{2,-10} \\ v_{3,-10} \\ v_{4,-10} \end{bmatrix}=Y^{-1}\left(-j\omega_{RF}\right)\cdot IN_{1,01}=Y^{-1}\left(-j\omega_{RF}\right)\cdot\begin{bmatrix} 0 \\ i_{LO} \\ 0 \\ 0 \end{bmatrix} \tag{3.17}$$

....

Equation (3.17) states the voltage responses at negative frequency, it is for the requirement of the high-order calculation, we will investigate in the following section.

3.3.2 Second-Order Response

The second-order response can be identified by the information from the first-order. As the same linearized network as the precious step solved again to get matching responses, but the input signal sources are different now. Instead of the external excitation, so-called nonlinear current source of order two must be applied. Each nonlinearity in the equivalent circuit generates a nonlinear current source. This second-order nonlinear current source can be obtained by the following method. We simplify our question by considering only one nonlinear current source at one time. Take nonlinearity $K_{2,\mathrm{gm}}$ for computing at first, the equivalent circuit for the analysis of second-order response is shown in figure 3.3, and we write the nodal equation at node 2 and get the following equation.

$$\begin{aligned} g_{Z_s}v_2 = {} & g_m\left(v_3-v_2\right)+g_m\left(v_4-v_2\right)+2g_{mb}\left(-v_2\right)+2g_o\left(v_1-v_2\right)+ \\ & 2sC_{sb}\left(-v_2\right)+sC_{gs}\left(v_3-v_2\right)+sC_{gs}\left(v_4-v_2\right)+i_{NL2} \end{aligned} \tag{3.18}$$

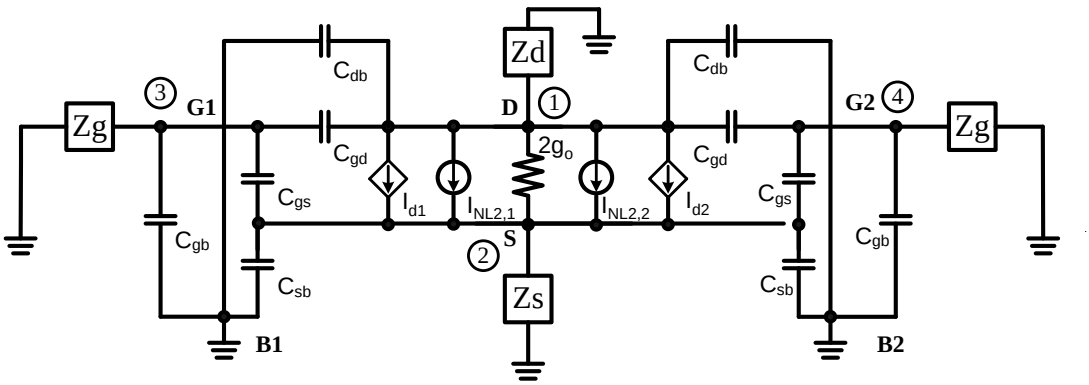


Figure 3.10 The equivalent circuit for the analysis of second-order response.

but here only $K_{2,gm}$ taking into consideration at first time.

and from equation (3.4), we get

$$v_1 = \frac{1}{2}\left[V_{1,10}e^{j\omega_{RF}t} + V_{1,01}e^{j\omega_{LO}t} + V_{1,20}e^{j2\omega_{RF}t} + V_{1,11}^{j(\omega_{RF}+\omega_{LO})t} + V_{1,02}e^{j2\omega_{LO}t} + V_{1,30}e^{j3\omega_{RF}t} + \ldots\right] +$$
$$\frac{1}{2}\begin{bmatrix} V_{1,-10}e^{-j\omega_{RF}t} + V_{1,0-1}e^{-j\omega_{LO}t} + V_{1,-20}e^{-j2\omega_{RF}t} + V_{1,-1-1}^{-j(\omega_{RF}+\omega_{LO})t} + V_{1,1-1}^{j(\omega_{RF}-\omega_{LO})t} + \\ V_{1,-1+1}^{-j(\omega_{RF}-\omega_{LO})t} + V_{1,0-2}e^{-j2\omega_{LO}t} + V_{1,-30}e^{-j3\omega_{RF}t} + \ldots \end{bmatrix} \quad (3.20)$$

and v_1, v_2, and v_3 have the same form. The negative frequency are for the high-order calculation and the calculation results will return to DC or return to the frequencies as same as the results of low orders.

Because we merely consider the second-order nonlinear response now, we only see the response at frequency $\omega_{LO}+\omega_{RF}$ at first time for simplification. So when we compute equation (3.16), the first thing is to find the corresponding items which are at our desired frequency. At this case, $i_{NL2,gm2}$ can be expended as equation (3.21).

$$i_{NL2,g_{m2}} = K_{2,g_m}v_{gs1}^2 + K_{2,g_m}v_{gs2}^2 = K_{2,g_m}\left[\left(v_3 - v_2\right)^2 + \left(v_4 - v_2\right)^2\right]$$
$$= K_{2,g_m}\left(v_3^2 + v_4^2 + 2v_2^2 - 2v_2v_3 - 2v_2v_4\right) \quad (3.21)$$

Then seek out the parameters of products at frequency $\omega_{LO}+\omega_{RF}$ as following :

$$v_3^2 \rightarrow \frac{1}{2}V_{3,10}V_{3,01} \qquad v_4^2 \rightarrow \frac{1}{2}V_{4,10}V_{4,01}$$
$$2v_2^2 \rightarrow V_{2,10}V_{2,01} \qquad -2v_2v_3 \rightarrow -\frac{1}{2}V_{3,10}V_{2,01} - \frac{1}{2}V_{3,01}V_{2,10}$$
$$-2v_2v_4 \rightarrow -\frac{1}{2}V_{4,10}V_{2,01} - \frac{1}{2}V_{4,01}V_{2,10}$$

make an arrangement and simplification:

$$i_{NL2,g_{m2}} = \frac{1}{2}\begin{bmatrix} V_{3,01}V_{3,10} - V_{2,10}\left(V_{3,01} + V_{4,01}\right) + \\ V_{2,01}\left(2V_{2,10} - V_{3,10} - V_{4,10}\right) + V_{4,01}V_{4,10} \end{bmatrix} e^{j(\omega_{RF}+\omega_{LO})t} + \left[\ldots\right]e^{j2\omega_{RF}t} + \ldots \quad (3.22)$$

Hence, we get the second-order nonlinear current source related to $K_{2,gm}$ with the desired frequency $\omega_{LO}+\omega_{RF}$. Other parts of nonlinear current source in equation (3.19) can be gotten by the same method. The next step is to find the nonlinear current

sources at other nodes. In this circuit, only node 2 and node 3 have the generation of nonlinear current sources, which come from second-order derivative of transconductance and high orders, respectively. Therefore, the matrix equations related to the second-order response are shown in the following equations.

$$U_{11}=\begin{bmatrix}V_{1,11}\\V_{2,11}\\V_{3,11}\\V_{4,11}\end{bmatrix}=Y^{-1}\left(j\omega_{LO}+j\omega_{RF}\right)\begin{bmatrix}i_{NL2}\\i_{NL2}\\0\\0\end{bmatrix},\quad U_{20}=\begin{bmatrix}V_{1,20}\\V_{2,20}\\V_{3,20}\\V_{4,20}\end{bmatrix}=Y^{-1}\left(j2\omega_{RF}\right)\begin{bmatrix}i_{NL2}\\i_{NL2}\\0\\0\end{bmatrix}$$

$$U_{02}=\begin{bmatrix}V_{1,02}\\V_{2,02}\\V_{3,02}\\V_{4,02}\end{bmatrix}=Y^{-1}\left(j2\omega_{LO}\right)\begin{bmatrix}i_{NL2}\\i_{NL2}\\0\\0\end{bmatrix},\quad U_{-11}=\begin{bmatrix}V_{1,-11}\\V_{2,-11}\\V_{3,-11}\\V_{4,-11}\end{bmatrix}=Y^{-1}\left(j\omega_{LO}-j\omega_{RF}\right)\begin{bmatrix}i_{NL2}\\i_{NL2}\\0\\0\end{bmatrix}$$

.....

The calculation is becoming more complicated when the order of nonlinearity is increasing. Here the calculation of second-order nonlinear behavior is already far more annoying than first-order nonlinearity. In the calculation of third-, forth-order, and higher orders even, it is nearly impossible to calculate manually. Therefore, a mathematic software to help you compute more effectively is necessary.

3.3.3 Third-Order Nonlinear Responses

We can obtain the third-order nonlinear response by the same procedure. The nonlinear current source of i_{NL3} is shown in equation (3.23).

$$\begin{aligned}i_{NL3}=&\underbrace{\begin{aligned}&K_{3,g_m}v_{gs}^3+K_{3,g_{mb}}v_{bs}^3+K_{3,g_o}v_{ds}^3+K_{3,2g_m\&g_{mb}}v_{gs}^2v_{bs}+K_{3,2g_m\&g_o}v_{gs}^2v_{ds}+K_{3,g_m\&2g_{mb}}v_{gs}v_{bs}^2\\&+K_{3,g_m\&2g_o}v_{gs}v_{ds}^2+K_{3,2g_{mb}\&g_o}v_{bs}^2v_{ds}+K_{3,g_{mb}\&2g_o}v_{bs}v_{ds}^2+K_{3,g_m\&g_{mb}\&g_o}v_{gs}v_{bs}v_{ds}\end{aligned}}_{\text{Third-order nonlinearity}}\\&\underbrace{\begin{aligned}&+K_{2,g_m}v_{gs}^2+K_{2,g_{mb}}v_{bs}^2+K_{2,g_o}v_{ds}^2+K_{2,g_m\&g_{mb}}v_{gs}v_{bs}+\\&K_{2,g_m\&go}v_{gs}v_{ds}+K_{2,g_{mb}\&g_o}v_{bs}v_{ds}\end{aligned}}_{\text{Second-order nonlinearity}}\end{aligned}\qquad(3.23)$$

The third-order nonlinear responses describe the responses at frequency $3\omega_{RF}$,

$2\omega_{RF}+\omega_{LO}$, $\omega_{RF}+2\omega_{LO}$, $3\omega_{LO}$, and $2\omega_{RF}-\omega_{LO}$, $\omega_{RF}-2\omega_{LO}$, ... From equation (3.23) we find that i_{NL3} contains i_{NL2}, this is because the second-order nonlinear behavior is determined by former section, so we at least have the information of each node's second-order nonlinear responses. The third-order nonlinear current is derived by these information, and the second-order nonlinear behavior maybe generates the nonlinear signal at the same frequency as the generation of third-order nonlinear behavior. For example, the signal at frequency $2\omega_{RF}$ generated by second-order nonlinear behavior, mixing with signal ω_{LO} through second-order nonlinear behavior again and it will generate the signal of frequency $2\omega_{RF}+\omega_{LO}$. After determining the i_{NL3} by some mathematic software, the matrix equations for third-order nonlinear responses can be gotten as the similar methods as the second-order, shown as followed:

$$U_{30}=\begin{bmatrix}V_{1,30}\\V_{2,30}\\V_{3,30}\\V_{4,30}\end{bmatrix}=Y^{-1}\left(j3\omega_{RF}\right)\begin{bmatrix}i_{NL3}\\i_{NL3}\\0\\0\end{bmatrix},\quad U_{21}=\begin{bmatrix}V_{1,21}\\V_{2,21}\\V_{3,21}\\V_{4,21}\end{bmatrix}=Y^{-1}\left(j2\omega_{RF}+j\omega_{LO}\right)\begin{bmatrix}i_{NL3}\\i_{NL3}\\0\\0\end{bmatrix},$$

$$U_{12}=\begin{bmatrix}V_{1,12}\\V_{2,12}\\V_{3,12}\\V_{4,12}\end{bmatrix}=Y^{-1}\left(j\omega_{RF}+j2\omega_{LO}\right)\begin{bmatrix}i_{NL3}\\i_{NL3}\\0\\0\end{bmatrix},\quad U_{03}=\begin{bmatrix}V_{1,03}\\V_{2,03}\\V_{3,03}\\V_{4,03}\end{bmatrix}=Y^{-1}\left(j3\omega_{LO}\right)\begin{bmatrix}i_{NL3}\\i_{NL3}\\0\\0\end{bmatrix},$$

.....;

3.3.4 Forth-Order Nonlinear Response

Like the way of the third-order nonlinear computing, the forth-order nonlinear computing is explored by the total information you have already determined. Principally, the voltage responses of each node from first-order to third-order nonlinear behavior are totally taken into consideration. As the same procedure to find out the nonlinear current source i_{NL4} shown in equation (3.24).

$$i_{NL4} = \underbrace{K_{4,g_m} v_{gs}^4 + K_{4,3g_{m\&}g_{mb}} v_{gs}^3 v_{bs}^1 + K_{4,3g_{m\&}1g_o} v_{gs}^3 v_{ds} + K_{4,2g_m\&2g_{mb}} v_{gs}^2 v_{bs}^2 + ...}_{\text{Forth-order nonlinearity}}$$
$$\underbrace{+K_{3,g_m} v_{gs}^3 + K_{3,g_{mb}} v_{bs}^3 + K_{3,g_o} v_{ds}^3 + K_{3,2g_m\&g_{mb}} v_{gs}^2 v_{bs} + ...}_{\text{Third-order nonlinearity}}$$
$$\underbrace{+K_{2,g_m} v_{gs}^2 + K_{2,g_{mb}} v_{bs}^2 + K_{2,g_o} v_{ds}^2 + K_{2,g_m\&g_{mb}} v_{gs} v_{bs} + ...}_{\text{Second-order nonlinearity}} \quad (3.24)$$

Equation (3.24) only shows dominant part of nonlinearity for each order. Comparatively, the nonlinearity that derives from g_m have more influence than others. For example, among the forth-order nonlinearity the top three are $K_{4,gm}v_{gs}^4$, $K_{4,3gm\&gmb}v_{gs}^3v_{bs}$, and $K_{4,3gm\&go}v_{gs}^3v_{ds}$, and the sum of top three occupy at least 95% of the total amount of the forth-order nonlinearity. So we can focus on several major components to simplify the computing, and get the results with sufficient accuracy. Finally, the matrix equations of forth-order nonlinear responses show as followed:

$$U_{40} = \begin{bmatrix} V_{1,40} \\ V_{2,40} \\ V_{3,40} \\ V_{4,40} \end{bmatrix} = Y^{-1}\left(j4\omega_{RF}\right)\begin{bmatrix} i_{NL4} \\ i_{NL4} \\ 0 \\ 0 \end{bmatrix}, \quad U_{31} = \begin{bmatrix} V_{1,31} \\ V_{2,31} \\ V_{3,31} \\ V_{4,31} \end{bmatrix} = Y^{-1}\left(j3\omega_{RF} + j\omega_{LO}\right)\begin{bmatrix} i_{NL4} \\ i_{NL4} \\ 0 \\ 0 \end{bmatrix}$$

$$U_{22} = \begin{bmatrix} V_{1,22} \\ V_{2,22} \\ V_{3,22} \\ V_{4,22} \end{bmatrix} = Y^{-1}\left(j2\omega_{RF} + j2\omega_{LO}\right)\begin{bmatrix} i_{NL4} \\ i_{NL4} \\ 0 \\ 0 \end{bmatrix} \quad ,.....$$

3.3.5 Computing

Before we start to calculate the nonlinear response, the nonlinear parameters need to be gotten. We extract these parameters from DC simulation of the circuit in figure 3.8 using Angilent ADS (version 2009). Now with the above equations and the extracted parameters we can compute the nonlinear responses of each order.

The nonlinear analysis of sub-harmonic mixing focus on the fourfold frequency response at the output. We show again in figure 3.11. and express the frequency of

each excitation, so we have a goal of the response with frequency $4f_0$ at the output. In the former sections, we see that the $4f_0$ is mainly constituted of three components, $2\omega_{RF}+\omega_{LO}$, $4\omega_{RF}$, and $2\omega_{LO}$.

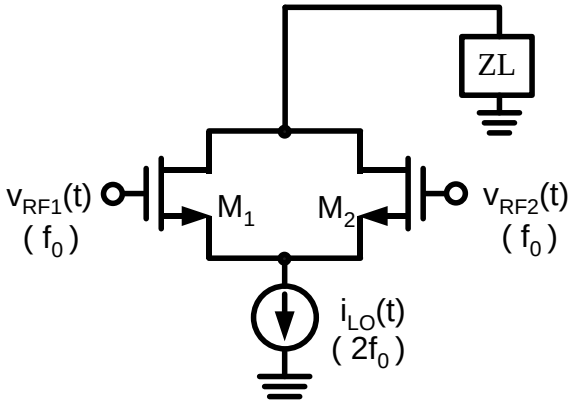


Figure 3.11 The circuit of sub-harmonic mixer for nonlinear analysis.

The nonlinear analysis is under the assumption of weak nonlinearity, so we ignore the feedback of high-order nonlinear behavior overlapping the low-order nonlinear behavior at the same frequency. Therefore, The input signals need to be small, at least smaller than 25mV.

The first step is looking into the direct generation of frequency $4\omega_{RF}$, which states the input sources are only v_{RF1} and v_{RF2} at frequency ω_{RF}, through the forth-order nonlinear behavior as we discuss in above sections, and then generate the signal at frequency $4\omega_{RF}$. As we all know, the magnitude of $4\omega_{RF}$ is mainly influenced by the DC bias (V_{GS} of transistor M1, M2), hence we test the V_{GS}-versus-$4\omega_{RF}$ on the beginning, and under the condition that ideal differential excitations v_{RF1} and v_{RF2} are 10mV at frequency 1.5GHz, which is the fundamental frequency f_0. The comparison of calculation and simulation results for the output current are shown in figure 3.12. It tell us that the deviation between calculation and simulation is smaller than 3%, which is accurate enough for the analysis. The curve obviously shows the point of maxima $4\omega_{RF}$. According to our theory of proposed quadrupler, the preliminary selection of

bias current is decided to be here.

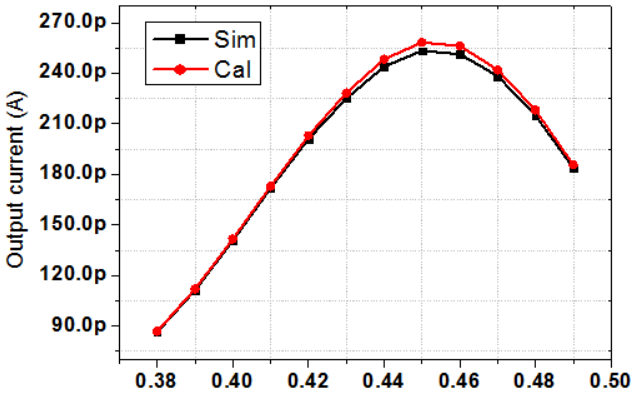


Figure 3.12 The comparison of calculation and simulation results for the output current at $4f_0$.

With the fabulous precision of calculation results , we move on to the topic of injection current i_{LO}. The i_{LO} is generated from a doubler which is formed by differential-pair transistors, so the frequency ω_{LO} is $2f_0$ in the spectrum. The amplitude of i_{LO} is about 1% of I_{bias}. Here we define alpha to be the generation efficiency shown in equation (3.25).

$$\alpha = \frac{|i_{LO}|}{I_{Bias}} \tag{3.25}$$

Because the input signals scale of doubler are identical to v_{RF1} and v_{RF2}, smaller signals, so its generation efficiency is poor. Our interest here are the amount of $2\omega_{RF}+\omega_{LO}$ and $2\omega_{LO}$ in comparison with $4\omega_{RF}$ because they are at the same location of frequency spectrum $4f_0$. Figure 3.13 shows the comparison of calculation and simulation results for spectrum $4f_0$ with *alpha* increasing from 0 to 1%. It clearly show the error between calculation and simulation can be ignored. The $4f_0$ is constituted of three components, $2\omega_{RF}+\omega_{LO}$, $4\omega_{RF}$, and $2\omega_{LO}$, we have mentioned. In calculation, the amount of $4f_0$ is totally the sum of three components. The point is from simulation we only see $4f_0$ in the spectrum, we can't distinguish the one from others. But from calculation we can easily get them one by one, because their

derivation are distinguishable. Just as the former sections we discuss, the $2\omega_{RF}+\omega_{LO}$ is the derivative of third-order nonlinear behavior, and the $2\omega_{LO}$ is from second-order nonlinear behavior. Figure 3.14 shows the three components separately.

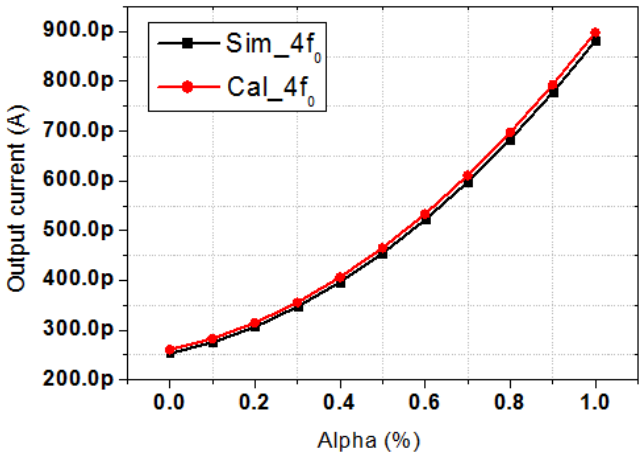


Figure 3.13 The comparison of calculation and simulation results for the output current at $4f_0$ with alpha increasing from 0 to 1%.

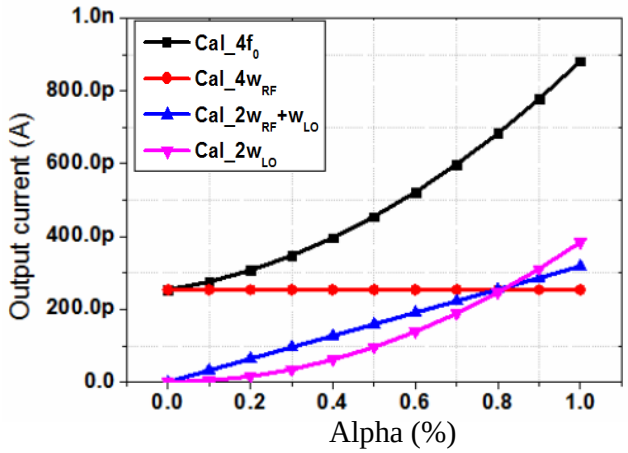


Figure 3.14 The calculation result of $4f_0$ and three components separately.

The calculation results tell us that with injection current i_{LO} the spectrum $4f_0$ can be increased by the derivatives of nonlinear mixing. Here the injection phase of i_{LO} is set as zero degree by empiricism.

With the input signals increasing, the deviation between calculation and simulation results increasing, too. This is because the high-order nonlinear behavior interfering with low orders. In addition, it will cause the DC offset as we discuss in

chapter 2. If we take high-order nonlinear behavior into consideration, it may become a very arduous task. But the small signal nonlinear analysis have clearly told us the mechanism of sub-harmonic mixing from mathematic equations.

3.4 Design for the Frequency Quadrupler

3.4.1 A Method to Analyze Sub-harmonic Mixing

In the last section we study the nonlinear behavior through Volterra series. By way of mathematic equations we can clearly comprehend the harmonic generation, but that is on the assumption of weak nonlinearity. In some circuits, for example, the low-noise amplifier (LNA), small-signal S-parameter is used to analyze the input impedance and the power gain, since an LNA is of small-signal operation. LNAs are categorized as weakly nonlinear circuits, therefore small-signal methods is suitable for analysis. Now what we are going to talk about are up-coverter Mixers or multipliers, however, usually a relative large signal is used. Furthermore, large signal will lead to the condition of strong nonlinearity, and the interference from high-order nonlinear behavior and DC drift can not be ignored; so there are troublesome problems in analysis by calculation. Therefore, exploring the possibility of a method coping with large signal nonlinear analysis directly is a required topic. Volterra series for nonlinear behavior tell us the fundamental theory. But in circuit design, using simulation tools such as ADS to help us can well reduce the duration of analysis.

Harmonic balance (HB) method and time-domain method are commonly used in the analysis of nonlinear circuits. In general, when refer to handling mixers design, especially the multiplier, the HB method is the best alternative. But as we have discussed, if there are several nonlinear derivatives at the same location of frequency spectrum, the simulation results can not distinguish one from the other. It only shows

the total amount at our desired frequency. Without enough information, we are hard for design, so we must figure out a way to solve this problem. An approximate simulation may be feasible. We make use of a small shift in the input frequency, this action will lead to the occasion that the circuit's nonlinear derivatives also have a small shift in their frequency. What this means is that we can distinguish the nonlinear derivatives which originally have the same frequency. However, this approximate simulation is established on a assumption that the small shift of frequency do not change AC response such as gain, phase.., etc. Take the sub-harmonic mixer of figure 3.8 for example. We show it again with some information in figure 3.15.

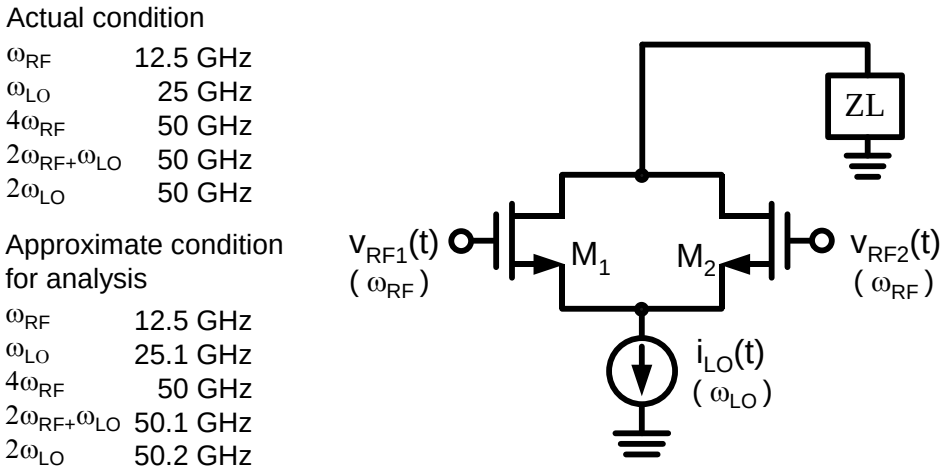


Figure 3.15 The alteration between the actual and the approximate condition for the nonlinear analysis of sub-harmonic mixer.

Figure 3.15 shows us the deviation between $4\omega_{RF}$, $2\omega_{RF}+\omega_{LO}$, and $2\omega_{LO}$ in the approximate condition. Instead of overlapping on the same location of the spectrum, the top three of $4f_0$ can be distinguish now. It effectively help us carry out the analysis. Nevertheless, the precision of this approximation is still a question. To verify the accuracy, we do a test simulation with large signal excitation, and its results are shown in figure 3.16. Where v_{RF} is sweeping up to 0.5V, and α is set as 0.3 and 0.5

respectively. The actual case, namely, the normal simulation, and the quantity you observed at frequency 50 GHz of the spectrum. That is due to a great many nonlinear derivatives overlapping on the same spot, $4f_0$. As for the approximate case, we assume that the $4f_0$ is got by linear adding of responses at 50, 50.1, and 50.2 GHz. In other words, we let a nonlinearity be treated as several nonlinearities totalling linearly. It is similar to the concept of Volterra series. However, the simulation shows that the accuracy degrades by input signals increasing gradually. But it is a predictable result because the larger signal, the more nonlinear derivatives can not be ignored. Nevertheless, it still offers a quick analysis with sufficient accuracy when the input signals are smaller than 0.4V.

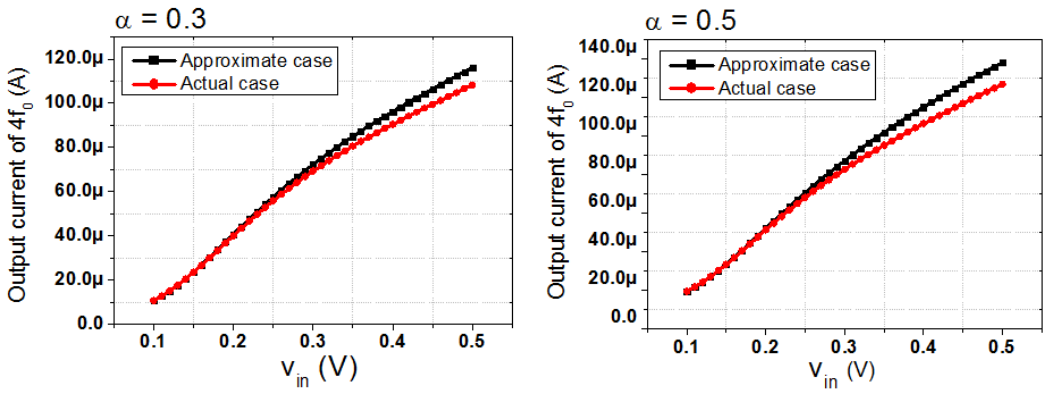


Figure 3.16 The alteration between the actual and the approximate condition for the nonlinear analysis of sub-harmonic mixer.

3.4.2 Design for the Frequency Quadrupler

In section 3.2 we proposed a preliminary architecture of the quadrupler. The half-circuit we show again in figure 3.17. From the nonlinear analysis, Our desired output current of $4f_0$ can be looked on as two parts, one is by the direct generation, and the other is by sub-harmonic mixing. The direct generation represents the way that the input signal v_{RF} with frequency ω_{RF} through the forth-order nonlinear behavior to generate the signal with frequency $4\omega_{RF}$. On the other hand, the

sub-harmonic mixing represents the mixing of two signals, v_{RF} with frequency ω_{RF} and i_{LO} with frequency ω_{LO}. Theoretically, the derivatives of mixing may be limitless, but there are two components corresponding to our interests. One with frequency $2\omega_{RF}+\omega_{LO}$, and the another with frequency $2\omega_{LO}$; the former is by third-order nonlinear behavior and the latter is second-order, respectively. Here, we must emphasize again that the frequencies we call ω_{RF} and ω_{LO} are exactly f_0 and $2f_0$ respectively. The reason is to differentiate the sources contributed towards $4f_0$, as we know, $4\omega_{RF}$, $2\omega_{RF}+\omega_{LO}$, and $2\omega_{LO}$. The expression is convenient when we analyze the behavior of sub-harmonic mixing.

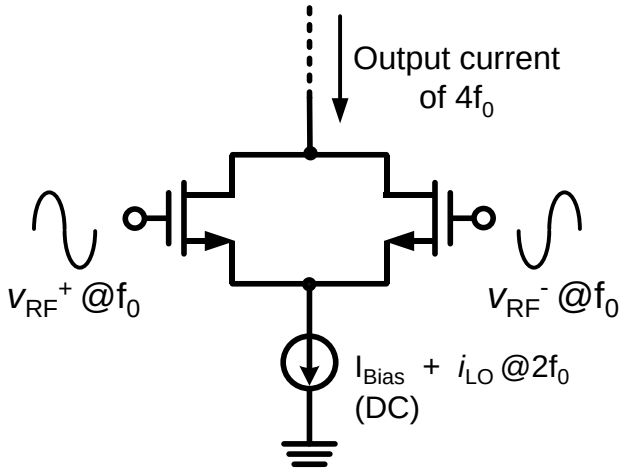


Figure 3.17 The half circuit of the proposed quadrupler.

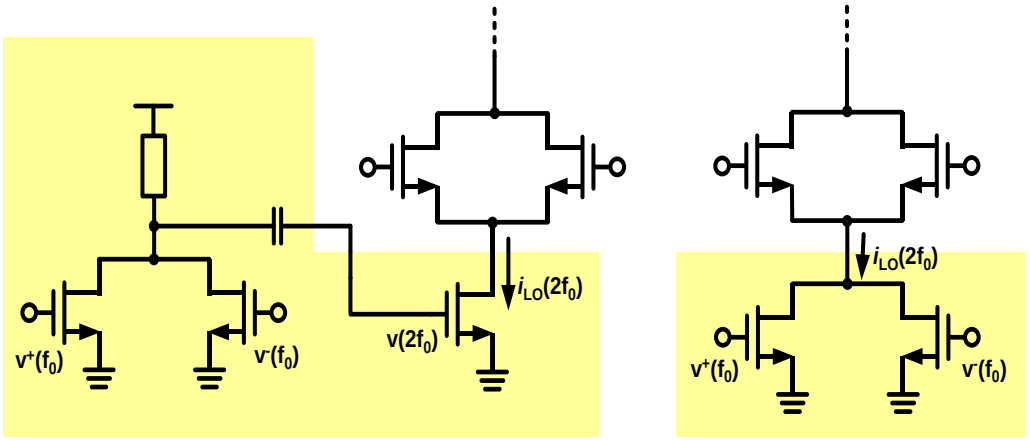
First of all, the current bias is defined as the place of maxima output current of $4\omega_{RF}$ without the injection current i_{LO}; because we are intending to confirm the contribution or benefit out of sub-harmonic mixing and how much of them. On the other hand, the main point is how to generates the injection current, this is about its magnitude, phase, and generation method. The practical topology of current sink like the circuits shown in figure 3.18 may provide both bias current and injection current i_{LO}. Although the cascade configuration can generate more i_{LO}, the cascode configuration, sometimes called current-reuse topology, is more preferable for the

reason of no extra DC consumption and no excess of inductors.

It is essential that we first determine the optimum injection phase. The injection current is expressed as following.

$$i_{LO} = I_{LO}\angle\phi = \alpha \cdot I_{Bias} \tag{3.26}$$

Equation 3.26 clearly shows the magnitude and phase of injection current. The magnitude depend on the efficacy of doublers and the input power level. In normal operating, the value of alpha is approximately from 0.3 to 0.6. We would discuss the detail in the following section. However, determining the optimum injection phase is our priority at present.



Cascade **Cascode**

Figure 3.18 The practical topology of current sink which combine bias current and injection current.

Under a proper settlement of the transistor size, excitation of v_{RF}, and corresponded I_{Bias}, the simulation for injection phase to output components of $4f_0$ with a fixed alpha of 0.5 is shown in figure 3.19. We illustrate the results with top three of $4f_0$ respectively. The injection phase is relative to the fixed phase of differential input signals v_{RF}, which are 90 and 270 degree. Apparently, the phase of $4\omega_{RF}$ is unrelated to the injection phase, but the phase of $2\omega_{RF}+\omega_{LO}$ and $2\omega_{LO}$ are exactly periodic variation. On the other hand, the magnitude responses are all steady

because of a fixed alpha. Therefore, the optimum injection phase where the top three of $4f_0$ are in-phase is around 180 degree. Although they do not exactly intersect at 180 degree, we take the proper and realizable choice into consideration.

Re-draw the figure 3.19 in polar plot shown in figure 3.20, which can let us directly perceive the detail through the senses. In response to the conclusion of figure 3.19, the curves of $2\omega_{RF}+\omega_{LO}$ and $2\omega_{LO}$ are exactly concentric circles to the injection phase increasing continuously, and $4\omega_{RF}$ is a dot. The $4f_0$ is also plot in the chart, and now we are aware of the reason that the irregularity is because it is the combination of a dot and two concentric circles. Moreover, the cross mark the location where the injection phase is 180 degree. The maxima of $4f_0$ is not here, nevertheless, it is the most realizable. Taking this small phase deviation into consideration can be the future work. As to the another half circuit, the injection phase is reversed as apposed to the first one in a similar way.

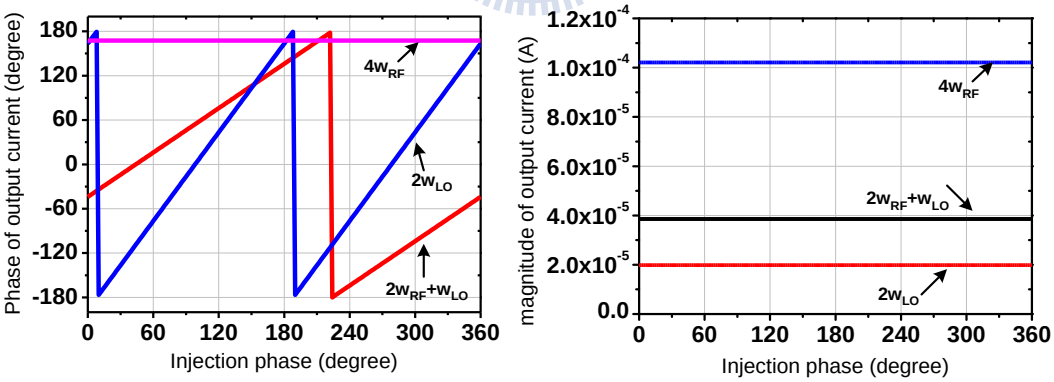


Figure 3.19 The simulation result for injection phase to the output components of $4f_0$, with a fix alpha of 0.5. Show the phase and magnitude respectively.

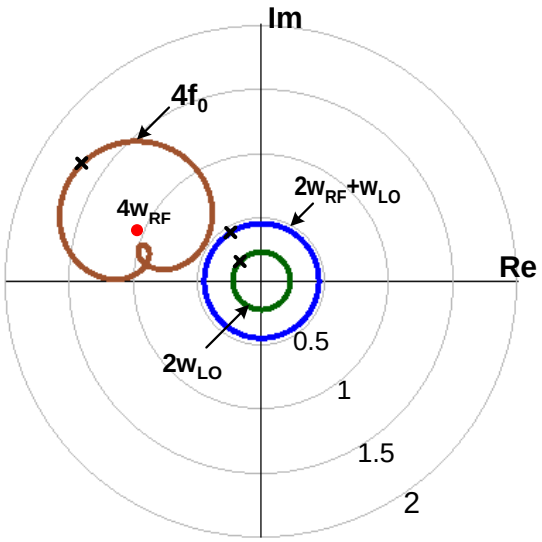


Figure 3.20 Re-draw the figure 3.19 in polar plot, the cross mark the location where the injection phase is 180 degree

After the phase of injection current determined, the corresponding phase of circuit's each input signal can be settled. The full schematic shows in figure 3.21. Because of using the differential-pair topology, the circuit have no odd-order spur harmonics appearing in the output. In addition, the two half circuits have reverse second-order spur harmonics at $2f_0$, so the cancelation happen in the output. Finally, we get a pure signal at frequency $4f_0$ in the output with other spurs eliminated.

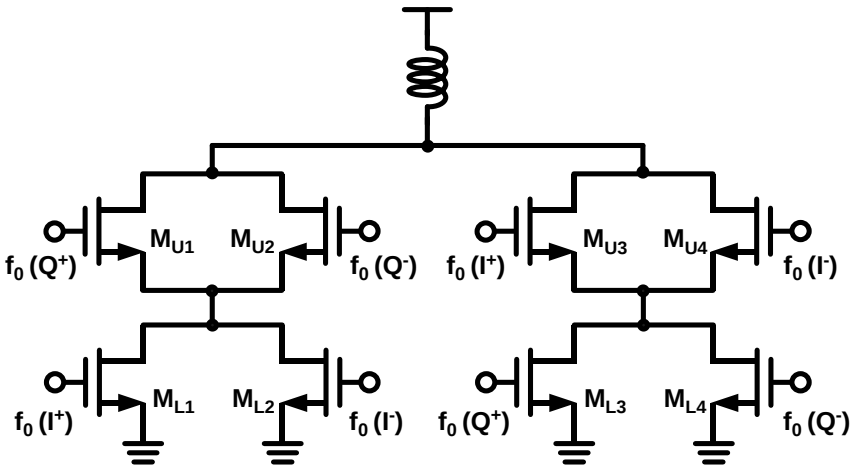


Figure 3.21 Full schematic of the proposed quadrupler with each phase condition of input.

The next topic is how to boost the generation efficiency of second-order injection current at $2f_0$. Here the generation efficiency is defined to be the ratio of injection current divided by bias current shown as equation 3.26 , and we named it α. Figure.3.22 shows the larger α, the more mixing as well as the more total output signal at $4f_0$.

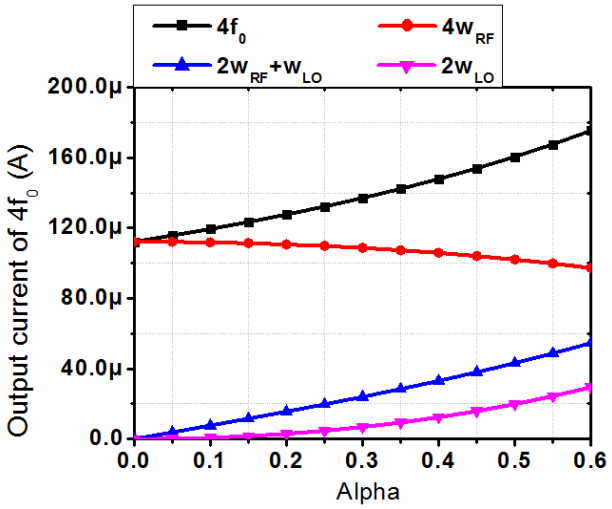


Figure 3.22 Simulation shows the larger α, the more mixing as well as the more $4f_0$

Consequently, the design to maximize the α of doublers will be a dominant theme. Well, we have mentioned that the bias current is settled by only the top differential pair operating at its maximum forth-order harmonic at $4f_0$. Therefore, under a fixed bias current, we need to find the maximum α we can get. Because of the smaller V_{GS}, the larger selection of transistor size resulting in larger leakage, α perhaps be found with a limit value. The simulation results shown in figure 3.23. According to the V_{GS} of doublers, the maximum α is about 0.6 where V_{GS} is around 0.4V. By the way, the threshold voltage of tsmc 90-nm technology is 0.48V under DC simulation. In other words, the DC bias voltage is set at the cut-off region of transistors, and the bias current is totally due to the large signal excitations when the circuit is in operating. As a result, the input signals have great influence upon the design.

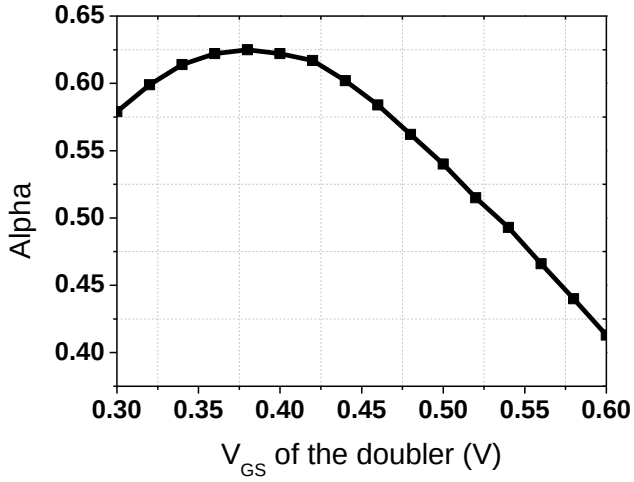


Figure 3.23 The simulation of α according to V_{GS} of the doubler

Then, we can carry out the further step of analysis under these V_{GS} and corresponding size selections of doubler. The circuit shown in figure 3.24 is the half of proposed quadrupler, and the simulation results is shown in figure 3.25. It seems to have the same conclusion of figure 3.22 that operating at the larger alpha, the much more mixing derivative will be gotten. Furthermore, you can find the optimum V_{GS} of doubler to obtain the maximum output signal at $4f_0$. The almost constant magnitude of harmonic $4\omega_{RF}$ is the same as it from the direct generation. What this means is that the derivative of $2\omega_{RF}+\omega_{LO}$ and $2\omega_{LO}$ by sub-harmonic mixing are completely benefit because of no additional power consumption. And it at least makes the output power be enhanced by 4dB.

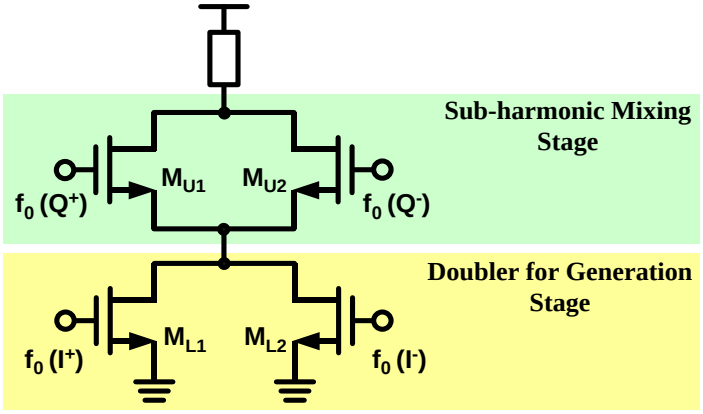


Figure 3.24 The half of the proposed quadrupler with definition of two stages.

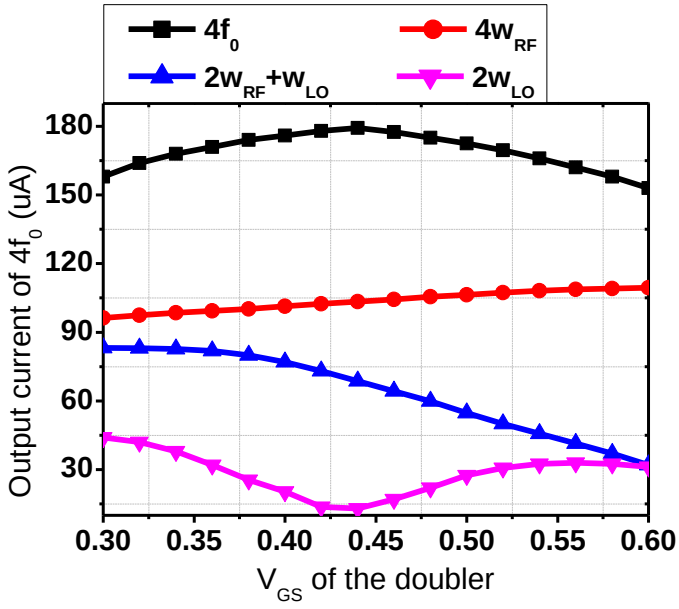
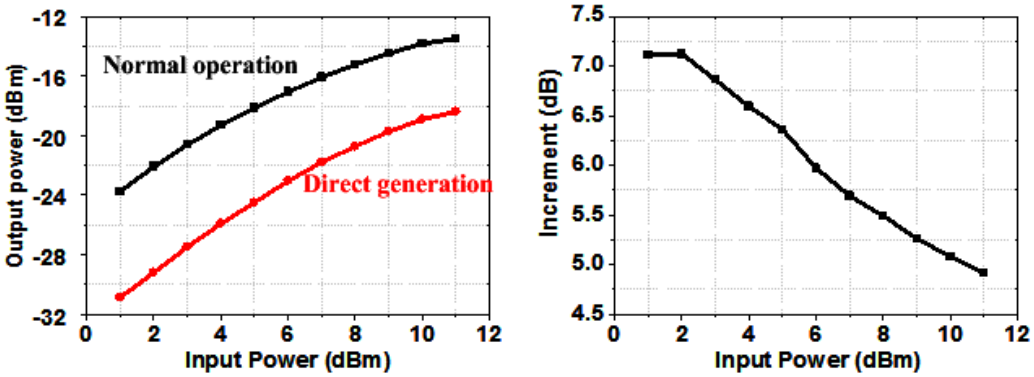


Figure 3.25 Simulation results of the half circuit according to the bias and size selection of the doubler stage.

After the complete procedure of circuit design, the simulation results of actual circuit are demonstrated as follows. Figure 3.26(a) shows the comparison of normal operation and direct generation, the latter represents the condition that the $4f_0$ is merely generated by $4\omega_{RF}$. Furthermore, the comparison is under the case of equal DC power consumption. Figure 3.26(b) shows the difference, which represents the increment by sub-harmonic mixing. This contribution is approximately 5 to 7 dB.



(a) (b)

Figure 3.26 (a) The comparison of normal operation and direct generation. (b) The increment by sub-harmonic mixing.

Figure 3.27 shows the $4f_0$ and each contribution in polar plot, which is the same form as figure 3.20. The input voltage is 0.4V, and we clear see the magnitude of $2\omega_{RF}+\omega_{LO}$ and $4\omega_{RF}$ are merely equivalent, this is to say, the gain enhancement by 6 dB. The efficacy in actual circuit is better than our preliminary simulation of test circuit. Anyway, the results correspond to our primitive assumption well.

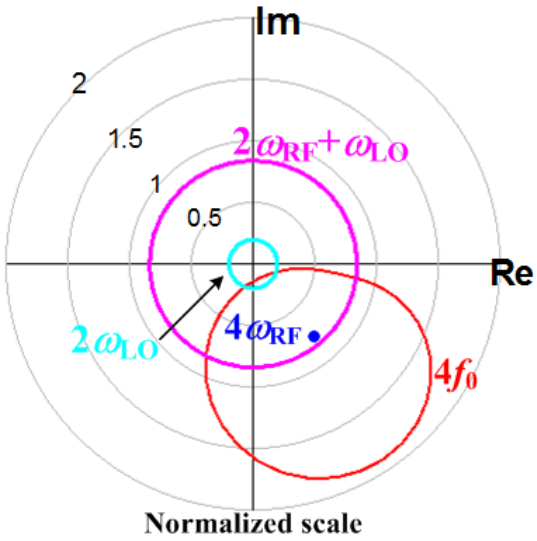


Figure 3.27 The $4f_0$ and each contribution in polar plot.

From another point of view, the sensitivity of bias voltage will tell us some information about sub-harmonic mixing. Figure 3.18 shows the sensitivity of bias voltage under the operation point. The large drift of bias voltage have little influence over the $4f_0$; this is because each contribution has various trend corresponding to the bias. As we all know, it is for the reason that they are derivatives with respect to the second- third- forth- order nonlinear behavior of transistor. Therefore, the total of $4f_0$ will be more flat in comparison with merely direct generation over the bias variation.

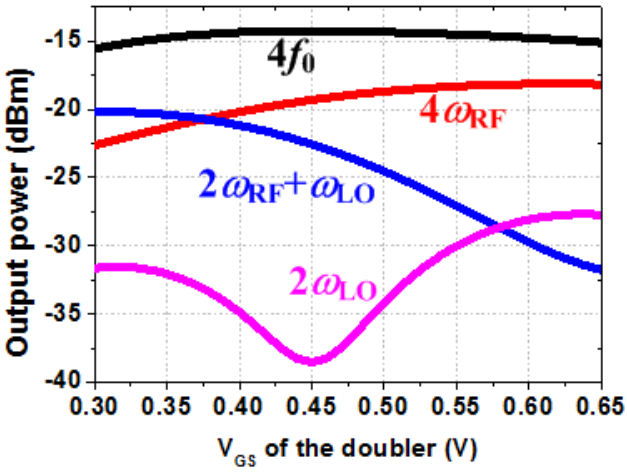


Figure 3.28 The sensitivity of bias voltage under the operation point.

3.4.3 Quadrature All-pass Filter(QAF)[4]

The proposed quadrupler need quadrature input signals for cancellation, therefore, the design contains an single-to-quadrature circuit. For the requirement of low power consumption, we take passive circuit and broadband application into our consideration. The quadrature all-pass filter(QAF) is perhaps the best alternative. From the paper, the mechanism of QAF is shown in figure 3.29. From another point of view, the inductor and capacitor create a path of imaginary part, and the resistor is real part; through these passive components the quadrature is formed. Like the polar plot shown in figure 3.30, it clearly shows the relationship of the quadrature created by proper arrangement of passive components.

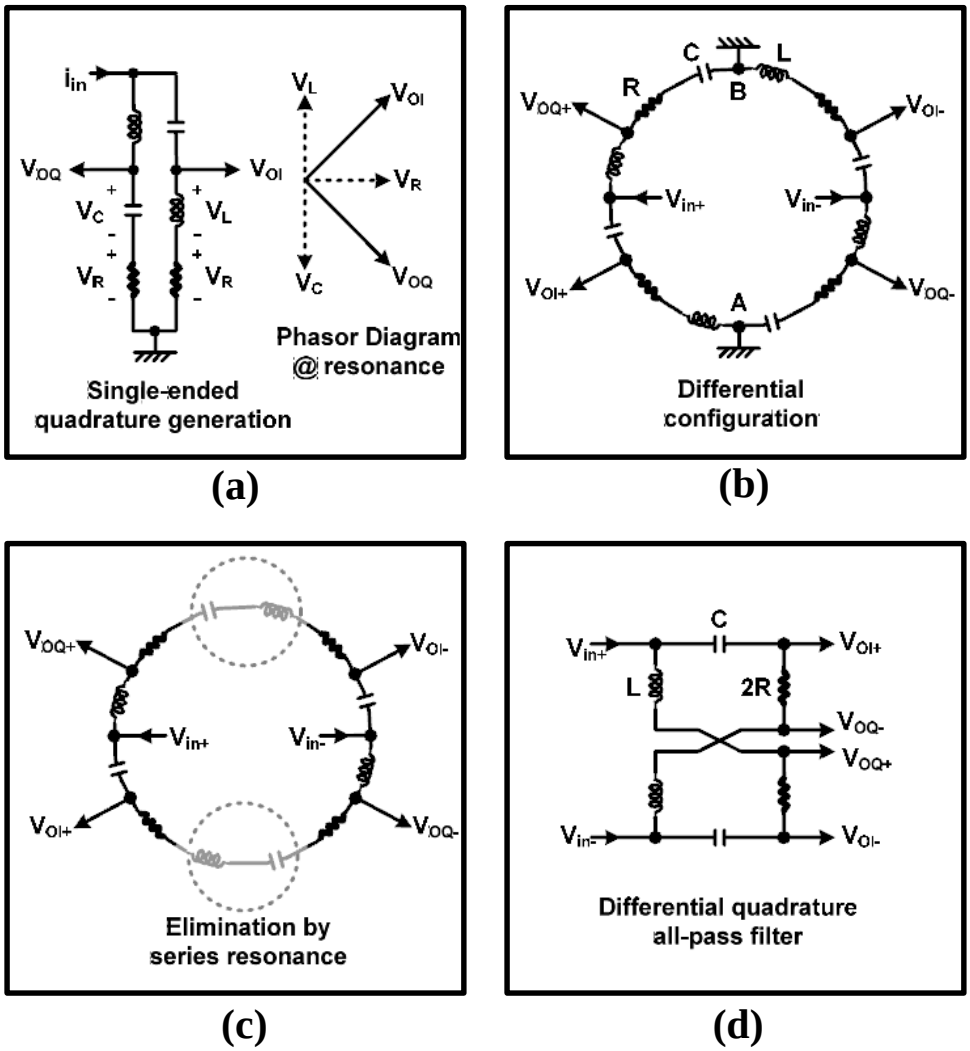


Figure 3.29 The mechanism of QAF from the paper.

However, poor capability to push relatively big load is the main drawback of QAF. A requirement of loading capacitance which need to be lower than 20% of the capacitor of QAF is tough in practical application. In our case it is at least 40% at the fundamental frequency of 12.5GHz. An excess of loading effect will cause severe mismatch. Even though the phase unbalance can be regulated by tuning the LC-tank of QAF, but the magnitude unbalance is unavoidable, which is by the reason that the four outputs of QAF are not symmetry with each other. Figure 3.31(a) shows the magnitude unbalance is because the two outputs which connect to C_Q having obvious loss by large load capacitance, but the another two outputs connecting to the inductor

are less influenced by load. However, we must figure out a way to deal with the unbalance problem at all costs. Our method is adding a resistor R_D connecting to the L_Q, and it is illustrated in figure 3.31(b). In spite of the method bringing about the imaginable degradation for QAF, but it make the quadrature totally balance under the large loading effect.

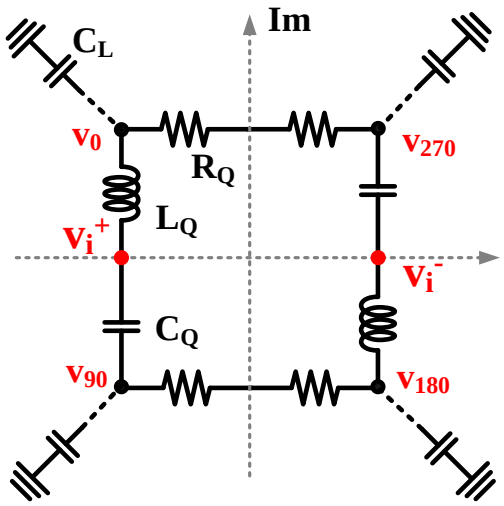


Figure 3.30 Express the OAF in polar plot

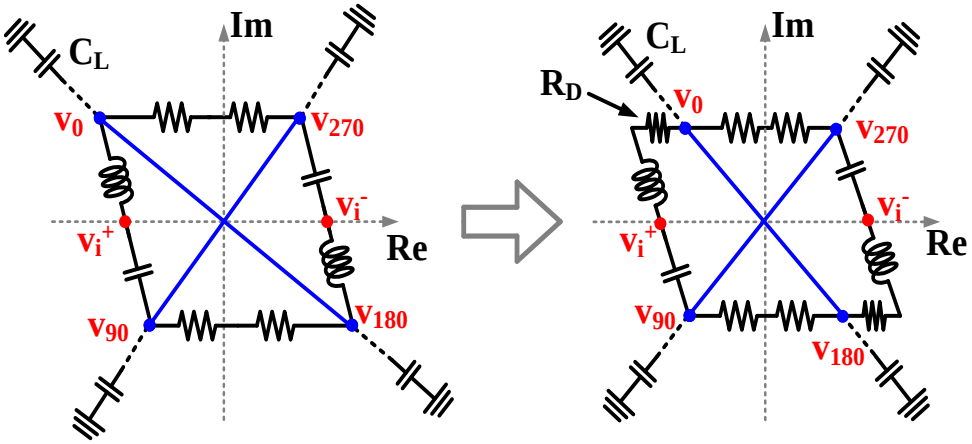


Figure 3.31 (a) The magnitude unbalance by large loading effect. (b) Melioration by adding a resistor R_D.

3.4.4 Output Buffer

For the measure requirement, we need a buffer stage to match 50 Ohm. The best alternative is C-D configuration because it maintain the performance of harmonic rejection by the broadband matching, except the drawback of considerable loss which is about 9.5dB at frequency 50 GHz.

Chapter 4

Chip Implement and Measurement Result

4.1 Measurement Setup

The quadrupler circuit is designed and fabricated in a 90-nm CMOS technology. The die micrograph is shown in figure 4.1 occupying an area of 832x733 μm^2, but the I/Q quadrupler only take 180x420 μm^2. We demonstrate the measurement setup in figure 4.2. Measurements were all conducted on wafer. Four probes were used, including a GSG probe, a GSGSG probe, a 6-pin DC probe, and a 3-pin DC probe. An off-chip 180 degree bulan coupler is used to produce the differential input signal; in addition, A phase shifter put after the bulan coupler to regulate the conceivable phase error by mismatch. Owing to the limitation of spectrum analyzer, the Agilent 11974V RF Pre-selector is required for V-band signal measurement. The conversion loss of this external frequency down-converter is automatically calibrated. As we have mentioned in last chapter, an Open-drain buffer are used at the quadrupler output for the measurement purpose. Based on simulations, the QAF and buffer introduce extra signal loss of 3dB and 9.5dB at 12.5 GHz input signals, which is included in the measure date.

4.2 Measurement

4.2.1 Sensitivity of Phase Mismatch

In the beginning, the mismatch from the 180-degree balun coupler result in phase error of differential input signal, so the off-chip phase shifter compensate the balun for phase error. On the other hand, we can also test the sensitivity to the phase mismatch of input signals by means of the phase shifter. The measure date is shown in

figure 4.3; the input power is 8dBm at frequency 12.5 GHz. The $4f_0$ is almost constant and the f_0 is the most sensitive to the phase mismatch. Therefore, the cancellation of f_0 require the input phase more precise. Even if the phase mismatch is five degrees, the HRRs at the output are still more than 30 dB, which is sufficient in most applications.

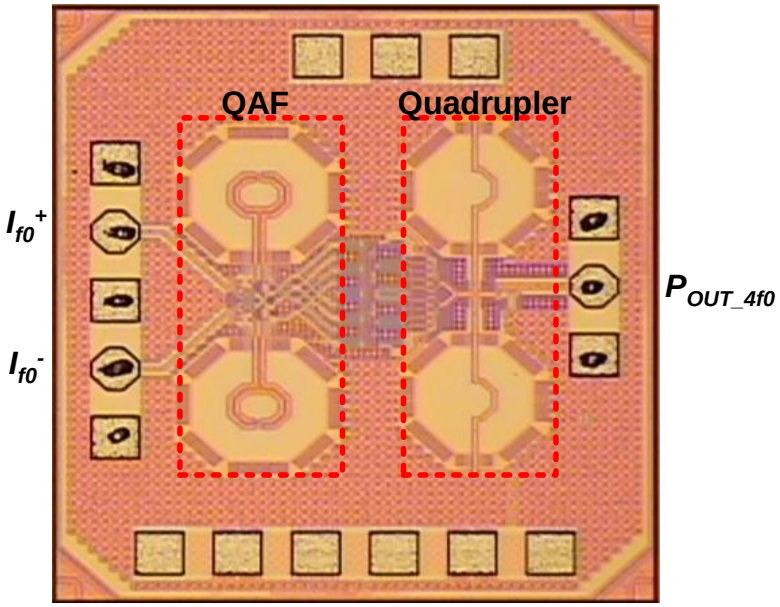


Figure 4.1 The die micrograph of chip implement.

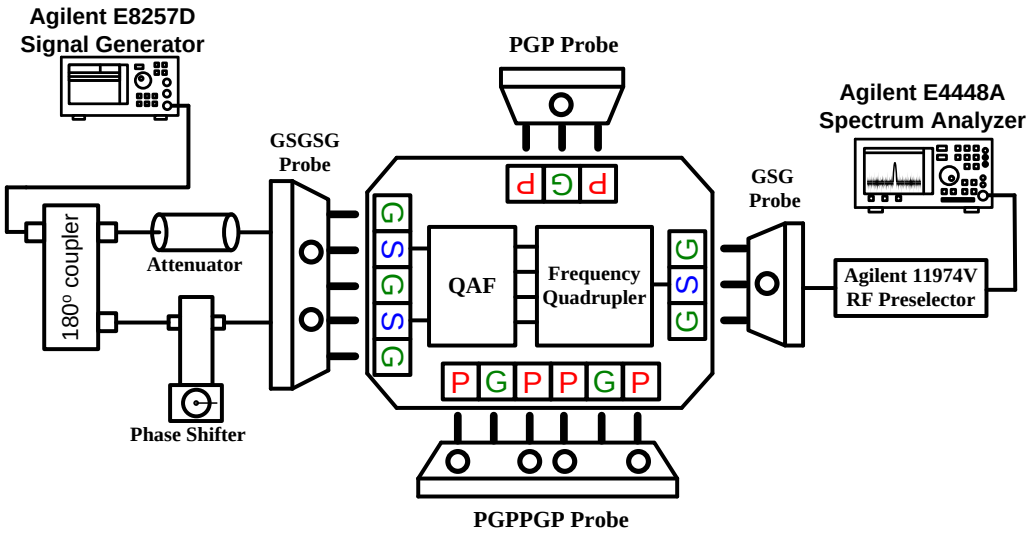


Figure 4.2 The measurement setup for V-band.

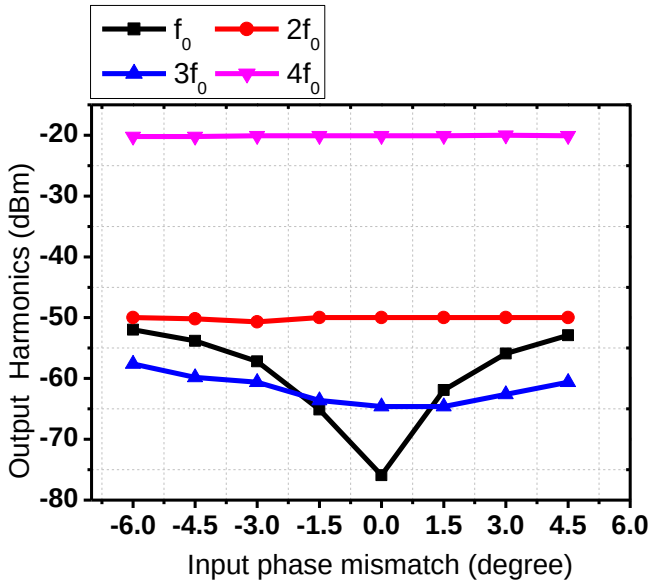
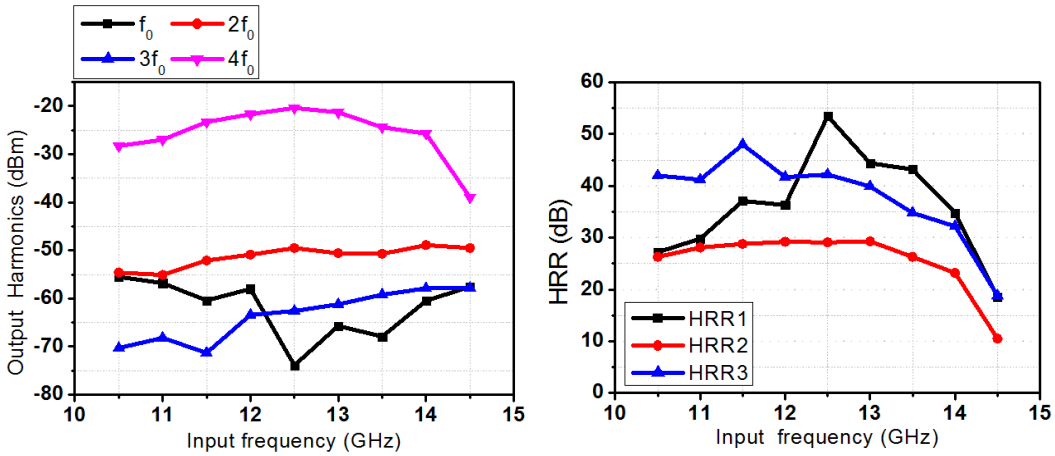


Figure 4.3 Output harmonics variation due to the mismatch of input phase .

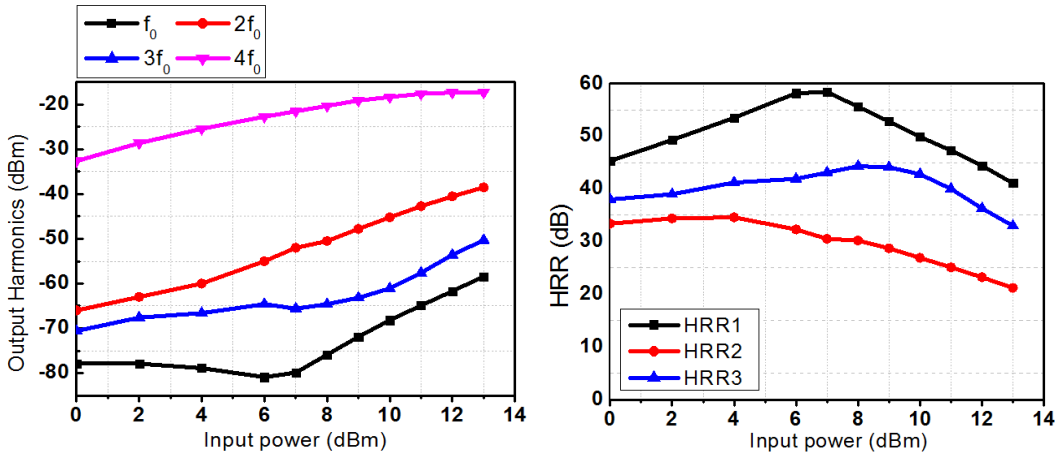
4.2.2 Output Harmonic Response

Figure 4.4(a) shows the frequency response of output harmonics with 8dBm input power, and the HRR also shows in the figure 4.4(b). The power transfer function of harmonics at input frequency 12.5GHz is shown in figure 4.5(a), and figure 4.5(b) shows the corresponding HRR. The HRR of the first-order, second-order, and third-order with the input signal of 12.5 GHz are 53.5 dBc, 29.2 dBc and 43 dBc, respectively. Apparently, the cancellation mechanism is in accordance with our expectancy, the broad range of operating frequency and power level. The power level of $4f_0$ at the chip output is -20 dBm after calibration of cable loss. The output power increases as the input signal level increases, but eventually saturates at -17 dBm, and the corresponding input power is 11 dBm. Furthermore, the more detailed information of frequency responses with varied input power level of 0, 4, 8 dBm respectively are shown in figure 4.6 including output power and HRRs.



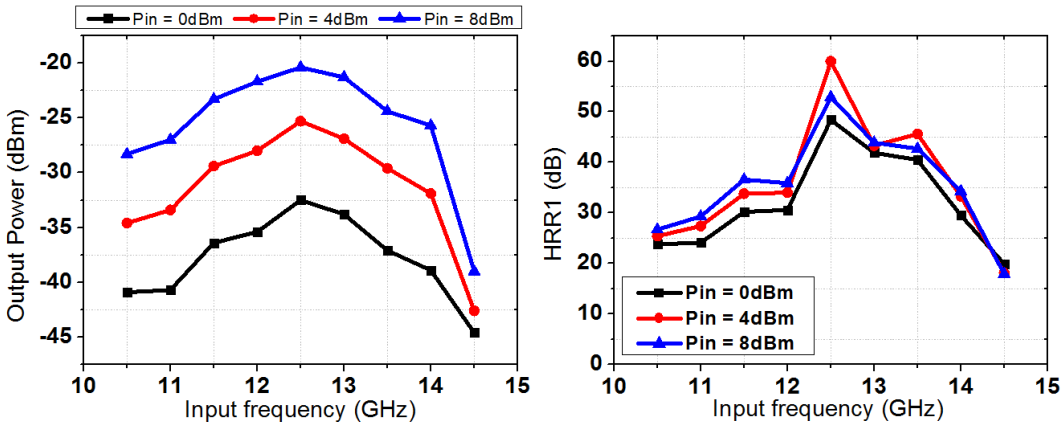
(a) (b)

Figure 4.4 (a) The frequency response of output harmonics with 8dBm input power. (b) the corresponding HRRs of (a).

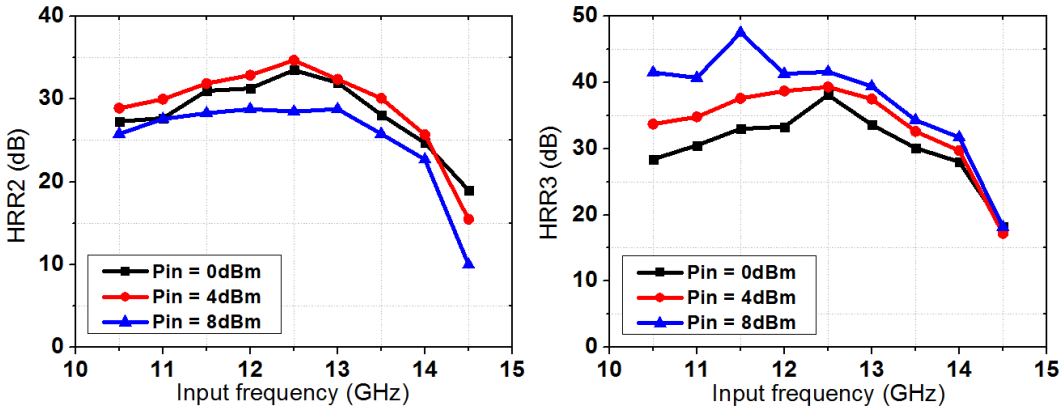


(a) (b)

Figure 4.5 (a) The power transfer function of harmonics at input frequency 12.5GHz. (b) the corresponding HRRs of (a).



(a) (b)



(c) (d)

Figure 4.6 The frequency responses with varied input power level of 0, 4 ,and 8 dBm respectively. (a) Output power. (b) HRR1. (c) HRR2. (d) HRR3.

Incidentally, we show the photograph of output spectrum in figure 4.7, which is under the condition that the fundamental frequency f_0 is 12.5 GHz with 8 dBm input power. In addition, the output spectrum of frequency 12.5, 25, 37.5, and 50 GHz are shown from figure 4.8(a) to 4.8(b) respectively with the span of 1 MHz,

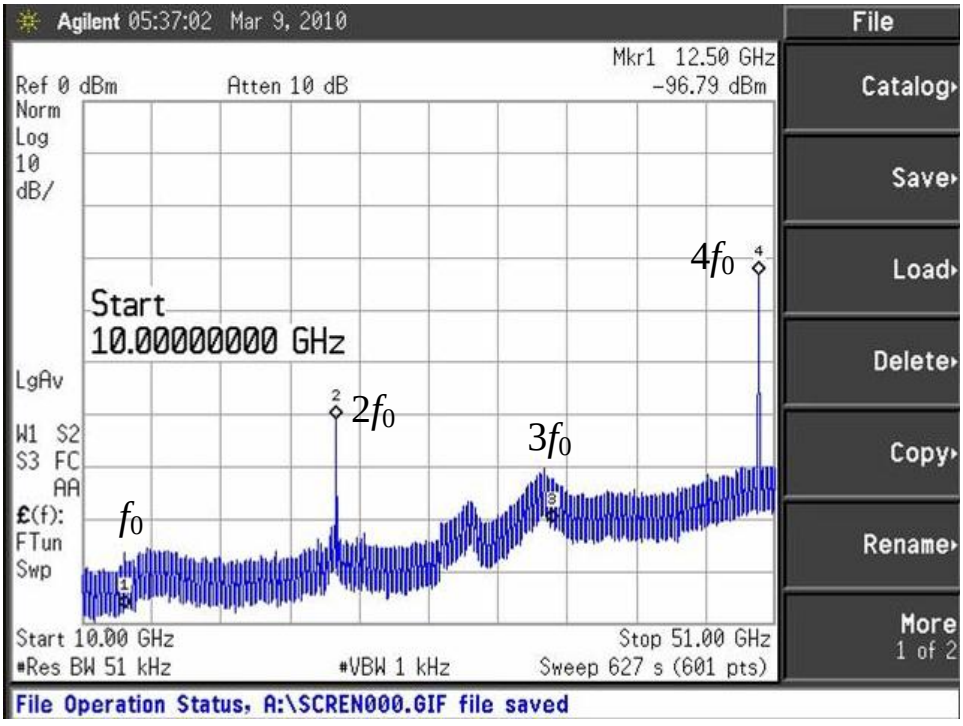


Figure 4.7 The photograph of output spectrum under the condition that fundamental frequency is 12.5GHz with 8 dBm input power.

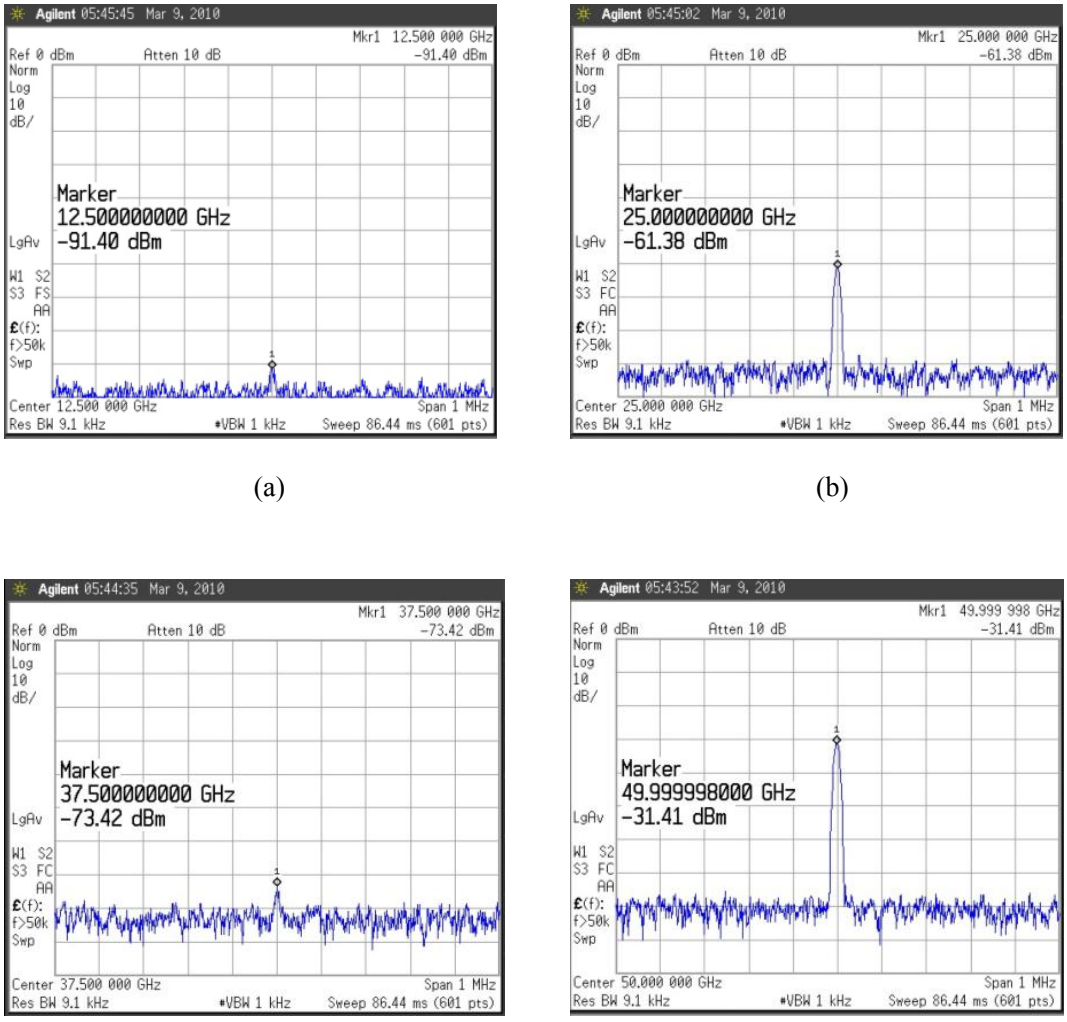


Figure 4.8 Individual output spectrum of figure 4.7 with the span of 1MHz
(a) f_0 (12.5GHz). (b) 2 f_0 (25GHz). (c) 3 f_0 (37.5GHz). (d) 4 f_0 (50GHz).

4.2.3 The Verification of the Enhancement by Sub-harmonic Mixing

The next topic of measurement is to verify the most representative feature we put forward, namely, the derivative of sub-harmonic mixing can contribute enormously to our desired $4f_0$. Moreover, we must perform the test and verification at the same chip to demonstrate the truth with reliability. By way of operating laser cut, we disconnect the signal paths of generation stage but keep the voltage bias paths intact. The reason is because the DC power consumption need to be under constant before and after laser cut, so we reach this requirement by adjusting the voltage bias of doublers. In other

words, we turn the doubler into a DC current sink exactly, and the magnitude of DC current is the same as the condition under normal operation for a fair comparison. Figure 4.9 illustrates the method of work, and the micrograph of chip after laser cut is shown in figure 4.10.

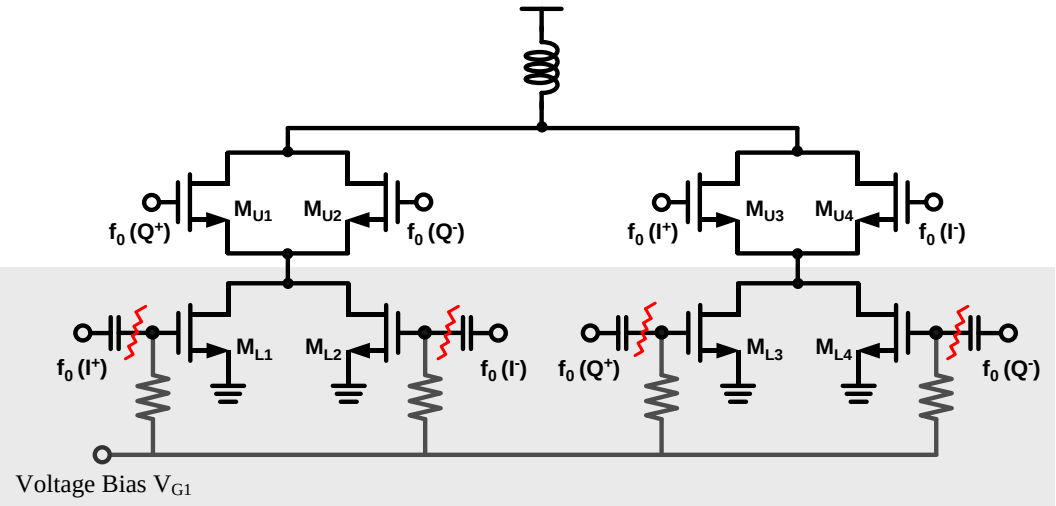


Figure 4.9 The location of laser cut in the circuit, we disconnect the signal paths of doubler stage but keep the voltage bias paths intact.

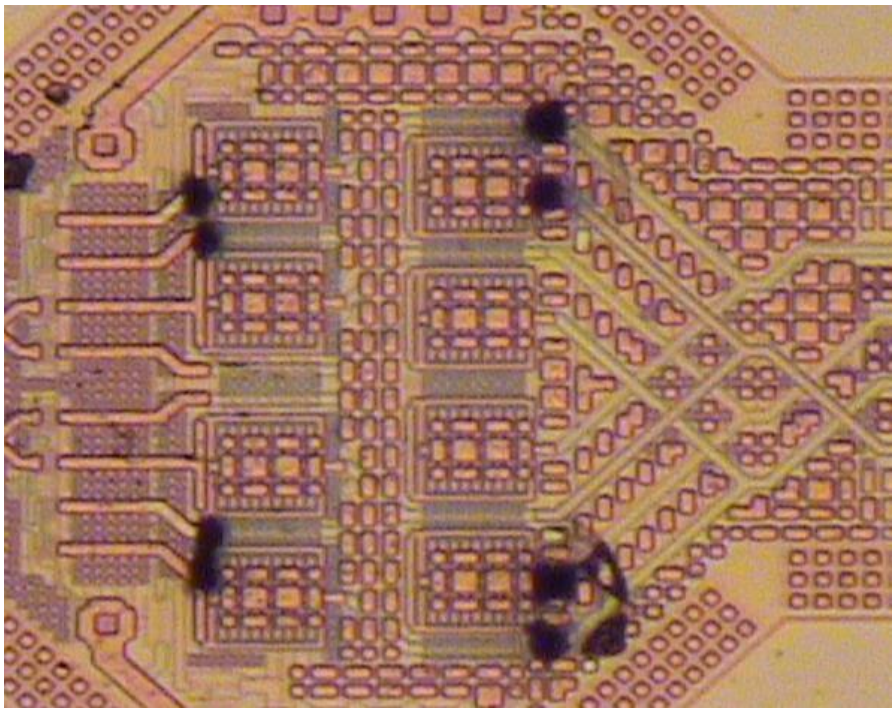


Figure 4.10 The location of laser cut in the chip.

After a successful test, the measure dates is listed in table 2 including DC power consumption, output power before and after laser cut, which represent the comparison between normal operation with sub-harmonic mixing and merely direct generation. The operation frequency is at 12.5 GHz. We also plot the output power of two conditions together in figure 4.11(a) and show the increment in figure 4.11(b) for the distinction. In general, the measure date verifies our thought about the enhancement due to sub-harmonic mixing. It is at least 5 dB of the increment without additional demand for power consumption. This is to say, a absolutely profit. However, everything has its price, the amelioration at the cost of signal paths more intricate. It make the layout of circuit more complex and therefore induce a little signal loss.

Before laser cut . The normal operation at 0.45V of V_{G1}			After laser cut, merely direct generation! Adjusting VG1 to maintain power consumption.	
P_{in} (dBm)	Power Consumption (mW)	P_{out} of $4f_0$ (dBm)	V_{G1} (V)	P_{out} of $4f_0$ (dBm)
1	0.98	-30.46	0.55	-37.92
2	1.15	-28.54	0.57	-35.84
3	1.34	-26.72	0.59	-34.48
4	1.58	-25.16	0.6	-32.1
5	1.85	-23.7	0.62	-30.73
6	2.17	-22.4	0.65	-29.03
7	2.53	-21.18	0.67	-27.4
8	2.95	-20.07	0.69	-26.17
9	3.41	-19.12	0.72	-24.72
10	3.92	-18.17	0.75	-23.55
11	4.5	-17.58	0.78	-22.64
12	5.12	-17.38	0.81	-22.05

Table 4.1 The measurement dates before and after laser cut.

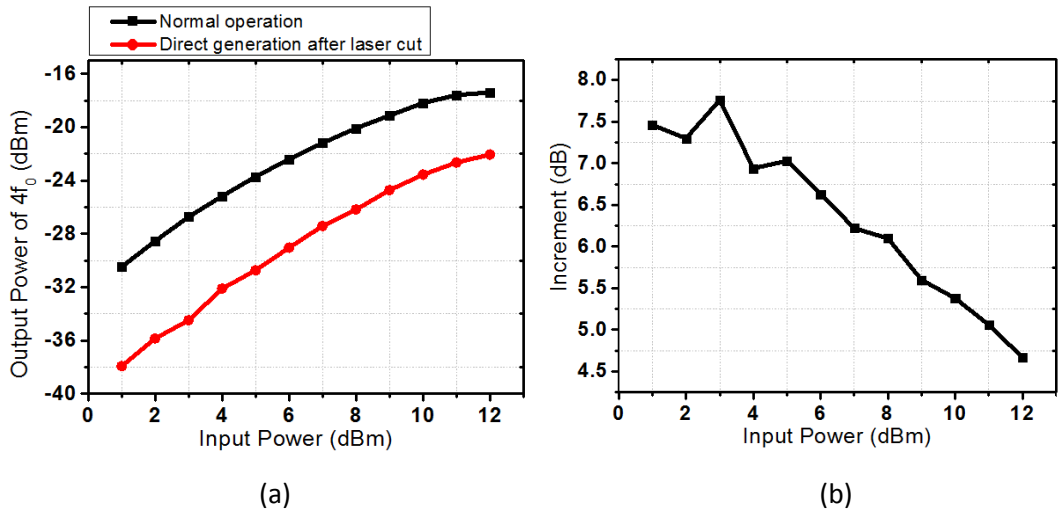


Figure 4.11 (a) The output power of two conditions. (b) The increment.

Now, we can compare the measurement date with simulation results. Figure 4.12 shows the comparison of figure 3.26(b) with figure 4.11(b), which represents the efficacy of sub-harmonic mixing. From the plot the similarity is enough to test and verify the design.

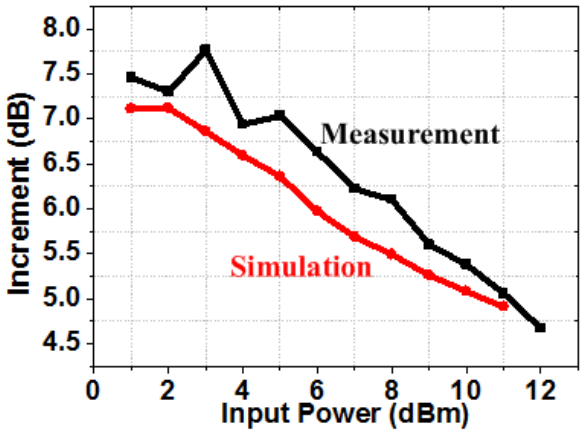


Figure 4.12 The comparison of figure 3.26(b) with figure 4.11(b).

4.2.4 Phase Noise Between Input and Output

Finally, the measured phase noise of the input and output signal are shown in figure 4.13. The phase noise measured shows the difference between the 12.5 GHz input signal source and forth-order output are around 12.5 dB, which is consistent

over the offset frequency range below 1 MHz. This difference agrees well with the theoretical value of 12 dB corresponding to the multiplication ratio of 4. This is an another merit of multiplier for the reason that maybe we can yield the signal source with lower phase noise.

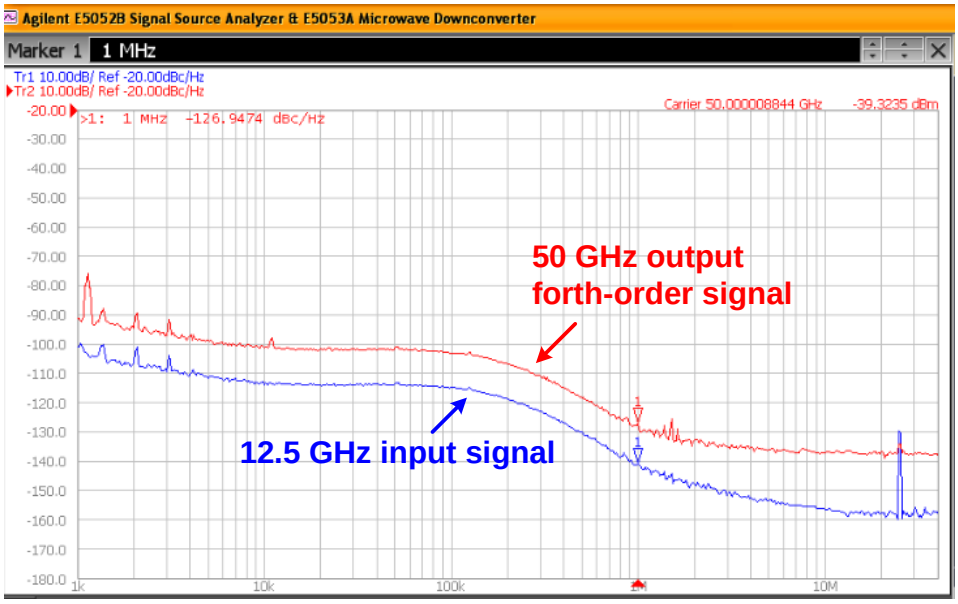


Figure 4.13 The measured phase noise of the input and output signal.

4.3 Comparison with Published Works

Table 4.2 summarizes the performance comparison between the proposed quadrupler and published results in literature. Apparently, this work has considerable prominence in respects of power consumption and spur harmonic rejection.

	[1] EuMIC 2010	[2] TMTT 2005	[3] EuMIC 2009	[5] JSSC 2008	[6] APMC 2009	[7] SOCC 2009	[8] JSSC 2004	This work
Technology	SiGe BiCMOS 0.25 μm	CMOS 0.18 μm	HBT	CMOS 90nm	CMOS 65nm	pHEMT	GaAs pHEMT	CMOS 90nm
Output frequency (GHz)	60	40	77	324	60.36	60	30	50
Power consumption (mW)	11.7	115	46	12	3.1~6.8	N/A	50	Core 2.95 Buffer 4.2
Supply voltage (V)	1.3	2.2	3.3	1	0.6	N/A	2	1.2
Pin / Pout (dBm)	8 / -10	-18 (QVCO)	0 /	-46 (QVCO)	-77	5 / -10	5 / -4	8 / -20
HRR (dB)	HRR1 34 HRR2 15 HRR3 16	HRR1 23 HRR2 >5 HRR3 27	N/A	HRR1 39	N/A	HRR1 23 HRR2 23 HRR3 21	HRR1 26 HRR2 34 HRR3 22	HRR1 56 HRR2 30 HRR3 44
Chip size (μm^2)	740x570	1280x850	250x750 (core)	210x180 (core)	300x60 (core)	1900x1000	2000x1500	832x733

Table 4.2 Summaries and Comparison with Published Works.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this thesis, a frequency quadrupler was designed and analyzed. This nonlinear circuit was fabricated using 90-nm low leakage CMOS technology.

The frequency quadrupler makes a better use of the existing sub-harmonic mixing to enhance the generation efficiency. According to the measurement results, the sub-harmonic mixing provides a increment of 4 to 6 dB for the method of merely direct generation without additional power consumption. Furthermore, the fabulous spur harmonic suppression make the practical application more convenient, and the DC power consumption is still lower than prior works. Of course, detailed analyses and investigations were demonstrated to optimize the performance.

5.2 Future Work

The mechanism of generating the forth-order harmonic at $4f_0$ is intrinsically a broadband technique. An output tank with broader frequency response could further accentuate the advantage of the quadrupler. Moreover, the frequency tuning range of VCO is rather narrow at high operating frequency. Therefore, base on the VCO operating at low frequency with the property of large FTR and low phase noise, through the multiplier to turn into a high frequency source with the great performance more than the VCO designed at high frequency.

Figure 5.1 shows the FTR of VCO published in recent years. It clear reveals the degradation as operation frequency increasing. Therefore, our target is the frequency which exceed the f_{max} of the most advanced process.

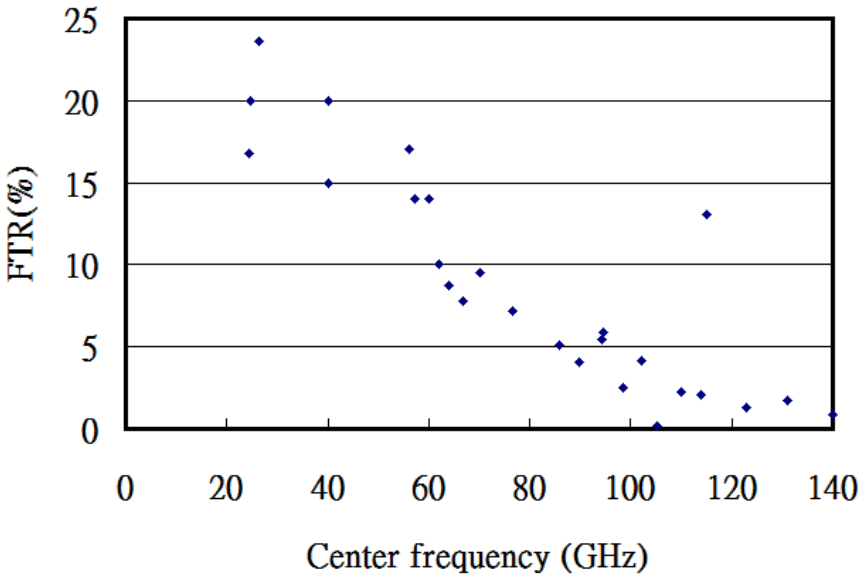


Figure 5.1 The FTR of VCO published in recent years.

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