國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

氟摻雜對應變矽於二氧化鉿堆疊式金氧半場效電晶體其特性和可靠度的影響

Impact of Fluorine Incorporation on Characteristic and Reliability Issues of the CESL Strained nMOSFETs with HfO_2/SiON Gate Dielectric Stack

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中 華 民 國 九 十 九 年 七 月

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A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of Master

In

Electronics Engineering

July 2010

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 九 年 七 月

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摘要

根據2007年ITRS所訂定出的金氧半場效電晶體的閘極尺寸，當元件尺寸持續縮小，因傳統的二氧化矽介電層，當厚度降到1至1.5奈米左右，會有顯著的量子穿隧效應而導致漏電流大到無法忍受的規範。近年來使用高介電質材料來取代二氧化矽介電層已被廣泛研究。相較於二氧化矽，在相同的等效厚度(EOT)之下，高介電質物質有較厚的實際厚度,因此可以抵擋因量子穿遂效應而導致的大量漏電。然而，以高介電質材料當閘極介電層卻遭遇到其它的問題要解決，如：介面

的粗糙度導致載子遷移率的下降;高介電質材料有較高的界面狀態產生及較多的電荷捕捉，對臨限電壓的漂移有較嚴重的影響。

研究指出，材料間的應變作用，可讓遷移率上升，故驅動電流會有大幅度的提升，對現今微縮的COMS元件來說，用應變作用導致遷移率上升，是非常重要的突破，因為它不用增加額外的製程步驟卻可以提供更高的驅動電流，如:淺塹渠絕緣(shallow trench isolation，STI)，矽化反應(slicidation)，接觸孔蝕刻停止層(contact etch stop layer，CESL)等製程，皆可運用存在其應力施加於通道，使遷移率上升。其中，接觸孔蝕刻停止層是最普遍使用於nMOSFET的方式。然而，以電漿增強型化學氣相沉積(PECVD)沉積出的Si_3N_4氮化物薄膜，理想比並不佳，其薄膜化學式更準確地可寫成SixNyHz，指出它為非理想比組成且其薄膜含有氫(通常為9至30%)。其氫離子在後續製程中，會向下擴散至通道，使表面有大量的Si-H鍵，這種較弱的鍵結，容易被熱載子打斷，造成元件在做熱載子應力的穩定性不佳和可靠度劣化的問題。

本文提出在閘極介電層沉積前，使用離子佈值的方式使氟離子在後續的高溫摻雜活化的過程中，使其擴散至通道和閘極介電層。我們發現，摻雜氟對於應變矽元件的基本特性沒有顯著的降低，而分析可靠度方面，我們深入探討固定電壓應力(CVS)和熱載子應力(HCS)效應下的影響。觀察到在應力的破壞下，有氟摻雜的元件，有較小的臨界電壓偏移，對於元件的可靠度和穩定性都有明顯的改善。其主要原因是來自於氟原子併入高介電閘極主體以及閘極層與通道界面間，不僅

可修補界面狀態的懸空鍵結(interface dangling bond)和較低界面狀態產生，且可有效減少高介電閘極本體的捕捉電荷情形。

最後在應力測試後再進行回復(relaxation)的行為，在CVS下的回復行為，觀察載子具有逃逸(de-trapping)特性，而有氟摻雜的元件有較少載子捕捉情形(應力下)及較高逃逸能障使得有較少逃逸現象產生(回復下)，這與先前討論Frenkel-Poole傳導機制，有較深的載子捕捉位置有好的關連性。

Impact of Fluorine Incorporation on Characteristic and Reliability Issues of the CESL Strained nMOSFETs with HfO_2/SiON Gate Dielectric Stack

Student : Fang-Yu Chiu **Advisor : Dr. Jen-Chung Lou**

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

Abstract

From the scaling trend in ITRS 2007, the conventional SiO_2 layer, which is only 1-1.5 nm thickness, would suffer serious leakage from tunneling effect. Therefore, the High-K dielectric layer is used to replace SiO_2 dielectric layer.

We could apply its predominance to avoid its serious tunneling leakage current from quantum tunneling effect under the same effective oxide thickness (EOT), because the High-K dielectric has thicker physical thickness. However, this replacement also faces some challenges to solve. Like, degraded channel mobility from interface roughness; more serious V_{TH} shift from higher interface states

generations and more oxide bulk charges, etc.

As our known, we could enhance mobility for drive current by strain engineering. In fact, for nowadays scaling CMOS, it is essential for better mobility. It is a good technique to improve driving current without extra processes. The techniques like, shallow trench isolation (STI), slicidation, contact etch stop layer (CESL) all could insert strain into channel for better mobility. Most of all, the most widely used technology is CESL for nMOSFETs. However, it could face the setbacks from its uncontrollable quality Si_3N_4 deposited by PECVD. Since its variable composition control, the layer is called SixNyHz precisely, which indicates its hydrogen content (9~30%). Worst of all, hydrogen would diffuse into the interface of dielectric layer and channel and then eventually result degraded reliability and uncontrollable characteristics。

In my thesis, we incorporate fluorine before gate dielectric deposition via channel implantation technique, which was subsequently diffused into the gate stack during annealing process. The implanted fluoride effect little for device characteristics degradation. For its reliability, we also analyze deeply its effect on constant voltage stress (CVS) and hot carrier stress (HCS). We found the device with fluoride dopants would suffer smaller V_{TH} shift after stress. It is on of evidences fluoride advantage on its reliability and stability improvement. The predominance mainly comes from

dopanted fluorine ions into the interface between interface of dielectric layer and channel would recovery interface dangling bonds result in lower interface state generations and eventually reduces High-K dielectric layer bulk trapping.

After CVS relaxation, with fluorinated device, less carrier are trapped after stress and less de-trapping from deeper traps barrier height after relax. This phenomenon could elucidate from Frenkel-Poole emission for relation between de-trapping and its traps location.

誌謝

考上交大後，很幸運的進到羅正忠老師的實驗室。在這兩年中，不論是在課業及論文遇到的困難，老師及學長都會適時地給我幫助，讓我總是克服一次又一次的問題，才能順利地拿到這個學位。由衷的感謝我的指導教授-羅正忠博士，不但在論文的研究方向給予我很明確的指示，更教我們做人的道理和處事應對的態度，讓我們日後出社會，不單是學到了專業知識，也學到了正確的學習態度，跟倫理規範。

再者感謝，實驗室的博班學長-智仁與威良學長。特別要感謝智仁學長在實驗及量測上給了我很多的幫助，每次量測看到不如預期的結果，多虧有智仁學長不厭其煩的幫我看哪個環節出了問題，是儀器沒接好，還是條件設錯，或根本是元件無法量測…等諸多原因，都會一一跟我細講是為什麼，慢慢的，自己也有了基礎概念跟獨力解決問題的能力。真的是非常感謝智仁學長的教導。而威良學長算是生活方面的益友，課業及論文上的幫忙當然是少不了，但在吃的方面，幫助更大，每次實驗室的聚餐，沒有威良學長的吆喝，哪能成行!。然後很感謝實驗室的奇葩-裳哥，在我們還是小碩一時，就很熱心的招待我們，過去的兩年訓練我們機台，三不五時就請我們吃東西，論文實驗也是裳哥帶著做，這當中有許多的酸甜苦辣，當下覺得很辛苦，有諸多的抱怨。但回過頭來想，這也是一種很特別的人生體驗。當然，尚勳、文新，都是一起同甘共苦的好夥伴。沒有他們，我就不能跟大家一起趴趴走，遠離只有二餐的日子!這份 ED523 的情誼，深刻印在我心中。

當然不能忘記，我的男友小量和那些麻吉們(小逸、喬、錦屏、阿田、熊、逼)，給予我很多的鼓勵，每每聽我發發牢騷，當我的垃圾桶，對一開始很不習慣交大生活的我，有人可以吐吐苦水。有這群夥伴相挺，才讓我有動力持續往前走。特別感謝小量在口試前還撥空下來，幫我這個電腦白癡的報告做精美動畫，讓我沒有後顧之憂。另外我在碩二的宿舍生活認識了兩個好室友-玉芬和佩砡，跟她們一起住，真正享受到何謂宿舍生活，那些一起玩紙牌遊戲，瘋狂團購、打打鬧鬧的日子,絕對是我第二年最美好的回憶,想到不能跟他們一起住,有無限感概啦！

最後要感謝的就是我的家人（充滿大道理的爸爸、超級辛苦的媽媽、酷酷的大弟、可愛的Q明小弟），不論是發生甚麼事，好的壞的，回到家跟他們一起吃飯、聊天，看電視…只是很普通的行為，就可以讓我煩惱，不順心的感覺都不再那麼強烈，人可以很自然的放鬆，不禁大喊：有家的感覺真好!! 另外感謝我小弟，考上隔壁校當我鄰居督促我這懶惰骨頭打羽球、慢跑，過著健康的生活，好像是我的體能教練。(雖然宵夜也吃得多)

要感謝的人實在是太多，(栗子、文仙、張耀仁、蘇倉賢、張博翔…等)大家的幫忙對我來說像一場又一場的及時雨，雖然無法一一列出所有的人和細節，只能誠摯的向那些幫忙過我但未提及的人說一聲：謝謝!

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Chapter 1 Introduction

1.1 Introduction to High-K gate dielectric

1.1.1 Background

With IC technology flourish, the Moore's Law, proposed by Gordon Moore in 1965, states that the number of transistors on integrated circuits doubles every 18 months. The key factor for Moore's Law being obeyed is that Wafer Fabrication can continuously introduce new manufacturing techniques, so as to decrease feature size and minimize critical dimension (CD). Therefore, they can increase the number of transistors on the chip on time. Scaling raises chip speed and promote performance； increasing the number of transistors costs down making chips[1-2]. Thinner gate oxide provide higher drive current and improve gate control to channel so that suppress short channel effect (SCE) [3-4]. According to the 2007 ITRS (International Technology Roadmap for Semiconductors) roadmap, the SiO_2 gate dielectric film thickness should be scaled down to 1.0 nm for 35nm technology node (Table 1.1)[7]. However an ultra-thin SiO_2 film comprising a few atomic layers causes a certainly large direct-tunneling current through the film. The direct tunneling current which depends on physical film thickness (T_{ph}) (equation1.1) could cause an intolerable level of off-current, leading to huge power dissipation and heat. (equation1.2)

$$I_{DT} \propto \exp\left(-\sqrt{\frac{2mq\phi}{(h/2\pi)^2}}T_{ph}\right) \qquad (1.1)$$

$$P_T = ACV^2f + VI_{peak} \qquad (1.2)$$

Where A is the fraction of gate actively switching and C is the total capacitance load of all gate. The sum of dynamic power component (ACV^2f) and static power component (VI_{peak}) defines total power consumption. Gate oxide continues shrinking, static power consumption will increase due to gate oxide leakage and subthreshold leakage current (Fig.1.1). In addition, reliability issues become a serious concern for a thin SiO_2 dielectric only 1-1.5nm. It points out that SiO_2 uniformity is even more difficulty in the growth of such a thin film, since even a mono-layer difference in thickness represents a large percentage difference and thus can result in the variation of threshold voltage (V_{th}) across the wafer. As shown in Fig. 1.2, we can see that when the gate oxide thickness scales down to 2nm, the leakage current will exceed the limit of $1A/cm^2$ set by the allowable stand-by power dissipation. Further scaling of oxide thickness to below 2 nm, the direct tunneling current will increase exponentially, causing intolerable power consumption.

To reduce the tunneling leakage current, the new materials High-k dielectric has been widely investigated as possible replacement to the SiO_2 film as gate insulators [5-6]. According to the first order current-voltage relation in equation (1.3), the driving current of a MOSFET can be given as

$$I_{D.sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (1.3)$$

$$C_{ox} = \frac{\kappa\varepsilon_0 A}{T_{ox}} \qquad (1.4)$$

Where V_{GS} is the applied gate to source voltage, L is the effective channel length, W is the channel width, V_{TH} is the threshold voltage, μ_n is the electron mobility, C_{ox} is the gate capacitance, k is the dielectric constant, $\varepsilon_0$is the permittivity of free space and T_{ox} is the oxide film thickness.

In order to improve the current drivability, we can reduce threshold voltage, increase operation voltage, shorter channel length and bigger capacitance or mobility. However, some methods have their limitations. A larger V_{GS} will cause the reliability issue. V_{Th} is too small to result in statistical fluctuation in thermal energy at typical operation conditions of up to 100 ℃. Hence a shorter L and bigger C_{ox} (means reduce oxide thickness equation (1.4)) will be useful to provide device performance. However, thinner oxide thickness could cause intolerable leakage current. To reduce the tunneling leakage current, the new materials High-k dielectric has been widely investigated that it replaced SiO_2 dielectric. In order to maintain the same C value, C can be written as follows: (equation (1.5))

$$C_{ox} = \frac{\kappa\varepsilon_0 A}{T_{high-k}} = \frac{\varepsilon_0 A}{EOT} \qquad (1.5)$$

The main reason is that base on the same equivalent oxide thickness (EOT), high-K dielectrics have thicker physical film thickness, so it can significantly reduce

direct tunneling leakage current generating without sacrificing the performance, as shown in Fig. 1.3

Otherwise, the reliability issues become a huge concern for this thin regime of SiO_2 film because the direct tunneling electrons make it more vulnerable for given conditions and eventually cause a possible threshold voltage fluctuation or even dielectric breakdowns of devices, which result in a malfunction or failure of device [8]. Therefore, searching a material with a high dielectric constant to replace SiO2 is urgently needed.

1.1.2 Recent High-K Gate Dielectric

There are some critical principles to select proper high-k dielectric material. The first one is that the k value should be as high as possible, but it shouldn't be too high. Because it could degrade the electrical properties due to increase field induced barrier lowering (FIBL) (Fig. 1.4) (i.e. fringing field from the gate to the source/drain which degrade short channel effects of MOSFETs [9].) On the same token, the k value shouldn't be too low, otherwise it will lose its main propose of substituting for high-k materials. Secondly, the band offset obstructs carriers injected from the gate or source into a dielectric film. Hence, higher band offset is required.

Thirdly, thermal stability and quality of interface between high-k dielectric and

Si substrate are important. For all thin gate dielectrics, the interface with Si substrate plays a key role, and in most cases is the dominant factor in determining the overall electrical properties. Therefore, the high-k dielectrics require an interfacial reaction barrier to minimize the undesirable reactions with Si substrate. In addition, Fig. 1.5 shows the characteristics of oxygen diffusion through high-k dielectric materials [10]. Due to the rapid oxygen diffusion, an additional interfacial layer forms between the high-k dielectric and Si substrate. However, it is no benefit to scale down due to its low permittivity. Therefore, proper capping technology might be applied to avoid undesirable interfacial reaction with high-k dielectric.

Fourthly, Gate and fabrication process compatibility also are considered. The conventional poly gate with high-k dielectric does not seem to be a good technology any more. Because poly gate concerns poly depletion effect, it results in increase of EOT [11-12]. Otherwise，boron diffusion through high-k dielectric also degrades V_{TH} stability and reliability [12]. Moreover, Fermi level pinning affects narrow down of on-off margin in operation voltage of CMOS [13].

Various high-K dielectrics, including tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), cerium oxide (CeO_2), strontium titanate ($SrTiO_3$), and hafnium oxide (HfO_2) have been extensively studied as the alternative gate dielectric. Among these high-K dielectrics, HfO_2 is considered as one of the most

proper candidates under investigation, since its thermal stability in contact with silicon (47.6Kcal/mole at 727℃) compared to TiO_2 and Ta_2O_5, high permittivity (k~25~30 for HfO_2) compared to Si_3N_4 and Al_2O_3, a large band gap 5.6eV with band offsets to silicon >1.5eV, appropriate barrier high for both electrons and holes (> 1eV), and compatible with poly-silicon.

1.1.3 Motivation

There are still a number of pending issues when high-k dielectrics are applied in future technology nodes, including high density of traps in the bulk dielectric and interfacial layer which will cause channel mobility degradation and threshold voltage instability. The high-k dielectric layer has soft optical phonons and the long-range dipole would degrade the effective carrier mobility in the inversion layer of the Si substrate [14]. Yang et al. [15] summarized the effects of all scattering and degradation mechanisms on the channel carrier mobility, as shown in Fig. 1.6.

The threshold voltage (V_{TH}) shift of the poly-Si/high-k stack is another challenge that must be considered. Reliability characteristics of the Hf-based dielectric such as hot carrier induced degradation (HCI), bias temperature instability (BTI), and time dependent dielectric breakdown (TDDB) have been investigated in the high-k dielectric gate stack. One of main issues for high-k gate stack is the charge trapping

characteristics during reliability test. Initial observation of instability was studied through capacitance-voltage (CV) characteristics in flat-band voltage change and current-voltage (IV) change.

Historically fluorine incorporation into gate dielectric is known as an effective way to passivate the interface traps in the conventional SiO_2 gate dielectric and it can improve device reliability because it was known that fluorine incorporation in the SiO_2 gate dielectrics replaces Si–H bonds with Si–F bonds, Si-F bonds rather strong than Si-H bonds. But the high-k oxides itself exist much more bulk defects than silicon oxide and suffer from a high density of charge traps. This causes instability of the gate threshold voltage, couloumbic scattering of carriers in the Si channel, and possible reliability problems. Recent research indicates that the main charge trap is the oxygen vacancy V_0 [16]. F was found to substitute at the V_0 site and passivates it. In addition, the high-k oxides differ from Si:H or SiO_2, i.e. they all have ionic bonding, thus F is one of the best passivation for defects in an ionic oxide because it is the only element that is more electronegative than oxygen and its bond length is similar. Therefore fluorine incorporation was found to have a large beneficial effect on charge trapping [17-19] and can improve both the device performance and reliability.

However, an excess amount of F incorporation increases oxide thickness. It is

known that excessive F annealing replaces Si–O bonds with Si–F bonds, which generates reactive oxygen atoms. The oxygen atoms react with silicon substrate and leading to form thick interfacial SiOx layer [20-21]. Therefore, the F ion concentration at the HfO_2/SiO_2 interface may be an essential aspect of such a defect passivation scheme. Previous research suggests an insight into this problem. It was observed that the concentration of interstitial F ions was reduced by two orders of magnitude after a 400℃ FGA. Hydrogen annealing seems to be able to remove excess F ions which are not strongly bonded in the bulk region of the HfO_2 films [22].

1.2 Introduction to CESL Induced Local Strained HfO_2 nMOSFET

As scaling of CMOS technology reaches its physical limitations, HfO_2 gate dielectric has received considerable attention due to advantages such as sufficiently high dielectric constant (15~25), good thermal stability, wide bandgap (5.6eV), and large band offset(~1.5eV)[23]. However, threshold voltage instability, low carrier mobility, and dielectric remain critical problems for High-K gate dielectric. The improvement of carrier mobility has also been intensely studied by introducing strain in the channel region. One of the most popular technologies is using high tensile-stress contact etch stop layer (CESL), which can obviously improve electron mobility and

drive current for nMOSFETs [24-26]. Therefore, a CESL strained high-K nMOSFET for high mobility application has been proposed. A high performance CESL strained nMOSFET with HfO_2 dielectric is successfully demonstrated.

However, it could face the setbacks from its uncontrollable quality Si_3N_4 deposited by PECVD. Since its variable composition control, the layer is called SixNyHz precisely, which indicates its hydrogen content (9~30%). Worst of all, hydrogen would diffuse into the interface of dielectric layer and channel and then eventually result degraded reliability and uncontrollable characteristics。Recent researches point out that at $Si:SiO_2$ interfaces, the defect density is further lowered by hydrogenation, with any Si dangling bond P_b scenters converted to Si–H bonds. Historically fluorine incorporation into gate dielectric is known as an effective way to passivate the interface traps in the conventional SiO_2 gate dielectric and it can improve device reliability because it was known that fluorine incorporation in the SiO_2 gate dielectrics replaces Si–H bonds with Si–F bonds, Si-F bonds rather strong than Si-H bonds. Therefore, for the first time, we try to do a novel CESL strained HfO_2/SiON gate dielectric with fluorinated to improve reliability problem.

1.3 Organization of the Thesis

This thesis consists of four chapters. The main topics are focused on the effects of

fluorine incorporation into passivation dielectric of n-MOSFETs with HfO_2/SiON gate stack, evaluated in terms of reliability and performances. We study systematically the electrical characteristics of the CESL strained HfO_2/SiON dielectric with fluorinated, its reliability issues, and the behavior of charge trapping. In addition to this chapter that is dedicated to introduce the reason of the strained high-k dielectrics on CMOS technology and systematic discuss the effects of fluorine incorporating on MOSFETs with high-k gate dielectric stacks, this thesis is organized as follows :

In chapter 2, we describe the experimental procedure for fabricating n-MOSFETs test devices with HfO_2/SiON gate stack as well as fluorine incorporation dielectric. First, we use SIMS to analysis fluorine profile on interface between high-K dielectric and silicon substrate and use XPS to see whether fluorine can effectively bond with Hf. Then, show some basic electrical characteristics with and without fluorine incorporation, i.e., I-V and C-V characteristics.

In chapter 3 presents the effects of fluorine incorporation on HfO_2 nMOSFET reliability. Charge trapping characteristics, i.e., dynamic trapping analysis with stress dependent high-k film quality, threshold voltage shifts as indicating factors will be discussed. Besides, hot carrier reliability of the strained HfO_2/SiON dielectric with fluorinated is also investigated. Finally, the lifetime extraction based on DC stress

suggests that the high-k dielectric with fluorinated can provide optimistic results.

In chapter 4, we conclude with summaries of the experimental results above and suggest the possible future researches in this area.

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Year of Production	2007	2009	2010	2011	2012	2013	2015
MPU/ASIC Metal1 ½ Pitch (nm) (contacted)	68	52	45	40	36	32	25
High Performance Logic Technology EOT Requirements							
Extended Planar Bulk (Å)	11	7.5	6.5	5.5	5		
UTB FD-SOI (Å)			7	6	5.5		
DG MOSFET (Å)				8	7	6	6
Low Operating Power Logic Technology EOT Requirements							
Extended Planar Bulk (Å)	12	10	9	8	8		
UTB FD-SOI (Å)				9	9	8	8
DG MOSFET (Å)				9	9	8	8
Low Stand-by Power Logic Technology EOT Requirements							
Extended Planar Bulk (Å)	19	15	14	13	12	11	
UTB FD-SOI (Å)					13	12	10
DG MOSFET (Å)					14	13	11

*UTB FD-SOI : ultra-thin body fully-depleted silicon-on-insulator
DG MOSFET : double-gate MOSFET.
: manufacturable solutions are NOT known.

Table 1.1 2007 ITRS roadmap

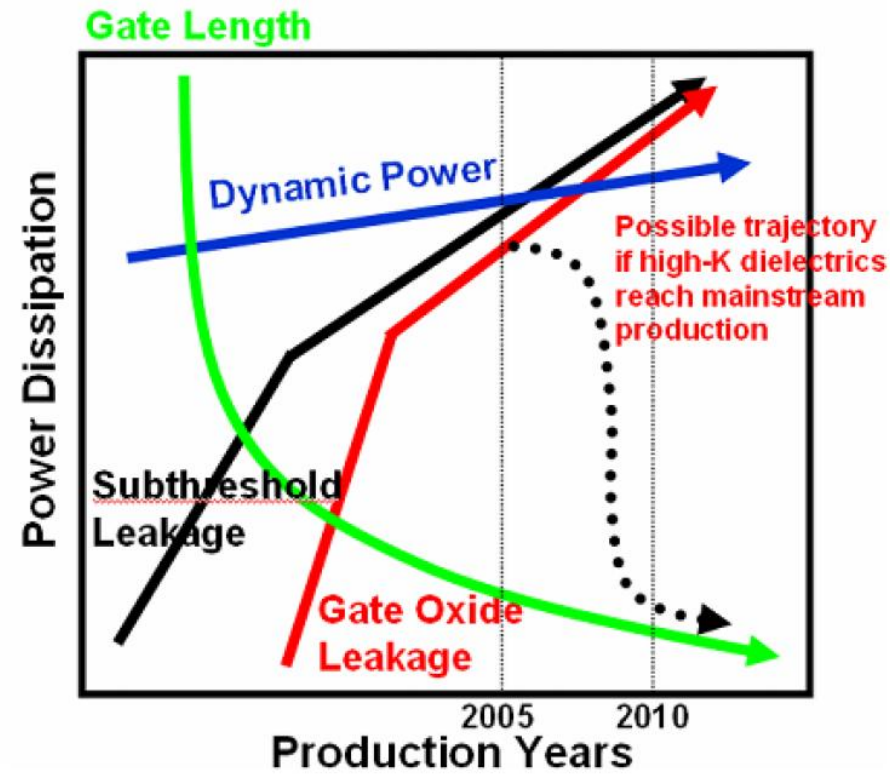


Fig.1.1 Power dissipation (dynamic + static power) with each generation

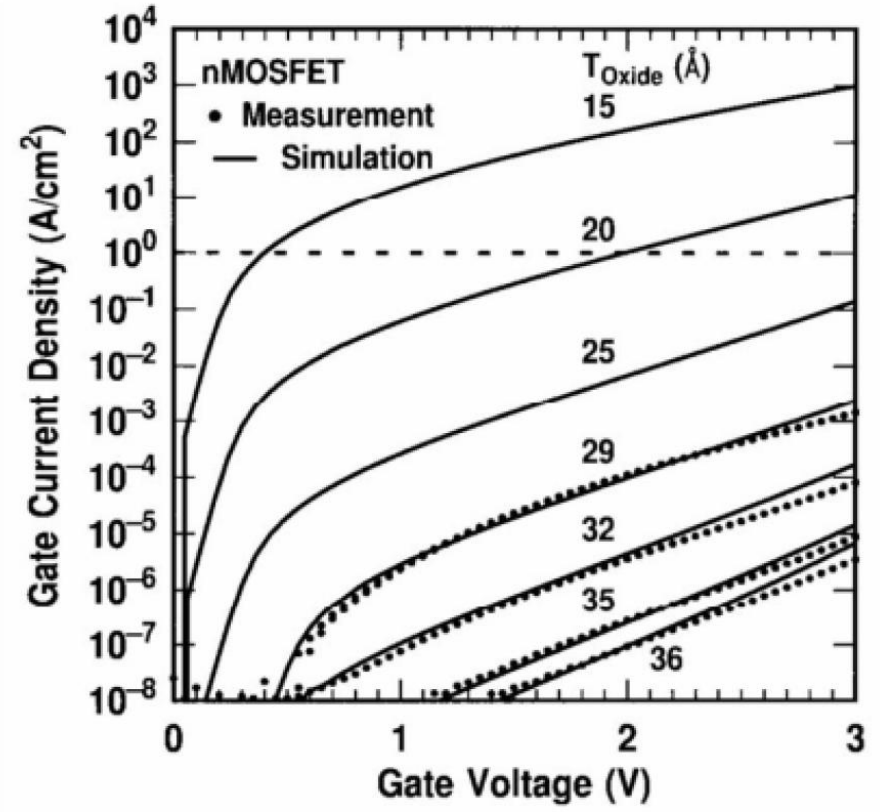


Fig. 1.2 Measured and simulated Ig-Vg characteristic under inversion conditions of SiO_2 nMOSFET device

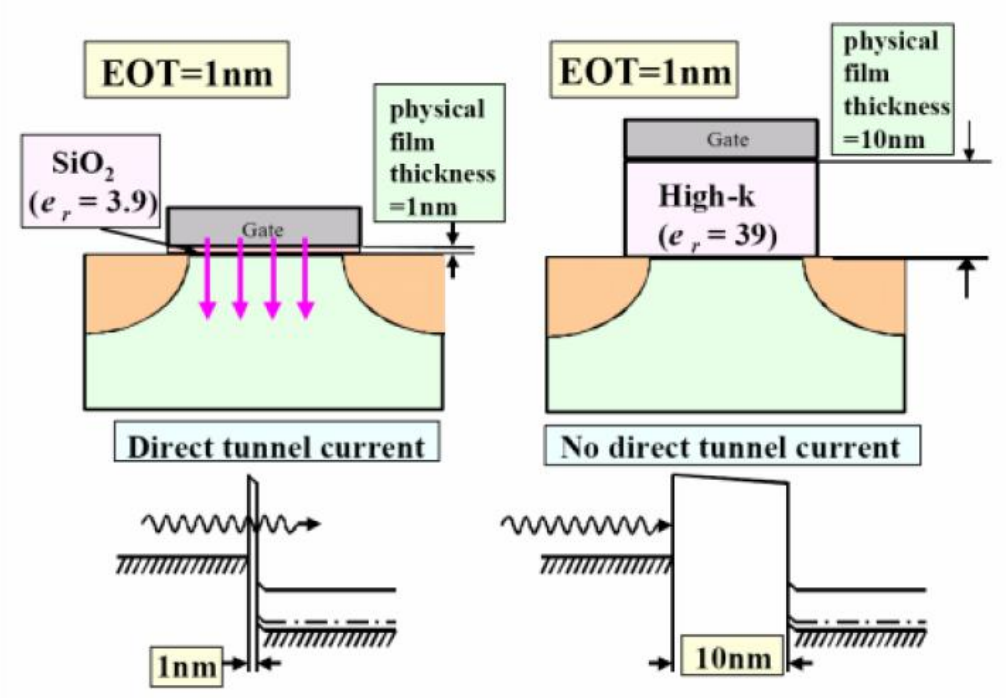


Fig. 1.3 By using high-k material to suppress gate direct-tunneling current

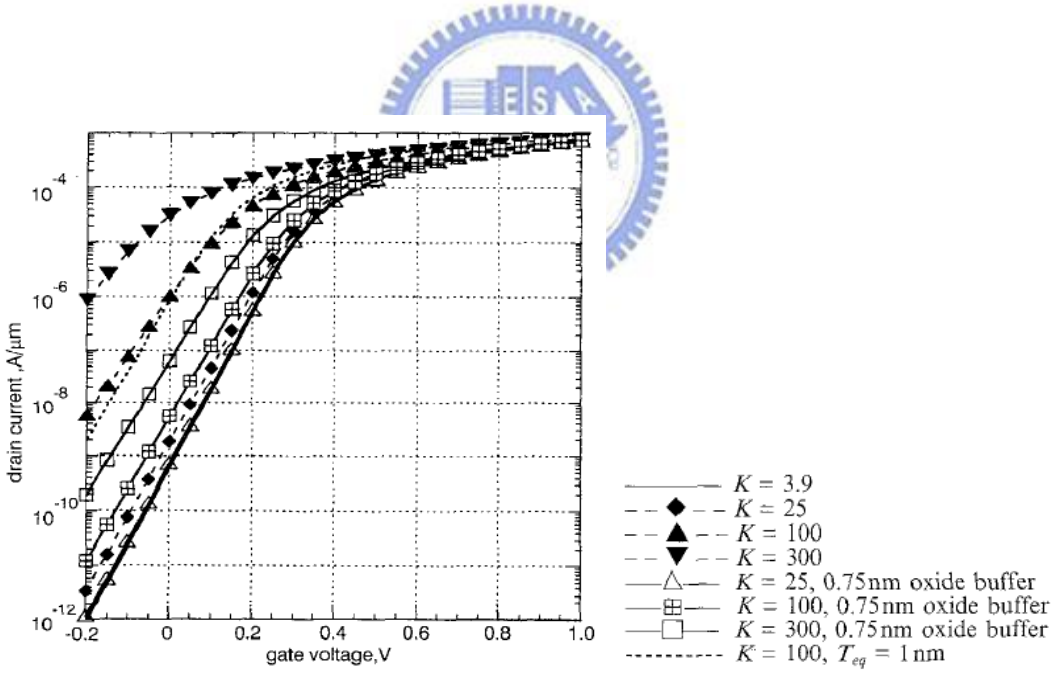


Fig. 1.4 FIBL causes increased off-state leakage in 1.5nm equivalent thickness high-K gate dielectrics devices (more for the case of no oxide buffer)

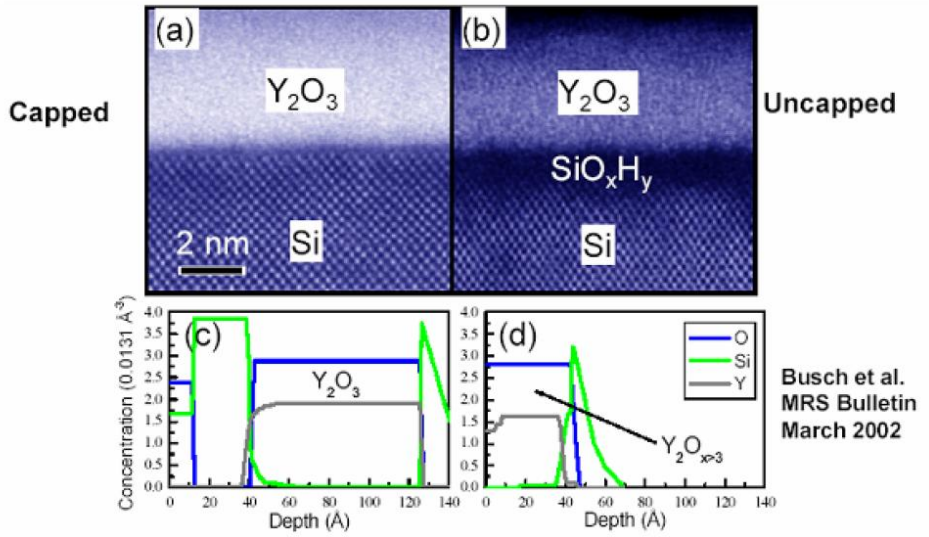


Fig. 1.5 TEM and SIMS analysis of Y_2O_3 high-k dielectric with capped and uncapped samples. Uncapped Y_2O_3 sample shows additional interfacial layer due to oxygen diffusion.

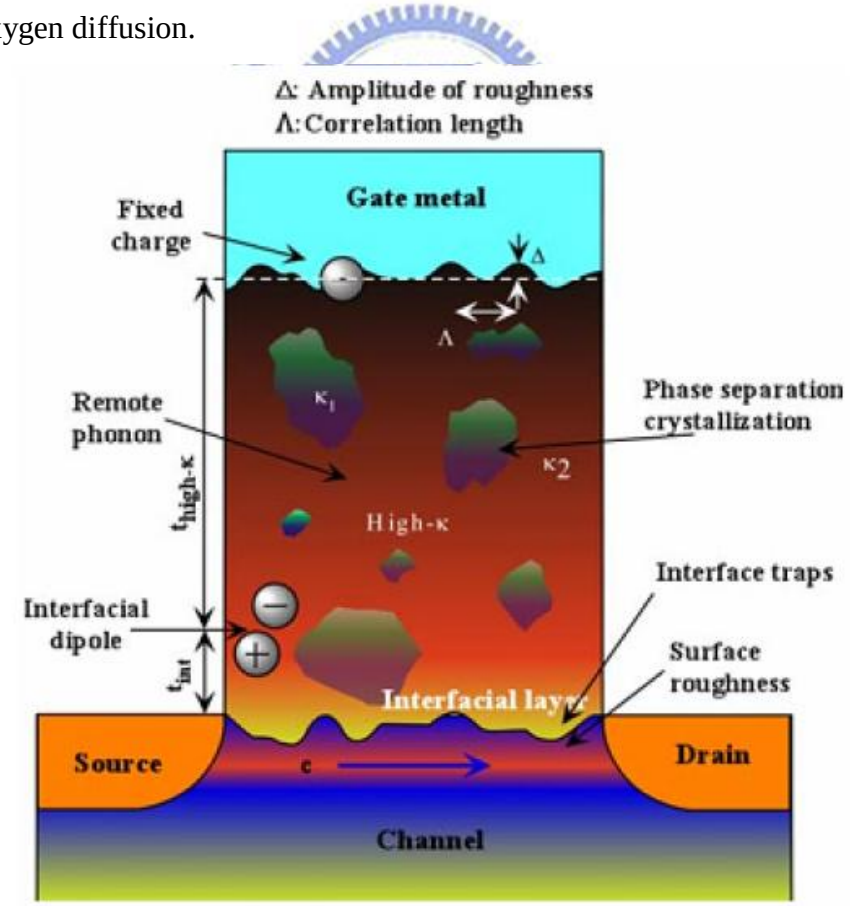


Fig. 1.6 Schematic representation of factors contributing to carrier mobility degradation in a high-k oxide layer.

Chapter 2

Characteristics Issues of Fluorine Incorporation on the CESL strained HfO_2/SiON gate dielectric

2.1 Introduction

There are still a number of pending issues when high-k dielectrics are applied in future technology nodes, including high density of traps in the bulk dielectric and interfacial layer which will cause channel mobility degradation [1-2] and threshold voltage instability [3].In order to improve device performance, strain engineering has been proposed to increase carrier mobility for metal oxide semiconductor field transistors (MOSFETs) below to sub 90nm node [4-5]. In this situation, a nitride contact etch stop layer (CESL) is the most common strained method for nMOSFET. However, using plasma-enhanced CVD (PECVD) that deposits nitride strained layer has an undesirable problem of reliability degradation. Because gas source of PECVD is usually ammonia (NH_3), in the follow-up process, hydrogen ions would downward diffuse to gate dielectric layer and interface between dielectric layer and Si substrate and then formed Hf-H bond or Si-H bond, and both of which bonding energy are relatively weak. Therefore, when testing hot-carrier stress (HCS) reliability issues, it shows poorer consequence[6]. Previous studies demonstrated that for usual (no strained) devie,the fluorine passivation to improve reliability by forming stronger

bonding energy and enhance the electrical characteristics of high-k dielectric MOSFETs by eliminating inherent bulk traps[7-9]. In this work, we use silicon surface fluorine implantation (SSFI) method to attain role of fluorine passivation and then investigated the defect passivation with fluorine in a CESL strained nMOSFET with hafnium oxide (HfO_2) and poly-Si gate. The novel fluorinated CESL gate stack device obviously improves the gate dielectric/Si substrate interface immunity hot-carrier damage and exhibits better dielectric breakdown characteristic.

2.2 Experimental Procedure

The experiment propose a simple and effective fluorine incorporation technique that use SSFI method embedded in the CESL strained HfO_2/SiON gate dielectric. In the proposed fluorine incorporation method, we introduce the fluorine atoms into the HfO2 bulk material and the gate dielectric/Si substrate interface.

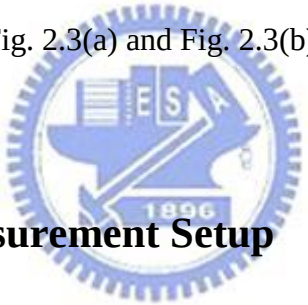
2.2.1 Device Fabrication Flow

We use standard local oxidation of silicon (LOCOS) process for device isolation. The nMOSFET device was fabricated on 6-inch p-type (1 0 0) Silicon wafer. After forming 300Å sacrificial oxide, fluorine was incorporated by ion implantation. To investigate the effect of various fluorine concentrations on the device performances,

doses that we implanted are 1E12cm^{-2}, 1E13cm^{-2} and 1E14cm^{-2}, which defined as SSFI A, SSFI B, and SSFI C, respectively. The schematic diagram is shown in Fig. 2.1. After removing sacrificial oxide by dipping in HF solution, standard RCA clean was used to remove particles, organics and metal contamination. Immediately, a thin interfacial layer about 1nm oxynitride layer (SiON) was formed by a conventional rapid thermal oxide (RTO) at 800℃ for 30sec in nitrous oxide (N_2O) ambient. And then 3nm HfO_2 film was deposited by the AIXTRON metal organic chemical vapor deposition system (MOCVD) at a substrate temperature of 500℃, followed by 600℃ in nitrogen (N_2) ambient RTA for 30sec in order to improve the quality of high-k dielectrics. The physical thickness of the SiON and HfO_2 films was measured by optical N&K analyzer. Then a 200nm poly-silicon was deposited by low pressure chemical vapor deposition (LPCVD). Subsequently, gate electrode was defined by I-line lithography stepper and etched by ECR etching system. After removing sidewall spacer, S/D extension implantation was implemented by As implantation. Spacer formation was carried out by plasma-enhance chemical vapor deposition (PECVD) and then S/D implantation was executed by Arsenic implantation. After implanting, rapid thermal anneal (RTA) was performed at 950℃ for 30sec in N_2 ambient to activate dopant. Afterward, 3000Å-thick SiNx passivation layer was deposited by PECVD at 300℃ with SiH_4 and NH_3. And then we deposited 1000Å

SiO_x layer to avoid excessive stress. For comparison, the control sample was deposited with a 4000Å -thick conventional PECVD-TEOS passivation layer. After passivation layer formation and contact hole pattering, Al-Si-Cu metallization was deposited by FSE-Cluster-Physical Vapor Deposition (PVD) system and then pattering. Finally, sintering process at 400℃ for 30 minutes in N_2 ambient is eventually executed to finish our devices in this thesis.

The main process flows are summarized in Fig. 2.2 (a) and (b). Schematic cross section of the control and strained HfO_2/SiON n-MOSFETs with fluorine incorporation is illustrated in Fig. 2.3(a) and Fig. 2.3(b), respectively.



2.2.2 Suitable Measurement Setup

The experimental setup for the I-V, C-V and reliability measurements of MOS device is illustrated in Fig. 2.4. Based on the PC controlled instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFET's can be easily achieved.

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated by a HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The capacitance equivalent thickness (CET) of the gate dielectrics was obtained from high frequency (100KHz) capacitance-voltage (C-V)

curve at strong inversion without considering quantum effect.

To understand the content and distribution of the fluorine atoms was measured by secondary ion mass spectroscopy (SIMS), X-ray Photoelectron Spectroscopy (XPS) was used to analyze the Hf-O and Hf-F bondings of the fluorinated HfO_2 thin films.

2.3 Result and Discussions

2.3.1 Effect of the strained device with and without fluorine

Fig. 2.5 shows the SIMS depth profile of the HfO_2/SiON gate dielectric with silicon surface fluorine implantation (SSFI) treatment. SIMS analysis is used to prove fluorine exist in HfO_2/SiON dielectric, further in order to understand fluorine depth profile. The experimental clearly result that fluorine atoms accumulated mainly at the interfacial layer. Therefore, we suggest that after fluorine implantation, the fluorine atoms would accumulate at the surface of the Si substrate, and then distributed into the bulk of HfO_2 thin film after annealing. Besides, these fluorine atoms also terminate the dangling bonds of silicon substrate and accumulate layer region [10]

The X-ray Photon electron Spectroscopy (XPS) analysis of surface and bulk HfO_2 thin films with SSFI treatment samples is shown in Fig. 2.7. XPS analysis is used to prove if fluorine can passivate oxygen vacancy so as to lower high-k bulk

traps due to the formation of Hf-F bonds. In Fig. 2.7, a distinct F 1s peak at 685eV can be observed. The silicon surface fluorine implantation process is obviously introducing fluorine atoms into the HfO_2 dielectric to form the HfOF gate dielectrics.

Fig. 2.6 indicates the Hf *4f* ESCA spectra of the HfO_2/SiON dielectric with and without fluorinated. We can observe that the fluorinated HfO_2/SiON dielectric has higher bonding energy, it proves that fluorine atoms would replace oxygen atoms to bond with hafnium atoms. Since fluorine atoms have the highest electronegativity, the Hf-F bonds could have much stronger bonding than Hf-O bonds. Therefore, Hf-F bonds could effectively immunity against damage.

Figure 2.8 shows the I_D-V_G at small drain voltage (V_{DS}=100mV) transfer characteristic of the control, the CESL and the CESL with SSFI (1E12cm^{-2}) strained HfO_2/SiON nMOSFETs, where the device channel length and width were 0.3 and 10μm, respectively. We can see that the CESL strained device has much higher drain current (I_D) and transconductance (G_m), as well as smaller subthreshold swing (SS). Comparing with conventional SiO_2 passivation layer, the strained without and with fluorinated gate dielectric can increase drain current and peak transconductance more than 100% and 115% , respectively. The subthreshold swing can be also improved from 108mv/dec to 97mv/dec and 96mv/dec to while instead SiO_2 passivation layer by Si_3N_4 capping layer without and with fluorine. The results prove that the CESL

could significantly increase carrier mobility and indicate that has better interface characterization. Previous study [11] on Zr-silicate indicates that electron transport in the channel can be degraded by the coulomb scattering of negative charges in the bulk film, and Fischetti et. al [12] also points out that electron mobility in the inversion layer is affected by remote phonon scattering due to ionic polarization in high-k films. Therefore, the peak transconductance degradation in HfO_2/SiON stack is probably due to charges or traps in the bulk film. On the other hand, fluorine incorporation on the strained device does not degrade transfer characteristic, it still maintain good performance of the strained device. The results suggest that fluorine implantation will not bring bad effect to the strained gate dielectric.

The I_D-V_D output characteristic of the conventional, the CESL and the CESL with SSFI (1E12cm^{-2}) HfO_2/SiON nMOSFETs are compared in Fig. 2.9 where the device channel length and width were 0.3μm and 10μm, respectively. Approximate 39% drain current improvement measured at V_G-V_{Th}=1.5V is obtained for the strained and the strain with fluorinated gate dielectric. The gate voltage has been normalized with respect to threshold voltage to minimize the effect of threshold voltage. And both of them (the strained with and without fluorinated) are not obviously different. The results also clearly suggest that the fluorinated CESL device does not degrade basic characteristic (transfer and output characteristic), it still maintain good performance of

the strained device. On the other hand, it clearly proves that strain process is beneficial to increase effective electron mobility which result in much higher saturation current. Fig. 2.10 displays the gate leakage current versus gate voltage (I_G-V_G) characteristic under inversion (positive sweep) and accumulation (negative sweep) mode. Both the gate leakage current and breakdown voltage can be obviously improved by applying strain with and without fluorine incorporation process, which can be also ascribed to reduced interfacial and bulk trap densities.

The high-frequency (100kHz) C-V characteristic of the control, the CESL strained and the CESL with SSFI HfO_2/SiON nMOSFETs are indicated in Fig 2.11 The extracted capacitance equivalent thickness (CET)is 3.79nm, 3.8nm and 3.77nm for the nMOSFETs with TEOS P.L, nitride P.L and nitride P.L with SSFI treatment, respectively, which were shown in the inset. Thickness of three is similar. It also means that fluorinated CESL device does not degrade basic characteristic. When fluorine concentration is higher than 1E12cm^{-2}, the resultant CET increment faster may be an excess amount of fluorine incorporation into HfO_2 film stacks. This is related to the general theoretical results are the opposite. General theory tells us that implant more fluorine dose before depositing oxide, thickness is less. Otherwise, some researches point out that incorporation fluorine is after depositing oxide, fluorine atom has the highest electronegativity, the implanted fluorine atoms reveal

higher potential to replace the oxygen atoms. Consequently, the Hf-F bonds replace the Hf-O bonds then part of the residual oxygen would diffuse to the interface between HfO_2/SiON stacked and Si substrate and react with the silicon dangling bonds at the interface to growth low dielectric constant interfacial layer[14-17], which results in reduced capacitance and increased CET. Therefore, wet cant not find a rational to explain this result.

The relation between Gm and channel length for all splits of HfO_2/SiON gate stack n-MOSFET is shown in Fig. 2.12. When channel length becomes shorter, the improvement from strain process is more obvious because strain process must be playing in the small size that could exhibit its effect. In short, it was found that all fundamental electrical properties, including drive current, swing, gate leakage current, CET. These could obviously improvement by strain process and fluorine incorporation does not significantly affect these better performances.

2.3.2 Effect of various fluorine dose

Fig. 2.13 shows the I_D-V_G at small drain voltage (V_{DS}=100mV) transfer characteristic of the CESL strained devices with fluorine dose are 1E12cm^{-2}, 1E13 cm^{-2}, 1E14 cm^{-2}, respectively. (where the device channel length and width were 0.3 and 10μm, respectively.) Unexpected, the improvement of the drain current,

transconductance and subthreshold swing do not change for the better with increasing fluorine doses. The subthreshold swing are 96mv/dec (1E12 cm^{-2}), 98mv/dec (1E13 cm^{-2}), 108mv/dec(1E14 cm^{-2}), respectively. We can observe that when fluorine dose is 1E12 cm^{-2}, the improvement effect is the best.

The I_D-V_D output characteristic of the the CESL strained HfO_2/SiON nMOSFETs devices with fluorine dose (1E12cm^{-2}, 1E13cm^{-2}, 1E14cm^{-2}, respectively.) are compared in Fig. 2.14 where the device channel length and width were 0.3μm and 10μm, respectively. The experimental also shows the same result is that as fluorine dose more than 1E12 cm^{-2}, the basic characteristic degrade with increasing fluorine. And Fig. 2.15 displays the gate leakage current versus gate voltage (I_G-V_G) characteristic under inversion and accumulation mode. The result is not obviously different. We surmise that because redundant fluorine ions will band with hydrogen ions, resulting in worse performance. Therefore, the following discussion will not consider SSFI B and SSFI C due to their worse performance.

2.3.3 Current Transport Mechanism

Fig. 2.16 (a) and (b) and (c) show gate current I_G as a function of V_G for the HfO_2/SiON gate stacks with TEOS P.L, SiN P.L and fluorinated SiN P.L ,respectively. They were measured at several different temperatures up to 100℃ in inversion and

accumulation regions. The current is temperature dependent that increases with increasing temperature. This implies that the conduction mechanism of gate current is trap-related, i.e., trap-assisted tunneling (TAT), Frenkel-Poole, etc. Base on the equation of Frenkel-Poole (F-P):

$$I \propto V\exp\left(\frac{2a\sqrt{V}}{T}-\frac{q\varphi_B}{K_BT}\right) \tag{2.1}$$

$$J = B \times E_{ox}\exp\left(\frac{-q\left(\varphi_B-\sqrt{qE_{ox}/\pi\varepsilon_H\varepsilon_0}\right)}{K_BT}\right) \tag{2.2}$$

$$\ln\left(\frac{J}{E_{ox}}\right)=\frac{q\sqrt{q/\pi\varepsilon_H\varepsilon_0}}{K_BT}\sqrt{E_{ox}}-\frac{q\varphi_B}{K_BT} \tag{2.3}$$

Where B is a constant in terms of the trapping density in the HfO_2 film, Ψ_B is the barrier height, E_{ox} is the electric field in HfO_2 film, ε_0 is the free space permittivity, ε_H is the HfO_2 dielectric constant, K_B is Boltzmann constant and T is the temperature measured in Kelvin. Fig. 2.16 (a), (b) and (c) show the F-P plot for the source/drain current in inversion region for the control device and the strained without and with fluorinated, respectively. Fig. 2.17 (a), (b) and (c) show the F-P plot for the substrate current in inversion region for the control device and the strained without and with fluorinated, respectively. These lines are fitting curves for all temperatures. In the high voltage I_{SD} and I_{SUB}, an excellent linearity for each current characteristic can be obtained, indicating that the control device and the strained without and with fluorinated devices exhibit the F-P conduction mechanism for the gate leakage current

in nature.

The barrier height Ψ_B can be calculated from the intercept of y axis and the dielectric constant ε_H of HfO_2/SiON gate stacks can be determined by the slope of the fitting curves according to Equation(2.3). On the other hand, the fitting parameters for the electron and hole barrier heights are 1.07eV and 1.36eV for the TEOS sample. The strained sample are1.2eV and 1.49eV, as compared to1.19eV and 1.5eV for the strained sample with fluorinated. Note that the barrier height for electrons has changed from 1.07eV for TEOS sample to 1.2eV for SiN sample and 1.19eV for strained SSFI sample, and for holes has changed from 1.36eV for TEOS to 1.49eV for SiN sample and 1.5eV for strained SSFI sample. This indicates that the trap position has moved closer to the conduction and valence band of the poly-si gate after strain process. The band diagrams are shown in Fig. 2.19 (a), (b) and (c) for the HfO_2/SiON gate stacks with TEOS P.L, SiN P.L and fluorinated SiN P.L, respectively. Because precursor of SiN sample is NH_3, nitrogen atoms could recover shallow traps. SiN samples with SSFI have fluorine atoms and it could recover shallow traps, similarly. Therefore both of them have deeper trap level than TEOS P.L. We consider the case when the injected carriers flow across HfO_2/SiON by hopping via the trap sites with energy barrier Ψ_B whose value depends on the fabrication process [4].This experimental results indicate that the position of traps level in the strained sample

with and without SSFI can be deeper than the TEOS sample, and the energy barrier Ψ_B for electrons is clearly lower than that for holes about 0.3eV in these samples.

2.4 Summary

In this chapter, a novel CESL strained high-k dielectric with implantation fluorine was presented. We have performed a systematical investigation of electrical characteristics. Significant device performance improvement in strained devices with and without fluorinated were found, such as the excellent subthreshold swing, increased transconductance, higher current drive, improved channel electron mobility, as compared to the control TEOS sample. These results suggest us that optimize fluorine incorporation (1E12cm$^{-2)}$ does not degrade basic electrical characteristic from strained effect. However, too much fluorine ions will degrade performance because of fluorine ions bending with because hydrogen ions.

Finally, the control device and the strained without and with fluorinated devices exhibit the F-P conduction mechanism for the gate leakage current in nature.

2.5 References

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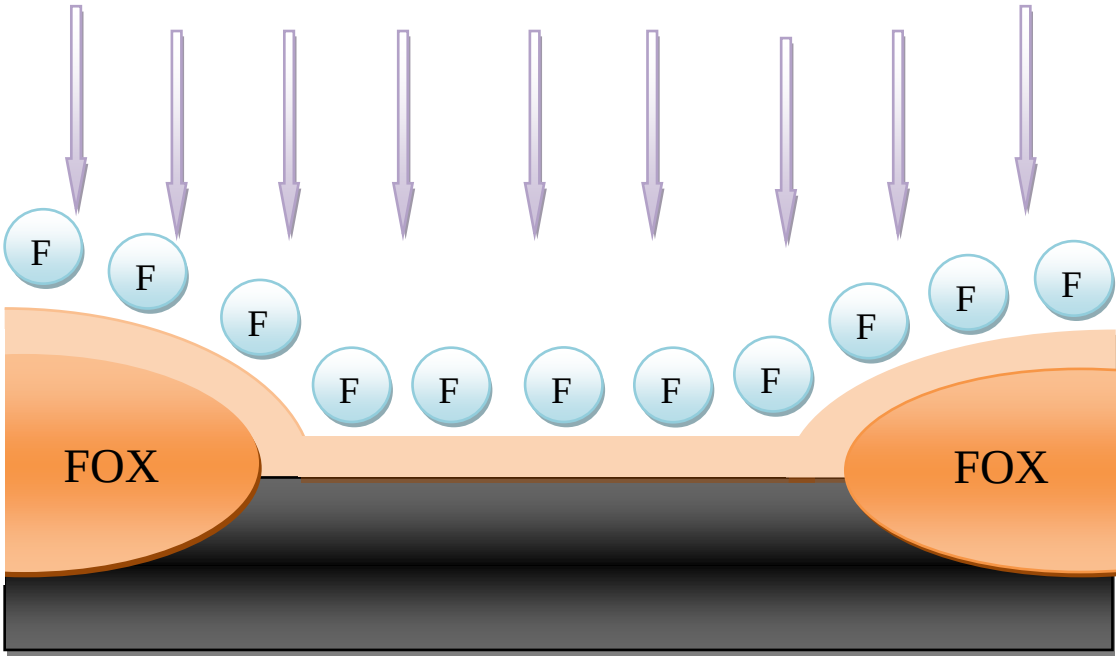


Fig. 2.1 Fluorine incorporation via channel implantation

- Stand LOCOS process
- RCA clean and HF dip. wet pre-cleaning
- SiON target ~1nm：RTA 800℃ 30sec in N_2O ambient
- MOCVD of 30Å HfO_2 (500℃)
- PDA 600℃ 30sec in N_2 ambient
- Poly-Si deposition 200nm and pattering
- Extension S/D implant + Space formation + Deep S/D implant
- Dopant activation ： 950℃ 30sec in N_2 ambient
- Passivation layer by PECVD

  Control ： TEOS 4000Å P.L
- Metallization ：Al-Si-Cu 9000Å
- Forming gas sintering ：400℃ 30min

- Stand LOCOS process
- Fluorine implantation

  Dose：0、1E12、1E13、1E14

  Energy ：10KeV
- RCA clean and HF dip. wet pre-cleaning
- SiON target ~1nm：RTA 800℃ 30sec in N_2O ambient
- MOCVD of 30Å HfO_2 (500℃)
- PDA 600℃ 30sec in N_2 ambient
- Poly-Si deposition 200nm and pattering
- Extension S/D implant + Space formation + Deep S/D implant
- Dopant activation ： 950℃ 30sec in N_2 ambient
- Passivation layer by PECVD

  SiNx 3000Å P.L + TEOS 1000Å P.L
- Metallization ：Al-Si-Cu 9000Å
- Forming gas sintering ：400℃ 30min

Fig. 2.2 The process flow of nMOSFETs with HfO_2/SiON gate stack (a) control (b) strained with and without SSFI

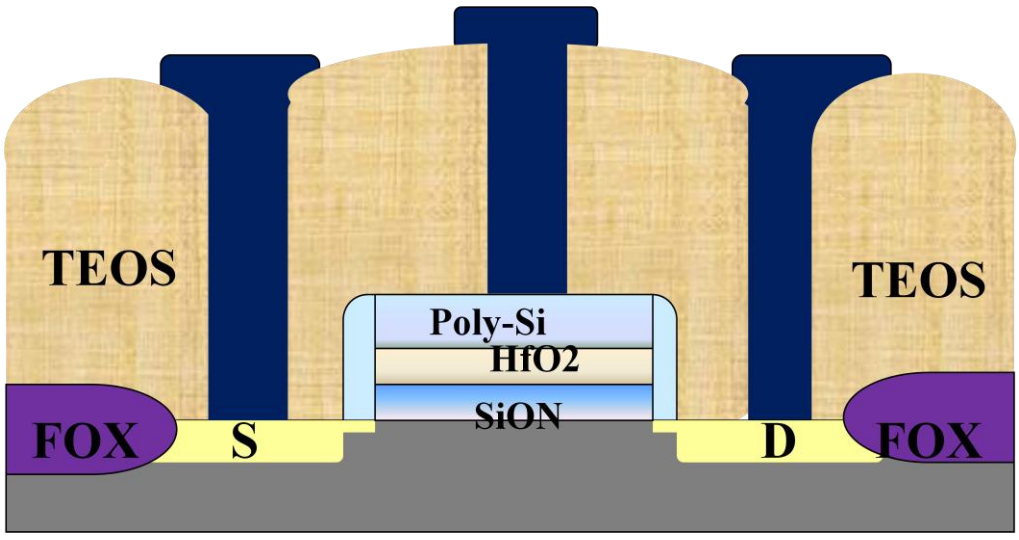


Fig. 2.3(a) Schematic cross section of nMOSFETs with HfO_2/SiON gate stack

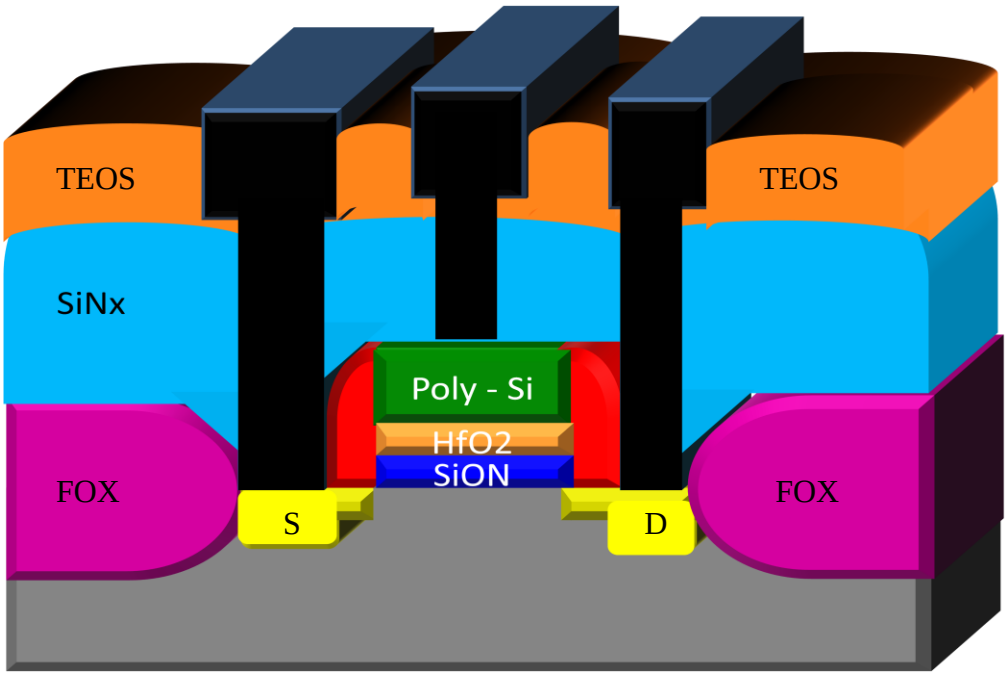


Fig. 2.3(b) Schematic cross section of CESL nMOSFETs with HfO_2/SiON gate stack with and without fluorinated

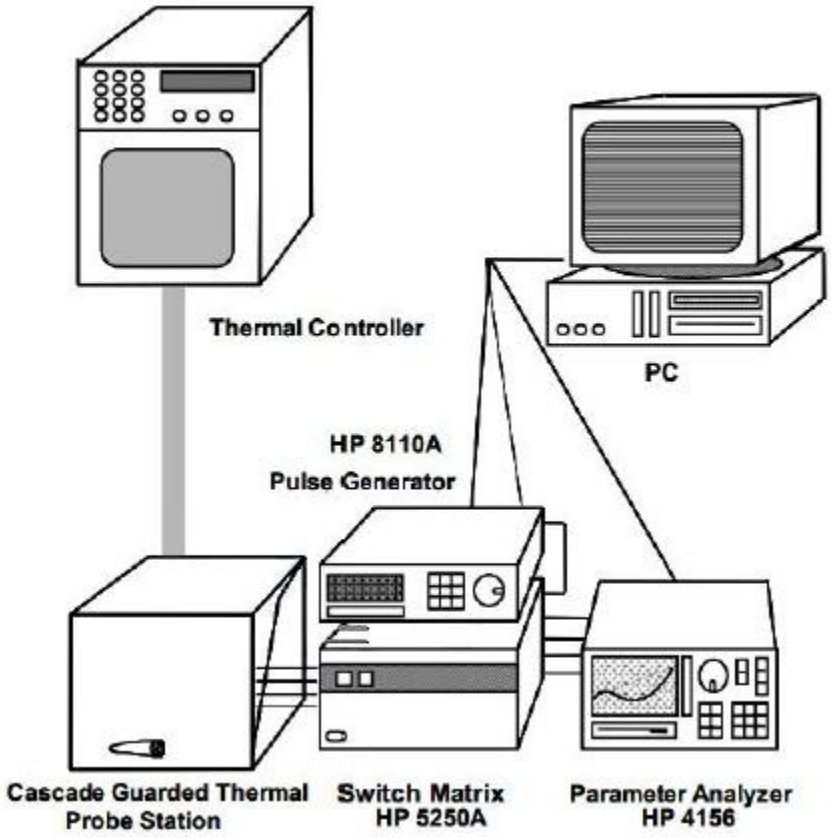


Fig. 2.4 The experimental setup for the basic electrical characteristics and long-term reliability test measurements

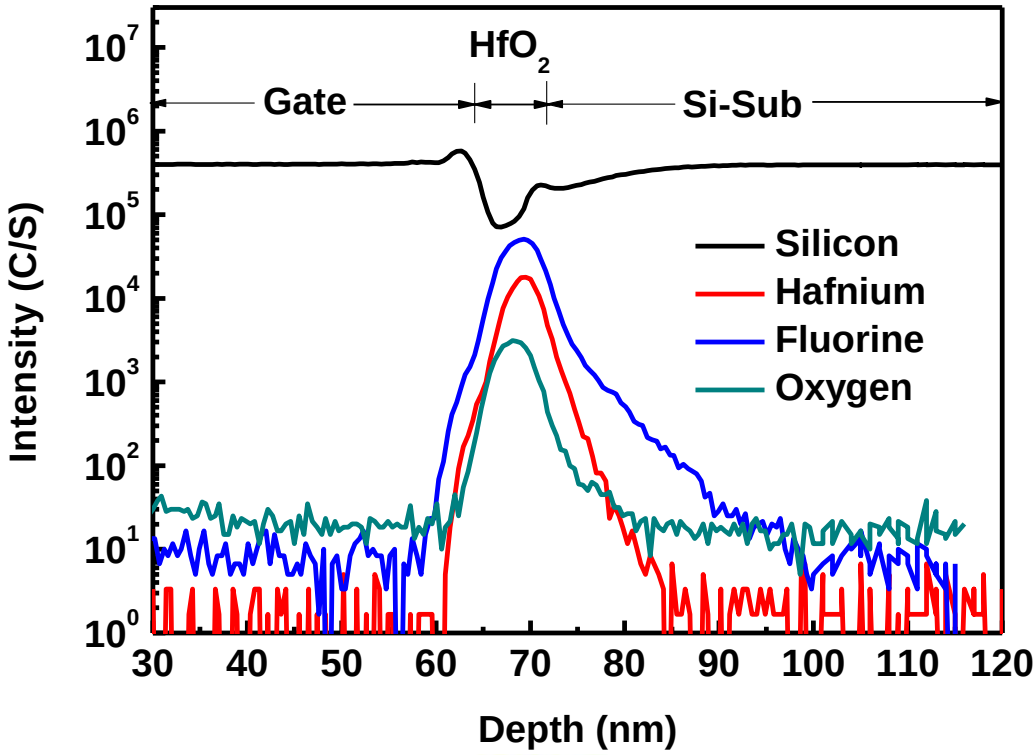


Fig. 2.5 SIMS depth profile of the HfO_2/SiON gate dielectrics. Fluorine atoms accumulated mainly at near the HfO_2/silicon substrate interface after silicon surface fluorine implantation (SSFI).

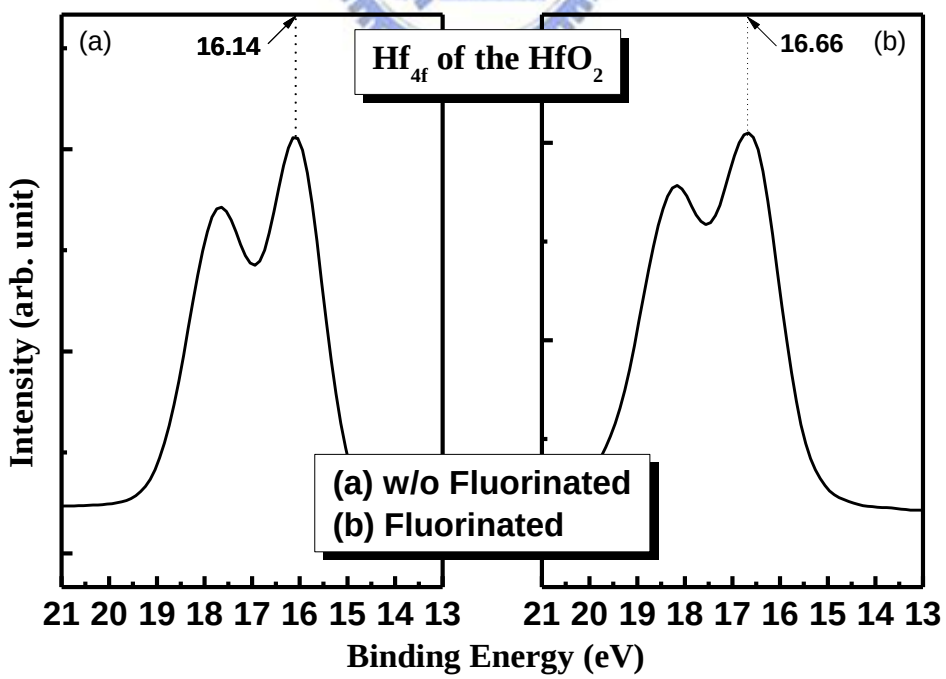


Fig. 2.6 The X-ray Photon electron Spectroscopy (XPS) analysis of the F 1s electronic spectra of SSFT treatment samples

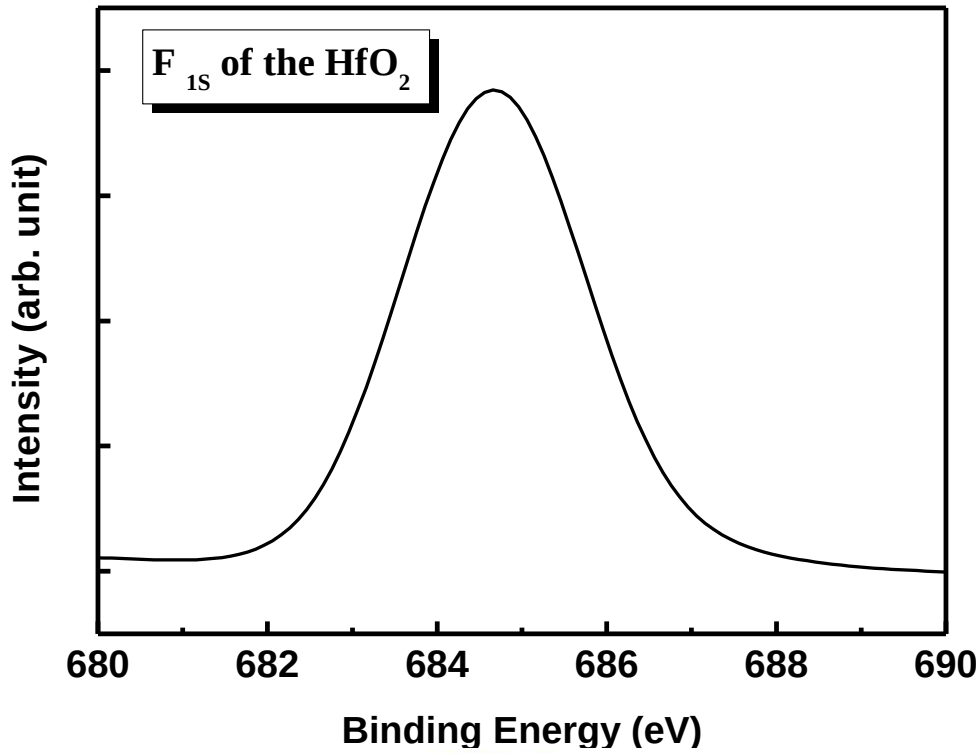


Fig. 2.7 Hf *4f* Electron Spectra Chemical Analysis (ESCA) of (a) without fluorinated and (b) fluorinated, respectively.

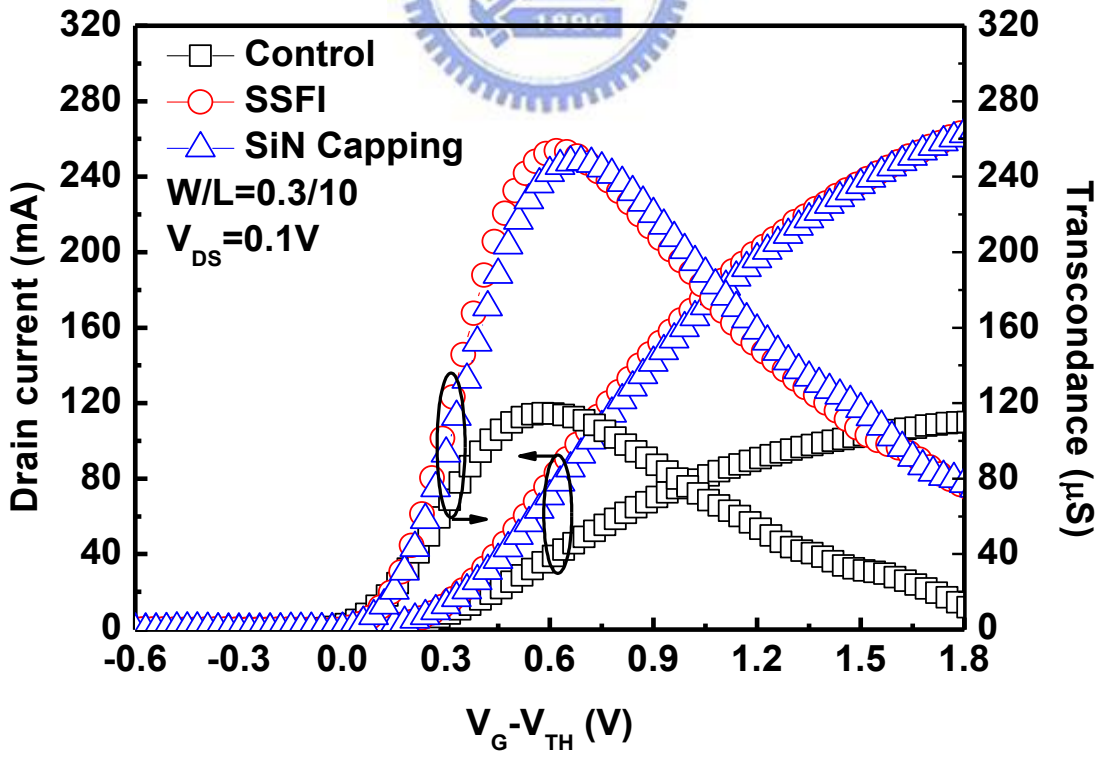


Fig. 2.8 The I_D-V_G and G_m-V_G (normalized V_G) characteristic of the control nMOSFET and the strained nMOSFET with and without fluorine.

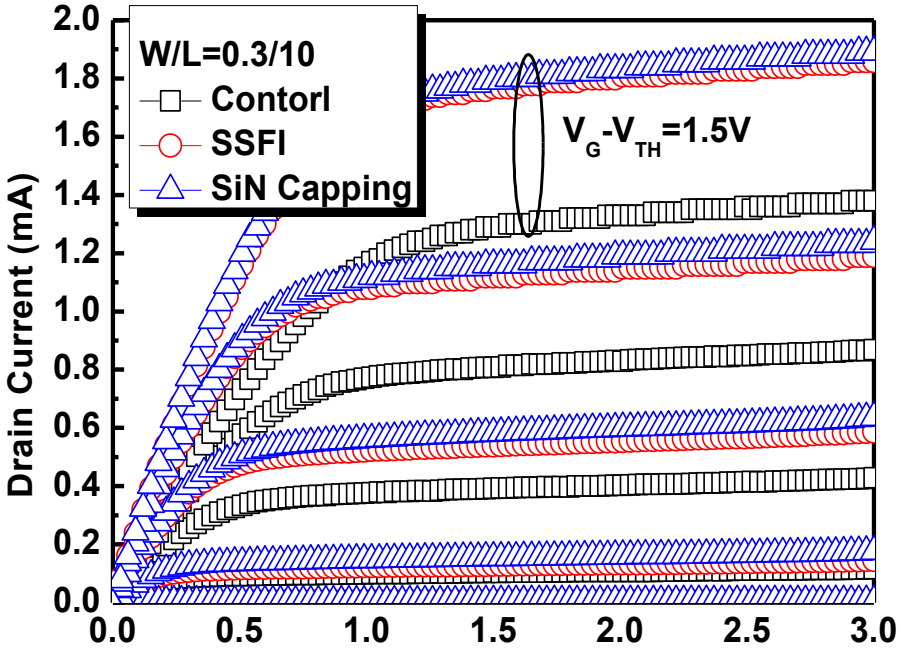


Fig.2.9 The I_D-V_D output characteristic curves of the control nMOSFET and the strained nMOSFET with and without fluorine.

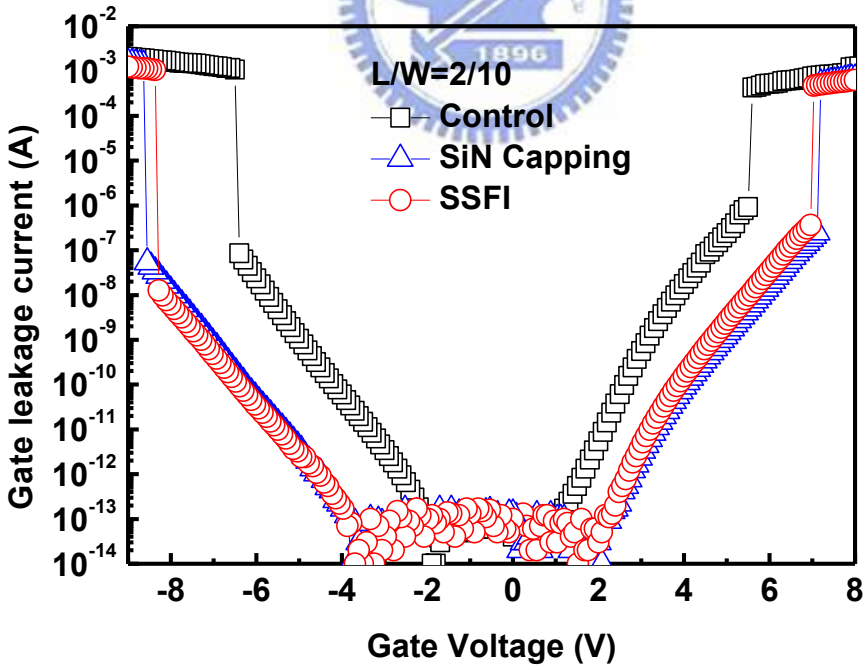


Fig. 2.10 Gate leakage current as a function of gate voltages of the control nMOSFET and the strained nMOSFET with and without fluorine. Both under inversion and accumulation regions.

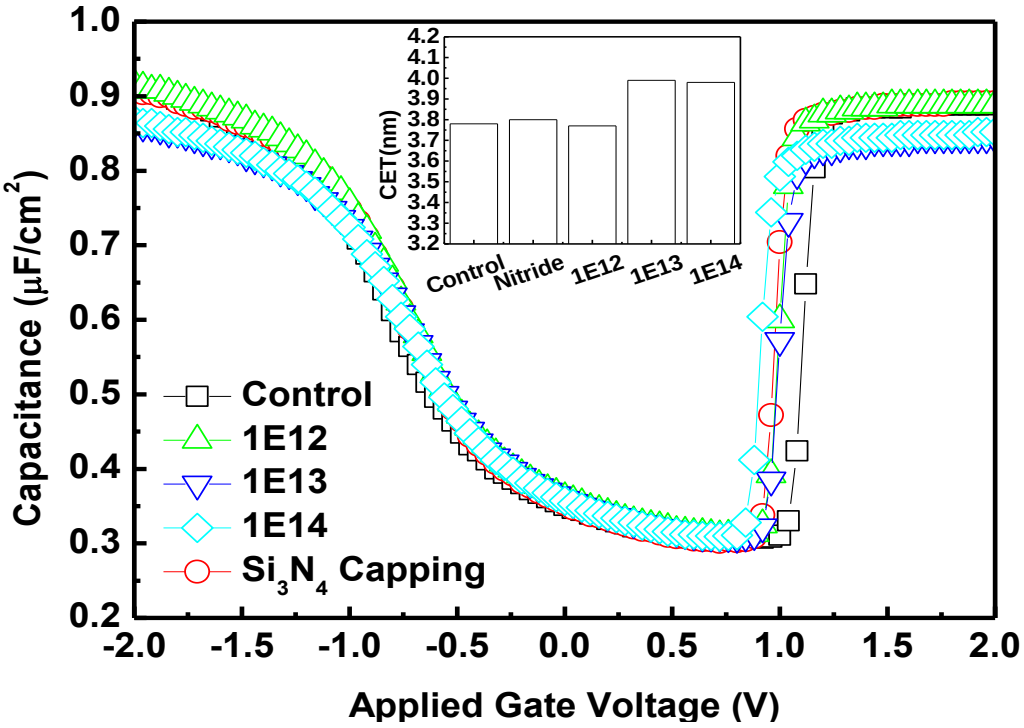


Fig. 2.11 The C-V characteristics of HfO_2 gate dielectrics with various fluorine doses

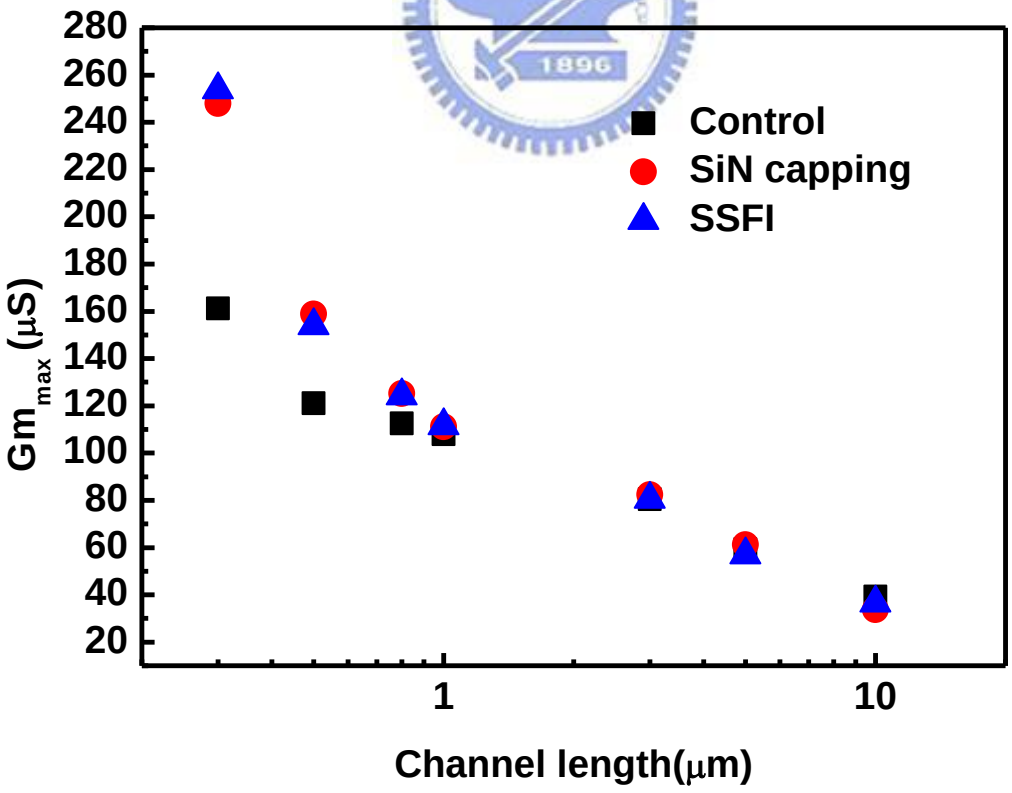


Fig. 2.12 The maximum transconductance versus channel length for all splits of HfO_2/SiON gate stack nMOSFETs.

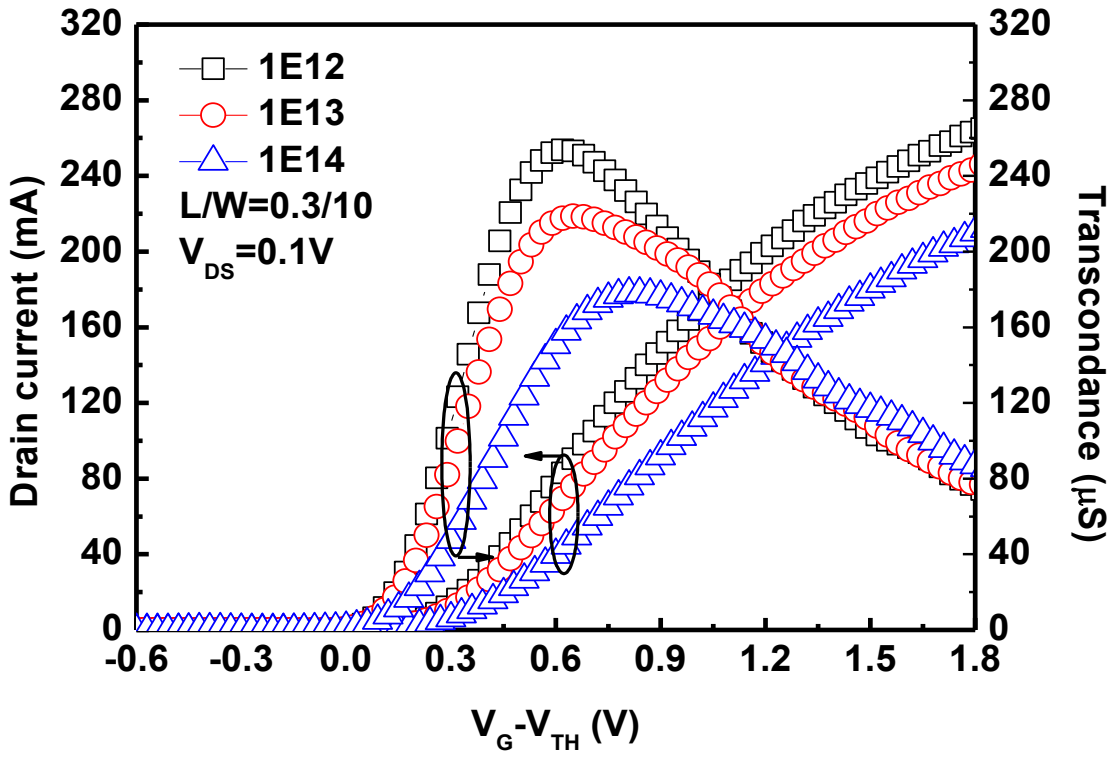


Fig. 2.13 The I_D-V_G transfer and Gm-V_G characteristic of the CESL strained devices with fluorine doses are 1E12cm^{-2}, 1E13cm^{-2}, 1E14cm^{-2}, respectively.

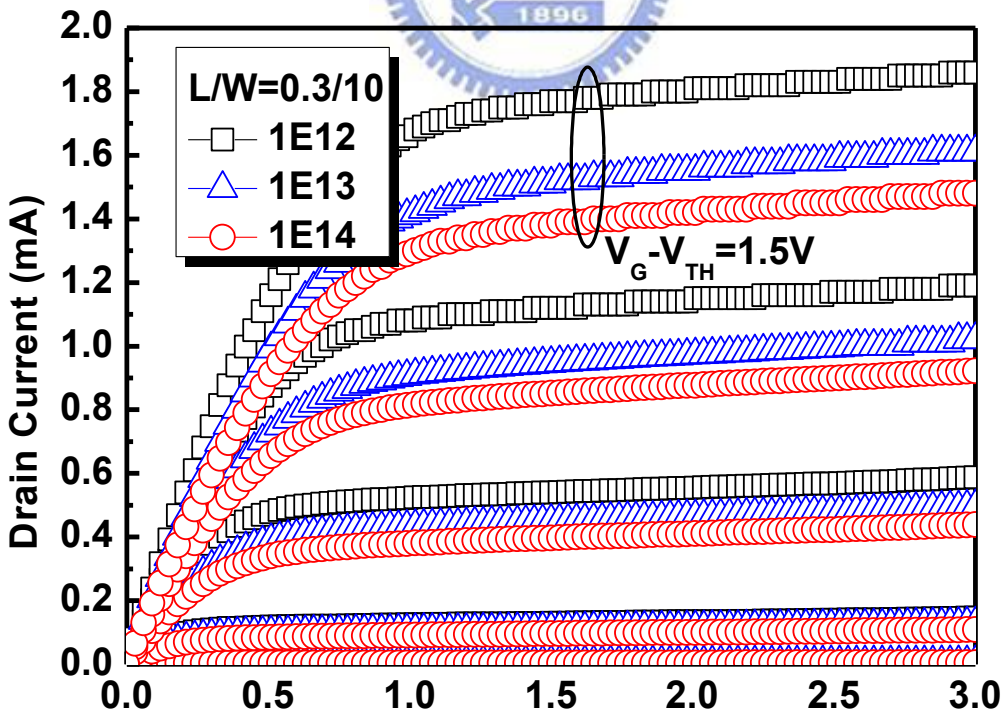


Fig. 2.14 The I_D-V_D output characteristic of the CESL strained devices with fluorine doses are 1E12cm^{-2}, 1E13cm^{-2}, 1E14cm^{-2}, respectively.

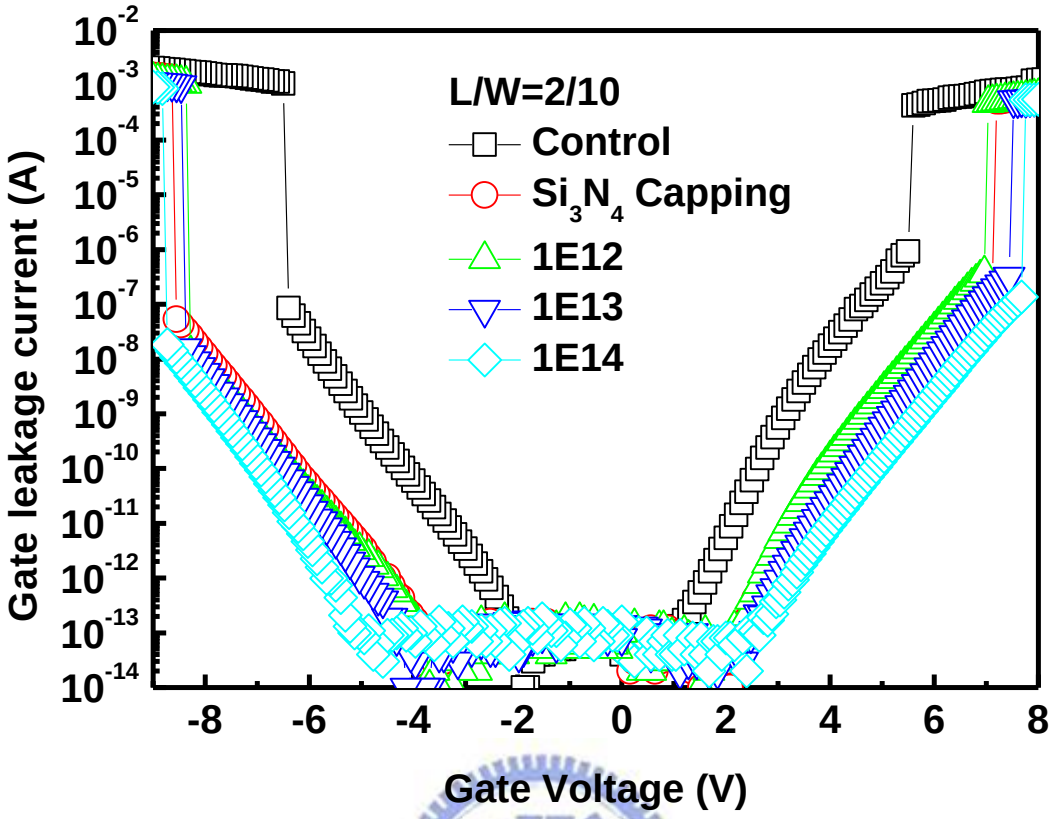
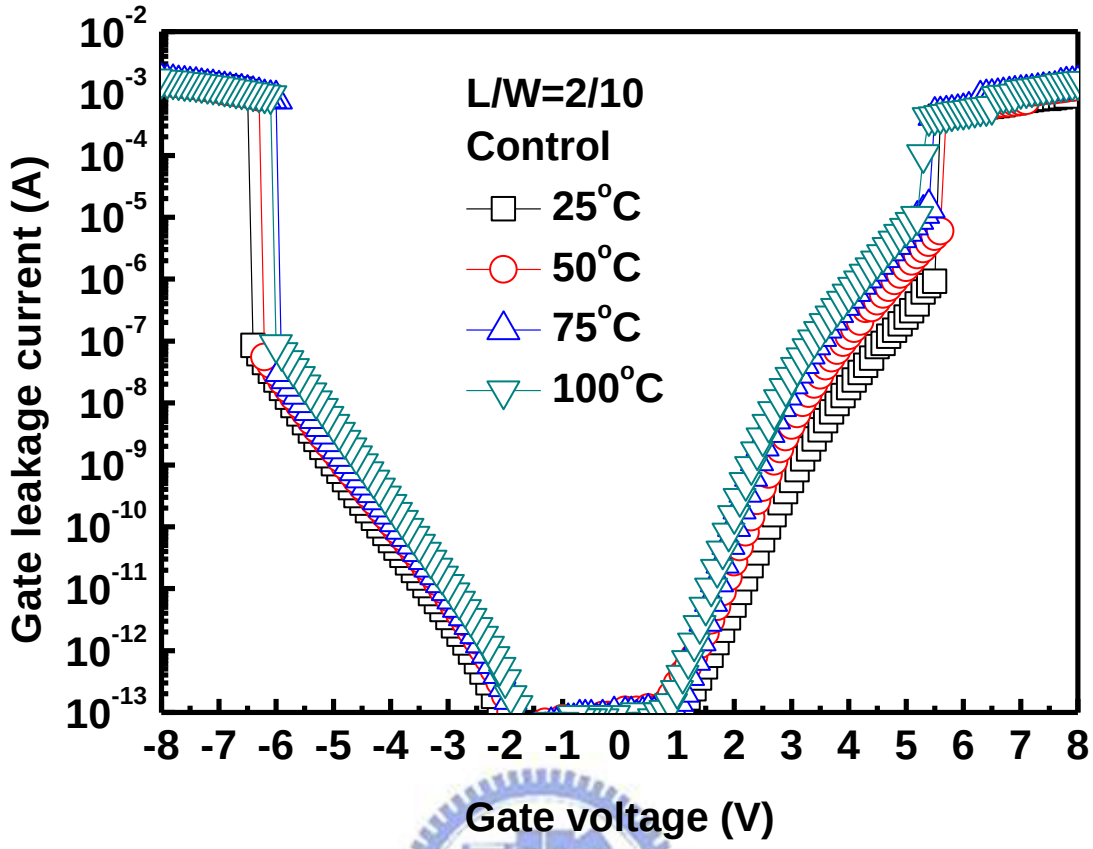
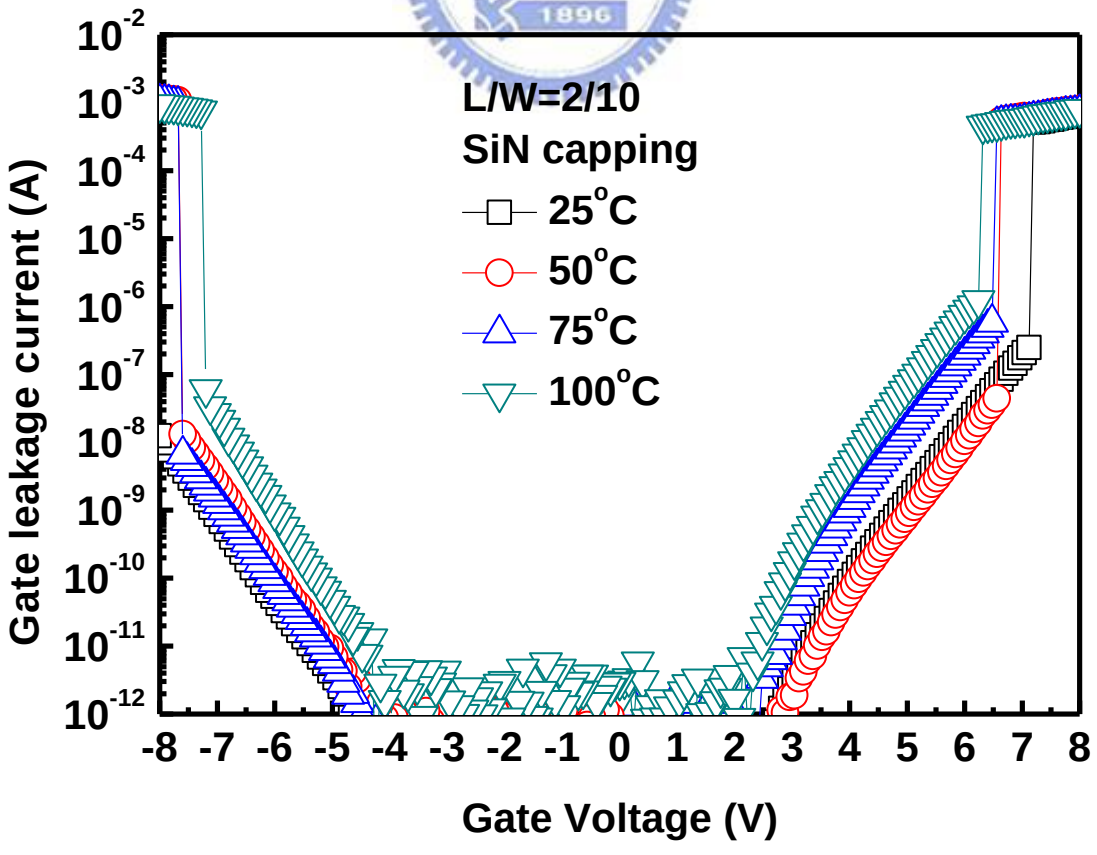


Fig. 2.15 Gate leakage current as a function of gate voltages with various fluorine doses


L/W=2/10
Control
25°C
50°C
75°C
100°C
Gate leakage current (A)
Gate voltage (V)


L/W=2/10
SiN capping
25°C
50°C
75°C
100°C
Gate leakage current (A)
Gate Voltage (V)

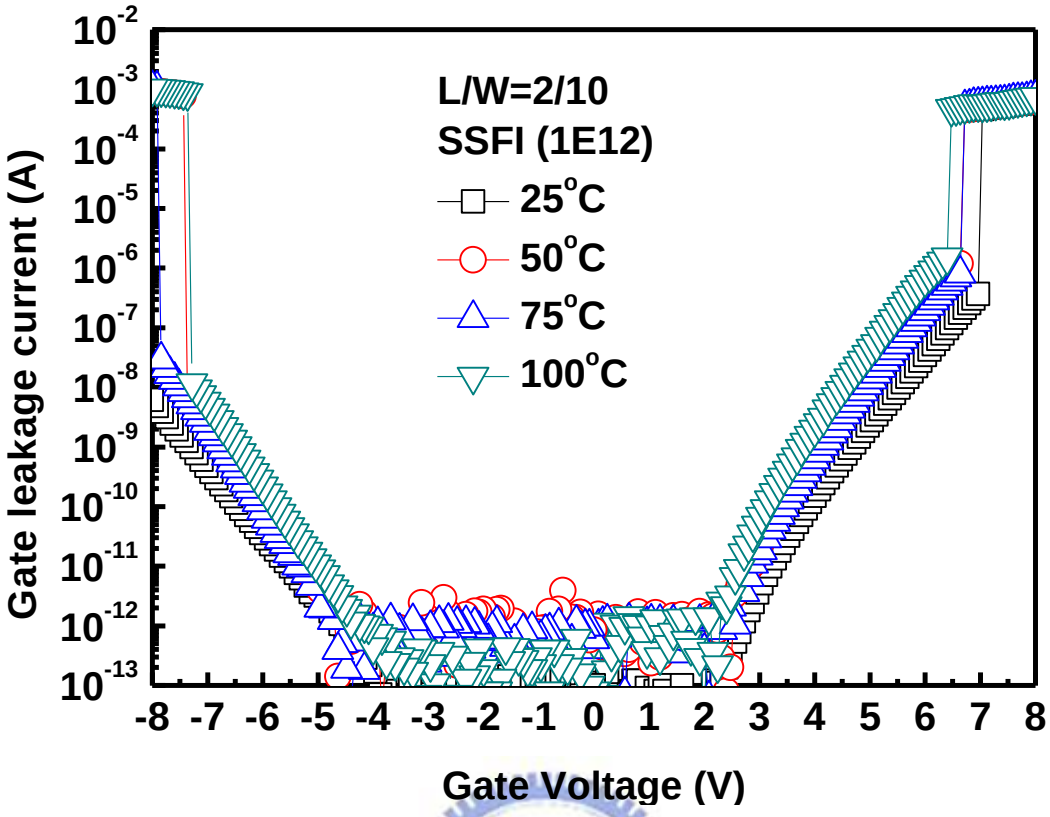
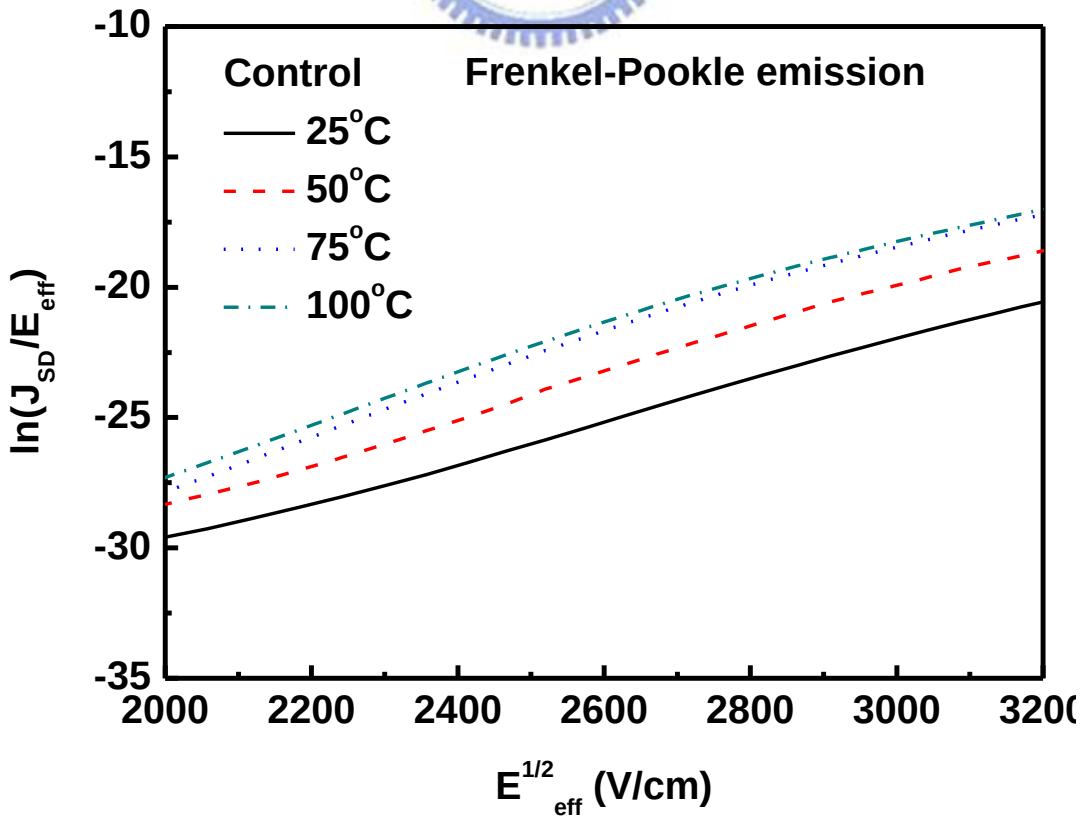


Fig. 2.16 Gate leakage current versus gate bias for fresh n-channel devices at different temperatures (a) TEOS P.L (b) SiN P.L (c) SiN P.L with SSFI



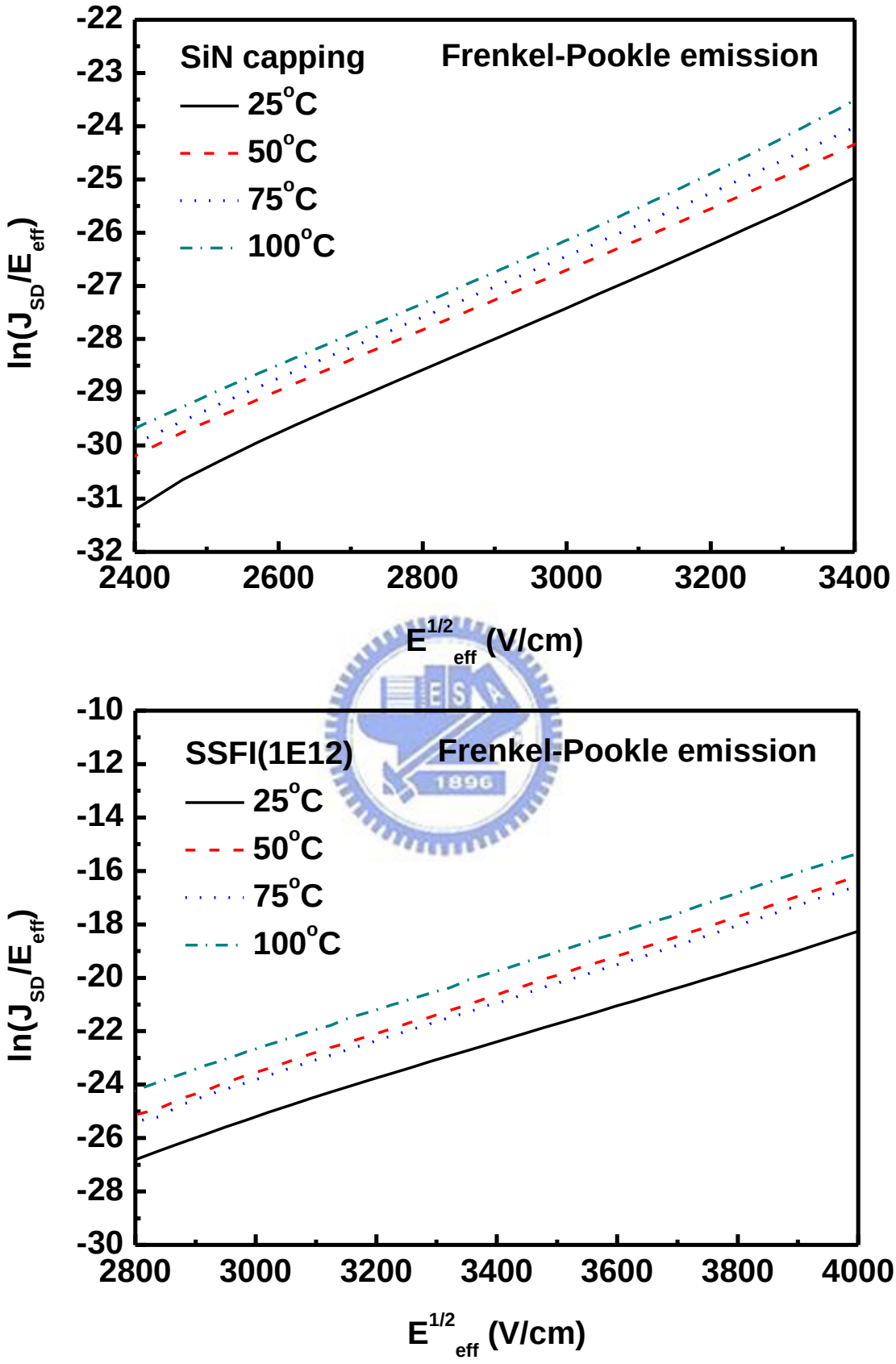
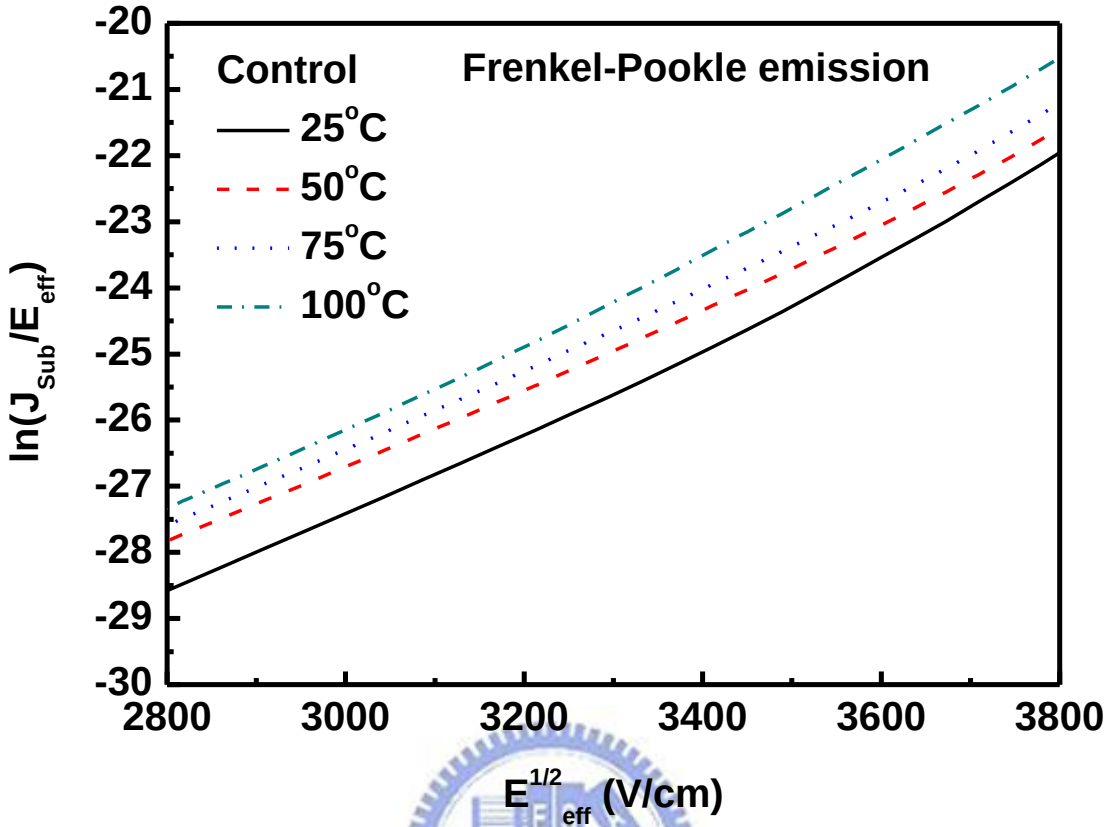
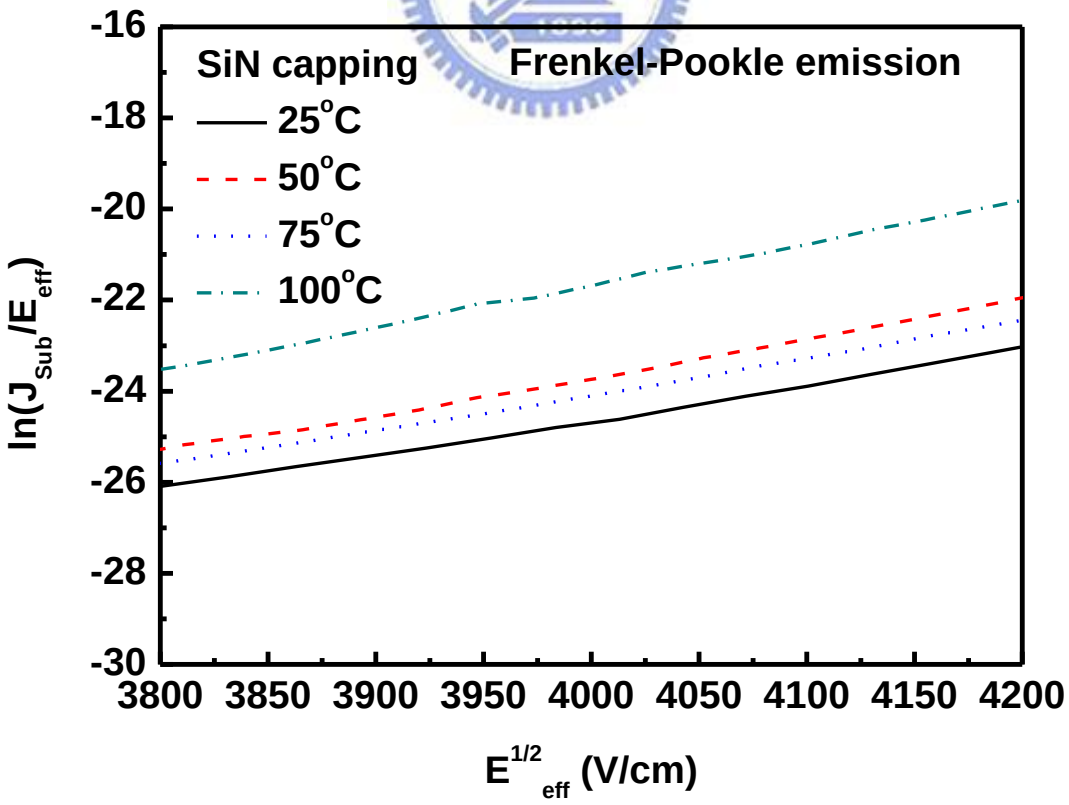


Fig. 2.17 Conduction mechanism for source/drain current fitting under inversion region (a) TEOS P.L (b) SiN P.L (c) SiN P.L with SSFI


Control
Frenkel-Pookle emission
25°C
50°C
75°C
100°C
ln(J_Sub/E_eff)
-20
-21
-22
-23
-24
-25
-26
-27
-28
-29
-30
2800
3000
3200
3400
3600
3800
E^1/2 eff (V/cm)


SiN capping
Frenkel-Pookle emission
25°C
50°C
75°C
100°C
ln(J_Sub/E_eff)
-16
-18
-20
-22
-24
-26
-28
-30
3800
3850
3900
3950
4000
4050
4100
4150
4200
E^1/2 eff (V/cm)

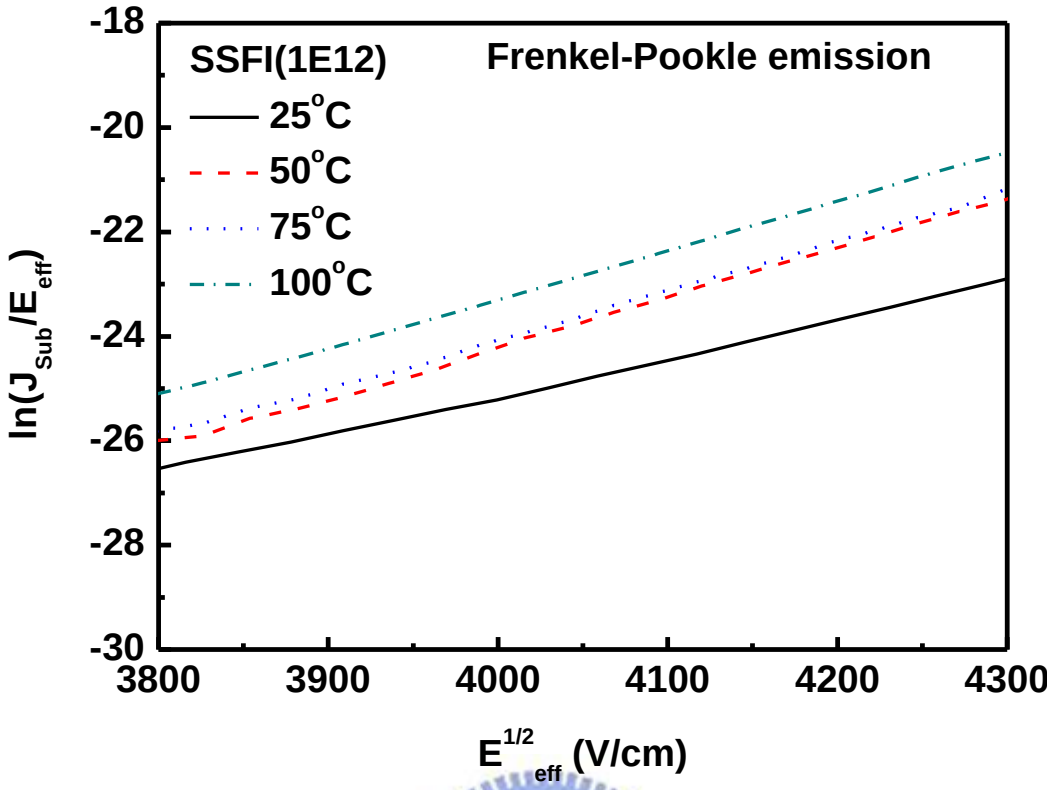
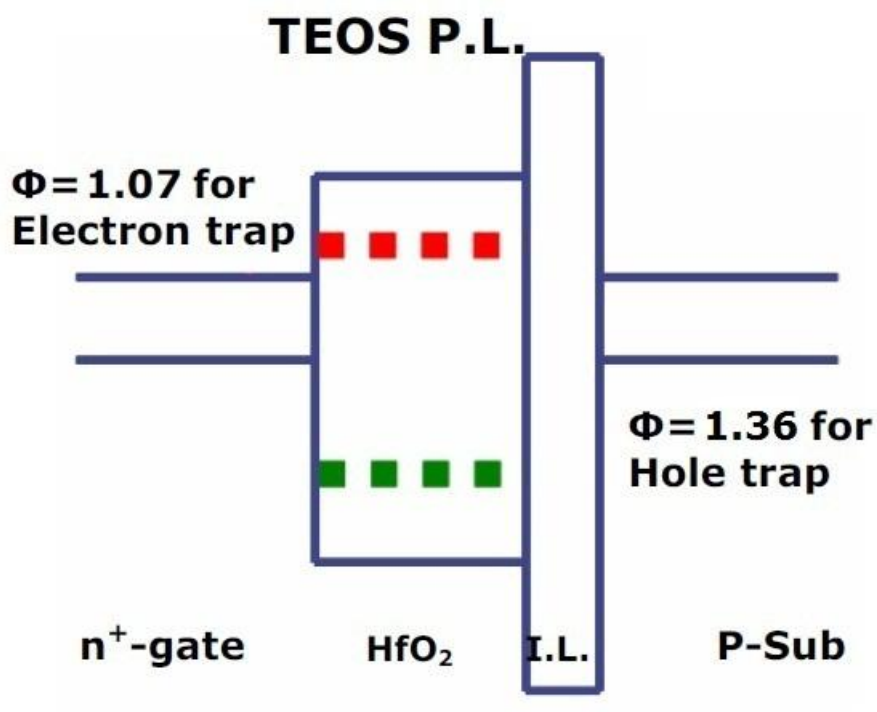
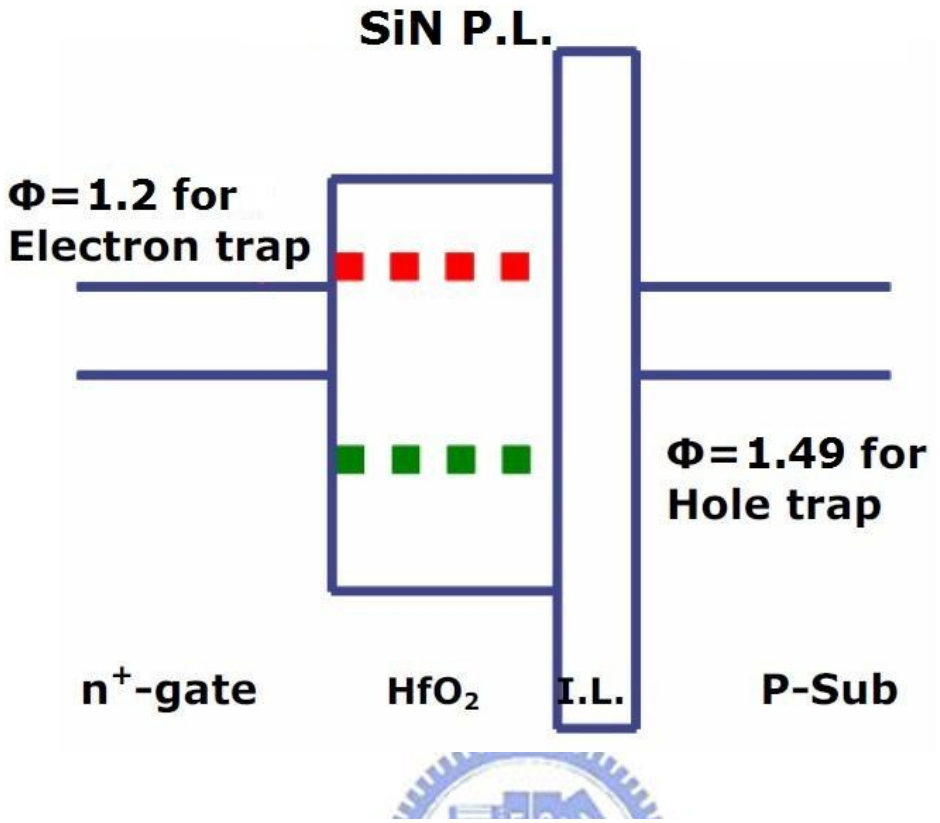


Fig. 2.18 Conduction mechanism for substrate current fitting under inversion region

(a) TEOS P.L (b) SiN P.L (c) SiN P.L with SSFI





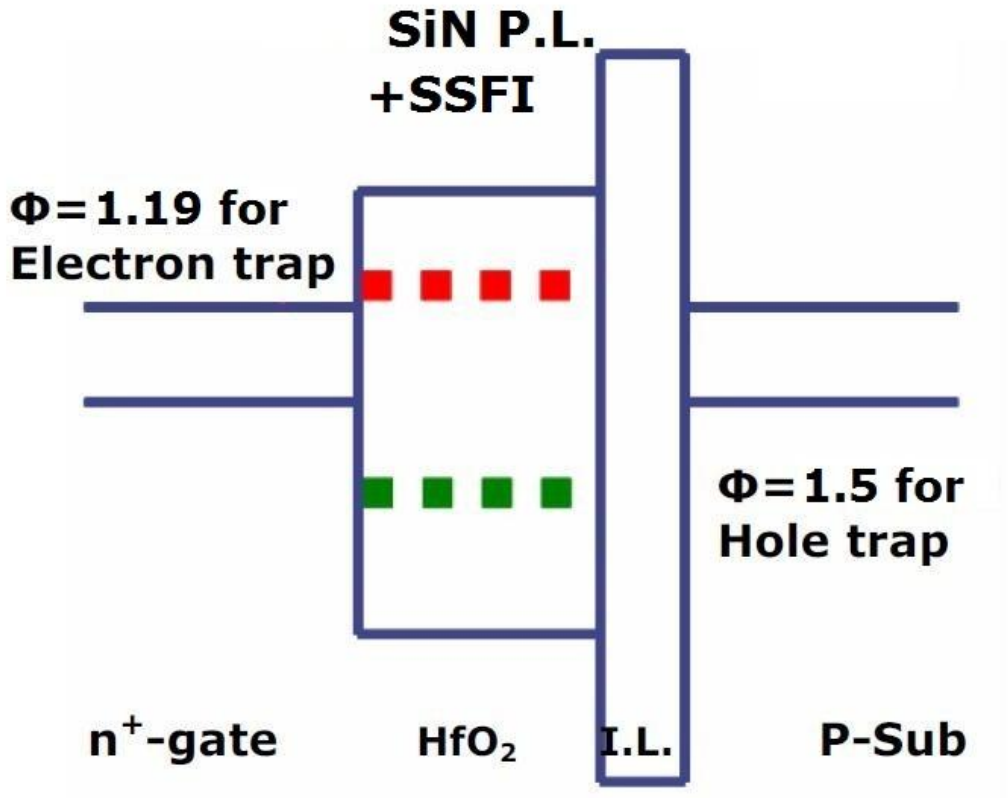


Fig. 2.19 Band diagrams for (a) TEOS P.L (b) SiN P.L (c) SiN P.L with SSFI illustrating the conduction mechanism of Frenkel-Poole emission.

CHAPTER 3

Reliability Issues of Fluorine Incorporation on the CESL strained HfO_2/SiON gate dielectric

3.1 Reliability Review

Reliability characteristics of the Hf-based dielectric such as hot carrier induced degradation (HCI), time dependent dielectric breakdown (TDDB), bias temperature instability (BTI) have been widely investigated with expected application of these materials in the high-k gate stack [1-5]. Threshold voltage (V_{TH}) instability induced by charge trapping has been considered as one of the critical reliability issues in Hf-based high-k gate dielectrics, especially for the n-MOSFETs under substrate electron injection conditions (positive bias stress). On the other hand, V_{TH} degradation of n-MOSFET PBTI was primarily caused by charge trapping in bulk high-k rather than interfacial degradation [6]. Since the threshold voltage is directly related to the n-MOSFET's on-off characteristics and eventually determines its output power supply voltage for its own purpose.

Hot carrier reliability is one of the major limitations for the implementation of the high-k gate dielectrics. We should consider the concurrent charging of the gate dielectric by the cold channel carriers injected into the dielectric when investigating hot carrier effects on high-k gate dielectrics [7-9]. The cause comes from both hot

carriers near the drain region of the channel and cold carriers (channel electrons) which would be injected and trapped in the high-k layer during HCS condition.

On the other hand, one of main issues for high-k gate stack is the charge trapping characteristics during reliability test, a threshold voltage instability associated with electron trapping/de-trapping in high-k layer [10-15] can significantly affect the transistor parameters and complicate the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate stacks. It is typically not an issue in the case of SiO_2 dielectrics because the reversible electron trapping is less prevalent in SiO_2 and could not significantly affect transistor parameters [16-17]. We can evaluate additional electron trapping effects on top of defect generation by a de-trapping step which has been proposed for studying generation of the electron trapping process and its impact on high-k device reliability [13-14]. As a result, in the Hf-based high-k gate dielectrics, these reversible charge trapping and de-trapping behaviors are highly related to the stress history of previously trapped charge carriers, implying these high-k traps are pre-existing bulk traps [18-19]. For further understanding as mentioned above, we will investigate trapping dynamics of carrier in HfO_2 high-k dielectric n-MOSFETs.

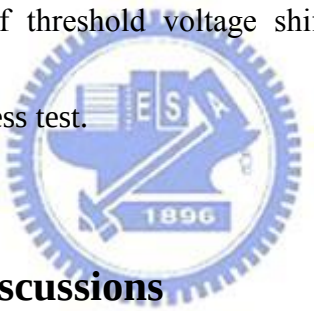
In this chapter, we investigate the characteristics of threshold voltage (V_{TH}) shift during CVS and HCS to find a way to differentiate the contribution of cold carrier

trapping and hot carrier injection.

3.2 Reliability Impact of Fluorine Incorporation on CVS

3.2.1 CVS Measurement Setup

In constant voltage stress (CVS) reliability measurements, devices were stressed with the gate voltage set at a higher positive voltage, and the source/drain/substrate are ground. To monitor the degradation, both the I_D-V_{GS} characteristics at V_{DS} = 100 mV (linear region) was measured before and after the stress. As shown in Fig. 3.1. The degradations in terms of threshold voltage shift (ΔV_{TH}) was examined and recorded in the accelerated stress test.



3.2.2 Result and Discussions

First of all, we focus on reliability characteristics of HfO_2/SiON gate stack nMOSFETs with fluorinated CESL compared to without fluorinated CESL and without CESL under constant voltage stress (CVS) condition. Fig. 3.2 shows the threshold voltage variations as a function of stress time for the fluorinated CESL device, CESL device and control TEOS devices of nMOSFETs, respectively. The given normalized stress was V_G-V_{TH}=3.0V at room temperature. In order to exclude the difference of in the threshold voltage between samples, normalized positive stress voltage of the gate terminal was used. It shows that the threshold voltage shift of the

control devices is the most serious and V_{th} shift of CESL is less than the former. As previous metioned, precursor of SiN sample is NH_3, nitrogen atoms could passivate bulk traps. The fluorinated CESL device shows the best reduced V_{th} degradation compared to the both devices because effect of fluorine passivation is better than nitrogen passivation. The high-k bulk traps (N_B) are an important factor of stress-induced degradation. To prove this degradation, the normalized gate current density during Fowler-Nordheim (FN) stress at V_{GS}=4V is plotted versus stress time for all splits shown in Fig. 3.3. As observed, the normalized gate leakage current density decreases with stress time for these samples, whereas the control devices shows a higher rate of J_g decrease than the strained devices with and without fluorinatrd. And the strained devices with SSFI have the least reduction. It is consistent of previous experimental. This result indicates that there are more high-k defect traps in the high-k bulk of the control devices, causing a higher number of electrons trapped and the strained device followed. Therefore, fluorine incorporation could significantly decrease oxide bulk traps.

3.3 Reliability Impact of Fluorine Incorporation on HCS

3.3.1 HCS Measurement Setup

In hot carrier stress (HCS) reliability measurements, devices were stressed with

the drain voltage set at a highly positive voltage, and the gate terminal was biased at the voltage where maximum absolute value of I_{SUB} occurred to accelerate the degradation. To find the condition, we first measured the I_{SUB}-V_{GS} characteristics with drain terminal biased at a given voltage. To monitor the hot electron degradation, both the I_D-V_{GS} characteristics at V_{DS} = 100 mV (linear region) was measured before and after the stress. As shown in Fig. 3.4. The degradations in terms of threshold voltage shift (ΔV_{TH}), was examined and recorded in the accelerated stress test.

3.3.2 Result and Discussions

Substrate current is an important factor to determine how much hot carriers are generated and injected during hot carrier stress. A hot carrier with sufficient energy can create more charge carriers through impact ionization. For n-MOSFET devices, holes generated by impact ionization are collected into the substrate. The substrate current (I_{SUB}) versus gate voltage (V_G) for these samples of devices at V_{DS} =3V is illustrated in Fig. 3.5. From the figure, it clearly exhibits that the fluorinated and the CESL device has larger substrate current than the control TEOS device. Because strain effect can enhance mobility and election velocity, resulting increase accelerated electron energy, they can get more hot holes. When testing hot carrier stress, the control device should have less degradation than the others. The threshold voltage shift increase as a function of stress time for these samples is shown in Fig. 3.6, after

receiving a hot-carrier stress at V_{GS} at the maximum value of substrate current. As expected, the control sample has the least V_{TH} shift among these samples. The fluorinated CESL samples have less threshold voltage shift than the strained samples but both samples have similar substrate current. It means that although the CESL strained with and without fluorinated generate similar amount of hot-carriers, the fluorinated samples can significantly reduce V_{TH} shift. It indicates that the CESL device is relatively easy to be damaged by hot carrier stress. The result suggests that this phenomenon is closely related to the incorporation of fluorine atoms forming stronger Si–F bonds near the source and drain sides instead of weaker Si–H and Si–Si bonds to enhance the interface hardness between HfO_2/SiON and silicon as well as the immunity against hot-carrier stress due to the inhibition of the channel avalanche multiplication of hot carriers. This mechanism could be expressed in Fig. 3.7

3.4 The Characteristics of Charge De-trapping

The threshold voltage was shifted to positive direction due to negative charges built up within the HfO_2 shown in Fig. 3.2.As shown in Fig. 3.8 shows the threshold voltage shift of the HfO_2/SiON gate stack nMOSFETs with fluorinated CESL, the CESL device and the control device as a function of the static stress/relaxation time with a fixed stress voltage V_G-V_{TH}=2V and relaxation voltage V_G=-2V. Basically, the

relaxation voltage plays a significant role to clean up the trapped charge carriers before the next stress cycle. It was also indicated that a charge de-trapping behavior can not cause an additional V_{TH} instability because the threshold voltage was still shifted above the initial V_{TH} for these samples. After relaxation, a subsequent stress-induced V_{TH} increase follows the initial pre-relaxation stress time dependence. It is clear that this relaxation does not fully recover the V_{TH} shift caused by the positive bias stress. The residual V_{TH} shift appears to be determined by the balance between the built-in potential due to trapped charges and the barrier height for de-trapping [20].

Based on the observations above, a model explaining V_{TH} instability behavior during the stress and relaxation can be proposed as shown in Fig. 3.8. There are two factors to shift V_{TH} during the stress. One is electrons filling the existing traps and the other is the charged damages created during the stress. Portion of the former electrons was de-trapped spontaneously to reduce the instant built-in potential after the stress was removed. However there are still some amount of trapped electrons and charged damage remaining. We can observe that a lot of trapped electron is significant to be instantly pulled out from the pre-existing traps and the created traps are also obviously decreased for the SSFI devices during de-trapping bias, resulting in a few of the residual electrons

This result could explain for two portions. For stress behavior, there are two factors to shift V_{TH} during the stress. One is electrons filling the pre-existing traps and the other is the charged damages created traps during the stress. The fluorinated device defect level is the deepest and Hf-F bonding is the stronger than others, so electron filling the pre-existing traps and created traps which charge damage could be the least, respectively. Therefore, the fluorinated device is the least shift. Although the CESL device defect level is similar to the fluorinated, its oxide has much more Hf-H bonds, resulting in more created traps in stress time. For relaxation behavior, detrapping electrons number of the fluorinated and strained is much less. Because their defect level is deeper, trapped electron should not be easily escape from pre-existing traps. It was associated with the good correlation of the barrier height between de-trapping behavior and F-P emission results for both samples.

3.5 Summary

In this chapter, a novel strained CMOS with fluorine incorporation into high-k technology and reliability characteristics has been successfully demonstrated. We observe that serious degradation such as interface state, bulk trap density and threshold voltage shift occurs in the CESL strained devices. The silicon surface fluorine implant (SSFI) improved reliability characteristics under CVS and HCS. It is

believed that the HCS and CVS degradation are related to the electron traps in gate dielectrics. CVS was found to be mainly caused by bulk trapped generation rather than the generation of interface trapped charge. The degradation of HCS occurs at V_{GS} at the maximum value of substrate current stress condition. The hot carrier contribution induces permanent damage while cold carrier contribution is shown to be reversible.

The time-to-breakdown (T_{BD}) characteristic of the nMOSETs with TEOS P.L, SiN P.L and fluorinated SiN P.L are shown in Fig. 3.9. The operating voltage extrapolated to ten year lifetime for the device with TEOS P.L, SiN P.L and fluorinated SiN P.L are 3.1V, 5.1V and 5.3V, respectively. And Fig. 3.10 indicates that on current degradation. The fluorinated device still has the least degradation (18%). Apparent time-to-breakdown lifetime improvement can also attribute to the stronger Hf-F and Si-F bonds formation, instead of the weaker interface dangling bonds and oxygen vacancies (Fig. 3.11).

3.6 References

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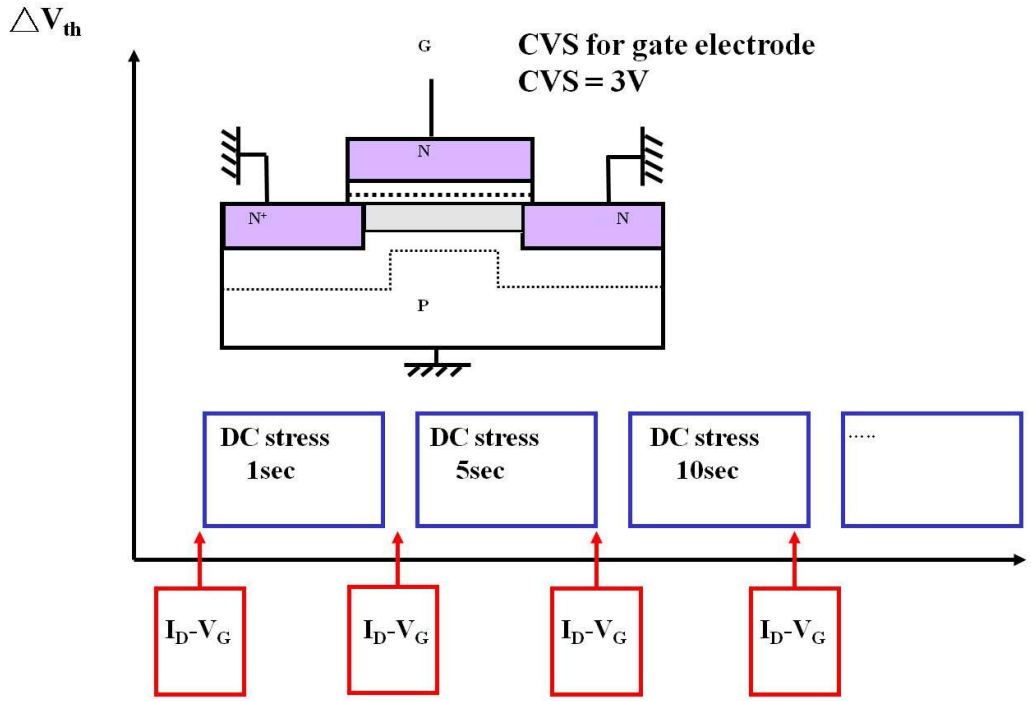

Fig. 3.1 Schematic of measurement setup for CVS measurement

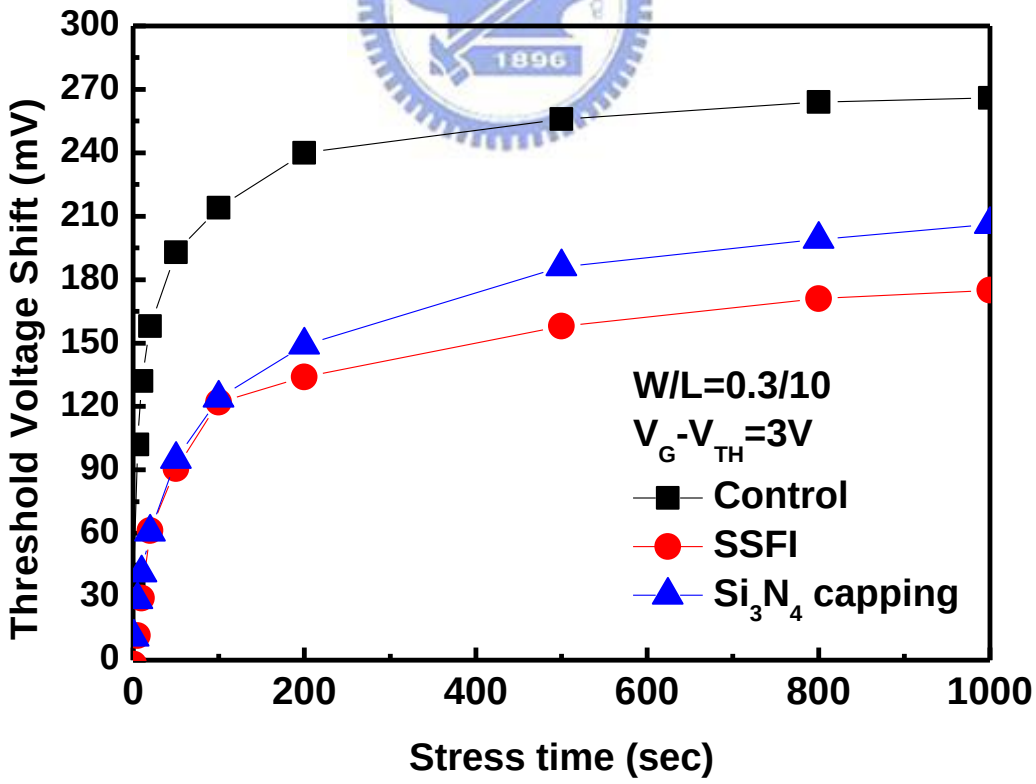

Fig. 3.2 CVS-stress-time dependence of ΔVth for Control, SiN capping and SiN capping with SSFI at 25℃.

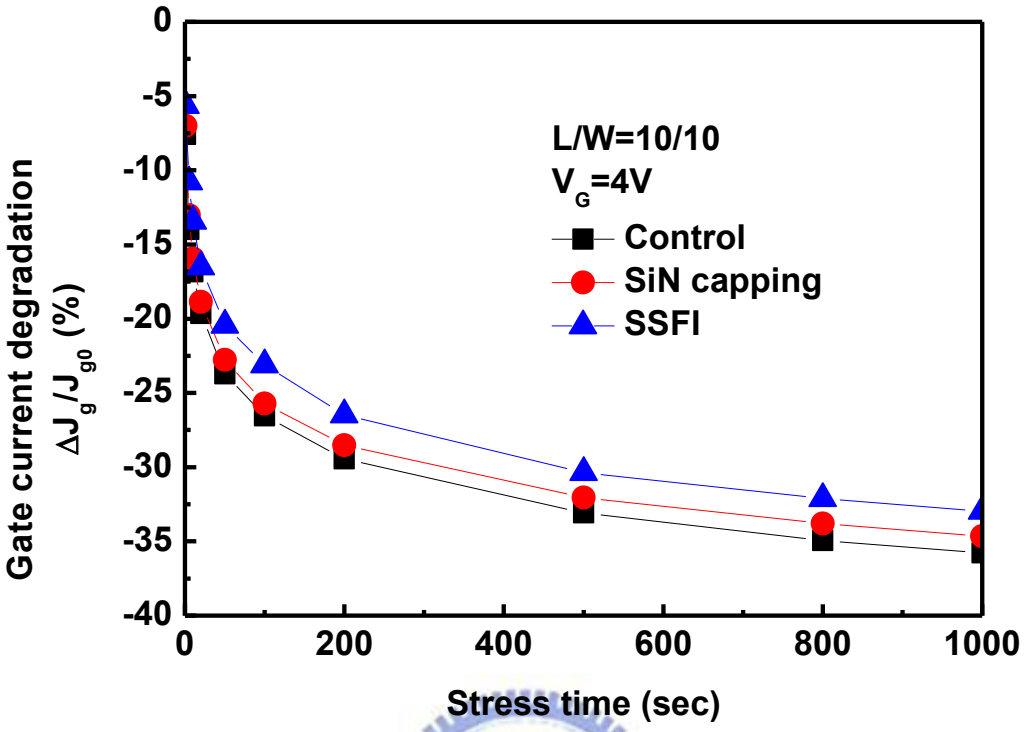

Fig. 3.3 The normalized gate current density ((Jg-Jg0)/Jg0) at a constant gate voltage of 4.0V versus stress time of all splits.

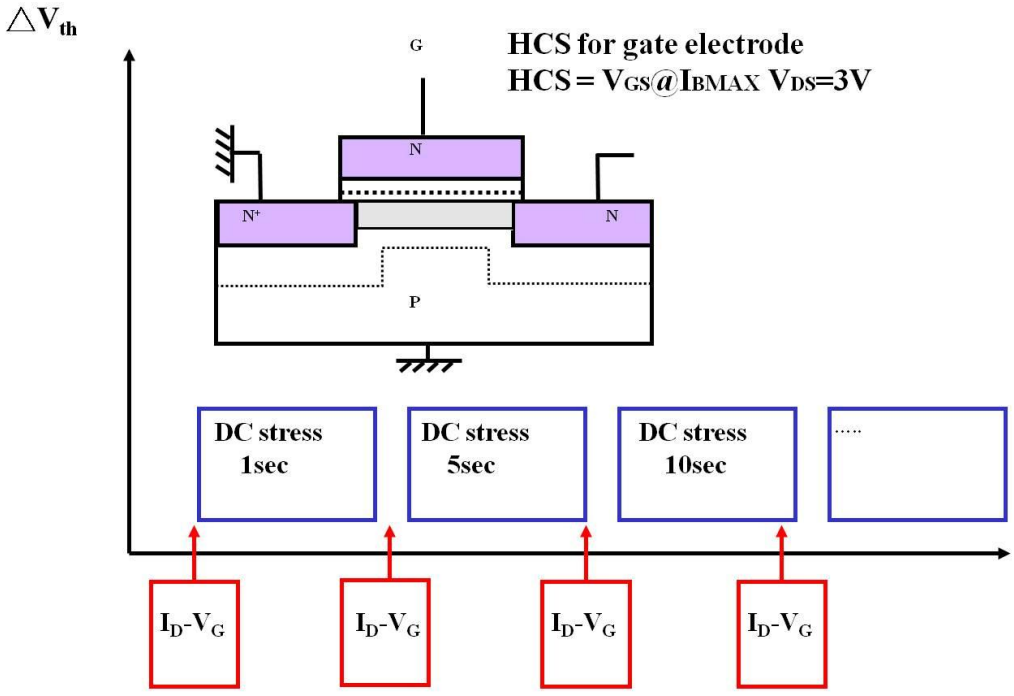

Fig. 3.4 Schematic of measurement setup for HCS measurement

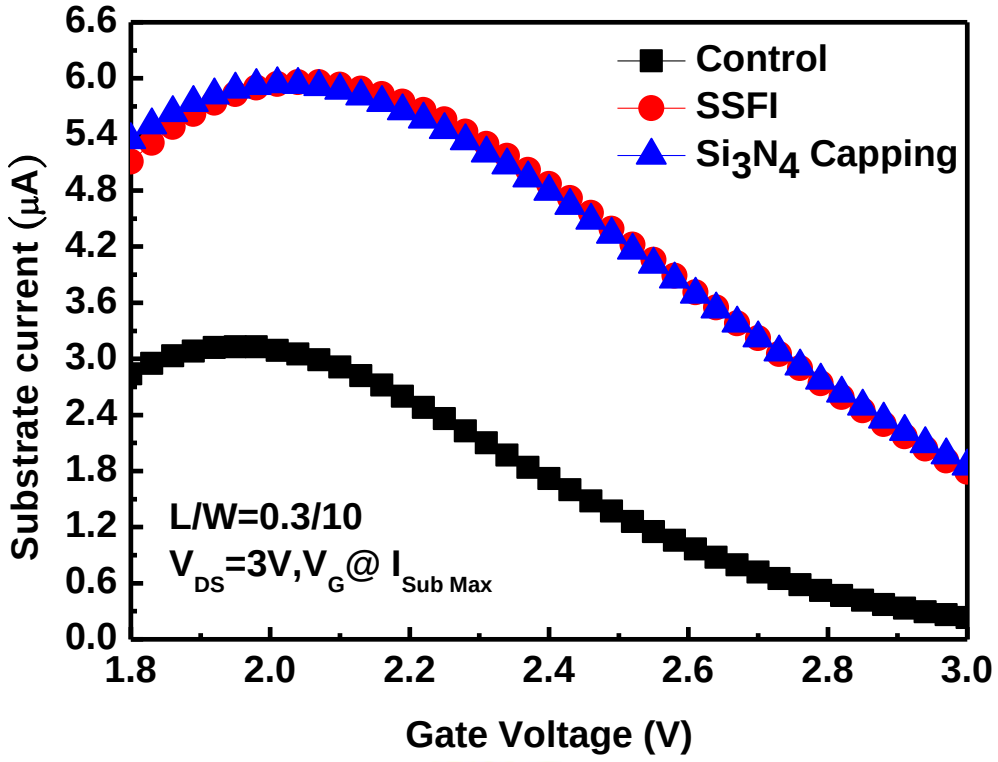

Fig.3.5 Substrate current versus gate voltage for these samples of HfO_2/SiON gate stack n-MOSFETs.

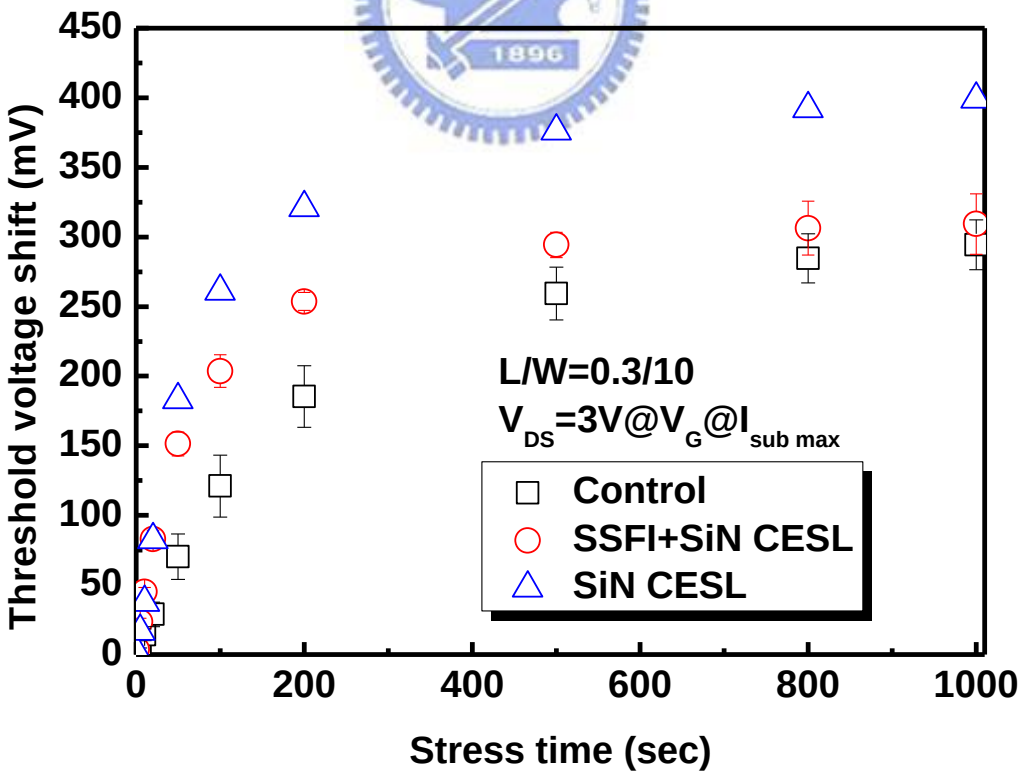

Fig. 3.6 Threshold voltage shift as a function of stress time with HCS which compares Control, SiN CESL and SSFI+SiN CESL.

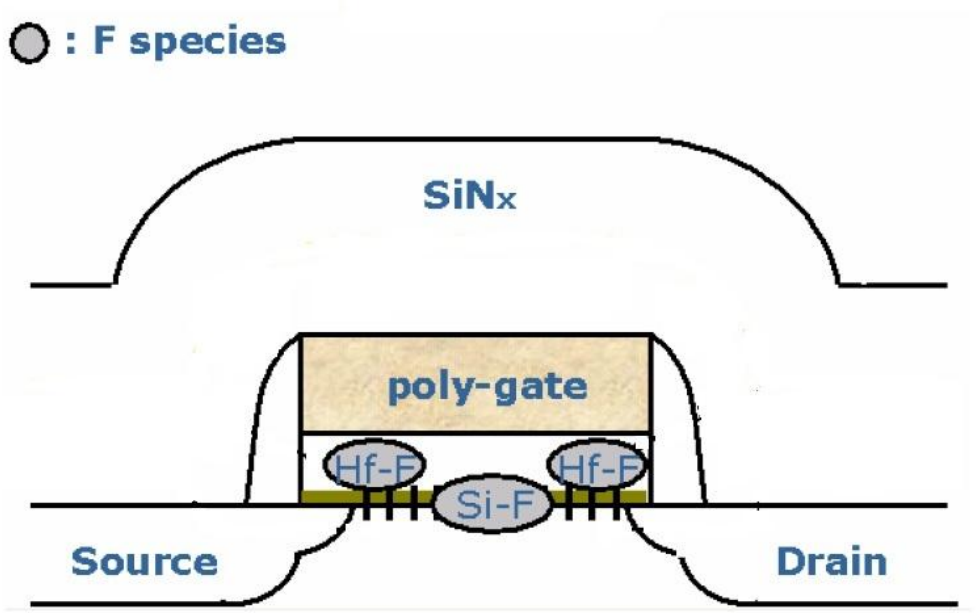

Fig. 3.7 The fluorinated CESL device has a large amount of F atoms incorporating to passivate the bulk and interface trap charges of HfO2/SiON gate stack n-MOSFET.

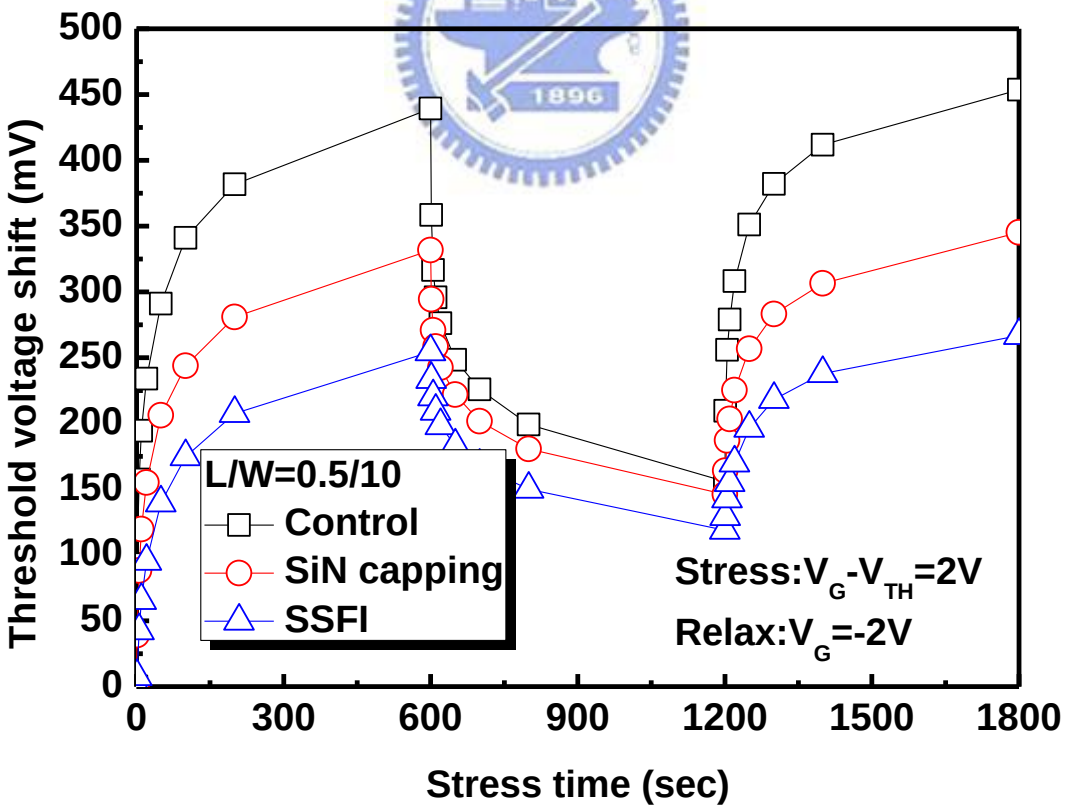

Fig. 3.8 Threshold voltage shift with de-trapping bias -2V dependence after positive voltage stress on these samples.

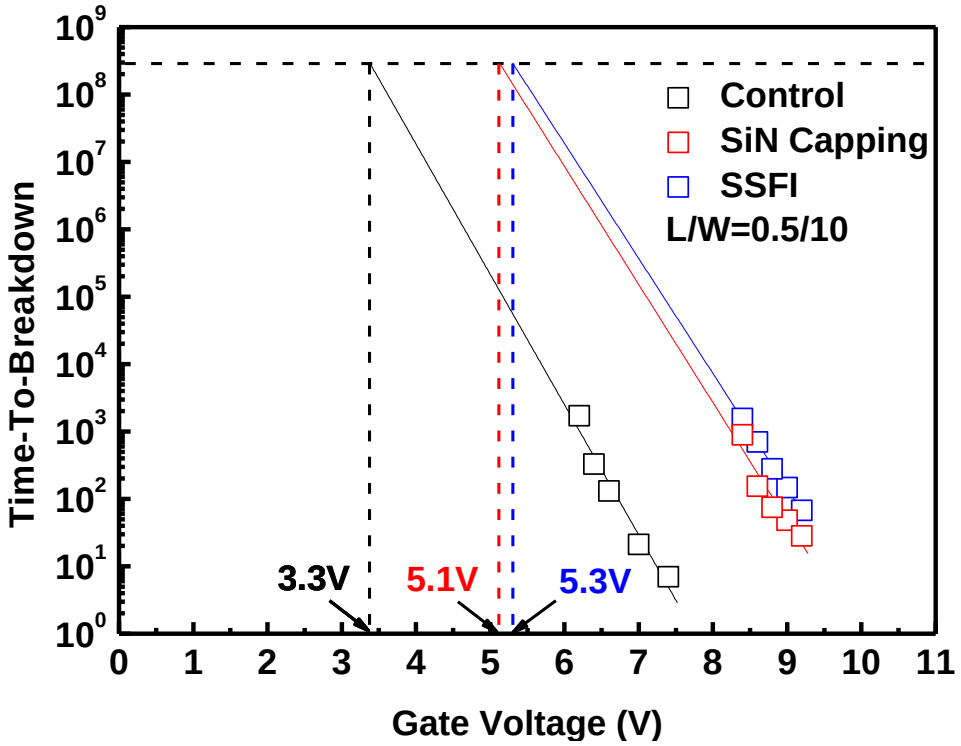

Fig. 3.9 The time-to-breakdown (T_{BD}) characteristic of the nMOSETs with TEOS P.L, SiN P.L and fluorinated SiN P.L

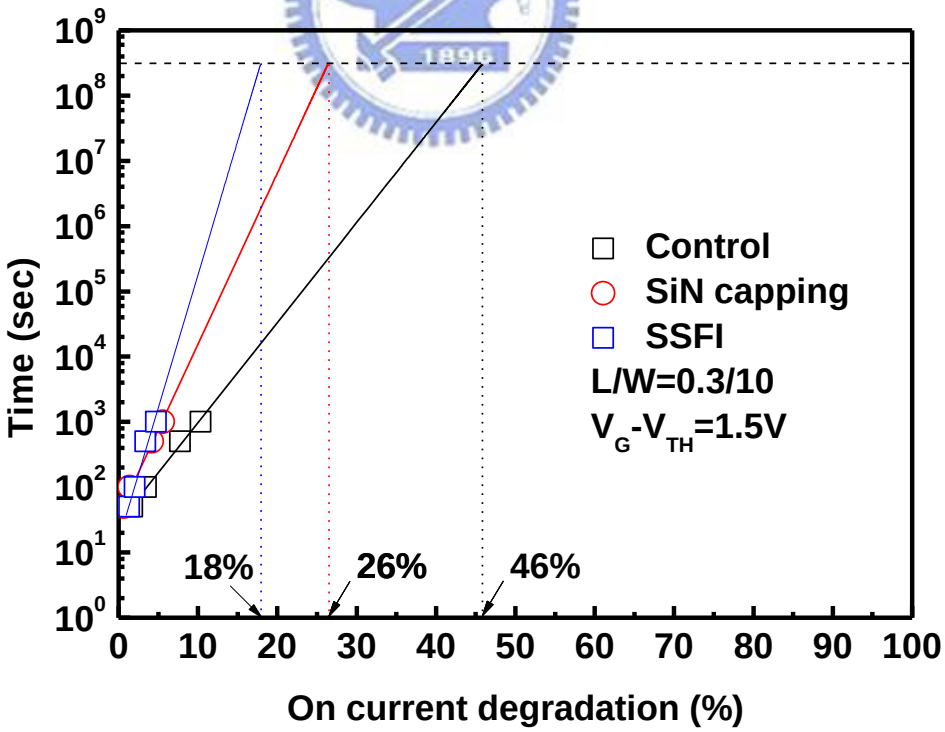

Fig. 3.10 On current degradation of the nMOSETs with TEOS P.L, SiN P.L and fluorinated SiN P.L

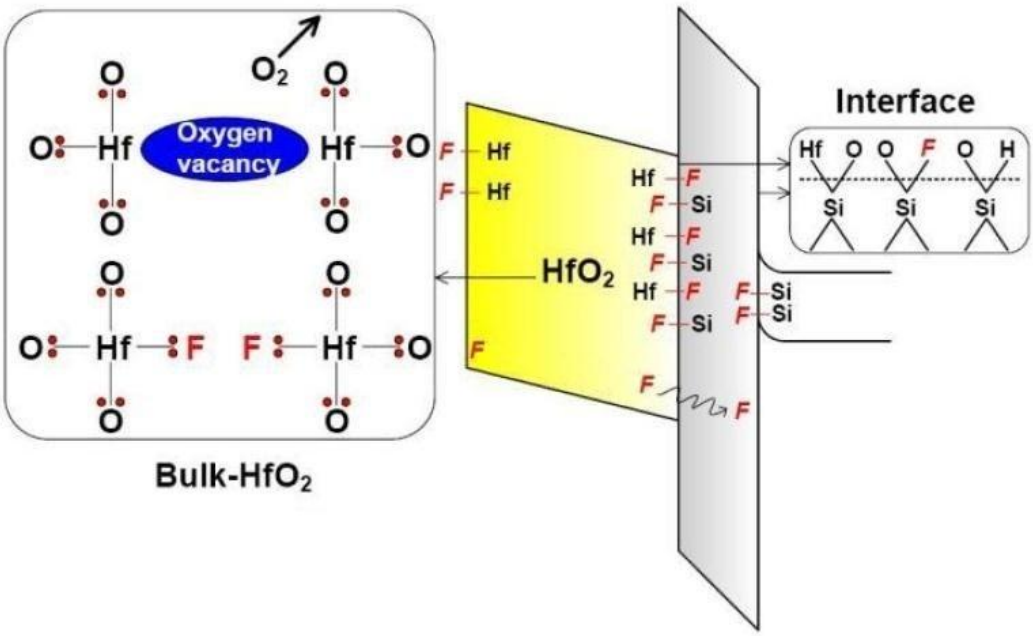

Fig. 3.11 Schematic of reliability improvement for the fluorine incorporation

CHAPTER 4

Conclusions and Future Works

4.1 Conclusions

In this thesis, a novel fluorinated CESL strained of HfO_2/SiON gate stack n-MOSFET is proposed. The impact of fluorine incorporation into strained HfO_2/SiON gate stack by silicon surface fluorine implantation (SSFI) was investigated. Several important phenomena were observed and summarized as follows:

First of all, we have investigated its basic electrical properties. The CESL strained high-k device to enhance the electrical characteristics due to enhance carrier mobility. We have found that improvements include many aspects, such as reduced gate leakage current, better subthreshold swing, enhanced normalized transconductance and driving current which correspond with higher mobility. Fluorine incorporation does not reduce the better basic characteristic caused by strained effect. They are almost similar on basic electrical characteristic. However, when fluorine doses are greater than 1E12 cm^{-2}, performance is not as good as 1E12cm^{-2}. Therefore, fluorine dose has a optimize value. The gate leakage current is analyzed by the carrier separation measurement, and can be explained by the band structure of the gate stack. The S/D current I_{SD} that corresponds to the electron current dominates the leakage

under inversion region, while the substrate current I_{SUB} that indicates the hole current dominants the leakage current under accumulation region. All leakage current can be categorized by fitting to be of Frenkel-Poole type.

In the second part of the thesis, we have studied the CVS, HCS and charge de-trapping mechanisms of poly-Si gate HfO_2/SiON dielectric with and without fluorinated. It is believed that the CVS and HCS degradation are related to the electron traps in high-k dielectric and the interfacial degradation, resulting in threshold voltage shift. The strained device with fluorinated also promotes the CVS and HCS immunity due to the formation of the rather stronger Si-F bonds in not only the HfO_2 bulk but also the interface including near S/D sides.

4.2 Suggestions for Future Works

There are many issues that we can't discuss completely. We list some goals for future work as follows:

1. HRTEM is used to verify real thickness and estimate value of the dielectric constant for HfO_2/SiON gate stack.
2. In actual CMOS circuit operation, AC gate bias with specific frequency and duty cycle is usually utilized. Therefore, AC stress with dynamic AC stress application is more realistic and can provide additional insights into the trapping behavior.

3. Fast transient pulsed I_D-V_{GS} measurement is also used to evaluate charge-trapping phenomena precisely.
4. We could use different fluorine incorporation methods (ex: CF_4 plasma treatment), whether it can provide better performance or reliability.
5. This process, whether it can be compatible with HG-MK process which is the most popular technology.

Vita (Chinese)

姓名：邱芳毓

性別：女

生日：民國74 年 2 月 11 日

籍貫：臺北市

學歷：淡江大學電機工程學系（94.9-96.6）

國立交通大學電子工程研究所（97.9-99.7）

碩士論文題目：

氟摻雜對應變矽於二氧化鉿堆疊式金氧半場效電晶體其特性和可靠度的影響

Impact of Fluorine Incorporation on Characteristic and Reliability Issues of the CESL Strained nMOSFETs with HfO_2/SiON gate dielectric stack