國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

電偶極工程與高介電係數阻絕層於氮化矽與奈米微晶粒非揮發性記憶體之研究

A Study of the Impact of Dipole Engineering and High-k Blocking Layer on Nonvolatile Memories with Nitride and Nanocrystal Trapping Layer

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中華民國 九十九 年 八 月

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摘　　要

在本論文中，我們先利用多晶矽-氧化矽-氮化矽-氧化矽-單晶矽型式(SONOS-type)的電容平帶電壓變化，探討氧化鋁(Al_2O_3)與二氧化鉿(HfO_2)在二氧化矽(SiO_2)的接面上產生的”本質電偶極”(intrinsic dipole)。我們發現當氧化鋁或二氧化鉿沉積在二氧化矽上會使電容的平帶電壓變大，反之若是二氧化矽沉積在氧化鋁或二氧化鉿會使其平帶電壓變小。我們也發現氧化鋁產生的本質電偶極大約是二氧化鉿的兩倍。接下來將這個結果運用在二氧化鉿的奈米結晶粒的非揮發性快閃記憶體元件，發現元件的電容平帶帶壓變化有相同的結果，但由於此次實驗元件有很嚴重的閘極注入電子，使元件在福勒-諾德漢穿隧(Fowler Nordheim tunneling)抹除操作時無法正常運作，但接下來的實驗中我們將解決此問題。

再者，我們利用了高介電係數材料(Al_2O_3,$HfAlO_x$)取代二氧化矽當作阻絕氧化層運用在奈米微晶粒(nanocrystal)的非揮發性的快閃記憶體元件，經過測試我們發現這層高介

電常數材料並不會因會我們的離子佈值後退火產生嚴重的劣化。我們驗證介電係數越高的阻絕氧化層材料記憶體操作速度亦越快，但由於此高介電係數材料中的缺陷，使我們在抹除操作時有暫態的現象。此元件擁有很快的寫入速度(programmin speed)，同時也有很高的資料保持度(retention)，在經過一萬次的寫入抹除操作下(endurance)依然可以維持很好的記憶體效果。

最後，我們結合了之前的分析，將本質電偶極(Al_2O_3, HfO_2)沉積在穿隧氧化層上，且運用高介電係數材料(Al_2O_3)的阻絕氧化層，做出多晶矽-氧化鋁-氮化矽-氧化矽-單晶矽型式的非揮發性記憶體元件。我們發現元件的臨界電壓會因電偶層存在而變大。我們分別利用福勒-諾德漢穿隧(Fowler Nordheim tunneling)與熱載子注入(hot carrier injection)兩種操作方式探討此電偶層對於元件的寫入與抹除的情況，並且探討其資料保(retention)度與元件的容忍度(endurance)和擾亂程度(disturbance)的影響。

A Study of the Impact of Dipole Engineering and High-k Blocking Layer on Nonvolatile Memories with Nitride and Nanocrystal Trapping Layer

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ABSTRACT

In this thesis, we first study the influence of the presence of "intrinsic dipole" on the electrical properties of a SONOS-type nonvolatile memory (NVM) by a capacitor structure. The magnitudes of "intrinsic dipole" were extracted by the V_{FB} shift observed in the C-V curves of the capacitors with adding Al_2O_3 or HfO_2 inside the standard gate stack structure of a SONOS-type NVM, i.e., $SiO_2/Si_3N_4/SiO_2$. We found that V_{FB} shifted toward positive direction when Al_2O_3 or HfO_2 were deposited on top of SiO_2 (tunneling layer). In contrast, V_{FB} shifted toward negative direction when Al_2O_3 or HfO_2 was deposited on top of Si_3N_4 (blocking layer). In addition, the magnitude of V_{FB} shift for Al_2O_3 was about twice larger than HfO_2. Next we also applied this scheme to the HfO_2 nanocrystal SONOS-type NVM, and found that the tendency of V_{FB} shift in the HfO_2 nanocrystal NVM was the same with the

conventional SONOS NVM. However, there was a serious gate injection problem in our device, so the fabricated devices can not be normally erased by FN-tunneling. We would tackle this problem in later chapters.

Then, we adopted the high-k material (Al_2O_3, $HfAlO_x$) to replace the traditional SiO_2 as blocking layer for the HfO_2 nanocrystal NVM. With high thermal budget processing for device fabrication, the high-k materials sustained pretty well and did not depict visible degradation. We exhibited the $HfAlO_x$ as blocking layer having faster programming and erasing speed. However, there were plentiful defects in the $HfAlO_x$ layer, and this made our device have "transient phenomenon" during erase operation. For our nanocrystal memory devices, there were advantages of fast programming speed, excellent data retention time at room temperature, and superior endurance after P/E cycles of 10^4.

Finally, we adopted the intrinsic dipole scheme, i.e., depositing additional Al_2O_3 and HfO_2 on top of tunneling oxide and used Al_2O_3 as blocking layer to make the so called SANOS-type NVM. The presence of dipole reflected on the observed larger device threshold voltage than the conventional one. Here we use both the FN-tunneling and hot carrier injection to study the electrical characteristics of the fabricated devices. We found that FN-tunneling operation has led to better endurance than hot carrier injection operation. Moreover, we also discussed the impact of dipole engineering on the retention and disturbance characteristics of our newly-developed nonvolatile memories.

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Chapter 1

Introduction

1.1 Overview of Nonvolatile Memory

The semiconductor industry have made progress continuously with complementary metal-oxide-semiconductor (CMOS) memory technology, thus people's life have been changed by various kinds of portable electronic products ,such as cell phone, MP3 player, digital camera, notebook computer, and other personal electronic consumed products whatever you can think. It's apparent to represent memory device, which playing the important role in our life.

It's simple to distinguish memories into two main categories by whether the stored data will vanish or not with power supply. If they lose stored information once power supply is switch off and it's called volatile memory, such as DRAM. Otherwise, it is Nonvolatile Memory (NVM) such as ROM. About NVM it let we can stored our picture in our digital camera and store music in MP3 player. Because it keep stored information also when the power is switch off.

With the NVM device continuously developed, we can also divide NVM into non-charge-based memory like MRAM [1.1], RAM [1.2] and charge-based memory like Intel ETOX [1.3].The typical charge-based memory is also called flash memory. As the different trapping layer, there are three types of flash memory including the floating gate (FG) type, SONOS [1.4] (Silicon/Oxide/Nitride/Oxide/Silicon) type, and nano-crystal [1.5] or metal-dot type. Among the types of memories mentioned about, flash memory has the advantage of good program/erase (P/E), low operation, small area ,low power consumption, and low cost. In 1967,D Kahng and S. M. Sze invented the first floating-gate(FG) nonvolatile semiconductor memory at Bell Labs[1.6]. These days, a lot of electronic products still adopt the floating-gate structure. Nevertheless, the current floating-gate flash faces a critical scaling challenge due to the floating gate coupling effect [1.7].

The tunnel oxide of floating gate device has to be thick enough (8~10nm) to maintain superior retention and endurance, but it also cause large operation voltage, high power consumption, slow program/erase (P/E) speed, and the most important, hard to be scaled. In addition to, the poly silicon floating-gate is conductive; the total charges stored in floating gate would be easily lost when the tunnel oxide has a single defect or damaged during P/E cycles, such as SILC issues [1.8]. On the other word, the scaling limit of floating-gate memory to lateral and vertical is charge loses due to SILC and the effect of parasitic capacitive coupling. Moreover, the trapping layer is conductive, so it can't use Multi-Level Cell (MLC) to make data with double density. To overcome these disadvantages mentioned above, new memory structure, such as SONOS type, and nano-crystal or metal-dot type memory, will be the solution to these problems.

SONOS-type (Silicon/Oxide/Nitride/Oxide/Silicon) devices are forecasted as the solution beyond the 45-nm node [1.9] because charge trapping devices are naturally immune to the floating gate coupling interference. The conventional SONOS memory is shown in **Figure 1.1(a)**. It has recently been a promising candidate for the next-generation nonvolatile memory. Contrary to the floating gate device where charge is uniformly stored in the floating gate, the charge is locally trapped in the nitride thin film. It can avoid to SILC issues, coupling effect, and not only SLC (single level cell) operation. However, conventional SONOS memory still has some problems, such as electron vertical and lateral migration show in Figure 1.1(b) and data retention. Next we did some discussion to see others people how to improve. There are three points of SONOS-type flash memory with O/N/O structure that we can discuss which were tunneling layer, trapping layer, and blocking layer.

Tunneling layer

The fist" O" is SiO_2 as tunneling oxide (bottom oxide) with normal SONOS-type device. In 2005 the MXIC use the ultra-thin "ONO" (Oxide/Nitride/Oxide) to replace the tunneling oxide and it named to BE-SONOS (Bandgap-Engineered SONOS) [1.10]. The structure is shown in **Figure 1.2(a)**. The ultra-thin ONO layer provide a modulated tunneling barrier, it reduces direct tunneling at low electric field during retention, but it allows efficient hole tunneling erase at high electric field due to the band offset. The band structure is shown in **Figure 1.2(b)** .Therefore, this BE-SONOS offers fast hole tunneling erase, while it is immune to the retention problem of the conventional SONOS. And the ultra thin ONO layer is trap free and use the simple material, which may improve the reliability issues with conventional SONOS.

Trapping layer

The "N" is Si_3N_4 as trapping layer with normal SONOS-type device. In recent years, the trapping layer materials have been investigated to improve the cell data retention. For example, the use of an Al_2O_3 trapping layer and HfAlOx to replace Si_3N_4 have been consider since their material band gaps and high trap densities offer superior program/erase speed and data retention [1.11]. Moreover, various kinds of nanocrystal, such as silicon (Si) [1.12], germanium (Ge) [1.13], and metal nanocrystal, may be use to provide charge storage for memory devices. A basic structure for nanocrystal is shown in **Figure 1.3 (a)**. Just like use $HfSiO_x$ to forming localized HfO_2 for application in high-density two-bit nonvolatile Flash memory [1.12]. And in 1995, Tiwari et al. first proposed a Si nanocrystal nonvolatile at IBM [1.14]. For conventional SONOS memory, erase saturation [1.15] and vertical stored charge migration [1.16] are two major drawbacks. The electron migration is shown in figure. Therefore, nanocrystal-type memories with very local storage have been invented, as the **Figure 1.3(b)** shows.

Blocking layer

The second "O" is SiO_2 as blocking oxide (top oxide) with normal SONOS-type device.

In 2003 Samsung Electronics use Al_2O_3 to replace SiO_2 for the blocking oxide. And they prose a new device structure with TaN metal gate instead of the n^+ poly-Si gate which named to TANOS [1.17], the structure is shown in **Figure 1.4(a)**. The electric field across the tunnel oxide can be increased with using high-k material for the blocking oxide. Simultaneously, the electric across blocking oxide is proportionally reduced with its dielectrics, and then the gate injection current is suppressed effectively, as the **Figure 1.4(b)** shows. Therefore the device can use a thicker tunneling oxide without losing P/E speed. The TaN has high value of work function to suppressed gate injection current, excellent thermal stability to over high temperature process and eliminated the ploy-depletion. Owing to the diligences on search, researches let the SONOS-type can be candidate for next-generation nonvolatile memory application.

Operation principle

About the operating mechanism of nonvolatile memory with programming and erasing, that we have Fowler-Nordheim tunneling and hot carrier injection methods. For floating gate nonvolatile memory is ”written” when we programmed the electrons into floating gate by Channel-Hot-Electron (CHE) [1.18] programming then the threshold voltage(V_T) increases for the MOSFET. Otherwise, we erase the stored electrons and restoring V_T to its original value by Fowler-Nordheim (FN) tunneling or band to band hot hole injection (BTBHHI) from floating to source. The V_T shift between the programmed and erased states is denoted by a quality know as the “memory window”. Unlike floating gate device the trapping is conductive, when SONOS-type nonvolatile memory uses CHE to program and its just only could be erased with BTBHHI; otherwise write electron to nitride with Fowler-Nordheim tunneling and erase electron with Fowler-Nordheim tunneling, too. The principle of CHE program and the and diagram of BTBHHI erase, FN program, and FN-erase are shown in **Figures 1.5(a), (b), (c), and (d)**. The memory state of the device can be determined by the sensing current with read voltage (V_{Read}) . The read voltage is set in the range of the memory window, as the

Figure 1.6 shows. It's simple enough to distinguish the states of "1" or "0", and make fast operating speed.

Extraordinary fast growing nonvolatile memory market mainly leaded by mobile applications push the nonvolatile memory technology to be cutting edge. As a result of the flexibility and higher effective speed and density which combined with a fast in-system erase capability, these low-power and robust Flash systems are ideal for a myriad of portable applications. It provide single cell electric program and fast simultaneous block electric erase. They even are going to replace random access memory in many applications. As more and more people's needs, the System-On-Chip (SOC) notion for ultra-large scale integration (ULSI) is more and more important. A complex system can be integrated into a single chip via SOC design methodology and achieve lower power, lower cost, and higher speed than the traditional board level design. Due to the different of device modules such, thermal, material and the ears issues, there are grate challenges wait for us to solve.

1.2 Motivation

As people demand more and more electronic technology, the pursuit of high performance and high reliability is the goal of many researchers. About the nonvolatile memory, there are still many problems under the rapid development. For an example, use the ultrathin tunneling oxide to obtain higher program/erase speed and it's not reliable due to the direct tunneling at retention. In addition to, SILC is also seriously affected on data retention after P/E cycles. As we know, there is a faster program/erase speed with thinner tunneling layer but much poor retention. It is making us into a dilemma for the device scaling.

In our study, we utilize the HfO_2 nanocrystals as the trapping layer, which may exhibit superior characteristics, such as large memory window, high program/erase speeds, long retention time, and excellent endurance. Moreover, we use the High-k material to replace SiO_2

as the blocking layer, which may reduce the driver voltage and improve the gate injection due to its high dielectric constant. Here, we also use the dipole layering to engineer the bandgap between the SiO_2 tunneling oxide and the Si_3N_4 trapping layer. On the basis of the band diagram, we may sacrifice the erase speed, however, the better program speed and data retention time we could get. This will help us solve the dilemma between the higher program speed and the poor retention. The process is very simple, and reliable with less metal contamination.

1.3 Organization of the Thesis

In **Chapter 2**, we use the capacitance to discus the shift of band diagram due to dipole layer deposition with conventional SONOS-type structure. There are four topics we can discus to. First, we can discuss the influence of the dipole layer deposition between bottom oxide and trapping layer. Second, discuss the influence of the dipole deposition on Si_3N_4. Third, discuss the influence of the dipole deposition between trapping layer and top oxide. Last, we can discuss the influence of the double dipole layer deposition both on bottom oxide and trapping layer. By the experiments, we can reasonably infer the impact of band structure.

In **Chapter 3**, we use the $HfSiO_x$ to obtain HfO_2 nanocrystal nonvolatile memory after RTA treatment. Using this technique, we can readily isolate the HfO_2 nanocrystals from each other within a SiO_2-rich matrix. And, we match the high-k material as a blocking oxide. Last, using the structure we may exhibit superior characteristics. Moreover, we can discuss the influence of different high-material as a blocking oxide.

In **Chapter 4**, we use the Al_2O_3 and HfO_2 as the dipole layer to apply on SANOS nonvolatile memory. We can discuss the impact of dipole layer on program/erase speed with two different operation mechanisms, and data retention time. Through the experiments among above, we hope to help the NVM development.

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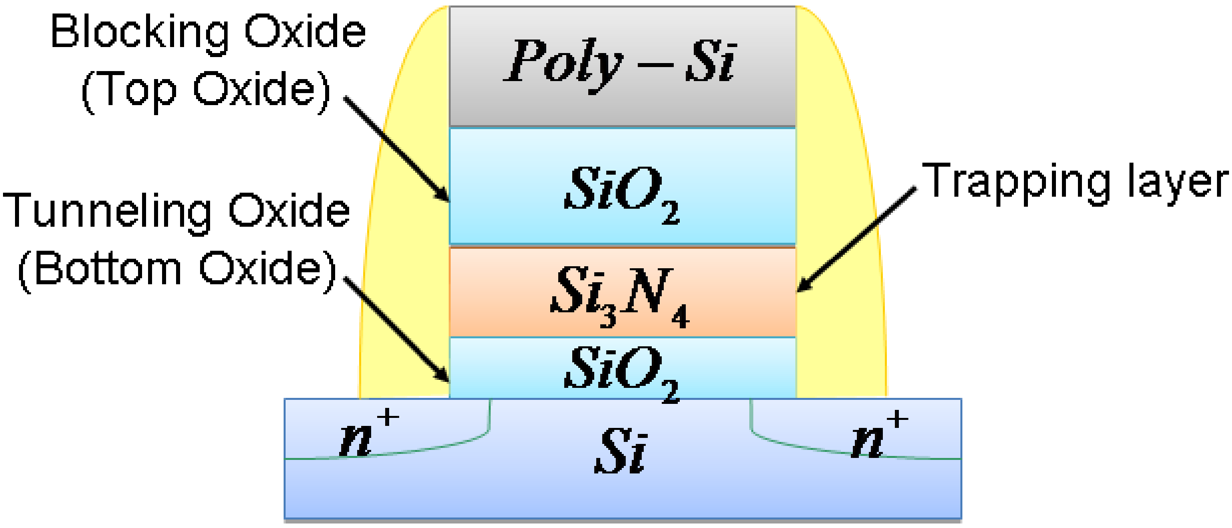

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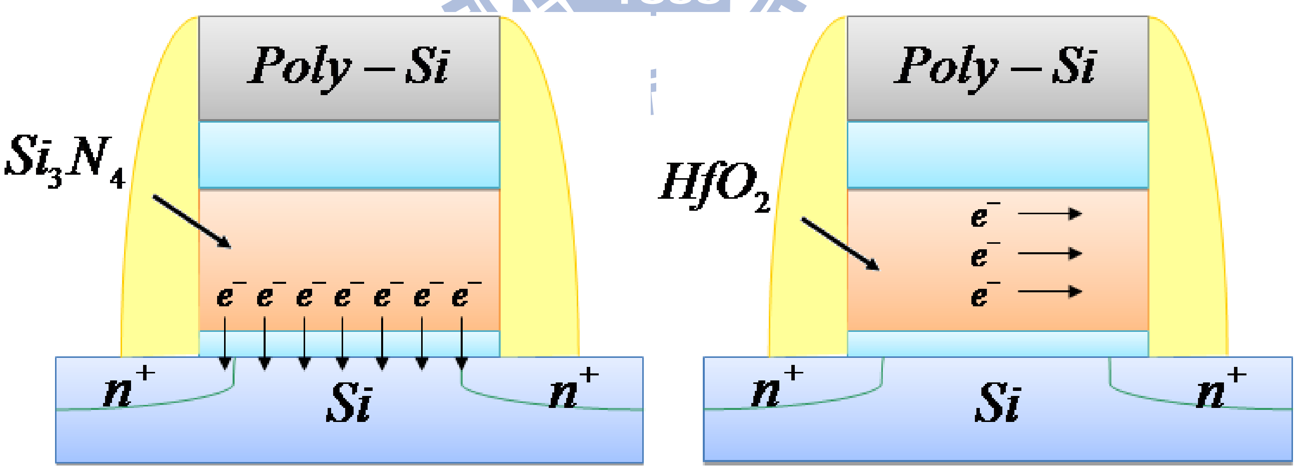
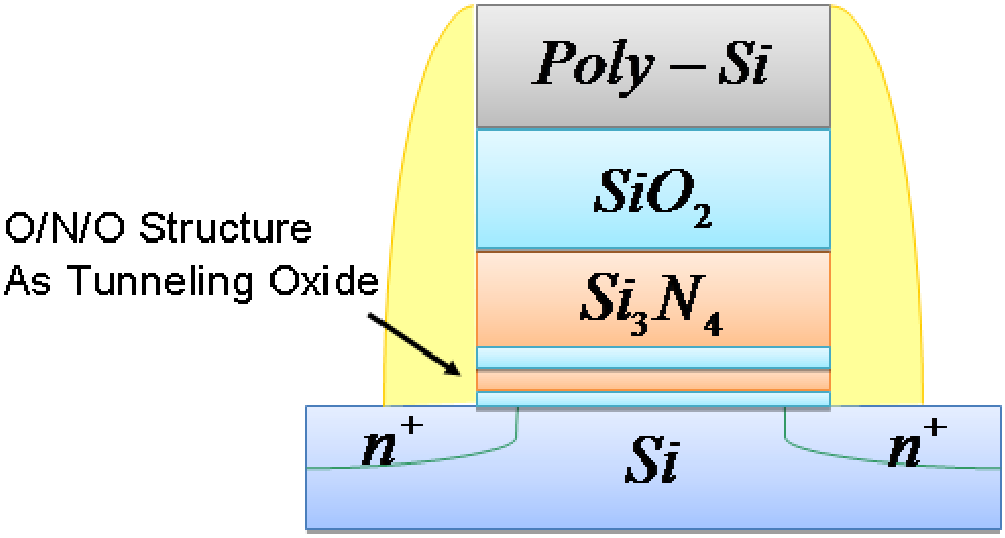


(b)

Fig 1.1 (a) Schematic of a basic conventional SONOS Flash memory device. (b) Vertical migration of stored charge in Si_3N_4 trapping and lateral migration of the stored in the HfO_2 trapping layer in SONOS memory device structure.



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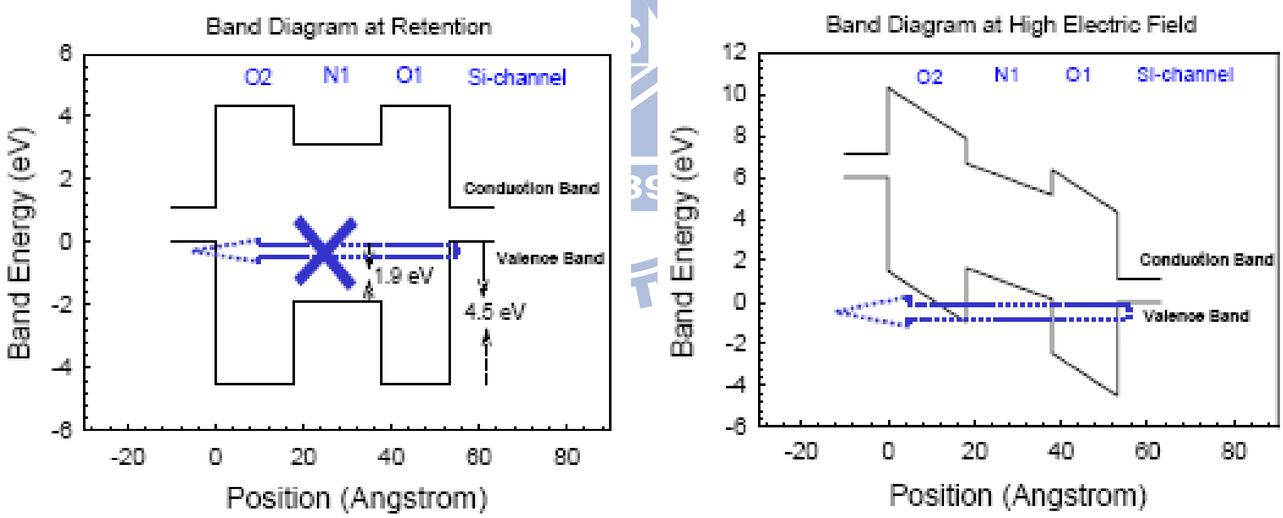
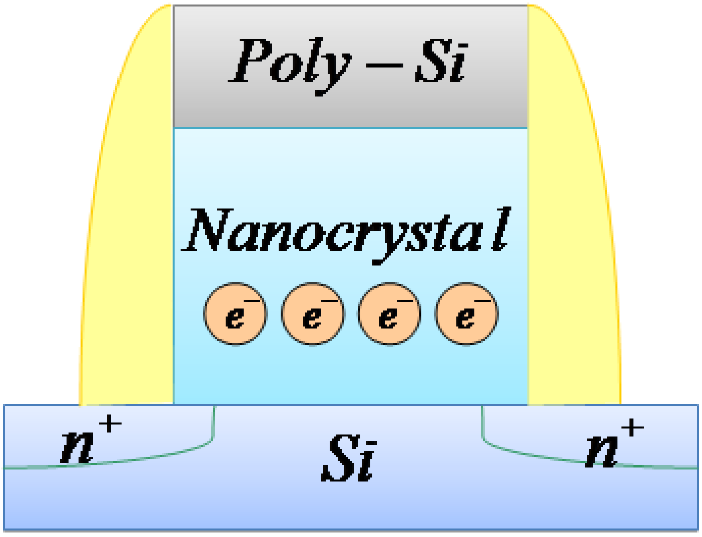


(b)

Fig 1.2 (a) Schematic of a basic BE-SONOS [10] Flash memory device. (b) The band structure of BE-SONOS tunneling layer at low electric field during retention and hole tunneling erase at high electric field due to the band offset.



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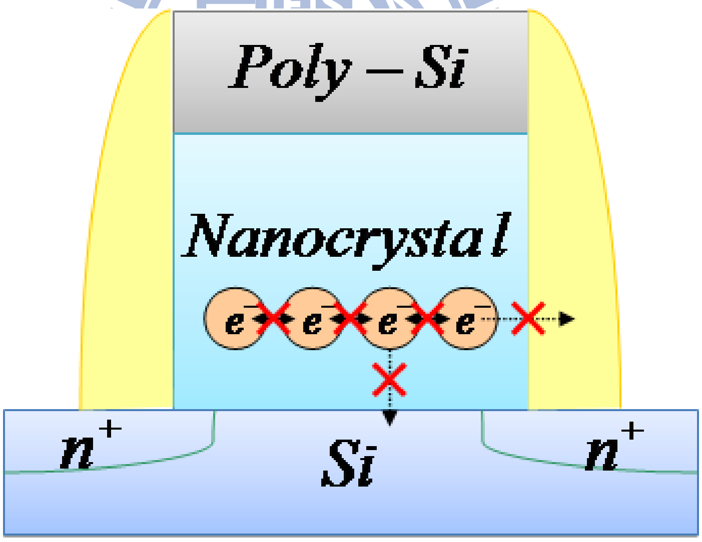
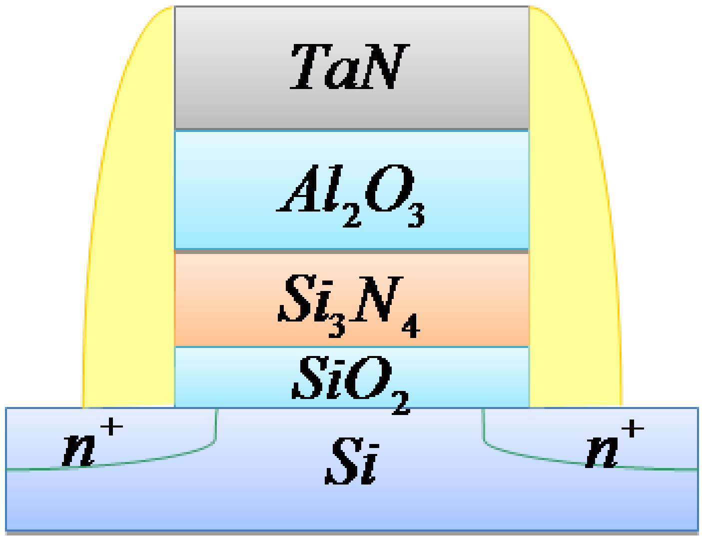


(b)

Fig 1.3 (a) An illustration of a nanocrystal memory. (b) The nanocrystal can store the charge locally due to the well isolation of nanocrystal from each other and effectively prevents formation of good conductive paths between the adjacent nodes.



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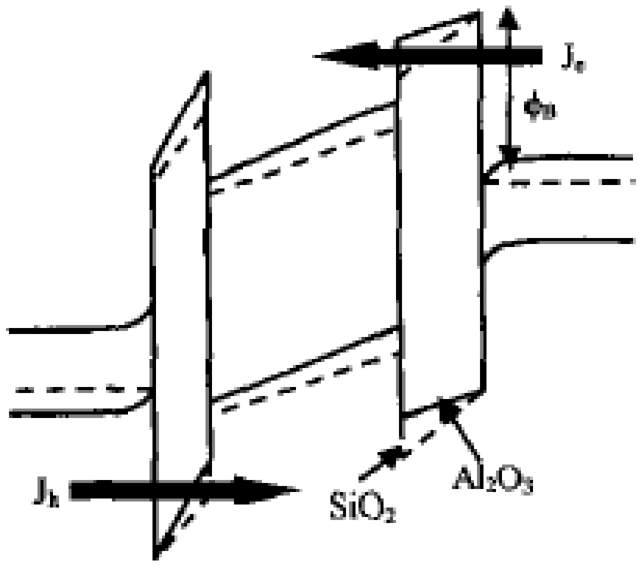

(b)

Fig 1.4 (a) Schematic of a basic TANOS [17] Flash memory device. (b) The band diagram compare with SiO_2 and Al_2O_3 as blocking oxide during erase situation. The Al_2O_3 can effectively inhibit gate injection than SiO_2.

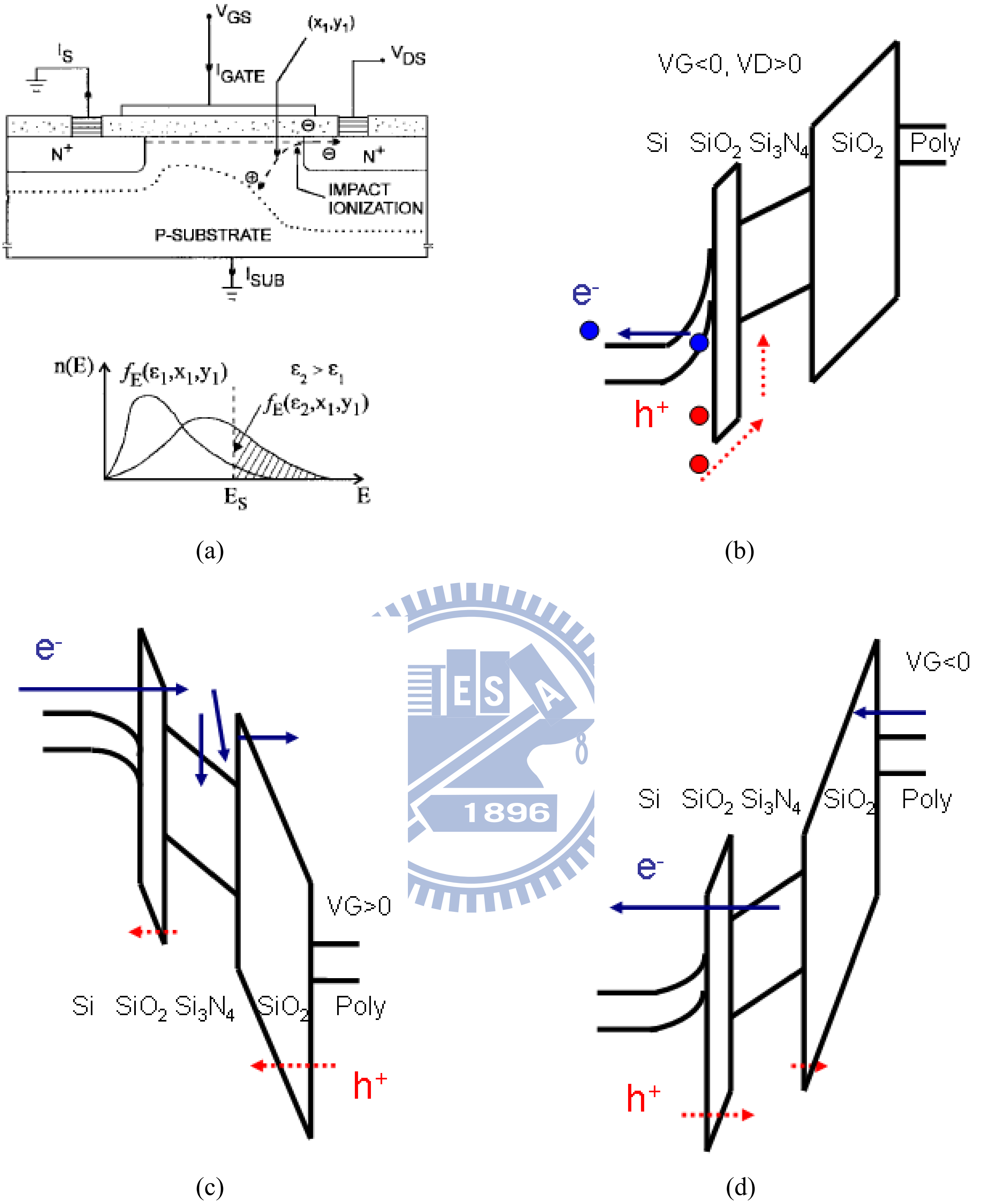

Fig 1.5 (a) The principle of CHE program. (b)The band diagram of band to band hot hole injection erasing. (c) The band diagram of Fowler-Nordheim tunneling programming.(d) The band diagram of Fowler-Nordheim tunneling erasing.

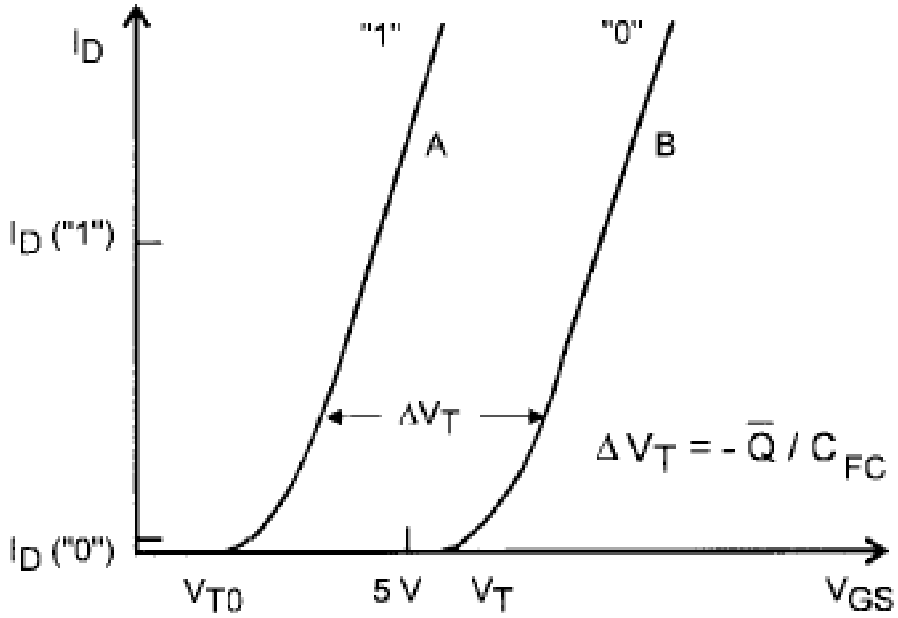

Fig 1.6 Current-Voltage characteristics of a memory device in the programmed state and erase state display the V_T shift and memory window.

Chapter 2

Effect of Interfacial Dipole on SONOS-type Memory Capacitors and Nanocrystals Memory Devices

2.1 Introduction

SONOS-type (Poly Si-Oxide-Nitride-Oxide-Silicon) flash memories have recently attracted much attention as a candidate for the next-generation. As a result of they have many advantages of operation characteristics such as, high P/E speed, low operation voltage, low power consumption, excellent retention, endurance, and disturbance [2.1-2.3]. As people demand more and more electronic technology, the pursuit of high performance and high reliability is the goal of many researchers.

In addition to, a high-k metal gate scheme for metal-oxide-semiconductor field-effect-transistors (MOSFET) above of 45nm technology is considered to replace the traditional SiO_2/polysilicon based device due to the poly depletion effect [2.4] and gate leakage for ultra thin oxide. One of serious problem of high-k/metal gate CMOS is to control the threshold voltage (V_T). As we know, the V_T of n and p MOSFT must be the same in CMOS logic circuits [2.5-2.7]. Recently, the interfacial dipole with high-k/SiO_2 interface has a significant role on V_{FB} shift due to the dipole layer formation [2.8-2.13].In they year of 2007, *K. Iwamoto et al* indicate that the high-k/IL-SiO_2 interface plays the significant role in the V_{FB} control of the high-k MOS device. And *Y. Kamimuta et al* further use the different material as gate with different high-k material to indicate the relationship such as the **Figure 2.1 (a)** shows. And the band diagram of high-k/SiO_2 with different high-k material is shown in **Figure 2.1(b)**. The energy offsets at the interface of Al_2O_3, HfO_2, and Y_2O_3 on SiO_2 are estimated to be ±-0.57±0.05, ±0.31±0.05, and 0.23±0.05eV, respectively.

There are three theories about the origin of the dipole layer at high-k/SiO_2. In the years of 2007, *Sivasubramani et al* considered that the dipole magnitude was determined by electronegativitiy and ionic radii of cations [2.11]. In the years of 2008, *Kita and Toriumi et al* reported that the areal density difference of oxygen atoms was the origin of dipole formation at high-k/SiO_2 interface [2.12]. They have predicted an effect of various oxides on V_{FB} in terms of interface dipole, as show in **Figure 2.1(c)**. And in 2010, *Xiolei Wang et al* proposes a DCIGS (dielectric contact induced gap states) model to interpret the physical origin of dipole formation for high-k/SiO_2 systems [2.13]. Although, they have different point of view on the interfacial dipole, they did confirm that the high-k/SiO_2 interface has a significant role on V_{FB} shift.

2.2 Experiment

Nitride-base SONOS-type memory capacitor are fabricated on a p-type, 20 ~ 30Ω cm, (100) 150-mm silicon substrate. After RCA clean, a 35 Å tunnel oxide was thermally grown at 800 ℃ in a horizontal furnace system. Then an ultra-thin high-k film (Al_2O_3 5 Å, 10 Å, 20 Å, and 30 Å or HfO_2 10 Å, 30 Å) is deposited by MOCVD system or not deposited and continuous to after that step. Next a 90 Å Si_3N_4 film is deposited by horizontal furnace LPCVD system. Then an ultra-thin high-k film (Al_2O_3 10 Å, 20 Å, 30 Å or HfO_2 10 Å, 20 Å) is deposited by MOCVD system or not deposited and continuous to next step. Afterward a 10nm blocking oxide is then deposited through TEOS precursor by horizontal furnace LPCVD system. Subsequently, we deposited Al as top and bottom electrode by thermal coater as well as the memory capacitor with dipole layer is finished, as the **Figure 2.2** shows.

Then an example of the fabrication process of the HfO_2 nano-crystal with dipole layer nonvolatile memory devices is demonstrated by a LOCOS isolation process on a p-type, 20-30 Ω cm, (100) 150-mm silicon substrate. First, a 30 Å tunnel oxide was thermally grown at 800℃ in a horizontal furnace system. Then an ultrs-thin high-k layer (HfO_2 or Al_2O_3) is deposited by MOCVD to form dipole layer. The flow rate and pulse number of precursors is carefully modulated to obtain ~ 10 Å high-k film. Next a 120 Å amorphous $HfSiO_x$ silicate layer was deposited by MOCVD. The samples were then subjected to RTA treatment in an N_2 ambient at 950℃ for 1 min to convert the $HfSiO_x$ silicate film into the separated HfO_2 and SiO_2 phase. Afterward a 100 Å blocking oxide is then deposited through TEOS precursor by horizontal furnace LPCVD system. Subsequently, poly-Si deposition, gate patterning, n^+ source/drain (S/D) implantation , p^+ body implantation, activation 950℃ for 30 second, and the remaining standard CMOS procedures were completed to fabricate SONOS-type nonvolatile memory devices, as the **Figure 2.3** shows.

2.3 Results and Discussion

2.3.1 Effect of Interfacial Dipole on SONOS-type Capacitor

Previously described in our nitride-base SONOS-type memory capacitor experiments, we can discuss the contents of four. First, we can discuss the influence of high-k layer between bottom oxide and trapping layer. Second, we can discuss the influence of the high-k on Si_3N_4. Third, we can discuss the influence of the high-k between trapping layer and top oxide. At last, we can discuss the influence of the double dipole layer. The Cross-sectional TEM image of Si/SiO_2 30 Å / Al_2O_3 20 Å / Si_3N_4 150 Å / SiO_2 150Å and Si/SiO_2 30 Å / Al_2O_3 15 Å / Si_3N_4 150 Å / Al_2O_3 20 Å /SiO_2 150 Å are shown in **Figures 2.4(a) and (b).**

1. Discuss the influence of dipole layer between bottom oxide and trapping layer.

Figures 2.5(a) and 2.5(b) illustrate the structure of capacitors and their Capacitance-Voltage (C-V) characteristics. The samples are deposited with Al_2O_3 5 Å, 10 Å, 20 Å, 30 Å, and HfO_2 10 Å, 30 Å by MOCVD. In **Figure 2.5(b)**, it is found that adding an

Al_2O_3 or HfO_2 layer causes positive V_{FB} shift, compared with conventional SONOS capacitor. Magnitudes of dipole are ordered in monotonous decrease: Al_2O_3 5 Å, Al_2O_3 10 Å, Al_2O_3 20 Å, Al_2O_3 30 Å HfO_2 10 Å, and HfO_2 30 Å. The result is shown in the **Figure 2.6(a)**. The magnitudes of V_{FB} shift of Al_2O_3 is about twice large than HfO_2. Moreover, the magnitudes of V_{FB} shift will saturate at the dipole layer with 20 Å. Here we find that the V_{FB} shifts is larger when the high-k layer is thinner (>5 Å). In the beginning, we speculate that the thickness of dipole layer is more than we imagine. The equation follows as:

$$V_{FB} = \psi_{ms} - Q_{ox} / C_{ox} \tag{2-1}$$

However, we can confirm that the thickness is not different through TEM analysis. The relationship between the V_{FB} shifts and thickness of dipole layer may require further analysis to know why they are different with others experiments. The different of experimental procedure between ours and others are the source of dipole layer. Here, we use MOCVD and others use ALD (Atomic Layer Deposition) to deposit the dipole layer. The band diagram of this structure is shown in **Figure 2.6 (b)**

2. Discuss the influence of the dipole on Si_3N_4.

Figures 2.7(a) and 2.7(b) show the structure of capacitors and their C-V characteristics. In **Figure 2.7(b)** we find the V_{FB} of the sample of Al_2O_3 10 Å and HfO_2 10 Å with conventional SONOS almost the same. With the little different with of V_{FB}, we took that as a variation of process. After all, the gap is much smaller than previous experiments in discussion one. Therefore, we believe the dipole is substantially suppressed on Si_3N_4 film in place of SiO_2 in our experiments and coherence to our expectations.

3. Discuss the influence of the dipole layer between trapping layer and top oxide.

Figures 2.8(a) and 2.8(b) illustrate the structure of capacitors and their C-V characteristics. The samples are deposited with Al_2O_3 10 Å, 20 Å, and 30 Å by MOCVD. We find that the structures make the dipole to appear a negative V_{FB} shift, and coherence to our expectations. Finally, we sort out the result showing in the **Figure 2.9(a)**. The band diagram is shown in **Figure 2.9(b)**. However, we still find the same situation with the previous that the V_{FB} shift is larger when the dipole layer is thinner and also saturate at thickness 20 Å. This result is the same as with the previous in discussion one, thus this rationale should exist some physical meaning we should go further analysis to understand why they like this.

4. Discuss the influence of the double dipole layer.

Figures 2.10(a) and 2.10(b) emerge the structure of capacitors and their C-V characteristics. The samples are deposited with Al_2O_3 10 Å, 20 Å, 30 Å, and HfO_2 10 Å, 30 Å by MOCVD. Here, we contrast the sample of conventional SONOS capacitors and the sample of SONOS-type structure with Al_2O_3 deposition on tunneling layer, and the V_{FB} of these samples are between this two. The V_{FB} shift of Al_2O_3 is about twice of HfO_2. The band diagram is shown in **Figure 2.11**. The relationship between the V_{FB} shifts and thickness of dipole layer are not clearly, this may be owing to our real thickness lightly thicker than expected. As a result, make this situation has already reached saturation.

2.3.2 Effect of Interfacial Dipole on Nanocrystal Memory Device

In these experiments, we find that our devices have two serious problems which are gate injection and poly-depletion. The serious gate injection problem prohibits us to analyze the device characteristics. However, in later chapters we will address these two issues.

1. Poly depletion

Figure 2.12 illustrates I_{DS}-V_{GS} curve of the nanocrystal flash memory with Al_2O_3 dipole layer engineering. The on-off ratio can reach eight orders . However, we can find out the subthreshold swing (S.S.) is poor. After calculations, we get subthreshold swing equal to 611mV/dec. The ideal subthersold swing we can calculate by the equation:

$$S.S. = 2.3\frac{kT}{q}(1+\frac{C_{dep}+C_{it}+C_{poly}}{C_{ox}})mV/dec \qquad (2\text{-}2)$$

Figure 2.13 shows the charge pumping current measurement and used to calculate the value of interface state (D_{it}). Therefore, we have ideal value equal to 126mv/dec .The actual value is far worse with the ideal. We are reasonable guess that there are poly depletion issues, since use the wrong self-alignment implantation energy. However, we will change the process conditions and solve the problem in later chapters.

2. Gate injection

Figure 2.14(a) shows the I_{DS}-V_{GS} curve of the nanocrystal flash memory with programming time 1s and erasing time 1s. We find out the erasing characteristics which are suppressed by gate injection issues. The band diagram of erasing is shown in **Figure 2.14(b)**. We even obtain the same outcome as programming characteristics. We consider the quality of blocking oxide we adopting is worse. However, we will change the process conditions and solve the problem in later chapters.

The retention characteristics of nanocrystal flash memory at room temperature (T=25℃) are illustrated in **Figure 2.15(a)**. It results in about 80% memory window loss for 10^4 second retention time at room temperature. For such a bad result we are not surprised, as a result of the poor blocking oxide. We think the trapping charge is going to escape from blocking oxide, not tunneling oxide. The band diagram of retention is shown in **Figure 2.15(b).** In the beginning, we are thinking whether the process using is mistake. However, we confirmed that the quality of blocking is poor and use other material in later chapters.

Although the serious gate injection problem prohibits us to analyze the device characteristics. By the C-V characteristics of conventional nanocrystal and the nanocrystal with dipole layer engineering flash memory is shown in **Figure 2.16**. Obviously, the discovery of positive V_{FB} shift owing to Al_2O_3 dipole layer engineering.

2.4 Summary

In this chapter, we demonstrate the effect of interfacial dipole on SONOS flash memory capacitors on C-V characteristics. We find that the dipole of ultra thin Al_2O_3 and HfO_2 layer on the SiO_2 tunneling layer has a positive V_{FB} shift and on the Si_3N_4 trapping layer (under SiO_2 blocking layer) has a negative V_{FB}. Furthermore, when the high-k layers are deposited on the SiO_2 tunneling layer and Si_3N_4 trapping layer, we can find that the value of V_{FB} is similar to V_{FB} of conventional SONOS capacitors. The shift of Al_2O_3 is about twice of HfO_2. Moreover, the thinner high-k layer cause a larger V_{FB} shift and saturate at 20 Å. The relationship between the V_{FB} shifts and thickness of dipole layer may require further analysis to know why they are different with others experiments. When the Al_2O_3 dipole layer applied in Hafnium silicate nanocrystal flash memory device, we can also find out the positive V_{FB} shift from C-V characteristic. Although there are gate injection and poly depletion problems in our devices, we will tackle these problems in later chapters.

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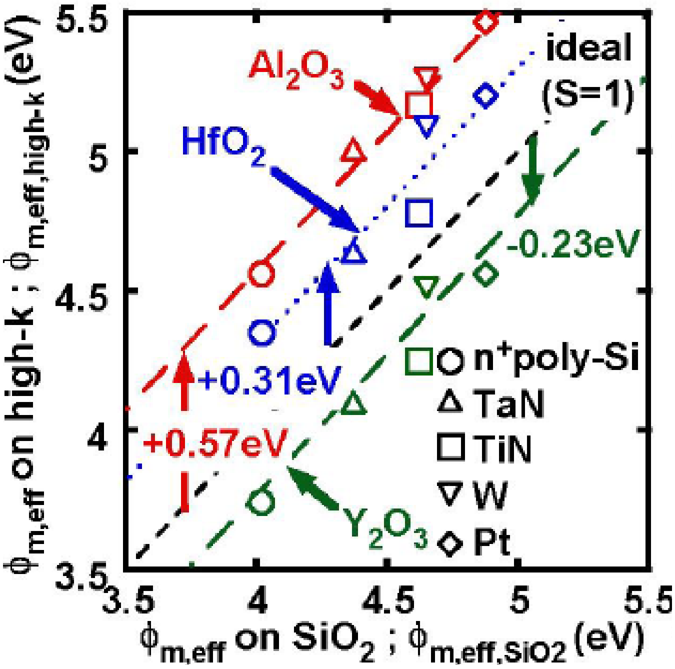

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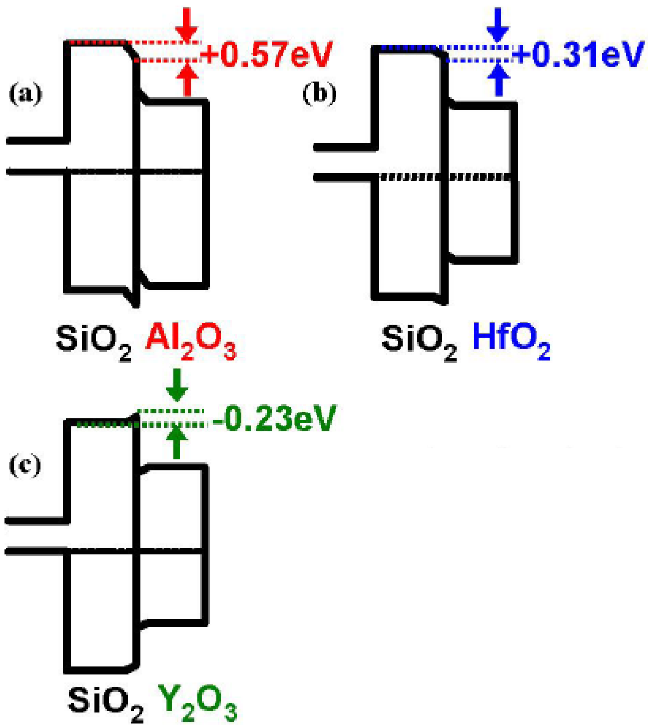

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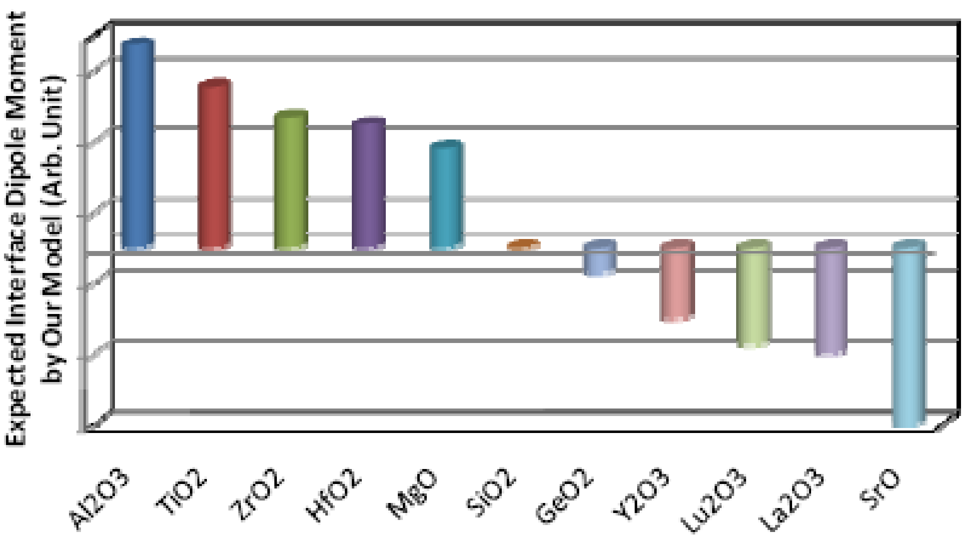


(c)

Fig. 2.1 (a) Relationship between EWF of metal gate along with n$^+$ poly-Si on high-k and SiO_2. (b)Schematic band diagram of Al_2O_3/SiO_2, HfO_2/SiO_2, and Y_2O_3/SiO_2 systems [2.8]. (c) Summary of the dipole moment formed at High-k/SiO_2 interface predicted by [2.12].

- RCA clean
- Thermal Oxide 35 Å
- MOCVD ultra thin dipole layer Al_2O_3&HfO_2
- LPCVD Si_3N_4 150 Å
- MOCVD ultra thin dipole layer Al_2O_3&HfO_2
- LPCVD SiO_2 150 Å
- Gate Al 4000 Å

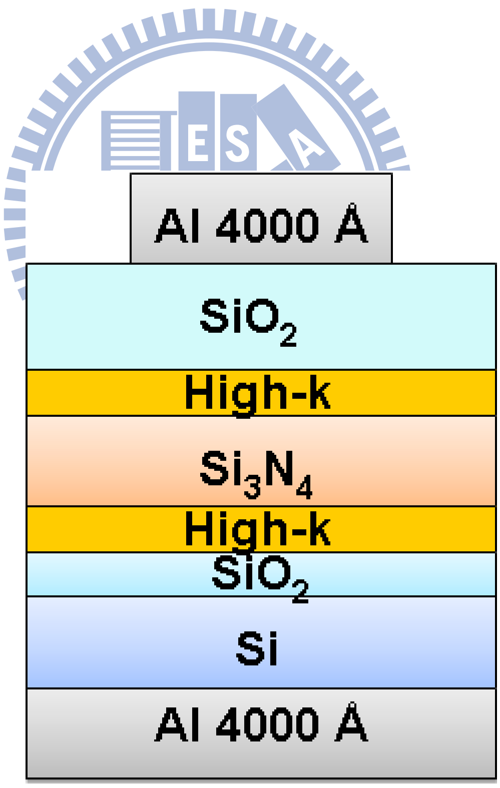


Fig 2.2 Schematic of conventional SONOS memory capacitors with interfacial dipole layer engineering.

- LOCOS isolation (Active region definition, P^+ Well ,Channel stop &anti punch through& V_T adjustment implant)
- Thermal Oxide 30 Å
- MOCVD Al_2O_3 10 Å
- MOCVD $HfSiO_x$ 120 Å
- RTA 950°C 60s
- LPCVD SiO_2 100A
- Deposition Poly-Si 2000 Å
- N^+ Source/Drain
- P^+ Body Contact
- Activation 950°C 30s
- Passivation
- Metallization

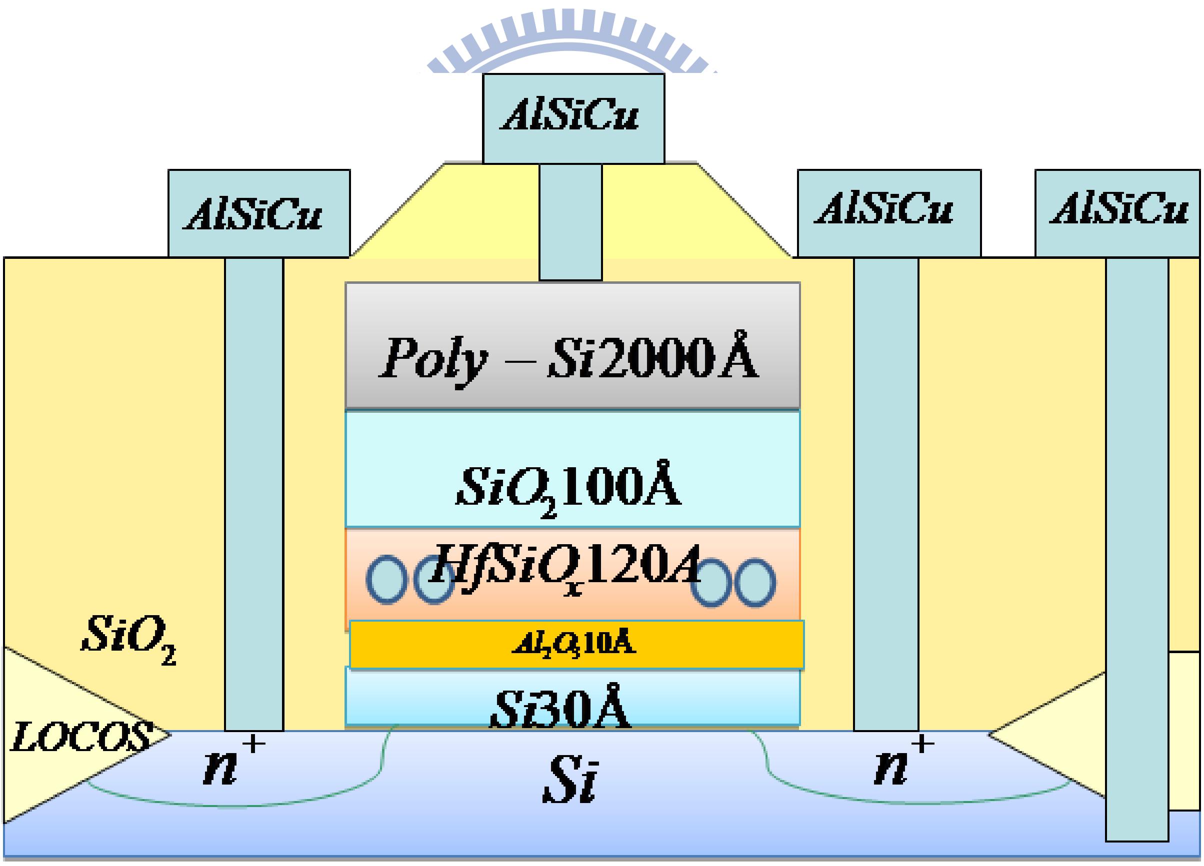
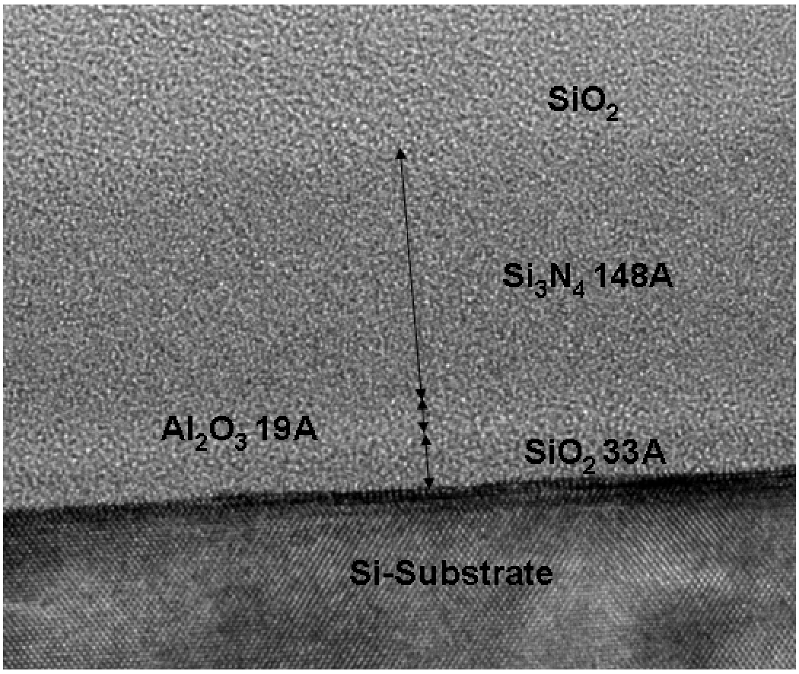
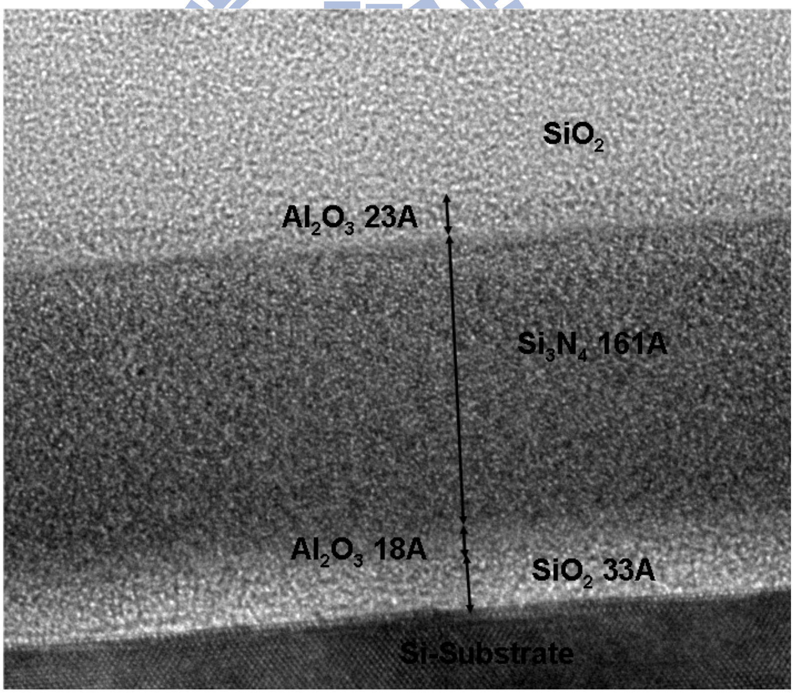


Fig 2.3 Schematic of HfO_2 nanocrystal flash memory structure with interfacial dipole layer engineering

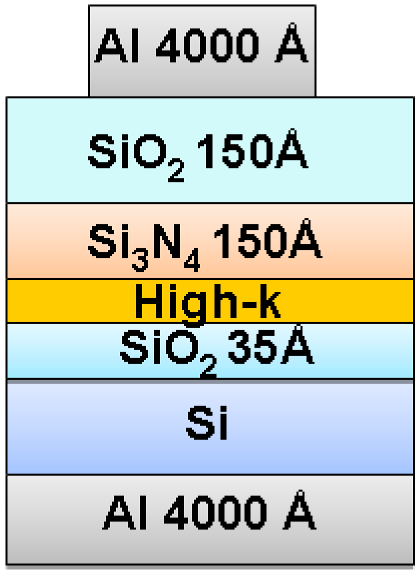


(a)

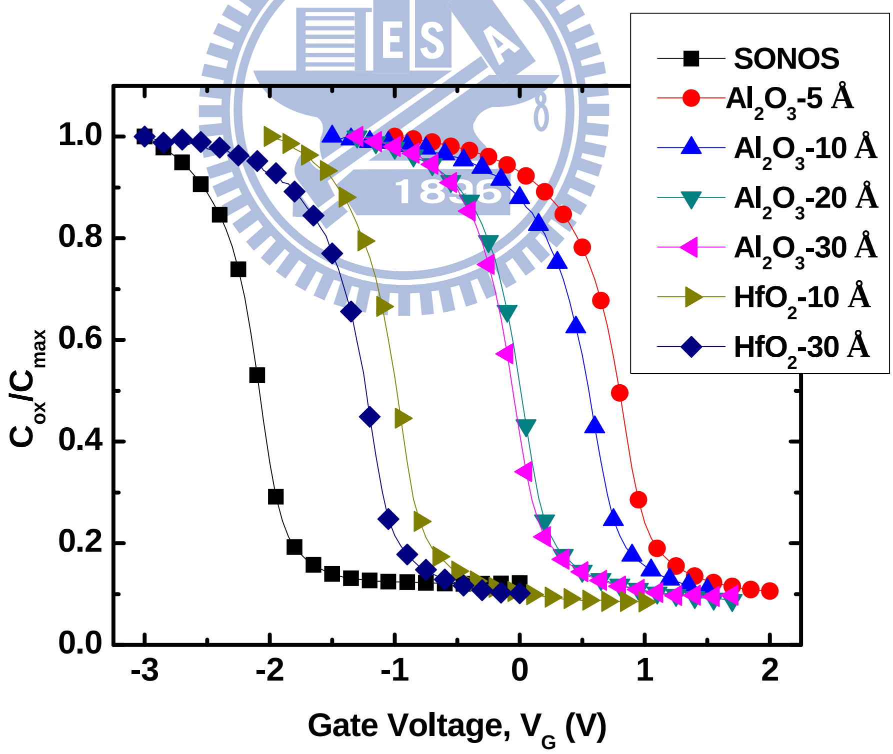


(b)

Fig 2.4 (a) Cross-sectional TEM image of $Si/SiO_2/Al_2O_3/Si_3N_4/SiO_2$. The ultra-thin Al_2O_3 layer is well formed upon the bottom SiO_2. (b) Cross-sectional TEM image of $Si/SiO_2/Al_2O_3/Si_3N_4/Al_2O_3/SiO_2$. The ultra-thin Al_2O_3 layer is well formed upon the bottom SiO_2 and Si_3N_4.

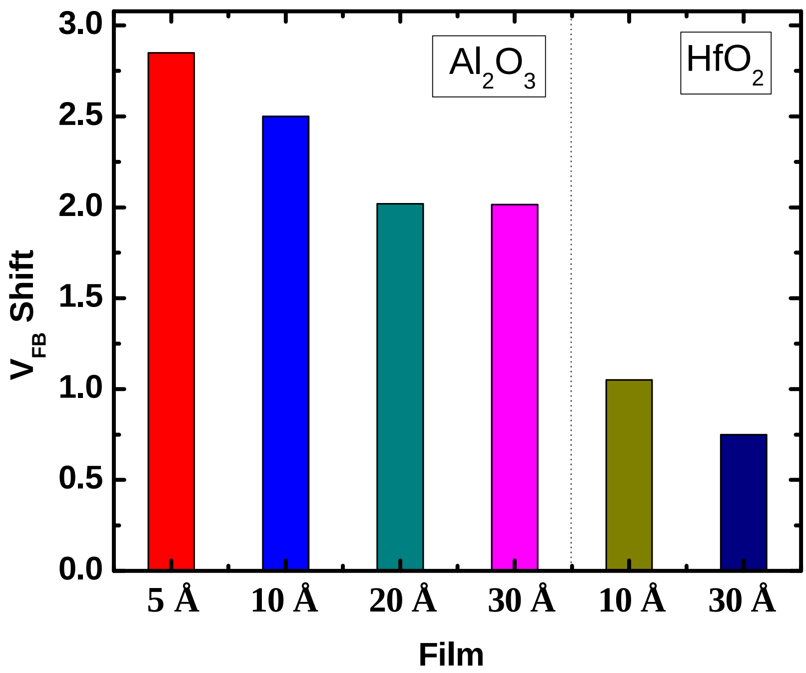


(a)

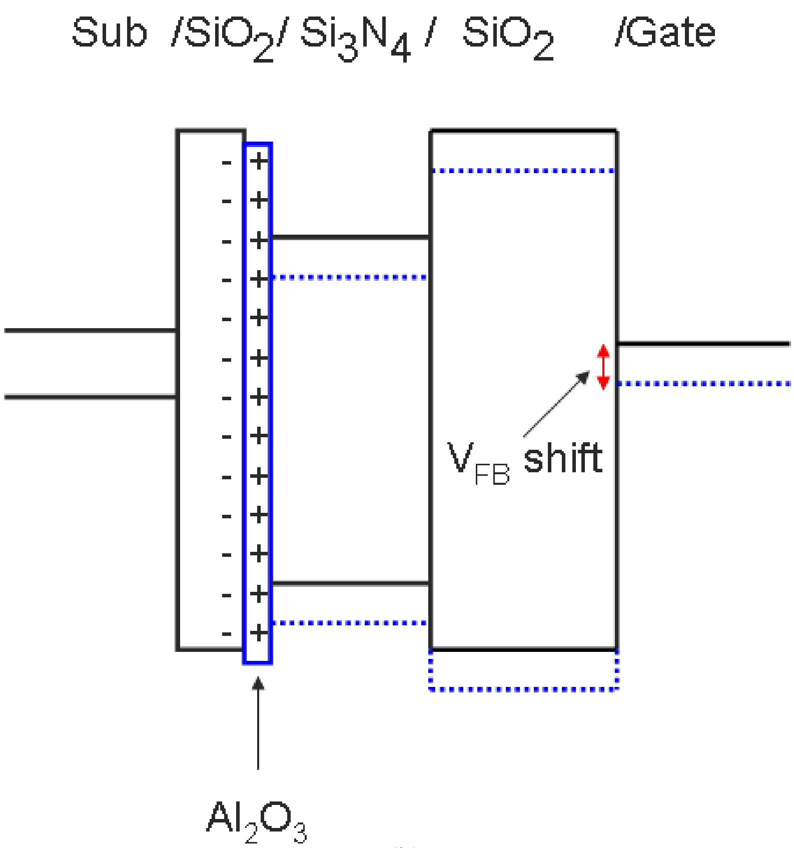


(b)

Fig 2.5 (a) Schematic of capacitor structure of discussion the influence of the dipole deposit between bottom oxide and nitride trapping layer and (b) their C-V characteristics with Al_2O_3 5 Å, 10 Å, 20 Å, 30 Å, HfO_2, 10 Å, and 20 Å.

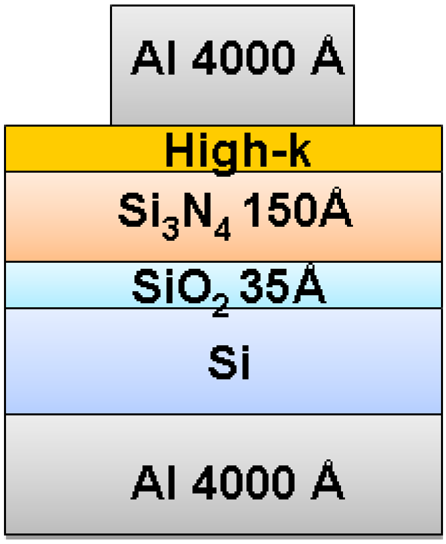


(a)

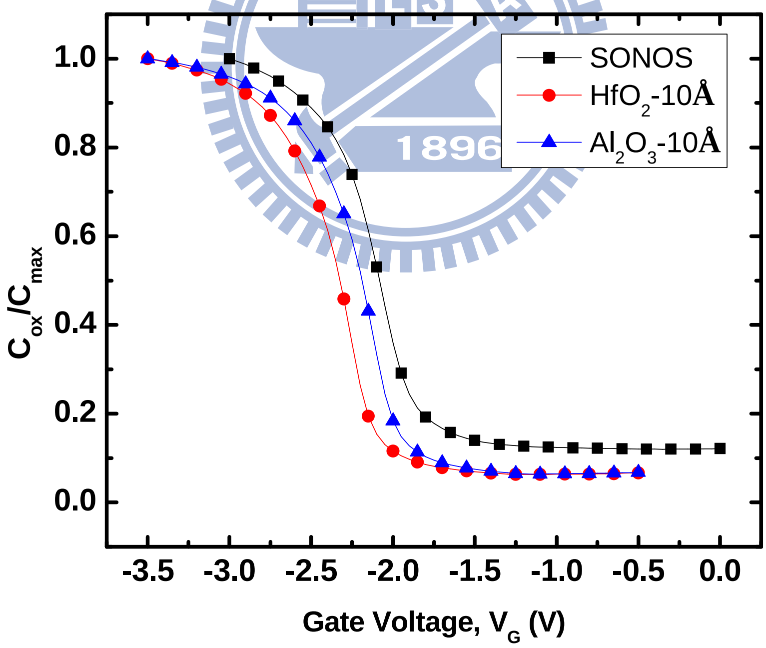


(b)

Fig 2.6 (a) The result of V_{FB} shift with interfacial deposit on bottom oxide in Figure 2.5(b). (b) The band diagram of SONOS-type capacitor with interfacial deposit on bottom oxide.

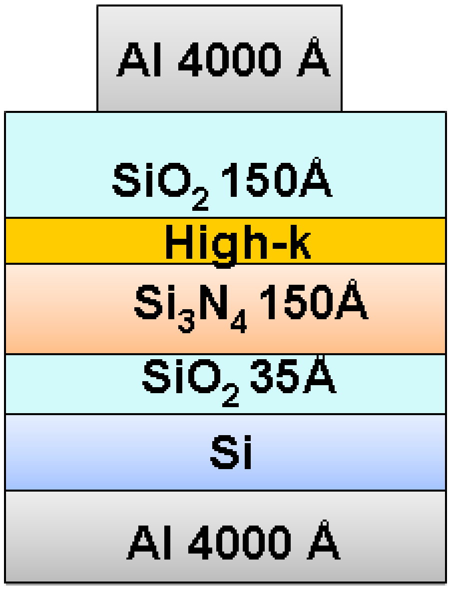


(a)

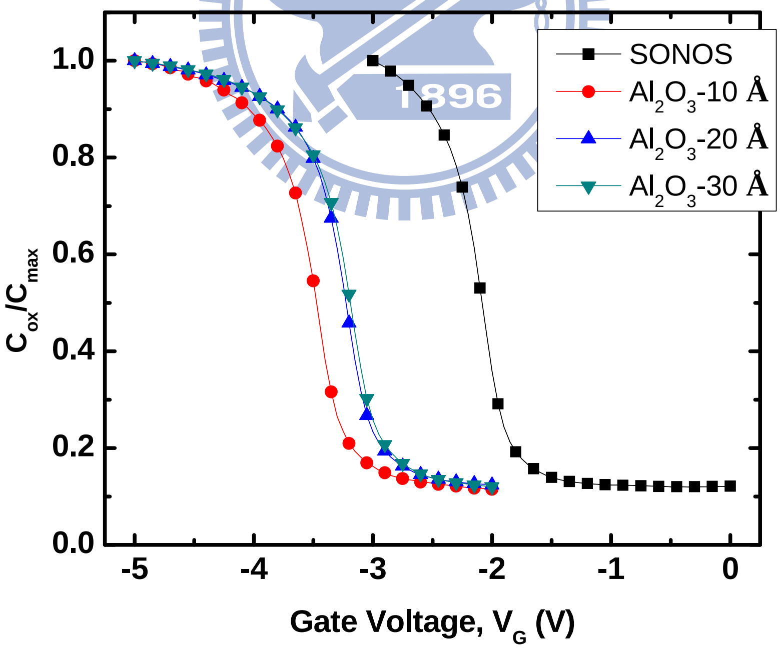


(b)

Fig 2.7 (a) Schematic of capacitor structure of discussion the influence of the dipole deposit on nitride trapping layer and (b) their C-V characteristics with Al_2O_3 10 Å and HfO_2 10 Å.

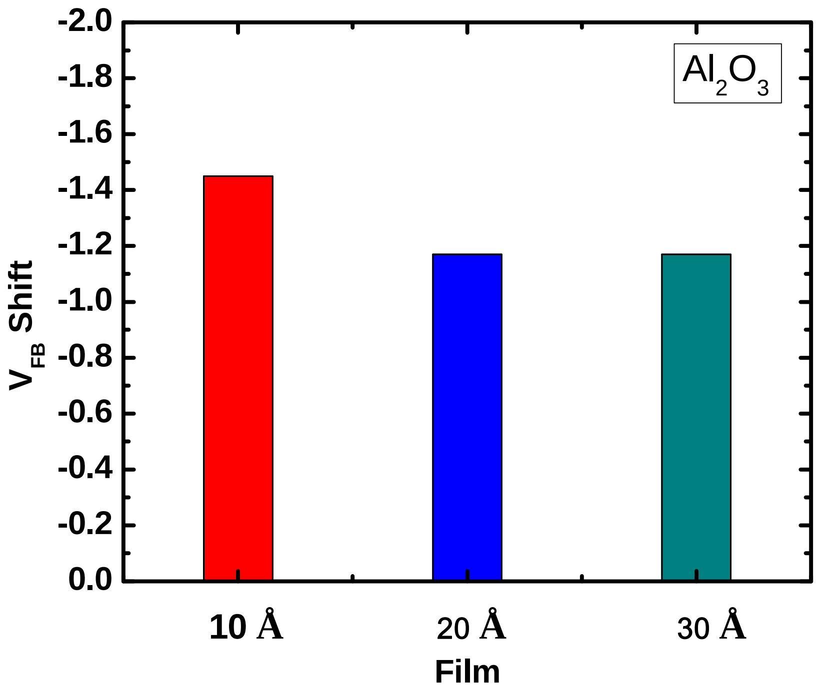


(a)

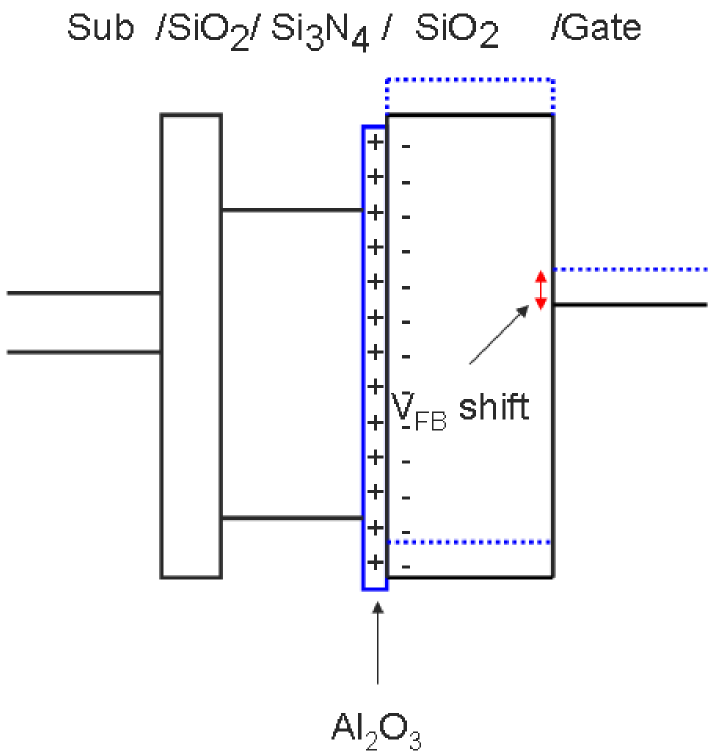


(b)

Fig 2.8 (a) Schematic of capacitor structure of discussion the influence of the dipole deposition between nitride layer and top oxide and (b) their C-V characteristics with Al_2O_3 10 Å, 20 Å, and 30 Å.

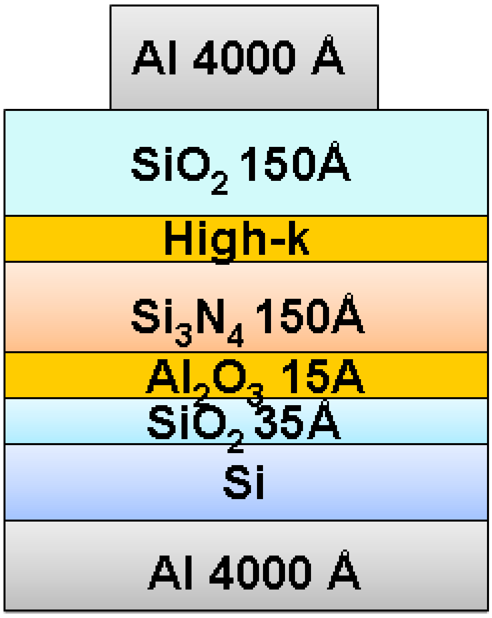


(a)

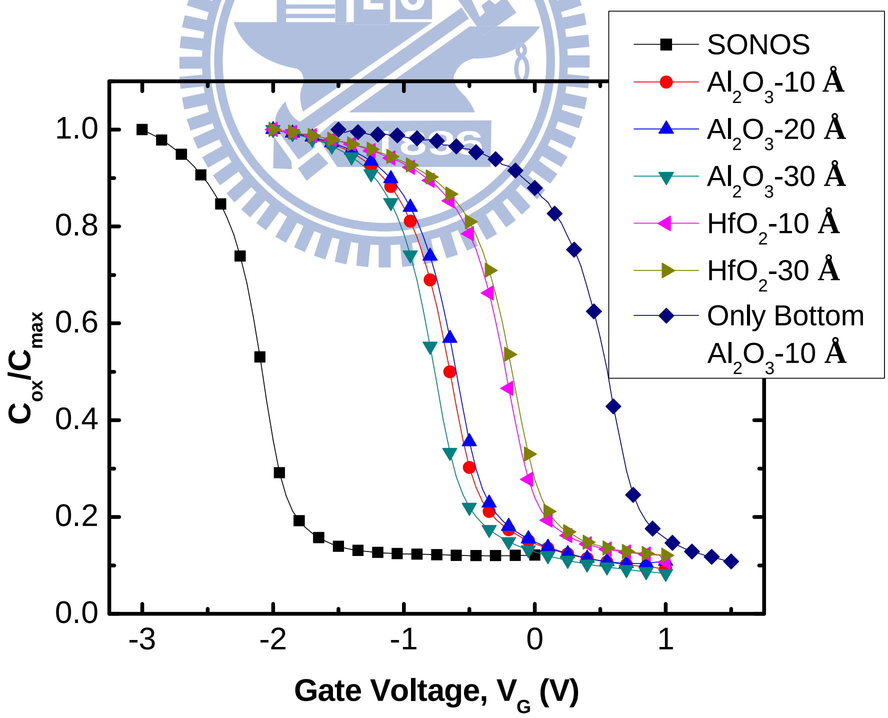


(b)

Fig 2.9 (a) The result of V_{FB} shift with interfacial deposit on nitride layer in Figure 2.8(b). (b) The band diagram of SONOS-type capacitor with interfacial deposit on nitride layer.



(a)



(b)

Fig 2.10 (a) Schematic of capacitor structure of discussion the influence of the double dipole layer deposition on bottom oxide and nitride layer and (b) their C-V characteristics with Al_2O_3 10 Å, 20 Å,30 Å, HfO_2,10 Å , and 30 Å on nitride layer.

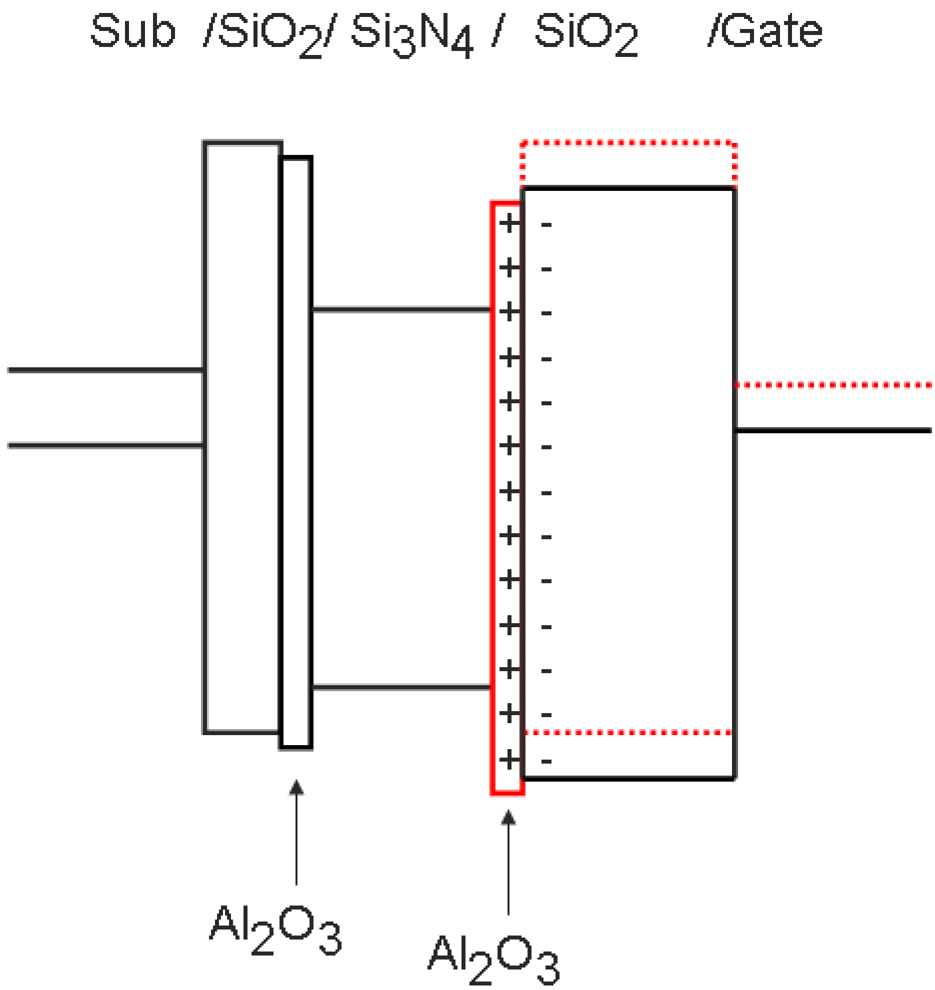


Fig 2.11 The band diagram of SONOS-type capacitor with interfacial deposit on bottom oxide and on nitride layer.

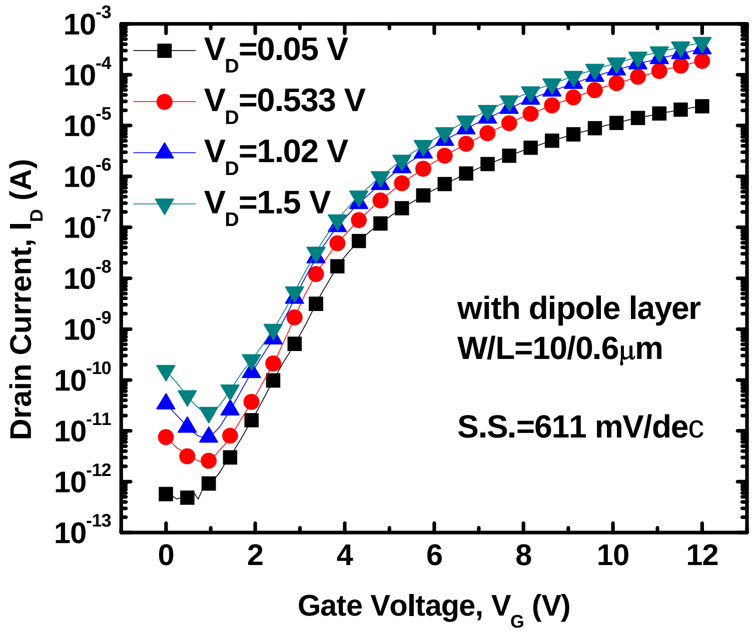
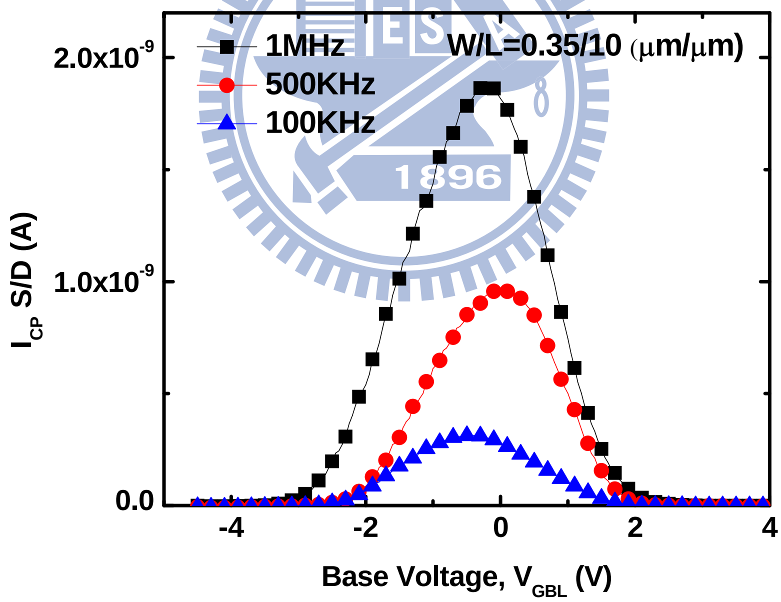


Fig 2.12 I_{DS}-V_{GS} curve of the nanocrystal flash memory with Al_2O_3 dipole layer engineering.



$$S.S. = 2.3\frac{kT}{q}\left(1+\frac{C_{dep}+C_{it}+C_{poly}}{C_{ox}}\right)$$

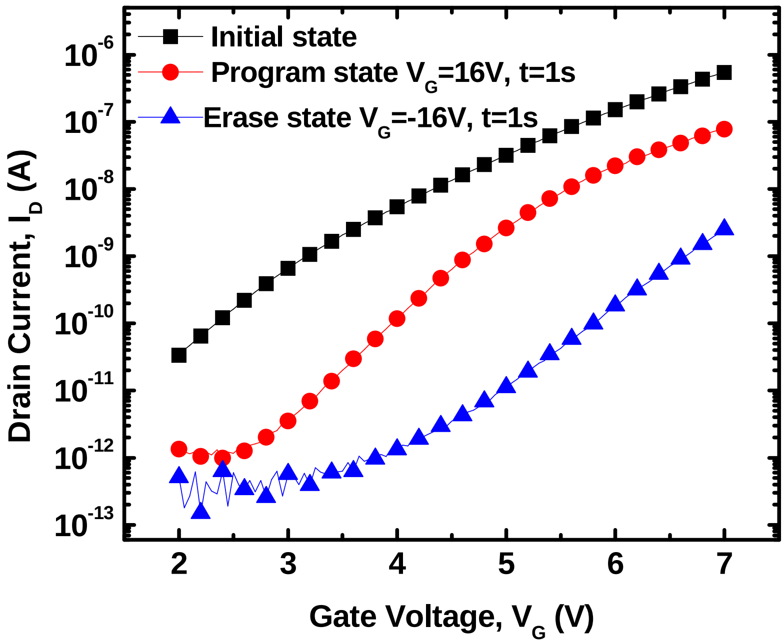
$$C_{ox} = 190 nF/cm^2$$

$$N_{sub} = 2\times10^{17} cm^{-3}, C_{dep} = 148 nF/cm^2$$

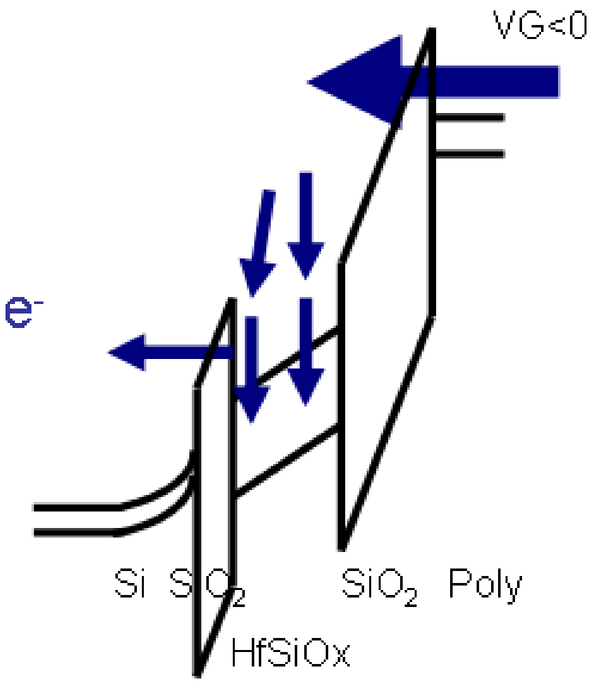
$$D_{it} = 4.02\times10^{11}, C_{it} = 64.3 nF/cm^2$$

$$S.S. \approx 126 mV/dec$$

Fig 2.13 Plots of I_{CP} vs V_{GBLl} for the HfO_2 nanocrystal memory cell with different frequency and the parameter after calculate.

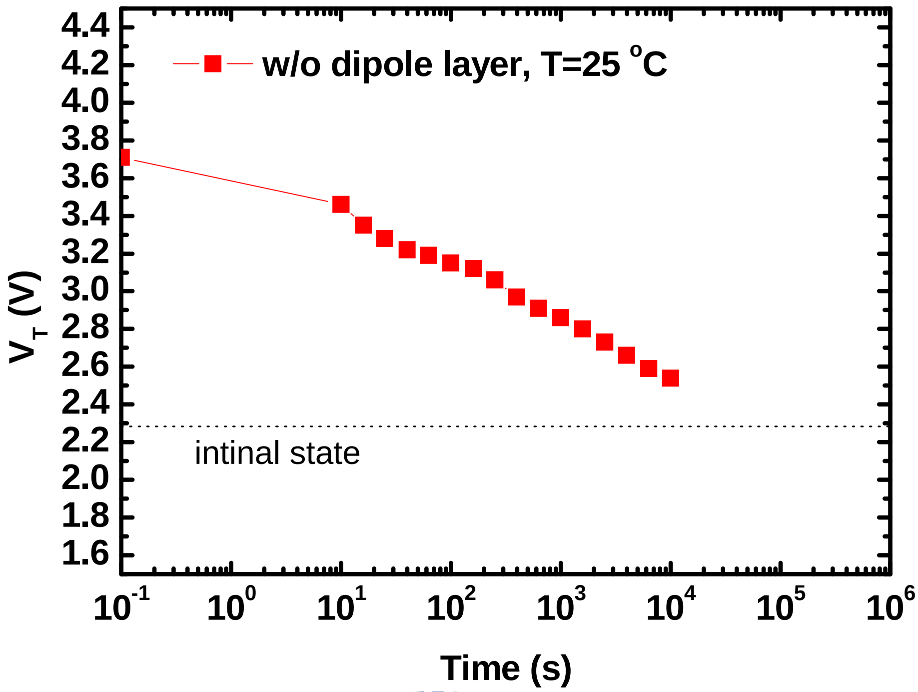


(a)

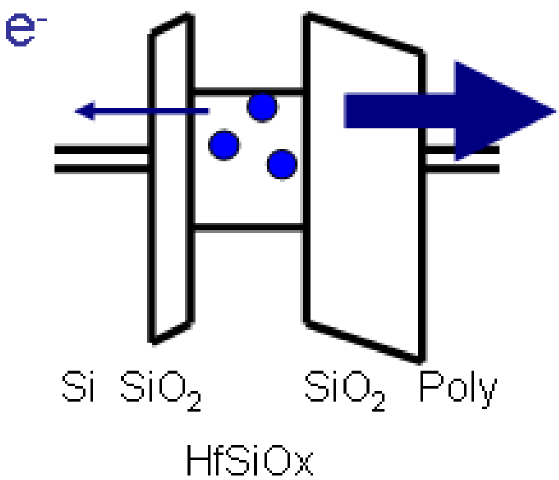


(b)

Fig 2.14 (a) I_{DS}-V_{GS} curve of the nanocrystal flash memory with programming time 1s and erasing time 1s. (b)The band diagram of nanocrystal memory at erasing operation and have seriously gate injection.



(a)



(b)

Fig 2.15 (a) Retention characteristics of nanocrystal flash memory at room temperature (T=25℃) with 10^4 second. (b) The band diagram of retention. The losing charge is mainly escape by blocking oxide not tunneling oxide.

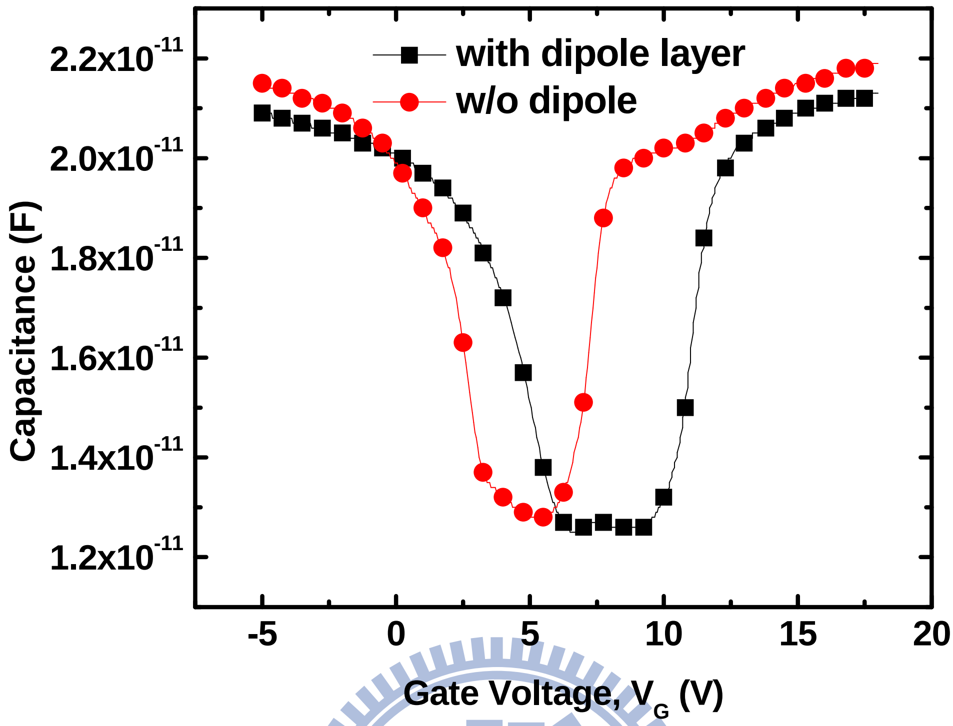


Fig 2.16 C-V characteristics of our nanocrystal and nanocrysta with dipole layer engineering flash memory.

Chapter 3

Characteristic of HfO_2 Nanocrystals Nonvolatile Flash Memory with High-k Blocking Layer

3.1 Introduction

Flash memory has been the subject of aggressive scaling during the past decade. The SONOS-type (Poly Si-Oxide-Nitride-Oxide-Silicon) structure memories, which include nitride and nanocrystal memories, have attracted much attention for their application [3.1-3.4] due to many advantages. In order to meet the performance requirements of future generation, one of the nearest major changes will concern the engineering of Interpoly Dielectric (IPD or we can say blocking layer) stack. The optimization of the blocking layer is necessary to avoid electron tunneling through the blocking oxide during the erase condition, which in turn causes an erased problem [3.5-3.6].

Since the high-k dielectric exhibits a significantly lower leakage current density for the relatively thinner effective oxide thickness, we can increase both the thickness and the electric field for the electric field for the tunnel oxide at the same operating voltage. Therefore, SONOS-type flash device with high-k blocking layer provides a faster P/E speed and longer data retention time [3.7-3.8]. But as we know, the higher permittivity the smaller energy band gap in general. For a example, HfO_2 has high permittivity (~25) and can increase the electric field for tunneling oxide, however, it is not appropriate blocking layer due to the small energy band gap (~5.2eV). On the contrary, Al_2O_3 offers the sufficient energy gap (~8) to block the hole and electron current with low permittivity (~9). The band diagrams are shown in **Figures (a), and (b)** .Therefore, how to choose the advantages of both is very important. In addition to, the thermal stability and trap free are important, too. Because the low thermal stability may cause to crystallize, and further result leakage current and trapping charge.

3.2 Experiment

A capacitor with blocking layer material as gate oxide are fabricated on a p-type, 20 ~ 30Ω cm, (100) 150-mm silicon substrate. After RCA clean, the 15nm Al_2O_3 and $HfAlO_x$ with pulse ratio Al: Hf= 3: 1 were deposited by MOCVD. The post deposition anneal with 950°C 30s embedded N_2. At last, we deposited Al as top and bottom electrode by thermal coater. The structure is shown in **Figure 3.2**

An example of the fabrication process of the HfO_2 nano-crystal nonvolatile memory devices is demonstrated by a LOCOS isolation process on a p-type, 20-30 Ω cm, (100) 150-mm silicon substrate. First, a 30 Å tunnel oxide was thermally grown at 800℃ in a horizontal furnace system. Next a 120 Å amorphous $HfSiO_x$ silicate layer was deposited by MOCVD. The samples were then subjected to RTA treatment in an N_2 ambient at 950° C for 1 min to convert the $HfSiO_x$ silicate film into the separated HfO_2 and SiO_2 phase. Their compositions were identified using X-ray photoelectron (XPS). A 100 Å Al_2O_3 and $HfAlO_x$ was then deposited through MOCVD. Subsequently, poly-Si deposition, gate patterning, n^+ source/drain (S/D) implantation, p^+ body implantation, activation 950℃ 30 second, and the remaining standard CMOS procedures were completed to fabricate the HfO_2 nano-crystal nonvolatile memory device. The nanocrystal flash memory structure is shown in **Figure 3.3**

3.3 Results and Discussion

3.3.1 Material Analysis of Al_2O_3 and $HfAlO_x$ Blocking Layer

First we use the MOS capacitor structure to analyze the material of blocking layer, such the **Figure 3.2** shows. Because our device have to endure the high temperature S/D annealing of 950℃ 30 second after gate dielectric deposition, we have to analyze whether it deteriorated or not after PDA. **Figures 3.4 (a), and (b)** illustrate the Current Density-Electric Field (J-E) characteristics of Al_2O_3 and HfAlO $_x$ (pulse ratio Al: Hf= 3 :1) 150 Å after PDA of 950℃ 30s embedded N_2. We can find out the leakage current of Al_2O_3 which is smaller than $HfAlO_x$ no matter it annealed or not, especially, when it operated at low field. Moreover, there is slight deterioration after PDA, but still within the acceptable range. In addition, the curve of $HfAlO_x$ have a peak in accumulation region at low field, and the leakage current is higher than the Al_2O_3 of the order of 1.5, we think this is caused by that there are some oxide trap making to Trap Assist Tunneling (TAT).

Figures 3 .5 (a), (b), (c), and (d), illustrates the C-V hysteresis of Al_2O_3 and $HfAlO_x$. The Al_2O_3 150Å nearly have no hysteresis. In contrast, the HfAlO $_x$ have hysteresis of 0.3V and 0.5V at without PDA and after PDA with 950℃ 30 second. Perhaps the discussion of hysteresis is not accurate to high-k oxide trap owing to the hysteresis may be caused by the interfacial layer. However, the hysteresis of $HfAlO_x$ is really larger than Al_2O_3; this may be an evidence of that the $HfAlO_x$ film existed higher oxide defect than Al_2O_3.

Figure 3.6 illustrates the analysis of XPS of $HAlO_x$ with pulse ratio Al: Hf= 3: 1 which contain the Intensity-Binding Energy characteristic of Al, Hf, and O. After calculation we can obtain the composition ratio of Al: Hf with pulse of Al: Hf= 7: 1 , 3:1, 1:1, and 5:1. The result was sorted out in **Table 3-1** and we have atomic ratio of Al: Hf with 94%: 6%, 87%: 13%, 64%: 36%, and 17%: 83%. The composition ratio of Al: Hf with 87%: 13% is we used in this experiment.

Finally, we can use the analysis of XRD to know weather it crystallized or not after PDA 950℃ 30s embedded N_2, such as **Figures 3.7 (a), (b), (c), (d), (e), and (f)** show. The thermal stability of Al_2O_3 is higher than HfO_2, so the higher compositions of Hf the easier crystallize. The pulse ratio of Al: Hf = 3: 1 we chose is the highest composition of Hf and didn't crystallize after high temperature annealing among these conditions. Therefore, we chose this composition of $HfAlO_x$ in our nancrystal flash memory.

3.3.2 Characteristics of Program/Erase Operation

Figure 3.8 illustrates I_{DS}-V_{GS} curve of the nanocrystal flash memory with $HfAlO_x$ as blocking layer. Because the process condition is the same of chapter 2, the subthreshold swing (S.S.) is still poor which is equal to 560 mV/dec. **Figure 3.9** illustrates I_{DS}-V_{GS} curve of initial state, programming state at V_G=16V 1us and erasing state with at V_G=-16V 10ms. The figure shows our nanocrystal flash memory with a high programming speed which can be achieved with a memory of about 2.5V in V_G=16V 1us. The elemental composition of trapping layer of $HfSiO_x$ we chose which average elemental of Hf: Si is about 1:1 to get the HfO_2 nanocrystal dots after 950℃ 60 second.

Figure 3.10 illustrates programming characteristic as a function of pulse width for different FN-tunneling operation condition. Source, drain, and substrate terminals are biased at 0V. The V_T shift is defined as the threshold voltage change of the device between programmed and erased states. We find out from this figure that the programming speed of $HfAlO_x$ is faster than Al_2O_3 due to its higher permittivity, and the sample of $HfAlO_x$ has excellent program speed at the V_G=16 operation. Meanwhile, **Fig 3.11** displays the erasing characteristics as a function of pulse width for different operation condition. Again, we find that the erasing speed of $HfAlO_x$ is faster than Al_2O_3 due to its higher permittivity.

3.3.3 Transient Phenomenon of Erasing Operation

Figure 3.12 (a) illustrates I_{DS}-V_{GS} curve of initial state, programming state with V_G=16V 1us, erasing state with V_G=-16V 100ms and a append I_{DS}-V_{GS} curve at last. The append I_{DS}-V_{GS} curve was after erasing operation immediately. We find out that the append curve have visible negative V_T shift compare with erasing state and reach the initial state at last. Next we change the conditions of erasing time to 1ms and follow the same action as **Figure 3.12 (a)**. Then **Figure 3.12 (b)** illustrates I_{DS}-V_{GS} curve of initial state, programming state with V_G=16V 1us, erasing state with V_G=-16V 1ms, first append I_{DS}-V_{GS} curve and second append I_{DS}-V_{GS} curve at last. We still find the first append curve have visible negative V_T shift compare with erasing state, but the shift is smaller than the erasing condition of 100ms. Then the second append I_{DS}-V_{GS} curve is almost equal to the first append I_{DS}-V_{GS} curve. The I_{DS}-V_{GS} has transient phenomenon after erase operation and stability after append I_{DS}-V_{GS} curve. In addition, the longer erase times the larger negative V_T shift. The phenomenon didn't happen in the sample of blocking layer with Al_2O_3. As to why this transient phenomenon exists, we consider it due to the charge trapping in the $HfAlO_x$.

The **Figures 3.13 (a), (b) and (c)** illustrate the speculation of our. In **Figure 3.13 (a),** the memory is programmed and storing electron in the trapping layer after FN programming operation. Then we erase the memory with FN erasing operation, such as the **Figure 3.13(b)** shows. In **Figure 3.13(b)**, the memory is erasing the trapping charge to substrate and at the same time, the electron is trapped in blocking layer from gate injection current due to the trapping state in $HfAlO_x$. Therefore, the much bigger V_T we obtain owing to the charge store in blocking layer. Then, when start the I_{DS}-V_{GS} curve to detect the erase state, the charge is back to gate due to the electric field from substrate to gate, such as the figure the **Figure 3.13(c)** shows. Then the V_T for append I_{DS}-V_{GS} is much smaller than erase state.

3.3.4 Data Retention

The retention characteristics of our nanocrystal flash memory with Al_2O_3 and $HfAlO_x$ as blocking layer at room temperature (T=25℃) are illustrated in **Figures 3.14(a) and (b).** For sample of Al_2O_3, it is results in about 0.13V (~6%) memory window loss for 10^4 second retention time at room temperature in the initial window with 2.3 V. Then for sample of

$HfAlO_x$, it is results in about 0.18V (~9%) memory window loss for 10^4 second retention time at room temperature. The **Figure 3.14(c)** shows the result of normalized V_T shit, the Al_2O_3 is better than $HfAlO_x$ due to the higher energy bandgap. Subsequently, the retention characteristics with Al_2O_3 and $HfAlO_x$ as blocking layer at high temperature (T=125℃) are illustrated in **Figures 3.15 (a) and (b)**. The sample of Al_2O_3 still maintain good retention characteristics, it is results in about 11% memory window loss for 10^4 second retention time. In contrast, the sample of $HfAlO_x$ has very poor retention characteristics due to TAT obvious occur in high temperature condition, it is results in about 56% memory window loss for 10^4 second retention time. This result also verifies that there are many defects in $HfAO_x$ layer.

3.3.5 Endurance

Figures 3.16 (a), (b), and (c) show the endurance characteristics with the sample of Al_2O_3 and $HfAlO_x$. From this figure, the individual threshold voltage shift becomes visible after 10^4 program/erase cycles. The high enough P/E cycles make this high-k blocking structure of HfO_2 nanocrystal memory applicable nonvolatile memory devices.

3.4 Summary

In this chapter, we investigate the HfO_2 nanocrystal memory with Al_2O_3 and $HfAlO_x$ as blocking layer. At first, we analyze the leakage current characteristics of Al_2O_3 and $HfAlO_x$ film after S/D annealing condition treatment. The qualities of Al_2O_3 still maintain excellent characteristics with low leakage current, no C-V hysteresis, and without crystallization after annealing. The $HfAlO_x$ also has low leakage in high field and without crystallization after annealing, but higher leakage current than Al_2O_3 at low field. This show the TAT phenomenon and indicate there are some defects in $HfAlO_x$. Subsequently we use Al_2O_3 and $HfAlO_x$ as blocking layer applying in HfO_2 nanocrystal memory. We find the sample of $HfAlO_x$ appear the excellent programming speed which have memory of about2.5V at programming time of 1 μs. The sample of HfAlOx shows better programming and erasing speed than A_2lO_3. However, there is transient phenomenon at erasing operation in the sample of $HfAlO_x$ due to the presence of defects for our speculation. The sample of Al_2O_3 show good retention at room temperature and high temperature of 125℃. The sample of $HfAlO_x$ also shows good retention at room temperature but much poor retention at high temperature of 125℃.. It is also due to the presence of defects causing TAT. Finally after analysis of endurance, both the sample of Al_2O_3 and $HfAlO_x$ have good characteristic after 10^4 cycles.

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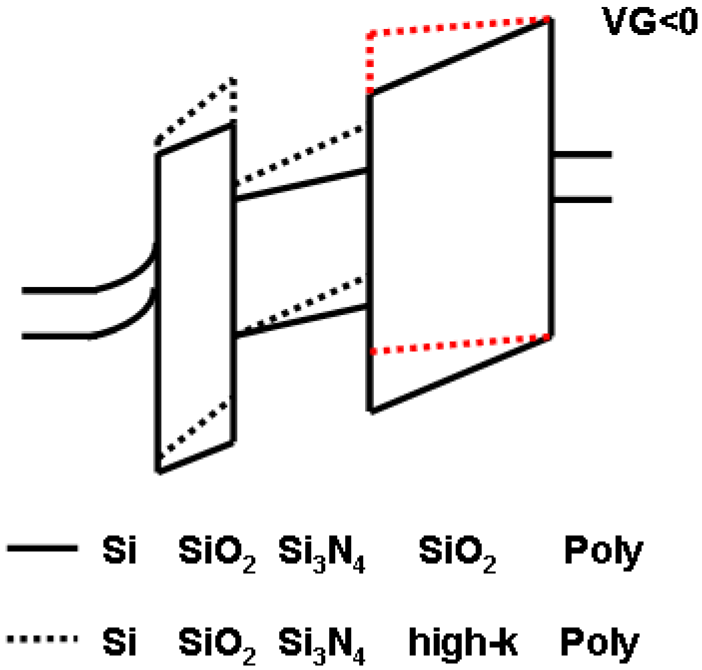
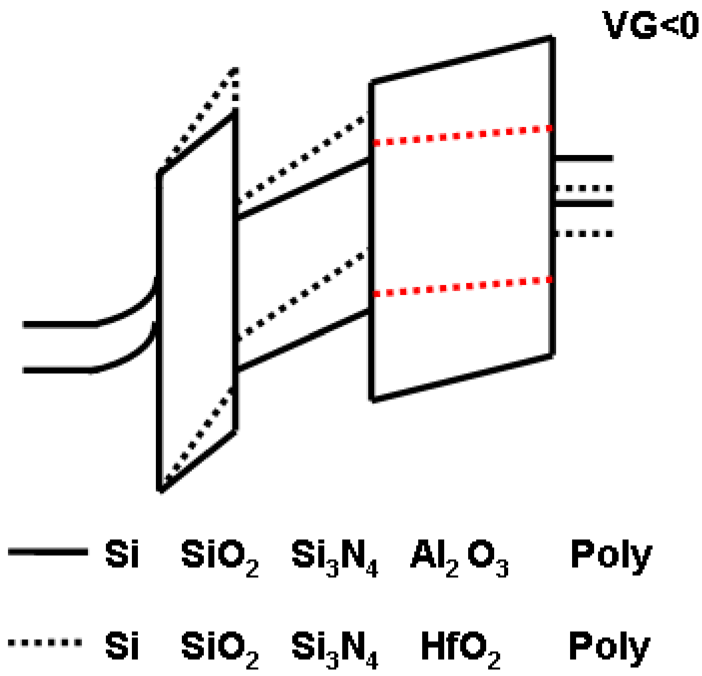


(a)



(b)

Fig 3.1 (a) The band diagram of SONOS-type memory with different primitive but equal bandgap material as blocking layer at negative gate voltage. (b) The band diagram of SONOS-type memory with Al_2O_3 and HfO_2 as blocking layer at negative gate voltage.

- **RCA clean**
- **MOCVD Al_2O_3&$HfAlO_x$ 150Å**
- **Post deposition anneal 950℃ 30s**
- **Gate Al 4000A**

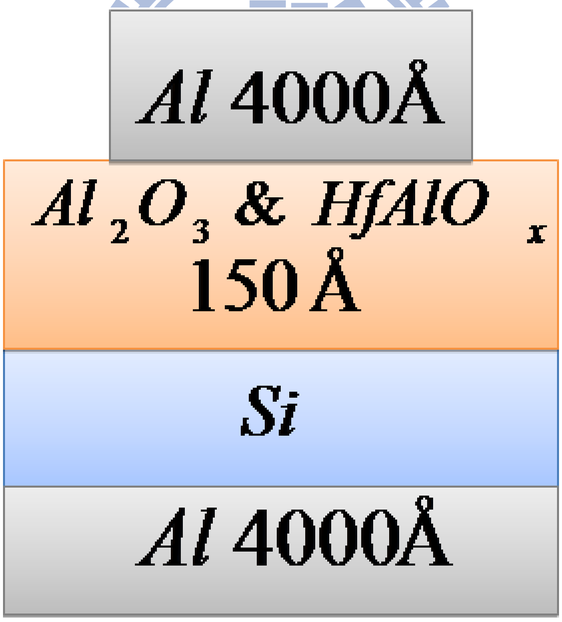


Fig 3.2 Schematic of MOS capacitors with Al_2O_3 and $HfAlO_x$.

- LOCOS isolation (Active region definition, P^+ Well ,Channel stop &anti punch through& V_T adjustment implant)
- Thermal Oxide 30Å
- MOCVD $HfSiO_x$ 120 Å
- RTA 950 °C 60s
- MOCVD Al_2O_3 & $HfAlO_x$ 100 Å
- Deposition In Situate Poly-Si 2000 Å
- N^+ Source/Drain
- P^+ Body Contact
- Activation 950 °C 30s
- Passivation
- Metallization

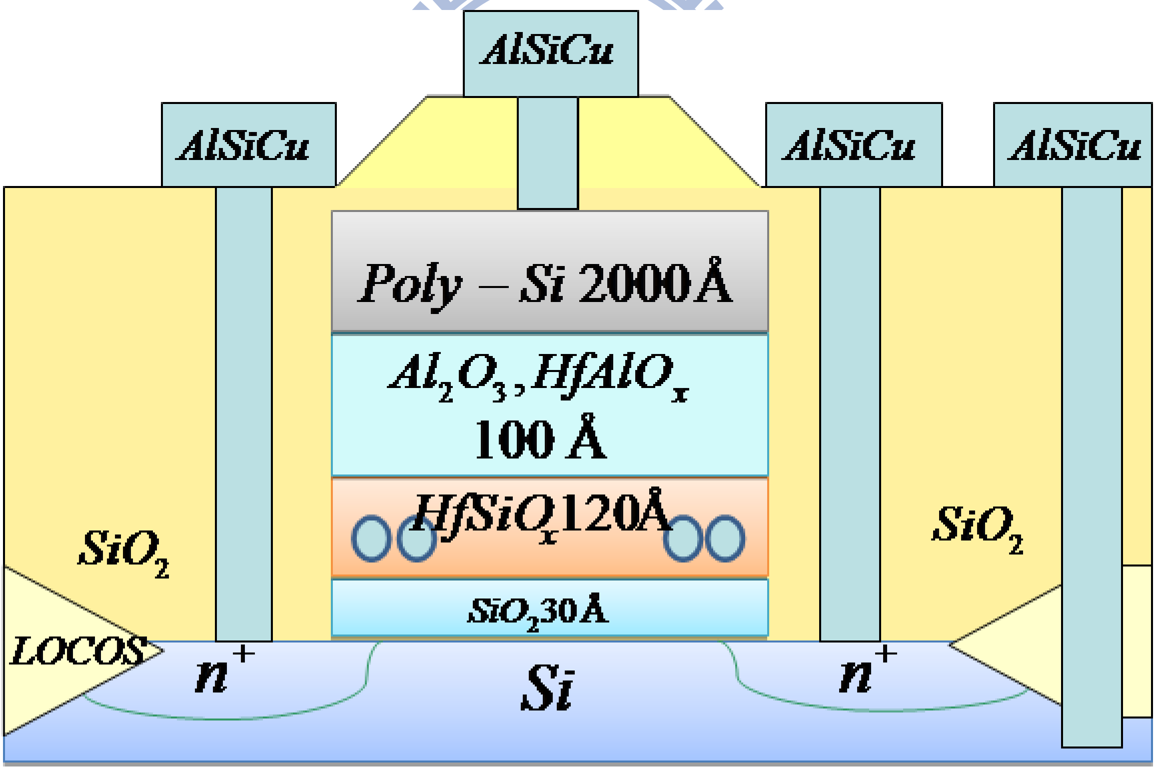
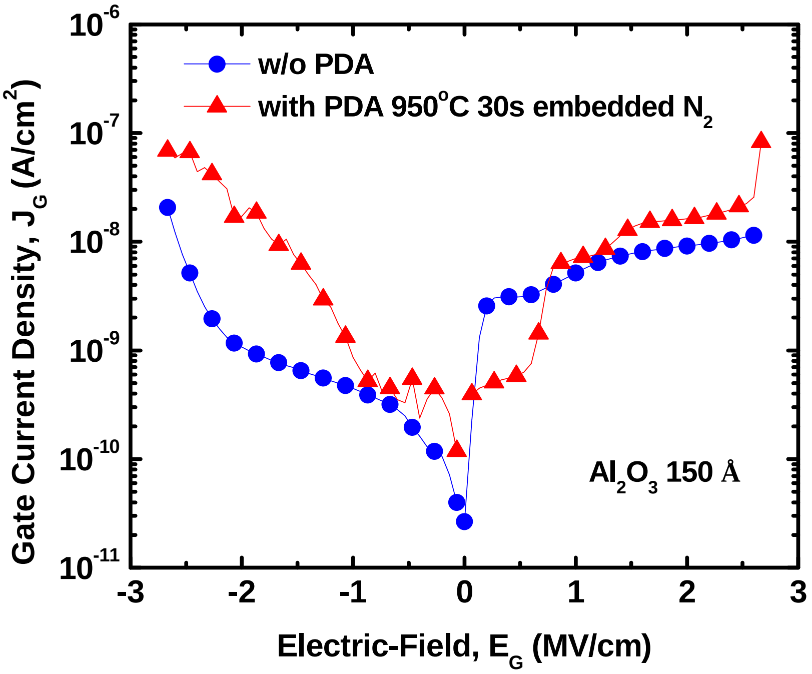
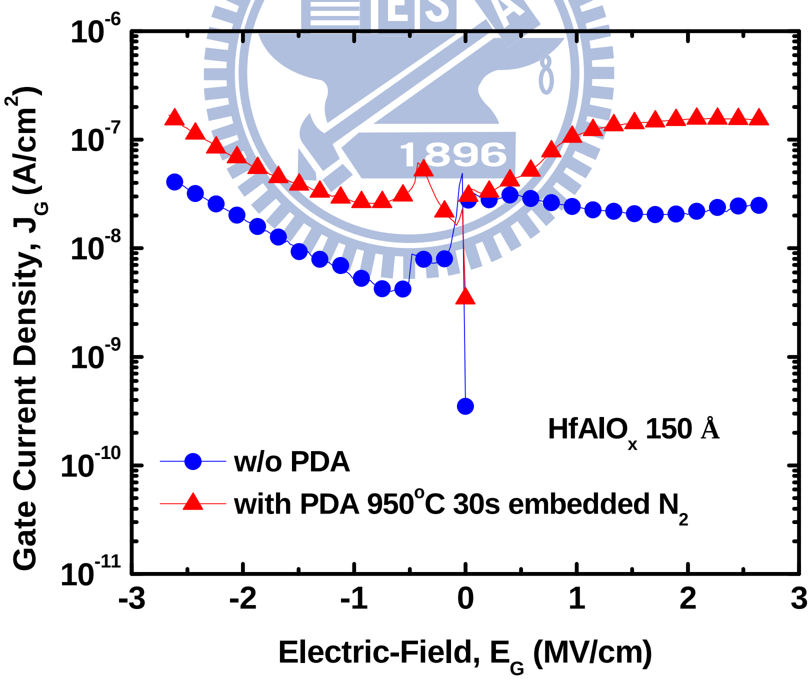


Fig 3.3 Schematic of HfO_2 nanocrystal flash memory structure with Al_2O_3 and $HfAlO_x$ as blocking layer.

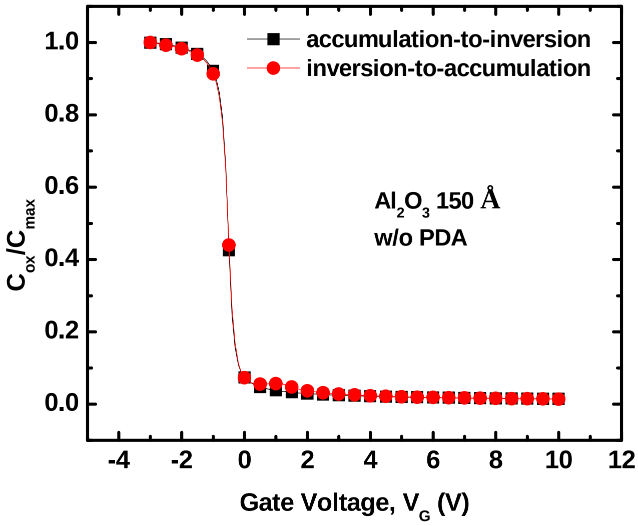


(a)

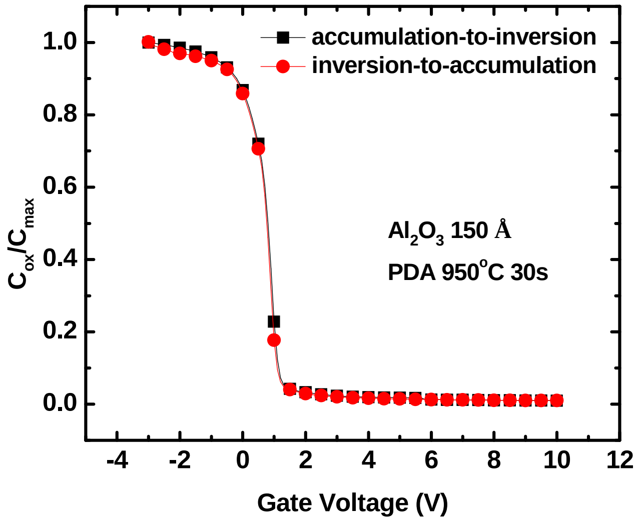


(b)

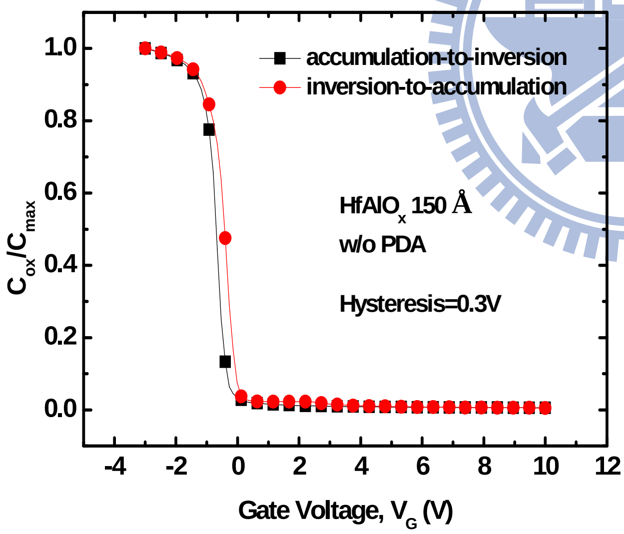
Fig 3.4 (a) The MOS capacitor Current Density-Electric Field (J-E) characteristics of Al_2O_3 and (b) $HfAlO_x$ without PDA and with PDA of 950℃ 30s embedded N_2.



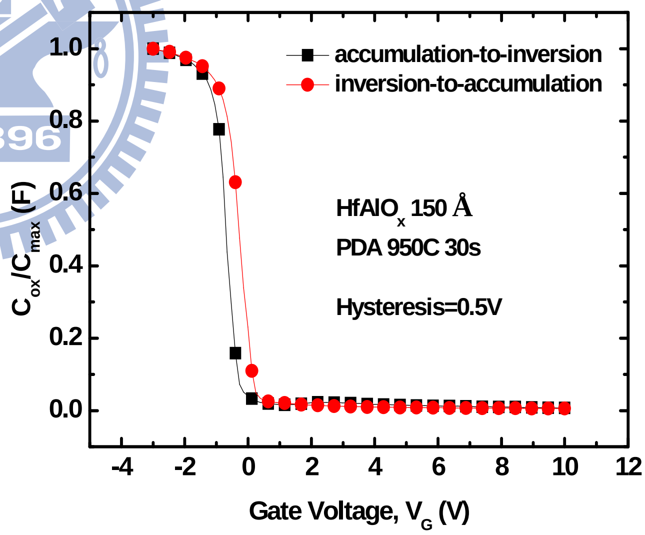
(a)



(b)



(b)



(d)

Fig 3.5 (a) The MOS capacitor C-V hysteresis characteristics of Al_2O_3 without PDA and (b) with PDA of 950℃ 30s embedded N_2. (c) The MOS capacitor C-V hysteresis characteristics of $HfAlO_x$ without PDA and (d) with PDA of 950℃ 30s embedded N_2.

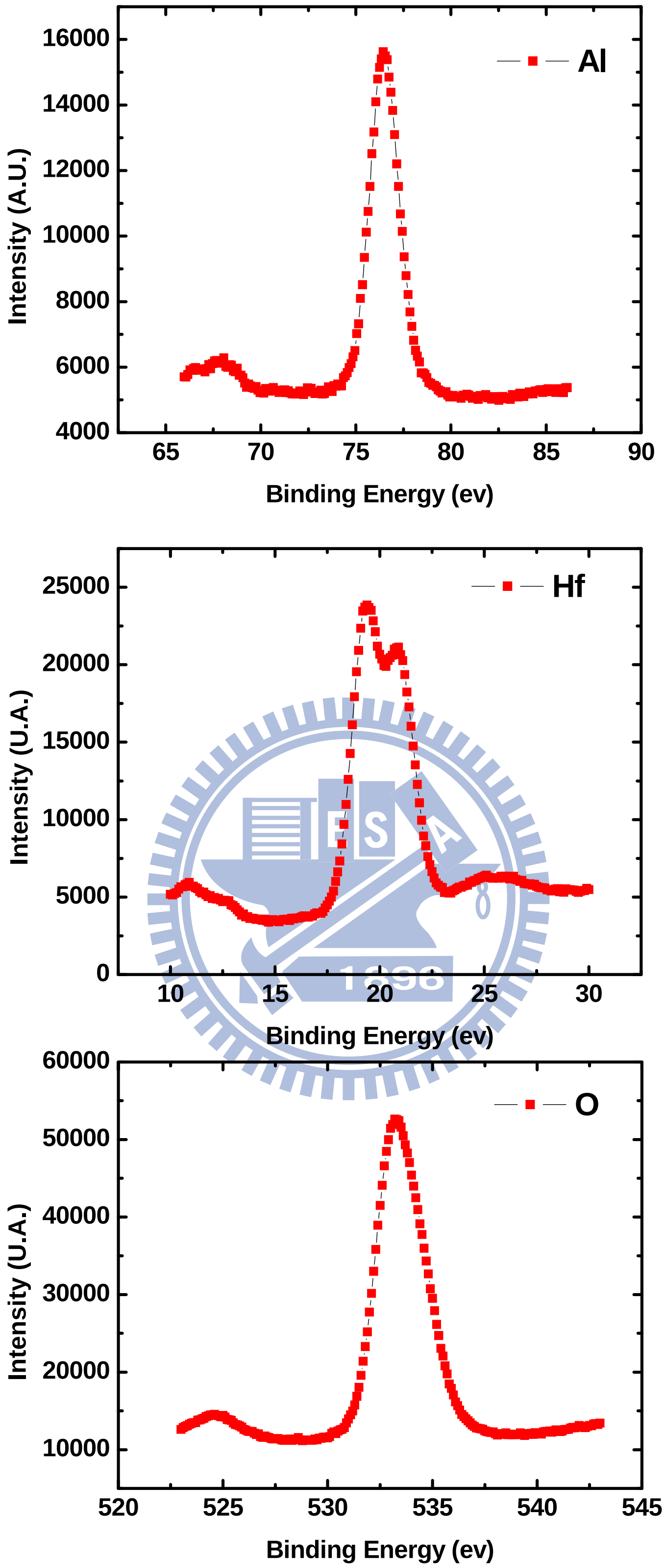


Fig 3.6 The analysis of XPS of $HAlO_x$ film with pulse ratio Al: Hf= 3: 1 which contain the Intensity-Binding Energy characteristic of Al, Hf, and O.

Pulse ratio	Al (%)	Hf (%)	O(%)	Al: Hf (%)
Al:Hf=7:1	39.84	2.46	57.7	94: 6
Al:Hf=3:1	36.54	5.22	58.24	87: 13
Al:Hf=1:1	24.8	13.99	61.21	64: 36
Al:Hf=1:5	6.01	29.2	64.79	17: 83

Table 3-1 After calculation, we can obtain the composition ratio of Al: Hf with different pulse ratio of Al: Hf= 7: 1 , 3:1, 1:1, and 5:1 in this table.

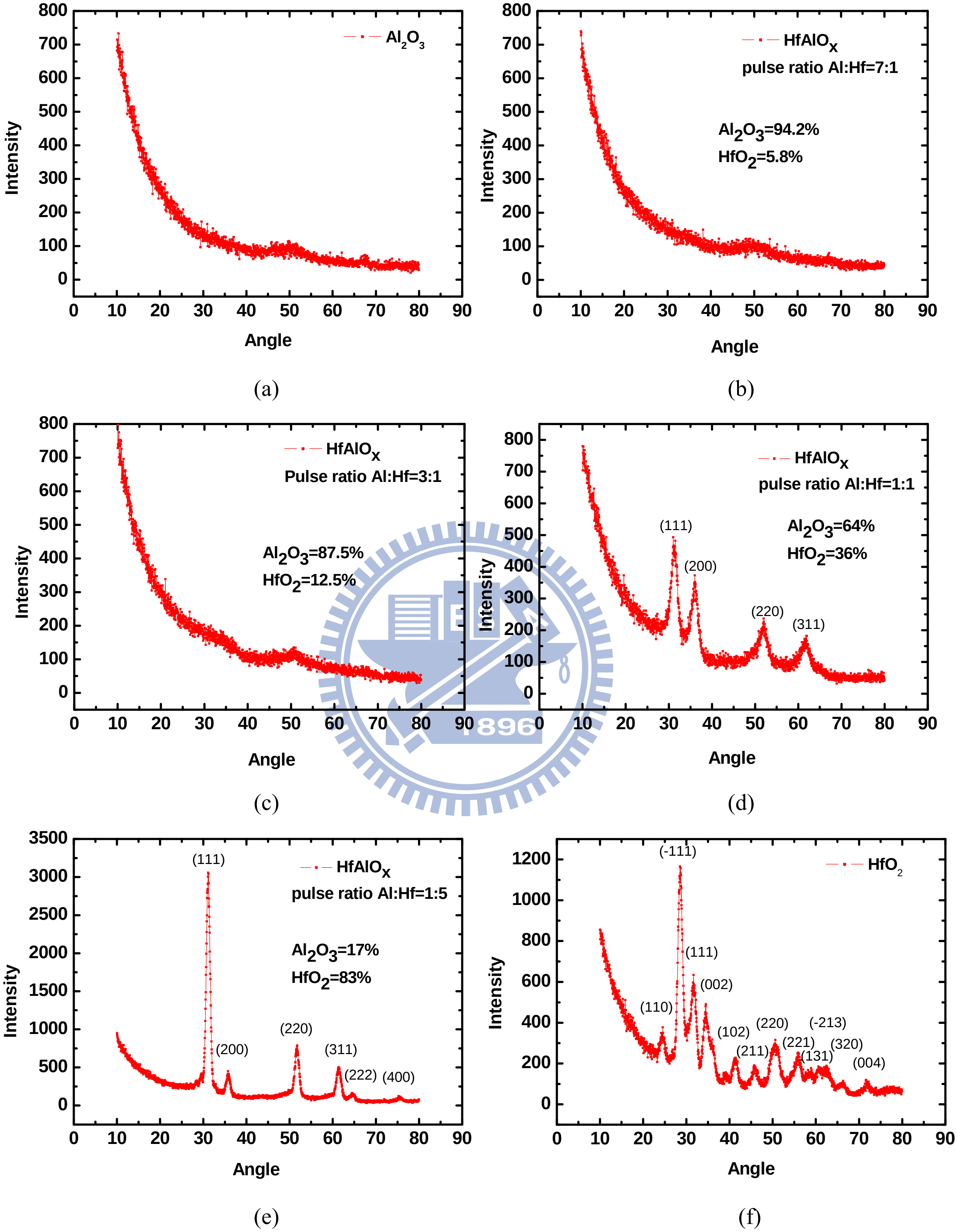


Fig 3.7 The analysis of XRD of (a) Al_2O_3, (f) HfO_2, and (b), (c), (e), (d), $HfAlO_x$ after 950℃ 30 second PDA treatment.

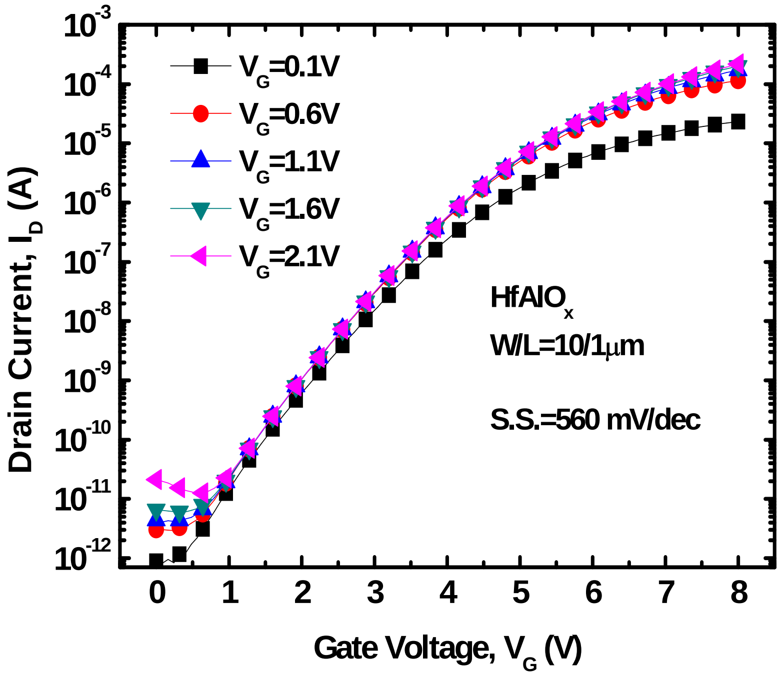


Fig 3.8 I_{DS}-V_{GS} curve of the nanocrystal flash memory with $HfAlO_x$ as blocking layer.

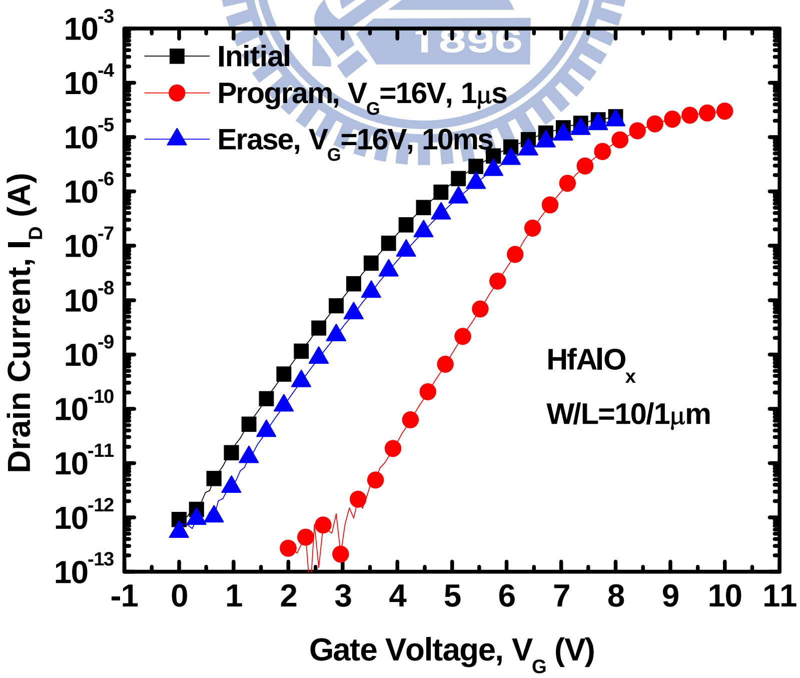


Fig 3.9 I_{DS}-V_{GS} curve of initial state, programming state with VG=16V 1us and erasing state with V_G=-16V 10ms.

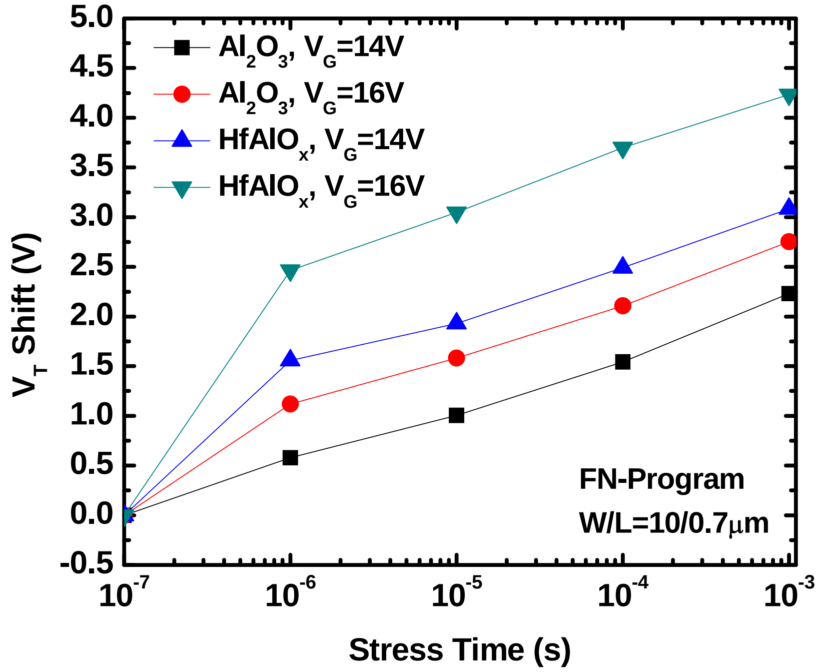


Fig 3.10 Programming characteristic of our nanocrystal memory as a function pulse width for different FN-tunneling operation condition.

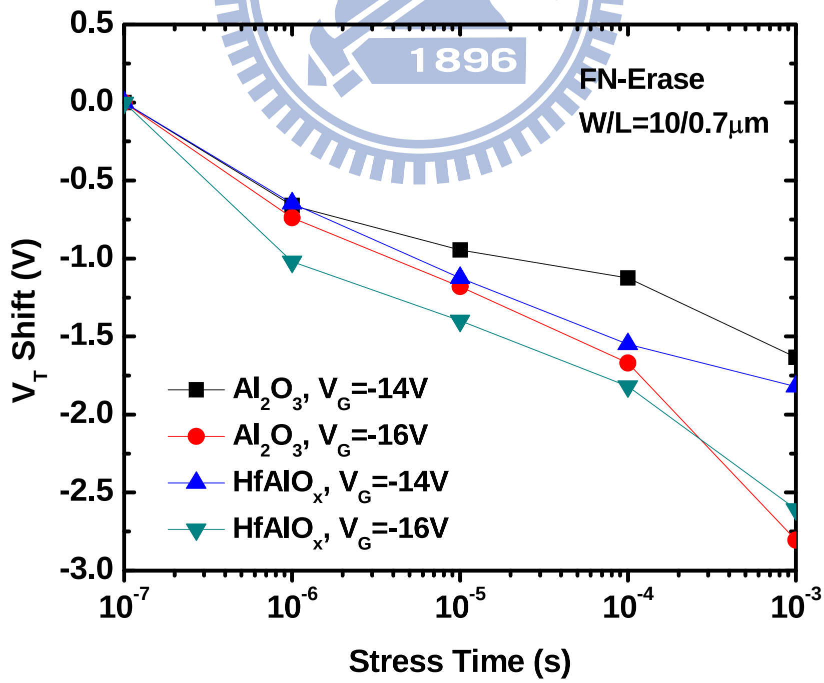
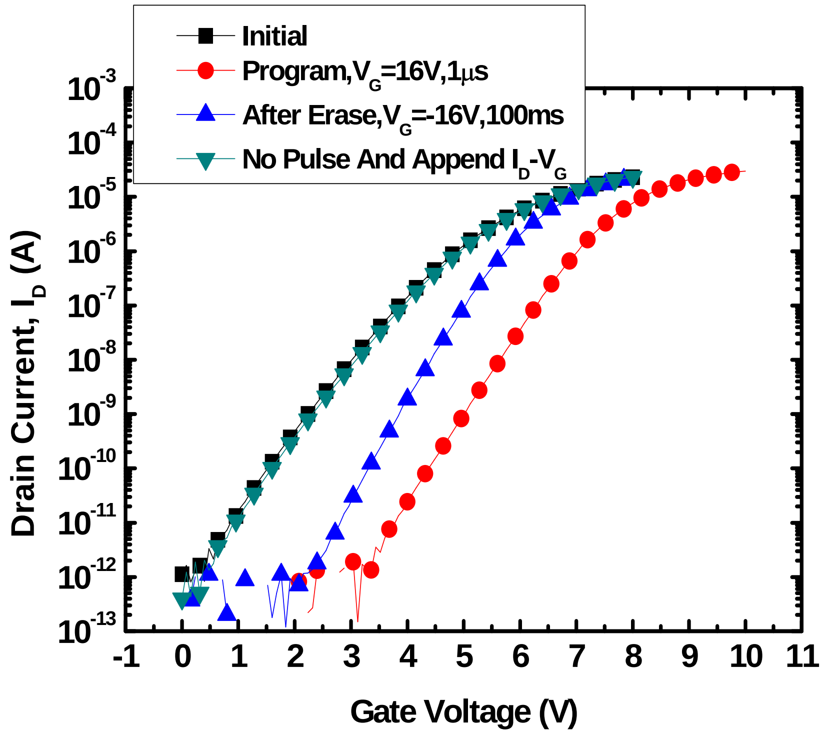
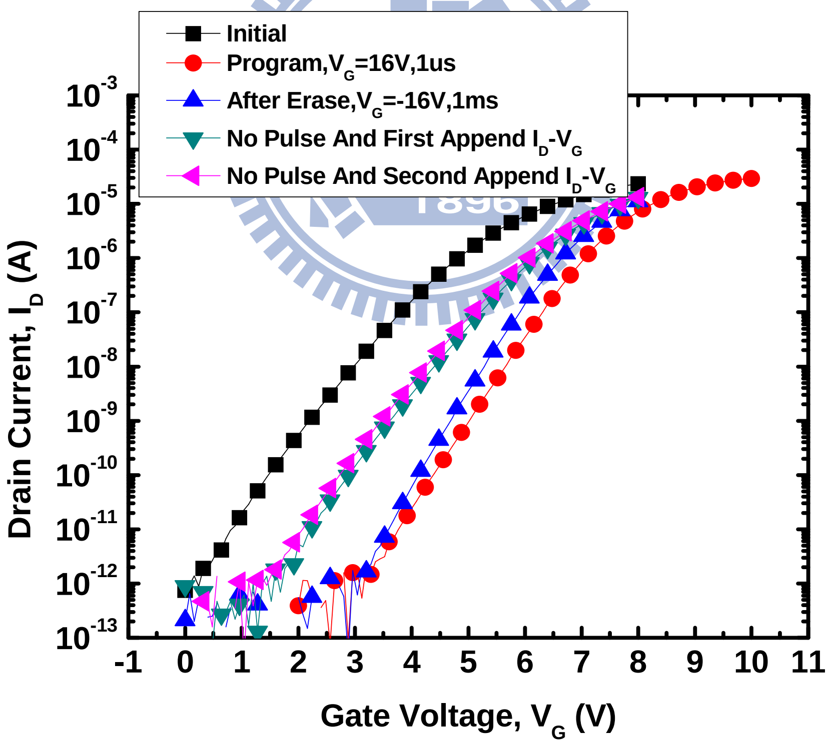


Fig 3.11 Erasing characteristic of our nanocrystal memory as a function pulse width for different FN-tunneling operation condition

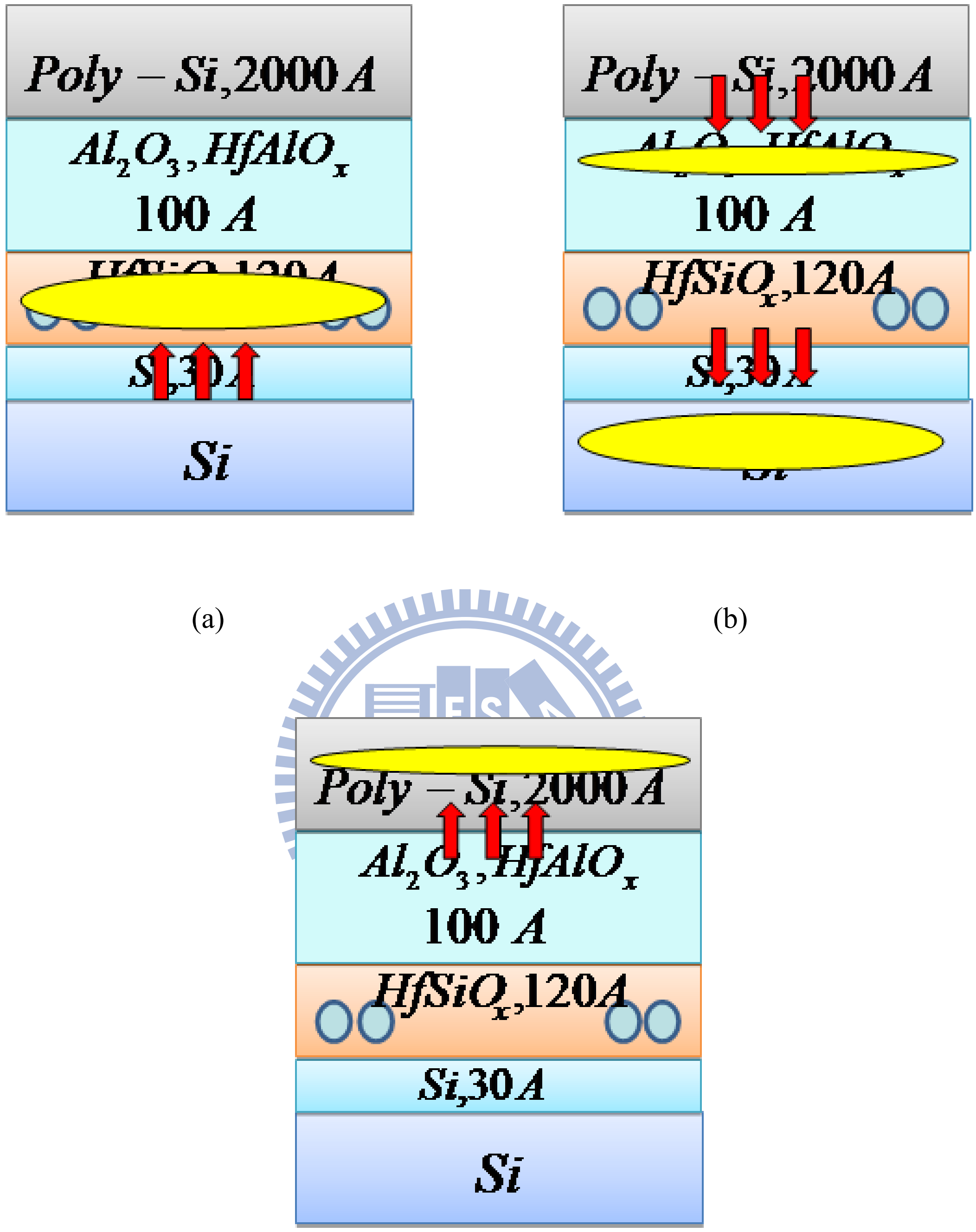


(a)



(b)

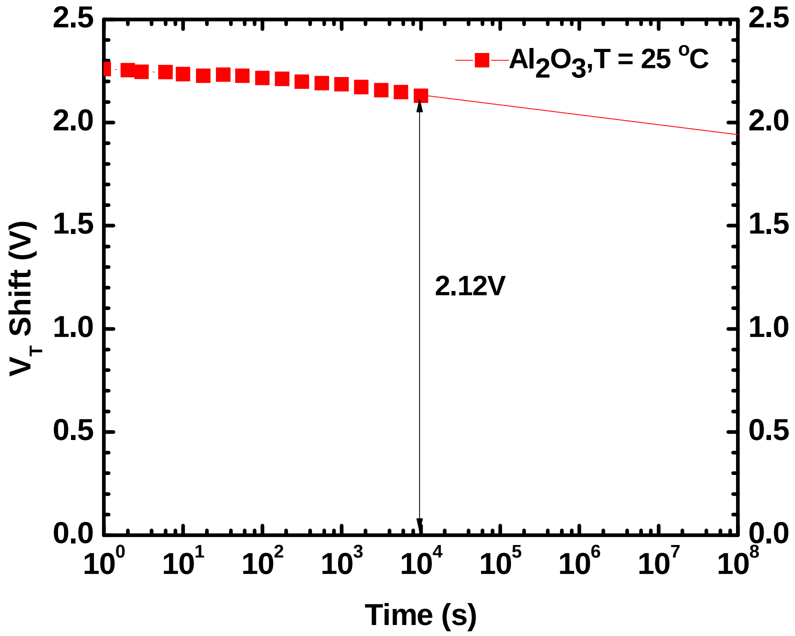
Fig 3.12 I_{DS}-V_{GS} curve of initial state, programming state with V_G=16V 1us and erasing state with V_G=-16V 100ms and (b) 1ms to discuss the transient phenomenon.



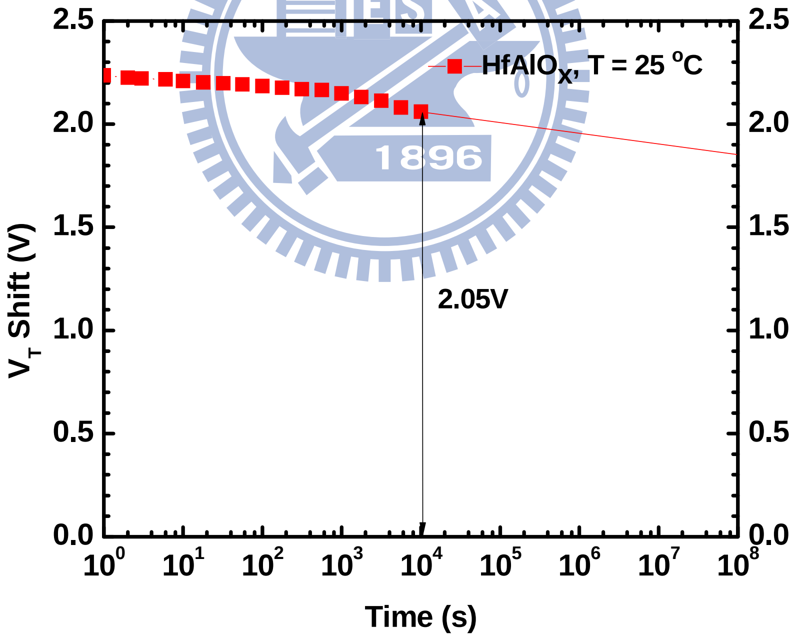
(a) (b)

(c)

Fig 3.13 (a), (b) and (c) The reason of the transient phenomenon for our speculation. (a) After the program pulse. (b)After erase pulse. (c) After Sweep I_{DS}-V_{GS} to detect erasing state.

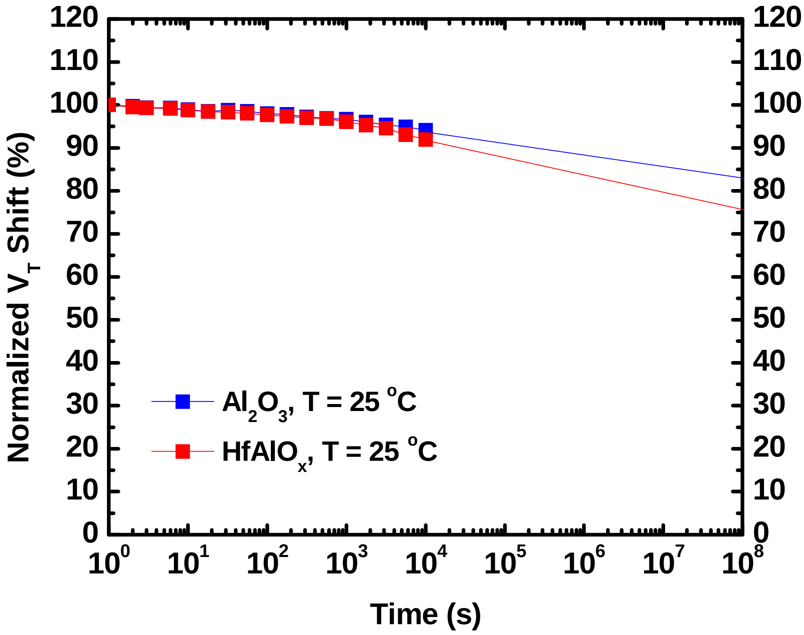


(a)



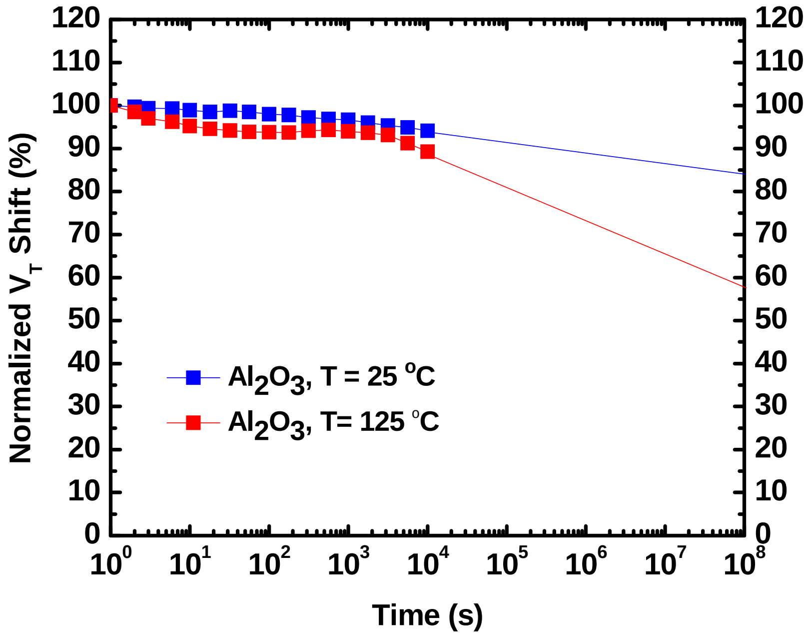
(b)

Fig 3.14 (a) Retention characteristics of our nanocrystal flash memory with Al_2O_3 and (b) $HfAlO_x$ as blocking layer at room temperature (T=25℃).

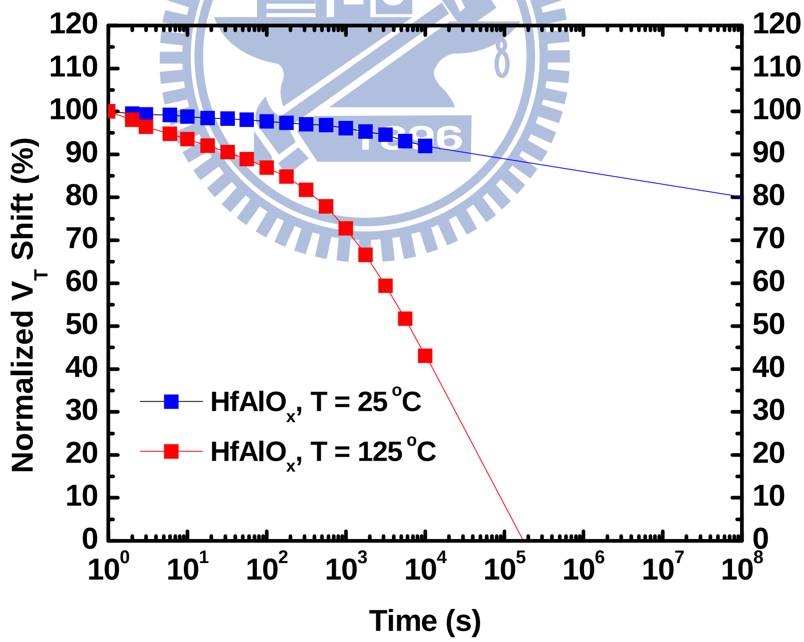


(c)

Fig 3.14 (c) Retention characteristics of our nanocrystal flash memory with Al_2O_3 and $HfAlO_x$ as blocking layer at room temperature (T=25℃) with normalized V_T Shift.

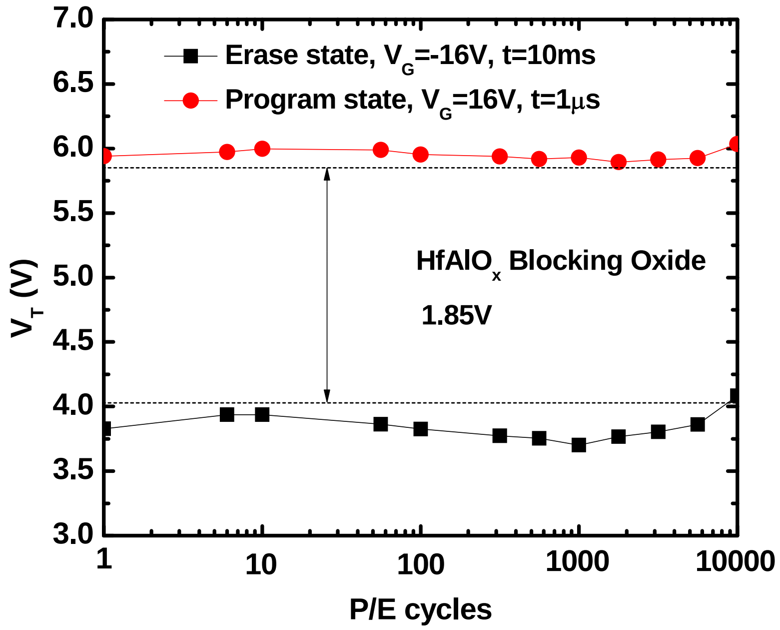


(a)

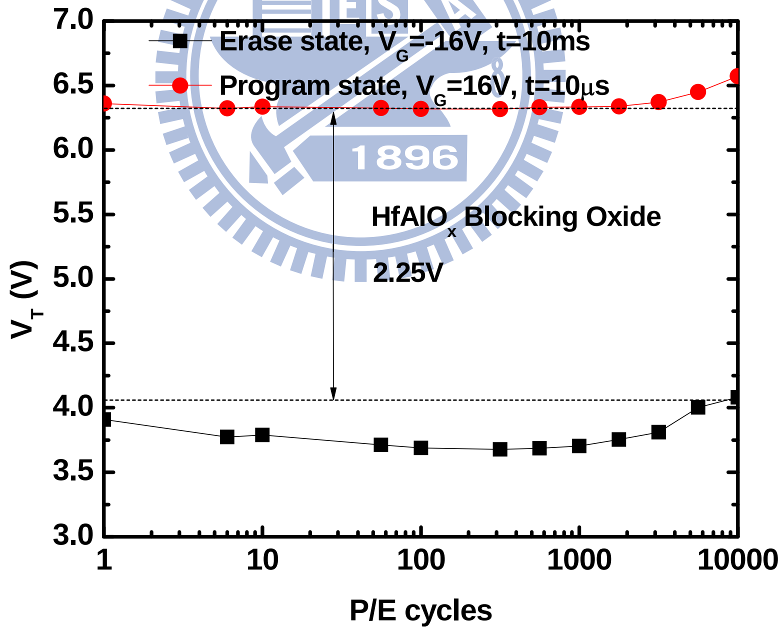


(b)

Figure 3.15 Retention characteristics of our nanocrystal flash memory with Al_2O_3 and (b) $HfAlO_x$ as blocking layer compare between T=25℃ and 125℃ with normalized V_T Shift.

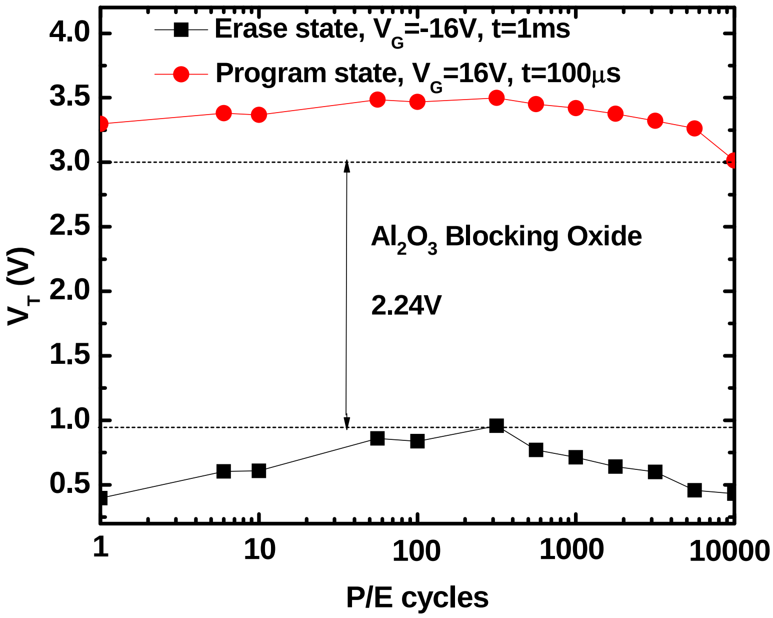


(a)



(b)

Figure 3.16 (a) and (b) Schematic of endurance characteristics of our nanocrystal flash memory with $HfAlO_x$ and (c) Al_2O_3 with different operation condition.



(c)

Figure 3.16 (c) Schematic of endurance characteristics with Al_2O_3 is under different operation condition.

Chapter 4

SANOS Nonvolatile Memory Devices with Dipole Layer Engineering

4.1 Introduction

According to the International Technology Roadmap for Semiconductor (ITRS), there are tough challenges for aggressively scaling down conventional floating-gate nonvolatile memory in sub-70nm node [4.1] .As a result, the SONOS-type flash memories, have recently attracted much attention in the next-generation nonvolatile memory. However, as semiconductor is prospering, there are many problems worth solving. Pursing high density and low cost per bit in nonvolatile memory application is inevitably important.

Therefore it is a major trend to scale down tunnel oxide thickness to increase P/E speed, and SILC happens to degenerate the reliability and get poorer retention performance. Here we demonstrate a SANOS nonvolatile memory device with dipole layer engineering to improve the programming speed and data retention simultaneously. Dipole layer by incorporating high-k material in the gate has been shown to be effective in modulating the effective work function towards the n-type band-edge. There are three hypotheses to the band structure of the gate stack being changed by the dipole layer. Due to the difference in electronegativities between the dipole layer material and Si, owing to the different oxygen density between dipole layer material and SiO_2, or as a result of there are dielectric contact induced gap states between dipole material and SiO_2.

4.2Experiment

An example of the fabrication process of the nitride-base SONOS-type nonvolatile memory devices is demonstrated by a LOCOS isolation process on a p-type, 20-30 Ω cm, (100) 150-mm silicon substrate, such as **Figure 4.1** shows. First, a 30 Å tunnel oxide was thermally grown at 800℃ in a horizontal furnace system. Then an ultra-thin high-k layer (HfO_2 or Al_2O_3) is deposited by MOCVD to form dipole layer. The flow rate and pulse number of precursors is carefully modulated to obtain ~ 10 Å high-k film. Next a 90 Å Si_3N_4 film is deposited by horizontal furnace LPCVD system. A 200 Å Al_2O_3 with blocking oxide is then deposited through MOCVD. Subsequently, poly-Si deposition, gate patterning, n^+ source/drain (S/D) implantation , p^+ body implantation, activation 950℃ 30 second, and the remaining standard CMOS procedures were completed to fabricate SONOS-type nonvolatile memory devices.

4.3 Results and Discussion

4.3.1 Characteristics of Program/Erase Operation

Figure 4.2 illustrates the I_{DS}-V_{GS} of our SANOS flash memory of W/L= 10μm/1μm and W/L=0.35 μm/1μm with different operation voltage, and shows excellent characteristics compare with the previous chapters. Here, we use the higher implant energy of phosphorus to reduce the poly effect. The subthreshold swing is equal to 205 mV/dec. **Figure 4.3** illustrates the I_{DS}-V_{GS} curve of SANOS and dipole layer engineering SANOS memory. We find the sample of Al_2O_3 has the biggest V_T and convention SANOS is the smallest. The Al_2O_3 make about 1V V_T shift and HfO_2 about 0.4V compare to conventional SANOS. The Al_2O_3 dipole is twice Al_2O_3 is about twice of HfO_2.Therefore, we can find the existence of dipole layer from I_{DS}-V_{GS} curve.

FN tunneling operation

Figure 4.4(a) illustrates I_{DS}-V_{GS} curve of initial state, programming state with FN tunneling at V_G=14V 1ms and erasing state at V_G=-16V 10ms of our conventional SANOS device. **Figure 4.5(a)** illustrates programming characteristic as a function of pulse width for different FN-tunneling operation condition. Source, drain, and substrate terminals are biased at 0V. The V_T shift is defined as the threshold voltage change of the device between programmed and erased states. For our expectations, we consider the dipole layer engineering with Al_2O_3 and HfO_2 will enhance programming speed than conventional SANOS. Here, we find out that the programming of dipole engineering is improved only at the time more than 10ms even though we try to give the same voltage to make up the different V_T due to the dipole layer, such as the **Figure 4.5(b)** shows. At the point, there is an intersection and the dipole layer of Al_2O_3 shows the fastest programming speed due to its larger dipole moment. Programming speed at the operation time more than 10ms follows the trend: SANOS-Al_2O_3 > SANOS-HfO_2 > SANOS. About that why the dipole layers don't show the advantage at the short operation time. We consider the thickness of dipole layer not match with tunneling oxide and it may have to do further research to know. However, the dipole layer can improve the programming speed truly in our experiment. The band structure is shown in **Figure 4.6** [4.2], the lower barrier seen by the electrons for tunneling is achieved. Meanwhile, **Figure 4.7** illustrates erasing characteristic as a function of various FN-tunneling operation conditions. Visibly, our flash memories of dipole engineering show a slower erasing speed compare to the conventional SANOS device. Erasing speed follows the trend: SANOS > SANOS-HfO_2 > SANOS-Al_2O_3. The erasing speed decreases due to the higher barrier seen by the electrons at charge storage layer during erase, such as the **Figure 4.8** shows [4.2].

Hot carrier injection

Figure 4.4 (b) illustrates I_{DS}-V_{GS} curve of initial state, programming state with CHE operation at V_G=8V and V_D=8V 5ms, and erasing state with BTBHHI operation at V_G=-7V and V_D=9V 10ms of our conventional SANOS device. **Figure 4.9** illustrates programming characteristic as a function of pulse width for different CHE operation condition. We find the same program speed with CHE operation. We consider the influence of dipole layer be obscured owing to the electron obtain high energy. Therefore, when electron tunnel the bottom oxide, the electron can't sense the slightly diversification of band structure. **Figure 4.10** illustrates erasing characteristic as a function of pulse width for different BTBBHI operation condition. We find the erasing speed follows the same trend of FN erasing operation. The conventional still has the fastest erasing speed. We consider it due to the heavier effective mass and higher SiO_2 bandoffset than electron, so the hole can sense the influence of dipole even it is in the "hot" state.

4.3.2 Retention

The retention characteristics of our SANOS flash memory and SANOS with dipole layer engineering at room temperature (T=25℃) are illustrated in **Figures 4.11(a), (b), and (c)**. For SANOS device, it results in ~ 0.35 V (~ 14.9%) memory window loss for 10^4 seconds retention time at room temperature in the initial window with 2.3 V. However, for SANOS devices with dipole layer engineering, the retention characteristics improve instead. The retention time can be up to 10^4 seconds with ~ 0.28V (~12.3%) window loss for SANOS-HfO_2 and ~0.13V (~5.9%) loss for SANOS-Al_2O_3. The **Figure 4.12** shows the result of normalized V_T shift, data retention characteristics follow the trend: SANOS-Al_2O_3 > SANOS-HfO_2 > SANOS.

Figure 4.13 shows the band diagram of SANOS devices with dipole layer engineering during retention [4.2]. By introducing dipole layer into SANOS-type devices, the nitride band is shifted down with respect to tunneling oxide. This would lead to a higher energy barrier for electrons out-tunneling from the charge storage layer to the silicon substrate during retention. Therefore a longer retention time is expected for our SANOS-type nonvolatile memory with an ultra-thin high-k layer (Al_2O_3 or HfO_2) inserted.

4.3.3 Endurance

Figures 4.15 and 4.16 show endurance characteristics of SANOS combined with SANOS-type flash memory device dipole engineering in different operate conditions. **Figure 15** shows the FN tunneling operation, the individual voltage shift becomes visible after 10^4 P/E cycles. **Figure 4.16** shows the hot carrier injection operation, the individual voltage shift becomes unclear after 10^4 P/E cycles due to hot carrier degradation or the not match injection profile of electrons and holes.

4.3.4 Disturbance

As we know, the NOR array circuit have gate, read, and drain disturbance phenomenon with the CHE programming and BTBHHI erasing, such as the **Figure 4.17** shows. The read disturbance take place under the applied stress wile read the cell. About gate disturbance, such as during programming cell A, gate disturbance occurs in the cells which connected with the same word-line (WL) because the gate stress is applied to the same WL. About drain disturbance, just like during programming cell A, drain disturbance happens in the cells which connected with the same bit-line (BL) and especially in the cells is in the programming state.

Figure 4.18 illustrates the gate disturbance characteristics in the erasing state. We observed the sample of dipole with Al_2O_3 having the most threshold voltage shift of 0.36V i.e., negligible disturbance, under the flowing conditions: V_G = 8V; Vs = V_D = V_{SUB} = 0V; stress for 1000s. The threshold voltage shift due to gate disturbance follows the trend: SANOS-Al_2O_3 > SANOS-HfO_2 > SANOS. It's in line with our expectations owing to the mechanism of gate disturbance is similar to FN-tunneling programming, such as the **Figure 4.6** show previously. **Figure 4.19** illustrates the drain disturbance characteristics in the programming state, under the flowing conditions: V_D = 8V; V_S = V_G = V_{SUB} = 0V; stress for 1000s. We observed the conventional SANOS having the most threshold voltage shift which is 0.12V. It's also in line with our expectations owing to the mechanism of gate disturbance just like the BTBHHI erasing. Therefore, the threshold voltage shift due to drain disturbance follows the trend SANOS > SANOS-HfO_2 > SANOS-Al_2O_3. Finally, **Figure 4.20** illustrates the read disturbance characteristics in the erasing state. There are under the flowing conditions V_G=4V for Al_2O_3, V_G=3.5V for HfO_2, and V_G = 3V for SANOS, and V_D=0.1V, V_S=V_{SUB}=0 V; stress for 1000s. The threshold voltage shift due to read disturbance follows the trend SANOS-Al_2O_3 > SANOS-HfO_2 > SANOS. The mechanism of read disturbance is similar to gate disturbance.

4.4 Summary

In this chapter, we discuss SANOS flash memory of the dipole layer engineering from FN-tunneling programming and erasing, hot carrier injection programming and erasing, data retention, endurance, and disturbance. We observed the programming speed of dipole layer engineering can be improved in long operation time (>10ms) by the FN-tunneling operation. Furthermore, the data retention can be improved by dipole engineering. However, the erasing speed will be sacrificed due to the engineering of band structure by dipole layer. In addition, if channel hot electron was utilized to program, no programming speed difference was observed with or without dipole layer engineering due to the tunneling electron is "hot". However, when we use BTBHHI to erase, the erasing speed of dipole layer engineering was slower for dipole layer engineering owing to the hot hole is heavy enough to sense the dipole layer engineering. About endurance measurements, we find that the characteristics of FN-operation are better than hot carrier injection operation. Finally, the presence of dipole layers was reconfirmed from disturbance measurement. The dipole samples showed better drain disturbance while it suffered from poor gate and read disturbance as expected.

References (chapter4)

[4.1] W. Arden, “Future semiconductor material requirements and innovations as projected in the ITRS 2005 roadmap,” *Materials Science and Enguneering*: B, vol. 134 pp. 104-108, 2006.

[4.2] Y. N. Tan, H. C. Wen, C. Park, D. C. Gilmer, C.D. Young, .D. Heh, P. Sivasubramani, J. Huang, P. Majhi, P.D. Kirsch, B.H. Lee, H.H. Tseng, and R. Jammy, ” Tunnel Oxide Dipole Engineering in TANOS Flash Memory for Fast Programming with Good Retention and Endurance ,” *in VLSI Technology*, Systems and Applications, 2008. VLSI-TSA 2008. International Symposium, 2008, pp. 54 – 55

- LOCOS isolation (Active region definition, P^+ Well ,Channel stop &anti punch through& V_T adjustment implant)
- Thermal Oxide 30Å
- MOCVD Al_2O_3&HfO_2 15 Å
- LPCVD Si_3N_4 90 Å
- MOCVD Al_2O_3 200 Å
- Deposition Poly-Si 2000 Å
- N^+ Source/Drain
- P^+ Body Contact
- Activation 950°C 30s
- Passivation
- Metallization

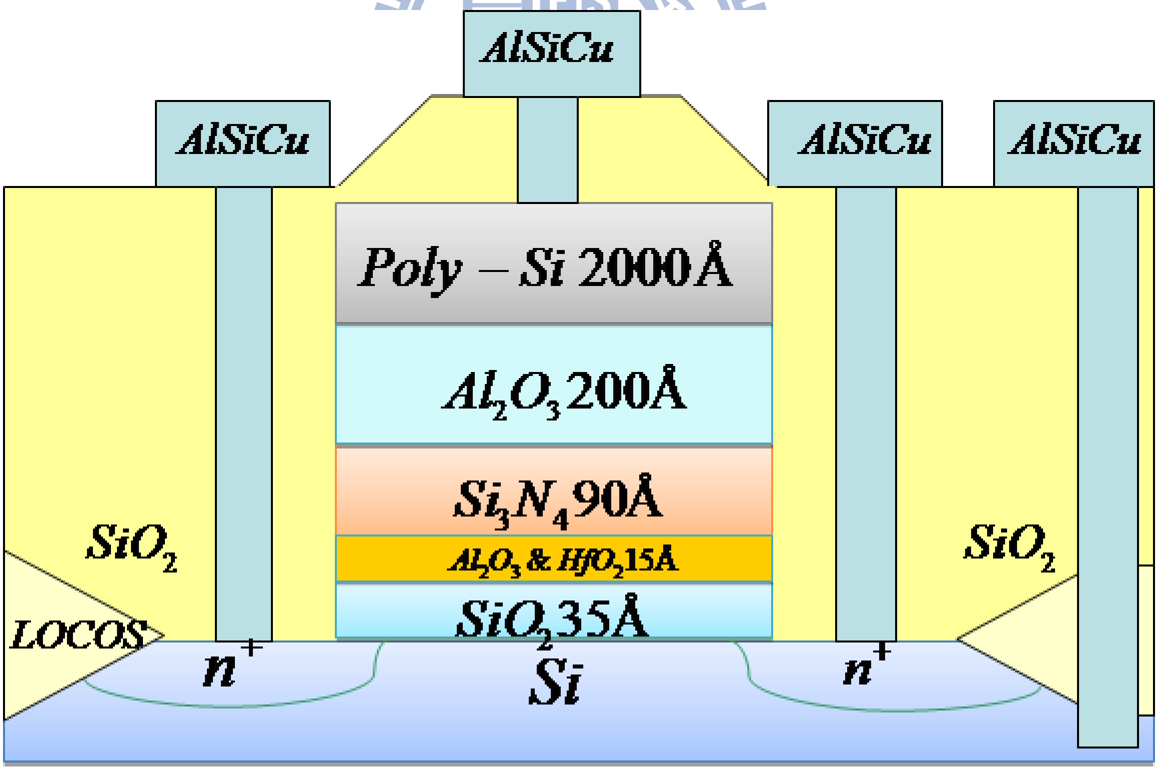
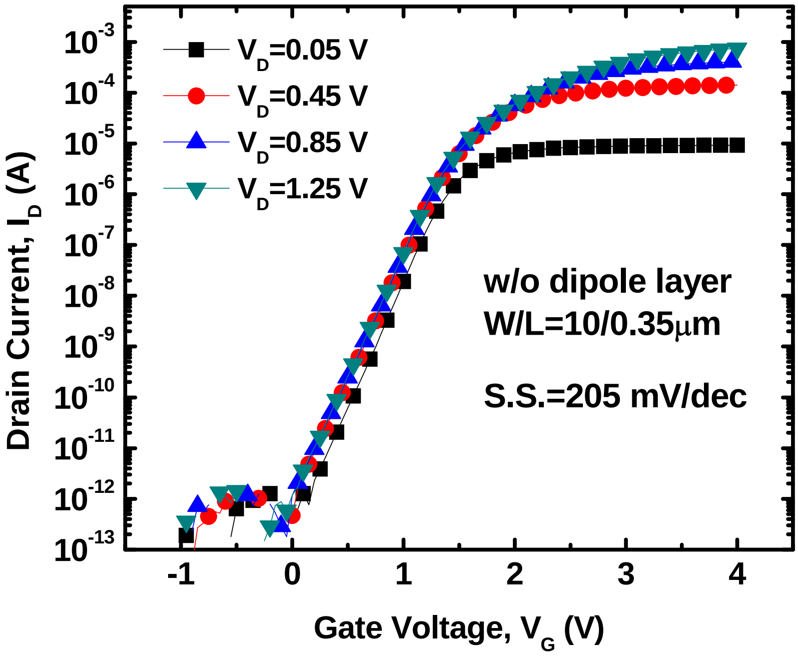
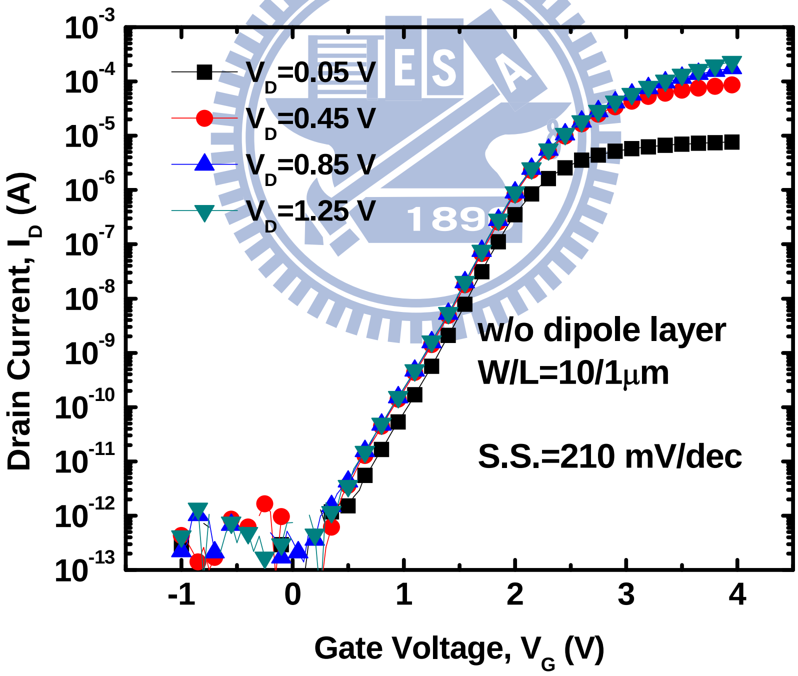


Fig 4.1 Schematic of SANOS of dipole engineering flash memory structure with Al_2O_3 blocking layer.



(a)



(b)

Fig 4.2 (a) I_{DS}-V_{GS} of our SANOS flash memory with different operation voltage of W/L=0.35 μm/1μm and (b)W/L= 10μm/1μm, and shows excellent characteristics compare with the previous chapters.

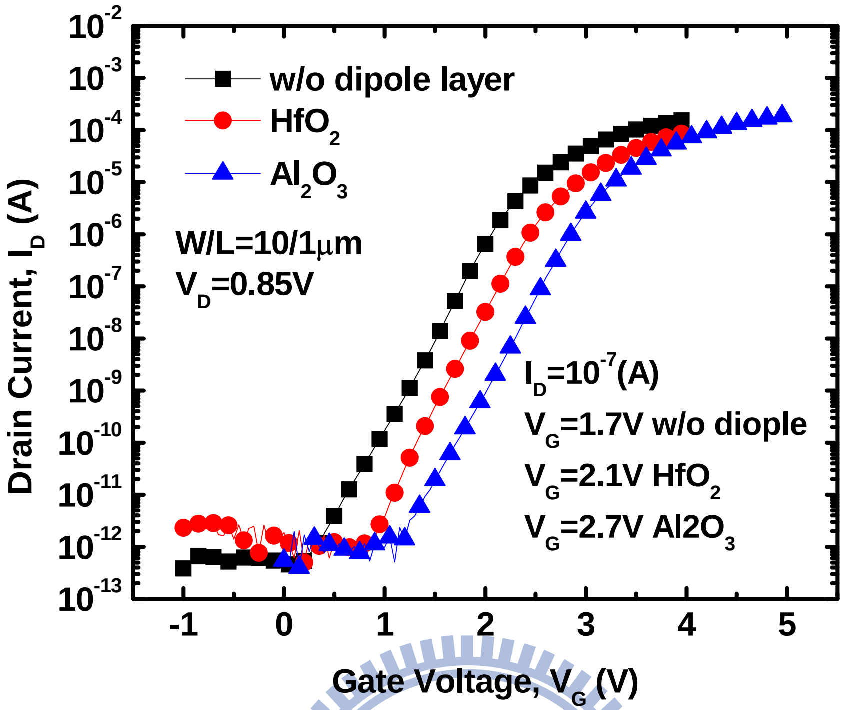
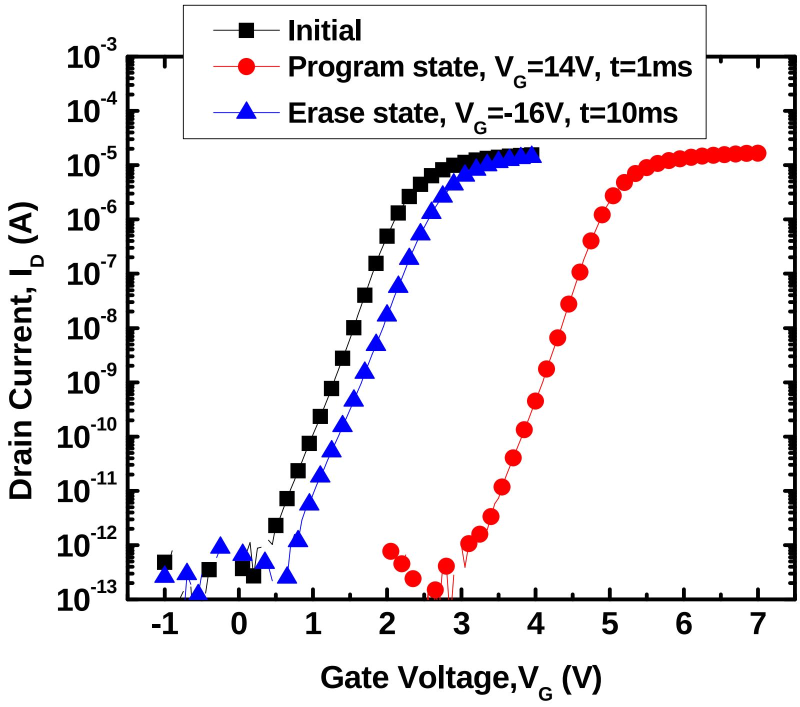
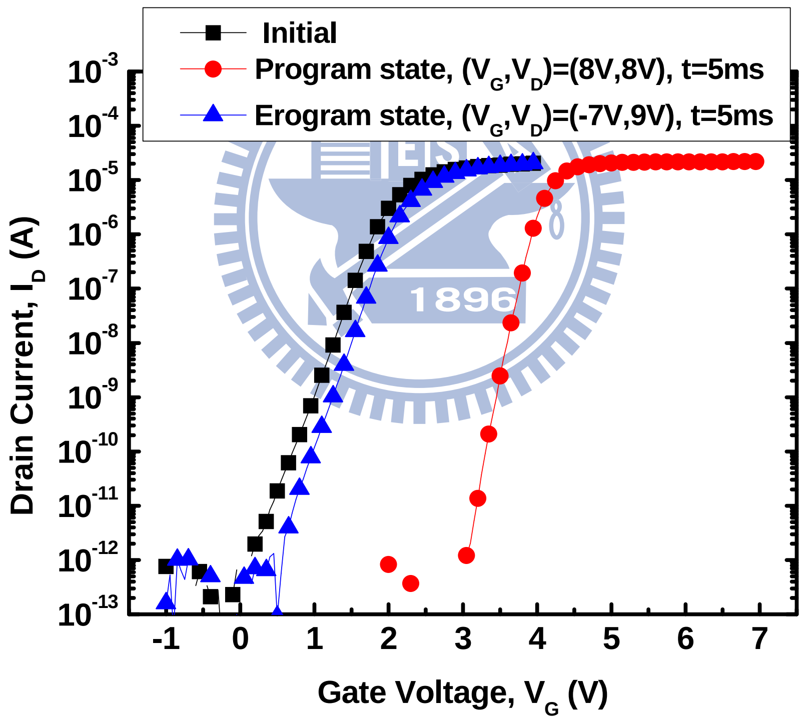


Fig 4.3 I_{DS}-V_{GS} curve of SANOS and dipole layer engineering SANOS memory.

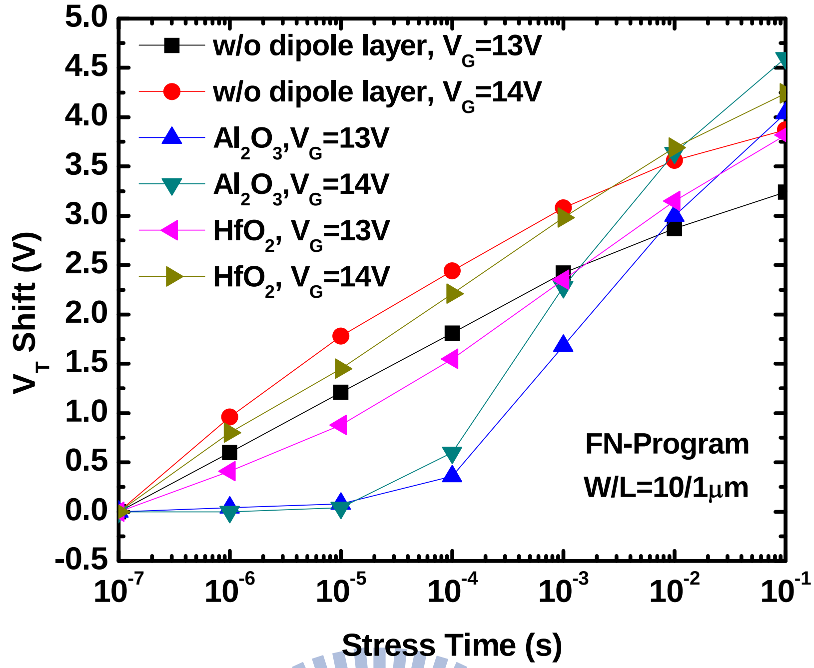


(a)

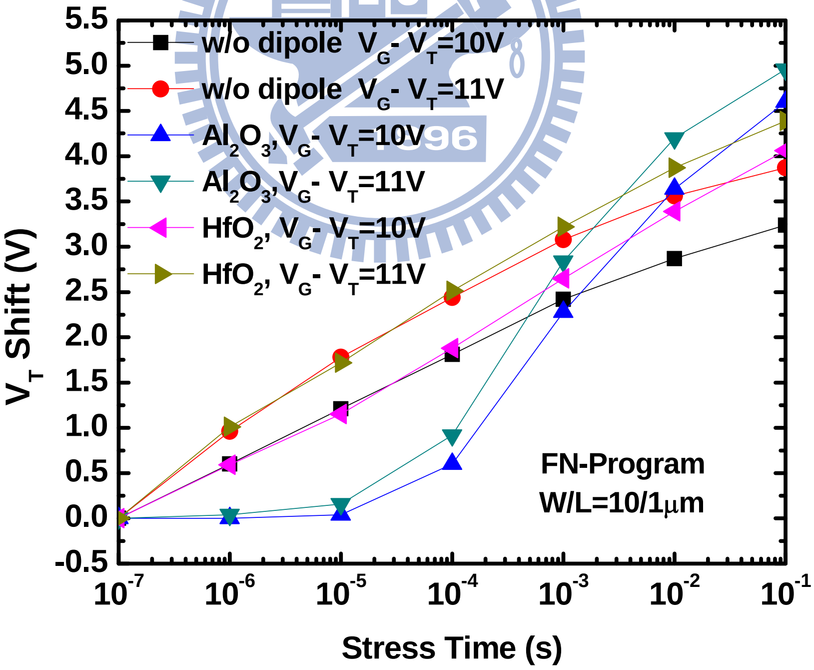


(b)

Fig 4.4 (a) I_{DS}-V_{GS} curve of initial state, programming state with FN tunneling at V_G=14 1ms and erasing state with FN tunneling at V_G=-16V 10ms of our conventional SANOS device. (b) I_{DS}-V_{GS} curve of initial state, programming state with CHE operation at V_G=8V and V_D=8V 5ms, and erasing state with BTBHHI operation at V_G=-7V and V_D=9V 10ms of our conventional SANOS device.



(a)



(b)

Fig 4.5 (a) Programming characteristic as a function of pulse width for different FN-tunneling operation condition. (b) We try to give the same voltage to make up the different V_T due to the dipole layer.

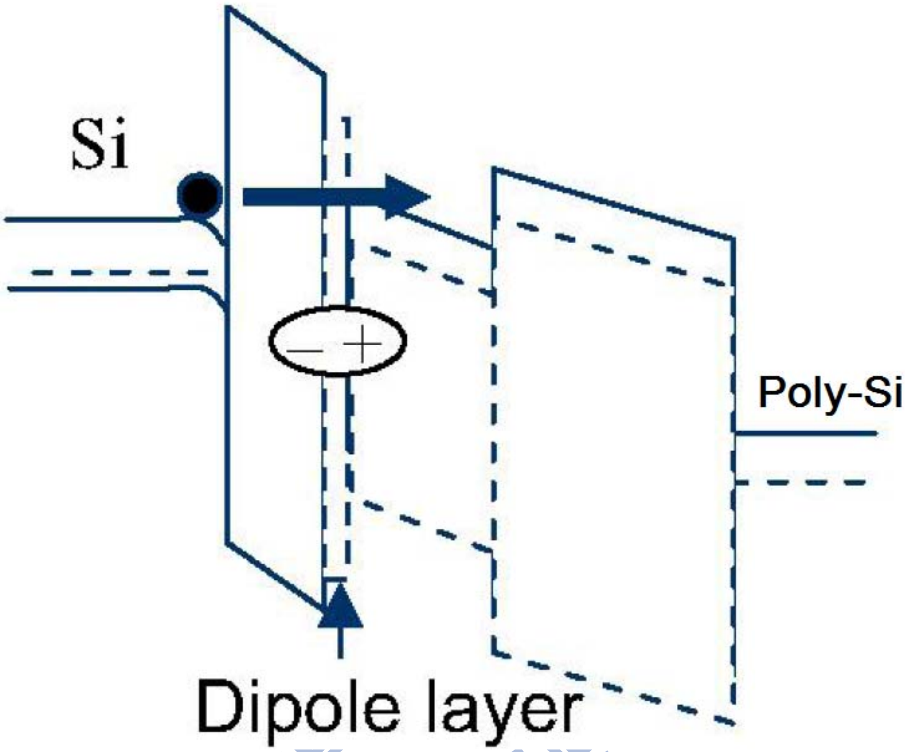


Fig 4.6 Using a dipole layer is expected to result in easier programming at a given tunnel oxide electric field [4.2].

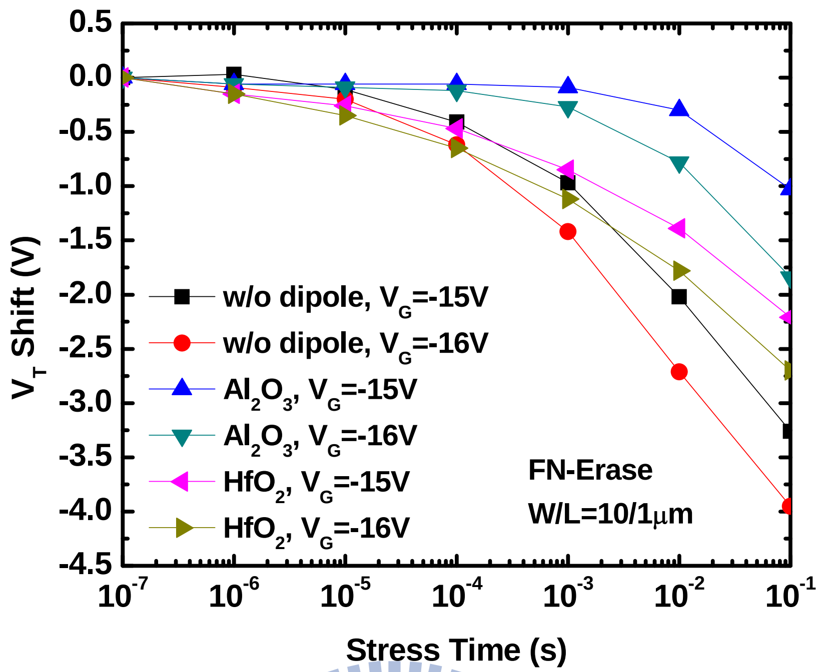


Fig 4.7 Erasing characteristic as a function of various FN-tunneling operation conditions.

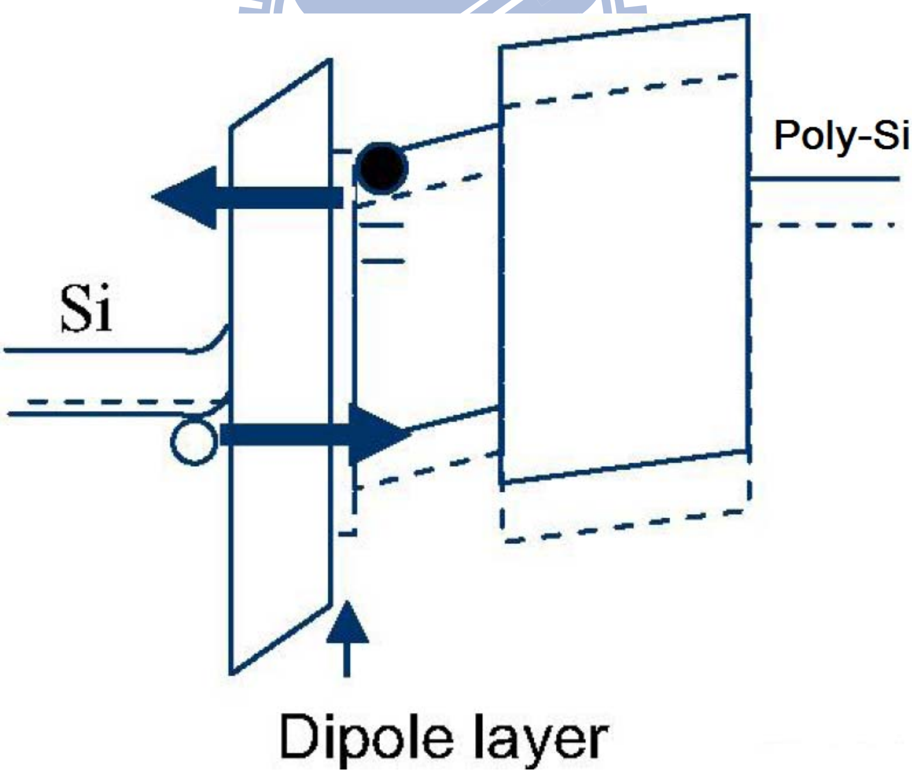


Fig 4.8 Dipole layer incorporation causes a slightly slower erase at a given tunneling oxide electric field as the nitride bands are shifted down with respect to the tunneling oxide [4.2].

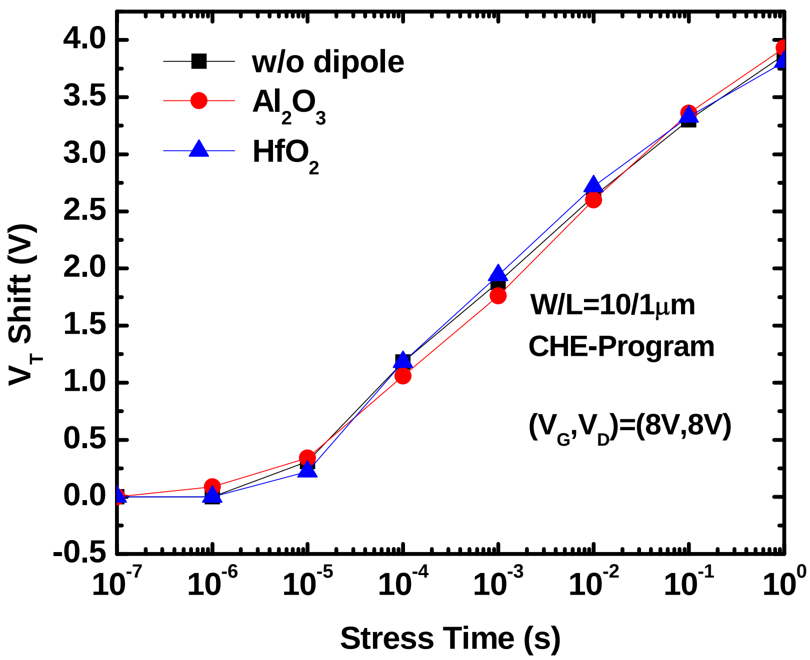


Fig 4.9 Programming characteristic as a function of pulse width for different CHE operation condition.

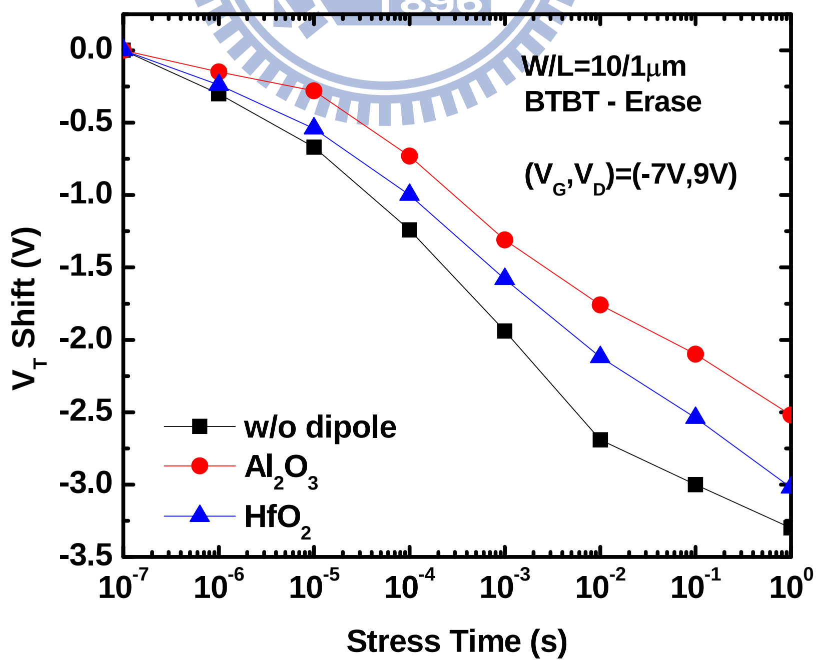


Fig 4.10 Erasing characteristic as a function of pulse width for different BTBBHI operation condition.

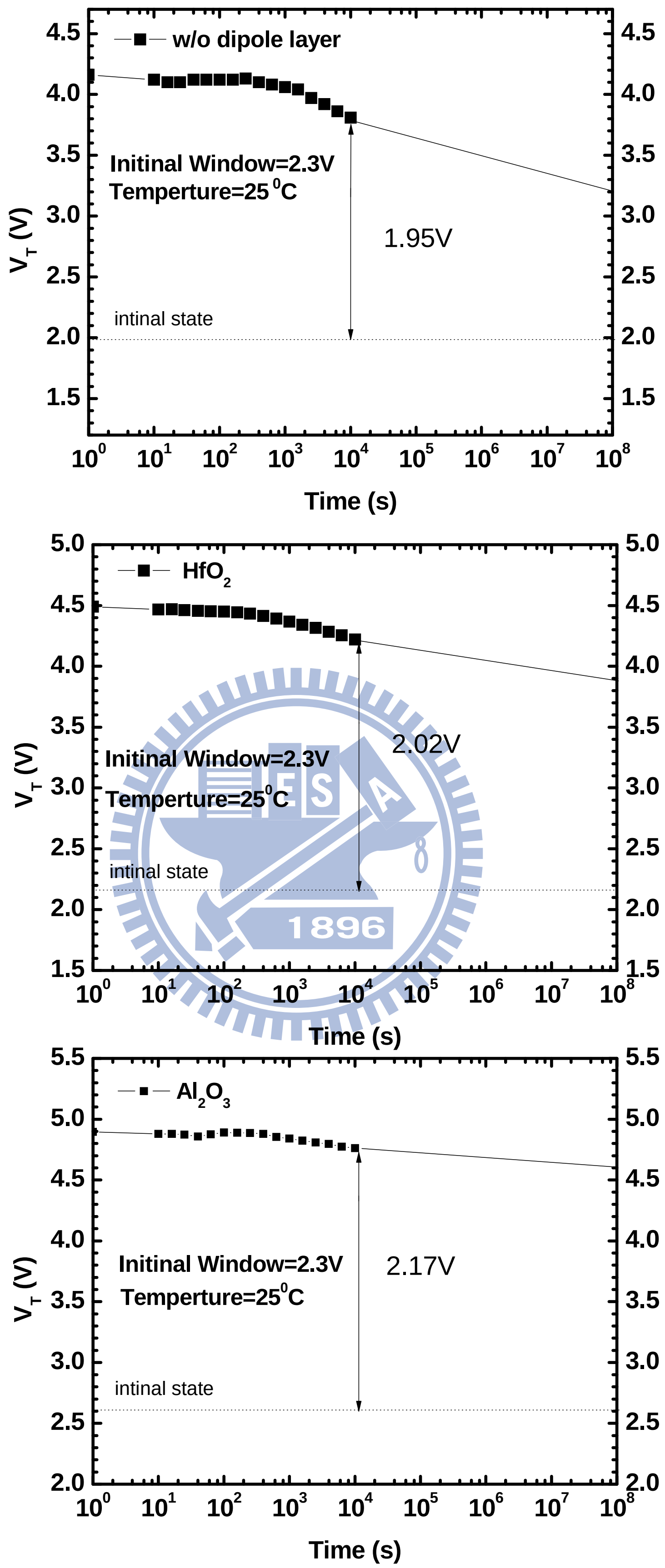


Fig 4.11 Retention characteristics of our SANOS flash memory and SANOS with HfO_2 and Al_2O_3 dipole layer engineering at room temperature (T=25℃).

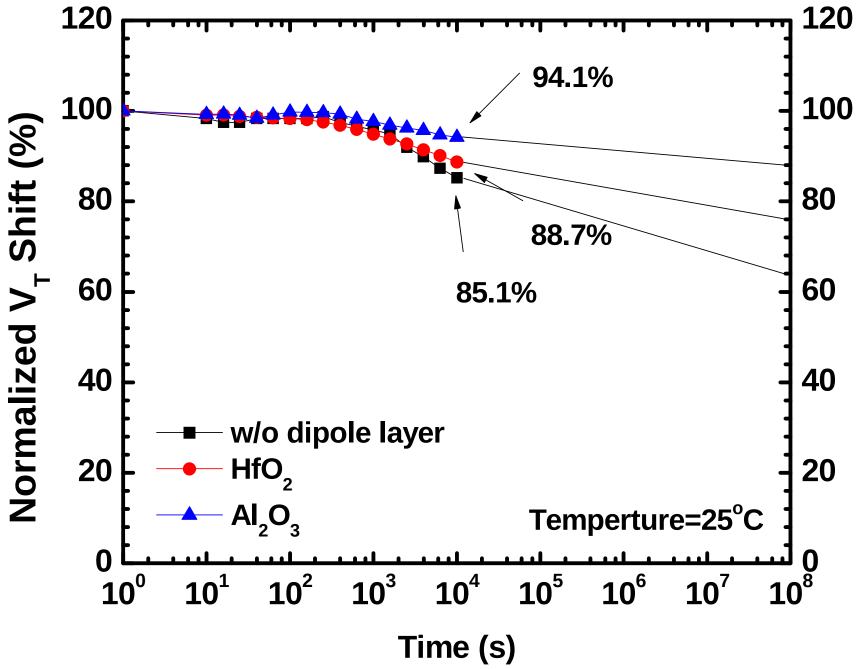


Fig 4.12 Data retention characteristics of normalized V_T shift at room temperature (T=25℃), the result follows the trend: SANOS-Al_2O_3 > SANOS-HfO_2 > SANOS.

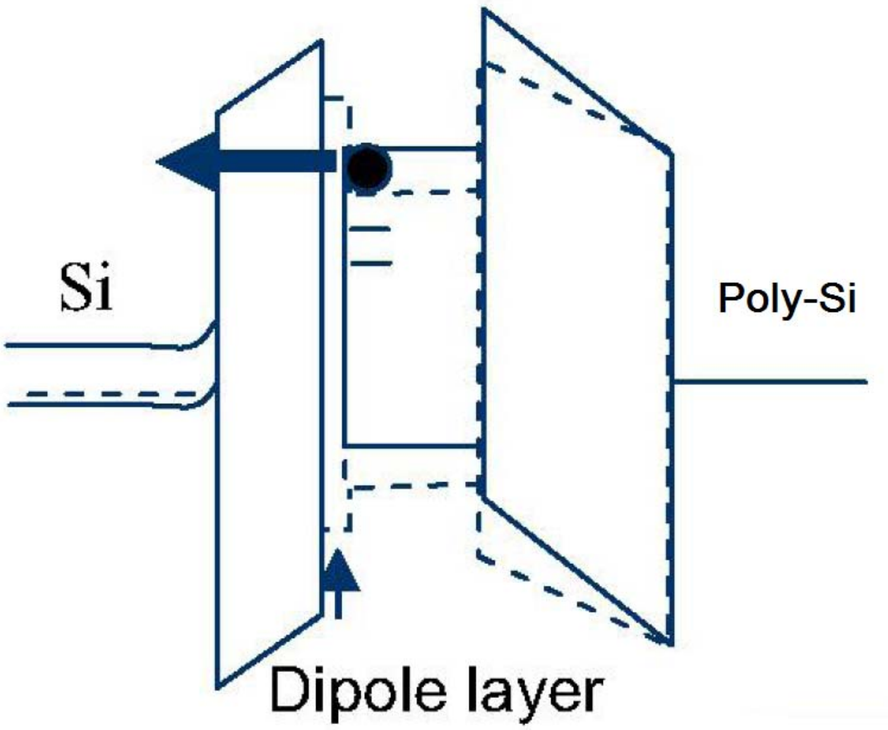


Fig 4.13 The band diagram of SANOS devices with dipole layer engineering during retention [4.2].

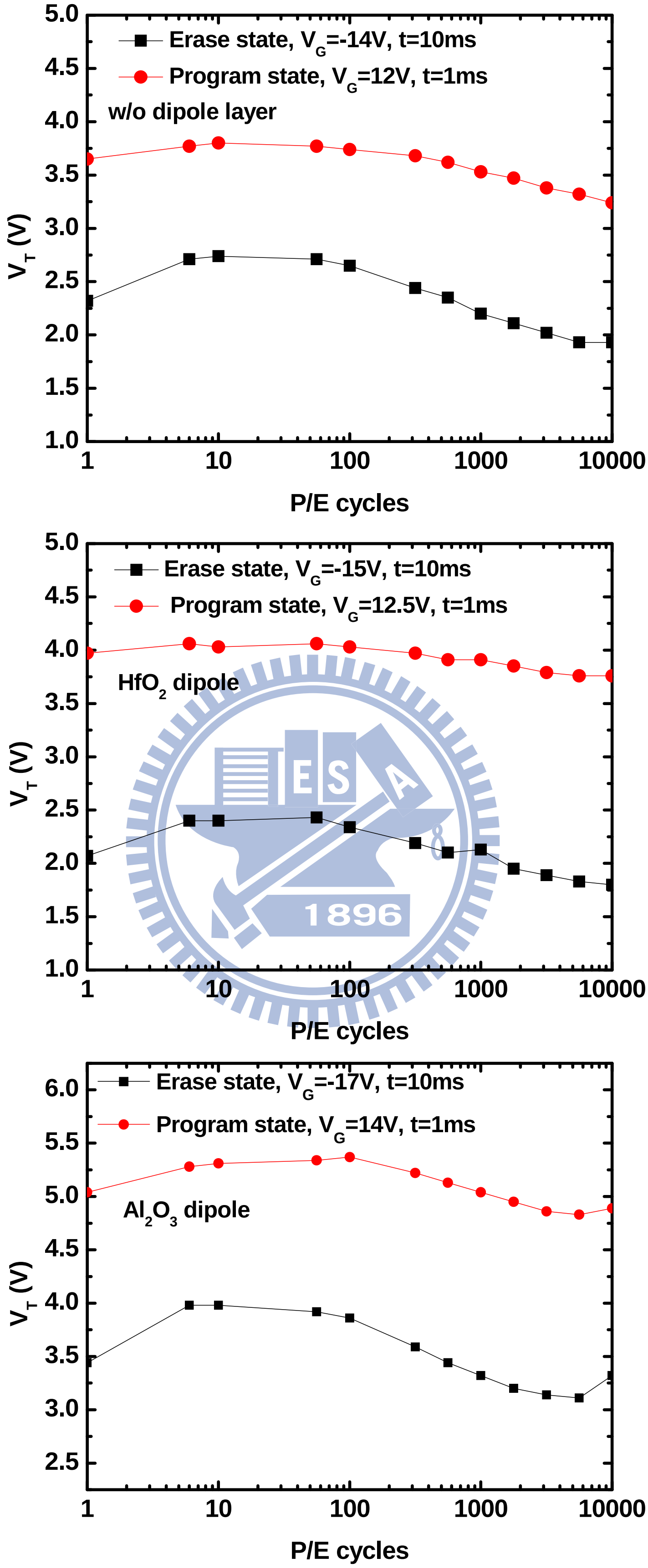


Fig 4.15 Schematic of endurance characteristics of SANOS and SANOS-type memory with dipole layer engineering with FN-tunneling operation.

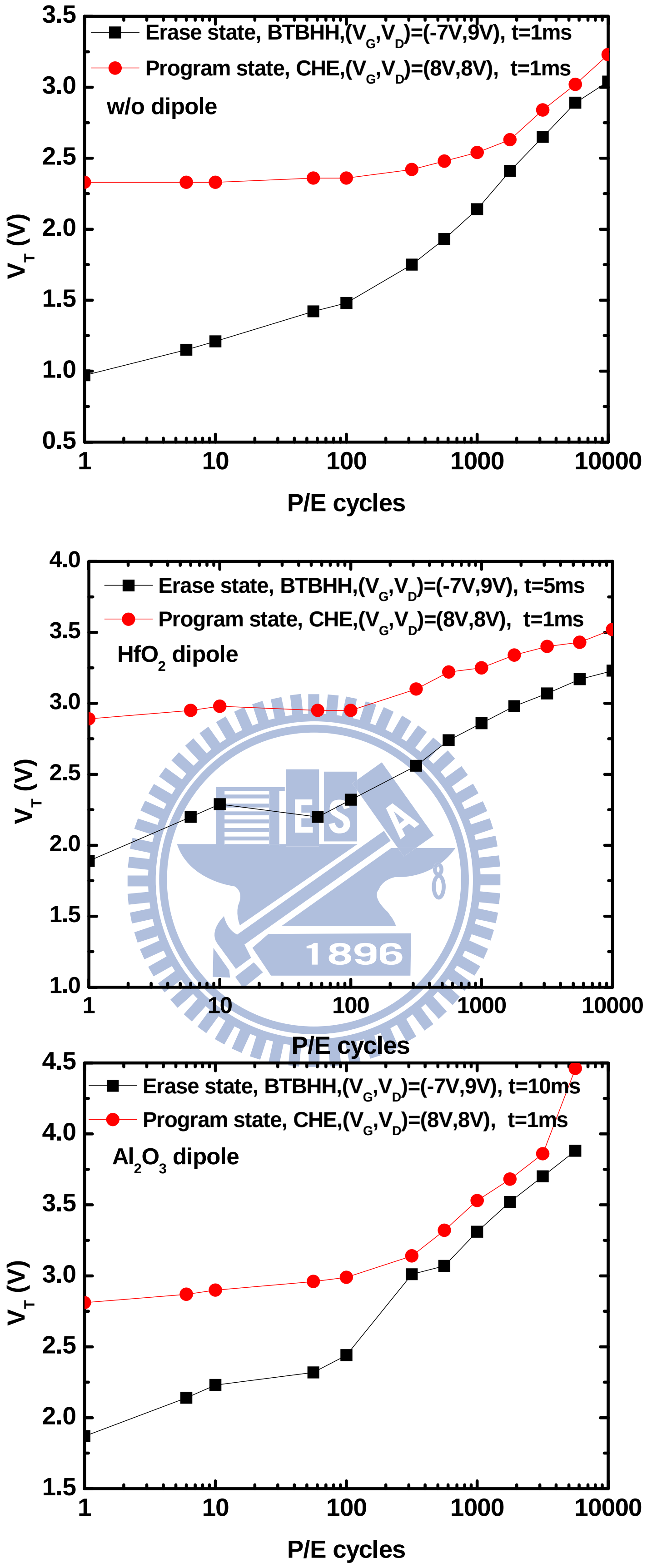


Fig 4.16 Schematic of endurance characteristics of SANOS and SANOS-type memory with dipole layer engineering with hot carrier injection operation.

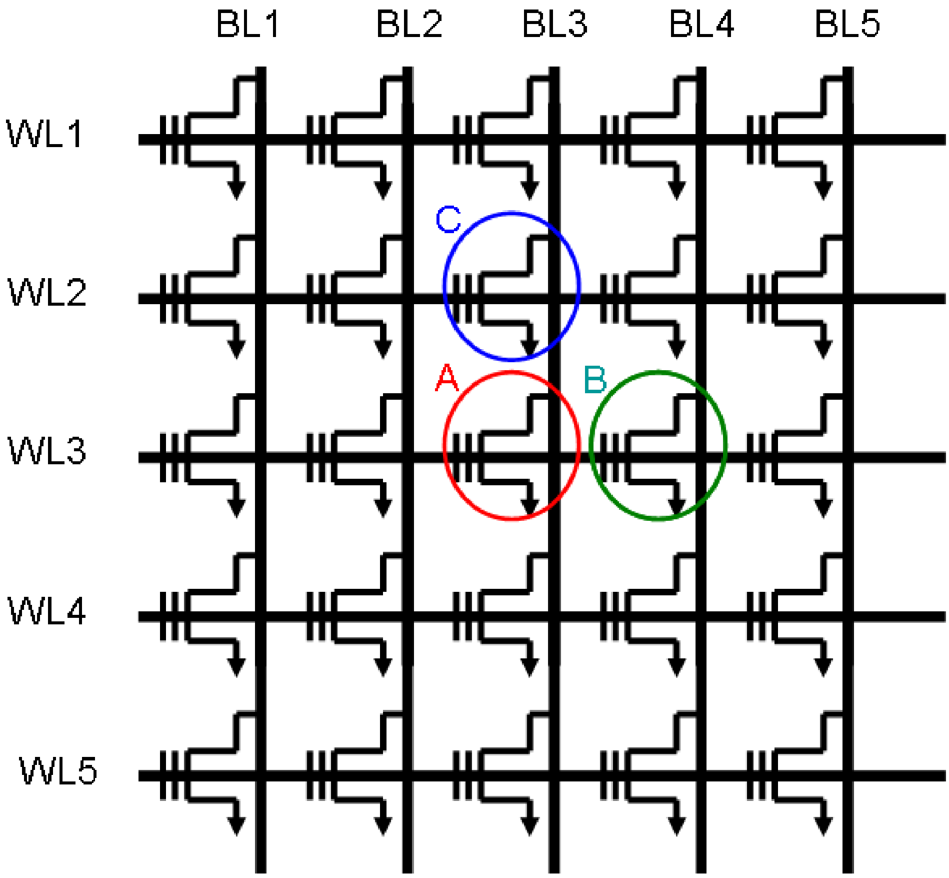


Fig 4.17 NOR array circuit for nonvolatile memory.

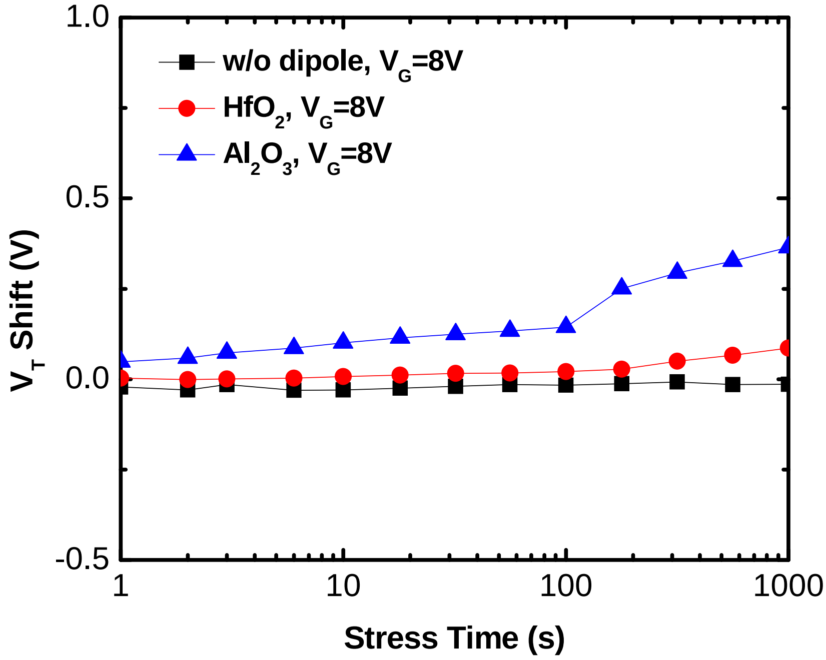


Fig 4.18 Gate disturbance characteristics of SANOS and SANOS-type memory with dipole layer engineering in the erasing state.

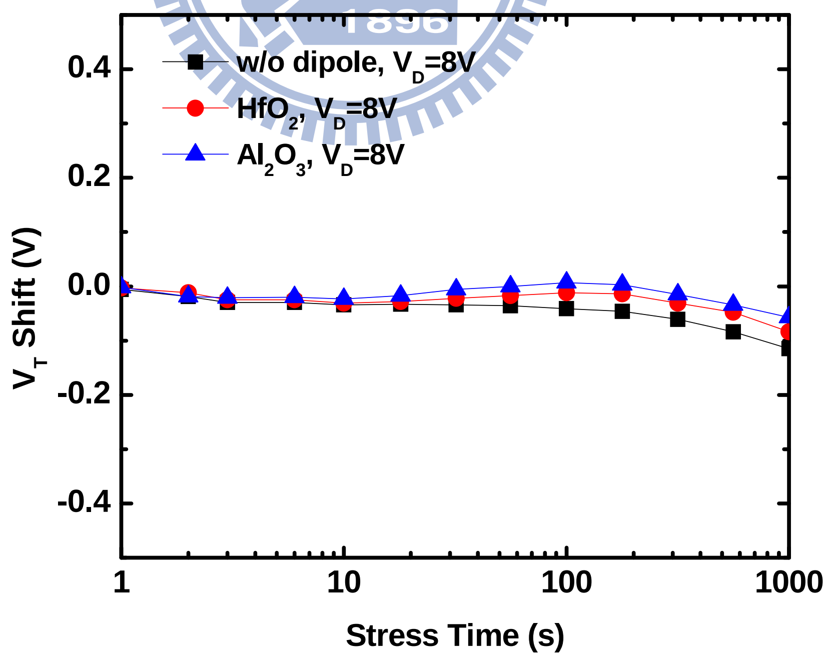


Fig 4.19 Drain disturbance characteristics of SANOS and SANOS-type memory with dipole layer engineering in the erasing state.

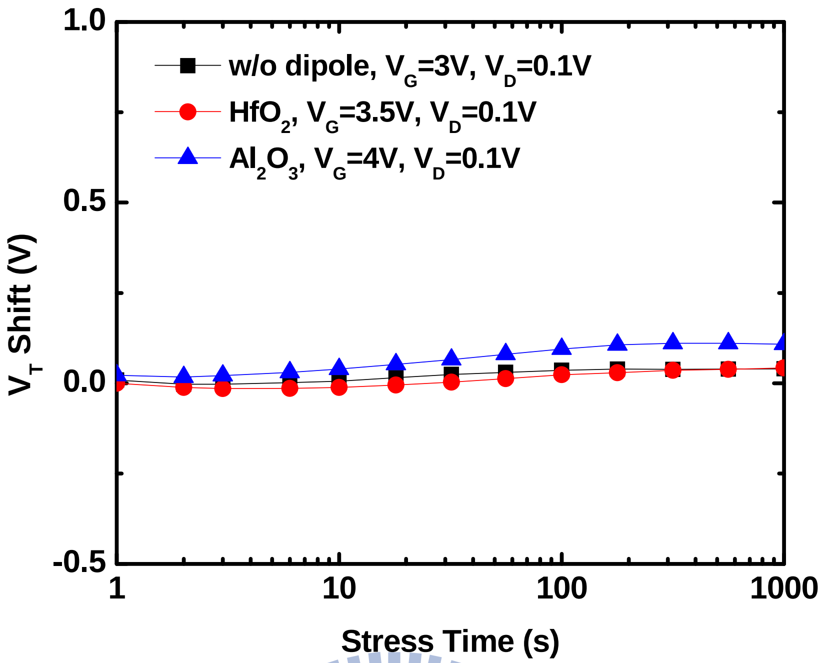


Fig 4.20 Read disturbance characteristics of SANOS and SANOS-type memory with dipole layer engineering in the erasing state.

Chapter 5

Conclusions and Further Recommendations

5.1 Conclusions

In **Chapter 2** of the thesis, the effect of inserting interfacial dipoles on SONOS flash memory capacitors was observed based on C-V characteristics. Adding an ultra thin Al_2O_3 or HfO_2 layer on the SiO_2 tunneling layer caused positive V_{FB} shift while negative V_{FB} shift occurred as it was placed under SiO_2 blocking layer. The dipole exhibited the strongest strength for 5Å Al_2O_3, and it saturated at 20Å. Besides, magnitudes of the Al_2O_3/SiO_2 dipole were demonstrated to be twice large than that of HfO_2/SiO_2, with the same high-k thickness. Adding an Al_2O_3 layer on tunneling layer of HfO_2 nanocrystal nonvolatile flash memory device was also proved to cause positive V_{FB} shift from C-V curves.

In **Chapter 3**, we investigated the HfO_2 nanocrystal memory with Al_2O_3 and $HfAlO_x$ as the blocking layer. The two adopted high-k materials showed acceptable leakage current and without crystallization after activation at 950℃ for 30sec. The $HfAlO_x$ sample exhibited faster P/E speed compared with the Al_2O_3 sample, due to higher k value of $HfAlO_x$. On the other hand, more traps existed in the $HfAlO_x$ layer, which caused trap-assisted tunneling at low field and thus data retention of $HfAlO_x$ device was expected to be poorer at high temperature. For our nanocrystal memory devices, advantages of fast programming speed, excellent data retention time at room temperature and endurance after P/E cycles of 10^4 were observed.

In **Chapter 4**, the Al_2O_3 and HfO_2 dipole layers were adopted to engineer the band diagram of SANOS-type nonvolatile flash memory. We observed not only the programming speed in long operation time (>10ms) by FN-tunneling operation but the data retention was improved by dipole engineering. However, the erasing speed was sacrificed due to the band structure engineering. In addition, if channel hot electron was utilized to program, no programming speed difference was observed with or without dipole layer engineering due to the tunneling electron is “hot”. However, when we used BTBHHI to erase, the erasing speed was slower for dipole layer engineering owing to the hot hole is heavy enough to sense the dipole layer engineering. Finally, the presence of dipole layers was reconfirmed from disturbance measurement. The dipole samples showed better drain disturbance while it suffered from poor gate and read disturbance as expected.

5.2 Further Recommendations

There are some interesting topics for further investigation. In **Chapter 2**, some problems were found in our study, such as the relationship between the V_{FB} shifts and thickness of dipole layers, and it may require further analysis to know why they are different from other experiments. Also, we can use other high-k materials to make the different directions of dipole moment. In **Chapter 3**, we had excellent programming speed, but TAT causes the poor retention so that some annealing treatment can be applied to repair these defects. In **Chapter 4,** our devices exhibited faster programming speed in longer operation time, which was inferred to be relate with the thickness of high-k layer and took the thickness into consideration.

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碩士論文題目：

電偶極工程與高介電係數阻絕層於氮化矽與奈米微晶粒非揮發性記憶體之研究

A Study of the Impact of Dipole Engineering and High-k Blocking Layer on Nonvolatile Memories with Nitride and Nanocrystal Trapping Layer