國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩士論文

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場效鰭狀電晶體之靜態隨機存取記憶體

Independently-Controlled-Gate FinFET Schmitt

Trigger Sub-threshold SRAMs

研究生：謝建宇

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研究生 ： 謝建宇 Student : Chien-Yu Hsieh

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國立交通大學

電子工程學系電子研究所

碩士論文

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中 華 民 國 九 十 九 年 十 一 月

以史密特觸發器為基礎操作在次臨界區以獨立閘極控制場效鰭狀電晶體之靜態隨機存取記憶體

研究生:謝建宇　　　　　　　　　　　　　指導教授:莊景德

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摘要

本論文提出了利用獨立閘極操作鰭狀場效電晶體操作在次臨界區以史密特觸發器為基礎的三種新穎的靜態隨機存取記憶體單元。這三種 8T 記憶體單元(IG_STs)利用獨立閘極特性鰭狀場效電晶體，前端閘極當作是推疊的電晶體；後端閘極當作是中間的節點來產生史密特觸發器內建回饋的機制。成功減少了電晶體數目以及縮小了面積，並且得到較佳的靜態雜訊邊界(SNM)值和對製程飄移及本質參數變異-線邊緣粗糙程度(Line Edge Roughness)有更佳的容忍度。

經由 3D mixed-mode 元件模擬器(TCAD)得知 SNM 值、靜止狀態漏電流值，並跟傳統 6T 及過去文獻上(ST1、ST2)的類似記憶體單元做比較。跟 6T 比較操作在 0.4V 時，讀取時靜態雜訊邊界(RSNM)增加了 81%並且操作在更低電壓(0.15V)同時更增加了 110%。根據 32 奈米節點的佈局規則，從實際佈局圖中得知這三種記憶體單元(IG_STs)有著比過去文獻中(ST1，ST2)更好的密度的優勢。另外記憶體單元的讀取、寫入時間、讀取時間因為同一條位元線其它非選取到記憶體細胞在讀取的同時由於其儲存的資料內容經由位元線漏電流造成讀取失敗的效應也都模擬了，此外加上溫度效應去看因漏電流的增加所導致不同的讀取時間。結果顯示出是符合操作在次臨界區域所要求的速度。

由於操作在次臨界區必須更關注於記憶體單元的穩定度，於是在本質參數變異部分我們考慮了線邊緣的粗糙程度(Gate − ,and Fin − Line Edge Roughness) 和功函數變異程度(Work Function Variability)並且利用 3D mixed-mode 蒙地卡羅模擬來檢驗其穩定度。此外更加上了考慮製程飄移(L_{eff}, EOT, $W_{fin}(T_{si})$ and H_{fin})而導致的變異可更系統性的來看其穩定度，結果可以得知在最差的製程飄移條件之下(FNSP)，我們提出的兩種新記憶體單元仍然能滿足足夠的 μ/σ 的比例。

Independently-Controlled-Gate FinFET Schmitt Trigger Sub-threshold SRAMs

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Abstract

In this paper, we propose three novel Independently-controlled-Gate Schmitt Trigger (IG_ST) FinFET SRAM cells for sub-threshold operation. The proposed IG_ST 8T SRAM cells utilize split-gate FinFET devices with the front-gate devices serving as the stacking devices, and the back-gate devices serving as the intermediate node conditioning devices to provide built-in feedback mechanism for Schmitt Trigger action, thus reducing the cell transistor count/area and achieving improved SNM and better tolerance to process variation and local random variation (LER).

3D mixed-mode simulations are used to evaluate the SNM, and Standby leakage of proposed cells, and results are compared with the standard 6T cells and previously reported 10T Schmitt Trigger sub-threshold SRAM cells (ST1 and ST2). Compared with the conventional tied-gate 6T cell, the proposed IG_ST SRAM cells demonstrate 1.81X and 2.11X higher nominal RSNM at V_{CS}=0.4V and 0.15V, respectively. The cell layouts and areas are assessed based on scaled ground rules from 32 nm node, and the density advantage over previously reported 10T Schmitt Trigger sub-threshold SRAM cells are illustrated. The cell AC performance (Read access time, Write time, and Read access time versus the number of cells per bit-line) and temperature dependence are evaluated, and shown to be adequate for the intended sub-threshold applications.

Stability is a critical concern in sub-threshold region, so we consider Gate –, and Fin – Line Edge Roughness, and Work Function Variability using 3D mixed-mode Monte Carlo simulations to investigate its stability. Moreover, process variations (L_{eff}, EOT, $W_{fin}(T_{si,})$, and H_{fin}) are performed for systematic variation concern. Our results indicate that even at the worst corner (FNSP), two of the proposed cells can provide sufficient margin of μ/σ ratio.

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Chapter 1

Introduction

1.1 Background

For ultra-low-power applications, such as portable devices, implanted medical instruments, and wireless body sensing networks, operating circuit below threshold voltage is an effective solution [1, 2] to reduce static and dynamic power consumption. However, with the scaling of technology, the stability of conventional 6T SRAM cell (Fig. 1.1) deteriorates significantly, as shown in Fig. 1.2, especially in sub-threshold operation [3-6]. Due to its superior short channel control, steeper sub-threshold swing, reduced leakage current, and immunity to Random Dopant Fluctuation (RDF) [7, 8], FinFET-based SRAM emerges as a promising candidate for future low-voltage operation.

1.2 Literature Review and Motivation

There were more and more various sub-threshold SRAM cells in bulk CMOS have been proposed to improve cell stability. Fig. 1.3 illustrates several bulk CMOS sub-threshold cell structures reported in the literature [4-6]. B. H. Calhoun *et al.* [4] used 10T bit-cell to decouple Read path that could eliminate Read disturb. Transistors of M7 to M10 reduce the bit-line leakage significantly. The worst-case SNM for this cell is just like Hold SNM, thus butterfly curve is opened during Read operation. Compared with 6T, the area increases 66%, leakage power reduces 2.25X and V_{CC} min is 0.3V. T.-H. Kim *et al.* [5] modified previous 10T structure [4] for data-independent bit-line leakage. In this cell structure, the bit-line leakage current

flow through PMOS (M10) and NMOS (M9) is almost constant instead of relating to storage node data value, so it is more robust for high density sub-threshold SRAM. V_{CC} min is 0.2V @ 1024 cells per bit-line. I. J. Chang *et al.* [6] proposed differential 10T cell. It has double word-line structure, W_WL for column direction and WL for row direction. Without half select problem that provides bit-interleaving structure for solving soft error rate problem, and V_{CC} min is 0.16V with boosting 80mV word-line voltage.

In particular, Schmitt Trigger based feedback mechanism [3, 9] also has been used to improve the RSNM, Write-ability, and to improve the tolerance to process variation. As shown in Fig. 1.4 (a) [3] and Fig. 1.4 (b) [9], these 10T Schmitt Trigger sub-threshold SRAM cells (designated as ST1 and ST2, respectively) add stacking transistors (NL1 and NR1) and feedback transistors (NFL/NFR in Fig. 1.4(a), and AXL2/AXR2 in Fig. 1.4(b)) to provide the feedback mechanism for conditioning the intermediate node to raise the cell-inverter trip voltage for rising input, thus improving RSNM. These cells have been shown to operate at $V_{CS} \sim 0.15$V. The Schmitt Trigger feedback mechanism has also been shown to improve the tolerance to process variations [3, 9].

With the capability of independent gate control in double-gate FinFET devices, a few novel cell structures have been proposed [10-13] (shown in Fig. 1.5). These cells have been investigated in sub-threshold region [14]. In [14], the result shows that because of Write failure, some of these cells are not properly using in sub-threshold region, and all of these cells do not have immunity to process variation. Therefore, there is still a need for using independently-controlled-gate FinFET devices to find new SRAM cell structure, solving the stability problem in sub-threshold region.

In this work, we propose 3 novel FinFET Independently-controlled-Gate Schmitt Trigger (IG_ST) SRAM cells (shown as IG_ST1, IG_ST2, and IG_ST3 in Fig. 1.6 (a), 1.6 (b), and 1.6 (c), respectively). These cells utilize split-gate FinFET devices with the front-gate devices serving as the stacking devices, and the back-gate devices serving as the intermediate node conditioning devices to provide built-in feedback mechanism for Schmitt Trigger action, thus reducing the cell transistor count/area and achieving improved SNM and better tolerance to process variations and random variations. In this work, we evaluate and compare the cell stability, leakage, area, performance, and tolerance to process variations and random variations of the proposed cells with conventional 6T SRAM cell and previously reported 10T Schmitt Trigger SRAM cells for sub-threshold operation using TCAD 3D mixed-mode simulations [15].

1.3 Organization

In chapter 2, the basic operations of conventional 6T, the previous 10T Schmitt Trigger sub-threshold SRAM cells and proposed 8T Schmitt Trigger sub-threshold SRAM cells are described. Chapter 3 investigates the cell RSNM, WSNM, HSNM and with considering self-heating and temperature dependence, and cell leakage in sub-threshold region. The cell layouts, areas, and cell AC performance (such as cell Read access time, cell Write time (Time-to-Write), Read access time versus the number of cells per bit-line considering worst-case data pattern for bit-line leakage, and temperatures dependence) are assessed based on scaled ground rules from 32 nm node in Chapter 4. In Chapter 5, describe the methodologies of LER (Line Edge Roughness), and then 3D mixed-mode Monte Carlo simulations are performed to

evaluate the impacts of local random variations, notably the Gate LER and Fin LER on FinFET SRAM stability. The combined effects with main process variations (L_{eff} and $W_{fin}(T_{si,})$) are then strictly examined for more robustness of cell stability. For overall robustness of cell stability, the sensitivity of process (L_{eff}, EOT, $W_{fin}(T_{si,})$, and H_{fin}) is also discussed. In the end of chapter 5, introduce another probability of local random variation – work function variability (WFV). The conclusion of the paper is given in Chapter 6.
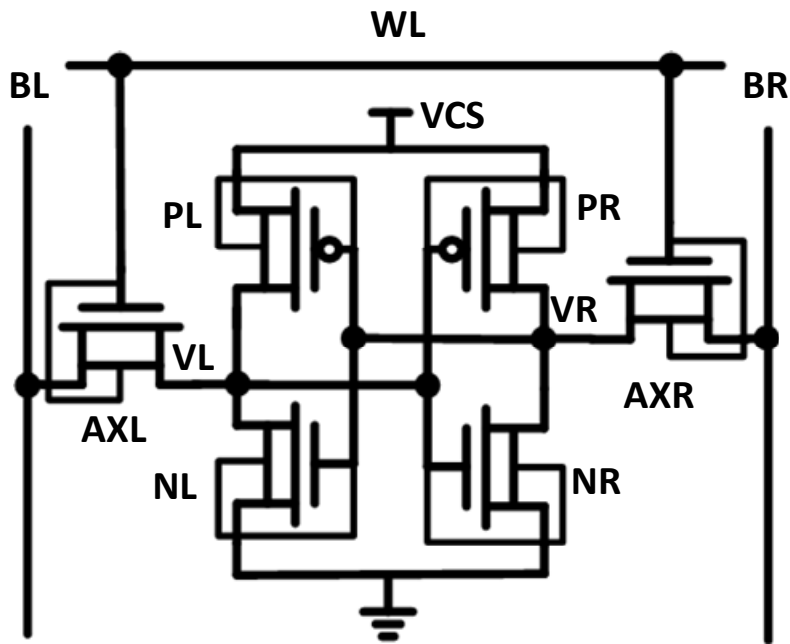
Fig. 1.1. Schematic of conventional 6T (6T).
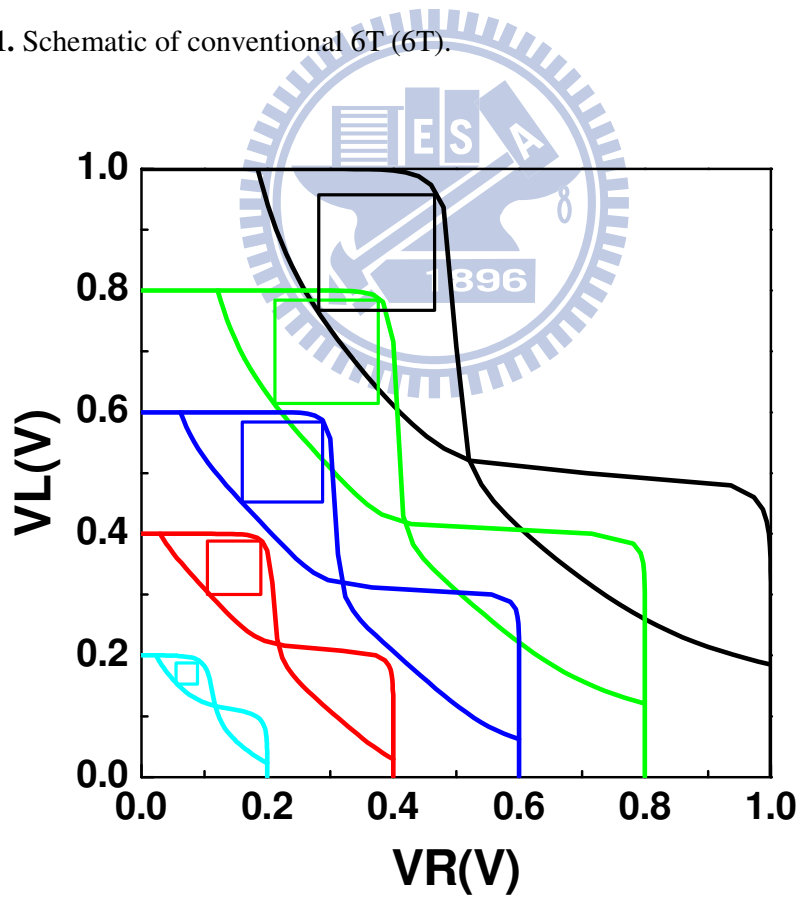
Fig. 1.2. The stability of 6T deteriorates significantly.
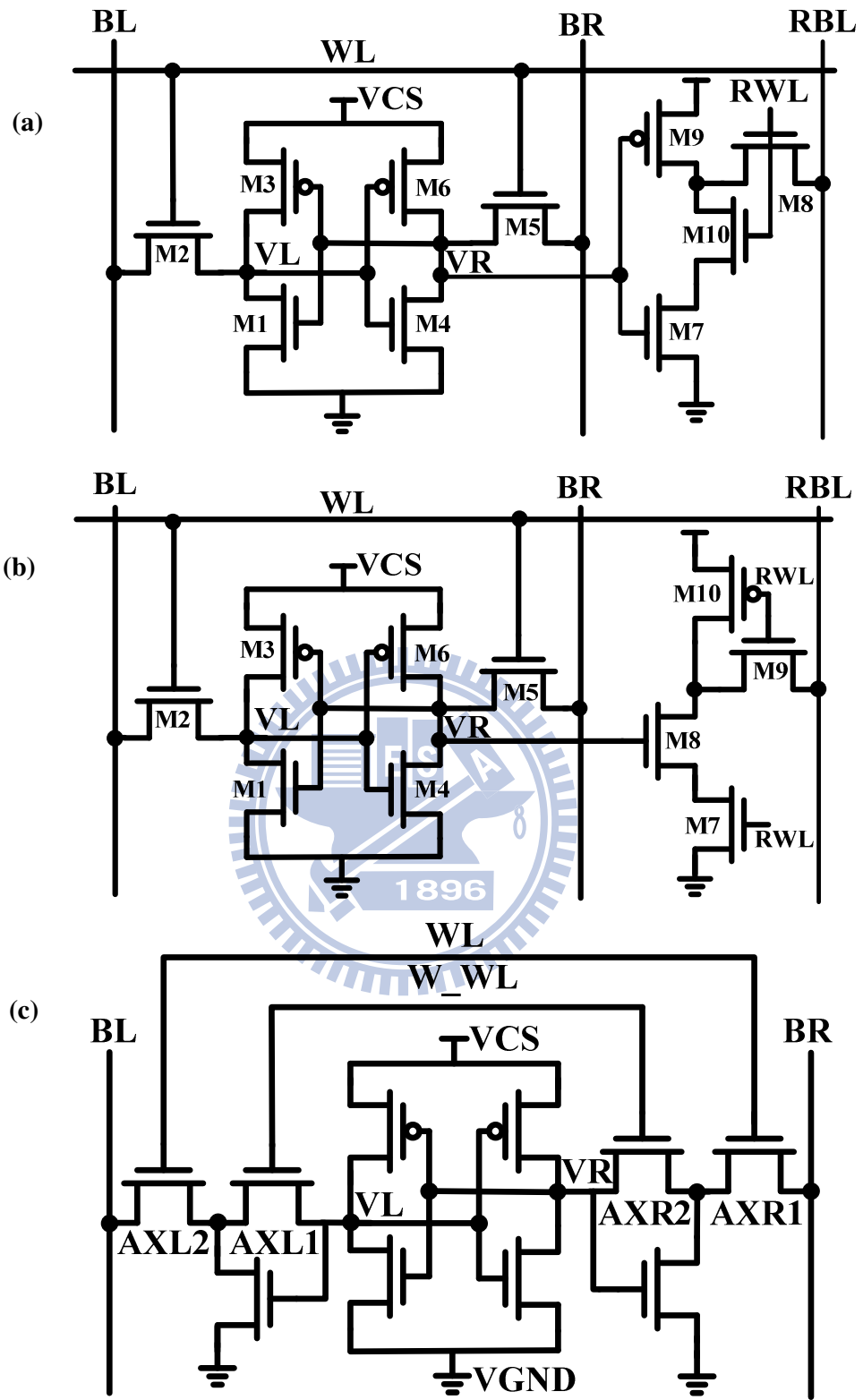
Fig. 1.3. Schematic of various bulk CMOS sub-threshold cells: (a) 10T [4], (b) high-density 10T [5], (c) fully differential 10T [6].

Fig. 1.4. Schematic of various FinFET cells: (a) Schmitt Trigger 10T (ST1) [3], and (b) Schmitt Trigger 10T (ST2) [9].
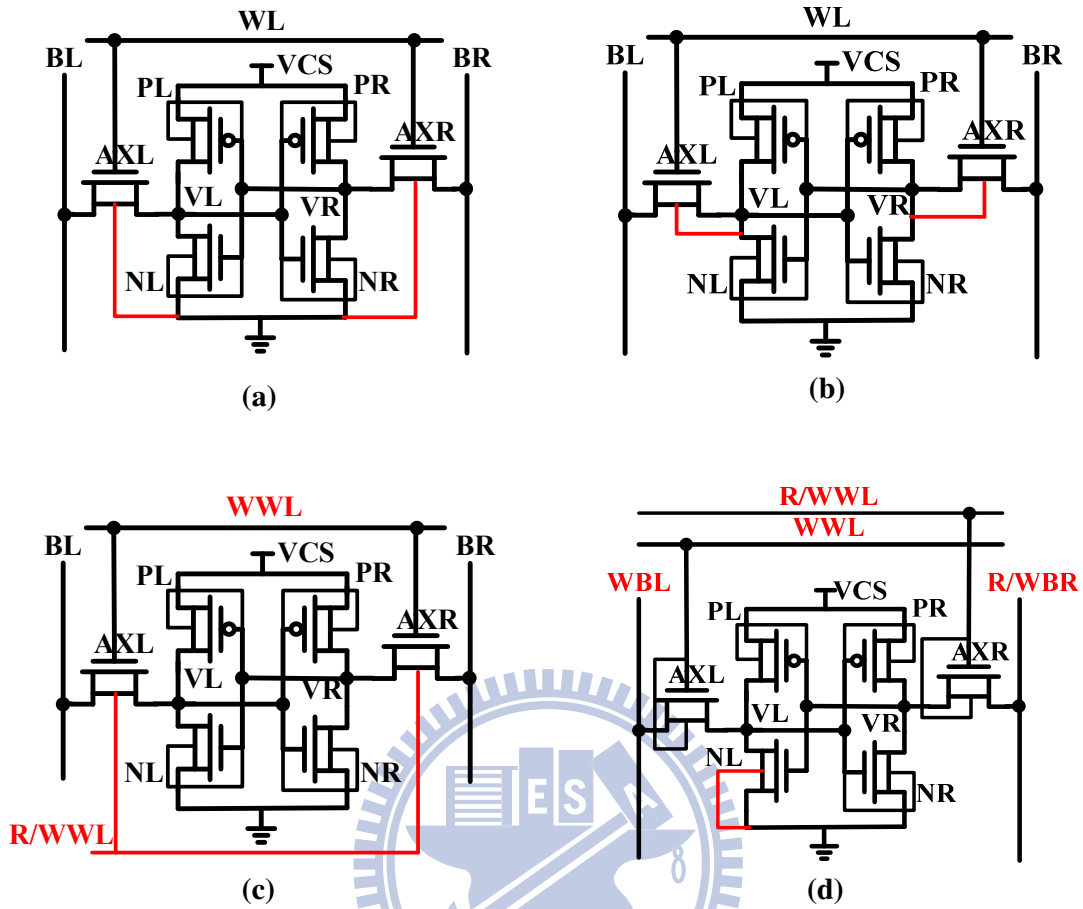
Fig. 1.5. Schematic of various independently-controlled-gate FinFET cells: (a) Ying-Yang feedback 6T [10], (b) improved Ying-Yang feedback 6T [11], (c) double word-line 6T [12], and (d) asymmetrical 6T [13].
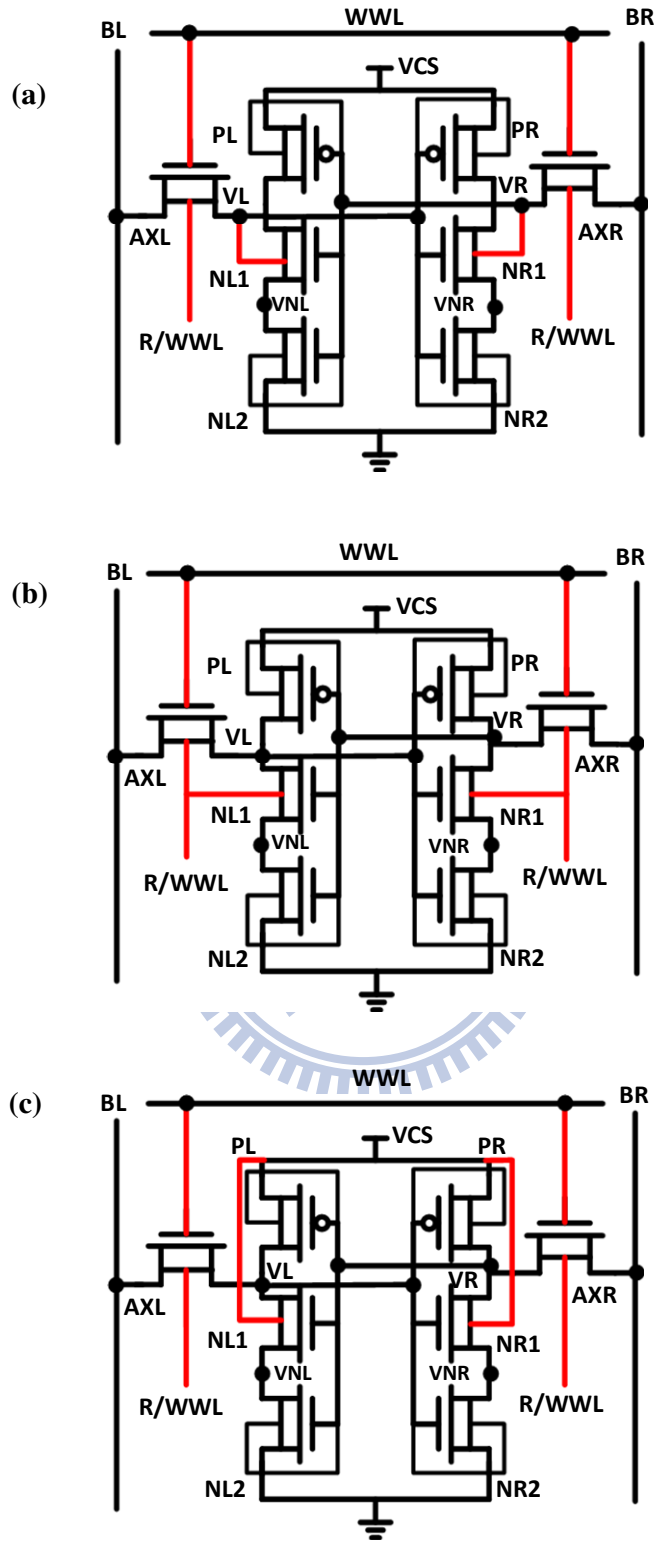
Fig. 1.6. Schematic of proposed Schmitt Trigger based Independently-Controlled Gate

FinFET cells: (a) IG_ST1, (b) IG_ST2, and (c) IG_ST3.

Chapter 2

Schmitt Trigger Based FinFET SRAMs

2.1 Introduction

With aggressive scaling of transistor dimensions, the density of transistor in integration circuit is increased more and more today. So that the power consumption will be a significant concern especially in SRAM design. Fig 2.1 shows the effective way to reduce the power consumption by reducing the V_{CS} which can reduce active power quadratically and static leakage power linearly [16]. Therefore, circuit operate in low voltage is important for today SRAM design. However, as supply voltage decreased into sub-threshold region, the sensitivity/stability is severe to process and local random variation [17]. To overcome this problem, some different SRAM cells have been proposed, though none of them have a built-in feedback mechanism to improve the stability under the process variation.

In previous works [3, 9], ST1 and ST2 have been proposed to improve the stability under the process variation. However, the bigger cell area would be another disadvantage factor in SRAM design. In this work, our initial idea is to remain the advantage of Schmitt Trigger action, and also reduces the cell area. Based on this idea, we use the capability of independent gate control in double-gate FinFET devices to create three new cells, thus successfully reduce the cell area. In the following section, we will basically introduce the operation of conventional 6T, ST1 and ST2 cells, and clearly introduce the operation (Read, Write, and Hold mode) of our new cells.

2.2 Conventional 6T SRAM

Fig. 1.1(a) shows conventional 6T cell structure in common SRAM design. This cell has two complementary bit-lines which are used to sensing data or writing data. There is one word-line which controls access transistors (AXR and AXL) to access the cell for Read or Write operation. In Hold mode, The cell consists of a pair of cross-coupled inverters to store the data.

For Read operation, bit-lines are precharged to V_{DD} initially and word-line turns on. Thus, one of the bit-lines will be discharged by pull-down transistor (NL or NR). For an example, assume VL=0 VR=V_{CS}, BL will be discharged by AXL and NL from V_{DD} to 0. In order to accelerate the discharge velocity, sense amplifier (SA) is also one of the important part in SRAM design, which can detect the small differential voltage and transforms into full swing quickly. For Write operation, in order to Write 0 or Write 1, there is one of the bit-lines will first be pulled down by write driver, and then word-line turns on. Thus, data of storage node will be flipped. For an example, assume VL=0, VR=V_{CS}, BL=V_{DD}, and BR=0, VR is going to be pulled to low, and VL will rise to high. Fig. 2.2 shows the schematic of Read/Write operating behavior.

2.3 Previous 10T Schmitt Trigger Cells

In previous works [3, 8], ST1 and ST2 use Schmitt Trigger characteristics to enhance RSNM in low voltage operation. For ST1 (Fig. 1.4(a)), the feedback mechanism from NFR (NFL) that conditions the intermediate stacking node VNR (VNL) is adaptively enabled according to the direction of input transition (1 to 0, or 0

to 1). During Read operation (assume VL=0 VR=V_{CS}), the voltage of VL would rise to V_{read} (Fig. 2.3(a)) due to the voltage divider effect between AXL and pull-down transistors (NL1-NL2). If V_{read} is higher than the switching threshold V_{trip} (Fig. 2.3(a)) of the opposite cell inverter (PR-NR1-NR2), the data in cell storage nodes would be flipped, thus causing Read failure. With the Schmitt Trigger feedback mechanism, the V_{trip} of the inverter (PR-NR1-NR2) is increased due to (1) higher VNR node voltage, which is conditioned to one V_T below VR (= V_{CS}) by the feedback transistor NFR, and (2) higher V_T of NR1 owing to its reverse body-to-source bias. As such, the RSNM improves and the stored data in VL and VR is preserved. The detailed Voltage Transfer Characteristics (VTC) is shown in Fig. 2.3 (c), where the improved RSNM due to higher V_{trip} can be seen. During Write operation (again assume VL=0 VR=V_{CS}), the feedback transistor NFL turns off. Due to series combination of pull-down transistors NL1 and NL2, the V_{trip} of the inverter (PL-NL1-NL2) is raised to higher voltage, resulting in better Write margin and Write-ability.

The ST2 cell uses AXR2 (AXL2) to adaptively control cell inverter switching threshold. The gates of the feedback transistors AXR2 (AXL2) are connected to word-line to provide a firmer/stronger intermediate node conditioning action than that in ST1 where the gates of NFL (NFR) are connected to cell storage nodes. Moreover, during Write operation, AXR2 (AXL2) provides extra path to discharge the cell internal nodes to improve the Write margin and performance. Therefore, both RSNM and Write-ability are further enhanced compared with ST1.

2.4 Proposed 8T Schmitt Trigger Cells

Due to the flexibility of Independently-controlled-Gate (IG) operation in FinFET structure, the role of the Schmitt Trigger feedback transistor could be realized from the existing transistor NR1 (NL1). By splitting the front- and back-gate of NR1 (NL1), one can use the front-gate as the stacking device, and the back-gate as the intermediate node conditioning device to provide built-in feedback mechanism for Schmitt Trigger action, thus reducing the cell transistor count/area.

Three novel SRAM cell structures are proposed in this work. IG_ST1 (Fig. 1.6(a)) forms Schmitt Trigger feedback path by connecting the back-gate of NR1 (NL1) to cell storage node VR (VL). During Read operation (assume VL=0 VR=V_{CS}), the feedback mechanism is enabled with the node voltage VNR conditioned to one diode drop (V_T) below VR by the back-gate of NR1, thus increasing V_{trip} of the cell inverter (PR-NR1-NR2) and improving the RSNM. Notice that as VL rises and VR falls, the feedback (intermediate node conditioning) mechanism becomes weaker and the switching slope (steepness) of IG_ST1 cell would degrade. Notice also that split-gate configuration is used for the access pass-transistor AXL (AXR), so only one gate is enabled during Read to reduce Read disturb, while both gates are enabled during Write to improve Write-ability and performance. During Write operation (assume VL=0 VR=V_{CS}), due to reduced NL1 strength with its back-gate connected to VL (= 0), and the series NL1-NL2 pull-down configuration, the trip voltage of the left cell inverter (PL-NL1-NL2) is raised, thus further improving the Write-ability.

In IG_ST2 (Fig. 1.6(b)), the back-gates of NR1 (NL1) and AXR (AXL) are connected to the R/WWL. The connection of the back-gates of NR1 (NL1) to R/WWL provides a firmer/stronger intermediate node conditioning action, and a steeper switching transition (since the back-gate of NR1 is always "High" during

Read) than IG_ST1. Furthermore, during Write operation (VL=0 VR=V_{CS}), due to stronger NL1 with its back-gate always at "High", its Write-ability is slightly degraded with respect to IG_ST1 cell.

In IG_ST3 cell (Fig. 1.6(c)), the back-gates of NR1 (NL1) are connected to V_{CS}. Therefore, the cell would preserve the Schmitt Trigger feedback mechanism even when the R/WWL and WWL are turned off (i.e. Hold mode). In Read and Write mode, IG_ST3 cell has the same Schmitt Trigger feedback mechanism as IG_ST2 cell. Hence, IG_ST3 would have better HSNM, and the same RSNM and WSNM compared with IG_ST2 cell.

Fig. 2.4(a) shows the FinFET device structure studied in this paper and Fig. 2.4(b) shows the tied-gate and independently-controlled-gate configurations [10]. Our analyses are based on FinFET device with N_a=1×10^{17}cm^{-3}, L_{eff}=25nm, $W_{fin}(T_{si,})$=7nm, H_{fin}=20nm and EOT=0.65nm, consistent with the ITRS Roadmap projection. The threshold voltage of the devices are V_{TN} ~ 0.43 V and V_{TP} ~ 0.45 V. The Framework of following TCAD 3D mixed-mode simulations including DC (SNM) and AC (Read and Write time) metrics are illustrated in Fig. 2.5, using individual transistors for various SRAM cells, and our simulations are based on drift-diffusion equations.

2.5 Summary

In this chapter, we introduce basic conventional 6T Read/Write operation, and then introduce the characteristic of Schmitt Trigger Based 10T cells (ST1 and ST2). The main advantage of ST1 is increasing Read stability and has built-in process

variation tolerance. The improved version ST2 gain lower Read disturb and better Write margin at the cost of two word-lines structure.

In this work, we reduced two transistors to create FinFET Schmitt Trigger cells. IG_ST1 use storage node connecting to back-gate of feedback transistor for Schmitt Trigger action, IG_ST2 use R/WWL connecting to back-gate of feedback transistor for Schmitt Trigger action, and IG_ST3 use supply voltage connecting to back-gate of feedback transistor for Schmitt Trigger action. It is detailed to explain the operation of three proposed new cells, including Read, Write and Hold mode.
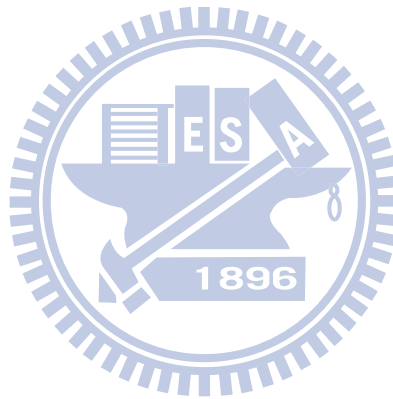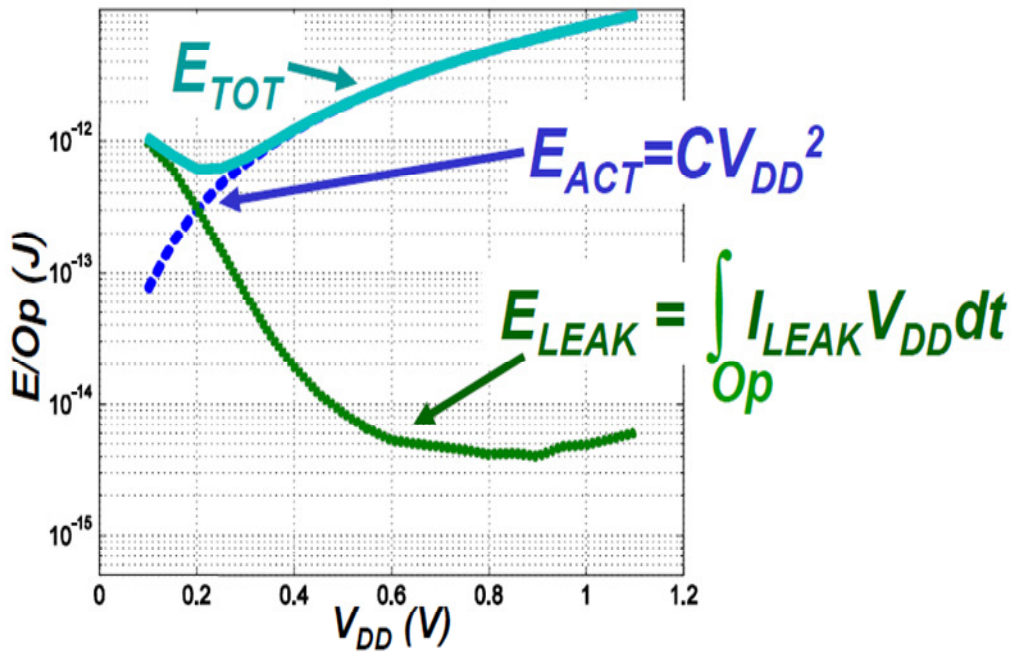
Fig. 2.1. Active, static, and total energy consumption versus V_{DD} [16].
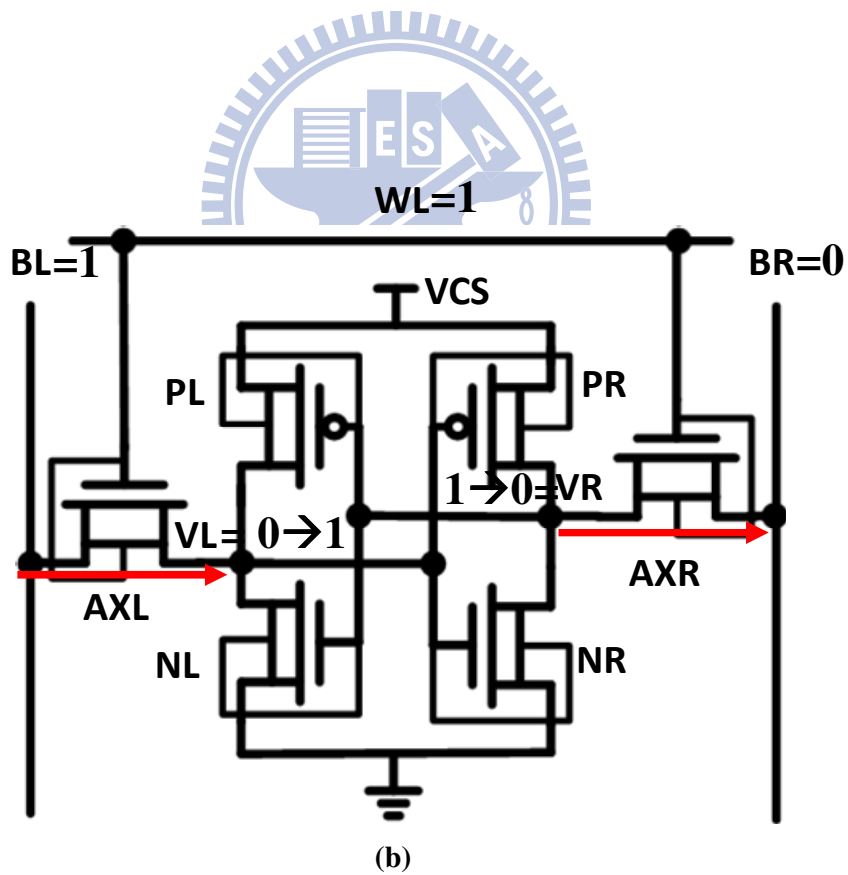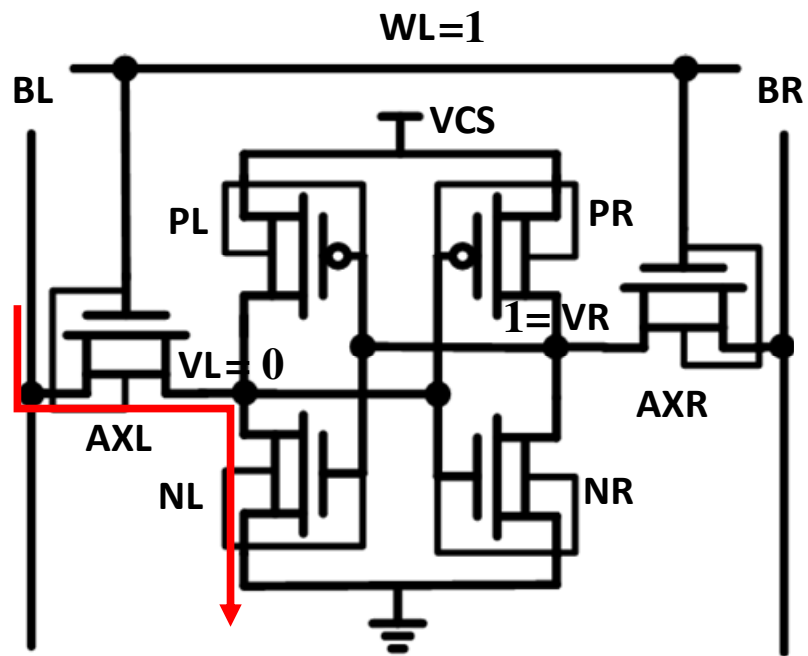
Fig. 2.2. Schematic of 6T (a) Read, and (b) Write operation.
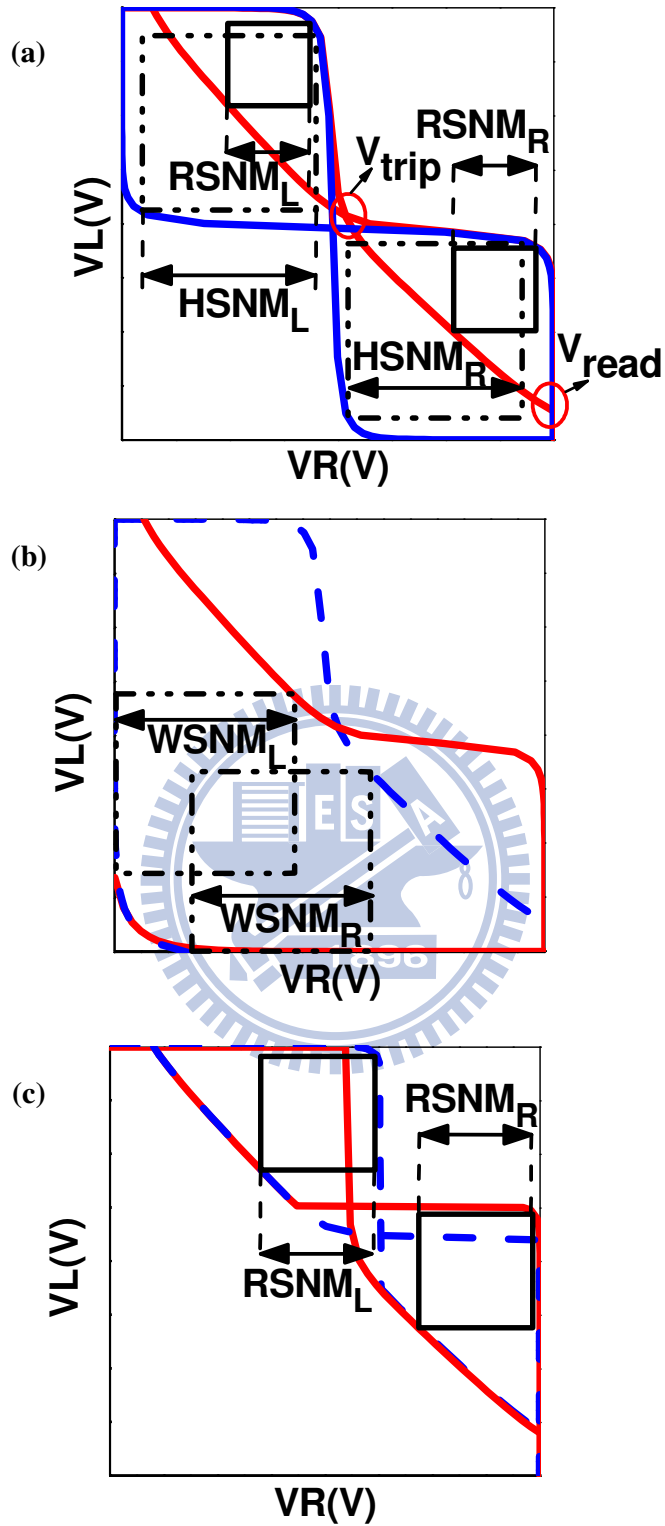
Fig. 2.3. Voltage transfer characteristic curves used to calculate SNM: (a) Read and Hold mode, (b) Write mode, and (c) ST1 in Read mode.

(a)
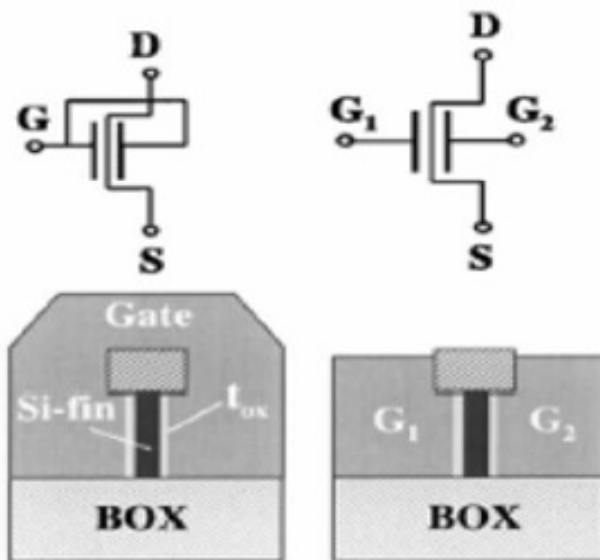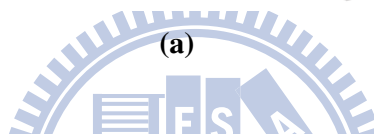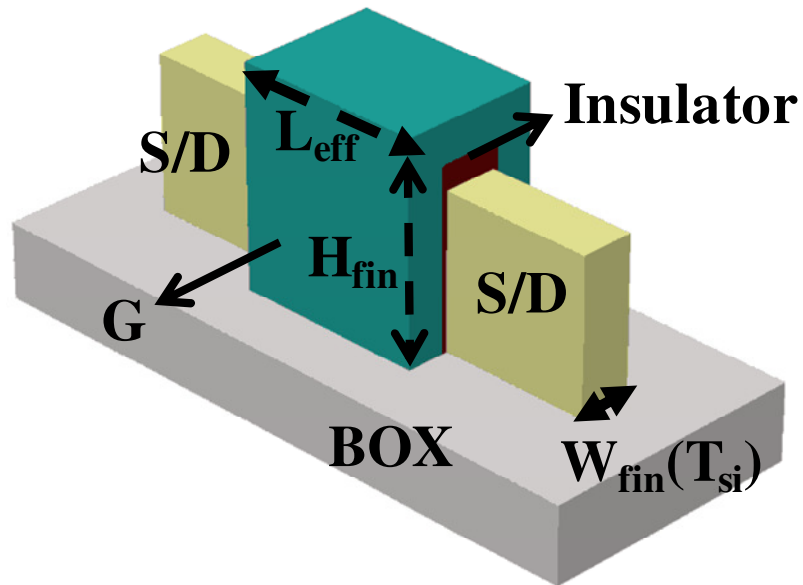
(b)

Fig. 2.4. (a) FinFET device structure, and (b) tied-gate and independently-controlled-gate configurations [18].

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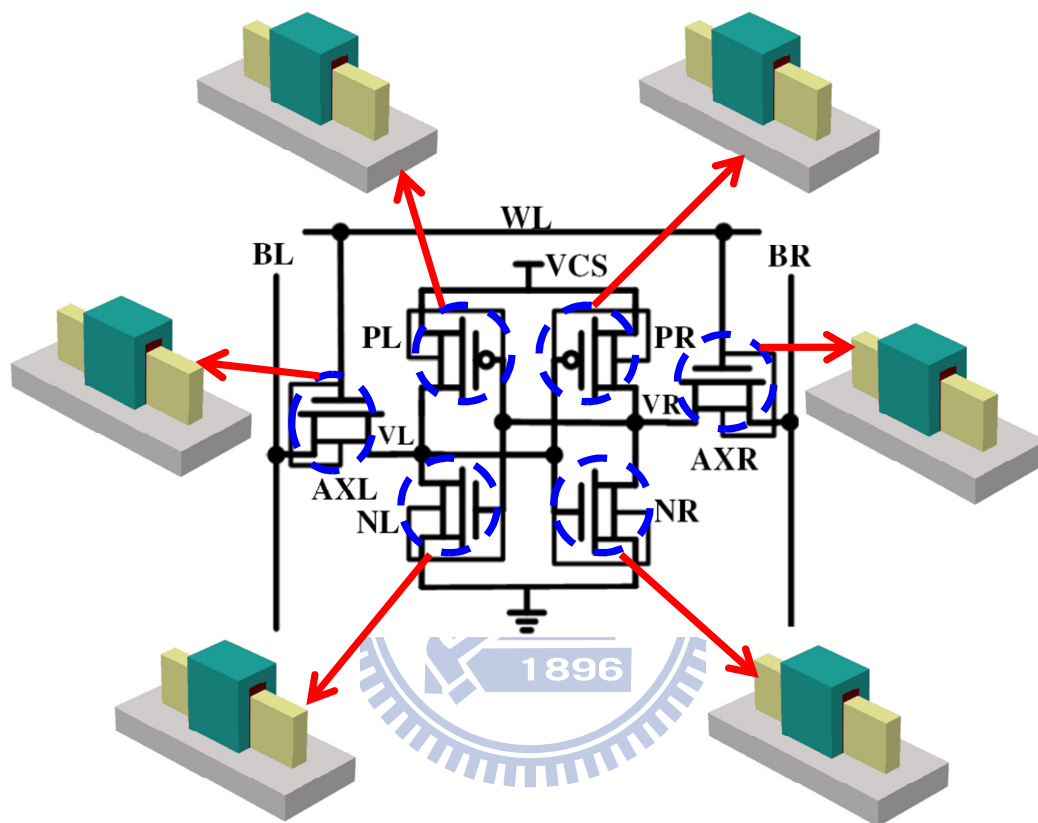
Fig. 2.5. Framework of TCAD 3D mixed-mode simulations.

Chapter 3

SNM and Standby Leakage Current Analysis

3.1 Introduction

Static Noise Margin (SNM) is a common criterion to investigate SRAM cell stability in DC mode, which is including Read, Write, and Hold mode. The RSNM is defined as the length of a side of maximum square that can fit inside the butterfly curves in Read mode [19], and the minimum of $RSNM_L$ and $RSNM_R$ is chosen as the cell RSNM (Fig. 2.3(a)). The HSNM is defined similar to RSNM with the cell in Standby (Hold) mode. The WSNM is defined as the minimum square spanning between the curves in Write mode (Fig. 2.3(b)), and the smaller of $WSNM_L$ and $WSNM_R$ is chosen as the cell WSNM. Due to the asymmetrical Voltage Transfer Curves (VTC) for ST1 cell (the direction of input transition (1 to 0, or 0 to 1)), the corresponding RSNM is as shown in Fig. 2.3(c). In this chapter we will comprehensively compare RSNM, WSNM, and HSNM with these sub-threshold SRAM cells.

Previous section has mentioned that static power consumption would be a critical concern when SRAM operates in sub-threshold region. In [3], this paper indicated that as the same Read failure probability, ST1 cell can save 18% static leakage power than 6T cell. But under this condition, ST1 operates at 175 mV lower supply voltage than 6T cell. In this chapter, for the fair comparison, we set the same supply voltage (V_{CS}=0.4V) to compare all the cells' static leakage current.

3.2 Comparison of Read, Write and Hold SNM

In Fig. 3.1 (a), the normalized nominal RSNM of different cells are compared in sub-threshold region (V_{CS} = 0.4V). With the help of feedback mechanism, Schmitt Trigger based cells show significantly better nominal RSNM (35% - 81%) than the conventional 6T cell. In particular, IG_ST2 and IG_ST3 have the most significant improvement in nominal RSNM (~81%) due to their steeper switching characteristics. In Write mode (Fig. 3.1(b)), Schmitt Trigger based cells also show better nominal WSNM (1% to 33%). The improvement is most significant for ST2 cell due to its two parallel discharging paths for cell internal nodes and tied-gate pass-transistor configuration. In Hold mode (Fig. 3.1(c)), IG_ST1 and IG_ST2 have slightly lower nominal HSNM due to the split-gate configuration of NL1 (NR1) which slightly degrades the switching slope (steepness). Notice that IG_ST1 maintains the feedback mechanism even in Hold mode, as the intermediate node VNL (or VNR) is still conditioned by the back-gate of NL1 (or NR1) to one V_T drop below the "High" cell storage node. Also the V_T of the front-gate of NL1 (or NR1) will be lower due to gate-to-gate coupling. The switching transition also tends to be soft as the feedback mechanism weakens and eventual diminishes with the switching transition.

For IG_ST2 in Hold mode, the back-gates of NL1 (and NR1) are at "Low", hence there is no feedback mechanism. The V_T of the front-gates of NL1 and NR1 will be a little bit higher due to gate-to-gate coupling, thus V_{trip} tends to be a little higher. The HSNM, however, does not constitute a limitation on SRAM stability, while RSNM does. IG_ST3 exhibits HSNM comparable to (1% better) 6T cell since it preserves the Schmitt Trigger feedback mechanism in Hold mode. The stability of the

cells operating at ultra-low-voltage is assessed in Fig. 3.2. It can be seen that RSNM is most critical for the supply voltage range from 0.4V down to 0.15V. Furthermore, the improvements of RSNM of the proposed cells over 6T cell become more significant as the supply voltage decreases. For IG_ST2 and IG_ST3 cell, the improvement increases from 81% to 110% as V_{CS} scales from 0.4V to 0.15V.

Notice that during Write operation, both R/WWL and WWL are turned on, so both the front- and back-gate of the access pass-transistor AXL (AXR) are enabled. As such, the half-select disturb along the selected WL is more serious than the half-select disturb during Read operation. Notice also that other sub-threshold SRAM cells, like those in [4, 5], and previously reported 10T Schmitt Trigger sub-threshold SRAM cells [3, 9] have similar Write half-select disturb constraint. Therefore, non-bit-interleaving architecture or Byte Writing architecture should be used to best exploit the improved RSNM of these sub-threshold SRAM cells.

3.3 Self-Heating and Temperature Dependence on Sub-threshold SRAM Stability

Compared with bulk device, due to lower thermal conductivity (κ) in thin-film silicon layer on insulator devices (PDSOI, FDSOI, and FinFET), these devices have self-heating problem [20]. With the calibrated thermal conductivity data [21], thermal conductivity (κ) of thin-film is 15 W m^{-1}K^{-1}. Fig. 3.3 shows device temperature versus various V_{DD}. As can be seen, in sub-threshold region (V_{DD}=0.4V), device temperature keeps as ambient temperature. Therefore, it seems that self-heating can negligible in sub-threshold region. The lattice temperature

distribution of our simulation devices at V_{DD}=0.4V and V_{DD}=1V is shown in Fig. 3.4.

Fig. 3.5 shows RSNM comparison of various cells at V_{DD}=0.4V versus temperature. We accessed with and without self-heating for RSNM comparison. Because cell operates in sub-threshold region (V_{DD}=0.4V), no matter considering self-heating or not, RSNM comparison of various cells are the same. It can be seen, RSNM of all cells slightly degrade ~10 mV as increasing temperature from 250K to 400K. This is because at 400K that sub-threshold swing is degraded [22] and operates in super-threshold region resulting higher V_{read} [23]. For an example, In Fig. 3.6, 6T butterfly curves of 250K and 400K are shown to explain this phenomenon.

3.4 Comparison of Standby Leakage Current

In sub-threshold region, static leakage power is a dominant source for power consumption. When SRAM operates in Standby mode, the schematic for leakage current path for 6T is shown in the Fig. 3.7. The conditions of cell storage nodes are VR="Low" and VL="High".

Fig. 3.8 compares the Standby leakage current of different cells. The conditions of cell storage nodes are VR="Low" and VL="High". Compared with 6T cell, Fig. 3.9 illustrates that ST1 and ST2 have extra leakage path through NFR and AXR2, and therefore exhibit 36% and 19% higher Standby leakage current, respectively. The proposed cells leakage path illustrate in Fig. 3.10. Without extra cell leakage path, IG_ST1 and IG_ST3 show slightly lower leakage (4%) compared with 6T cell. Moreover, IG_ST2 cell, with the back-gate of the stacking transistor (NL1/NR1) off

in Standby, reduces up to 21% cell leakage current compared with 6T cell.

3.5 Summary

We have analyzed overall SRAM stability, including Read, Write, and Hold mode. Schmitt Trigger based cells could significantly have better nominal RSNM (35% - 81%) than the conventional 6T cell. In particular, IG_ST2 and IG_ST3 have the most significant improvement in nominal RSNM (~81%). Write ability of Schmitt Trigger based cells are slightly improved due to stacked pulled-down NMOS transistors. In Standby mode, stability is more robust than Read mode. In particular, As V_{CS} scales from 0.4V to 0.15V, for IG_ST2 and IG_ST3, the RSNM improvement increases from 81% to 110%.

With considering self-heating in FinFET devices, device temperature is not impacted by self-heating effect in sub-threshold region (V_{DD}=0.4V). Furthermore, in SRAM level simulations, increasing temperature from 250K to 400K, RSNM is slightly degraded 10 mV for each cells.

In the second part, cell leakage analysis has been investigated. At V_{CS}=0.4V, due to extra leakage path through feed-back transistors, ST1 and ST2 cells exhibit 36% and 19% higher Standby leakage current, respectively. Our proposed cells can save 20% to 50% cell leakage current than previously reported ST1 and ST2 cells, because of the stacking transistors.
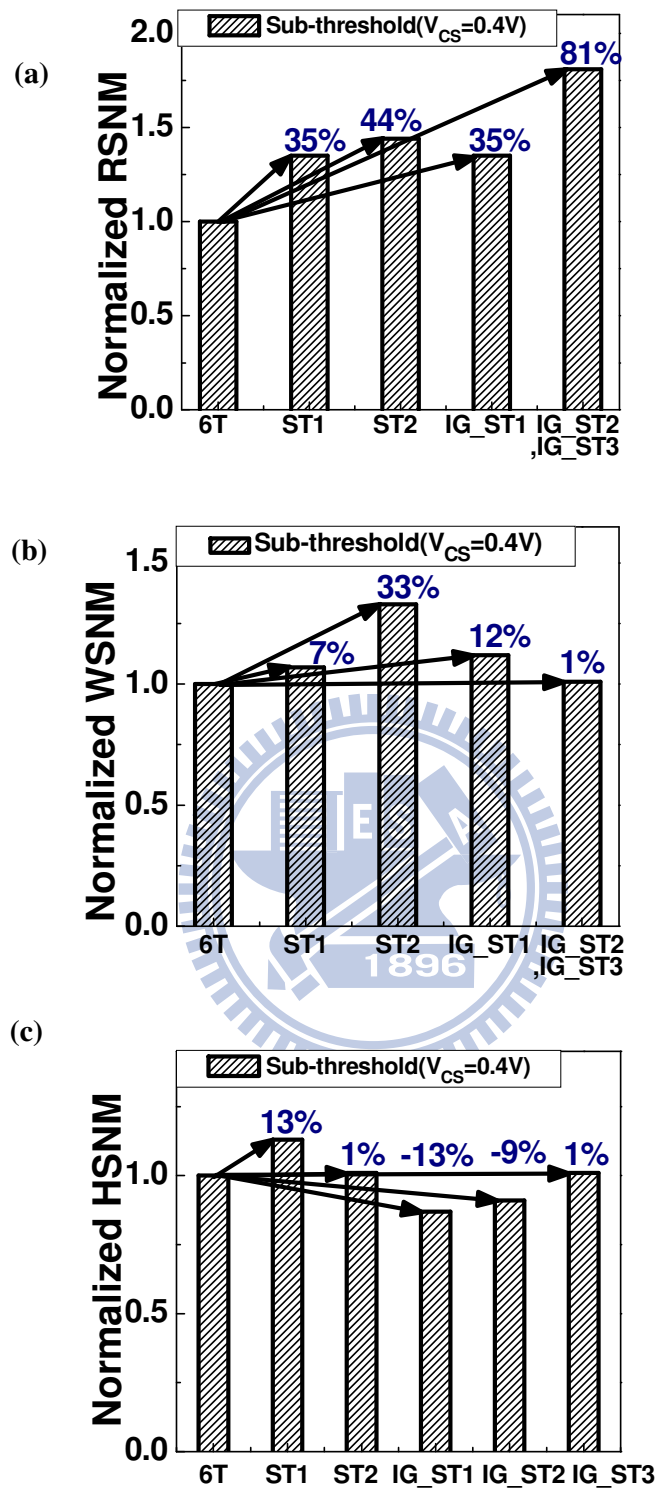
Fig. 3.1. Comparison of normalized nominal (a) RSNM, (b) WSNM, and (c) HSNM for different cells.
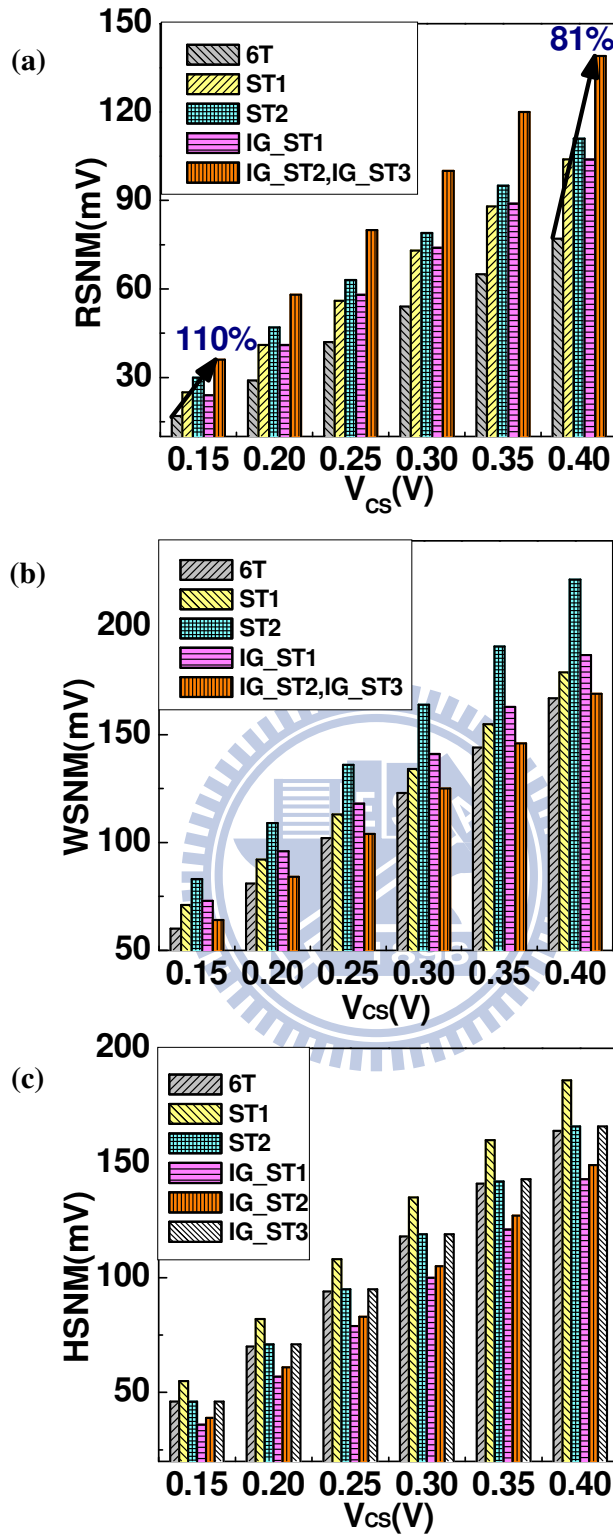
Fig. 3.2. Comparison of nominal (a) RSNM, (b) WSNM, and (c) HSNM in ultra-low voltage operation.
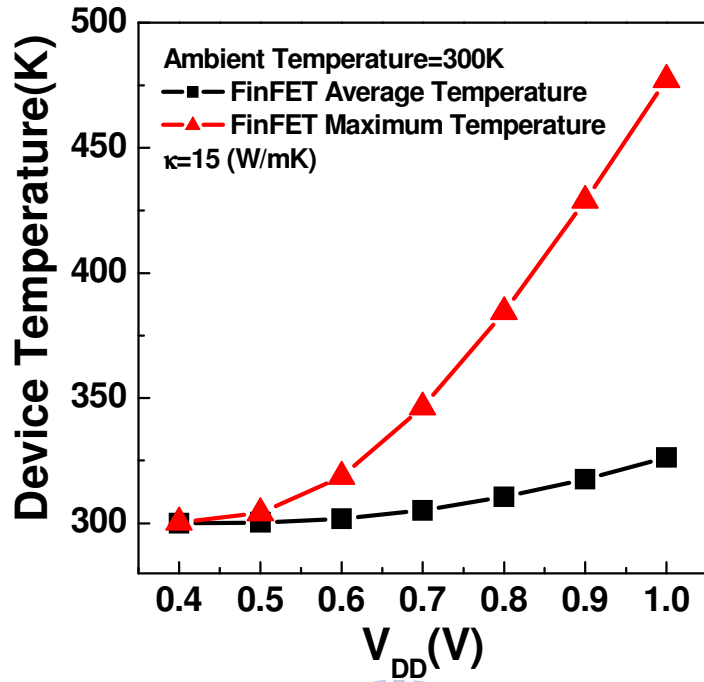
Fig. 3.3. Impact of V_{DD} on the device average and maximum temperature FinFET SOI

device (ambient temperature is set to 300K).

(a)   (b)
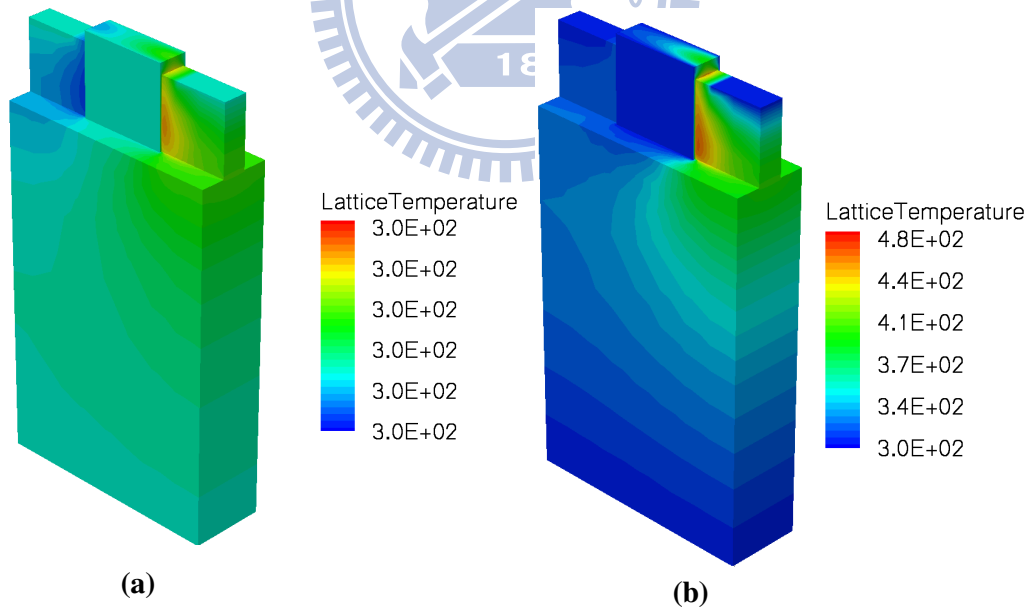
Fig. 3.4. Temperature distribution in whole FinFET device at (a) V_{DD}=0.4V, and (b)

1V respectively.
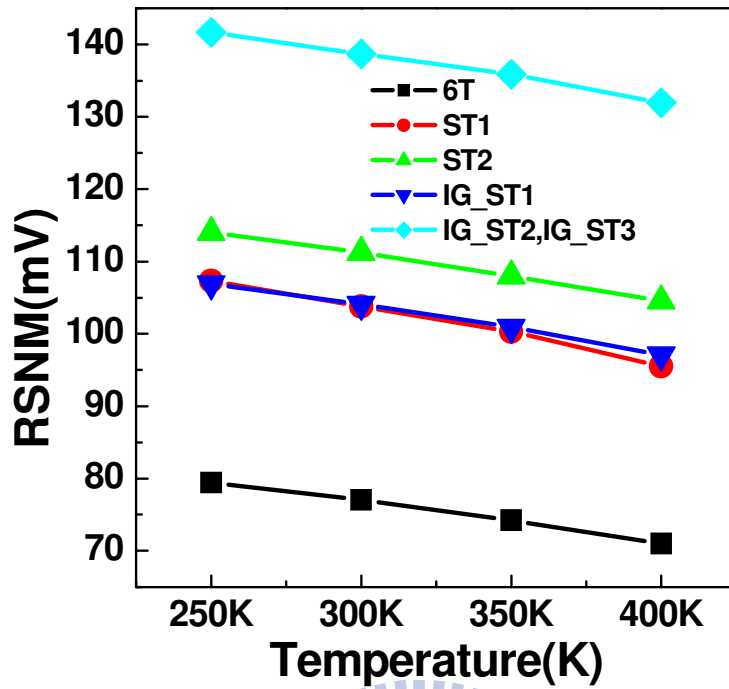
Fig. 3.5. Impact of temperature on RSNM for various FinFET sub-threshold cells.
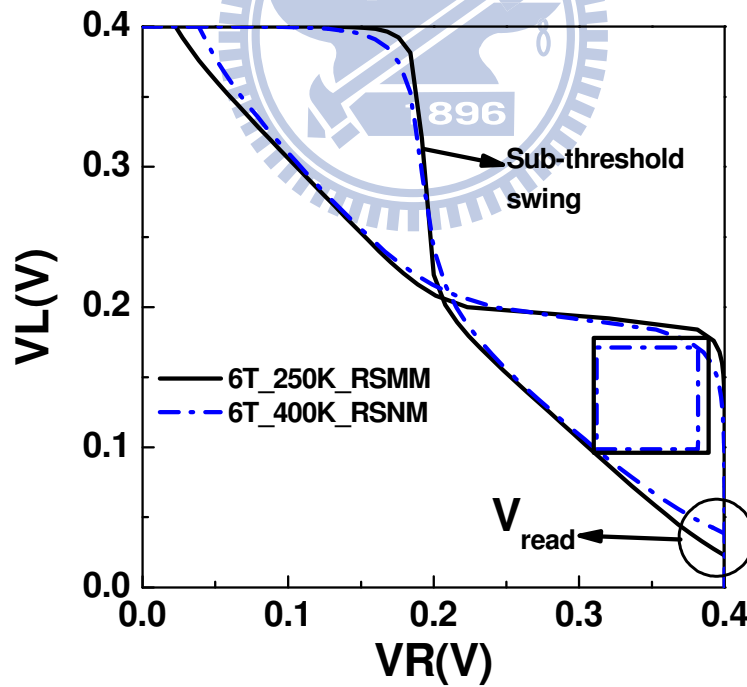
Fig. 3.6. Butterfly curves of 6T degrade at high temperature (400K) which is because of degradation of sub-threshold swing and higher V_{read}.
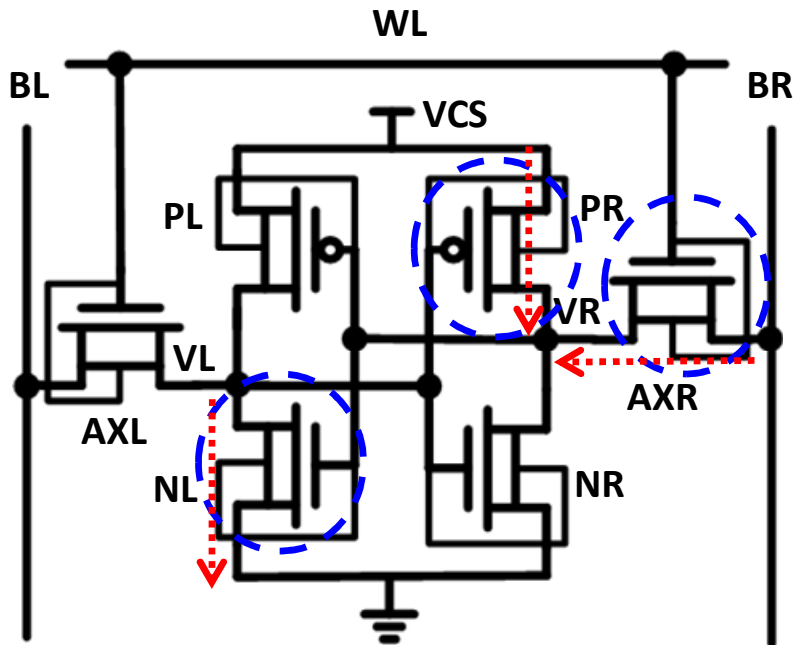
Fig. 3.7. Schematic of Standby leakage path for 6T.
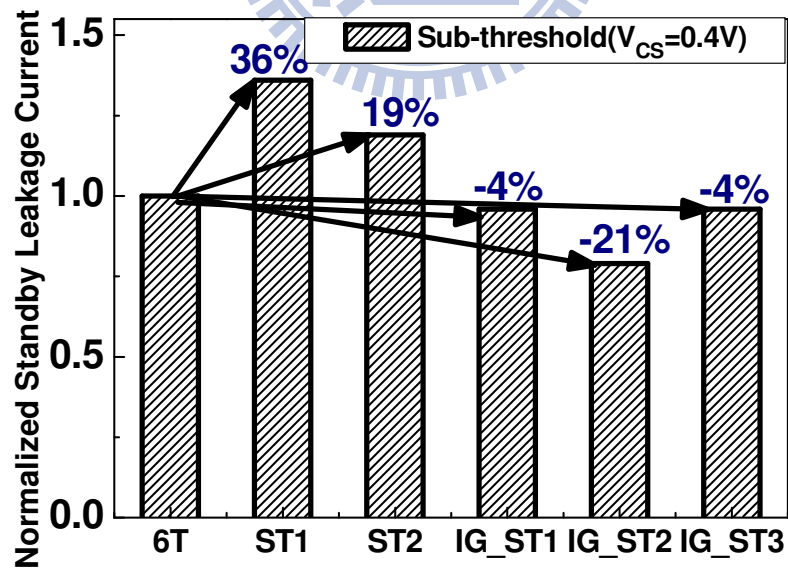
Fig. 3.8. Comparison of cell Standby leakage current (at V_{CS} = 0.4V) of various cells.
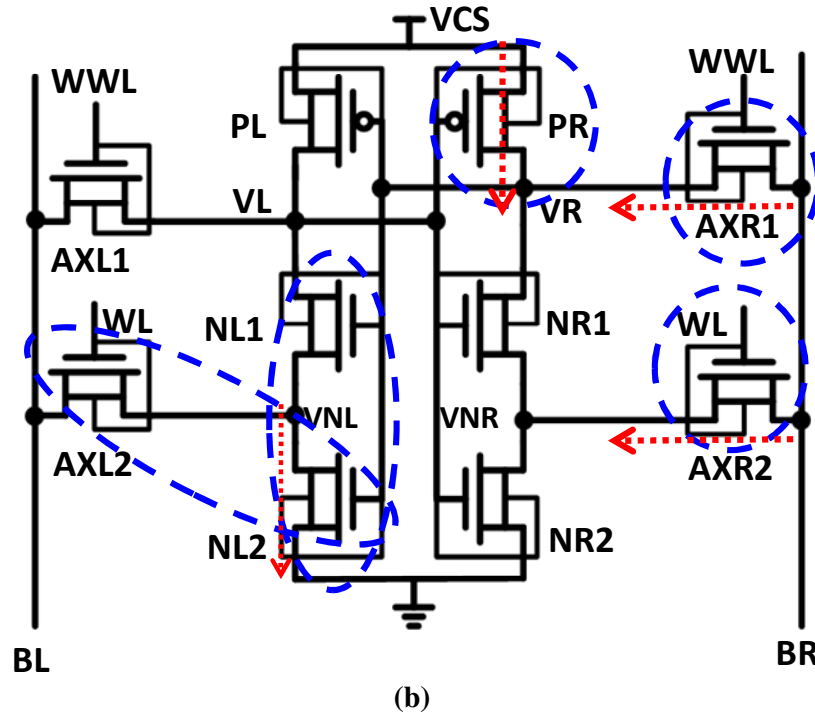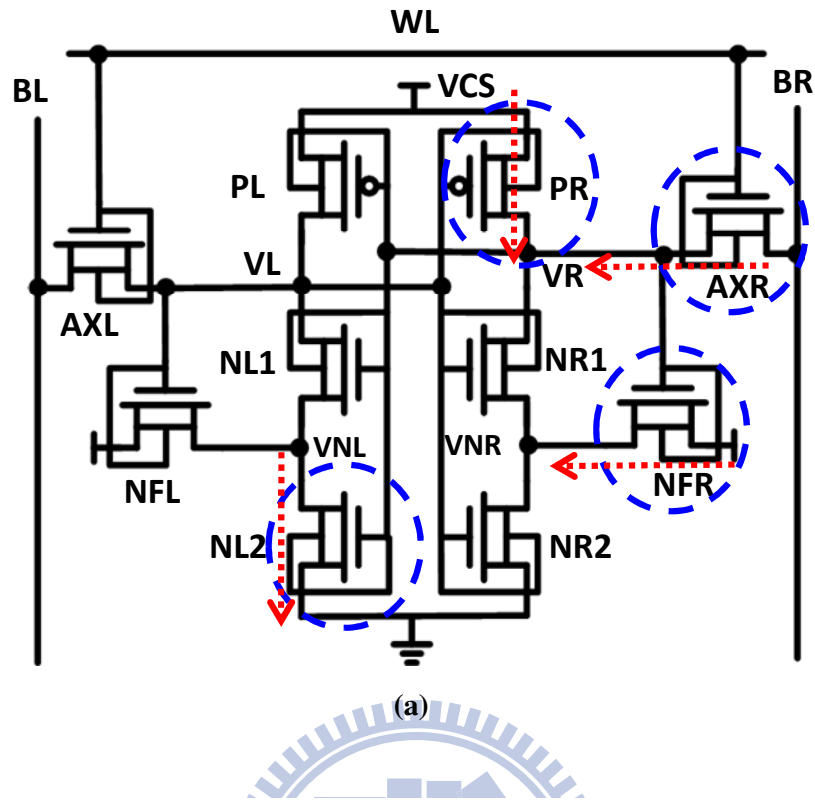
Fig. 3.9. Schematics of Standby leakage path for (a) ST1 and, (b) ST2.
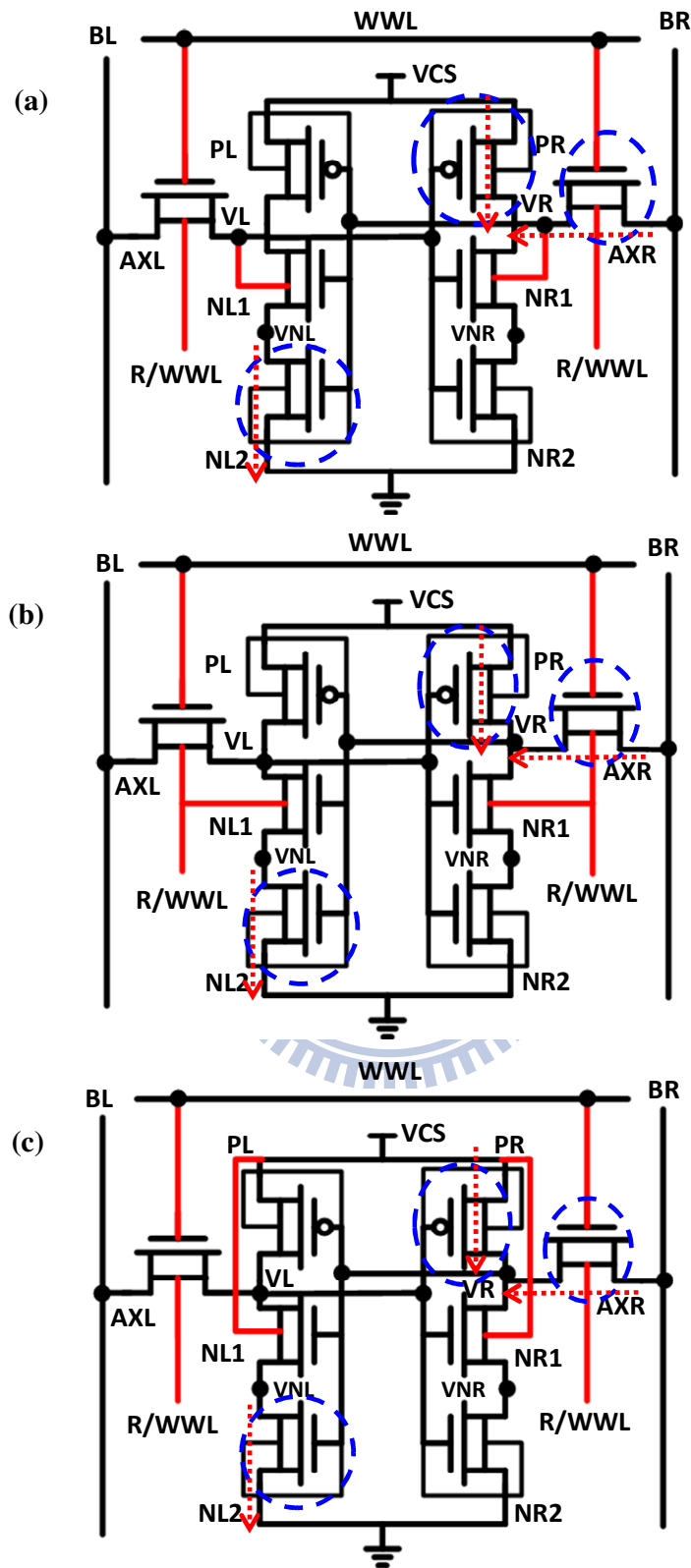
Fig. 3.10. Schematics of Standby leakage path for (a) IG_ST1 , (b) IG_ST2, and (c) IG_ST3.

Chapter 4

Cell Area and AC performance

4.1 Introduction

Area of SRAM is usually the biggest part in whole chip area today ~ 90% [24]. Schmitt Trigger based cells use adding extra transistors to gain better stability, but at the expense of increased area. Due to various cell structures, the layouts are in different way. In this chapter, we will illustrate one possible "thin cell" layout for various cells, and estimate the corresponding area overhead.

We have investigated various SRAM cells stability in DC mode. On the other hand, transient (AC) analysis is a need to show the timing information in Read and Write mode. In the following section, we can get a capacitive load onto each bit-line from estimated cell height and then evaluate Read time and Write time (Time-to-Write). In order to make sure successful Read in the worst SRAM bit-line pattern, the worst-case bit-line leakage current has been considered. In addition, increased leakage current caused by temperature also has been considered with worst-case bit-line leakage current.

4.2 Area Comparison

M. Khare *et al.* [25] claimed that the "thin-cell" layout is a better type for SRAM cell layout compared to "conventional-cell" layout. The 6T "conventional-cell" layout

is shown in Fig. 4.1. It can be seen, height of this type cell layout (bit-line track direction) is longer than width (word-line track direction) and metal (polysilicon) lines are not in the same direction. "Thin-cell" represents the length to width ratio, and the shape is just like elongated rectangle. All metal (polysilicon) lines are in the same direction in "thin cell" which is friendly in lithography and offers better process window. Another advantage is "thin-call" layout reduces bit-line capacitance load for performance.

Based on published design rules of 32 nm technologies [26-28] and scaling factor from ITRS Roadmap, the cell area of various FinFET SRAM cells are estimated and compared. Table 1 summarizes the pertinent layout design rules used in this work. In Fig. 4.2, we illustrate the layouts of different cells and estimate the corresponding area overhead. We establish a standard 6T thin-cell layout [29] which requires 4.5 fin pitch in horizontal dimension and 2 contacted gate pitch in vertical dimension, and the area is 0.09 μm^2. For ST1 and ST2 cells, extra feedback (NFL (NFR) and AXL2 (AXR2)) and stacking (NL1 (NR1)) transistors result in increase of 69% and 50% in horizontal and vertical dimension, respectively. Furthermore, extra Metal-2 track is required to connect the internal nodes. In contrast, our proposed cells could reduce the areas occupied by the two feedback transistors (horizontal dimension) and the contacts at NL2 (NR2) drain side (vertical dimension). As shown in Fig. 4.3, the proposed cells (IG_ST1, IG_ST2 and IG_ST3) can save 30% - 39% area compared with ST1 and ST2 cells.

4.3 AC Performance

In this section, the cell Read access time and Write time (Time-to-Write) are assessed by 3D TCAD mixed-mode transient simulations. A capacitive load is added onto each bit-line to account for the capacitance of wires and connected devices. The bit-line wire length and capacitance for various cells are calculated from the heights of cell layouts described in Section 4.2. Capacitance from the drain side of connected devices is simulated from AC TCAD simulation. As shown in Fig 4.4, the drain side capacitance (~5e-18F) can be negligible to bit-line wire loading (~e-14F).

4.3.1 Read/Write cell performance

Fig. 4.5(a) shows the definition of "cell" Read access time, which is measured as the time required for developing 50 mV bit-line differential voltage after the word-line turns on. The "cell" Read access time strongly depends on the Read current through the access and pull-down transistors. In Fig. 4.5(b), we compare "cell" Read access time of various FinFET SRAM cells for operating voltages (V_{CS}) ranging from 0.40V down to 0.20V. For IG_ST1, IG_ST2 and IG_ST3 cells, the reduced strength of access transistor (with only one-gate on during Read) benefits the RSNM, but severely degrades the cell Read access time as compared with 6T cell in tied-gate configuration (93X slower). However, with the scaling of V_{CS} to 0.2V, the difference decreases to 20X. This is because the current driving capability of the access transistor depends exponentially on the gate voltage (V_{CS}) in sub-threshold region and the effect of device sizing (device width of single-gate mode versus tied-gate mode) becomes less significant at lower voltage. Notice that sub-threshold SRAMs typically aim for applications such as implantable devices, medical instruments, and wireless sensor networks with operating frequency ranging from several hundred Hz to several

hundred KHz, and power dissipation from μW to tens of μWs. Thus, the Read access times for the proposed cells appear adequate for the intended application.

For Write operation, the "cell" Write time is defined as the time it takes for the voltages of two cell storage nodes to cross over after the word-line turns on (Fig. 4.6(a)). Fig. 4.6(b) compares the Write time of different cells operating at various V_{CS}. As can be seen, the Write time of these cells are comparable due to the similar configuration of access and pull-up transistors during Write. The Write times of cell ST1 and ST2 are slightly larger than other cells at V_{CS}=0.2V due to their increased node capacitances. Also notice that compared with cell Read access time, the cell Write time is significantly shorter.

4.3.2 Read Access Time with Worst-Case Bit-Line Leakage Current

In this section, the impact of bit-line leakage, due to the Standby leakage currents from un-selected cells on the selected bit-line pair, on "cell" Read access time is investigated. Fig. 4.7(a) illustrates the worst-case data pattern for bit-line leakage. All un-selected cells have the same data which is opposite to the selected cell. The solid arrow line symbolizes the Read current in the selected cell, while the dashed arrow lines represent the leakage currents from the unselected cells which rival the Read current. The leakage currents would charge up the low-going bit-line while discharge the bit-line which is supposed to be held at "High". Thus, the bit-line differential voltage is reduced, resulting in degradation of sensing margin and speed. Fig. 4.7(b) shows the dependence of "cell" Read access time on the number of cells per bit-line.

Due to the better gate control and lower leakage current of FinFET devices (compared with bulk devices, which is shown in Fig.4.8), increasing the number of cells per bit-line from 32 to 256 degrades the cell Read access time by about 5-6X. Thus, the proposed cells can support adequate number of cells per bit-line to meet the density requirement with adequate performance (several hundred Hz to several hundred KHz) for the intended applications.

4.3.3 Temperature Dependence on Read Access Time with Worst-Case Bit-Line Leakage Current

It is important to point out that the temperature significantly affects transistor leakage current (two orders difference from 27℃ to 125℃), as shown in Fig. 4.9. Fig. 4.10 shows the Read access time of 512 cells per bit-line for the worst-case bit-line data pattern versus temperature. It can be seen that except for IG_ST1 cell at 125℃, other cells can successfully perform Read operation across the temperature range. The failure of IG_ST1 cell is mainly due to its slower sense signal development (longer Read access time), rendering it more susceptible to bit-line leakage. The failure case of IG_ST1 is shown in Fig. 4.11.

4.4 Summary

Based on 32nm layout design rule, we have estimated area of various cells from popular "thin cell" layout style. Our proposed cells can save 30% - 39% area compared with ST1 and ST2 cells. In our transient simulations, due to the reduced

strength of access transistor (only one gate is opened in Read mode), Read time is severely degraded compared with other cells at V_{CS}=0.4V. However, our cells still adequate for sub-threshold SRAM applications, the frequency is from several hundred Hz to several hundred KHz. Write time of various cells are comparable because of the same configuration of access and pull-up transistors.

Despite of "cell" Read time, we evaluated the Read access time with worst-case bit-line leakage current. As can be seen, increasing the number of cells per bit-line from 32 to 256 only degrades the cell Read access time by about 5-6X. Thus, our cells can meet the density requirement with adequate performance. Temperature affects on device leakage has also been considered to the Read access time with worst-case bit-line leakage current. Most of temperature range can be tolerated except for IG_ST1 cell at 125℃.
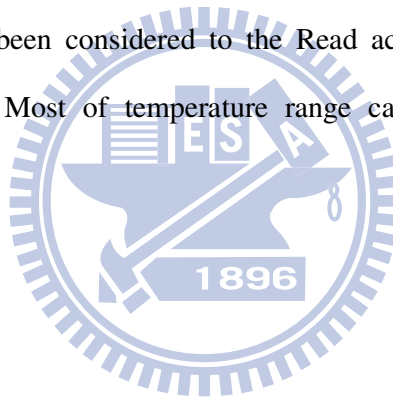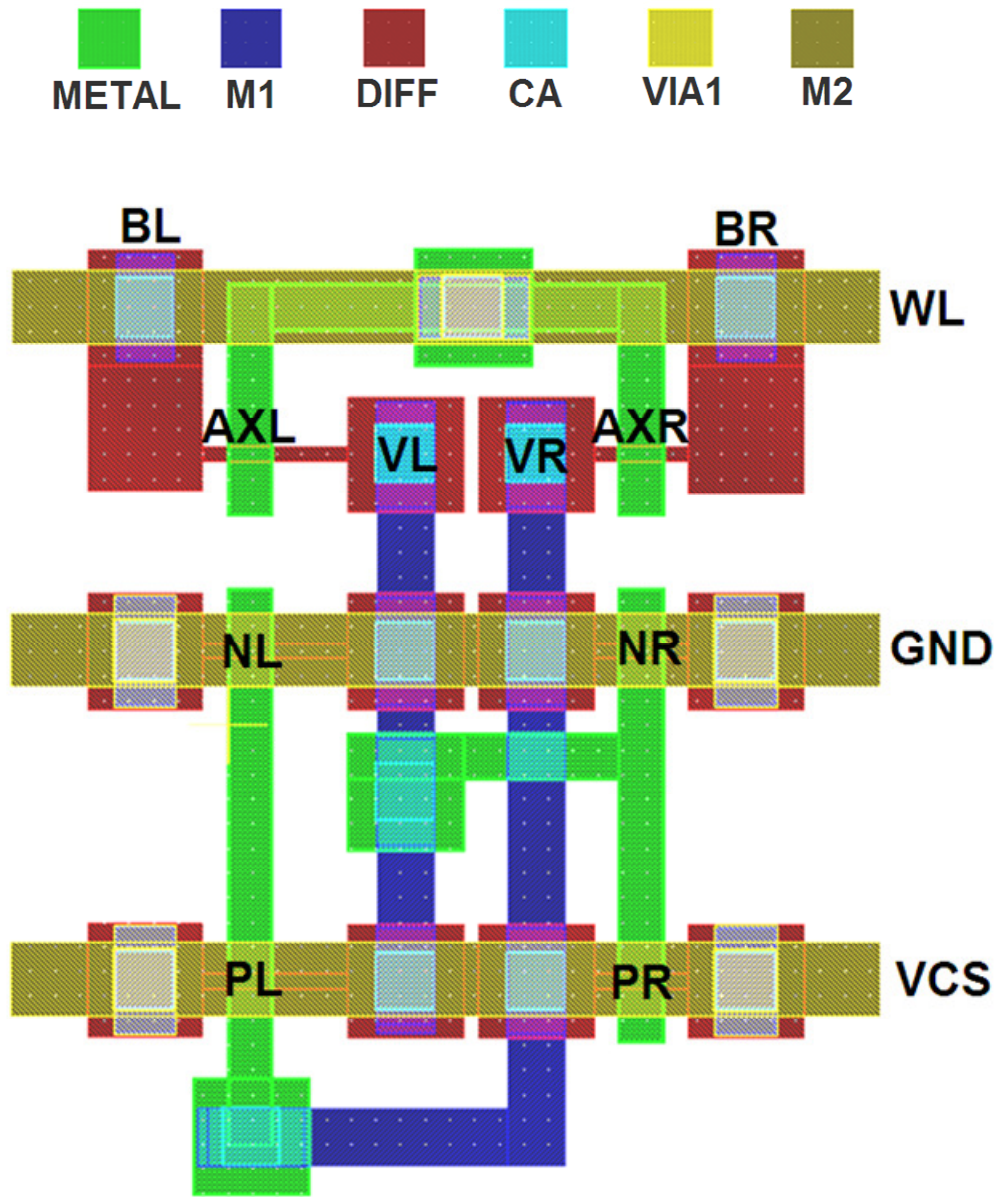
Fig. 4.1. "Conventional cell" layout of 6T cell.

METAL M1 DIFF CA VIA1 M2

4.5y=450nm (6T)

6y+2z=760nm(ST1)

6y+2z=760nm(ST2)
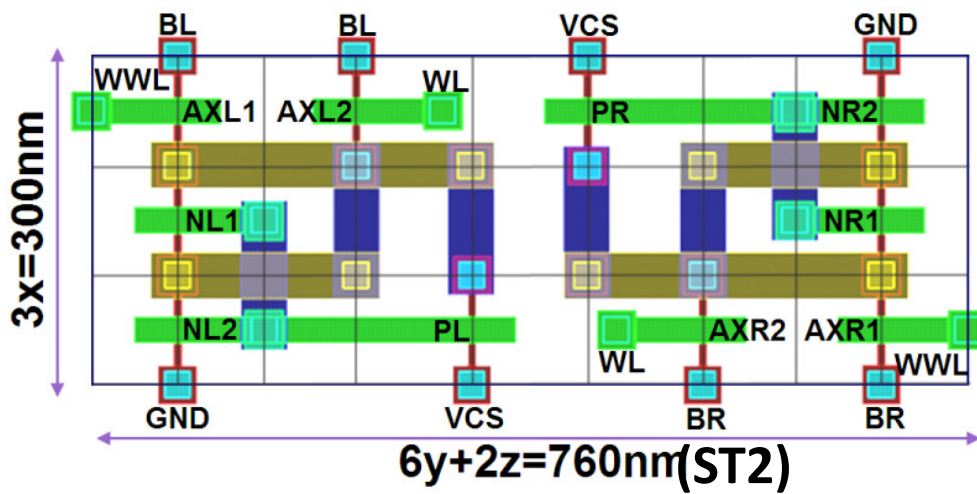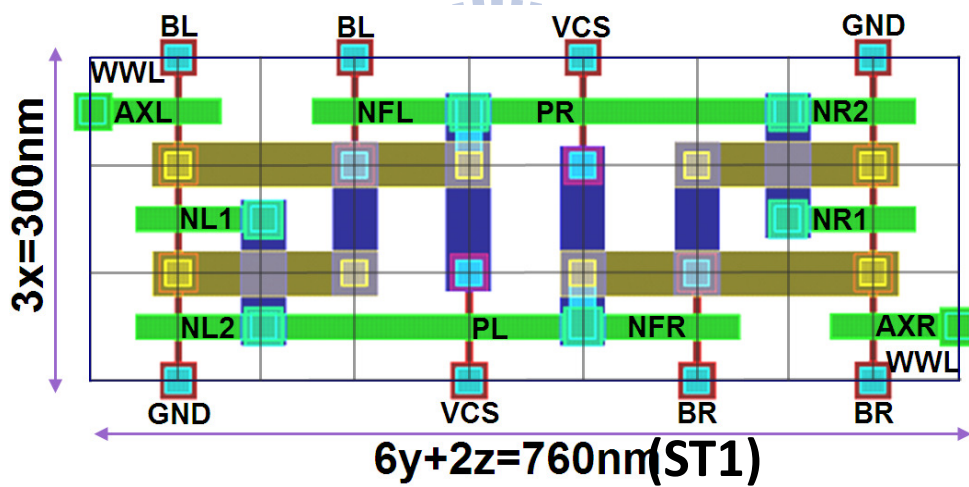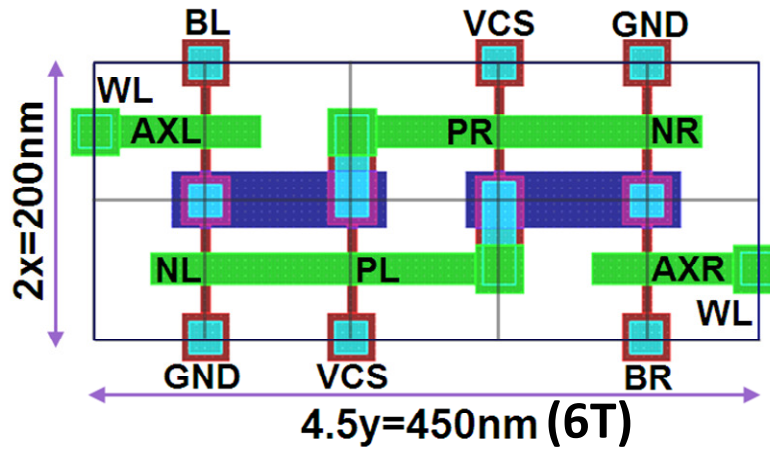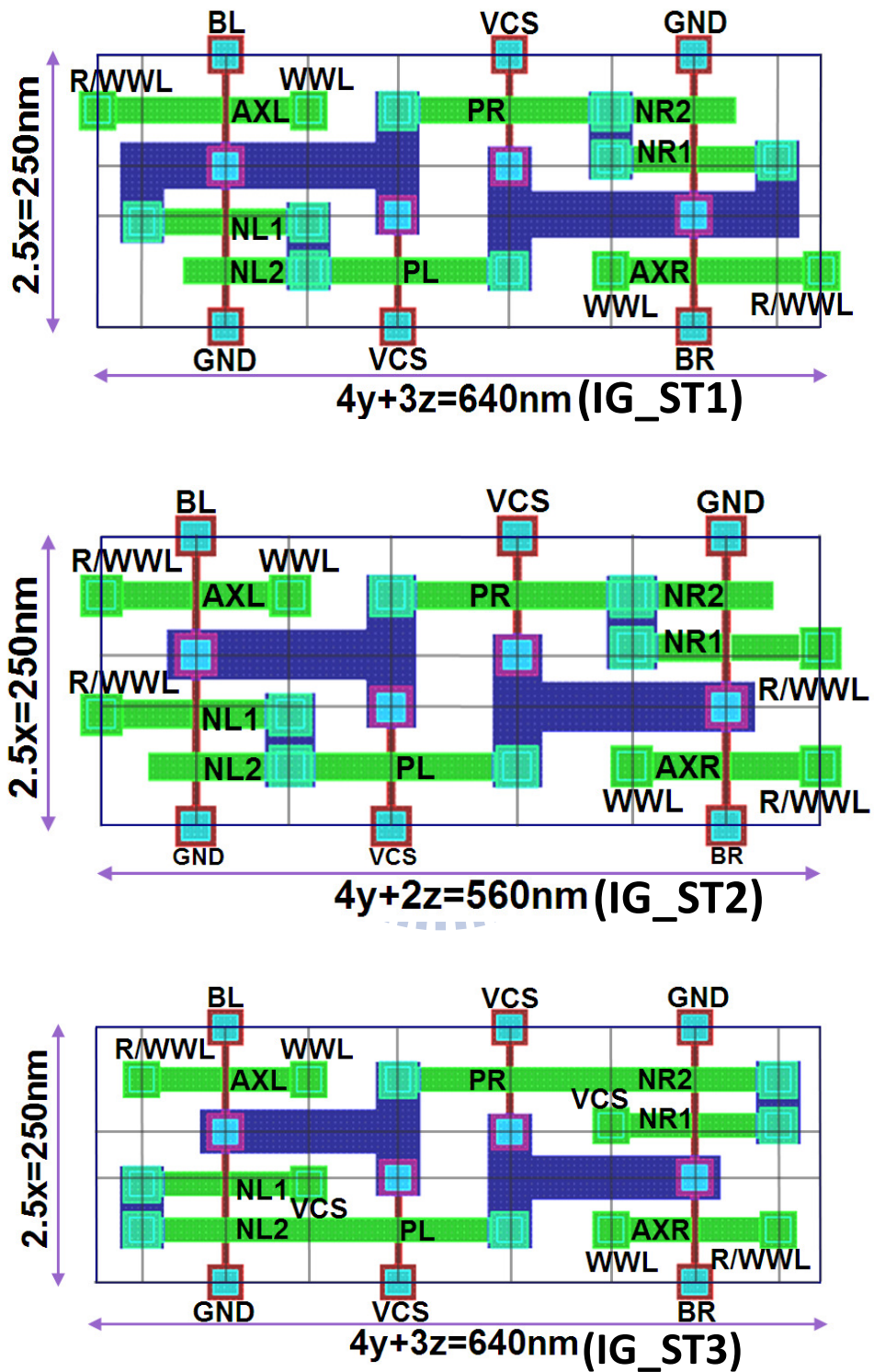
Fig. 4.2. Various FinFET cell layouts.

Table 4.1. Layout design rules.

L_{eff}=25nm node	scale
x=contacted gate pitch	100nm
y=fin pitch	100nm
z=contact to contact pitch	80nm
M1 pitch	80nm
M2 pitch	80nm
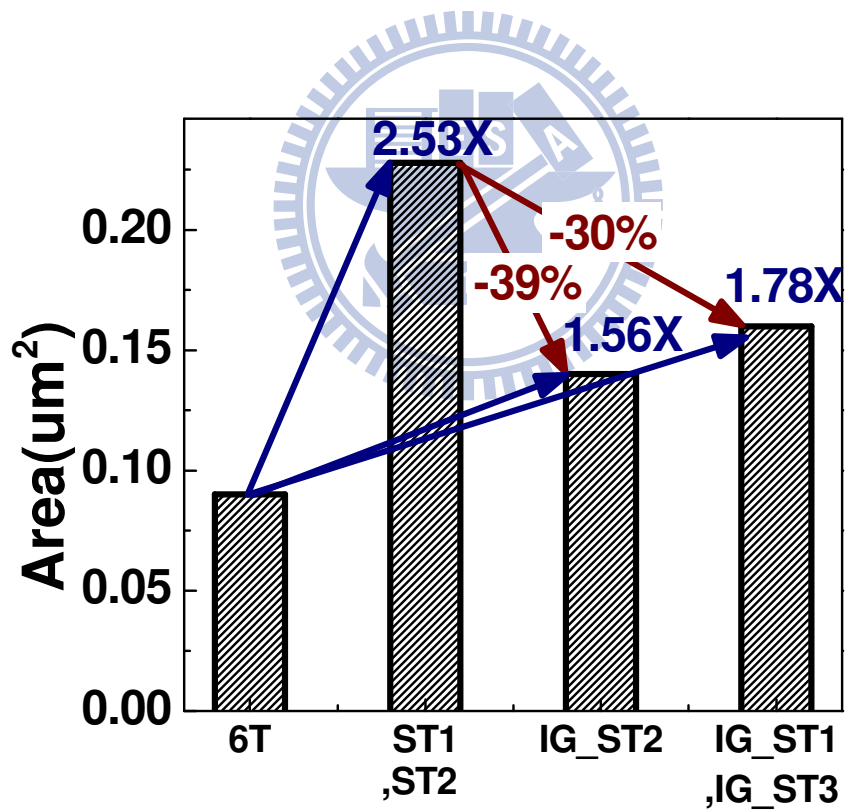
Fig. 4.3. Comparison of cell areas of various FinFET cells.
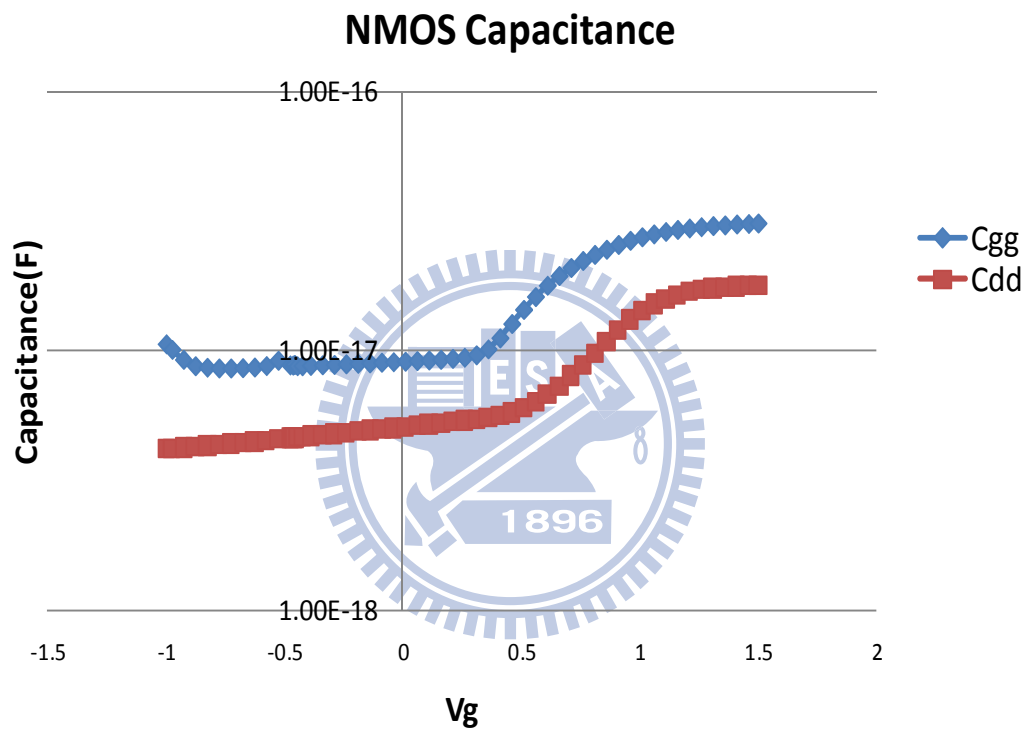
Fig. 4.4. Drain side and gate capacitance versus gate voltage (V_g).
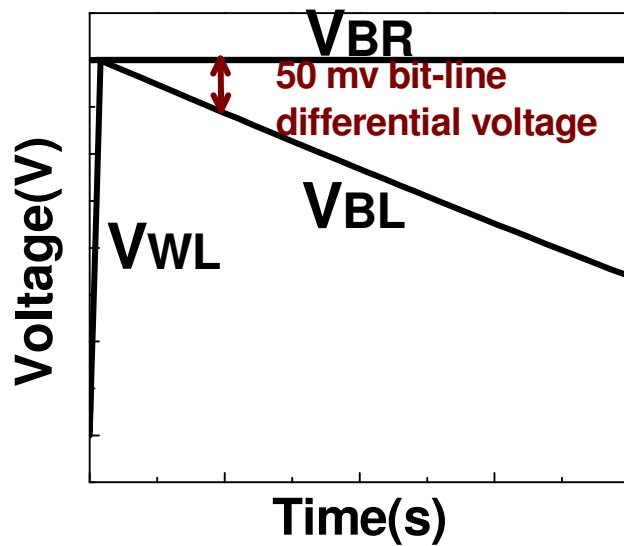
(a)
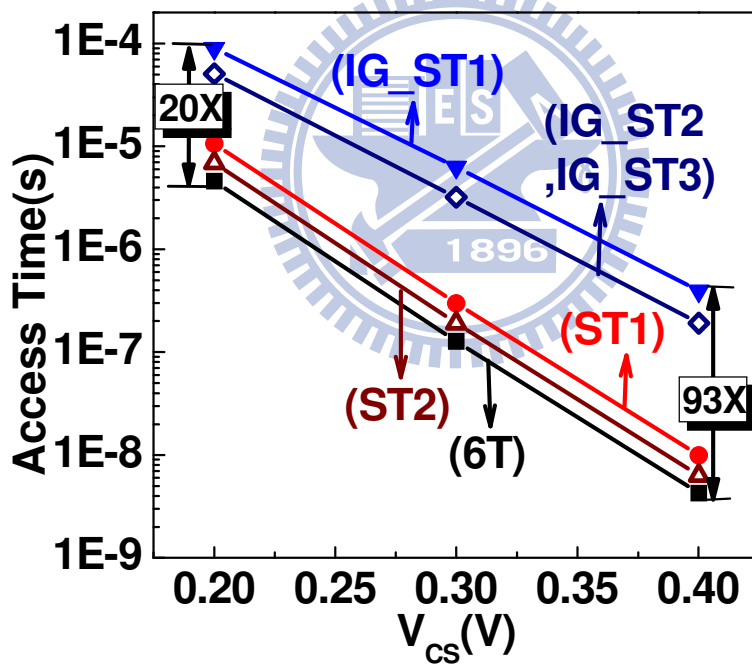
(b)

Fig. 4.5. (a) The definition of "cell" Read access time, and (b) comparison of "cell" Read access time for different FinFET cells operating at various V_{CS}.

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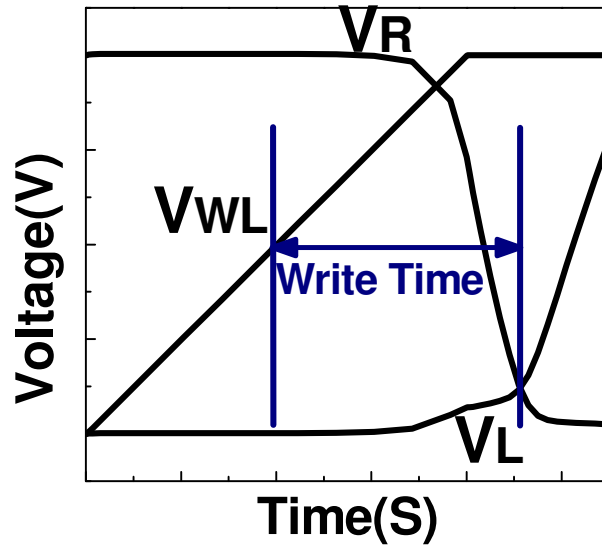
(a)
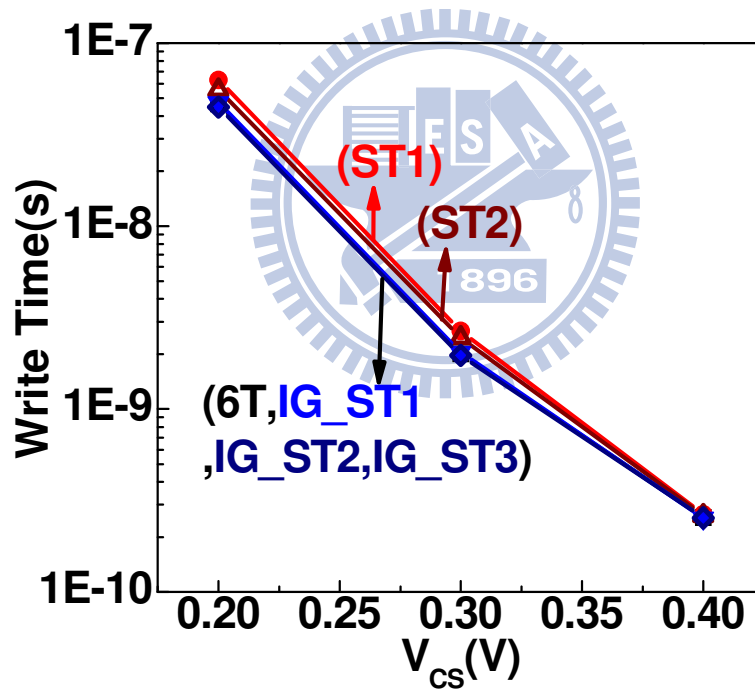
(b)

Fig. 4.6. (a) The definition of "cell" Write time (Time-to-Write), and (b) comparison of "cell" Write time of different FinFET cells operating at various V_{CS}.
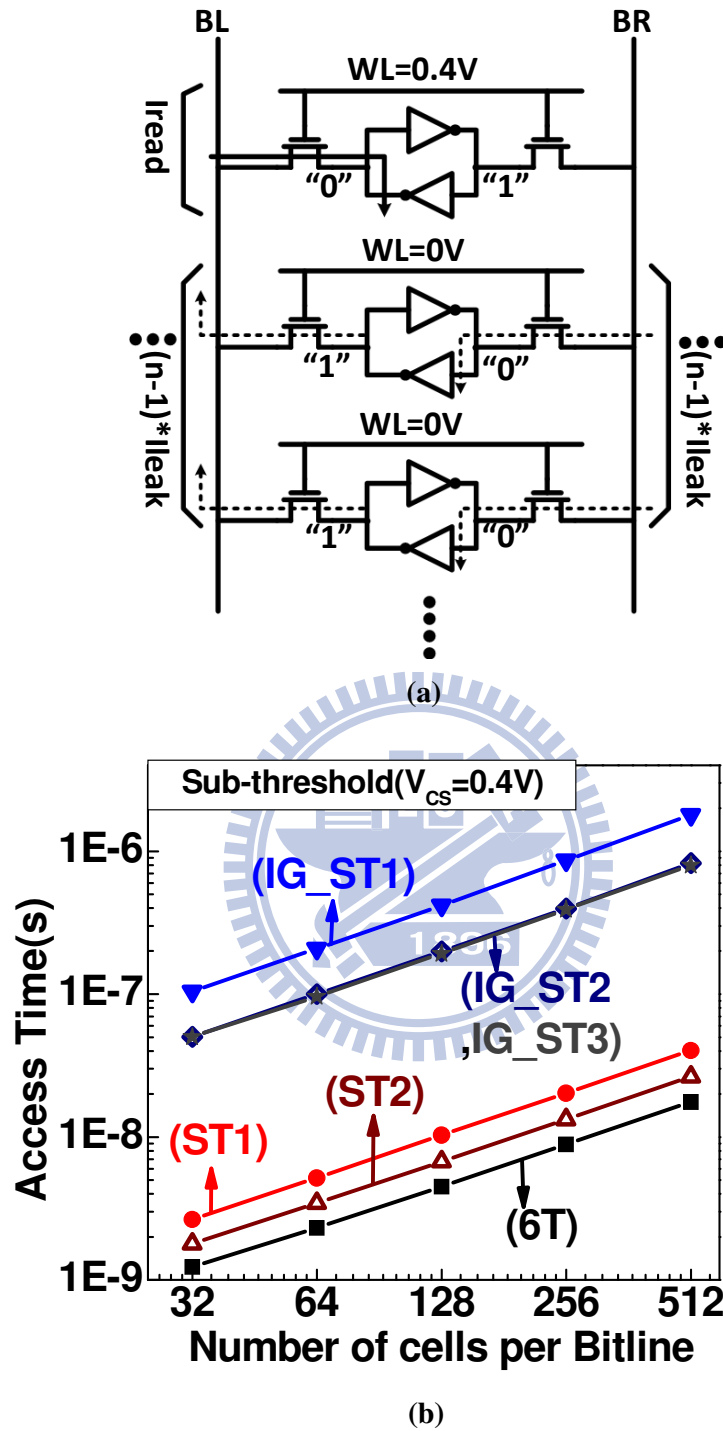
Fig. 4.7. (a) Schematics showing the worst-case bit-line data pattern for leakage current affecting Read operation, (b) Read access time considering worst-case bit-line leakage current versus number of cells per bit-line.
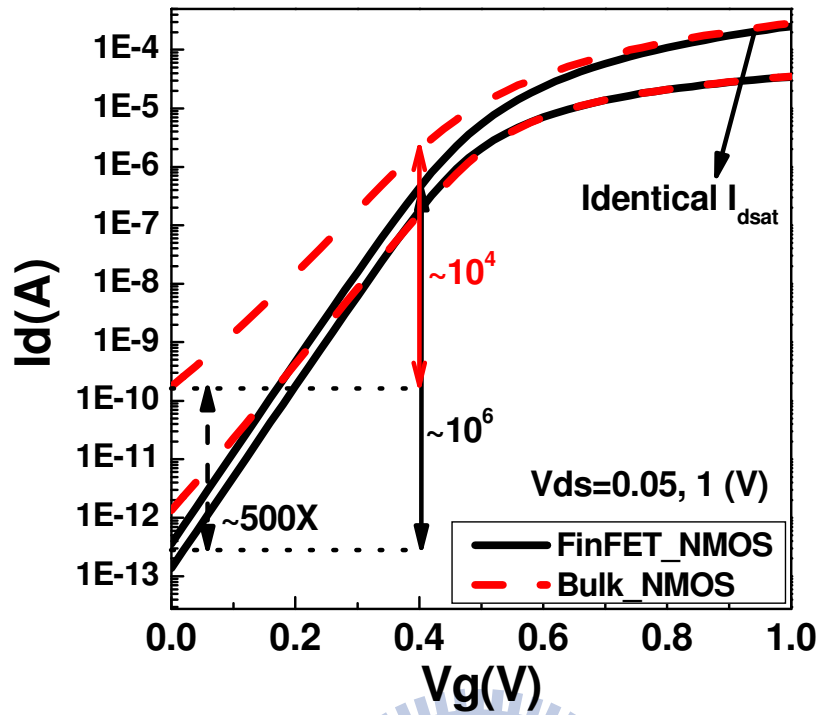
Fig. 4.8. Comparison of I_d-V_g curves for 25nm bulk and FinFET devices.
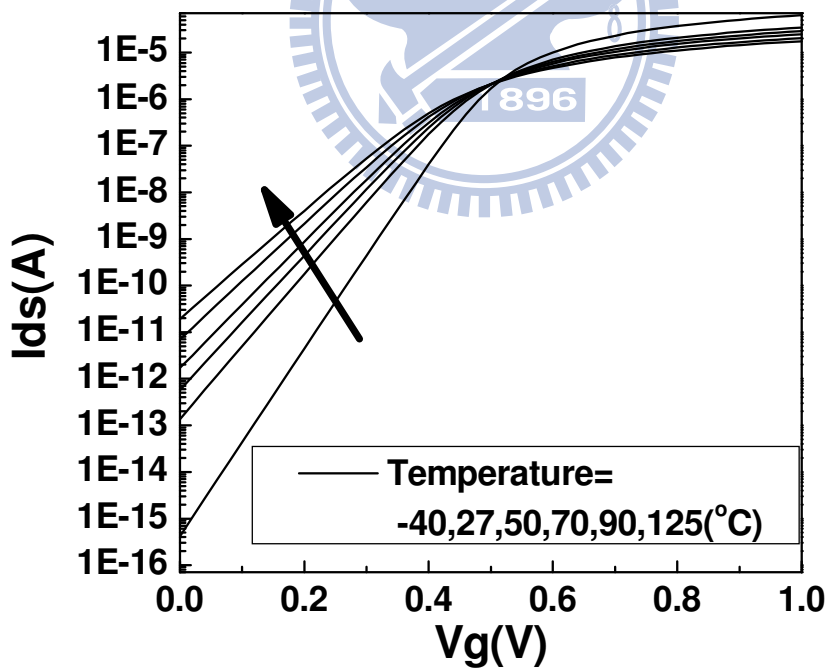
Fig. 4.9. Standby leakage current increases with risen temperature.

(a)
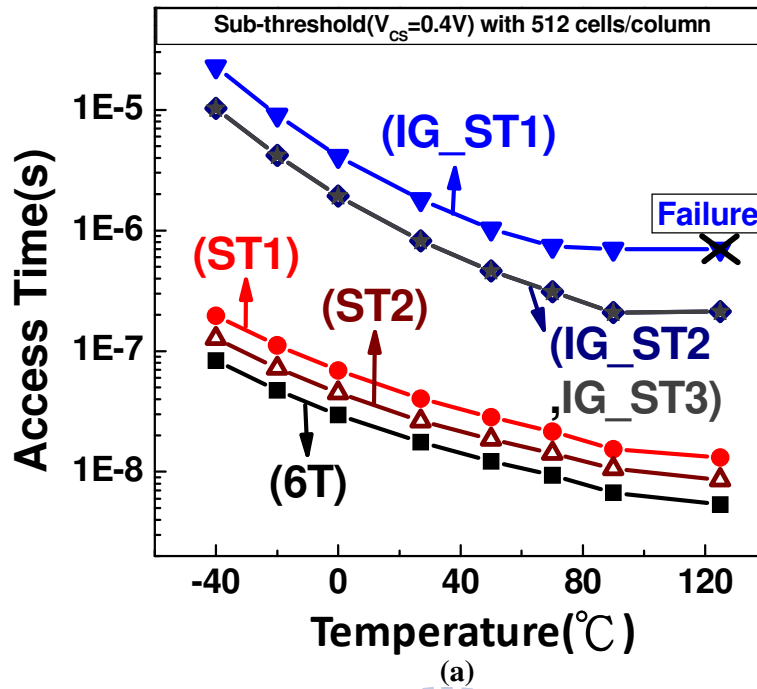
Fig. 4.10. Read access time of 512 cells per bit-line (worst-case bit-line data pattern) versus temperature.

(b)
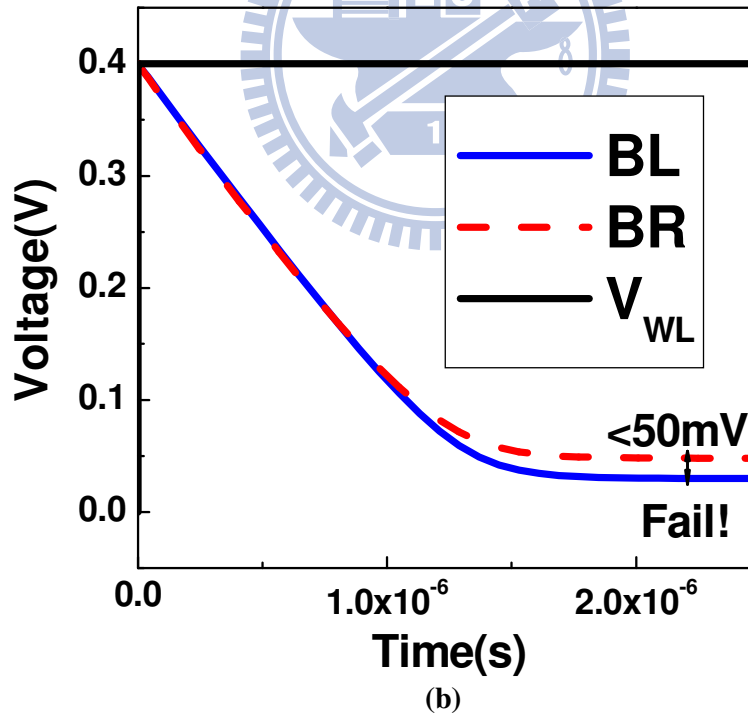
Fig. 4.11. Simulated waveform for Read failure operation at 125℃ with 512 cells per bit-line of IG_ST1 cell.

Chapter 5

Analysis of Process/Random Variation for FinFET Sub-threshold SRAM Cells

5.1 Introduction

In the recent years, MOSFETs have kept scaling to decananometer region (between 10nm and 100nm). 32nm technology node with 2nd generation high-k metal gate planar MOSFETs have been in mass production in 2010 [30]. However Short-channel effects (SCE) are still the main deviation in bulk device. In order to improve SCE, increase channel doping and enhance gate control ability are two conventional solutions. The other solution is using multi-gate devices, such as FinFET [31]. FinFET has inherent advantage of better channel control ability. Due to its better gate control characteristic, FinFET device doesn't need high channel doping to solve SCE. Except for SCE and process variations, there are some local random fluctuations, such as Random Dopant Fluctuations (RDF), Line Edge Roughness (LER) and Work Function Variability (WFV). RDF is random small dopant numbers which randomly locate in channel region. It will lead to significant variations on threshold voltage and drive current. However, the channel concentration is a significant factor on RDF [32]. As previously mentioned that FinFET has undoped channel is less suffered by RDF [8]. Therefore, in the following sections, we will not focus on the effect of RDF on FinFET SRAM stability.

In the recent years, to enhance gate control ability, metal has become the feasible

material due to incompatibility of polysilicon with high-k materials. Since (1) metals have different grain size and (2) metals have work function dependency on orientation, WFV would be a series concern in the threshold voltage variability (TVV) [33]. There were some experimental data to verify how TVV was impacted by WFV, and in order to model this phenomenon, a few models have been proposed for SRAM variability analysis [34, 35]. However, WFV effect can be weaken by some special process and choosing appropriate material.

As described in [3, 9], the feedback mechanism also provides built-in process tolerance. This is because the feedback NFET would track the process variation and adjust the feedback for conditioning the intermediate node accordingly. Using ST1 as an example, at Fast-N (FN) corner, the V_T of the feedback NFET (NFL/NFR) would be lower, resulting in higher intermediate node (VNL or VNR) voltage, thus partially compensating for the lower V_T of the cell pull-down NFET transistor stacks. In this Section, we describe results from 3D mixed-mode Monte Carlo simulations considering the impacts of process variations and local random variations on cell stability.

5.2 Analysis of Local Random Variation - Line Edge Roughness (LER)

5.2.1 Introduction

LER is caused by material and tools which is not a critical intrinsic variation

source in the past. This is because critical dimensions of MOSFETs were orders of magnitude larger than the roughness. However as LER becomes close to device critical dimensions, LER does not scale down with aggressive technology process development [36]. In 2006, there is a paper indicate that LER would be a dominant local random variation for beyond 45nm technology node [37]. And more severe for FinFET (compare with bulk device, FinFET has less RDF effect) [38, 39]. It consists of variations from the deviations of gate length (Gate LER) and fin width (Fin LER).

In the following sections, we will briefly introduce the methodology for LER simulation on SRAM stability. Moreover, our simulations including process variation and sensitivity of cell overall stability.

5.2.2 Methodologies
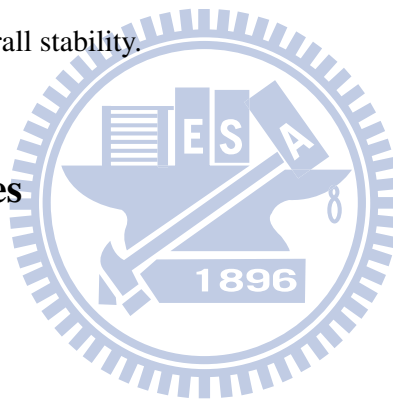
5.2.2.1 Concept

According to real experimental data [40], the line edge roughness pattern can reconstruct by magnitude in frequency domain and random phases. Fig. 5.1 shows the magnitude is just similar to low-pass filter [40]. There are two models, Gaussian and exponential which literature used to use. This is the concept of Fourier synthesis approach [36].

5.2.2.2 Simulation Approach

As previous section mentioned that two popular models for LER magnitude simulation are Gaussian and exponential models. These two models have the same parameters in autocorrelation function as follows:

$$S_G(k) = \sqrt{\pi}\Delta^2\Lambda e^{-(k^2\Lambda^2/4)} \qquad (3.1)$$

$$S_E(k) = \frac{2\Delta^2\Lambda}{1+k^2\Lambda^2} \qquad (3.2)$$

The same parameters are the rms amplitude Δ and correlation length Λ. Δ represents the roughness amplitude, and Λ is a fitting parameter for a particular type of LER. The parameter k = i(2π/N dx) which is the index of discrete sampling points, where dx is the discrete spacing of sampling points.

Fig 5.2 shows the FinFET device design flow of LER in TCAD simulation. First, choose appropriate rms amplitude Δ and correlation length Λ, and combined with randomly selected phases. Then take inverse Fourier transform to rebuild 1D rough line. As we know, FinFET device has both gate length and fin width dimension of LER sources. Thus, 1D rough line is extended to 3D Fin LER and Gate LER devices. Assume that Fin LER and Gate LER are two irrelevant deviations and thus $\sigma^2_{Total\_LER} = \sigma^2_{Fin\_LER} + \sigma^2_{Gate\_LER}$ [38].

To determine the model parameters, we can choose an appropriate rms amplitude Δ from ITRS roadmap and advanced lithography processes from various labs. Due to less experimental data, correlation length Λ is less known. P. Oldiges et al. [41]

reported that the measurement data indicate that correlation length Λ varied between 10nm and 50 nm. A. Asenov *et al*. [36] reported that the SEM micrographs indicate that values of correlation length Λ in the range of 20-30nm. For the typical values of Δ and Λ, Fig. 5.3 shows the detected power spectrum compared with Gaussian and exponential models [36]. Due to lack of high frequency components in Gaussian model, curve with Gaussian autocorrelation is smoother than exponential model. Although two models both can fit the captured autocorrelation date well [42], our next TCAD 3D mixed-mode simulations will base on using Gaussian autocorrelation function.

In summary, we pick fair values of Δ and Λ (Δ=1.5nm Λ=20nm), and by using Gaussian autocorrelation function for the following TCAD 3D mixed-mode simulations. As we know, Monde Carlo simulation is very time-consuming, so how to select appropriate sample number to capture the statistical characteristic of device fluctuation is very important. In [8, 39], authors claimed 100 samples were enough to achieve a clear trend. In this work, we take 100 samples for next SRAM level simulations.

5.2.2.3 Results and Discussions

Fig. 5.4 and Fig. 5.5 illustrate the butterfly curves (at V_{CS} = 0.4V) induced by Gate LER and Fin LER of difference cells. 3D TCAD mixed-mode Monte Carlo simulations with 100 samples for each case are analyzed. Fig. 5.6 compares the probability distribution of the RSNM (at V_{CS} = 0.4V) of difference cell structures induced by Gate LER (Fig. 5.6(a)) and Fin LER (Fig. 5.6(b)), respectively. As can be

seen, Fin LER represents the dominating source of RSNM variation. For Gate LER, the μ/σ ratios of all Schmitt Trigger based cells are well over 30. For Fin LER, the μ/σ ratio can be seen to be much smaller than that for Gate LER. Notice that a μ/σ ratio of at least around 5-6 is desirable. We can see that except for IG_ST1 cell (μ/σ ratio = 5.45), other Schmitt Trigger based cells can provide significantly better margin than that of 6T (μ/σ ratio = 5.83). This is because IG_ST1 cell operating in independent-gate mode has worse electrostatic integrity than the tied-gate mode [43], and its nominal RSNM improvement (over 6T cell) is less significant than IG_ST2 and IG_ST3 cells due to its softer (less steep) switching characteristics as discussed in Section 2. Fig. 5.7 shows the I_d-V_g dispersion curves considering Fin LER from 3D TCAD Monte Carlo simulations with 150 samples. It clearly shows that independent-gate mode has larger σVth than tied-gate mode. The results are consistent with the difference of σRSNM of various cells.

5.3 Process Variation Combined with LER

In order to evaluate the robustness of these FinFET SRAM cells under process variations, different process corners are defined in Fig. 5.8(a). In this work, ±20% device parameter deviations are assumed and two most critical device parameters (L_{eff} and $W_{fin}(T_{si,})$) are used to characterize fast and slow devices. Three corners (TT, FNSP and FPSN) combined with local random Fin LER are considered in these cells and compared in Fig. 5.8(b). It can be seen that FNSP corner exhibits relatively smaller μ/σ ratio than other corners, and most cells fail to satisfy the requirement of μ/σ > 6 at this corner. Notice that IG_ST2 and IG_ST3 can still provide sufficient margin (μ/σ ratio = 7) and show the best robustness for RSNM under the combined influence of

process variations and local random variations.

5.4 Analysis of Local Random Variation – Work Function Variability (WFV)

5.4.1 Introduction

Fig. 5.9(a) shows how the metal gate impact the work function, (1) various-sized grains to amorphous, and (2) work function dependency on surface orientation [33]. According to experimental data, there are two guidelines for optimize WFV, (1) reduce the grain size (preferring amorphous) of the metal gate, (2) use the small dependency of work function on orientation. For an example, Fig. 5.9(b) shows the fcc crystal structure has small orientation dependency than bcc crystal structure [33].

There have been proposed two models to demonstrate this variability. First, H. Dadgour *et al*. [34] indicate that due to the uncertainty of work function in metal gate, the gate work function should be modeled as probabilistic distribution. Because of work function values are calculated as a weighted average of all the existing grains, this method is called averaged work function (AWF). And second, X. Zhang *et al*. [35] claimed that using AWF lacks physical validity and can't accurately perform WFV effect. While AWF only uses a single averaged work function for each device to calculate its V_t variations, which assumes uniform inversion densities along the channel. In [35], due to various work function on grain orientations for each device, the metal gate which is formed by pieces of grain with various work function. This

model incorporates the dependency of the inversion densities on various grain orientations for each device. Thus, a whole transistor should be divided to many small transistors to describe its electrical behavior. Fig. 5.10 shows the concept of how to effectively and physically model the transistor.

5.4.2 Methodologies

5.4.2.1 Concept

During the process, due to grain orientation difference, we can't accurately control the direction of grain orientation. Thus, the gate work function should be modeled by probabilistic distribution rather than a fixed number. According to this concept, work function can be calculated as a weighted average of the work function in the entire gate area [34].

5.4.2.2 Simulation Approach

In this work, we adapted weighted averaged work function (AWF) method to analysis of various SRAM cells reliability under WFV. In our case, for our nominal work function value (NMOS:4.60eV, PMOS:4.68eV), we choose TiN for our metal gate material. Physical property of TiN is shown in Table 5.1.

There are several parameters need to be determined in this model. The symbols

$\varphi_1, \varphi_2, \ldots \varphi_n$ and $P_1, P_2, \ldots P_n$ represent work function values of different grain orientations and their corresponding probabilities. The grain size (G) of each type of gate materials are different, in our case, the average grain size of TiN is 4.3nm from TEM experimental data [33]. The number of grains (N) can be calculated as $(L_{eff}/G)*(H_{fin}/G)*2$. Assuming $X_1, X_2, \ldots X_n$ to be random variables which is the number of grains with corresponding work function values of $\varphi_1, \varphi_2, \ldots \varphi_n$ respectively. (φ_M) as a weighted average of work function which is probability distribution in gate area. Thus, the formula of φ_M is $\phi_M = \left(\dfrac{X_1}{N}\right)\phi_1 + \left(\dfrac{X_2}{N}\right)\phi_2 + \ldots + \left(\dfrac{X_n}{N}\right)\phi_n$ (1). Our goal is to obtain its mean and standard deviation for the random variable φ_m.

In our special case for TiN with only two grain orientations, the probability density function can be calculated by "binomial distribution". $f_{x1}(k) = \begin{pmatrix} N \\ k \end{pmatrix} P_1^k (1-P_1)^{N-k}$ where $\begin{pmatrix} N \\ k \end{pmatrix} = \dfrac{N!}{k!(N-k)!}$. Equation (1) can rewrite as $\phi_M = \left(\dfrac{X_1}{N}\right)\phi_1 + \left(\dfrac{X_2}{N}\right)\phi_2$.

5.4.2.3 Results and Discussions

Fig. 5.11 shows standard deviation of WFV has dramatic variation below 20 grain numbers, and gradually saturate above 20 grain numbers. It represents that grains numbers (N) (grain size (G)) will be a critical parameter in this model. Due to device geometry (H_{fin}=20nm L_{eff}=25nm) and grain size of gate material (TiN=4.3nm), our number of grains (G) is 54, and standard deviation is 12.9 mV.

Fig. 5.12 illustrates the butterfly curves (at V_{CS} = 0.4V) induced by WFV of difference cells. 3D TCAD mixed-mode Monte Carlo simulations with 100 samples

for each case are analyzed. Fig. 5.13 compares the probability distribution of the RSNM (at $V_{CS} = 0.4$V) of difference cell structures induced by WFV. As can be seen, at the extent of impact of WFV to RSNM is between Gate LER and Fin LER. All of the Schmitt Trigger based cells can provide significantly better margin than 6T, and IG_ST2 and IG_ST3 are the most promising cells under WFV (μ/σ ratio=20).

5.5 Sensitivity of Cell Stability

In addition to RSNM variations described above, the sensitivity of cell stability (ΔSNM) to device parameters are also assessed. ΔSNM is calculated from the SNM difference by taking $\pm 20\%$ device parameter deviations, including L_{eff}, $W_{fin}(T_{si},)$, EOT, and H_{fin} , i.e. ΔSNM = |SNM(P+20%)-SNM(P-20%)|. The % change in SNM is defined as ΔSNM / SMM$_{nominal}$. Table 5.1 shows various device parameter deviations (L_{eff}, $W_{fin}(T_{si},)$, EOT, and H_{fin}), calculated respectively during Read, Write, and Hold operations. It can be seen that L_{eff} and $W_{fin}(T_{si},)$ are the main deviation sources. Fig. 5.9 compares the % change in SNM of various cells during Read, Write, and Hold operations. The results are consistent with previous analyses/observations. In Fig. 5.9(a), IG_ST2 and IG_ST3 cells can be seen to exhibit least sensitivity (smallest % change in RSNM) to device parameter variations. In Fig. 5.9(b), Schmitt Trigger based cells show slightly better (lower) WSNM sensitivity. In Fig. 5.9(c), IG_ST2 shows the worst % change in HSNM since there is no feedback mechanism during Hold operation. Among our proposed cells, IG_ST3 cell, with the strongest feedback mechanism, demonstrates better HSNM than that in IG_ST1 and IG_ST2 cells.

5.6 Summary

In this Chapter, we introduce the design flow to construct LER device. This approach is deeply related to two parameters, rms amplitude Δ and correlation length Λ. Thus, we reference the relevant literatures to make sure our simulation will be right with appropriate parameters.

In TCAD 3D mixed-mode simulations, we can consider Read stability with Gate LER and Fin LER respectively. In the results, (1) Fin LER represents the dominating source of RSNM variation, and (2) μ/σ ratio of various cells can be more than 5. In order to know which cell is more robust, different process corners combined with Fin LER have been investigated. In the worst corner (FNSP), only IG_ST2 and IG_ST3 cells can exceed μ/σ ratio over 6.

Besides LER, we introduce another local random variation - WFV. We adapted AWF method to simulate WFV. The extent of impact of WFV to RSNM is between Gate LER and Fin LER. All of the Schmitt Trigger cells have better margin than 6T cell, especially IG_ST2 and IG_ST3 cells which have the highest μ/σ ratio of various cells.

In addition to evaluate overall stability, which are including Write and Hold. The result shows Schmitt Trigger based cells have better immunity to process sensitivity.
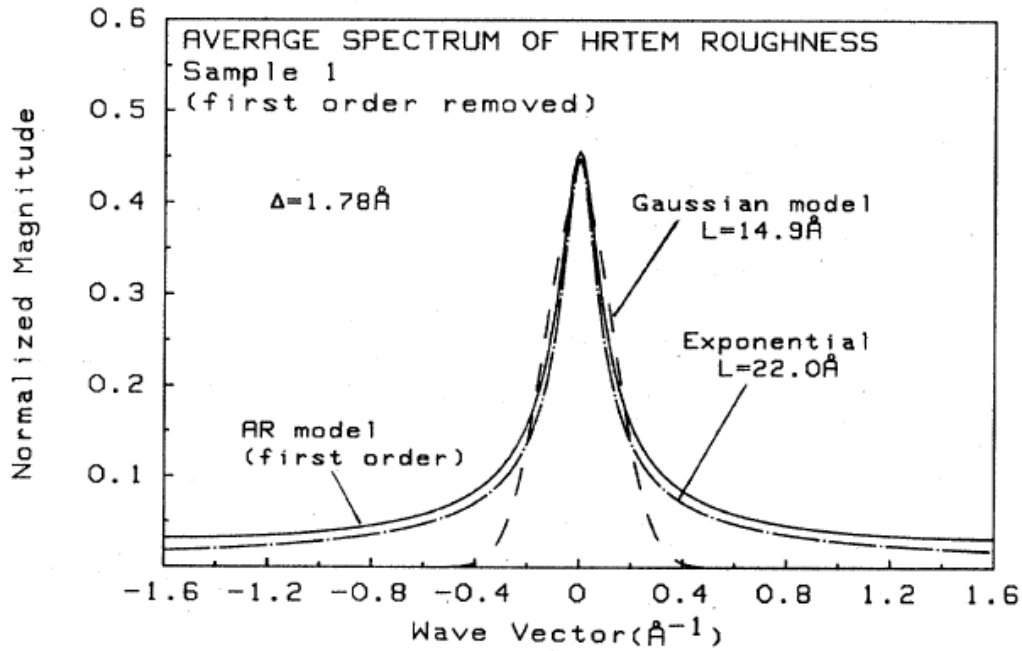
Fig. 5.1. Frequency spectrum which is similar to low pass filter [40].

Magnitude:
$$S_G(k) = \sqrt{\pi}\Delta^2 \Lambda e^{-(k^2\Lambda^2/4)}$$
$$S_E(k) = \frac{2\Delta^2 \Lambda}{1+k^2\Lambda^2}$$

Phase : Random selected phases between 0~2π

Take inverse Fourier transform

1D rough line:

Extend to 3D FinFET devices

Fin LER:
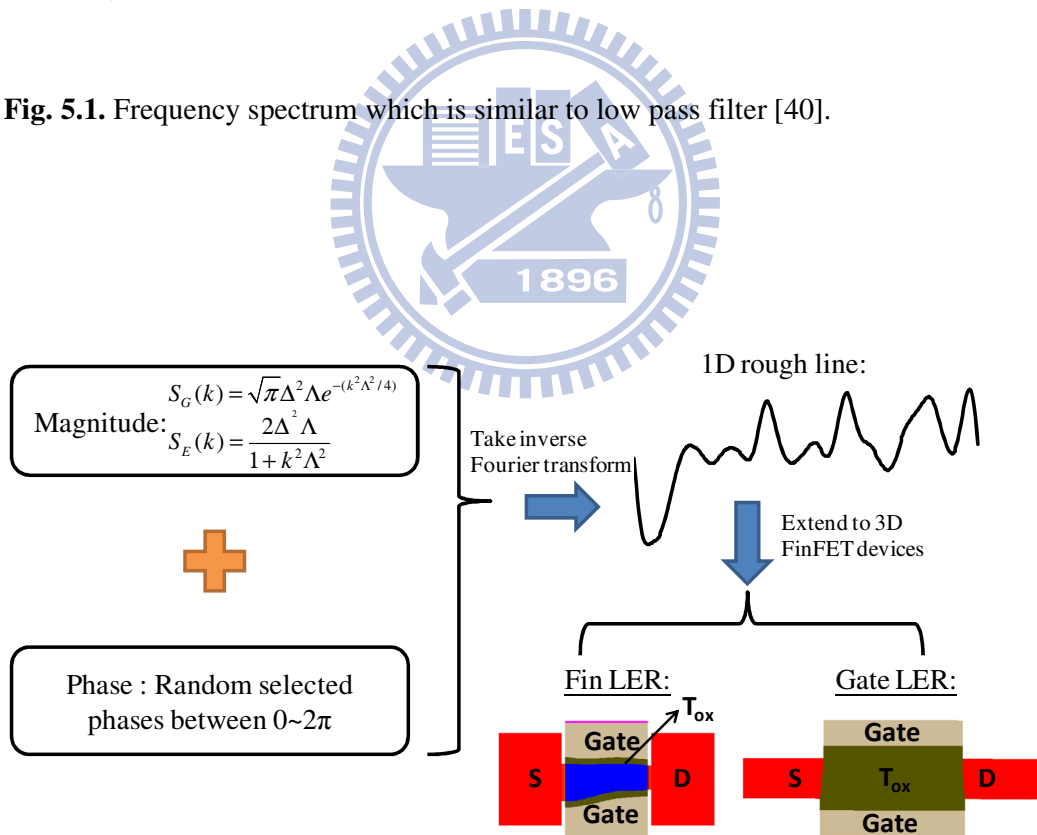
Gate LER:

Fig. 5.2. Design flow to set up FinFET Fin- and Gate- LER devices.
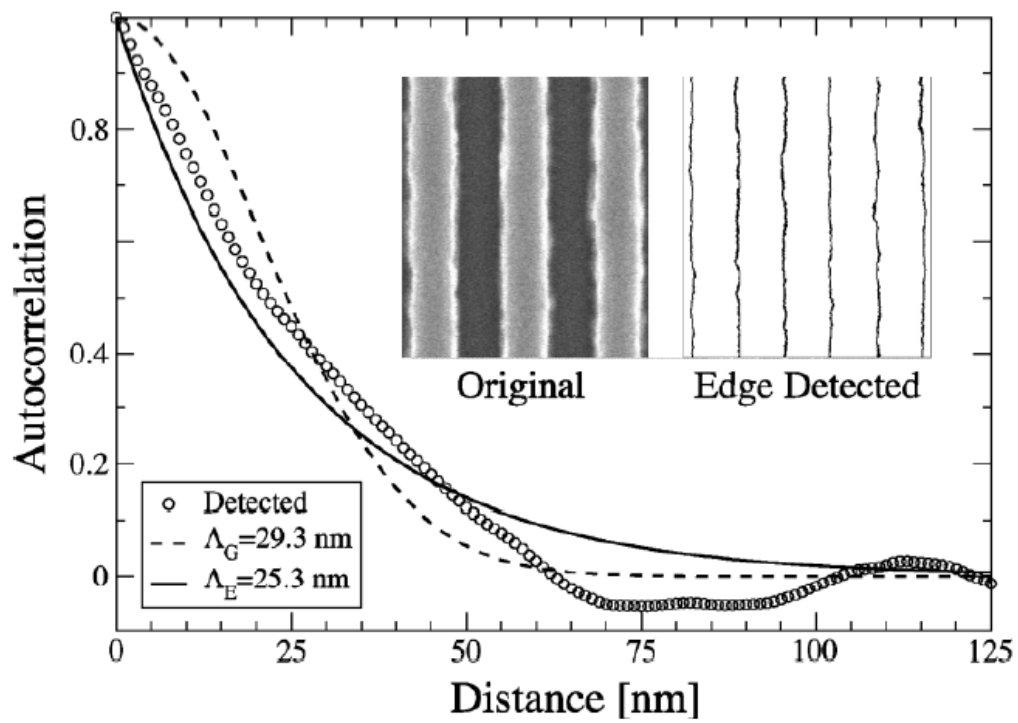
Fig. 5.3. Detected line edge roughness compared with Gaussian and exponential models [36].

Fig. 5.4. Voltage transfer characteristics of various cells considering Gate LER from 3D mixed-mode Monte Carlo simulations.

Fig. 5.5. Voltage transfer characteristics of various cells considering Fin LER from 3D mixed-mode Monte Carlo simulations.

	6T	ST1	ST2	IG_ST1	IG_ST2 IG_ST3
μ (mV)	73.4	99.76	107.34	101.36	136.77
σ (mV)	2.79	2.97	2.34	2.86	2.6
μ/σ	26	34	46	35	53

	6T	ST1	ST2	IG_ST1	IG_ST2 IG_ST3
μ (mV)	65.29	94.34	99.94	89	127.51
σ (mV)	11.2	10.94	9.04	16.34	13.39
μ/σ	5.83	8.62	11.06	5.45	9.52

Fig. 5.6. Probability distribution of RSNM (at V_{CS} = 0.4V) considering (a) Gate LER, and (b) Fin LER for different SRAM cell structures from 3D mixed-mode Monte Carlo simulations.
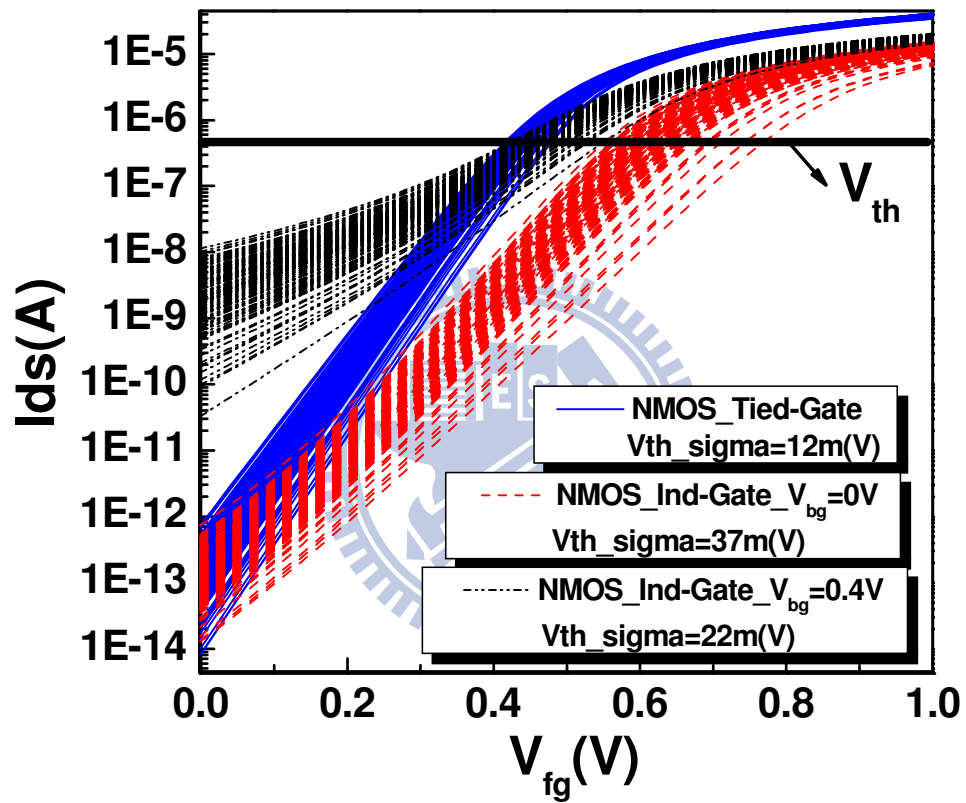
Fig. 5.7. *I$_d$-V$_g$* curves of independent-gate and tied-gate mode considering Fin LER from 3D Monte Carlo simulations (150 samples).
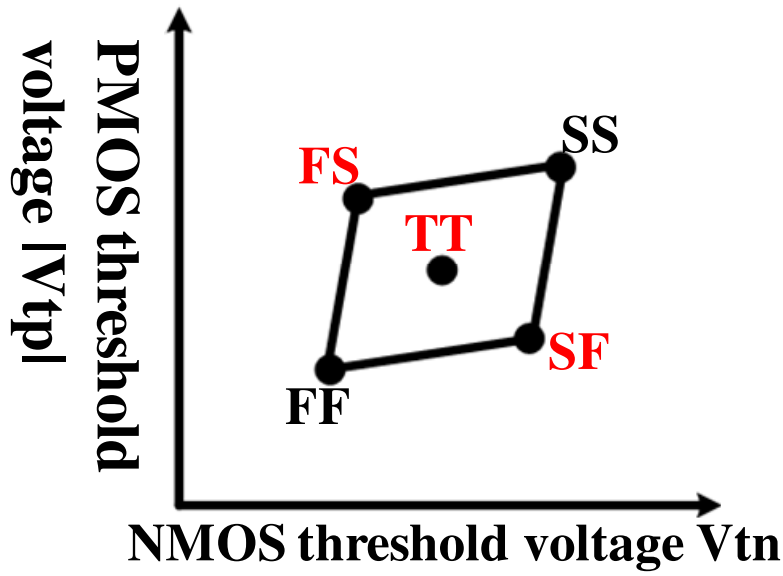
(a)
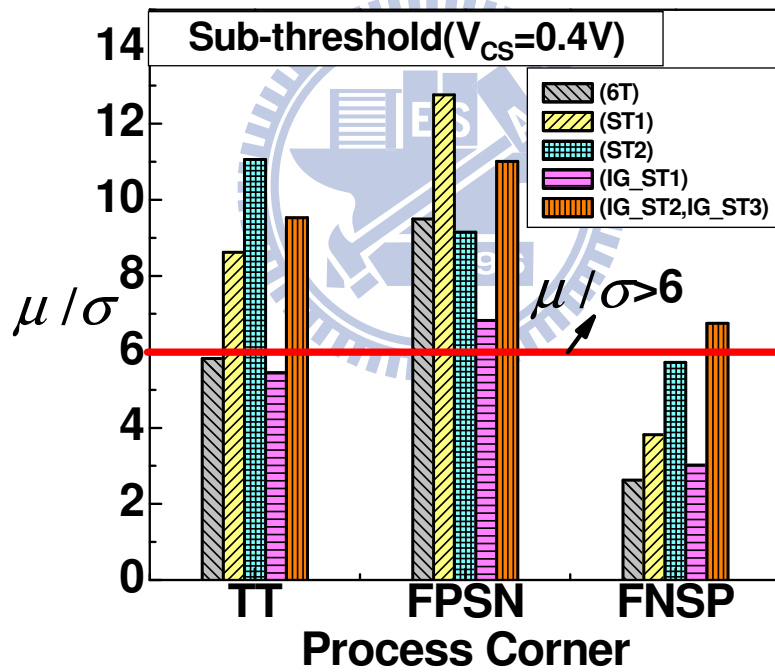
(b)

Fig. 5.8. (a) Definition of various process corners. (b) Comparison of μ/σ for RSNM of various cells at different process corners combined with local random variation (Fin LER)

(a)

(b)
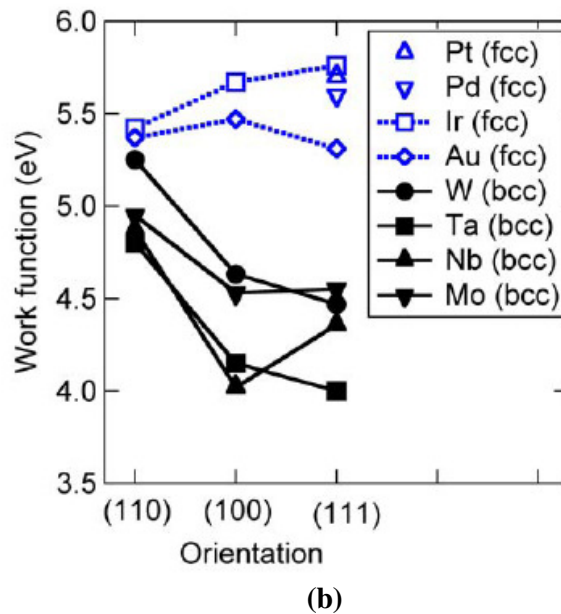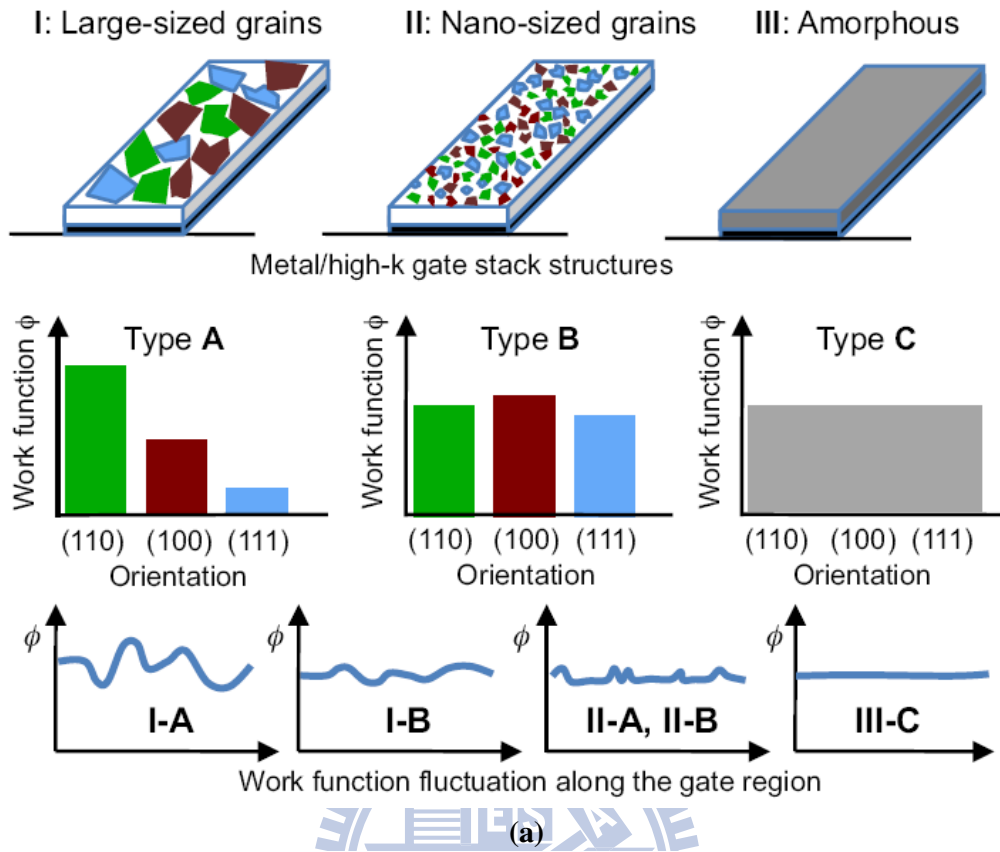
Fig. 5.9. (a) Work function variation in metal gate material from different grain size and the orientation dependency. (b) Two crystal structures, fcc and bcc, which are different in work function variation on orientation dependency [33].
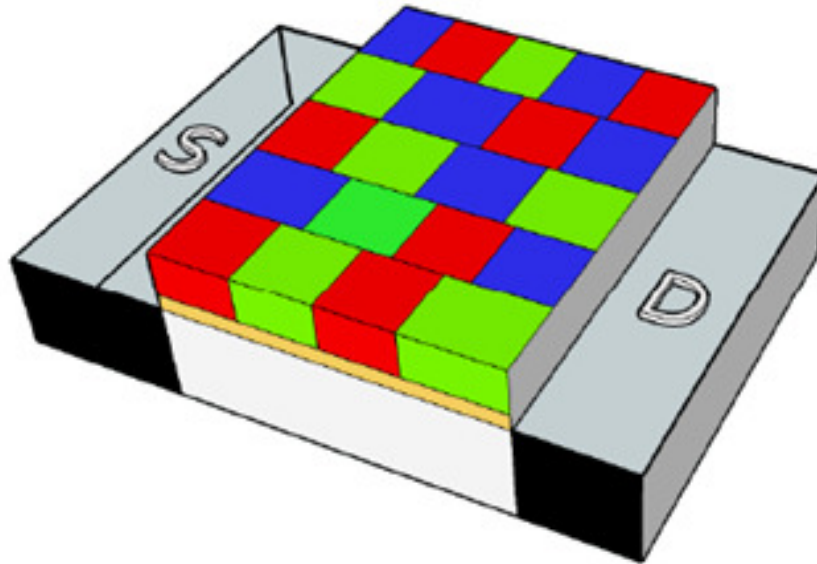
(a)
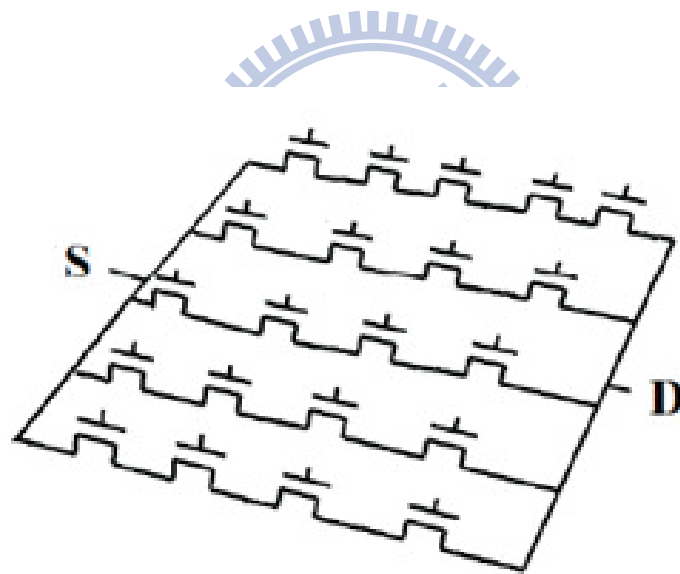
(b)

Fig. 5.10. (a) The distribution of metal grains for a metal gate transistor. Different colors represent different orientations. (b) The effective model for describing the transistor electrical behavior [35].

Table 5.1. Physical properties of TiN, which has been used in this work [33, 34]

Material	Orientation	Probability	Work function(eV)	Grain Size(nm)
TiN	<200>	60%	4.6	4.3nm
	<111>	40%	4.4	
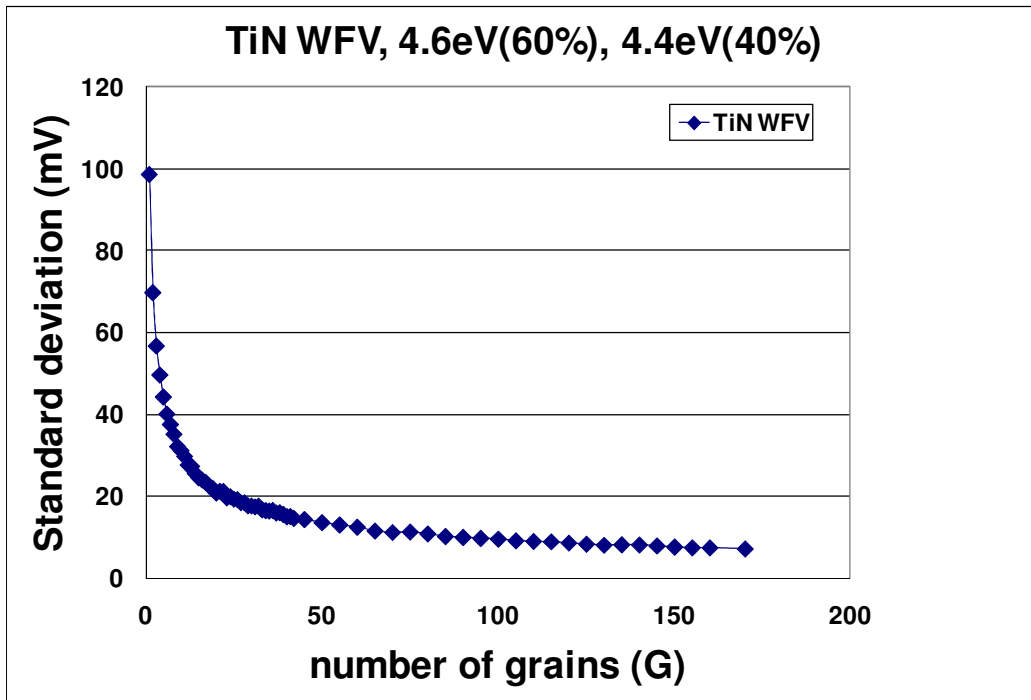
Fig. 5.11. Work function variability for various number of grains.
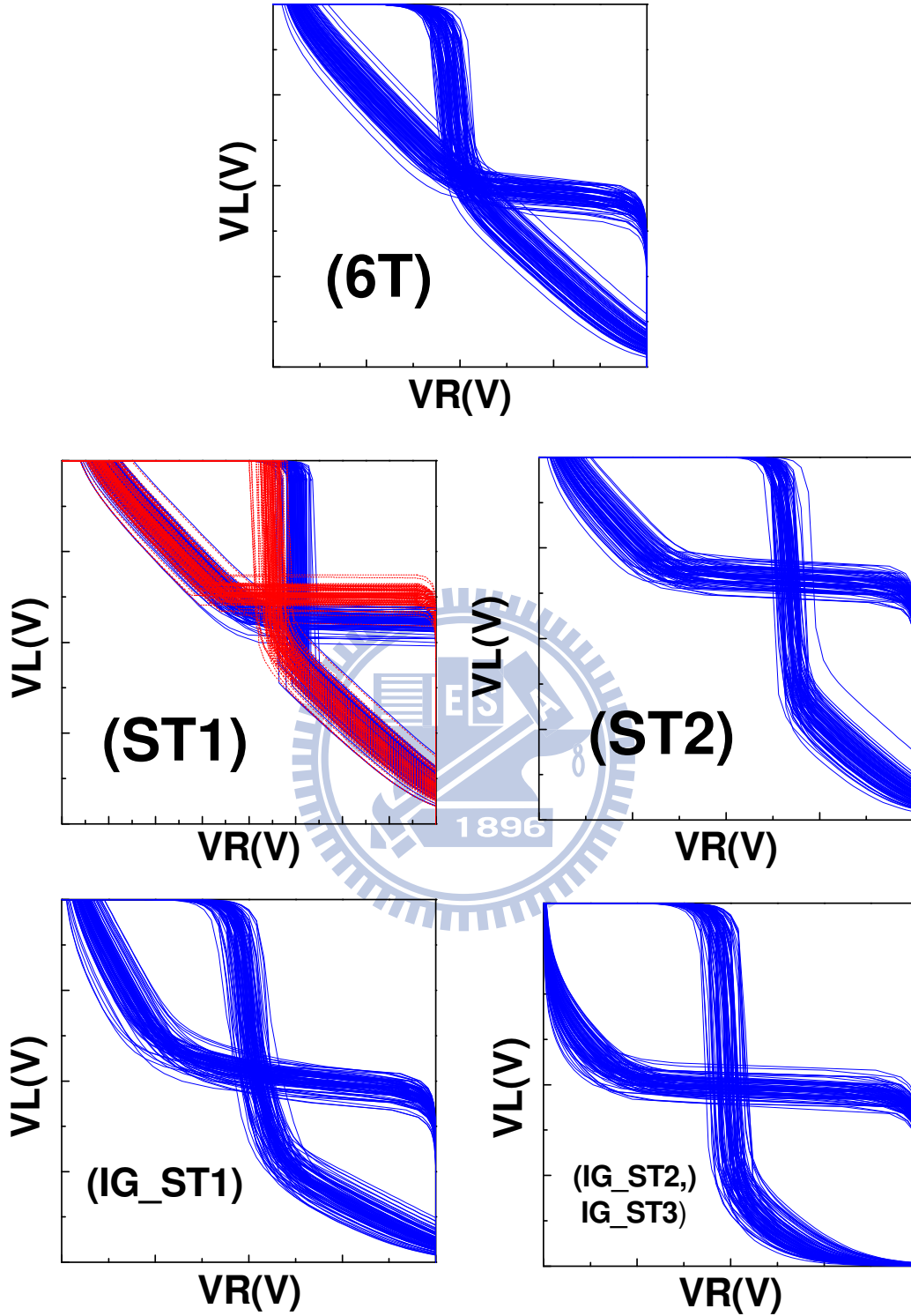
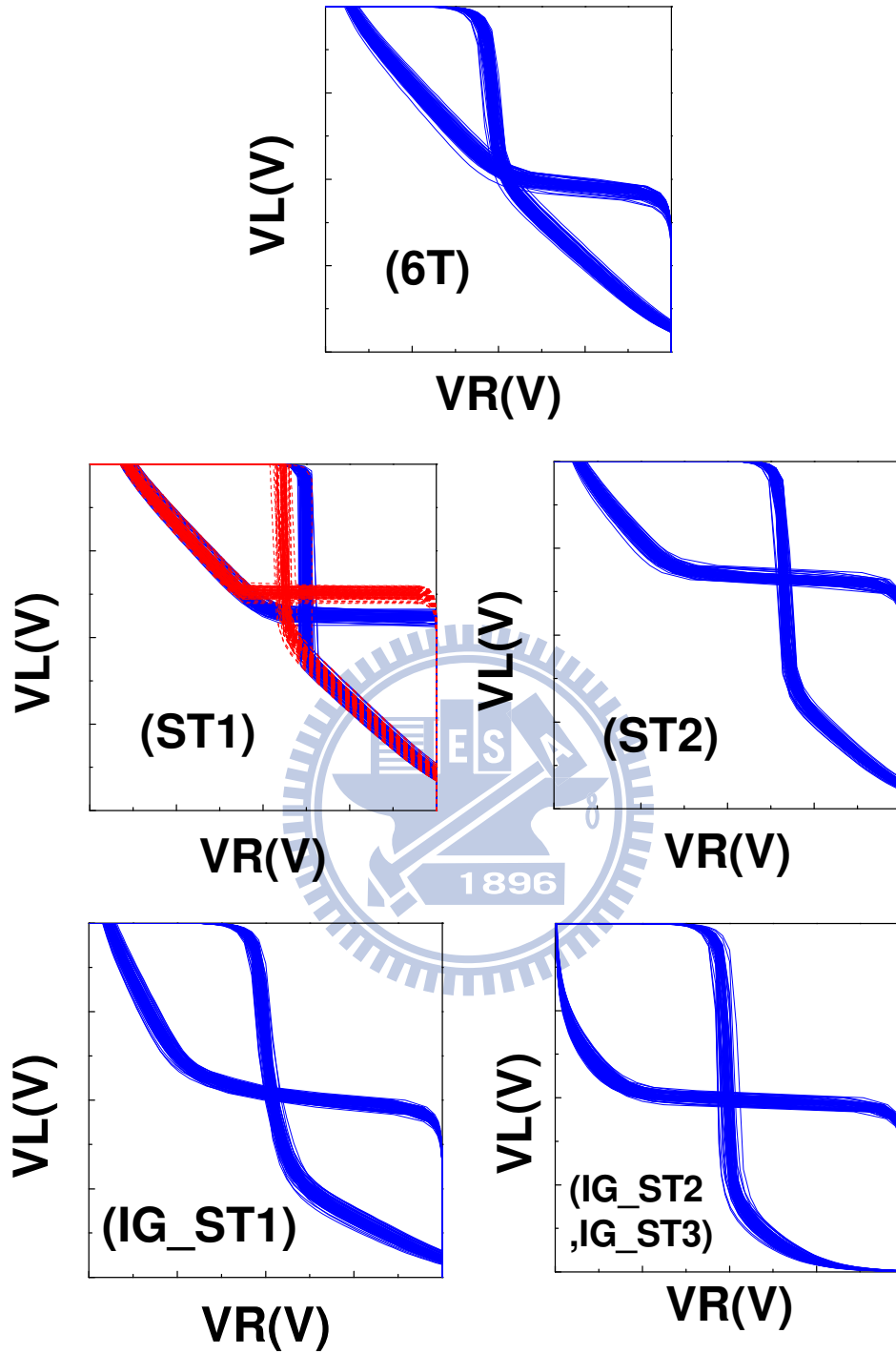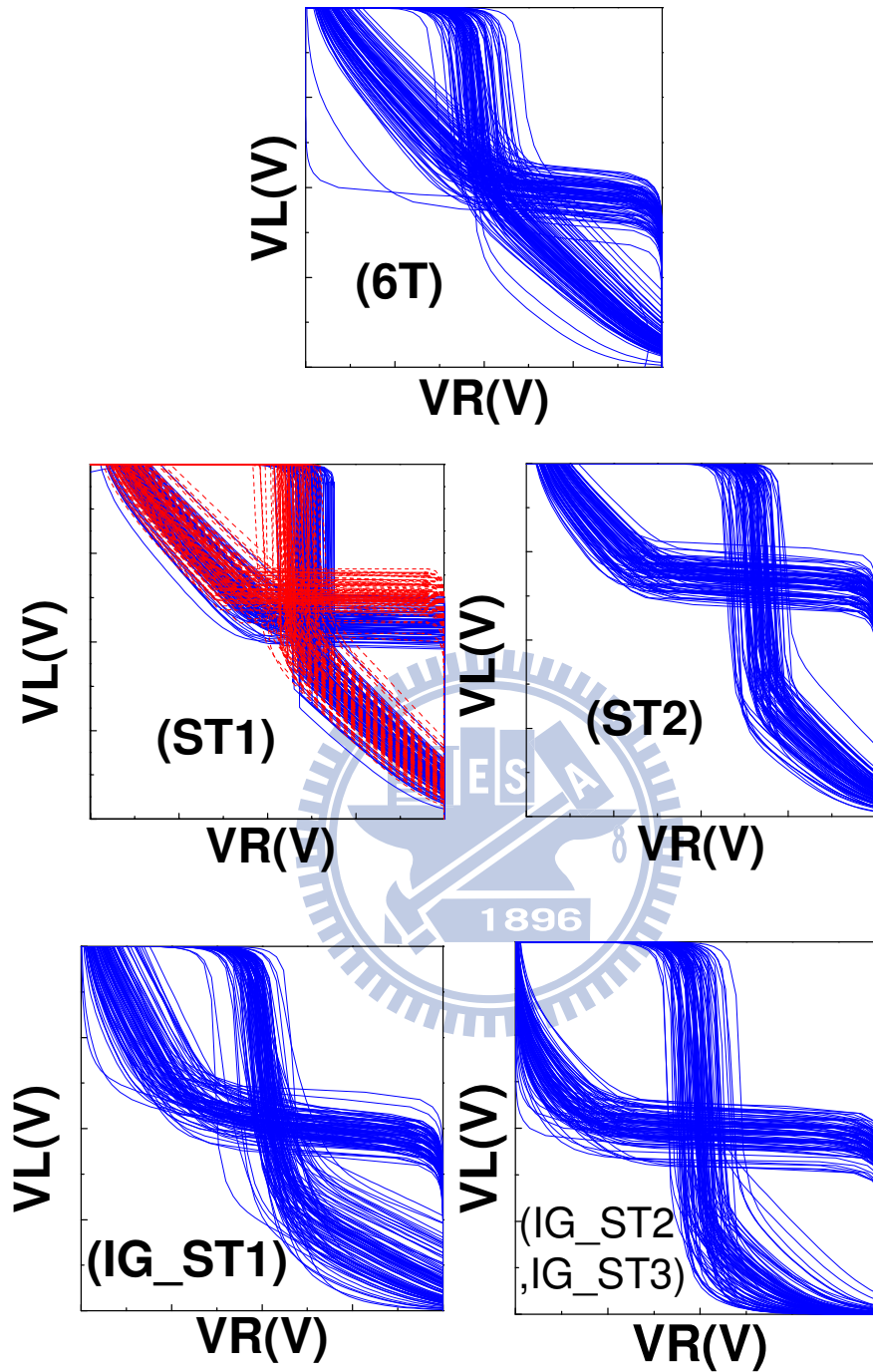**Fig. 5.12.** Voltage transfer characteristics of various cells considering WFV from 3D mixed-mode Monte Carlo simulations.

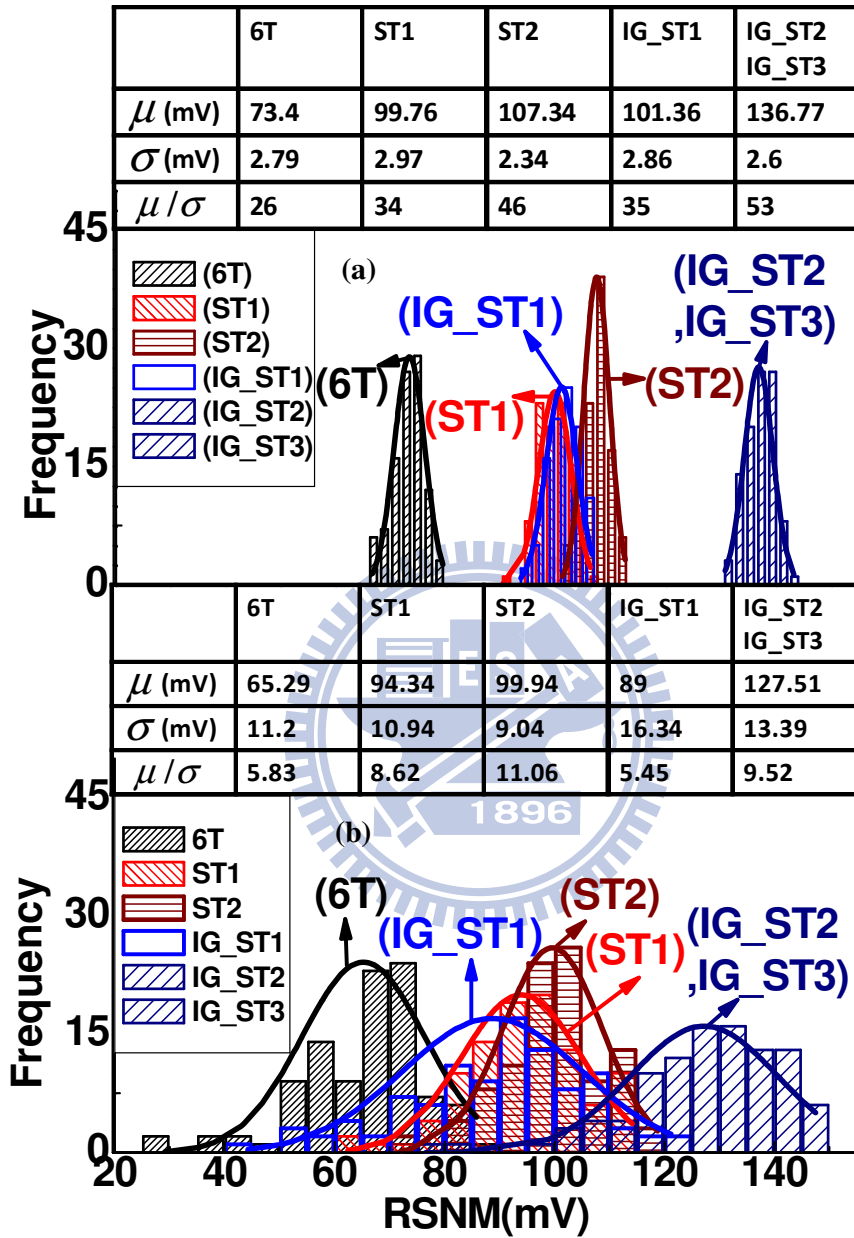|	6T	ST1	ST2	IG_ST1	IG_ST2 IG_ST3
μ (mV)	70.98	98.43	104.58	97.19	132.55
σ (mV)	6.08	6.96	6.87	7.95	6.49
μ/σ	11.67	14.14	15.22	12.22	20.42
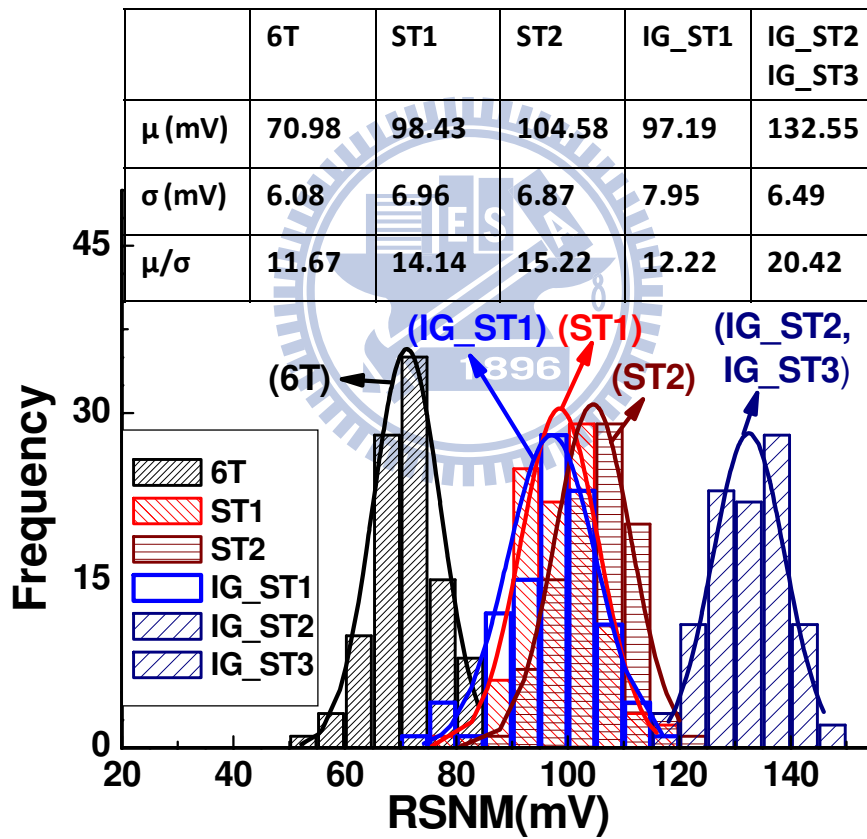
Fig. 5.13. Probability distribution of RSNM (at V_{CS} = 0.4V) considering WFV for different SRAM cell structures from 3D mixed-mode Monte Carlo simulations.

**Table 5.2.** Various parameter (L_g, $W_{fin}(T_{si,})$, EOT, and H_{fin}) of (a) RSNM, (b) WSNM, and (c) HSNM deviations.

Variation source / Cell type	L_g	$W_{fin}(T_{si})$	EOT	H_{fin}	Total Variation
6T	9.85%	6.41%	2.62%	0.32%	12.04%
ST1	6.07%	4.17%	1.8%	0.52%	7.6%
ST2	5.83%	3.94%	1.64%	0.21%	7.23%
IG_ST1	5.71%	7.33%	1.74%	0.27%	9.46%
IG_ST2, IG_ST3	3%	5.41%	2.42%	1.53%	6.82%

(a)

Variation source / Cell type	L_g	$W_{fin}(T_{si})$	EOT	H_{fin}	Total Variation
6T	8.58%	5.55%	2.39%	0.49%	10.51%
ST1	6.7%	4.53%	1.93%	0.41%	8.32%
ST2	7.67%	5.04%	2.22%	0.41%	9.45%
IG_ST1	4.76%	3.19%	1.18%	0.2%	5.85%
IG_ST2, IG_ST3	7.51%	4.88%	2.03%	0.45%	9.19%

(b)

Variation source / Cell type	L_g	$W_{fin}(T_{si})$	EOT	H_{fin}	Total Variation
6T	4.23%	2.74%	1.08%	0.21%	5.15%
ST1	3.56%	2.51%	0.74%	0.05%	4.42%
ST2	3.81%	2.57%	1.07%	0.14%	4.72%
IG_ST1	4.91%	1.94%	2.65%	0.15%	5.91%
IG_ST2	8.18%	2.11%	4.77%	0.15%	9.7%
IG_ST3	3.52%	2.48%	0.86%	0.06%	4.39%

(c)
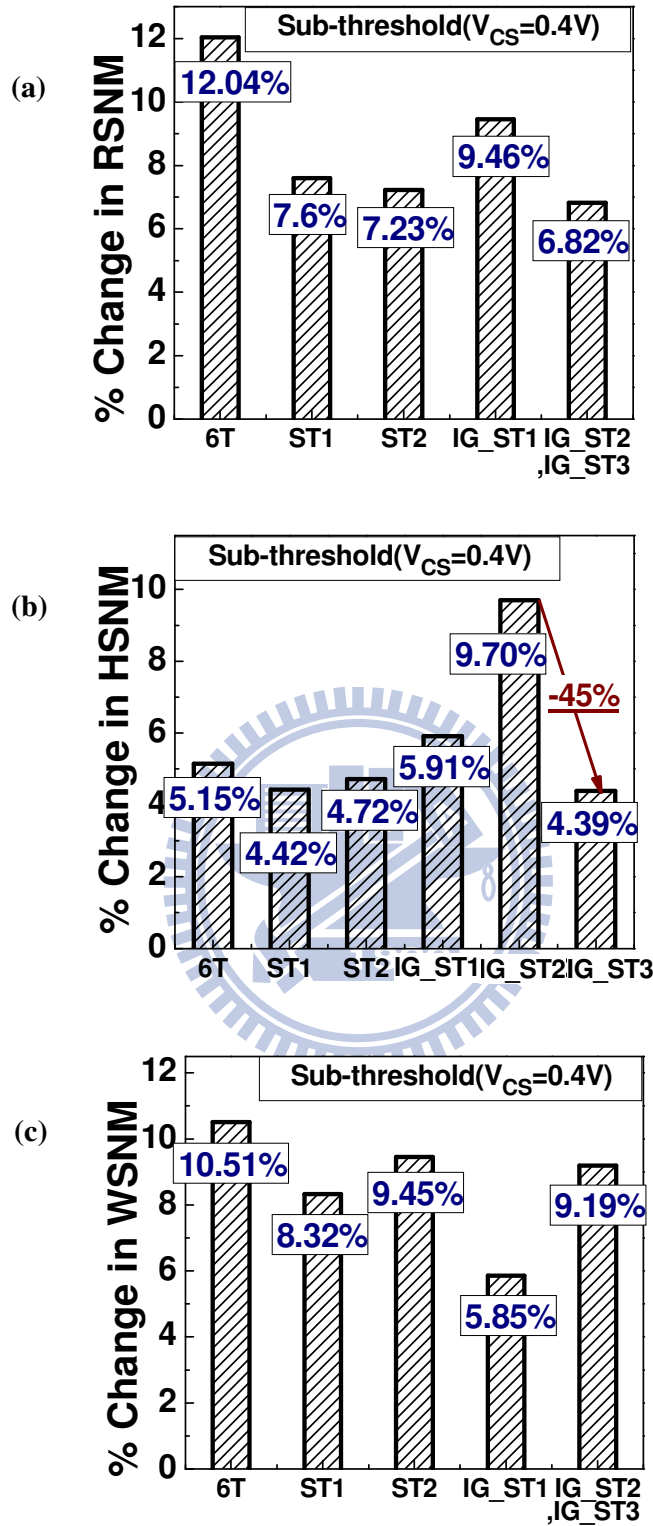
Fig. 5.14. (a) RSNM, (b) WSNM, and (c) HSNM sensitivity to process parameter variations such as L_{eff}, $W_{fin}(T_{si,})$, EOT and H_{fin} variation (-20% to 20%).

Chapter 6

Conclusions

We proposed three novel Schmitt Trigger based independently-controlled-gate FinFET SRAM cells for sub-threshold operation, and detailed the characteristic operation of Read, Write, Hold mode.

For the stability part, we comprehensively analyzed and compared the proposed cells with conventional 6T and previously reported 10T Schmitt Trigger sub-threshold SRAM cells. Our results showed significant nominal RSNM improvements in IG_ST2 and IG_ST3 cells (81% over 6T cell at V_{CS} = 0.40V) without degrading nominal WSNM and HSNM. At ultra-low-voltage (V_{CS}=0.15V), the nominal RSNM improvement could reach 110%.

The areas of the proposed cells were shown to be 30%-39% smaller (and cell Standby leakage from 20% to over 50% lower) than previously reported 10T Schmitt Trigger sub-threshold SRAM cells. The cell AC performance (Read access time, Write time) were assessed using TCAD 3D mixed-mode simulations. The proposed cells were shown to support sufficient number of cells per bit-line and offer adequate performance for the intended sub-threshold applications under worst-case bit-line data pattern for leakage current.

3D mixed-mode Monte Carlo simulations were carried out to investigate the impacts of process variations and random (LER) variations and work function variability (WFV) on the cell stability. Due to Fin LER, IG_ST2 and IG_ST3 cells

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were shown to exhibit sufficient margin (μ/σ ratio = 7) even at the worst corner (FNSP). With enhanced cell stability, reduced cell area and Standby leakage, adequate performance, and robust tolerance to process variations and random variations, the proposed IG_ST2 and IG_ST3 cells are the promising candidates for future ultra-low-voltage sub-threshold applications.
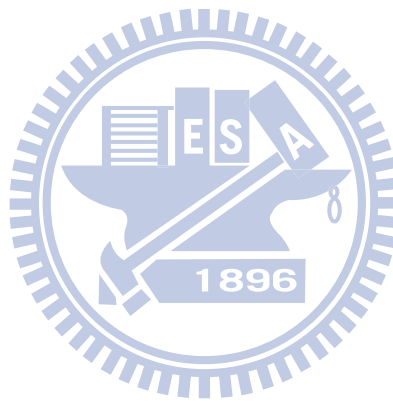
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碩士論文題目 ：

史密特觸發器為基礎操作在次臨界區以獨立閘極控制場效鰭狀電晶體之靜態隨機存取記憶體

Independently-Controlled-Gate FinFET Schmitt Trigger Sub-threshold SRAMs