國立交通大學

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極紫外光輻射對先進非揮發性記憶體的影響

Effect of Extreme Ultra-Violet Radiation on Advanced Non-volatile Memories

研 究 生：顏志展

指導教授：崔秉鉞 教授

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摘要

在本論文中，我們研究極紫外光對非揮發性記憶體照射產生的傷害進行研究，主要分為在薄膜電晶體(TFT)基板上的矽/氧/氮/氧/矽(SONOS)記憶體與多閘極氮化鈦奈米晶粒（TiN NC）記憶體兩類。

這兩類記憶體元件的臨界電壓值皆隨著照射時間增長而逐漸地減少，顯示在極紫外光照射時，閘極介電層中有少量的正電荷產生。

在 TFT-SONOS 記憶體中，寫入狀態的臨界電壓值在記憶窗口特性中稍微的上升，表示有一些新的補陷產生。經過長時間的室溫存放，寫入及抹除狀態的臨界電壓可回復至照射前的值，顯示輻射產生的補陷可以隨著時間自我修復。我們擷取補陷密度的能量分佈，其結果可支持補陷密度增加又回復的解釋。照射後寫入速度提昇但抹除速度減緩，不過這些現象同樣地經過長時間存放後可以回復。在高抹除電壓時可觀察到抹除飽和現象，推測是由於照射傷害到阻擋層所造成。受照射元件在儲存資料持久性的表現上沒有明顯的劣化。耐久度的測試則嚴重劣化，特別在抹除狀態的部份，顯示劣化的阻擋層造成強烈的背向電子注入發生。這個劣化現象在經過攝氏六百度退火後仍無法回復。

在多閘極氮化鈦奈米晶粒記憶體中，幾乎所有記憶體特性皆未被極紫外光輻射影響，顯示奈米晶粒記憶體相對於SONOS記憶體擁有較好的輻射抵抗能力，這主要是因為兩者儲存電荷機制的差異。此研究顯示極紫外光微影技術對於先進奈米晶粒記憶體的進一步微縮是一個可能的解決方法並且不會有可靠性的問題發生。SONOS記憶體則需要進一步的研究，以改善對EUV輻射損傷的抵抗能力。

Effect of Extreme Ultra-Violet Radiation on Advanced Non-volatile Memories

Student: Chih-Chan Yen Advisor: Bing-Yue Tsui

Department of Electronics Engineering
Institute of Electronics
National Chiao Tung University

Abstract

In this thesis, the effects of extreme ultra-violate (EUV) irradiation on the characteristics of the thin film transistor (TFT) Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) non-volatile memory (NVM) and multi-gate TiN nano-crystal (NC) NVM are investigated.

Both memory devices exhibit a gradually reduction of threshold voltage (V_t) with irradiation time, which indicates that a small amount of the net positive charges are generated in the stacked dielectric during EUV irradiaiton.

On the TFT-SONOS memory, The V_t values in the program state increase slightly after EUV irradiation, which implies that a few new traps are generated. After long-term storage at room temperature, the V_t values in both program and erase states recover to the pre-irradiation values, which indicates the EUV irradiation generated traps can be self-annealed with time. The extracted energy distribution of trap density in the Si3N4 charge trapping layer confirms the above explanation. Erase saturation is observed at high erase voltage operation because the blocking layer is damaged by EUV irradiation. The program speed increases but the erase speed decreases. However,

these phenomena can also be recovered after long-term storage. The charge retention characteristic does not degrade significantly. The endurance degrades severely, especially in the erase state, which implies the strong electron backside injection occurs due to the degradation of blocking layer. This degradation cannot be recovered after 600°C annealing.

On the multi-gate TiN NC memory, almost all the memory characteristics are not affected by the EUV irradiation. It exhibits the NC memory has much better EUV radiation immunity than the SONOS memory due to the difference in the charge trapping mechanisms. This work suggests that the EUV lithography could be a potential solution for advanced NC memories to further scaling-down without reliability issue. Further study on the SONOS memory is required in order to improve the EUV radiation damage immunity.

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Chapter 1
Introduction

1-1 Extreme Ultraviolet Lithography Technology

The development trend for semiconductor industry follows the Moore's law continuously in the past several decades, that is, the number of transistors on an integrated circuit (IC) chip doubles approximately every 18 months. To scale down device geometry, fine pattern technology is strongly demanded. Currently, immersion lithography with 193nm argon fluoride (ArF) excimer laser as light source is the main technology to fabricate IC chips at 45nm or even 32nm nodes by combining various methods such as double patterning, immersion fluid, and higher refractive-index lens to enhance resolution. However, 193nm immersion lithography has been faced the physical limitation, it is hard to support patterning further down beyond 22nm. In order to keep pace with the demand for the patterning of ever smaller dimensions, the direct solution is to use a shorter wavelength light source. Thus, extreme ultraviolet lithography (EUVL) technology attracts more and more attention recently. [1-5].

According to the International Technology Roadmap for Semiconductors (ITRS) 2009 report [6], EUVL and maskless lithography like E-beam writing are the two most promising mainstreams for the next generation lithography (NGL) technology with a resolution down to 22nm and beyond, the other is imprint lithography. The advantages of E-beam writing are high resolution, maskless, diffraction-free, high design flexibility, and relatively mature instrumentation. However, low throughput is still a big issue because of its long writing time; therefore, E-beam writing is suitable for production of multiple but low volume of logic ICs. In contrast to E-beam writing, EUVL can mass-produce IC chips with mask by adapting conventional optical lithography principle, so it is suitable for production of simple but high volume of memory ICs. Thus, the most attraction over the other candidates is that EUVL is an optical lithography technology which has many similarities with conventional optical lithography, this means that many years of industry learning on optical lithography can be applied directly to EUVL; so it is in reality an extendible technology that can support resolution down to 16nm node by using binary masks and to 11nm node by using more advanced mask types. Other advantages of EUVL such as use of 4X reticles are easier to write than 1X reticles, lower numerical aperture (NA) optics which provides good depth of focus (DOF) can eliminate the need for optical proximity or phase shift correction of masks and so on. [2-3]

However, EUVL has some significant differences compared with conventional optical lithography; all of these differences are owing to the extremely short wavelength light used in EUVL. The wavelength of EUV light is 13.5nm which would be strongly absorbed in all materials. For the purpose of minimizing EUV absorption, a number of constraints have been emerged on the design of EUV lithography tools. There are typically four points at which the design of EUV lithograph tools differ significantly from conventional deep ultraviolet (DUV) tools [2].: The first point is EUV light source. Compared with conventional DUV tools using excimer laser as light source, EUV light is produced by hot plasma of suitable materials like tin, xenon, or lithium [7], mainly two types of mechanism which materials excited are either by laser produced plasma (LPP) sources or by discharge produced plasma (DPP) sources. The second point is reflective optics. Optical systems are the core of an exposure tool which determines the performance of lithographic technology. Since EUV radiation is strongly absorbed in all materials, EUV optical systems must be designed as completely reflective instead of employing conventional refractive optical systems. Nevertheless, the EUV reflectivity at near-normal incidence is too low for singular materials. In order to achieve superior reflectivity, surfaces must be coated with multilayer thin films which consist of a number of alternating layers of molybdenum and silicon (MoSi), called "pseudo-Bragg reflectors". By applying the optimum of multilayer in the range between 11 and 14 nm, EUV reflectivity of up to 70% can be achieved. The third difference is reflective reticles. EUV light is not penetrated by any optical materials as mentioned previously, so EUV reticles are also reflective same as optical systems. Reflective reticles are made by coating MoSi multilayers stack on an ultra low thermal expansion glass substrate, followed by a series of buffer, absorber, and anti-reflecting layers. The absorbing layers are then patterned by using conventional mask-manufacturing technology to define required features. Moreover, defects in any coating layer is a critical issue should be prevented. Reticles must be essentially defect-free in order not to deform the printed pattern on the wafer. The last difference is vacuum environment. Wafers must be exposed under high vacuum environment in EUV exposure tool to prevent EUV intensity losses by gaseous absorption and contamination or oxidation of the optical elements.

EUVL developments have been investigated nearly thirty years. The first concepts regarded for applying EUV light to all-reflective projection lithography were proposed by groups of Lawrence Livermore National Laboratories (LLNL) [8] and Bell Laboratories [9] in 1988. Thereupon most of researches and developments were performed during the early 1990s. The EUV Limited Liability Company (EUV LLC) was formed in the US in 1997 to provide funding and development, this consortium is composed of six semiconductor manufacturers (AMD, Intel, etc.) and three national laboratories. In 2001, EUV LLC constructed the first full-field EUV exposure tool which called Engineering Test Stand (ETS) to demonstrate the feasibility and capability. Other leading countries of semiconductor industry have also paid many efforts to develop EUVL. Especially in European Union, ASML built the world’s first 0.25NA EUV full-field step-and-scan systems with automated wafer and reticle handling, Alpha Demo Tools (ADT) [10-12] in 2006, two of the ADTs have been shipped to two research centers, IMEC in Leuven, Belgium [13] and CNSE in NewYork, US. Fig. 1-1 shows pictures of ASML ADT at the two research centers [14]. The typical ADT structure consisting of source module, illuminator, projection optics box, wafer and reticle stages, material handling module is shown in Fig. 1-2 [14]. In addition, a joint association of EUVA was founded in Japan in 2002. In Korea, SAMSUNG purchases the first pilot EUVL beta-tool in 2008. Recently, TSMC will take delivery of a TWINSCAN NXE:3100 EUVL system which is one of the six same-type systems for ASML’s customers in the world. Hence, in spite of EUVL still has some issues to be optimized including power, optics, mask, resist, and metrology, many of efforts until today show that EUVL can be implemented by semiconductor manufacturers for mass-production later in this decade.

1-2 Radiation Damage Effects

In the past, the driving force on the study of radiation damage effects on semiconductor devices is that in order to develop the radiation-hardened devices which can function appropriately in certain radiation-rich environments. It is because when MOS devices are exposed to an ionizing radiation environment, various radiation sources with high energetic photons or particles such as gamma-ray, X-ray, electrons, protons, alpha-particles, and heavy ions, will lead to several degradations of the device performance or shrink the operating lifetime. Moreover, the most serious of all, MOS devices may be failed with the increase of exposed time.

The common requests for better radiation tolerance devices in a radiation-rich situation are including artificial satellites revolution and spacecraft exploration in outer space, nuclear weaponry and radio detector in military or light source with high energetic particles physical experiments. However, radiation damage takes place not only in the above environments, the semiconductor industry manufactures, for the sake of scaling down the devices to get ever higher density and performance IC chips for the next generation technology nodes, utilizes advanced processing techniques such as reactive ion etching (RIE) and high density plasma RIE (HDP-RIE) in dry etching process, lithography with X-ray or E-beam light source, and other plasma processes. These techniques contain potential radiation sources which may cause significant radiation damage to the devices being fabricated. Today, EUVL is one of promising candidates for the NGL technology, the wavelength of EUV light source in the range of soft X-ray could also degrade the device performance that should be avoided. Since integrated circuits are the foundation stone of the semiconductor industry, it is necessary to understand the basic mechanisms affected on the alteration of electrical characteristics of MOS devices, and then the methods for improvement and the elimination of radiation damage effects can be achieved to ensure normal functionality of the IC chips after finishing the fabrication.

A useful, comprehensive, understandable study on the radiation damage was published by T. P. Ma for realizing deeply in this field [15]. The basic concept of ionizing radiation is that radiation sources which have enough energy to break atomic bonds and generate a large amount of electron/hole pairs in materials; as for the structure of MOS devices, the most sensitive to ionizing radiation is gate dielectric layer because of its weak radiation tolerance. Fig. 1-3 shows a schematic energy band diagram of ionizing radiation induced electron/hole pairs in the MOS structure, with the case of positive bias applied to the gate [16]. In the first picosecond (ps) behind carrier generation, a small portion of the electrons and holes will recombine which depends on the type of incident particles and the applied field and the energy, but most of the other electrons are swept to the gate rapidly on the order of 1 ps and the holes that escape initial recombination are relatively motionless because radiation induced electrons possess much high mobility in comparison to holes. As a result, the significant concept for ionizing radiation is that electrons do not play an important role in determining the alteration of electrical characteristics of MOS devices. This event typically results from two key factors. First, electrons are more mobile than holes in the oxide layer which has been mentioned above; the mobility of electrons is probably 20 $cm^2V^{-1}s^{-1}$ at room temperature and gradually increase to 40 $cm^2V^{-1}s^{-1}$ at lower temperature. Instead, the mobility of holes is simply about 10^{-4} to 10^{-11} $cm^2V^{-1}s^{-1}$. Second, long term trapping rate of hole is three to six times greater than electron trapping rate, so hole trapping dominates the whole effect with respect to the long term charges trapping caused by radiation in the oxide layer. Consequently, the holes prefer to stay behind and are adjacent to their generation center, transforming into net positive charges and then leading to negative threshold voltage shifts in MOS devices. Over a period of time, approximately one second, the relatively movable holes proceed a irregular trap-hopping transport through the oxide to the SiO_2/Si interface; of course, some holes may also be trapped within the oxide during this process. In addition, it is worth noting that the hole transport is a temporarily process, will give rise to a transient annealing in the threshold voltage shift. As holes arrive at the SiO_2/Si interface, a portion of them are captured in deep-level trapping sites for a long time, causing a permanent threshold voltage shift unless devices undergo a relatively high temperature annealing process for the purpose of detrapping the holes which are captured in deep sites. The last process is a radiation-induced buildup of interface traps at the SiO_2/Si interface. Once hopping of holes move to the interface then they may capture electrons and create interface traps within silicon bandgap. Interface traps can be charged as positive, negative or neutral depending on the silicon surface potential.

MOS devices exposed to a radiation environment could exhibit threshold voltage shift, subthreshold swing degradation, high gate leakage current, gain decrease, and speed slow-down or even devices breakdown. Recently, most of the studies regarding the radiation damage on MOS devices typically investigated the dependence of different total dose and oxide thickness [17] with a variety of gate dielectric materials, especially in high-k dielectrics [18-22]. Another researches studied the reliability issue that combine the bias temperature instability measurement and irradiation effect [22-24]. In addition, annealing effect is a significant factor to increase the radiation tolerance in dielectrics [20, 25] or on the recovery of radiation-damaged devices [19, 25-26], whether it proceeds during the process or after the radiation. However, not only logic ICs, memory ICs also suffer from ionizing radiation that could be severely damaged the memory characteristics such as the degradation of memory window, program/erase (P/E) speed, retention, endurance, and disturbance. Several works in the literature have shown that conventional floating gate non-volatile memories exhibit poor tolerance against ionizing irradiation [27-29]. Compared to floating gate non-volatile memories, nano-crystal non-volatile memories possess higher tolerance to radiation effects because of the different trapping mechanism of discrete charge storage centers [30-33]. Nevertheless, to our knowledge, no works have been devoted to investigate the EUV radiation damage affects on the different type of advanced non-volatile memories.

1-3 Evolution of Non-volatile Memory

In a modern life, we can find everywhere the novel of portable electronic products bringing the convenience and practicality for people. For instance, cellular phones, digital still camera, notebook, USB flash drive, iPod, and even gaming like PSP, etc [34]. The successes of all of them as mentioned above are attributed to the applications of memory technology. There are two typical types of memory: volatile and non-volatile. The former means a memory that requires power supply to maintain the stored information and data lose while the power is turned off. Instead, the latter has a capability to retain the storage data for a long time even without power supply. Today, flash is the mainstream of the non-volatile memory technology [35-36]. The evolution of flash memory mainly can be classified into three types: floating gate (FG), Silicon/Oxide/Nitride/Oxide/Silicon (SONOS), and nano-crystal (NC) type in sequence.

In history the first FG non-volatile memory was published by D. Kahng and S. M. Sze at Bell Labs in 1967 [37]. The stack-structure FG memory used a conductive layer as a charge stored layer, which is sandwiched between two insulated dielectrics. The current FG memory device structure is shown in Fig.1-4. Despite the conventional FG memories have widely applications in non-volatile memory market share, they face some crucial constraints while the device is scaling down. First, the issue of reducing the operation voltage, it will degrade memory performance since the read and program/erase (P/E) speeds are related to the operation voltage. Second, much thinner tunneling oxide is required for continuous scaling the device structure. Although the thinner tunneling oxide would speed up the operation speed, the retention characteristics of charges stored in FG may degrade severely. Thus there is a trade-off between reliability and speed for determining the tunneling oxide thickness.

Third, the quality of tunneling oxide degrades via tens of thousands of P/E cycles, generated defects form leaky path will result in the whole charges stored in the FG losing. It is because that conventional FG memory uses conductor as a charge trapped layer, as long as one leaky path generates, all of charges would leak through the path to the silicon substrate.

Therefore, in order to improve the way of charge storage, SONOS-type memory has been developed [38-39]. In 1967, Wegener et al. invented the first metal gate nitride memory device [40] with stack of Metal/Nitride/Oxide/Silicon (MNOS) structures. However, charges stored in the nitride trapping layer would leak to the top gate directly. Therefore a method to improve the retention was introduced the silicon dioxide as a blocking layer between the top gate and the nitride charge trapping layer. The Oxide/Nitride/Oxide (ONO) gate dielectric stack is shown in Fig. 1-5. The basic charge storage mechanism of SONOS-type memory is storing charges in discrete traps of the silicon nitride layer. When defects are generated by several P/E operations in the tunneling oxide, only portion of charges which are proximal to the defect will lose. Hence, SONOS-type memories exhibit better retention characteristic with respect to the conventional FG memory and have other advantages such as good compatibility with standard CMOS process, lower operation voltage and power consumption, and the importance of scaling feasibility. Nevertheless, they still have some problems to be solved. First, erase can operate in the long pulse width only when the erase voltage is small. Once erase voltage is large, threshold voltage may saturates owing to the counteract of electron current tunneling through blocking layer and hole current tunneling through tunneling layer, which is called "erase saturation" [41], is a poor characteristic for SONOS-type memories. Second, charges stored in the trapping layer may migrate to the nearest trapping nodes, called "charge migration" [42]. It will lead to the change of memory characteristics. In addition, the disturbance effect on SONOS memory cell array is also an issue that stored charges may transfer to the other memory cell due to the sharing of the same word-line or bit-line.

For the sake of further modifying these problems mentioned above, a novel structure of NC non-volatile memory has been proposed and is view as a good potentiality for next generation non-volatile memories. The main attraction is its charge stored mechanism. As shown in Fig. 1-6, every isolated nano-dot can store few electrons and each of them is surrounded by insulated dielectrics in the trapping layer. Besides, the surrounding dielectric and nano-dots possess higher potential barrier to prevent stored electrons from escaping. Consequently, NC memories exhibit better retention characteristics than SONOS type memories. When leak paths are generated by defects, only few electrons stored in specific nano-dot which connects with leaky path will be lost while most of the others are remained. In addition, the disturbance effect can be eased up since the charge migration is suppressed by good isolation between any two nano-dots. Another advantage is the increasing of gate coupling effect when vertical electric field across nano-crystals, the work function of nano-crystals can be tuned to optimize the device performances by using variety of metal materials to form nano-crystals [43-45]. Due to these merits, the thickness of tunneling oxide in NC memories can be decreased without degrading the retention performance, and then the P/E speed and power consumption can be improved. For optimizing memory performances of the NC memory, higher density, uniform distribution and suitable size [46] of nano-crystal should be achieved.

1-4 Motivation

As mentioned in Section 1-1, EUVL is one of the most promising next generation lithography technologies for sub-22nm technology nodes. In the recently years, many semiconductor manufacturing companies have installed full-field EUV lithography systems showing the possibility for substituting present lithography technology. However, the wavelength of EUV light is 13.5nm which is strongly absorbed in all materials. The relative energy is 91.8eV which is much higher than the chemical bonding energy in dielectrics and the band gap of gate dielectric layers. Once MOS devices are exposed to EUV, such high energy radiation may cause some problems including the generation of electron-hole pairs in dielectric, interface states at dielectric/silicon interface, and traps or defects due to broken bonds in bulk dielectric. These phenomena will severely degrade the performance of electrical characteristic in MOS devices.

On the other hand, because EUVL can mass-produce IC chips by adapting mask sets, it is recognized more suitable for memory ICs rather than logic ICs. For this reason, the impact of EUV irradiation induced damages on the characteristics of memory devices being fabricated should be investigated. Although the EUV light is prone to be absorbed in all materials which is mentioned above, indicating that gate dielectric layers will not be damaged at the back-end-of-line process owing to the protection by gate electrodes and inter layer dielectrics. Nevertheless, if the protected layer is not thick enough, EUV will penetrate the gate electrode to damage the gate dielectrics at the back-end-of-line processed and of course at the front-end-of-line process.

Among non-volatile memories, SONOS and NC memories are two of the most promising candidates for next generation non-volatile memories. Therefore, they will face the lithography process with EUVL systems absolutely. Only when we investigated the degree of EUV radiation damage affected on the electrical characteristics of these memory devices, the improved methods for prevent from damaging can be achieved to confirm normal functionality of memory ICs after process fabrication. Some literatures have been reported that the radiation damage on the FG [27-28, 47-48] and NC [28, 30-33] non-volatile memories with different radiation source such as X-ray, heavy ion, and protons. However, according to our knowledge, the EUV irradiation induced damage on the SONOS-type and NC non-volatile memories have not been reported.

In this work, we will investigate the radiation damage of EUV on advanced thin film transistor (TFT) -SONOS and multi-gate NC non-volatile memories with different dosage. After EUV irradiation, memory characteristic measurement such as memory window, P/E speed, charge retention, and endurance will be performed to observe the total dose dependent device damage. Besides, post-irradiation annealing will also be implemented to investigate whether the memory performances could be recover or not.

1-5 Thesis Organization

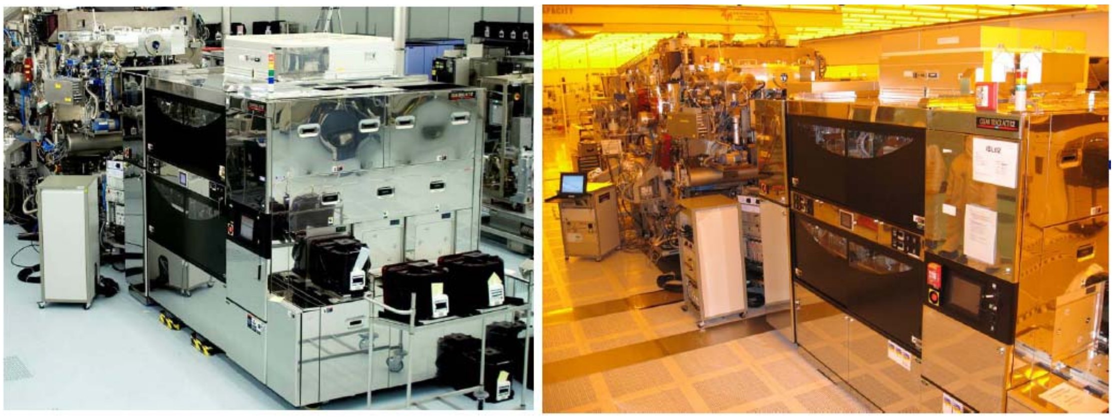
This thesis is divided into four chapters and the contents of each chapter are described as follows.

In chapter 1, the development of EUVL technology has been introduced, the effect of radiation damage on MOS devices has been explained, and the evolution of non-volatile memory has been reviewed. The motivation of using EUV as a radiation source exposing on advanced non-volatile memories has been illustrated.

In chapter 2, the experimental procedure and instrument setup will be described. The fabrication process of SONOS memory based on TFT structure and multi-gate TiN NC memory on SOI wafer will be illustrated. Besides, the considerations of memory characteristic measurement before and after EUV irradiation are also mentioned. Last, the method to calculate total dose will be introduced.

In chapter 3, the memory characteristics of TFT-SONOS memory and multi-gate TiN NC memory before and after EUV irradiation, and long-term storage at room temperature after EUV irradiation will be demonstrated. For the TFT-SONOS memory, we will show that the threshold voltage of memory window increases gradually with irradiation time and recovers to the pre- irradiation value nearly after long-term storage. P/E speed and endurance performances degrade after EUV irradiation. However, charge retention does not seem to change significantly. In contrast with TFT-SONOS memory, multi-gate TiN NC memory exhibits much better EUV radiation tolerance.

In chapter 4, summary and conclusions are presented and some future works are suggested.



(a) (b)

Fig. 1-1: Pictures of the ASML Alpha Demo Tool at two research centers. (a) IMEC in Leuven, Belgium. (b) CNSE in NewYork, US [14].

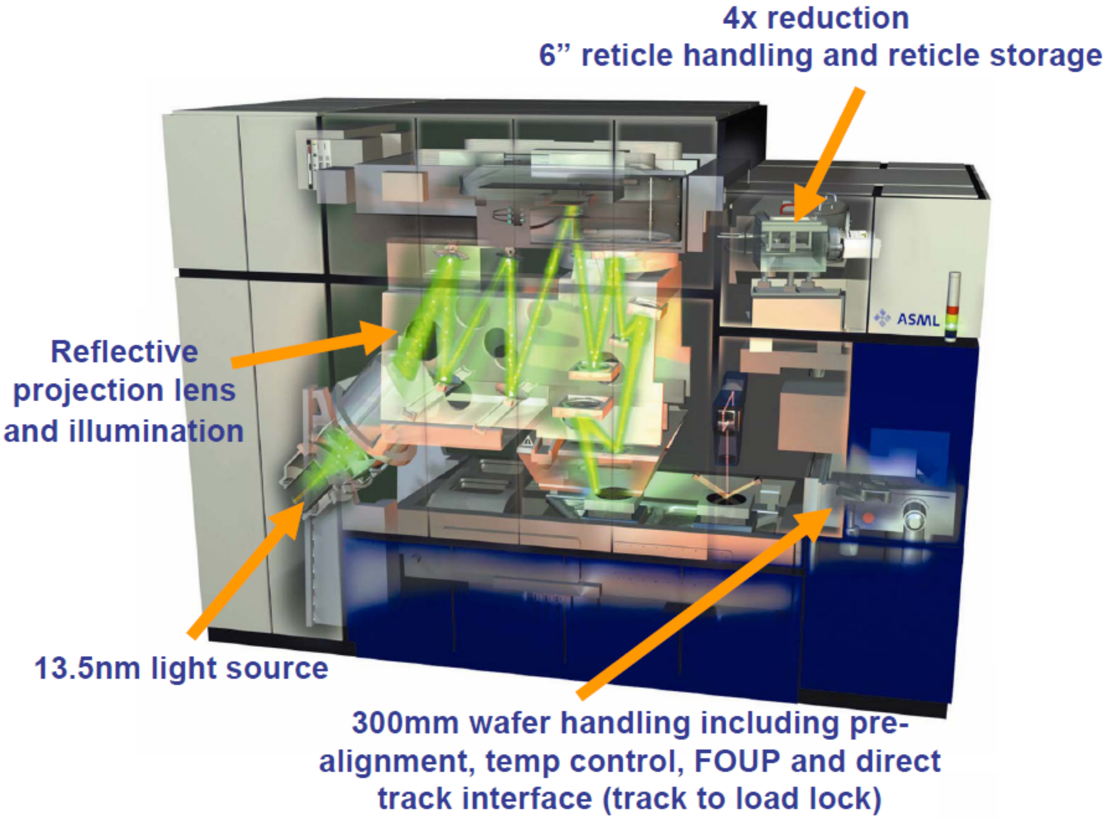


Fig. 1-2: Schematic cross-sectional configurations of the ASML Alpha Demo Tool [14].

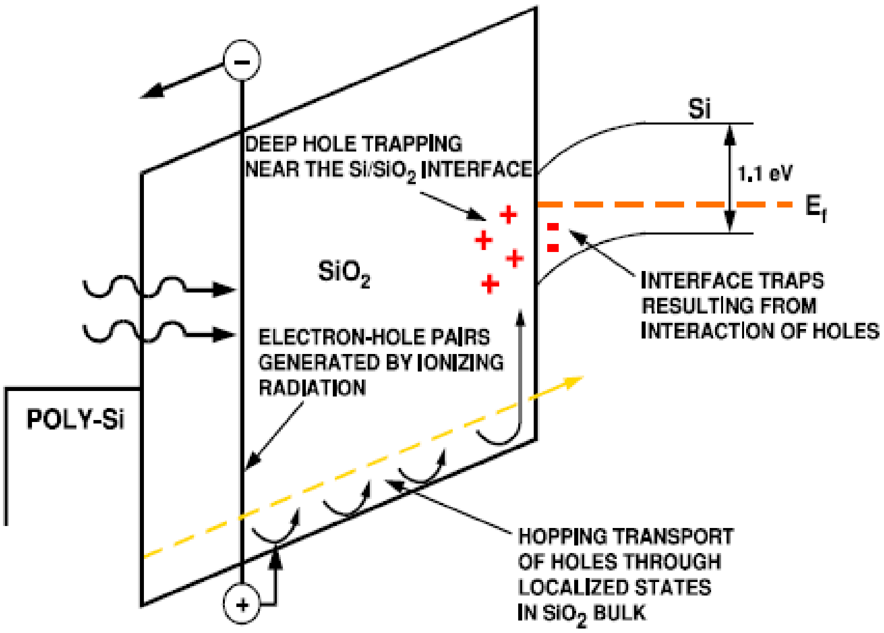


Fig. 1-3: Schematic energy band diagram of ionizing radiation induced electron/hole pairs in the MOS device with a positive gate bias [16]

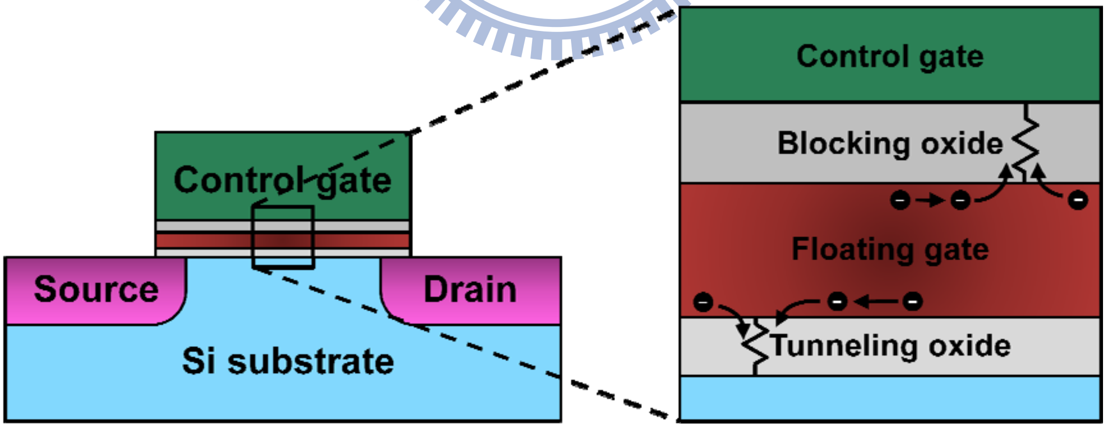


Fig. 1-4: The basic concept of floating gate non-volatile memory.

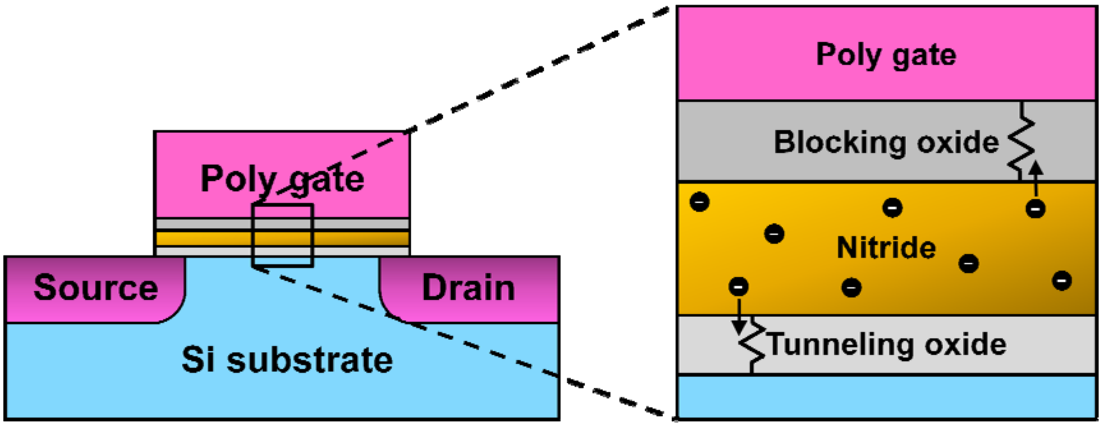


Fig. 1-5: The basic concept of SONOS non-volatile memory.

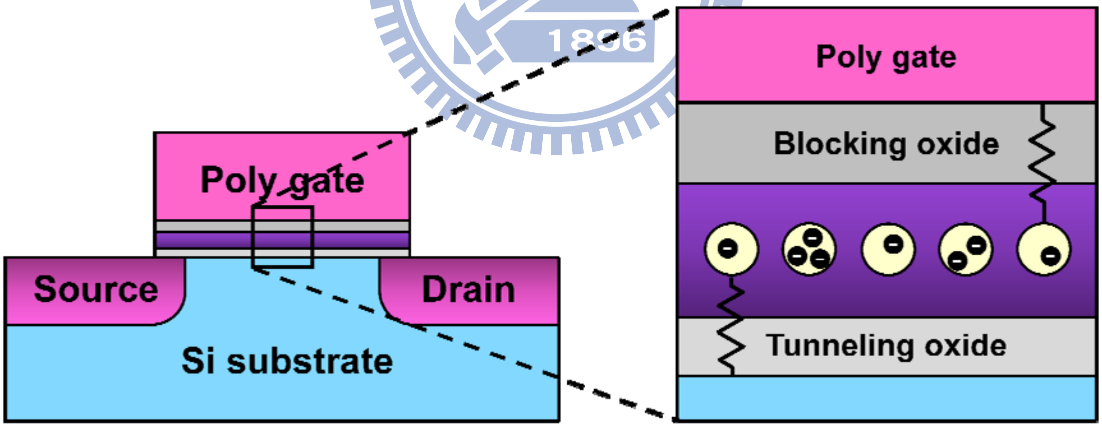


Fig. 1-6: The basic concept of nano-crystal non-volatile memory.

Chapter 2
Experimental Procedure

2-1 Instrument Setup and Environment

To investigate the EUV radiation damage on non-volatile memories, experimental equipment and system must be established. EUV irradiation experiment in this thesis was implemented at the National Synchrotron Radiation Research Center (NSRRC). The principle of the radiation produced is that electrons are accelerated in the linear accelerator and then are sent through the transport line into the storage ring, they emit synchrotron radiation after circulating in vacuum pipes for several hours. The emitted light passed through beam lines to the experimental stations and then experiments can be performed. We used both BL08A beam line and BL21B beam line as the EUV light source, the former has the energy in the range of 15-200 eV and the later has the energy in the range of 5-100 eV, both are suitable for the study of EUV radiation damages. To access more information on these beam lines, readers can refer to the website of NSRRC.

As the experimental station, our experimental system mainly consists of a main chamber, a loaded plate, a dry mechanical pump, two turbo pumps, and an ion gauge. Fig. 2-1 shows the photograph of the main chamber for irradiation experiment at NSRRC. We can see from this photograph that the main chamber has several view poles in different directions; they are used to inspect devices in the chamber to make sure the position of EUV light is directed on the device. Besides, for the sake of preventing devices from direct irradiation during alignment, a dumpy level must be utilized which is an optical instrument used in surveying to set the horizontal levels. The cross in the telescope of dumpy level is used as the light source target instead of directly irradiation to device when alignment. Fig. 2-2 (a) shows a memory IC chips on the loaded plate which is ready for irradiation. A block plate with holes in the figure is used to avoid exposing on the whole chip. The loaded plate is placed on the top of main chamber and can be adjusted in vertical direction by a mechanical axis. Fig. 2-2 (b) shows the shape of the light source of the BL08A beam line. As seen from this figure, the light source is smile-shaped and its area is about $0.016cm^2$. It is noticed that the light source in Fig. 2-2 (b) is white light instead of EUV light since the EUV light is not visible but their shapes are the same. In addition, in order to prevent the EUV light source from hitting on molecules in the air, the beam line must be maintained at ultra-high vacuum. Therefore pumping system is an important factor for this irradiation experiment which decides the time spent on each run. We utilized two turbo bumps installed on the front-end and back-end of the main chamber to speed up the pumping rate. An ion gauge is used to detect the pressure inside the chamber, generally a pressure less than $5x10^{-8}$ torr is required to start experiments.

2-2 Device Fabrication

In this study, the TFT-SONOS memory and multi-gate TiN nano-crystal memory are used to investigate the effect of EUV radiation damages. The TFT-SONOS memory sample is provided by J. Y. Lai [50] and multi-gate TiN nano-crystal memory sample is provided by C. P. Lu [51]. The device fabrications will be described briefly here and the detailed process conditions can refer to their theses.

2-2-1 TFT- SONOS Non-volatile Memory

Fig. 2-3 shows the main process flow of the TFT-SONOS non-volatile memory. The devices were fabricated on 6” p-type Si wafers with TFT structure. For the TFT structure, wet oxide was first grown to 150-nm-thick in a lateral furnace system. Then, a 50-nm-thick amorphous-Si was deposited in a low pressure chemical vapor deposition (LPCVD) system followed by a two-step annealing process. The first step was performed at 600°C for 24 hours for solid phase crystallization and the second step was performed at 900°C for 30 minutes to make sure that the grain structure would not change in the remaining thermal budget. The device structure at this step is shown in Fig.2-3(a). Active regions were then patterned by i-line lithography and etched by a poly-Si plasma etcher of model TCP 9400. After active regions patterning, 4-nm-thick TEOS oxide as tunneling oxide, 7-nm-thick Si_3N_4 as trapping layer, and 20-nm-thick TEOS oxide as blocking layer were deposited in sequence in a LPCVD system, followed by a deposition of 150-nm-thick amorphous-Si gate in the same LPCVD system. Then, the gate was heavily doped to p-type by BF_2^+ implantation at 50 keV to a dose of $5x10^{15}cm^{-2}$, and the gate dopant activation was performed by RTA annealing at 900°C for 20 seconds in nitrogen ambient. Before gate patterning, an 80-nm-thick TEOS oxide was deposited as hard mask to avoid unwanted anti-doping during n^+ S/D ion implantation. The gate patterns were transferred from i-line photo resist to hard mask by dry etching. Then, the photo resist was stripped and the gate was continuously etched by using the TEOS oxide as etching mask. Fig. 2-3(b) shows the schematic cross-sectional structure after gate patterning. Next, 10-nm-thick TEOS oxide and 50-nm-thick Si_3N_4 were deposited in a LPCVD system to form the composite spacer, as shown in Fig. 2-3(c). Then, P_{31}^+ ions were implanted into the S/D region at 20 keV to a dose of $5x10^{15}cm^{-2}$ and activated at 900°C for 20 seconds in nitrogen ambient. The gate hard mask and native oxide on S/D region were removed by dipping in dilute HF solution, as shown in Fig. 2-3(d). A

Ni film of 30-nm-thick was deposited by E-gun evaporation followed by a two-step Ni-salicide process. After first step annealing at 300°C for 30 minutes in a vacuum system to form Ni_2Si phase, unreacted Ni was removed by $H_2SO_4/H_2O_2 = 3:1$ solution. The second step was performed at 500°C for 30 seconds to transform Ni_2Si phase to NiSi phase. The finished device structure is shown in Fig. 2-3(e).

2-2-2 Multi-gate TiN Nano-crystal Non-volatile Memory

Fig. 2-4 shows the main process flow of the multi-gate TiN nano-crystal non-volatile memory. The devices were fabricated on 6” SIMOX SOI wafers with a lightly boron doped SOI layer. The doping concentration of Si layer is $1\text{x}10^{15}$ cm^{-3}, the Si layer was 40nm thick, and the buried oxide was 150nm thick as shown in Fig. 2-4(a). At first, fin-type active regions were patterned by E-beam lithography and plasma etching. Then, the tunneling oxide was thermally grown to 4-nm-thick at 800°C in a vertical furnace system. TiN (0.5 nm)/Al_2O_3 (1.0 nm) nano-laminate with 5 periods were deposited as trapping layer in the PEALD/ALD system and a 20-nm-thick Al_2O_3 was then deposited as blocking layer in the same ALD system followed by a deposition of 150nm thick poly-Si gate in a LPCVD system. The deposition condition of TiN and Al_2O_3 used $TiCl_4$ as precursor at 350°C and $Al(CH_3)_3$ as precursor at 300°C, respectively. Post-deposition annealing was performed at 900°C for 10 seconds in nitrogen ambient to form TiN nano-crystals. Next, the poly-Si gate was heavily doped to p-type by BF_2^+ ion implantation at 40 keV to a dose of $5\text{x}10^{15}$ cm^{-2} and the gate dopant activation was performed by a RTA annealing at 900°C for 20 seconds in nitrogen ambient. An 80-nm-thick TEOS oxide was then deposited on the poly-Si gate as hard mask; the reason has been explained in the previous subsection. During gate patterning, gate patterns were transferred from E-beam photo resist to hard mask by dry etching, stripped the photo resist, and used the hard mask to continue finishing the remaining etching steps. The structure after gate etching is shown in Fig. 2-4(b). Then, spacer with 10-nm-thick SiO_2 and 40-nm-thick Si_3N_4 was formed as shown in Fig. 2-4(c). Next, P_{31}^+ ions were implanted into the S/D region at 20 keV to a dose of $5\text{x}10^{15}$ cm^{-2} and were activated at 900°C for 20 seconds in nitrogen ambient. The gate hard mask and the native oxide on S/D region were removed by dilute HF solution as shown in Fig. 2-4(d). Last, Ni-salicide was formed, the process step has mentioned previously with slightly different conditions. The first step annealing was executed at 300°C for 45 minutes and the second step annealing was executed at 600°C for 30 seconds. Then, the S/D region was converted to fully silicide structure and the gate electrode became Ni-polycide structure, the finished device structure is shown in Fig. 2-4(e).

2-3 Electrical Characterization Techniques

To extract the characteristics of the TFT-SONOS and multi-gate TiN NC non-volatile memories used in this thesis, the measurement conditions are introduced in this section. The static current-voltage (I-V) characteristics of the memory device were measured by a semiconductor parameter analyzer of model Agilent 4156C. Program and erase operations utilized an Agilent 41501A pulse generation expander to generate pulse signals. The definition of threshold voltage (V_t) in this thesis uses constant drain current method, which is commonly applied to non-volatile memories. The threshold voltage was defined as the gate voltage at which the drain current is 0.01 μA for the TFT-SONOS memory and 0.1 μA for the TiN NC memory, both drain voltage is at 1V. In addition, the sweeping range of gate voltage should be chose carefully during I-V measurement to avoid unexpected V_t shift. It is better to measure repeatedly in the same sweeping range to confirm the V_t value is stable, then record the data of memory characteristic.

In order to compare the differences of memory characteristic before and after EUV irradiation in the same device, the memory characteristics should be measured in advance and the V_t value must be adjusted to the initial value before EUV irradiation. Incidentally, the V_t value of every measured device has to be checked again when ready for irradiation experiment. The definitions of memory characteristics and methods to measure these memory devices before EUV irradiation, after EUV irradiation, and recovery after irradiation are described as follows:

(A) Memory window and P/E speed

Fowler-Nordheim (FN) tunneling was used for charge injection, so both the source and drain terminals were grounded during program and erase operations. The memory window is defined as the V_t difference between program state and erase state. To characterize the P/E speed, V_t should be measured immediately after each program or erase operation at different pulse voltages and pulse widths to obtain the correct V_t value. The "V_t shift" is defined as the change of the V_t value after each program or erase operation. It should be noted that the V_t must be adjusted to the original state before applying the next P/E signal. In other words, when measuring the program speed, V_t must be returned to the same erase state after each program pulse, otherwise the program speed will be overestimated.

In order to compare the memory performance before and after EUV irradiation, the characteristics of memory window and P/E speed should be measured on the same memory cell. The sequence of measurements is firstly P/E speed and then memory window because the measurement of memory window uses much stronger pulse conditions than that of P/E speed. This sequence can avoid the operating conditions to affect the properties after irradiation. In addition, for the measurement of memory window, the initial V_t will vary after irradiation. This post-irradiation V_t value must be recorded in advance. After measuring the P/E speed characteristic, V_t should be adjusted to the post-irradiation value as the initial state to continuously measure the memory window characteristic. For measuring the P/E speed after irradiation and its recovery phenomenon, the selected program state for erase speed and erase state for program speed should be adjusted to almost the same value before irradiation.

(B) Retention

Charge retention is a significant reliability issue for the non-volatile memory product. Retention characteristic is defined as the variation in the program state and erase state as a function of storage time at specified storage temperature. There are many ways to express the performance of retention characteristic such as V_t, V_t shift, and charge loss rate. The charge loss rate can be calculated from the variation of memory window with storage time. In addition, when detecting the V_t during storage, a small gate sweeping range should be used to avoid changing the existing memory state. For measuring the retention characteristic after EUV irradiation and its recovery characteristic, the V_t in both program state and erase state should be chose at the same values before irradiation as possible because retention performance is related to the P/E state.

(C) Endurance

Endurance is to evaluate if a memory cell after numbers of P/E cycles that could still have sufficient memory window. The typical standard is 10^5 P/E cycles for the non-volatile memory. A sequential pulse signals with fixed pulse width and rise/fall time were pulsed into memory devices. For measuring the endurance characteristic after irradiation in this thesis, there is one thing differs from previous memory characteristic measurement. Since the endurance test could cause permanent damage to the memory cell, therefore, different memory cells must be used before and after EUV irradiation. Besides, it is essential to select memory cells with similar properties of P/E performance in advance.

2-4 Total Dose Calculation

Radiation dosimetry is an important indicator for the study of radiation damage on any kind of devices since it is in general hard to measure the real energy deposited per unit mass at the location which we concern, that is, in the gate dielectric layer of a MOS device. Radiation dosimetry is defined as the calculation of the absorbed dose in matter resulting from the irradiation to ionizing radiation. The customary unit of dose is the “rad”, and 1 rad = 100 ergs/g. In addition, “Total dose” is generally used to express the total amount of dosage absorbed by the MOS device in radiation literature.

Both BL08A and BL21B beam line at NSRRC are linear EUV sources; therefore the dose absorption rate calculation should be based on the linear source model, which slightly differs from the point source model [17, 49]. The method to derive the total dose is introduced in the following. At first, we define the particle flux, which is given by

$$\Phi_0 = \frac{N(E)}{A} \left(\frac{\text{counts}}{\text{s cm}^2}\right) \tag{2-1}$$

, where N(E) is the number of photons that emitted per unit time by the source as a function of energy E, A is the area of the light source. The radiation beam Φ_0 crossing the material may decay as a function of distance, so the attenuation of the flux $\Phi(x)$ is defined as the following equation:

$$\Phi(x) = \Phi_0\, exp(-\mu x) \tag{2-2}$$

, where μ is the linear attenuation coefficient and it follows the relation

$$\mu = \mu_m \rho \tag{2-3}$$

, where μ_m is the mass attenuation coefficient and ρ is the material density. Utilizing the above three equations, the dose absorption rate D_R of gate dielectric layer in a MOS device can be expressed as

$$D_R = \frac{E \times \Phi_0[1 - exp(-\mu d_{ox})]}{d_{ox}} \times \frac{1}{\rho}$$

$$\approx E \times \Phi_0 \times \mu_m \left(\frac{\mathrm{eV}}{\mathrm{s\ g}}\right), \text{ for } d_{ox} \ll \mu^{-1} \qquad (2\text{-}4)$$

, the approximate condition is because that generally the thickness of gate dielectric layer d_{ox} is much less than the attenuation length μ^{-1}. Besides, since 1 rad = 6.24×10^{13} eV/g, it can substitute Eq. (2-4) into

$$D_R = \frac{E \times \Phi_0 \times \mu_m}{6.24 \times 10^{13}} \left(\frac{\mathrm{rad}}{\mathrm{s}}\right) \qquad (2\text{-}5)$$

, and then use Eq. (2-5) with our experimental conditions to determine the value of dose absorption rate. It is worthy to mention that the expression of dose depends on the material due to μ_m in the equation. The particular material should be referenced in parentheses all the time such as rads(Si), rads(SiO_2), rads(GaAs), etc.. Because dose is similar for different oxide dielectrics and silicon at the same radiation source, the commonly used unit rads(SiO_2) can be utilized in this thesis when irradiating different structure of devices. The value of μ_m can be referred to the NIST [52].

Take the BL08A beam line as an example, E= 91.85eV, N(E)~ 10^{12} photons/s, A~ 0.016cm^2, and μ_m= 3.636×10^4 cm^2/g for silicon dioxide, the dose absorption rate D_R is about 3.345×10^6 rads(SiO_2)/s. Before calculating the total dose, an attenuation factor should be considered since NiSi layer of 40-nm-thick and poly-Si gate of 110-nm-thick are stacked above the gate dielectrics. The intensity of radiation beam decays after penetrating the two layers and approximately 16% of the flux really irradiates on the gate dielectrics according to the calculation. The value of attenuation length can be referred to the CXRO [53]. Thus, the total dose can be determined by the dose absorption rate multiplied by the irradiation time and the attenuation factor. The experimental conditions for EUV irradiation are 10, 20, and 30 minutes, the total doses are probably 321, 642, and 963 Mrads(SiO_2), respectively. For the BL21B beam line, the flux is about 6 $\times 10^{12}$ photons/s according to the experimental result since the flux is not clear at that moment, therefore the total dose are 193, 386, and 579 Mrads(SiO_2) at 1, 2, and 3 minutes irradiation, respectively. Table 2-1 lists the total dose with various EUV irradiation times at BL08A and BL21B beam line.

2-5 Trapped Charge Energy Distribution

In chap 3, the energy distribution of the charge trapping density in the SONOS memory will be discussed. To derive these data, the method based on Frenkel-Poole model to extract the silicon nitride trap density is used [54]. In fact, some measurement methods for the extraction of nitride trap density have been proposed in the past such as estimation by direct tunneling model, the low-frequency (<1 kHz) charge pumping technique, and a reverse model of V_t retention loss by trapped electrons. However, the above methods only can be applied to ultrathin tunneling oxides of memory cell (1.5 - 2.5 nm). Nowadays, as our memory sample, the SONOS-type memory generally utilizes thicker tunneling oxide to achieve better charge retention, an analytical model of Frenkel-Poole emission is available for these cells. The derivation is introduced briefly as follows:

At first, we define the nitride charge detrapping time τ, which is given by

$$\tau = \tau_0 \, exp\left(\frac{\Phi_t - \beta\sqrt{E}}{kT}\right) \qquad (2\text{-}6)$$

, where Φ_t is the corresponding nitride trap energy and E is the electric field, other variables have their usual definitions. The theoretical value of $\beta = 2.77$ ($eVcm^{1/2}V^{-1/2}$) and $\tau_0 = 10^{-13}$s. The electric field E can be obtained by the following equation:

$$E = \frac{V_0 - V_g}{d_{nitride}} \tag{2-7}$$

, where V_0 is the programmed V_t value, V_g is the stressed gate voltage, and $d_{nitride}$ is the equivalent nitride thickness of the ONO layer. Take our TFT-SONOS memory as an example, $d_{nitride}$ = 53.15 nm. According to these extracted parameters, the nitride trap energy Φ_t can be achieved and we rearrange Eq. (2-6) for convenience as follows:

$$\Phi_t = kT\, ln\left(\frac{\tau}{\tau_0}\right) + \beta\sqrt{E} \tag{2-8}$$

, next, the nitride trap density $N(\Phi_t)$ can be expressed as the following equation:

$$\frac{C \cdot dV_t}{q} = A \cdot N(\Phi_t) \cdot d\Phi_t \tag{2-9}$$

, and it can be rearranged as

$$N(\Phi_t) = \frac{C}{A \cdot q} \cdot \frac{dV_t}{d\Phi_t} \tag{2-10}$$

Consequently, by utilizing the Eq. (2-8) and Eq. (2-10), the nitride trap density corresponds to its trapped charge energy can be profiled. Our measurement steps are illustrated in the following. First, the memory cell was stressed with I_g = -500 nA for 1000s, its purpose is to create sufficient traps in the tunneling oxide, therefore the blocking effect can be neglected. Second, the memory cell was programmed with V_g= +14V for 1s by FN injection to store electrons. Third, the detrapping V_g was stressed from V_g = -4V to V_g = -24V with 4V intervals to measure the V_t values at each detrapping time, these measurement results were then substituted into Eq. (2-8) and Eq. (2-10), the energy distribution of the charge trapped density can be obtained.

Table 2-1: Total dose with various EUV irradiation times at BL08A and BL21B beam line.

Beam line	Flux (photons/s)	Total dose (EUV irradiation time)		
BL08A	1×10^{12}	321Mrads (10 min)	642Mrads (20 min)	963Mrads (30 min)
BL21B	6×10^{12}	193Mrads (1 min)	386Mrads (2 min)	579Mrads (3 min)

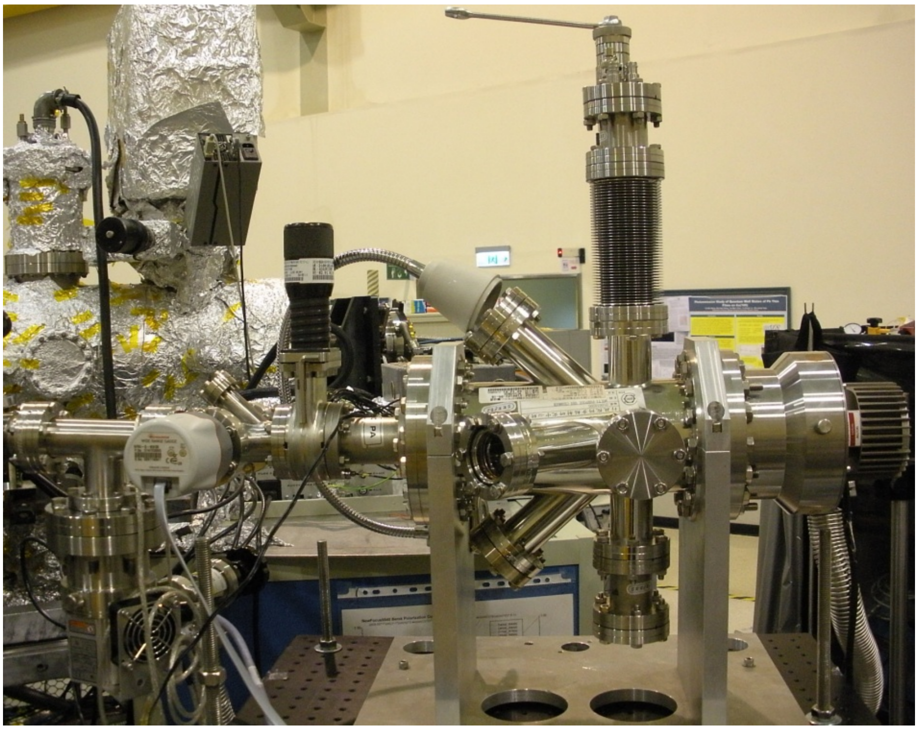


Fig. 2-1: The main chamber for irradiation experiment at NSRRC.

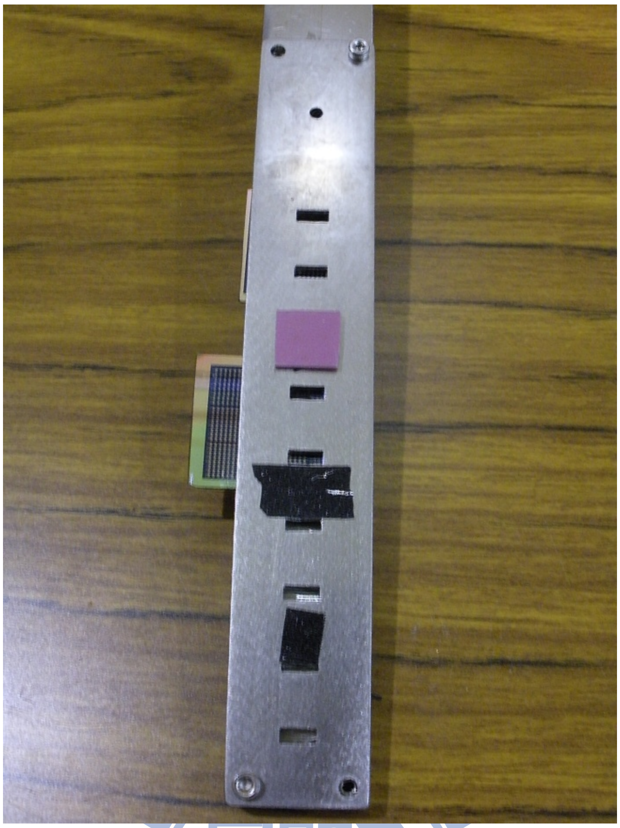
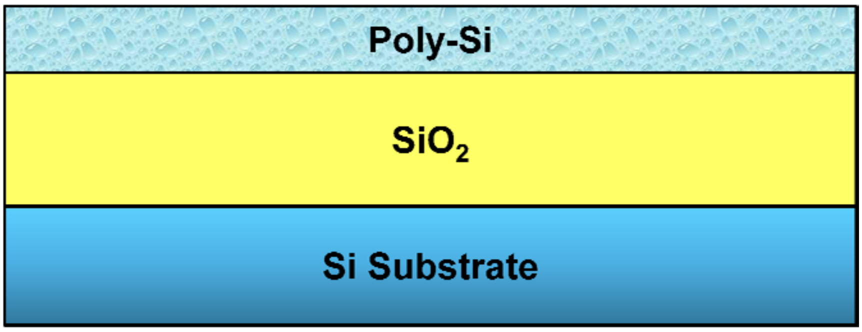
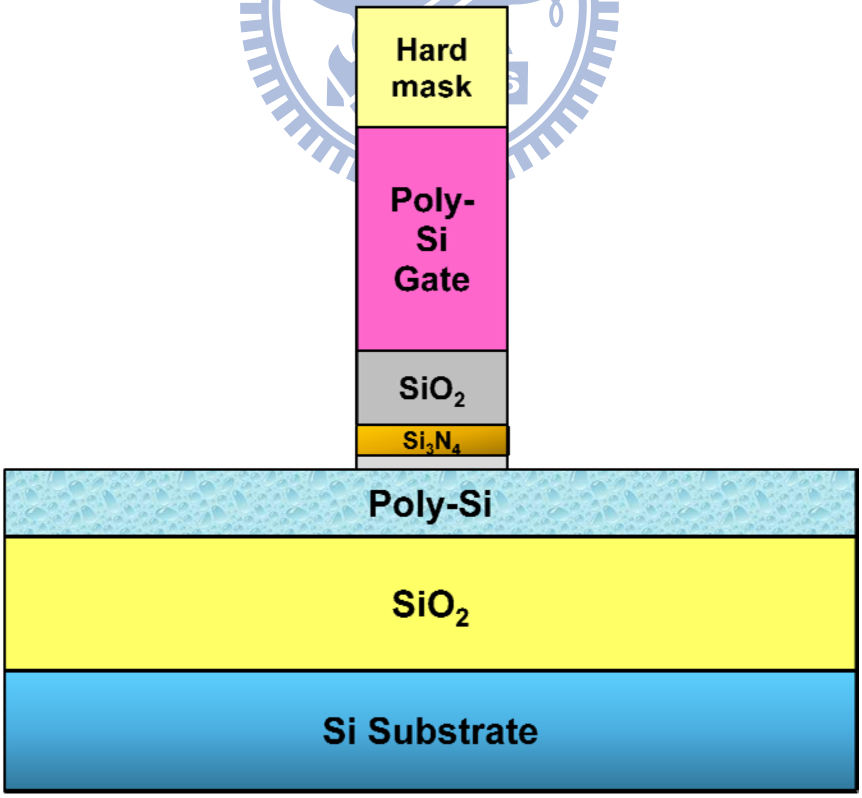


Fig. 2-2: (a) A memory IC chips on the loaded plate which is ready for irradiation.

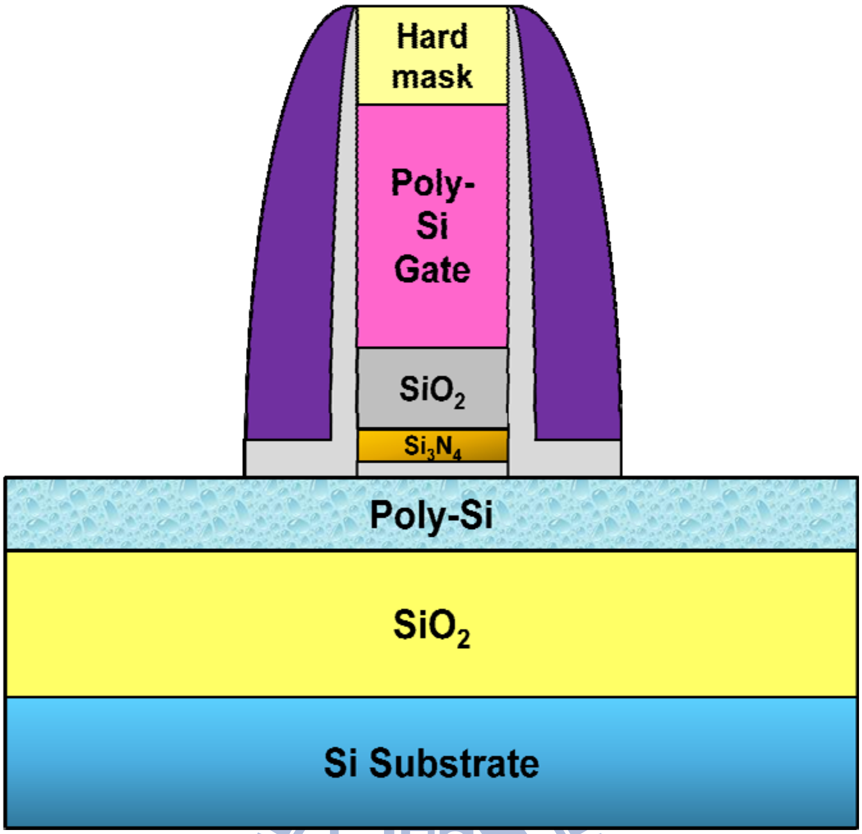
Fig. 2-2: (b) The shape of the light source of the BL08A beam line.


Poly-Si
SiO_2
Si Substrate

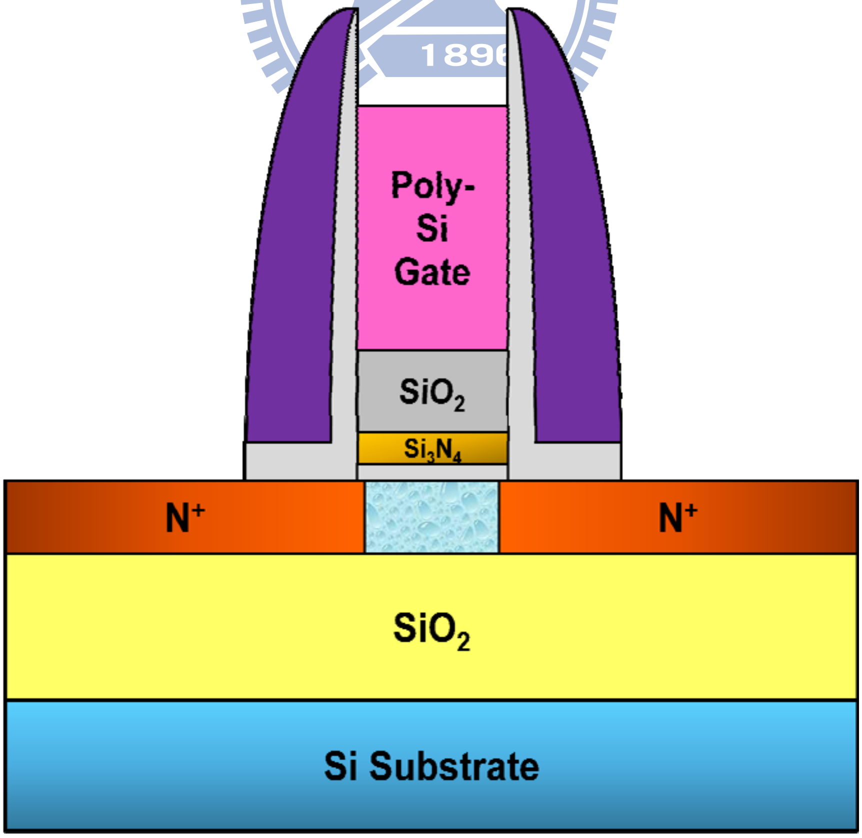
(a)


Hard mask
Poly-Si Gate
SiO_2
Si_3N_4
Poly-Si
SiO_2
Si Substrate

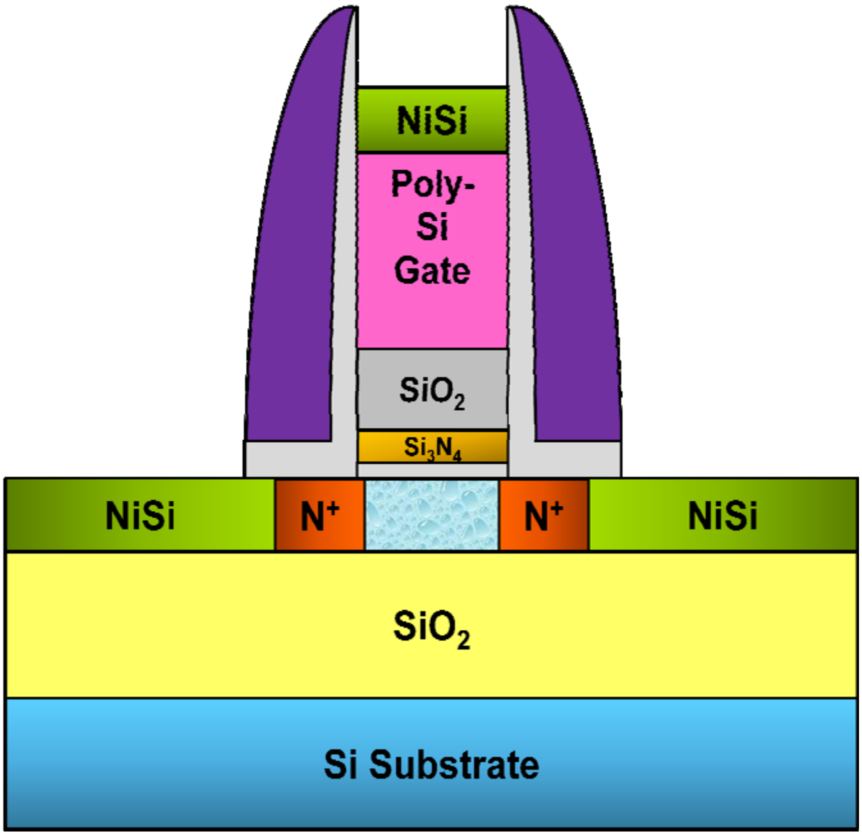
(b)


Hard mask
Poly-Si Gate
SiO_2
Si_3N_4
Poly-Si
SiO_2
Si Substrate

(c)

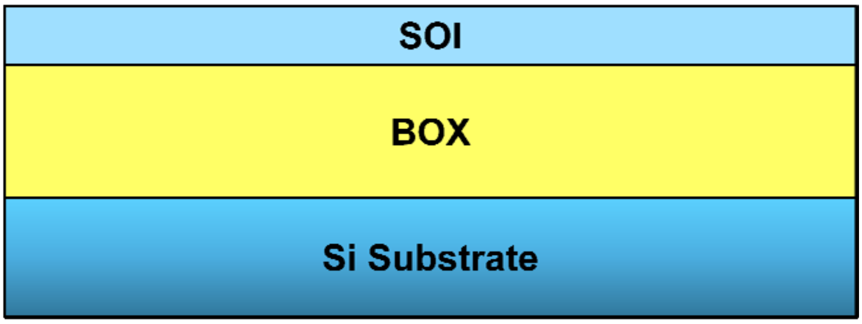

Poly-Si Gate
SiO_2
Si_3N_4
N^+
N^+
SiO_2
Si Substrate

(d)

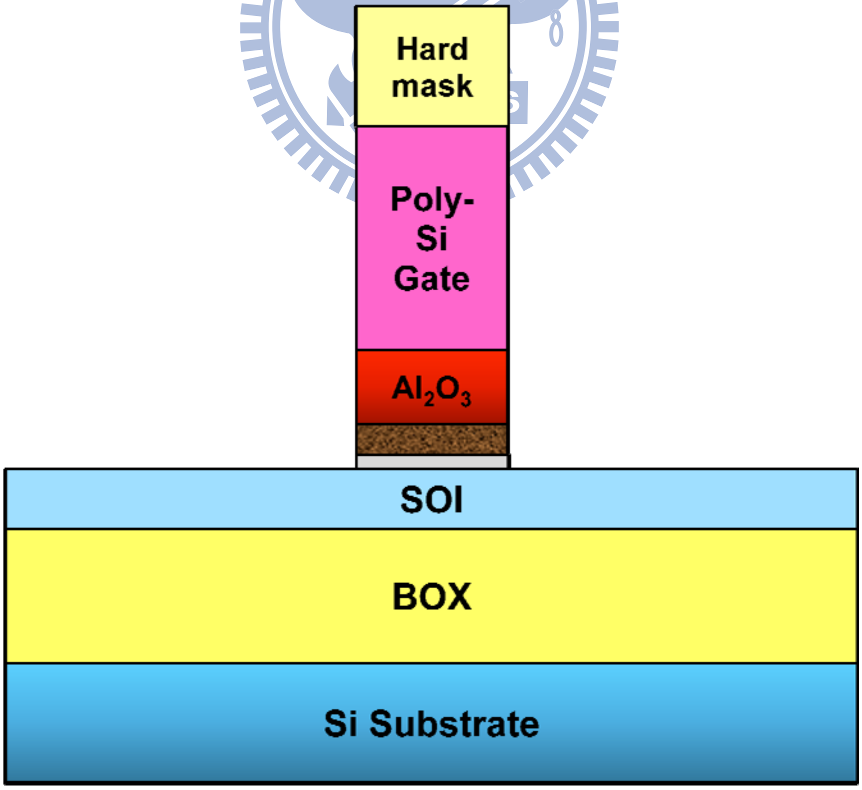


(e)

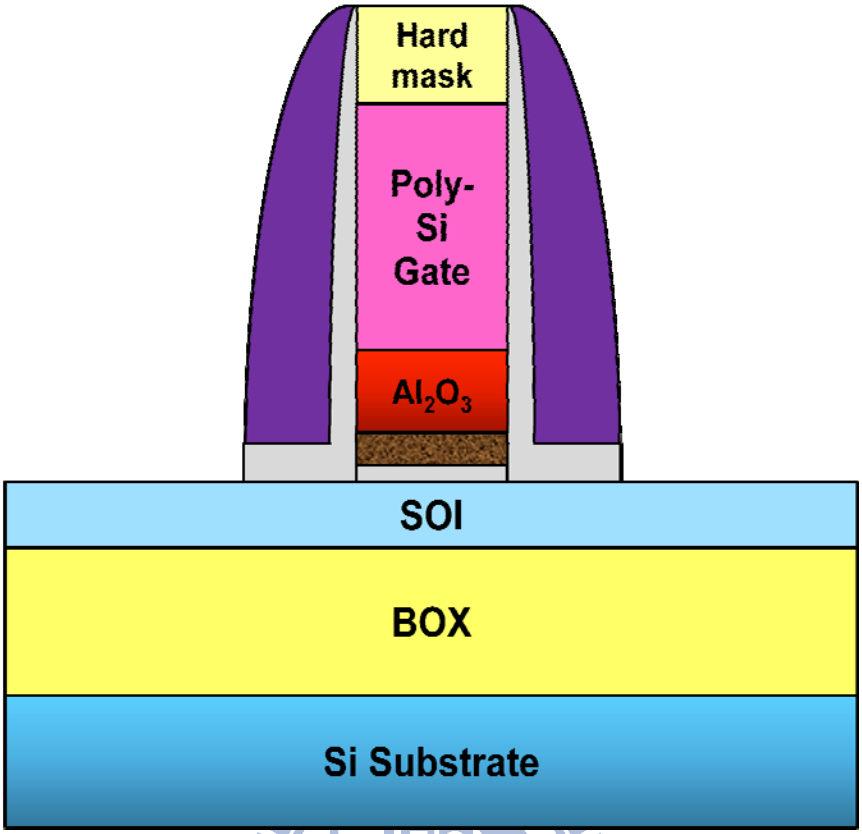
Fig. 2-3: Process flow and cross-sections of the TFT- SONOS non-volatile memory. (a) TFT structure, (b) after dielectric stack deposition and gate patterning, (c) after spacer formation, (d) after S/D ion implantation, S/D activation, and gate hard mask removal, (e) after silicide formation.


SOI
BOX
Si Substrate

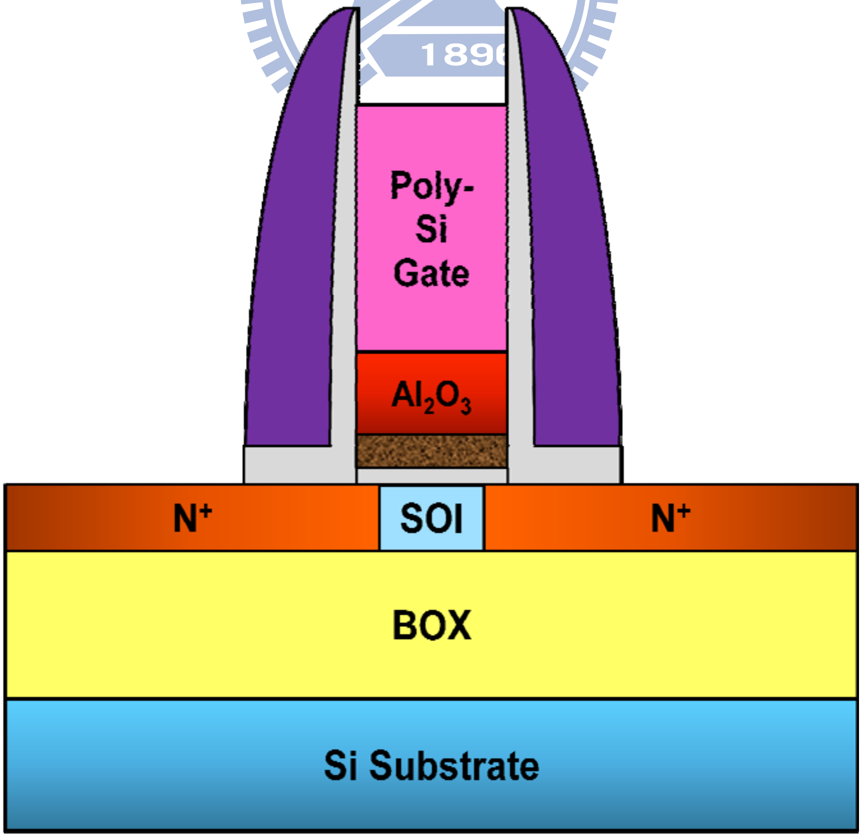
(a)


Hard mask
Poly-Si Gate
Al_2O_3
SOI
BOX
Si Substrate

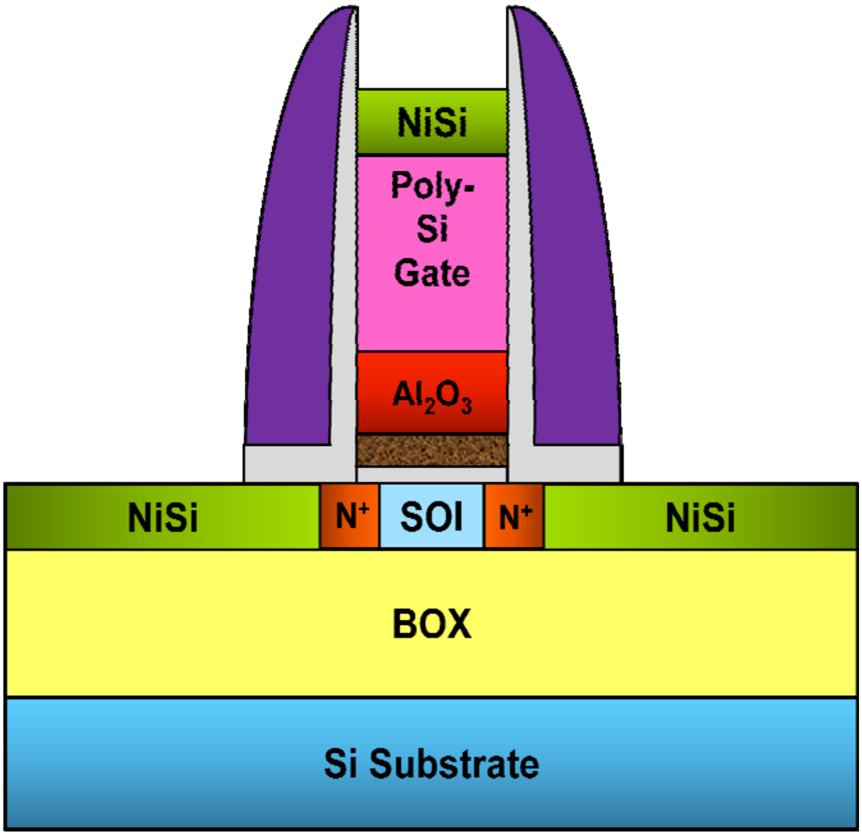
(b)


Hard mask
Poly-Si Gate
Al_2O_3
SOI
BOX
Si Substrate

(c)


Poly-Si Gate
Al_2O_3
N^+
SOI
N^+
BOX
Si Substrate

(d)



(e)

Fig. 2-4: Process flow and cross-sections of the multi-gate TiN nano-crystal non-volatile memory. (a) SOI material, (b) after dielectric stack deposition and gate patterning, (c) after spacer formation, (d) after S/D ion implantation, S/D activation, and gate hard mask removal, (e) after silicide formation.

Chapter 3

Extreme Ultra-violet Radiation on Non-volatile Memory Characteristics

3-1 Introduction

In this chapter, we discuss the memory characteristics of the TFT-SONOS and multi-gate TiN NC non-volatile memory devices before and after EUV irradiation. Basic memory characteristics including memory window, program/erase (P/E) speed, charge retention, and endurance of the memory devices are evaluated carefully. The effect of post-irradiation annealing at high temperature on endurance characteristic is also discussed. In addition, the energy distribution of the trap density in the Si_3N_4 charge trapping layer (CTL) of the TFT-SONOS memory before and after EUV irradiation is extracted. The device dimensions for different irradiation times are the same for the sake of easy comparison.

3-2 TFT-SONOS Non-volatile Memory

3-2-1 Basic Electrical Characteristic

Fig. 3-1 shows the I_d-V_g curves of the TFT-SONOS memory before EUV irradiation and experienced 1 min EUV irradiation. Since the memory characteristics of every memory cell should be measured before EUV irradiation, they must be tuned to the initial states and be checked again when ready for irradiation, as shown in Fig. 3-1. After 1 min EUV irradiation to a dose of 35 Mrads(SiO_2), the I_d-V_g curve exhibits a small negative threshold voltage (V_t) shift of 0.035 V. The V_t is defined as the gate voltage at which the drain current is 0.01 μA. This phenomenon indicates a small amount of the net positive charges generated in dielectrics caused by EUV irradiation. Although EUV irradiation generates electron-hole pairs, electrons are more mobile than holes in dielectrics and then more holes would be trapped in dielectrics and contribute to net positive charges. This process has been illustrated in section 1-2.

More apparent V_t shifts toward negative voltage direction are observed on the 2 min and 3 min EUV irradiated TFT-SONOS memories as shown in Fig. 3-2 and Fig. 3-3, respectively. The values of V_t shift are 0.438V for 2 min irradiation and 0.55V for 3 min irradiation, which can be understood by a relatively large amount of radiation induced electron-hole pairs. The longer irradiation time, the more electron-hole pairs are generated, so the V_t shift is dose-dependent. In addition, compared with other radiation studies [27, 30], our memory devices exhibit relatively smaller V_t shift at an even higher total dose. Nevertheless, the radiation source and memory-type are different.

3-2-2 Memory Window

In order to identify the difference in the memory window characteristic before and after EUV irradiation, the basic characteristic of memory window of the fresh TFT-SONOS memory should be examined firstly to avoid mistaking some phenomena as the cause of EUV irradiation. Fig. 3-4 shows the program and erase windows of the TFT-SONOS memory experienced three times memory window measurements with pulse width of 1 s. The initial V_t is at $V_g = 0V$ and FN tunneling is used for both program and erase operations. The P/E voltage pulses from $V_g = \pm 8$ V to $V_g = \pm 18$ V with a 2 V interval. It is clear that the values of V_t in the program state in the range of V_g = 10V to V_g = 18V after P/E operations increase obviously with respect to the 1st operation. This phenomenon can be explained by the imperfect bonding in the Si_3N_4 CTL. The memory effect on SONOS is due to the charge trapping by the defects induced traps in the CTL. The residual hydrogen in the Si_3N_4 CTL may passivate some defects and then reduce the trap density. During P/E operations, the applied high voltages may break the hydrogen bonds and/or break the other bonds in the Si_3N_4 CTL and generate defects or traps as new charge storage sites, causing the increase of V_t shift in the program state. The third P/E operations exhibits even lager memory window but the generated trapping sites are gradually saturated and relatively stable. Fig. 3-5 compares the energy distribution of the trap density in the CTL after the 1st and 3rd times P/E operation. It is obvious that the trap density after three times P/E operations is much higher than that only performed one P/E operation, which proves that more defects or traps are generated during high-voltage P/E operations. The trap density is about $1x10^{11}$ - $2x10^{11}$ $eV^{-1}cm^{-2}$ after one P/E operation and about $5x10^{11}$ - $8x10^{11}$ $eV^{-1}cm^{-2}$ after three times P/E operation. Thus, to record the memory window characteristic before EUV irradiation, memory devices must receive P/E operations for at least three times in advance.

Fig. 3-6 shows the P/E windows of the TFT-SONOS memory before EUV irradiation, experienced 1 min EUV irradiation, and 264 hrs after EUV irradiation. Some important phenomena are observed in Fig. 3-6. First, a slightly reduction of the initial V_t at V_g = 0V after EUV irradiation indicates that a small amount of the net positive charges are generated, which has been explained in section 3-2-1. Second, the V_t values in the program state at higher program voltage (14V ~ 18V) increase slightly, which implies a few new traps were generated during EUV irradiation. It is postulated that EUV has sufficient energy to break bonds in the dielectrics, causing some traps produced in the Si_3N_4 CTL. Third, the V_t values in the erase state show an hump around $V_g = \pm10$ V, which indicates the electron injection into the CTL is more easier than electron escape from traps. As the P/E voltage increases to $V_g = \pm18$ V, the V_t in the erase state after EUV irradiation is higher than that before EUV irradiation. This phenomenon is suspected to be due to the EUV induced damages in the blocking layer. For the SiO_2 tunneling layer, the hole injection barrier is higher than the electron injection barrier, therefore, holes are relatively hard to tunnel through the SiO_2 during erase operation. Meanwhile, electrons may tunnel through the blocking layer to the CTL. Thus, the damaged blocking layer results in electrons injection from the top gate much easier than holes injection from substrate during erase operation.

The P/E characteristic after 264 hrs room temperature storage after EUV irradiation is also shown in Fig. 3-6. It is observed that the memory device can be programmed to even higher V_t value with respect to that immediately after EUV irradiation. The reason is not clear yet but we suspect it may be due to the deviation in the measurement process since not all irradiated memory cells exhibit the same phenomenon. The V_t can be erased to lower level at high erase voltage (-18V), this improvement indicates that EUV radiation induced defects in the blocking layer can be repaired with time.

Similar but more pronounced phenomena such as net positive charge generation by EUV irradiation, higher V_t values in the program state, and erase saturation at high erase voltage are observed on the 2 min and 3 min EUV irradiated TFT-SONOS memories as shown in Fig. 3-7 and Fig. 3-8, respectively. An apparent reduction of the initial V_t at $V_g = 0$V implies that more positive charges are generated with respect to 1 min EUV irradiation since e-h pair generation is a dose-dependent process. The increase of program state V_t at higher program voltage (14V ~ 18V) shown in Fig. 3-7 indicates even more trapping sites are generated. Moreover, the increase of V_t in both program and erase states is observed in Fig. 3-8. It is suspected that the 3 min EUV irradiation generates relatively deep-level traps and severely damaged blocking layer and results in hard-to-erase so that all the erase state V_t values increase. The phenomenon of erase saturation is more pronounced in Fig. 3-7 and Fig. 3-8 than in Fig.3-6, which indicates that more defects are generated in the blocking layer during the longer EUV irradiation time.

The recover characteristics of memory window shown in Fig. 3-7 and Fig. 3-8 are slightly different from that shown in Fig. 3-6. The V_t values in both program and erase states after long term room temperature storage recover to the pre-irradiation values, which implies the EUV irradiation generated traps in the Si_3N_4 CTL are self-annealed with time.

In order to confirm our explanations on the observed phenomena, the energy distributions of the trap density in the CTL before and after EUV irradiation, and after long-term storage after EUV irradiation are extracted. The results are shown in Fig. 3-9. It is clear that the trap density after EUV irradiation increases approximately to $7x10^{11}$ - $1x10^{12}$ $eV^{-1}cm^{-2}$, which is higher than that before EUV irradiation. This result proves that new traps are indeed generated during EUV irradiation. After long-term storage, the trap density gradually recovers to the pre-irradiation value, which supports that the EUV irradiation produced traps can be self-annealed with time at room temperature.

3-2-3 P/E Speed

The program speed and erase speed of the TFT-SONOS memory are shown in Fig. 3-10 and Fig. 3-11, respectively. The gate pulse is +14V for program speed measurement and -18V for erase speed measurement. As expected, the program and erase speeds increase obviously with the increase of the magnitude of gate voltage. The programmed V_t shift is larger than the erased V_t shift. That is why we chose higher gate voltage for erase operation. A slightly increase of the V_t shift in both program state and erase state at the 2nd and 3rd times measurement is observed in Fig. 3-10 and Fig. 3-11, respectively. This phenomenon is consistent with that observed in Fig.3-4 and is explained by the imperfect bonding in the Si_3N_4 CTL. The difference between the 2nd and the 1st times measurement is more apparent for the 1s pulse width. The P/E conditions with 1s pulse width are identical to those used in memory window characterization at V_g = 14V for program and V_g = -18V for erase in Fig. 3-4. It should be noted that new traps would be generated by high voltage and long pulse width P/E operations. After the 1st time P/E speed measurement, new traps are generated so that the V_t shifts at the 2nd time P/E speed measurement increases. After 2-3 times high voltage and long pulse width P/E operation, the trap density becomes stable.

Fig. 3-12 and Fig. 3-13 show the program speed and erase speed, respectively, of the TFT-SONOS memory before EUV irradiation, after 1 min EUV irradiation, and after 264 hrs room-temperature storage after EUV irradiation. The program speed increases after 1 min EUV irradiation, which implies that the EUV irradiation generates new traps in the Si_3N_4 CTL. Instead, the erase speed decreases slightly in the range of 1μs to 10ms and more seriously in the range of 0.1s ~ 1s, which indicates that the EUV irradiation degrades the blocking layer and causes electron backside injection, especially at long pulse width. Both phenomena are consistent with those observed in the memory window characterization on the device after 1 min EUV irradiation as shown in Fig. 3-6. After 264 hrs room-temperature storage, both program speed and erase speed recover. The recovery of erase speed at 1s pulse width implies that the EUV irradiation generated defects in the blocking layer can repair with time so that the effect of electron backside injection decreases. This phenomenon can also be seen in Fig. 3-6.

The program and erase speeds of the TFT-SONOS memories after 2 min EUV irradiation are shown in Fig. 3-14 and Fig. 3-15, respectively. It is clear that a 2 min EUV irradiation increases the program speed, which is similar to that observed in Fig. 3-12. The erase speed changes slightly as the erase pulse width is shorter than 0.1s. Obvious erase saturation occurs at 1 sec pulse width. After 240 hrs room temperature storage, the program speed completely recovers to the pre-irradiation characteristic. However, the erase saturation at 1 sec erase pulse width does not recover. These phenomena imply that the irradiation produced traps in the Si_3N_4 CTL recover with time but the defects in the blocking layer do not.

More pronounced but similar phenomena of the program and erase speeds are observed on the 3 min EUV irradiated TFT-SONOS memories as shown in Fig. 3-16 and Fig. 3-17, respectively. The overall program speed increases greatly which implied that more traps are generated during the 3 min EUV irradiation. This result is consistent with that shown in Fig. 3-12. The erase speed decreases obviously at short pulse width but slightly decreases at high pulse width. After 257-hrs room temperature storage, similarly, the program speed gradually recovered to the pre-irradiation characteristic. The erase speed at short pulse width increases apparently but decreases severely at long pulse width. This unique phenomenon is different from the other memory cell and need to be examined in the future work.

3-2-4 Retention Performance

To study the EUV irradiation effects on the retention characteristic of the TFT-SONOS memory, appropriate V_t values in the program and erase states are pre-selected before EUV irradiation.

Fig. 3-18 shows the retention characteristic of the TFT-SONOS memory before and after 1 min EUV irradiation, and after 240 hrs room temperature storage after EUV irradiation. It is clear that the retention characteristic does not degrade immediately after EUV irradiation. However, after 240 hrs room temperature storage, the V_t in the program state slightly decreases which implies some degradation occurs in the EUV irradiated memory cell. It is suspected that additional defects are generated in the tunneling layer during long term storage and cause the increase of charge loss rate. These defects may be generated by the gradually recombination of the trapped holes with electrons. The retention characteristic in the erase state does not show apparent change which is relatively invariant.

Similar phenomena can be observed on the 2 min and 3 min EUV irradiated TFT-SONOS memories as shown in Fig. 3-19 and Fig. 3-20, respectively. In Fig. 3-19, the retention characteristic does not change in the program state but slightly degrades in the erase state. After 207 hrs room temperature storage, memory window narrows down due to the generation of additional defects, which is consistent with that observed in Fig. 3-18. As for the 3 min irradiated memory cell, the retention characteristic degrades immediately after EUV irradiation, especially in the program state. These results indicate that as the EUV irradiation time is short, the tunneling layer would not be damaged severely. However, EUV irradiation damages the tunneling oxide more greatly as the EUV irradiation time is longer. The above inference is on the basis of the charge loss mechanism of SONOS memory, which mainly results from electron tunneling back to channel through the tunneling layer. After long-term room temperature storage, the retention characteristic in the program state becomes even worse.

3-2-5 Endurance Performance

Measuring the endurance characteristic can learn some important information on the reliability of memory devices such as charge trapping uniformity and gate dielectrics quality. For the former, charge non-uniform distribution generally occurs in one side injection case, for example, only drain-side or source-side injection. Therefore, it is not a main issue in this thesis since FN tunneling is used for both program and erase operation. For the latter, memory device degrades during numerous of P/E cycles due to the deterioration of the tunneling oxide. Thus, endurance characteristic is prone to observe whether the EUV radiation damages the oxide quality or not.

Fig. 3-21 shows the endurance characteristic of the TFT-SONOS memory before EUV irradiation. The pulse condition is $V_g = +17$ V for program and $V_g = -20$ V for erase, both pulse widths are 10 msec. It is noted that all the memory cells in this part use the same pulse condition. Fig. 3-21 shows the memory windows of the device before EUV irradiation up to 10^5 P/E cycles. The 56% degradation of memory window means the endurance performance of our memory devices is not good enough. In order to clarify what mechanism resulting in degradation, the I_d-V_g curves before and after endurance test are shown in Fig. 3-22. In the 1st P/E cycle, the subthreshold swing (SS) in the program state is poorer than that in the erase state. Since the program operation is performed in advance of erase operation, the better SS in erase state indicates that the SS degradation in the program state is not due to increase of the interface state. This phenomenon can be attributed to the surface roughness of the poly-Si channel. The rough interface between poly-Si channel and tunneling oxide will cause non-uniform electric field for FN tunneling and leads to SS degradation because of non-uniformly stored charges. After 10^5 P/E cycles, the SS in both program and erase states degrades furthermore. Since the SS in program state is very close to that in erase state, the degradation mechanism is also attributed to the non-uniform charge storage. The narrowing of the memory window after repeated P/E operations may result from the degradation of the blocking layer so that back side injection from control gate occurs in both P/E operations.

After EUV irradiation, much worse endurance characteristic is observed on the 1 min EUV irradiated TFT-SONOS memory, especially in the erase state, as shown in Fig. 3-23. The V_t value of erase state increases after 10^5 P/E cycles, which is mainly attributed to the damaged blocking layer. As mentioned in the previous discussion, defects are generated in the blocking layer by EUV radiation and it will accelerate the degradation of blocking layer after numerous high-voltage P/E operations. Thus, electron backside injection enhanced and results in a large increase of the V_t in the erase state. The memory window shows 83% degradation which is relatively worse than the non-irradiated memory cell. In addition, we can also verify our explanation from the I_d-V_g curves which is shown in Fig. 3-24. Despite the memory window shrinks due to the SS degradation, an apparent V_t shift of erase state implied the enhanced electron backside injection due to EUV damaged blocking layer.

Similar but more pronounced phenomena can be also found on the memory cells experienced 2 min and 3 min EUV irradiation as shown in Fig.3-25 and Fig.3-26, respectively. The memory window shows 87% degradation in Fig. 3-25 and 90% degradation in Fig. 3-26 after 10^5 P/E cycles. The V_t value in the erase state after 10^4 P/E cycles increases obviously in Fig. 3-26, which implies longer EUV irradiation time generated more defects and causes even worse endurance characteristic. The I_d-V_g curves of the endurance characteristic after 2 min and 3 min EUV irradiation are shown in Fig. 3-27 and Fig. 3-28, respectively. Strong electron backside injection can be observed in the erase state due to longer irradiation time.

From the above experimental results, it is clearly that the SONOS memory cell would be damaged by EUV irradiation. If the damaged memory cells can be recovered through the typical thermal budget in the back-end-of-line process, then it is not necessary to worry about the EUV irradiation induced damages. Otherwise, careful process design and/or additional thermal budget must be employed. The process temperature in the back-end-of-line process is generally lower than 500°C. Fig.3-29 and Fig.3-30 shows the endurance characteristic of the 30 min EUV irradiated TFT-SONOS memory before and after 600°C post-irradiation annealing, respectively. After 30 min EUV irradiation, the memory window shows 93% degradation and the erase state degrades severely. The 600°C post-irradiation annealing can improve the endurance characteristic partially, however, the memory window still shows a 63% degradation. It is concluded that the endurance degradation cannot be recovered by a 600°C annealing.

Finally, the retention characteristic of memory cells which have been experienced endurance test is discussed. Fig. 3-31 shows the retention characteristic of the TFT-SONOS memory after endurance test. It is clear that the V_t values in the erase state cannot be as low as that before endurance test since the blocking layer has been degraded after numerous of P/E operations and then results in strong electron backside injection. The V_t values in the program state is higher than that after endurance test since the lower pulse voltage and longer pulse width are used to increase the V_t value so that the larger memory window is obtained. In addition, the retention performance in the erase state is worse than that of the device before endurance test and it shows a monotonic increase of V_t during the storage period. We try to explain this special phenomenon by the trapping of the backside injected electrons in the blocking layer. During the erase operation, the strong electron backside injection occurs and some electrons are trapped in the blocking layer, meanwhile, holes from channel are injected into the CTL. Thus, the trapped hole may tunnel through the thin tunneling layer during storage. However, it is relatively harder for the trapped electron in the blocking layer to escape because the blocking layer is rather thick. In this case, the V_t values in the erase state increases with the storage time instead of decreasing. In addition, the retention performance in the program state is also worse than that of the device before endurance test, which indicates the tunneling layer is degraded after numerous of P/E operations. This can also support the detrapping of holes in the erase state. This memory cell exhibits about 50% window loss after 10^5 seconds.

In addition, the retention characteristics of the TFT-SONOS memory after endurance test with different EUV irradiation time are shown in Fig. 3-32 to Fig. 3-34. The retention performances are even worse after EUV irradiation. Almost all the irradiated memory cells exhibit more than 60% window loss after 10^5 seconds. It can be observed that the retention performance in the program state is worse than that of the device before endurance test as shown in Fig. 3-31, which supports that the tunneling layer is damaged by the EUV irradiation again.

3-3 TiN NC Non-volatile Memory

3-3-1 Basic Electrical Characteristic

Fig. 3-35 shows the I_d-V_g curves of the multi-gate TiN NC memory before EUV irradiation and experienced 2 min EUV irradiation to a dose of 70 Mrads(SiO_2). It exhibits a negative V_t shift of 0.257V and slightly SS degradation due to irradiation generated net positive charges and interface states, respectively. The V_t is defined as the gate voltage at which the drain current is 0.1 μA. More apparent V_t shift and SS degradation are observed on the 30 min EUV irradiated multi-gate TiN NC memory to a dose of 963 Mrads(SiO_2), as shown in Fig. 3-36. The magnitude of the V_t shift is 0.457V. In addition, it is found that the V_t shift of the NC memory is slightly less than that of the SONOS memory at the same dose, which implies the NC memory is not prone to net positive charges generation with respect to the TFT-SONOS memory.

3-3-2 Memory Window

Before measuring the P/E window of the irradiated multi-gate TiN NC memory, the basic characteristic of P/E window before EUV irradiation is examined, as shown in Fig. 3-37. FN tunneling is used for both program and erase operations and the P/E voltage pulses from $V_g = \pm 2$ V to $V_g = \pm 12$ V with a 2 V interval. It is clear that in the first three times P/E operations, the memory window characteristic is stable with respect to that of the TFT-SONOS memory cell. Therefore, it is not necessary to perform several times P/E operations before recording the memory characteristics. Fig. 3-38 and Fig. 3-39 show the P/E windows of the multi-gate TiN NC memory experienced 2 min and 30 min EUV irradiation, respectively. It is apparent that the P/E window characteristic are not degraded by the EUV irradiation and exhibits better radiation tolerance for the multi-gate TiN NC memory. In addition, the V_t values in both program and erase states on the 30 min irradiated memory cell increase slightly, the reason for this phenomena have not been clear yet.

3-3-3 P/E Speed

The program and erase speeds of the multi-gate TiN NC memory are examined as shown in Fig. 3-40 and Fig. 3-41, respectively. The gate voltage is +12 V for program speed measurement and -12 V for erase speed measurement. Both program and erase speeds are invariant after three times operations, which imply a good stability to the multi-gate TiN NC memory sample. Fig. 3-42 and Fig. 3-43 show the program and erase speeds, respectively, of the multi-gate TiN NC memory which experienced 2 min EUV irradiation. It is observed that the P/E speed is also stable after EUV irradiation and after long term room temperature storage. Even on the 30 min irradiated memory cell, the program and erase speeds are not affected by the

EUV irradiation, as shown in Fig. 3-44 and Fig. 3-45, respectively.

From the above experimental results, it is found that, unlike the TFT-SONOS memory, the EUV irradiation almost does not affect the P/E window and P/E speed of the multi-gate TiN NC memory. These phenomena can be explained by the difference in charge storage mechanisms between SONOS memory and NC memory. Detailed discussion will be illustrated in Chap 4.

3-3-4 Retention Performance

Fig. 3-46 and Fig. 3-47 show the retention characteristic of the 2 min and 30 min EUV irradiated multi-gate TiN NC memory, respectively. The poor retention characteristic is observed in both memory cells, the V_t values in the erase state only increases slightly because the selected erase state is close to the initial V_t so that only a small amount of holes are trapped in the NCs and escaped from trapping layer with retention time. Nevertheless, the retention characteristics after EUV irradiation are not degraded and still stable during long term storage after irradiation.

3-3-5 Endurance Performance

Fig. 3-48 shows the endurance characteristic of the multi-gate TiN NC memory before EUV irradiation. The pulse condition is V_g = +12V for program and V_g = -9V for erase, both pulse widths are 10 msec. The V_t values in both program and erase states increase obviously after 10^5 P/E cycles, which indicates that every P/E cycle leaves some electrons in the NCs. Fig. 3-49 and Fig. 3-50 show the endurance characteristics of the multi-gate TiN NC memory experienced 2 min and 30 min EUV irradiation, respectively. It is observed that both endurance characteristics are not affected by the EUV irradiation apparently. These robust endurance characteristics may be attributed to the low P/E operation voltage. Because Al_2O_3 has higher dielectric constant, its good gate coupling can reduce the operation voltage so that the electric field in the Al_2O_3 blocking layer of NC memory is lower than that in the SiO_2 blocking layer of the SONOS memory. Therefore, more robust endurance of the NC memory is observed with respect to the SONOS memory. In addition, the retention characteristics of the multi-gate TiN NC memory cells which have been performed endurance test are shown in Fig. 3-51 to Fig. 3-53. These memory cells exhibits much worse retention performance, especially in program state, which implies that the tunneling oxide is degraded after endurance test and EUV irradiation induced damage is not apparent according to the result of retention characteristics.

3-4 Summary

The effect of EUV irradiation induced damages on the characteristics of TFT-SONOS memories and multi-gate TiN NC memories are investigated.

On the TFT-SONOS memory, a slightly reduction of the V_t after EUV irradiation indicates a small amount of the net positive charges is generated. For the memory window, the V_t values in the program state increase, which implies a few new traps were produced during the EUV irradiation. After long-term storage, the V_t value can recover to the pre-irradiation value, which indicates that radiation produced traps can be self-annealed with time. In addition, the energy distribution of the trap density is extracted and its results can support our explanations on the observed phenomena. Erase saturation is observed at high erasing voltage because electron backside injection occurs due to the radiation damaged blocking layer. This phenomenon can be slightly recovered after long term storage.

For the P/E speed, the program speed increases but the erase speed decreases after EUV irradiation. These phenomena can also be recovered after long-term storage. The retention performance is reserved at short irradiation time but the program state degrades slightly at long irradiation time due to the damaged tunneling oxide. After long term storage, the retention performance is slightly degraded due to the generation of additional defects in the tunneling layer.

After EUV irradiation, the endurance performance degrades more severely, especially in the erase state, which implied the blocking layer is also damaged by the EUV irradiation. This degradation cannot be recovered after 600°C annealing. The retention performance after endurance test is degraded because of damaged tunneling layer. More severely degradation in tunneling layer is observed after EUV irradiation.

On the multi-gate TiN NC memory, similarly, net positive charges are generated after EUV irradiation but the amount is less than that on the TFT-SONOS memory. Moreover, almost all the memory performances are not affected by the EUV irradiation. The NC memory exhibits much better EUV radiation tolerance than the SONOS memory due to the difference in the charge trapping mechanisms.

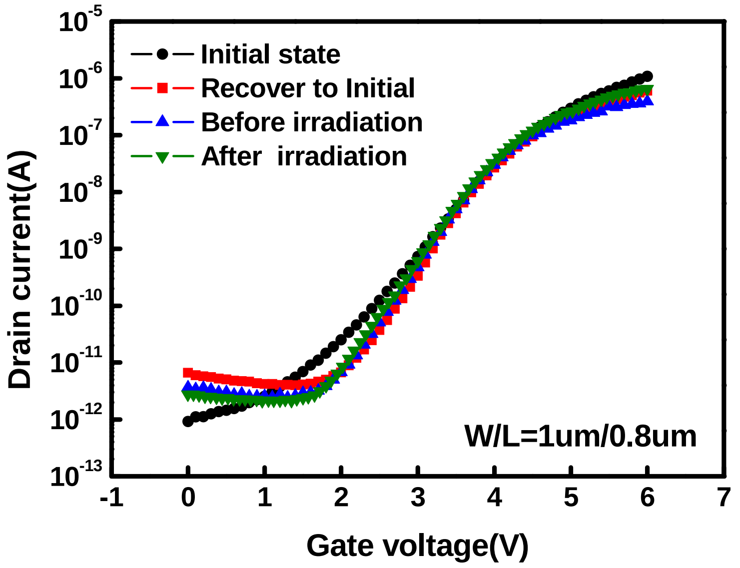


Fig. 3-1: The I_d-V_g curves of the TFT-SONOS memory before EUV irradiation and experienced 1 min EUV irradiation.

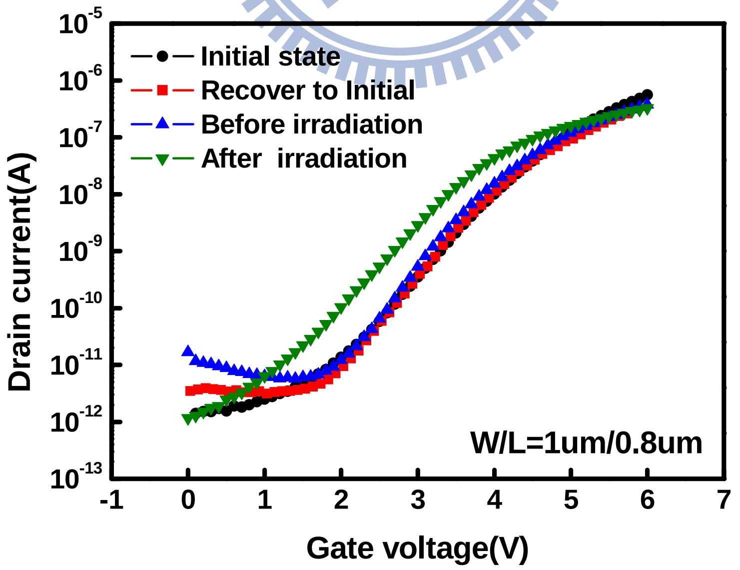


Fig. 3-2: The I_d-V_g curves of the TFT-SONOS memory before EUV irradiation and experienced 2 min EUV irradiation.

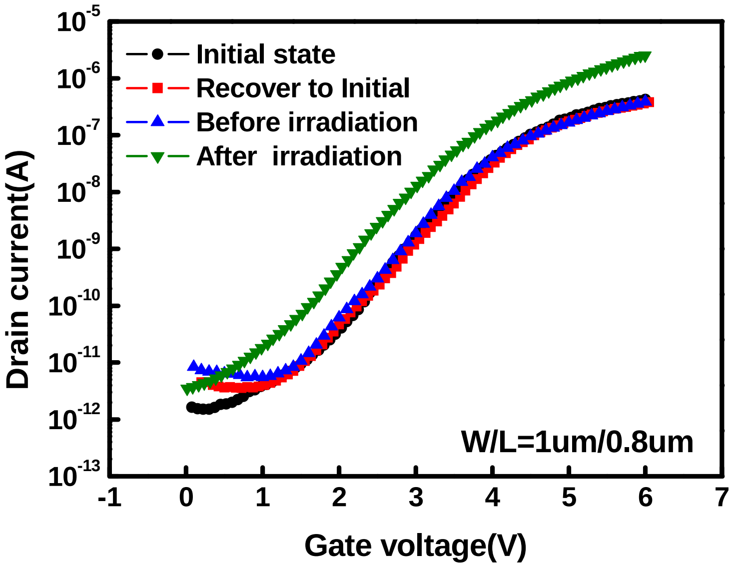


Fig. 3-3: The I_d-V_g curves of the TFT-SONOS memory before EUV irradiation and experienced 3 min EUV irradiation.

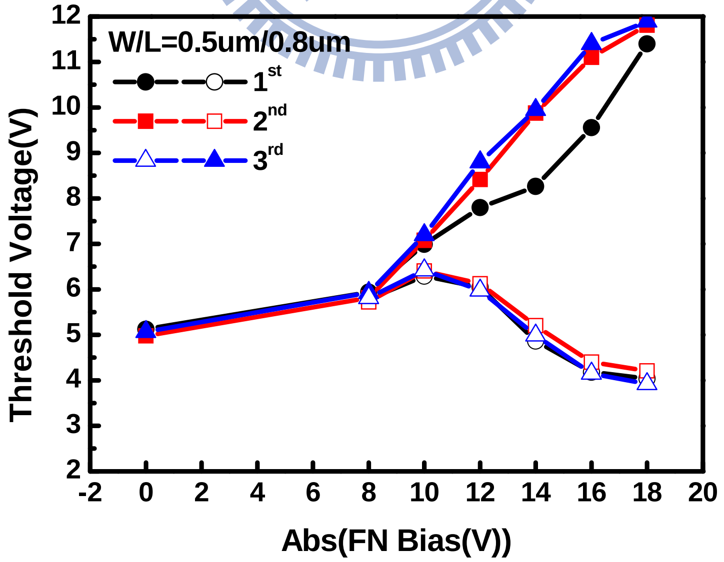


Fig. 3-4: Program and erase windows of the TFT-SONOS memory experienced three times P/E operations with pulse width of 1 s.

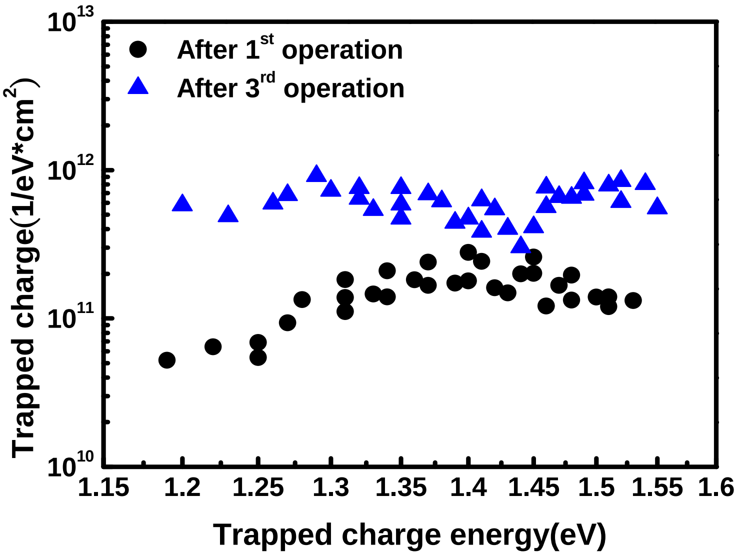


Fig. 3-5: The energy distribution of the charge trapping density in the CTL of the TFT-SONOS memory after 1st and 3rd time P/E operation.

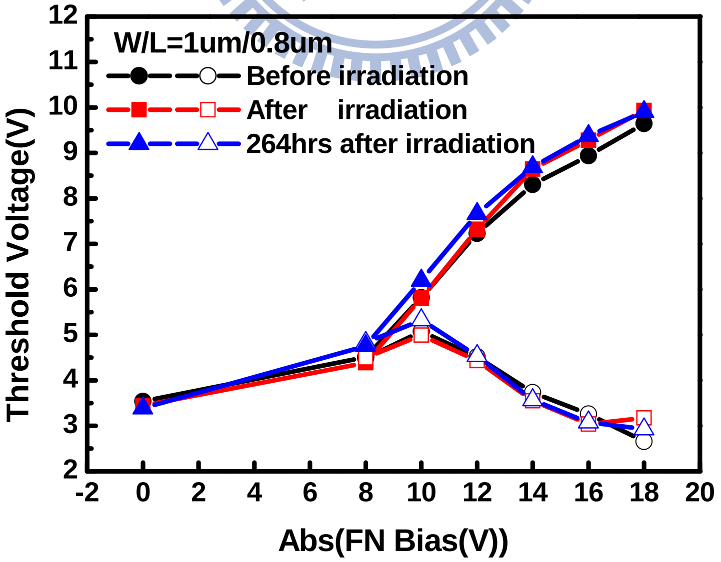


Fig. 3-6: Program and erase windows of the TFT-SONOS memory. The pulse width is 1 s and the EUV irradiation time is 1 min.

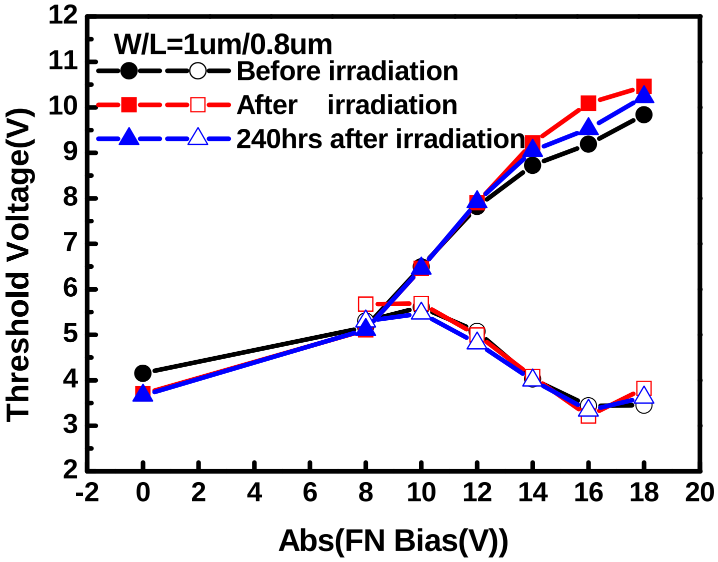


Fig. 3-7: Program and erase windows of the TFT-SONOS memory. The pulse width is 1 s and the EUV irradiation time is 2 min.

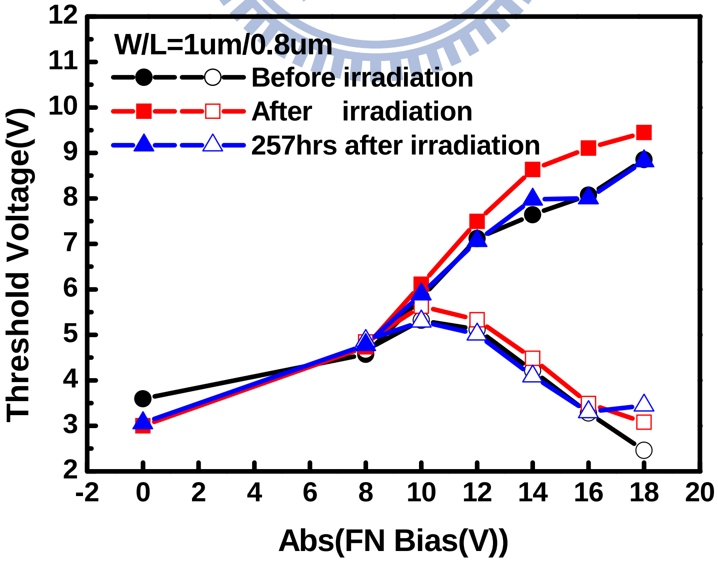


Fig. 3-8: Program and erase windows of the TFT-SONOS memory. The pulse width is 1 s and the EUV irradiation time is 3 min.

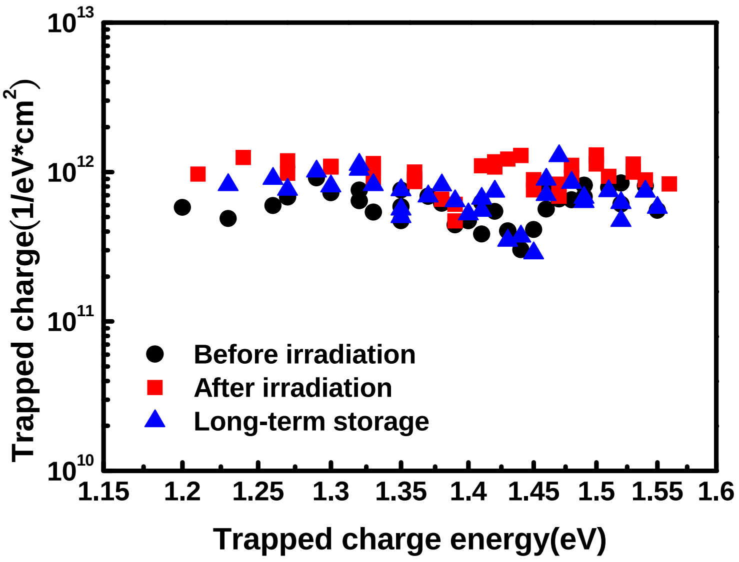


Fig. 3-9: The energy distribution of the charge trapping density in the CTL of the TFT-SONOS memory before and after EUV irradiation, and long-term storage after EUV irradiation.

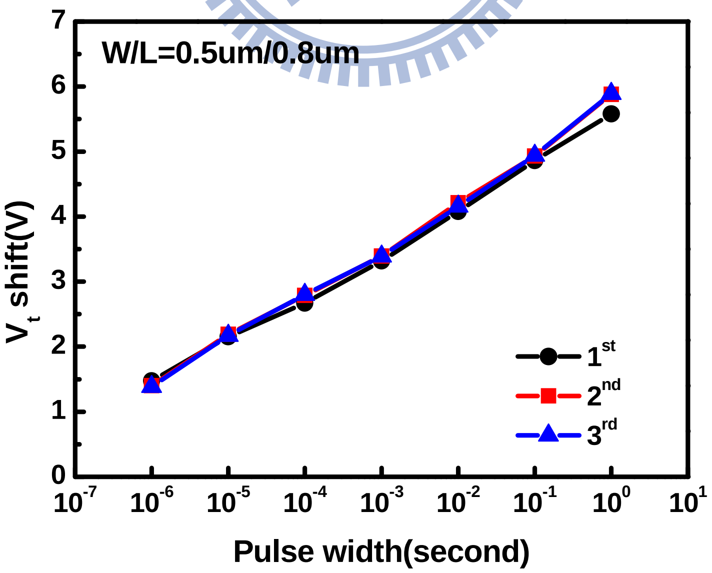


Fig. 3-10: Program speed of the TFT-SONOS memory at V_g = 14V by three times program speed operations.

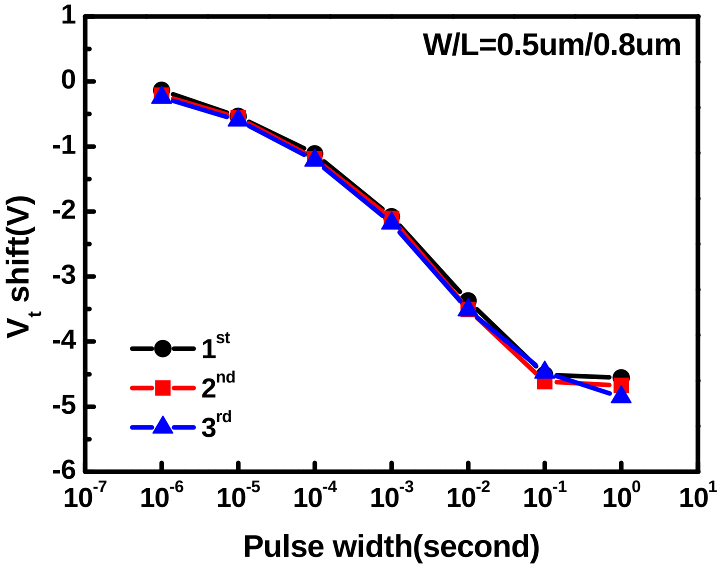


Fig. 3-11: Erase speed of the TFT-SONOS memory at V_g = -18V by three times erase speed operations.

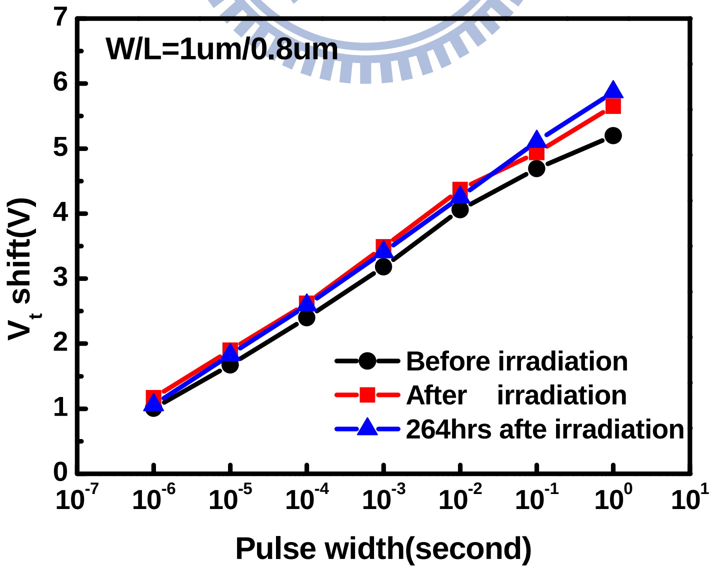


Fig. 3-12: Program speed of the TFT-SONOS memory at V_g = 14V. The EUV irradiation time is 1 min.

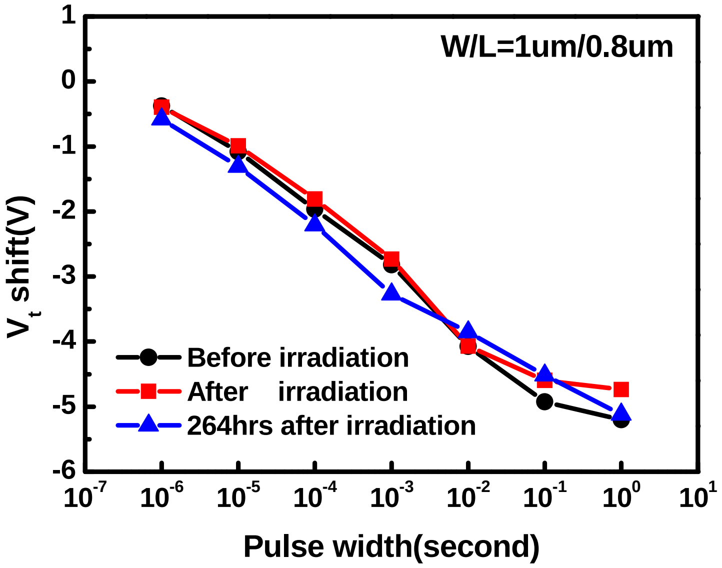


Fig. 3-13: Erase speed of the TFT-SONOS memory at V_g = -18V. The EUV irradiation time is 1 min.

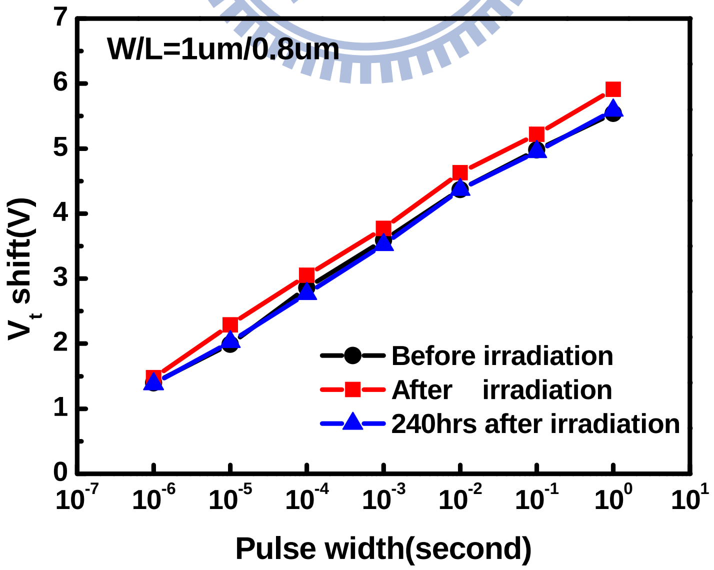


Fig. 3-14: Program speed of the TFT-SONOS memory at V_g = 14V. The EUV irradiation time is 2 min.

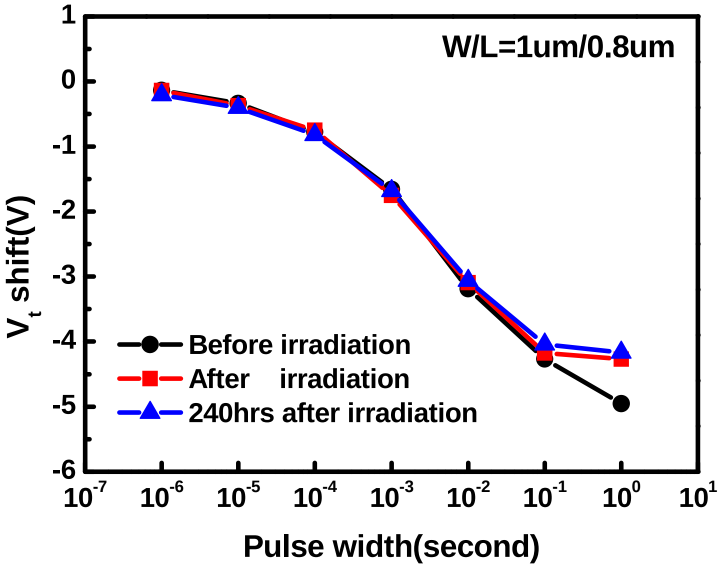


Fig. 3-15: Erase speed of the TFT-SONOS memory at V_g = -18V. The EUV irradiation time is 2 min.

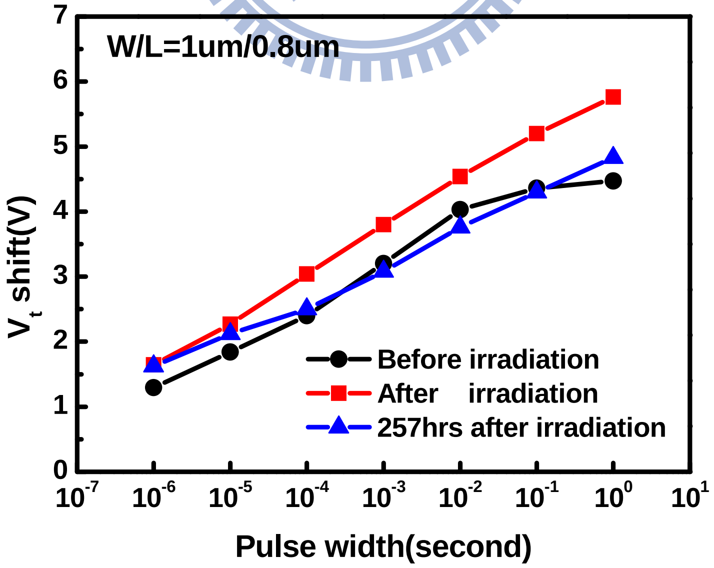


Fig. 3-16: Program speed of the TFT-SONOS memory at V_g = 14V. The EUV irradiation time is 3 min.

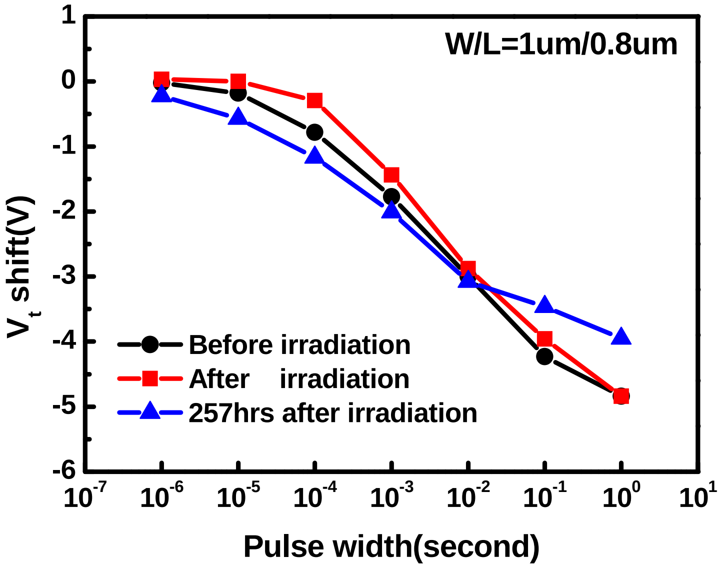


Fig. 3-17: Erase speed of the TFT-SONOS memory at V_g = -18V. The EUV irradiation time is 3 min.

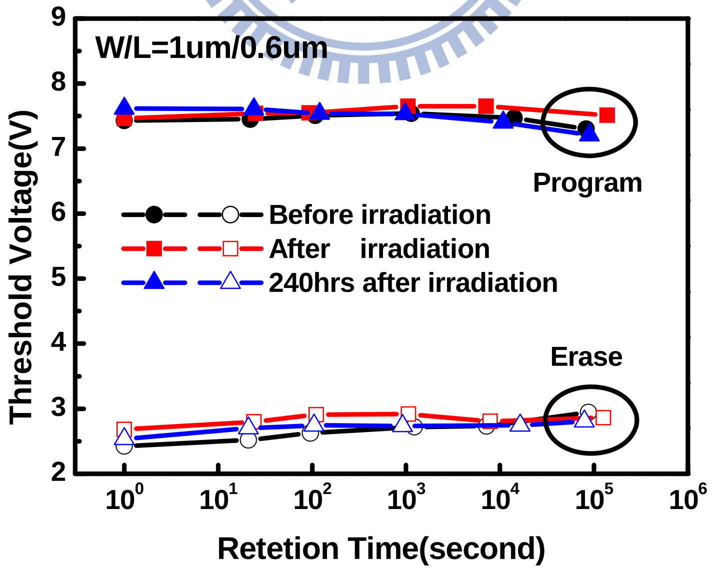


Fig. 3-18: Retention characteristic of the TFT-SONOS memory. The EUV irradiation time is 1 min.

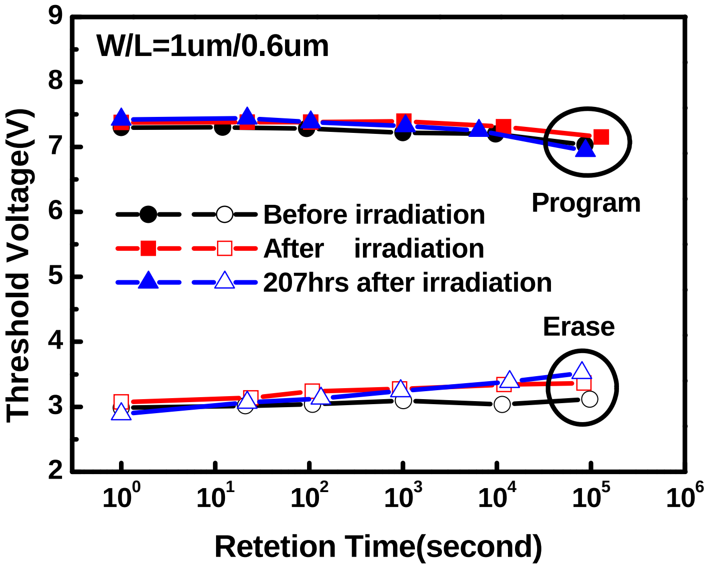


Fig. 3-19: Retention characteristic of the TFT-SONOS memory. The EUV irradiation time is 2 min.

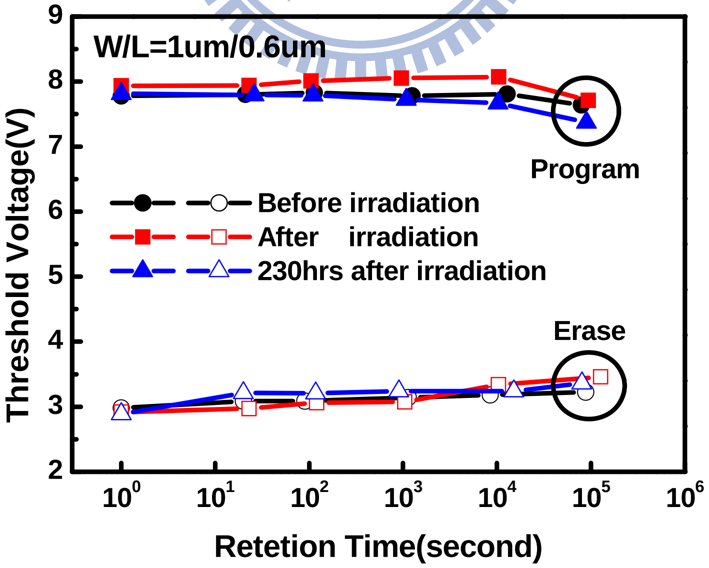


Fig. 3-20: Retention characteristic of the TFT-SONOS memory. The EUV irradiation time is 3 min.

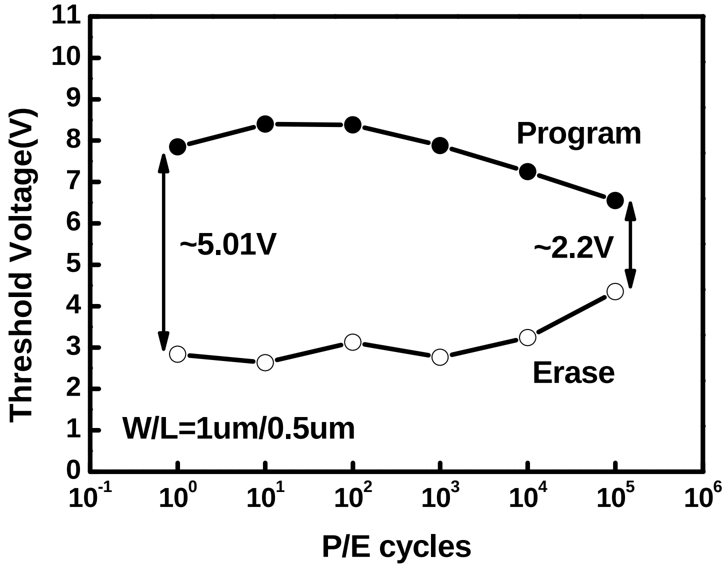


Fig. 3-21: Endurance characteristic of the TFT-SONOS memory before EUV irradiation. The gate voltage is +17V for program and -20V for erase with 10 msec pulse width.

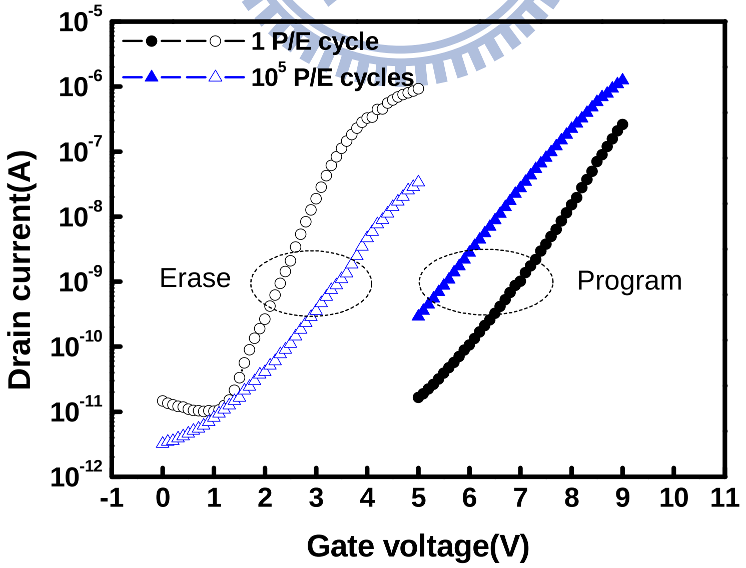


Fig. 3-22: The I_d-V_g curves of the endurance characteristic before EUV irradiation.

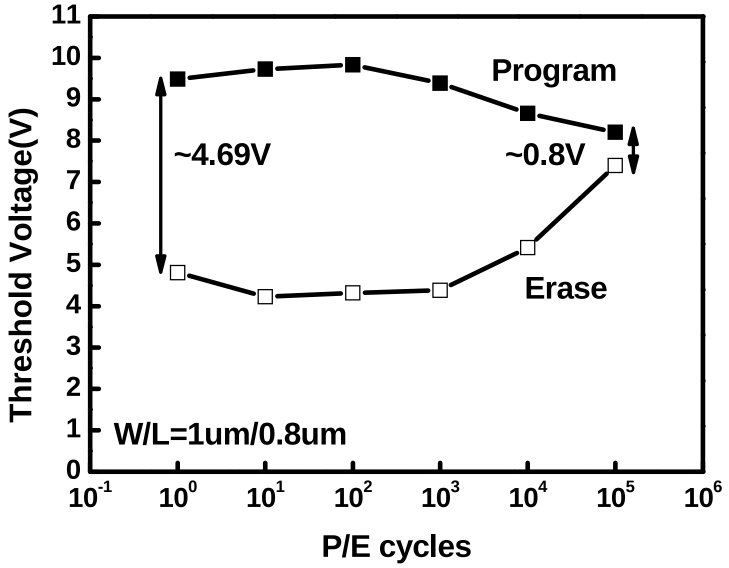


Fig. 3-23: Endurance characteristic of the TFT-SONOS memory after 1 min EUV irradiation. The gate voltage is +17V for program and -20V for erase with 10 msec pulse width.

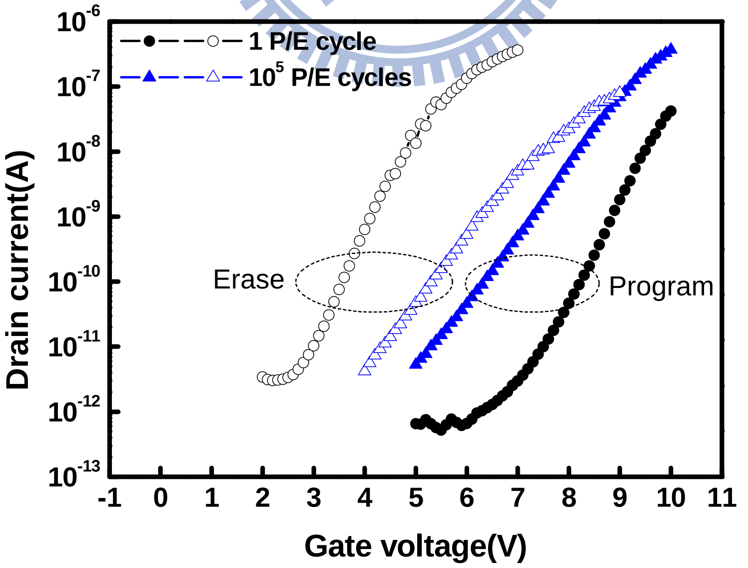


Fig. 3-24: The I_d-V_g curves of the endurance characteristic after 1 min EUV irradiation.

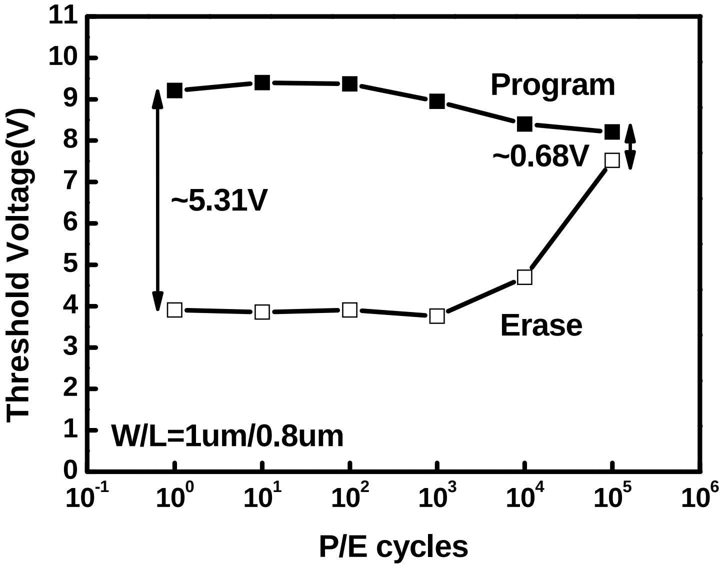


Fig. 3-25: Endurance characteristic of the TFT-SONOS memory after 2 min EUV irradiation. The gate voltage is +17V for program and -20V for erase with 10 msec pulse width.

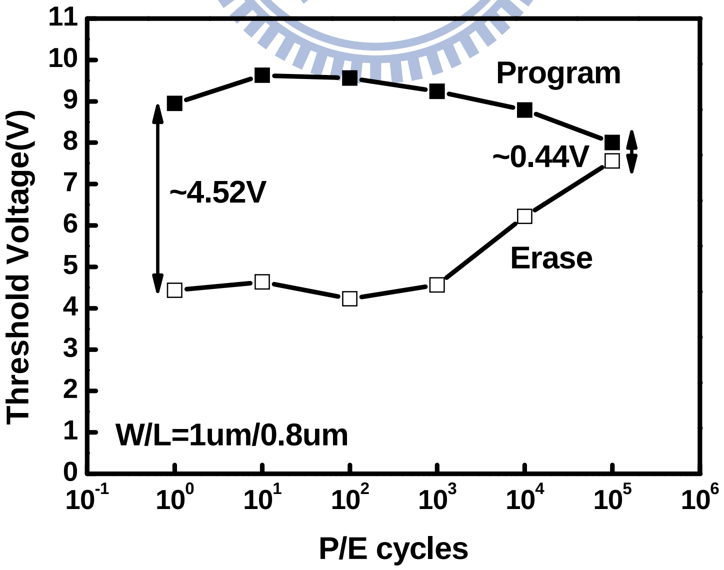


Fig. 3-26: Endurance characteristic of the TFT-SONOS memory after 3 min EUV irradiation. The gate voltage is +17V for program and -20V for erase with 10 msec pulse width.

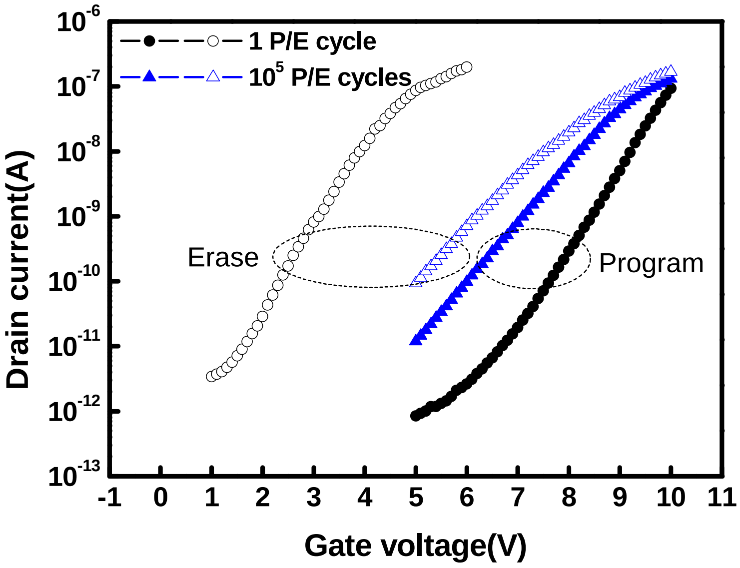


Fig. 3-27: The I_d-V_g curves of the endurance characteristic after 2 min EUV irradiation.

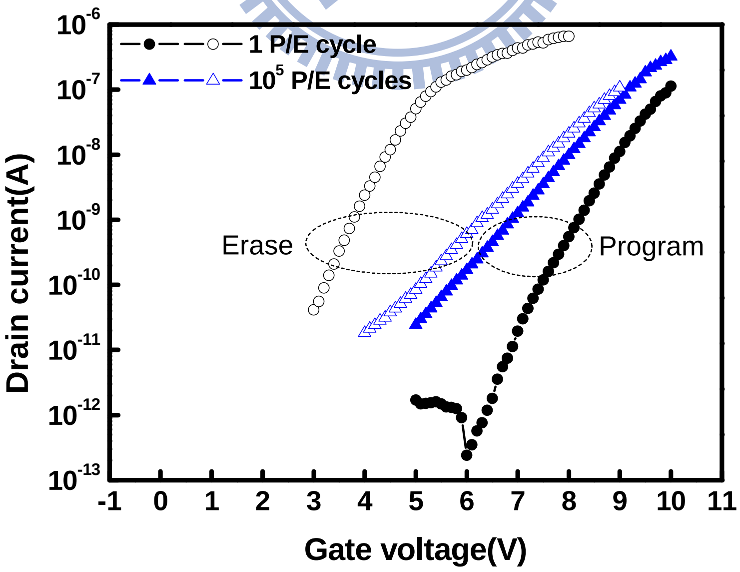


Fig. 3-28: The I_d-V_g curves of the endurance characteristic after 3 min EUV irradiation.

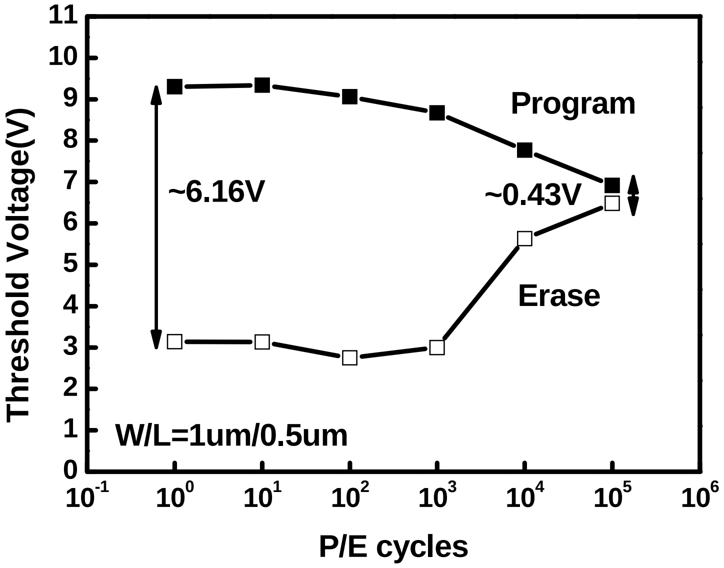


Fig. 3-29: Endurance characteristic of the TFT-SONOS memory after 30 min EUV irradiation. The gate voltage is +17V for program and -20V for erase with 10 msec pulse width.

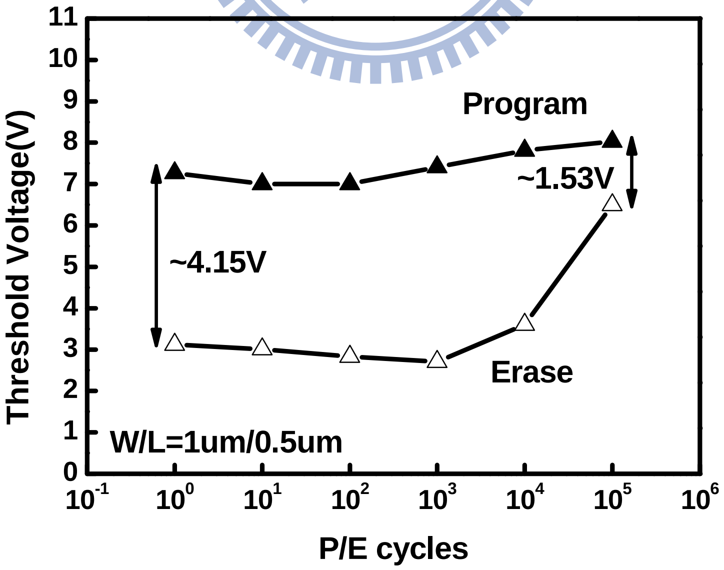


Fig. 3-30: Endurance characteristic of the 30 min EUV irradiated TFT-SONOS memory performed at 600°C annealing. The gate voltage is +17V for program and -20V for erase with 10 msec pulse width.

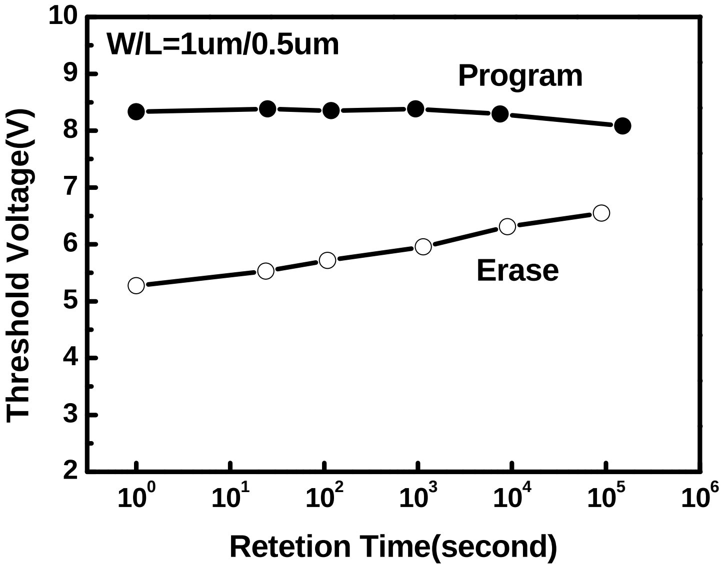


Fig. 3-31: Retention characteristic of the TFT-SONOS memory after endurance test.

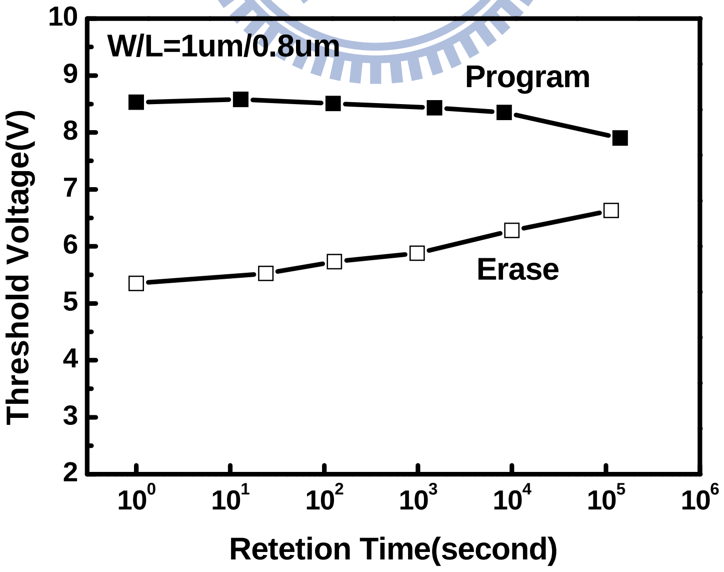


Fig. 3-32: Retention characteristic of the 1 min EUV irradiated TFT-SONOS memory after endurance test.

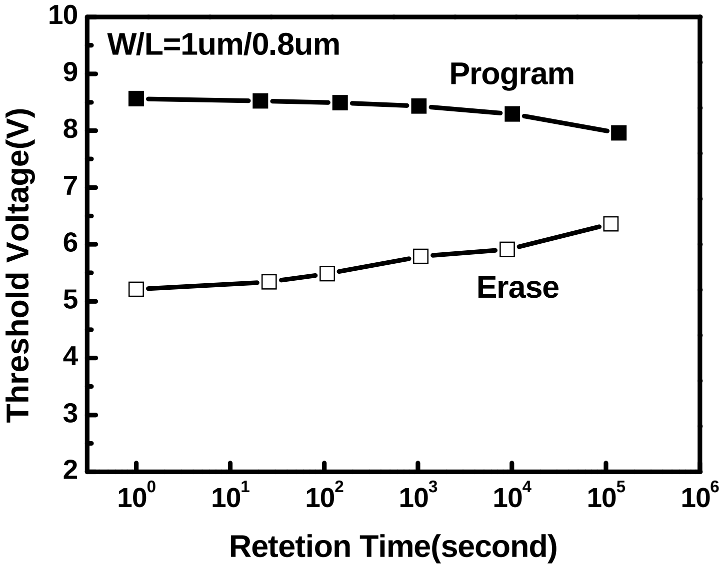


Fig. 3-33: Retention characteristic of the 2 min EUV irradiated TFT-SONOS memory after endurance test.

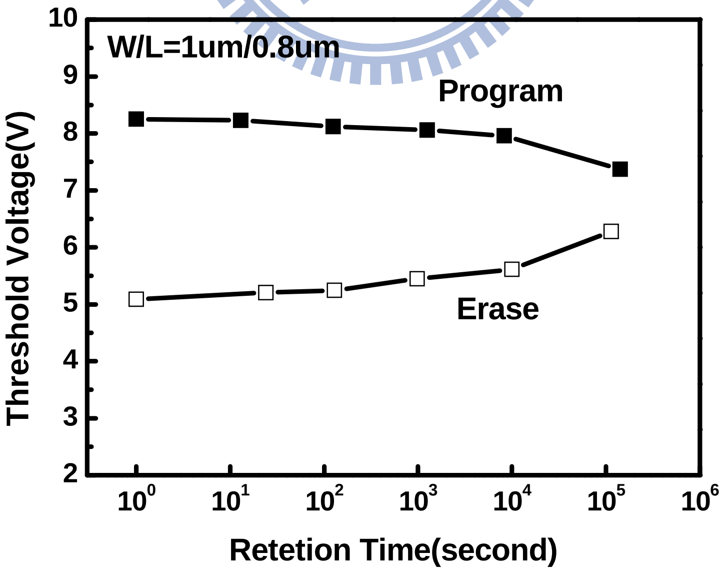


Fig. 3-34: Retention characteristic of the 3 min EUV irradiated TFT-SONOS memory after endurance test.

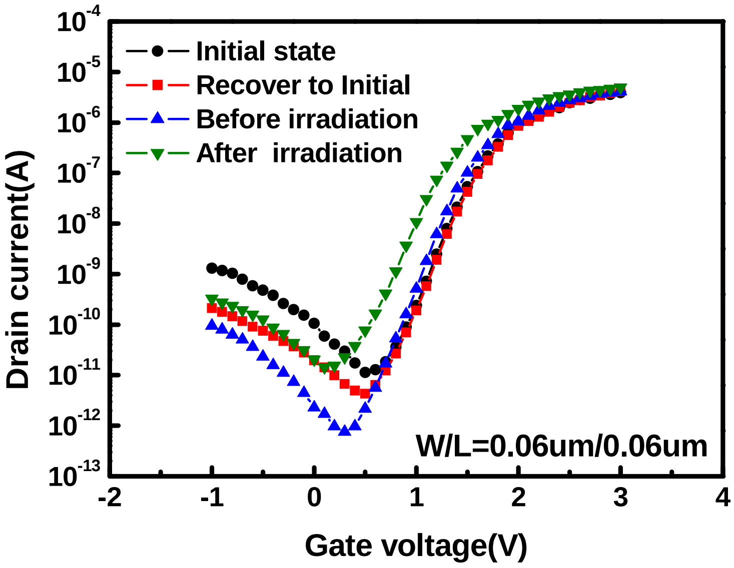


Fig. 3-35: The I_d-V_g curves of the multi-gate TiN NC memory before EUV irradiation and experienced 2 min EUV irradiation.

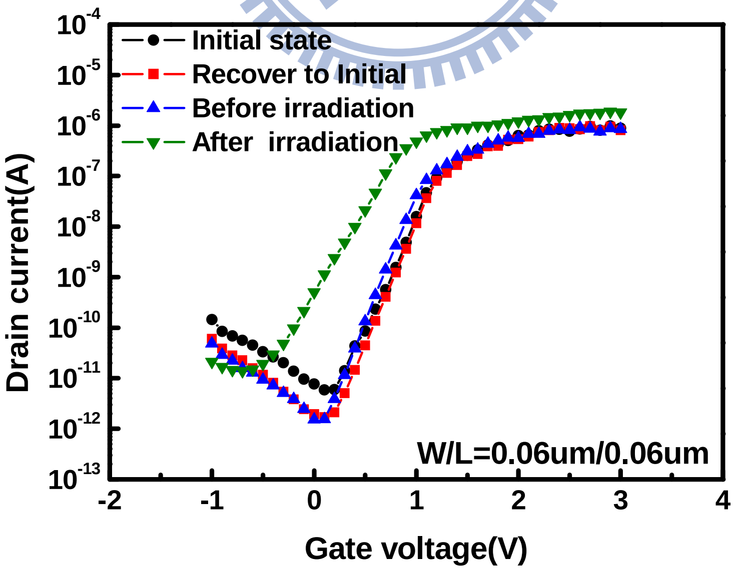


Fig. 3-36: The I_d-V_g curves of the multi-gate TiN NC memory before EUV irradiation and experienced 30 min EUV irradiation.

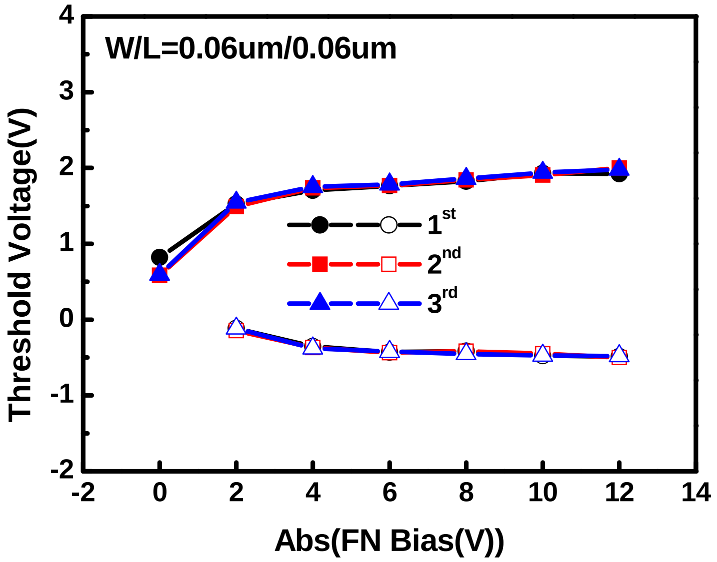


Fig. 3-37: Program and erase windows of the multi-gate TiN NC memory experienced three times P/E operations with pulse width of 1 s.

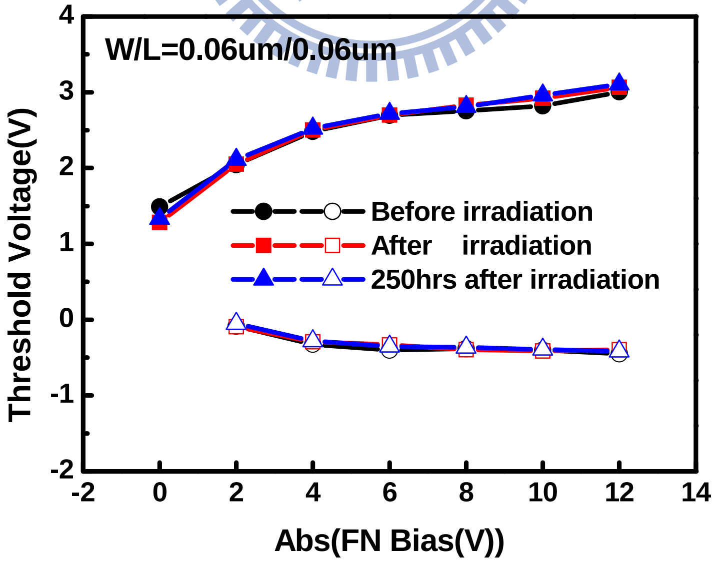


Fig. 3-38: Program and erase windows of the multi-gate TiN NC memory. The pulse width is 1 s and the EUV irradiation time is 2 min.

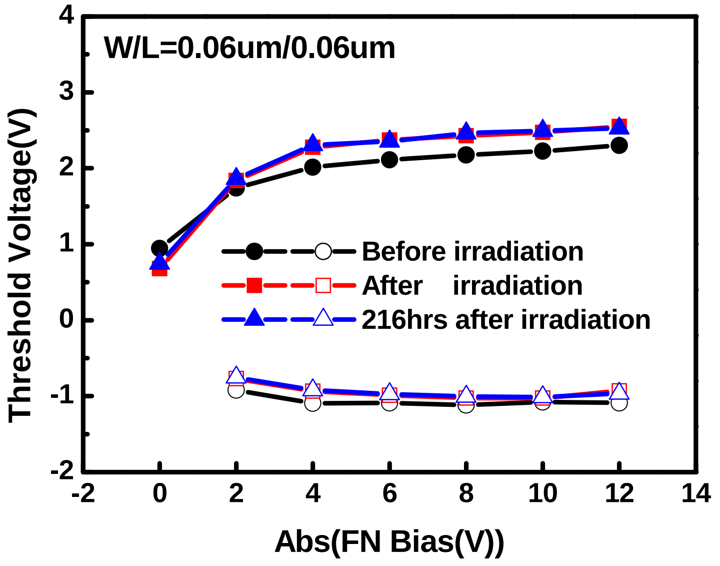


Fig. 3-39: Program and erase windows of the multi-gate TiN NC memory. The pulse width is 1 s and the EUV irradiation time is 30 min.

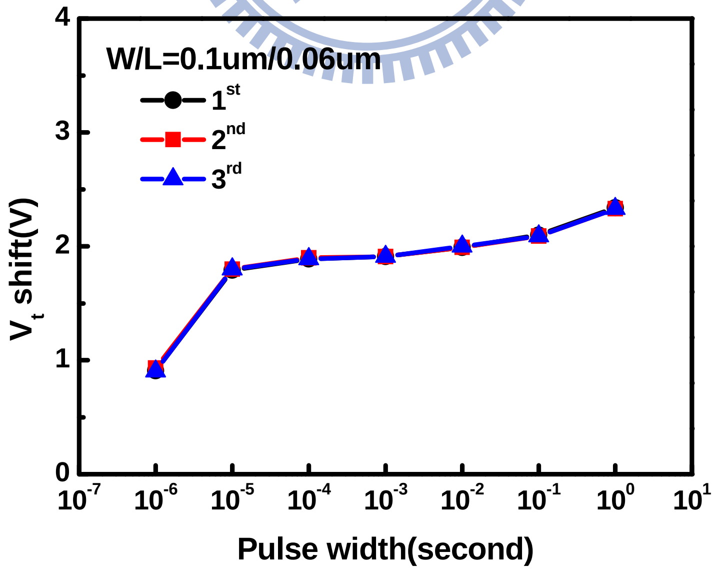


Fig. 3-40: Program speed of the multi-gate TiN NC memory at V_g = 12V by three times program speed operations.

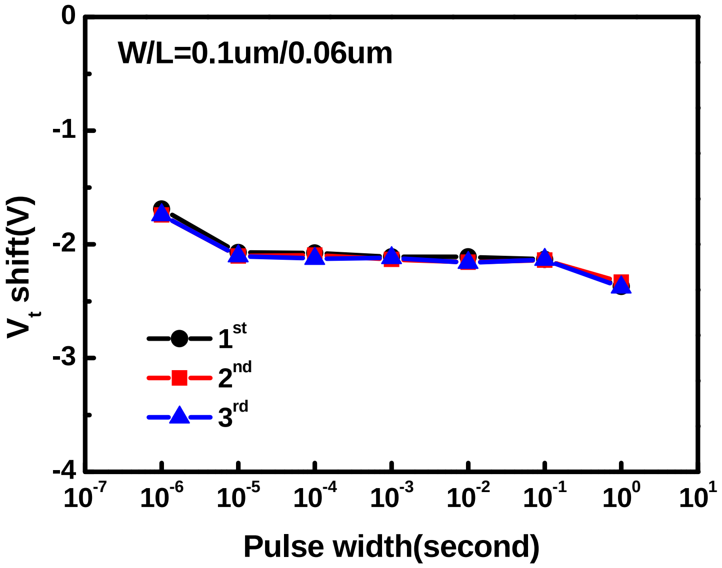


Fig. 3-41: Erase speed of the multi-gate TiN NC memory at V_g = -12V by three times erase speed operations.

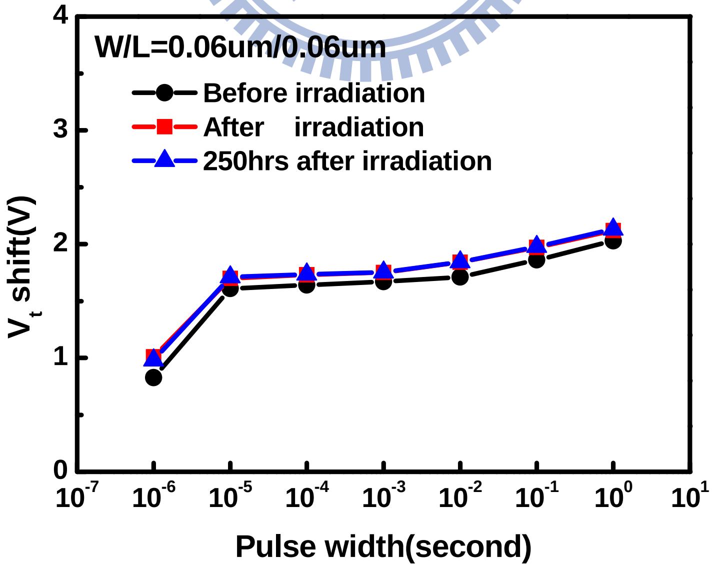


Fig. 3-42: Program speed of the multi-gate TiN NC memory at V_g = 12V. The EUV irradiation time is 2 min.

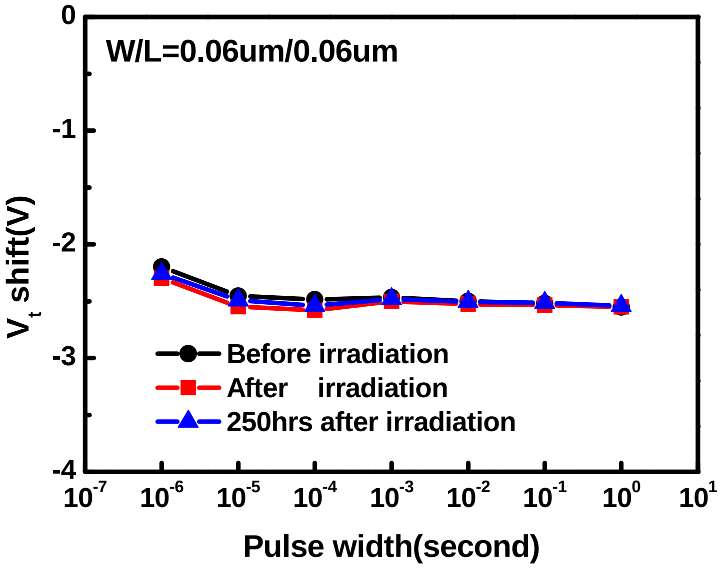


Fig. 3-43: Erase speed of the multi-gate TiN NC memory at V_g = -12V. The EUV irradiation time is 2 min.

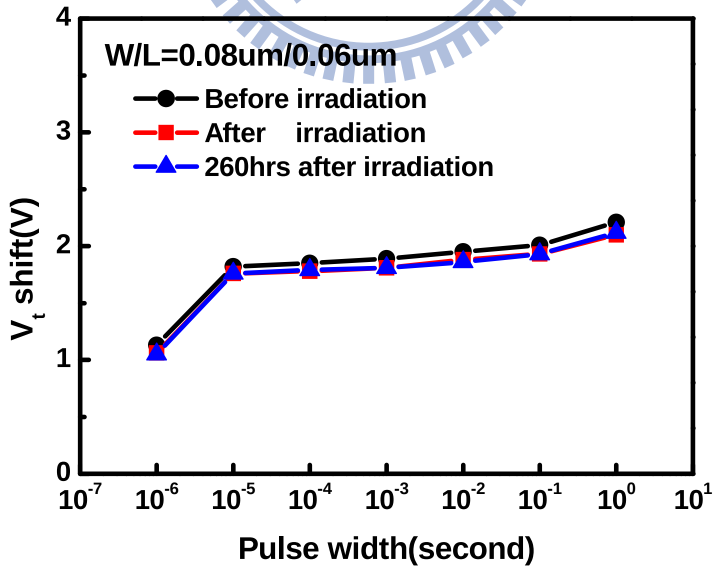


Fig. 3-44: Program speed of the multi-gate TiN NC memory at V_g = 12V. The EUV irradiation time is 30 min.

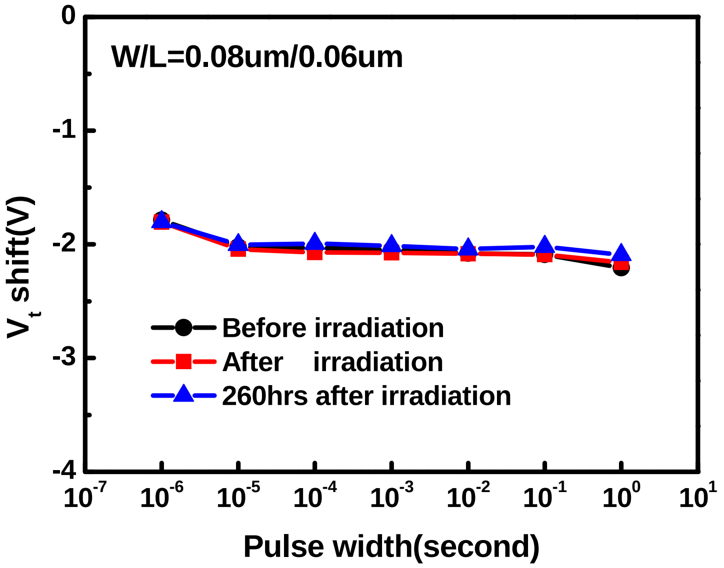


Fig. 3-45: Erase speed of the multi-gate TiN NC memory at V_g = -12V. The EUV irradiation time is 30 min.

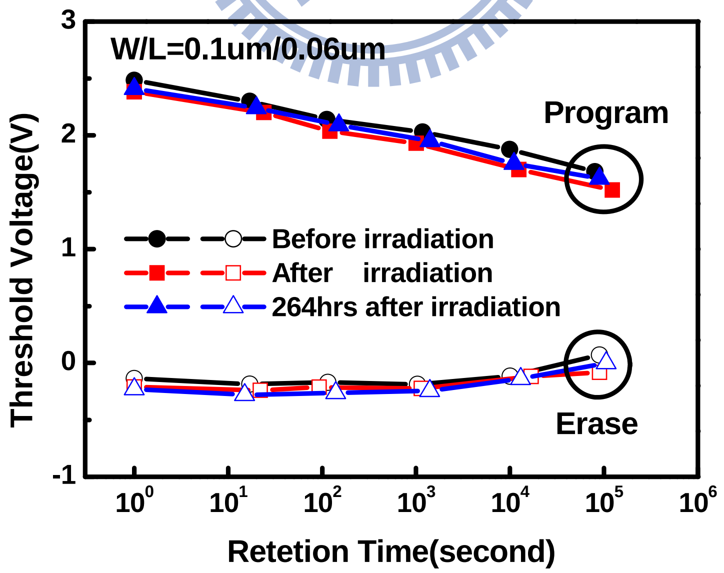


Fig. 3-46: Retention characteristic of the multi-gate TiN NC memory. The EUV irradiation time is 2 min.

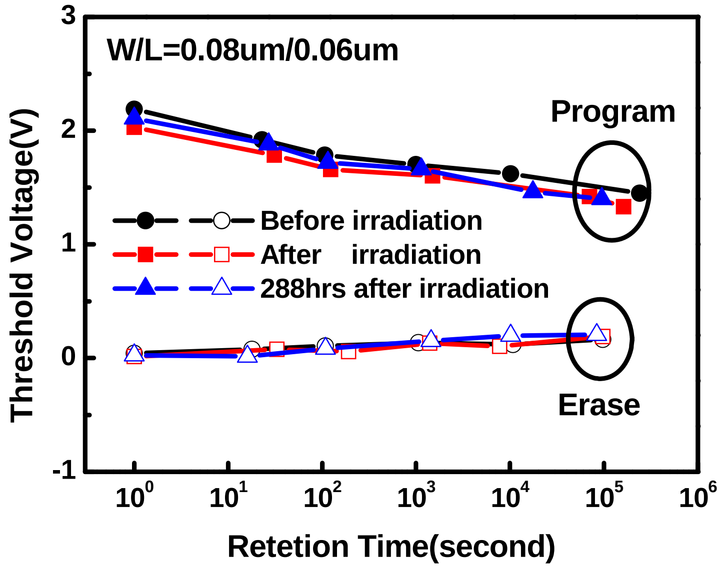


Fig. 3-47: Retention characteristic of the multi-gate TiN NC memory. The EUV irradiation time is 30 min.

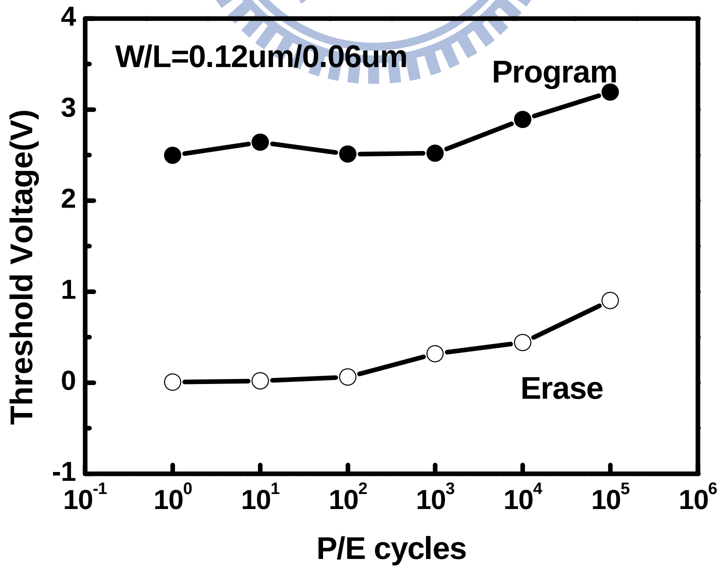


Fig. 3-48: Endurance characteristic of the multi-gate TiN NC memory before EUV irradiation. The gate voltage is +12V for program and -9V for erase with 10 msec pulse width.

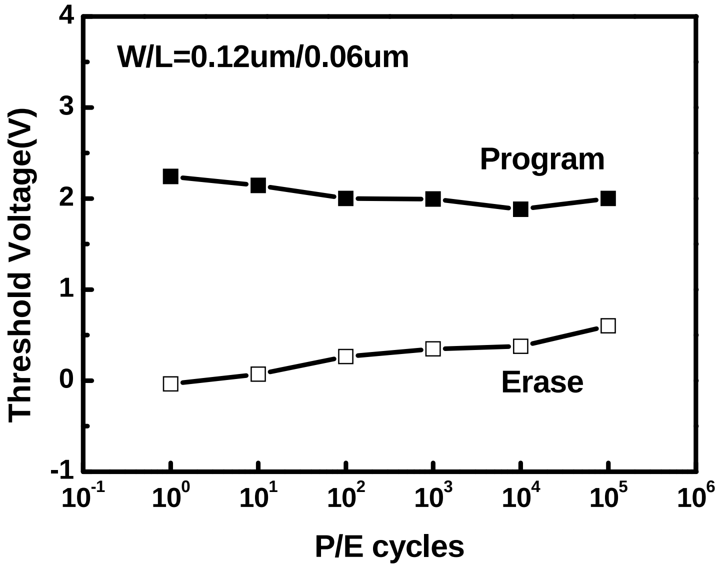


Fig. 3-49: Endurance characteristic of the multi-gate TiN NC memory after 2 min EUV irradiation. The gate voltage is +12V for program and -9V for erase with 10 msec pulse width.

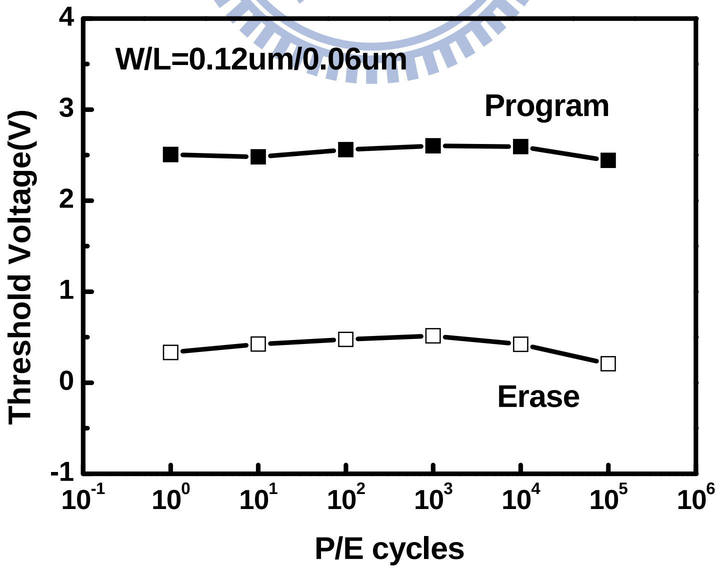


Fig. 3-50: Endurance characteristic of the multi-gate TiN NC memory after 30 min EUV irradiation. The gate voltage is +12V for program and -9V for erase with 10 msec pulse width.

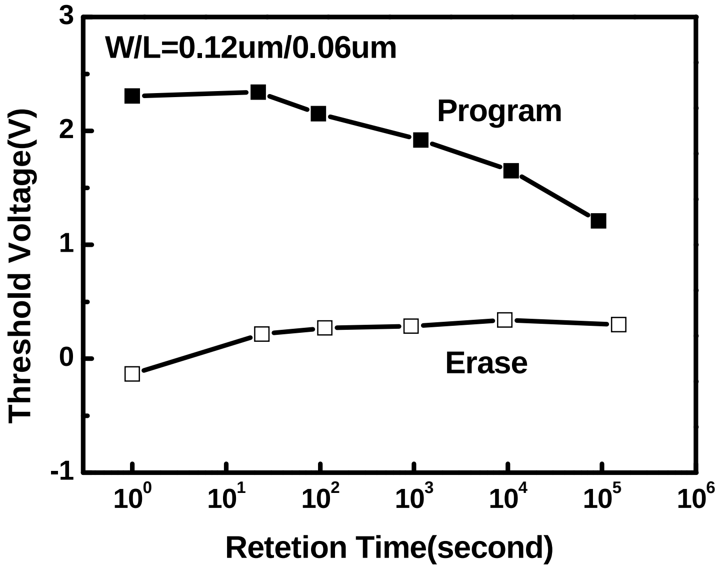


Fig. 3-51: Retention characteristic of the multi-gate TiN NC memory after endurance test.

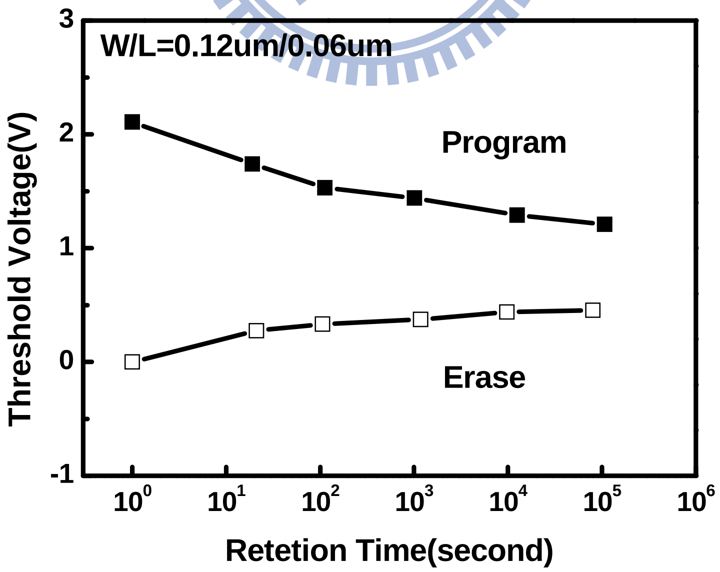


Fig. 3-52: Retention characteristic of the 2 min EUV irradiated multi-gate TiN NC memory after endurance test.

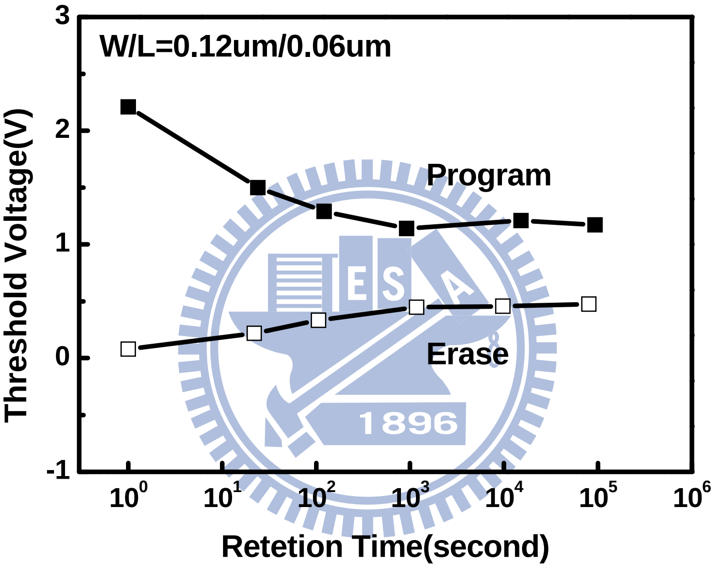


Fig. 3-53: Retention characteristic of the 30 min EUV irradiated multi-gate TiN NC memory after endurance test.

Chapter 4

Conclusions and Future Works

4-1 Conclusions

In this work, we studied the impact of EUV irradiation induced damages on the characteristics of TFT-SONOS memory and multi-gate TiN NC memory since it is an unavoidable issue once the EUVL becomes the next generation lithography technology and is used in mass-production of memory ICs. On the TFT-SONOS memory, several degradation phenomena are observed after EUV irradiation, as summarized in Fig. 4-1. In the blocking layer, irradiation generated defects enhances the electron backside injection. Therefore, erase saturation occurs at high erase voltage in memory window and erase speed characteristics. . Similarly, endurance degradation is also caused by the irradiation generated defects in the blocking layer. In the Si_3N_4 charge trapping layer (CTL), the increase of V_t values in the program state are observed in the memory window characteristic, which implies a few new traps are generated during EUV irradiation. The reduction of the initial V_t after EUV irradiation indicates that a small amount of the net positive charges are generated in stacked dielectrics. It is suspected that most of these charges are located in the Si_3N_4 CTL. In the tunneling oxide, the irradiation induced damages degrade the retention characteristic at long EUV irradiation time. But the degradation is not very significant. After long-term storage at room temperature, more severe degradation of retention characteristic is observed because additional defects are generated by the recombination of the trapped holes with electrons. Compared with the TFT-SONOS memory, EUV irradiation has weak impact on the multi-gate TiN NC memory, as shown in Fig. 4-2. Almost all the memory performances are still stable, even after long-term storage.

The difference in the immunity to EUV irradiation between SONOS and NC memories is due to the difference in the charge trapping mechanisms. The charge storage mechanisms with different types of non-volatile memory have been introduced in section 1-3. The memory characteristics after EUV irradiation are strongly related to the charge storage mechanism. On the SONOS memory, charges are stored in discrete traps in the Si_3N_4 CTL. As the CTL layer is irradiated by the EUV, in addition to the generation of electron-hole pairs, additional new traps are produced due to the broken bonds caused by high-energy EUV irradiation. These traps are regarded as charge trapping sites for electron storage so that the memory characteristic changes after EUV irradiation. On the NC memory, charges are mainly stored in isolated metallic NCs and each of them is surrounded by insulated dielectrics in the CTL. Both surrounding dielectric and metallic NCs possess higher potential barrier which can prevent stored charges from escaping. Thus, in spite that some defects or traps may be produced in the insulated dielectrics after EUV irradiation, the amount of charges stored in these new produced traps are still much less than the charges stored in the metallic NCs so that the memory characteristics do not change significantly. Besides, because charges are stored in the well-protected metallic NCs, the EUV irradiation is not prone to affect the stored charges. Thus, combine the above illustrations; the stored charges have well-protection against EUV irradiation so the memory characteristics exhibit no significant change after EUV irradiation.

In addition, we also discuss the recovery feasibility for the severely degraded endurance characteristic on the TFT-SONOS memory. However, this EUV damaged phenomenon cannot be recovered at the typical thermal budget of the back-end-of-line process. For this reason, it is suggested that high dose EUV irradiating on the SONOS stack after front-end-of-line process should be avoided if the EUVL is used in mass-production of the SONOS memory. On the other hand, since the NC memory exhibits much better EUV radiation immunity than the SONOS memory; it is recommended that the EUVL could be a potential solution for advanced NC memories to further scaling-down without reliability issue.

4-2 Future Works

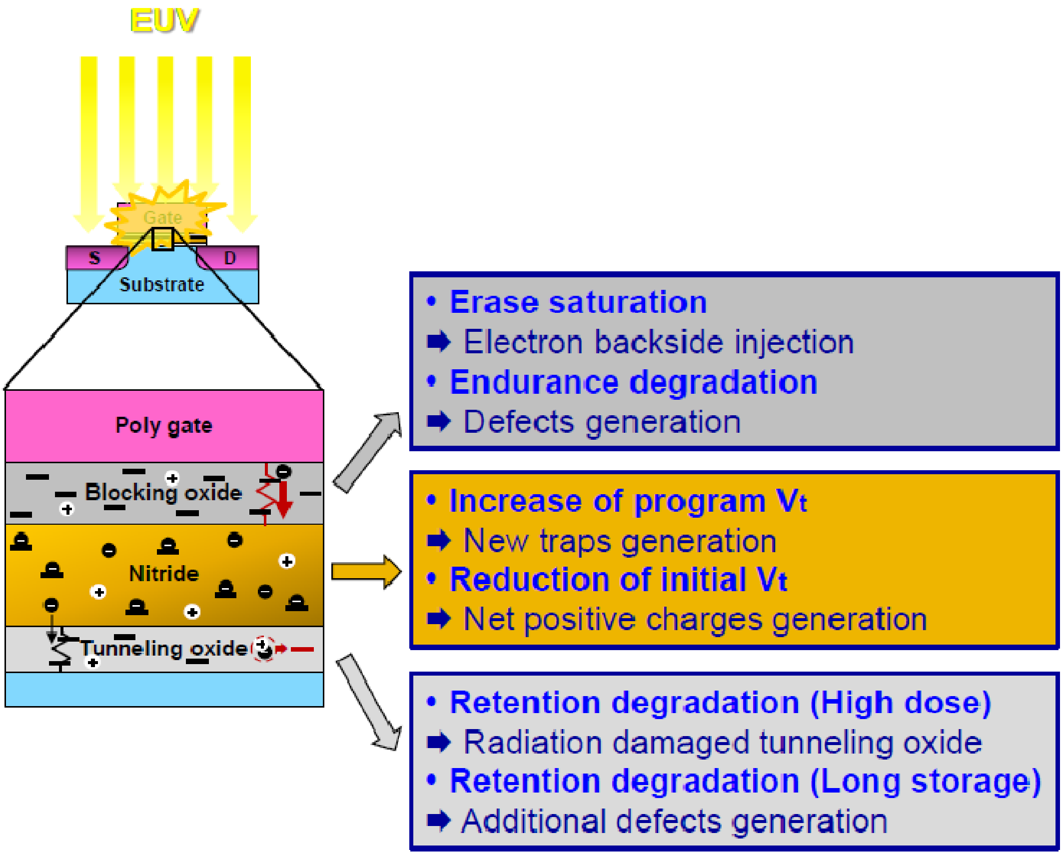
First, the flux of the BL21B beam line must be measured by using photodiode to calculate the actual dose rate.

According to the EUV irradiation induced damages on the memory characteristics discussed in Chap 3, it is clear that the most critical issue is the severely degraded blocking layer in the TFT-SONOS memory. Therefore, improving the EUV irradiation immunity to the blocking layer is needed. Since SiO_2 is stronger than most of the dielectric used in IC industry to resist the high energy radiation [55], SiO_2 should be the best candidate of the blocking layer. In this case, those radiation hardness techniques which have been reported would be helpful.

In addition, decreasing the program/erase (P/E) voltages is another possible solution to improve the endurance characteristic. Using high dielectric constant material as blocking layer can improve the gate coupling efficiency so that the operation voltage can be lowered. Using high-k blocking layer can also reduce the electric field intensity in the blocking layer, which is also helpful to improve the endurance characteristic. The Al_2O_3 used in the TiN NC memory in this thesis is promising. Another high-k materials are worthy for investigation.

In this thesis, poly-Si SONOS memory prepared in academic laboratory was used. It is acknowledged that the device performance of our devices is not as good as that of the SONOS memory fabricated by industry. The response of the high performance SONOS memory to the EUV irradiation should be examined.

For the multi-gate TiN NC memory, the memory characteristics before EUV irradiation are not good enough, especially the retention characteristic. Samples with better performance would be more sensitive to radiation damages. Therefore, the immunity to EUV irradiation of the NC memory should be reconfirmed by using other sample which has better performance.

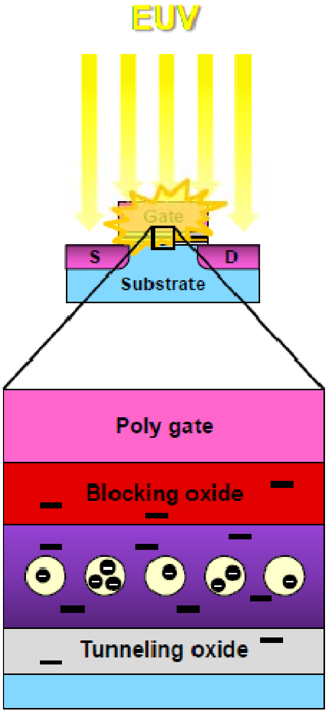


- **Erase saturation**
  - ➡ Electron backside injection
- **Endurance degradation**
  - ➡ Defects generation

- **Increase of program V_t**
  - ➡ New traps generation
- **Reduction of initial V_t**
  - ➡ Net positive charges generation

- **Retention degradation (High dose)**
  - ➡ Radiation damaged tunneling oxide
- **Retention degradation (Long storage)**
  - ➡ Additional defects generation

Fig. 4-1: The observed phenomena of the TFT-SONOS memory after EUV irradiation.



- Almost all the memory performances are not affected by the EUV irradiation.
- **It exhibits much better EUV radiation tolerance with respect to the SONOS memory due to the difference in the charge trapping mechanisms.**

Fig. 4-2: The observed phenomena of the multi-gate TiN NC memory after EUV irradiation.

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個人簡歷

姓名：顏志展

性別：男

出生年月日：西元 1985 年 9 月 11 日

出生地：台灣 台南市

學歷：

國立台南第二高級中學（2001.9 ~ 2004.6）

私立東海大學物理學系學士（2004.9 ~ 2008.6）

國立交通大學電子研究所碩士（2008.9 ~ 2010.6）

碩士論文：

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Effect of Extreme Ultra-Violet Radiation on Advanced Non-volatile Memories