國立交通大學

電子工程學系　　電子研究所碩士班

碩 士 論 文

應用於超寬頻系統之低雜訊放大器之設計

Design Low Noise Amplifier for

Ultra- Wideband Application

研 究 生：王柏之

指導教授：郭建男　教授

中 華 民 國 九 十 三 年 六 月

應用於超寬頻系統之低雜訊放大器之設計

Design Low Noise Amplifier for Ultra- Wideband Application

研 究 生：王柏之　　Student：Po-Chi Wang

指導教授：郭建男　　Advisor：Chien-Nan Kuo

國 立 交 通 大 學

電 子 工 程 系　電子研究所碩士班

碩 士 論 文

A Thesis

Submitted toInstitute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

In partial Fulfillment of the Requirements

For the Degree of

Master

In

Electronics Engineering

June 2004

Hsinchu, Taiwan, Republic of China

中華民國九十三年六月

應用於超寬頻系統之低雜訊放大器之設計

學生：王柏之　　指導教授：郭建男教授

國立交通大學

電子工程學系 電子研究所碩士班

摘要

本篇論文主旨在於利用標準0.18um CMOS製程設計適用於超寬頻系統前端接受器之低雜訊放大器積體電路。此外，使用達靈頓對架構之窄頻低雜訊放大器亦被設計與分析。此兩顆低雜訊放大器已經由晶片製作而被驗證。

第一顆晶片在於設計與分析一適用於 5-GHz 頻帶無線區域網路之高增益低雜訊放大器。此放大器使用達靈頓對之兩倍截止頻率之特性來達到高增益之目的。實驗結果顯示此一放大器在 6GHz 頻率有著最高功率增益(S21) 15.5dB，輸入返回損耗(S11) -12 dB 以及最低雜訊指數 3.5dB，此外此電路消耗之功率為 13mW。

在第二顆晶片裡，適用於接收端超寬頻系統之寬頻放大器被設計與分析。我們利用負回受電阻達到寬頻之輸入阻抗匹配以及自偏壓，增益補償方法達到操作頻率範圍內之平坦增益，進而濾除操作頻率範圍外之訊號。實驗結果顯示此一放大器在 3-8 GHz 頻率下有著最高功率增益(S21) 9.2dB，輸入返回損耗(S11)低於 -5.8dB 以及平均雜訊指數 6.1dB，此電路消耗之功率為 15mW。此外，改善性能之超寬頻放大器已被製作，並且加入了可變增益之功能以增加輸入信號動態範圍。

Design Low Noise Amplifier for Ultra-Wideband Application

Student: Po-Chi Wang Advisor: Prof. Chien-Nan Kuo

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

ABSTRACT

The aim in this thesis is mainly based on the design of low noise amplifier (LNA) in the receiver path of ultra-wideband system using standard 0.18um CMOS process. Also, a narrow band LNA using Darlington pair structure is designed for 5.5-GHz frequency band. The two low noise amplifiers were verified through 2 individual chips.

In the first chip, a narrow band high gain low noise amplifier using Darlington pair structure is analyzed and designed for wireless local network area (WLNA) operating at 5-GHz frequency band. We employ the double cutoff frequency property of Darlington pair to achieve high gain design. Measured data show that the amplifier achieves maximum power gain (S21) of 15.5 dB, -12 dB input return loss (S11), and minimal noise figure of 3.5 dB at the 6GHz frequency while consuming 13mW.

In the second chip, a wideband amplifier (LNA), intended for use in the receiver path of an ultra-wideband (UWB) system, is analyzed and designed. We employ the techniques of negative feedback resistors to achieve broadband matching together with self-biasing, and gain compensation method to derive flat gain over the entire operating frequency band as well as filter out the signal out of band. Measured data show that the amplifier achieves maximum

power gain (S21) of 9.2 dB, input return loss (S11) below -5.8 dB, and average noise figure of 6.1dB in the frequency range from 3 to 8-GHz, while consuming only 15mW. The improved and modified version in terms of the measured result from this chip has been implemented. Also, variable gain function has been added to enlarge the input dynamic range in the modified chip.

誌謝

終於完成這篇論文，首先要感謝我的指導教授郭建男博士這一年半以來給我的指導與鼓勵，不但讓我在射頻積體電路設計的領域中獲益良多，並且對積體電路設計又更深入的了解與認識。再者，感謝實驗室每一位同學這一年半的照顧與提攜，在這實驗室裡不僅讓我學習到了做學問的方法以及對專業領域深入的研究，更讓我交到了一堆志同道合的好朋友，這是我這段時間除了學問外所獲得的最大資產。另外，亦要感謝國家晶片中心(CIC)以及洪英瑞同學在晶片製作與量測上的大力幫忙，使得我能更順利的完成此篇碩士論文。最後更要感謝我的家人給我精神上與經濟上的支持，特別是我母親的栽培與鼓勵使我能夠順利完成碩士的生涯。其他要感謝的人還有很多，不可剩數，在此一併謝過

CONTENTS

ABSTRACT (CHINESE) ….....i

ABSTRACT (ENGLISH) ii

ACKNOWLEDGEMENT …….....iv

CONTENTS…….....v

TABLE CAPTIONS.....ix

FIGURE CAPTIONS.....x

Chapter 1 Introduction……....1

1.1 Motivation…….....1

1.2 Thesis Organization…….....2

Chapter 2 Low Noise Amplifier Basic Concepts.....3

2.1 Noise in MOSFET…….....3

2.1.1 Source of Noise…….....3

2.1.1.1 Drain Noise.....4

2.1.1.2 Gate Noise.....4

2.1.1.3 Flicker Noise.....7

2.1.2 Noise Models of the MOS Transistors…….....7

2.2 Low Noise Amplifier Basic……8

2.2.1 Low Noise Amplifier Topology and Basic…..……... …….8

2.2.2 Inductive Source Degeneration LNA……..11

2.2.2.1 Operational Basic.....11

2.2.2.2 Optimizations of LNA Design Flow……14

2.2.3 Introduction to Broadband LNA…….18

Chapter 3 5.5 GHz High Gain LNA Using Darlington Pair…….....22

3.1 Motivation…….....22

3.2 Analysis of Darlington Pair LNA Topology……22

3.2.1 Design principle…….....22

3.2.2 Analysis and Design of the LNA Using Darlington Pair.....24

3.2.2.1 Trans-conductance in Darlington Pair Stage.....24

3.2.2.2 Input Impedance Matching……..25

3.3 Discussion on Simulation and Measurement Result……26

3.3.1 Verification of Equation(3-4)..…….…….....26

3.3.2 Chip Implementation…….....29

3.2.3 Simulation and Measurement Result……...29

3.4 Conclusion…….33

Chapter4 A 3 to 8GHz Ultra-Wideband CMOS LNA……34

4.1 Introduction……..34

4.2 Principle of the circuit design…….....34

4.2.1 Ultra-Wideband LNA Circuit Topology…….34

4.2.2 Broadband Input Matching…….36

4.2.3 Gain Flatness Technique…….37

4.2.4 Design Considerations and Trade Off…….39

4.3 Chip Implementation and Measured Result…….40

4.3.1 Microphotograph of Chip…….....40

4.3.2 Measurement and Simulation Result……...41

4.4 Improved UWB LNA…….....45

4.4.1 Wide-band Input Matching…….....46

4.4.2 Variable Gain Function…….....48

4.4.3 Simulation Result…….....52

4.4.3.1 Noise Figure.....52

4.4.3.2 S-Parameter……...53

4.4.3.3 Linearity……56

4.4.3.4 Summary of Performance and Comparison with other Wideband Amplifier…….....57

4.4.3.5 Chip Photograph……...58

4.4.4 Conclusion……..59

Chapter5 Summary and Future Work.....……61

5.1 Summary……..61

5.2 Future Work……62

REFERENCES.....…….....63

VITA……65

TABLE CAPTIONS

Table Ⅰ Summary of simulation and measured result of Darlington pair LNA and comparison with single input MOS……..33

Table Ⅱ Summary of measured result of the Ultra Wide-band LNA and performance comparison to other wideband amplifier…….....45

Table Ⅲ Simulation result and specification of the modified ultra wide-band LNA.....58

Table Ⅳ Summary of performance comparison with other wideband amplifier……58

FIGURE CAPTIONS

Fig .2.1 Drain current noise model.....4

Fig .2.2 (a) Gate noise circuit model (b) its equivalent voltage noise model.....5

Fig .2.3 Flicker noise model……7

Fig .2.4 (a) MOSEFET noise model (b) equivalent input referred noise model……..7

Fig .2.5 Common LNA architecture (a) Resistive termination (b) 1/gm termination (c) shunt-series feedback, and (d) inductive degeneration…….....9

Fig .2.6 (a) Common source input stage (b) input stage of ISD LNA noise model……...11

Fig .2.7 Configuration of an N-stage distributed amplifier…….....18

Fig .2.8 Configuration of shunt-series amplifier…….....20

Fig .3.1 Schematic of Darlington pair low noise amplifier…….....23

Fig .3.2 Cutoff frequency of device m_1, m_2 and M_1 versus drain current……..27

Fig .3.3 Profit (M) versus total current of input stage…….....27

Fig .3.4 Influence of miller effect on the S_{21}……..28

Fig .3.5 Microphotograph of the Darlington LNA circuit…….....28

Fig .3.6 Simulation and measured result of power gain (S21) and isolation (S12)……..30

Fig .3.7 Simulation and measured result of input match……..31

Fig .3.8 Simulation and measured result of output match…….....31

Fig .3.9 Simulation and measured result of noise figure……..32

Fig .3.10 Measured result of two-tone test at 5 GHz……..32

Fig .4.1 Schematic of Ultra Wide-band LNA……35

Fig .4.2 Small signal analysis of ultra wide band LNA……36

Fig .4.3 Illustration of signal amplification……37

Fig .4.4 Microphotograph of the UWB LNA circuit……..41

Fig .4.5 Simulation and measured result of power gain (S21) and isolation(S12).....43

Fig .4.6 Simulation and measured result of input match and output match……..43

Fig .4.7 Simulation and measured result of noise figure…….....44

Fig .4.8 Measured result of two-tone test at 5 GHz; Measured IIP3 versus frequency.....44

Fig .4.9 Schematic of the modified UWB LNA……..46

Fig .4.10 Modified input matching network to improve S11 at high frequency in band..

…….....47

Fig .4.11 Using mutual inductance to reduce spiral inductor area…….47

Fig .4.12 Simulation result of the transformer-like spiral inductor……48

Fig .4.13 Illustration of variable gain method……50

Fig .4.14 The variable gain tank G_{load}……..…….50

Fig .4.15 Simulation result of variable gain function……...……..51

Fig .4.16 Simulation result of Noise Figure……....52

Fig .4.17 Simulation result of power gain (S21) at different control voltage…….53

Fig .4.18 Simulation result of power gain (S21) versus different control voltage at

different frequency……..54

Fig .4.19 Simulation result of voltage gain without the buffer stage……..54

Fig .4.20 Simulation result of reverse isolation S12…….....55

Fig .4.21 Simulation result of input return loss (S11) at different control voltage……..55

Fig .4.22 Simulation result of output return loss (S22) at different control voltage….....56

Fig .4.23 Simulation result of two-tone test at 5 GHz…….57

Fig .4.24 Simulation result of IIP3 versus frequency……..57

Fig .4.25 Photograph of the modified UWB LNA……..59

CHAPTER 1

INTRODUCTION

1.1 Motivation

Wireless communications at multi-gigahertz frequencies are a huge market that drives the semiconductors technology toward low-cost solutions. CMOS technology, which is attractive due to its advantages of low cost, high-level integration, and enhancing performance by scaling [1, 2], will meet the market requirement in system implementation.

Typically, the first stage of a receiver is a low noise amplifier (LNA), whose main function is to provide enough gain to suppress the noise of subsequent stages as well as adding as little noise as possible in itself. The major problem of CMOS technology at high frequencies is the low amplification as result of parasitic capacitance and conducting silicon substrate. Hence, to derive enough signal amplification and low noise contribution of a low noise amplifier using CMOS technology often involves high power consumption. How to provide enough gain in a low noise amplifier (LNA) suitable for a specific wireless communication system without consuming too much power is the main object of this thesis. In the thesis, two low noise amplifiers intended for the receiver path of 5.8-GHz wireless LAN and Ultra-Wideband System are analyzed, designed and implemented.

In the first one for narrow band application, popular inductive source degeneration architecture for the first stage of the LNA is replaced with Darlington pair combined with modified matching network. Under input matching condition, the Darlington pair acts as a current amplifier at the operating frequency to provide larger amplification compared to inductive source degeneration architecture under same dc current consumption.

In the second one for Ultra-Wideband system, the gain compensation method to derive flat gain over the entire frequency band is designed to redeem the tradeoff between gain,

bandwidth and power consumption. Also, a variable gain function between 3 and 8 GHz to enhance the dynamic range of the input signal is added to the second improved UWB LNA circuit.

1.2 Thesis Organization

In the Chapter 2 of the thesis, some theoretical MOSFET noise model and noise theory are introduced. Although these basic concepts provide a guidance to design a low noise amplifier, it is not enough to design a superior fully on-chip CMOS LNA including the consideration of some other important figure of merit such as gain, power consumption etc. . A systematic LNA design method associated with CMOS process is developed earlier [3] and represented in this chapter.

In the Chapter 3, a narrow band LNA using Darlington pair structure intended for application of the 5-GHz wireless LAN is introduced. The detailed circuit analysis and design equation is presented. Circuit simulation and comparison with single-ended inductive source degeneration topology are also discussed. Finally, measurement result of the LNA chip fabricated by TSMC 0.18um CMOS technology is discussed.

In the Chapter 4, a 3 to 8-GHz wideband amplifier intended for UWB system is proposed. The gain flatness technique using frequency compensation method to derive flat gain over the entire frequency band is introduced. The combination of negative feedback resistor and inductive source degeneration network is designed to achieve input matching. Also, some design consideration and trade-off is discussed. The measured data and simulation result of the circuit is compared and discussed. Finally, based on the measurement result of this chip, a second modified version is designed to achieve better performance. Also, the variable gain function is added to the circuit. In the last chapter, all the work is summarized and concluded.

Chapter 2

Low Noise Amplifier Basic Concepts

In this Chapter, some theoretical MOSFET noise model and noise theory are presented in section 2.1. Although these basic concepts provide a guidance to design a low noise amplifier, it is not enough to design a superior fully on-chip CMOS LNA including the consideration of some other important figure of merit such as gain, power consumption etc.. In section 2.2, a systematic narrow band LNA design method associated with CMOS process developed earlier [3] is discussed. Finally, some broadband LNA architecture is discussed in section 2.3

2.1 Noise in MOSFET

To develop good CMOS RF circuit design skills, a fundamental understanding of noise source in a MOSFET is necessary. Noise can be roughly defined as any random interference unrelated to the signal of interest, which can be sorted out interference noise and inherent noise. Interference noise results from interaction between circuit and outside world, or between different parts of the circuit itself. Interference noise can be reduced by carefully circuit layout and wire routing. On the other hand, inherent noise originates from the fundamental property of the circuit itself and it can be reduced but never eliminated. Inherent noise is only moderately affected by circuit layout, such as using multiple finger number to reduce the gate resistance of a MOSFET. However, inherent noise can be significantly reduced by proper circuit design, such as choosing circuit topology and increasing power consumption.

2.1.1 Source of Noise

In this section, we will focus on the inherent noise of a MOSFET, which can be categorized into three parts: drain noise, gate noise and Flicker noise, mainly.

2.1.1.1 Drain Noise

The dominant noise source in a MOSFET is the channel noise, which basically is a thermal noise originated from the voltage-controlled resistor mechanism of a MOSFET. Thus, one would expect noise commensurate with the resistance value. Indeed, detailed theoretically considerations lead to the following expression for the channel noise of a MOSFET, which is modeled as a shunt current noise "$\overline{i_{nd}^2}$"in the output current of the device, as shown in Fig.2.1:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \qquad (2\text{-}1)$$

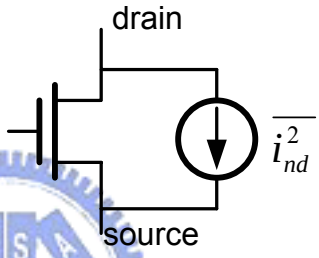


Fig.2.1 drain current noise model

Where g_{d0} is the zero-bias drain conductance of the device, and γ is a bias dependence factor. In long channel device, the value of parameter γ is unity at zero drain-source voltage, and decreased to 2/3 when device is saturated. Unfortunately, γ is much greater than 2/3 for short channel device operating in saturation. This excess noise is originated from carrier heating by large electric field in short channel device. This value would worsen the noise performance as the technology proceeds.

2.1.1.2 Gate Noise

In addition to channel noise, the thermal agitation of channel charge has another important consequence: gate noise. If the MOSFET are biased so that channel operates in the inverted condition, fluctuations in channel charge will induce physical current in the gate due to capacitive coupling. Although this noise can be neglected at low frequencies, it dominates

at radio frequencies. The companion effect of the gate noise that occurs at high frequencies arises due to its 'distributed' nature of the MOSFET. As operating frequency approaches cutoff frequency ω_t of a MOSFET, the gate impedance of the device exhibits a significant phase shift from it purely capacitive value at lower frequencies. This shift can be accounted for a real, noiseless conductance, g_g, in the gate current. Thus, the circuit model to represent the gate noise is the current noise connected between gate and source terminal shunted by a conductance g_g, as shown in Fig.2.2 (a). Van der Ziel [4] has shown that the gate noise may be expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \qquad (2\text{-}2)$$

where the parameter g_g

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$$

and the typical value of the coefficient of gate noise "δ", equal to 3/4 in long channel device while 4 to 6 in short channel one. The gate noise current clearly has a power spectral density that is not constant. In reality, gate noise increases as frequency increases, so it is often called "blue noise" to continue the optical analogy. For those who prefer not to analyze a system that has no blue noise source, it is possible to recast the model in a form with a noise voltage source that possesses a constant power spectral density. The alternative model can be derived first transform the parallel RC network into equivalent series RC network. If one assumes

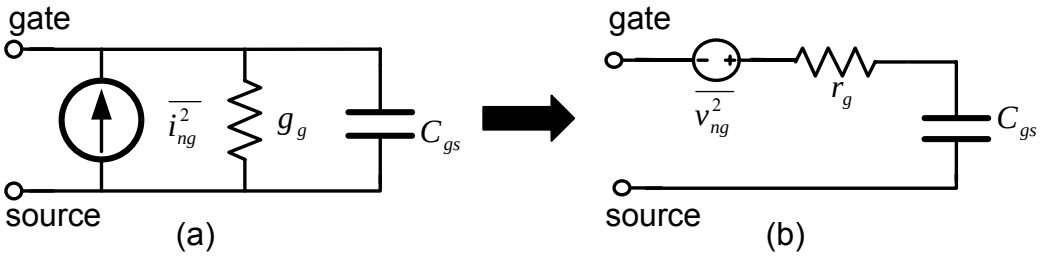


Fig.2.2 (a) Gate noise circuit model (b) its equivalent voltage noise source model

high Q of the network, then the capacitance C would roughly not change during the transformation, while the parallel resistance becomes a series resistance whose value is

$$r_g = \frac{1}{g_g} \cdot \frac{1}{Q^2+1} \approx \frac{1}{g_g} \cdot \frac{1}{Q^2} = \frac{1}{5g_{d0}} \tag{2-3}$$

which is independent of frequency. Finally, equate the short circuit currents of the original network and the transformed version, the equivalent voltage noise source is then found to be

$$\overline{v_{ng}^2} = 4kT\delta r_g \Delta f \tag{2-4}$$

which possesses a constant power spectral density. Hence, the final noise model contains a voltage noise source in series with a equivalent resistance whose value is not dependent on the frequency as shown in Fig.2.2(b).

Because the two noise source do share a common origin, they are also correlated, that is, there is a component of the gate noise current that is proportional to the drain current on an instantaneous basis. The correlation between gate and drain noise can be expressed mathematically as follows [4]:

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} = 0.395j \tag{2-5}$$

where the value of 0.395j is exact for long channel devices. The correlation can be treated by expressing the gate noise as the sum of the two components, the first of which is fully correlated with the drain noise, and the second of which is uncorrelated with the drain noise. Hence, the gate noise is re-expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g(1-|c|^2)\Delta f + 4kT\delta g_g |c|^2 \Delta f \tag{2-6}$$

where the first term is uncorrelated and the second term is correlated to drain noise. Because of the correlation, special attention must be paid to the reference polarity of the correlated component. The value “c” is positive for the polarity shown in Fig.2.2 (a)

2.1.1.3 Flicker Noise

Charge trapping and releasing by the defects and impurities on the interface between thin oxide and channel are usually invoked to explain the flicker noise (1/f noise). Since a MOSFET is surface device, it would exhibit more 1/f noise than bipolar device. One means of comparison is to specify a 'corner frequency', where the flicker noise is equal to the thermal noise. A lower corner frequency means less total noise. In RF circuit design, it is not important to care about flicker noise in bipolar devices, whose corner frequency often below tens or hundreds of hertz, while MOSFET often exhibit 1/f corners of tens of kilohertz to a megahertz or more. For a MOSFET, the 1/f noise can be represented by a drain current noise connected between drain and source terminal as shown in Fig2.3, and its value is

$$\overline{i_{1/f}^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f \qquad (2\text{-}7)$$

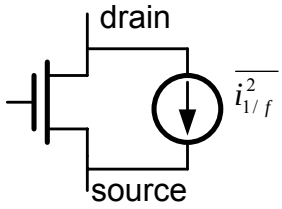


Fig.2.3 Flicker noise model

where "A" is the area of the gate(=WL) and K is a device-specific constant. For NMOS device, K is typically about 10-28 C^2/m^2, whereas for PMOS devices it is about 50 times larger. From the first equation above, one can observe that larger dimension size and thinner dielectric exhibit less 1/f noise, because larger gate capacitance smoothes the fluctuations of the channel charge. For the second equation, one can see the 1/f would worsen as technology proceeds because of the positive proportional dependence on the cutoff frequency (ω_t).

2.1.2 Noise Models of the MOS Transistors

From previous introduction of noise source, a standard MOSFET noise model is

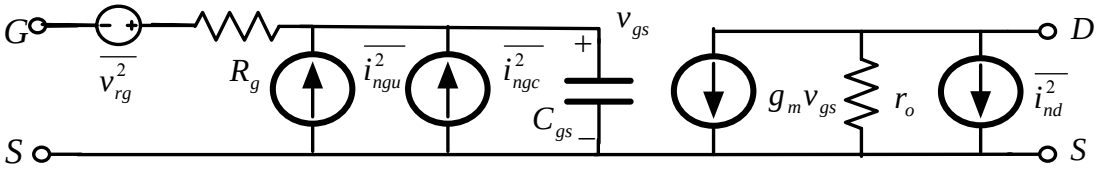


Fig.2.4(a) MOSFET noise model

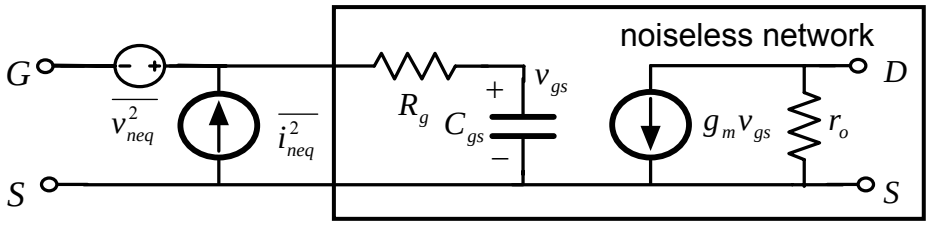


Fig.2.4 (b) equivalent input referred noise model

presented in Fig.2.4. In Fig.2.4 (a), $\overline{i_{nd}^2}$ is the drain current noise, and $\overline{i_{ng}^2}$ is the gate current noise, which is separated into correlated ($\overline{i_{ngc}^2}$) and uncorrelated ($\overline{i_{ngu}^2}$) terms. Also, $\overline{v_{rg}^2}$ is added to represent the noise originated from the parasitic resistor of gate terminal, which may be due to the gate resistor of the device or the parasitic resistor of the input inductor. Also, we have neglected the effect of g_g under the assumption that the gate impedance is largely capacitive at the frequency of interest. Here, the noise model also can be represented as a noiseless network together with two equal noise sources ($\overline{v_{eq}^2}$ and $\overline{i_{eq}^2}$) in Fig.2.4 (b). The relationship between two equivalent models is as follows

$$\overline{v_{neq}^2} = \overline{v_{Rg}^2} + \overline{i_{ng}^2}\cdot R_g^2 + \frac{\overline{i_{nd}^2}}{g_m^2}\cdot(1+\omega^2 C_{gs}^2 R_g^2) \tag{2-7}$$

$$= 4kT(R_g^2 + \delta g_g R_g^2 + \frac{\gamma g_{d0}}{g_m^2}\cdot(1+\omega^2 C_{gs}^2 R_g^2))\Delta f$$

$$\overline{i_{neq}^2} = \overline{i_{ngc}^2} + \overline{i_{ngu}^2} + \frac{\overline{i_{nd}^2}}{g_m^2}\cdot\omega^2 C_{gs}^2 = 4kT(\delta g_g + \frac{\gamma g_{d0}}{g_m^2}\cdot\omega^2 C_{gs}^2)\Delta f \tag{2-8}$$

2.2 Low Noise Amplifier Basic

In this section, we discuss some LNA architecture, and introduce the most popular architecture, inductive source degeneration topology [3].

2.2.1 Low Noise Amplifier Topology and Basic

In the design of low noise amplifiers, there are several common goals. These include minimizing the noise figure of the amplifier, providing gain with sufficient

linearity—typically measured in terms of the third-order intercept point, IP3—and providing a stable 50Ω input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier. A good input match is even more critical when a pre-select filter precedes the LNA because such filters are often sensitive to the quality of their terminating impedances. The additional constraint of low power consumption which is imposed in portable systems further complicates the design process.

The first work of designing LNA circuit is to provide stable input impedances. Here, the four basic architectures are illustrated in simplified form in Fig 2.5. Each of these architectures may be used in a single-ended form, or in a differential form. Note that differential form will require the use of a balun or similar element to transform the single-ended signal from the antenna into a differential signal. Practical baluns introduce extra loss which adds directly to the noise figure of the system.

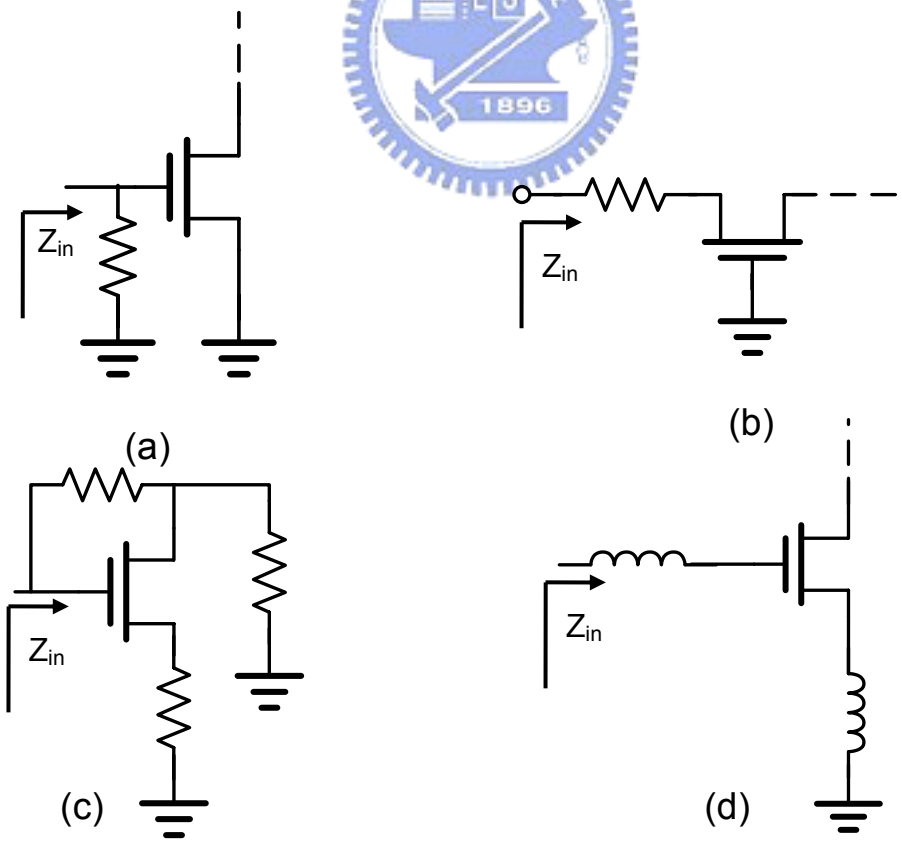


Fig.2.5 Common LNA architecture (a) Resistive termination (b) 1/gm termination (c) shunt-series feedback, and (d) inductive degeneration

The first technique uses resistive termination of the input port to provide a 50Ω impedance. There are two effects to degenerate the noise performance of the amplifiers. First, the added resistor contributes its own noise to the output which equals to the contribution of the source resistance. Second, the input is attenuated by the added input resistance. The larger noise penalty resulting from these effects therefore makes this architecture unattractive for the more general situation where a good input termination is desired. A second approach uses the source of the common-gate stage as the input termination, is shown in Fig 2.5(b). A simplified analysis of the common-gate architecture, assuming matched conditions, yield the following lower bounds on noise factor for the cases of and CMOS amplifiers

CMOS: $$F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} = 2.2(\text{dB})$$

where the γ is the coefficient of the channel thermal noise and α is the ratio of the device trans-conductance g_m and zero-bias drain conductance g_{d0} . In the short-channel device, α is smaller than one and γ is greater than one due to hot electrons in the channel. Above the previous analysis, the minimum theoretically achievable noise figure tend to be around 2.2dB or greater practically.

The third architecture of the amplifiers is shunt-series feedback, as illustrated in Fig 2.5(c). In this topology, input-matching and output-matching network can be achieved by using shunt and series feedback resistances. However, the amplifiers using that shunt-series feedback usually have high power dissipation compared to other types of low noise amplifiers. The higher power consumption is partially owing to the fact that shunt-series amplifiers are wideband ones. In many applications, such as GPS, GSM, a wideband front end is not required and it is able to make use of the narrowband structure to reduce power. For this reason, the shunt-series feedback method is not applied in the narrow band design. The Forth architecture utilizes inductive source degeneration impedance as represented in Fig 2.5(d) to generate a real term in the input impedance. The narrow band matching can get good power

performance as well as better tuning of the input matching of amplifiers. This technique is not only used in the narrow-band wireless communications, such as GPS or GSM receivers, but also employed for ultra-wideband system, which we will introduce in Chapter 4. In the following section, the discussion of low noise amplifier will focus on the inductive source degeneration structure.

2.2.2 Inductive Source Degeneration LNA

In 1997, Thomas H. Lee and Derek K. Shaeffer suggested a popular method to optimize the noise performance of the inductive source degeneration (ISD) LNA [3]. In the section, the noise optimization on the inductive degeneration topology under gain and power constraint is discussed.

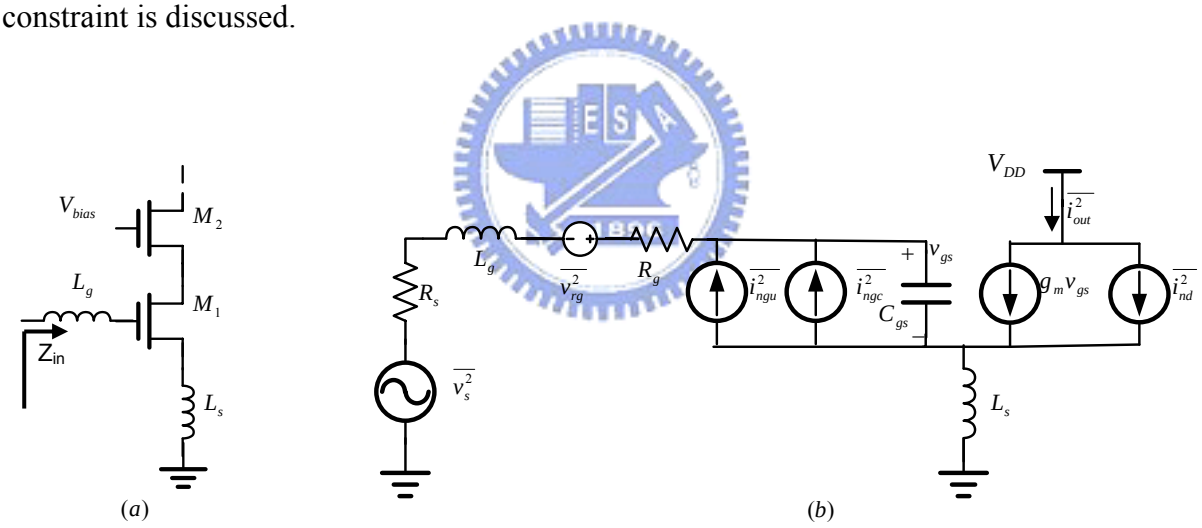


Fig.2.6 (a) Common source input stage (b) input stage of ISD LNA noise model

2.2.2.1 Operational Basic and noise figure calculation

Selecting the first stage of a LNA is a very important thing for obtaining good noise and input matching. The topology of the cascode LNA with ISD and the equivalent circuit for input stage noise calculation are shown in Fig 2.6(a) and Fig 2.6(b). In Fig 2.6(a), the input impedance of the cascode amplifier is represented by

$$Zin = s(L_g + L_s) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s$$
$$= \omega_T L_s \qquad (\omega = \omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}}) \tag{2-9}$$

where we obtain the input impedance Z_{in} is equal to the multiplication of cutoff frequency of the device and source inductance at resonant frequency, this value will be set to 50Ω for input matching. In Fig 2.6(b), R_g represents the series resistance of the inductor as well as the gate resistance of the NMOS device, and $\overline{i_{nd}^2}$ represents the channel thermal noise of the device, while the $\overline{i_{ngc}^2}$ and $\overline{i_{ngu}^2}$ are the gate noise with correlated and uncorrelated term. Here, analysis based on this circuit neglects the contribution of subsequent stages to the amplifier noise figure. This simplification is justifiable provided that the first stage possesses sufficient gain and permits us to examine in detail the salient features of this architecture. Then recall the noise figure for a circuit is defined as:

$$NF = \frac{Total\_output\_noise}{Total\_output\_noise\_from\_the\_source} \tag{2-10}$$

To find the output noise, we first evaluate the trans-conductance of the input stage. With the output current proportional to the voltage on C_{gs} and nothing that the input circuit takes the form of series-resonant network, the trans-conductance at the resonant frequency is given by

$$G_m = g_m Q_{in} = \frac{g_m}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_0 R_s} \tag{2-11}$$

where Q_{in} is the effective Q of the amplifier input circuit. From this equation, the output noise power density due to the source is

$$S_{a,srce}(\omega_0) = S_{src}(\omega_0)G_{m,eff}^2 = \frac{4kT\omega_T^2}{\omega_0^2 R_s(1 + \frac{\omega_T L_s}{R_s})^2} \tag{2-12}$$

In a similar way, the output noise power density due to R_g can be expressed as

$$S_{a,R_g}(\omega_0)=\frac{4kTR_g\omega_T^2}{\omega_0^2R_s^2(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-13}$$

Next, the noise power density associated with the correlated portion of the gate noise and drain noise can be expressed as

$$S_{a,i_d,i_g,c}(\omega_0)=\frac{4kT\gamma\kappa g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-14}$$

where

$$\kappa=\left[1+|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2+\frac{\delta\alpha^2}{5\gamma}|c|^2$$

$$Q_L=\frac{1}{\omega_0 R_s C_{gs}}$$

$$\alpha=\frac{g_m}{g_{d0}}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise. This contributor has the following power spectral density:

$$S_{a,i_d,u}(\omega_0)=\xi S_{a,i_d}(\omega_0)=\frac{4kT\gamma\xi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-15}$$

where $\xi=\frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q_L^2)$

We observe that the equation (2-14) and (2-15) can all proportional to the power spectral density of drain current noise, then the two equation can be combined as a simplified form:

$$S_{a,M_1}(\omega_0)=\frac{4kT\gamma\chi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-16}$$

where χ is defined as

$$\chi=1+2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{\delta\alpha^2}{5\gamma}(1+Q_L{}^2)$$

According to (2-10), (2-13) and (2-16), the noise figure at the resonant frequency can be written by the following equation:

$$NF = \frac{S_{a,source}(\omega_0) + S_{a,R_g}(\omega_0) + S_{a,M_1}(\omega_0)}{S_{a,source}(\omega_0)} = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \quad (2\text{-}17)$$

To understand the implications of this new expression for F, we observe that χ includes terms which are constant, proportional to Q_L, and proportional to Q_L^2. It follows that (2-17) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. Therefore, a minimum F exits for a particular Q_L.

2.2.2.2 Optimizations of LNA Design Flow

So far, we have analyzed the noise performance of the input stage of an inductive source degeneration topology. This analysis can now be drawn upon in designing the LNA. Besides noise performance, gain and power dissipation are another important considerations in LNA circuit design. In this subsection, how to pick the appropriate device width and bias point to optimize noise performance given specific objectives for gain and power dissipation is our goal.

To quantify these terms, a simple second-order model of the MOSFET trans-conductance can be employed which accounts for high-field effects in short channel devices. Assume that drain current I_d has the form

$$I_d = WC_{ox}v_{sat}\frac{(V_{gs} - V_T)^2}{(V_{gs} - V_T) + L\varepsilon_{sat}} \quad (2\text{-}18)$$

where C_{ox} is the gate oxide capacitance per unit area, ν_{sat} is the saturation velocity, and ε_{sat} is the velocity saturation field strength. To simplify the following analysis, (2-18) can be reformulated as

$$I_d = WC_{ox}v_{sat}\frac{\eta^2}{1-\eta} \quad (2\text{-}19)$$

where we define $\eta = \dfrac{V_{gs} - V_T}{(V_{gs} - V_T) + L\varepsilon_{sat}}$

Because the device M1 must operate in saturation region, the range of overdrive should be within:

$$0 \le V_{gs} - V_T \le V_{ds} \tag{2-20}$$

Hence, the parameter η should be within the range

$$0 \le \eta \le \frac{V_{ds}}{V_{ds} + L\varepsilon_{sat}} \tag{2-21}$$

Having established an expression for I_d, we can formulate the power consumption of the amplifier as follows:

$$P_D = V_{dd} I_d = V_{dd} W C_{ox} v_{sat} \frac{\eta^2}{1-\eta} \tag{2-22}$$

To differentiate (2-18), we can determine the trans-conductance of device M1

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = W C_{ox} v_{sat} (2\eta - \eta^2) \tag{2-23}$$

From (2-22), we can derive the cutoff frequency of the device M1

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{3v_{sat}[-(\eta-1)^2 + 1]}{2L} \tag{2-24}$$

Here, we have assumed that gate-source capacitance is equal to $(2/3)WLC_{ox}$, and the gate-drain capacitance(C_{gd}) have been neglected. Substituting (2-23) into (2-11) gives

$$G_m = \frac{3v_{sat}}{4L\omega_0 R_s}[-(\eta-1)^2 + 1] \tag{2-25}$$

This expression shows that the trans-conductance of the input stage is only dependent on the bias condition and frequency of operation given specific technology and source resistance, while the power dissipation not only depend on bias condition but also on the gate width of device M1 as shown in (2-22).

Finally, substituting (2-24) into (2-17) gives

$$F = 1 + \frac{R_g}{R_s} + \frac{mW + \frac{n}{W} + I}{-(\eta - 1)^2 + 1} \tag{2-26}$$

where $m = \frac{4\gamma L^2 C_{ox}}{9\alpha v_{sat}}(\omega_0{}^2 R_s)(1 + \frac{\delta\alpha^2}{5\gamma})$

$$n = \frac{\delta\alpha}{5R_s C_{ox} v_{sat}}$$

$$I = \frac{4\gamma^2 \omega_0 L|c|}{3\alpha^2 v_{sat}}$$

The expression shows that a minimum F exits for a particular width W, and the higher the bias point, the lower the F.

There are two approaches to this optimization problem which deserve special attention. The first assumes a fixed trans-conductance, G_m, for the amplifier. The second assumes fixed power consumption. Now, we review the two different conditions using the equation we have developed.

1) *Fixed G_m optimization*: To fix the value of the trans-conductance, Gm, we need only assign a constant value to η. Once η is determined, we can minimize the noise factor by taking

$$\frac{\partial F}{\partial W} = 0 \tag{2-27}$$

which, after some algebraic manipulations, results in

$$W_{opt,Gm} = \sqrt{\frac{n}{m}} = \frac{3}{2\omega_0 R_s L C_{ox}} \cdot \sqrt{\left(1 + \frac{5\gamma}{\delta\alpha^2}\right)^{-1}} \tag{2-28}$$

The optimal width will gives the minimal noise factor given that bias condition has been determined by G_m. Finally, the power consumption is determined by the optimal width and bias condition. In this approach, the main advantage is that designer can choose the trans-conductance of input stage arbitrary to achieve high gain and low noise performance.

The disadvantage is that we sacrifice the power consumption to achieve noise performance.

2) *Fixed P_D Optimization*: An alternative method of optimization fixes the power dissipation and adjusts width, W, and bias point, ρ, to minimize the noise factor. Under fixed power consumption P_D, we re-express noise factor as:

$$F = 1 + \frac{[i\frac{1-\eta}{\eta^2} + j\frac{\eta^2}{1-\eta} + l]}{-(\eta-1)^2 + 1} \tag{2-29}$$

where $i = \frac{P_D}{v_{sat}E_{sat}V_{DD}} m = \frac{4\gamma L^2 C_{ox}}{9\alpha v_{sat}^2 E_{sat}}(\omega_0{}^2 R_s)(1+\frac{\delta\alpha^2}{5\gamma})\frac{P_D}{V_{DD}}$

$$j = \frac{V_{DD}LE_{sat}}{P_D} n = \frac{\delta\alpha V_{DD}LE_{sat}}{5R_s P_D}$$

$$l = \frac{4\gamma^2\omega_0 L|c|}{3\alpha^2 v_{sat}}$$

after some algebraic manipulations by taking $\frac{\partial F}{\partial \eta} = 0$, results in

$$\eta_{opt} = \sqrt{\frac{1+\sqrt{l^2+12ij}}{2j}} \tag{2-30}$$

$$W_{opt} = \frac{P_D}{V_{dd}C_{ox}v_{sat}}\frac{1-\eta_{opt}}{\eta_{opt}^2} \tag{2-31}$$

where we have assumed $\eta << 1$**.**Given fixed power constraint, the minimal noise factor is determined by (2-30) and (2-31). Finally, the Gm has been designed under the optimal bias condition, η_{opt}.

In this approach, the main advantage is that designer can specify the power dissipation and find the optimal low noise performance. The disadvantage is that the trans-conductance of the input stage is held up by the optimal noise condition.

From (2-11) and (2-17), we found that the cutoff frequency of the input device determine the gain and noise performance of the inductive source degeneration LNA. As CMOS process technology continues to improve, the higher gain and lower noise

performance may be expected. Now, device cutoff frequency, f_T, is bounded within any given technology, so it would seem that once biasing conditions that maximize f_T have been established, the designer has done all that can be done. However this facile conclusion overlooks the possibility of topological routes to increasing f_T. In chapter Ⅲ, an alternative inductive source degeneration LNA using Darlington pair input stage to double f_T is discussed and implemented.

2.2.3 Introduction to Broadband LNA

Ultra wideband (UWB) systems are a newly wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates. Although the UWB standard (IEEE 802.15.3a [5]) has not been completely defined, most of the proposed applications are allowed to transmit in a band between 3.1 and 10.6 GHz. How to design a low noise amplifier suitable for the receiver path of the UWB system becomes a challenge for RF circuit designer. In general, this type of amplifier would have constant gain and good input matching over the desired frequency bandwidth, and provide low enough noise figure while consuming power as little as possible.

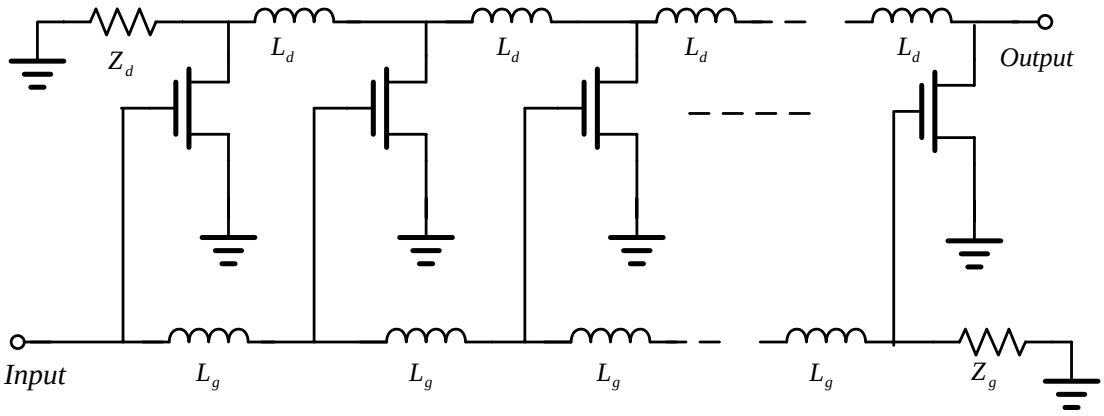


Fig.2.7 Configuration of an N-stage distributed amplifier

With recent advances in RF integrated circuit and device processing technology,

distributed amplifiers (DAs) were widely used to realize broadband amplifier [6-8]. The basic configuration of DAs is shown in Fig 2.7. A cascade of N identical FETs have their gates connected to a series inductors, L_g , while the drains are connected to a series inductors, L_d. The combination of gate-source capacitance(C_{gs}) of each device and the series inductors, L_g, forms a approximate transmission line with characteristic impedance Z_g' ($\sqrt{L_g / C_{gs}}$) equal to Z_g. If the Z_g is equal to 50Ω, the approximate transmission line will give good input matching to 50Ω. In the same way, the output matching will be achieved. In amplification aspect, the input signal propagates down the gate line, with each FET tapping off some of the input power. The output signals amplified by the trans-conductance of FETs form a traveling wave on the drain line. The inductors (L_d's) are chosen for constructive phasing of the output signals, and the termination impedances on the lines serve to absorb waves traveling in the reverse directions [9].

In CMOS technology, Bandwidths extending to tens of giga-hertz of DAs are possible, with good input and output matching. Distributed amplifiers can not achieve very high gains or very low noise figure, however, and generally are larger in size because of many on-chip inductors. The main drawback on the DAs is that power consumption is generally large owing to several stages cascaded to derive an adequate gain level. Also, the bandwidth of the DAs basically is a low pass filter, whose excess amplification below 3.1 GHz would distort the wanted signal for ultra-wideband application.

An alternative approach to the design of broadband amplifiers is to use negative feedback [10]. One particularly useful broadband circuit that employs negative feedback is the shunt-series amplifier as shown in Fig 2.8. With the assistance of negative feedback resistor, the R_{in} and R_{out} can be matched to 50 easily in low frequency. Formally, R_{in} and R_{out} is given by

$$R_{in} = \frac{R_E(R_F + R_L)}{R_E + R_L} \qquad (2\text{-}32)$$

$$R_{out} = \frac{R_E(R_F + R_S)}{R_E + R_S} \qquad (2\text{-}33)$$

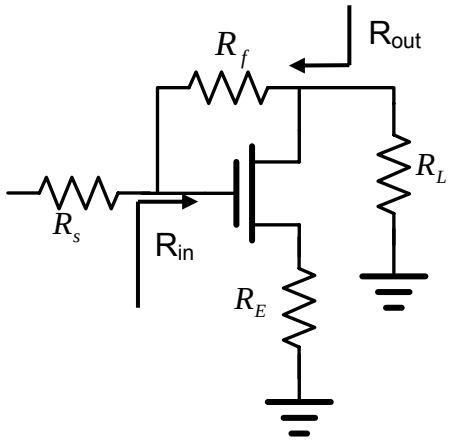


Fig.2.8 Configuration of shunt-series amplifier

Comparing the expressions for input and output resistance, we see that if R_s and R_L are equal (as is commonly the case) then R_{in} and R_{out} will also be precisely equal. This happy coincidence is one reason for the tremendous popularity of this topology. Unfortunately, the presence of gate-source capacitance, C_{gs} , and Miller-augmented gate-drain capacitance, C_{gd} , which appear between gate and ground, makes it impossible to achieve perfect input impedance matching at high frequency. These effects can be mitigated to a certain extent by using L-match network to transform the resistive part up to the desired level. Of the possible types of L-matches, the best choice is usually one that places an inductance in series with the gate and a shunt capacitance across the amplifier input; such a network becomes transparent at low frequencies, where no correction is required. After some assumption and calculation, we can derive the relationship between voltage and bandwidth:

$$BW \cdot |A_v| \approx \left(\frac{C_{gs}}{g_m} + \frac{R_s C_{gd}}{2} \right)^{-1} \qquad (2\text{-}34)$$

This topology trades gain for bandwidth, so amplifier bandwidths in excess multi-gigahertz using CMOS technology are possible at the expense of gain and noise figure.

From previous discussion, we found that a broad band amplifier generally suffers from two problems: low gain and power hungry. The first problem would degrade noise performance on the following stage in the receiver path, and the second one would not be

suitable for general portable device. In section 2.2.2, we have known that inductive source degeneration architecture possess near-optimum noise performance [3], and high gain potential in term of cutoff frequency of input MOS device, while dissipating less power than broad band amplifier. In Chapter 4, we will utilize these advantages of inductive source degeneration combined with the resistive feedback technique to design a wideband amplifier suitable for the UWB system.

CHAPTER 3

5.5 GHz High Gain LNA Using Darlington Pair

3.1 Motivation

We have introduced the inductive source degeneration topology to design LNA in section 2.2.2. From (2-11) and (2-17), we found that the cutoff frequency of the input device determines the gain and noise performance of the inductive source degeneration LNA. As CMOS process technology continues to improve, the higher gain and lower noise performance may be expected. Now, device cutoff frequency, f_T, is bounded within any given technology, so it would seem that once biasing conditions that maximize f_T have been established, the designer has done all that can be done. However this facile conclusion overlooks the possibility of topological routes to increasing f_T. In this chapter, an alternative inductive source degeneration LNA using Darlington pair input stage to increase f_T is analyzed and implemented.

3.2 Analysis of Darlington Pair LNA Topology

3.2.1 Design principle

In section 2.2.2, we have derived the trans-conductance of an inductive source degeneration LNA input stage as shown in (2-11). Now, we rewrite and reconsider this equation.

$$G_{m,M1} = g_m Q_{in} = \frac{g_m}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_0 R_s} \tag{3-1}$$

we can reformulate this equation as

$$G_{m,M1} = \frac{g_m}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{\omega_0 (R_s + Z_{in})} = \frac{\beta}{R_s + Z_{in}} \quad (\omega = \omega_0) \tag{3-2}$$

where β is the current gain of the input stage, which is proportional to the cutoff frequency

of the input device and inverse proportional to the frequency of operation, and the Z_{in} is the input impedance of the input stage. Eq.(3-2) stands for the trans-conductance of the input stage is proportional to the current gain itself at the operating frequency under input matching condition. In other words, the input stage acts as a current amplifier at the frequency of operation. If we can increase the current gain of the input stage without changing the input matching condition, we will get larger trans-conductance to derive more gain and suppress noise of the subsequent stage at the operating frequency.

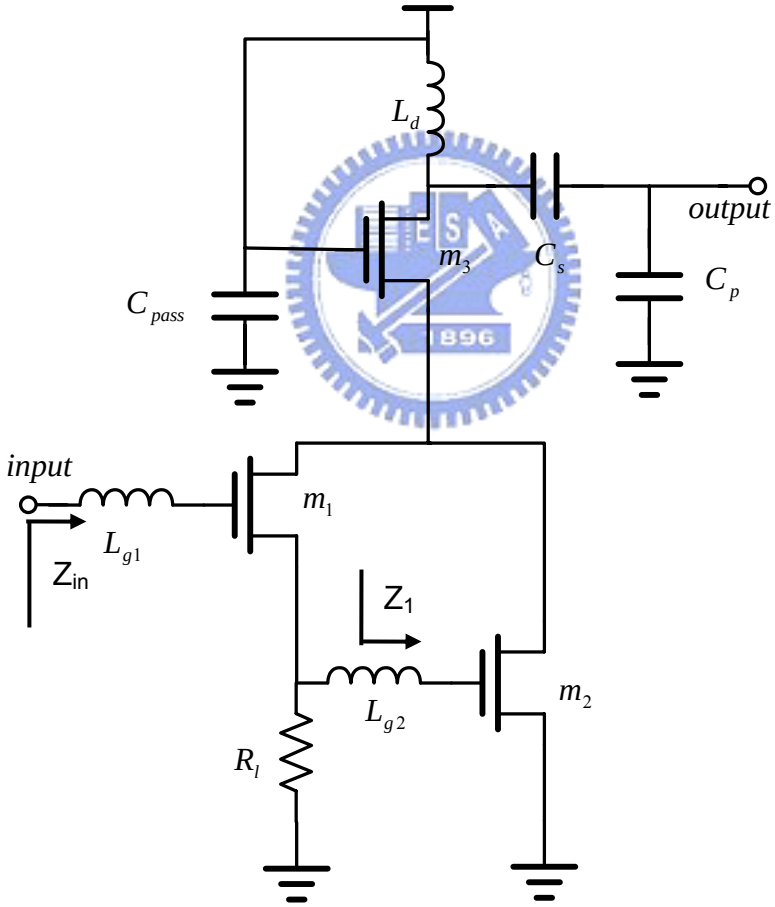


Fig 3.1 Schematic of Darlington pair low noise amplifier

3.2.2 Analysis and Design of the LNA using Darlington Pair

Because Darlington pair has approximate double cutoff frequency [10], it means that Darlington pair has larger current gain. Now, the Darlington pair topology has been employed to replace the input stage of our designed LNA circuit as shown in Fig 3.1. The L_{g1} and L_{g2} are designed to achieve input matching, and cascode common-gate device m2 for less Miller's effect and better reverse isolation. The resistor, R_l, is designed for biasing. Because the value of R_l is large enough compared to Z_1 at operating frequency, the bias resistor would not affect the normal operation of the Darlington Pair. Also, L_{d1}, C_s and C_p are designed for output matching, while C_{pass} for local small signal ground.

3.2.2.1 Trans-conductance in Darlington Pair Stage

To analyze the trans-conductance of input stage, we neglect the contribution of subsequent stages and the overlap capacitance C_{gd}. The use of a cascoded first stage helps to ensure that this approximation will not introduce serious errors. After some small signal calculation, the trans-conductance of the Darlington pair at operating frequency gives

$$G_{DAR} = \left| -\left(\frac{g_{m1}g_{m2}}{2Z_s\omega_0{}^2 C_{gs1}C_{gs2}} \right) - j\left(\frac{g_{m1}C_{gs2} + g_{m2}C_{gs1}}{2Z_s\omega_0 C_{gs1}C_{gs2}} \right) \right| \approx \frac{\sqrt{\left(\frac{\omega_{t1}\omega_{t2}}{\omega_0{}^2} \right)^2 + \left(\frac{\omega_{t1}+\omega_{t2}}{\omega_0} \right)^2}}{2Z_s} \quad (3\text{-}3)$$

where the ω_{t1} and ω_{t2} are the cutoff frequency of the m_1 and m_2 devices, respectively. Also, we have assumed input impedance matching to R_s.

To compare the trans-conductance of the Darlington pair and a single device, (3-1) and (3-3) were combined as

$$M = \frac{G_{DAR}}{G_m} = \sqrt{\left(\frac{\omega_{t1}\omega_{t2}}{\omega_t\omega_0} \right)^2 + \left(\frac{\omega_{t1}+\omega_{t2}}{\omega_t} \right)^2} \quad (3\text{-}4)$$

where the M means the profit using Darlington pair compared to single device.

To gain more insight of the profit, we consider the following case. If we roughly assumed that $\omega_T \propto \sqrt{P_D}$ and $\omega_{T1} = \omega_{T2} = \frac{\omega_T}{2}$, we can derive the following result

$$G_{DAR} \approx 1.8 G_m \quad \text{and} \quad P_{D(\text{darlington})} = \frac{P_D}{2} \tag{3-5}$$

where we have assumed the frequency of operation is 5 GHz, and the cutoff frequency (ω_T) is 30 GHz, a typical value in 0.18um CMOS process. More detailed will be simulated in Section 3.3.1.

3.2.2.2 Input impedance matching

The configuration of inductive source degeneration topology provides impedance matching to 50Ω with the help of source inductor (L_s). To derive input matching to 50Ω in the Darlington pair topology, an inductor L_{g2} is inserted between the source of the device m_1 and the gate of the device m_2 as shown in Fig 3.1. A portion of L_{g2} (L_t) is designed to tune out the gate-source capacitance of device m2, while the remainder serves as the inductive source degeneration inductor (eq. L_s) of device m1 for input matching. The analysis is shown as follows

$$\begin{aligned} Z_1 &= sL_{g2} + \frac{1}{sC_{gs2}} = s(L_t + L_s) + \frac{1}{sC_{gs2}} \\ &= sL_s \quad (\text{at resonance}) \end{aligned} \tag{3-6}$$

$$\begin{aligned} Z_{in} &= sL_{g1} + \frac{1}{sC_{gs1}} + Z_{in2} \\ &\approx \omega_T L_s \quad (\text{at resonance}) \end{aligned} \tag{3-7}$$

3.3 Discussion on Simulation and Measurement Result

3.3.1 Verification of Equation (3-4)

The 0.18um RF CMOS model provided by the TSMC is employed to simulate and verify the validity of equation (3-4). Here, we have assumed the drain current of device m1 and m2 are one half of that of the single device. In other words, the total current consumed by Darlington pair is equal to that of a single device. Now, we find out the cutoff frequency of every device (m_1, m_2 and M_1) under the specified bais condition, the result is shown in Fig 3.2. Finally, we substitute the cutoff frequency for the (3-4), and compared it to the simulated result, as shown in Fig 3.3. The calculation result of (3-4) agrees well with the simulated result. Thus, the validity of (3-4) is verified. Also, we find under the same current consumption the trans-conductance of Darlington pair is 1.5 to 6 times larger than a single device. This means, we can use the Darlington pair to derive larger trans-conductance without dissipating too much power compared to a single device.

In previous verification, we have assumed the output load of the input stage is zero. Unfortunately, the cascoded stage still hold low input impedance, this would degrade the trans-conductance of the input stage due to Miller effect. Because the Darlington pair has larger trans-conductance, it would result in larger voltage gain from output to the input compared to the single device under the same cascoded input impedance. In Fig 3.4, we saw the trans-conductance degradation of Darlington pair is larger than that of single device due to Miller effect. Here, we have assumed the cascoded stage is an ideal current buffer with a low impedance 20Ω (a typical value of 0.18um NMOS) and the output of the cascoded stage has been matched to 50Ω.

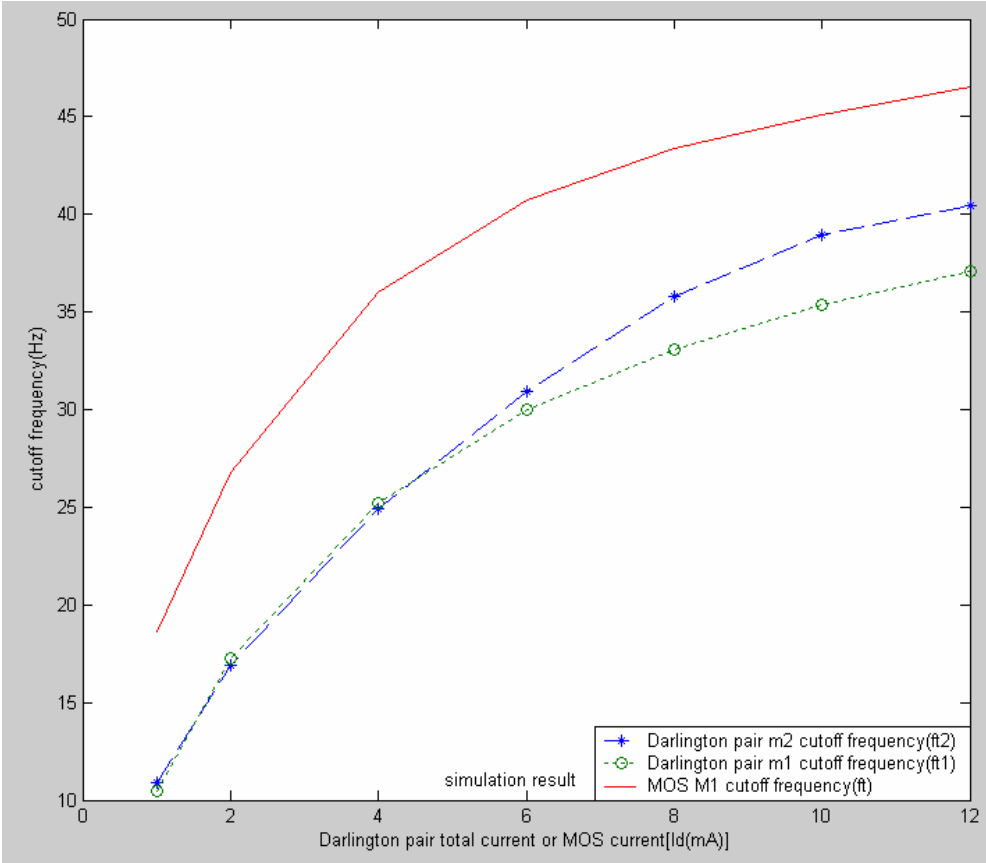


Fig 3.2 Cutoff frequency of device m_1, m_2 and M_1 versus drain current

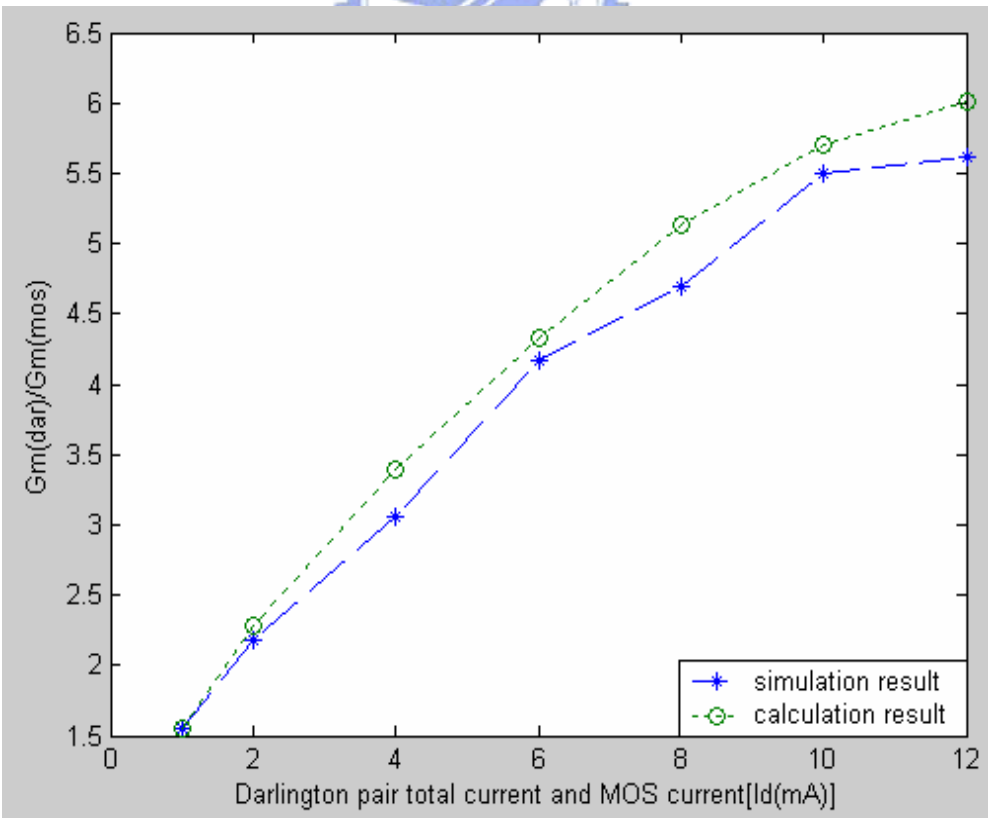


Fig 3.3 Profit (M) versus total current of input stage

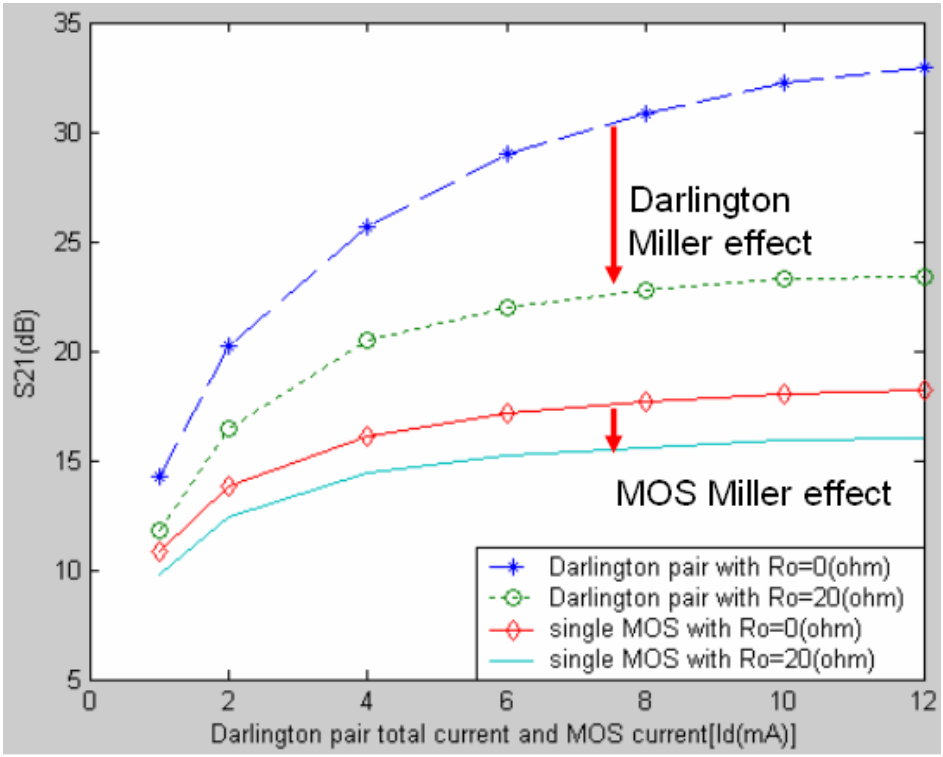


Fig 3.4 Influence of miller effect on the S_{21}

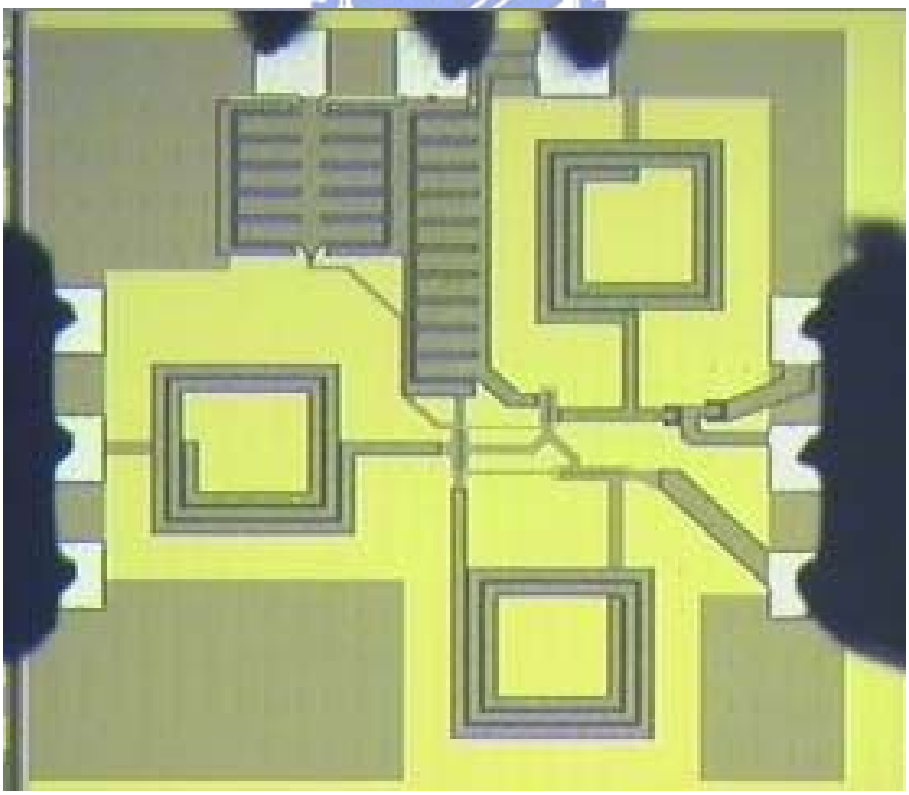


Fig 3.5 Microphotograph of the Darlington pair LNA circuit

3.3.2 Chip Implementation

Fig 3.5 shows the microphotograph of the Darlington pair LNA circuit. The circuit is fabricated in the TSMC 0.18um CMOS technology. The die area including bonding pads is 0.89 mm by 0.87 mm. Careful layout is observed in order to maximize performance. The layout is done in a uni-directional fashion, i.e. no signal returns close to it origins, to avoid coupling back to the input. The RF input and output ports are placed on opposite sides of the chip to improve port-to-port isolation. Since on-chip probing is used to measure the LNA's performance, standard Ground-Signal-Ground (GSG) configuration is used at both the input and output RF ports. In order to minimize the effect of substrate noise on the system, a solid ground plane, constructed using a low resistive metal-1 material, is placed between the signal pads (metal-6 and metal-5) and the substrate. Also, since the operation of inductors involves magnetic fields, they can affect nearby signals and circuits, and cause interference. Therefore, inductors are placed far apart from each other, as well as from the main circuit components, with reasonable distances. Furthermore, many ground connections to substrate are located near all inductors to reduce substrate noise.

3.3.3 Simulation and Measurement Result

Measured S-parameters are plotted in Fig. 3.6, 3.7 and 3.8, together with simulation results for comparison. The circle plot is the simulation result by using inductor model provided by the TSMC model file, and the triangle plot is the one by using inductor together with passive interconnection analyzed by the electromagnetic simulation tool of Agilent MOMENTUM. The solid line is the measured data. The measured power gain achieves the maximum value of 15.5dB at 6GHz, and input return ratio reaches -19dB at 6.2 GHz. The measured data drift to higher frequency may be due to the inaccurate inductor modeling, and all the S-parameter show the consistent trend. The square plot is the MOMENTUM

simulation minus ten percent of inductance of every inductor for trouble shotting. After trouble shotting, the simulated curve agree well to the measured date. Thus, we attribute the drift to that the realistic inductance of the inductor is smaller than the inductor modeling. Fig 3.9 shows the minimum noise figure is 3.5dB at 5.8GHz. Also, Linearity analysis is conducted by the two-tone test. Measured at 6 GHz, the two-tone test results of the third-order inter-modulation distortion are plotted in Fig. 3.10. The IIP3 is -6dBm and the 1-dB compression point -15dBm. The total power of the LNA circuit dissipates 11mW with a power supply 1.8V. TABLE I summarizes the performance of the Darlington pair LNA and comparison with general inductive source degeneration topology simulated by TSMC 0.18um CMOS model.

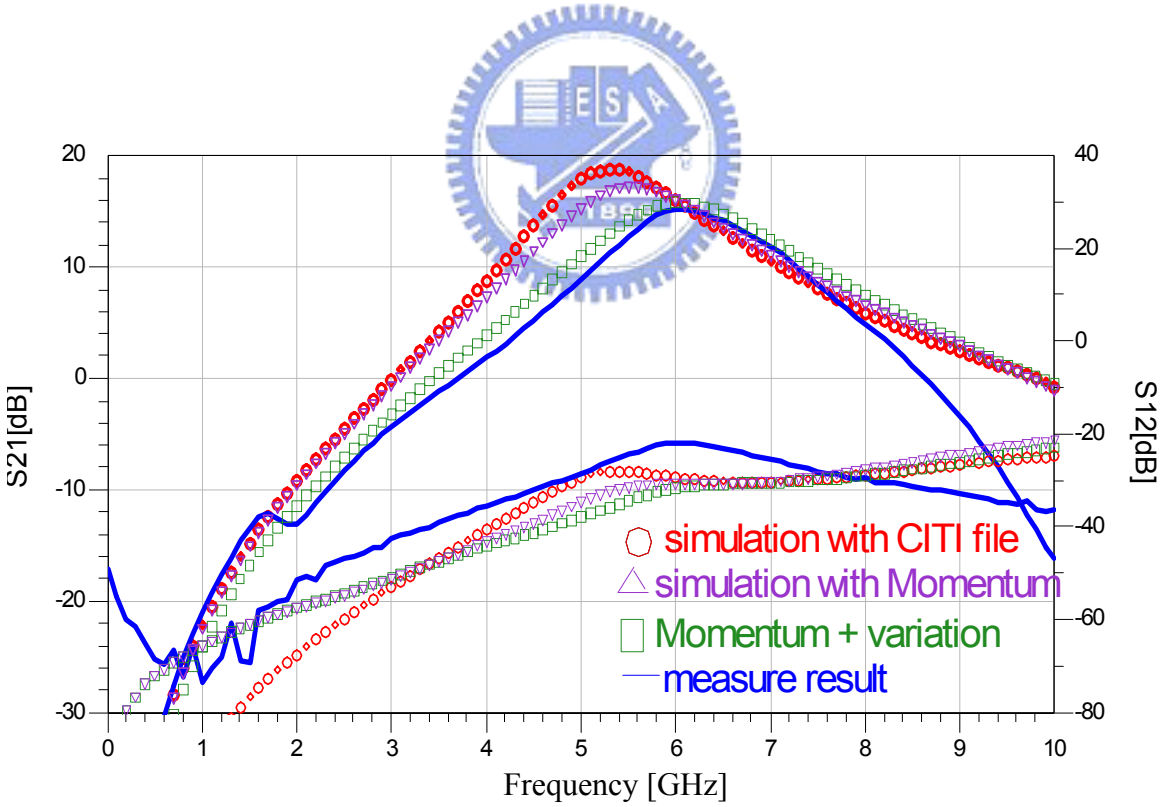


Fig 3.6 Simulation and measured result of power gain (S21) and isolation (S12)

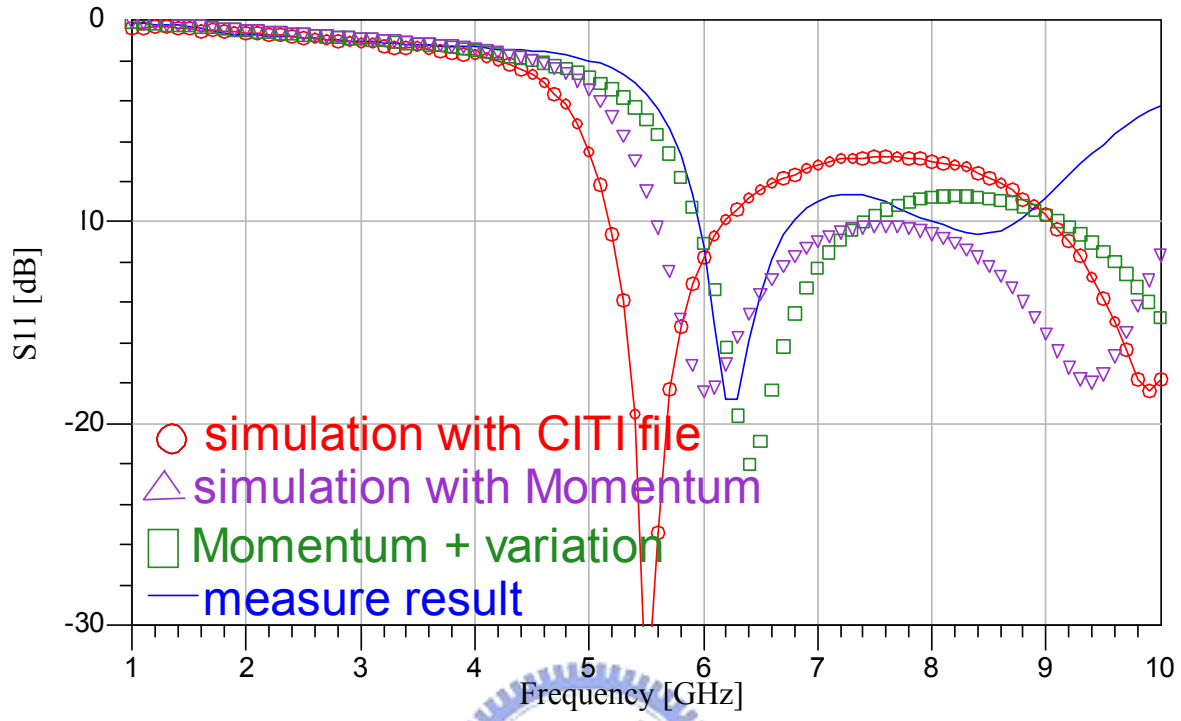


Fig 3.7 Simulation and measured result of input match

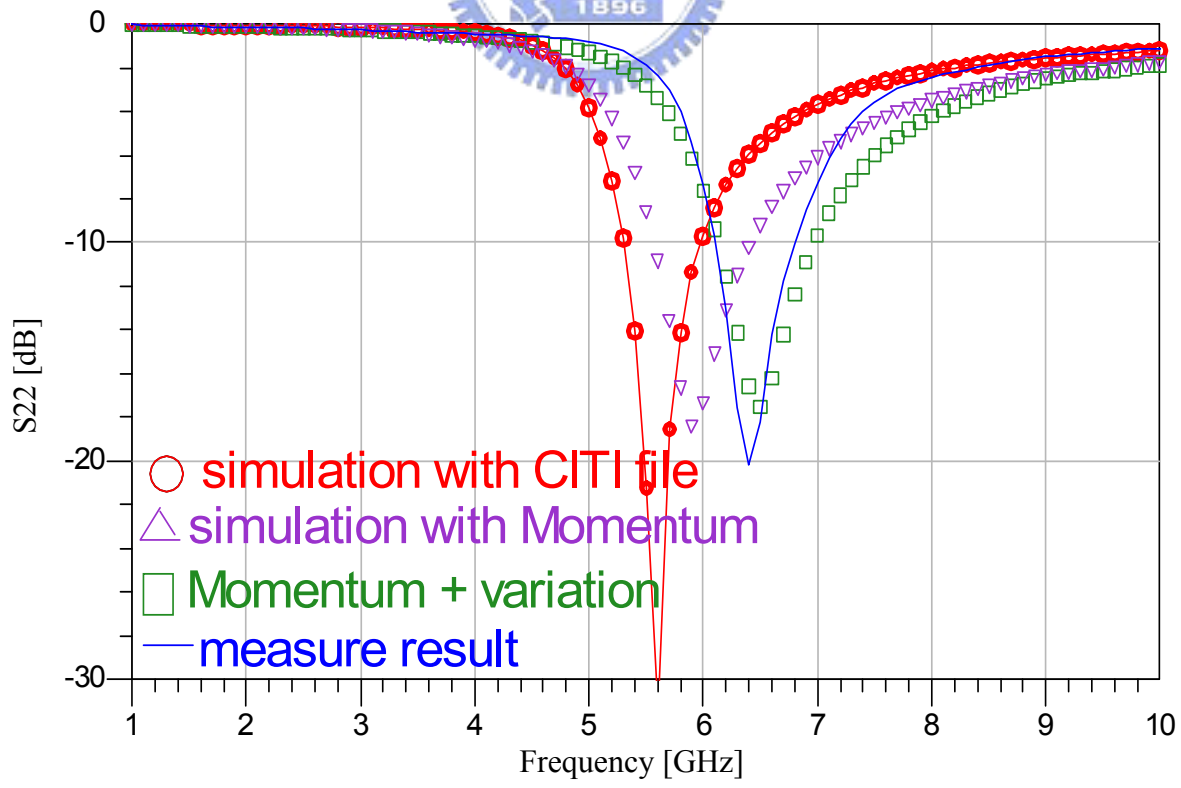


Fig 3.8 Simulation and measured result of output match

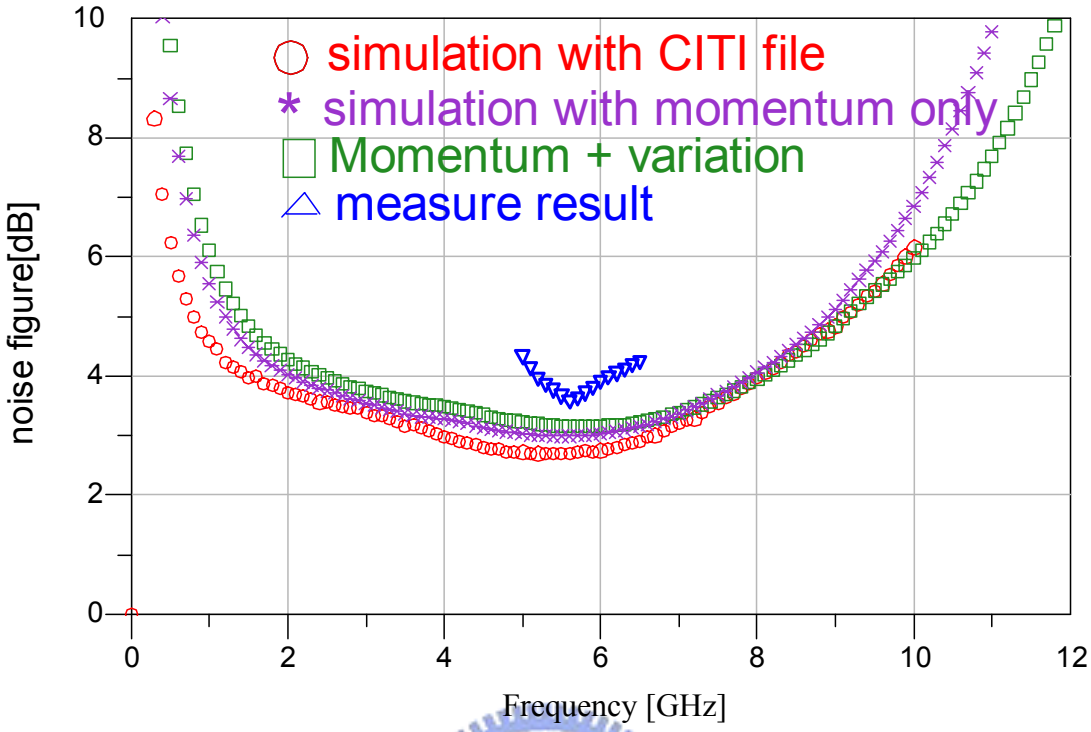


Fig 3.9 Simulation and measured result of noise figure

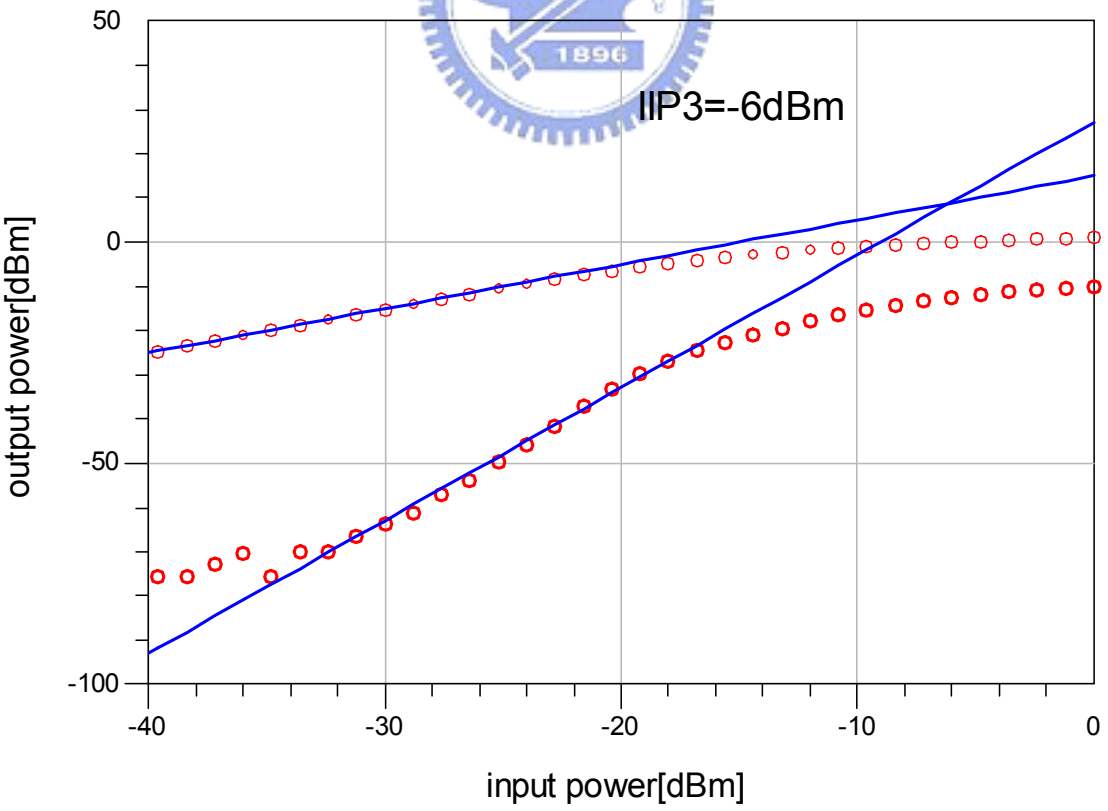


Fig 3.10 Measured result of two-tone test at 5 GHz

TABLE I Summary of simulation and measured result of Darlington pair LNA and comparison with single input MOS

Circuit	ISD architecture	Darlington pair (Sim.)	Darlington pair(Meas.)
S11	**-11(dB)**	**-28(dB)**	**-20(dB)**
S22	**-29(dB)**	**-35(dB)**	**-24(dB)**
S21	**14(dB)**	**18.6(dB)**	**15.5(dB)**
S12	**-28(dB)**	**-29(dB)**	**-21(dB)**
NF	**2.5(dB)**	**2.7(dB)**	**3.5(dB)**
1dB	**-14(dBm)**	**-20(dBm)**	**-15(dBm)**
IIP3	**-4(dBm)**	**-9(dBm)**	**-6(dBm)**
Power	**10(mW)**	**11(mW)**	**13(mW)**

3.4 Conclusion

A narrow band high gain low noise amplifier using Darlington pair structure is analyzed and designed for wireless local network area (WLNA) operating at 5.5 GHz frequency band. We employ the double cutoff frequency property of Darlington pair to achieve high gain design. Measured data show that the amplifier achieves maximum power gain (S21) of 15.5 dB, -10 dB input return loss (S11), and minimal noise figure of 3.5dB on the 5.8GHz frequency while consuming 13mW.

CHAPTER 4

A 3 to 8GHz Ultra-Wideband CMOS LNA

4.1 Introduction

As the demand for broadband data communication increases, the ultra-wideband (UWB) system is an emerging wireless technology for transmitting high-speed digital data over a wide spectrum of frequency bands at a very low power level. The low noise amplifier (LNA) in the receiver path of the UWB system critically determines several system parameters. The amplifier must hold flat gain, minimum noise figure, broadband input impedance matching, and good linearity, over the entire frequency band. In recent years, distributed amplifiers (DAs) were widely used to realize broadband amplifier [6-8]. The architecture is generally large in size because of many on-chip inductors, and consumes a high power level owing to several stages cascaded to derive an adequate gain level. An interesting approach employs a band-pass filter as the broadband impedance matching network, and the technique of gain peaking to derive flat gain [11]. In doing so, an additional capacitor is required to be placed in parallel to the gate-source of the input device for the filter design, which results in lower cut-off frequency (ω_t) and available gain.

In this chapter, an LNA suitable for ultra-wideband system is designed in a standard 0.18um CMOS process. With the techniques of negative feedback and gain compensation, this LNA circuit achieves the broadband requirement in low power consumption.

4.2 Principle of the circuit design

4.2.1 Ultra-Wideband LNA Circuit Topology

The schematic of the LNA circuit is shown in Fig.4.1. The circuit includes three stages of the common-source input stage m1 for input trans-conductance, the common-gate inter-stage m2 for less Miller's effect and better reverse isolation, and the common-source buffer stage m3 as the output buffer. The resistors R_f and R_{f1} not only provide negative feedback but also self-biasing.

Circuit performance can be analyzed by the small signal equivalent circuit as shown in Fig4.2. The shunt elements, Z_{fm}, R_{fm1} and R_{fm2}, represent the Miller's effect for R_f and R_{f1}. Note that we neglect the Miller impedance produced by R_f at the drain node of m1 since the input impedance of the common-gate stage is typically low. The overlap capacitance C_{gd} is ignored without loss of generality. The DC block capacitor C_{pass} is also neglected. Detail analysis is described as in the following.

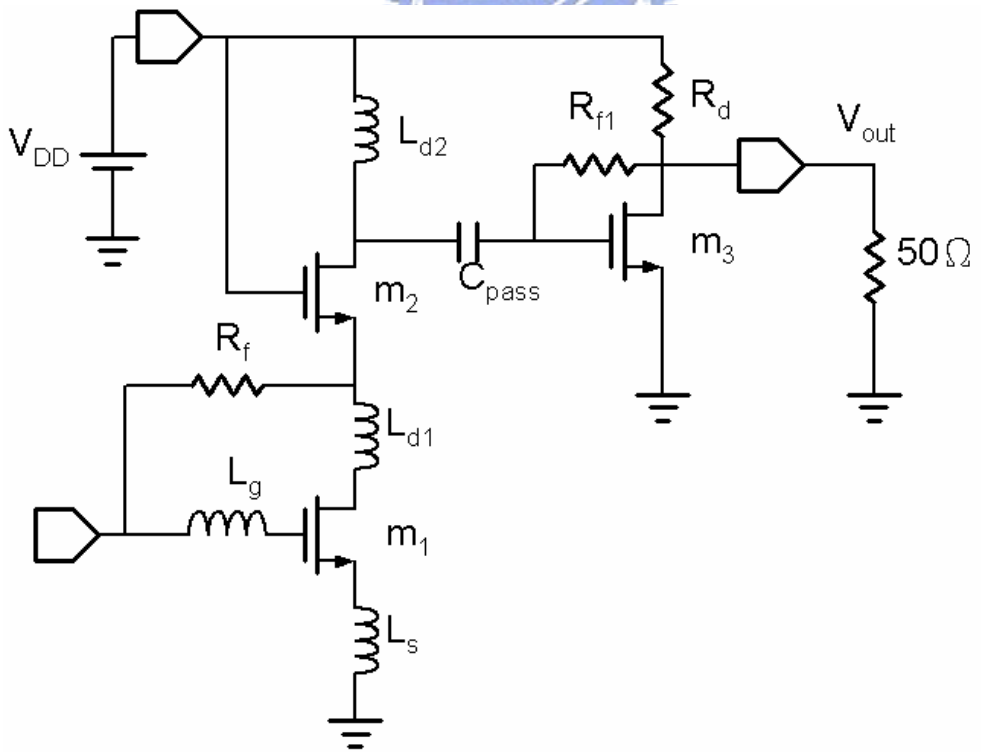


Fig.4.1 Schematic of Ultra Wide-band LNA

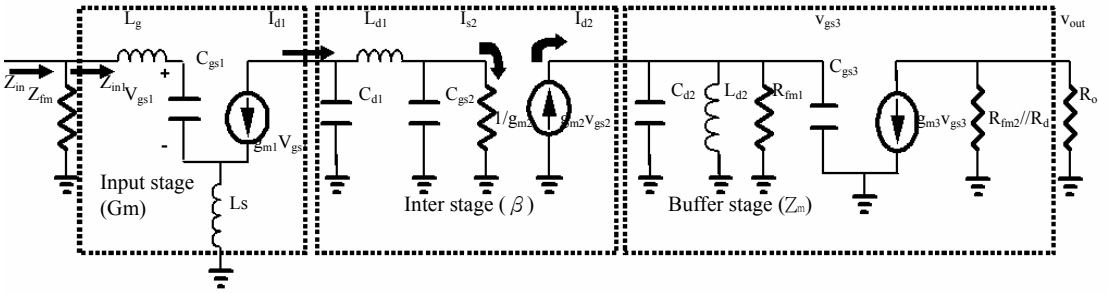


Fig.4.2 Small signal analysis of ultra wide band LNA

4.2.2 Broadband Input Matching

The configuration of inductive source degeneration would only provide narrow-band impedance matching to 50Ω [3]. The main advantage of the inductive source degeneration matching is on the high input trans-conductance at resonant frequency of the matching network. The detailed analysis of the input trans-conductance is shown in the following section 4.2.3. To preserve the advantage, the technique of resistive negative feedback is therefore employed to extend the frequency band of the matching network [8]. Thus, the matching network of the LNA is the combination of resistive negative feedback and inductive source degeneration matching network.

From small signal analysis in Fig.4.2, The input impedance can be derived as

$$Zin = Z_{fm} \parallel Zin1 \approx \frac{R_f}{1 - A_{v0}(s)} \parallel \left(s(L_g + L_s) + \frac{1}{sC_{gs1}} + \omega_t L_s \right) \tag{4-1}$$

where Z_{fm} is the miller impedance of the feedback resistor R_f and Av0(s) is the voltage gain from V_{in} to V_{sg2}. For the case at very low frequencies, Z_{in1} is close to an open-circuit due to the gate capacitance C_{gs1}, and the input impedance is

$$Zin(\omega \approx 0) = \frac{1 + R_f g_{m2}}{g_{m1} + g_{m2}} \tag{4-2}$$

a resistive level determined by the feedback resistor (R_f) as well as the trans-conductance of transistors m1 and m2. On the Smith chart as shown in Fig.4.6, we place the Zin(ω~0) at point

I, which is a resistive value higher than 50(Ω). For the case at the resonant frequency (ω01), Z_{in1} is a low resistive value ($\omega_t L_s$) compared to Z_{fm}, thus the total input impedance Z_{in} is approximately equal to Z_{in1}:

$$Zin(\omega = \omega_{01}) \approx Z_{fm} \left\| \frac{g_{m1}}{C_{gs1}} L_s \approx \frac{g_{m1}}{C_{gs1}} L_s \right. \tag{4-3}$$

The Zin ($\omega=\omega_{01}$) which is approximately a resistive value lower than 50(Ω) were placed around Point Ⅱ in Fig.4.6. Since these two levels Zin(0) and Zin(ω_{01}) give the impedance range as the frequency sweeps, adjusting both levels near 50Ω shall ensure good S11 over the entire frequency band. Similarly output impedance matching is realized by the parallel connection of R_{fm2} and R_d, as shown in Fig.4.2.

4.2.3 Gain flatness technique

Gain flatness is realized by gain compensation among the three stages. Under the condition of impedance match, available power gain shall be the same as the voltage gain. From the model in Fig.4.2, the overall voltage gain can be expressed as

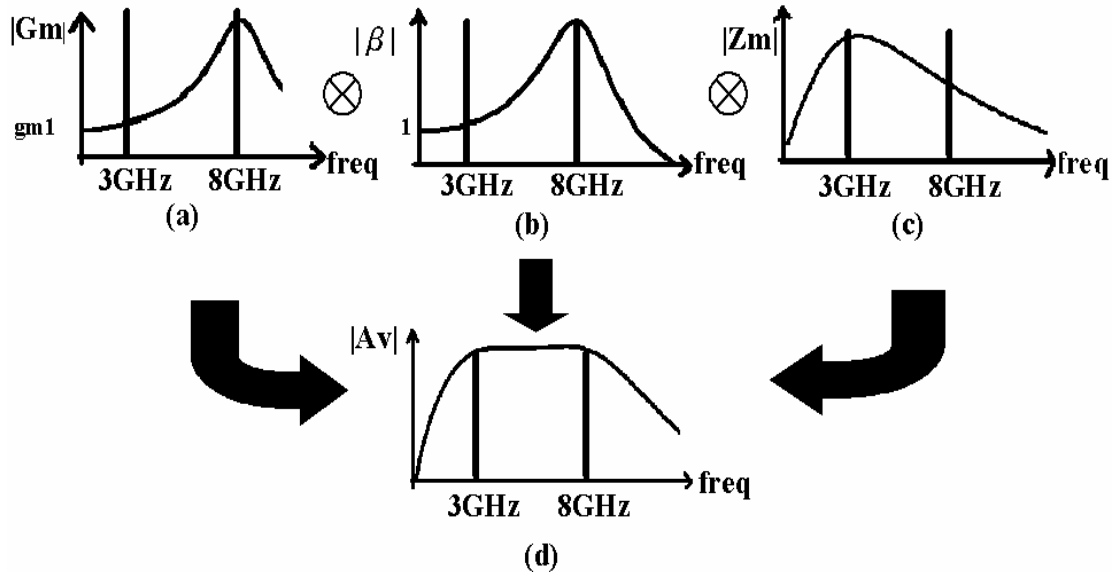


Fig.4.3 Illustration of signal amplification

$$Av = \frac{V_{out}}{V_{in}} = \frac{I_{d1}}{V_{in}} * \frac{I_{d2}}{I_{d1}} * \frac{V_{out}}{I_{d2}} = Gm * \beta * Zm \tag{4-5}$$

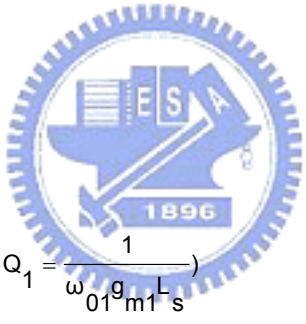
where G_m is the trans-conductance of the input stage, β is the current gain of the inter-stage, and Z_m is the transfer function of the buffer stage.

Although the frequency response of each stage appears as narrow-band tuned, the composite response can achieve broadband gain flatness with appropriate design. An inter-stage matching inductor L_{d1} is inserted in the cascoded configuration to enhance the gain level at high frequencies [12]. As illustrated in Fig.4.3, the frequency responses of the first two stages are tuned with peaking around 8-GHz, while that of the third stage around 3-GHz. As a result, the frequency response of the cascaded circuit yields to broadband gain flatness.

The trans-conductance G_m of the input stage can be derived as

$$G_m = \frac{I_{d1}}{V_{in}} = \frac{g_{m1}\omega_{01}^{\ 2}}{s^2 + s\frac{\omega_{01}}{Q_1} + \omega_{01}} \tag{4-6}$$

where $\omega_{01} = \frac{1}{\sqrt{(L_g + L_s)C_{gs1}}}$ $Q_1 = \frac{1}{\omega_{01} g_{m1} L_s}$)



the response which is a second low pass filter reaches for a maximum at the resonant frequency (ω_{01}). In this work the resonant frequency is set to be around the frequency of 8GHz, and the value of Q_1 is chosen to broaden the bandwidth. The frequency response of the Gm is shown in Fig.4.3 (a). Note that, the larger the Q_1, the higher the trans-conductance (Gm) in our operating frequency band. Under matching issue from above section mentioned in (4-3), the Ls is chosen lower than general inductive source degeneration narrow band LNA, which gives matching input impedance to 50(Ω) at resonant frequency. Thus, we can derive higher Q_1 as well as G_m in the frequency band from 3 to 8 GHz.

The inductor L_{d1} is tuned to resonate with the drain capacitance (C_{d1}) of m_1 and

gate-source capacitance (C_{gs2}) of m_2. Together they are considered as a part of the inter-stage. The transfer function of current gain β is

$$\beta = \frac{g_{m2}}{s^3 C_{gs2} C_{d1} L_{d1} + s^2 g_{m2} C_{d1} L_{d1} + s(C_{gs2} + C_{d1}) + g_{m2}} \tag{4-7}$$

With the inductor L_{d1}, the response at the frequency of 8-GHz is further boosted, as shown in Fig.4.3 (b).

The trans-impedance Z_m of the buffer stage is required to compensate for the roll-off generated by the overall trans-conductance of the first two stage, G_m*β. The transfer function of Z_m is derived as

$$Zm = \frac{V_{out}}{i_{g2}} = \frac{s\omega_{02}^2}{s^2 + s\frac{\omega_{02}}{Q_2} + \omega_{02}^2} * g_{m3} * (R_{fm2} \| R_d \| R_o) \tag{4-8}$$

where $(\omega_{02} = \frac{1}{\sqrt{C_t L_{d2}}} \quad Q_2 = R_{fm1}\omega_{02}C_t \quad C_t = C_{gs3} + C_{d2})$

The inductor L_{d2} is tuned to resonate with the gate-drain capacitance (C_{gd2}) and the gate-source capacitance (C_{gs3}) at the frequency of 3GHz. The response is shown in Fig.4.3(c). The cascaded circuit can achieve a flat voltage gain over the entire frequency band, as shown in Fig.4.3 (d).

4.2.4 Design Considerations and Trade off

The resistance of R_f shall be designed appropriately for impedance matching. The resistance, however, shall be large to minimize noise performance degradation. From simulation the value is chosen as 200Ω.

High trans-conductance in the input stage yields to good noise performance. Since the

trans-conductance of the input stage appears as narrow-band tuned, noise performance of the designed circuit is better near the in-band high frequency of 8-GHz. In addition, tuning at higher frequency calls for a smaller gate inductance Lg. Consequently the parasitic resistance is smaller in practice, and the degradation to noise performance is minimized. Simulation shows the minimum noise figure is 4.5 dB around 8GHz, and the maximum value is 6 dB around 3-GHz.

To meet the requirement of Z_m, the value of the inductor L_{d2} is chosen around 6 nH. The self resonant frequency of this inductor must be high above the frequency range for broadband operation. On the other hand, use of a low-Q inductor is acceptable as far as the broadband application is concerned. Thus, the metal width of 8um, narrower than the typically size in the design kit, is actually applied to this design to reduce parasitic capacitance and the occupied area. All of the inductors and interconnects are analyzed by the electromagnetic simulation tool of Agilent MOMENTUM. Circuit performance is analyzed together with the simulated S-parameters of the passives.

4.3 Chip Implementation and Measured Result

4.3.1 Microphotograph of Chip

A microphotograph of the LNA circuit is shown in Fig.4.4. The circuit is fabricated in the TSMC 0.18um CMOS technology. The die area including bonding pads is 0.81 mm by 0.8 mm. As can be seen, the size of L_{d2} is approximately the same as that of the inductor L_g (~1.2nH and metal width =15um).

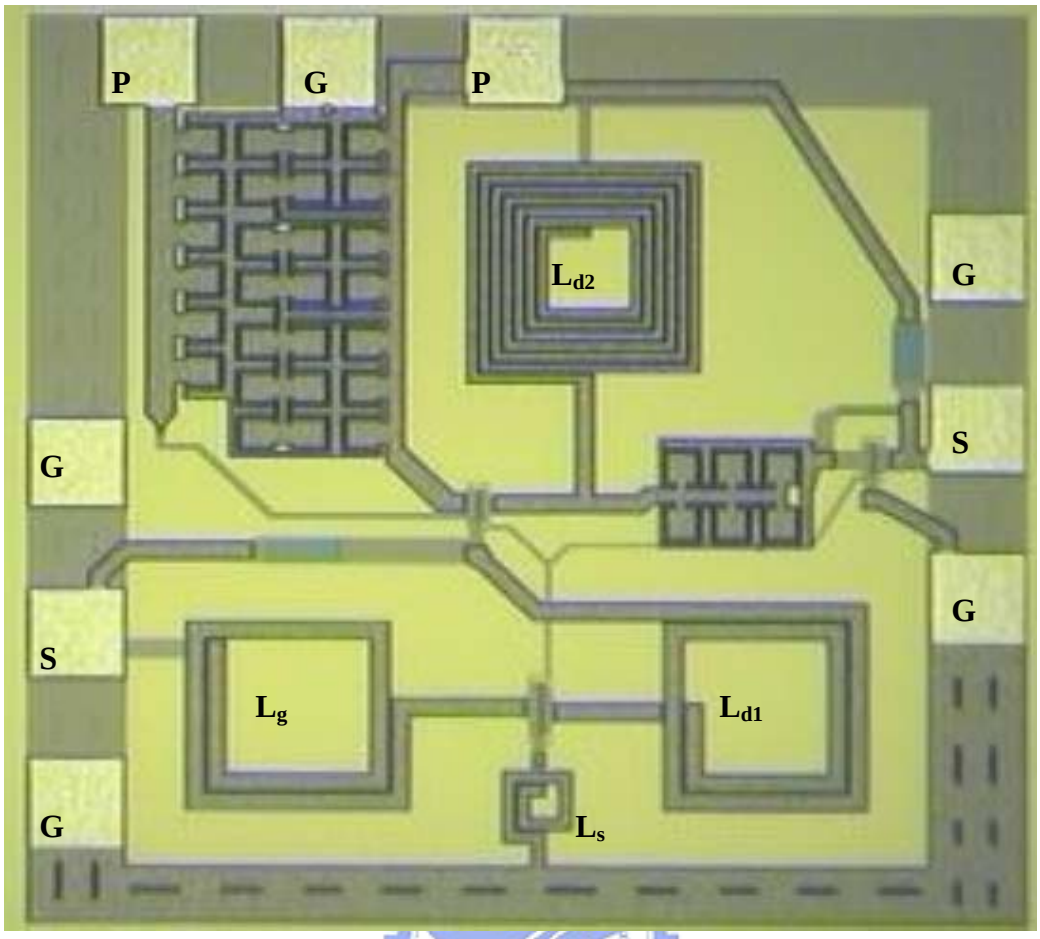


Fig.4.4 Microphotograph of the UWB LNA circuit

4.3.2 Measurement and Simulation Result

Measurement is conducted by on-wafer RF probing. Measured S-parameters are plotted in Fig.4.5 and Fig.4.6, together with simulation results with and without trouble shotting for comparison. The measured power gain achieves the maximum value of 9.2 dB at 3GHz and degrades to 6.3 dB at 8GHz. It agrees well with the simulated data below 6GHz. Above 6GHz, the measured power gain start to decrease and deviate from the simulation result. There is a difference of 1.5dB at 8GHz and the 3dB-bandwidth is 2-to-8.2GHz. From the gain flatness technique, the inductive source degeneration structure was employed to provide enough trans-conductance gain to suppress noise figure of in band high frequency. The lower the trans-conductance gain of input stage, the lower S21 and higher noise figure would result. Hence, the discrepancy between measured data and simulation result on the S21 may be due to

the lower trans-conductance of input stage in the implemented circuit. From (3-1), we have known the cutoff frequency of input stage transistor m1 ($\omega_T = g_m / C_{gs}$ determines the input trans-conductance, a capacitor (C=0.08pF) is included between the gate and source node of the transistor m1 to reduce the input trans-conductance for trouble shooting. Note that, because the measured power consumption and biasing are roughly equal to the simulation result, we consider the intrinsic trans-conductance of transistor m1 (g_{m1}) doesn't change compared to simulation result. In Figure 4.5, the square plot shows the S21 result after adding the capacitor C, it agrees well with the measured result. On the other hand, the measured S11 is worse than -10dB above 5.5 GHz, while the S22 achieves excellent performance due to resistive matching. It can be observed that the input impedance deviates from 50Ω at high frequencies on the Smith chart, the discrepancy may be due to unexpected parasitic capacitance that has not been included in the transistor model or resulted from process variation. We added parasitic capacitance (C1=0.1 pF and C2=0.4 pF) between ground and source node of transistor m1 and m2 respectively. We consider the parasitic capacitance mainly result from the PN junction capacitor between Deep n well and P-substrate. Note that, this parasitic effect has not been included in the device model provided by TSMC. The square plot of Figure 4.6 shows the conjecture agrees well with the measured result.

Fig.4.7 shows the noise figure, which is with an average value of 6.1 dB and minimum value of 5.65 dB at 7.5 GHz. Measured data agree with simulated data below 6GHz. Discrepancy at high frequencies may be due to degradation of S21 and inaccurate noise model. Linearity analysis is conducted by the two-tone test. Measured at 5 GHz, the two-tone test results of the third-order inter-modulation distortion are plotted in Fig.4.8. The IIP3 is -3.1dBm and the 1-dB compression point -19dBm. The total power of the LNA circuit dissipates 15mW with a power supply 1.5V. The comparison of wideband LNA between previously published work and this work is summarized in TABLE Ⅱ.

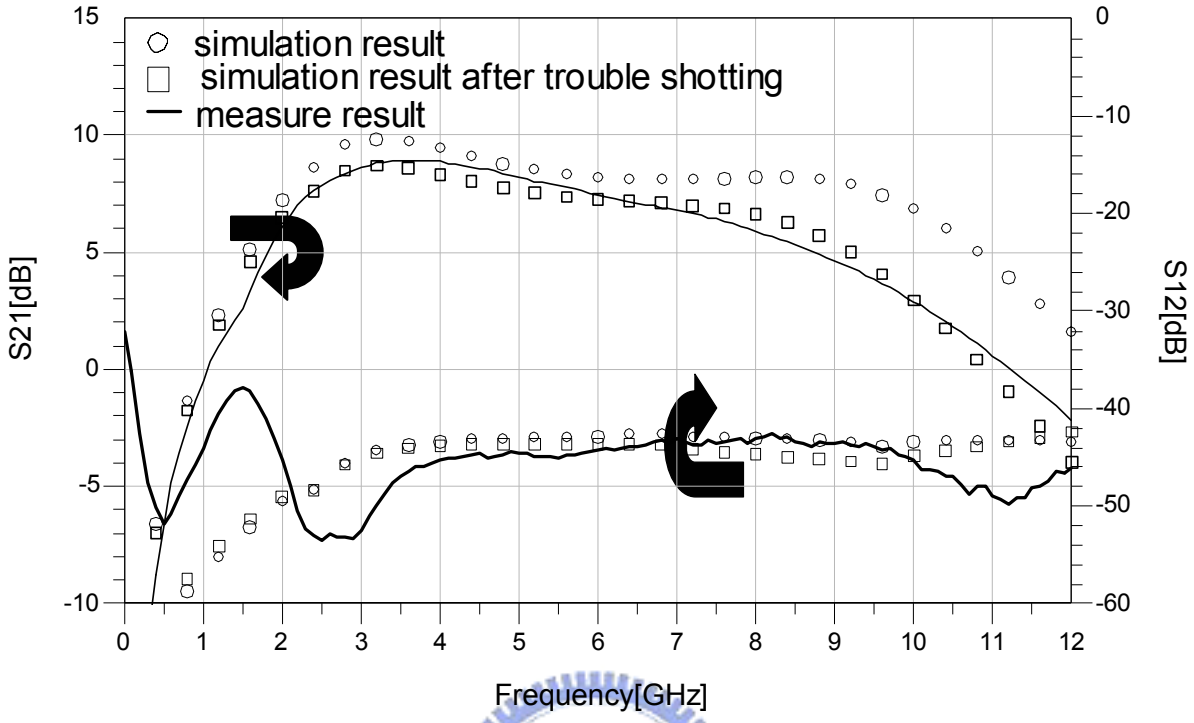


Fig.4.5 Simulation and measured result of power gain (S21) and isolation (S12)

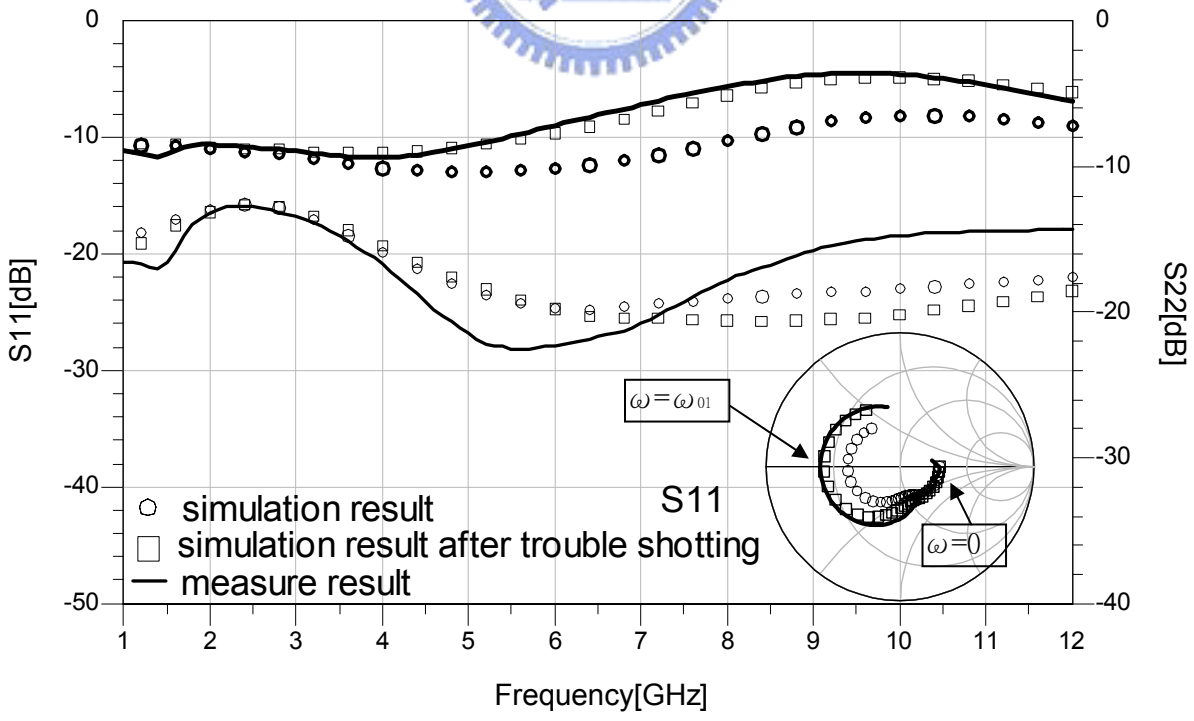


Fig.4.6 Simulation and measured result of input match and output match

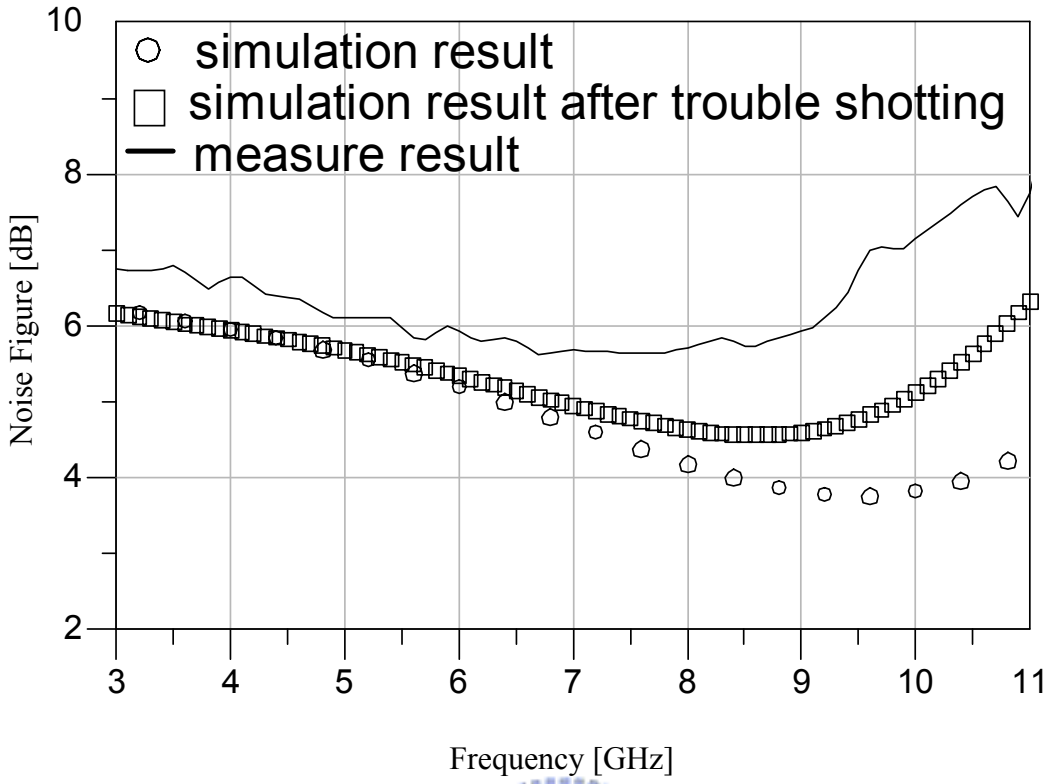


Fig.4.7 Simulation and measured result of noise figure

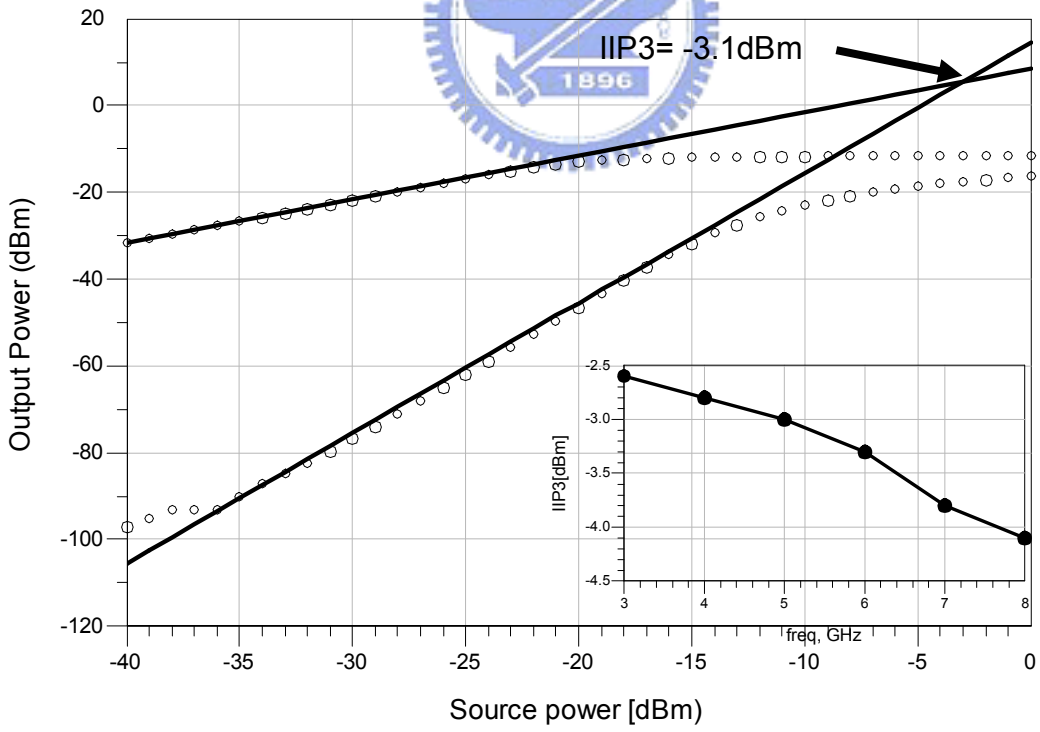


Fig.4.8.Measured result of two-tone test at 5 GHz; Measured IIP3 versus frequency

TABLE Ⅱ. Summary of measured result and performance comparison to other wideband amplifier.

	BW† **[dB]**	Gmax **[dB]**	S11 **[dB]**	NFmin **[dB]**	IIP3 **[dBm]**	Area **[mm²]**	Pw **[mW]**
*	2-2.8	9.2	< -5.8	5.65	-3.1	0.65	15
[11]	2.9-9.2	9.3	<-9.9	4	-6.7	1.1	18‡
[6]	0.6-22	8.1	<-8	4.3	N/A	1.35	52
[7]	0.5-4	7.4	<-7	5.4	N/A	1.12	83.4
[8]	1.5-7.5	7	<-6	8.7	N/A	3.67	216

*this work †-3dB bandwidth ‡total circuit power

4.4 Improved UWB LNA

From previous UWB LNA design, measured data show some deviation from simulation result at high frequency. It can be observed from the S11 on the Smith chart that unexpected parasitic occur such that the response is far from 50-Ω at high frequencies above 6GHz. The S21 degradation at high frequency may be due to low trans-conductance of input stage. Noise figure also show consistent trend as result of the degradation S21. To solve these problems, a modified UWB LNA circuit as shown in Fig.4.9 is introduced. The matching network is modified to achieve good input matching at high frequency and higher trans-conductance of the input stage by adding L_{g1} and C_p. Output buffer stage is transformed to a common drain stage to reduce the complexity of the previous resistive feedback common source stage. Also, a broadband variable gain function is added by tuning the RC network between second and third stage.

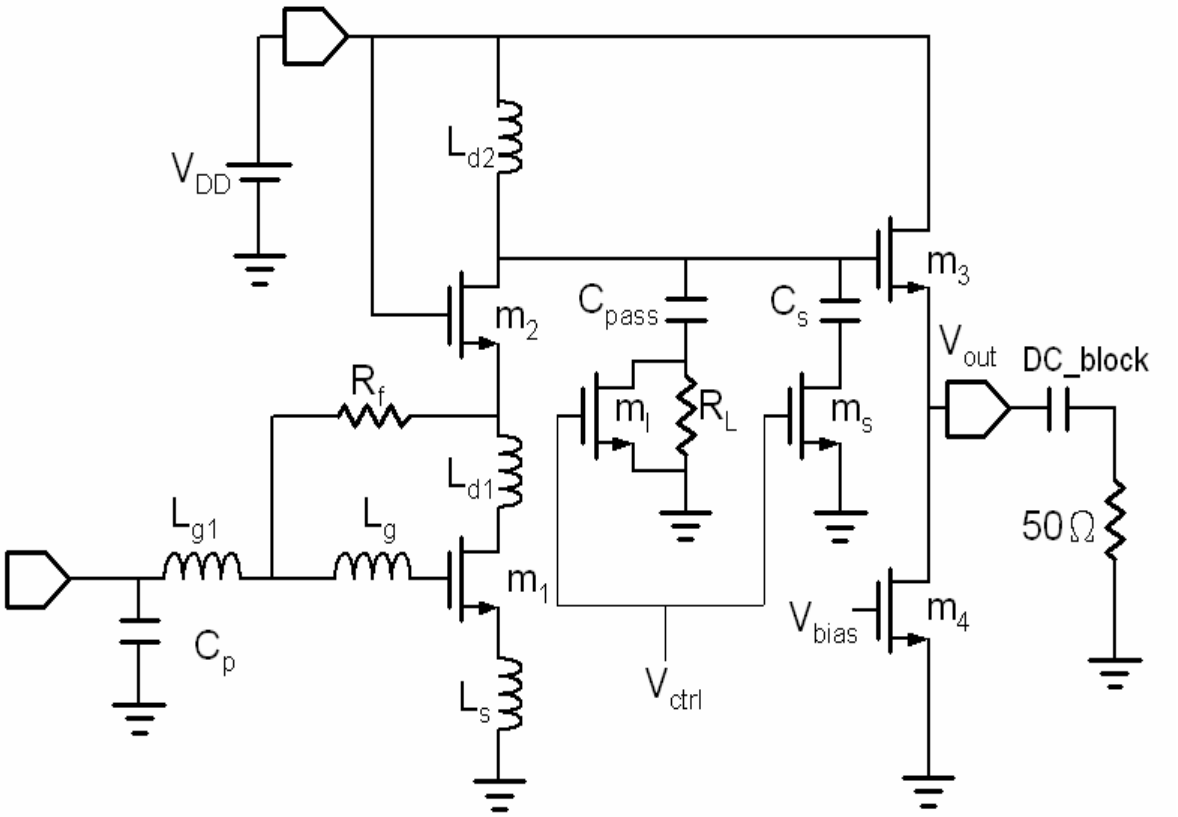


Fig.4.9 Schematic of the modified UWB LNA

4.4.1 wide-band input matching

From previous UWB LNA design, we combined the resistive feedback resistor and inductive source degeneration to achieve input matching in-band. The measured results show some parasitic effect at high frequency, hence the S11 deviate from the simulation result. Also, to increase the trans-conductance of the first stage, the Q1 of the equation (4-6) should be increased. The only way to increase the Q1 without increasing DC power is to decrease the source degeneration inductance Ls. From equation (4-3), the input impedance Z_{in} will be much far from 50Ω, this will worsen the input return loss. To overcome the awkward situation, the input matching network is modified to remedy the poor input return loss at high frequency. An L-section matching network (L_{g1} and C_p) is added to our previous one as shown in Fig.4.10.

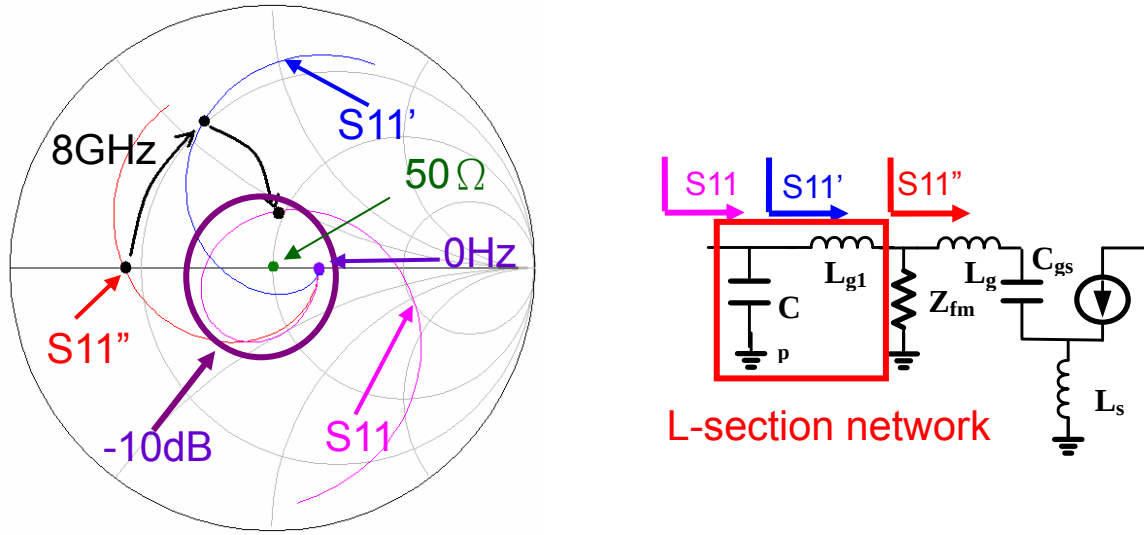


Fig.4.10 Modified input matching network to improve S11 at high frequency in band

The S11" is the previous input matching network. The only difference is that the Ls were decreased to increase the Q1 of input trans-conductance. From the Smith chart, the resonant frequency point is far from the 50Ω. Our goal is to provide good input matching between 3 and 8 GHz. The L_{g1} is added to shift the S11" to inductive direction. The S11' shows the input return loss after adding L_{g1}. Finally, the inductive part is compensated by the parallel capacitance (C_p), the S11 shows the input return loss of the overall input matching network. From the matching network, we not only remedy the degradation of the input return loss at high frequency to within -10dB, but also increase the input trans-conductance.

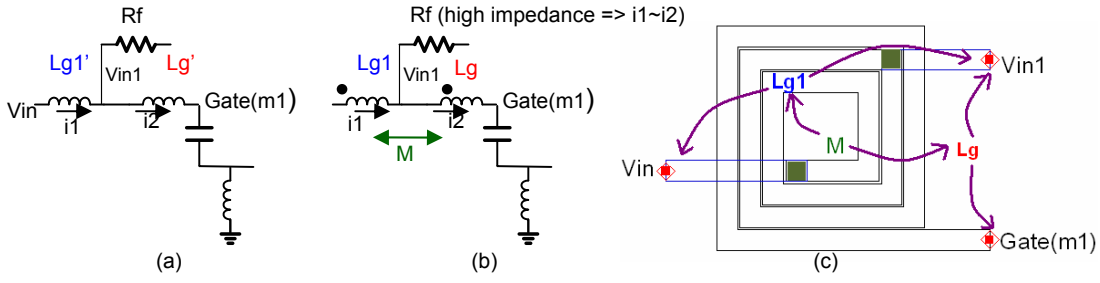


Fig.4.11 Using mutual inductance to reduce spiral inductor area

Taking the chip area into consideration, the input matching network which has two inductors L_{g1} and L_g will require larger die area to implement the two spiral inductors. A

transformer-like inductor shown in Fig.4.11(c) is implemented to reduce die size. From simulation result, the inductance value of the two uncoupled inductors ($L_{g1'}$ and $L_{g'}$) require 0.6 (nH) and 0.9 (nH) respectively, as shown in Fig.4.11(a). Taking the coupling effect of the two inductors into consideration as shown in Fig.4.11(b), if the impedance seeing into the resistive feedback resistor is high enough compared to the inductive source degeneration impedance Z_{in1} (Fig.4.2) , the $i_1 \sim i_2$ holds. As a result, we can derive

$$L'_{g1} \approx L_{g1} + M \quad M > 0$$
$$L'_{g} \approx L_{g} + M \quad M > 0 \qquad (4\text{-}9)$$

The mutual inductance M not only reduce the separate inductor value that we require but also can help to integrate the two inductors into one inductor with a tapping connected to R_f. Fig.4.11(c) shows layout of the transformer-like inductor. And the simulation result is shown in Fig.4.12.

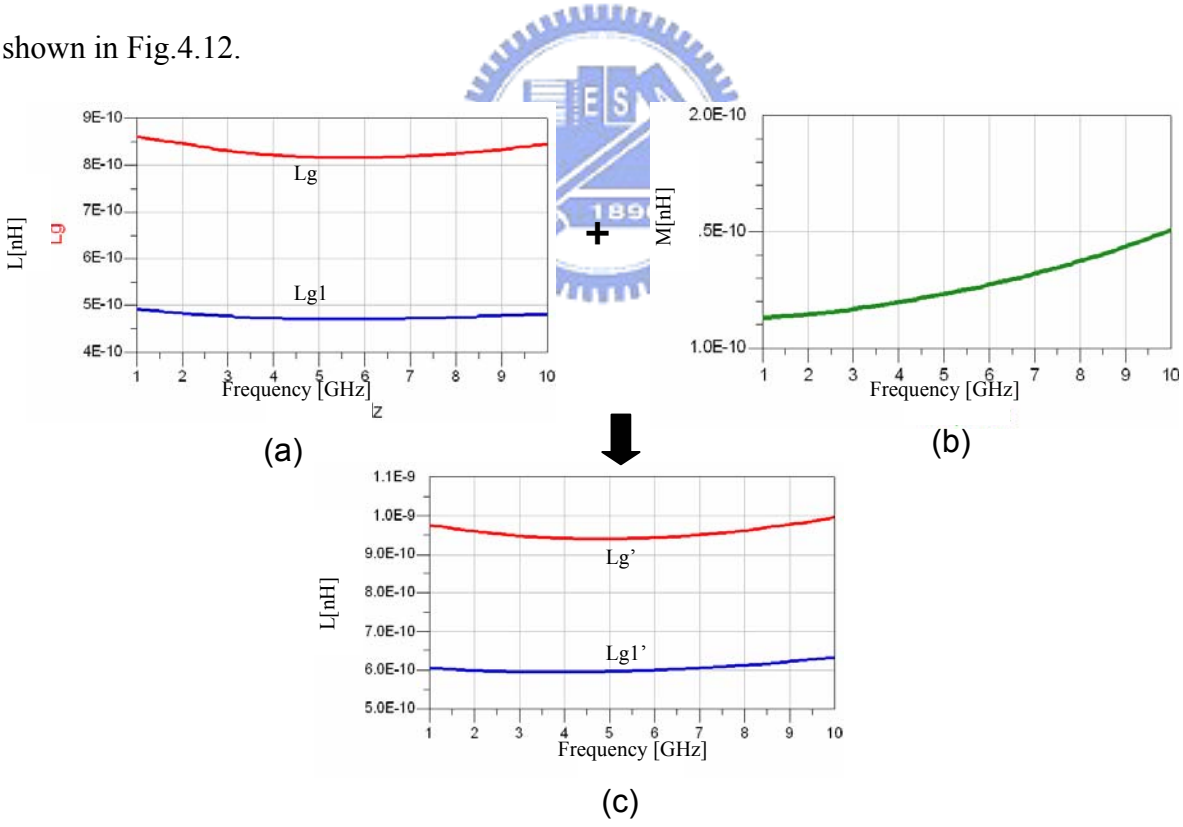


Fig.4.12 Simulation result of the transformer-like spiral inductor

4.4.2 Variable Gain Function

The noise figure of LNA is dictated by the sensitivity specification (the lowest power to

be received at the specified BER) of the receiver to provide the weakest received signal. The LNA should provide enough gain to suppress the noise of the following stage. But under strong received signal conditions, the LNA or the whole receiver gets saturated and degrades the linearity (IIP3) performance. Hence, the large amplitude range of signals requires variable gain function. This is to enhance the signal to noise ratio, in presence of minimum amplitude signals, while not saturating the last stages of the receiver, in presence of maximum amplitude signals.

One of the popular method of controlling the gain of the cascoded LNA is by diverting a portion of drain current from the cascoded transistor through another MOSFET [13], as shown in Fig.4.13(a). Although the method is suitable for the wideband amplifier as result of the broad band reduction of the current splitting mechanism, this scheme of gain control significantly degrades the NF and affects the input impedance matching. An enhanced scheme proposed in [14] controls the gate bias of the PMOS transistor in the folded cascade topology and does not sacrifice the noise figure in low gain mode. But in high gain mode, the power consumption may be large due to the low trans-conductance of the PMOS transistor. The other variable gain method is to place the control gain circuit at the drain node of the cascoded MOS transistor [15]. The advantage of the method not only preserves noise figure performance but also keeps the same power consumption at different gain modes. However, the method is only suitable for narrowband application.

In our LNA variable gain design, we can change the current gain of the inter stage (β) to achieve broadband variable gain, as shown in Fig.4.13(c). If we have a voltage controlled load (G_{load}), as shown in Fig.4.13(b), to let only some constant portion of the i_{d2} to flow into

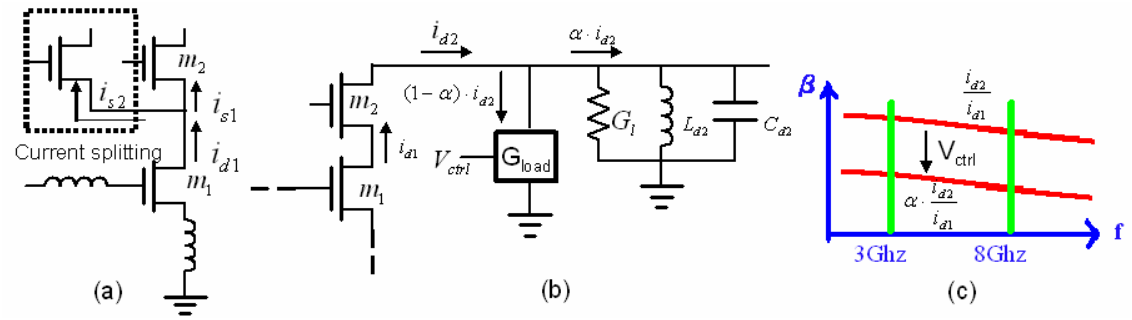


Fig.4.13.Illustration of variable gain method

RLC tank, a broad band mechanism is achieved. From simple calculation, the load G_{load} satisfies

$$G_{load} = \frac{1}{s\left(\frac{\alpha}{1-\alpha}\right)L_{d2}} + s\left(\frac{1-\alpha}{\alpha}\right)C_{d2} + \left(\frac{1-\alpha}{\alpha}\right)G_l \qquad (4\text{-}10)$$

In our interest band, the frequency is higher than the resonant frequency of the RLC load. The first term of right hand side in (4-10) can be neglected as result of its smaller value compared to another two terms. Thus, the G_{load} can be further simplified as

$$G_{load} \approx s\left(\frac{1-\alpha}{\alpha}\right)C_{d2} + \left(\frac{1-\alpha}{\alpha}\right)G_l \quad \left(\omega > \frac{1}{\sqrt{L_{d2}C_{d2}}}\right) \qquad (4\text{-}11)$$

which shows that the G_{load} is the parallelism of capacitor and resistor. If we can control the two components concurrently, the broadband variable gain is reached.

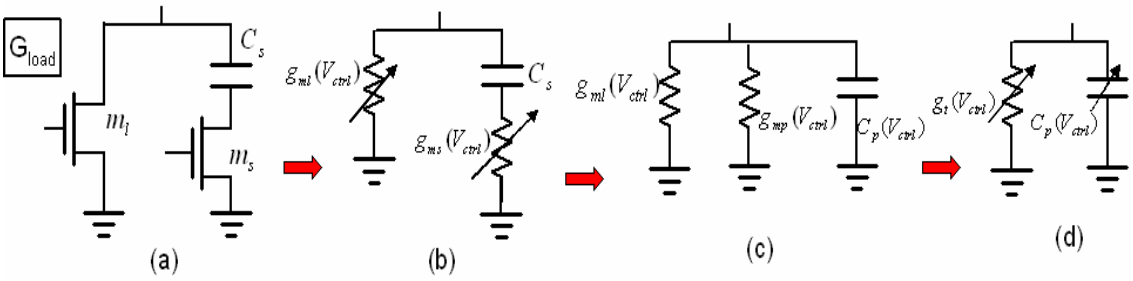


Fig.4.14 The variable gain tank G_{load}

The control circuit is shown in Fig.4.14 (a). The MOSFET can be seen as a voltage -controlled resistor, as shown in Fig.4.14 (b). The series RC network (Cs and g_{ms}) can be further expressed as parallel form, as shown in Fig.4.14 (c). Finally, the voltage-controlled

network is obtained, as shown in Fig.4.14 (d), and the g_t and Cp can be expressed as

$$g_t = \frac{g_m^2 + 2C_s^2\omega^2}{g_m^2 + C_s^2\omega^2} g_m \sim\propto g_m(V_{ctrl}) \qquad C_p = \frac{g_m C_s}{g_m^2 + C_s^2\omega^2} g_m \sim\propto g_m(V_{ctrl}) \tag{4-12}$$

where we have assumed the trans-conductance of the two MOSFET were equal in value. With the help of the term $C_s^2\omega^2$ in the denominator, the above two equations can roughly depend on the trans-conductance of the two MOS transistor. Note that the capacitor Cs now can be transformed to a voltage-controlled capacitor by means of the voltage controlled-resistor g_{ms}.

Fig.4.15 shows the simulation result of Fig.4.13 (b). Here, we have set the G_l=5(mA/V), L_{d2}=7(nH) and C_{d2}=0.25(pF) to derive the single tuned load with peak value at low frequency in band and we can observe the broadband variable gain is achieved by increasing the g_m, thus V_{ctrl} ,in the frequency band between 3 and 8 GHz.

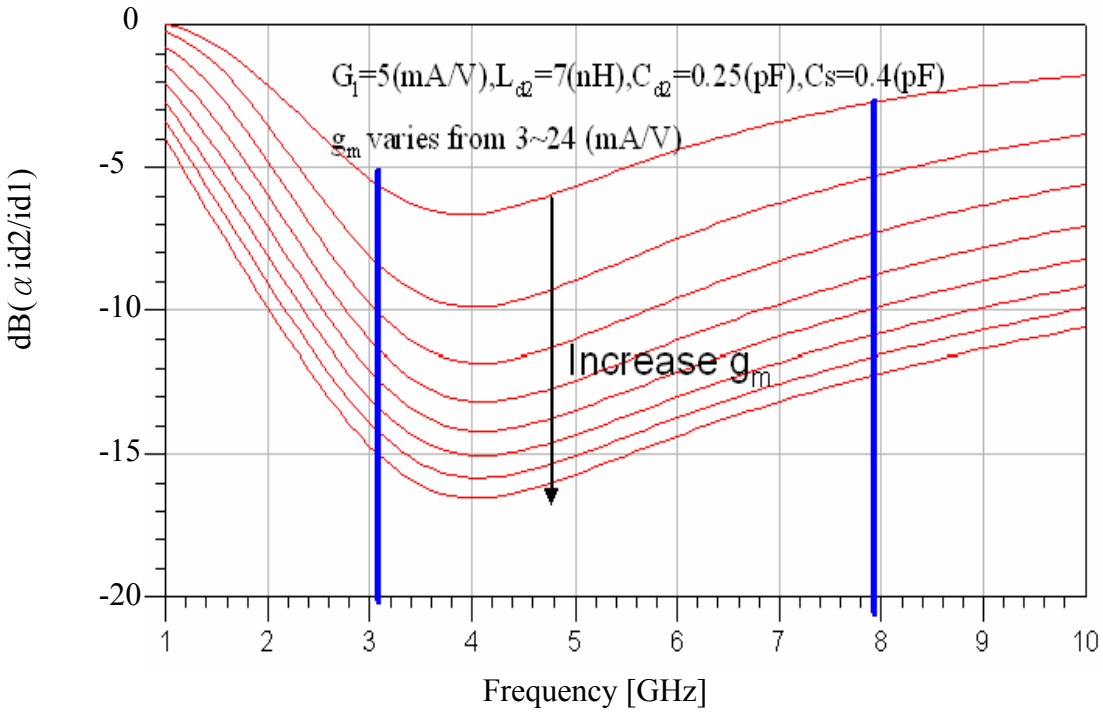


Fig.4.15 Simulation result of variable gain function

4.4.3 Simulation result

The modified circuit has been simulated by means of ADS simulation tool together with electromagnetic simulation tool of Agilent MOMENTUM.

4.4.3.1 Noise Figure

Because the input stage offers the maximum trans-conductance at high frequency in band, the noise figure in Fig.4.16 has the minimum noise figure of 2.99 dB. Also, compared to previous work, the noise figure decreased 1.2dB in average as result of the higher trans-conductance in band.

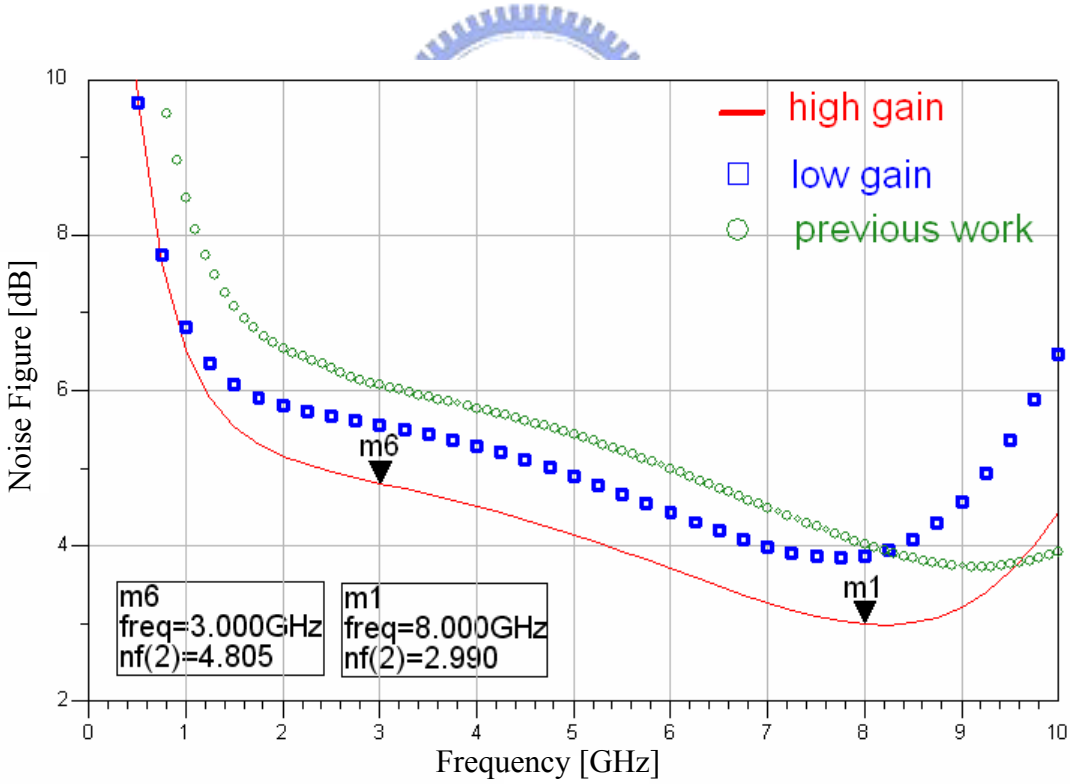


Fig.4.16 Simulation result of Noise Figure

4.4.3.2 S-Parameter

Fig.4.17 shows the S21 of the modified LNA, which achieves maximum power gain of 13.8 dB and dynamic range of 8.5 dB. In Fig.4.18, the power gain versus control voltage was simulated at 3-Ghz, 5.5-Ghz and 8-Ghz, respectively. Under the same control voltage, the maximum gain difference between different frequencies is 0.8 (dB). Also, neglecting the attenuation of the buffer stage, the LNA has voltage gain of 6 dB higher than S21 in the core circuit (without buffer) as shown in Fig.4.19, which will be suitable for the next stage in the fully on chip receiver front end. In Fig.4.20, the reverse isolation is below -45(dB). Because of the help of L-section input matching network, the S11 achieves good input return loss as shown in Fig.4.21. By means of the broadband resistive output impedance of common drain configuration, the S22, shown in Fig.4.22, can be matched to 50-ohm load easily for S-parameter measurement.

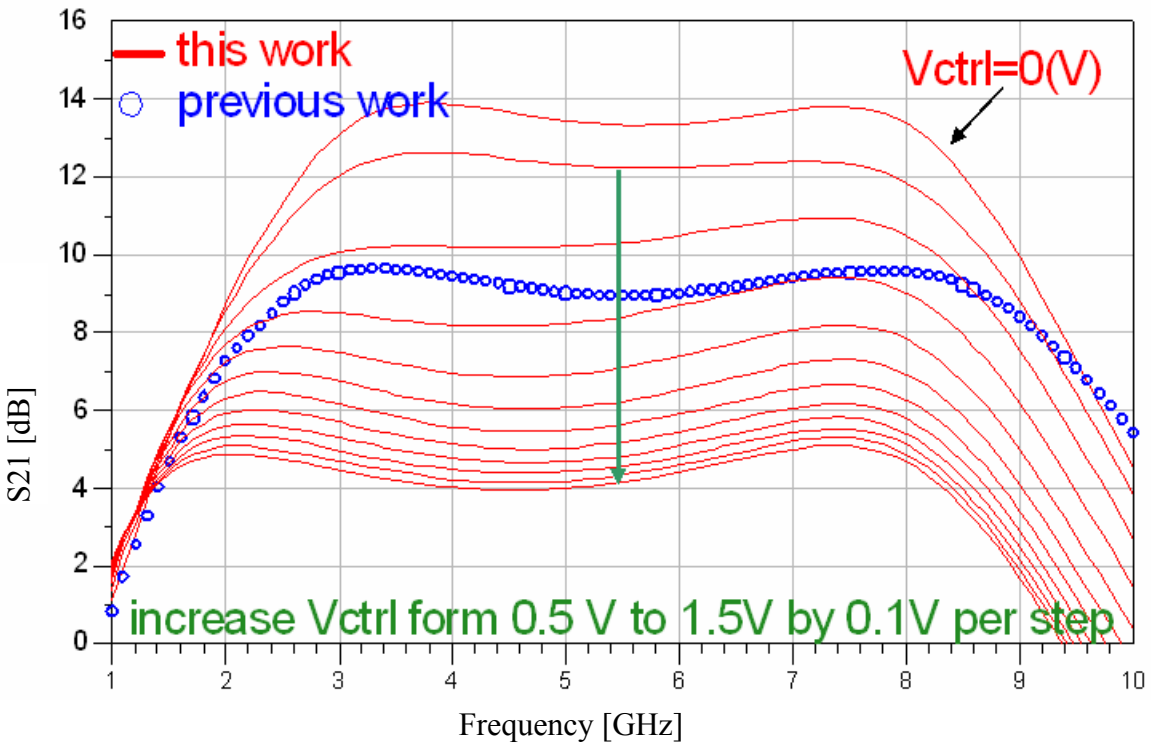


Fig.4.17. Simulation result of power gain (S21) at different control voltage

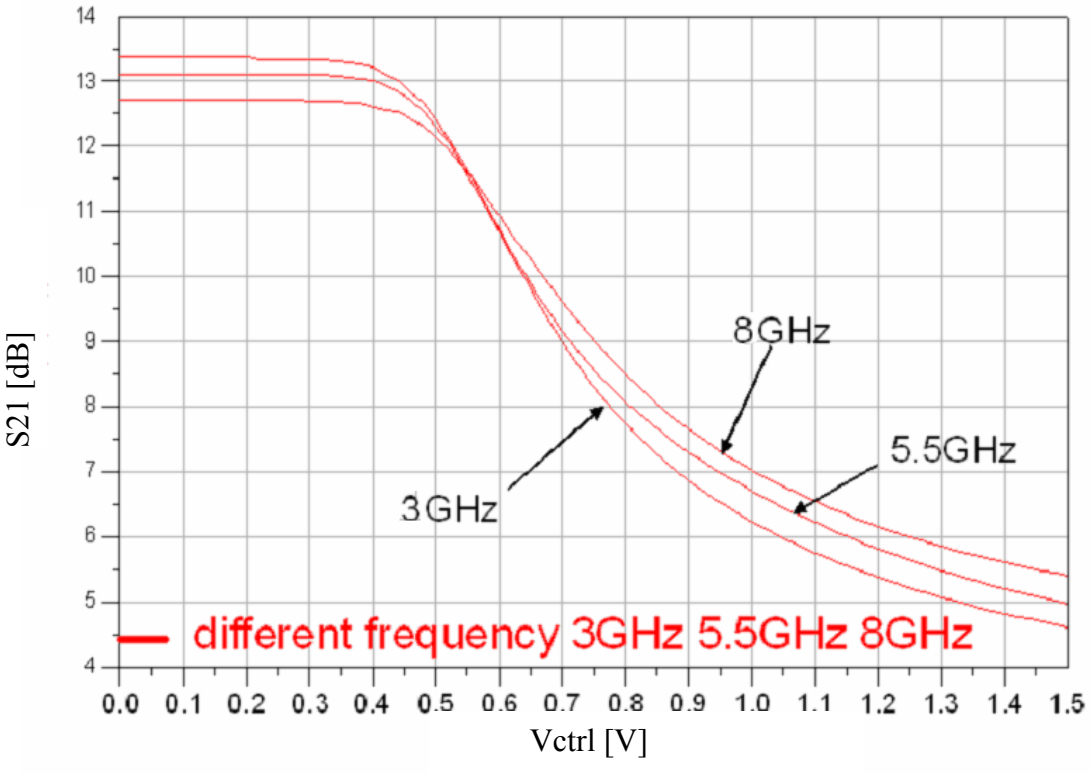


Fig.4.18 Simulation result of power gain (S21) versus different control voltage at different frequency

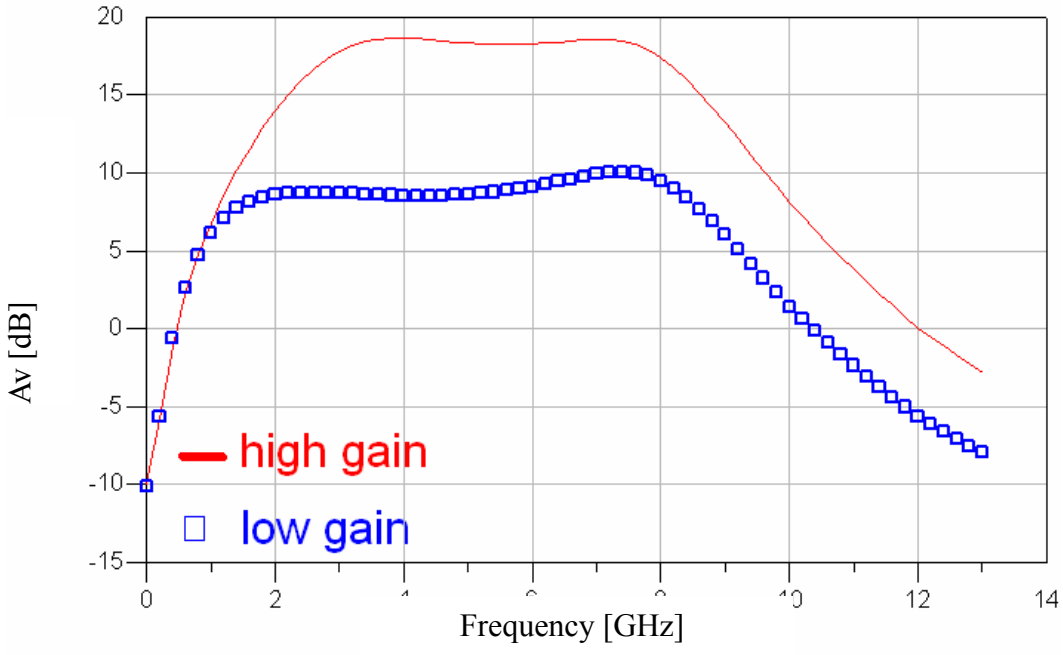


Fig.4.19 Simulation result of voltage gain without the buffer stage

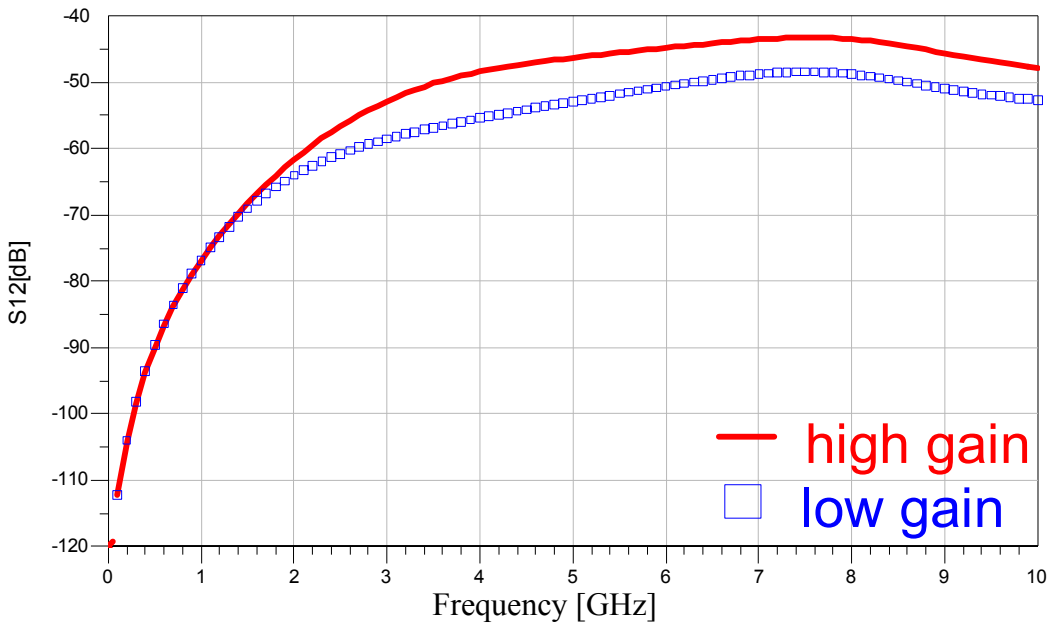


Fig.4.20 Simulation result of reverse isolation S12

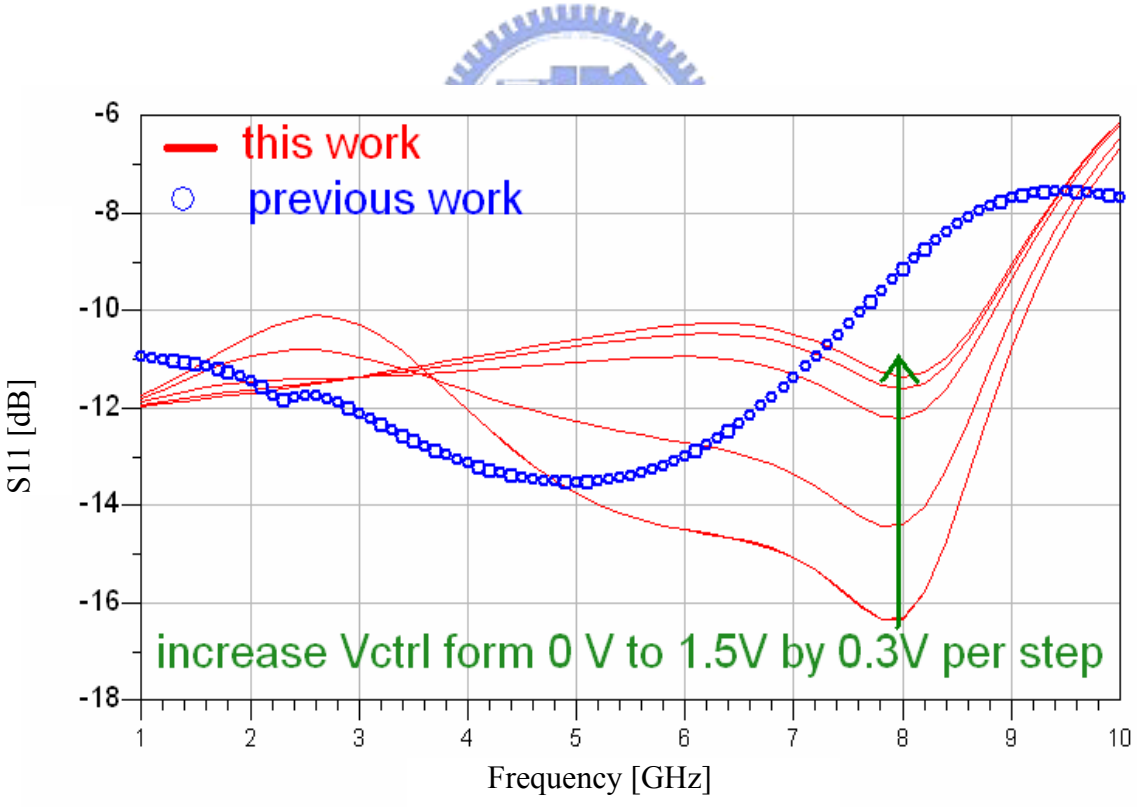


Fig.4.21. Simulation result of input return loss (S11) at different control voltage

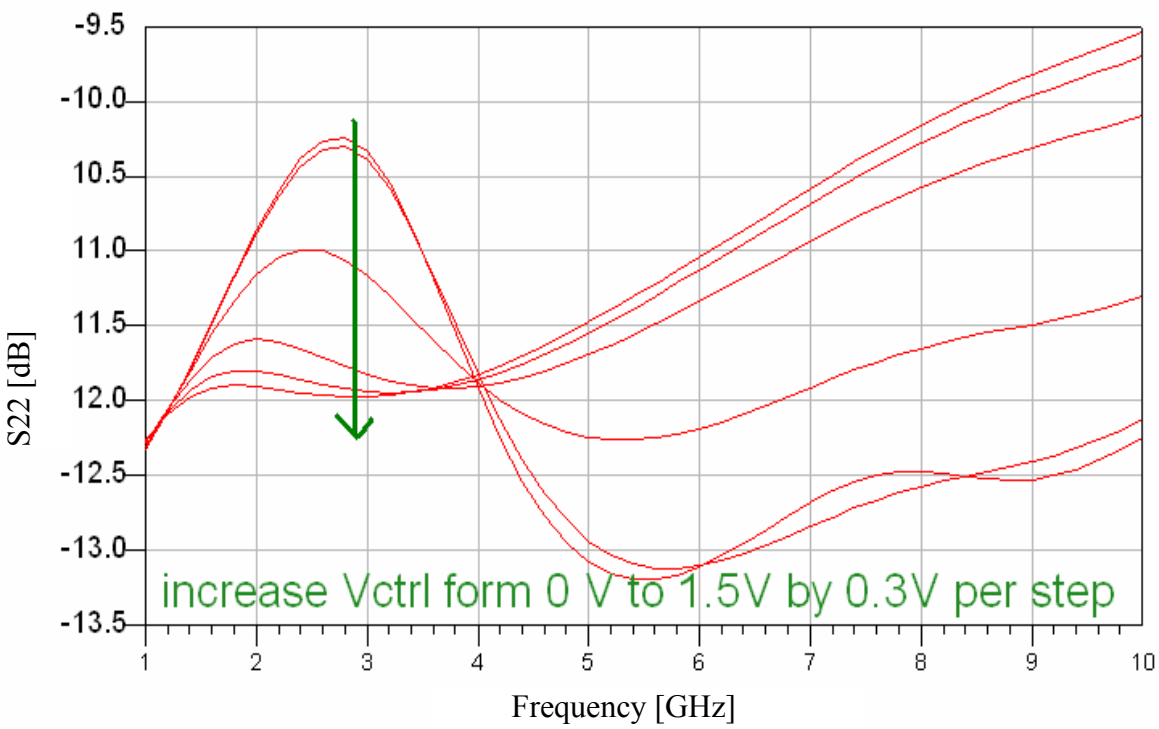


Fig.4.22 Simulation result of output return loss (S22) at different control voltage

4.4.3.3 Linearity

The two-tone test simulation results for third-order inter-modulation distortion are shown in Fig.4.23. Test is performed at 5-GHz. IIP3 is -3dBm, and the input referred 1-dB compression point (ICP) is -15 dBm. Moreover, Fig.4.24 shows IIP3 versus frequency. In the 3-8 GHz range, IIP3 is higher than -4.5 dBm in high gain mode and -3 dBm in low gain mode, respectively.

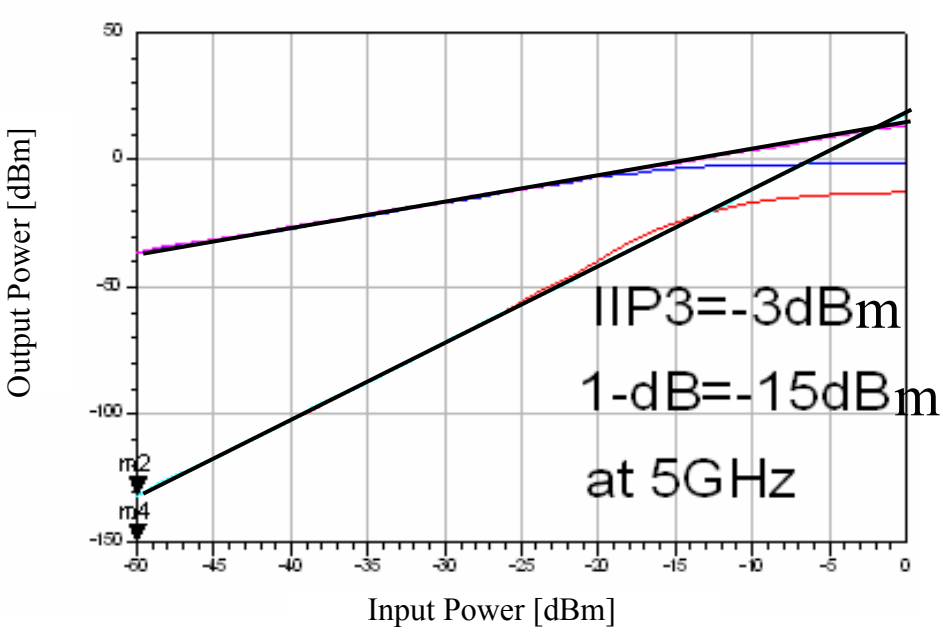


Fig.4.23.Simulation result of two-tone test at 5 GHz

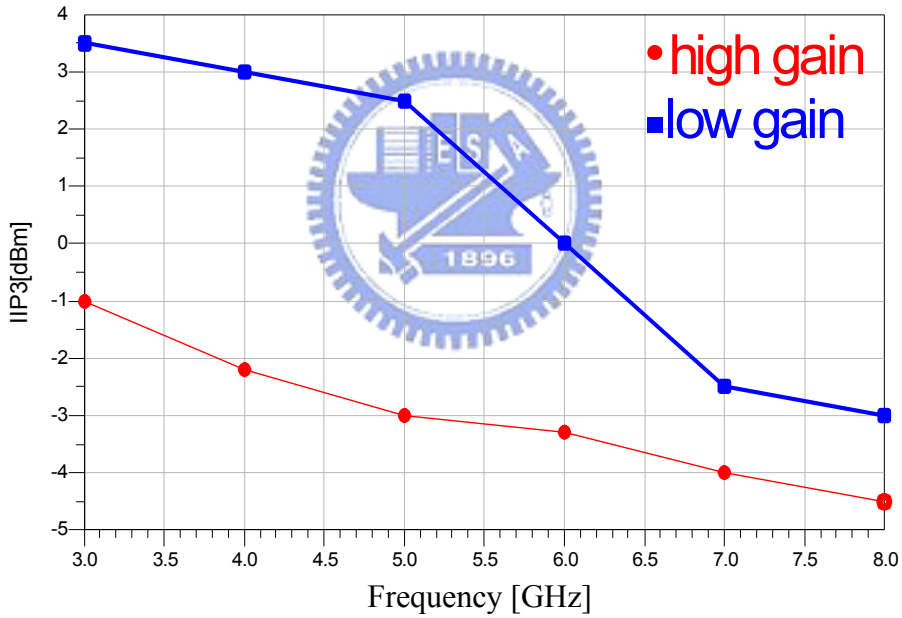


Fig.4.24 Simulation result of IIP3 versus frequency

4.4.3.4 Summary of Performance and Comparison with other Wideband Amplifier

The modified chip has been taped out through CIC. Although the improved LNA has only simulation result till now, we still can estimate its measured performance from previous simulation and measured result. TABLE Ⅲ shows the simulation result and our estimated specification. TABLE Ⅳ summarizes the comparison of wideband LNA between previously published work and this work

TABLE Ⅲ. Simulation result and specification of the modified ultra wide-band LNA

design	simulation		spec	
mode	High gain	Low gain	High gain	Low gain
S11	-11~-18(dB)	<-11(dB)	<-10(dB)	<-10(dB)
S22	-11~-16(dB)	<-11(dB)	<-10(dB)	<-10(dB)
S21	13.5~14.5(dB)	4~5(dB)	>13(dB)	>4(dB)
S12	<-44(dB)	<-48(dB)	<-35(dB)	<-40(dB)
NF	4.8~2.9(dB)	5~3.5(dB)	<5(dB)	<6(dB)
P-1dB	~-15(dBm)	~-15(dBm)	>-20(dBm)	>-20(dBm)
IIP3	-1~-4.5(dBm)	3.5~-3(dBm)	>-5(dBm)	>-4(dBm)
Power	20(mW) (12(mW) without buffer)		20(mW) (12(mW) without buffer)	
Gain range	9.5(dB)		9(dB)	
Operating freq	3~8Ghz		3~8Ghz	

TABLE Ⅳ. Summary of performance comparison with other wideband amplifier.

	BW* [GHz]	Gmax[dB]	S11[dB]	NFmin[dB]	IIP3[dBm]	I-dB[dBm]	Area[mm2]	Pdiss[mW]
This work	2.5~8.5	14.3	<-10	2.9	-1~-4.5	-15	0.60	12‡
Previous	2-8.2	9.2	<-5.8	5.65	-3.1	-19	0.65	9‡
[11]	2.9-9.2	9.3	<-9.9	4	-6.7	N/A	1.1	9‡
[6]	0.6-22	8.1	<-8	4.3	N/A	N/A	1.35	52
[7]	0.5-4	7.4	<-7	5.4	N/A	6-7.5 †	1.12	83.4
[8]	1.5-7.5	7	<-6	8.7	N/A	N/A	3.67	216

-3dB bandwidth † in the 1-4 GHz range ‡ core circuit power

4.4.3.5 Chip Photograph

The circuit will be fabricated in the TSMC 0.18um CMOS technology. The die area including bonding pads is only 0.83 mm by 0.74 mm. The chip photograph is shown in Fig.4.25.

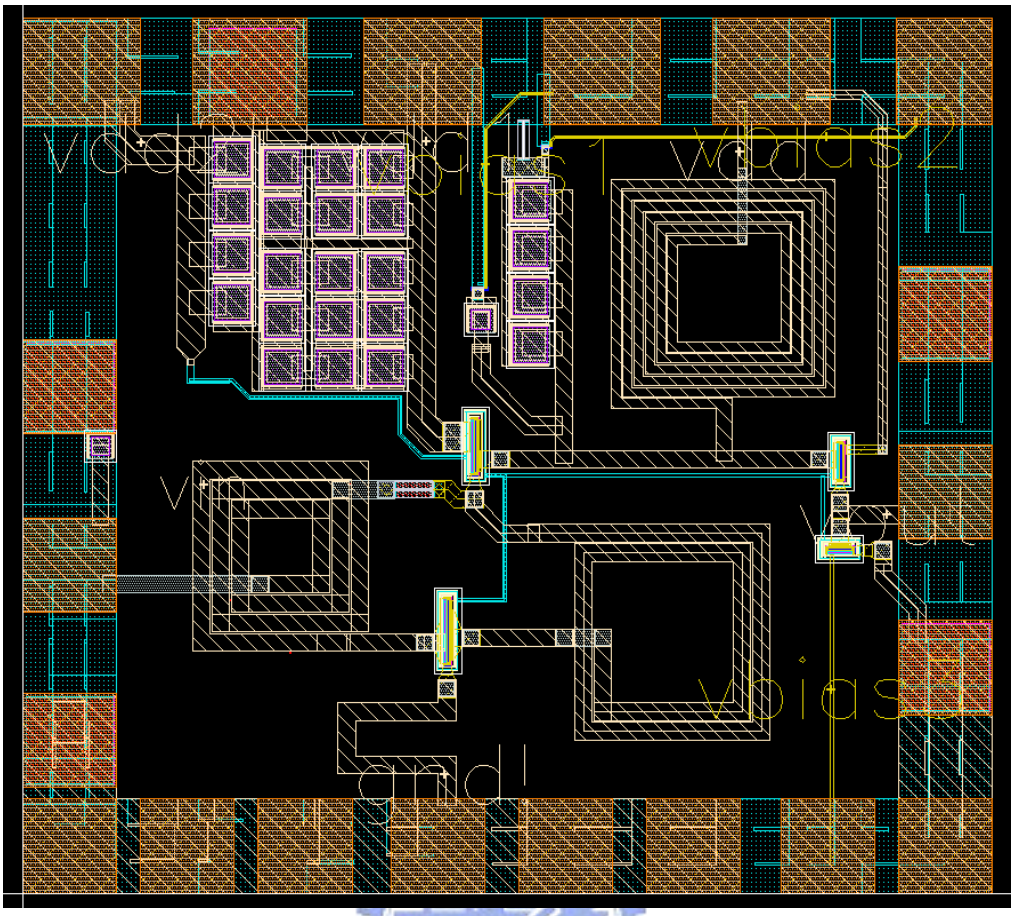


Fig.4.25 Photograph of the modified UWB LNA

4.4.4 Conclusion

A low noise amplifier (LNA), intended for use in the receiver path of an ultra-wideband (UWB) system, is designed in a standard 0.18um CMOS process. The inductive source degeneration input stage with an inter-stage matching inductor combined with a single-tuned load is applied to boost up signal at the high and low in-band frequencies between 3GHz and 8 GHz. Measured data agree well with the simulation results below the frequency of 6 GHz. For the discrepancy at the high frequency, an improved design is presented for better performance. The modified UWB LNA added the L-section matching network to overcome the poor input return loss at high frequency resulted from some unknown parasitic effect and the Q issue of the input stage to derive higher trans-conductance. Also, a broad band variable gain function is

included in the modified LNA to increase the input dynamic range. Simulation result shows the variable gain range achieves 9-dB in the frequency between 3 to 8 GHz.

CHAPTER 5

Summary and Future Work

5.1 Summary

In the chapter 2, some theoretical MOSFET noise model and noise theory are presented. Besides the noise consideration, some other important figure of merit such as gain, input matching, and power consumption etc. are another critical issue to design a superior fully on-chip CMOS LNA. A systematic narrow band LNA design method associated with CMOS process developed earlier [3] is discussed. Also, some broadband LNA architecture is discussed to develop the Ultra wide-band LNA design.

In the chapter 3, an alternative inductive source degeneration LNA using Darlington pair input stage to increase f_T is analyzed and implemented in a standard 0.18um CMOS process. Although, measured result show some operating frequency deviation from 5.5-GHz to 6-GHz. Measured data still show that the amplifier achieves maximum power gain (S21) of 15.5dB, -12 dB input return loss (S11), and minimal noise figure of 3.5dB on the 6GHz frequency while consuming 11mW.

In the chapter 4, a LNA, intended for use in the receiver path of an ultra-wideband (UWB) system is designed in a standard 0.18um CMOS process. With the techniques of negative feedback and gain compensation, this LNA circuit achieves the broadband requirement in low power consumption. Measured data agree well with the simulation results below the frequency of 6 GHz. For the discrepancy at the high frequency, an improved design is presented for better performance. The modified UWB LNA added the L-section matching network to overcome the poor input return loss at high frequency as result of some unknown parasitic effect and the Q issue of the input stage to derive higher trans-conductance. Also, a broad band variable gain function is included in the modified LNA to increase the input dynamic range. Simulation result

shows the variable gain range achieves 9dB in the frequency between 3 to 8 GHz.

5.2 Future Work

Although ultra-wideband LNA circuit using frequency compensation technique can achieve adequate power gain while consuming low power and small chip area. The measured data show the performance of noise figure is poor and far from the simulation result at high frequency. The discrepancy may be due to the inaccuracy of the noise model and low trans-conductance of the input stage. In the modified LNA circuit, we have increased the input stage trans-conductance to reduce the noise figure about 1.2 dB in average and simulation result shows the noise figure is between 4.8 and 2.9-dB in band. Although this improvement is not bad, the realistic noise level can be estimated around 5-dB from the discrepancy between simulation and measured data of the first UWB LNA circuit. How to further decrease the noise level under low power consumption and estimate the noise figure accurately become a challenge. If this problem is solved, the frequency compensation technique will be more useful than the distributed amplifier for the receiver path of the ultra-wideband system.

REFERENCES

[1] A. A. Abidi, "CMOS wireless tranceivers: The new wave," *IEEE Commun. Mag.*, vol. 37, pp. 119-124, Aug. 1999.

[2] T. H. Lee and S. S. Wong, "CMOS RF integrated circuits at 5 GHz and beyond," *Proc. IEEE*, vol. 88, pp. 1560-1571, Oct. 2000.

[3] D.K. Shaeffer and T.H.Lee,"A 1.5V, 1.5GHz CMOS Low Noise Amplifier,"*IEEE Journal of Solid-State Circuit*, vol. 32,no.5,p.745, May.1997.

[4] A. van der Ziel, *Noise in Solid State Device and Circuits.* New York:Wiley, 1986.

[5] http://www.ieee802.org/15/pub/TG3a.html

[6] R.-C. Liu et al.,"A 0.6-22GHz Broadband CMOS Distributed Amplifier," *RFIC Symp. Dig.*, pp. 103-106, 2003.

[7] B. M. Ballweber et al., "A Fully Integrated 0.5-5.5GHz CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 231-239, Feb. 2000.

[8] H. Ahn and D. Allstot, "A 0.5-8.5GHz Fully Differential CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp 985-993, 2002.

[9] Pozar, David M, *Microwave engineering.* New York:Wiley, 1998.

[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge, U.K.: Cambridge Univ. Press, 1998.

[11] Andrea Bevilacqua and Ali M Niknejad, "An Ultra-Wideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receivers," *ISSCC Dig. Tech. Papers*, pp. 382-383, Feb. 2004.

[12] W.-S. Kim, X. Li, Ismail, M. "A 2.4 GHz CMOS low noise amplifier using an inter-stage matching inductor," *Circuit and Systems*, 1999. 42nd Midwest Symposium on, Vol. 2,pp 1040-1043, 8-11 Aug ,1999.

[13] E.Sacchi, I.Bietti, F.Gatta, FSvelto and R.castello, "A 2 dB LNA," *Symposium on VLSI Circuits Digest of Technical Papers 2000.*

[14] T.K.K, Tsang and M.N. El-Gamal, “Gain Controllable Very Low Voltage (≦1 V) 8-9 GHz Integrated CMOS LNAs,” *IEEE RFIC Symposium 2002.*

[15] M.Kumarasamy Raja, Terry Tear Chin Boon, K.Nuntha Kumar and Wong Sheng Jau, “A Fully Integrated Variable Gain 5.75-GHz LNA with on chip Active Balun for WLAN,” *IEEE RFIC Symposium 2003.*

簡歷

姓　　名: 王柏之

學　　歷:

高雄市立高雄高級中學	(84 年 9 月 ~ 87 年 6 月)
國立中山大學電機工程學系	(87 年 9 月 ~ 88 年 6 月)
國立清華大學電機工程學系	(88 年 9 月 ~ 92 年 1 月)
國立交通大學電子工程所碩士班	(92 年 2 月 ~ 93 年 6 月)