國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

應變矽 CMOS 元件中隨機摻雜與隨機界面缺陷引起的臨界電壓變異度研究

The Random Dopants and Random Traps Induced Threshold Voltage Variations in Strained CMOS Devices

研 究 生 ：程政穎

指導教授 ：莊紹勳 博士

中華民國 九十九 年 九 月

應變矽 CMOS 元件中隨機摻雜與隨機界面缺陷引起的臨界電壓變異度研究

The Random Dopants and Random Traps Induced Threshold Voltage Variations in Strained CMOS Devices

研 究 生 ： 程政穎　　Student : Cheng-Ying Cheng

指導教授 ： 莊紹勳 博士　　Advisor : Dr. Steve S. Chung

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master of Science

in Electronics Engineering

September 2010

Hsinchu, Taiwan, Republic of China.

中華民國 九十九 年 九 月

應變矽 CMOS 元件中隨機摻雜與隨機界面缺陷引起的臨界電壓變異度研究

學生：程政穎　　指導教授：莊紹勳博士

國立交通大學電子工程學系電子研究所碩士班

摘要

90 奈米及以下的 CMOS 技術，採用應變矽技術得以延續摩耳定律(Moore's Law)，以提昇元件性能。近年的研究中顯示在 n 型 MOSFET 元件，SiC 在 S/D 的結構提供了高的驅動電流。而在 p 型 MOSFET 元件中，單軸的應變結構 SiGe 在 S/D 及嵌入式擴散阻擋層(EDB)，有著良好的可靠度和效能。然而隨著 CMOS 元件微縮到奈米尺度，對於前瞻 CMOS 技術而言，如何降低臨界電壓變異度(V_{th} variation)成為一項重要的議題。而隨機摻雜擾動(Random Dopant Fluctuation, RDF)被認為是臨界電壓變異度的主要原因。此外，由製程技術所產生的隨機界面缺陷擾動(Random Interface Trap Fluctuation, RTF)亦會增加臨界電壓變異度。

本論文中，我們利用可將由隨機摻雜擾動引致臨界電壓變異度正則化(Normalization)的 Takeuchi plot 來分析應變矽元件的變異度。首先，我們解釋了應變矽元件可改善臨界電壓變異度的原因，並藉由溫度、汲極電壓和基板電壓等效應來驗證應變矽元件擁有較佳的變異

度。此外，stress 之後所造成的隨機界面缺陷導致臨界電壓變異度的增加亦可利用 Takeuchi plot 來分析。實驗結果顯示，退化的 B_{VT} 與界面缺陷的數目呈比例關係。然而，在應變矽 n 型 MOSFET 元件中，由於反轉層電子與界面缺陷的距離較近，使得庫倫散射(Coulomb scattering)變得較強導致臨界電壓變異度退化的較嚴重。對應變矽 p 型 MOSFET 元件而言，退化的臨界電壓變異度即與應變效應無關。

The Random Dopants and Random Traps Induced Threshold Voltage Variations in Strained CMOS Devices

Student：Cheng-Ying Cheng　　Advisor：Dr. Steve S. Chung

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

ABSTRACT

For the CMOS device technology with gate length 90 nm and beyond, strained technique has been a successful technology to extend the Moore's law with further device scaling. Recent studies have revealed that the most mature CMOS technology is by the use of different strain techniques for n-MOSFET and p-MOSFET respectively. The use of SiC in the source and drain structure shows high driving current ability for n-MOSFET device. For p-MOSFET device, uniaxial structure with SiGe on source and drain with EDB (embedded diffusion barrier) seems to be promising in terms of its performance and reliability. However, as CMOS devices are scaled to the nanoscale dimension, reducing V_{th} variation becomes a significant issue for advanced CMOS technology. Random dopant fluctuation (RDF) is the major source of V_{th} variation in scaled bulk CMOS. Furthermore, stress-induced random traps fluctuation (RTF) is also considered to be another source of the enhanced V_{th} variation after the hot carrier stress.

In this thesis, the variability of strained devices has been reported. The random dopant fluctuation induced V_{th} variation can be normalized by Takeuchi plot. First,

the reasons for V_{th} variation improvement of strained devices are analyzed. The factors affecting the V_{th} variation which include temperature, drain bias, and substrate bias are examined. Experimental results show better variability of strained devices. Secondly, the basis of the enhanced V_{th} variation caused by stress-induced random traps can still follow the Takeuchi plot. The results show that the aggravated B_{VT} is proportional to the number of interface traps. However, for strained n-MOSFETs, due to the closer distance between inversion layer electrons and interface traps, Coulomb scattering limited by interface traps becomes strongly enhanced which results in a faster aggravation of V_{th} variation. For strained p-MOSFETs, the aggravated V_{th} variation is unrelated to the strain effect.

Acknowledgements

兩年的實驗室生活是精采豐富的，但同時也充滿艱辛與汗水。首先要感謝的是我的指導教授：莊紹勳教授，老師給予的生活上與專業上的指導與建議，讓我在學業上與研究上獲益良多並學習到對事物應有的嚴謹態度以及處理方法。除此之外，對於課業外的生活技能、觀念的督促，讓我必須在此表達感謝之意。

感謝在兩年研究生涯中，與我一起嚐遍酸甜苦辣的同學，包括永涵、元宏與士嵩，我們一起經歷困苦的研究過程，相信數年後再聚首，一定倍感溫馨。對於汪老師研究群的同學，即使我們身在不同的研究群，但我們的感情就像是一家人一樣，希望以後在業界相遇時還能保有我們現在的真誠，也祝福小馬、佑亮與榮標學長能夠順利取得博士學位，此外也感謝承翰、書民與嘉偉，感謝有你們這群學弟平日對於實驗室的付出，使學長們能夠專心於研究上，在此，輕遞一份真摯的祝福，希望明年亦能看見你們順順利利的畢業。

另外，在此也要感謝聯華電子在測試元件和技術上的協助，使本研究得以順利完成。

最後，要感謝我的家人與女友湘怡，你們是我最大的精神支柱，有了你們的支持和鼓勵，使我能堅持到現在。

謹將這份榮耀獻給培養我多年的父母親。

Contents

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

stress and (b) NBTI stress.

Chapter 1

Introduction

1.1 Background

Moore's Law has driven CMOS devices scaling for several decades. However, the scaling limits continue to be a great challenge. In order to properly operate today's very large scale CMOS integrated circuits, where hundreds of millions of transistors are gathered to analyze more complex integration, it is desirable to obtain the identical characteristics or small tolerance from the target characteristics of all the manufactured MOSFETs. However, due to several reasons, it becomes a serious issue today [1.1-1.2]. One of the most significant issues is the variability induced by the increase of random fluctuation for continuing further scaling down of transistors. Random fluctuations refer to a kind of variability that exhibits no correlation between neighboring devices as shown in Fig. 1.1 [1.3]. Various sources of the MOSFETs variability such as random placement of doped impurities (random dopant fluctuation, RDF), line edge roughness, gate oxide roughness and so on. It is increased by the reduction of device size since the electrical characteristics become more sensitive to the number of dopants in the depletion region. As a result, it cannot be eliminated by simply improving the process and device design. Therefore, as CMOS devices are scaled to the nanoscale dimension, there are multiple challenges to be overcome for advanced CMOS technology.

1.2 The Motivation of This Work

Since CMOS technology has reached 45 nm node at this time, further scaling to

32 nm and even beyond has been widely acknowledged as encountering many more challenges with regard to V_{th} variation issues. Recent study [1.4] has revealed that random dopant fluctuation (RDF) is the major source of V_{th} variation in scaled bulk CMOS. To improve the RDF, FDSOI or FinFET with undoped (lighter) channel [1.5-1.7], has been proposed subsequently to reduce the variability effectively.

Also, recent developments [1.8] in CMOS technology have highlighted the need in using the strain technique as a method to extend the scaling of CMOS device for high speed and low power logic applications. Several approaches among them, such as process-induced stress techniques, strained SiGe channel devices, substrate engineering, and hybrid substrate technology, have been utilized to improve device performance. However, so far, the sources and the mechanisms of V_{th} variation have not been experimentally clarified on strained devices. As a consequence, we are interested in understanding the variability of strained devices.

For the first time, in this thesis, we apply the Takeuchi plot [1.9], which normalizes V_{th} variation in terms of electrical equivalent gate dielectric thickness at inversion T_{inv} and V_{th}, to observe the V_{th} variation in various n-MOSFETs and p-MOSFETs employing different process-induced strain. The impact of their strains on the device reliability and variability will be investigated and compared.

1.3 Organization of the Thesis

There are five parts in this thesis. Chapter 1 is the introduction. We describe the motivation and organization of this thesis. In Chapter 2, we describe the experimental setup and the method of normalizing the V_{th} variation (Takeuchi plot) used in experiments. In Chapter 3, the variability study based on the V_{th} variation and the

effects of temperature, drain bias, and substrate bias of strained n-MOSFETs will be examined. Moreover, the enhanced V_{th} variation caused by stress-induced interface traps was proposed. In Chapter 4, by applying similar analysis, we will discuss the variability for strained p-MOSFETs. Finally, the summary and conclusion will be included in Chapter 5.

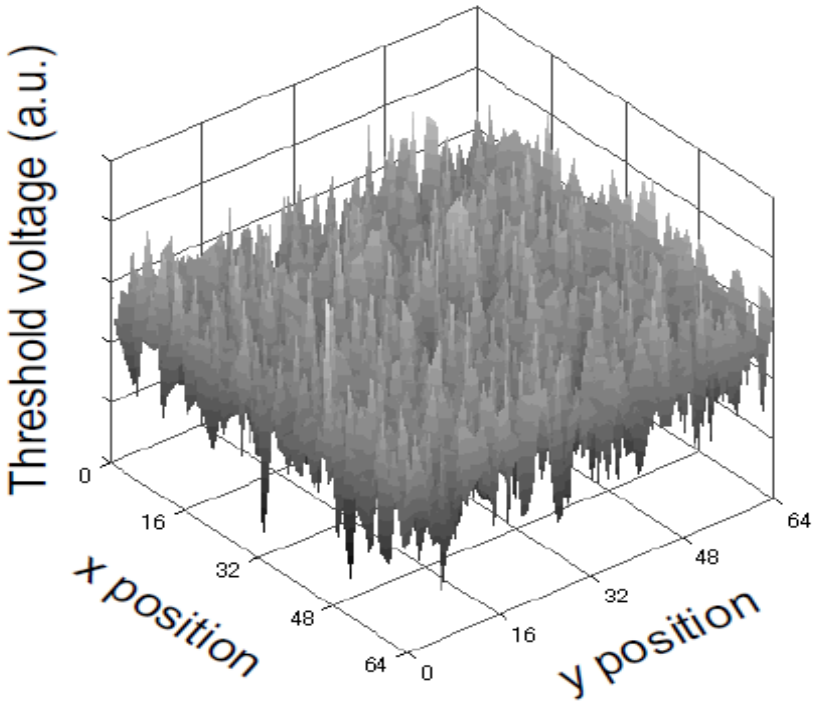


Fig. 1.1 Example of random threshold voltage fluctuations. Closely located identically designed 4k transistors are measured [1.3].

Chapter 2

Experimental Setup and V_{th} Variation

2.1 Introduction

As devices are scaled to the nanoscale dimension, it is important to understand random fluctuations. Since there are many possible microscopic causes, it is desirable to understand the mechanism of variability. Therefore, electrical measurement of random fluctuations is a useful technique to observe such microscopic effects. It is necessary to collect a lot of data of σ (standard deviation) values for various kinds of transistors fabricated by different process conditions. If such data are properly compared and analyzed, it may become possible to extract quantitative information about random fluctuations. Based on this consideration, a simple normalization method for comparing σ values of random threshold voltage fluctuations was proposed. The method was used to compare devices of various origins to analyze the causes of random fluctuations [2.1].

This chapter is divided into two sections. First, we will illustrate the fundamental experimental setup to characterizing CMOS devices. Second, the method of normalizing the V_{th} variation (Takeuchi plot) used in this thesis will be introduced, and its fundamental theory will be described in detail.

2.2 Experimental Setup

The experimental setup for the current-voltage measurement of devices is illustrated in Fig. 2.1. Based on the PC controlled instrument environment by HP-IB (GP-IB, IEEE-488 Standard) interface, the complicated and long-term characterization procedures during analyzing the behaviors in MOSFETs can be easily achieved. As shown in Fig. 2.1, the equipments, including the semiconductor parameter analyzer (HP 4156C), low leakage switch mainframe (HP E5250A), dual channel pulse generator (HP 8110A), cascade guarded thermal probe station and a thermal controller, provides an adequate capability for measuring the device characteristics. In addition, programs written by HT-Basic were used to execute the measurement via HP-IB interface.

2.3 Theory of Takeuchi Plot

It is well known that standard deviation of threshold voltage σV_{th} usually follows a relationship [2.2]

$$\sigma V_{th} = \frac{A_{VT}}{\sqrt{WL}} \tag{2.1}$$

where L is channel length and W is channel width. Here, the coefficient A_{VT} (Pelgrom coefficient) can be taken as a normalized σV_{th} with respect to the channel size, and is often used for evaluating and comparing fluctuations. By using A_{VT}, fair comparison between FETs with different geometry is possible. However, it is not suitable for comparing different kinds of transistors, where gate oxide thickness or threshold voltage is not necessarily identical. According to a simple model [2.3], the σV_{th}

dominated by RDF is expressed by

$$\sigma V_{th} = \frac{q}{C_{inv}} \sqrt{\frac{N_{sub} W_{dep}}{3LW}} \propto N_{sub}^{1/4} \tag{2.2}$$

where $C_{inv} = \varepsilon_{OX}/T_{inv}$ is the electrical gate capacitance per area at inversion, N_{sub} is the channel impurity concentration, and W_{dep} is the width of the channel depletion layer. Note that the dependence on L and W is common to (2.1) and (2.2). At the same time, the $N_{sub}W_{dep}$ term is also included in the theoretical calculation of V_{th} as

$$V_{th} = V_{fb} + \Phi_s + \frac{qN_{sub}W_{dep}}{C_{inv}} \quad . \tag{2.3}$$

By substituting the $N_{sub}W_{dep}$ term in (2.3) into (2.2), we can derive

$$\sigma V_{th} = \frac{q}{C_{inv}} \sqrt{\frac{N_{sub} W_{dep}}{3LW}}$$

$$= \sqrt{\frac{q(V_{th} - V_{fb} - \Phi_s)}{3LWC_{inv}}} = \sqrt{\frac{q}{3\varepsilon_{ox}}} \sqrt{\frac{T_{inv}(V_{th} - V_{fb} - \Phi_s)}{LW}} \tag{2.4}$$

$$= \sqrt{\frac{q}{3\varepsilon_{ox}}} \sqrt{\frac{T_{inv}(V_{th} + V_O)}{LW}} = B_{VT} \sqrt{\frac{T_{inv}(V_{th} + V_O)}{LW}}$$

where T_{inv} is the electrical gate oxide thickness at inversion, and V_O is defined as

$$V_O \equiv -V_{fb} - \Phi_s \cong 0.1V. \tag{2.5}$$

Here, V_{fb} is the flat-band voltage, and Φ_S is the surface band bending at inversion.

Equation (2.4) indicates that σV_{th} is proportional to $\sqrt{T_{inv}(V_{th}+V_O)/LW}$. In the Takeuchi plot, σV_{th} is normalized by $\sqrt{T_{inv}(V_{th}+V_O)/LW}$. Here, T_{inv}, V_{th} , V_O, L and W are the median values of the devices.

As an example, the measured data for σV_{th} are plotted in Fig. 2.2(a). The slope A_{VT} is a conventional index of V_{th} variation and depends on V_{th} and T_{inv}. The measurement of σV_{th} is also plotted with a different x-axis as shown in Fig. 2.2(b), where the slope is defined as B_{VT} [2.4]. The slope is an indicator of V_{th} variation. It is found that B_{VT} remains constant with varying V_{th} and T_{inv}. It is due to V_{th} variation normalized in terms of T_{inv} and V_{th}. Therefore, B_{VT} is a useflu tool to investigate the origins of V_{th} variation.

Moreover, when V_{th} variation is dominated solely by RDF, the analytically calculated B_{VT} equals $\sqrt{q/3\varepsilon_{ox}}$ (about 1.2). Since the analytical calculation does not take the effect of the discreteness of the channel dopant on the channel surface direction into account, it underestimates B_{VT}. According to the 3-D technology computer-aided design (3-D-TCAD) calculation, which takes the discreteness of the channel dopant fully into account, B_{VT} of RDF is 1.5 [2.1]. In Fig. 2.3, B_{VT} of PMOS is 1.7 and close to that of RDF (which is 1.5). This result indicates that the V_{th} variation of PMOS is dominated by RDF [2.5-2.9]. B_{VT} of NMOS is 2.7 and larger than that of RDF (which is 1.5). This result indicates that V_{th} variation of NMOS is dominated not only by RDF but also by other factors.

To explain the larger B_{VT} of NMOS, a Boron clustering model is proposed. In general, it is well known that Boron atoms with high concentration are clustered in Si [2.10]. Some Boron atoms of channel dopants gather with weak binding force and act as one Boron cluster. In this case, the charge of a carrier q is replaced with nq and

N_{SUB} is replaced with N_{SUB}/n. V_{th} is not changed by these replacements, i.e.,

$$V_{th} = V_{fb} + \Phi_s + \frac{qN_{sub}W_{dep}}{C_{inv}} \tag{2.6a}$$

$$\text{and} \quad V_{th} = V_{fb} + \Phi_s + \frac{(nq)(N_{sub}/n)W_{dep}}{C_{inv}}. \tag{2.6b}$$

σV_{th} increases by a factor of $\sqrt{n}$, i.e.,

$$\sigma V_{th} = \frac{q}{C_{inv}}\sqrt{\frac{N_{sub}W_{dep}}{3LW}} \tag{2.7a}$$

$$\sigma V_{th} = \frac{nq}{C_{inv}}\sqrt{\frac{(N_{sub}/n)W_{dep}}{3LW}} = \sqrt{n}\,\frac{q}{C_{inv}}\sqrt{\frac{N_{sub}W_{dep}}{3LW}}. \tag{2.7b}$$

As a result, B_{VT} increases by a factor of $\sqrt{n}$, i.e.,

$$\sqrt{\frac{q}{3\varepsilon_{ox}}} \Rightarrow \sqrt{\frac{nq}{3\varepsilon_{ox}}}. \tag{2.8}$$

Fig. 2.4 shows the relationship between B_{VT} and the number of clustering Boron atoms, n, calculated by the analytical and 3-D-TCAD calculation [2.11]. On the basis of the 3-D-TCAD calculation and measured B_{VT} of 2.7, actual B_{VT} can be explained by a cluster of five Boron atoms.

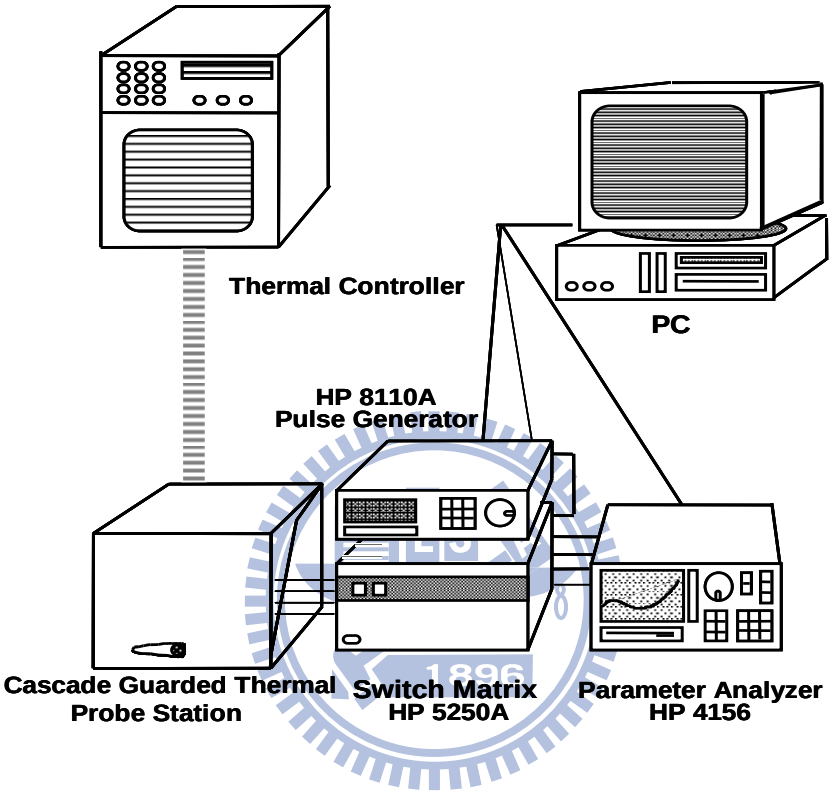


Fig. 2.1 The experimental setup for the current-voltage measurement of MOSFETs. Automatic controlled characterizations system is setup based on the PC controlled instrument environment.

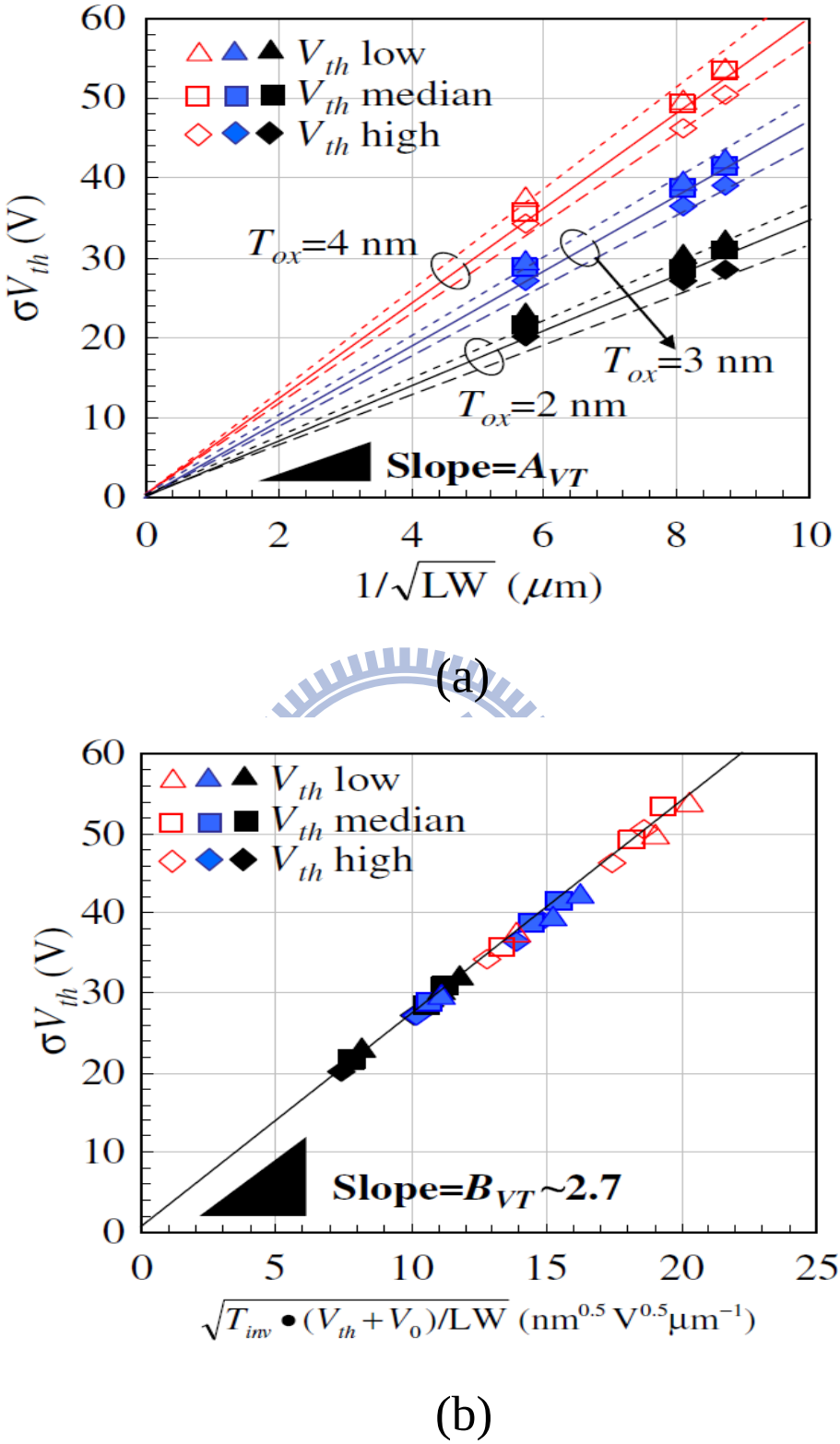


Fig. 2.2 Measured NMOS V_{th} variation with (a) slope A_{VT} and (b) slope B_{VT}. The slope A_{VT} depends on V_{th} and T_{inv} while B_{VT} does not [2.4].

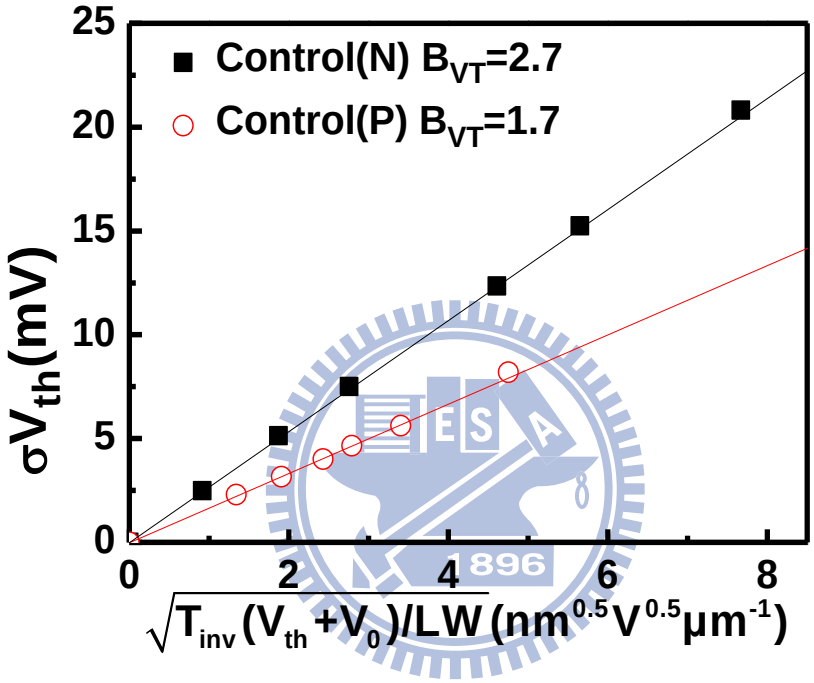


Fig. 2.3 Example of Takeuchi plots for NMOS and PMOS. B_{VT} of NMOS is larger than that of PMOS.

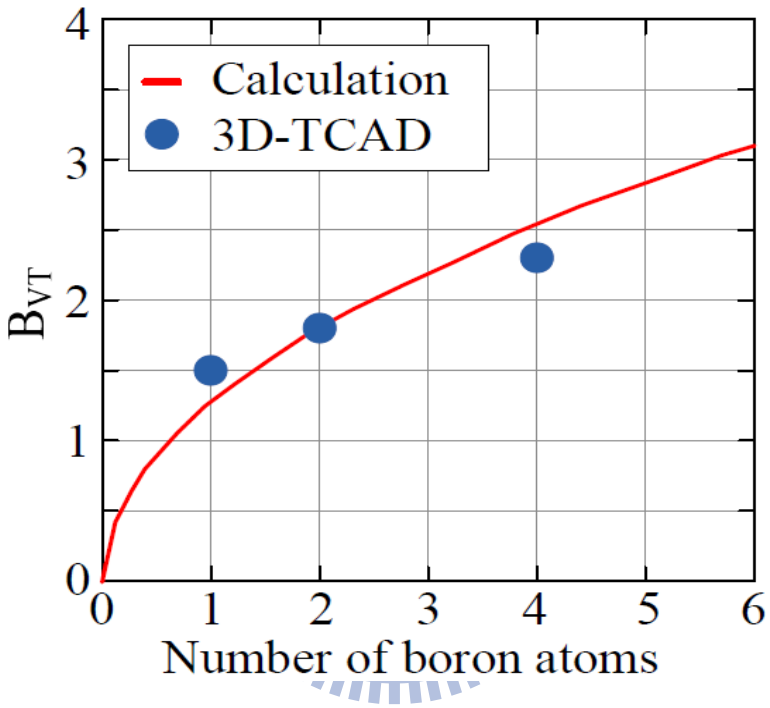


Fig. 2.4 The analytical calculation and the 3D-TCAD simulation results of a Boron clustering model [2.11].

Chapter 3

The Variability of Strained n-MOSFETs

3.1 Introduction

Recently, researches have shown an increasing interest in the strain technology. Strained silicon technology is essential for the continuation of the scaling in MOSFET devices, owing to its high impact on carrier mobility and thus on drive current improvement [3.1]. When applied to the direction of the channel, tensile strain improves the performance of n-MOSFET devices, while compressive strain is beneficial for p-MOSFET devices. The local strain, such as capping layer, SiGe on S/D, and SiC on S/D are induced by the process. They are usually uniaxial strain. Compared to the global strain usually biaxial strain, the local strain has less dislocation issues.

However, as the devices are scaled, a variety of process-induced variations become more obvious. One of the most critical issues is V_{th} variation. Random dopants in the channel and source/drain regions are the dominant source of V_{th} variation in scaled bulk CMOS. It already profoundly affects the SRAM design [3.2] and, in logic circuits, causes statistical timing problems [3.3]. In both cases, statistical variability restricts threshold and supply voltage scaling, causing static and dynamic power dissipation problems [3.4].

In this chapter, we will demonstrate V_{th} variation which can be suppressed by advanced strained-Si technology meanwhile the performance of devices keeps improved for n-MOSFETS. Extensive comparisons between strained and control

n-MOSFETs will be justified on examining the effects of temperature, drain bias, and substrate bias. In addition, the impact of stress-induced random interface traps fluctuation (RIF) on the device variability will also be verified.

3.2 Device Preparation

The devices were fabricated by the advanced 40nm CMOS technology at UMC. The schematic cross section diagram of n-MOSFET splits is shown in Fig. 3-1. In this figure, Fig. 3-1(a) is the control device, Fig. 3-1(b) is the SiC on S/D device (uniaxial-strain) and Fig. 3-1(c) is the SiC on S/D-E device (uniaxial-strain). Both n-MOSFETs are <100> channel on (100) substrate. All these test devices have 12Å EOT gate oxide with SiON process. Devices with various areas were measured for Takeuchi plots. The device threshold voltage was measured by the extrapolation and constant current method.

3.3 Performance of Strained n-MOSFETs

In Fig. 3.2, the I_{on}-I_{off} curve of the SiC S/D-E devices show 23.6% current gain over the control (bulk-Si) and 13% improvement for typical SiC S/D devices. Moreover, Fig. 3.3 shows 67% enhancement of $I_{D,sat}$ for the SiC S/D-E devices over the control. As shown in Fig. 3.4, the peak mobility of the SiC S/D-E devices exhibits a 94% increase in comparison to the control.

3.4 Variability of Strained n-MOSFETs

Figure 3.5 shows the Takeuchi plot of the n-MOSFET splits, in which the B_{VT} of strained devices are smaller than that of control. In particular, SiC S/D-E shows the

reduction of 26% to the control in Fig. 3.6. To explain the smaller B_{VT} of strained devices, we consider that the strain effect could reduce the number of clustering Boron atoms by using Boron clustering model [3.5]. In addition, the Carbon diffuses out to the vicinity of S/D junction and substrate region is also capable of describing the suppression of V_{th} variation. The diffusion of interstitial diffuser species such as Boron through annihilation of interstitials (Boron TED) will be reduced by the Carbon, resulting in decreasing V_{th} variation [3.6-3.7]. In other words, as the stressors (Carbon) diffuse out to the vicinity of S/D junction and channel region, the effective dopant concentration is decreased, and V_{th} fluctuation is improved. Moreover, the SiC S/D and SiC S/D-E with low C% have larger B_{VT} than that of SiC S/D-E due to less channel strain effect [3.8]. Therefore, the more the strain in channel is, the smaller the B_{VT} of device becomes.

3.5 Factors Affecting the V_{th} Variation

3.5.1 Effect of the Temperature

To understand the effect of the temperature on strained n-MOSFETs, devices are measured at elevated temperature (85^{O}C). It was found that B_{VT} is larger at 85^{O}C in Fig. 3.7 for all the n-MOSFET device splits. As the temperature increases, the thermal fluctuation of the lattice becomes larger. The carrier moving through the crystal is easier to be scattered by a vibration of the lattice results in enhanced B_{VT}. Moreover, a higher leakage current of device at elevated temperature is also a source of increasing B_{VT}, i.e.,

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{q(V_g - V_{th})/mkT} \left(1 - e^{-qV_{ds}/kT}\right) \quad (3.1)$$

where m is the body effect coefficient [3.9]. Therefore, the V_{th} variation is increased as the device is heated. Also, the result shows the amount of enhanced B_{VT} of SiC S/D and SiC S/D-E is similar to that of control which exhibits no degradation compared to the control.

3.5.2 Effect of the Drain Bias

The effect of the drain bias (V_{DS}) on V_{th} variation was also examined. Fig. 3.8 shows the V_{th} variation increases with increasing drain bias. This is because the depletion region around the drain junction becomes wider as the drain bias increases such that more ionized impurities are produced. SiC S/D and SiC S/D-E exhibit weak dependence of V_{th} variation on the drain bias as a result of the strain effect. Because there are less Boron atoms clustered in strained-Si, the effect of RDF becomes minor. It indicates good SCE immunity (small DIBL) and this immunity is a primary requirement for small variability because devices are operated at high drain bias.

3.5.3 Effect of the Substrate Bias

Dependence of B_{VT} on substrate bias (V_{BS}) is shown in Fig. 3.9. B_{VT} increases as substrate bias increases. It is well known that ionized impurities in depletion region are the major source of V_{th} variation. By applying substrate bias, more ionized impurities are produced since the bulk depletion width becomes wider results in enhanced B_{VT}. Also, based on the same reasoning as that in section 3.4.2, SiC S/D and SiC S/D-E show better B_{VT} as substrate bias increases due to the strain effect which could reduce V_{th} variation.

3.5.4 Discussion of the Bias Effect

Figure 3.10 shows the variances in depletion width under different bias conditions. It is well known that the depletion width increases with increasing bias. Moreover, random ionized impurities in the depletion region are the dominant source of V_{th} variation. As substrate concentration is increased, RDF becomes more serious since V_{th} variation is proportional to $N_{sub}^{1/4}$ as derived in section 2.3, i.e.,

$$\sigma V_{th} = \frac{q}{C_{inv}} \sqrt{\frac{N_{sub} W_{dep}}{3LW}} \propto N_{sub}^{1/4}. \tag{3.2}$$

Therefore, it is expectable that the effects of drain and substrate bias become more dramatic as the substrate concentration is increased.

3.6 Impact of Stress-induced Random Interface traps

3.6.1 Introduction

A large number of variation effects of both types have been revealed in many studies. Examples include: random dopant fluctuation (RDF) [3.10], line-edge roughness (LER) [3.11-3.12], and local oxide thickness variations [3.13]. In addition to these effects, recent study [3.14] has proved that process-induced random interface traps fluctuation (RIF) are required for proper interpretation of V_{th} variation in CMOS technologies. However, so far, none has been reported on the effect of stress-induced random interface traps. Thus, in this section, we will discuss the device variability after FN and PBTI stresses.

3.6.2 Charge Pumping Measurement

The charge pumping (CP) measurement is efficient for the reliability characterization. However, the charge pumping measurement can't be used reliably in the small size devices due to the small charge pumping current and the gate leakage current. Recently, a low leakage Incremental Frequency Charge Pumping (IFCP) measurement for CMOS devices has been developed [3.15] to get more reliable results. Since charge pumping current is proportional to the generated interface traps, we use IFCP to evaluate the interface traps for the stressed devices.

3.6.3 Variability After FN Stress

Figure 3.11 shows the measured I_{CP} for studying the vertical field effect using FN stress (V_{GS}-V_{th}= 2V for 300sec). It is observed that the I_{CP} of SiC S/D-E is larger than the others which could be attributed to the Carbon out-diffusion [3.16] and the I_{CP} of SiC S/D is the smallest one which exhibits better reliability. The average interface traps generation among these three devices during stress time, from 100sec to 500sec, is shown in Fig. 3.12. The number of interface traps increases with increasing stress time. Since the positions and number of charges trapped at the SiO_2/Si interface randomly vary, it is possible for this variation to affect the V_{th} variation [3.17]. Thus, the comparison of B_{VT} during stress time is shown in Fig. 3.13 to verify the possibility. Also, Fig. 3.14 shows the relationship of B_{VT} with interface traps. It is obvious that B_{VT} is aggravated after FN stress. Moreover, the aggravated B_{VT} is proportional to interface traps. This result indicates that stress-induced interface traps are the dominant source of the enhanced V_{th} variation after FN stress.

3.6.4 Variability After PBTI Stress

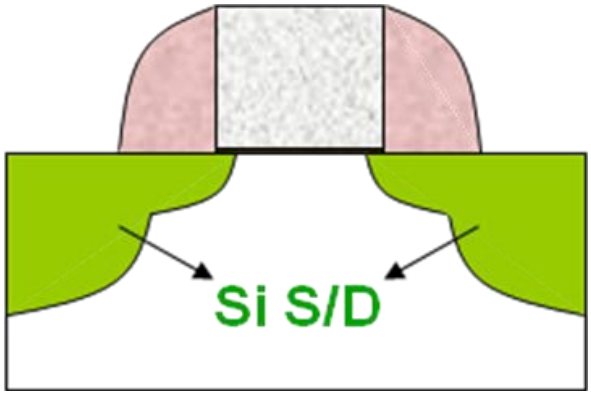
By applying similar analysis, we apply the PBTI stress (V_{GS}-V_{th}= 2V at 85℃) to produce the interface traps at the SiO_2/Si interface which would show a more aggravated B_{VT}. Fig. 3.15 shows the measured I_{CP} after PBTI stress (V_{GS}-V_{th}= 2V for 300sec, at 85℃). Based on the same reasoning as described in 3.5.3, the I_{CP} of SiC S/D-E is larger than the others. In addition, the I_{CP} of all n-MOSFET splits after PBTI stress are larger than that of FN stress. It indicates that more interface traps are produced after PBTI stress as shown in Fig. 3.16. Fig. 3.17 shows the comparison of B_{VT} during stress time. Fig. 3.18 shows the relationship of B_{VT} with interface traps. We observe a more aggravated B_{VT} after PBTI stress which is attributed to the more interface traps generation, but the aggravated B_{VT} is also proportional to interface traps.

3.6.5 Discussion

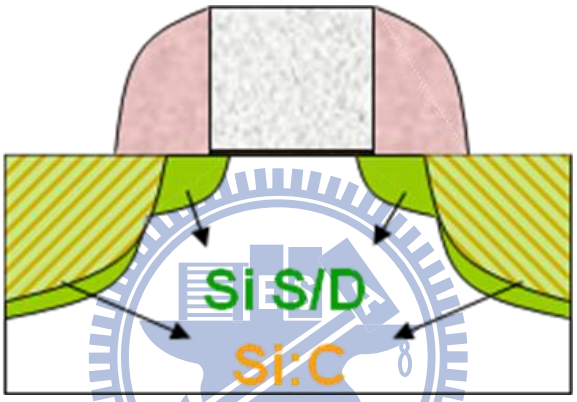
Figure 3.19(a)-(b) show the enhanced B_{VT} during FN and PBTI stress. The results give us a more specific evidence to confirm the interface traps which results from the FN and PBTI stress would enhance V_{th} variation, i.e. $\sigma(V_{th})^2 = \sigma(\text{dopant})^2 + \sigma(N_{it})^2$. In addition, this result shows that the control of the interface quality in SiC S/D and SiC S/D-E is very important and even more than in control devices.

It was also found that the amount of enhanced B_{VT} is larger in strained devices. The distance between inversion layer electrons and interface traps located at the SiO_2/Si interface can be a key parameter to explain the impact of strain on the enhanced B_{VT}. Fig. 3.20 schematically shows the electron distributions in the Δ2 and Δ4 valleys in the inversion triangular potential, as well as the location of N_{it} and N_{sub}

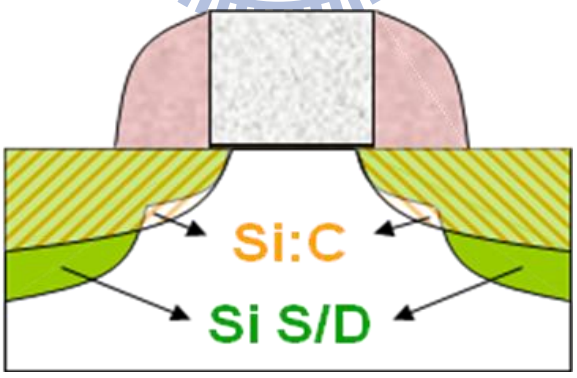
scattering centers [3.18]. It is well known that in strained-Si, most electrons are in the twofold valleys (Δ2) where the electron distribution is more confined near the interface than in the fourfold valleys (Δ4). Thus, the Coulomb scattering limited by interface traps becomes strong causing a great impact on enhanced V_{th} variation.



(a)



(b)



(c)

Fig. 3.1 The cross-section view of the experimental devices. (a) control, (b) SiC S/D (uniaxial-strain), and (c) SiC S/D-E devices (uniaxial-strain). All of them are <100> channel on (100) substrate.

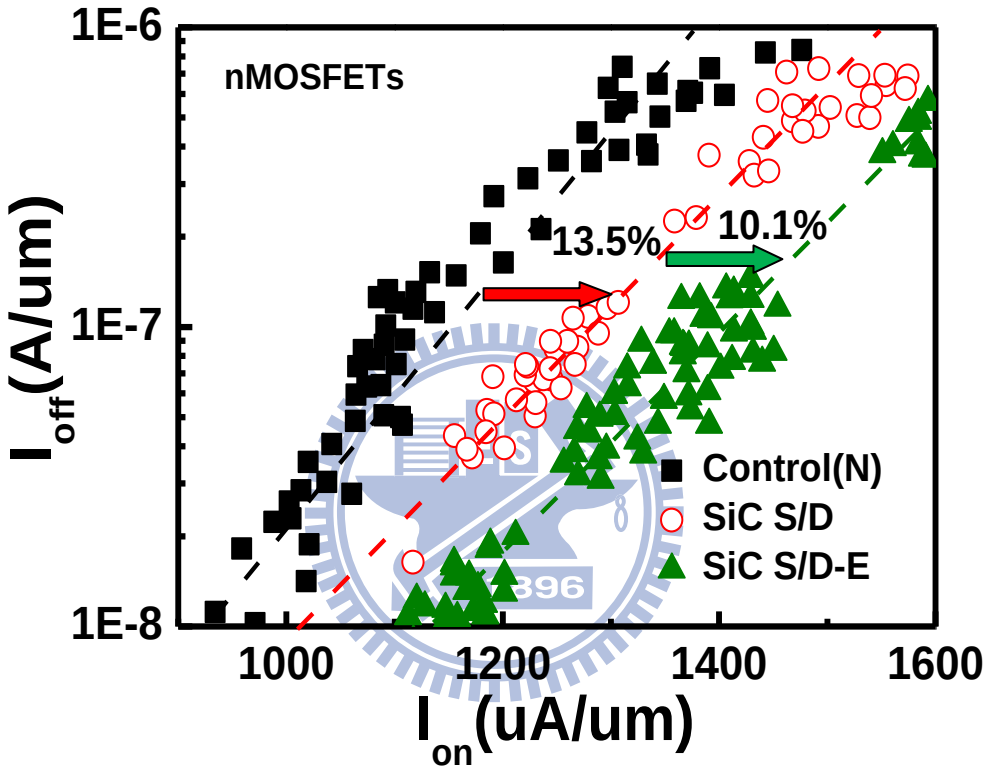


Fig. 3.2 The I_{on}-I_{off} characteristics of all the nMOSFET devices. SiC S/D-E device can improve the driving current by an increment of 23% over the control (Si-bulk).

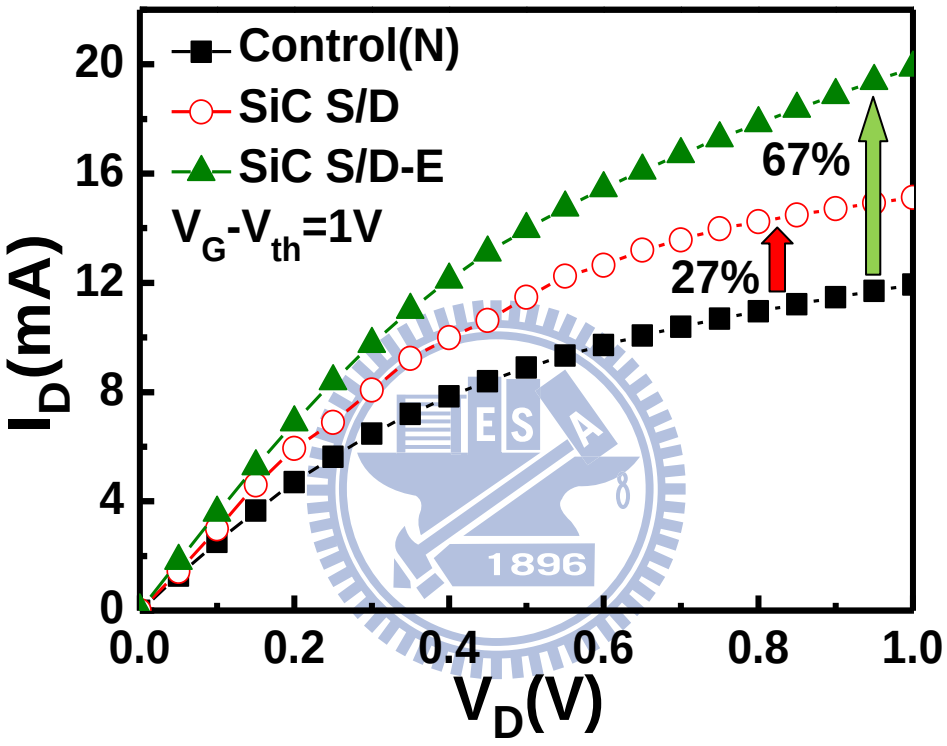


Fig. 3.3 The I_D-V_D curves of the splits and control. The SiC S/D-E device shows 67% $I_{D,sat}$ enhancement over control devices.

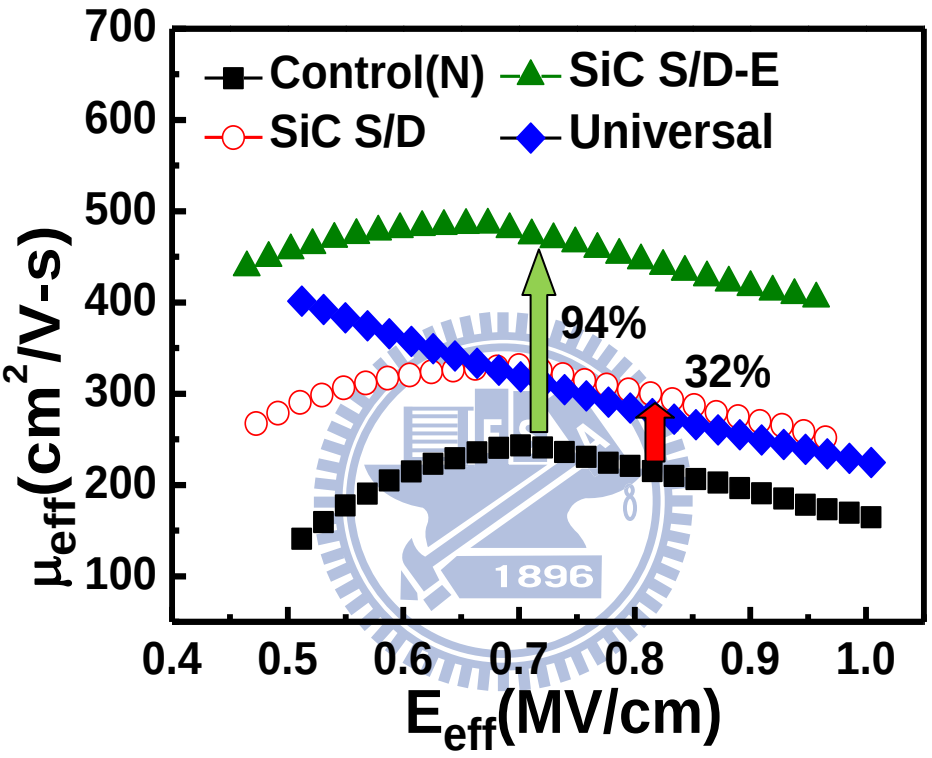


Fig. 3.4 A 94% electron mobility enhancement is obtained for the long SiC S/D-E device compared to the control.

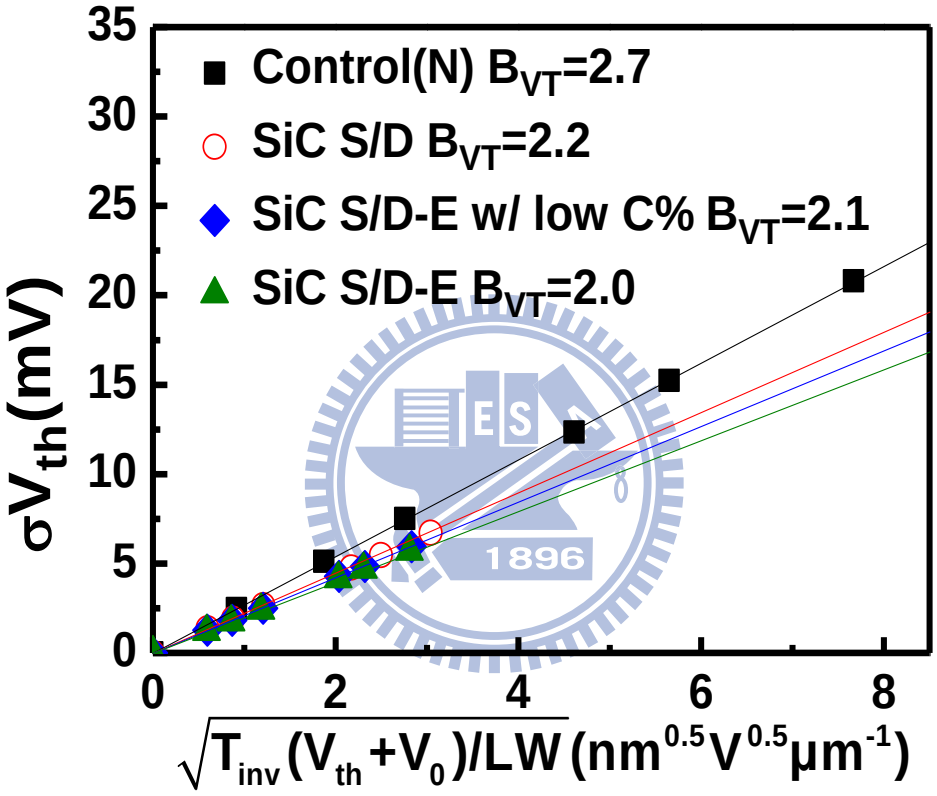


Fig. 3.5 Takeuchi Plots of n-MOSFETs. The slope indicates the value of B_{VT}.

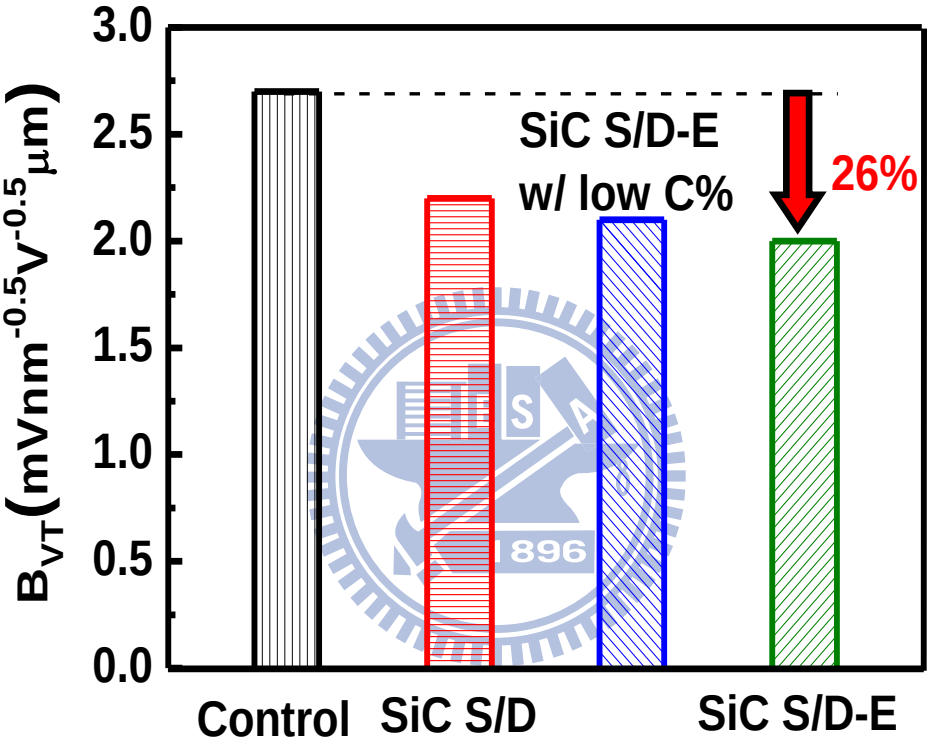


Fig. 3.6 Comparison of B_{VT} for n-MOSFETs. B_{VT} of SiC S/D-E shows a 26% improvement to the control.

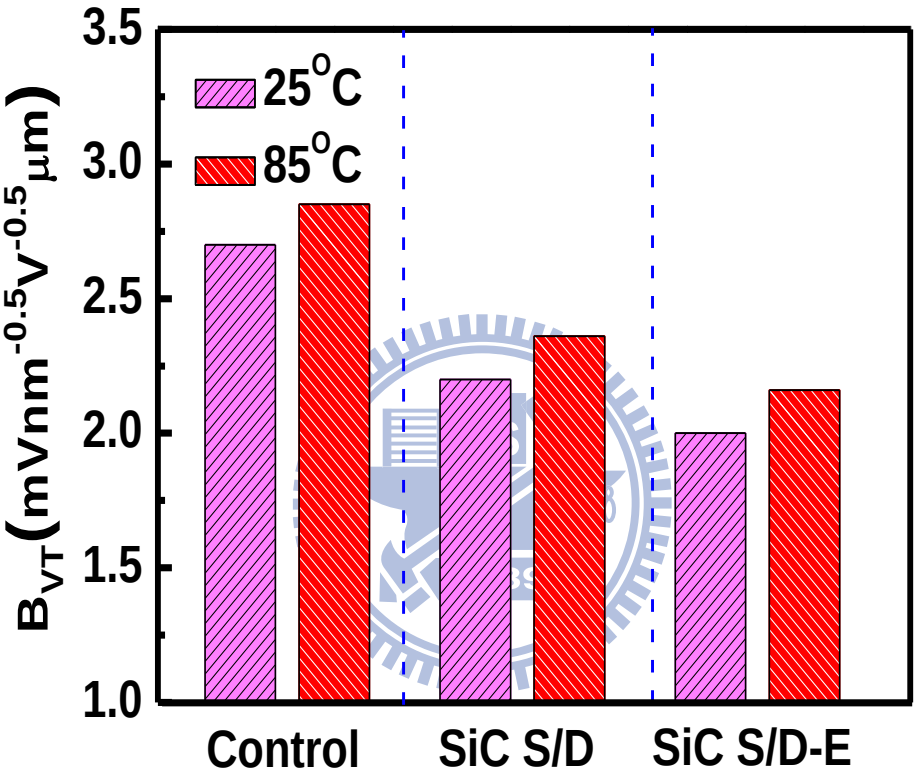


Fig. 3.7 Dependence of B_{VT} on the temperature. Strained devices show no degradation compared to control devices.

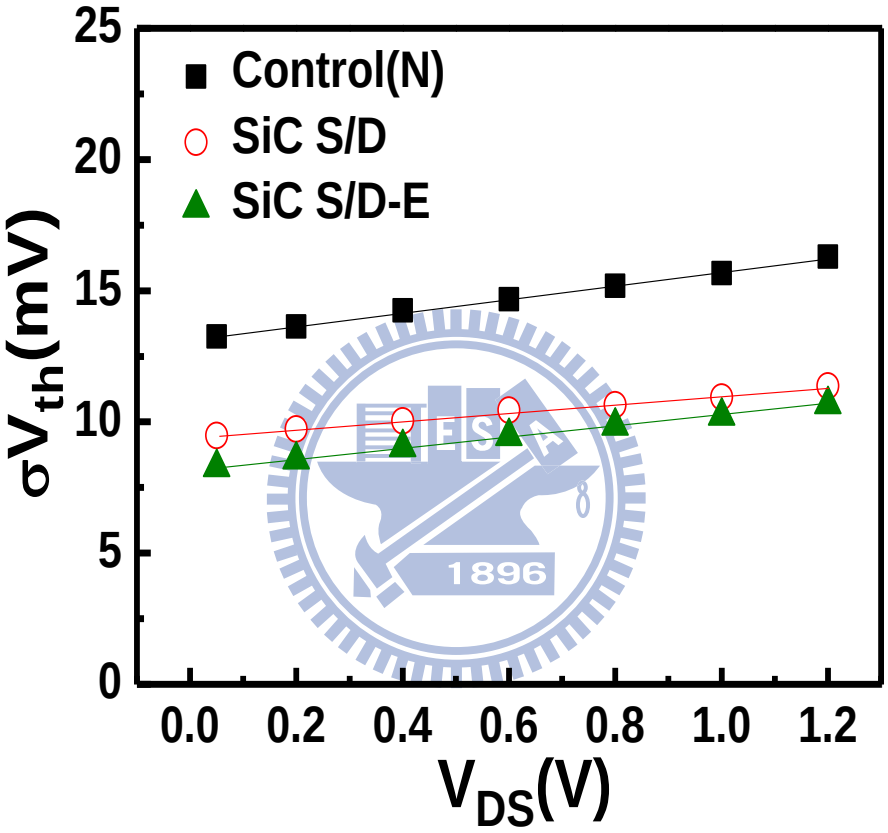


Fig. 3.8 V_{DS} dependence of σV_{th}. Strained devices exhibit weak dependence of V_{th} variation on the drain bias.

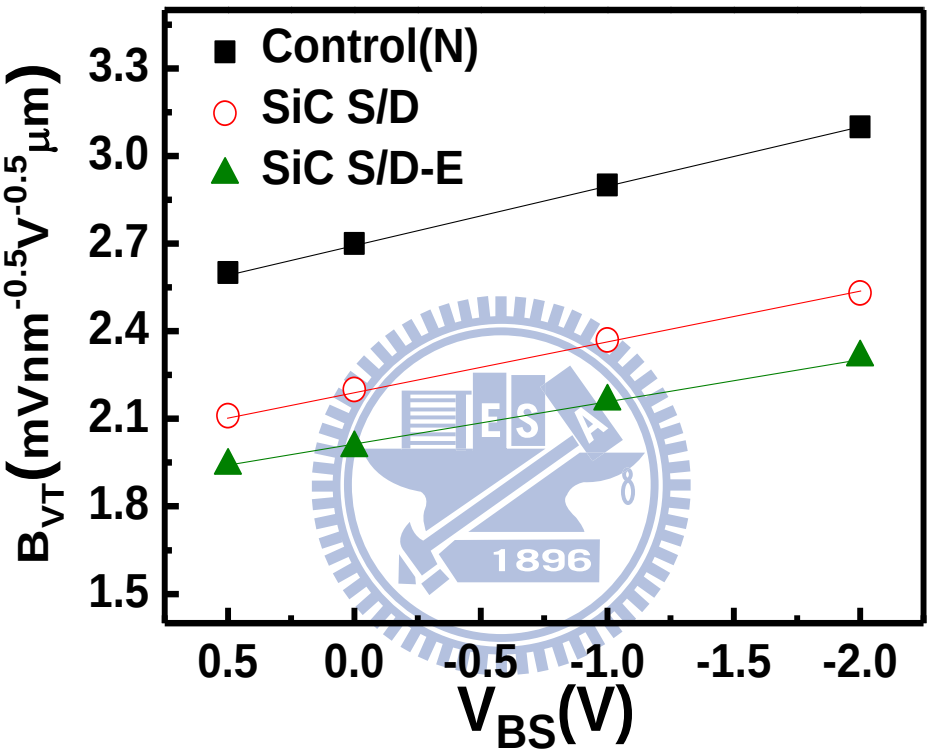


Fig. 3.9 Dependence of B_{VT} on V_{BS}. Strained devices show better B_{VT} as substrate bias increases.

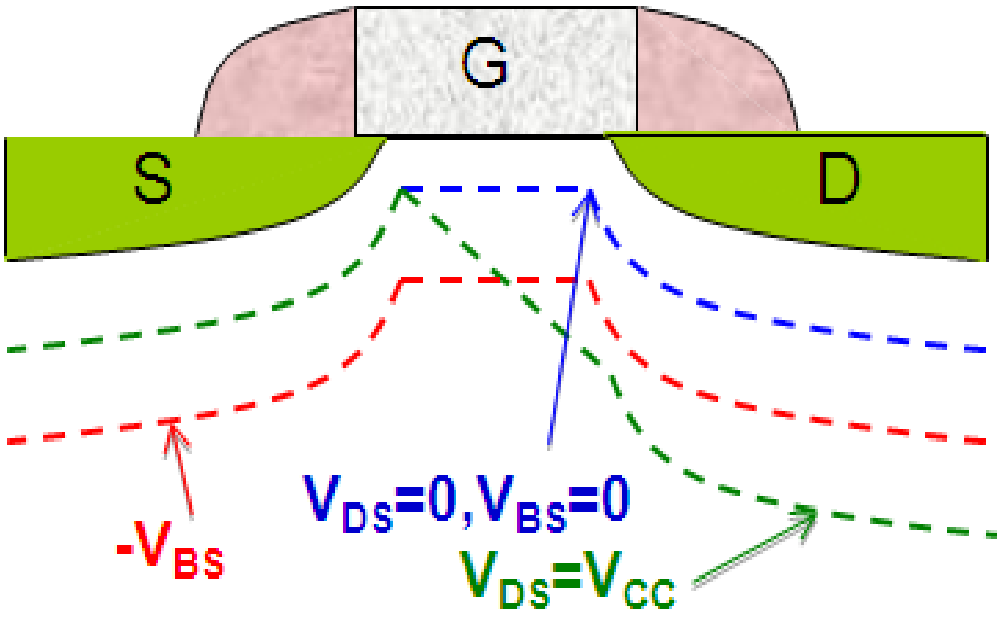


Fig. 3.10 Schematic diagram of the depletion region profile under different bias conditions.

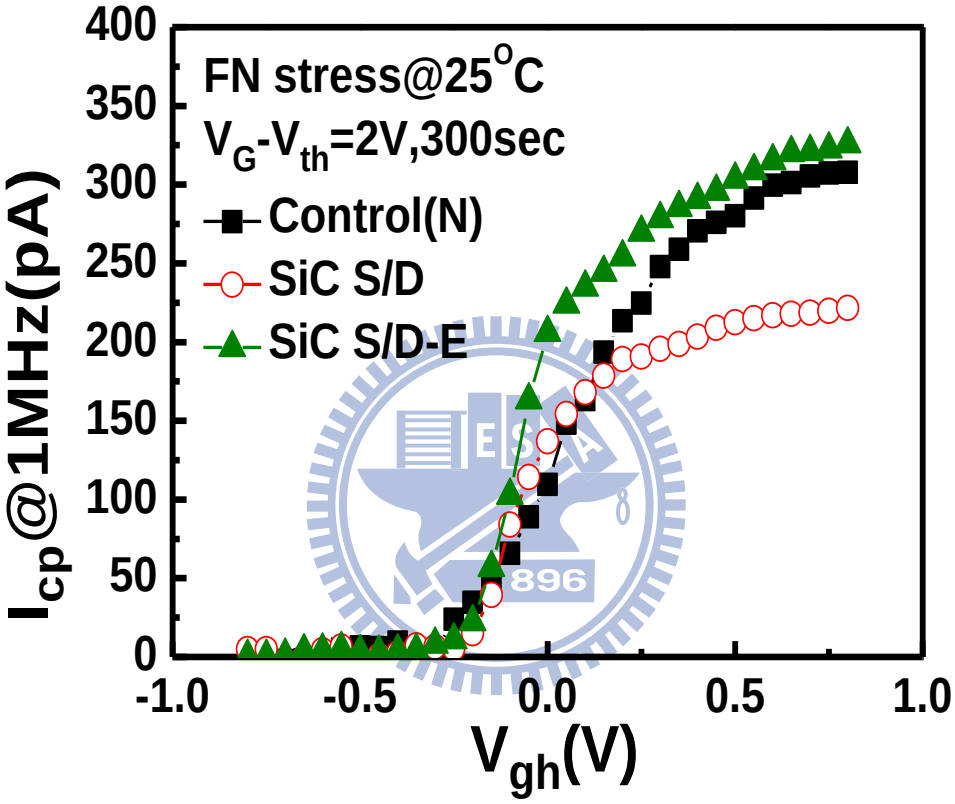


Fig. 3.11 The charge pumping currents of all the n-MOSFETs after FN stress.

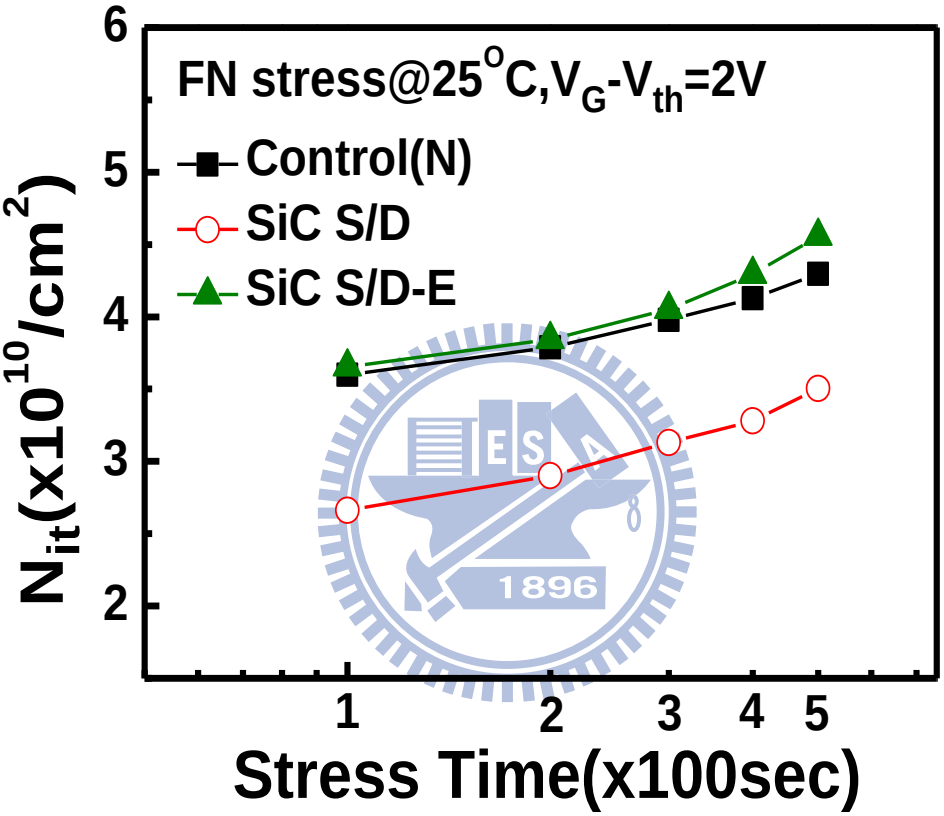


Fig. 3.12 The average interface traps of all the n-MOSFETs after FN stress.

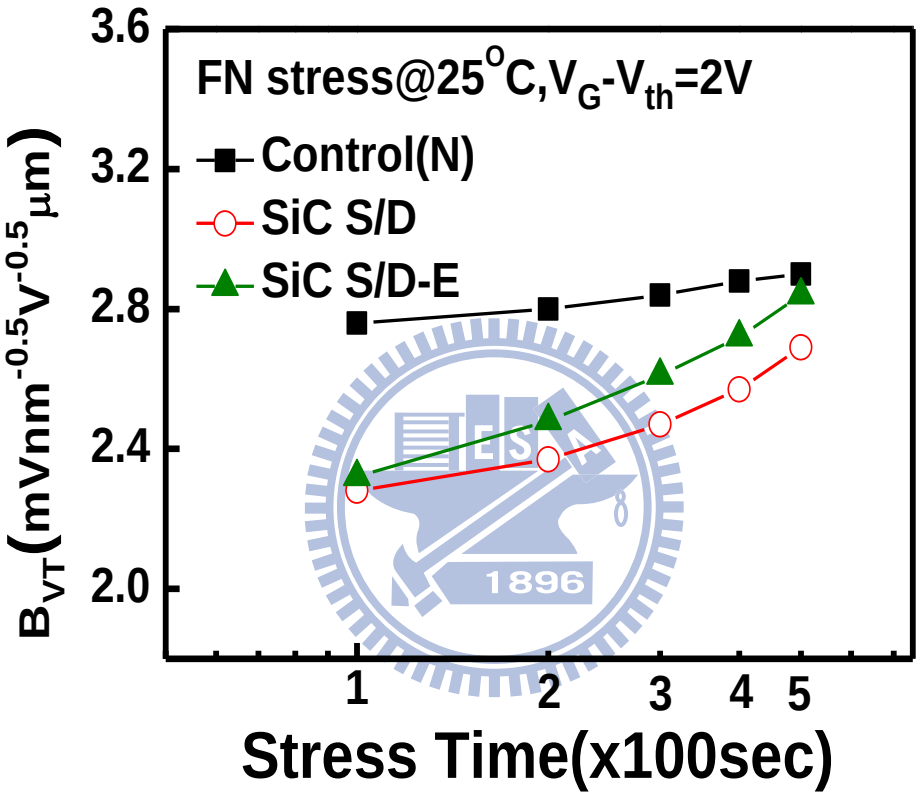


Fig. 3.13 The evolution of B_{VT} for all the n-MOSFETs during FN stress.

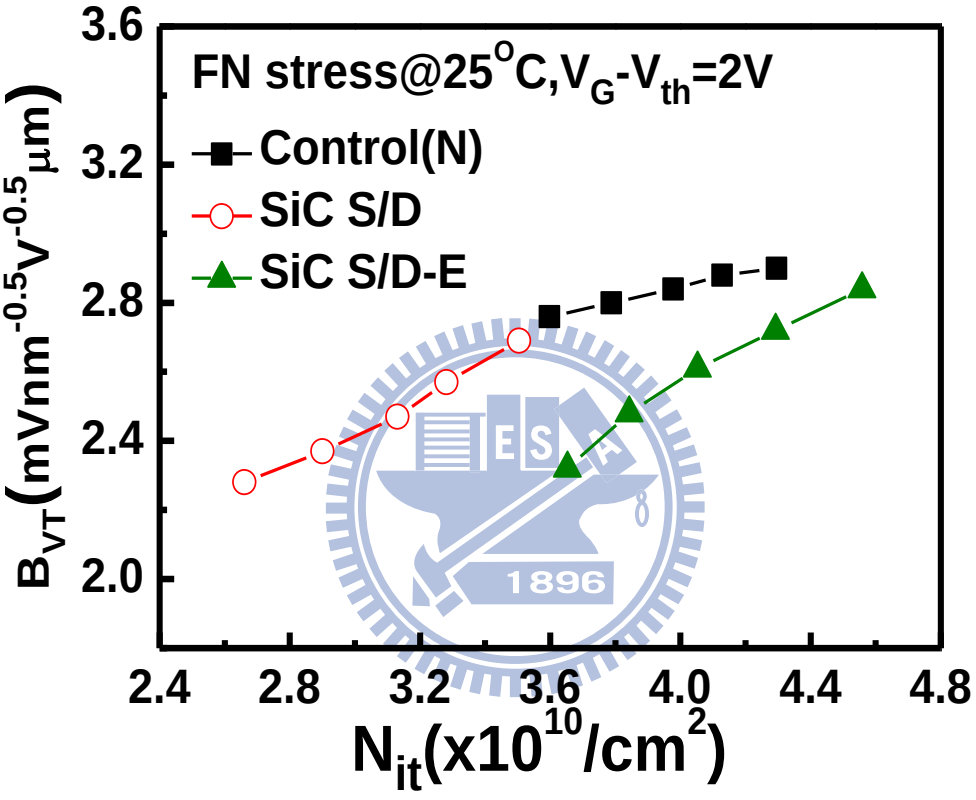


Fig. 3.14 Relationship of B_{VT} with interface traps for all the n-MOSFETs after FN stress.

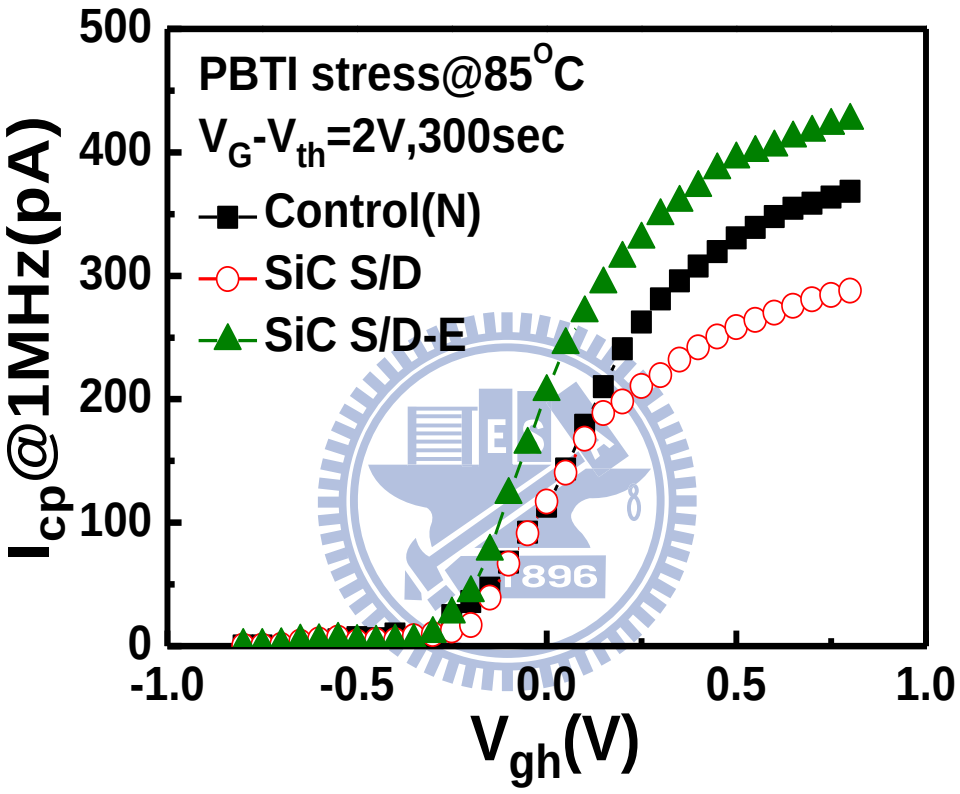


Fig. 3.15 The charge pumping currents of all the n-MOSFETs after PBTI stress.

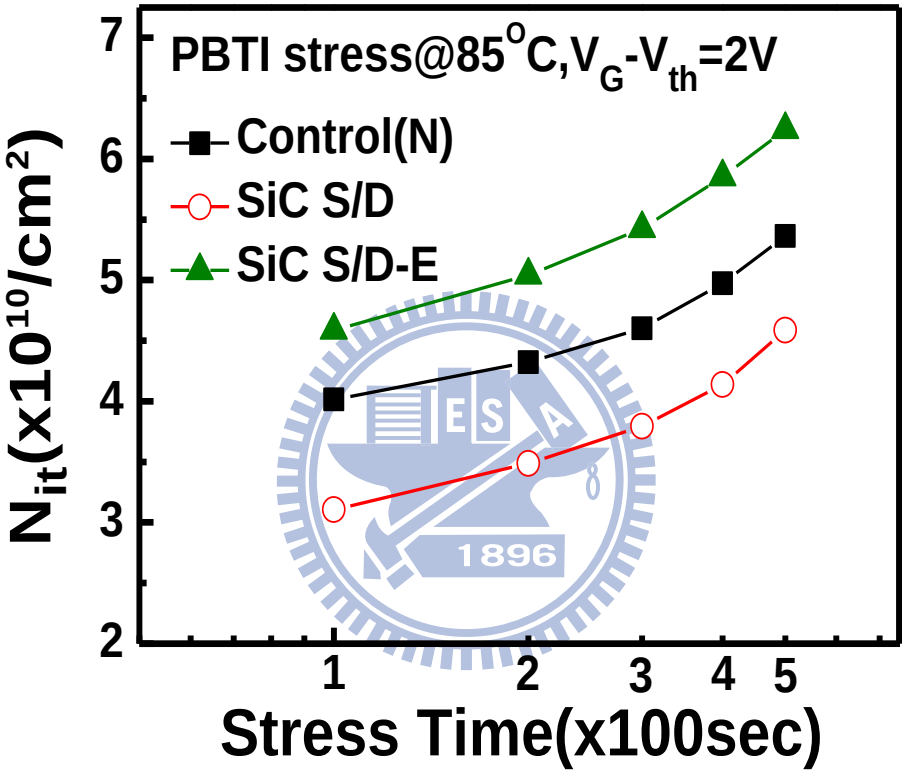


Fig. 3.16 The average interface traps of all the n-MOSFETs after PBTI stress.

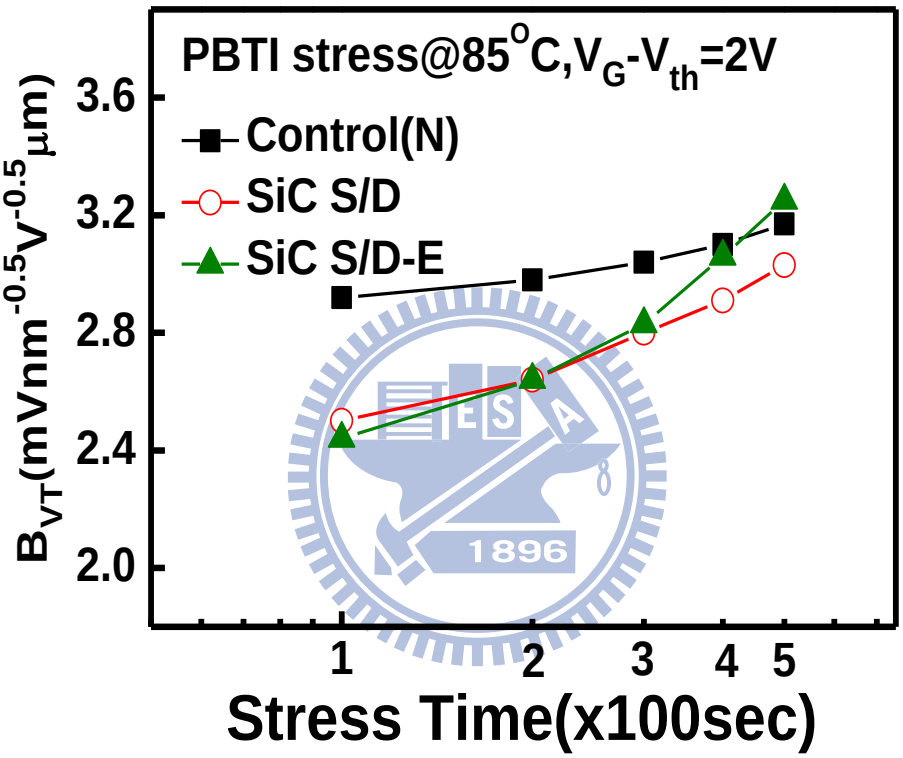


Fig. 3.17 The evolution of B_{VT} for all the n-MOSFETs during PBTI stress.

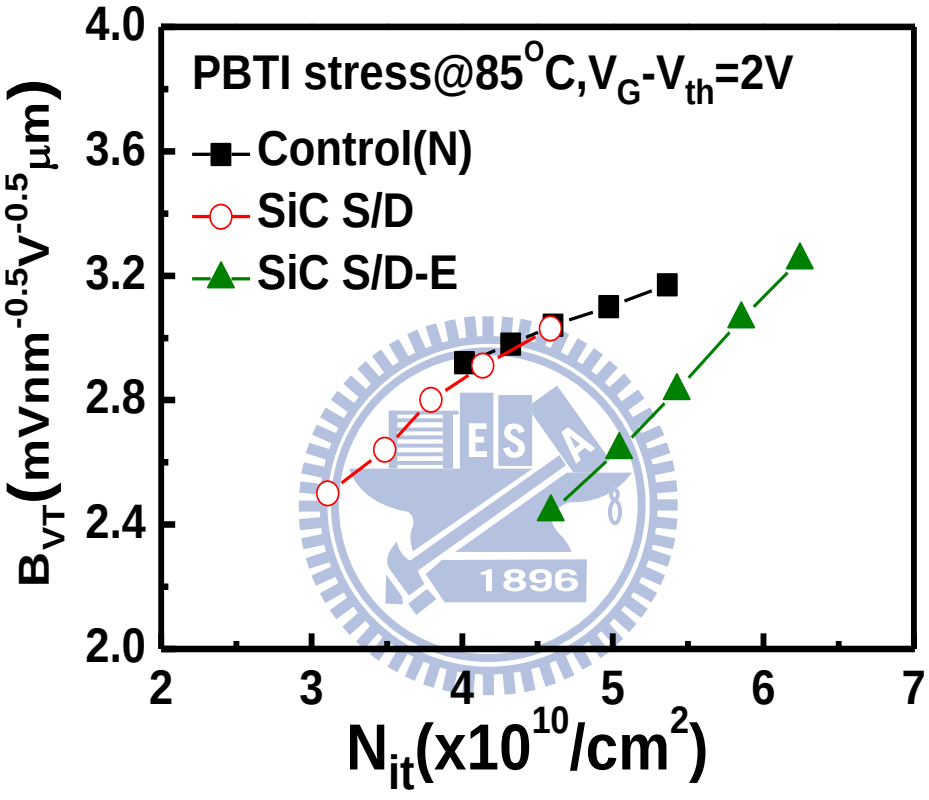
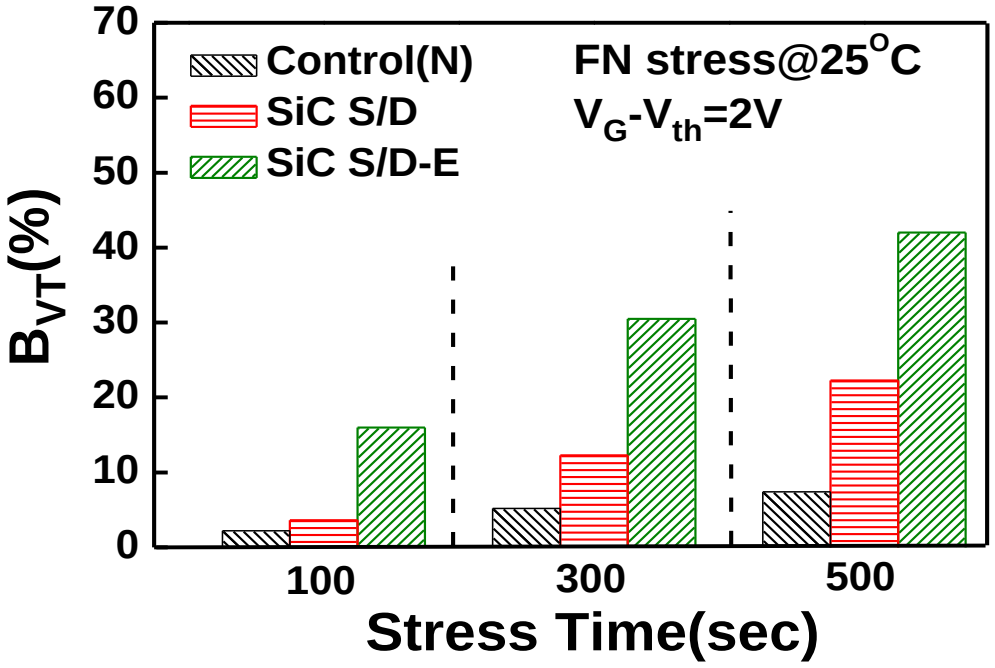
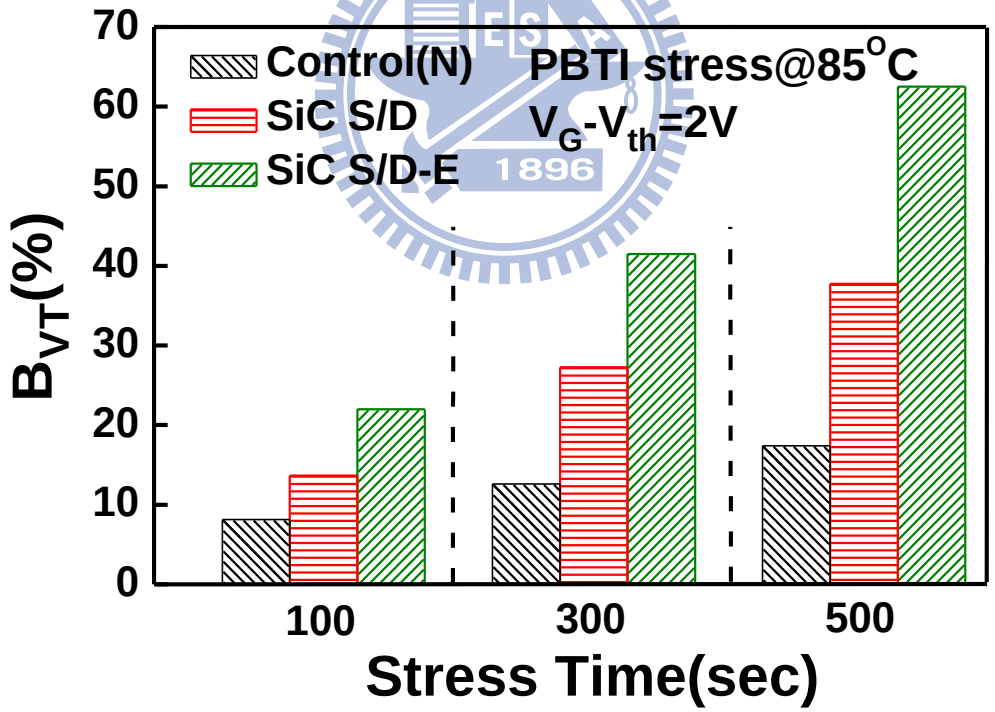


Fig. 3.18 Relationship of B_{VT} with interface traps for all the n-MOSFETs after PBTI stress.



(a)



(b)

Fig. 3.19 The enhanced B_{VT} caused by stress-induced interface traps during (a) FN stress and (b) PBTI stress.

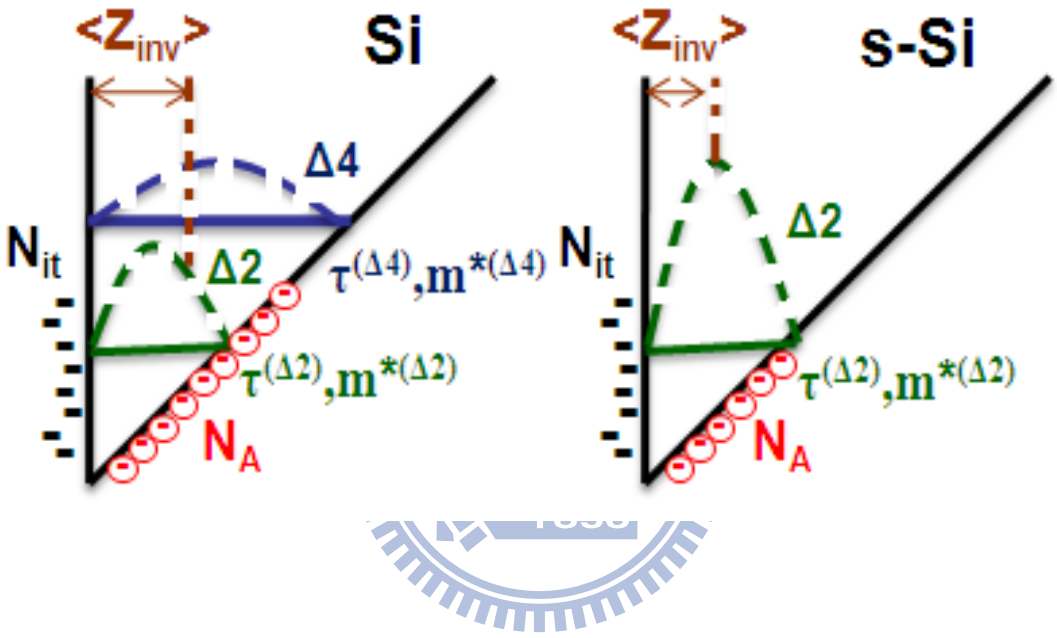


Fig. 3.20 Schematics of the valley configuration in Si and strained-Si inversion layers to illustrate the larger σV_{th} in strained devices after stress.

Chapter 4

Variability of Strained p-MOSFETs

4.1 Introduction

Mobility enhancement is a method to improve the CMOS devices performance with the scaling of the device size. The increase of carrier mobility is necessary to realize the high-speed logic CMOS devices. Recently, various strain technologies have been utilized to enhance the drive current. It is necessary to understand the introduced uniaxial and biaxial strains in n-MOSFET or p-MOSFET devices. Initially, the typical mobility enhancement of n-type strained-Si is much larger than that of p-type devices. Several techniques have been further developed to enhance the p-MOSFET performance, i.e., SiGe on S/D device [4.1]. Materials with same crystal structure but different lattice are good candidates for the strain engineering. The SiGe has been successfully incorporated in the source and drain of p-MOSFET devices to strain the channel compressively and increase the hole mobility. However, as the devices being scaled, a variety of process-induced variations will need to be overcome. One of the most critical issues is V_{th} variation. We have demonstrated in previous chapter that strained n-MOSFET with embedded SiC on source and drain could suppress variability.

In this chapter, we will demonstrate V_{th} variation is suppressed by advanced strained-Si technology meanwhile the performance of devices keeps improved for p-MOSFETs. Extensive comparisons between strained and control p-MOSFETs will be justified on examining the effects of temperature, drain bias, and substrate bias. In addition, the impact of stress-induced random interface traps fluctuation (RTF) on the

device variability will be also verified.

4.2 Device Preparation

The devices were fabricated by the advanced 40nm CMOS technology at UMC. The schematic cross section diagram of p-MOSFET splits is shown in Fig. 3-1. In this figure, Fig. 4-1(a) is the control device, Fig. 4-1(b) is the SiGe on S/D device (uniaxial-strain) and Fig. 4-1(c) is the SiGe on S/D with EDB (Embedded Diffusion Barrier, an undoped SiGe layer) device (uniaxial-strain). Both p-MOSFETs are <110> channel on (100) substrate. All these test devices have 12Å EOT gate oxide with SiON process. Devices with various areas were measured for Takeuchi plots. The device threshold voltage was measured by the extrapolation and constant current method.

4.3 Performance of Strained p-MOSFETs

In Fig. 4.2, the I_{on}-I_{off} curve of the SiGe S/D devices show 51% current gain over the control (bulk-Si) and 24% improvement for SiGe S/D w/ EDB devices. Moreover, Fig. 4.3 shows 38% and 18% enhancement of $I_{D,sat}$ for the SiGe S/D and SiGe S/D w/ EDB devices over the control, respectively. As shown in Fig. 4.4, the peak mobility of the SiGe S/D devices exhibits a 148% increase in comparison to the control.

4.4 Variability of Strained p-MOSFETs

Figure 4.5 shows the Takeuchi plot of the p-MOSFET splits, B_{VT} of strained devices are smaller than that of control. In particular, SiGe S/D with EDB shows the decrease of 10% to the control in Fig. 4.6. Based on the same reasoning as those in

strained n-MOSFETs, the strain effect could reduce V_{th} variation of strained p-MOSFETs. Moreover, the retarded Boron diffusion inside SiGe epitaxial layer was revealed [4.2] which could avoid Boron out-diffusion. If Boron diffuses out to the vicinity of S/D junction and the substrate region, it would be the counter dopant such that B_{VT} is enhanced even though V_{th} lower due to the counter dopant [4.3]. It was found that SiGe S/D with EDB has the smallest B_{VT} (1.55), which is very close to that of RDF (1.5), could be attributed to EDB process. To preserve ultra shallow junction and lower extension resistance, EDB was introduced in SiGe S/D. EDB drastically suppresses Boron out-diffusion from subsequent thermal treatment and forms a much more abrupt junction profile due to the lower boron diffusivity in SiGe. Moreover, the thicker EDB layer shows the more boron out-diffusion constrained. The higher Ge concentration barrier layer also obviously suppresses boron out-diffusion more with the same barrier layer thickness [4.1]. Since Boron out-diffusion is suppressed, the interference of counter dopant is reduced. Thus, it is expected that V_{th} variation is also suppressed.

4.5 Factors Affecting the V_{th} Variation

4.5.1 Effect of the Temperature

To understand the effect of the temperature on strained n-MOSFETs, devices are measured at elevated temperature (85^{O}C). Fig. 4.7 shows the dependence of B_{VT} on the temperature for all the p-MOSFET device splits. From the same reasoning as discussed in section 3.4.1, B_{VT} is larger at 85^{O}C. Also, the result shows the amount of enhanced B_{VT} of SiC S/D and SiC S/D-E is similar to that of the control, which exhibits no degradation compared to the control ones.

4.5.2 Effect of the Drain Bias

The effect of the drain bias (V_{DS}) on V_{th} variation was also examined. Based on the same reasoning as discussed in section 3.4.2, Fig. 4.8 shows that the V_{th} variation increases with increasing drain bias. Also, it shows weak dependence of V_{th} variation on V_{DS} for SiGe S/D with EDB which could be attributed to the strain effect and less Boron out-diffusion. Furthermore, much better DIBL improvement of SiGe S/D with EDB compared to the cases of SiGe S/D and control devices is manifested in [4.1] which is also a cause results in smaller V_{th} variation. This indicates good SCE immunity of SiGe S/D with EDB.

4.5.3 Effect of the Substrate Bias

Figure 4.9 shows the dependence of B_{VT} on the substrate bias (V_{BS}) for all p-MOSFETs. It is well known that ionized impurities in depletion region are the major source of V_{th} variation. By applying substrate bias, more ionized impurities are produced due to the bulk depletion width becomes wider results in enhanced B_{VT}. Thus, B_{VT} increases as substrate bias increases. Furthermore, due to the strain effect and less interference from counter dopant as discussed in section 4.3, SiGe S/D with EDB shows better B_{VT} as substrate bias increases.

4.6 Impact of Stress-induced Random Interface Traps

4.6.1 Introduction

For many strained approach to enhance the carrier mobility, the reliabilities are still a serious issue. The biaxial strained SiGe-channel device provides good drive

current enhancement, it suffers from the Ge-outdiffusion such that exhibits worse reliability. The SiGe on S/D device is a promising structure for p-MOSFET design since it keeps at about the same reliability as the SiGe-channel ones while exhibits a much higher performance. In contrast, SiGe-channel has a major concern with lattice misfit [4.4]. Besides, for p-MOSFET devices, the SiGe S/D with EDB [4.1] is the most promising in terms of performance and reliability. However, we have demonstrated that the variability is improved by utilizing SiGe S/D with EDB before stress. None has been reported on the effect of stress-induced random interface traps. Thus, in this section, we will discuss the device variability after FN and NBTI stresses.

4.6.2 Variability After FN Stress

To study the impact of stress-induced interface traps on V_{th} variation, we use IFCP to evaluate the interface traps for the stressed devices. The charge pumping result after FN stress (V_{GS}-V_{th}= -2V for 300sec) is shown in Fig. 4.10. It was found that SiGe S/D with EDB has the smallest I_{CP} reveal better reliability than SiGe S/D and control. The average interface traps are extracted from $I_{CP,MAX}$ during stress time, from 100sec to 500sec, are shown in Fig. 4.11. It is observed that the number of interface traps increases with increasing stress time. Since the stress-induced random interface traps fluctuation is a possible source to affect the V_{th} variation, Fig. 4.12 shows the comparison of B_{VT} during stress time to observe this phenomenon. Fig. 4.13 shows the relationship of B_{VT} with interface traps. It is found that B_{VT} is enhanced during stress time and increases with increasing interface traps. Moreover, the enhanced B_{VT} is proportional to interface traps. The result is similar to that of n-MOSFETs which indicates that stress-induced interface traps are the dominant source of the enhanced V_{th} variation after FN stress.

4.6.3 Variability After NBTI Stress

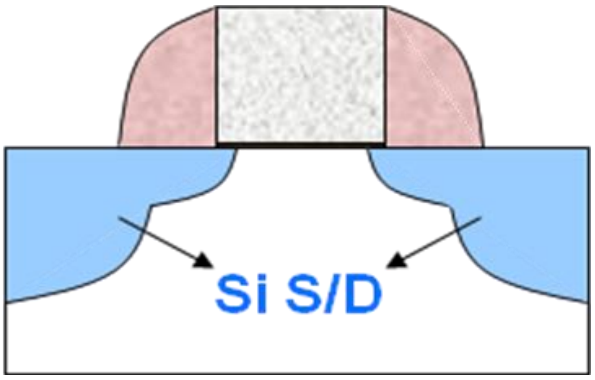
By applying similar analysis, we apply the NBTI stress (V_{GS}-V_{th}= -2V at 85℃) to produce the interface traps at the SiO_2/Si interface which would show more degraded V_{th} variation. To study the stress-induced degradation, Fig. 4.14 shows the measured I_{CP} after NBTI stress (V_{GS}-V_{th}= -2V for 300sec, at 85℃). The I_{CP} of SiGe S/D is larger than the others. The result indicates that SiGe S/D generates more interface traps at the SiO_2/Si interface in comparison to the others. In addition, the I_{CP} of all p-MOSFET splits after NBTI stress are larger than that of FN stress. It also shows that more interface traps are produced after NBTI stress as shown in Fig. 4.15. Fig. 4.16 shows the comparison of B_{VT} after NBTI stress. Fig. 4.17 shows the relationship of B_{VT} with interface traps. The result is similar to that of n-MOSFETs, we observe a more enhanced B_{VT} after NBTI stress which is attributed to the more interface traps generation, but the enhanced B_{VT} is also proportional to the number of interface traps.

4.6.4 Discussion

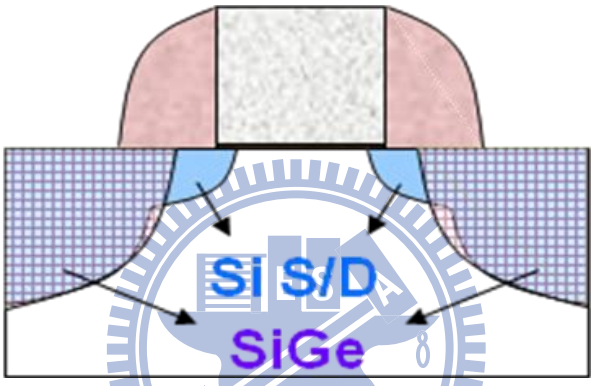
Figures 4.18(a)-(b) show the enhanced B_{VT} after FN and NBTI stresses. Again, we demonstrate that the stress-induced interface traps are the major source of enhanced V_{th} variation after stress. It is also obvious that B_{VT} of strained p-MOSFETs are much enhanced after NBTI stress than that after FN stress. This result shows that the control of the interface quality in strained p-MOSFETs is more critical than that in control.

However, the relationship of B_{VT} with interface traps of p-MOSFETs is different from that of n-MOSFETs. In Fig. 4.13 and 4.17, it is obvious that the slopes of all the

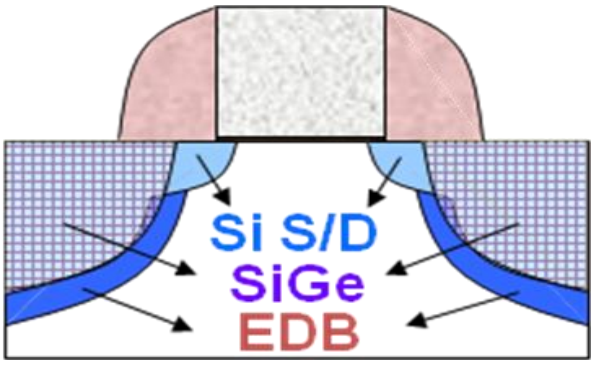
p-MOSFETs are the same, only proportional to the number of interface traps. Moreover, strained p-MOSFETs show slower trend of B_{VT} aggravation than strained n-MOSFETs. It is expected that the effect of stress-induced interface traps in strained p-MOSFETs is unrelated to strain effect, because the relationship between B_{VT} and interface traps of strained p-MOSFETs is consistent with that of the control.



(a)



(b)



(c)

Fig. 4.1 The cross-section view of the experimental devices. (a) control, (b) SiGe S/D (uniaxial-strain), and (c) SiGe S/D w/ EDB devices (uniaxial-strain). All of them are <110> channel on (100) substrate.

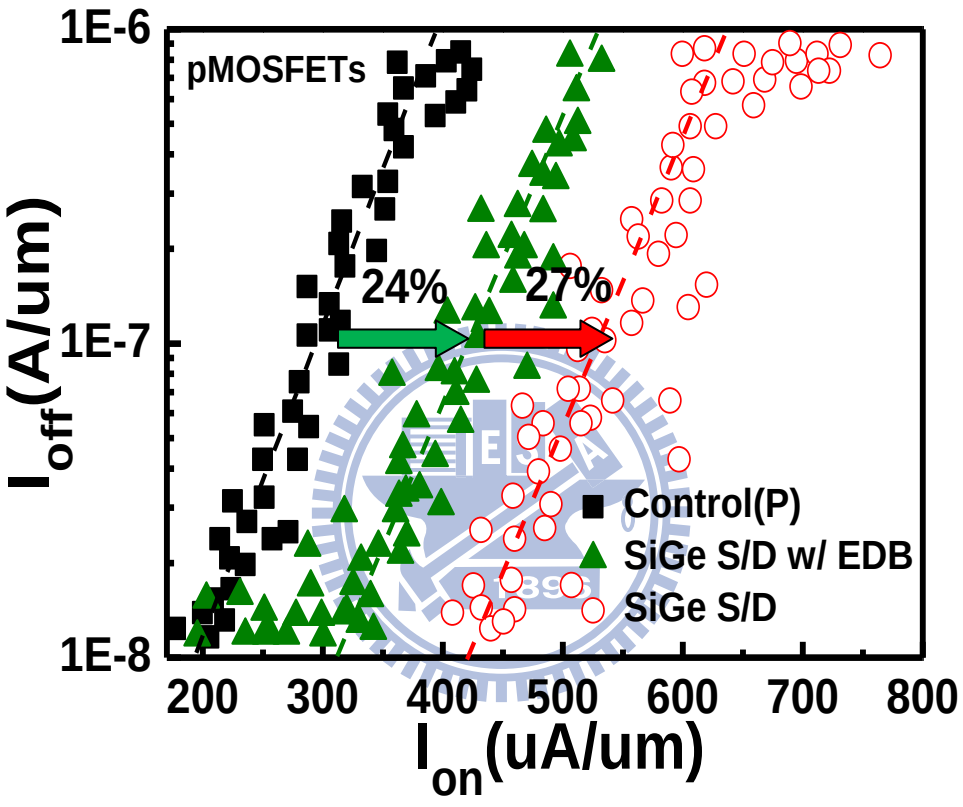


Fig. 4.2 The I_{on}-I_{off} characteristics of all the pMOSFET devices. SiGe S/D device can improve the driving current by 51% over the control(Si-bulk).

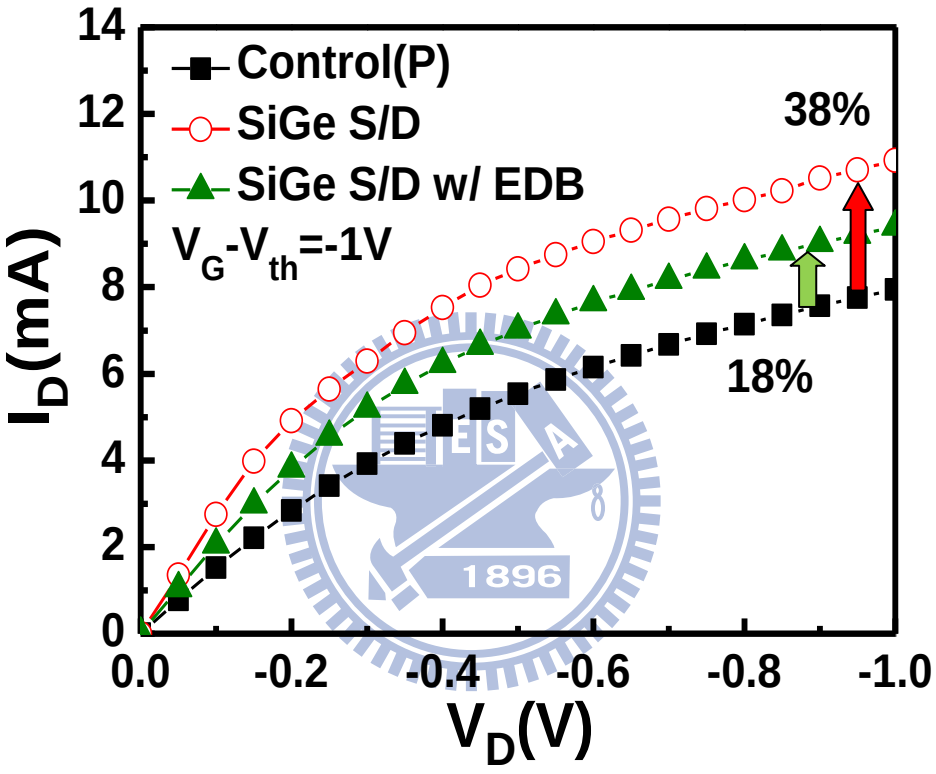


Fig. 4.3 The I_D-V_D curves of the splits and control. The SiGe S/D device shows 38% $I_{D,sat}$ enhancement over control devices.

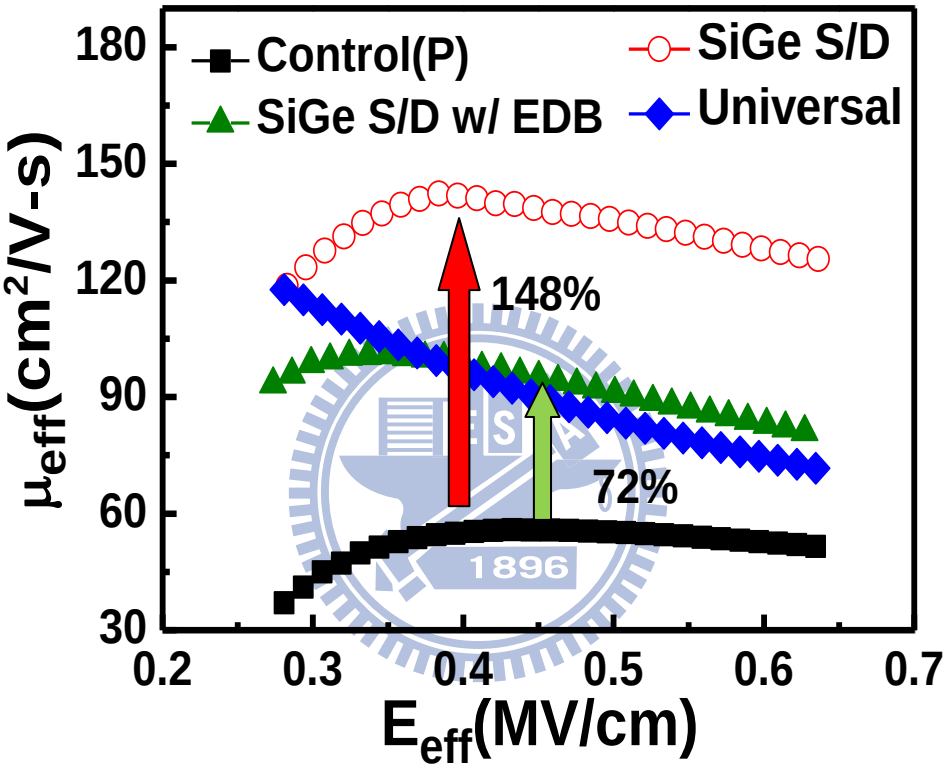


Fig. 4.4 A 148% hole mobility enhancement is obtained for the long SiGe S/D device compared to the control.

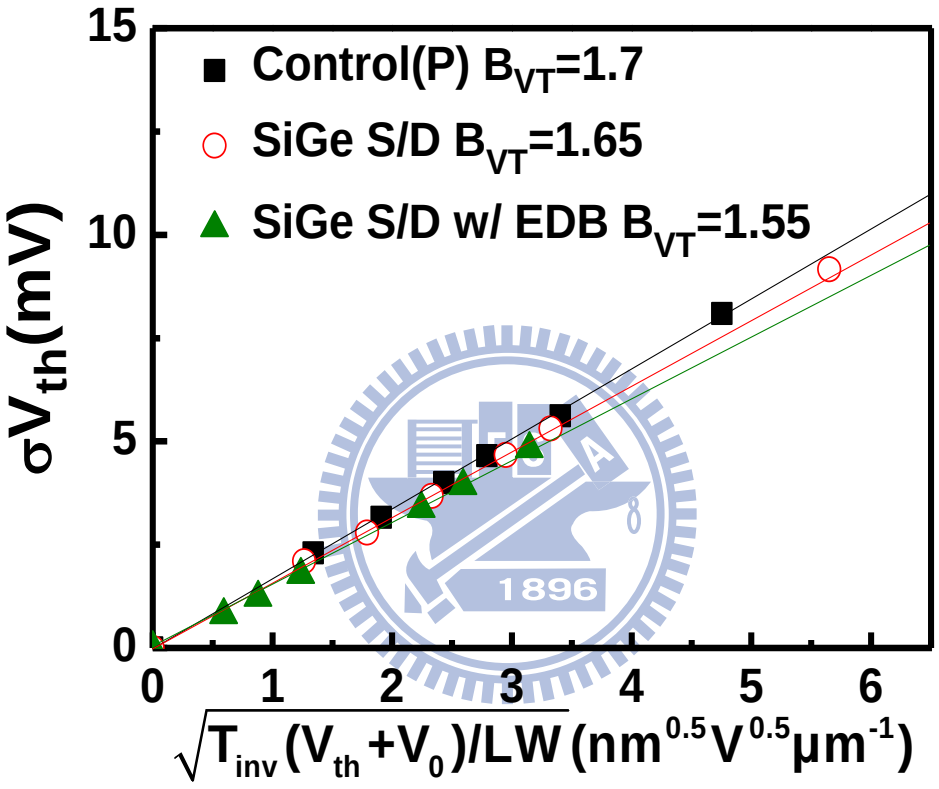


Fig. 4.5 Takeuchi Plots of p-MOSFETs. The slope indicates the value of B_{VT}.

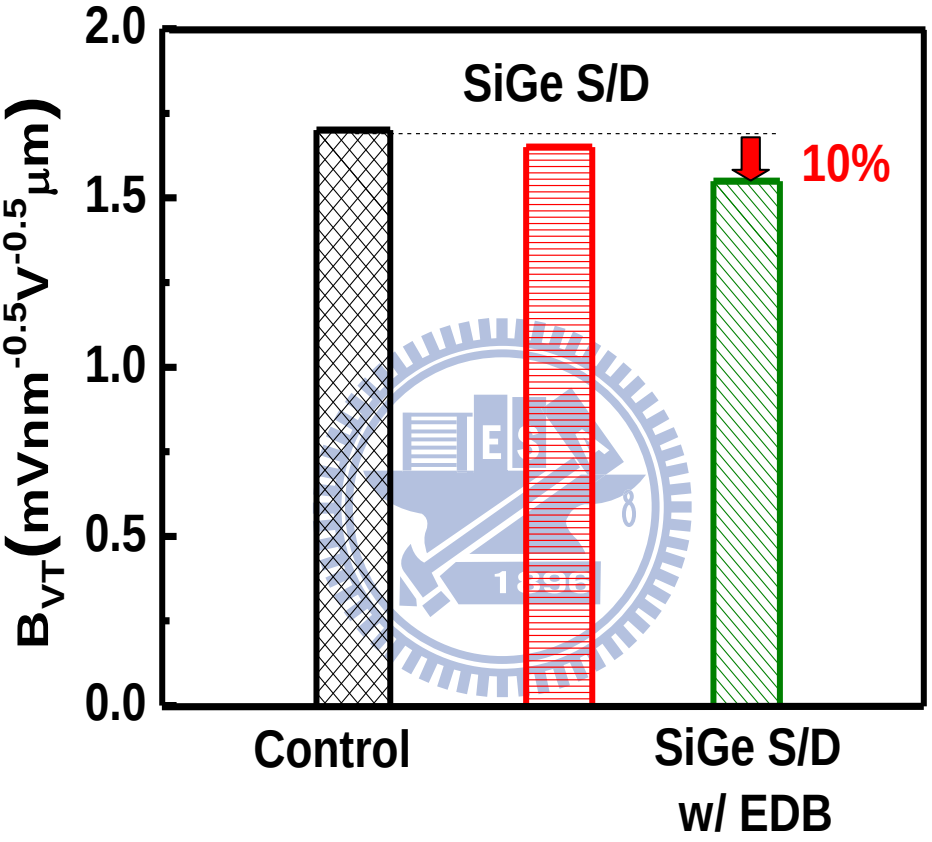


Fig. 4.6 Comparison of B_{VT} for p-MOSFETs. B_{VT} of SiGe S/D w/ EDB shows the 10% improvement to the control.

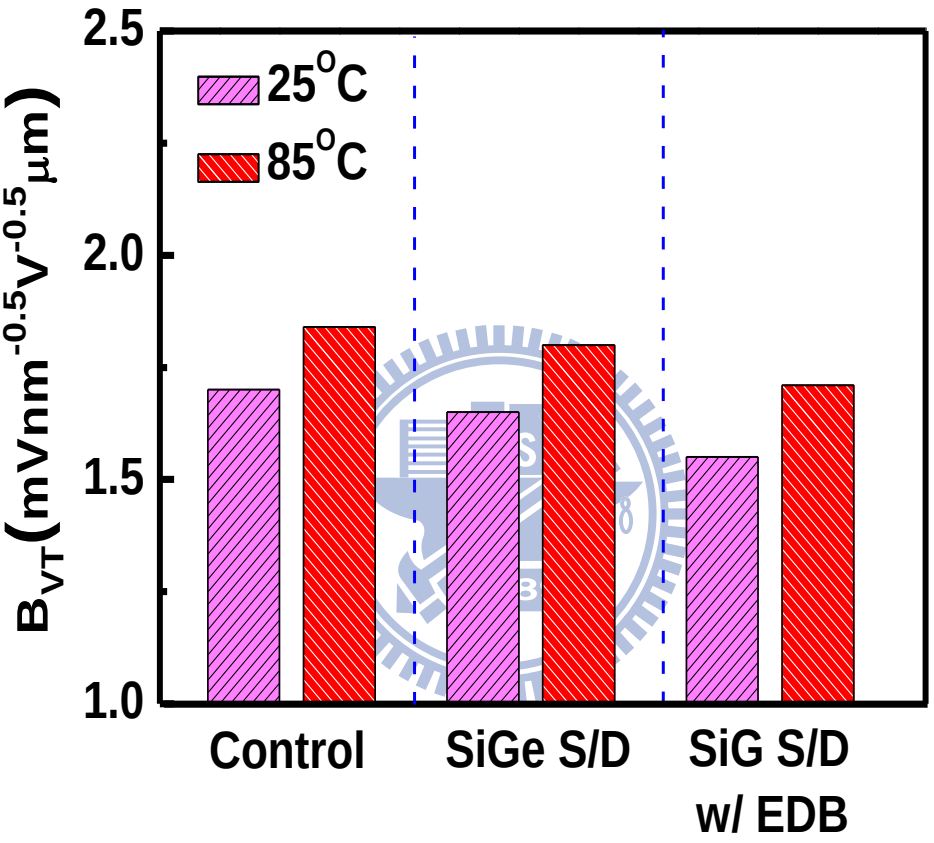


Fig. 4.7 The dependence of B_{VT} on the temperature. Strained devices show no degradation compared to the control device.

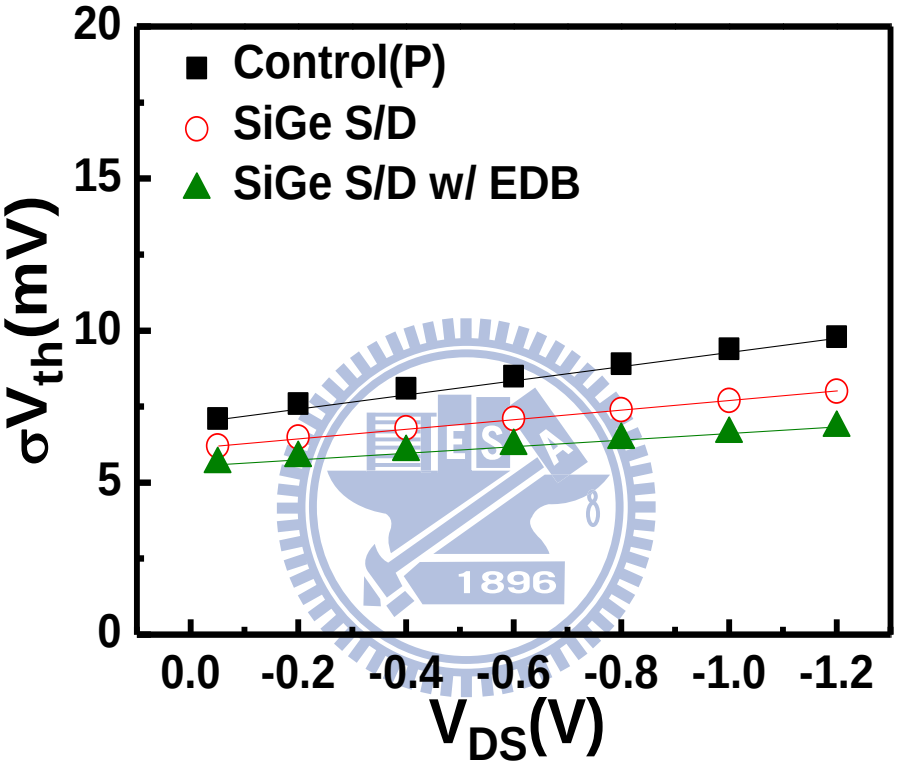


Fig. 4.8 V_{DS} dependence of σV_{th}. Strained devices exhibit weak dependence of V_{th} variation on the drain bias.

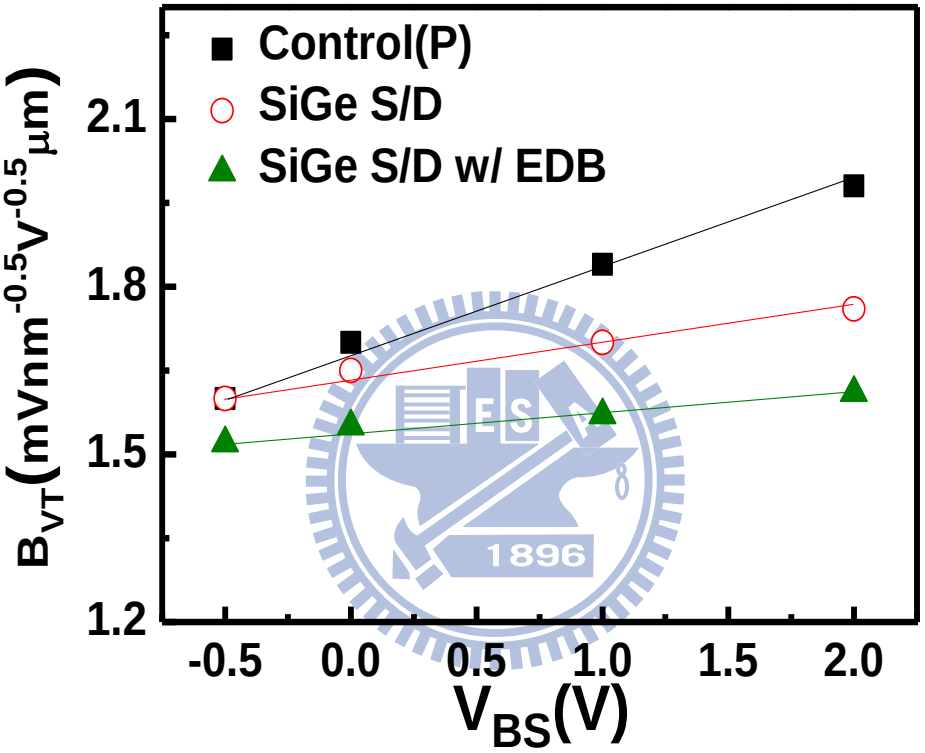


Fig. 4.9 The dependence of B_{VT} on V_{BS}. Strained devices show better B_{VT} as substrate bias increases.

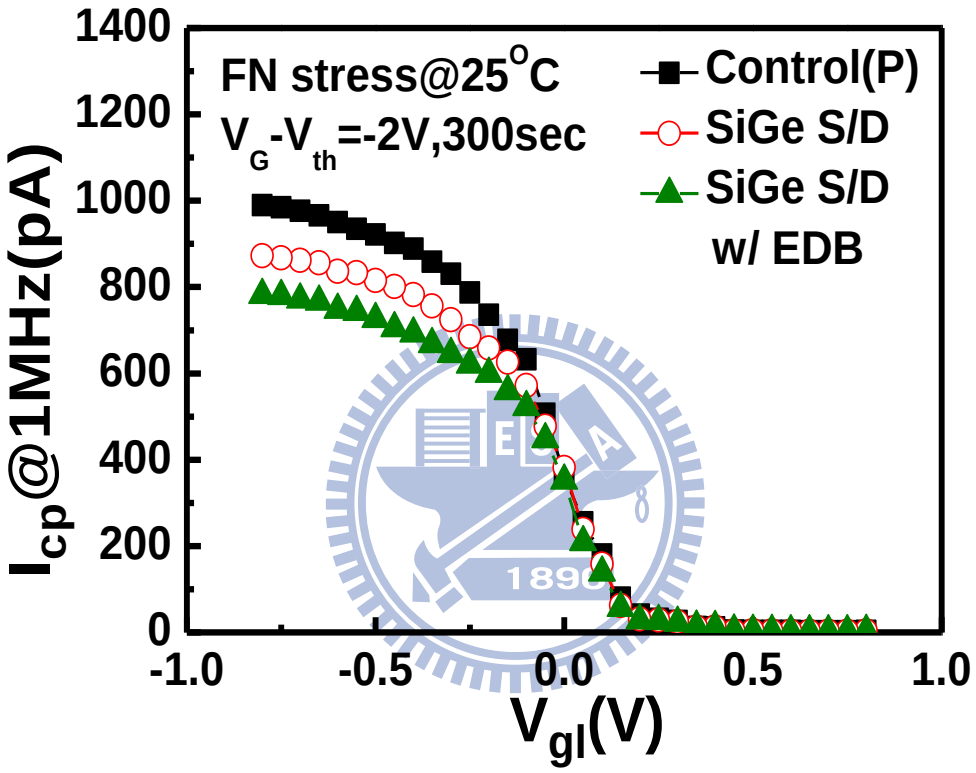


Fig. 4.10 The charge pumping currents of all the p-MOSFETs after FN stress.

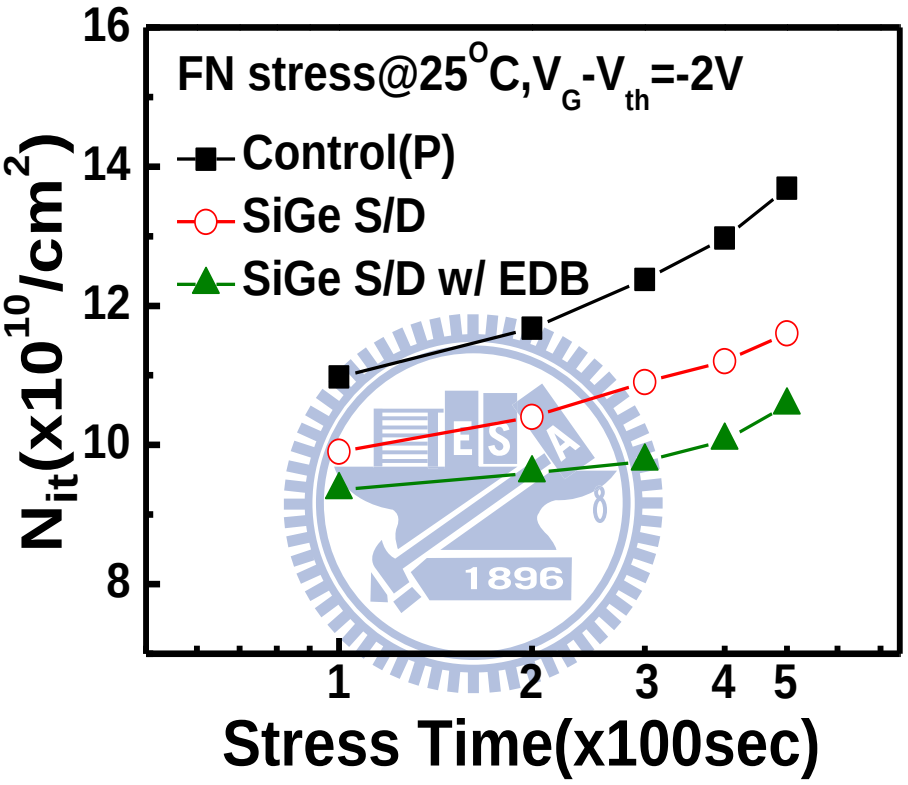


Fig. 4.11 The average interface traps of all the p-MOSFETs after FN stress.

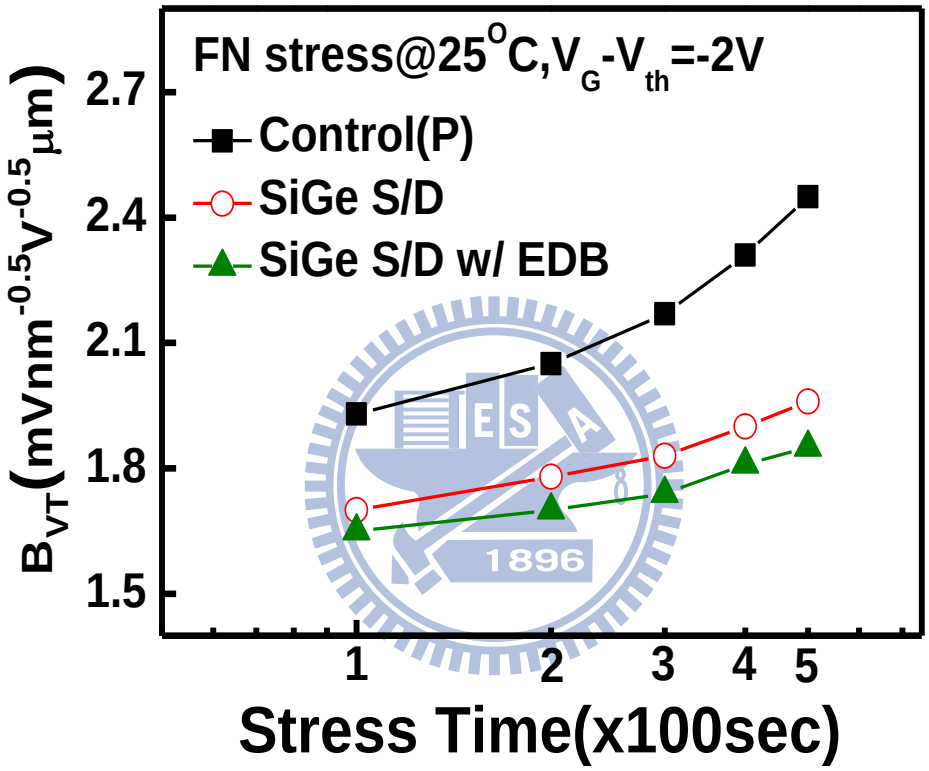


Fig. 4.12 The evolution of B_{VT} for all the p-MOSFETs during FN stress.

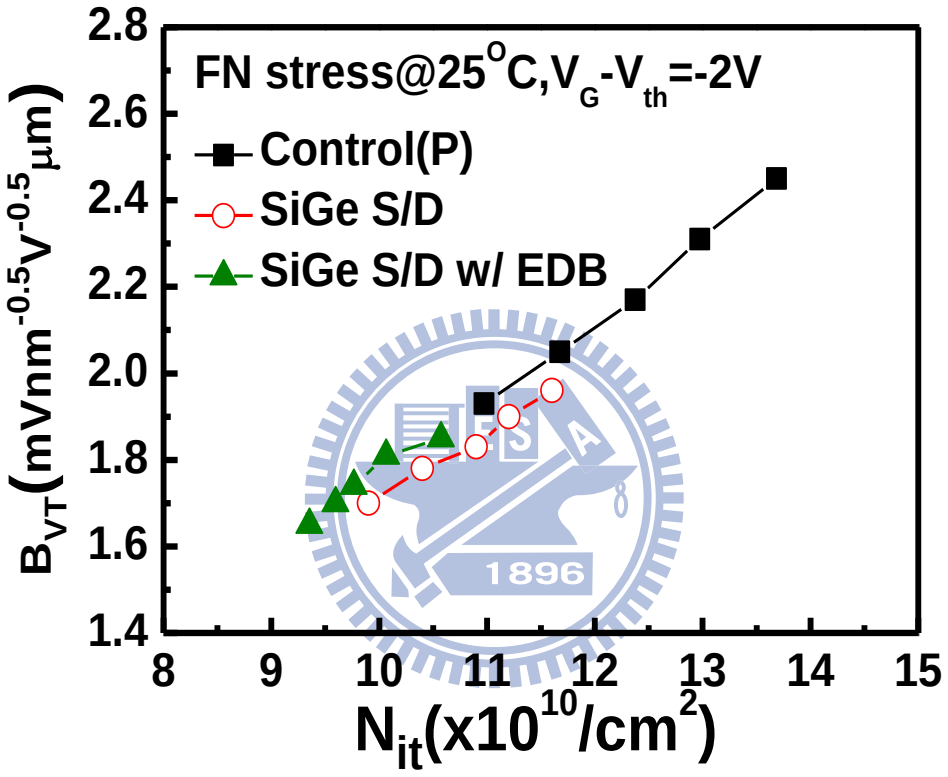


Fig. 4.13 Relationship of B_{VT} with interface traps for all the p-MOSFETs after FN stress.

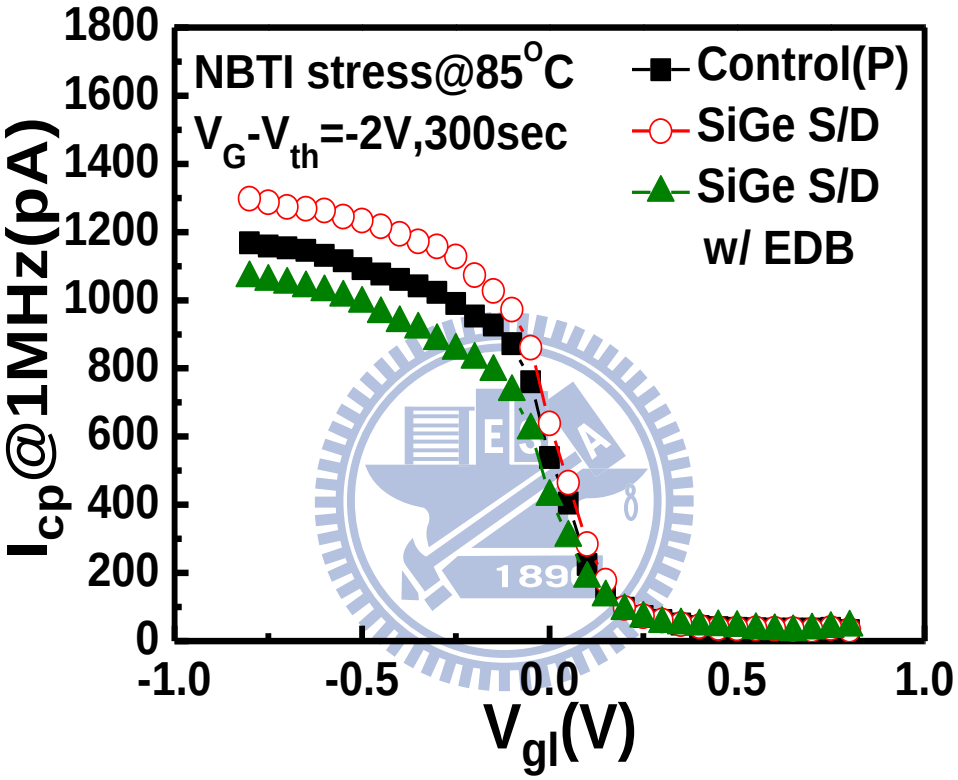


Fig. 4.14 The charge pumping currents of all the p-MOSFETs after NBTI stress.

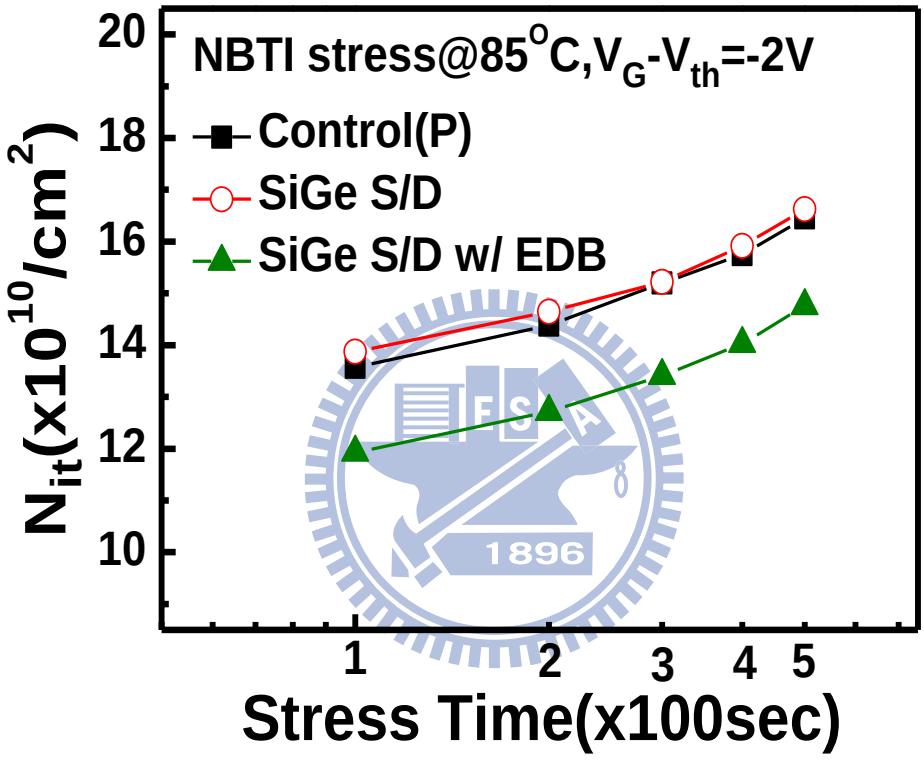


Fig. 4.15 The average interface traps of all the p-MOSFETs after NBTI stress.

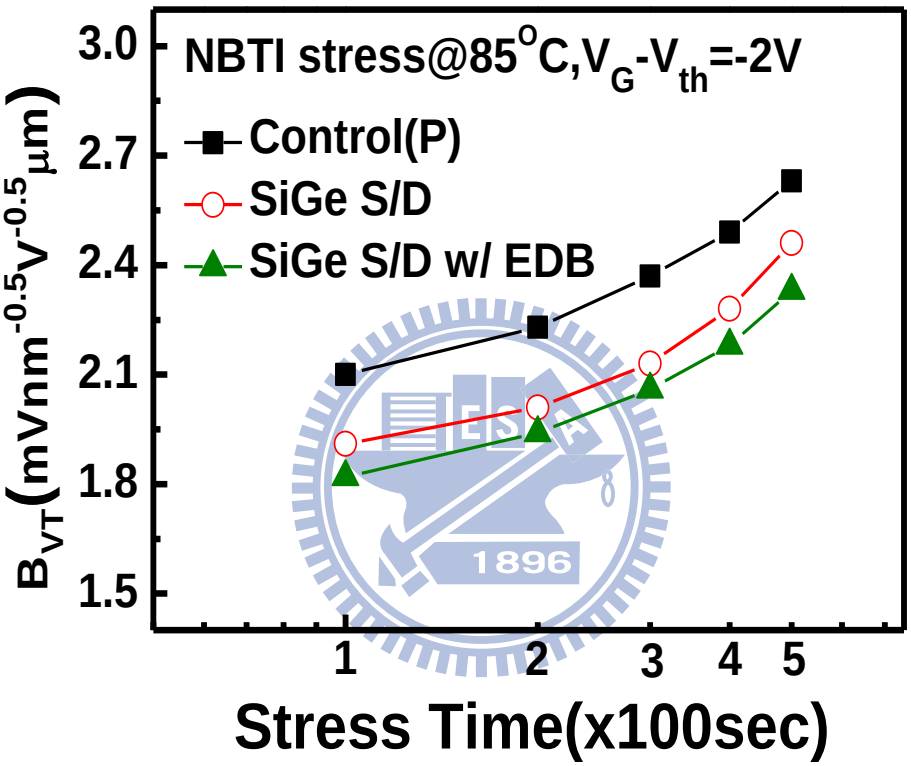


Fig. 4.16 The evolution of B_{VT} for all the p-MOSFETs during NBTI stress.

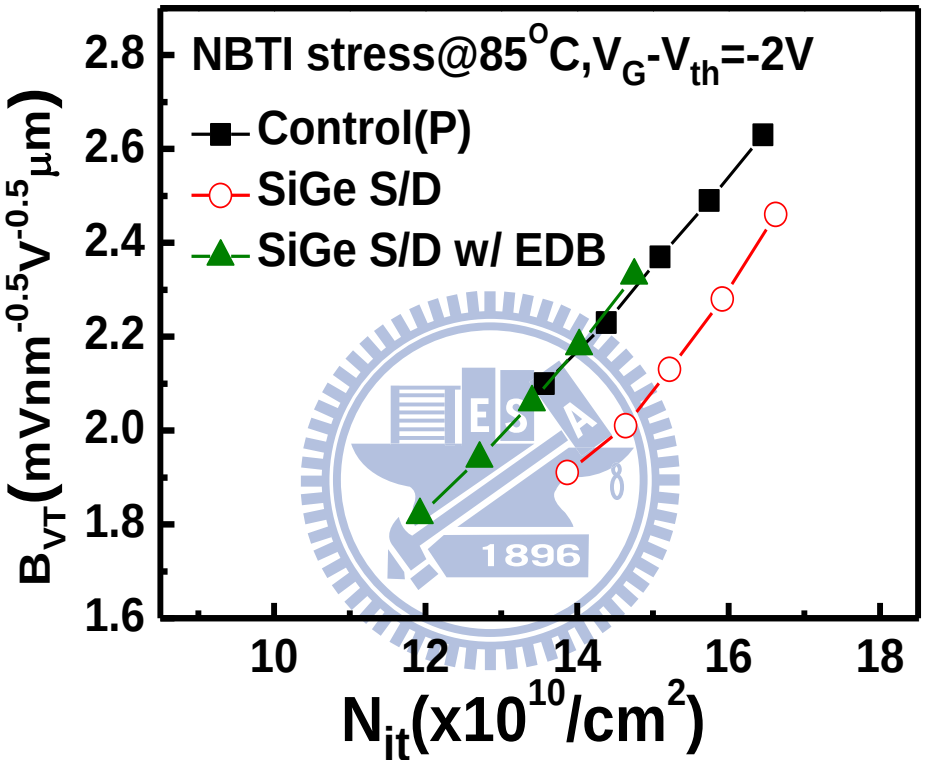
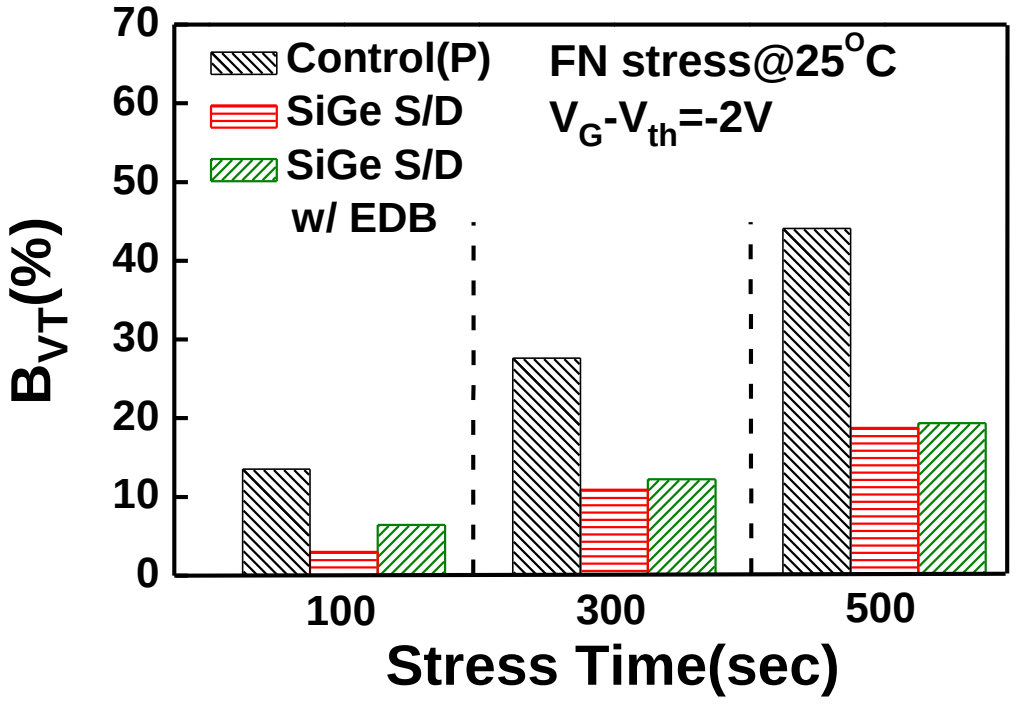
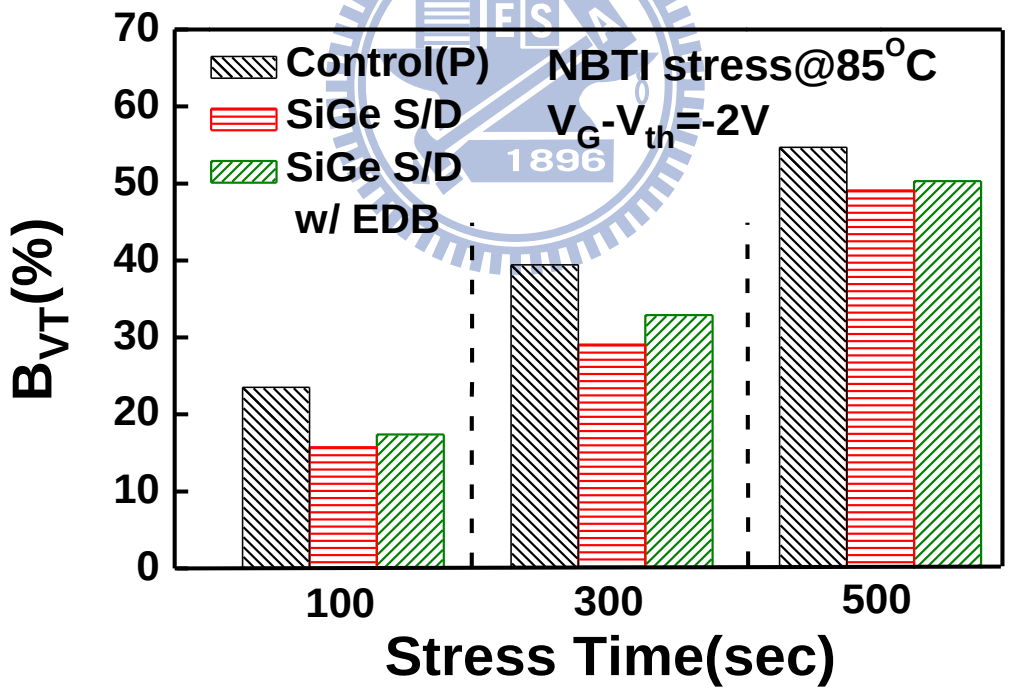


Fig. 4.17 Relationship of B_{VT} with interface traps for all the p-MOSFETs after NBTI stress.



(a)



(b)

Fig. 4.18 The enhanced B_{VT} caused by stress-induced interface traps during (a) FN stress and (b) NBTI stress.

Chapter 5

Summary and Conclusion

In this thesis, we are the first to examine the variability of various n-MOSFETs and p-MOSFETs employing uniaxial-strain using Takeuchi plot. The random dopant fluctuation induced V_{th} variation in strained devices can be normalized by Takeuchi plot. The FN and BTI stress which induces the aggravated V_{th} and produces random interface traps fluctuation (RTF) are also studied for both uniaxial strained n-MOSFETs and p-MOSFETs.

First, the variability of all the MOSFET splits is investigated in this thesis. The reasons for V_{th} variation improvement of strained devices are analyzed. Then, the factors affecting the V_{th} variation which include temperature, drain bias, and substrate bias are examined. Experimental results show better variability of devices with the uniaxial strained channel. In particular, strained devices show much better SCE immunity. Furthermore, the stress-induced random interface traps which are the dominant source of enhanced V_{th} variation after stress, were also examined. For strained n-MOSFETs, due to the closer distance between inversion layer electrons and interface states, Coulomb scattering limited by interface states becomes strong made a faster trend of V_{th} variation aggravation. However, the aggravated V_{th} variation of strained p-MOSFETs is unrelated to strain effect.

In summary, the improved variability of uniaxial strained CMOS devices have been verified by using Takeuchi plot. Extensive comparisons between strained and control devices have been justified on examining the effects of temperature, drain bias, and substrate bias. The impact of stress-induced random interface traps on V_{th}

variation, another source of V_{th} variability, was also examined. These results provide a good understanding of the random dopant fluctuation (RDF) and random interface traps fluctuation (RTF) of uniaxial strained devices.

References

Chapter 1

[1.1] G. Declerck, "**A Look into the Future of Nanoelectronics**", in *VLSI Symp. Tech. Dig.*, pp. 6-10, 2005.

[1.2] K. Kuhn, C. Kenyon, A. Kornfeld, M. Liu, A. Maheshwari, W. Shih, S. Sivakumar, G. Taylor, P. VanDerVoorn, and K. Zawadzki, "**Managing Process Variation in Intel's 45nm CMOS Technology**", in *Intel Technology Journal*, 12, pp. 93-109, 2008.

[1.3] K. Takeuchi, T. Tsunomura, A. T. Putra, T. Fukai, A. Nishida, S. Kamohara, and T. Hiramoto, "**Analyses of Random Threshold Voltage Fluctuations in MOS Devices**", in *International Workshop on Junction Technology*, pp. 7-10, 2009

[1.4] F. L. Yang, J. R. Hwang, H. M. Chen, J. J. Shen, S. M. Yu, Y. M. Li, and D. D. Tang, "**Discrete Dopant Fluctuated 20nm/15nm-Gate Planar CMOS**", in *VLSI Symp. Tech. Dig.*, pp. 208-209, 2007.

[1.5] A. V-Y Thean, Z. H. Shi, L. Mathew, T. Stephens, H. Desjardin, C. Parker, T. White, M. Stoker, L. Prabhu, R. Garcia, B. Y. Nguyen, S. Murphy, R. Rai, J. Conner, B. E. White, and S. Venkatesan, "**Performance and Variability Comparisons between Multi-Gate FETs and Planar SOI Transistors**", in *IEDM Tech. Dig.*, pp. 881-884, 2006.

[1.6] K. J. Kuhn, "**Reducing Variation in Advanced Logic Technologies: Approaches to Process and Design for Manufacturability of Nanoscale CMOS**", in *IEDM Tech. Dig.*, pp. 471-474, 2007.

[1.7] O. Weber, O. Faynot, F. Andrieu, C. B. Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. F. Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B. Y. Nguyen, and S. Deleonibus, "**High Immunity to Threshold Voltage Variability in**

Undoped Ultra-Thin FDSOI MOSFETs and its Physical Understanding", in *IEDM Tech. Dig.*, pp. 245-248, 2008.

[1.8] N. Nakanishi, S. Kudo, M. Kawakami, T. Hayashi, H. Oda, T. Uchida, Y. Miyagawa, K Asai, K. Ohnishi, N. Hattori, Y. Hirose, T. Koyama, K. Asayama, and E. Murakami, "**Strain Mapping Technique for Performance Improvement of Strained MOSFETs with Scanning Transmission Electron Microscopy**", in *IEDM Tech. Dig*., pp. 431-434, 2008.

[1.9] K. Takeuchi, T. Fukai, T. Tsunomura, A. T. Putra, A. Nishida, S. Kamohara and T. Hiramoto, "**Understanding Random Threshold Voltage Fluctuation by Comparing Multiple Fabs and Technologies**", in *IEDM Tech. Dig.*, pp. 467-470, 2007.

Chapter 2

[2.1] K. Takeuchi, T. Fukai, T. Tsunomura, A. T. Putra, A. Nishida, S. Kamohara, and T. Hiramoto, "**Understanding Random Threshold Voltage Fluctuation by Comparing Multiple Fabs and Technologies**", in *IEDM Tech. Dig.*, pp. 467-470, 2007.

[2.2] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "**Matching Properties of MOS transistors**", in IEEE J. Solid-State Circuits, vol. 24, no.5 , pp. 1433-1439, 1989.

[2.3] K. Takeuchi, T. Tatsumi, and A. Furukawa, "**Channel Engineering for the Reduction of Random-Dopant-Placement-Induced Threshold Voltage Fluctuation**", in *IEDM Tech. Dig.*, p.841-844, 1997.

[2.4] T. Putra, A. Nishida, S. Kamohara, T. Tsunomura, and T. Hiramoto, "**Consideration of Random Dopant Fluctuation Models for Accurate Prediction of Threshold Voltage Variation of Metal–Oxide–Semiconductor Fieldeffect-Transistors in 45nm**

Technology and Beyond", in *Japanese. J. Appl. Phys.*, vol. 48, no. 4, pp. 044502-1-5, 2009.

[2.5] T.Mizuno, J. Okamura, and A. Toriumi, "**Experimental Study of Threshold Voltage Fluctuation due to Statistical Variation of Channel Dopant Number in MOSFETs**", in *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216-2221, 1994.

[2.6] A. Asenov, "**Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 μm MOSFETs: A 3-D 'Atomistic' Simulation Study**", in *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2505-2513, 1998.

[2.7] K. Takeuchi, "**Channel Size Dependence of Dopant-Induced Threshold Voltage Fluctuation**", in *VLSI Symp. Tech. Dig.*, pp. 72-73, 1998.

[2.8] T. Tanaka, T. Usuki, Y. Momiyama, and T. Sugii, "**Direct Measurement of Vth Fluctuation Caused by Impurity Positioning**", in *VLSI Symp. Tech. Dig.*, pp. 136-137, 2000.

[2.9] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, "**Role of Long-Range and Short-Range Coulomb Potentials in Threshold Characteristics under Discrete Dopants in Sub-0.1 μm Si-MOSFETs**", in *IEDM Tech. Dig.*, pp. 275-278, 2000.

[2.10] S. B. Herner, H.-J. Gossmann, L. P. Pelaz, G. H. Gilmer, M. Jaraz, D. C. Jacobson, and D. J. Eaglesham, "**Ion Mass Influence on Transient Enhanced Diffusion and Boron Clustering in Silicon: Deviation from the '+1' Model**", *J. Appl. Phys.*, vol. 83, no. 11, pp. 6182-6184, 1998.

[2.11] T. Tsunomura, A. Nishida, F. Yano, A. T. Putra, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada, T. Hiramoto, and T. Mogami," **Analyses of 5σ Vth Fluctuation in 65 nm-MOSFETs Using Takeuchi Plot**", in *VLSI Symp. Tech. Dig.*, p.156-157, 2008.

Chapter 3

[3.1] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "**A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate length Strained silicon CMOS Transistors**", in *IEDM Tech. Dig*., pp. 978-980, 2003.

[3.2] B. Cheng, S. Roy, G. Roy, F. Adamu-Lema, and A. Asenov, "**Impact of Intrinsic Parameter Fluctuations in Decanano MOSFETs on Yield and Functionality of SRAM Cells**", in *Solid State Electron.*, vol. 49, pp. 740-746, 2005.

[3.3] A. Agarwal, K. Chopra, V. Zolotov, and D. Blaauw, "**Circuit Optimization Using Statistical Static Timing Analysis**", in *Proc. ACM/IEEE Des. Autom. Conf.*, pp. 321-324, 2005.

[3.4] N. A. Kamsani, B. Cheng, S. Roy, and A. Asenov, "**Statistical Circuit Simulation with Supply-Voltage Scaling in Nanometre MOSFET Devices under the Influence of Random Dopant Fluctuations**", in *Proc. FTFC*, pp. 95-100, 2008.

[3.5] T. Skotnicki, "**Nano-CMOS and Emerging Technologies—Myths and Hopes**", in *Proc. Int. Conf. SSDM*, pp. 2-5, 2006.

[3.6] T. Tsunomura, A. Nishida, F. Yano, A. T. Putra, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada, T. Hiramoto, and T. Mogami," **Analyses of 5σ Vth Fluctuation in 65 nm-MOSFETs Using Takeuchi Plot**", in *VLSI Symp. Tech. Dig.*, p.156-157, 2008.

[3.7] A. Ono and I. Sakai, "**Suppression of Vth Fluctuation by Minimizing Transient Enhanced Diffusion for Deep Sub-Quarter Micron MOSFET**", in *IEDM Tech. Dig.*, pp. 755-758, 1996.

[3.8] H. Rucker, B. Heinemann, D. Bolze, D. Knoll, D. Kruger, R. Kurps, H. J. Osten, P. Schley, B. Tillack, and P. Zaumseil, "**Dopant Diffusion in C-doped Si and SiGe: Physical Model and Experimental Verification**", in *IEDM Tech. Dig.*, pp. 345-348, 1999.

[3.9] E. R. Hsieh, Steve S. Chung, P. W. Liu, W. T. Chiang, C. H. Tsai, W. Y. Teng, C. I. Li, T. F. Kuo, Y. R. Wang, C. L. Yang, C. T. Tsai, and G. H. Ma, "**A New and Simple Experimental Approach to Characterizing the Carrier Transport and Reliability of Strained CMOS Devices in the Quasi-Ballistic Regime**", in *IEDM Tech. Dig.*, pp. 779-782, 2009.

[3.10] Y. Taur and T. H. Ning, "**Fundamentals of Modern VLSI Devices (Cambridge University Press, Cambridge, U.K., 1998)**".

[3.11] F. L. Yang, J. R. Hwang, H. M. Chen, J. J. Shen, S. M. Yu, Y. M. Li, and D. D. Tang, "**Discrete Dopant Fluctuated 20nm/15nm-Gate Planar CMOS**", in *VLSI Symp. Tech. Dig.*, pp. 208-209, 2007.

[3.12] H. Fukutome, Y. Momiyama, T. Kubo, Y. Tagawa, T. Aoyama, and H. Arimoto, "**Direct Evaluation of Gate Line Edge Roughness Impact on Extension Profiles in Sub-50-nm n-MOSFETs**", in *IEEE Trans. Electron Devices*, vol. 53, no. 11 , pp 2755-2763, 2006.

[3.13] M. Miyamura, T. Fukai, T. Ikezawa, R. Ueno, K. Takeuchi, and M. Hane, "**SRAM Critical Yield Evaluation Based on Comprehensive Physical/Statistical Modeling, Considering Anomalous Non-Gaussian Intrinsic Transistor Fluctuations**", in *VLSI Symp. Tech. Dig.*, pp. 22-23, 2007.

[3.14] A. Asenov, S. Kaya, and J. H. Davies, **"Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations**", in *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 112-119, 2002.

[3.15] P. Andricciola, H. P. Tuinhout, B. De Vries, N. A. H. Wils, A. J. Scholten, and D. B. M. Klaassen, "**Impact of interface states on MOS transistor mismatch**", in *IEDM Tech. Dig.*, pp. 711-714, 2009.

[3.16] S. S. Chung, S. J. Chen, C. K. Yang, S. M. Cheng, S. M. Lin, S. H. Cheng, S. H. Lin, Y. C. Shen, H. S. Lin, K. T. Hung, D. Y. Wu, T. R. Yew, S. C. Chien, F. T. Liou, and F. Wen, "**A Novel and Direct Determination of the Interface Traps in Sub-100nm CMOS Devices with Direct Tunneling Regime (12~16Å) Gate Oxide**", in *VLSI Symp. Tech. Dig.*, pp. 74-75, 2002.

[3.17] E. R. Hsieh, S. S. Chung, P. W. Liu, W. T. Chiang, C. H. Tsai, W. Y. Teng, C. I. Li, T. F. Kuo, Y. R. Wang, C. L. Yang, C. T. Tsai, and G. H. Ma, "**A New and Simple Experimental Approach to Characterizing the Carrier Transport and Reliability of Strained CMOS Devices in the Quasi-Ballistic Regime**", in *IEDM Tech. Dig.*, pp. 779-782, 2009.

[3.18] J. R. Brews, "**Surface Potential Fluctuations Generated by Interface Charge Inhomogeneities in MOS Devices**", in *J. Appl.Phys.*, vol. 43, pp. 2306-2313, 1972.

[3.19] O. Weber and S. Takagi, "**Experimental Examination and Physical Understanding of the Coulomb Scattering Mobility in Strained-Si nMOSFETs**", in *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2386-2396, 2008.

Chapter 4

[4.1] C. H. Tsai, B. C. Lan, Y. H. Lin, W. T. Chiang, T. Y. Chang, P. W. Liu, J. W. Pan, Y. C. Liu, J. L. Tsai, T. F. Chen, and C. T. Tsai, "**Unique Ultra Shallow Junction Scheme with Conventional Activation Process**", in *VLSI Symp. Tech. Dig.*, pp. 188-189, 2006.

[4.2] K. Rajendran and W. Schoenmaker, "**Studies of Boron Diffusivity in Strained $Si_{1-x}Ge_x$ Epitaxial Layers**", in *IEEE Trans. Electron Devices*, vol. 89, no. 2, pp. 980-987, 2001.

[4.3] T. Tsunomura, A. Nishida, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada, T. Hiramoto and T. Mogami, "**Process Condition Dependence of Random V_T Variability in NFETs and PFETs**", in *Proc. Int. Conf. SSDM*, pp. 1010-1011, 2009.

[4.4] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson, and M. Bohr, "**Delaying Forever: Uniaxial Strained Silicon Transistors in a 90 nm CMOS Technology**", in *VLSI Symp. Tech. Dig.*, pp. 50-51, 2004.