國立交通大學

電子工程學系　　電子研究所碩士班

碩士論文

多層堆疊氧化鉿/氧化鋁電阻轉態層之透明電阻式記憶體特性研究

Characterization of Transparent Resistive Random Access Memory Devices Based on HfO_2/Al_2O_3 Multi-layer Stacking as Resistive Switching Film

研 究 生：溫岳嘉

指導教授：張國明　教授 / 汪大暉　教授

中 華 民 國 九 十 九 年 八 月

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摘　　要

我們首開先例的運用原子層沉積法沉積出九循環、十九循環以及三十八循環的氧化鉿及氧化鋁多層堆疊式電阻轉態層，並且運用在透明電阻式記憶體上。其中九循環元件展現出最佳的性能，最多的耐久度，最小的平均操作電壓以及最小的操作電壓標準差，相信是因為三十八循環元件內部過於散佈的氧化鋁導致不易生成穩定傳導絲的緣故。

儘管現今透明電阻式記憶體的性能表現尚無法和非透明電阻式記憶體相提並論，相較於近年透明電阻式記憶體的發展，我們的九循環元件在耐久度、平均操作電壓和操作電壓標準差上已經展現出極佳的性能。根據相關研究指出，氧空缺生成能可因加入鋁而降低，如此有助於生成較為穩定的傳導絲來強化電阻轉態的性能。就我們所知，我們首先應用此一原理於透明電阻式記憶體上來控制傳導絲的生成，不但呼應了前人的研究結果，也將透明電阻式記憶體的性能表現推向更高的水平。將此多層堆疊式電阻轉態層應用在透明電阻式記憶體上，使得透明電阻式記憶體有極大的潛力，來成為新世代未來時尚科技電子產品。

Characterization of Transparent Resistive Random Access Memory Devices Based on HfO_2/Al_2O_3 Multi-layer Stacking as Resistive Switching Film

Student: Yue-Jia Wun Advisors: Dr. Kow-Ming Chang / Dr. Tahui Wang

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Abstract

We first demonstrate the resistive switching characteristics of ***Transparent Resistive Random Access Memory Devices (TRRAM)*** with HfO2/Al2O3 multi-layer stacking via different ALD deposition cycles as resistive switching films for 9-cycle, 19-cycle and 38-cycle devices respectively. The-9-cycle device has the best performance of endurance times, average set operation voltage, standard deviation of set voltage distribution; average reset operation voltage, standard deviation of reset voltage distribution than the other two (19-cycle and 38-cycle) . For the reason that Al_2O_3 spread out more in resistive switching layers of the 38-cycle device, it is more difficult to form stable conducting filaments.

In addition, our 9-cycle device with endurance times, set/reset operation voltage and standard deviation of reset voltage distribution is relatively excellent compare to recent published transparency memory devices. It was

claimed that oxygen vacancy forming energy could be lower down by Al atoms which leads conducting filaments formed more stable in previous non-transparent RRAM. Even though, the performances of TRRAM in this thesis are still not comparable to non-transparent RRAM. To the best of our knowledge, we first apply this mechanism to control the conducting filament formation in TRRAM. Not only echo the previous study of the mechanism but also demonstrate TRRAM with the higher performance. The multi-layer stacking as the resistive switching films in TRRAM shows great potential in the future modern electronics.

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首先要感謝的是我們實驗室的大家長--張國明老師。感謝張國明老師營造出這樣氣氛愉快相處融洽的實驗室，除了在研究方面的指導之外，老師還時常不厭其煩的分享他個人求學經歷以及待人處事的道理，這類書本上學不到的東西更是老師難能可貴的智慧結晶。還要感謝汪大暉老師的共同指導，幫助我進入這個實驗室，老師在半導體物理相關的知識教導也對我的研究提供了莫大的幫助。

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溫岳嘉于新竹交通大學 2010 年 8 月

Contents

Table Captions

Figure Captions

Chapter 1
Introduction

1.1 Introduction to Nonvolatile Memory

Due to the popularity of portable devices, such as cell phone, digital camera and USB memory stick, the requirements of the nonvolatile memories (NVMs) increase significantly in semiconductor industry. Ideal NVMs should have the properties of low power consumption, low operation voltage, low operation current, high operation speed, high endurance, long retention time, nondestructive readout, simple structure, small size, low cost, and high cell density, etc [1].

Although, there is no such NVM meet the all above properties yet. Nowadays, the most popular NVM is flash memory. There are two kinds of flash memories, NAND flash and NOR flash. The NAND flash is used for large data storage because of the higher cell density. And because the NOR can be operating at higher speed, it is suitable for operation system storage. The structure of Flash memory is a MOSFET-like with a floating gate, as shown in Fig. 1.1.1. However, some issues still needed to be solved, such as high operation voltage, low operation speed, poor retention time, and coupling interference effect [2]. Especially because of the coupling interference effect, it will set a scaling down limitation. People are looking forward to the next-generation NVM.

There are four possible candidates for the next-generation NVMs, such as *phase change memory (PCM)*[3][4], *ferroelectric random access memory (FeRAM)*[5][6], *magnetroresistive random access memory (MRAM)*[7][8] and *resistive random access memory (RRAM)*[9]. In this thesis, we introduce one of the most future modern NVMs, fully transparent RRAM (TRRAM)[10]. A brief comparison of flash memory with these next-generation NVMs are shown in Table 1.1.1. These next-generation NVMs are discussed in the following section.

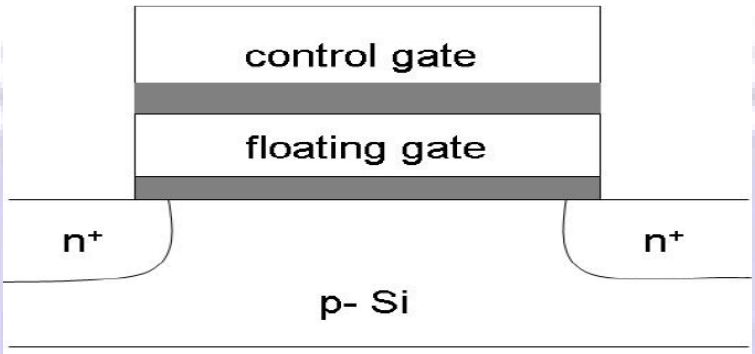

Fig. 1.1.1 Floating gate flash memory

Table 1.1.1 NVMs comparison

	Flash	PCM	FeRAM	MRAM	RRAM
Integration	Good	Good	Poor	Poor	Good
Multi Level Cell	Yes	Yes	No	No	Yes
Current	~ μA	~ mA	~ μA	~ mA	< 0.1mA
Write/Erase Voltage (V)	12	3	0.9 ~ 3.3	1.5	< 3
Write/Erase Time	~ ms	~ 100ns	~ 40ns	< 10ns	< 10ns
Read Voltage (V)	4 ~ 5	3	0.9 ~ 3.3	1.5	0.7
Read Time	70~90ns	60ns	45ns	20ns	< 50ns
Write/Erase Cycles	> 10^5	10^8	10^{14}	> 3×10^{16}	> 10^5
Retention Time	> 10 years	> 10 years	> 10 years	> 10 years	> 10 years

ITRI : New Non-Volatile Memory Workshop 2008, Hsinchu, Taiwan

1.2 Introduction to Next-generation Nonvolatile Memory

1.2.1 Phase Change Memory

The phase change memory (PCM) [3][4], also called Ovonic Unified Memory (OUM), is a hopeful technology to fit the requirements of the ideal NVM. The basic PCM cell is shown in Fig. 1.2.1.1. The primary material of the PCM is GeSbTe (GST), which utilize tow different structural phase of GST, amorphous and polycrystalline, for data storage. In reset process, a high magnitude current pulse with short tailing edge is applied on the programmable volume of the phase change material. The temperature of the material exceeds the melting point which eliminates the polycrystalline order in the volume. When the reset pulse is terminated, the memory cell cools to “freeze in” the amorphous state. This cooling time about several nanoseconds is determined by the thermal situation of the memory cell and fall time of the reset pulse. In set process, a moderate magnitude current pulse with sufficient duration is applied to maintain the device temperature for crystal growth. The amorphous structural state or the polycrystalline structural state is ready by applying a low magnitude and long duration current pulse. The time-temperature relationship of the PCM is shown in Fig. 1.2.2.1. During the set and reset process, large Joule heating is applied on the phase change material, and hence, the power consumption is huge. How to reduce the operation power consumption is becoming the primary challenge

of the PCM.

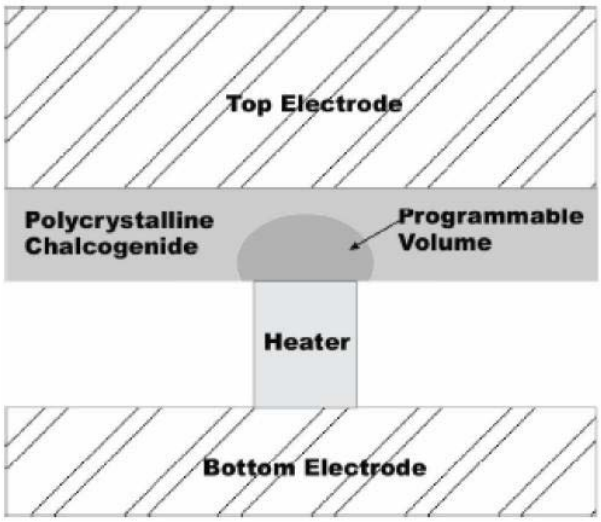

Fig. 1.2.1.1 Basic PCM cell

1.2.2 Ferroelectric Random Access Memory

Ferroelectric random access memory (FeRAM) [5][6] is a device typically fabricated by ferroelectric material. The ferroelectric material is a material with a spontaneous polarization and the polarization can be altered by applying electric field. The typical structure of the ferroelectric material is the perovskite structure (ABO_3), where the A, B and O atoms are located at corner, body center and face center of the cubic cell. The B atom has two thermodynamically stable positions which depend on the polarity of the applied electric field. The polarity hysteresis curve of the ferromagnetic material can be used for NVM application and this is so called ferroelectric random access memory (FeRAM). One of the typical structures of FeRAM

is the metal-ferroelectric-semiconductor FET (MFSFET) as shown in Fig. 1.2.2.1. The polarization of the ferroelectric material in FeRAM can affect the drain current of the transistor, and the memory effect of the typical MFSFET structure FeRAM is nonvolatile and with nondestructive readout property.

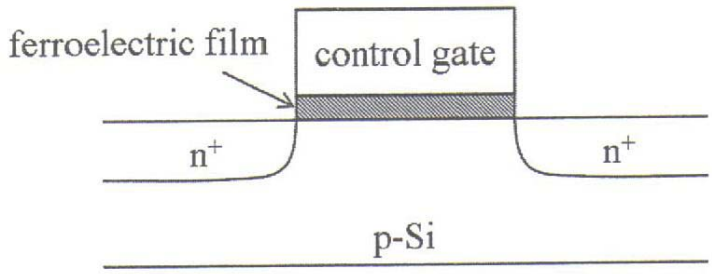

Fig. 1.2.2.1 Typical MFSFET structure of FeRAM

1.2.3 Magnetroresistive Random Access Memory

The Magnetroresistive Random Access Memory (MRAM) [7][8] cell is the magnetic tunneling junction which consists of two magnetic layers sandwiching a thin tunneling layer as shown in Fig. 1.2.3.1. One of the magnetic layers is fixed and kept in a specific direction, called reference layer. The other magnetic layer is used to switching its magnetic field so it could be parallel or antiparallel to the reference layer, called storage layer. This two magnetic states cause two different resistance states, so the two different logic states are generated. Although the MARM has many merits, the tunneling layer causes the scaling limitation of the device and becoming the most important challenge of MRAM.

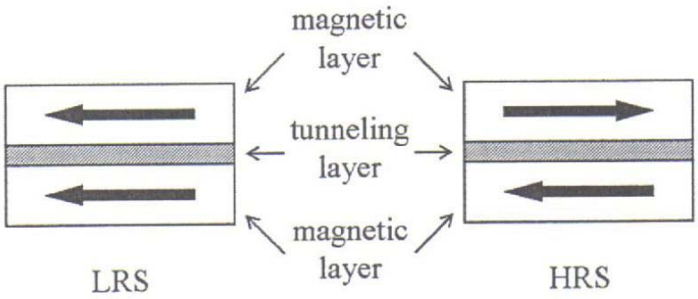

Fig. 1.2.3.1 Parallel state and antiparallel state of the MRAM

1.2.4 Resistive Random Access Memory

The resistive random access memory (RRAM) [9] cell is mostly designed into a metal- insulator-metal (MIM) sandwich structure. It can exhibit different resistance states by applying voltage bias. It is so called resistive switching (RS). The RS may generate more than two different resistance states by applying different compliance current or different reset voltage. Moreover, RRAM has merits of low operation voltage, high operation speed, excellent scalability, retention time, and endurance. And because of its very simple MIM sandwich fabrication sequence is compatible with the back-end process of standard CMOS process, it is very convenient to proposing into mass production in the market. However, the main issue of nowadays RRAM research is the physical mechanism of RS which are not well revealed. If the RS mechanism is cleared, we can expect the well-design RRAM to becoming the most ideally NVM.

1.2.5 Transparent Resistive Random Access Memory

Here we introduce one of the most future modern NVMs, the transparent resistive random access memory (TRRAM). TRRAM is the RRAM fabricated by glass substrate and using transparent conducting oxide for electrode. TRRAM research had been done by JW. Seo et al [10], and we know that the performances of TRRAM and non-transparent RRAM are not comparable. TRRAM could bring us a fully transparent device. We know that the transparent TFT is under developing nowadays. If we can put the transparent TFT with the transparent memory devices, the fully transparent electronics even a modern see-through electronic system may come true one day.

1.3 Introduction to Resistive Random Access Memory

1.3.1 Basic Resistive Switching Current-voltage Curves

In order to discuss the functions and the influences of each stack in the RS device structure, a brief introduction to the primary electrical properties is necessary. Suppose the RRAM device can operate between two different resistance states, the lower resistance state is called low-resistance-state (LRS) or on-state and the higher one is called high-resistance-state (HRS) or off-state. In this paper, we define the process that make the RRAM device change its resistance from LRS to HRS is set process. And the reset process turns the RRAM device from HRS into LRS. There are three sorts of RS operation polarization, unipolar[11], bipolar[12] and nonpolar[13], as shown in Fig. 1.3.1.1 and Fig. 1.3.1.2. The unipolar RS means the set and reset

process are happened in the same electrical polarity. And the bipolar RS means the set and reset process are happened in different electrical polarity. As for bipolar RS, it depicts that the RS phenomenon is observed as applying the specific polarity of the voltage and current biases to do the set process, and the reset process has to be done by applying the other polarity of the voltage and current biases. The nonpolar RS means that the device can be switched to another resistance state by applying a voltage regardless of the polarity. The first set process is called the forming process, because this process forms the filament of the device and the device could start the RS operation. The filament model is discussed in the following sections. But some RRAM devices start in the LRS. Because it does not need the forming process, it is called forming-free RRAM.

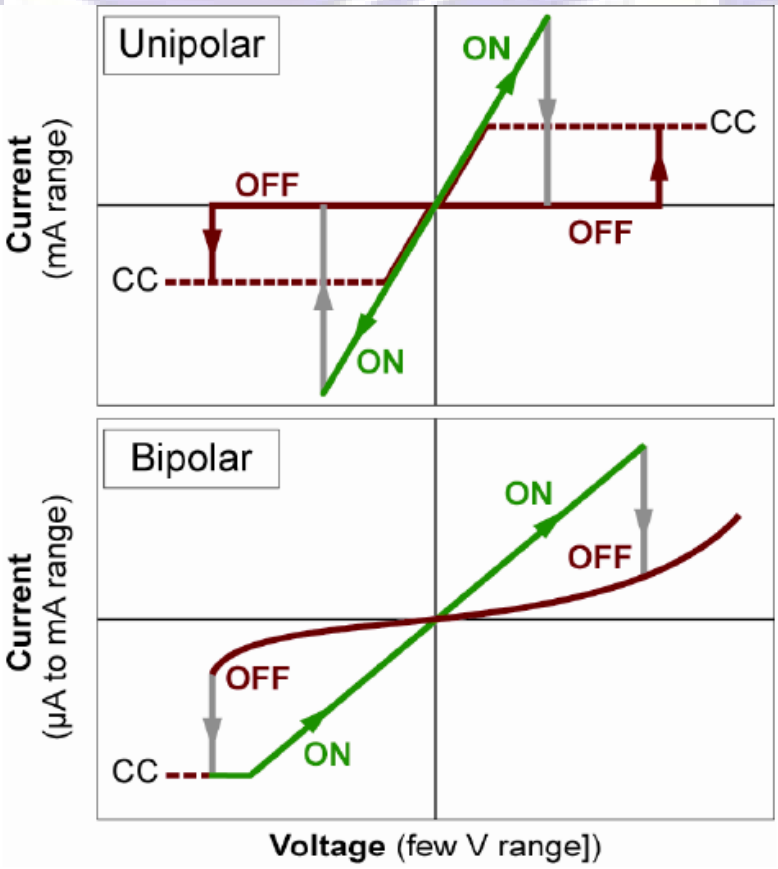

Fig. 1.3.1.1 Unipolar and bipolar type of RS operation

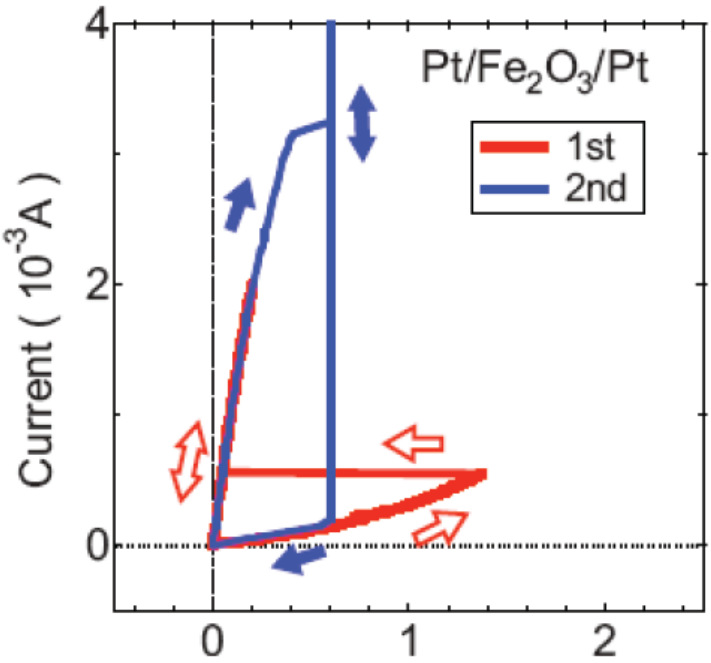

Fig. 1.3.1.2 Nonpolar RS operation

1.3.2 Basic Resistive Switching Device Structure

The basic RRAM device fabrication is a metal-insulator-metal (MIM) sandwiched structure, where the insulator often represents the RS material. The metal layer is not only stands for metal material but also for the low-resistivity electron conductor and sometimes for the ion conductor such as SrRuO (SRO) and $YBa_2Cu_3O_7$ (YBCO). Some researchers improved the RS properties by modified RS device structure, such as adding a reactive metal layer between the resistive layer and the electrode layer. In this paper, we chose glass substrate instead of silicon substrate and use transparent conducting oxide for electrode layer to demonstrate a fully transparent resistive random access memory.

1.3.3 Carrier Conduction Mechanisms

The RRAM device is operated between two resistance state, and both may follow different kinds of carrier conduction mechanisms according to the species and the related electrode combination. Although the RS mechanism is not totally clear, carrier conduction mechanism discussion is another way to discover RS mechanism might be.

There are six different kinds of carrier conduction, Schottky emission, Frenkel-Poole emission, tunnel or field emission, space-charge-limited current conduction (SCLC)[11][14], Ohmic conduction and ionic conduction. A brief comparison of these carrier conduction mechanisms are shown in Table 1.3.3.1. When the carriers pass across the interface between metal and insulator by thermionic emission, this carriers behavior is called Schottky emission. Schottky emission is believed to dominated the conduction mechanism of the HRS, which has also been reported in ZrO_2 an TiO_2-based RRAM device[15]-[17]. The Frenkel-Poole emission is the effect that exciting the trapped electrons into conduction band by field-enhance thermal excitation. There are Al_2O_3 and SZO-based devices obey the Frenkel-Poole emission[18]. The tunnel or field emission effect is the action of the electrons tunneling from the Fermi level of the metal into the conduction band of the insulator. This emission is strongly dependent on the applied voltage, but is essentially independent of the temperature. The space-charge-limited current is the current generated by carrier injected into the insulator and no compensation charge is present. SCLC only happens in Ohmic contact with lower electron mobility. Therefore the charge tends to be rapidly repulsive. And it is also independent of the temperature. The Ohmic conduction is results from thermally excited electrons hopping from one

isolated state into the next state [19]. The ionic conduction is very similar to carrier diffusion. The voltage and current dependence of ionic conduction is the same with Ohmic conduction at fixed temperature. In addition, each conduction mechanism may dominate in some voltage and temperature ranges. There are possibly more than one conduction mechanisms happening at one time and causing the current conduction in an insulator.

Table 1.3.3.1 Basic carrier conduction mechanism

mechanism	expression	voltage and temperature dependence
Schottky emission	$J = A^{*}T^{2}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right]$	$J \sim T^{2}\exp\left(+a\sqrt{V}/T - q\phi_B/kT\right)$
F-P emission	$J \sim E\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right]$	$J \sim V\exp\left(+2a\sqrt{V}/T - q\phi_B/kT\right)$
tunnel or field emission	$J \sim E^{2}\exp\left[-\frac{4\sqrt{2m^{*}}(q\phi_B)^{3/2}}{3q\hbar E}\right]$	$J \sim V^{2}\exp(-1/V)$
SCLC	$J = \frac{9\varepsilon_i\mu V^{2}}{8d^{3}}$	$J \sim V^{2}$
Ohmic conduction	$J \sim E\exp(-\Delta E_{ac}/kT)$	$J \sim V\exp(-1/T)$
ionic conduction	$J \sim \frac{E}{T}\exp(-\Delta E_{ac}/kT)$	$J \sim \frac{V}{T}\exp(-1/T)$

1.3.4 Resistive Switching Mechanisms

Although the exact resistive switching mechanism is a controversial issue, the filament model is often used and accepted extensively [20]. The filament model explains that the RS happened because of the formation and

rupture of the conducting filaments. The conducting filaments are confined, local and so tiny that is hard to be analyzed, and therefore, lots of nanoscale analysis instruments are necessary for filament studying. The electrical observations of filamentary conductions for RS are proposed by current bias method as well. By this method, the intermediate resistance states and anomalous resistance fluctuations between resistance states are observed during the transition from HRS to LRS, which is interpreted to be associated with filamentary conducting paths with their formation and rupture for the RS memory switching.

The oxygen migration near the interface of electrode layer and resistive layer is also a very popular way to explain the bipolar RS mechanism. Because the oxygen ions migrate by applied voltage bias, the oxygen vacancies are generated to allow electrons go through the insulator easier. The oxygen vacancy generation switches the device into LRS. As the opposite bias applied, the oxygen ions are pushed back into the insulator to fill the oxygen vacancies and switch the device back into HRS. This oxygen migration model usually combines with SCLC carrier conduction mechanism.

Chapter 2
Experimental Details

2.1 Fabrication of Resistive Switching Memory Devices

2.1.1 Sample Preparation

The Indium Tin Oxide (ITO) -coated glass was used for the TRRAM substrate. The ITO-coated glass was cleaned by the standard cleaning process. The cleaning procedures for ITO-coated glass substrate are as the following steps：

Step 1：ITO-coated glass substrate is taken into DI (de-ionized) water bath with ultrasonic oscillator environment for 10 minutes to remove the particles.

Step 2：Using nitrogen gun to dry the ITO-coated glass substrate, and repeat step 1.

Step 3：ITO-coated glass substrate is taken into acetone liquor bath with ultrasonic oscillator environment for 10 minutes to remove the organic residues.

Step 4：Using nitrogen gun to dry the ITO-coated glass substrate, and repeat

step3.

Step 5：ITO-coated glass substrate is taken into isopropyl alcohol liquor bath with ultrasonic oscillator environment for 10 minutes.

Step 6：120℃ baking for 15 minutes.

After the standard cleaning process, the substrate with bottom electrode was well prepared and ready to the next process. A 25-nm-thick HfO_2/Al_2O_3 multi-layer stack resistive switching film was deposited on the cleaned ITO-coated glass substrate by atomic layer deposition (ALD) system.

2.1.2 Atomic Layer Deposition of Resistive Switching Layer

After the standard cleaning process, the resistive switching layer is going to be deposit on the bottom electrode. Atomic layer deposition is a chemical vapor deposition (CVD) method of self-limiting thin film deposition. (the amount of film material deposited in each reaction cycle is constant), continuous surface chemistry that deposits conformal thin-films of materials onto substrates of varying compositions. By keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as ~0.1 Å (10 pm) per monolayer. Separation of the precursors is accomplished by a purge gas (typically nitrogen or argon) after each precursor pulse to remove excess precursor from the process chamber and prevent 'parasitic' CVD deposition on the substrate.

The HfO_2/Al_2O_3 multi-layer stack resistive switching film is deposited

by Savannah 100 ALD system (Cambridge Nanotech Inc.) with 100℃ deposition temperature. During the deposition, the chamber base pressure is set at 0.1 torr and the carrier gas for the precursors was high-purity N_2 gas (flow rate＝20 sccm). The precursors of Al_2O_3 are trimethylaluminum (TMA) and H_2O and the precursors of HfO_2 are Tetrakis (dimethylamino) hafnium (TDMAHf) and H_2O. The sequence of pulses for one cycle deposition of Al_2O_3 is TMA (0.03s)/ purge (5s)/ H_2O (0.05s)/ purge (5s), and the TDMAHf (1s)/ purge (5s)/ H_2O (0.05s) purge (5s) sequence is defined as one cycle deposition of HfO_2. A cycle produced ~1 Å as determined by ellipsometry (EP3, Nanofilm Tech.). This method is used for stacking the three different kinds of period multi-layer resistive switching layer.

2.1.3 Top electrode

We use two kinds of top electrode, one is a 100nm-thick ITO conducting film deposit by DC sputtering and the other is the tungsten probe electrode to form the MIM sandwich structure. Sputtering deposition is a physical vapor deposition (PVD) method of thin film deposition, ejecting materials from the target onto the sample surface.

2.2 Material Analyses

2.2.1 X-ray Diffraction (XRD)

The crystal structure of the RS layer is investigated by the X-ray diffraction. The scanning step was 0.02°, and the scanning speed was 4°/min. According to the theory of X-ray diffraction, the average grain size of each orientation can be estimated by using Scherrer's equation.

2.2.2 Transmission Electron Microscopy (TEM)

Transmission electron microscopy is used for observing the thickness, interface and the specific local region of the resistive random access memory device. When electron beam is transmitted through an ultra thin specimen and interacting with it, an image can be generated by the transmission electrons. This image is focused and magnified by an objective lens and to be detected by an image sensor, then turns into a digital picture.

2.2.3 Atomic Force Microscopy (AFM)

Atomic force microscopy is used for detecting the surface roughness and the surface morphology of thin films.

2.3 Electrical Analyses

2.3.1 Current-Voltage Measurement

The current-voltage (I-V) characteristics of the resistive random access

memory devices are performed by Agilent 4156A. The resistive switching phenomenon is that the resistivity of the device can be altered by applying a specific voltage bias, which is reproducible. During the switching into the low resistive state (LRS), a large current pass through the device and a current compliance is imposed on the device to prevent the electrical damage.

2.3.2 Endurance Measurement

The endurance is the number that a device can be stably operated among various memory states by sweeping voltage bias, and the endurance cycle with excellent stability is expected to be as large as possible. The more endurance cycles the device can reach means the more stable the device is. Endurance measurement by sweeping voltage bias is achieved by Agilent 4156A.

2.3.3 Data Retention Time Measurement

The data retention time is the time of the stored data which can be kept without any power supply. Two identical devices are switched into different resistance states. After a specific period of time, read voltage is applying to read the resistance of the device. The read voltage is the voltage used for reading the resistance in the endurance measurement, which cannot change the device into another resistance state. The data retention time measurement is measured by Agilent 4156A.

2.3.4 Nondestructive Readout Measurement

The nondestructive readout measurement is applying a DC voltage bias to read the current of various memory devices to estimate the maximum read time and the stability of the memory states. The nondestructive readout measurement is measured by Agilent 4156A.

Chapter 3
Result and Discussion

3.1 Physical Analysis of Multi-layer Resistive Switching Film

We show our physical analysis result in this section. The reasons why we use glass for substrate and ITO for electrode are making fully transparency device. It is named transparent resistive random access memory (TRRAM). In order to investigate how resistive switching works in amorphous oxide layer, we design our resistive switching layer into a series of multi-layer oxide insulator by Atomic layer deposition. A ratio 6:1 for HfO_2 : Al_2O_3 has been chosen and make it to 38-cycle to reach about 25nm oxide thickness. Because this sample changes its material 76 times in about 25nm, it is not enough thickness for getting crystallized. Then we double the thickness of each cycle but deposited half cycles of the multi-layer insulator. Then do it again. Here comes our three samples, Sample 1 (HfO_2:Al_2O_3=6:1, 38-cycle, 260 Å), Sample 2 (HfO_2:Al_2O_3=12:2, 19-cycle, 260 Å) and Sample 3 (HfO_2:Al_2O_3=24:4, 9-cycle, 260 Å). In this thesis, we named these samples by its cycles, 9-cycle, 19-cycle and 38-cycle. After depositing the resistive switching layer, we use DC sputtering to deposit 100 nm ITO as the top electrode of resistive memory devices. Also we use the tungsten probe as top electrode of resistive memory devices. In this thesis, we discuss the tungsten probe top electrode memory device mostly.

The transmittances of the three samples are measured in the visible light region from 400 nm to 800 nm wavelength. Fig. 3.1.1. The transmittance including the substrate is approximately 81% averaged, maximum: 86%, minimum: 76%.

The cross-section HR-TEM images of the three samples with ITO top electrode are shown in Fig. 3.1.2, Fig. 3.1.3 and Fig. 3.1.4. Obviously, we can see the multi-layer configuration of 9-cycle and 19-cycle in Fig. 3.1.2 and Fig. 3.1.3. In addition, because of each Al_2O_3 layer has only one monolayer in 38-cycle, it has no interface configuration in oxide layer as we expected before and is shown in Fig. 3.1.4. Each sample demonstrates analogous amorphous phase type. Moreover, the bottom electrode ITO films showed nearly polycrystalline configuration. The oxide layer thickness of each sample is about 26nm.

The surface roughness is measured by AFM, as shown in Fig. 3.1.5, Fig. 3.1.6 and Fig. 3.1.7. The mean roughness of the samples is about 2~3 nm. As a result, 9-cycle has the smoothest surface. And the Fig. 3.1.8 shows the XRD patterns of these samples. The four peaks at 30.2°, 35.3°,50.6°, and 60.1° are caused by the bottom electrode ITO film. Therefore, according to these XRD patterns the multi-layer resistive switching layers are amorphous films, as we expected before.

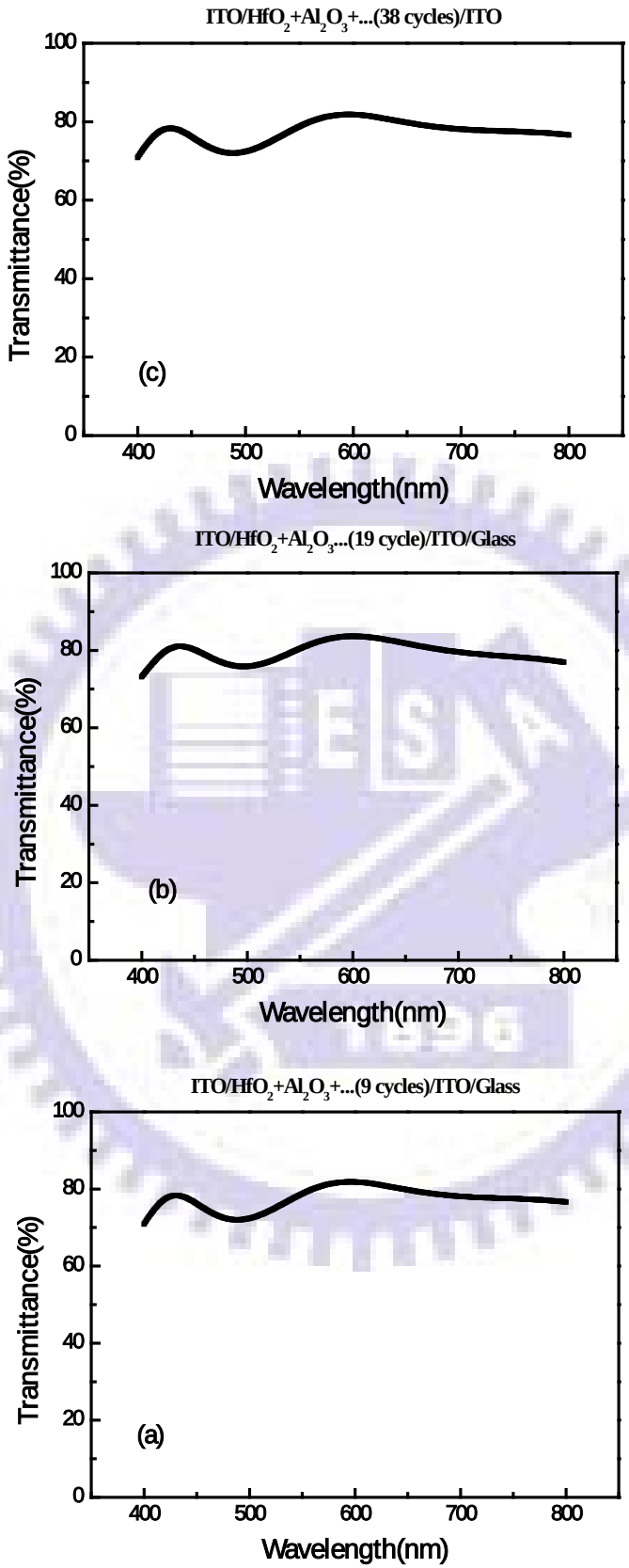

Fig. 3.1.1 Optical transmittance spectrum of 9-, 19- and 38-cycle devices

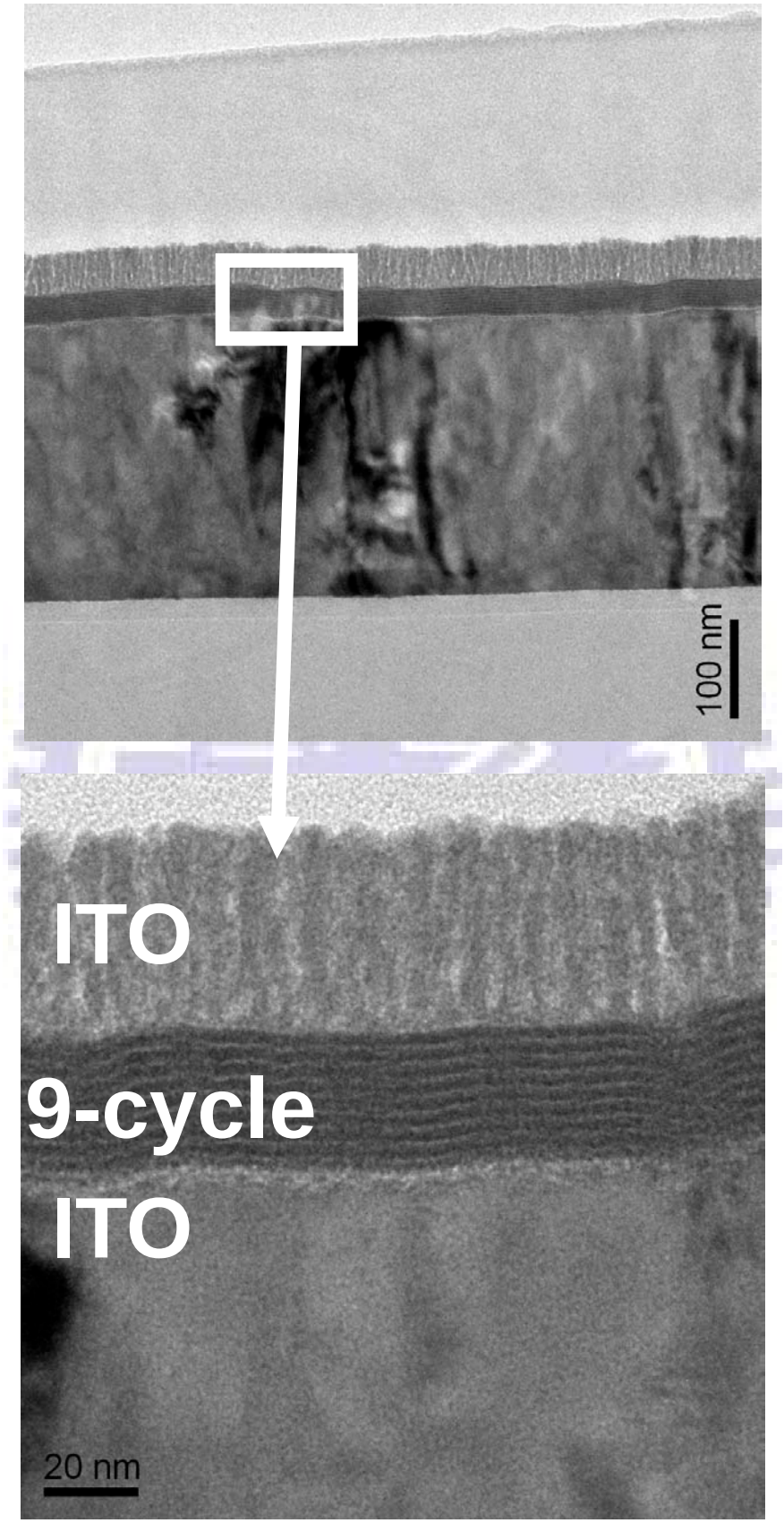

Fig. 3.1.2 The cross section HR-TEM images of ITO/9-cycle/ITO memory devices

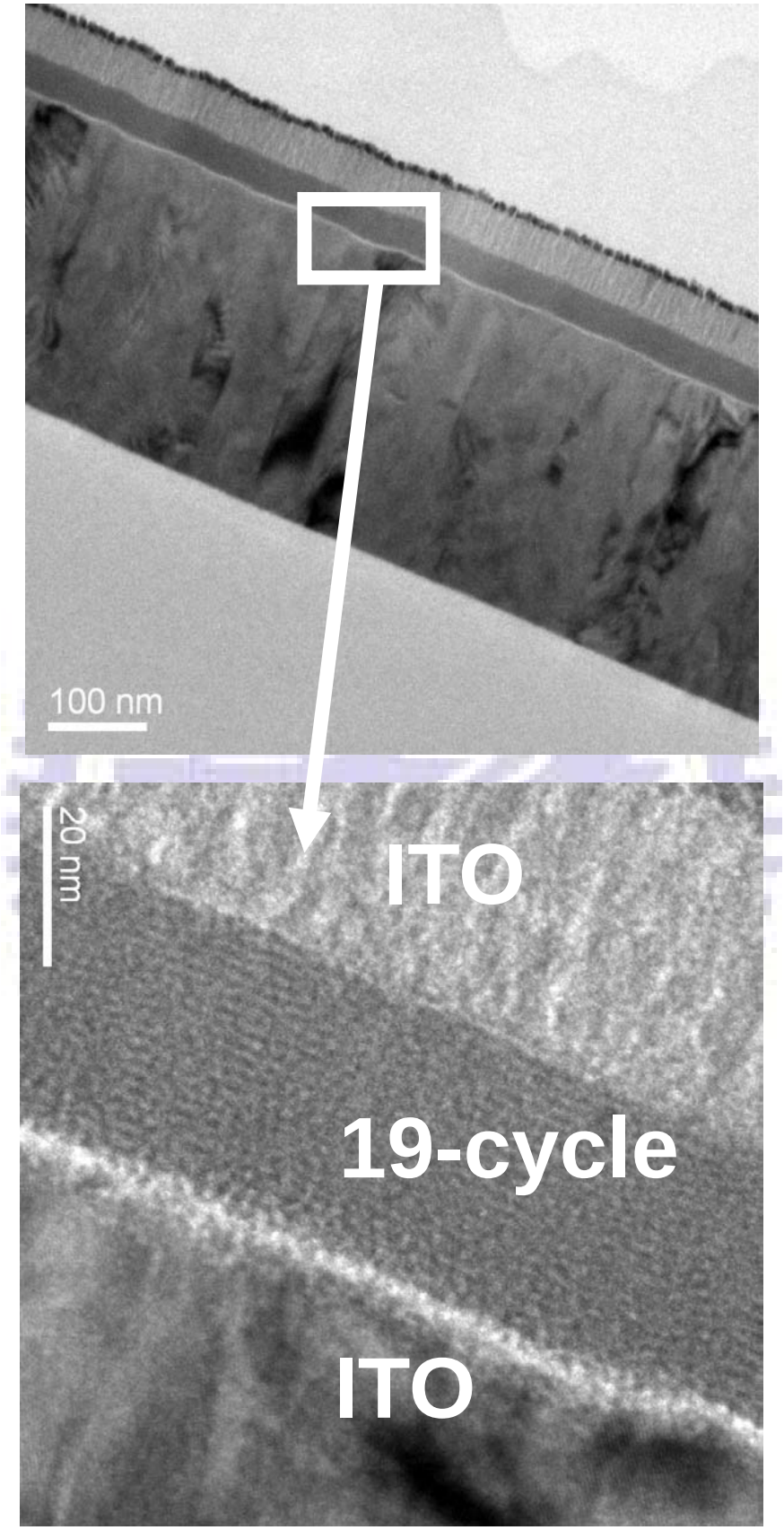

Fig. 3.1.3 The cross section HR-TEM images of ITO/19-cycle/ITO memory devices

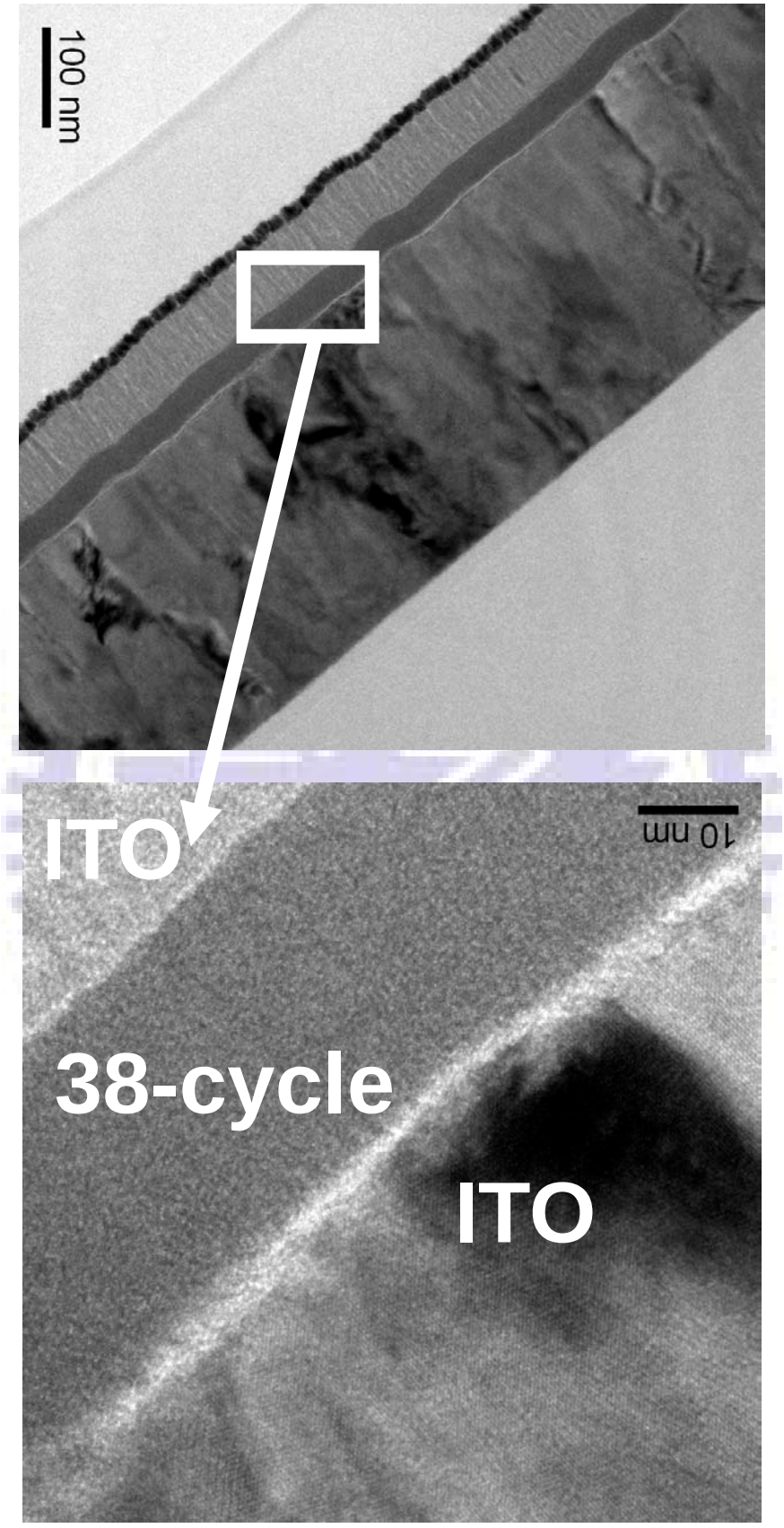

Fig. 3.1.4 The cross section HR-TEM images of ITO/38-cycle/ITO memory devices

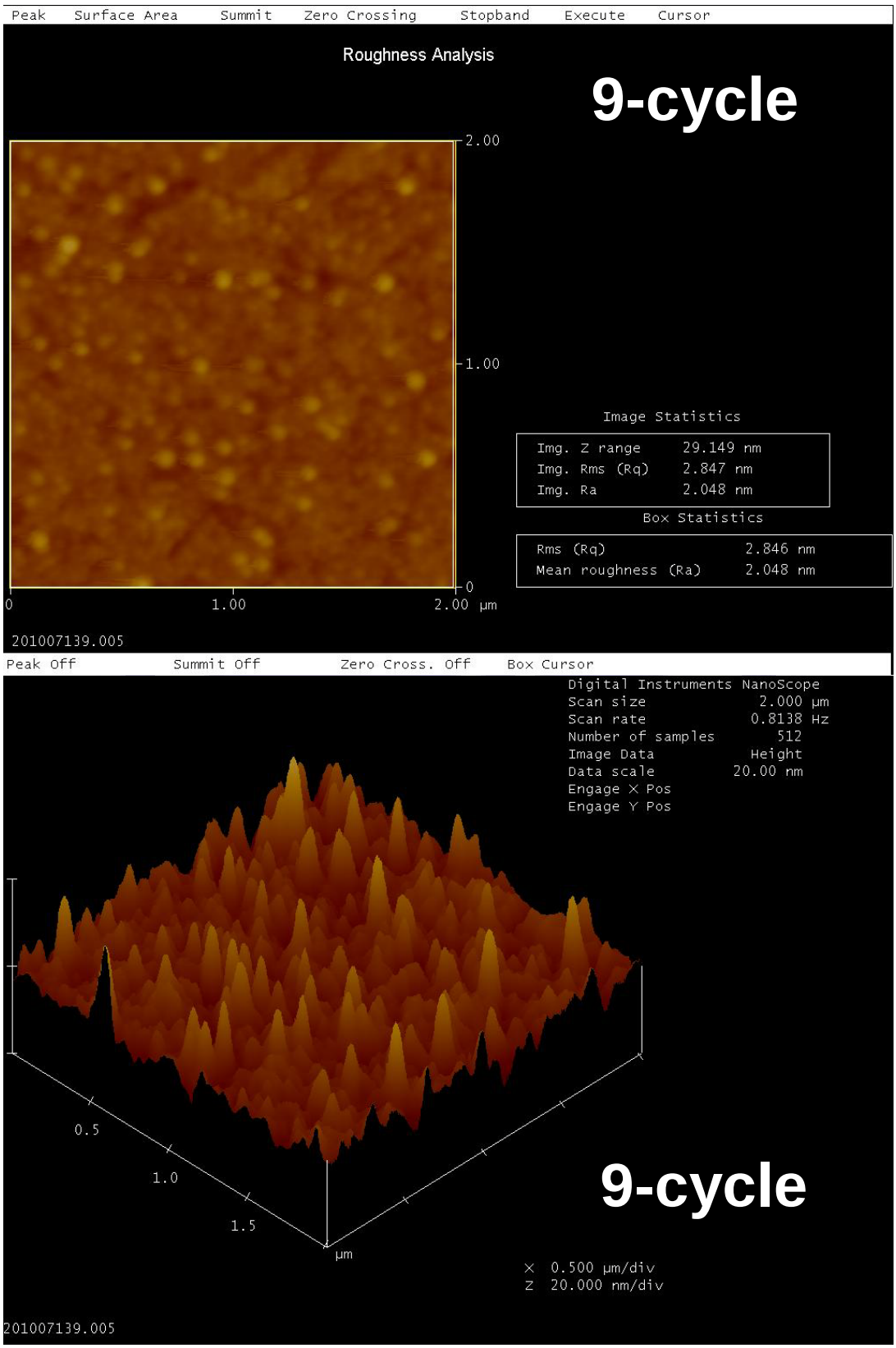

Fig. 3.1.5 The surface AFM images of 9-cycle

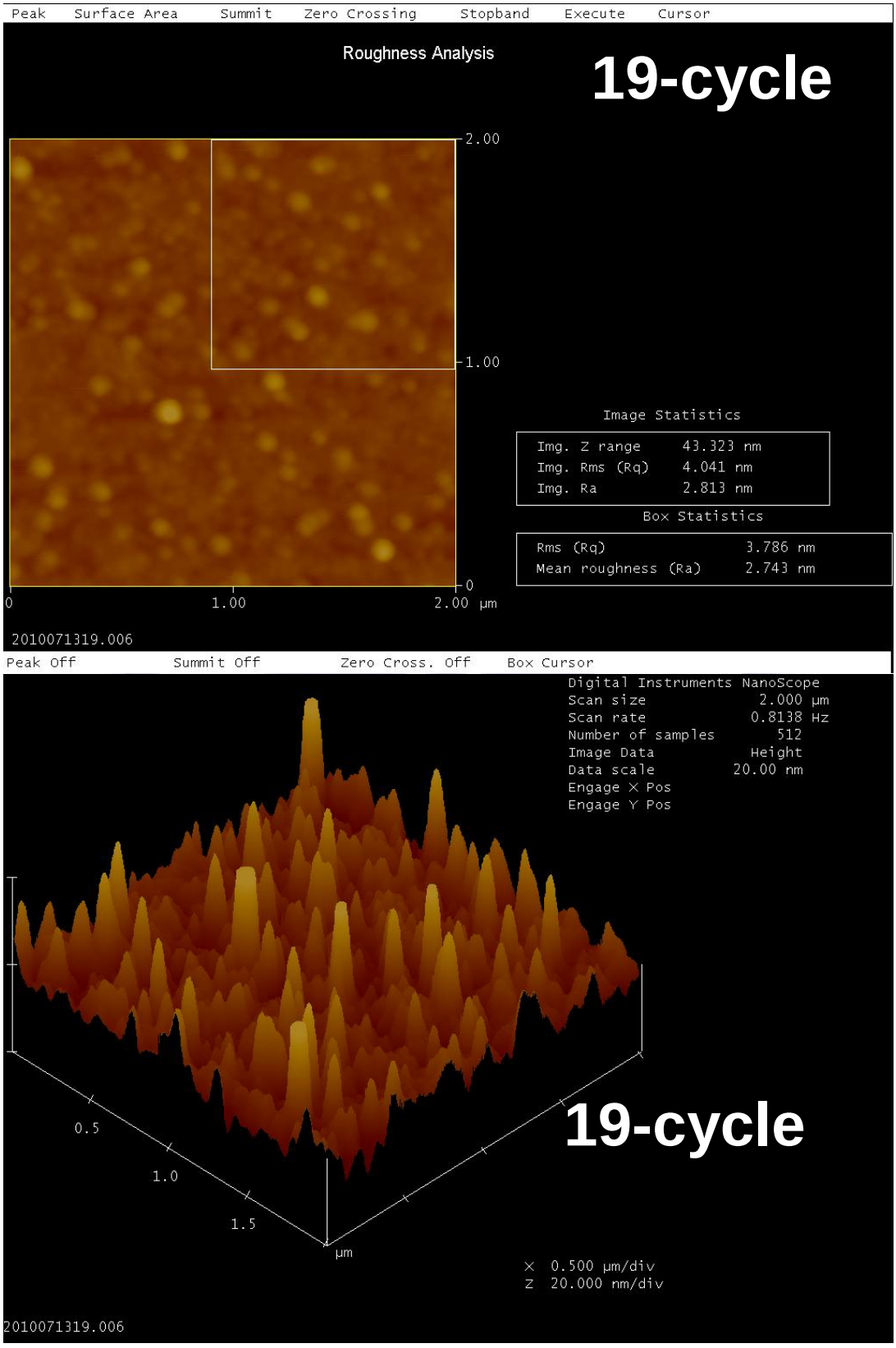

Fig. 3.1.6 The surface AFM images of 19-cycle

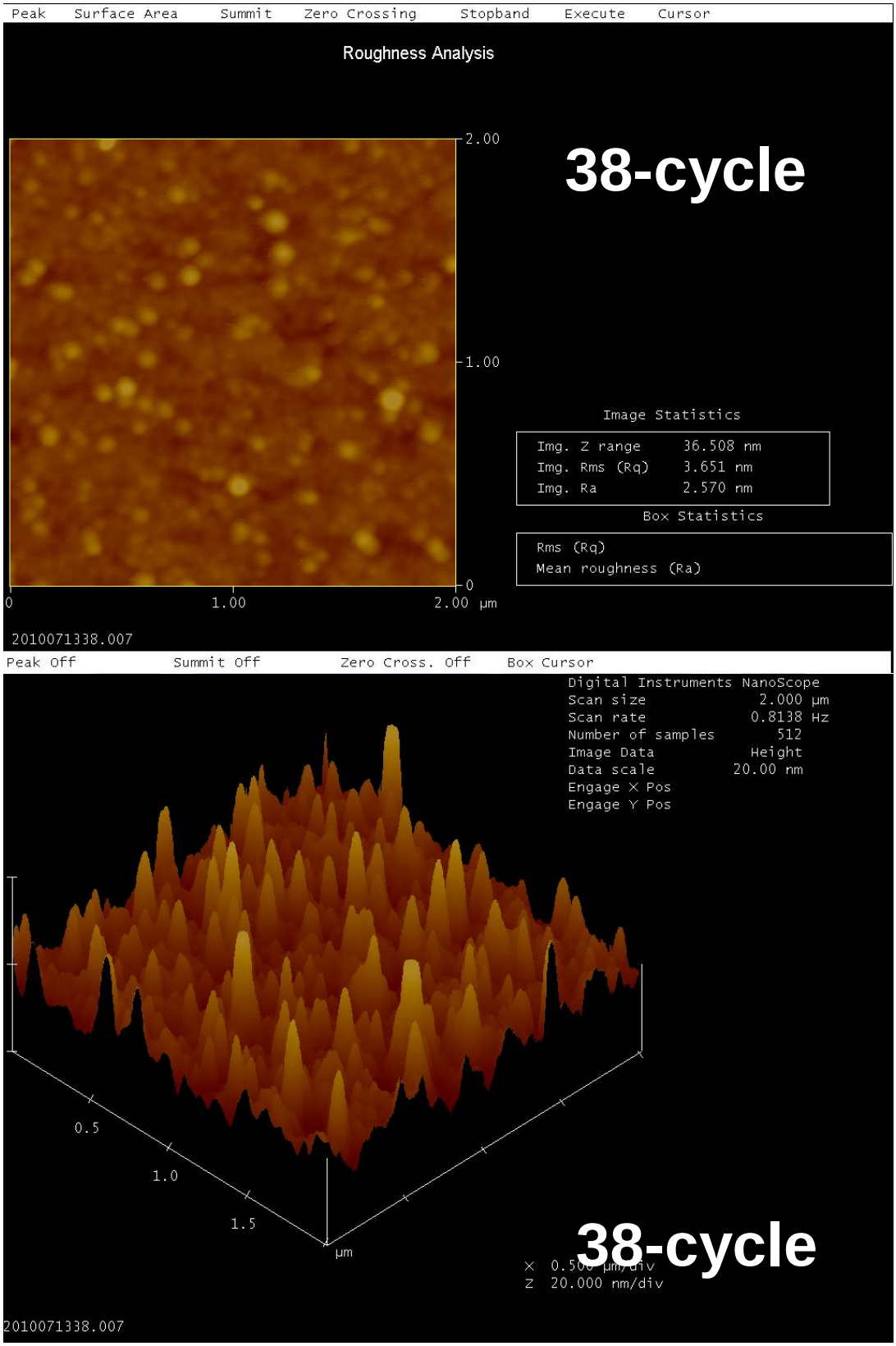

Fig. 3.1.7 The surface AFM images of 38-cycle

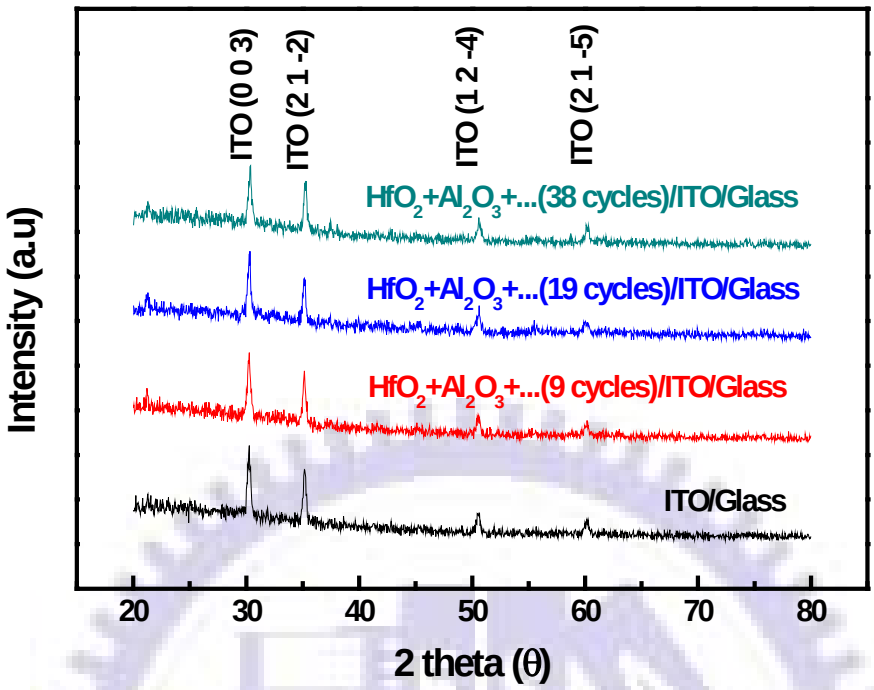

Fig. 3.1.8 The XRD patterns of 9-cycle/19-cycle/38-cycle

3.2 Electrical characteristics of resistive switching layer

In order to turning the insulator film into a resistive switching layer, we have to apply the forming process. In previous report [21]-[23], the forming process is defined as applying a high voltage bias to make a soft breakdown (SBD) happened to the insulator film, and this SBD switches it form original state to LRS. After forming process, multi-layer resistive switching memory device can be switched between LRS and HRS. Fig 3.2.1, Fig 3.2.2 and Fig 3.2.3 show the I-V curve of these devices. Obviously, the hysteresis can be observed for The-9-cycle devices /19-cycle/38-cycle.

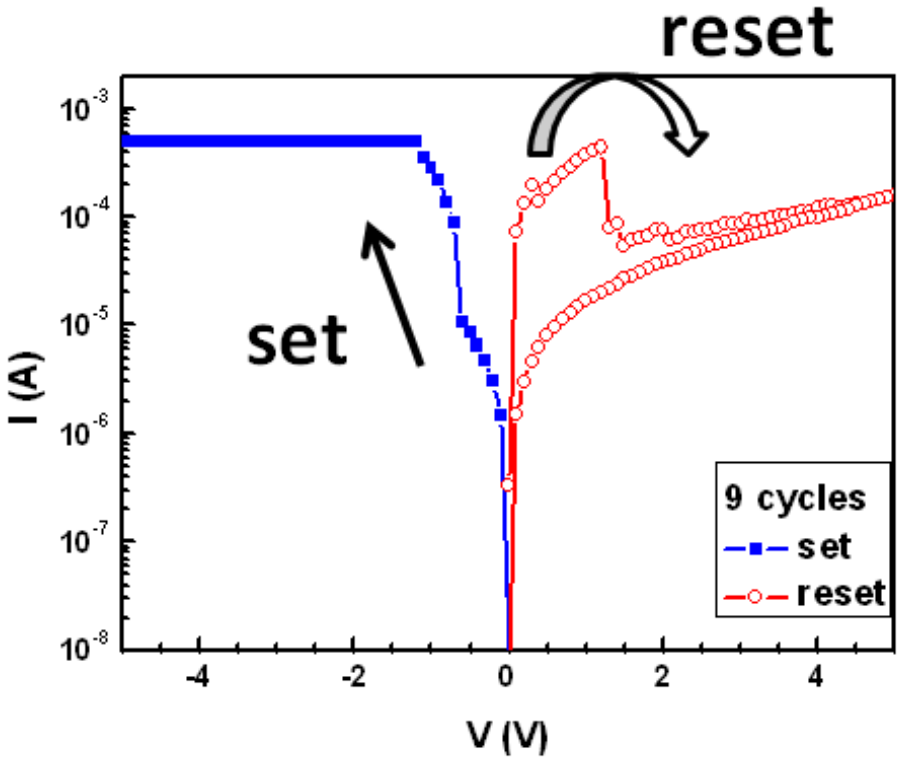

Fig 3.2.1 Resistive switching behavior of 9-cycle

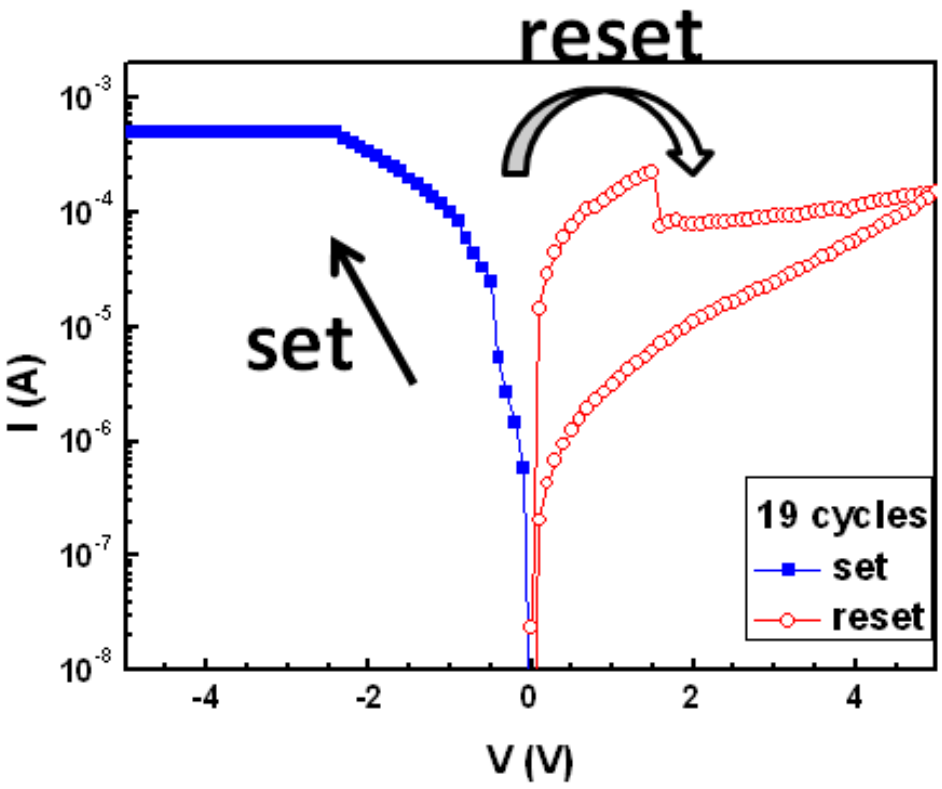

Fig 3.2.2 Resistive switching behavior of 19-cycle

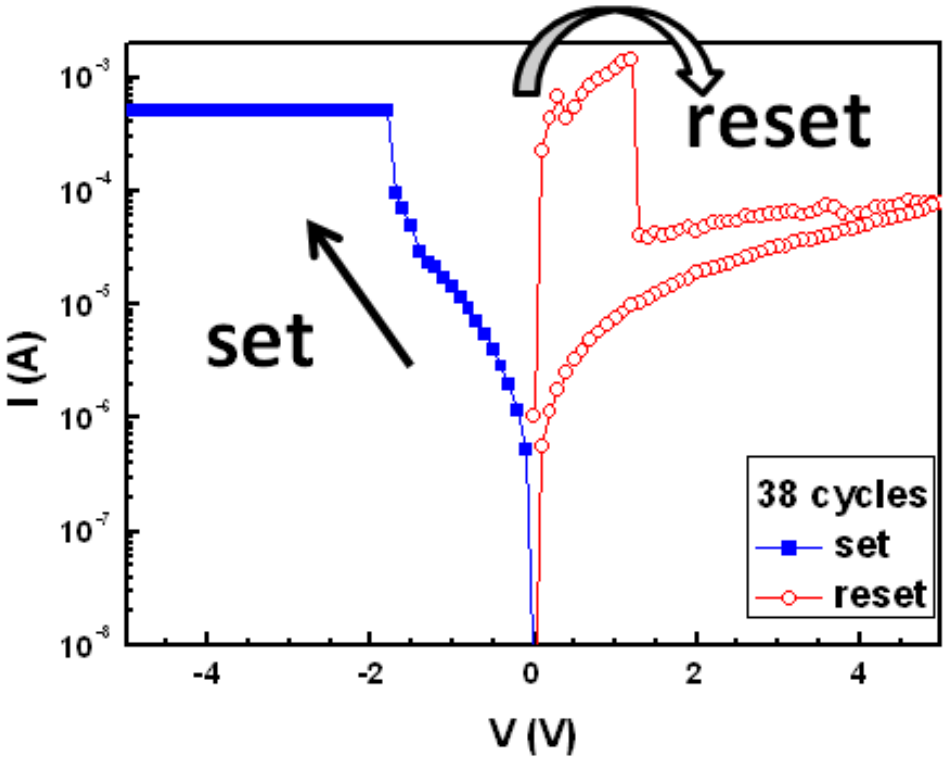

Fig 3.2.3 Resistive switching behavior of 38-cycle

3.3 Resistive Switching Properties of Multi-layer Resistive Switching Film

In this section, we demonstrate the electrical properties of basic resistive switching characteristics, set/reset voltage distribution dispersion, retention time, endurance cycles and resistances of LRS and HRS

3.3.1 Electrical Property

At the first time we applying a negative voltage bias on the device, the forming process, filaments have been formed in the device, the device has been switched to LRS. Then a positive voltage bias is applied on the device, this reverse bias could switch the device back into the HRS, this is called the reset process. After the forming process and the first reset process, a negative voltage bias apply to the device again and this time it could make the device switch to LRS again, this is called the set process. Then we could keep doing set and reset process to make the device switch between LRS and HRS again and again.

When set process is happening the device switched to LRS. It needs a current compliance in order to protect the device from the permanent damage by sudden high current. This current compliance is also a very important

operation parameter of the device. Different compliance currents cause different LRSs. As shown in Fig. 3.3.1 , the larger compliance currents enhance hysteresis curve. This means the larger compliance current cause lower LRS, as shown in Fig. 3.3.2. The lower LRS also induce lager HRS/LRS ratio. This phenomenon might be attributed to that because lager compliance current forms stronger conducting filaments and cause the LRS becoming lower. In this reset process, the stronger conducting filaments need more energy power to rupture [24]. However, X. CaO et al. [25] believed that the switching current and voltage depend on the microstructures and stoichiometric of the materials. According to Kim et al [26], this can be related to the average power dissipated at SET and RESET processes.

The reason of filament rupture can be considered of the temperature of forming filaments, using the steady state temperature model, where the equation is given by $T_m=(T_0^4+J^2\rho\gamma/2P_w)^{1/4}$ [27]. T_m is the filaments temperature raised by Joule heating, T_0 is the room temperature (=300K), J is the current density, ρ is the sample resistivity. γ is the filament radius, and P_W is the radiative loss parameter of the filament. This result about the Joule heating effect is important factor for the RESET. However, there is another way to enlarge the HRS/LRS ratio. As shown in Fig. 3.3.3 and Fig. 3.3.4, the lager stop voltage can also enhance the hysteresis curve by making the HRS higher. These two phenomena help us to decide what compliance current and stop voltage we should chose for operating the device. And these two phenomena had been discovered by HY. Lee et al [11].

We chose 500 uA for compliance current and 5 V for stop voltage to

endurance experiment and read HRS/LRS resistances by 0.1 V. The results of these devices are shown in Fig. 3.3.5, Fig. 3.3.6 and Fig. 3.3.7. Obviously, these three kinds of devices have very different result. The-9-cycle devices has the best performance over 1250 cycle times. The 19-cycle could be operated to about 950 cycle times. And the 38-cycle has a result about 300 cycle times. Therefore, the set/reset voltage distributions are shown in Fig. 3.3.8, the average set voltage and the standard deviation are -1.258 V, 0.162 V (9-cycle), -1.927 V, 0.92 V (19-cycle) and -1.706 V, 0.932 V (38-cycle), the average reset voltage and the standard deviation are 1.275 V, 0.193V (9-cycle), 1.867 V, 0.375 V (19-cycle) and 1.412 V, 1.131 V (38-cycle). Obviously 9-cycle has the tighter distribution of set/reset voltage and the operation voltage is also the smallest. According to the above result, 9-cycle must have some good property that can help the resistive switching become more stable. And the comparison of these devices is shown in Table. 3.3.1.

3.3.2 Resistive Switching Localization Test

We wonder what mechanism is of the resistive switching and what cause the difference among the three devices. So we start with the resistive switching localization test. Here we have to make a description of how we operate the device. Generally, the typical set/reset process is applying a voltage bias to the top electrode and the bottom electrode is grounding. In this test, another tungsten probe is used for second top electrode and is grounding as the bottom electrode used in typical set/reset process, as shown in Fig. 3.3.9. Unlike the typical operation, this test is just like applying a

apply the voltage bias on the twice thicker resistive switching layer with a conducting ITO layer in the middle and this middle conducting layer could split the resistive switching layer into two sides, the anode side and the cathode side. Where the anode side is defined by the voltage bias we applied for the forming process. Here we use negative bias for the forming process, so the side we applied bias is the cathode side and the other side, which is grounding, is the anode side. We can apply a small read voltage bias to get to know the resistance of both side and find out which side is the resistive switching happening.

This experiment had been done by KM. Kim et al [28]. The READ 1, READ 2 and READ 3 are shown in Fig. 3.3.10. READ 1 finds out the resistance of the cathode side and READ 2 is going to read the resistance of the anode side. READ 3 helps us to know if the device has been separated into anode side and cathode side by calculate the READ 1 resistance plus READ 2 resistance is equal to the READ 3 resistance. The results of this resistive switching localization test are shown in Fig. 3.3.11, Fig. 3.3.12 and Fig. 3.3.13. Obviously, all the READ 1 resistances are not switching, but the READ 2 resistances are switching its resistance after each set/reset process. Even though the conducting filament is going through the entire resistive switching layer, the resistive switching could still be localized on the anode side.

3.3.3 Retention Time Property

As a nonvolatile memory, storing data without applying bias is a very important property. The retention time means how long does the data can be stored in the memory. The devices had been put in our retention time experiment and could stored data more than 10^4 seconds at room temperature, as shown in Fig. 3.3.14, Fig. 3.3.15 and Fig. 3.3.16, and are without apparently degradation. Therefore, these three devices could be developed as nonvolatile memories.

3.3.4 Nondestructive Readout Property

The previous section mentioned that we use 0.1V bias to read the resistance. Therefore, a no destructive read out experiment gives to the devices to find out does the small read voltage really not affect the resistance state. Each device is applying a voltage bias of 0.6V, which is much larger than the 0.1V read voltage, to read the current of various memory states. All the devices can survive more than 2000 seconds at RT, based on this result, as shown in Fig. 3.3.17, Fig. 3.3.18 and Fig. 3.3.19, the maximum read times and the stability of the memory states can be estimated.

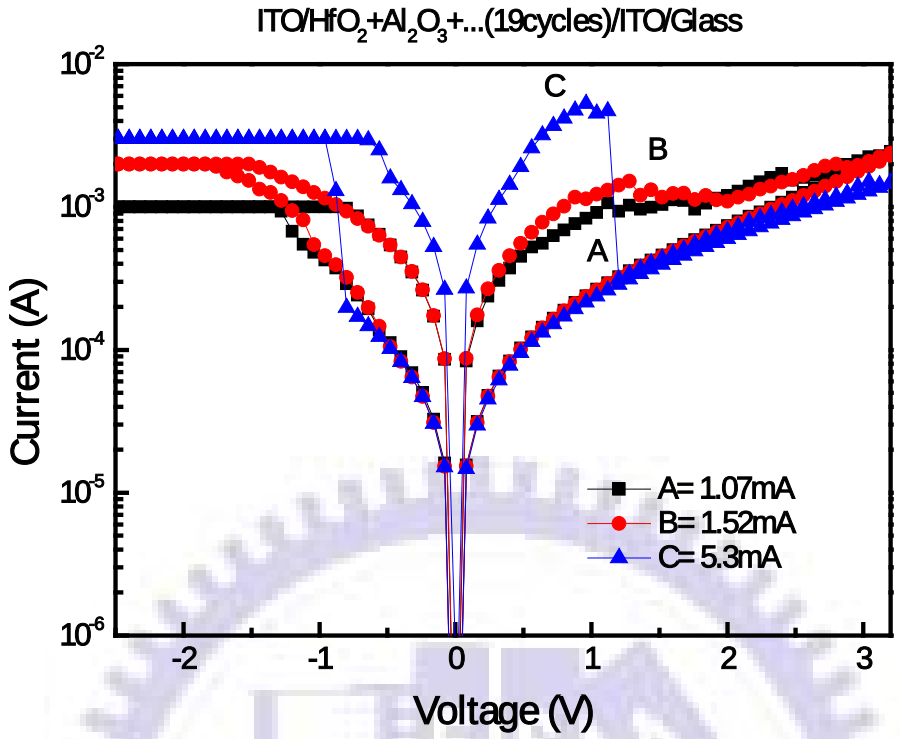

Fig. 3.3.1 (I-V) Different LRS due to different compliance current for 19-cycle

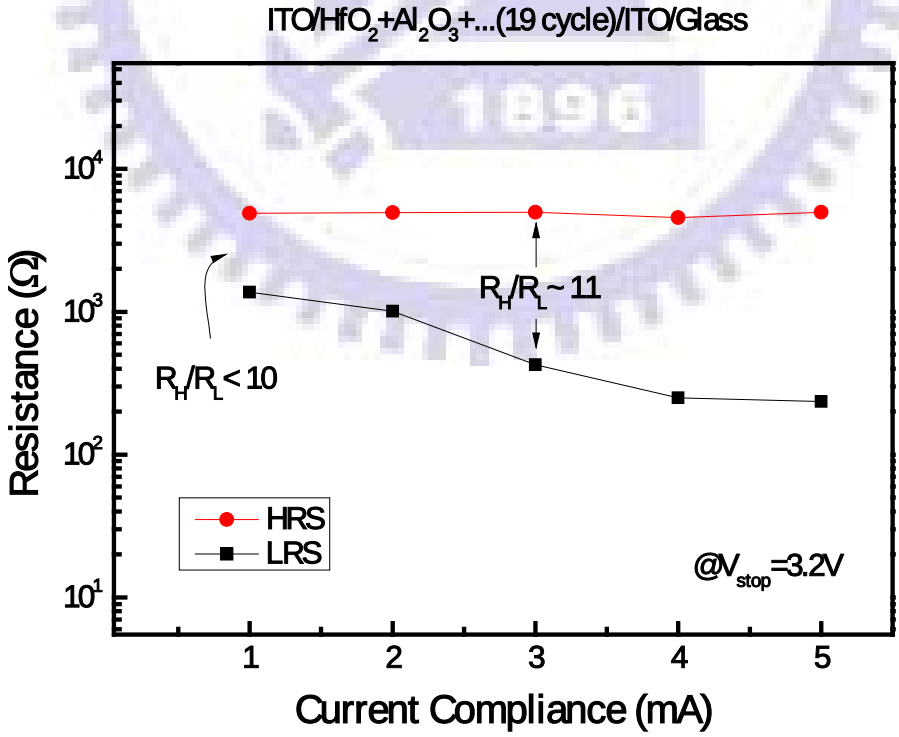

Fig. 3.3.2 (R-I) Different LRS due to different compliance current for 19-cycle

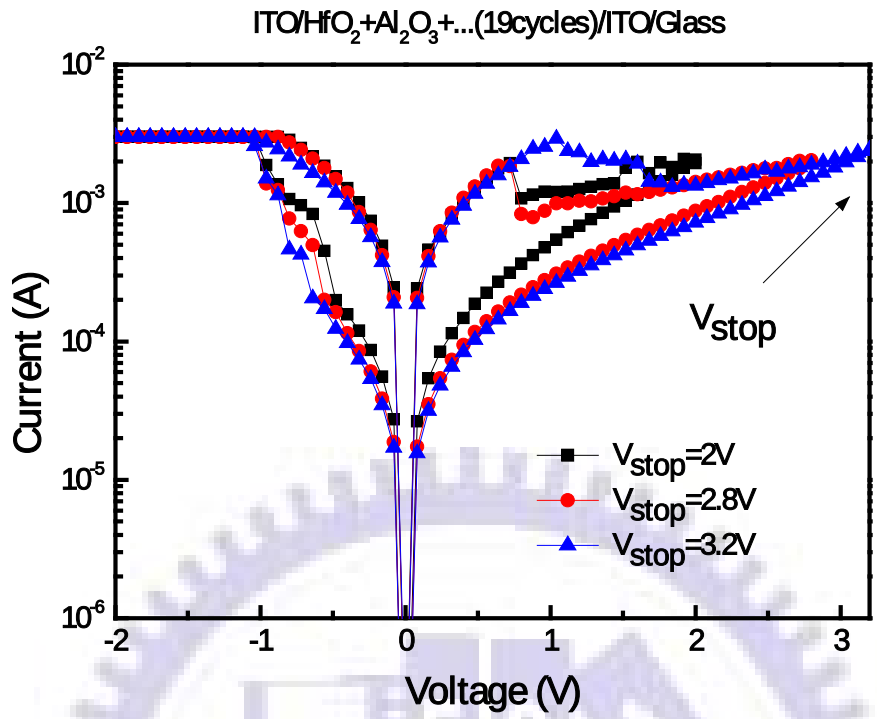

Fig. 3.3.3 (I-V) different stop voltage cause different HRS for 19-cycle

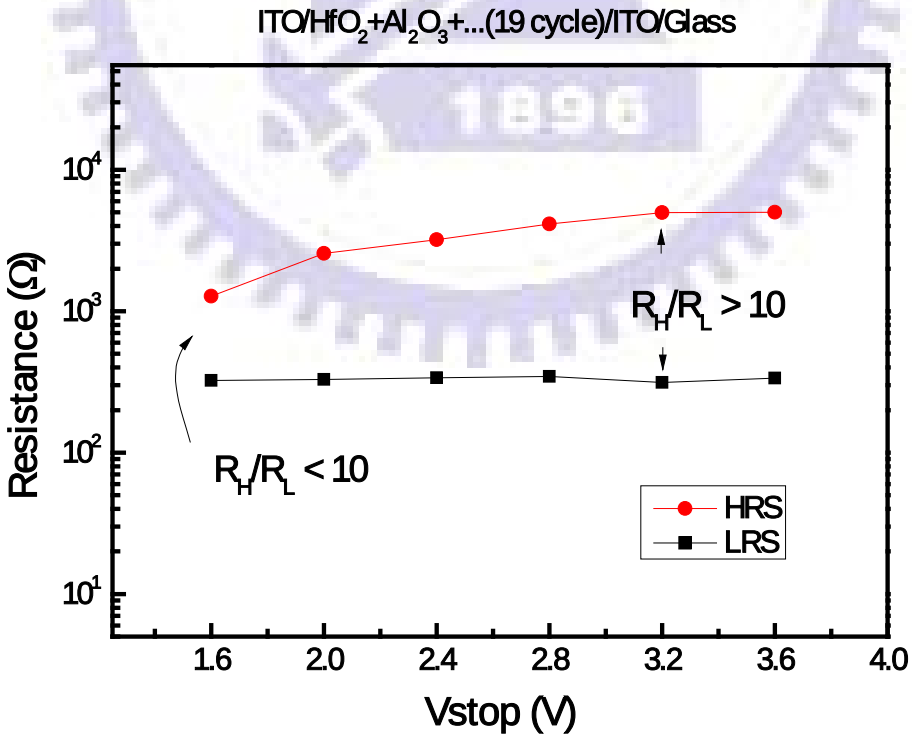

Fig. 3.3.4 (R-V) different stop voltage cause different HRS for 19-cycle

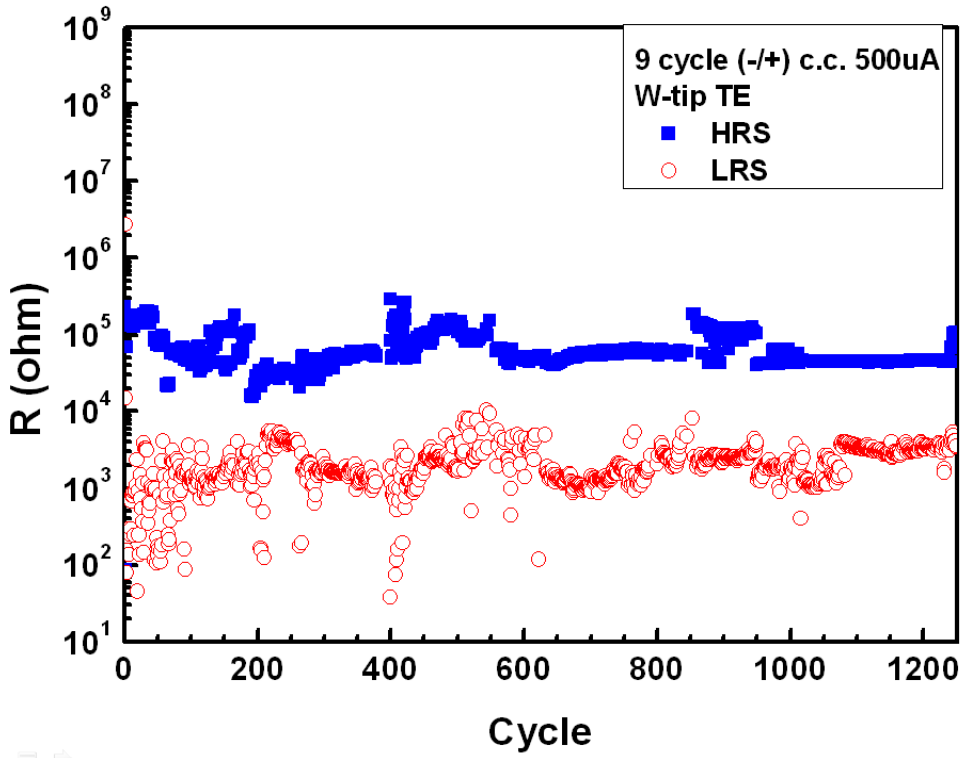

Fig. 3.3.5 Endurance experiment of 9-cycle

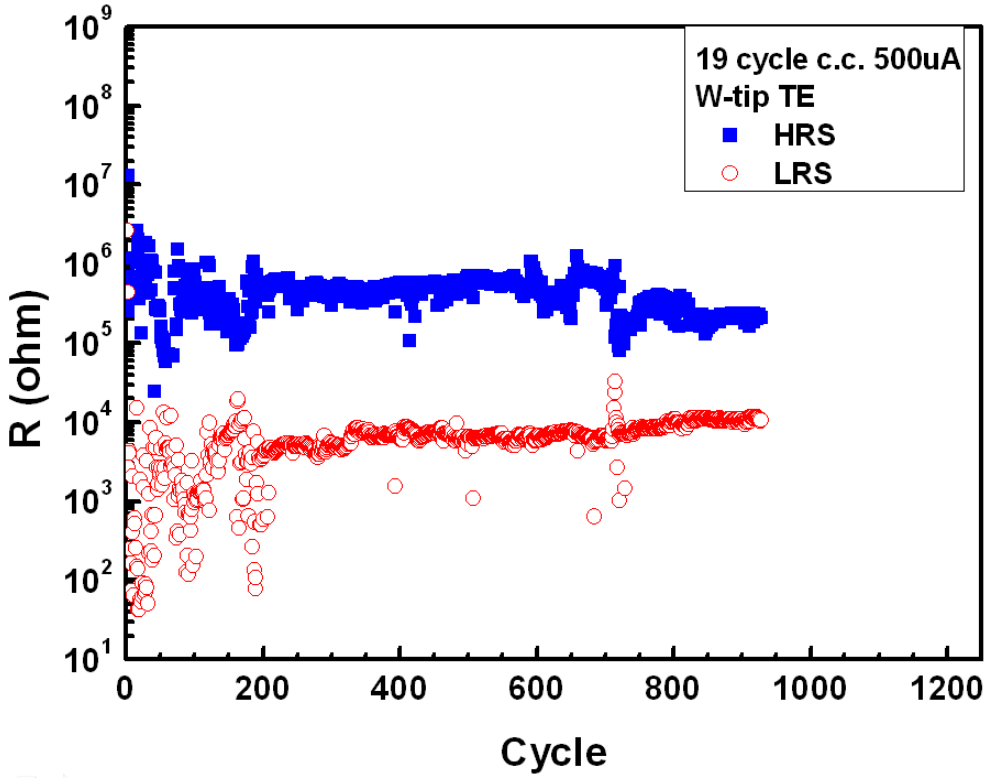

Fig. 3.3.6 Endurance experiment of 19-cycle

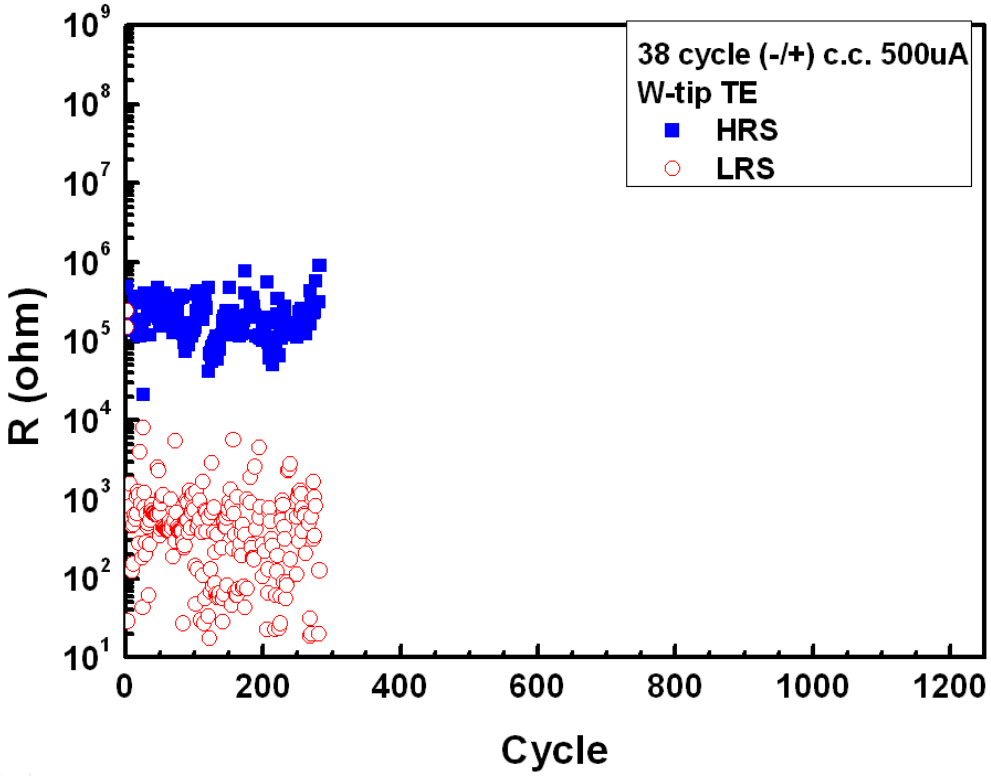

Fig. 3.3.7 Endurance experiment of 38-cycle

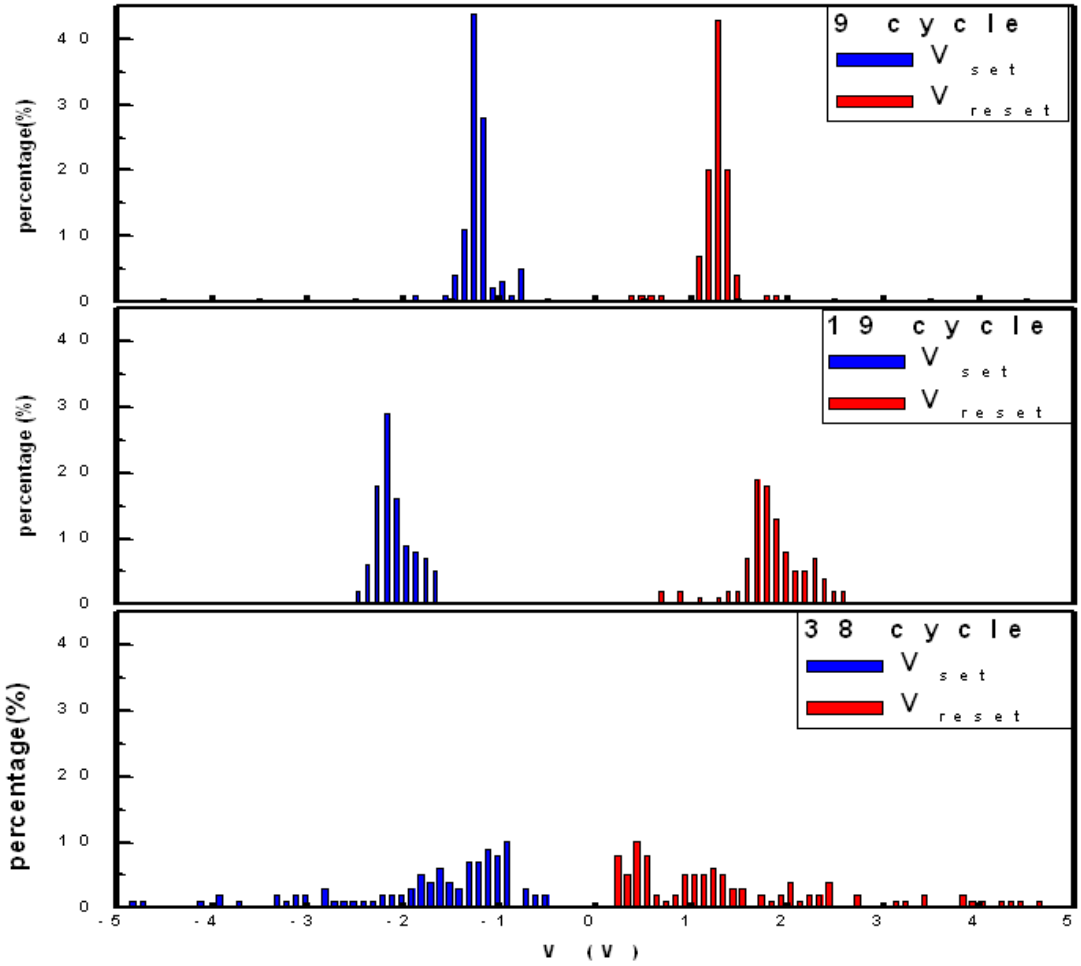

Fig. 3.3.8 Set/Reset voltage distribution of 9cycles/19-cycle/38-cycle

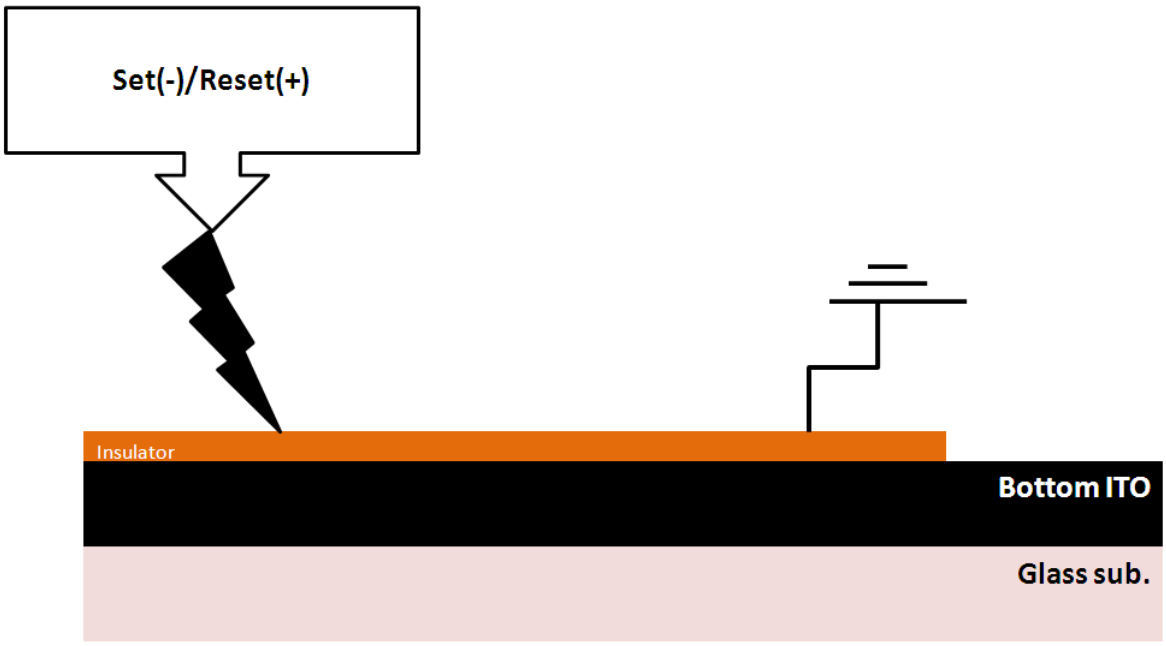

Fig. 3.3.9 The set/reset process of resistive switching localization test

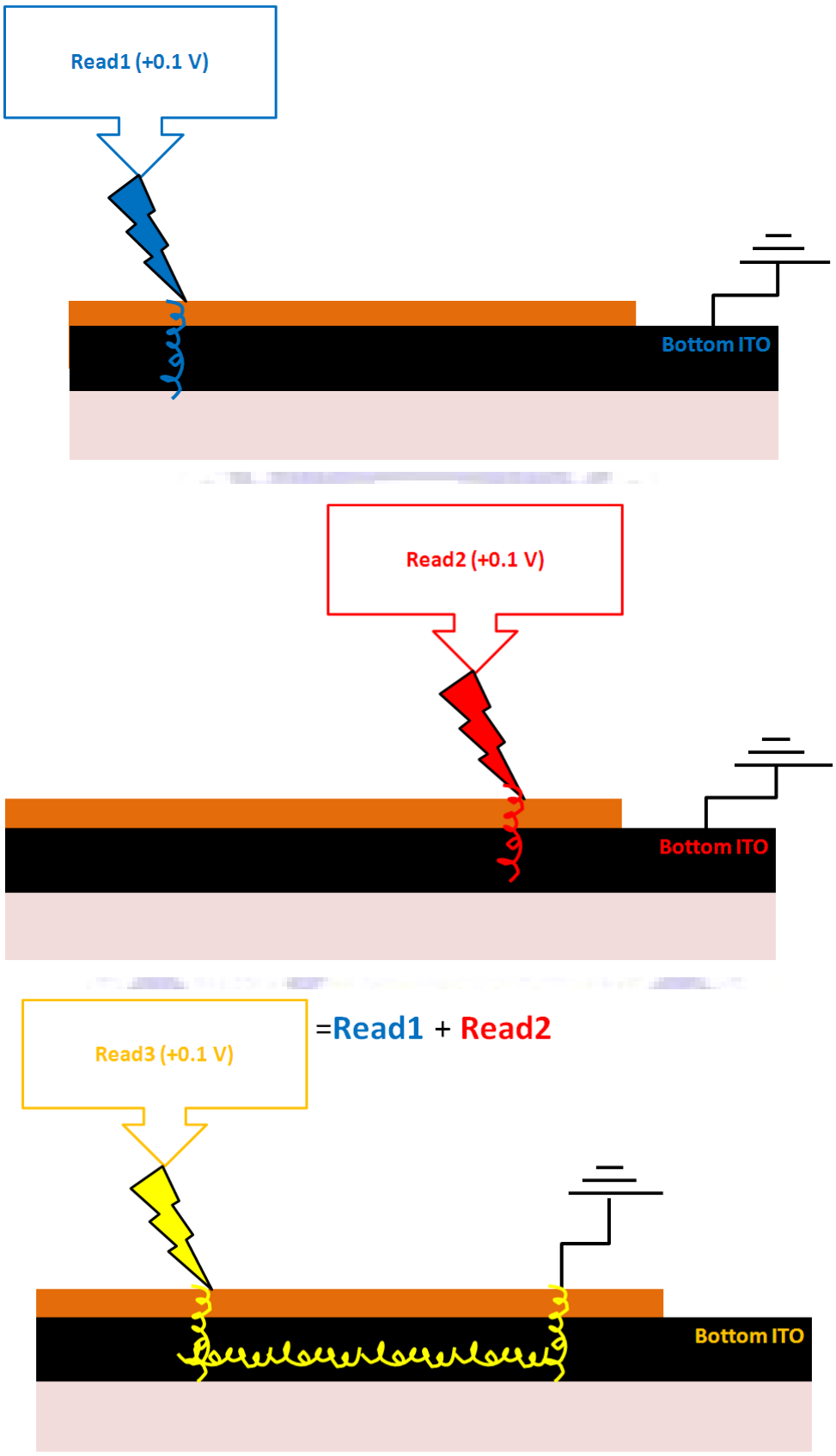

Fig. 3.3.10 READ 1, READ 2 and READ 3 in resistive switching localization test

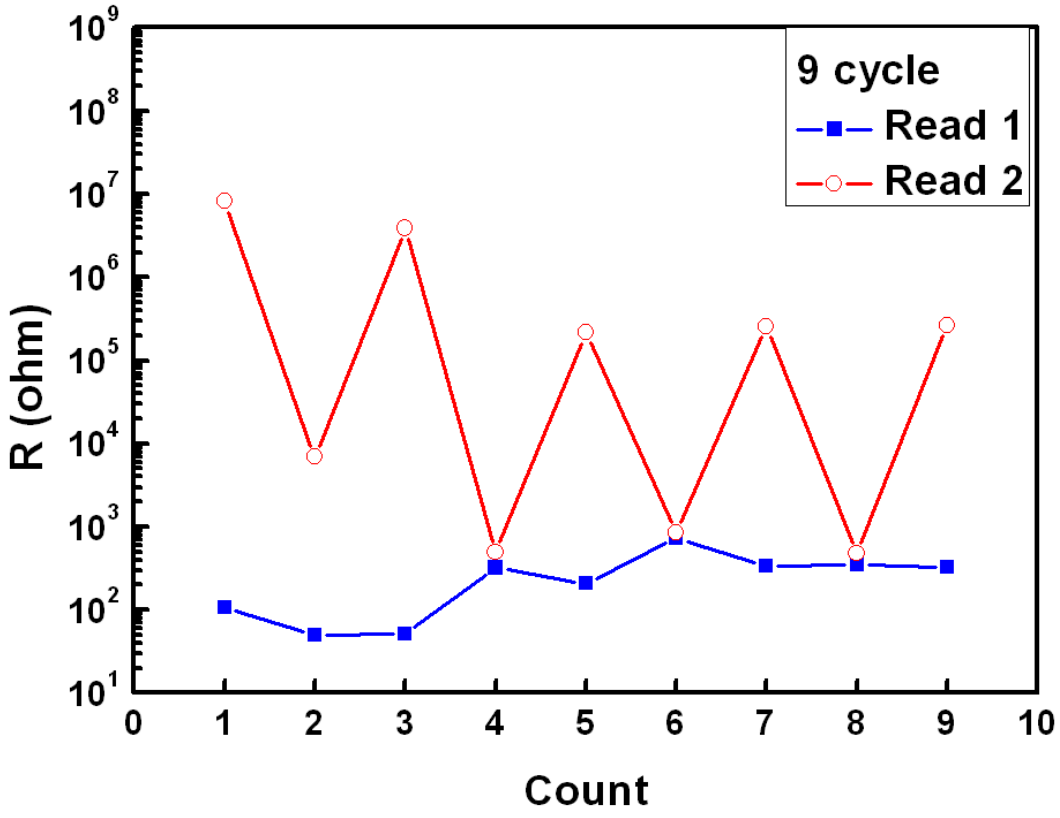

Fig. 3.3.11 READ 1/READ 2 resistances of 9-cycle by resistive switching localization test

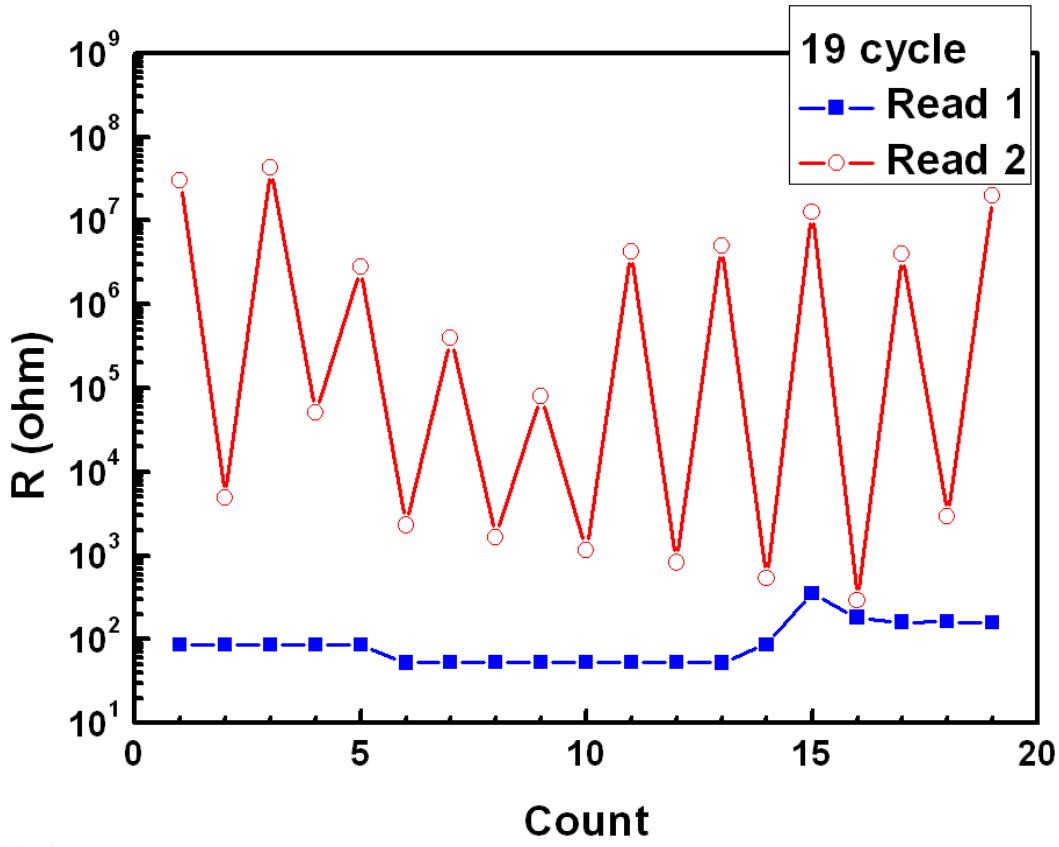

Fig. 3.3.12 READ 1/READ 2 resistances of 19-cycle by resistive switching localization test

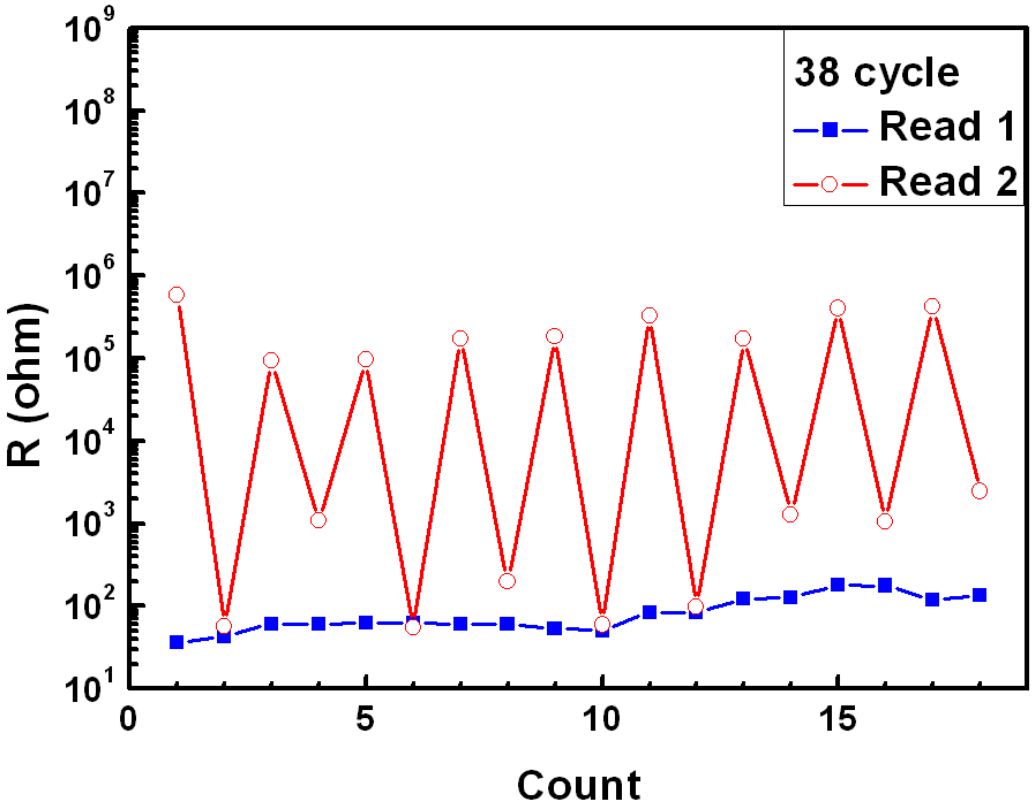

Fig. 3.3.13 READ 1/READ 2 resistances of 38-cycle by resistive switching localization test

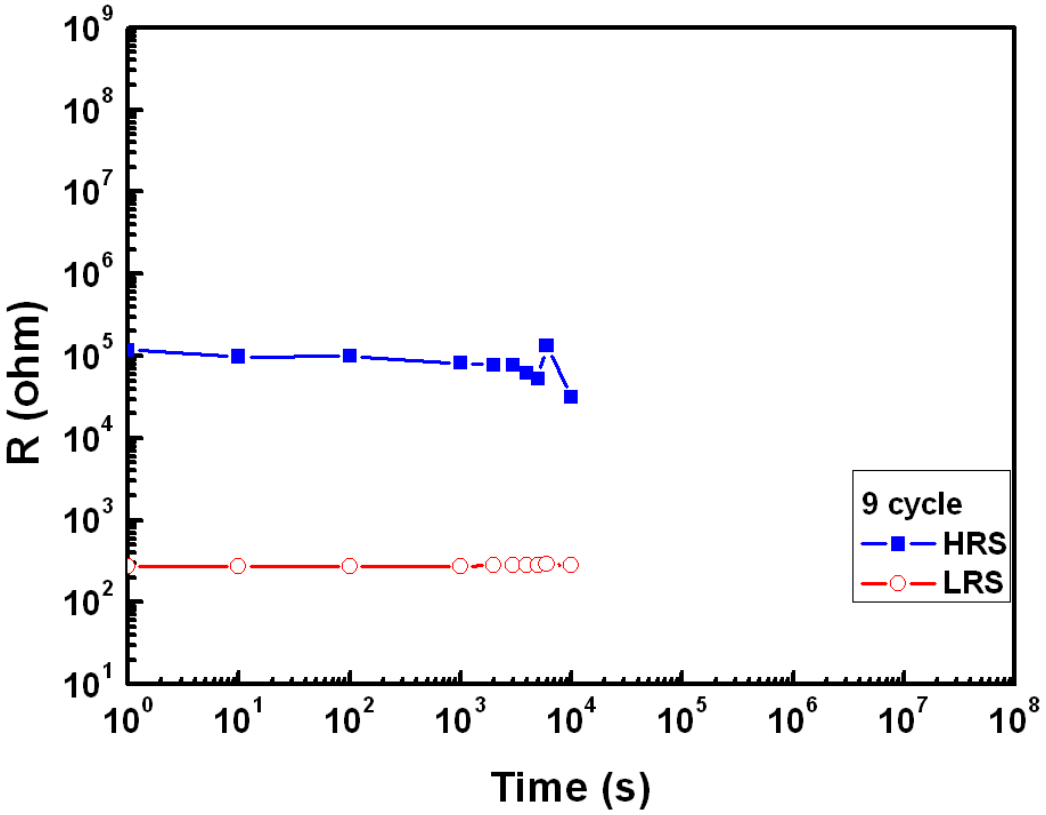

Fig. 3.3.14 Retention time experiment of 9-cycle

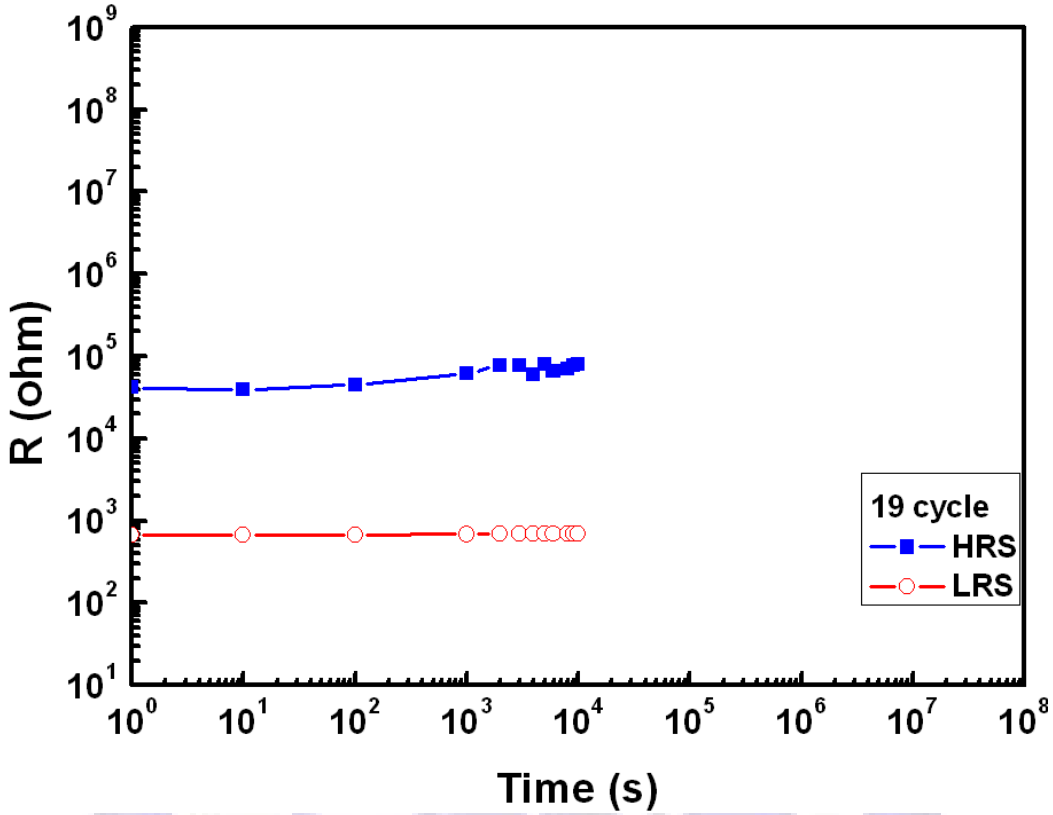

Fig. 3.3.15 Retention time experiment of 19-cycle

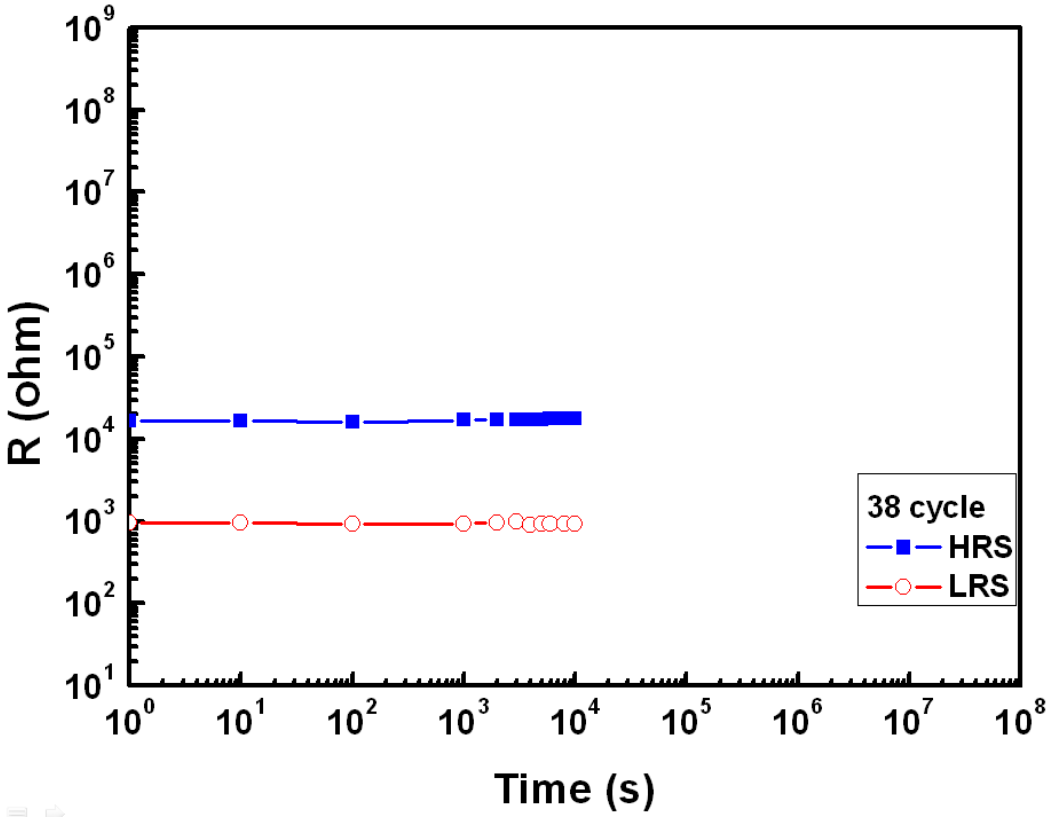

Fig. 3.3.16 Retention time experiment of 38-cycle

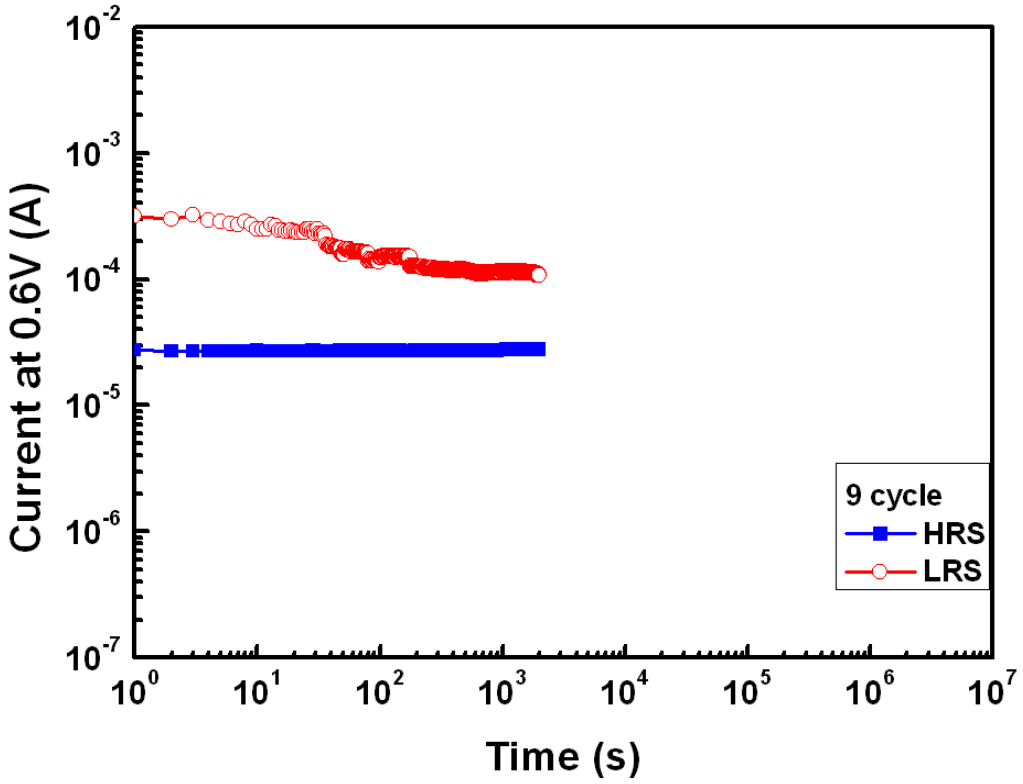

Fig. 3.3.17 Nondestructive readout experiment of 9-cycle at 0.6V

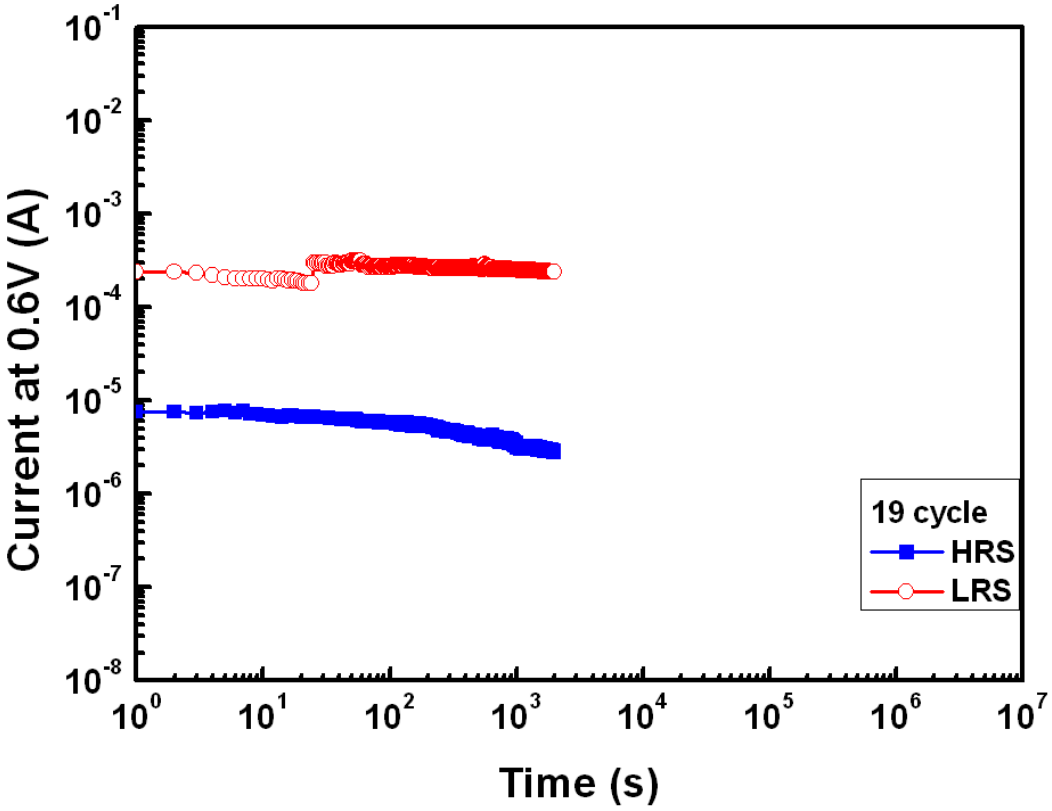

Fig. 3.3.18 Nondestructive readout experiment of 19-cycle at 0.6V

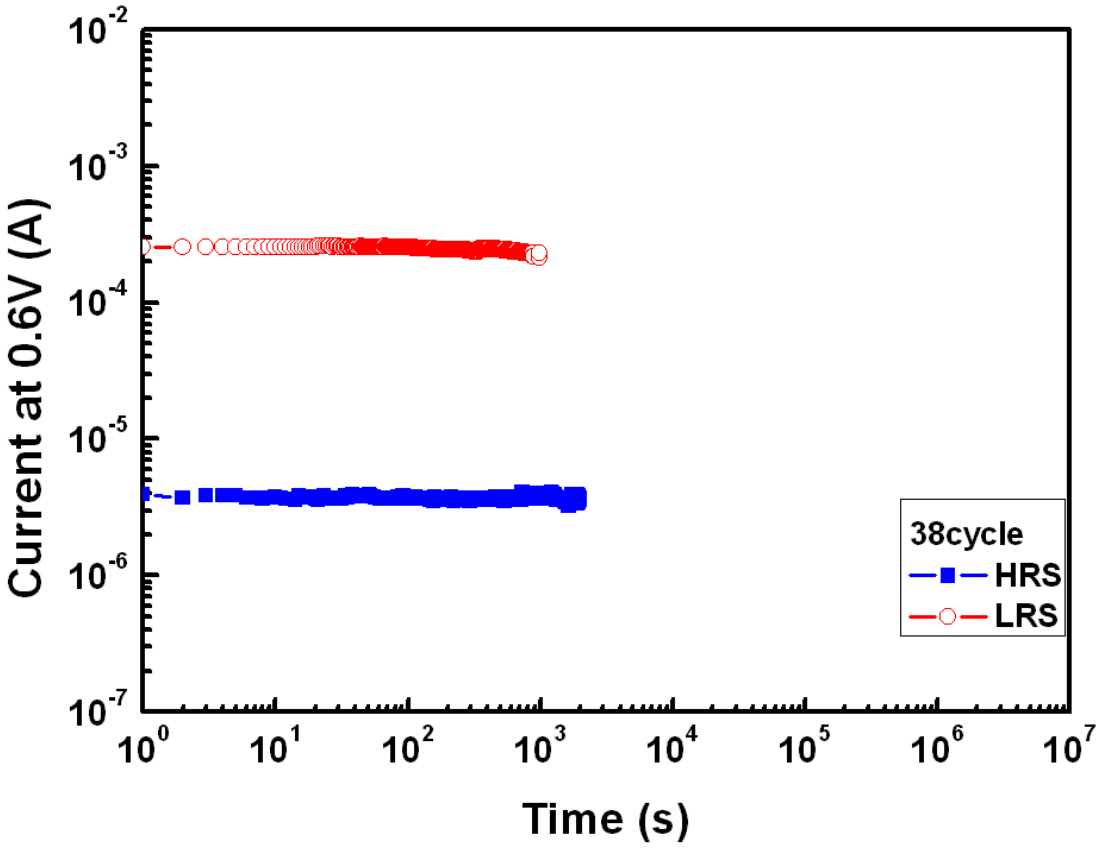

Fig. 3.3.19 Nondestructive readout experiment of 38-cycle at 0.6V

Table. 3.3.1 Comparisons of 9-cycle, 19-cycle and 38-cycle device

	9-cycle	19-cycle	38-cycle
Endurance times	1250	950	300
Set/reset voltage	-1.258 V / 1.275 V	-1.927 V / 1.867 V	-1.706 V / 1.412 V
Std. of Set/reset voltage	0.162 V / 0.193 V	0.92 V / 0.375 V	0.932 V / 1.131 V
HRS/LRS ratio	~ 1 order	~ 1 order	~ 1 order
Retention time	over 10^4s	over 10^4s	over 10^4s
Nondestructive readout at 0.6V	over 2000s	over 2000s	over 2000s
Transmittance	~80%	~80%	~80%
Increase Compliance current	LRS decrease	LRS decrease	LRS decrease
Increase stop voltage	HRS increase	HRS increase	HRS increase

3.4 Conduction Mechanism of Resistive Switching Layer

Fig. 3.4.1, Fig. 3.4.2 and Fig. 3.4.3 show the double-logarithmic plots of current-voltage curve for negative bias in set process for 9-cycle, 19-cycle and 38-cycle with the fitting results. Obviously they show $I \propto V$ at first in low voltage region and then show $I \propto V^2$ characteristics with the increase of voltage bias. This is the typical behavior of trap-controlled space-charge-limited current (SCLC) behavior. Because it happens before set process gets finished, this SCLC behavior stands for HRS carrier conduction mechanism[11][14].

And Fig. 3.4.4, Fig. 3.4.5, Fig. 3.4.6 show the double-logarithmic plots of current-voltage curve for positive bias in reset process for 9-cycle, 19-cycle and 38-cycle with the fitting results and $I \propto V$ relation can be observed. So the Ohmic conduction mechanism could stands for the carrier conduction mechanism of LRS in the resistive memory. Also the HRS fit well as SCLC here, this echo the statement in the above paragraph.

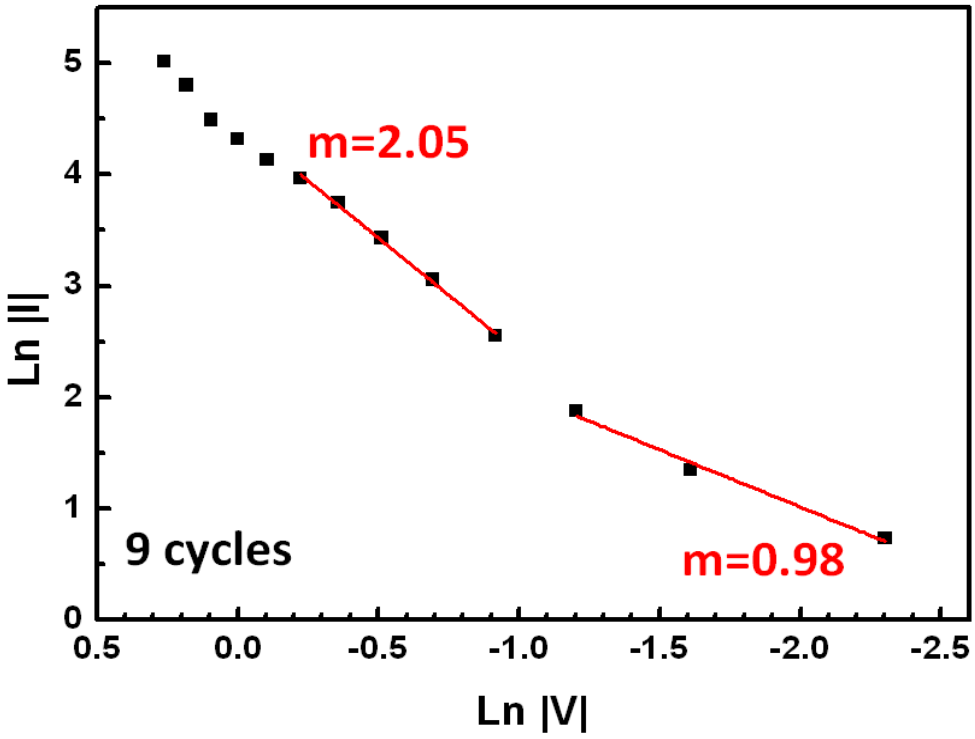

Fig. 3.4.1 SCLC conduction fitting of 9-cycle in HRS by set process

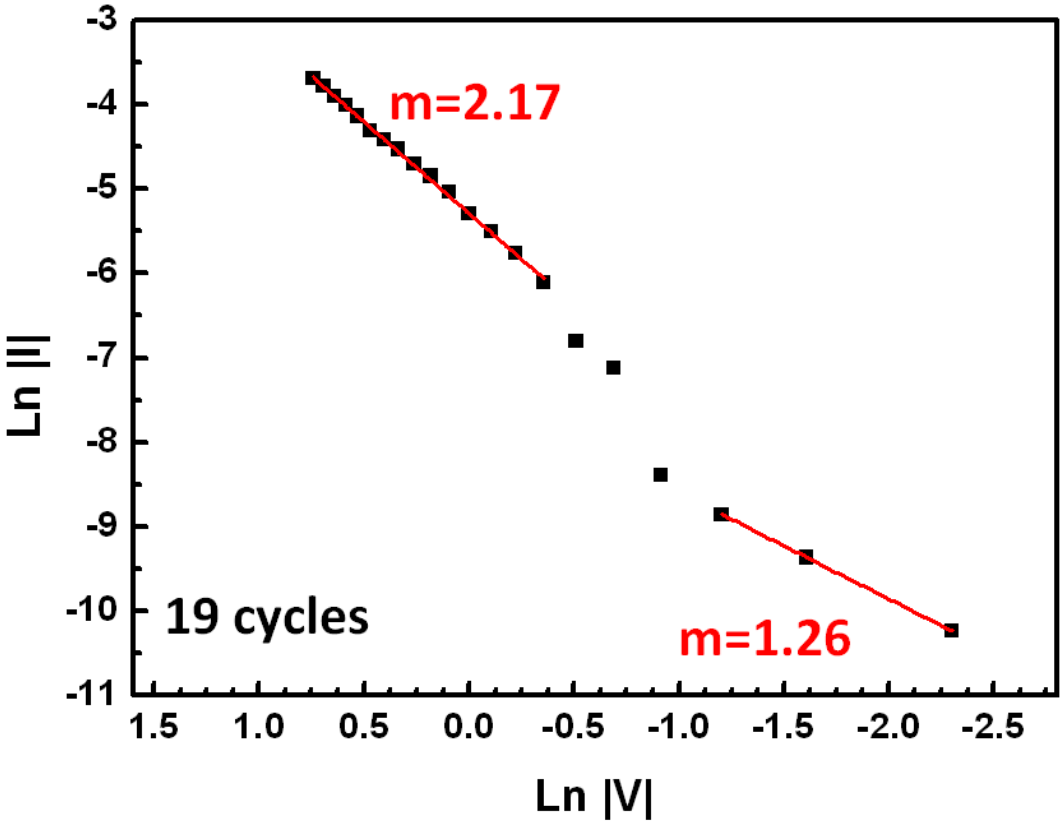

Fig. 3.4.2 SCLC conduction fitting of 19-cycle in HRS by set process

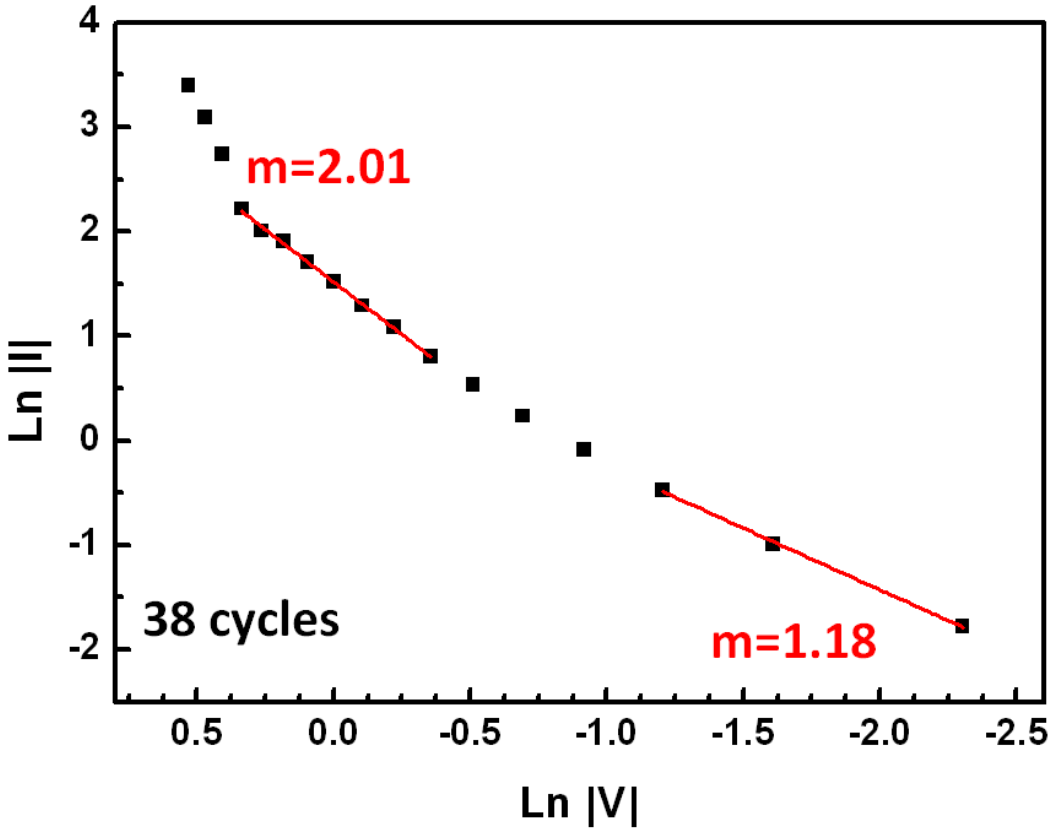

Fig. 3.4.3 SCLC conduction fitting of 38-cycle in HRS by set process

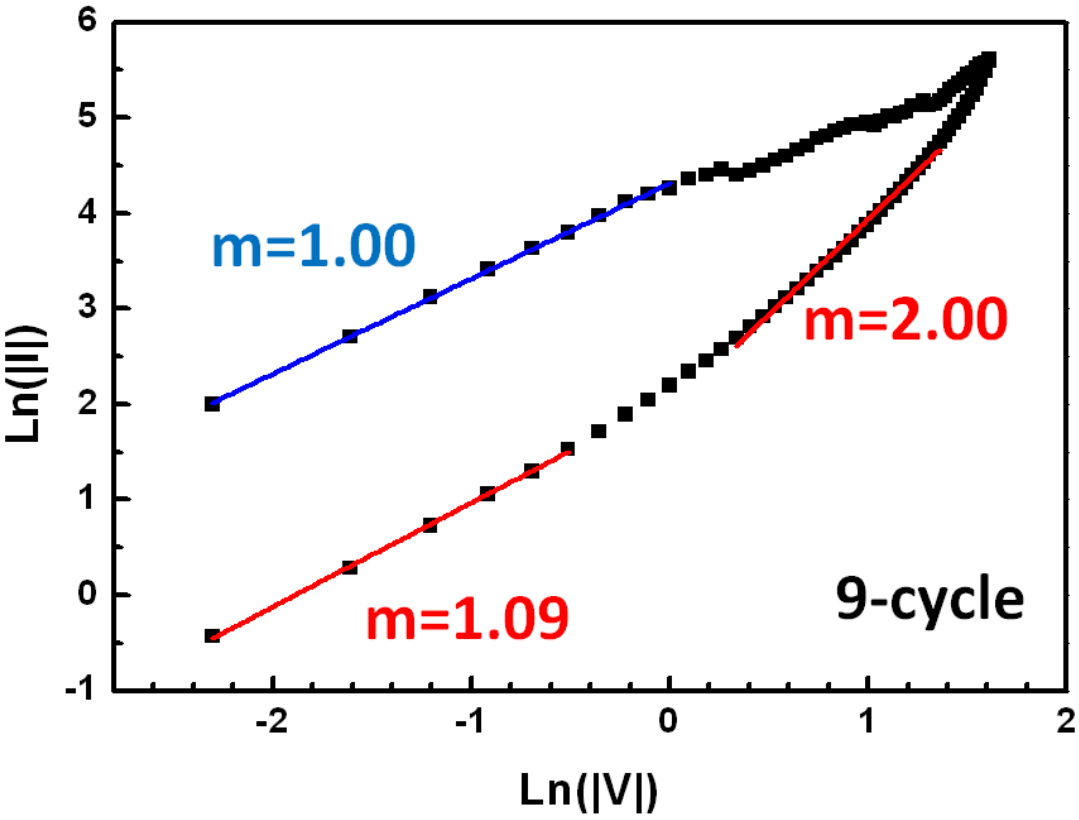

Fig. 3.4.4 Ohmic conduction fitting of 9-cycle in LRS by reset process and SCLC fitting in HRS

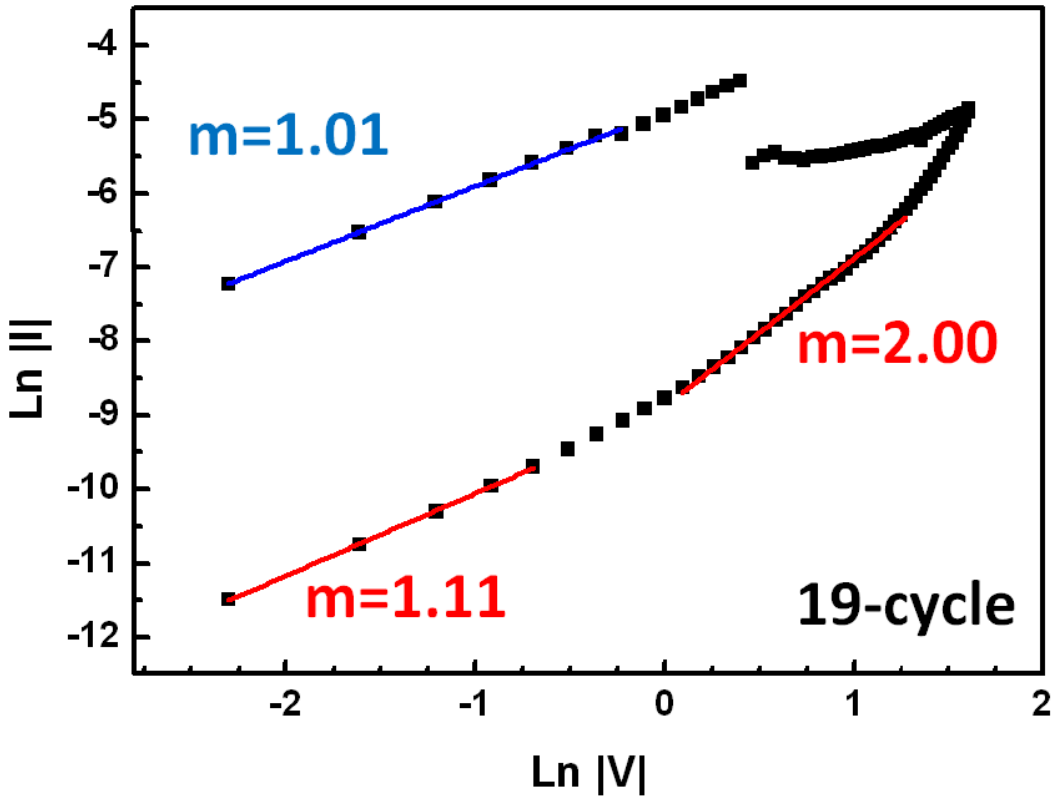

Fig. 3.4.5 Ohmic conduction fitting of 19-cycle in LRS by reset process and SCLC fitting in HRS

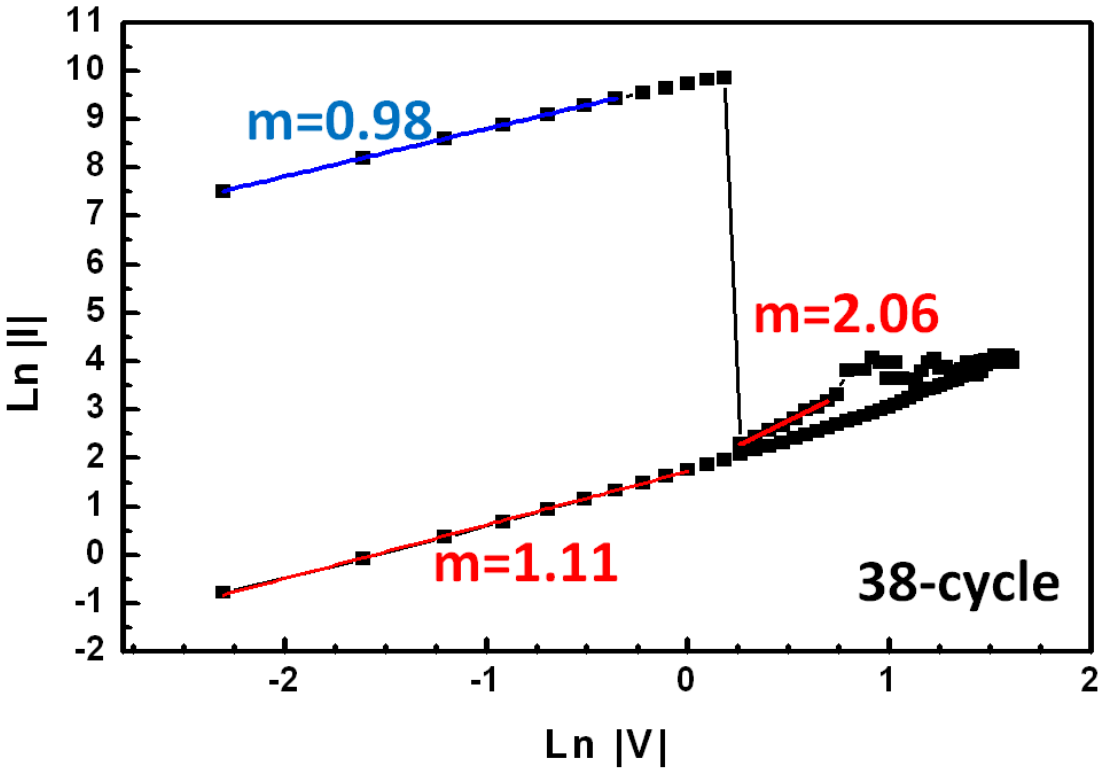

Fig. 3.4.6 Ohmic conduction fitting of 38-cycle in LRS by reset process and SCLC fitting in HRS

3.5 Resistive Switching Mechanisms for Multi-layer Resistive Switching Film

The evolution of the resistive switching hysteresis is demonstrated in previous section. Even though the basic physical resistive switching mechanisms are not clear in details, we still work on that. Overall, the memory devices fabricated by multi-layer stacking as resistive switching films could be treated as the transition-metal oxides such as HfO_2 mixed with Al_2O_3 in different level. In other words, the Al_2O_3 has different distribution in resistive switching layers. And 38-cycle device has the widest distribution of Al_2O_3. According to the research by X. F. Wang et al [29], Al atoms in HfO_2 thin films would introduce a significant amount of oxygen vacancies. And it was reported that the single Al_2O_3 films usually show random resistive switching behaviors during repeated current–voltage measurements [30].

S. Yu et al [31] confirmed that the Al diffusion into HfO_2 may be mainly responsible for the improved switching uniformity. Therefore, the oxygen vacancies in transition-metal oxides plays an important role, and it is widely believed that resistive switching is triggered by an electrical migration of anions, such as oxygen anions, which are typically described by the motion of corresponding vacancies [9]. The resistive switching from HRS to LRS is associated with the enrichment of oxygen vacancies arranged in chains under an electric field. Thus, stabilizing the generation of oxygen vacancies is the key issue for stabilizing the switching behaviors. The ab initio calculations

reveal that the oxygen vacancy formation energy in a HfO_2 supercell is effectively reduced from 6.53 to 4.09 eV in the vicinity of Al atoms [32], while it is almost unaffected at locations several atoms away from the impurities. Therefore, the chains of oxygen vacancy are easier to generate and be localized along the Al atoms, and more stable conducting filaments are expected to be formed during different switching processes, which could account for the experimentally observed the difference among these devices of switching parameters as shown in previous section.

For our devices, we have known that 38-cycle meets Al_2O_3 every 6 monolayer and 9-cycle meets Al_2O_3 every 24 monolayer as we mentioned in chapter 2. Because the chains of oxygen vacancy are easier to generate and be localized along the Al atoms, the 38-cycle device could have so many oxygen vacancies that when electron current flows in the oxide after the forming process. These oxygen vacancies generate unstable conducting filaments that electron current will spread out very easy, because there are oxygen vacancies almost everywhere. For the reason that Al_2O_3 spread out more in resistive switching layers of the 38-cycle device, it is more difficult to form stable conducting filaments. Therefore, the performance of 38-cycle could be attributed to the random formation of the conducting filaments in the resistive switching layer during each switching process. On the contrary, The-9-cycle device does not happen this way. The Al toms in 9-cycle device distribute tighter and it helps us to control the oxygen vacancies generation, so the conducting filaments are more stable after the forming process, as illustrated in Fig. 3.5.1. Accordingly, 9-cycle has better performance than 38-cycle and 19-cycle is between two parties.

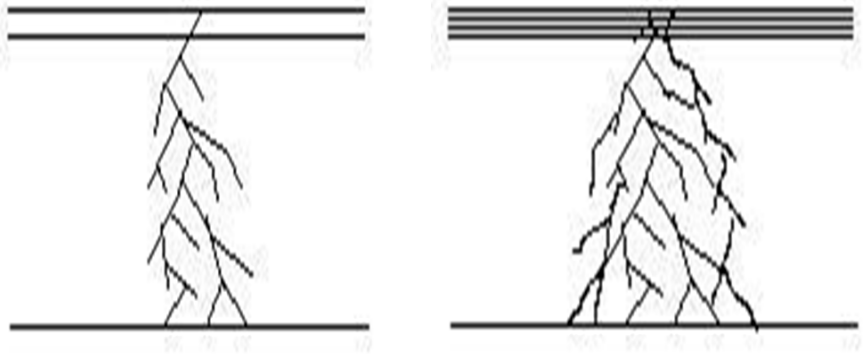

Fig. 3.5.1 Abridged general view of proposed conducting filaments distribution in 9-cycle and 38-cycle

Chapter 4
Conclusion

We first demonstrate the resistive switching characteristics of ***Transparent Resistive Random Access Memory Devices (TRRAM)*** with HfO_2/Al_2O_3 multi-layer stacking via different ALD deposition cycles as resistive switching films for 9-cycle, 19-cycle and 38-cycle devices respectively. The endurance times, average set operation voltage, standard deviation of set voltage distribution; average reset operation voltage, standard deviation of reset voltage distribution for the three devices are: 1250 times, -1.258V, 0.162V; 1.275V, 0.193V (9-cycle), 950 times, -1.927V, 0.92V; 1.867V, 0.375V (19-cycle) and 300 times, -1.706V, 0.932V; 1.412V, 1.131V (38-cycle). The-9-cycle device has the best performance than the other two (19-cycle and 38-cycle) from the electrical characteristics shown above. For the reason that Al_2O_3 spread out more in resistive switching layers of the 38-cycle device, it is more difficult to form stable conducting filaments.

In addition, our 9-cycle device with endurance times up to 1250 times, -1.258V, 1.275V set/reset operation voltage and 0.162V, 0.193V standard deviation of reset voltage distribution is relatively excellent compare to recent published transparency memory devices [10]. It was claimed that oxygen vacancy forming energy could be lower down by Al atoms which leads conducting filaments formed more stable in previous non-transparent RRAM [11]. Even though, the performances of TRRAM in this thesis are still not comparable to non-transparent RRAM. To the best of our knowledge, we first

apply this mechanism to control the conducting filament formation in TRRAM. Not only echo the previous study of the mechanism but also demonstrate TRRAM with the ever highest performance. The multi-layer stacking as the resistive switching films in TRRAM shows great potential in the future modern electronics.

Chapter 5
Future Work

Even though the performance of TRRAM in this thesis is excellent, it still does not match the criterion of NVM application today. Due to the proposed resistive switching mechanism in this thesis, changing the deposition cycles could improve the performance and changing the Al_2O_3/HfO_2 ratio may give a big help too. Furthermore, this thesis use tungsten probe as the top electrode might not be the best choice, deposition a metal between the resistive switching layer and ITO should make the performance better. Hopefully the future research could focus on these views to further make the modern TRRAM in commercial applications come true.

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