國 立 交 通 大 學
電子工程學系 電子研究所
碩 士 論 文

# 金氧半場效應電晶體在次臨界區的不匹配效應

# Mismatch of MOSFETs in Subthreshold Region

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中華民國九十九年九月

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研究生：蔡濬澤　　指導教授：陳明哲博士

國立交通大學 電子工程學系

電子研究所碩士班

## 摘要

本論文研究隨機摻雜物以及電路的不匹配效應對於臨界電壓擾動的影響與其物理模型。首先，我們量測各種不同尺寸的電晶體，並觀察到在次臨界區存在比過臨界區更大的電特性誤差。接著我們萃取出許不同的製程參數，並且建立一個有關通道摻雜濃度變異的新模型來解釋臨界電壓隨著閘極長度的縮短而上升。同時我們發現到萃取出的臨界電壓變動值會與元件面積平方根的倒數成正比，這與前人所提出的理論符合。我們也發現背閘順向偏壓可以減少製程參數變動值並可用來補償小尺寸電晶體較大的參數變動值。

接著我們特別著重在進一步探討臨界電壓的擾動特性。過程中我們觀察到在不同的汲極電壓下，所造成的臨界電壓的差異，此時因電子的能階產生變化，而會導致元件的控制力有所升降。再來我們利用 Takeuchi 的模型做比對，並考慮到隨機摻雜以及硼簇合族對於臨界電壓擾動的影響。從我們分析的結果看來，隨機摻雜對於臨界電壓擾動的影響會因為硼簇合族的原子個數上升而更加明顯。在最後，我們推導出一個在次臨界區中，與汲極電流誤差相關的新的臨界電壓擾動模型，並且此模型能經由電流誤差成功的估計臨界電壓的擾動值。

# Mismatch of MOSFETs in Subthreshold Region

Student: Chun-Tse Tsai Advisor: Dr. Ming-Jer Chen

Department of Electronics Engineering
Institute of Electronics
National Chiao Tung Universitty

## Abstract

The physical model of the threshold voltage fluctuation from random dopant, as well as current mismatch, is investigated in the thesis. At first we have extensively characterize MOSFETs with different gate widths and lengths, especially in subthreshold region of operation. We observe that the mismatch exhibits a larger mismatch while operating in subthreshold region than in above-threshold region. We extract various process parameters and hence construct a new model due to varying of channel doping to explain the threshold voltage increase with gate length decrease. The threshold voltage variations are shown to follow the inverse square rule. Simultaneously, the back-gate forward bias is found to be able to reduce the mismatch and compensate for larger variations for smaller devices.

Further, we pay more attention to the threshold voltage fluctuation, and observe that the drain voltage might cause the DIBL. Then we discuss the threshold voltage fluctuation by a Takeuchi plot, and the effect of random dopant and the boron clusters are taken into account. From our analysis, the random dopant induced threshold voltage fluctuation has more significant effect on threshold variation while the number of boron atoms per cluster increases. Finally, we also statistically derive a new model that can estimate the threshold voltage fluctuation from drain current mismatch in subthreshold region. The validity of the model is verified.

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兩年的時間，稍縱即逝，轉眼之間，畢業的時刻已經到來。回想兩年間的日子，充滿了許多的回憶，有歡笑，也有淚水。但是天下無不散的筵席，雖然充滿許多不捨，但還是必須離開，邁向新的人生階段。

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# Contents

# Figure Captions

# Chapter 1

# Introduction

## 1.1 Overview

As the feature size of integrated MOSFET's is decreasing, the mismatch has gathered great importance in recent years. In order to achieve steady lowering of the supply voltage, reducing the power consumption while holding the reliability of the device, will lead to the worsened mismatch of device characteristic. Because of this, there are some researches concerning the mismatch of MOSFETs in subthreshold region [1],[2]. Even if the lithographic dimensions and layer thicknesses are well controlled, there are still having many factors that will lead to significant variations in the threshold voltage and drive current. In general, the designers might increase the device area to improve the matching of the device. But this method is opposite to the technology trends and will cause disadvantages. If the conservative transistor geometries are used, the consequence is a waste of area, while increasing the circuit capacitances. Therefore increases the circuit power consumption and degrades the speed specifications. However, using reduced transistor geometries cab produce large deviations in the transistor electrical parameters. Therefore, a precise mismatch characterization as a function of transistor area is necessary for optimizing the trade-offs between the area, speed, power consumption, and noise and precision in circuit design. How to obtain balanced between them is worth discussing.

In this work, a large number of statistical data then yields the standard deviation and mean of the distribution for random variables. For example, we can obtain the fluctuation of the subthreshold threshold voltage, the drain-induced barrier lowering,

the subthreshold swing, and the effective channel doping concentration. It can be found that threshold voltage mismatch follows inverse square root of area. The forecast threshold voltage fluctuations have been experimentally confirmed for a wide range of fabricated and measured MOSFET's down to the nanoscale region. The performance and yield of the corresponding systems may be seriously affected in the presence of these fluctuations. Thus, we generate different mismatch models for subthreshold region in terms of the subthreshold current and threshold voltage. All the results will be revealed in the following chapters.

## 1.2 Subthreshold Region of Operation

Traditionally, the operation of MOSFETs utilizes the above-threshold region, especially the saturation region. In the saturation region, MOSFET is considered as the gate-controlled current source, and the current is essentially independent of the drain voltage. But when operated in subthreshold region, the drain voltage may have effect the current obviously. Subthreshold MOSFET conduction first attracted attention as the leakage current in several decades before [1]. The subthreshold conduction of MOSFET can also be used as the fundamental element for micropower integrated circuits in early eighties [2].

In recent years, how to reduce the power consumption becomes very important as the transistor density continuously grows in VLSI technology. Thus the subthreshold operation of MOSFET is becoming increasingly interesting because of the low power consumption. Following are the advantages of the MOSFET operating in subthreshold region:

(i) Extremely low power consumption.

(ii) Low voltage swing.

(iii) Exponential dependence of drain current on gate voltage.

In this thesis, we explore some characteristics of MOSFET operating in subthreshold region, and discuss the mismatch of parameters such as threshold voltage, drain current and drain induced barrier lowering. And we will also focus on the fluctuation of the threshold voltage.

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## 1.3 Mismatch in Subthreshold Region

It is well known that there are no two things identical in the world. This is the case for MOSFETs. Even in the same size, there are no two transistors that are identical because of the variation of manufacturing process. Pelgrom [4] pointed out that the mismatch of MOSFET is proportional to the inverse square root of gate area and are proved experimentally. Therefore, as the dimension of semiconductor device continues to be reduced with today's technology, mismatch becomes more and more important. From the research works of [5] ,we can clearly know that back-gate bias has a very huge relation with current mismatch and the back-gate forward bias can suppress it. Thus we should simultaneously take both device area and back-gate bias into account during the mismatch analysis.

As we mentioned above, one of the advantages of subthreshold region is the exponential dependence of drain current on gate voltage. But on the contrary, this relation is also to cause the large mismatch especially in the small device. Different from the dependencies following the square rule for operating in above-threshold region, the subthreshold region of operation has the exponential dependencies on process parameters. Therefore, it is expected that drain current exists larger mismatch in subthreshold region than that in the above-threshold region as shown in Fig 1.

In subthreshold region, there are many parameters to form a mismatch model,

while our parameters will be based on threshold voltage, drain-induced barrier lowering and subthreshold swing are included. In order to reduce the mismatch effectively, we can operate the device with back-gate forward bias applied. So, with the device area decreasing, the mismatch increasing can be compensated by the back-gate forward bias. This characteristic will make the subthreshold operation become more attractive.

# Chapter 2

# Parameters of Mismatch

## 2.1 Experimental Subthreshold Operation

The measurement of mismatch for identical devices was achieved in terms of the dies in wafer. In this thesis, we used the measured capacitance-voltage(C-V) curve fitting by Schred simulator to obtain the parameters due to the manufacturing processes. They are: gate oxide thickness is $1.27\,nm$, $n^+$ doping concentration is $1\times10^{20}cm^{-3}$ and the substrate doping concentration is $4\times10^{17}cm^{-3}$. All dies on wafer contain many n-channel MOS transistors with the same structure. All of them were fabricated using a $65\,nm$ CMOS process. The devices under study were n-channel MOSFETs with varying gate widths ($W = 0.13\mu m$, $0.24\mu m$, $0.6\mu m$, $1\mu m$, $10\mu m$) and mask gate lengths ($L = 0.065\mu m$, $0.1\mu m$, $0.5\mu m$, $1\mu m$).

In our measurement, the p-well-to-$n^+$-source bias $V_{BS}$ was fixed with the gate voltage sweeping from 0 V to 1.2 V in a step of 25 mV. The drain current was measured and recorded for subsequent analysis. All the procedure was performed under four different back-gate bias: -0.8 V, -0.4 V, 0 V, and 0.4 V, the same as which applied in [5]. In order to make sure of the action of the gate lateral bipolar transistors, the choice for maximum forward bias is equal to 0.4 V. The drain voltages that we chose are two values, one is fixed at 0.01 V in the subthreshold region, and the other value is 1 V for extracting the drain-induced barrier lowering.

The measurement setup contains the HP4156B and a Faraday box which is used for shielding the test wafer. All were performed in an air-conditioned room with the temperature at 298 K. We operate the n-channel MOSFET devices in the weak

inversion region. Fig. 2 displays typical measured I-V characteristics with back-gate bias parameter on a single n-channel MOSFET.

## 2.2 Extraction of Threshold Voltage

There are many electrical parameters in modeling of MOSFETs. The most important is the threshold voltage $V_{th}$. In general, threshold voltage may be understood as the gate voltage for the transition from weak inversion to strong inversion region in the MOSFET's channel. The threshold voltage can be extracted from the capacitance-voltage (C-V) curve or the drain current versus gate voltage characteristics. While the latter method is quite common to be used, there are various methods to extract threshold voltage [6] and they have been given several distinct definitions.

In order to extract the threshold voltage in subthreshold region, we choose the constant current method to extract the threshold voltage in this thesis. The constant method evaluates the threshold voltage as the value of the gate voltage, corresponding to a given constant drain current measured at drain voltage less than 100mV. A typical value [7] for this constant drain current is $\left(\frac{W_m}{L_m}\right)\times 10^{-7}(A)$, where $W_m$ and $L_m$ are the mask channel width and channel length. The threshold voltage can be determined with voltage measurement as shown in Fig. 3. From Fig. 3, we can observe there are large sample number ($\geq 2000$) used in measurement. All threshold voltages we extracted for this chosen current are from the subthreshold region. The threshold voltage values of all device sizes we obtained by constant current method are shown in Fig. 4.

## 2.3 General Mismatch Model

The mismatch parameters of a group of equally designed devices are the result of several random processes encountered during the fabrication phase of the devices. According to [3], the standard deviation $\sigma_{f(x,y)}$ of a function $f(x,y)$ with two random variables $x$ and $y$ can be expressed as

$$\sigma_{f(x,y)}^2 \cong \left(\frac{\partial f}{\partial x}\right)^2 \sigma_x^2 + \left(\frac{\partial f}{\partial y}\right)^2 \sigma_y^2 + 2\left(\frac{\partial f}{\partial x}\right)\left(\frac{\partial f}{\partial y}\right) C_{ov}(x,y) \quad (1)$$

where $\sigma_x$ and $\sigma_y$ are the variances of $x$ and $y$, respectively; and the $C_{ov}(x,y)$ is the correlation coefficient between $x$ and $y$. For three random variables $x$, $y$ and $z$, the standard deviation of the distribution can also be presented in a similar way.

We should make sure the existence of the relationship between different parameters while using this model. If there is no correlation between each other, we can get the simplest formula for the mismatch model. So, we need to confirm the parameters are independent every time we want to build a new mismatch model. But we all know that everything in the world may affect each other. In the following chapters, we will use Eq. (1) as the threshold voltage fluctuation model, and the correlation coefficient may be negligible due to the weak relation between different parameters in our mismatch model.

## 2.4 Subthreshold Swing

In order to evaluate the value subthreshold leakage current, subthreshold swing is defined as the gate voltage variation per decade of current. It is found from [8]:

$$I_d = I_0 e^{\frac{q}{kT}\frac{(V_{GS}-V_{th})}{n}} \quad (2)$$

$$S = \frac{\partial V_{GS}}{\partial \log I_d} = 2.3\frac{kT}{q}n \tag{3}$$

where $1/n$ is the fraction of $(V_{GS} - V_{th})$ that affects the source-channel barrier and the thermal voltage $\frac{kT}{q} = 0.0259V$ at room temperature. The ideal value of subthreshold swing is $60mV/decade$ for $n$ is equal to $1$. The results of subthreshold swing extracted from experimental data are shown in Fig. 5. The extracted subthreshold swing will be used in following chapter.

## 2.5 DIBL Effect on Threshold Voltage

As the advance in technology, channel length is scaling down. It is gradually important to consider short-channel effect and drain-induced barrier lowering (DIBL). Here we focus on the DIBL effect. In order to further discuss the DIBL, we derive a mismatch model of DIBL as a parameter of threshold voltage fluctuation. In this work, we use constant current method to determine the threshold voltage for large drain voltage.

DIBL is defined as the threshold-voltage shift divided by the drain voltage change. It can be expressed as:

$$DIBL = -\frac{V_{th1}(V_{d1}) - V_{th0}(V_{d0})}{V_{d1} - V_{d0}} \tag{4}$$

where $V_{th1}(V_{d1})$ is the threshold voltage extracted under $V_d = 1V$ shown in Fig. 6, and $V_{th0}(V_{d0})$ is designated as $V_{th}$ ,which is the threshold voltage extracted under $V_d = 0.01V$ as shown in Fig. 4. With these two parameters, we can obtain the DIBL. The extracted DIBL is shown in Fig. 7.

For using the DIBL we extracted to examine the mismatch model, we write Eq. (4) as another form:

$$V_{th1} = (V_{d0} - V_{d1}) \times DIBL + V_{th} \tag{5}$$

According to Eq. (1) and Eq. (5) and assume the correlation is negligible, we can derive the mismatch model:

$$\sigma^2_{V_{th1}} = \left(V_{d0} - V_{d1}\right)^2 \times \sigma^2_{DIBL} + \sigma^2_{V_{th}} \quad (6)$$

where $V_{d0} - V_{d1} = -0.99V$ in our case. Similarly with the threshold voltage standard deviation, the DIBL standard deviation also has inverse relation of the device size as shown in Fig. 8. Fig. 9 demonstrates the experimental data and the calculated results of the model, where we can observe that the results are as anticipating as we can infer. Thus we can write the standard deviation of DIBL as a function of threshold voltage for different drain voltages.

# Chapter 3

# Random Threshold Voltage Fluctuation

## 3.1 Channel Doping Concentration

Along with the advanced technology, device size is more and more small. Channel doping concentration becomes an essential parameter of MOSFET. From threshold voltage we display before, we observed when the channel length gets shorter, the threshold voltage might become larger. Contrary to the short channel effect, it is widely known that heavy channel doping may increase the threshold voltage. Consequently, we consider that the halo doping (near the source/drain and under the inversion channel) will affect the effective channel doping concentration $N_{A\_eff}$ to bring about this phenomenon. The schematic drawing of halo doping device is shown in Fig. 10.

In order to find the effective channel doping concentration of our experimental data, we start at finding the flat band voltage $V_{FB}$. The flat band voltage is defined as the gate voltage at zero band bending. From semiconductor physics studied, we understand that the existence of many kinds of traps may affect the flat band voltage, such as oxide trap, interface trap and fixed oxide charge. It is difficult for us to quantify each of them. Because of this, we attempted to use the threshold voltage we have extracted from constant current method to obtain the flat band voltage including the trap effect.

First, the formula of threshold voltage can be derived as:

$$V_{th} = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_f - V_{BS}} \tag{7}$$

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{8}$$

$$\gamma = \frac{t_{ox}\sqrt{2q\varepsilon_{si}N_A}}{\varepsilon_{ox}} \tag{9}$$

where $\phi_f$ is the Fermi level, $N_A$ is the effective well doping concentration, $n_i$ is the intrinsic concentration of silicon, $t_{ox}$ is the oxide thickness, and $\varepsilon_{si}$ and $\varepsilon_{ox}$ are the silicon and oxide permittivities, respectively. Here we assume that flat band voltage does not change with gate length, and the channel doping concentration of long channel effect by halo doping can be negligible. Thus we can use the extracted threshold voltage from five different gate widths ($W = 0.13\mu m$, $0.24\mu m$, $0.6\mu m$, $1\mu m$, $10\mu m$) at longest gate length ($L = 1\mu m$) and $N_A = 4\times10^{17} cm^{-3}$ and according to Eq. (7) to obtain five different flat band voltages with corresponding gate widths. The extraction result is shown in Fig. 11.

Next, with the flat band voltage we have extracted and the threshold voltage of other gate lengths ( $L = 0.065\mu m$, $0.1\mu m$, $0.5\mu m$), similarly, according to Eq. (7), we can obtain the effective channel doping concentration $N_{A\_eff}$ of different gate lengths as shown in Fig. 12. In order to confirm if $N_{A\_eff}$ we extracted is reasonable, we substituted them into the Eq. (7) for different back-gate bias to derive the corresponding threshold voltage, and then compared the results with the experimental data. As a result, we find that they almost match the experimental data as shown in Fig. 13.

Although these effective channel doping concentrations we extracted may be not the real doping concentration of the MOSFETs, but it can reveal the characteristics of channel doping concentration. Thus we can use them for the undertaken study as an

equivalent channel doping concentration of our devices.

## 3.2 Random Threshold Voltage Fluctuation

One of the important things of operating the MOSFETs is the applied voltage. The applied voltage is being steadily lowered to reduce the power consumption and keep the reliability. There are many factors that may affect threshold voltage fluctuation, such as random dopant, oxide thickness, oxide interface roughness and polysilicon gate enhancement [9]-[13]. In this chapter, first, we start at models from Takeuchi's paper [14],[15], and repeat some work of threshold voltage fluctuation. Next, we use a model of random dopant threshold voltage fluctuation, to evaluate the threshold voltage fluctuation induced by random dopants. Finally, we eliminate the random doping effect of threshold voltage fluctuation to find others effect of threshold voltage fluctuation and give a discussion.

The vertical electric field in this model is a function of depth $x$ in the channel region. If there is an extra charge sheet $\Delta Q$ added within the channel depletion layer, we assume the voltage drop between the surface and the depletion region edge ($x = W_{DEP}$) is constant. Thus the relationship between threshold voltage charge sheet can be shown as a function of charge sheet $\Delta Q$ and depth $x$:

$$\Delta V_{th} = \frac{\Delta Q}{C_{ox}}\left(1 - \frac{x}{W_{DEP}}\right) \tag{10}$$

And if we further assume that the impurity number distribution in the charge sheet volume is of binomial type, thus the standard deviation of $\Delta Q$ will be:

$$\Delta Q = q\sqrt{\frac{N_{SUB}(x)\Delta x}{LW}} \tag{11}$$

where the $N_{SUB}(x)$ is the doping concentration and $L$ is the effective channel length. Therefore, the standard deviation of the threshold voltage can be obtained by

integrating the contributions of the charge sheets from $x = 0$ to $x = W_{DEP}$, leading to a result:

$$\sigma_{V_{th}} = \frac{q}{C_{ox}} \sqrt{\frac{N_{EFF} W_{DEP}}{3WL}} \tag{12}$$

where $N_{EFF}$ is a weighted average of $N_{SUB}(x)$ defined as

$$N_{EFF} = 3\int_0^{W_{DEP}} N_{SUB}(x)(1 - \frac{x}{W_{DEP}})^2 \frac{dx}{W_{DEP}} \tag{13}$$

If we assume the $N_{SUB}(x)$ is constant, from Eq. (13) we can derive $N_{EFF} = N_{SUB}$.

Eq. (12) can be slightly modified into:

$$\sigma_{V_{th}} = \frac{q}{C_{ox}} \sqrt{\frac{N_{SUB} W_{DEP}}{3WL}} \tag{14}$$

Threshold voltage formula is written as follows:

$$V_{th} = V_{FB} + 2\phi_f + \frac{qN_{SUB} W_{DEP}}{C_{ox}} \tag{15}$$

Substituting the Eq. (15) to Eq. (14), we can derive:

$$\sigma_{Vth} = \sqrt{\frac{q}{3\varepsilon_{ox}}} \sqrt{\frac{t_{ox}(V_{th} - V_{FB} - 2\phi_f)}{WL}} \tag{16}$$

In this thesis, threshold voltage was obtained from constant current method as mentioned above. As the flat band voltage and effective channel doping concentration we have mentioned above, our results of this part is shown in Fig. 14. Since the fluctuation model has offered an effective way to compare and analyze the different kinds of transistors manufactured by different processes. The substrate bias dependence of threshold voltage standard deviation also can be properly normalized base on this fluctuation model. From Fig. 14, we can observe that the effect of the back-gate bias according to the fluctuation model has the same trend in agreement with our experimental data.

Next, we discuss the well known fact that the $V_{th}$ standard deviation commonly

satisfied the relationship:

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}} \tag{17}$$

where $A_{V_{th}}$ is the proportionality constant. The $A_{V_{th}}$ changes due to the different oxide thickness and threshold voltage, the results of this model are shown in Fig. 15. From Fig. 15, we can observe obviously that the $V_{th}$ standard deviation is being proportional to the inverse square root of the device area, and the mismatch became severe with back-gate reverse bias. The result agrees well with the arguments as mentioned above.

## 3.3 Random Dopant Induced Threshold Voltage Fluctuation

In above statements, we assume that impurity in the channel region has most tremendous influence on threshold voltage fluctuation. As MOSFET scales down to the deep submicrometer feature size, the intrinsic spreading in various parameters also is a significant factor in the matching performance of the identically transistors. In fact, the random dopant also plays an important role in the threshold voltage fluctuation model.

In this work, we consider the effect of random dopant on the threshold voltage fluctuation of the MOSFETs. The depletion region in the MOSFET increased while the reverse substrate bias decreases in magnitude. Thus there exist extra dopants that are now included in the depletion region and may induce the threshold voltage fluctuation. This means that the mismatch in the body effect factor depends on back-gate bias. But what we focus on is the threshold voltage fluctuation attributed to a variation in the doping concentration, thus we can establish a threshold voltage fluctuation model of channel doping to estimate the random dopant effect on the threshold voltage fluctuation.

In order to derive the channel doping fluctuation model, we start from Eq. (7), and with Eq. (9) and Eq. (15), we can derive:

$$W_{DEP} = \left( \frac{2\varepsilon_{si}(2\phi_f - V_{BS})}{qN_A} \right)^{1/2} \tag{18}$$

From Eq. (1), assuming the correlation coefficient of channel doping and other parameters can be ignored, we can obtain:

$$\sigma_{V_{th}}^2 = \sigma_{Vth,dopant}^2 + \sigma_{Vth,others}^2 \tag{19}$$

where $\sigma_{Vth,others}$ are the other unknown parameters that influence the threshold voltage fluctuation. We substituting Eq. (18) to Eq. (14) , we can derive a threshold voltage fluctuation model of channel doping concentration [16]:

$$\sigma_{Vth,dopant}^2 = \frac{\sqrt{2q^3\varepsilon_{si}\left(2\phi_f - V_{BS}\right)N_A}}{3C_{ox}^2 WL} \tag{20}$$

Here we still using the effective channel doping concentration extracted above. Fig.16 shows the results of calculated $\sigma_{Vth,dopant}$ by the model. By using Eq. (17), we can obtain the threshold voltage fluctuation effect due to the other unknown parameters as shown in Fig. 17. Based on these results, we can observe that the channel doping induced threshold voltage fluctuation is not obviously compared with other parameters, especially for the large device. But from the threshold voltage fluctuation model of channel doping concentration, we observe that when device size become more and more small with the technology advancement, channel doping concentration may become a more important factor of threshold voltage fluctuation.

In order to further discuss the effect of the random dopant, we take the boron clustering effect into consider [17],[18]. In this case, the charge of carrier $q$ is replaced with $nq$ and $N_A$ is replaced with $N_A/n$. The threshold voltage is not change by these replacements as in the following:

$$V_{th} = V_{FB} + 2\phi_f + \frac{(nq)(N_{SUB}/n)W_{DEP}}{C_{ox}} = V_{FB} + 2\phi_f + \frac{qN_{SUB}W_{DEP}}{C_{ox}} \quad (21)$$

Then we can modify Eq. (20) into the form related with the number of boron atoms per cluster:

$$\sigma^2_{Vth,dopant} = \frac{n\sqrt{2q^3\varepsilon_{si}\left(2\phi_f - V_{BS}\right)N_A}}{3C^2_{ox}WL} \quad (22)$$

Fig. 18 shows the $\sigma_{Vth,dopant}$ of different number of boron atoms per cluster $n = 1 \sim 6$ at zero back-gate bias. We can observe obviously that the boron clusters influences the $\sigma_{Vth,dopant}$ very significantly. When taking the boron clustering effect into consider, the random dopant effect on threshold voltage fluctuation become more obviously. Fig.19 shows the $\sigma_{Vth,others}$ of different number of boron atoms per cluster $n = 1 \sim 6$. Therefore, the number of boron atoms per cluster must be taken into account while examining the threshold voltage fluctuation in the future.

# Chapter 4

# Mismatch Model Analysis and Modeling

## 4.1 Current Mismatch Model

It is widely known that the most important two parameters of mismatch are drain current and threshold voltage. Here we will connect them and derive a mismatch model in the following works. First, we define the current standard deviation as $\sigma_{Id}$ and threshold voltage standard deviation as $\sigma_{Vth}$. We use statistics tool to calculate the mean and standard deviation of our experiment data. In the subthreshold region, the threshold voltage $V_{th}$ affects the drain current $I_d$ through the following expression [5],[8]:

$$I_d = Ae^{-\frac{q}{kT}\frac{V_{th}}{n}} \tag{23}$$

Then we differentiate Eq. (23) and get:

$$dI_d = -\frac{q}{kTn} Ae^{-\frac{q}{kT}\frac{V_{th}}{n}} dV_{th} \tag{24}$$

The slope $n$ can be written as:

$$n = 1 + \frac{C_B'}{C_{ox}'} = 1 + \frac{\gamma}{2\sqrt{2\phi_f - V_{BS}}} \tag{25}$$

$$C_B' = \left( \frac{\varepsilon_{si} q N_A}{2(2\phi_f - V_{BS})} \right)^{1/2} \tag{26}$$

and from Eq. (3), we can find $S = 2.3\frac{kT}{q}n$,

where $A$ is a constant, $C_B'$ is the junction capacitance per unit area , $C_{ox}'$ is the oxide capacitance per unit area and $S$ is the subthreshold swing. We choose thermal voltage $kT/q = 0.0259(V)$ at room temperature. Because the standard

deviation is always the positive value, Eq. (24) can be applied with the absolute value at both side. Since we can easily combine above-mentioned functions and build up a mismatch model of current and threshold voltage [19]:

$$n \cong \frac{S\ (V/decade)}{0.06\ (V/decade)} \tag{27}$$

$$\frac{\sigma_{I_d}}{I_d} \cong \frac{q}{kT}\frac{\sigma_{V_{th}}}{n} \tag{28}$$

In previous works, we have extracted the subthreshold swing and standard deviation of threshold voltage and drain current. Now we take them into this model, assuming that the subthreshold swing mismatch is negligible here. The following are the results of using our experiment to fit this model. Fig. 20 shows the result of our experimental data at zero back-gate bias condition by using this model. From the correlation, it can be found that the difference between the model and experimentally extracted values are quite small.

## 4.2 Discussion of Current Mismatch Model

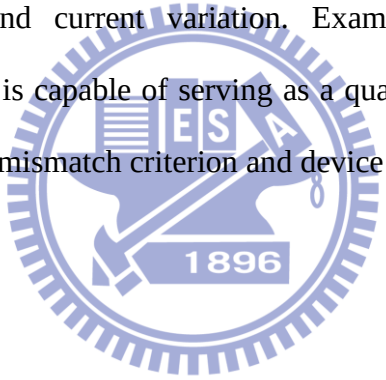
To make further use of this model, we observed that we can easily estimate the standard deviation of threshold voltage with only the standard deviation of drain current and subthreshold swing, and the result is worth being trusted. Eq. (28) can be rewritten as follows:

$$\sigma_{V_{th}} \cong \frac{nkT}{q}\frac{\sigma_{I_d}}{I_d} \tag{29}$$

Fig. 21 shows the comparison between the calculated result and the experiment, thus confirming the validity of model. While this mismatch model has great estimation of the fluctuation, there are two points that should be mentioned. First, this model is just available in subthreshold region because it was derived from the subthreshold current

formula. Second, the applied current mismatch for different gate voltages might affect the slope of the fit-line because the current mismatch changes with applied gate voltage. Thus, besides the two points we mentioned-above, we can utilize this model with ease.

We have extensively measured the n-type device over a small back-gate bias range having different drawn gate widths and lengths. Experiment has exhibited that the significant drain current mismatch occurs in weak inversion, especially for small size devices. An analytic mismatch model has been developed and successfully reproduced the extensively measured data. With the aid of this model, threshold voltage mismatch can be expressed as a function of the process parameters, namely the subthreshold swing and current variation. Examples have been given to demonstrate that the model is capable of serving as a quantitative design tool for the optimal design between the mismatch criterion and device size.



# Chapter 5

# Conclusion

At first, we have addressed the advantages and disadvantages of operating MOSFETs in the subthreshold region, along with the discussions from different aspects. Due to many related researches of mismatch, we have found that there are two important characteristics of mismatch. One is process parameters that might followed the inverse square root of the device area and the other is the back-gate forward bias that might reduce the mismatch of the device.

Next, we have discussed the extraction of mismatch parameters. We have obtained several important parameters including the threshold voltage, the drain-induced barrier lowering, and the subthreshold swing. We have constructed a new model to explain that the threshold voltage increases with the channel length decrease and have confirmed it by experiment. After these parameters have been extracted, we have further established the mismatch model. We have reproduced with this model by the threshold voltage data and have made further discussions about the influence of the random dopant and boron clusters. Finally, we have derived a useful current mismatch model which can easily estimate the threshold voltage fluctuation from the drain current mismatch in subthreshold region. The schematic flowchart to summarize the procedure of our works is shown in Fig. 22.

Mismatch is indeed more and more important today, and our work is just a little step in this direction. It is expected that our studies and the models might be helpful for the future research.

# References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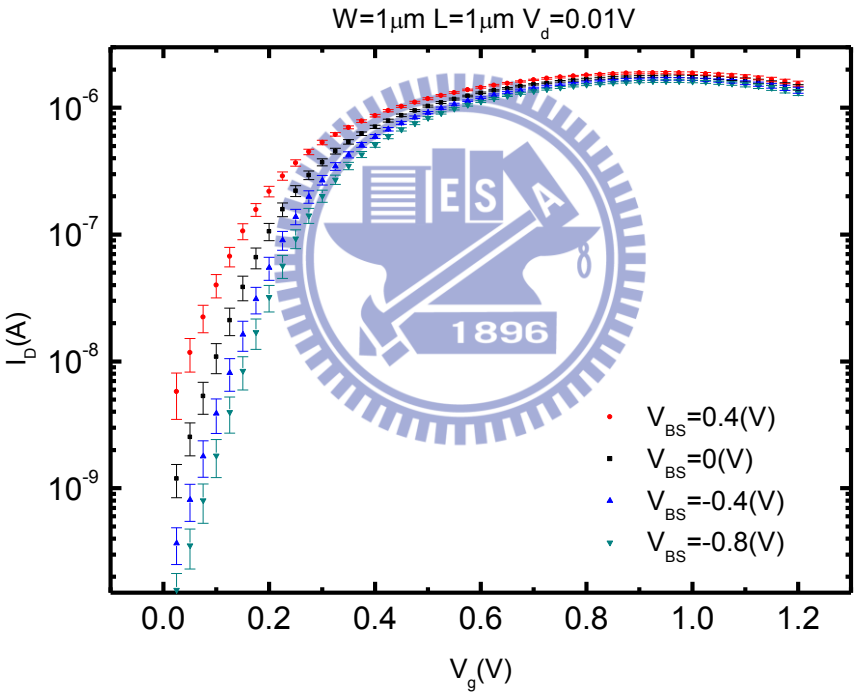


Fig.1 The measurement $I_D$ mean and standard deviation in both subthreshold region and above-threshold region with different back-gate biases.

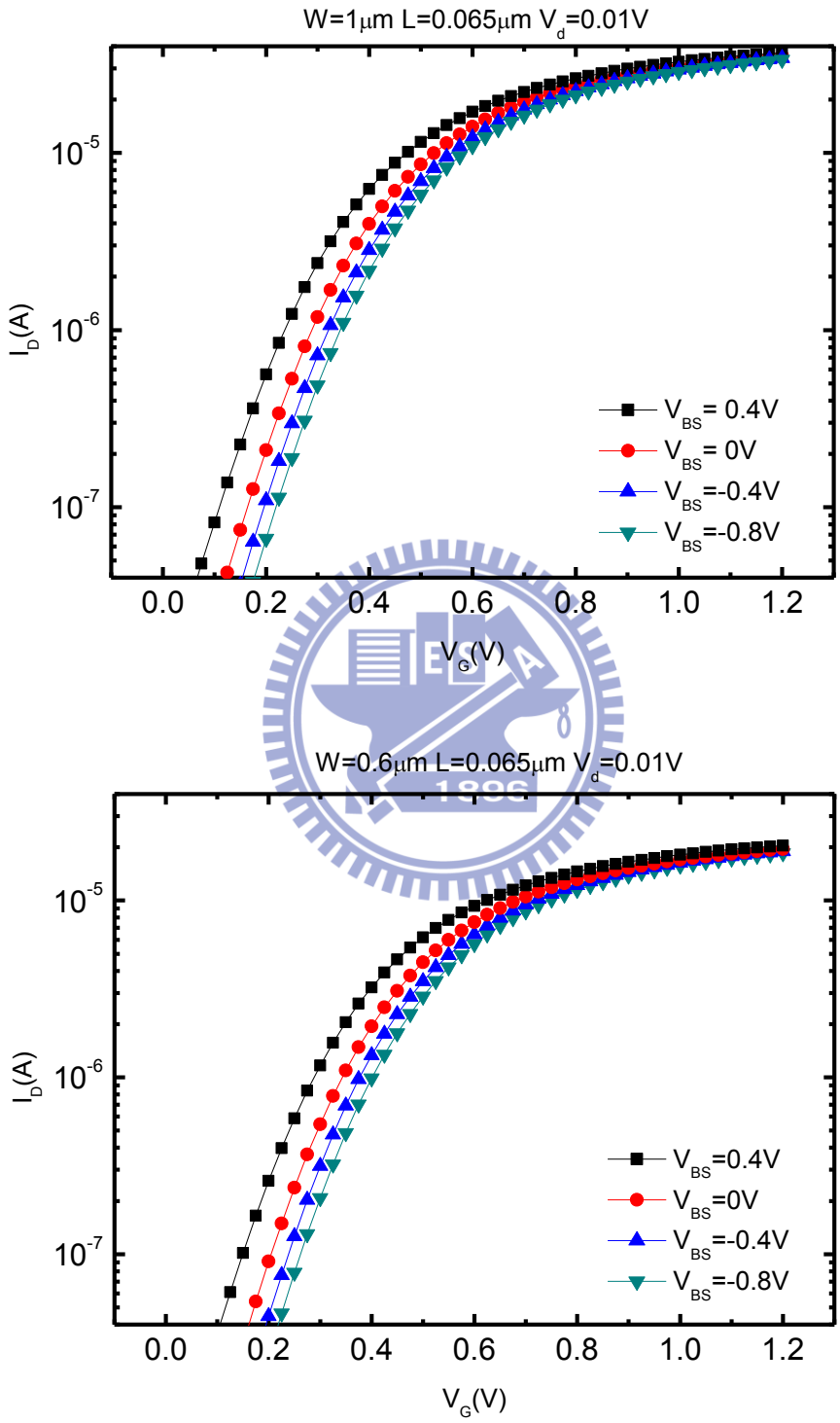


Fig. 2 The measured drain current versus gate voltage characteristics with different back-gate biases.

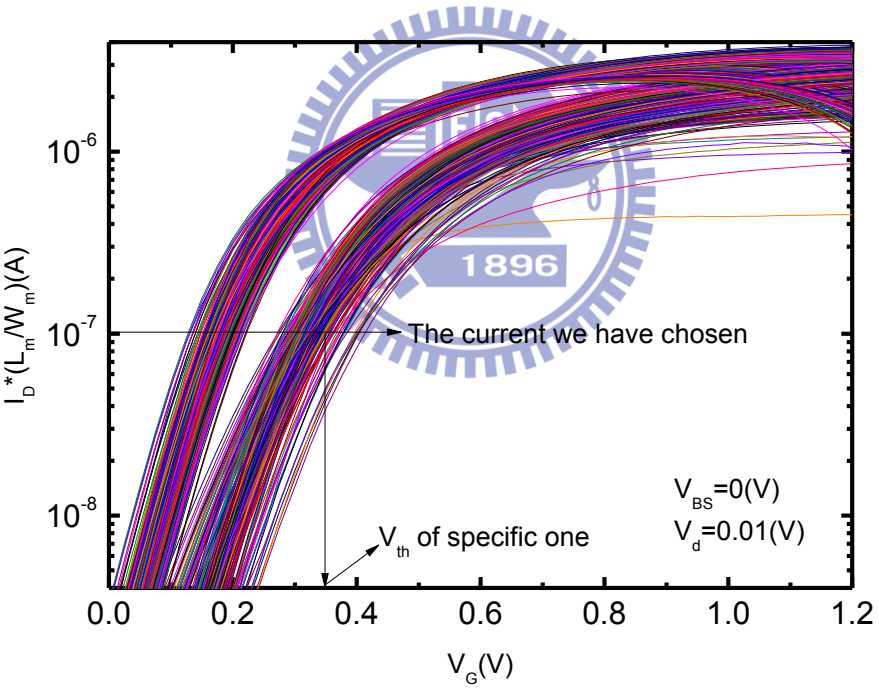


Fig. 3 Using constant current method to determine the threshold voltage in subthreshold region.

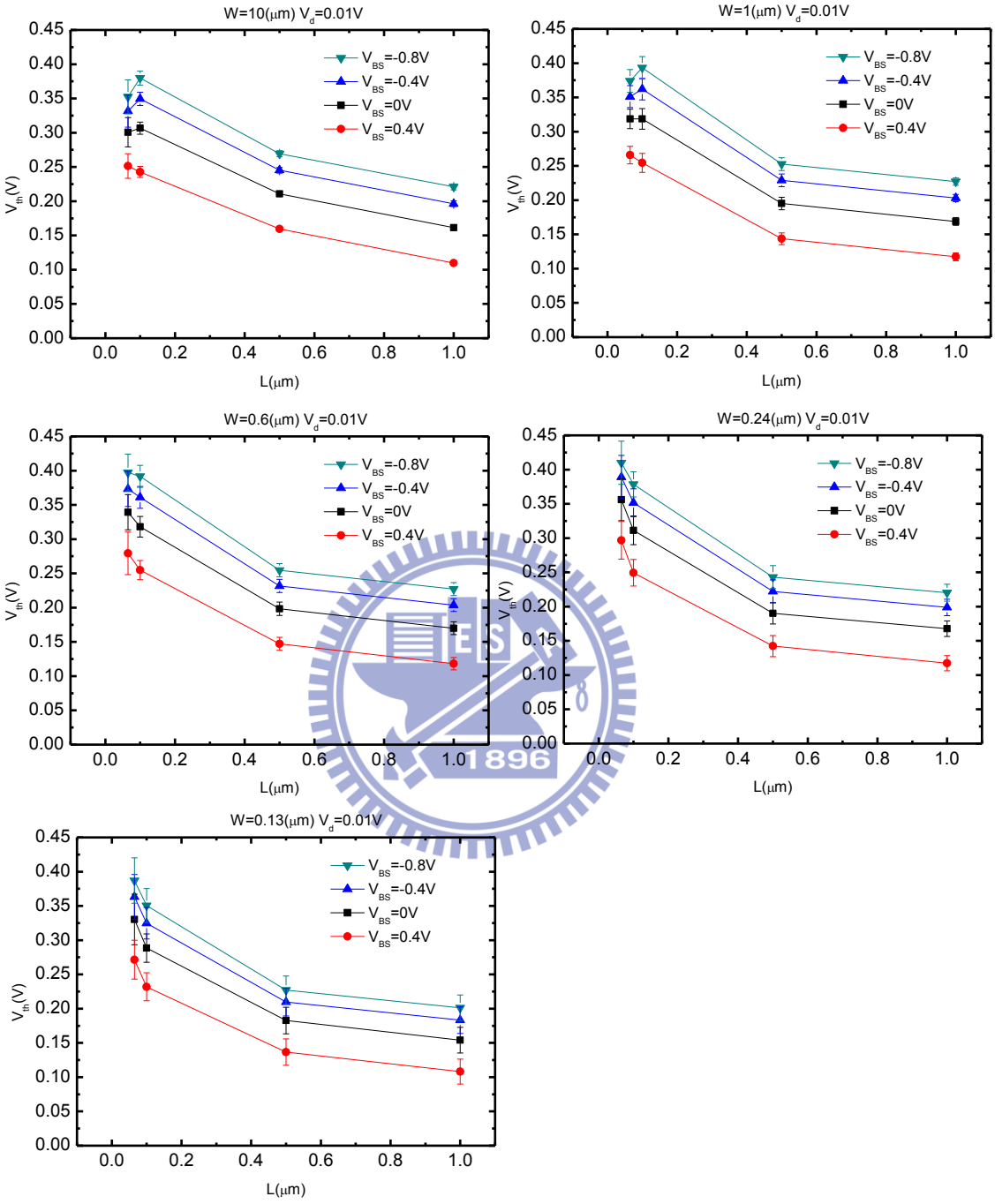


Fig. 4 Measured mean threshold voltage with standard deviation versus the channel length for different back-gate biases.

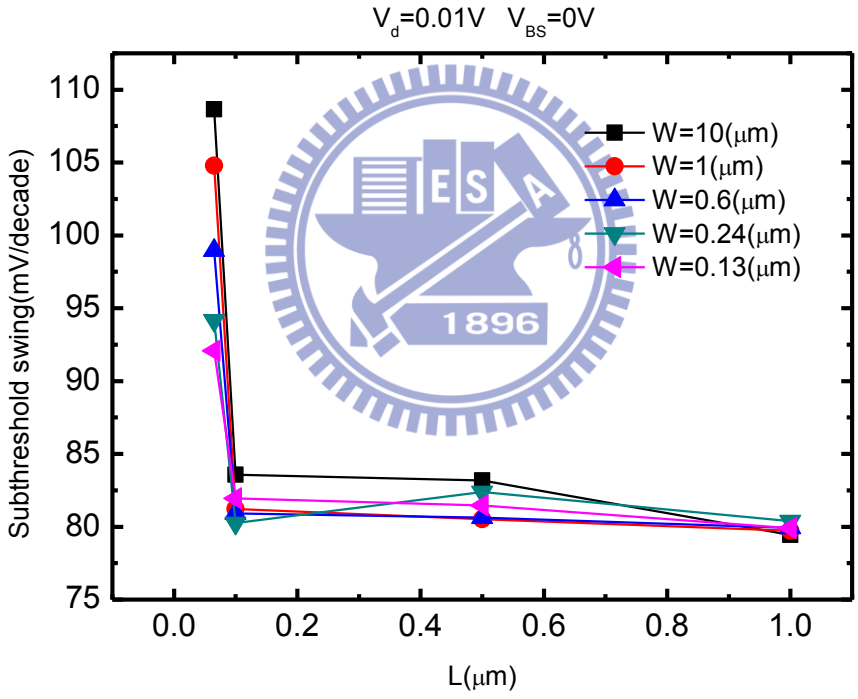


Fig. 5 The measured subthreshold swing versus gate length for different gate widths.

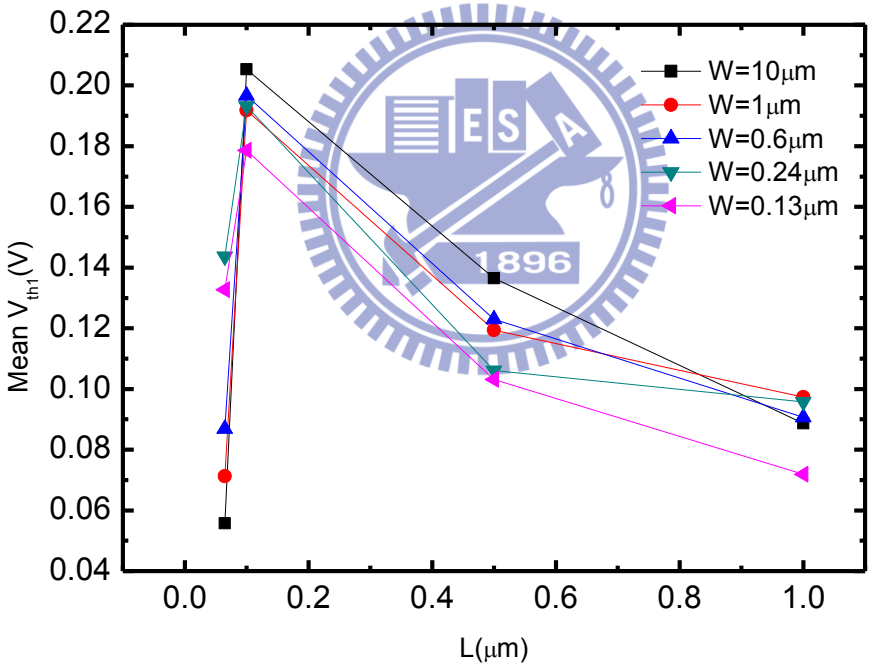


Fig. 6 Measured mean threshold voltage versus L for different channel widths for $V_d = 1V$.

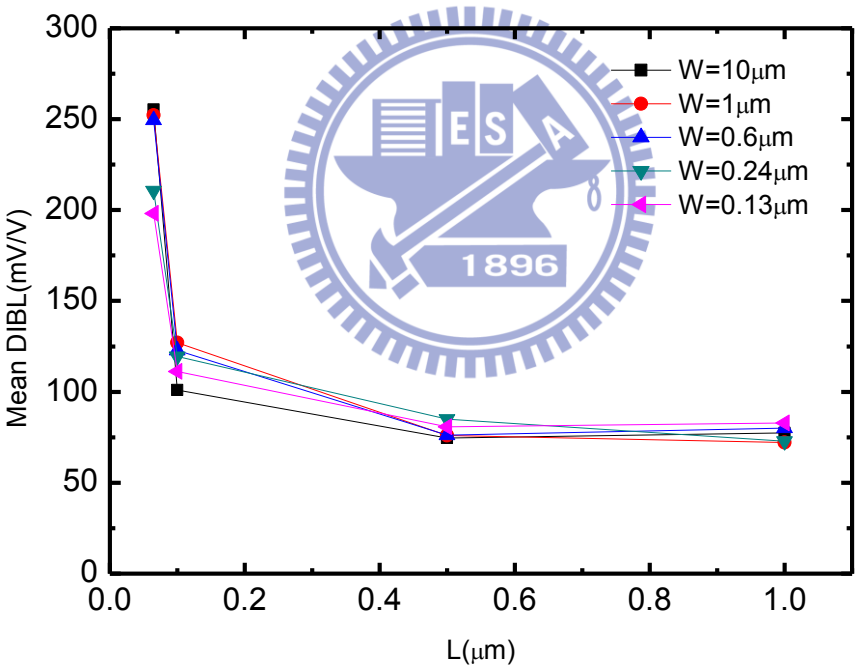


Fig. 7 Extracted DIBL versus L for different channel widths.

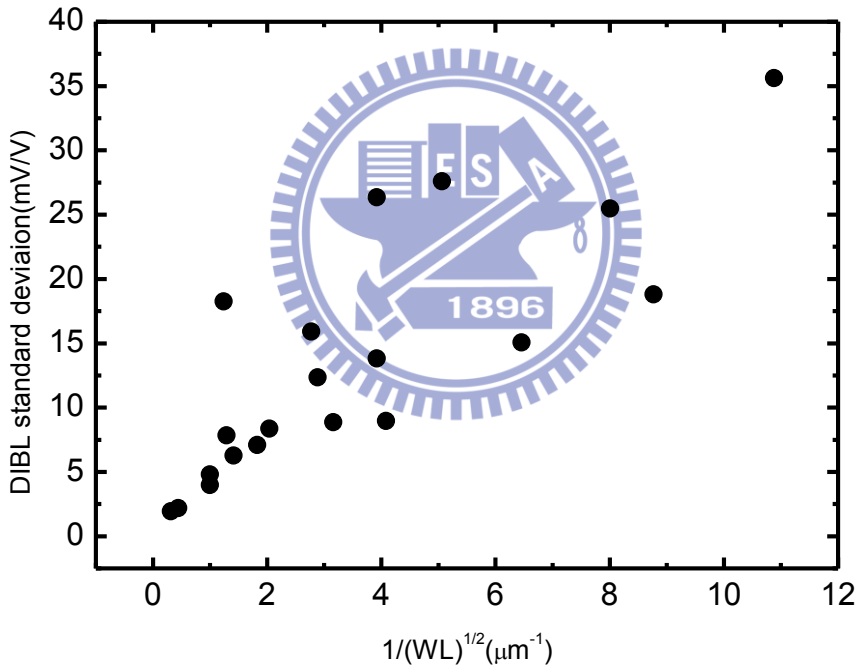


Fig. 8 The measured DIBL standard deviation versus the inverse square root of the device area.

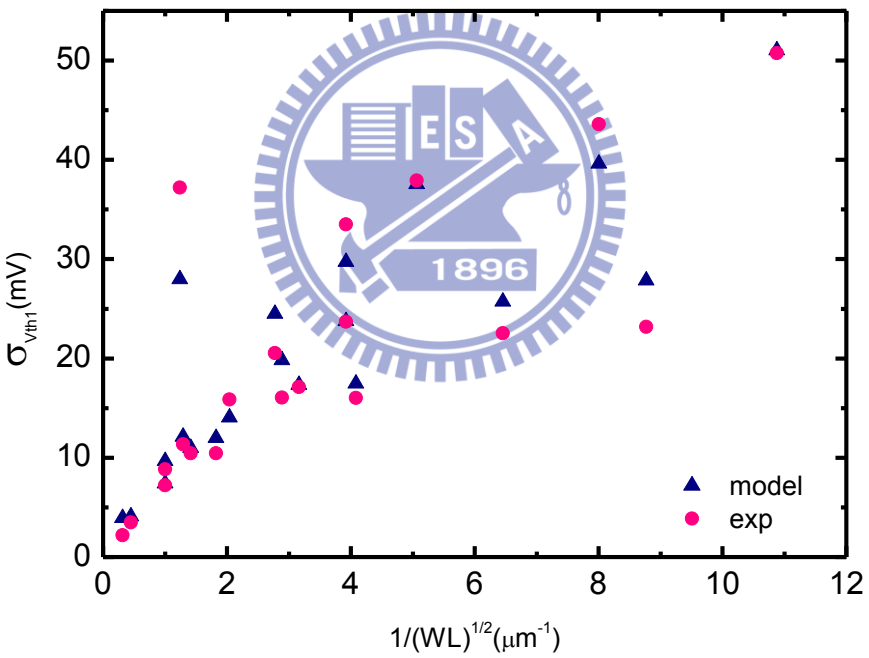


Fig. 9 The measured and calculated $V_{th1}$ standard deviation versus the inverse square root of the device area.

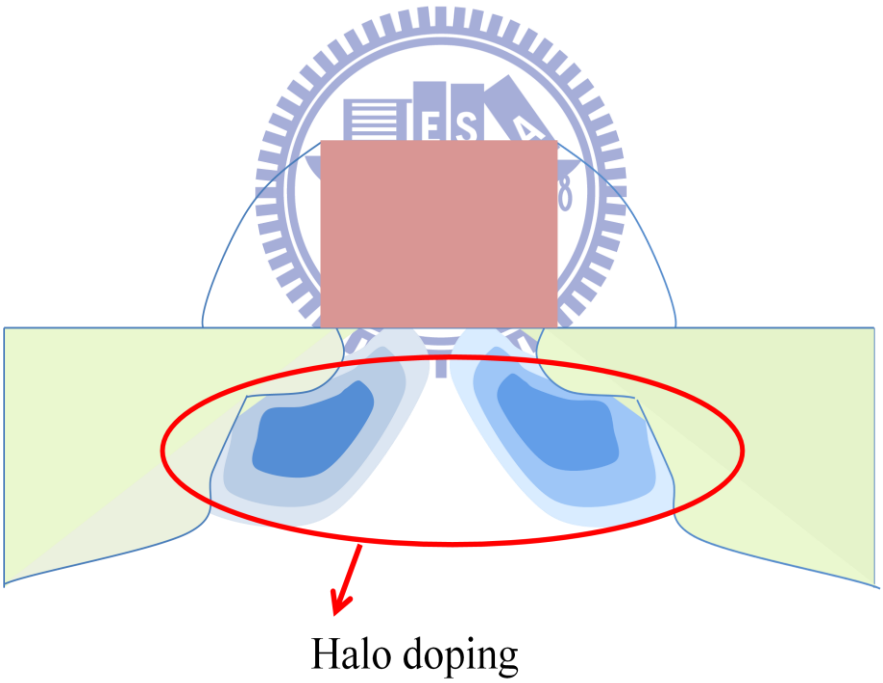


Fig. 10 The schematic drawing of halo doping device.

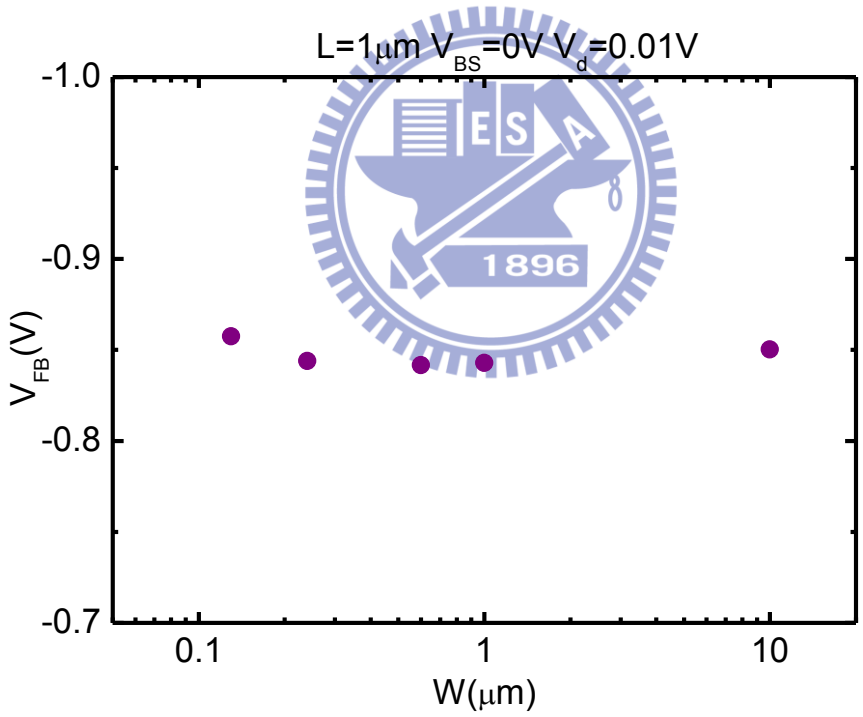


Fig. 11 The flat band voltage versus channel width at L=1 $\mu m$.

| $N_{A\_eff}(cm^{-3})$ | W=10 ($\mu m$) | W=1 ($\mu m$) | W=0.6 ($\mu m$) | W=0.24 ($\mu m$) | W=0.13 ($\mu m$) |
|---|---|---|---|---|---|
| L=1 ($\mu m$) | 4.00E+17 | 4.00E+17 | 4.00E+17 | 4.00E+17 | 4.00E+17 |
| L=0.5 ($\mu m$) | 5.92E+17 | 4.96E+17 | 5.04E+17 | 4.81E+17 | 5.05E+17 |
| L=0.1 ($\mu m$) | 1.13E+18 | 1.16E+18 | 1.15E+18 | 1.12E+18 | 1.05E+18 |
| L=0.065 ($\mu m$) | 1.09E+18 | 1.16E+18 | 1.30E+18 | 1.44E+18 | 1.35E+18 |

Fig. 12 The extracted $N_{A\_eff}$ of all device sizes.

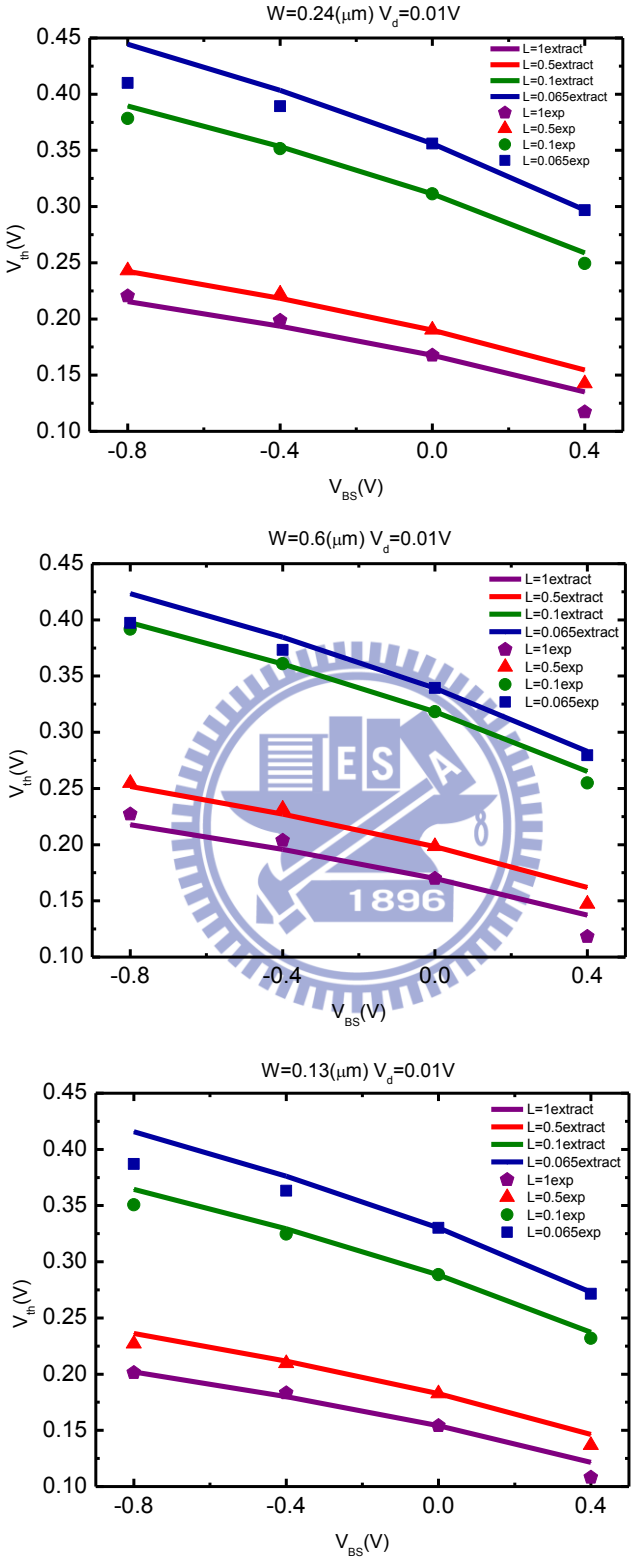


Fig. 13 Comparison of the $V_{th}$ extracted from $N_{A\_eff}$ and the experimental data.

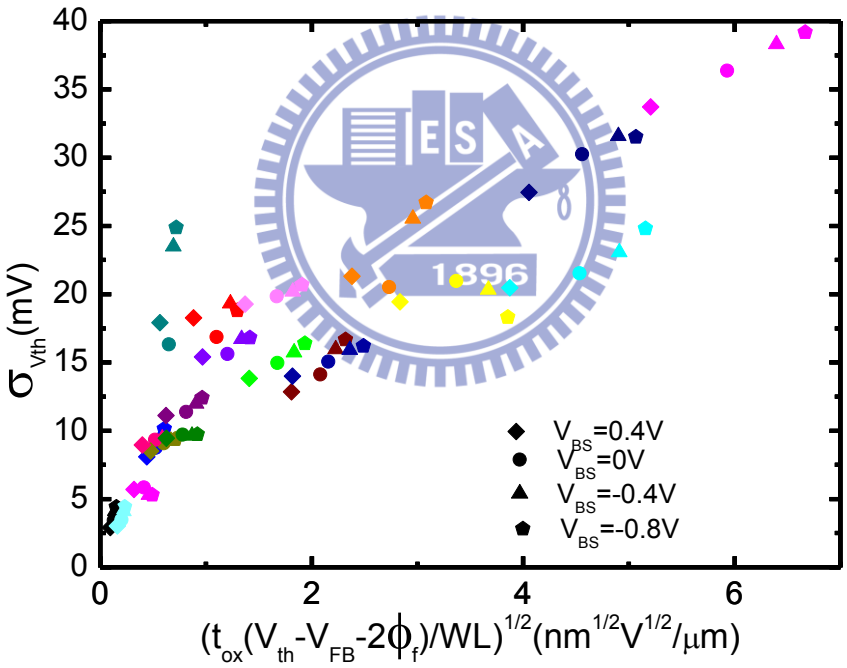


Fig. 14 Using measured data based on the fluctuation model to show the results of all device sizes for different back-gate biases.

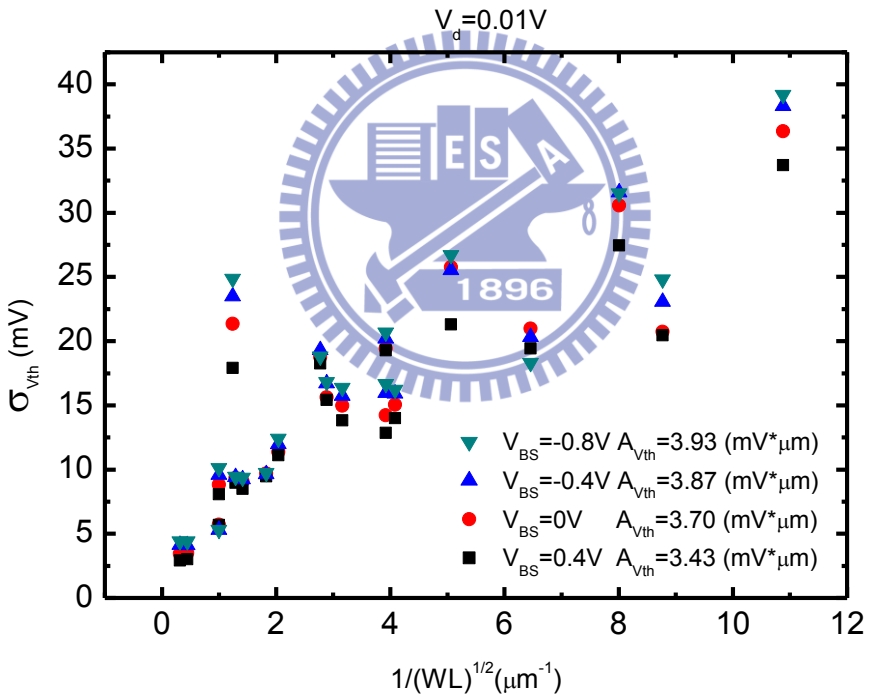


Fig. 15 The measured standard deviation of threshold voltage difference versus the inverse square root of the device area for different back-gate biases.

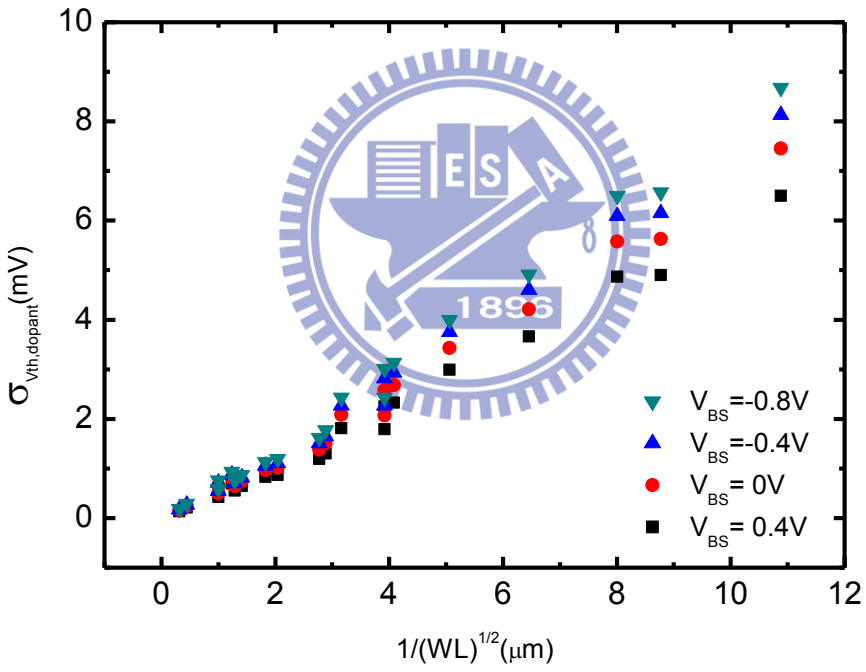


Fig. 16 The calculated $\sigma_{Vth,dopant}$ versus the inverse square root of the device area for different back-gate biases.

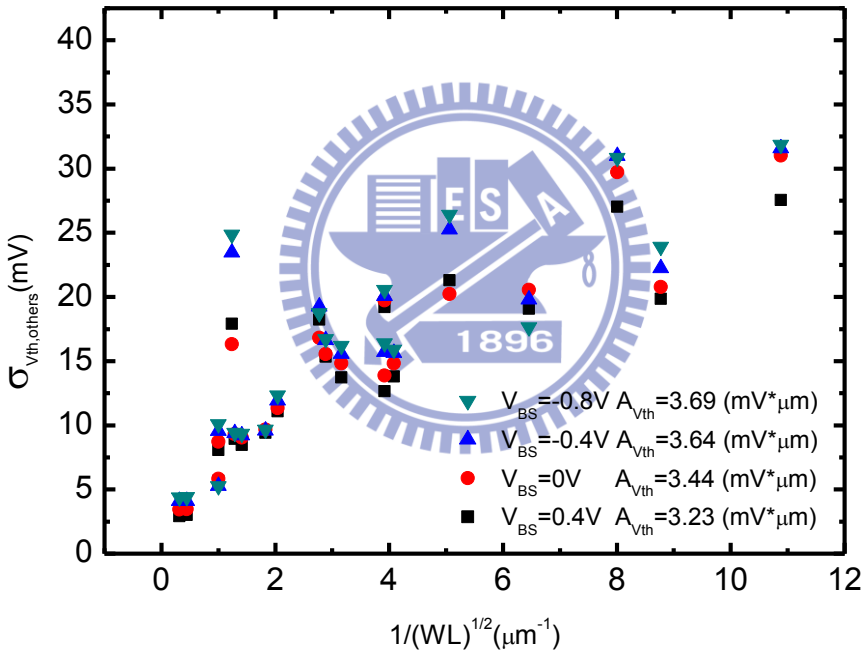


Fig. 17 The extracted $\sigma_{Vth,others}$ versus the inverse square root of the device area for different back-gate biases.

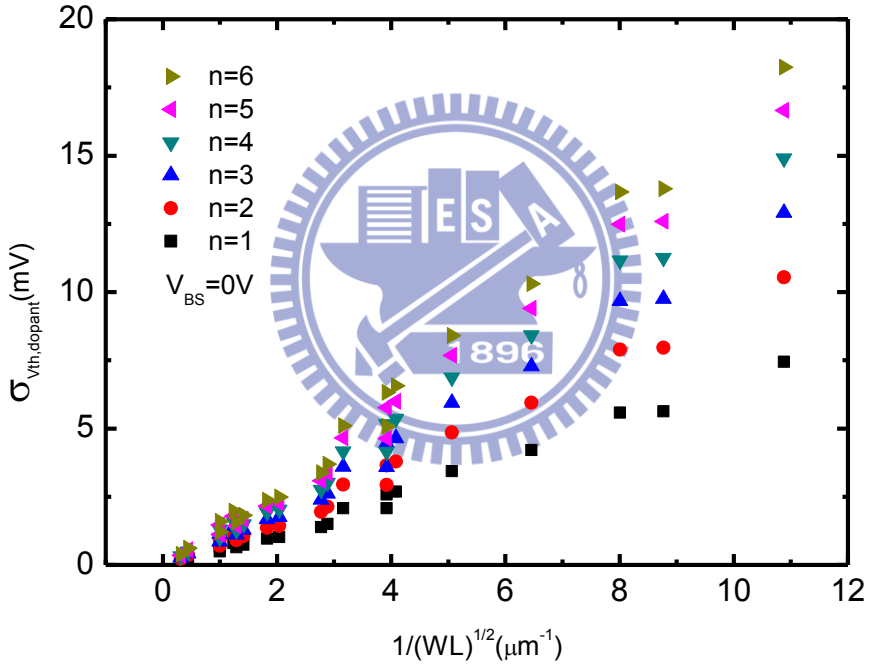


Fig. 18 The $\sigma_{Vth,dopant}$ with different number of boron atoms per cluster versus the inverse square root of the device area for zero back-gate bias.

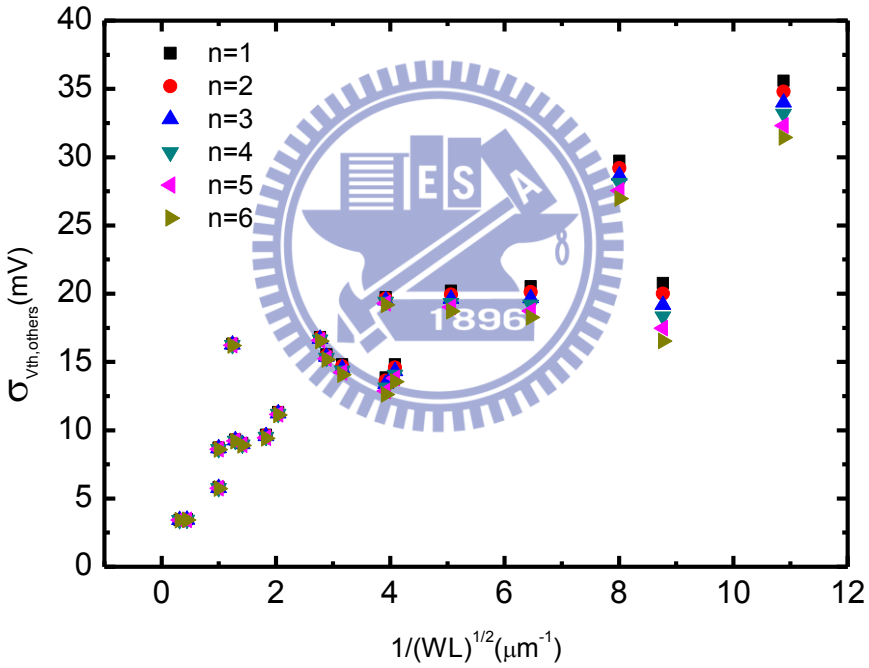


Fig. 19 The $\sigma_{Vth,others}$ with different number of boron atoms per cluster versus the inverse square root of the device area for zero back-gate bias.

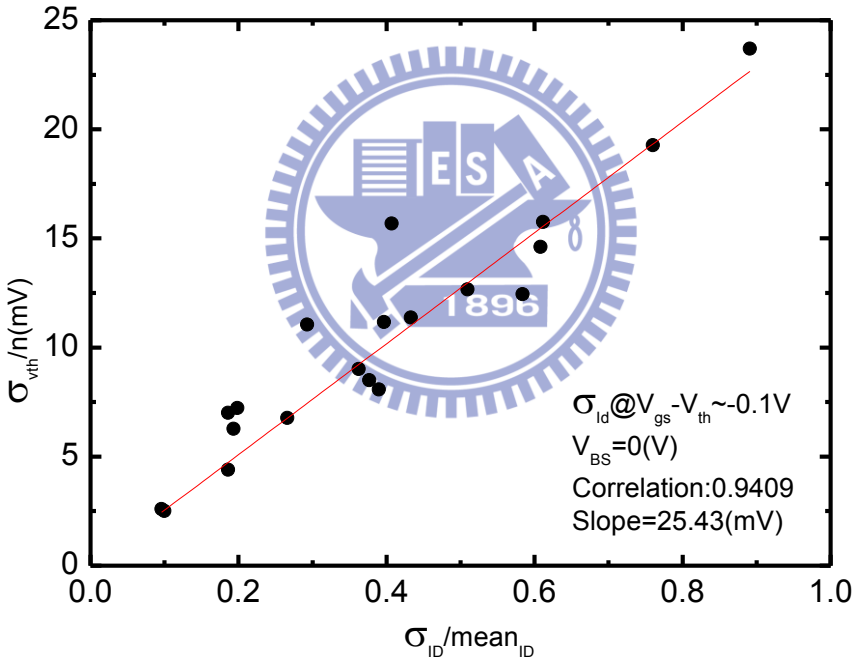


Fig. 20 The experimental data and fitting line from the drain current and threshold voltage mismatch model.

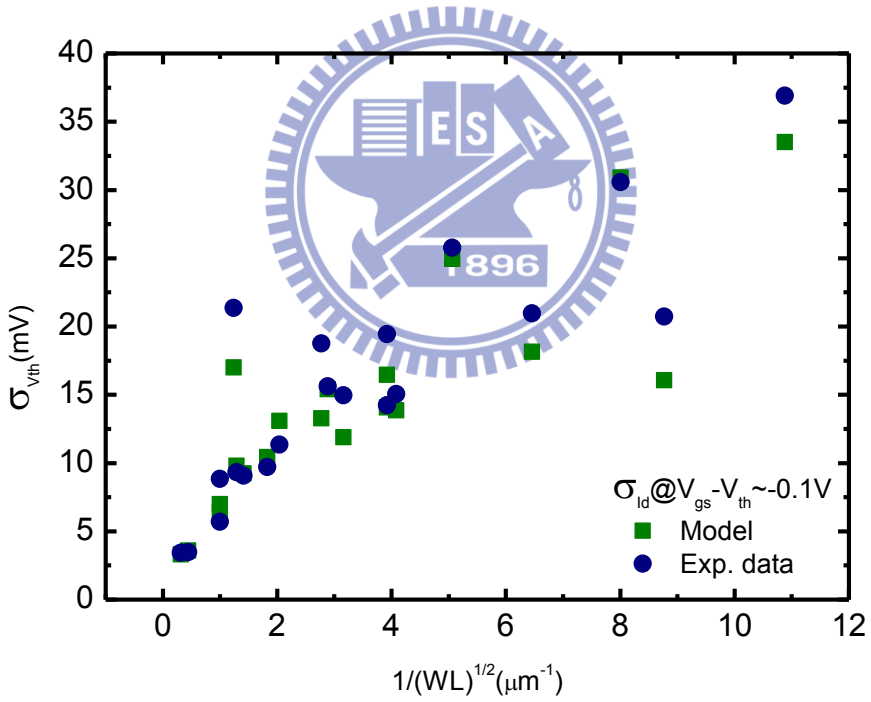


Fig. 21 The standard deviation of threshold voltage from model and experiment.

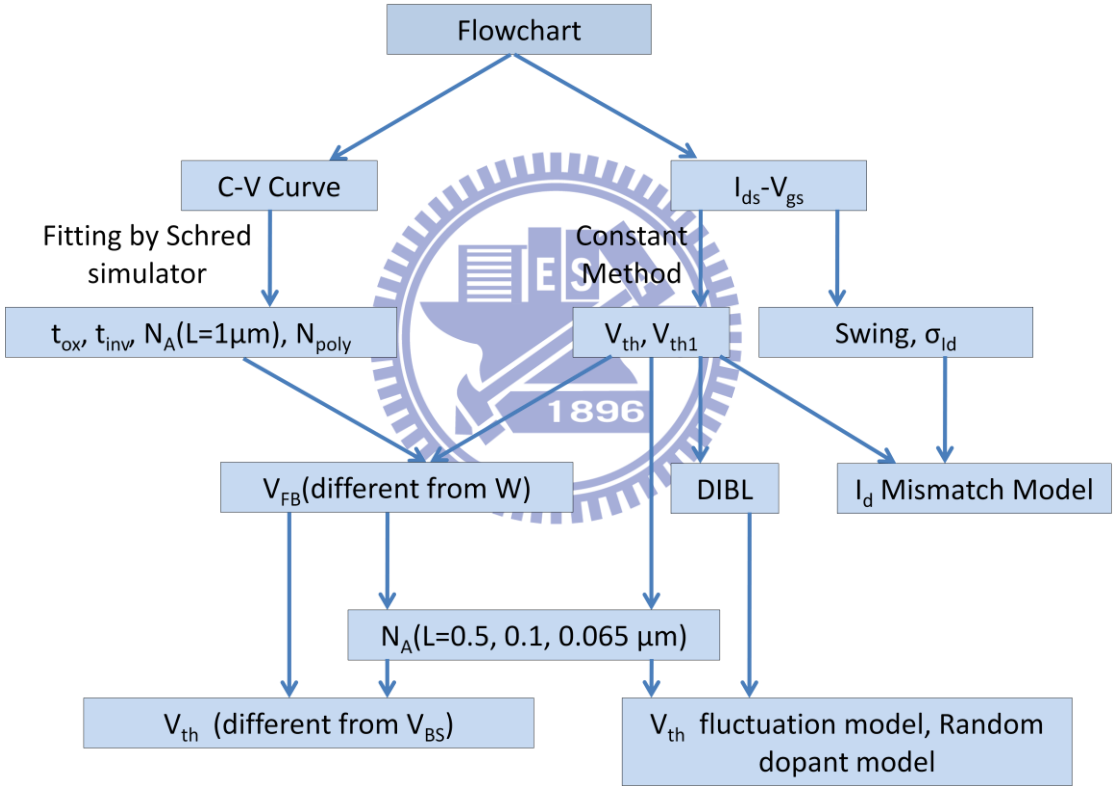


Fig. 22 The schematic flowchart for the procedure used in our works.