國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

具有低電壓之金屬-氧化層-氮化層-氧化層-矽
結構非揮發性記憶體之製程技術應用與研究

Process and Technology For Low Voltage MONOS Non-Volatile Memory

研 究 生：李宗翰

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中 華 民 國 九 十 九 年 七 月

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A Thesis

Submitted to Department of Electrical Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

In partial Fulfillment of the Requirements

For the Degree of Master

In

Electronics Engineering

July 2010

Hsinchu, Taiwan, Republic of China

中華民國九十九年七月

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摘要

近年來，在半導體產業中，記憶體元件的發展已成為另一主流。其中，屬於非揮發性型態的快閃式記憶體因其具有高密度特性、良好的資料保存能力和重複抹寫功能而被廣泛的使用在個人行動電子產品，例如手機或數位相機。隨著這些電子產品的普及化，對快閃式記憶體的需求也快速增加。因此，快閃式記憶體的發展和技術已成為重要的研究之一。

隨著元件尺寸持續縮微，快閃式記憶體主要的製程技術關鍵為其具有導電性的多晶矽浮停閘。基於非揮發性記憶體基本的需求，以多晶矽材料當作電荷儲存層的快閃式記憶體需要厚度至少約 6－7奈米的穿遂氧化層來防止儲存電荷遺以增加資料儲存能力。其主要原因為反覆的編碼和抹除過程將會對穿遂氧化層造成應力而產生缺陷，這些缺陷可能形成漏電路徑而導致多晶矽全面性的漏電。然而，較厚的穿遂氧化層不僅需要較大的操作電壓也增加元件製程縮微的困難度。為了解決此問題，多晶矽材料將被氮化矽所取代。由氮化矽電荷儲存層所形成的多晶矽或金屬閘極-氧化矽-氮化矽-氧化矽-矽結構記憶體元件可以解決平面微縮的問題且同時具有良好電荷儲存能力、低工作電壓特性和符合目前互補式金氧半場效電晶體元件的製程，因此已開始受到大家的關注。

在此論文中，我們使用全新的高介電係數介電質材料氧化鉿（介電係數約25）和氧化鋯（介電係數約35）形成交錯層取代傳統的氮化矽電荷捕獲層。高介電係

數介電質的使用，不僅可以有效降低操作電壓，同時也可以將電壓有效的跨在薄二氧化矽穿遂層以增加編碼和抹寫速度。此外，應用具高功函數的金屬閘極氮化鉭替代傳統多晶矽閘極可以防止在抹除狀態時電荷從閘極端注入並增加抹除效率。

Process and Technology For Low Voltage MONOS Non-Volatile Memory

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Abstract

Recently, the Flash memory is commonly used in portable electronic products, such as cell phone, MP3 player and USB Flash. However, with the increase in requirements for products, the technology and process must be still improved.

The key issue for poly-Si floating gate non-volatile memory is the electrically conductive charge storage layer, where the programmed electrons will leak out through the single oxide defect. Such oxide defects are generated by the program and erase stress operation. In order to maintain the data retention, the thick tunnel oxide (6-7 nm) is required. That is opposite to the VLSI scaling trend. In addition, the memory device with thick tunnel oxide requires a higher operation voltage. To overcome this problem, the conductive poly-Si is replaced by discrete trapping nitride to form the [poly-Si or metal gate]-SiO_2-Si_3N_4-SiO_2-Si SONOS or MONOS memory. The isolated charges stored in discrete traps can prevent complete charge leakage. Therefore, a thinner tunnel oxide can be used. This in turn yields lower voltage and faster speed for program and erase.

In this dissertation, we demonstrated a low voltage, fast speed and good data retention MONOS memory device with high work function MoN metal gate, novel

interactive high-κ HfO_2-ZrO_2 structure for trapping layer substituted conventional Si_3N_4 trapping layer.

誌謝

兩年忙碌的碩士班生活，也隨著論文的完成而進入尾聲，首先，要感謝我的指導老師- 荊鳳德博士對我耐心的指導，讓我在這兩年中學習到做研究的態度和方法，也培養出我面對問題時的解決能力，並告訴我們第一手的世界級科技新知讓我們做的研究能跟上世界的腳步，讓我們碩班兩年所學足以應付未來工作。

我首要感謝博士班 蔡竣揚學長的耐心指導，從機台訓練、學業指導、量測方式、到結果討論全都傾囊相授，讓我受用無窮；真的很慶幸能有你這樣的學長，伴隨我這兩年碩士生活。還有我要感謝博士班 陳維邦學長、周坤億學長以及博士後研究 鄭淳護學長，你們的經驗傳授，讓我克服了許多大大小小問題。另外也感謝我的同屆同學們-明倫、佳芸、智偉以及柏君，一起討論不好意思詢問學長的簡單問題，一起分享研究的酸甜苦辣，你們是碩士班這段旅途裡不可或缺的夥伴，謝謝你們。我必須感謝我的學弟 廷瑜，不僅努力跟隨我學習也陪伴我做實驗，讓空虛的無塵室有一點笑聲。

接著，我要感謝國家奈米元件實驗室與交大奈米中心提供優良的製程環境。

最後，我要感謝我的母親鄭香梅女士和我的兄長宗憲，謝謝他們一路上的栽培與耐心的陪伴，在我遭受挫折或沮喪時給我安慰與能量，使我有勇氣面對困境並得以順利突破，你們是我心靈最後的歸宿，謝謝你們。

李宗翰

99年7月

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Chapter 1

Introduction

1-1 Motivation to study high-κ dielectrics

Along of the improvement of the semiconductor processing technology, the scaling trend of MOSFETs devices will produce the large gate leakage current due to thinner gate oxide [1.1]-[1.2]. The MOSFETs exhibit significant leakage current more than 1 A/cm^2 when the thickness of ultra-thin silicon gate oxide (SiO_2) is less than 2 nm. To reduce the leakage current related higher power consumption in highly integrated circuit and overcome the physical thickness limitation of silicon dioxide, the conventional SiO_2 will be replaced with high dielectric constant (high-κ) materials as the gate dielectrics beyond the 0.1μm technology node [1.3]-[1.8]. Therefore, the engineering of high-κ gate dielectrics have attracted great attention and played an important role in technology pull for VLSI. Although high-κ materials often exhibit smaller bandgap and higher defect density than conventional silicon dioxide, using the high-κ gate dielectric can increase efficiently the physical thickness in the same effective oxide thickness (EOT) that shows lower leakage characteristics than silicon dioxide by several orders without the reduction of capacitance density [1.4]-[1.7]. Recently, some high-κ materials have been widely studied and successfully intergraded in advanced MOSFETs or semiconductor devices, such as DRAMs or Flash memory and RF metal-insulator-metal (MIM) capacitors [1.9]-[1.10]. According to the ITRS (International Technology Roadmap for Semiconductor), the suitable gate dielectrics must have κ value more than 8 for 50-70 nm technology nodes and that must be more than 15 when the technology dimension less than 50

nm.

Fig. 1-1 shows the evolution of MOSFET technology requirement.Moreover, the useful gate dielectrics should meet the following fundamental requirements:

- Thermodynamic stability on silicon with respect to formation of SiO_2 and MSi_x.
- Amorphous after device integration, implies that the dielectrics should remain amorphous after S/D or elevated temperature activation.
- Low conduction for low leakage and low power consumption. For metal oxides (MO_x), it is well known that bandgap is inversely related to κ value (the aluminum oxide as an exception). Low leakage current implies large band-offset for electrons and holes.
- High carrier mobility at the dielectric/Si interface. Therefore, the low D_{it} and lowbulk charges (low effective fixed charges) are requirements.
- High breakdown strength and acceptable reliability. The breakdown strength isinversely related to κ value for metal oxides.

The most popular high-κ materials which are studied extensively nowadays are metal oxides (MO_x), such as Ta_2O_5, TiO_2,HfO_2, ZrO_2,Al_2O_3 and La_2O_3 which have the higher κ values ranging from 9 to 80. However, the most metal oxides will have the characteristics of crystallization at elevated temperature which cause devices generate non-uniform leakage distribution and give large statistical variation for nano-meter devices across the chip. Therefore, replacement gate strategies have been proposed to prevent crystallization and deleterious effects of mass and electrical transport along grain boundaries. Figs.1-2 and 1-3 summarize the κ value and band offset for popular high-κ dielectric candidates.

1-2 Motivation to study metal gate

Metal gate is required for advanced CMOS transistors to eliminate poly gate

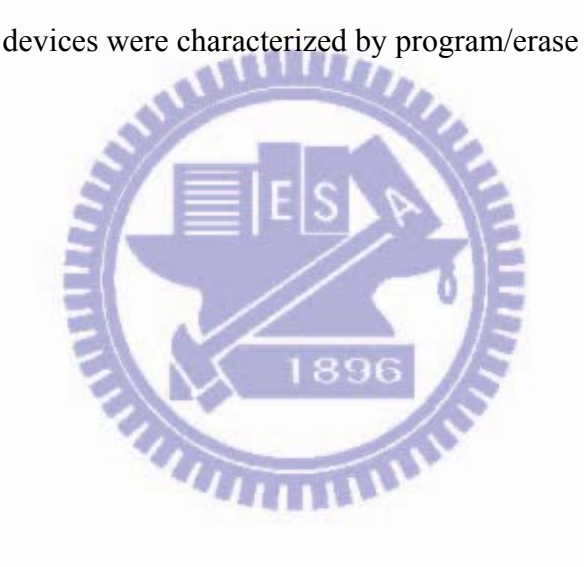
depletion [1.11]-[1.18]. Since the EOT target prescribed by the ITRS roadmap in years 2018 is only 0.5 nm for 7 nm CMOS, any depletion of the poly-Si gate electrode will be unacceptable. To overcome this problem, the metal gate electrode will be required to make poly-depletion free due to the poly depletion will reduce the capacitance and contribute a degradation to EOT in inversion state [1.11]-[1.23], is shown in Fig.1-4. The work function (Φ_B) of metal (in Fig.1-5) play an important role for metal-gate/high-κ MOSFET. The preferred work function of the metals are ~5.1 eV for p-MOSFETs and ~4.2 eV for n-MOSFETs. However, one of the difficult challenges for metal-gate/high-ķ CMOS devices is large threshold voltage (Vth) due to Fermi-level pinning effect. This is especially difficult for p^-MOSFET [1.11] since only Ni (5.15 eV), Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table have work function close to the desired 5.2 eV used in conventional p^+ poly-Si gated p^-MOS (in Fig.1-5). In addition, thermal stability of the effective metal electrode and metal diffusion are also important considerations. Recently, lots of metal or metal-nitride materials have been widely researched and successfully intergraded in advanced CMOSFET's, such as TiN, TaN, Pt, Mo, MoN and Ir [1.11]-[1.23]. Molybdenum (Mo) has a work-function close to n^+ poly-Si. Molybdenum nitride (MoN) is quite stable (to maintain thermal stability up to a 1000^{o}C RTA) because the activation energy of metal and nitrogen is relatively low. Molybdenum is bonded tightly within nitride and no obvious diffuse was observed in fabricated devices. However, MoN gate on high-ķ HfO_2 shows a significant shift of flat band voltage (V_{FB}) toward the mid-gap of Si due to the interface reaction between the MoN and HfO_2 at the high temperature. This is called the "Fermi-level pinning effect." Therefore, the Fermi-level pinning effect needs to be avoided by selecting suitable metal gate and high-κ materials for advanced MOSFETs.

For MONOS structured non-volatile memory device, the metal electrode with high

work function is needed. The metal gate with higher work-function can prevent the electron injection from electrode in erase operation [1.24]. That improves efficiently erase speed.

1-3 The measurement of the devices

To investigate the electrical characteristics of devices, we measured the I_g-V_g curves for gate leakage current by using HP4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the gate capacitance and the conductance ranging from 100 kHz to 1 MHz. For memory measurement, the fabricated MONOS devices were characterized by program/erase measurements.



		2003	2005	2007	2009	2012	2015	2018
Gate Length (nm)		107	80	65	50	30	25	18
EOT (nm)	High Speed	1.3	1.2	0.9	0.8	0.7	0.6	0.5
	Low Power	1.6	1.4	1.2	1.0	0.9	0.8	0.7
S/D Junction Depth (X_j, nm)*		49.5	35.2	27.5	NA	NA	NA	NA
Interconnect Levels		9	11	11	12	12	13	14
Logic V_{DD} (V)	High Speed	1.2	1.1	1.1	1.0	0.9	0.8	0.7
	Low Power	1.0	0.9	0.8	0.8	0.7	0.6	0.5

Source: International Technology Roadmap for Semiconductor (ITRS 2003)

Fig.1-1 The evolution of MOS technology requirement.

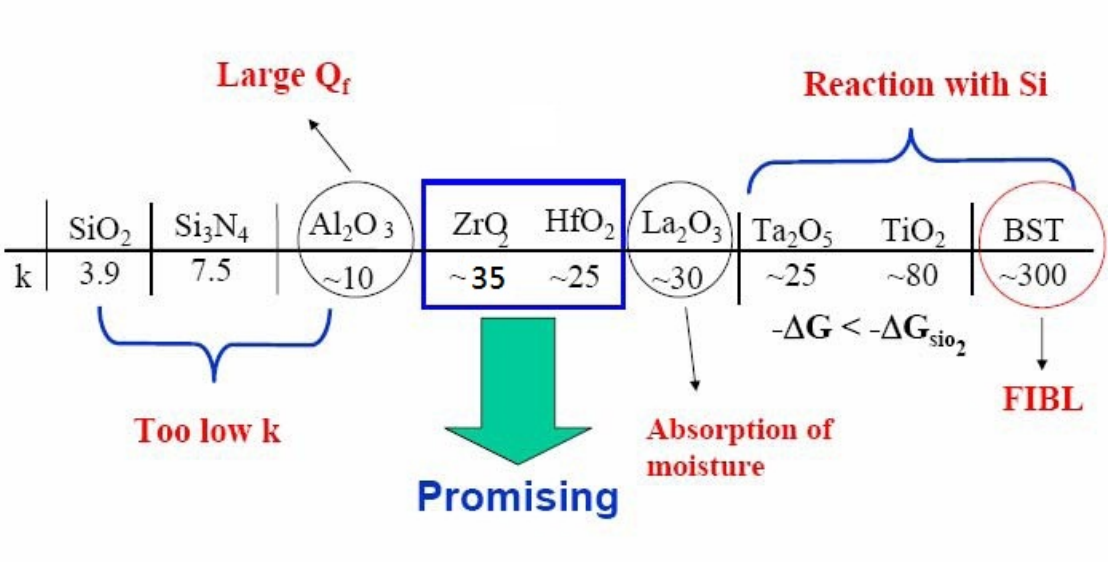


Fig.1-2 The value of high-κ materials.

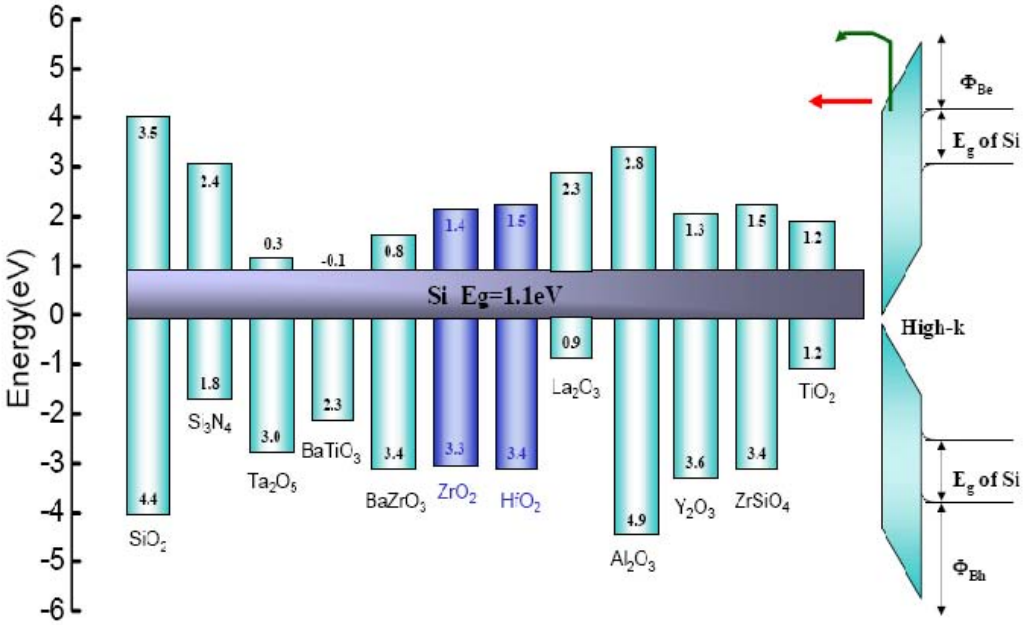


Fig.1-3 The band offset of popular high-κ materials.

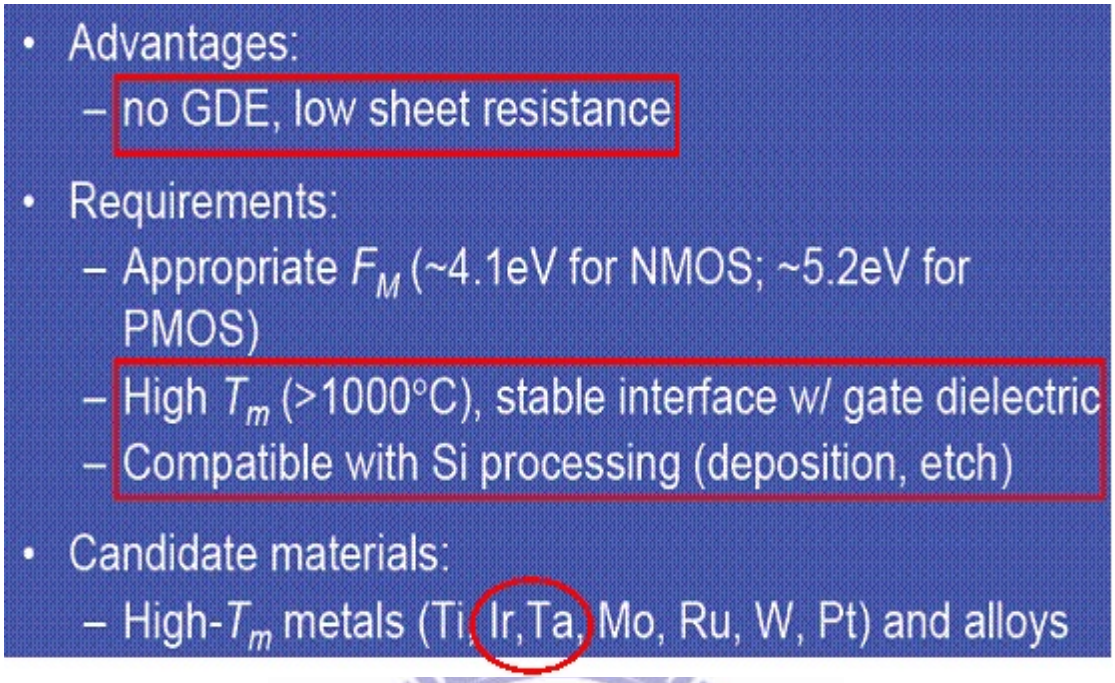


Fig.1-4 The advantages and requirements of metal gate technology.

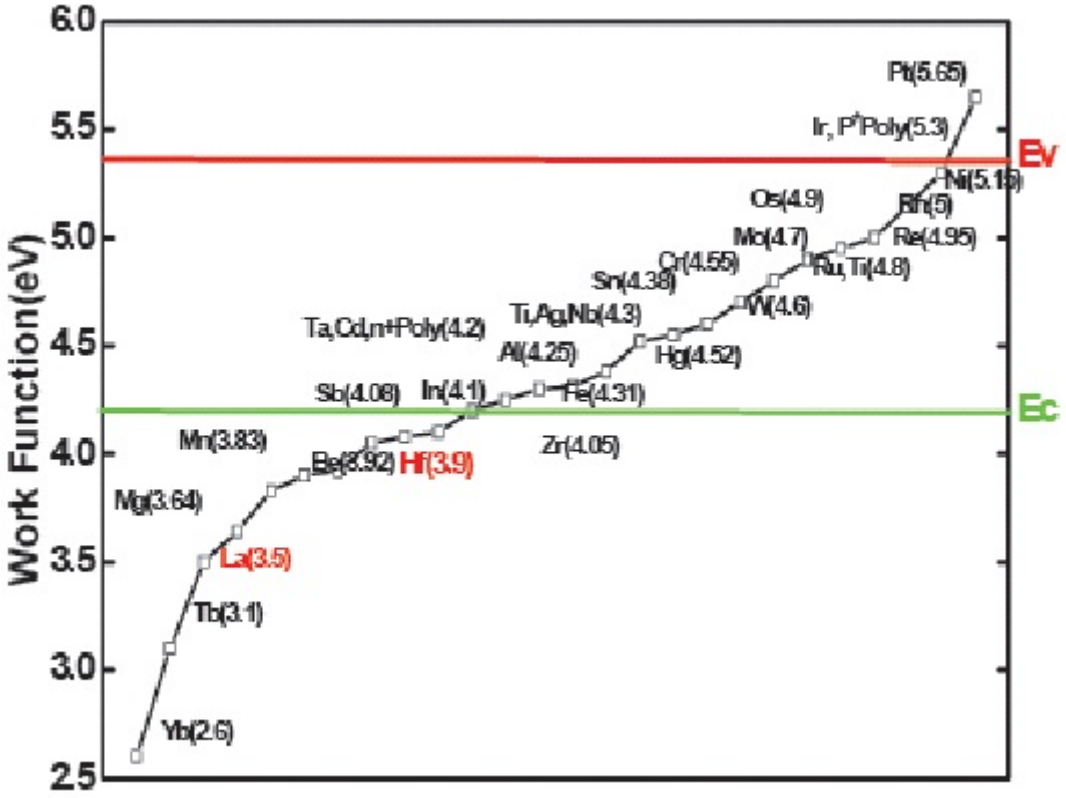


Fig.1-5 The values of work function for different metal materials.

Chapter 2

General Background of Flash Memory

2-1 Evolution of Non-volatile Memory

Since the millennium, people's daily life habit has been changed by various kinds of portable electronic products, such as notebook computer, digital camera, MP3 player, personal digital assistant (PDA), USB, iPod…and so on. The memory devices need to be adopted into all of these electronic products to make them work for different functions. These memories can be divided into volatile memory and non-volatile memory. The use of non-volatile memory (NVM) is to remain the storage data for a long time without power supply, and then portable electronic products can work just by battery due to low power consumption of non-volatile memory.

Non-volatile memories are mainly classified into non-charge-based memory and charge-based memory. The typical charge-based memory is the so called flash memory. There are three types of flash memory including the floating gate (FG) type, SONOS (Silicon/Oxide/Nitride/Oxide/Silicon) type, and nano-crystal type. The mainstream of NVM nowadays is floating gate (FG) type. Some non-charge-based memories have been in small volume production, such as magnetroresistive random access memory (MRAM). The production technologies of ferroelectric random access memory (FeRAM) and phase change random access memory (PCRAM) are still under development. A novel resistive random access memory (RRAM) attracts much more attention recently . All types of flash memories and non-charge-based memories are introduced in detail in the following section.

Smart system must have larger brains which include both sophisticated functions

(code storage) and more memory capacity (data storage). These characteristics can be served by two types of flash memories. The NOR-type memory has fast and random access capability for the code storage, and the NAND-type memory has the page access architecture for date storage [2.1].

2-1.1 Overview of Non-volatile Memory Development

After decades of development with device scaling, several technologies have been employed for product manufacturing, including earlier metal-nitride-oxide-semiconductor (MNOS), electrical programmable read-only-memory (EPROM), and more recently Flash [2.2][2.3].

Because of mass data storage requirement in electronic products, Flash device has become the mainstream in non-volatile semiconductor memory products nowadays [2.4]. An indispensable trend for technology development is to shrink the channel length for a higher storage capacity. Moreover, lowering the voltage for writing/erasing operations is essential for lower power consumption, while high speed access is required to shorten mass data storage time.

2-1.2 Floating Gate and SONOS Memory Device physics

Fig. 2-1 shows that it is necessary to extend the actual flash memory device technology lifetime as much as possible. Through decades of development, flash devices are categorized into two types of structures, namely, FG [2.5] and charge trapping structures, as illustrated in Fig. 2-2. For FG devices, owing to the high topography of the gate structure, the interference between neighboring cells by gate coupling becomes an almost unsolvable issue beyond 45nm-node. As a consequence charge trapping flash memory devices such as SONOS is revisited as the succeeding technology to avert interference between neighboring cells.

Before the floating gate (FG) non-volatile memory, the magnetic-core memory[2.7] has a lot of issues, such as large volume, high power consumption, and high cost. Therefore, new kind of memory needs to be invented to replace the magnetic-core memory. In 1967, the first floating gate non-volatile memory was invented by D. Kahng and S. M Sze at Bell Labs [2.8]. FG structure is composed of a POLY1 floating gate inserted between an underlying tunnel oxide and a blocking oxide layer. A POLY2 layer is deposited on top of the blocking oxide layer to serve as the control gate, as shown in Fig. 2-3. In SONOS structure, in Fig. 2-4, a carrier-trapping layer made up of nitride is inserted between two silicon oxide layers to prevent charge loss. Such flash cells resemble a standard MOS transistor except that the gate oxide is replaced by an oxide-nitride-oxide dielectric stack [2.9].

The storage material is typically a degenerately doped poly-Si for floating-gate devices and a nitride layer for SONOS devices. The mechanisms of charge storage are different between the two types of devices due to the different storage materials. Since the floating gate is made up of a conducting material, the stored electrons flow freely inside the floating gate. This raises a reliability issue in that if certain paths for stress induce leakage current (SILC) are created in the tunnel oxide during operation, the stored charges may easily find the path to leak out which in turn lead to poor retention and endurance characteristics. On the other hand, the nitride storage layer in SONOS device contains discrete traps serving as the charge storage sites. The injected electrons are trapped in deep level of the nitride layer and become immobile, so the aforementioned SILC issue can be avoided and better retention and endurance are expected [2.10].

Programming operation can be achieved by injecting charges into the storage layer, a nitride for the SONOS or a poly layer for the FG type. Channel or substrate hot carrier injections are usually employed for this purpose. On the other hand, erasing

mechanism could be implemented via band-to-band hot holes injection from drain side. For efficiency, both programming and erasing operations need high biases on the gate and drain. The high electric field may provoke potential reliability concerns such as oxide breakdown and generation of excessive SILC. Moreover, high power consumption while the devices are under programming and erasing operations is inevitable [2.11].

The difference between FG and SONOS-type devices lies in the method of charge storage, which is fundamental to issues such as scaling and radiation hardness. The concept of nonvolatile data storage based on a shift in the threshold voltage of the nonvolatile semiconductor memory (NVSM). The threshold voltage has the following expression [2.12]

$$V_{th} = \Phi_{GS} + 2\Phi_F - \frac{Q_{SS}+Q_S}{C_I} + \frac{Q_T}{\varepsilon_I} \qquad \text{(Eq.2-1)}$$

where Qss is the fixed charge at Si-SiO_2 interface, Q_S is the charge in silicon semiconductor, Q_T is the charge stored in the gate insulator, C_I and ε_I are the capacitance per unit area and dielectric constant of the gate insulator layer, respectively. Based on Eq.2-1, threshold voltage increases when more electrons are trapped. On the contrary, threshold will be decreased, if Q_S quantities are reduced. Therefore we can control Q_S by means of varying the substrate doping concentration to adjust the threshold voltage of flash devices. The threshold voltage window (Program V_{th} – Erase V_{th}) should be maintained at least 1.5V to easily distinguish between "1" and "0" states by peripheral sense amplifier circuits [2.13]. The storage charges will gradually leak away as the storage time progresses because of the existence of different leakage mechanisms. The capability of preserving the charge

storage is directly related to the data retention and device life time. Therefore the FG device has added a thick oxide layer or ONO (oxide-nitride-oxide) layer above POLY1 to reduce charge loss through the top side while keeping the gate coupling ratio. On the other hand, SONOS must maintain a tunneling oxide thickness of around 2nm or above to prevent the excessive direct tunneling of charges from nitride layer to substrate. When thickness of oxide is smaller than 25Å or extreme big electric field across on the thin oxide, it is easier to happen direct tunneling which is hopeless for ONO structure and it could be eliminate retention. High temperature data retention analysis is usually performed to monitor the variation of programmed threshold voltage as a function of the elapsing time. The measurements are typically performed between 150^{O}C and 250^{O}C to ensure 10-year data retention time. Both programmed and erased operations affect the endurance capability of flash devices. These procedures should thus be carefully designed and optimized to improve the endurance characteristics. Conventionally for floating-gate devices, channel hot electron injection (CHEI) and hot hole injection (HHI) mechanism are employed to program and erase the device, respectively. CHEI has better speed performance. Nevertheless, the hot electrons are injected into POLY1 layer from the channel region near the drain, and may cause defects like trapped charges in the oxide and interface states, so the threshold voltage window narrows with program/erase (P/E) cycles. For SONOS devices, channel induced secondary electron injection (CHISEL) can be an alternative approach for programming, while HHI is used for erasing. CHISEL programming method proceeds by negatively biasing the substrate. As a result, more hot electrons and secondary electrons are generated and the programming speed is effectively improved. CHISEL thus provides better programming efficiency than CHEI. However, CHISEL will also result in interface state damage, so that subthreshold swing (SS) and mobility (Gm) are degraded after P/E cycling.

2-1.3 Charge-tapping type is More Competitive to Floating Gate Structure

Charge-tapping type is superior to floating gate structure in the following aspect:

- Tunneling oxide
  - Thickness can not be thinner than 8nm.
  - Defects generated in oxide
  - SILC causes poor reliability
- Blocking oxide
  - Thickness is non-scalable
  - Gate electron injection if too thin
  - Poor coupling ratio if too thick
  - Worse erase efficiency
- Lateral scaling limit
  - Floating gate coupling

Charge-trapping type is the solution for Floating Gate Memory, stored charges in trapping layer spatially isolated within insulator which avoiding charges leakage with individual leak path. For vertical and horizontal direction, charge-trapping type has good scalability compatible to ITRS of NVM (in Fig.2-5).

2-2 Motivation to study MONOS Flash memory

In general, poly-Si as top electrode is widespread applied in ONO charge trapping type of non-volatile memory because poly gate is used in a lot of mature process technology node. Poly-Si is utilized in these roles because of its compatibility with subsequent high temperature processing (temperature from 250-1100^{o}C), its excellent interface with thermal SiO_2 (low concentration of interface states). On the other hand, poly gate have poly gate depletion, and polysilicon exhibits significantly higher

resistivity than single-crystal silicon (except at very high dopant concentrations, where the resistivity is only slightly greater). This is primarily due to two mechanisms:

- Under heat treatment some of the dopant atoms segregate to the grain boundaries, where they do not effectively produce free carriers.
- The grain boundaries are rich in incomplete bonds, and these cause some free carriers to be trapped at the grain boundaries.

The influence of various types of metal nitride gate electrodes, i.e., tantalum nitride, molybdenum nitride, and tungsten nitride, on electrical characteristics of metal-oxide-semiconductor capacitors with hafnium oxide as the gate dielectric material has been studied. The result shows that both the physical and electrical properties of the high-κ gate stack are influenced by the gate electrode materials and the post-metal-annealing temperature. Both the physical thickness and equivalent oxide thickness of the gate stack These metal nitride electrodes are suitable for n-channel metal-oxide-semiconductor device applications increased after the high-temperature N_2 annealing step. The interface state density and oxide trap density of the high-κ gate stack were also reduced by the high-temperature N_2 annealing step. Molybdenum nitride (MoN) is quite stable (to maintain thermal stability up to a 1000^{o}C RTA) because the activation energy of metal and nitrogen is relatively low. Molybdenum is bonded tightly within nitride and no obvious diffuse was observed in fabricated devices. However, MoN gate on high-κ HfO_2 shows a significant shift of flat band voltage (V_{FB}) toward the mid-gap of Si due to the interface reaction between the MoN and HfO_2 at the high temperature. Therefore, we study on MONOS rather than SONOS.

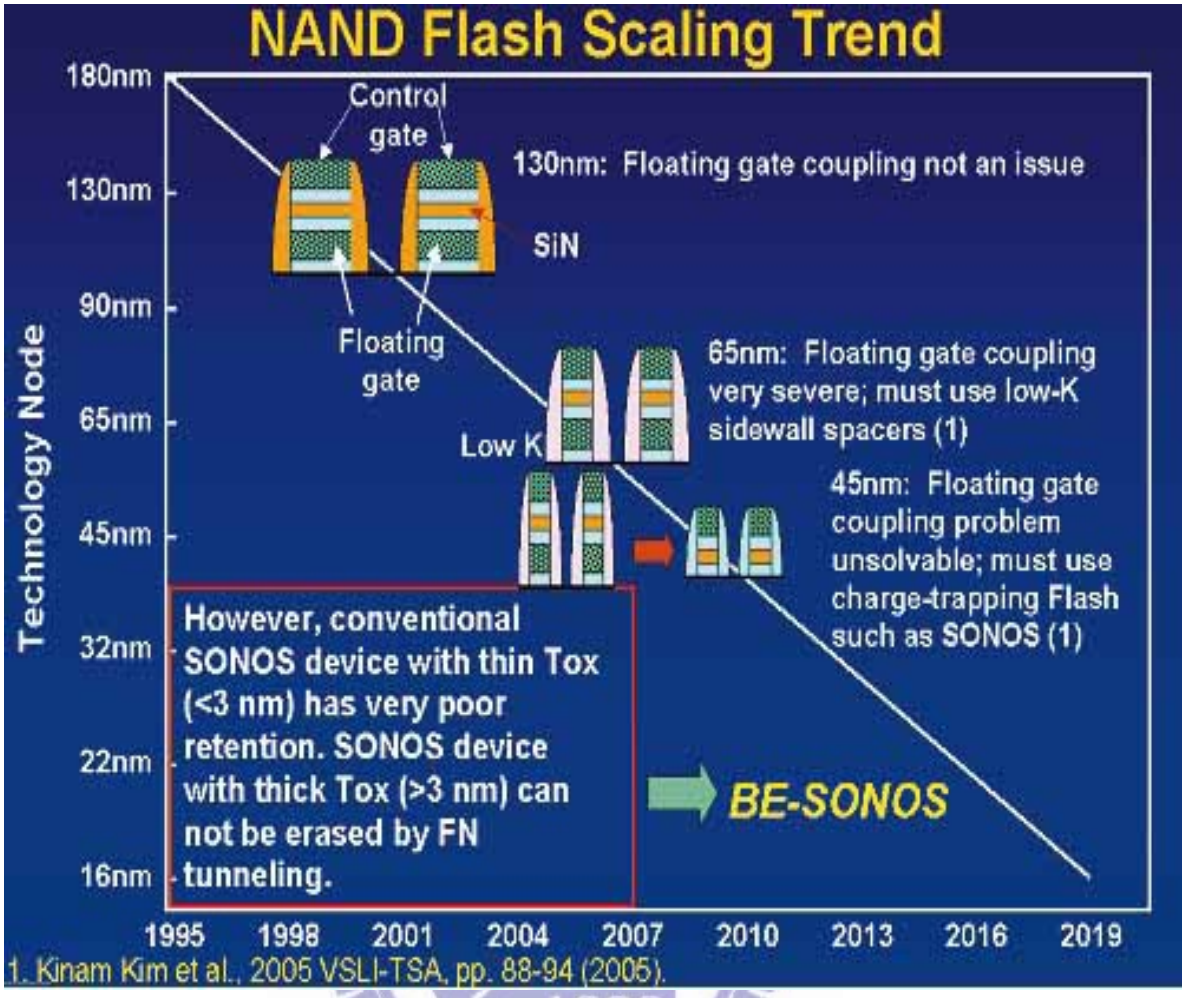


Fig.2-1 Scaling trend for flash memory device development.

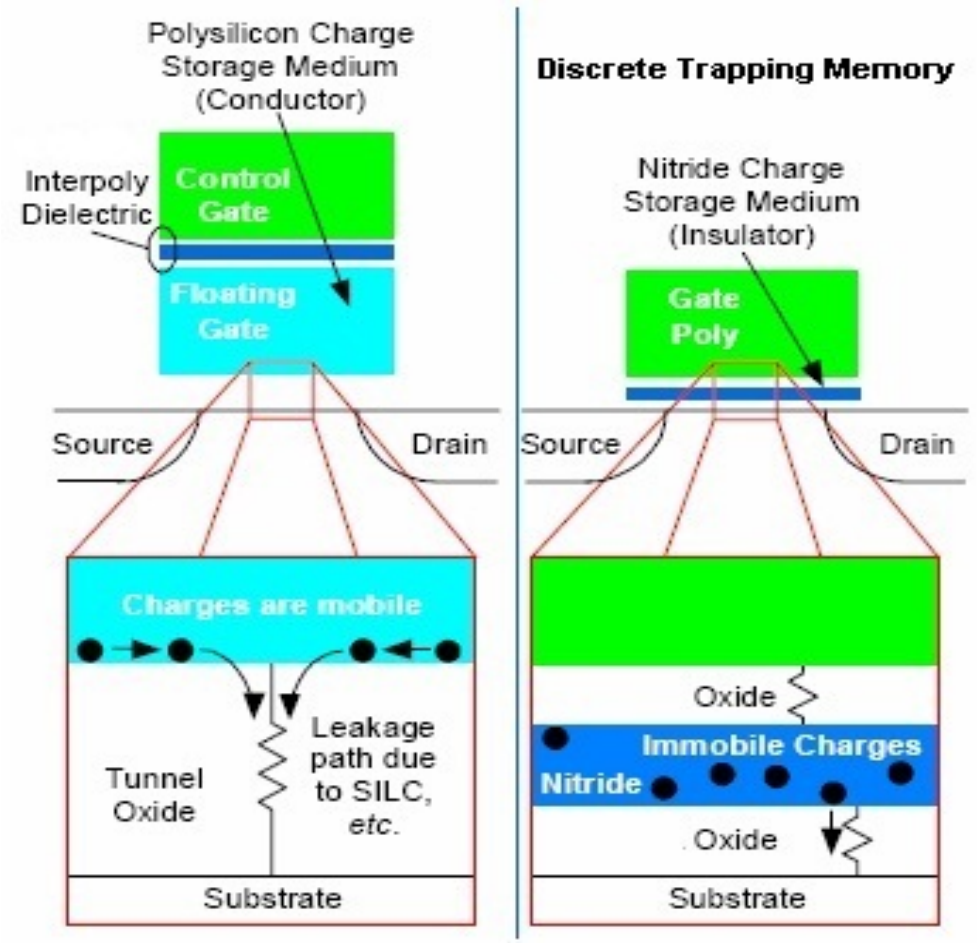


Fig.2-2 Diagrams illustrating physical structures of floating-gate and discrete trapping (SONOS) devices [2.6].

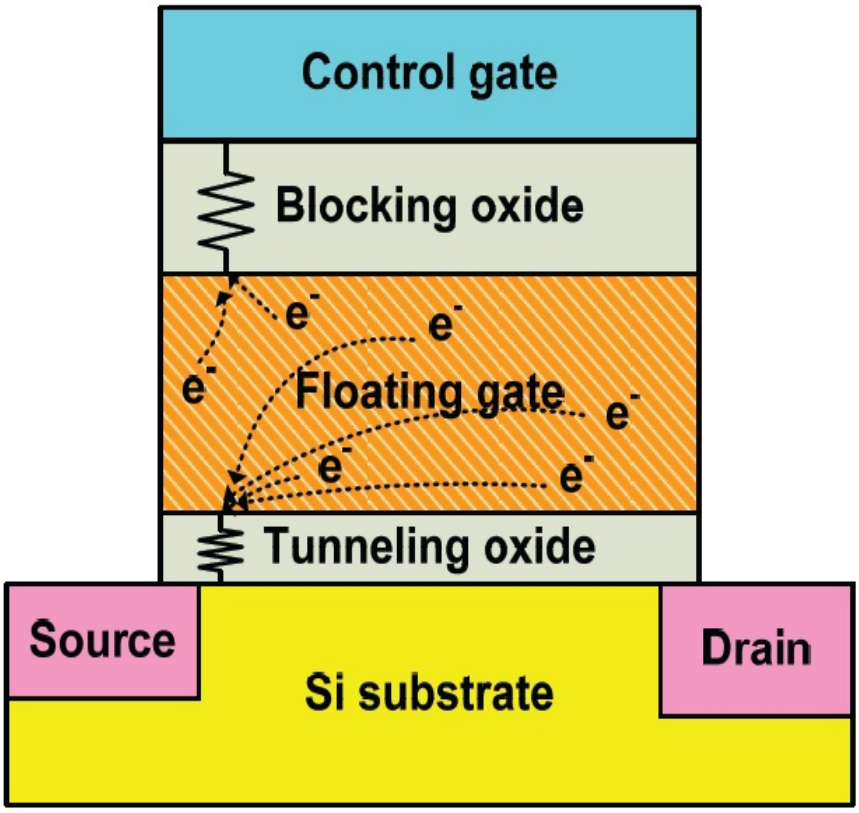


Fig.2-3 Basic concept of floating gate (FG) non-volatile memory.

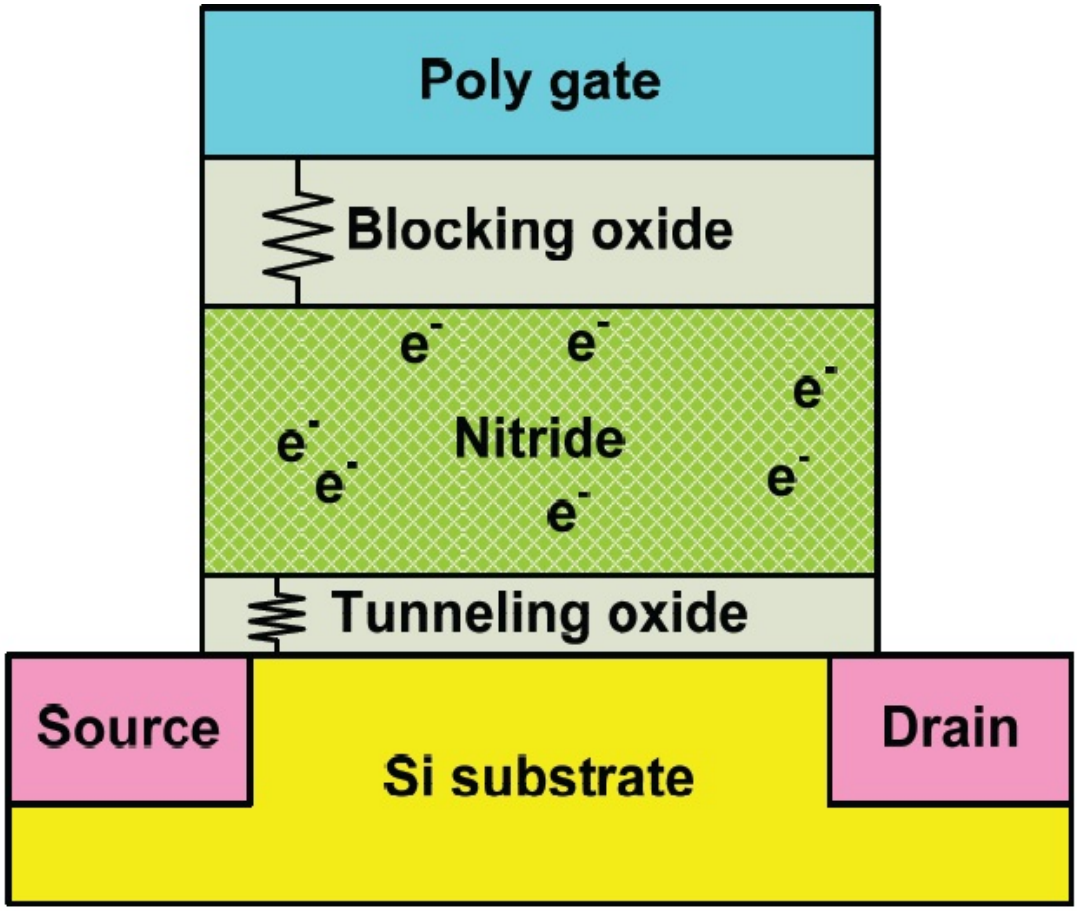


Fig.2-4 Basic concept of SONOS non-volatile memory.

Year of Production	2014	2015	2016	2017	2018	2019	2020
SONOS/NROM technology – F (nm) [34]	32	28	25	23	20	19	18
SONOS/NROM cell size – area factor a in multiples of F^2 [35]	6.5	6.5	7	7	7	7	7
SONOS/NROM typical cell size (μm^2) [36]	0.007	0.005	0.004	0.0037	0.003	0.0025	0.002
SONOS/NROM maximum number of bits per cell ((physical 2-bit/cell) x MLC) [37]	4	4	4	4	4	4	4
SONOS/NROM area per bit (μm^2) [38]	0.0018	0.0013	0.0011	0.0009	0.0007	0.0006	0.0005
SONOS L_g-stack (physical – μm) [39]	0.15	0.15	0.14	0.14	0.14	0.13	0.13
SONOS highest W/E voltage (V) [40]	5.0–5.5	5.0–5.5	4.5–5.0	4.5–5.0	4.0–4.5	4.0–4.5	4.0–4.5
SONOS/NROM I_{read} (μA) [41]	23–33	22–32	21–31	21–31	20–30	20–30	20–30
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
SONOS/NROM tunnel oxide thickness (nm) [42]	3	3	2.5	2.5	2.5	2	2
SONOS/NROM nitride dielectric thickness (nm) [43]	4	4	4	4	4	4	4
SONOS/NROM blocking (top) oxide or dielectric thickness (nm) [44]	6	6	5	5	5	5	5
SONOS/NROM endurance (erase/write cycles) [45]	1.00E+08	1.00E+08	1.00E+09	1.00E+09	1.00E+09	1.00E+09	1.00E+09
SONOS/NROM nonvolatile data retention (years) [46]	10–20	10–20	10–20	10–20	10–20	10–20	10–20

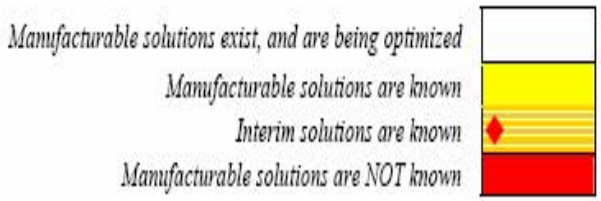


Fig.2-5 The requirements for NV memory (the international technology roadmap for semiconductors: 2006 update).

Chapter 3

A Novel Program-erasable High-κ HfO_2-ZrO_2/Si MIS Capacitor

3-1 Introduction

Capacitors are essential devices for various analog, RF and DRAM functions [3.1]-[3.8] in circuits. It is also desirable to have a program-erasable capability. This is especially important for RF ICs where process variations can shift the resonance frequency of LC tank away from designed values, creating impedance mismatches and bandpass frequency differences [3.9]. Program-erasable capacitors can also extend the data retention for DRAMs leading to less frequent re-flashing cycles. In this dissertation , we propose and demonstrate a MIS capacitor on Si using interactive high-κ materials of Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) as dielectric, as Fig3.1, which exhibits the program-erase function as well as good data retention. The structure has a programmable and erasable C-V character. In contrast, we execute and demonstrate a MIS capacitor on Si using a single layer of high-κ HfO_2 as dielectric(in Fig.3-2), which shows the program-erase function. The single layer high-κ capacitor has a and erasable C-V character.

3-2 Experimental

The MIS devices were formed by sputter-depositing a ~18 nm thick single layer HfO_2 on Si substrate which is processed RCA clean. Then, the dielectric layer suffered suffered post-deposition annealed at $600^{O}C$ for 5 min in a furnace under N_2 ambient. Eventually, I sticked shallow mask on wafer tightly, metal electrode was deposited by

PVD and patterned after removing shallow mask. (in Fig.3-2)

For comparison, the MIS capacitors were fabricated using high-κ dielectric process on 4-in 1-10Ω-cm p-type Si wafer. After standard pre-gate clean, moving some particles and native oxide on the surface away, the interactive layer (in Fig.3-1) of 18 nm was deposited by physical vapor deposition (PVD) system. This layer first deposits HfO_2 of 2nm then deposits ZrO_2 of 2nm, repeats it with four cycles, eventually deposits HfO_2 of 2nm. And then separate into two classifications. One is post-deposition annealed (PDA) at $600^{O}C$ for 5 min in a furnace under O_2 ambient, another is post-deposition annealed (PDA) at $600^{O}C$ for 5 min in a furnace under N_2 ambient. Finally, MoN metal was deposited by PVD and then patterned by shallow mask to form top electrode with capacitor area of circle with 140μm diameter.

All the C-V characteristics were measured by HP4284A at 1 MHz.

3-3 Results and discussion

Fig.3-3 show the *C-V* characteristics of the single high-κ HfO_2 layer MIS capacitors processed by PDA at $600^{o}C$ flowed in N_2 ambient. We apply voltage on MoN electrode and erase the high-κ HfO_2 /Si MIS capacitors from -13V to 13 Volt, and program the high-κ HfO_2-ZrO_2/Si MIS capacitors from 13V to -13 V, and it just has 3.5V memory window. the holes tunnel in HfO_2 layer to recombine electrons and eliminate the V_{FB} in erase operation, On the contrary, the electrons tunnel in HfO_2 layer and V_{FB} elevate. The value of capacitance density is 9.3 $fF/\mu m^2$, we can calculate the κ value is 19. There are three kind of leakage mechanism. MoN metal Gate has large work function so that electron will suffer a high barrier when the external voltage is small. In this way, electrons can not transport to dielectric film, called Schottky Emission. We can use following equation to represent.

$$J\alpha \exp\left[\frac{\gamma E^{1/2} - \nu_b}{kT}\right] \quad \text{(Eq.3-1)}$$

$$\ln(J)\alpha \frac{\gamma}{kT} E^{1/2} - \frac{\nu_b}{kT} \quad \text{(Eq.3-2)}$$

Poole-Frenkel Effect, it means there have charges be trapped in dielectric layer. The Poole-Frenkel effect is the lowering of a Coulombic potential barrier when it interacts with an electric field, and is usually associated with the lowering of a trap barrier in the bulk of an insulator, as shown in Fig.3-4. We can use following equation to represent.

$$\frac{J}{T^2}\alpha \exp\left[\frac{\gamma E^{1/2} - \nu_b}{kT}\right] \quad \text{(Eq.3-3)}$$

$$\ln\left(\frac{J}{T^2}\right)\alpha \frac{\gamma}{kT} E^{1/2} - \frac{\nu_b}{kT} \quad \text{(Eq.3-4)}$$

If the external bias is big enough, F-N tunneling will decide the leakage mechanism. We can draw ln(J)-$E^{1/2}$ and ln(J/T^2)-$E^{1/2}$ relation, and calculate the value of ν_b is -0.78 (the intercept of y-axis in Fig.3-5(b) multiplied kT), knowing that the charges was not catch to deep level. To measure retention, I triggered a constant voltage of +10V for program during the pulse length of 1s to the MoN electrode, then, I measured the C-V curves and extracted V_{FB} shift pass through times. Repeat the same action for erase, the V_{FB} became larger. Figs.3-6(a) and (b) show poor retention for HfO_2 single layer, therefore, improving the trapping layer by interactive structure.

HfO_2 and ZrO_2 these two materials can't endure temperature more than 35^OC when programming process. If depositing them by E-Gun system, temperature is hard to control and the dielectric film may be destroyed. Therefore, I deposit them by sputter system.

Due to the κ value of Hafnium oxide (HfO_2) is 25 and Zirconium oxide (ZrO_2) is

35, we can elementarily count up ideal capacitance density. In Eq.3-5, ε_0 is permittivity, A is the capacitor area and t is the thickness of capacitor.

$$C = \frac{k \times \varepsilon_0 \times A}{t} \quad \text{(Eq.3-5)}$$

Calculation of ideal capacitance density of interactive structure in the following equations:

$$C = \left\{ \left(\frac{8.851 \times 10^{-14} \times 25}{20 \times 10^{-8}} \right)^{-1} \times 5 + \left(\frac{8.851 \times 10^{-14} \times 35}{20 \times 10^{-8}} \right)^{-1} \times 4 \right\}^{-1} \quad \text{(Eq.3-6)}$$

$$= 1.4 \times 10^{-6} \left(\frac{F}{cm^2} \right) = 14 \left(\frac{fF}{\mu m^2} \right) \quad \text{(Eq.3-7)}$$

$$= \frac{8.851 \times 10^{-14} \times 3.9}{EOT} \quad \text{(Eq.3-8)}$$

By Eqs.3-6 and 3-7, EOT is 2.4nm for MIS which mix up Zirconium oxide (ZrO_2) to Hafnium oxide (HfO_2), it is obviously increasing the EOT.

Figs.3-7 and 3-8 show the measured C-V hysteresis of interactive dielectric MoN/HfO_2-ZrO_2/Si capacitors measuring by HP4284. We apply voltage on MoN electrode and erase the high-κ HfO_2-ZrO_2/Si MIS capacitors from -13V to 13 Volt, and and program the high-κ HfO_2-ZrO_2/Si MIS capacitors from 13V to -13 V. It shows large memory window character of 4.7V and the value of capacitance density is 12.2 $fF/\mu m^2$ whose dielectric is post-deposition annealed in O_2 ambient at 600°C for 5 min. The interactive dielectric HfO_2-ZrO_2 after post-deposition annealed in N_2 ambient at 600°C for 5 min shows 4.3V memory window and the value of of capacitance density is 11.5 $fF/\mu m^2$. The value of capacitance density elevates. Memory window increasing may be due to increasing charges trapped in dielectric. Single layer has small memory window, the recipes of going through PDA at 600°C flowed N_2 ambient just exhibit 3.5V P/E shift by contrast. Double-layer

Double-layer structure lattice was recombined by PDA process and two high-κ materials could be mix together. Although HfO_2 and ZrO_2 have similar band-gap and band-diagram, ZrO_2 in HfO_2 increase the κ value (the κ value of ZrO_2 and HfO_2 is 35 and 25 respectively) and decrease effective oxide thickness. The high capacitor density density is especially important for backend capacitor due to the very thick equivalent-oxide thickness (EOT) > 5 nm and hence the low leakage current. On the other hand, low leakage current is one of the most important factors for high-κ gate dielectric with typical EOT ≤2 nm[3.10]-[3.16].

Fig.3-9 shows the schematic band diagram of metal-gate/HfO_2-ZrO_2/Si capacitor. The possible erase mechanism may arise from the smaller bandgap (EG ~6.0 eV), small bandgap has more probabilities to catch electrons. This could permit hole injection or electron tunneling out from the high density of trap states, electrons tunnel from Si-sub to trapping layer when metal gate applied positive bias, and hole injection recombines electron trapped deeply in dielectric as metal applied negative bias (Fig.3-10).

In Fig.3-11(b), the value of ν_b PDA in O_2 ambient at 600°C for 5 min in Poole-Frenkel Effect is -0.971, and the value of ν_b PDA in N_2 ambient at 600°C for 5 min in Poole-Frenkel Effect is -0.931 calculated by intercept of Fig.3-12(b) multiply to the value of kT. Compare modulus of ν_b, PDA in O_2 ambient has excellent ability to catch charges in deep position of trapping layer.

In addition to trapping position, retention is one of the important issue for discuss interactive HfO_2-ZrO_2 layer. On the whole, a device revealing good retention should have slow velocity to P/E. Figs. 3-13 and 3-14 exhibit the research of interactive HfO_2-ZrO_2. It says that processed PDA in O_2 ambient at 600°C for 5 min shows shows good retention for ten years and has excellent speed in erase

operation. PDA in N_2 ambient at 600^{o}C for 5 min revealed inferior retention for ten years and the P/E speed is slow because saturation need more time.

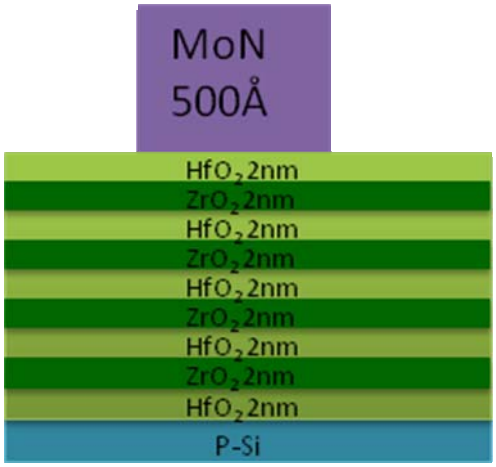


Fig.3-1 Cross section view of novel program-erasable interactive structure high-κ HfO_2-ZrO_2 MIS capacitors.

Fig.3-2 Cross section view of novel program-erasable high-κ HfO_2 MIS capacitors.

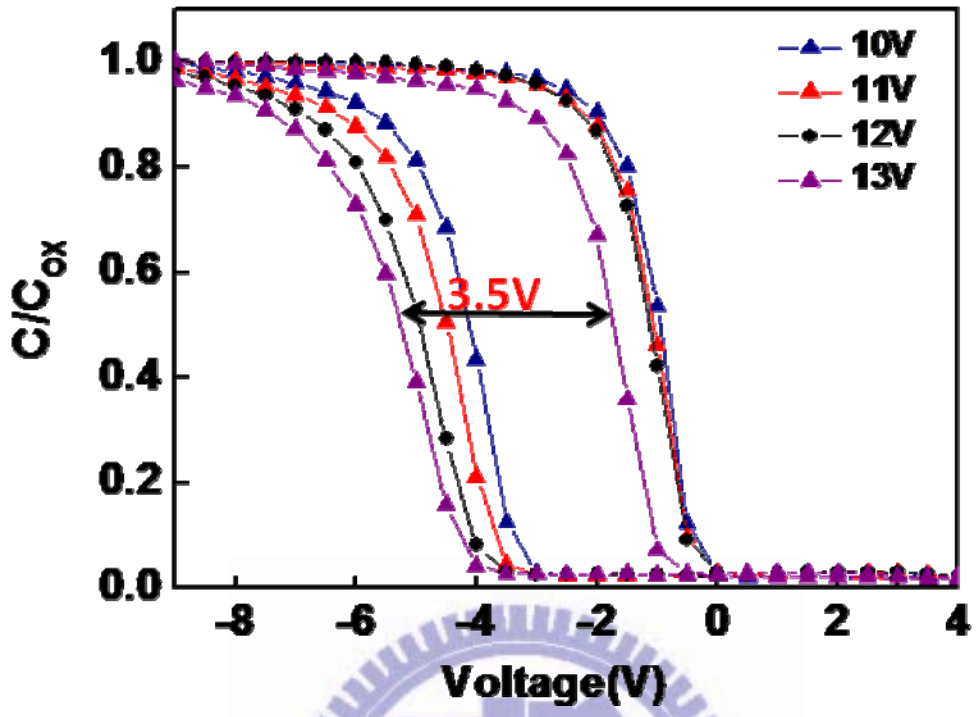


Fig.3-3 The measured C-V hysteresis of high-κ HfO_2 MIS capacitors after Post-deposition annealing (PDA) in N_2 ambient at 600°C for 5 min.

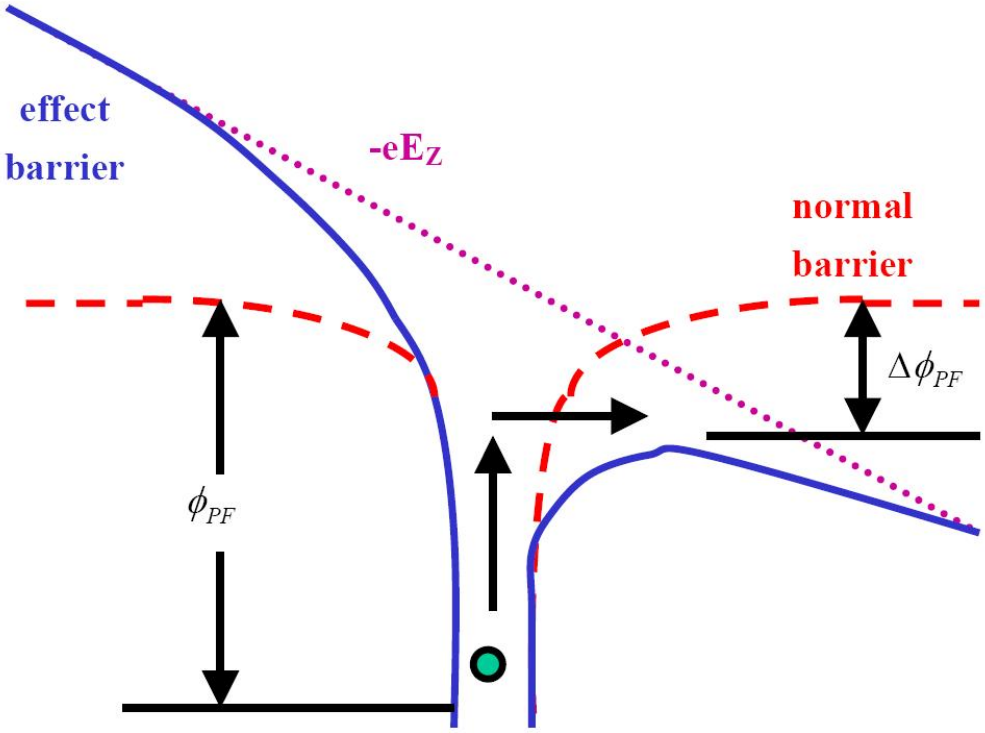


Fig.3-4 Mechanism of Poole-Frenkel effect. The solid line represents the Coulombic barrier without a field. The dashed line shows the effect of an electric field on the barrier. The slope of the dash-dot line is proportional to the applied field.

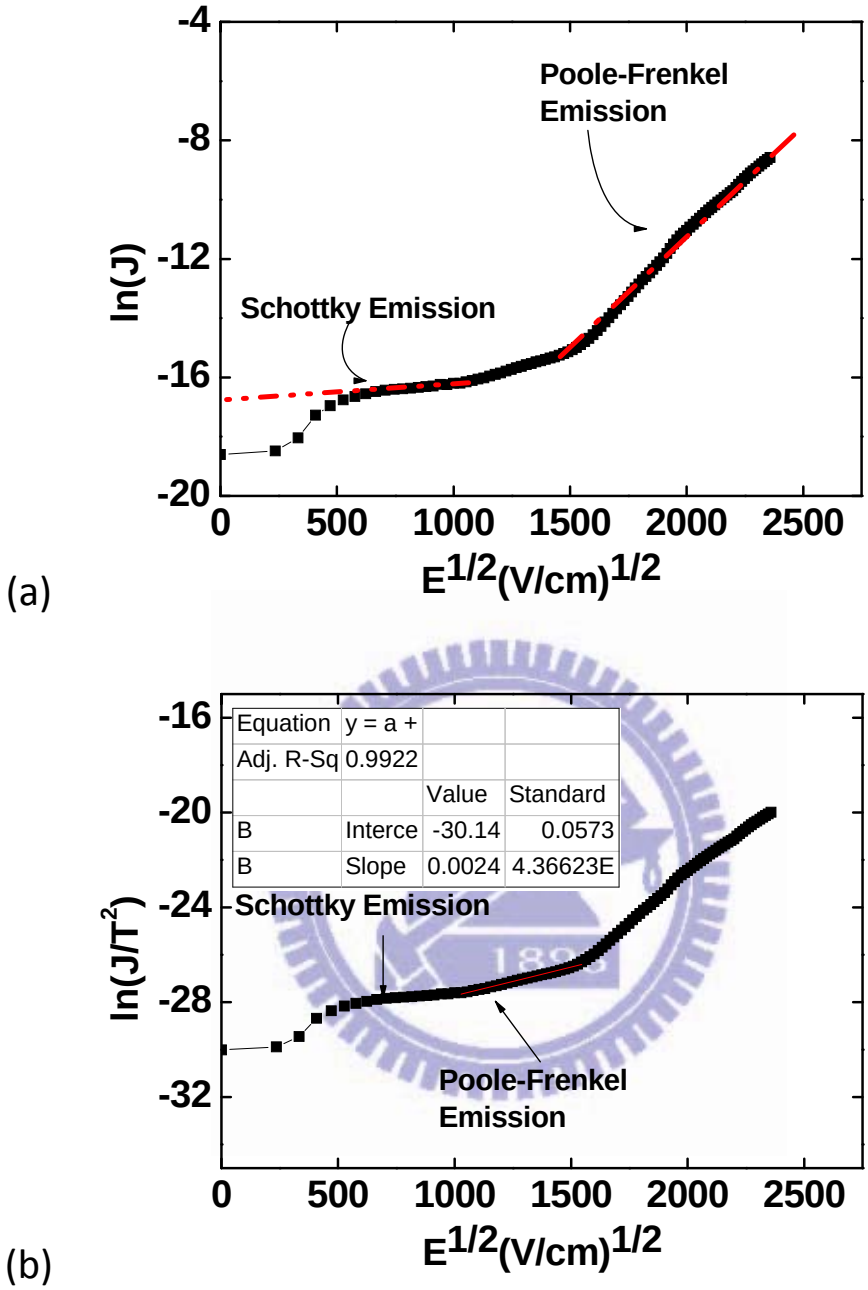
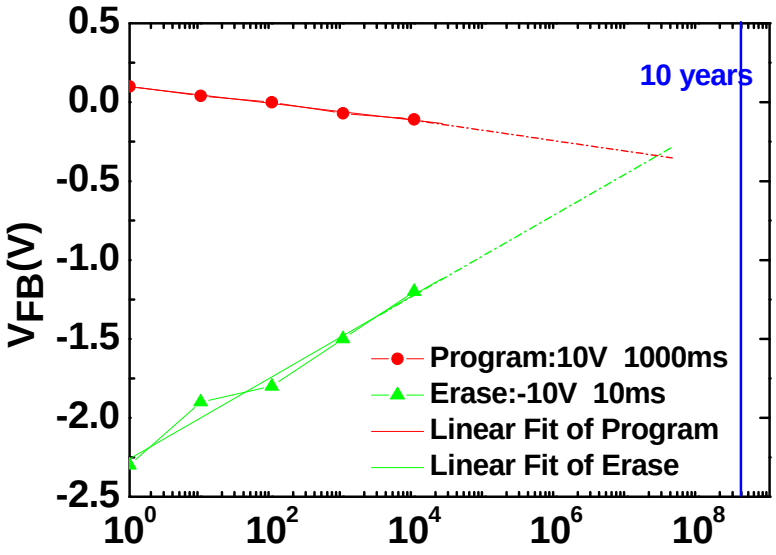
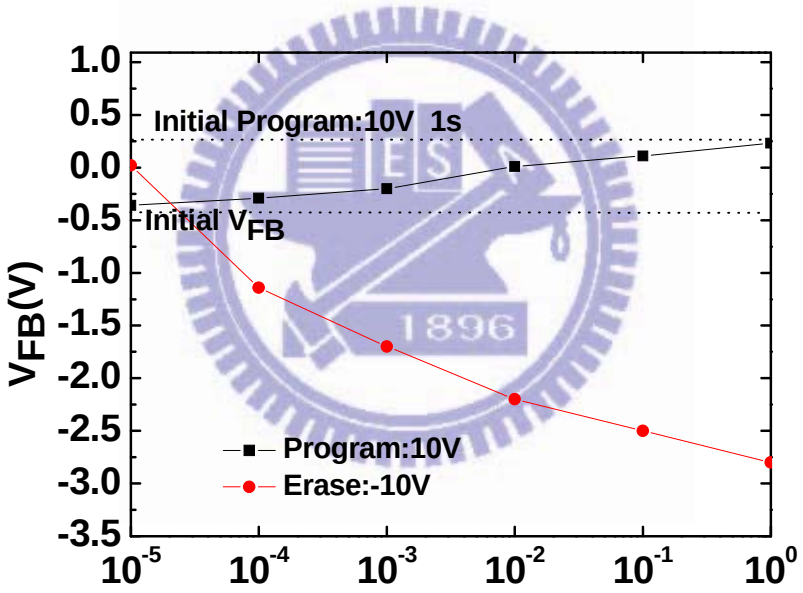


Fig.3-5 The ln(J)-$E^{1/2}$ and ln(J/T^2)-$E^{1/2}$ plots, using the measured J-V of a MoN/HfO_2/Si MIS device, where the electron injection is from the Si.(a) Calculated data using Schottky Emission (SE) and (b) Frenkel-Poole (FP) conduction models are included.



(a)



(b)

Fig.3-6 (a) The retention characteristics of V_{FB} from the C-V curves programmed or erased at +10V or -10 V,(b) The P/E characteristics for HfO_2 MIS capacitor.

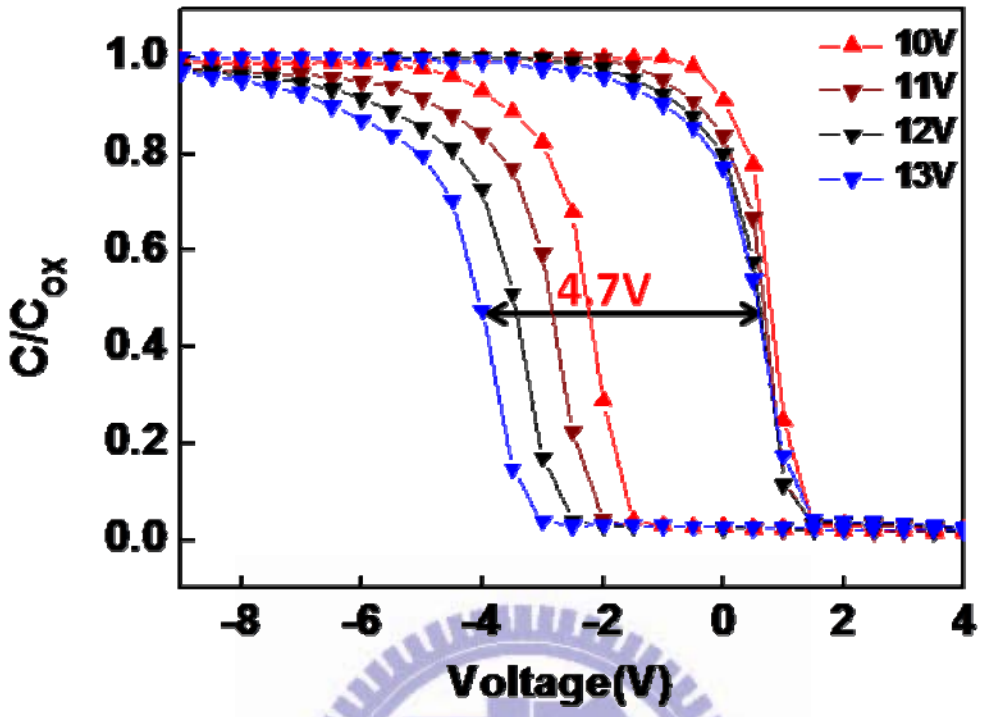


Fig.3-7 The measured C-V hysteresis of interactive structure high-κ HfO_2-ZrO_2 MIS capacitors after Post-deposition annealing (PDA) in O_2 ambient at 600°C for 5 min.

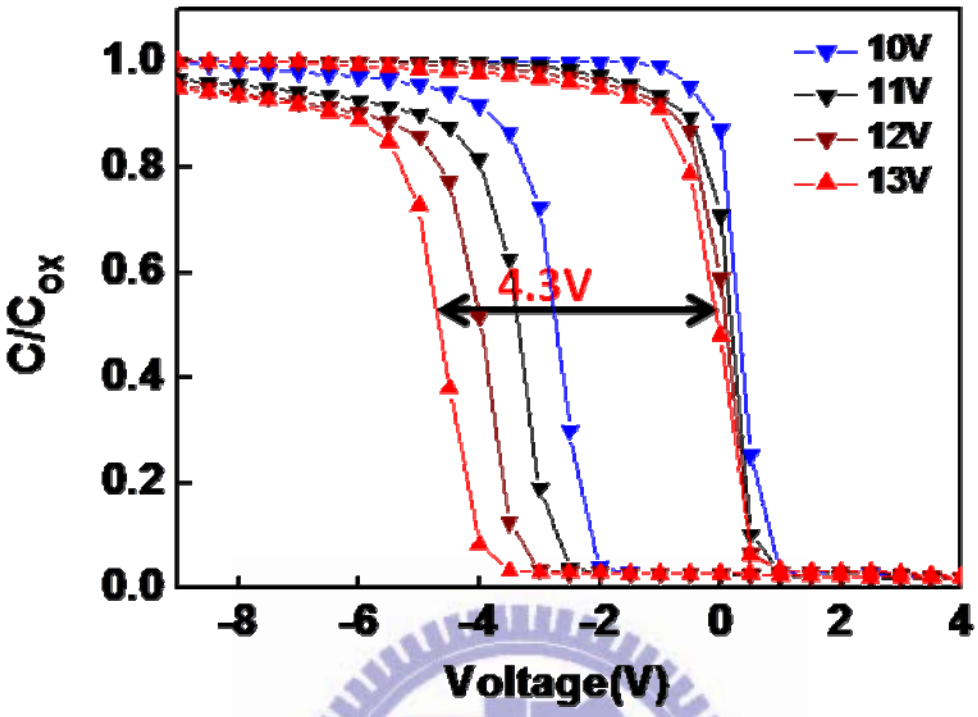


Fig.3-8 The measured C-V hysteresis of interactive structure high-κ HfO_2-ZrO_2 MIS capacitors after Post-deposition annealing (PDA) in N_2 ambient at 600°C for 5 min.

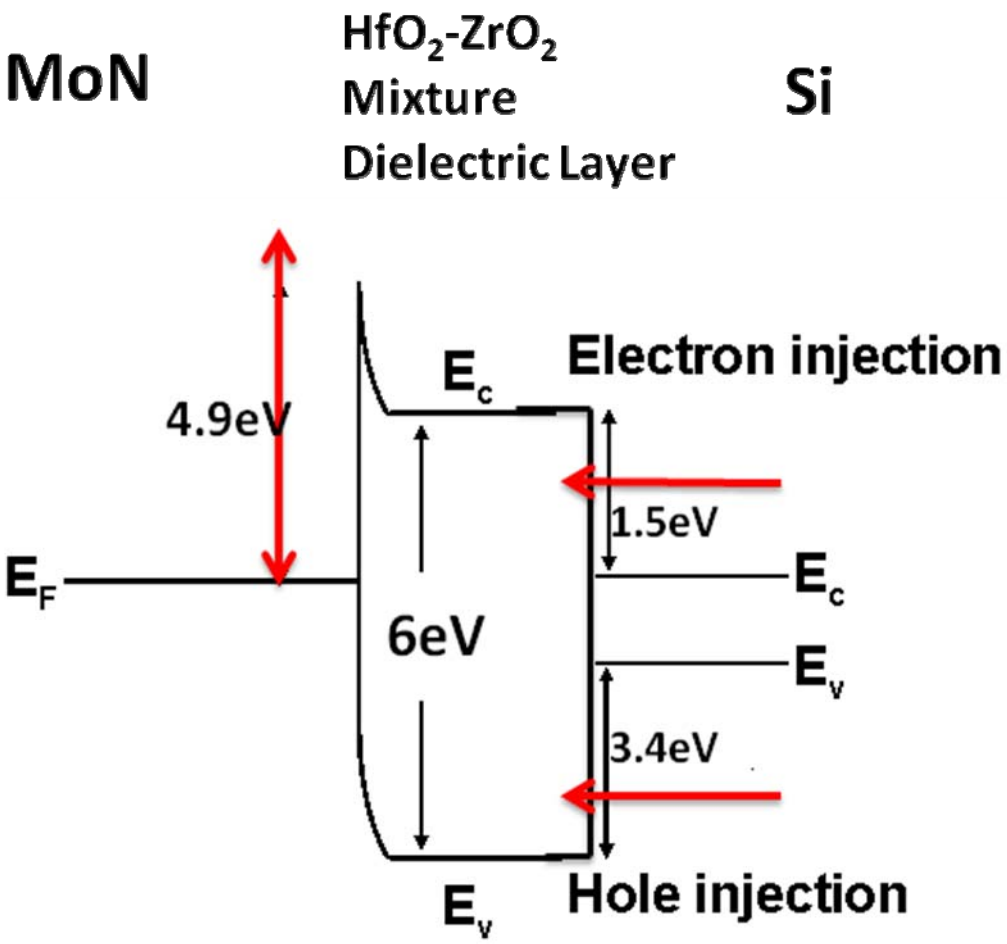


Fig.3-9 The schematic band diagram of the MoN metal gate/high-κ HfO_2-ZrO_2/Si MIS capacitor.

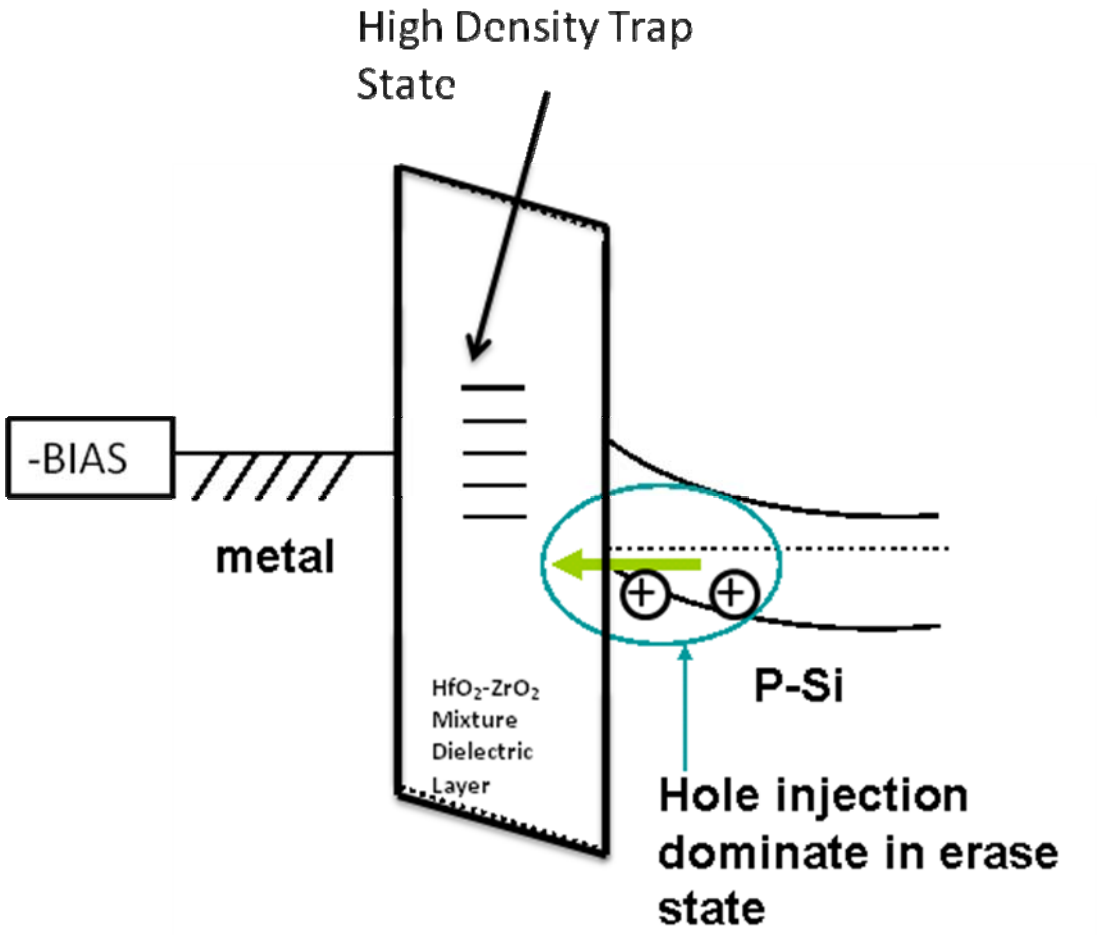
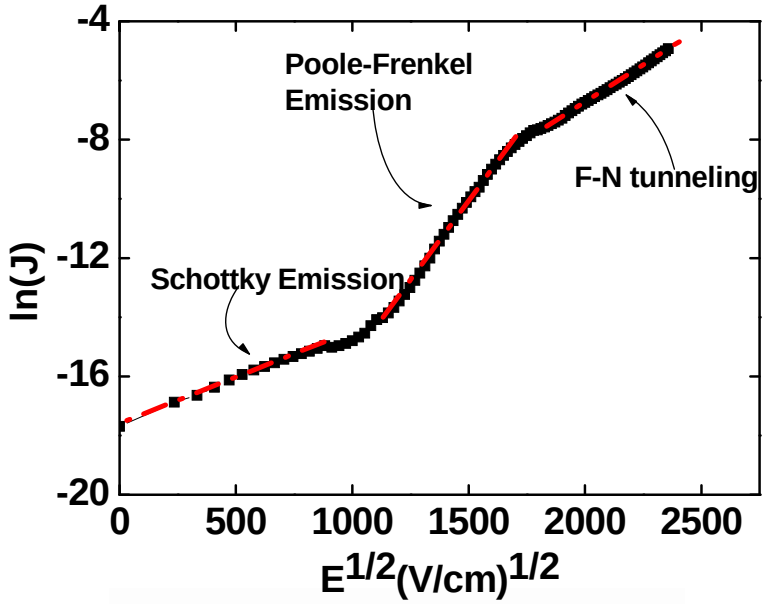
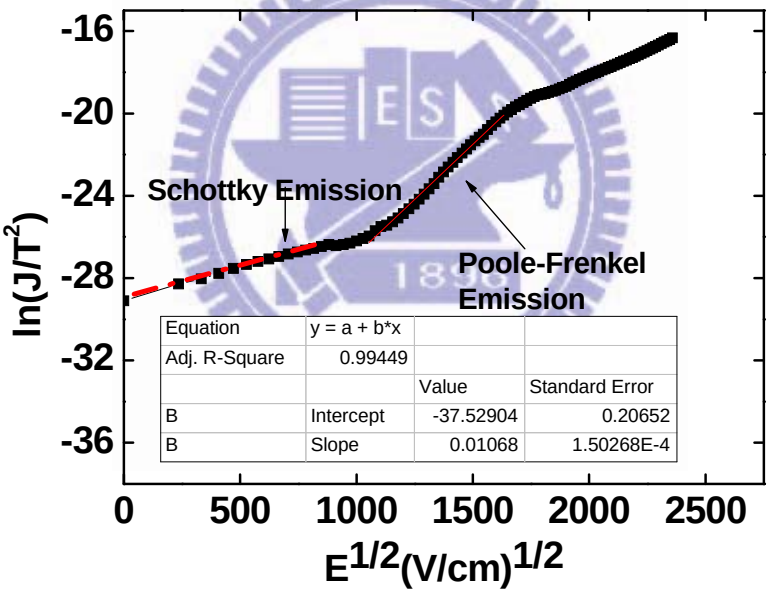


Fig.3-10 The schematic band diagram of the metal-gate/high-κ dielectric/Si MIS capacitor in erase state.

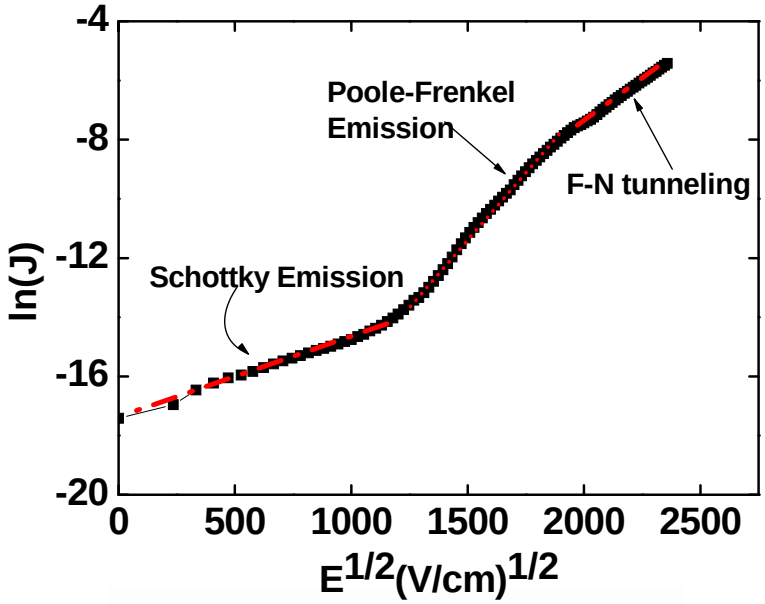


(a)

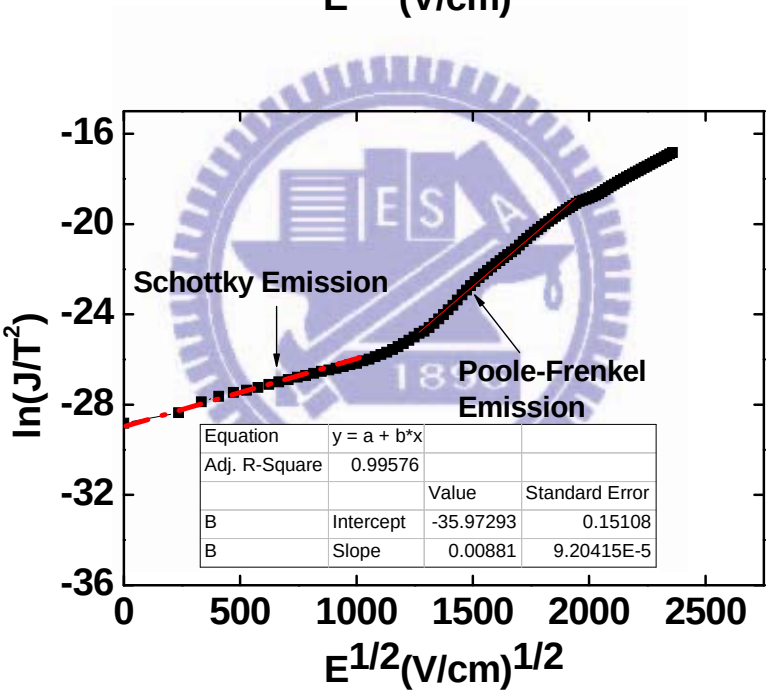


(b)

Fig.3-11 The $\ln(J)$-$E^{1/2}$ and $\ln(J/T^2)$-$E^{1/2}$ plots, using the measured J-V of a MoN/HfO_2-ZrO_2/Si MIS processed PDA in O_2 ambient at 600°C for 5 min, where the electron injection is from the Si.(a) Calculated data using Schottky Emission (SE) and (b) Frenkel-Poole (FP) conduction models are included.

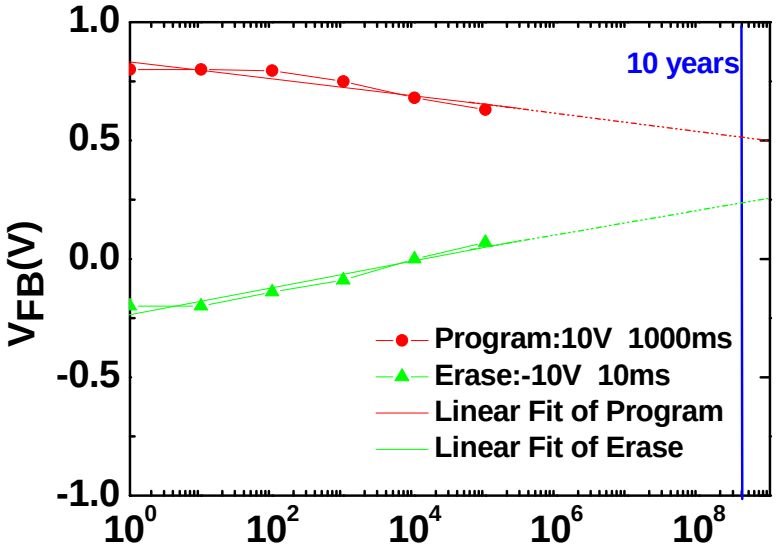


(a)

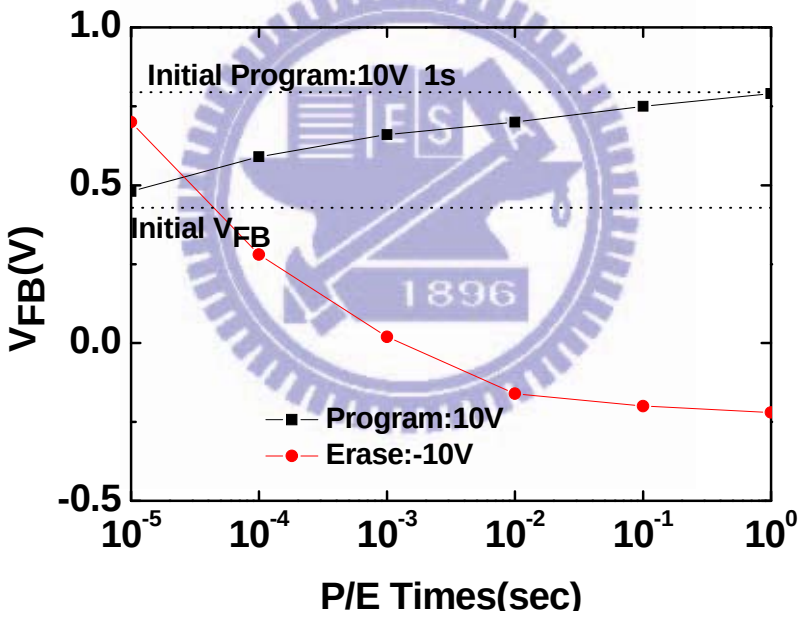


(b)

Fig.3-12 The $\ln(J)$-$E^{1/2}$ and $\ln(J/T^2)$-$E^{1/2}$ plots, using the measured J-V of a MoN/HfO_2-ZrO_2/Si MIS processed PDA in N_2 ambient at 600°C for 5 min, where the electron injection is from the Si.(a) Calculated data using Schottky Emission (SE) and (b) Frenkel-Poole (FP) conduction models are included.



(a)



(b)

Fig.3-13 (a) The retention characteristics of V_{FB} from the C-V curves programmed or erased at +10V or -10 V (b) The P/E characteristics of MoN/HfO_2-ZrO_2/Si MIS processed PDA in O_2 ambient at 600°C for 5 min.

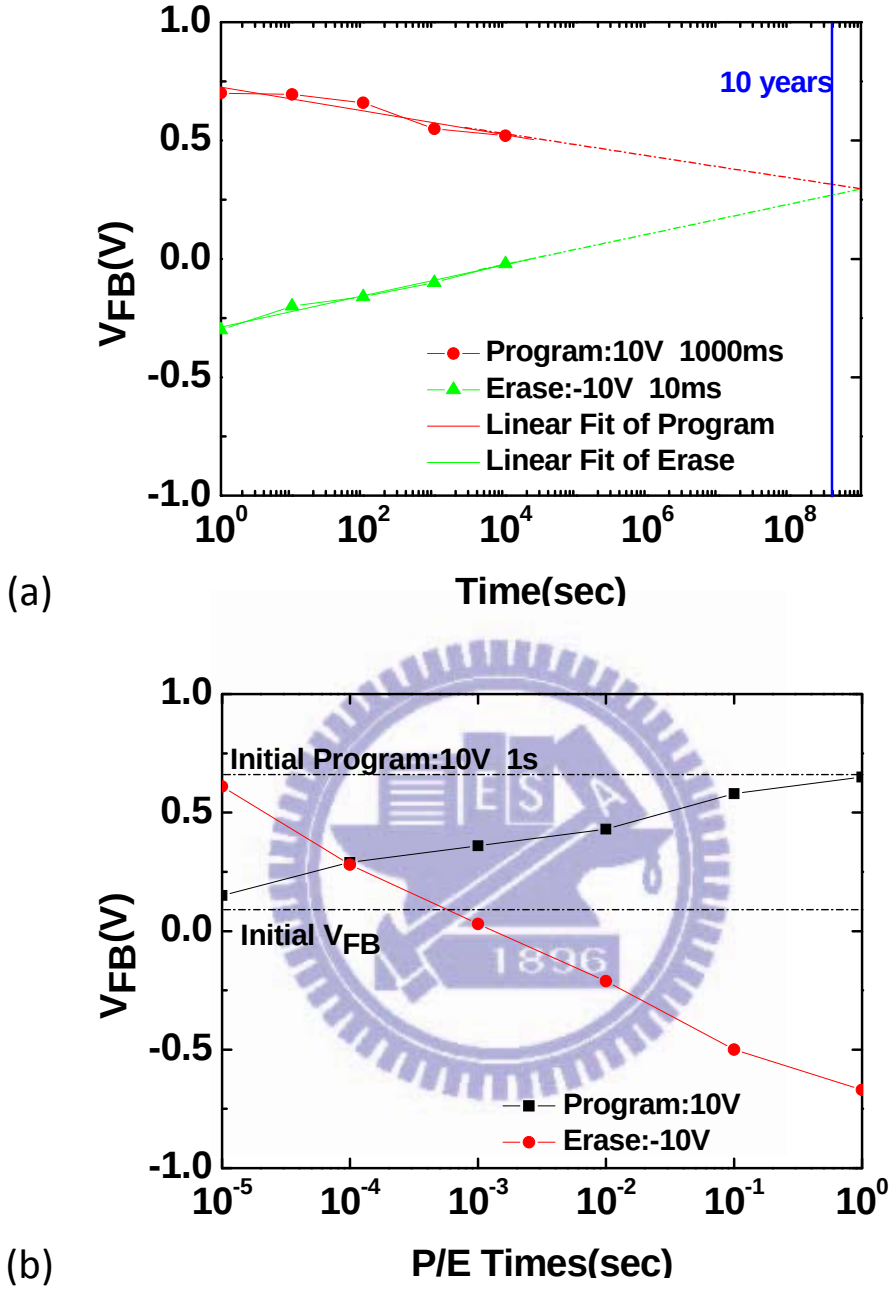


Fig.3-14 (a) The retention characteristics of V_{FB} from the C-V curves programmed or erased at +10V or -10 V (b) The P/E characteristics of MoN/HfO_2-ZrO_2/Si MIS processed PDA in N_2 ambient at 600°C for 5 min.

Chapter 4

Low Voltage SiO_2/HfO_2-$ZrO_2/SiO_2/MoN$ MONOS Memory

4-1 Introduction

Poly-Si/SiO_2/Si_3N_4/SiO_2/Si (SONOS) devices are promising for non-volatile memory applications as scaling decreases below 50 nm. This is because of the merit of charge storage in discrete traps within the Si_3N_4, which prevents charge leakage through a single oxide defect, as compared with the conventional poly-Si floating gate memory case. By replacing the poly-Si in SONOS with a high work-function metal-gate (MONOS), further improvements of the erase performance can be achieved by decreasing the electron injection over the gate. However, one difficulty in SONOS or MONOS is the small conduction band discontinuity (ΔE_C) of only 1.1 eV at the Si_3N_4/SiO_2 interface [4.1], which causes charge leak out from shallow trap levels near E_C of Si_3N_4. In contract, a conventional poly-Si floating gate device has a much deeper energy of ~3.15 eV for storage of charge. Therefore, the high temperature retention is a serious concern for a shallow trap energy MONOS device that uses a Si_3N_4. To address this requires the use of a thick SiO_2 tunnel layer to improve the charge storage, but unfortunately this leads to a performance degradation of increased program/erase (P/E) voltage and write speed. This is contrary to the scaling trend indicated in the International Technology Roadmap for Semiconductors (ITRS). To overcome this problem, we have previously proposed using a novel Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) interactive layer which has deeper ΔE_C than Si_3N_4. This improved the P/E voltage, and write speeds in such

deep-trap MONOS devices.

4-2 Experimental

The fabrication process of the MoN/SiO_2/HfO_2-ZrO_2/SiO_2/Si MONOS devices was similar to previous work. First, a 2.8 nm thick thermal SiO_2 was grown on a standard p-Si substrate. Then a 18 nm the interactive layer was deposited by physical vapor deposition (PVD) system. This layer first deposits HfO_2 of 2nm then deposits ZrO_2 of 2nm, repeats it with four cycles, eventually deposits HfO_2 of 2nm. And the dielectric layer suffered post-deposition annealed (PDA) at 600^{O}C for 5 min in a furnace under O_2 ambient. A 17 nm SiO_2 blocking oxide was formed by TEOS, included because of its good thermal stability at 1000^{o}C. Pull the wafer to PDA at 500^{O}C for 5 min in a furnace under O_2 ambient. A 50 nm MoN layer was added by sputtering and processed it by rapid thermal anneal at 450^{o}C in N_2 flow for 15 sec. After standard processing, the structure is as Fig.4-1. To pattern the MONOS, then photo-resist deposition and exposure by mask. The MoN top layer was etched by a high density plasma reactive ion etch (HDP-RIE) system using the gas mixture of BCl_3 and Cl_2 as the etchant source, and then remove photo-resist in acetone, showed in Fig.4-2.

4-3 Results and discussion

To promote the injection efficiency of electrons, the feasibility of using channel-initiated secondary electron (CHISEL) programming has been demonstrated in the MONOS devices [4.2]. CHISEL programming conditions and mechanisms are shown in Fig.4-3(a). The hot holes generated near the drain mainly drift toward the substrate and contribute to the substrate current (I_B). Some of these hot holes create electron-hole pairs by secondary impact ionization, which are greatly enhanced under a a high electric field by the applying of a reverse substrate bias (V_B <0). As a result,

the hot electrons caused by the secondary impact ionization tend to be injected into the MONOS structure and result in a wide distribution of trapped electrons, compared with the case of channel hot electron injection (CHEI) [4.3]. Fig.4-3(b) illustrates the energy band diagram for CHISEL programming operation. Owing to the reverse substrate bias, the conduction band (E_C) of the substrate is raised, and the substrate hot electrons can more easily tunnel through the oxide energy barrier (i.e., 3.1eV). Discrete charge storage memories (e.g., SONOS and nanocrystal) are typically erased using hot holes injection (HHI) [4.4], generated by band-to-band tunneling (BBT) in the channel and drain side overlap region. The HHI erasing conditions and mechanisms are shown in Fig.4-4(a). During the HHI erasing operation, the n-type SONOS device is turned off while maintaining a negative gate bias with positive drain and substrate biases. The energy band diagram [4.5] during the HHI erasing operation is shown in Fig.4-4(b). The increased positive bias in substrate causes a downward shift of valance band of the substrate and also helps promote charge trapping efficiency of the nitride layer [4.6]. My discussion replaced the Si_3N_4 to HfO_2-ZrO_2 layer own the same program and erase mechanism to above-mentioned.

We apply low voltage on MoN electrode and erase the MONOS capacitors from -6Volt to 6 Volt, and program the MONOS capacitors from 6Volt to -6Volt, and then raise the external voltage to erase the MONOS capacitors from -7Volt to 7 Volt, and program the MONOS capacitors from 7Volt to -7Volt, continuously to 8Volt. In Fig.4-5, the *C-V* hysteresis window of 4.6V, 5.2V and 7 V was measured respectively. Low leakage current exhibits the blocking oxide has good quality to isolate electrons as Fig.4-6.

Fig.4-1 Cross section view of MoN/SiO_2/HfO_2-ZrO_2/SiO_2/Si structure which was not patterned.

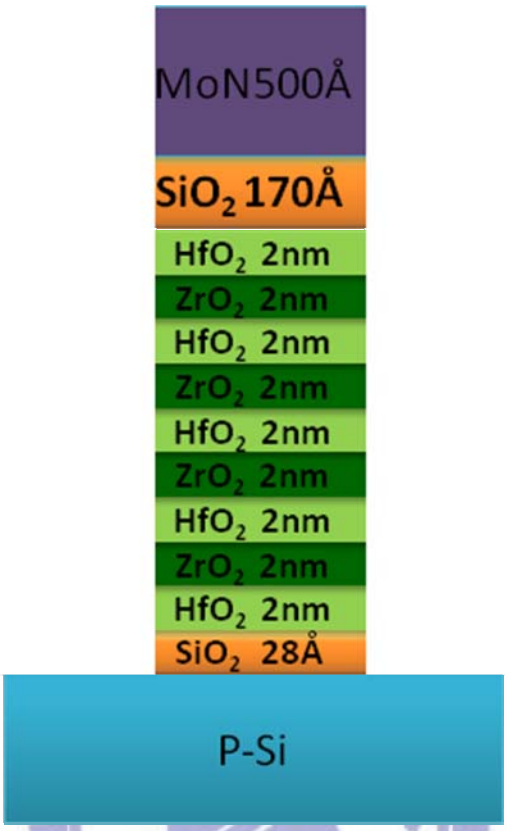
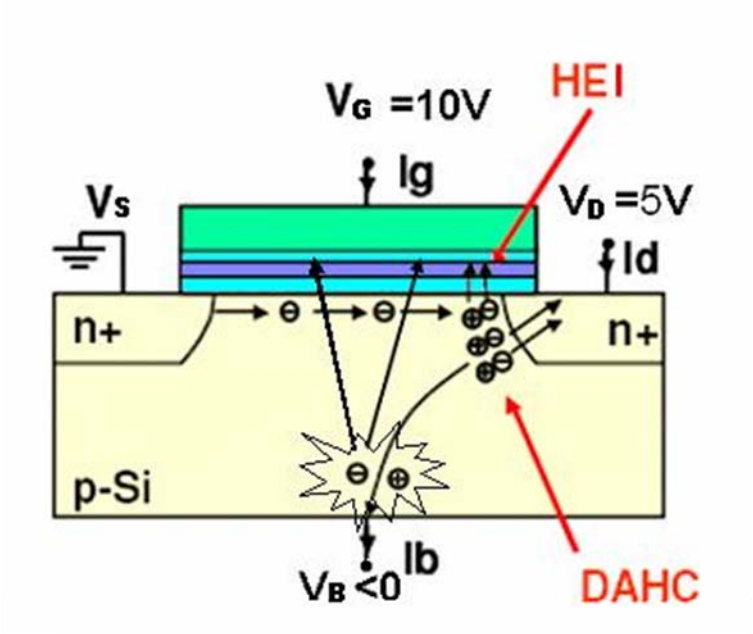
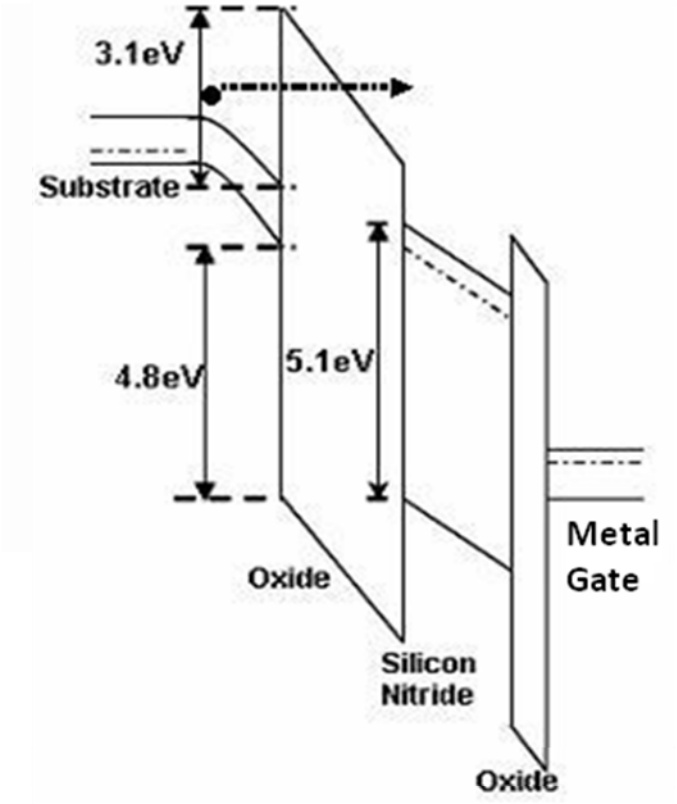


Fig.4-2 Cross section view of MoN/SiO_2/HfO_2-ZrO_2/SiO_2/Si MONOS.

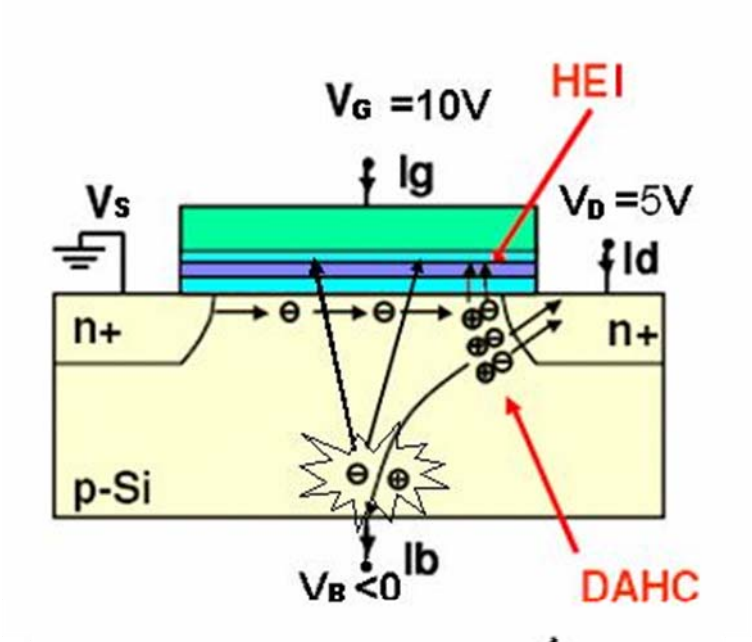


(a)

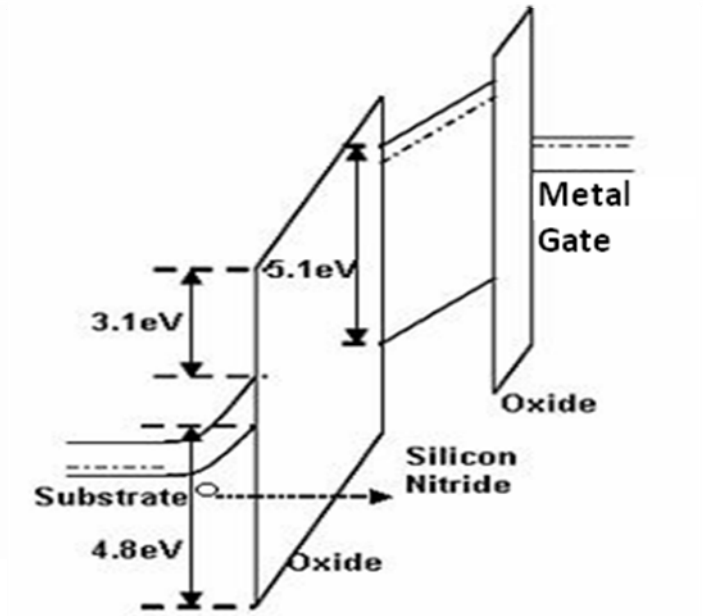


(b)

Fig.4-3 Channel-initiated secondary electron (CHISEL) programming mechanism for n-channel MONOS memory device. (a) Programming conditions and related events inside the substrate. (b) Band gap diagram for the programming.



(a)



(b)

Fig.4-4 Hot holes injection (HHI) erasing characteristics of N channel MONOS memory device. (a) Erasing conditions and mechanisms. (b) Erasing band gap diagram.

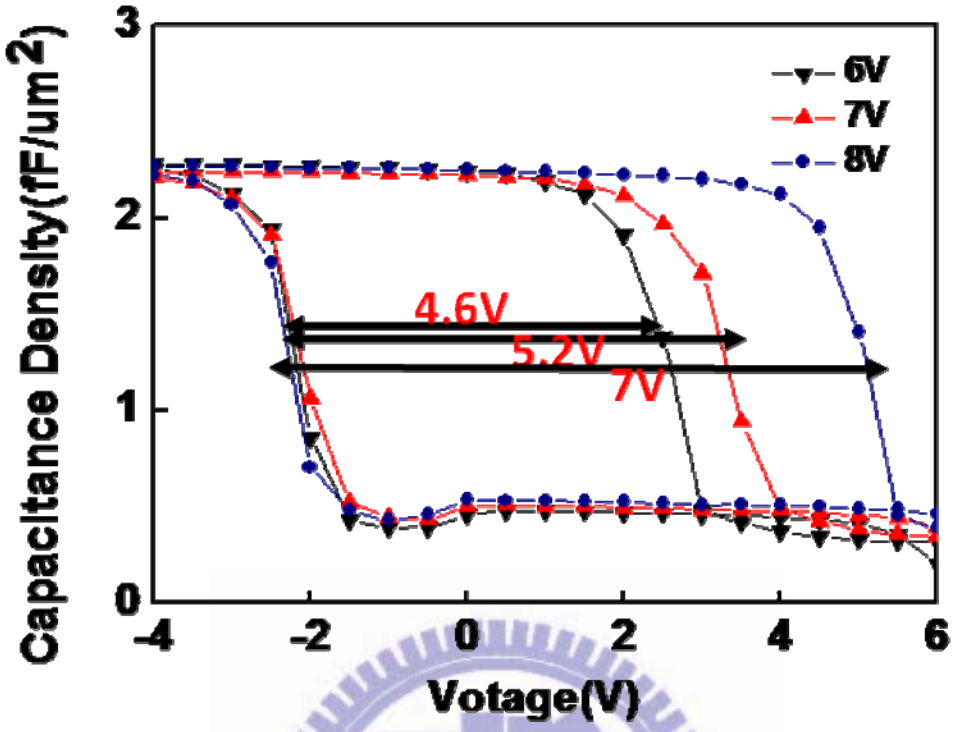


Fig.4-5 The measured C-V hysteresis of high-κ HfO_2-ZrO_2 interactive trapping MONOS capacitor.

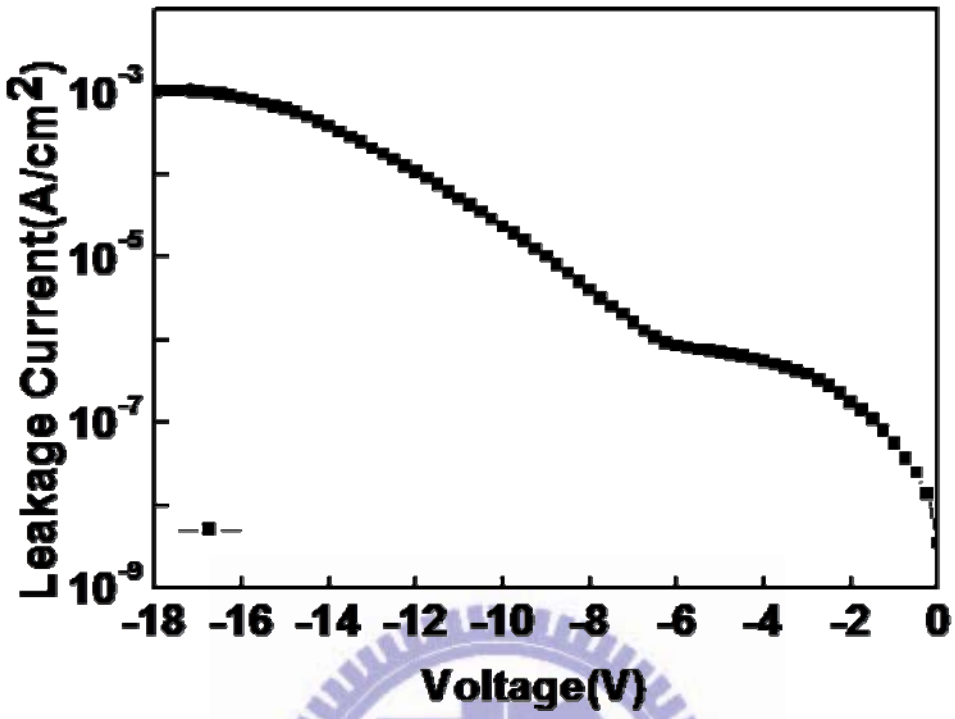


Fig.4-6 The measured J-V characteristics of high-κ HfO_2-ZrO_2 interactive trapping MONOS capacitor.

Chapter 5

Conclusions

Semiconductor flash memory device technology will continue to play an important role in the electronics industry, although its development has been facing a lot of challenges. Conventional FG structure suffers from serious coupling issues that degrade the device characteristics and may eventually limit further device scaling. It thus faces fierce competition from a number of new types of devices, including the MONOS.

In this dissertation, we emphasize on improvement of the trapping layer. If the trapping layer can efficiently catch more charges in a thin film, storage capability may become outstanding. High-κ material of Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) mix together by post-deposition annealing (PDA) process, in chaper3 and chapter4, we see that the interactive structure reveals big memory window, good retention and program-erase function by charge trapping or de-trapping in the high trap density HfO_2-ZrO_2.

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