國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

四埠射頻金氧半電晶體與共用源汲極主動區之
新型串疊結構的小訊號等效電路模型
建立與驗證

**Small Signal Equivalent Circuit Models Development
and Verification for Four-port RF MOSFET and New
Cascode Structure with Merged Source Drain Diffusion**

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中華民國一〇〇年十二月

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Structure with Merged Source Drain Diffusion

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摘要

　　本論文中，建立了小訊號等效電路模型，其中包括新型基板網路模型及其參數萃取方法，以應用於含有深 N 型槽(deep n-well)的射頻互補式金氧半場效電晶體電路模擬上。本研究設計四端點的射頻金氧半電晶體於四埠測試結構，並利用 UMC 65 奈米互補式金氧半場效電晶體製程(UN65)研製出來探討元件高頻特性及模型的發展。本論文提出之新型基板網路模型，具備完整之參數萃取流程並且解決了傳統模型與 BSIM-4 內建模型之問題。此基板網路模型乃是四埠元件小訊號等效電路模型之核心，直接影響四埠散射參數模擬之準確性，並且能夠簡易地取代 BSIM-4 內建模型以改進其四埠元件模擬之嚴重誤差。所建立的小訊號等效電路模型在不同偏壓進行模擬以作廣泛的驗證，其準確性已證明可應用於高達 40GHz 的寬頻範圍，以及不同的偏壓條件如截止區、線性區與飽和區。此外，本論文涵蓋 BSIM-4 模型之參數校正以及探討基板效應與電容模型中內部電荷計算方法。

　　論文的第二部份為新型串疊結構之設計與小訊號等效電路模型研發，其構成元件為共用源汲極主動區之雙閘極金氧半場效電晶體。此小訊號等效電路模型亦在不同偏壓下透過模擬做廣泛的驗證。再者，為了能夠同時模擬雙閘極金氧半場效電晶體大訊號特性與小訊號特性，我們利用 BSIM-4 建立傳統的串疊結構，即二個串疊之電晶體，並外掛寄

生元件和調整 BSIM-4 參數以近似雙閘極金氧半場效電晶體模型，並透過模擬做廣泛的
驗證，以應用於 40GHz 的寬頻範圍。
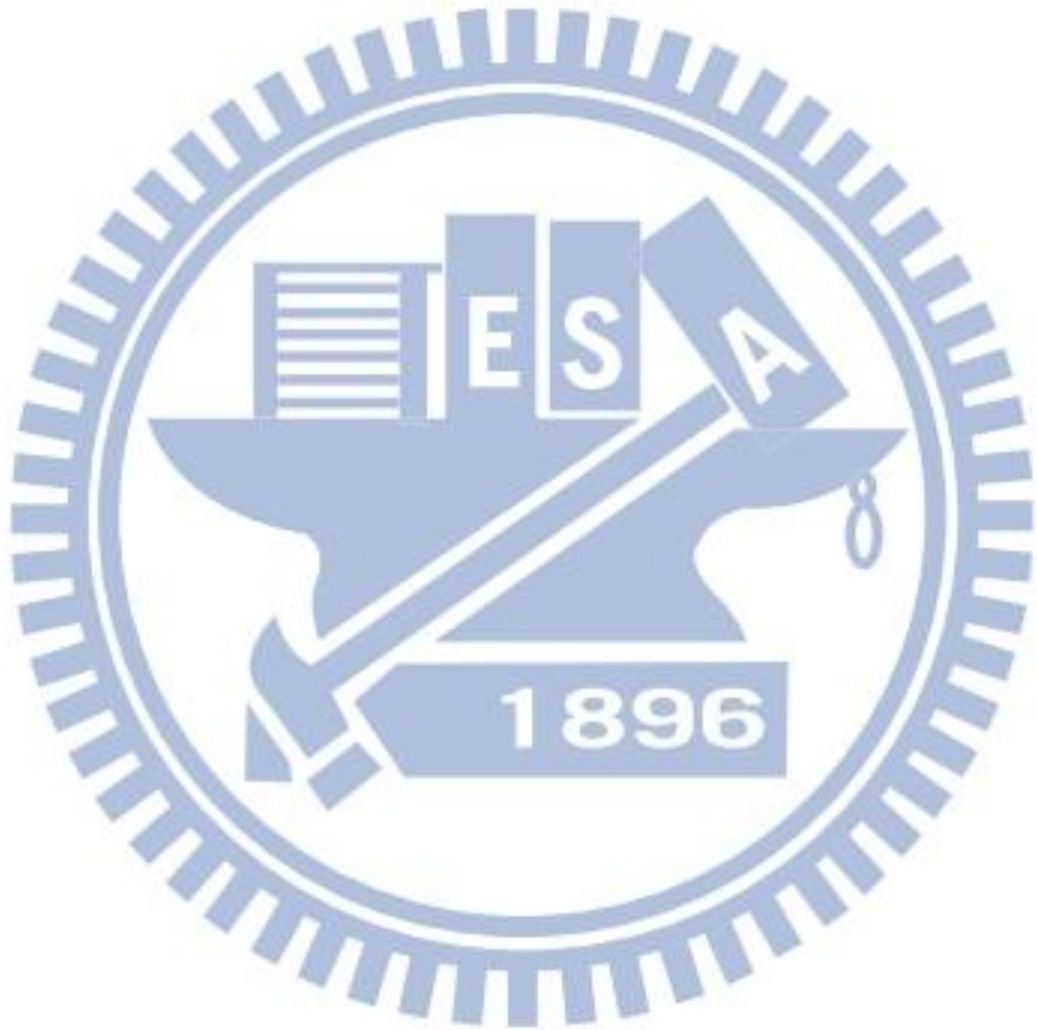
驗證，以應用於 40GHz 的寬頻範圍。

Small Signal Equivalent Circuit Models Development and Verification for Four-port RF MOSFET and New Cascode Structure with Merged Source Drain Diffusion

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Abstract

In this thesis, small signal equivalent circuit models have been established for 4-port RF MOSFET and new cascade structure. For the first time, a new body network model is developed for RF MOSFET fabricated with UN65 process in which the 4-port test structure was arranged with p-well body and deep n-well tied together to one port for body terminal. The proposed body network model is supported with a comprehensive model parameters extraction method and can be easily integrated with intrinsic MOSFET to build a small signal equivalent circuit model. The simulation accuracy has been proven by good match with measured 4-port S-parameters up to 40GHz and under different operation conditions, such as off-state, linear region, and saturation. On the other hand, the simulation using BSIM-4 with default body network fails to predict 4-port S-parameters with particularly large deviation in the parameters related to body node. The problem with BSIM-4 can be solved by replacing the default model with our new body network model.

In the second part, a small signal equivalent circuit is developed for new cascode structure, which is a kind of dual gate MOSFET with merged source/drain diffusion region. A modified body network model is adopted to match different configurations in deep n-well and p-well body. 4-port S-parameters can facilitate the extraction of complicated model parameters in dual gate MOSFET, such as in-stage capacitances, inter-stage capacitances, and cross-stage capacitances. The small signal equivalent circuit model built with core model for dual gate MOSFET and modified body network model demonstrates acceptable simulation accuracy at off state and saturation region. BSIM-4 is utilized to approach new cascode structure by incorporating parasitic elements such as inter-stage resistance and capacitances into conventional cascode with two single MOSFETs and enable both small signal and large signal simulations.
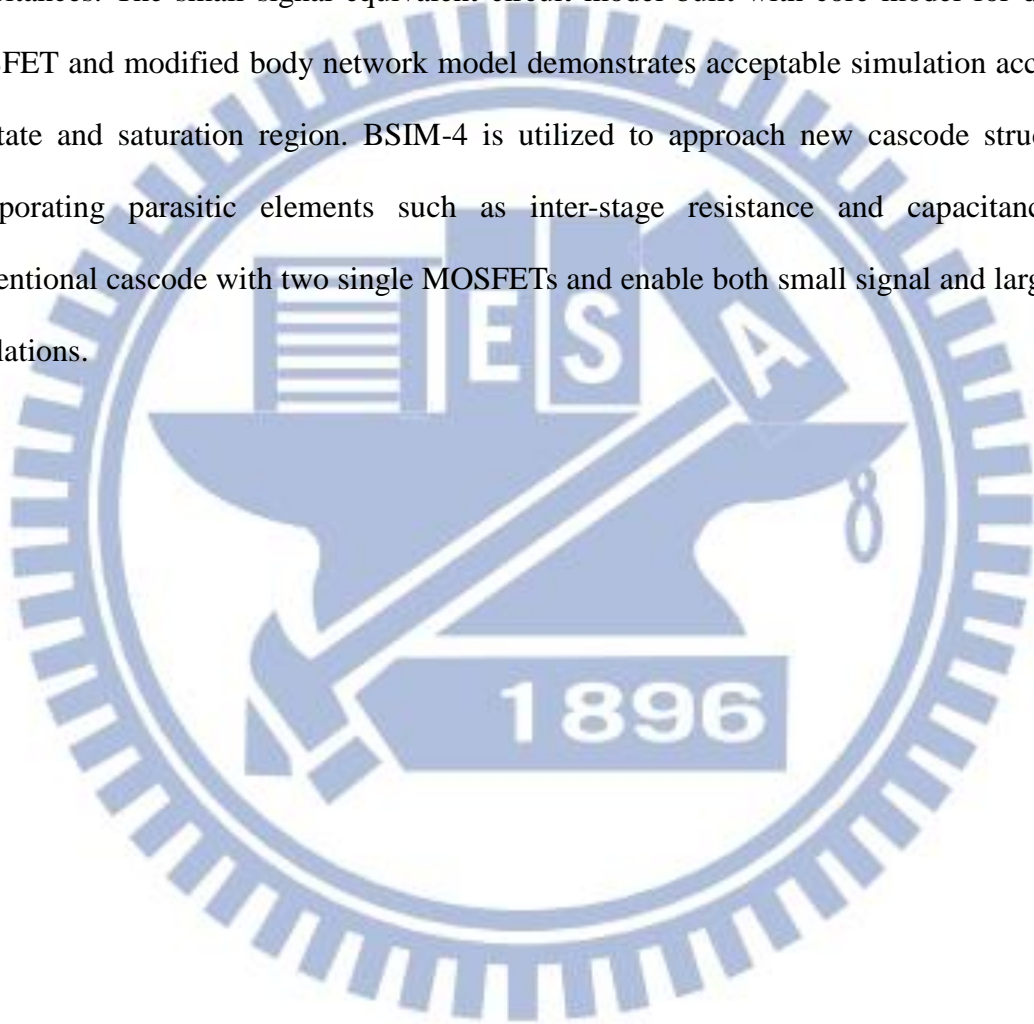
誌謝

首先，我要感謝我的指導教授--郭治群教授。過去三年多來在研究方法及態度上的指導，不斷地替學生尋找研究資源，並且嚴格要求學生完成許多基礎工作。在這過程中，除了建立許多研究領域相關的能力，也體會到許多待人接物的觀念，相信將會成為我未來工作上或者研究上的準則。

此外，還要感謝 NDL 的研究員—鄧裕民，在研究設備上的支持，讓我能夠接觸並學習到高頻量測設備。也感謝 RFTC 的工程師們，劉汶德在量測實驗上的協助以及建議，讓我能夠順利完成量測。

感謝 LAB635 中的所有成員們，敬文學長、智友學長、弈岑學長、唯倫、智翔的陪伴 ，讓我在實驗室的生活更豐富有趣。

最後，我要感謝一直在背後支持我的家人。

Content

Figure Caption

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Chapter 1

Introduction

1.1 An Overview and Motivation

Four-port (4-port) RF MOSFET appears as the basic building block to implement new biasing schemes. The dynamic body biases method has been recognized as one of the best approaches adapted to nanoscale CMOS device and circuit design in trade-off between the active and standby power. New circuit topologies for low power and low noise can be created on the RF/MS CMOS platform, with added features and freedom of DC/RF signal supply enabled by 4-terminal (4T) MOSFETs. Unfortunately, the existing RF CMOS models established by conventional 2-port test structures are valid only for 3T MOSFETs, which are restricted to zero body biases (ZBB) scheme. In addition, the 3T MOSFETs are limited to a common source (CS) topology. Even though CS topology can fit many RF and analog circuits design, common gate (CG) are frequently required for RF and analog circuits, e.g. CG for low power receiver design and for transimpedance amplifier. However, most of the characterization and model development stay with 3T MOSFETs residing on 2-port test structures, due to the relative simplicity compared with 4T MOSFETs in 4-port testers. To solve the mentioned problems and limitations exposed in previous work, extensive research effort has been focused on 4-port test structures design, measurement, de-embedding methods, and body network model development for 4T RF MOSFET modeling. The ultimate goal is to establish a comprehensive 4-port MOSFET model, which can ensure simulation accuracy for RF circuits design adopting dynamic body biases scheme.

In recent two decades, substrate network model becomes an important topic in the area of RF CMOS and different models have been published. However, most of the works have been focused on some minor modifications on the simplest model, i.e. single resistor model. Substrate network model is not available in BSIM-3 and it allows the freedom of deploying

different external networks. A π-type substrate network with 4 bulk resistors was proposed as a direct extension to BSIM-3 to improve simulation accuracy of output characteristics, such as S_{22} and R_{out} at high frequencies. However, this π-type substrate network model requires an extensive modification to BSIM-3 and makes the parameters extraction more complicated. A simplified lumped resistance model with 3 resistors (one gate resistor and two substrate resistors) was proposed to reduce the complexity in parameters extraction and maintain the simulation accuracy for both RF and baseband circuits. As for BSIM-4, an internally built substrate network with 5 resistors is a modified version, trying to enhance the simulation accuracy. Substrate network models with parallel RC instead of simple resistance network were proposed to improve modeling accuracy at high frequency. In summary, the trade-off between the curve fitting capability and difficulty in parameters extraction becomes one of the major limitations.

The mentioned problems and challenges motivate our interest in this research topic. A new body network model is developed in this thesis, based on 4-port RF MOSFETs built with deep n-well on p-substrate and the measured 4-port S-parameters. Note that body network model instead of substrate network model is named in this thesis, to make a clear definition that p-well body is separated from p-substrate by the deep n-well surrounding the p-well body. Furthermore, dual gate MOSFET with merged source/drain diffusion appears as an interesting structure for new cascode with the advantage of smaller cell size and then smaller parasitic junction capacitances. This new cascode structure introduces one more interesting topic of body network model and small signal equivalent circuit model for RF amplifier simulation and design. Again, 4-port S-parameters measurement is required for dual gate MOSFET characterization and model parameters extraction. The new cascode structure has been fabricated in the first test chip using UN65 process to carry out the mentioned model development and verification.

1.2 Thesis Organization

The major objective of this thesis is the development of small signal equivalent circuit models for 4-port RF MOSFET and new cascode structure with different configurations to facilitate RF CMOS circuit simulation and design.

First, chapter 2 addresses the fundamental theory of scattering matrix and parameters and RF amplifier consideration. The former one will cover both 2-port and 4-port networks. The latter one includes impedance matching, gain, noise, linearity, and stability.

In chapter 3, a new body network model is developed for 4-port RF MOSFET fabricated with UN65 process in which the p-well body and deep n-well tied together to one port for body terminal. A complete model parameters extraction flow will be provided with details of the extraction formulas. The proposed body network model and can be easily integrated with intrinsic MOSFET to build a small signal equivalent circuit model. The simulation accuracy will be verified by an extensive comparison with measured 4-port S-parameters up to 40GHz and under different operation conditions, such as off-state, linear region, and saturation. Also, a comparison with simulation by BSIM-4 using default body network has been carried out to explore the problem and solution.

In chapter 4, a small signal equivalent circuit is developed for new cascode structure based on a dual gate MOSFET with merged source/drain diffusion region. A modified body network model is created to match different configurations in deep n-well and p-well body. 4-port S-parameters can facilitate the extraction of complicated model parameters in the dual gate MOSFET, such as in-stage capacitances, inter-stage capacitances, and cross-stage capacitances. The small signal equivalent circuit model built with core model for dual gate MOSFET and modified body network model demonstrates acceptable simulation accuracy at off state and saturation region. BSIM-4 is utilized to approach new cascode structure by incorporating parasitic elements such as inter-stage resistance and capacitances into conventional cascode with two single MOSFETs and enable both small signal and large signal

simulations.

Finally, chapter 5 concludes with a summary and plan for future work.

Chapter 2

Fundamental theory

2.1 Scattering Matrix and Parameters

At microwave frequency the Z, Y and H parameters are very difficult to measure, the reason is that short and open circuits to ac signals are difficult to implement at microwave frequencies, so that, the scattering matrix are used usually in the analysis of two port networks usually.

2.1.1 Two–port network and scattering parameters

Considering the two-port network with incident wave a1 and reflected wave b1 at port1, and incident wave a2 and reflected wave b2 at port 2, the S parameters can be written in matrix form as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a \\ a \end{bmatrix} \tag{2.1}$$

2.1.2 Four –port scattering matrix and parameters

The extension of the formulation to four-port network is simple, the transmission lines are assumed to be lossless with characteristic impedance Z0, and then, we can write the scattering parameters of the four-port in matrix form.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} ; \quad [b] = [S][a] \tag{2.2}$$

Note that the value of S11 in (2.2) will be different from the value of S11 in a two-port common source configuration. For example, S11 can be arranged form the S matrix in (2.2) as

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=a_3=a_4=0} \tag{2.3}$$

To measure S11, the matched resistive terminations of 50Ω are used at ports 2, 3, and 4, and the ratio b1/a1 is obtained. In a two-port common source configuration, S11 is measured with reference resistance 50Ω at port 2 and source/body grounding. Similarly, the parameters S12, S21, and S22 in four-port S matrix will be different form the parameters in two-port matrix.

2.1.3 Port reduction method

Considering a 4-port networks system, the I-V relationship of the extrinsic and intrinsic parameters can be written as a 4X4 Y matrix.

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \tag{2.4}$$

According to equation (2.4), grounding a terminal is simply giving the corresponding zero supply voltage, and the remained sub-matrix will be the Y matrix representing the resulting configuration of the MOSFET, therefore, the 4 x 4 matrix of the 4-port networks can be reduced to 3-port or 2-port Y matrix. For example, the common source(CS) configuration is source (port3) and body (port4) grounding, the CS 2-port Y matrix can be obtained by setting the Vs=Vb=0V in the 4-port measurement, in this case, the term of source and body in (2.4) is negligible, the reduced Y matrix can be written as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.5}$$

2.2 RF Amplifier Design Consideration

In this section, we introduce the consideration in RF amplifier. It include impedance

6

matching , gain,noise Inter modulation and linearity.

2.2.1 Impedance matching

Low noise amplifier is the first stage in the receiver front-end circuits and is used to amplify the received weak RF signal with the minimum noise figure. As it is well recognized that impedance matching is the fundamental requirement in LNA designs for achieving the target performance of both gain and noise. There are four basic 50-Ω input matching architectures that have been explored in the traditional transistor-amplifier shown in **Fig. 2.1** In this section, we will have a review and discussion on the mentioned matching circuit architectures that can be used in LNA design. [1, 2]

(1) Resistive termination   (2) Inductive degeneration   (3) Shunt-series feedback   (4) 1/gm termination
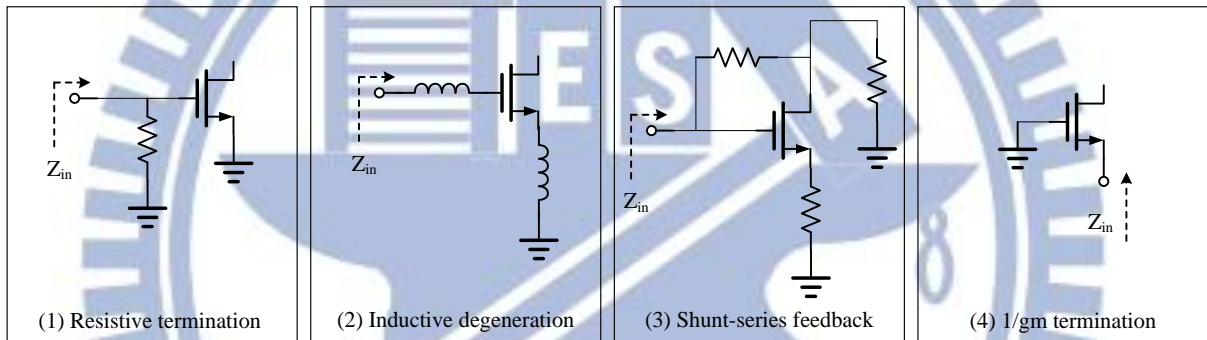
Fig. 2.1 Traditional transistor-amplifier of input matching

2.2.2 Power gain and voltage gain

Consider an arbitrary two-port network connected to source and load impedances Zs and Z_L, respectively, the reflection coefficient seen looking toward the load is

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.6}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2.7}$$

Consider Network analyzer Agilent 8510C in measurement, It's internal impedance is set 50Ω,so Γ_S and Γ_L are too small to ignore. By the way , the process which Network analyzer is set 50Ω is called calibration. We define expression for power gain in terms of the S parameters of the two-port network and the reflection coefficients, Γs and Γl, of the source and

load. Because Γ_L and Γ_L are small, we can get power gain.

$$\text{power Gain} : G = \frac{\text{Power dissipated in the load}}{\text{Power delivered to the input}} = \frac{|S_{21}|^2 (1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2} \tag{2.8}$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{2.9}$$

$$\text{power Gain} : |S_{21}|^2 \tag{2.10}$$

S_{21} can expressive by Y parameter and Z_0.

$$S_{21} = \frac{-2Y_{21}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \tag{2.11}$$

Consider the same s parameter ,we can convert from s parameter to ABCD parameter.ABCD

parameter define as follow

$$ABCD = \begin{bmatrix} A = \dfrac{V_1}{V_2}\Big|_{I_2=0} & A = \dfrac{V_1}{-I_2}\Big|_{V_2=0} \\ C = \dfrac{I_1}{V_2}\Big|_{I_2=0} & D = \dfrac{I_1}{-I_2}\Big|_{V_2=0} \end{bmatrix} \tag{2.12}$$

A is the reciprocal of voltage gain.voltage gain can expressive by Y parameter as follow,

$$\text{voltage gain} : \frac{1}{A} = \frac{-Y_{22}}{Y_{21}} \tag{2.13}$$

Observe measure data in **Fig. 2.2** ,and the voltage gain and power gain is different about

frequency depend, we can understand even power gain match well from simulation data to

measure data,but it don't mean voltage gain as well. The most influence of voltage gain is

Rds.we can check Rds and voltage gain has same trend.
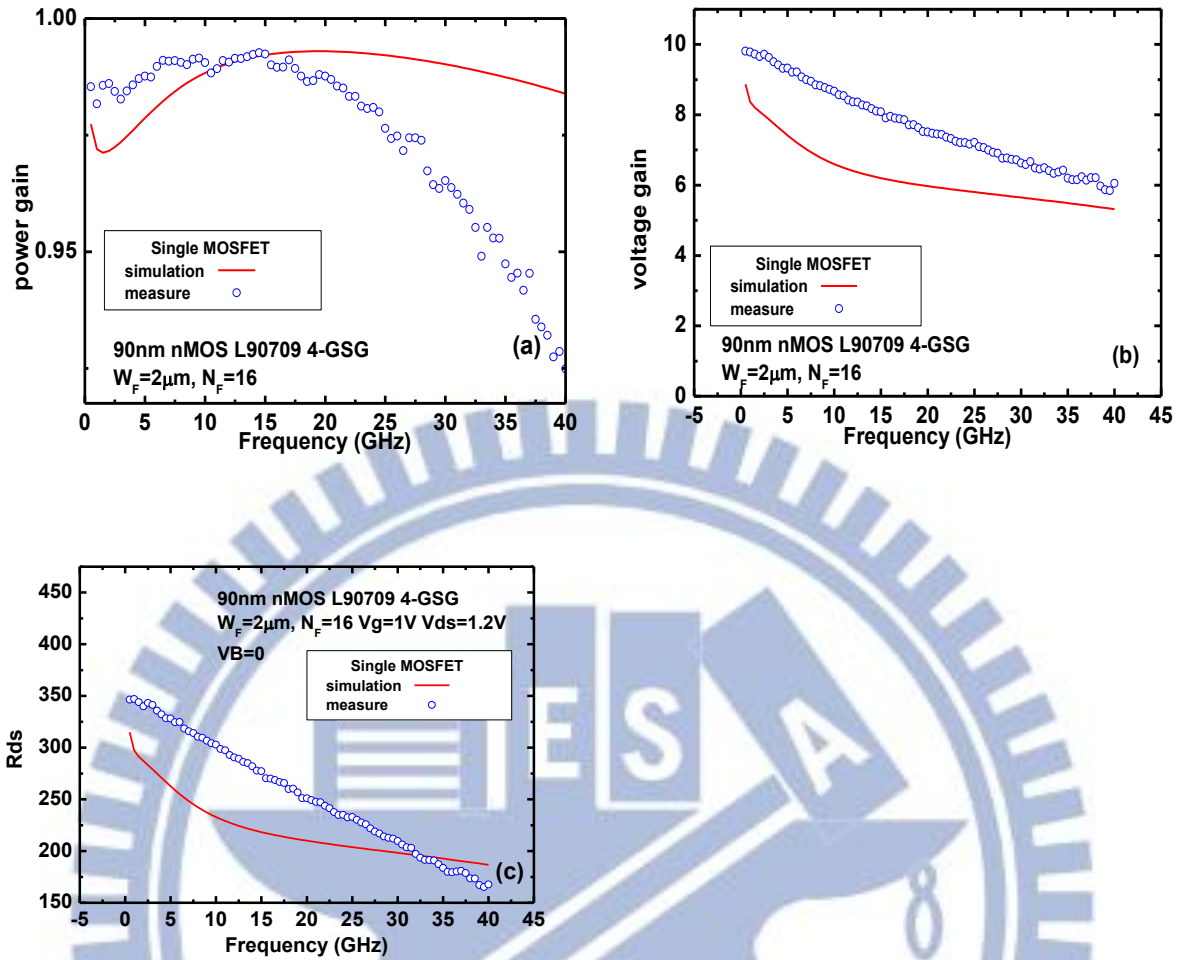
Fig. 2.2 (a) MOSFET's power gain comparisons between simulation and measurement

(b) MOSFET's voltage gain comparisons between simulation and measurement

(c) MOSFET's Rds comparisons between simulation and measurement

2.2.3 Noise [1]

Noise Factor

Noise factor (F) is defined as the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output. Considering a network with gain G and noise N_a, noise factor then can be express as (2.14)

$$F \equiv \frac{S_i / N_i}{S_o / N_o} = \frac{S_i / N_i}{(GS_i)/[G(N_i + N_a)]} = \frac{N_i + N_a}{N_i} = \frac{N_o}{GN_i} = \frac{Total\ noise\ power\ @\ output}{Noise\ power\ @\ output\ due\ to\ source\ only}$$

(2.14)

Generally we use this measure in the unit of dB, namely noise figure (NF) written in (2.15)

$$NF = 10\log F \qquad (2.15)$$

A useful measure of the noise performance of a system is the noise factor, denoted as F and given in (2.14). To define it and understand why it is useful, consider a noisy (but linear) two-port network driven by a source that has an impedance Z_s and an equivalent series noise voltage $\overline{e_s^2}$, illustrated in **Fig. 2.3**.

If we are concerned only with overall input-output behavior, it is an unnecessary complication to keep track of all of internal noise source. Fortunately, the net effect of all of those sources can be represented by just one pair of external sources like a noise voltage $\overline{e_n^2}$ and a noise current $\overline{i_n^2}$ as shown in **Fig. 2.4**. This simplification allows a rapid evaluation of how the source impedance affects the overall noise performance. As a consequence, we can identify the criteria, which one must satisfy for optimum noise performance.
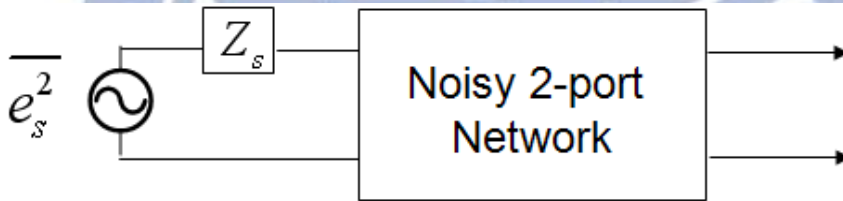
Fig. 2.3. Noisy two-port driven by noisy source
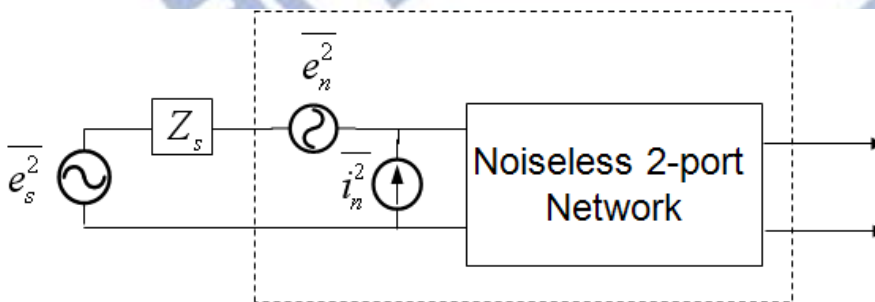
Fig. 2.4. Equivalent circuit for two-port noise model

Carrying out the calculations based on the equivalent circuit of noisy two-port illustrated in **Fig. 2.4**, the noise factor is written as

$$F = \frac{N_i + N_a}{N_i} = \frac{\overline{e_s^2} + \overline{|e_n + Z_s i_n|^2}}{\overline{e_s^2}} \tag{2.16}$$

In order to accommodate the possibility of correlations between e_n and i_n, express e_n as the sum of two components in (2.17) in which e_{nc}, represents the term correlated with i_n, and e_{nu}, the un-correlated term.

$$e_n = e_{nc} + e_{nu} \tag{2.17}$$

Since e_n is correlated with i_n, it may be treated as proportional to $\mathbf{i_n}$ through a constant namely Z_C whose dimensions are those of impedance:

$$e_{nc} = Z_c i_n \tag{2.18}$$

Combining (2.16),(2.17),(2.18) and, the noise factor becomes

$$F = \frac{\overline{e_s^2} + \overline{|e_{nu} + (Z_c + Z_s)i_n|^2}}{\overline{e_s^2}} = 1 + \frac{\overline{e_{nu}^2} + |Z_c + Z_s|^2 \overline{i_n^2}}{\overline{e_s^2}} \tag{2.19}$$

The expression in (2.19) contains three independent noise sources, each of which may be treated as thermal noise produced by an equivalent resistance or conductance:

$$R_u \equiv \frac{\overline{e_{nu}^2}}{4kT\Delta f}, \quad R_s \equiv \frac{\overline{e_s^2}}{4kT\Delta f}, \quad G_n \equiv \frac{\overline{i_n^2}}{4kT\Delta f} \tag{2.20}$$

Using these equivalences, the expression for noise factor can be written purely in terms of impedances and admittances:

$$F = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s} = 1 + \frac{R_u + \left[(R_c + R_s)^2 + (X_c + X_s)^2\right]G_n}{R_s} \tag{2.21}$$

where $Z_c = R_c + jX_c$ is the correlation impedance and $Z_s = R_s + jX_s$ is the source impedance.

2.2.4 Linearity[3]

Linearity is one of the key requirements in LNA design to maintain linear operation in the presence of a large interfering signal and when the input is driven by a large signal. Any nonlinear transfer function can be mathematically written as a series expansion of power-law

11

terms unless the system contains memory. The input V_i and output V_o of a two-port network

can be related by a power series. For simplicity, we make an approximation to the third order

term:

$$V_o = \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3 \qquad (2.22)$$

where $\alpha_1, \alpha_2, \alpha_3$ are constants.

If a sinusoidal waveform is applied to a nonlinear system, the output generally exhibits

frequency dependent components that are integer multiples of the input frequency. In (2-22),

setting $V_i(t) = A\cos(\omega t)$, the

$$V_o(t) = \alpha_1 A\cos(\omega t) + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t \qquad (2.23)$$

$$= \alpha_1 A\cos(\omega t) + \frac{\alpha_2 A^2}{2}[1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3\cos(\omega t) + \cos(3\omega t)] \qquad (2.24)$$

$$= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \qquad (2.25)$$

In (2.23), the term with the input frequency ω is called the "fundamental" and the

higher-order terms the "harmonics". The first term in (2.23) is the linear term and is the ideal

output if the two-port network is completely linear. Other terms in (2.23) are responsible for

nonlinearity, and they cause a DC shift as well as distortion at frequencies 2ω, 3ω, and higher

harmonics derived in (2.24) and (2.25), which result in either gain compression or gain

expansion. It can be observed from (2.25) that distortion is present in any signal level.

In most circuits of interest, the output is a "compressive" or "saturating" function of the

input; that is, the gain approaches zero for sufficiently high input levels. In (2.25) this occurs if

$\alpha_3 < 0$. Written as $\alpha_1 A + \dfrac{3\alpha_3 A^3}{4}$, $\alpha_1 A$ represents the fundamental amplitude and the gain is

therefore a decreasing function of the third-order harmonic proportional to $\alpha_3 A^3$. In RF circuits,

this effect is quantified by the "1-dB compression point", defined as the input signal level that

causes the small-signal gain to drop by 1 dB. As shown in **Fig. 2.5**, which is plotted on a log-log

scale as a function of the input level, the output level falls below its ideal value by 1 dB at the 1-dB compression point [3].
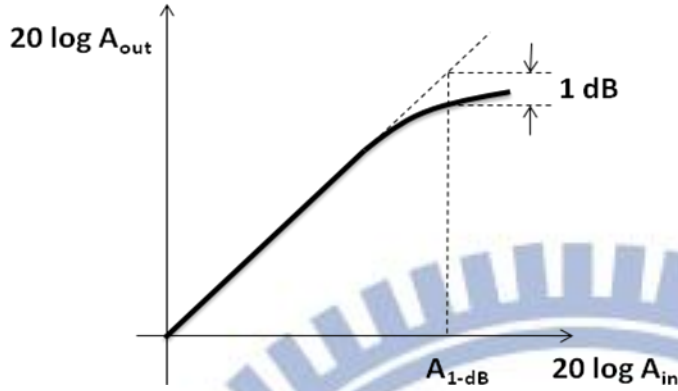
Fig. 2.5 Definition of the 1-dB compression point

To calculate the 1-dB compression point, we can write from (2.25)

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{1-dB}^2\right| = 20\log|\alpha_1| - 1dB \tag{2.26}$$

That is,

$$A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.27}$$

2.2.5 Intermodulation [3]

Harmonic distortion that was introduced previously is the result of nonlinearity due to a single sinusoidal input. When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Called intermodulation (IM), this phenomenon arises from "mixing" (multiplication) of the two signals when their sum is raised to a power greater than unity. To investigate the effects of both harmonic distortion and intermodulation, we assume that the input signal is composed of two different frequencies ω_1 and ω_2 given in (2.28)

$$V_i(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t) \tag{2.28}$$

(2.28) can be substituted into (2.22) Thus, the output can be expressed as

$$V_o(t) = \alpha_1 [A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)] + \alpha_2 [A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)]^2$$
$$+ \alpha_3 [A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)]^3 \tag{2.29}$$

Expanding the right-hand side and discarding the dc terms and harmonics, we obtain intermodulation products expressed in (2.30) and (2.31) for the second order and (2.32) for the third order IM products, namely IM2 and IM3.

$$\omega = \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2 \cos[(\omega_1 + \omega_2)t] + \alpha_2 A_1 A_2 \cos[(\omega_1 - \omega_2)t] \tag{2.30}$$

$$= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} \cos[(2\omega_1 + \omega_2)t] + \frac{3\alpha_3 A_1^2 A_2}{4} \cos[(2\omega_1 - \omega_2)t] \tag{2.31}$$

$$= 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4} \cos[(2\omega_2 + \omega_1)t] + \frac{3\alpha_3 A_2^2 A_1}{4} \cos[(2\omega_2 - \omega_1)t] \tag{2.32}$$

and the fundamental components written in (2.33)

$$\omega = \omega_1, \omega_2 : (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2) \cos(\omega_1 t)$$
$$+ (\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2) \cos(\omega_2 t) \tag{2.33}$$

Of particular interest are the third-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, illustrated in **Fig. 2.6** in which the input RF signals are two-tone with two different frequencies such as ω_1 and ω_2

Fig. 2.6 Intermodulation in a nonlinear system

where it is assumed that $A_1 = A_2 = A$.

From **Fig. 2.7(a)**, it is apparent that the third-order intermodulation distortion IM3 signals are close to the signals of interest F, which makes the filtering out of IM3 signals difficult when recovering the signals of interest. Therefore minimizing intermodulation distortion is a key

objective in many RF circuit design.

Third-Order Intercept Point (IIP3) [3]

From(2.30)~(2.33) and let $A_1 = A_2 = A$, we can drive the expression

$$V_o(t) = (\alpha_1 + \frac{9}{4}\alpha_3 A^2)A\cos(\omega_1 t) + (\alpha_1 + \frac{9}{4}\alpha_3 A^2)A\cos(\omega_2 t)$$
$$+ \frac{3}{4}\alpha_3 A^3 \cos[(2\omega_1 - \omega_2)t] + \frac{3}{4}\alpha_3 A^3 \cos[(2\omega_2 - \omega_1)t] + \ldots$$

(2.34)

We note that as the input amplitude A is small to keep $\alpha_1 \gg \frac{9}{4}|\alpha_3|A^2$, the fundamentals

increase proportional to A, whereas if the input level A increases to the intercept point so that

$\alpha_1 \gg \frac{9}{4}|\alpha_3|A^2$ is no longer valid, the gain will drop and the third-order IM products in

proportion to A^3 will take over the fundamentals, as shown in **Fig. 2.7(a)**. Plotted on a

logarithmic scale in **Fig. 2.7 (b)**, the magnitude of the IM products grows at three times the rate

at which the main components increase. The third-order intercept point, namely IP$_3$ is defined

to be at the intersection of the two lines. The horizontal coordinate of this point is called the

input IP$_3$ (IIP$_3$), and the vertical coordinate is called the output IP$_3$ (OIP$_3$).

(a)	(b)
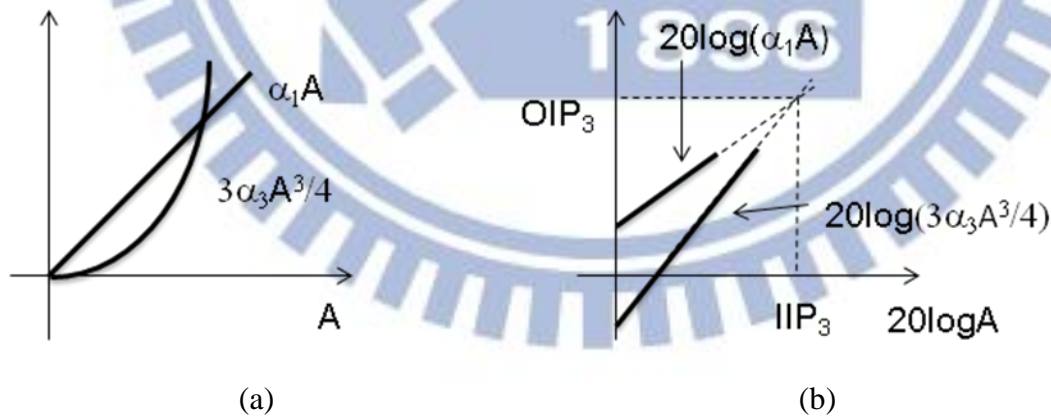
Fig. 2.7 (a) The linear gain and the nonlinear component (b) The IIP$_3$ and OIP$_3$

If $\alpha_1 \gg \frac{9}{4}|\alpha_3|A^2$, the input level for which the output components at ω_1 and ω_2 have the

same amplitude as those at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ is given by

$$|\alpha_1| A_{IP3} = \frac{3}{4} |\alpha_3| A_{IP3}^3 \qquad (2.35)$$

Thus, the input IP$_3$ is

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} \qquad (2.36)$$

2.2.6 Stability [4]

One more important consideration for an amplifier design is the assurance of stability. For example, LNAs in the form of a two-port network, the requirement for ensuring stability is that it must not produce an output with oscillatory behavior. The stability of a two-port network can be determined from the S-parameters, the matching networks, and the terminations. Simpler tests can be used to determine unconditional stability [4]. One of these is the K-△ test, where it can be shown that a device will be unconditionally stable if Rollet's condition, defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad (2.37)$$

along with the auxiliary condition that

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \qquad (2.38)$$

are simultaneously satisfied. These two conditions are necessary and sufficient for unconditional stability.

If the transistor, as unconditionally stable, so that $K > 1$, the maximum transducer power gain can be reduced as follows:

$$G_{T_{max}} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \qquad (2.39)$$

The maximum transducer power gain is also sometimes referred to as the matched gain. The maximum gain does not provide a meaningful result if the device is only conditionally stable, since simultaneous conjugate matching of the source and load is not possible if $K < 1$. In this case a useful figure of merit is the maximum stable gain, defined as the maximum transducer

power gain of with K=1. Thus.

$$G_{msg} = \frac{|S_{21}|}{|S_{12}|}$$

(2.40)

The maximum stable gain is easy to compute, and offers a convenient way to compare the

gain of various devices under stable operating conditions.
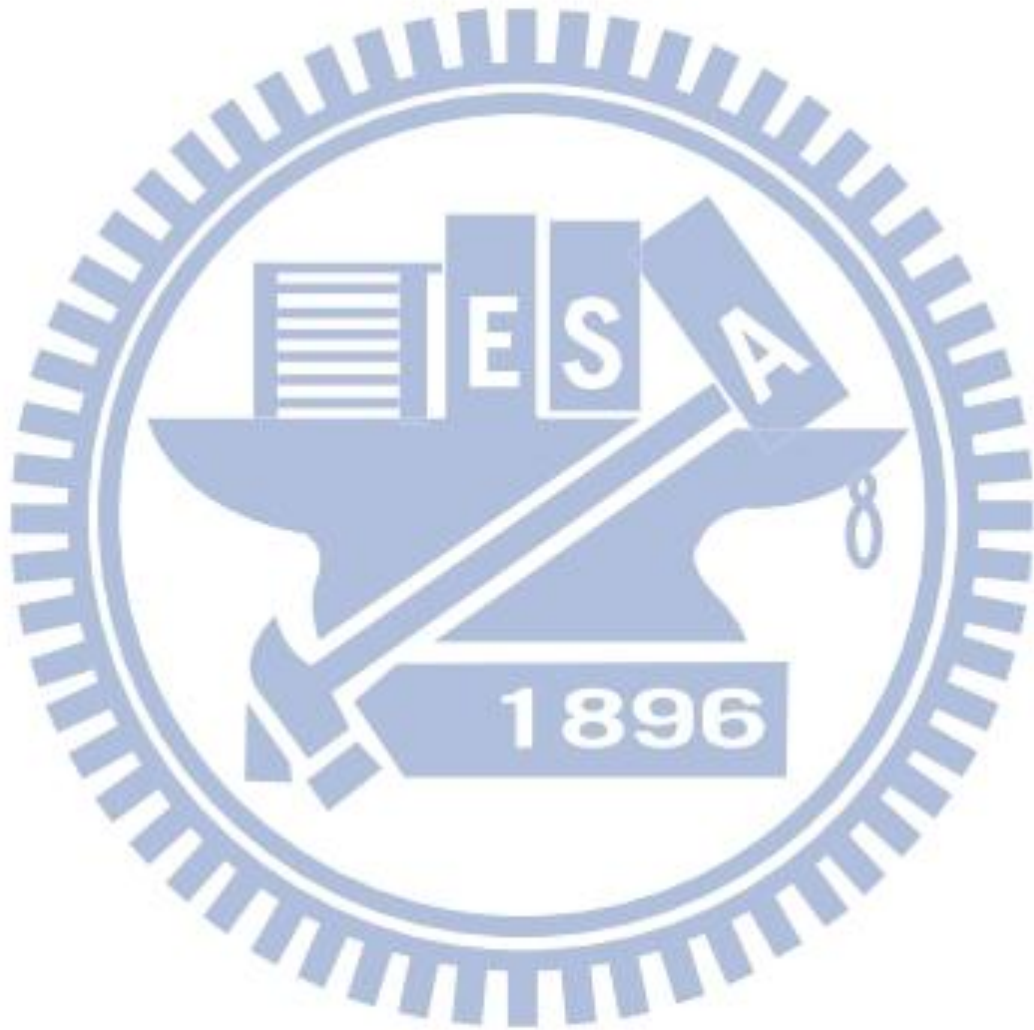
Chapter 3

Four-port RF MOSFET Modeling for Simulation with DBB (UN65 CMOS Technology)

In this chapter, four-port (4-port) RF MOSFET model development will be carried out based on experimental data from UN65 RF n-MOSFET. At first, 4-port RF MOSFET layout design, measurement and deembedding methods will be described in sec. 3.1 to address layout effects on high frequency characteristics and equivalent circuit model for simulation. In sec. 3.2, a new body network model will be introduced and proven for 4-port RF MOSFET with deep n-well and different layouts in the connections of p-well body, deep n-well, and p-substrate. In sec. 3.3, small signal equivalent circuit models will be developed for 4-port RF MOSFET in different operation regions, such as off state, linear region, and saturation region. The new body network model can be easily adopted into the small signal equivalent circuits to enable accurate simulation of 4-port S- and Y-parameters. In sec. 3.4, BSIM-4 calibration will be performed on both I-V and C-V models to improve simulation accuracy for 4-port RF MOSFET under dynamic body biases (DBB). The comparison of measurement and simulation by using BSIM-4 and small signal equivalent circuit models will be presented in sec. 3.3.

3.1 Four-port RF MOSFET Layout and Measurement

In this thesis, there are totally three kinds of 4T RF MOSFET layouts and 4-port test structures implemented in different CMOS processes, such as UN90 (L90709), UN65 (L65003), and TN90RF (100A). 4-port RF MOSFET layout analysis for parasitic RLC extraction is introduced in sec. 3.1.2. 4-port RF MOSFET measurement and deembedding method are addressed in sec. 3.13. Finally, the parasitic resistance extraction from 4T RF MOSFET in 4-port test structure and the impact on electrical performance, such I-V and g_m

are presented in sec. 3.1.4. with a comparison with 3T RF MOSFET in 2-port test structure.

3.1.1 4T MOSFET Layout Analysis for Body Network Model Development

The circuit architectures of body network model and small signal equivalent circuits are critically determined by the layouts of RF MOSFETs, particularly for those built in 4-port test structures. **Fig. 3.1(a)~(c)** illustrate 3 different layouts of 4-port RF MOSFETs, which were implemented by UN65, UN90, and TN90RF processes, with test chip names given as L65003, L90709, and 100A, respectively.

Table 3.1 (a) summarizes 3 items of layout features in 4-port RF MOSFETs, which are identified as the major differences between the mentioned 3 test chips. For body contacts layout, L65003 adopts two rows of contacts in parallel with the gate finger, namely parallel body contacts. As for L90709 and TN90RF-100A, ring type body contacts enclosing the multi-finger MOSFET is employed to reduce body resistance. All of the 3 test chips were fabricated with deep n-well but different layouts in the connection to deep n-well and p-well body. For L65003, the deep n-well is tied together with p-well body and connected to port-4. For L90709, deep n-well is connected to ground and p-well body is individually connected to port-4. As for TN90RF-100A, deep n-well is floating, i.e. without any connection to the external node. In this chapter, we will focus on the characterization, analysis, and modeling on L65003 and also the differences between L65003 and L90709. The study on TN90RF-100A will be presented in chapter 5.

In our previous work (YH Tsai in Prof. Guo group), a simple body network model as shown in **Fig. 3.2** was developed for 4-port RF MOSFET in L90709. This body network model incorporates C_{js} and C_{jd} for junction capacitances from source and drain to body, and C_{dnw} for junction capacitance between deep n-well and p-well body. R_{bb} represents p-well body resistance and R_{dnw} is deep n-well resistance. According to L90709 layout feature, i.e. body to port-4 and deep n-well to ground, this simple body network model is built with simple series $R_{dnw}C_{dnw}$ from port-4 to ground (**Fig. 3.2**). Thus, the model parameters can be

extracted from 4-port Y-parameters, based on equivalent circuit analysis on the proposed body network model as follows. First, C_{js} and C_{jd} are extracted from $Im(Y_{42})$ and $Im(Y_{43})$ at very low frequency, given by (3.3) and (3.4). Then, the body resistance R_{bb} can be extracted from $Re(Y_{42})$ or $Re(Y_{43})$ with pre-extracted C_{js} and C_{jd} at very low frequency, denoted as $R_{bb(LF)}$ given by (3.5) or (3.6). Also, R_{bb} can be determined from $Re(Y_{42})$ or $Re(Y_{43})$ at very high frequency, according to (3.9) or (3.10) and denoted as $R_{bb(HF)}$. Note that it is considered that the Y-parameters under cold device condition ($V_g=V_d=V_s=V_b=0$) follow symmetric rule between source and drain to body, i.e. $Y_{42}=Y_{43}$ or $Y_{24}=Y_{34}$.

$$Y_{24} = Y_{42} = \frac{-j\omega C_{js} - \omega^2 C_{js}(C_{jd} + C_{js})R_{bb}}{1 + \omega^2(C_{jd} + C_{js})^2 R_{bb}^2} \tag{3.1}$$

$$Y_{34} = Y_{43} = \frac{-j\omega C_{jd} - \omega^2 C_{jd}(C_{jd} + C_{js})R_{bb}}{1 + \omega^2(C_{jd} + C_{js})^2 R_{bb}^2} \tag{3.2}$$

At very low frequency, $\omega^2(C_{jd} + C_{js})^2 R_{bb}^2 \ll 1$

$$C_{js[LF]} = -\frac{Im(Y_{42(LF)})}{\omega} \tag{3.3}$$

$$C_{jd[LF]} = -\frac{Im(Y_{43(LF)})}{\omega} \tag{3.4}$$

$$R_{bb[LF]} = \frac{Re(Y_{42(LF)})}{-\omega^2 C_{js[LF]}(C_{jd[LF]} + C_{js[LF]})} \tag{3.5}$$

$$R_{bb[LF]} = \frac{Re(Y_{43(LF)})}{-\omega^2 C_{jd[LF]}(C_{jd[LF]} + C_{js[LF]})} \tag{3.6}$$

at very high frequency, $\omega^2(C_{jd} + C_{js})^2 R_{bb}^2 \gg 1$

$$Re(Y_{24(HF)}) = Re(Y_{42(HF)}) \cong \frac{-C_{js[LF]}}{(C_{jd[LF]} + C_{js[LF]})R_{bb[HF]}} \tag{3.7}$$

$$Re(Y_{34(HF)}) = Re(Y_{43(HF)}) \cong \frac{-C_{jd[LF]}}{(C_{jd[LF]} + C_{js[LF]})R_{bb[HF]}} \tag{3.8}$$

$$R_{bb[HF]} = -Re(Y_{42(HF)})\frac{C_{js[LF]}}{(C_{jd[LF]} + C_{js[LF]})} \tag{3.9}$$

$$R_{bb[HF]} = -\text{Re}(Y_{43(HF)}) \frac{C_{jd[LF]}}{(C_{jd[LF]} + C_{js[LF]})} \tag{3.10}$$

Theoretically, all of the RLC elements in the equivalent circuit should be constant independent of frequency. It is expected that $R_{bb(LF)}$ extracted at very low frequency is equal to $R_{bb(HF)}$ extracted at very high frequency. **Table 3.2(b)** summarizes R_{bb} extracted from L90709 and L65003 to verify 4-port RF MOSFET layout effects and frequency dependence. The results from L90709 indicate very minor difference between $R_{bb(LF)}$ and $R_{bb(HF)}$ and prove that R_{bb} extracted from the equivalent circuit model is a simple resistance in dependent of frequency. Furthermore, the larger finger number can help reduce R_{bb}. However, R_{bb} extracted from L65003 reveal dramatic difference between $R_{bb(LF)}$ and $R_{bb(HF)}$. The extraordinary frequency dependence suggests that the body network model proposed for L90709 cannot be applied to L65003, due to fundamental differences in the 4-port RF MOSFET layout summarized in **Table 3.2(a)**. As for L90709, the body network model is proven by a good match between the measured and simulated $\text{Re}(Y_{43})$ using (3.2), as shown in **Fig. 3.3**. Note that $\text{Re}(Y_{43})$ tends to saturate to a constant at very high frequency, which is predicted by (3.10). The saturation of $\text{Re}(Y_{42})$ or $\text{Re}(Y_{43})$ at high frequency suggests the saturation of substrate loss when the frequency increases beyond the attenuation frequency of the series RC in the body network model. However, the comparison of measured $\text{Re}(Y_{42})$ or $\text{Re}(Y_{43})$ between L90709 and L65003 shown in **Fig. 3.4** indicates that both $\text{Re}(Y_{42})$ and $\text{Re}(Y_{43})$ reveal a fall off without any saturation when increasing frequency. Again, the results suggest that the simple body network model derived for L90709 is no longer valid for L65003. Potentially, a simple series RC for deep n-well cannot be applied to L65003 and a new body network model will be presented in sec. 3.2. Besides $\text{Re}(Y_{42})$ and $\text{Re}(Y_{43})$ for R_{bb}, C_{dnw} is one more important parameter to verify the difference between L90709 and L65003 with different layouts in deep n-well and p-well body. Considering that all of the capacitances related to body, i.e. port-4 have to follow charge conservation law, C_{dnw} can be extracted from 4 components of $\text{Im}(Y_{4i})$

(i=1,2,3,4) at very low frequency given by (3.11).

$$C_{dnw} = \frac{1}{\omega}\left[\text{Im}(Y_{44}) + \text{Im}(Y_{43}) + \text{Im}(Y_{42}) + \text{Im}(Y_{41})\right]\big|_{\omega \to 0}$$
(3.11)

Fig. 3.5 (a) and (b) present C_{dnw} extracted from L90709 and L65003, respectively. Note that C_{dnw} determined at very low frequency reveal different body biases dependence between L90709 and L65003. For L90709 with deep n-well separated from p-well body, the body biases (ZBB, FBB, and RBB) applied to p-well lead to corresponding biases at body to deep n-well (grounded) and significant variation of C_{dnw} at very low frequency. As for L65003 with deep n-well tied together with p-well body, the body biases are applied to p-well body and deep n-well simultaneously and it leads to zero bias at the junction between deep n-well and p-well and explains why the C_{dnw} are not sensitive to various body biases.

| (a) | (b) | (c) |
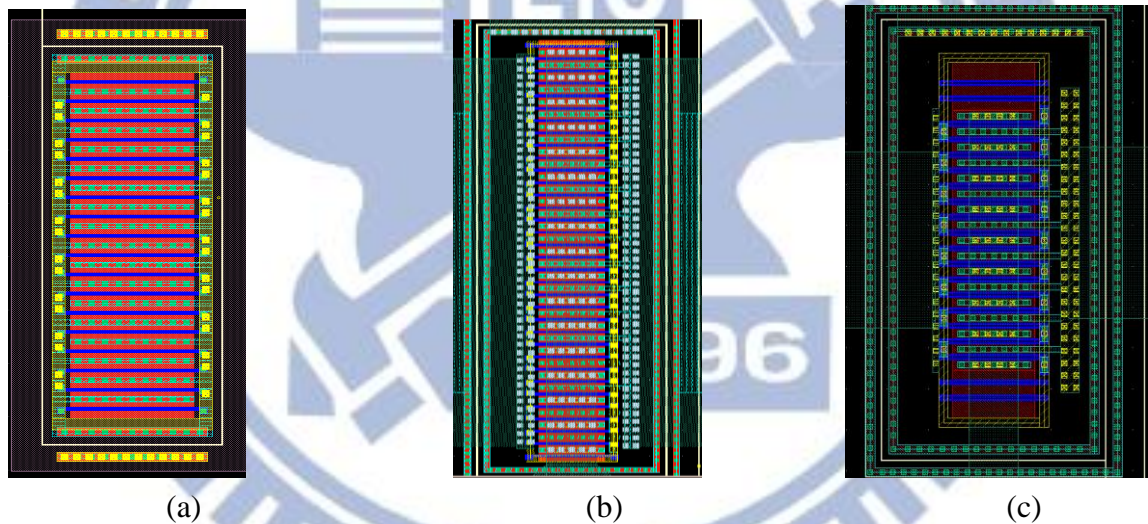
Fig. 3.1 4T RF MOSFET layouts implemented in test ships using different processes (a) UMC 65nm standard logic UN65SP (b) UMC 90nm low leakage process UN90LL (c) TSMC 90nm RF process TN90RF
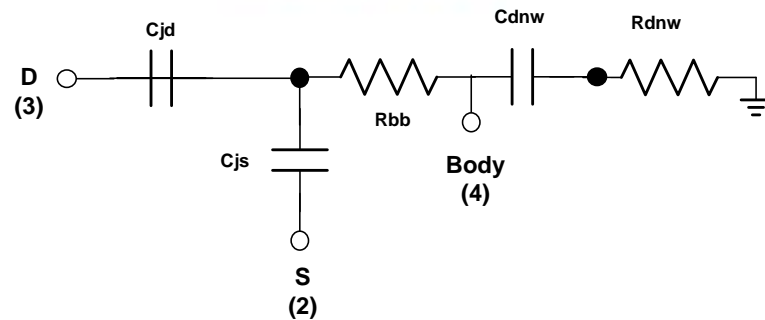
Fig. 3.2 A Simple body network model for L90709 4T RF MOSFET with deep n-well and

p-substrate connected to ground and p-well body to port-4

Table 3.1 (a) 4T RF MOSFET layouts in test chips using different processes

Processes	4T MOSFET layout features		
	body contact	deep n-well	Dummy poly
UN65sp_L65003	Parallel	Connected to body	1
UN90LL_L90709	Guarded Ring	Connected to Ground	1
TN90RF_100A	Guarded Ring	Floated	2

Table 3.1 (b) R_{bb} extracted from $Re(Y_{42})$ and $Re(Y_{43})$ under very low and very high frequencies for 4T RF MOSFETs in UN90_L90790 and UN65_L65003

4T MOSFET process/layout	Rbb (Ω)			
	$Re(Y_{43})$ (LF)	$Re(Y_{42})$ (LF)	$Re(Y_{43})$ (HF)	$Re(Y_{42})$ (HF)
L90709_W2N8	1002	729	992	869
L90709_W2N16	601	522	596	642
L90709_W2N32	372	344	368	361
L90709_W05N64	478	444	498	485
L90709_W1N32	539	486	531	567
L65003_W2N32	1050	958	385	324
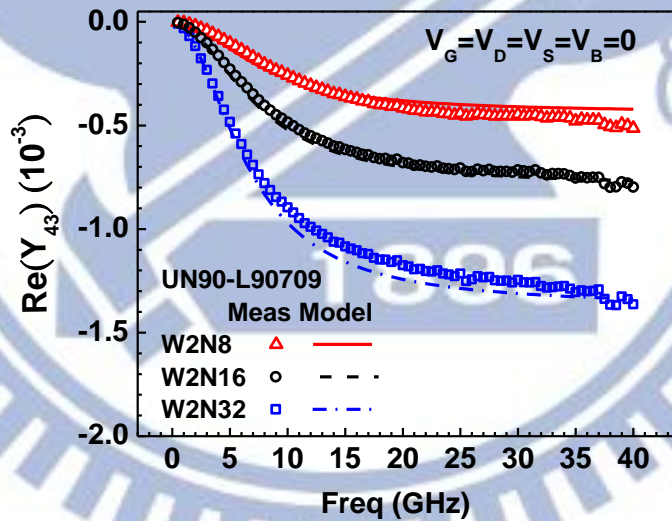
Fig. 3.3 Comparison of measured $Re(Y_{43})$ and simulated $Re(Y_{43}) = \dfrac{-\omega^2 C_{jd}(C_{jd}+C_{js})R_{bb}}{1+\omega^2(C_{jd}+C_{js})^2 R_{bb}^2}$ derived from simple body network model proposed for UN90 4T RF MOSFE layout with deep N-well connected to ground and body to port-4   (3 : drain, 4: body)
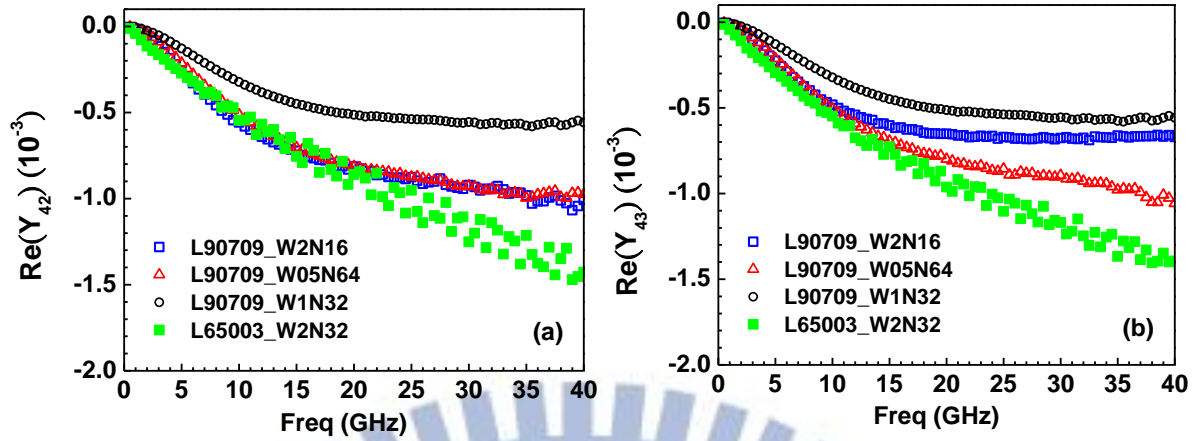
Fig. 3.4 Re(Y$_{43}$) measured from 4T RF MOSFETs in test chips UN90 L90709 and UN65 L65003 with different layouts in deep N-well, P-well body, and P-substrate summarized in table 3.1(a)
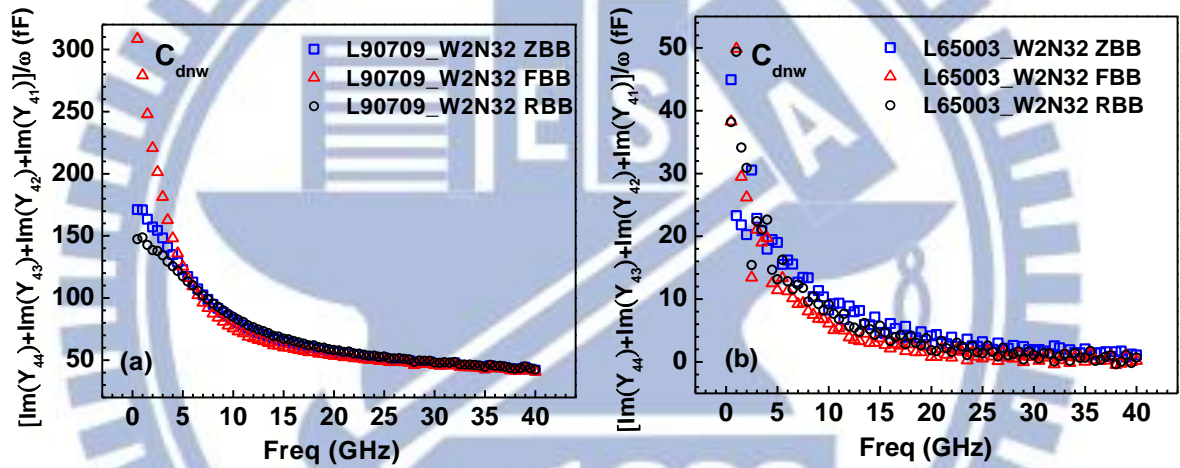
Fig. 3.5 Deep n-well to body junction capacitance C$_{dnw}$ extracted from Y-parameters at very low frequency for 4T RF MOSFET with different layouts (a)UN90 L90709 (b) UN65 L65003

3.1.2 4T MOSFET Layout Analysis for Parasitic RLC Extraction

Four-port (4-port) S-parameters measurement and deembedding are fundamental works for 4-port RF MOSFET characterization and equivalent circuit model development. As mentioned previously, the high frequency characteristics is critically determined by the layout of the core device and test structure. In generally, there are two kinds of 4-port test structures, such as 4 GSG pads (4-GSG) and 2 GSGSG pads (2-GSGSG). In this thesis, the latter one, i.e. 2-GSGSG is adopted for taking the advantages of smaller parasitic RL and small chip area due to shorter interconnection. Regarding the deembedding method, open deembedding is employed to extract and remove the parasitic capacitances and short deembedding is taken to remove the parasitic resistances (R) and inductances (L). It has been known from our previous work that parasitic capacitances are contributed from the pads, interconnection lines, and lossy substrate underneath, and dummy open pad with interconnection lines to bottom metal, namely open-M1 is necessary to realize a truly clean open deembedding. Unfortunately, open-M1 is not available in this thesis, due to limited chip area. **Fig. 3.6(a)** illustrates the layout of 4-port open deembedding structure. The parasitic capacitances associated with this open deembedding structure can be determined by 4-port Y-parameters given by (3.12)~(3.15). Note that 4 ports are assigned corresponding to 4 electrodes of the 4T RF MOSFET given by 1 : Gate (G), 2 : source (S), 3: drain (D), 4 : body (B). Fig. 3.6(b) presents the parasitic capacitances associated with gate, source, drain, and body, which were extracted from 4-port Y-parameters. The results indicate difference of around 1~5 fF in the parasitic capacitances between every two ports and reveal difference in the layout of interconnection lines to each port. Also, the significant difference between $C_{ss,open}$ and $C_{dd,open}$ suggests that layouts for interconnection to source and drain are exactly not identical and it will lead to asymmetric effect in the S- and Y-parameters between source and drain.

$$C_{gg,open} = \frac{Im(Y_{11})_{open}}{\omega} \qquad (3.12)$$

$$C_{ss,open} = \frac{\text{Im}(Y_{22})_{open}}{\omega} \quad\quad\quad\quad (3.13)$$

$$C_{dd,open} = \frac{\text{Im}(Y_{33})_{open}}{\omega} \quad\quad\quad\quad (3.14)$$

$$C_{bb,open} = \frac{\text{Im}(Y_{44})_{open}}{\omega} \quad\quad\quad\quad (3.15)$$

(a)

(b)
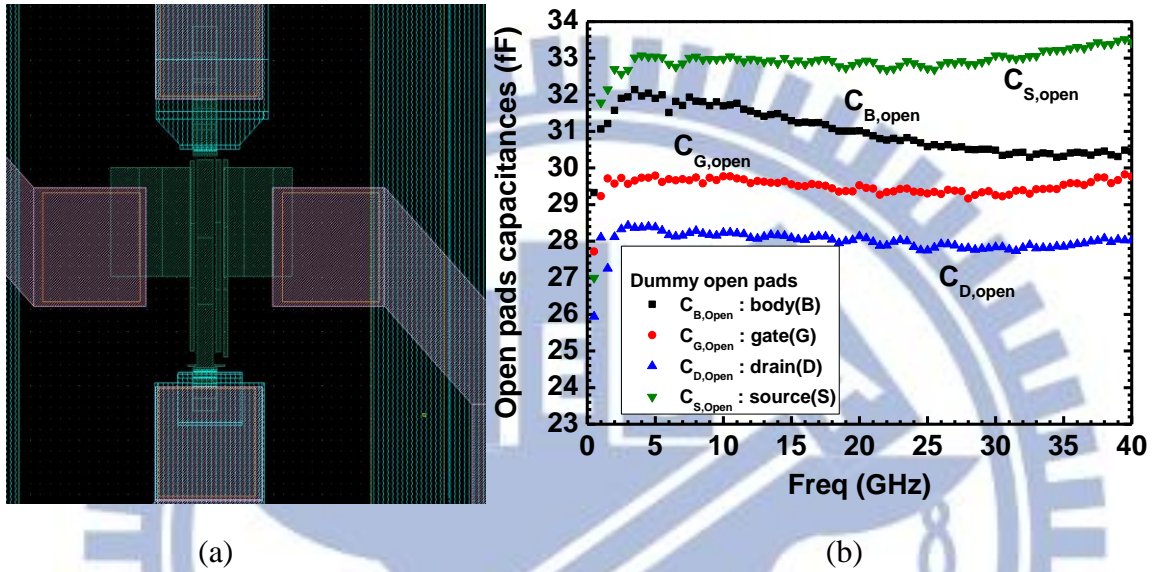
Fig. 3.6 (a) 4-port open deembedding test structure   (b) parasitic capacitances of dummy open pads

3.1.3 4-port RF MOSFET Measurement and De-embedding Method

■ 4-port S-parameters measurement system setup

Fig. 3.7 illustrates the equipments configuration for 4-port S-parameters measurement. This system incorporates Agilent PNA E8364B、test set N4421 for extending 2-port to 4-port and Agilent 4155 for DC parameter analyzer as shown Fig. 3.8. Note that RF cables and adapters are selected with the spec. of 2.4 mm to enable RF measurement up to 50 GHz. The off chip calibration before on-wafer measurement, namely short-open-load-thru (SOLT) is carried out through programmable control of wincal, which is offered by cascade.

■ **DC measurement setup**

I-V measurement for DC characterization was performed using another system to avoid any change to the configuration of the 4-port S-parameters measurement system. This arrangement comes from the consideration that the 4-port S-paramters system with special configuration is not suitable for simultaneous measurement of S-parameters and DC parameters. In this work, the system for low frequency noise measurement as shown in Fig. 3.9 and Fig. 3.10 is utilized for DC measurement. The basic criterion to approve this approach is that the DC parameters measured by using mentioned two systems should be consistent for the same device and it has been proven through our verification.

■ **De-embedding methods**

For the purpose of extracting MOSFET parameters from measured data, the on-chip RF measurement is adopted. After calibration of measurement system, we suppose to make the reference planes be located at the probe tips, as shown in Fig. 3.11. The rest work is focused on that how we get device parameters from measured data which excludes parasitic effects by using de-embedding method.

Open de-embedding

The open pad is the full structure only taken off device. Before doing any de-embedding step,

we have to transform measured S-parameter data of device with pads into measured Y-parameter data. The representation is shown as **Fig. 3.12**. Also, the measured S-parameter data of open pad have to be transformed into measured Y-parameter data.

From **Fig. 3.13** of open pad equivalent circuit and **Fig. 3.12**, we can construct the Y-parameter matrices to represent open pad and device with pads.

$$S_{mea} \rightarrow Y_{mea} \tag{3.16}$$

$$S_{open} \rightarrow Y_{open} = \begin{bmatrix} Y_{C1a} + Y_{C1b} & -Y_{C12} & -Y_{C13} & -Y_{C14} \\ -Y_{C12} & Y_{C2a} + Y_{C2b} & -Y_{C23} & -Y_{C24} \\ -Y_{C13} & -Y_{C23} & Y_{C3a} + Y_{C3b} & -Y_{C34} \\ -Y_{C14} & -Y_{C24} & -Y_{C34} & Y_{C4a} + Y_{C4b} \end{bmatrix} \tag{3.17}$$

$Y_{C1a(b)}$, $Y_{C2a(b)}$, $Y_{C3a(b)}$ and $Y_{C4a(b)}$ are coupling parameters between pads and reference ground. Y_{CXY} is the coupling parameter between two ports.

So far, we can use equation (3.16) and (3.17) to do the open de-embedding. The coupling parameters included in Y_{mea} can be de-embedded by this way.

$$Y_{mea\_o} = Y_{mea} - Y_{open} \tag{3.18}$$

But remember that the $Z_{RL1} \sim Z_{RL3}$ parameters are still remained in Y_{mea_o} matrix.
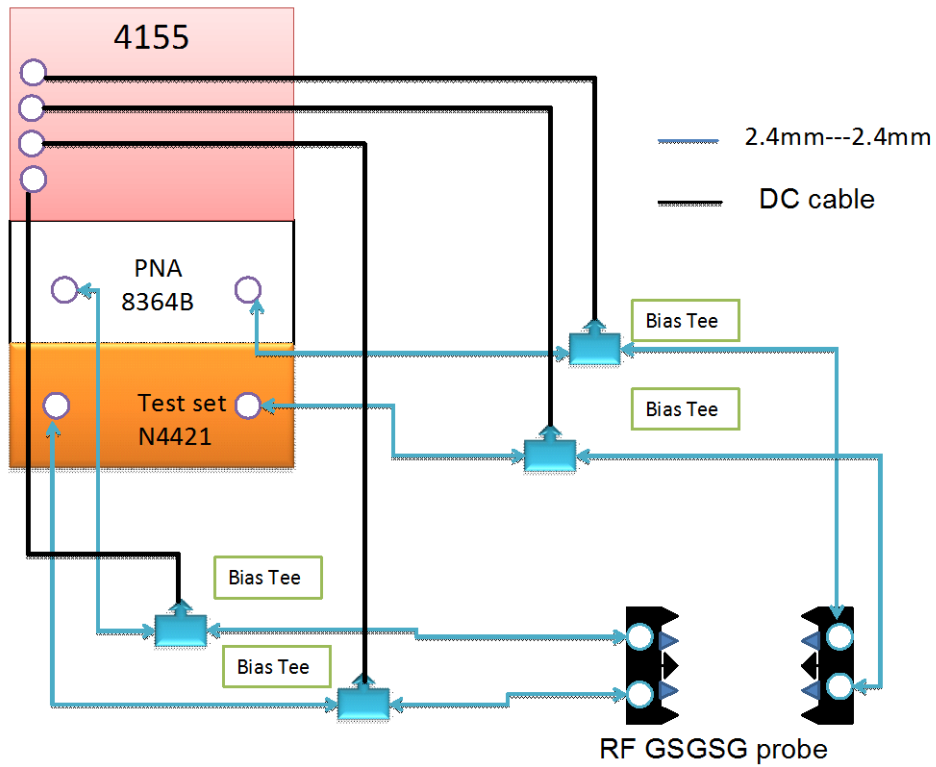
Fig. 3.7 4 port S-parameters measurement setup including Agilent PNA E8364B, test set N4421, bias-Tee, RF cables, and adapters with 2.4mm spec. for high frequency measurement up to 50 GHz.

(a)

(b)

(c)

Fig. 3.8 Measurement equipments (a)Agilent PNA E8364B (b) 4-port test set Agilent N4421 (c) DC parameters analyzer Agilent 4155
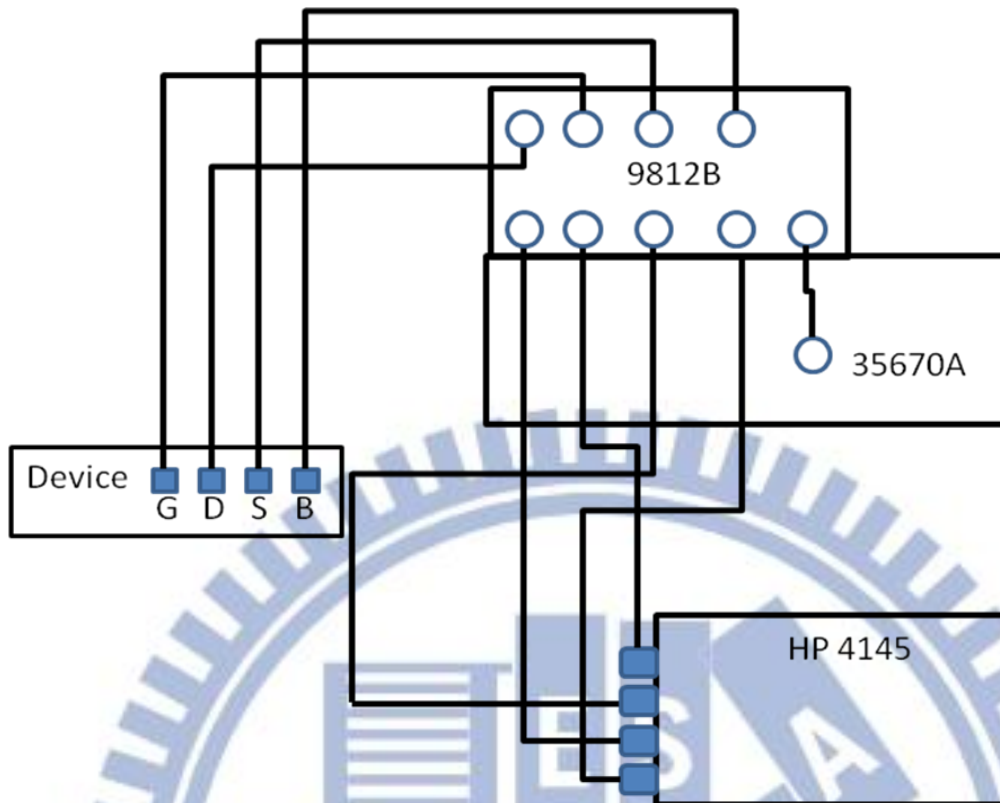
Fig. 3.9 Low frequency noise measurement system setup
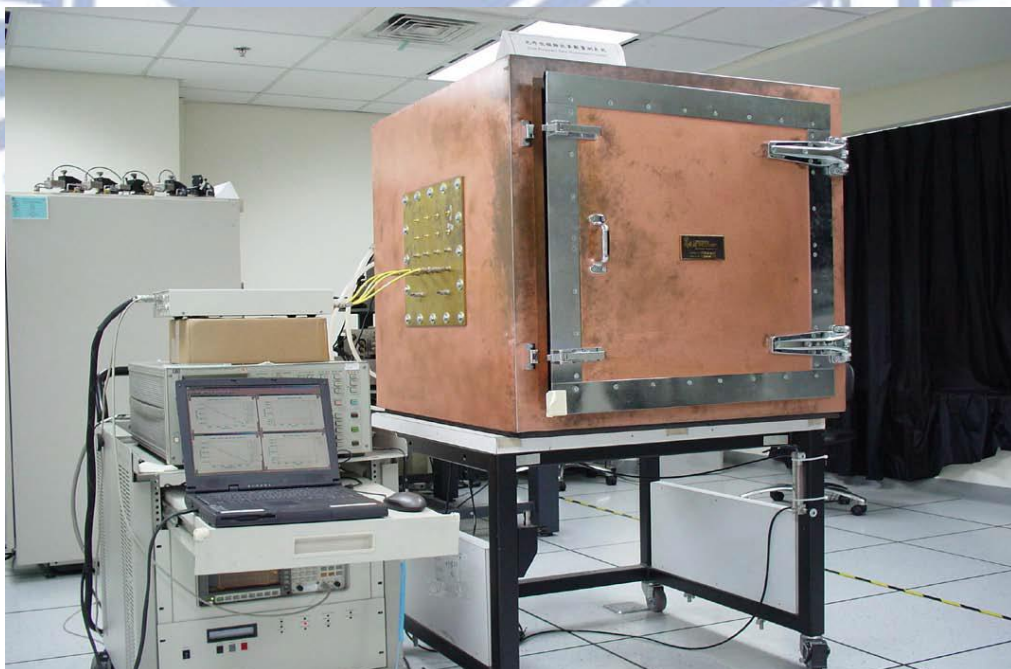
Fig. 3.10 Low frequency noise measurement system in NDL
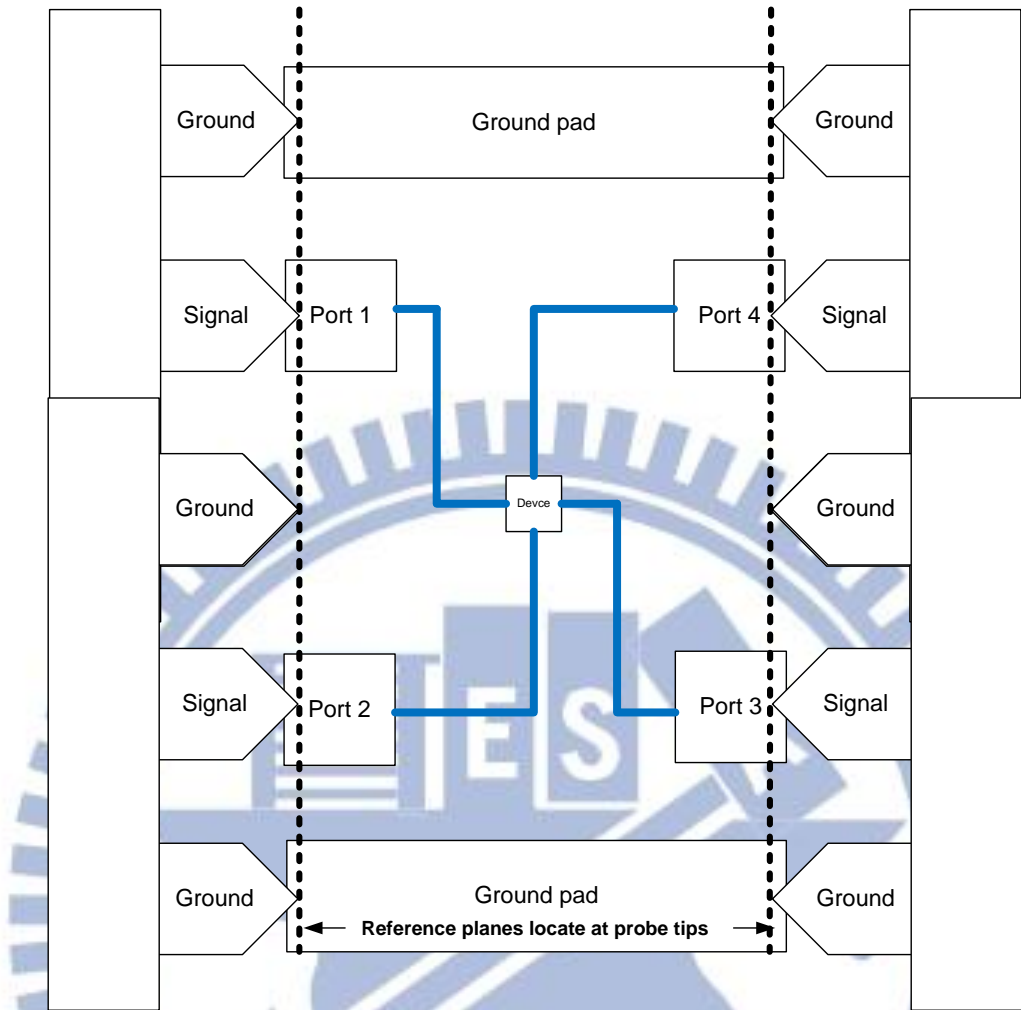
Fig. 3.11 Four-port test structure 2-GSGSG for 4-port S-parameters measurement
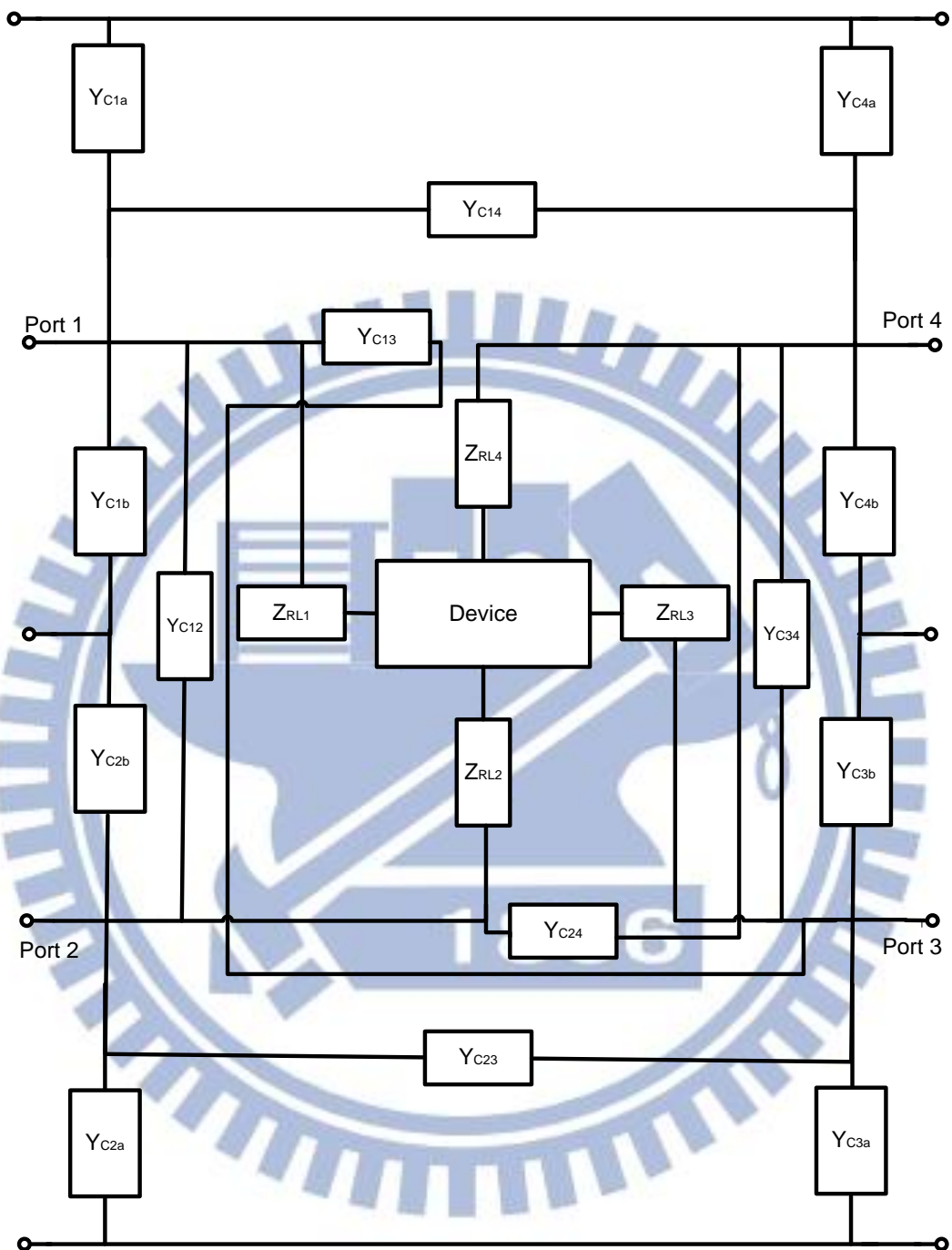
Fig. 3.12 The equivalent circuit of a 4-port test structure with DUT and pads
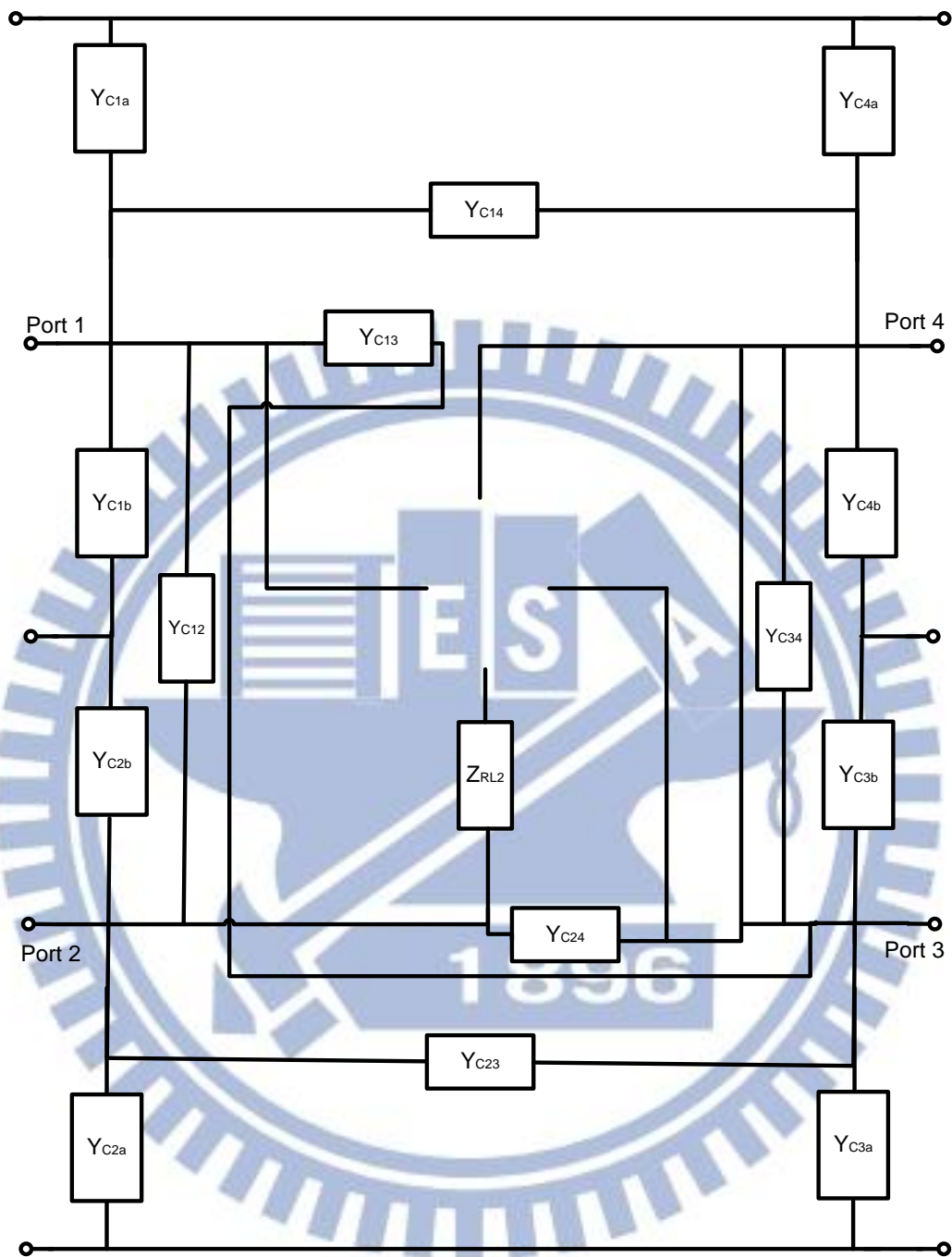
Fig. 3.13 The equivalent circuit of 4-port dummy open pads for open deembedding

3.1.4 4-port RF MOSFET Parasitic RLC Extraction Results and

Comparison with 2-port Structure

According to the pads layout for 4-port test structure and interconnect configuration for DC

measurement as shown in **Fig. 3.14,** the parasitic resistances can be identified coming from two

major sources, such as on-chip pads to DUT interconnection lines denoted as $R_{S(DUT)}$ and off-chip DC cables denoted as $R_{S(Cable)}$.

$$R_s \cong R_s \big|_{DC-cable} + R_s \big|_{DUT}$$
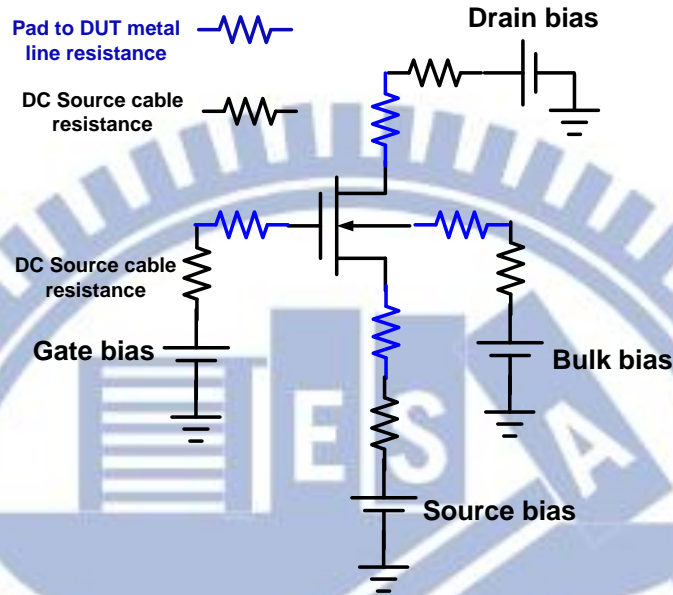
Fig. 3.14 The schematics of 4-port equivalent circuit incorporating parasitic resistances from off-chip DC cables and on-chip interconnection lines.

The aggressive device scaling driven by CMOS technology advancement can boost the gate speed and cut-off frequency, attributed to gate length scaling and driving current enhancement. However, the merit achievable from device scaling is limited to the ideally intrinsic devices, which are free from parasitic resistances(R), capacitances(C), and inductance (L). In practice, the parasitic RLC cannot be eliminated to zero, under either chip operation or measurement and the merit from device scaling will be degraded. The impact of parasitic resistances on I-V characteristics can be identified from the I-V measurement on UN65 and UN90 RF MOSFETs in 2-port and 4-port test structures, as shown in **Fig. 3.15(a)** and (b), respectively. It has been known from our previous study that 4-port test structures generally lead to current degradation, due to longer interconnection line from the pads to DUT. As shown in **Fig. 3.15(a),** UN65 4-port n-MOSFET (W2N32) in L65003 reveals I_{dsat} degradation as high as 21.63%, as

compared with that of 2-port n-MOSFET in L65909. Note that the adoption of DC bias-Tee in L65909 measurement is another key factor for suppressing parasitic resistance effect and improving I_{dsat}. As for UN90 n-MOSFET shown in **Fig. 3.15(b),** the comparison between 2-port and 4-port nMOSFET (W2N16) indicates I_{dsat} degradation of around 10.16%, which is only half that of UN65 devices. The results suggest the higher driving current, the more degradation from the parasitic resistance.

(a)   (b)
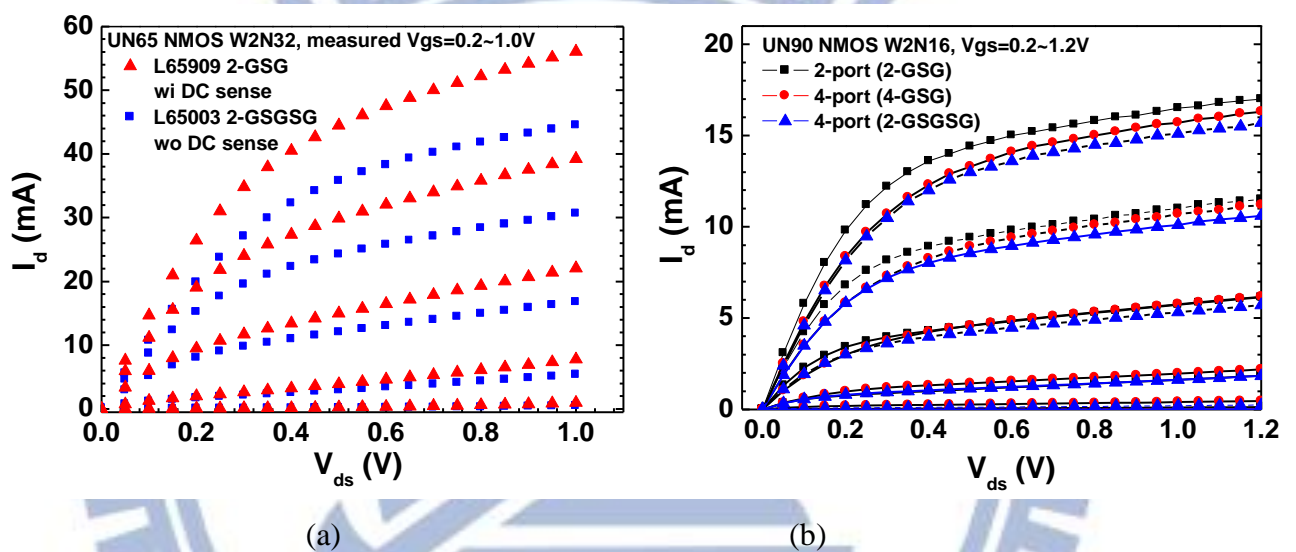
Fig. 3.15 The Ids-Vds measured from RF MOSFET W2N32 (a) 65nm devices : comparison between 2-port tester (2-GSG) in L65909 and 4-port tester (2-GSGSG) in L65003 (b) 90 nm devices in L90709 : comparison between 2-GSG, 4-GSG, and 2-GSGSG.

Presently, the 4-port S-parameters measurement system set up by NDL RF Lab. doesn't incorporate bias Tee with DC sense and cannot eliminate DC cable resistance when offering the DC voltage. **Table 3.2** summarizes the configurations for DC I-V measurement, 2-port S-parameters, and 4-port S-parameters for a comparison.

According to the comparison of I-V characteristics for RF MOSFET with the same dimension (W2N32), measured from 2-port tester in L65909 and 4-port tester in L65003, shown in **Fig. 3.15(a)**, the total parasitic resistance contributed from off-chip DC cable and on-chip

35

interconnection line is around 2Ω.The former, i.e. DC cable resistance can be measured by I-V meter (三用電表) and the result is around 1Ω.It suggests that the latter, i.e. pad-to-DUT interconnection line contributes remaining 1Ω.The assumed parasitic resistances were employed in the 4-port RF MOSFET for I-V simulation (BSIM-4) and the results shown in **Fig. 3.16** indicates a good match between the measured and simulated I_{ds}-V_{ds} under various V_{gs}. The good agreement justifies the accuracy of the assumed parasitic resistance.

Table 3.2 The configurations for DC I-V measurement, 2-port and 4-port S-parameters measurement

	DC measurement	2 port S parameter	4 port s parameter
Bias Tee	N	Y	Y
Power supply with DC sence	N	Y	N
Power supply	HP4145	HP4142	HP4155
Bias Tee with DC sence	N	Y	N
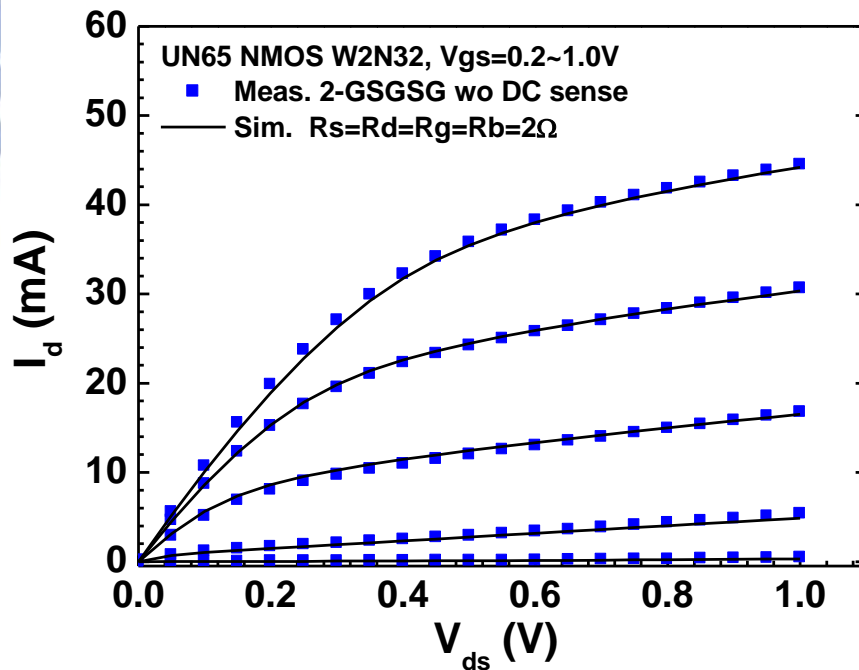
Fig. 3.16 Comparison of the measured and simulated I_{ds}-V_{ds} under various V_{gs} (0.2~1.0V) for 4-port RF NMOS W2N32 (65 nm L65003). Parasitic resistances at 4 terminals, Rs=Rd=Rg=Rb=2Ω were employed for I-V simulation

Due to the mentioned restriction of 4-port S-parameters measurement system currently available in NDL RF Lab., DC cable resistance cannot be removed from the measured I-V characteristics. Subsequently, the transcondutance g_m derived from I_{ds}-V_{gs}, i.e. $g_m=dI_{ds}/dV_{gs}$ cannot avoid the influence from the cable resistance and the g_m degradation may become significant for DUT with larger dimension and higher current. 。For I-V and large signal simulation performed by BSIM-4, the parasitic resistances from off-chip DC cable and on-chip interconnection lines have to be considered. As for small signal equivalent circuit simulation, it is assumed that the DC bias shift due to DC cable resistance can be neglected. The assumption comes from the fact that S-parameters measurement under normal condition is performed with bias Tee with DC sense, which can eliminate the effect of DC cable resistance. Furthermore, the g_m from small signal measurement is derived from the Y-parameters after open and short deembedding, which can eliminate the effect of pads to DUT interconnection lines resistance. To verify the assumption, the impact of DC cable resistance on g_m from large signal I-V and small signal Y-parameters was investigated by BSIM simulation, as shown in **Fig. 3.17**. The g_m from large signal I-V is apparently lower than those from Y-parameters with or without DC cable resistance and the later one indicates very minor sensitivity to DC cable, due to bias Tee effect (with DC sense). Unfortunately, the 4-port S-parameters measurement system currently available at NDL RF Lab. doesn't incorporate bias Tee with DC sense. Due the undesired restriction, DC cable resistance effect cannot eliminated from g_m even using small signal measurement and the measured g_m is always smaller compared to the intrinsic g_m. However, the g_m degradation due to mentioned on-chip and off-chip parasitic resistances can be reduced by using Y-parameters than that determined I-V method.
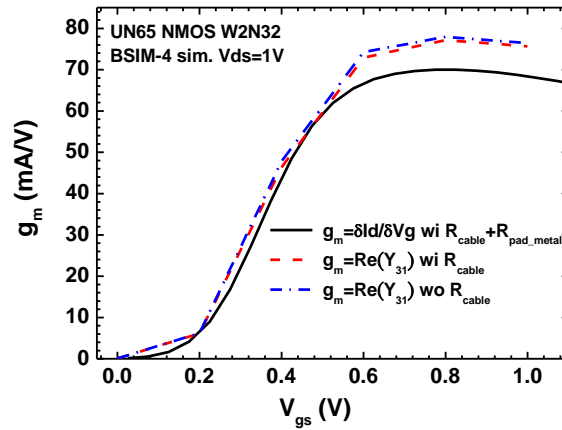
Fig. 3.17 Comparison of simulated g_m-V_{gs} at V_{ds}=1.0V for 4-port RF NMOS W2N32 (65 nm L65003) under three conditions : I-V characteristics, Y-parameter without DC cable resistance, and Y-parameters with DC cable resistance.
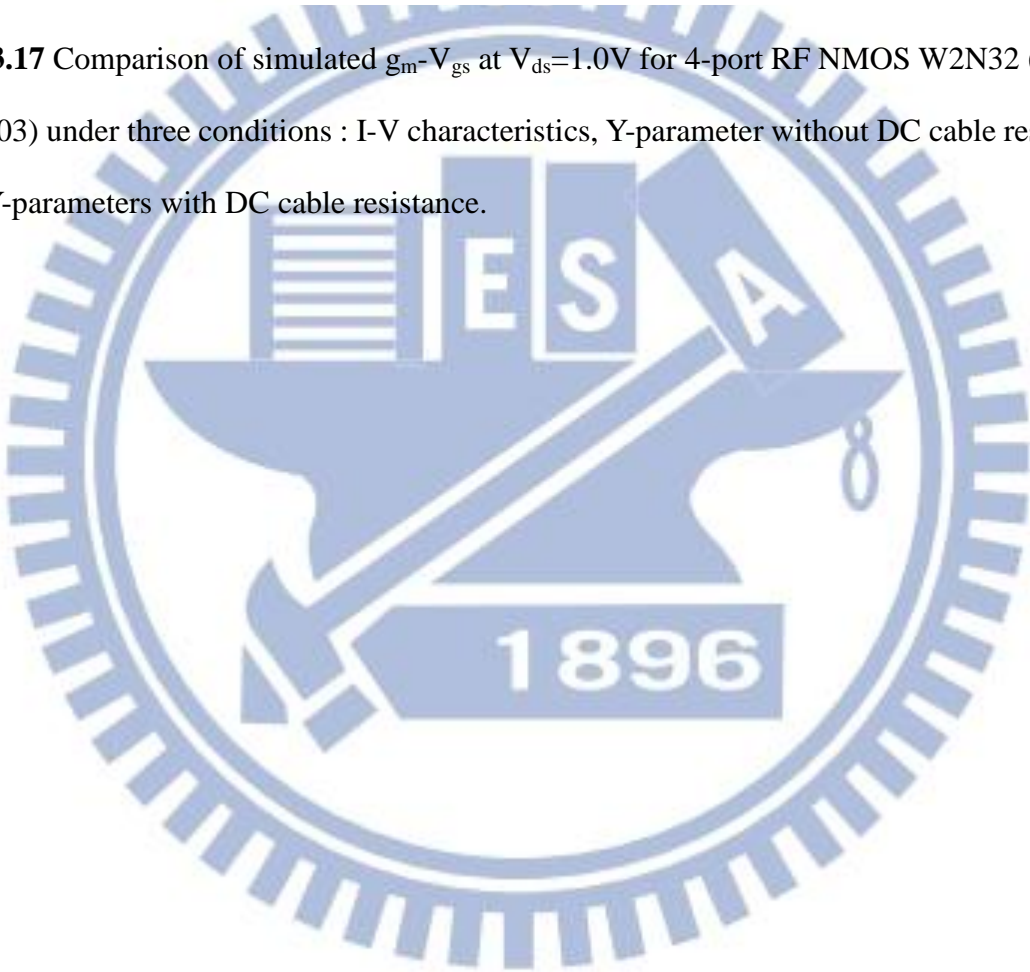
3.2 Improved Body Network Model for Four-port RF MOSFET with DBB

4-port RF MOSFET was implemented in this work to allow the adoption of dynamic body biases (DBB). An appropriate application of DBB can realize low voltage and low power at active state under forward body bias (FBB) and low leakage power at standby state under reverse body bias (RBB). However, the first challenge to RF CMOS circuits design using 4-port MOSFETs with DBB is lacking a reliable and accurate 4T MOSFET model for RF circuits simulation. Furthermore, body network model is identified as the most critical element, which will determine the simulation accuracy under DBB. In the following, different body network models published by previous work will be reviewed in sec. 3.2.1. Then, a new body network model proposed in this thesis and the model parameters extraction method will be presented in sec. 3.2.2. This new body network model developed based on 4-port S-parameters measured from UN65 L65003 can be deployed in BSIM-4 for a benchmark with default model to verify the simulation accuracy under DBB. Note that Agilent ADS is employed to perform high frequency simulation in this study.

3.2.1 Review of Previous Work

In recent two decades, substrate network model becomes an important topic in the area of RF CMOS and different models have been publishe[5]-[16]. However, most of the works have been focused on some minor modifications on the simplest model, i.e. single resistor model [5]-[6]. Substrate network model is not available in BSIM-3 and it allows the freedom of deploying different external networks[7]-[9]. A π-type substrate network with 4 bulk resistors was proposed as a direct extension to BSIM-3 to improve simulation accuracy of output characteristics, such as S_{22} and R_{out} at high frequencies [8]. However, this π-type substrate network model requires an extensive modification to BSIM-3 and makes the parameters extraction more complicated **[8].** A simplified lumped resistance model with 3 resistors (one gate resistor and two substrate resistors) was proposed to reduce the complexity in parameters extraction and maintain the simulation accuracy for both RF and baseband

circuits [9]. As for BSIM-4, an internally built substrate network with 5 resistors is a modified version, trying to enhance the simulation accuracy [10]. Substrate network models with parallel RC instead of simple resistance network were proposed to improve modeling accuracy at high frequency[11]-[12]. In summary, the trade-off between the curve fitting capability and difficulty in parameters extraction becomes one of the major limitations.

One more fundamental limitation comes from the two-port measurement in which common source (body and source shorted to ground) or common gate (gate shorted to ground) configurations is the only choice and hinders the direct probing and extraction of the parasitic resistances (inductance and capacitances) at 4 individual terminal (G, S, D, B). The former one, i.e. common source configuration (topology) has been most widely used but leads to the difficulty in substrate network parameters extraction[5]-[12]. The latter one, i.e. common gate configuration is an alternative solution to access the substrate from source and drain terminals [13]. As for the condition that gate is ac shorted to the body, the gate network is visible through the gate/source and gate/drain admittances [13]. No matter which configuration is taken, the parasitic elements extracted from 2-port S-parameters cannot be identical with those actually existing in 4T MOSFET, due to the fundamental differences in interconnection lines routing between the 2-port and 4-port test structures. Also, the verification of simulation accuracy is limited to 2-port characteristics, which is insufficient for 4-port circuits design allowing DBB. Three port measurement was employed to enable an analytical parameter extraction method for a π-type substrate resistance network and the simulation was verified up to 110 GHz [14]. However, the fitting results as demonstrated were limited to the real part of output admittance, i.e. $Re(Y_{dd})$ and the substrate (body) related parameters were not available. Four port measurement was implemented for a direct extraction of a T-type substrate network with 3 resistors and the simulation results was verified to 26.5 GHz [15]. Again, the curve fitting result was limited to $Re(Y_{22})$ (2: drain) and the body bias effect was not available, eventhough 4-port measurement was carried out. The last limitation is that most

of the existing models is restricted to test structure without deep n-well and the deep n-well related components are not available in the substrate (body) network model. The mentioned limitation makes it fail to capture the important feature, such as deep n-well to p-well (body) and to p-substrate coupling effects. A standard test structure adopting deep n-well was fabricated and T-type substrate network with parallel RC instead of simple resistors was proposed to improve simulation accuracy up to 40 GHz [16]. However, this work is still limited to 2-port S-parameters and the verification is limited to $Re(Y_{22})$ (2: drain). **Fig. 3.18(a)~(e)** summarize the equivalent circuit schematics for different substrate network models published in previous work [5]-[16].

To fix the problems as mentioned for the existing substrate network models, a new body network model is developed in this thesis, based on 4-port RF MOSFETs built with deep n-well on p-substrate and the measured 4-port S-parameters. Note that **body** network model instead of substrate network model is named in this thesis, to make a clear definition that p-well body is separated from p-substrate by the deep n-well surrounding the p-well body itself. Fig. 3.18(f) illustrates the circuit blocks diagram in which body network and substrate network are separated to represent equivalent circuit associated with p-well body enclosed by deep n-well and p-substrate outside the deep n-well. In the following, we will introduce an improved body network model and have a detailed description of the equivalent circuit schemes and model parameters extraction methods.

(a)   (b)
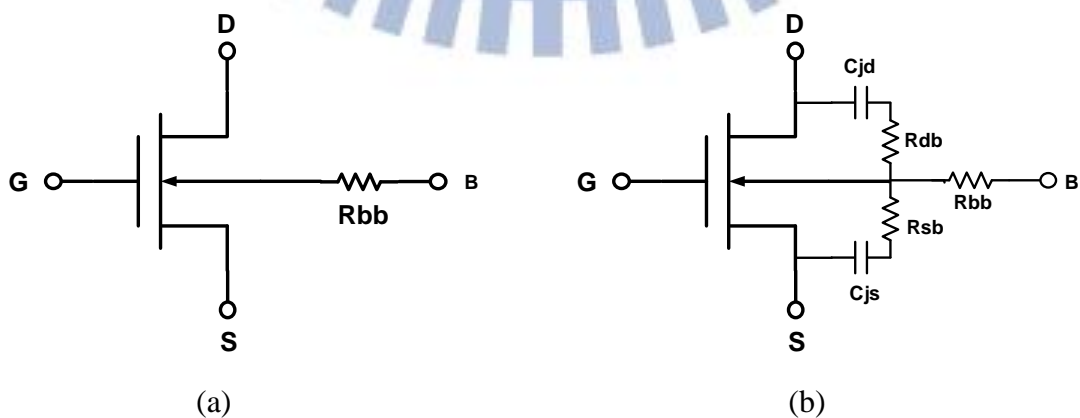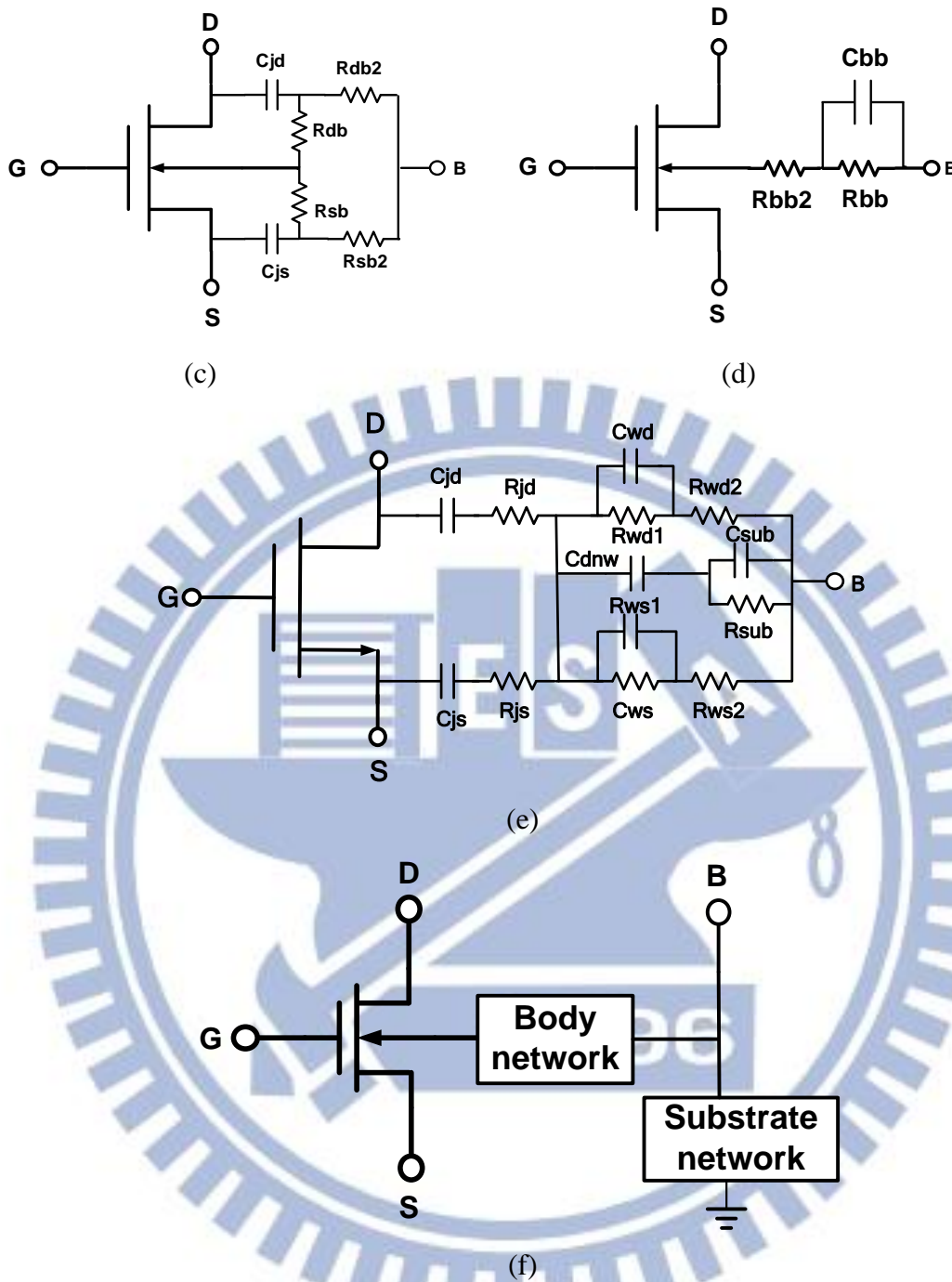
Fig. 3.18 (a) Substrate network modeled by a single resistor. [5]-[6] (b) T-type substrate network [13],[15]. (c) Ω-type substrate network. [8], [14] (d) RC parallel substrate network. [11]-[12] (e) substrate network in [16]. (f) The schematic diagram of body network and substrate network.

3.2.2 Improved Body Network Model-Equivalent Circuit and Extraction Method

According to the comments made in 3.1.1, the simple body network model proposed for L90709 (**Fig. 3.2**) cannot be applied to L65003, owing to different layout in the interconnection to p-well body and deep n-well. Due to the fact, a new body network becomes indispensable for 4-port RF MOSFET in L65003. First, the device structure of the 4-port MOSFET designed in L65003 is illustrated in **Fig. 3.27** to facilitate the body network model development. Herein, R_{bb} represents the body resistance associated with p-well, R_{dnw} is the series resistance going through the deep n-well, and R_{bb2} as well as R_{bb3} denote p-substrate resistance. Regarding the capacitive components, C_{js} and C_{jd} are well known as the source and drain to body junction capacitances. C_{dnw1} and C_{dnw2} define the junction capacitances from deep n-well to p-well and p-substrate, respectively. Based on the device structure and RC components allocation defined in **Fig. 3.19**, an equivalent circuit can be derived as shown in **Fig. 3.20**. Note that the RC network in the solid-line box is composed of R_{bb3} in parallel with the series $R_{bb2}C_{dnw2}$ and the equivalent impedance is defined as Z_{sub}. As for the RC network in the dash-line box, it is consisted of R_{bb} in parallel with the series $R_{bb}C_{dnw1}$ and the equivalent impedance is defined as $Z_{bb}{}'$. The idea underlying the proposed RC network comes from the strong frequency dependence of $Re(Z_{44})=Re(Z_{sub})$ as shown in **Fig. 3.21,** which was measured from port-4 (body) when all the other 3 ports (1 : G, 2 : D, 3 : S) are at open state. The fast fall off of $Re(Z_{44})$ when increasing frequency and saturation to a constant when beyond 5 GHz suggests a large resistance at very low frequency (due to low open circuit) but fast decay at higher frequency, due to parallel resistors effect from high pass circuit. The proposed mechanism can be simulated by the substrate RC network denoted by solid-line box in **Fig. 3.20** and shown in **Fig. 3.22 (a)** in which $Re(Z_{44})$ at very low frequency is equivalent to R_{bb3} due to open circuit of series $R_{bb3}C_{dnw2}$ but $Re(Z_{44})$ at very high frequency approach $R_{bb3}//R_{bb2}$ (R_{bb3} and R_{bb} in parallel) due to high pass of C_{dnw2}. According to the proposed RC network,

$Z_{44}=Z_{sub}$ can be derived as given by (3.19). Note that Z_{sub} can be approximated by (3.20) when operating at very low frequency, i.e. $\omega^2 C_{dnw2}^2 (R_{bb2}+R_{bb3})^2 \ll 1$ and then R_{bb3} can be extracted from $Re(Z_{sub(LF)})$ given by (3.21). As for very high frequency, $Re(Z_{sub(HF)})$ is given by(3.22), which is equal to $R_{bb3}//R_{bb2}$. The experimental data of $Re(Z_{sub(LF)})$ and $Re(Z_{sub(HF)})$ can be determined from **Fig. 3.21** and then the initial values of R_{bb2} and R_{bb3} can be extracted from (3.21) and(3.22).

$$Z_{sub}=R_{bb3}\bullet\frac{1+\omega^2 C_{dnw2}^2 R_{bb2}(R_{bb2}+R_{bb3})-j\omega C_{dnw2}R_{bb3}}{1+\omega^2 C_{dnw2}^2 (R_{bb2}+R_{bb3})^2} \tag{3.19}$$

At very low frequency

$$\omega^2 C_{dnw2}^2 (R_{bb2}+R_{bb3})^2 \ll 1$$

$$\omega^2 C_{dnw2}^2 R_{bb2}R_{bb3}(R_{bb2}+R_{bb3}) \ll 1$$

then

$$Z_{sub[LF]} \cong R_{bb3}-j\omega C_{dnw2}R_{bb3}^2 \tag{3.20}$$

$$Re(Z_{sub[LF]}) \cong R_{bb3} \tag{3.21}$$

At very high frequency

$$\omega^2 C_{dnw2}^2 (R_{bb2}+R_{bb3})^2 \gg 1$$

$$\omega^2 C_{dnw2}^2 R_{bb2}R_{bb3}(R_{bb2}+R_{bb3}) \gg 1$$

then

$$Re(Z_{sub[HF]}) \cong \frac{R_{bb2}R_{bb3}}{(R_{bb2}+R_{bb3})} \tag{3.22}$$

It can be understood

$$Re(Z_{sub[LF]}) \cong R_{bb3} > \frac{R_{bb2}R_{bb3}}{(R_{bb2}+R_{bb3})} \cong Re(Z_{sub[HF]})$$

Regarding the frequency dependence of $Re(Z_{sub})$ shown in **Fig. 3.21**, C_{dnw2} plays a key role and has to be taken into account. C_{dnw2} can be determined from $Y_{sub}=1/Z_{sub}$ at very low

frequency, according to (3.23)-(3.26).

$$Y_{sub} = \frac{1}{Z_{sub}} = \frac{1+\omega^2 C_{dnw2}^2 R_{bb2}(R_{bb2}+R_{bb3})+j\omega C_{dnw2}R_{bb3}}{R_{bb3}\left[1+(\omega C_{dnw2}R_{bb2})^2\right]}$$ (3.23)

At very low frequency,

$$(\omega C_{dnw2}R_{bb2})^2 \ll 1 \Rightarrow 1+(\omega C_{dnw2}R_{bb2})^2 \cong 1$$

$$Y_{sub(LF)} \cong \frac{1}{R_{bb3}} + (\omega C_{dnw2}R_{bb2})^2\left(\frac{1}{R_{bb3}}+\frac{1}{R_{bb2}}\right)+j\omega C_{dnw2}$$ (3.24)

$$\text{Im}(Y_{sub(LF)}) \cong \omega C_{dnw2}$$ (3.25)

$$C_{dnw2} = \frac{\text{Im}(Y_{sub(LF)})}{\omega} = \frac{1}{\omega}\text{Im}\left(\frac{1}{Z_{sub(LF)}}\right) = \frac{1}{\omega}\text{Im}\left(\frac{1}{Z_{44(LF)}}\right)$$ (3.26)

The accuracy of the proposed substrate RC network model and the extracted model parameters, such as R_{bb2}, R_{bb3}, and C_{dnw2} has been verified and proven by good agreement with the measured data, as shown in **Fig. 3.21**.

Considering that the structure of p-well/deep n-well is similar to p-sub/deep n-well, the proposed RC network can be extended to p-well(body)/ deep n-well, by adding **body RC network,** as shown in **Fig. 3.22(b)**. According to this body RC network defined by dash-line box in Fig. 3.20, the equivalent impedance Z_{bb}' can be derived as given by (3.27). Similar with the analysis made on Z_{sub}, Z_{bb}'$_{(LF)}$ representing Z_{bb}' at very low frequency can be approximated by (3.27) and then R_{bb} can be extracted from $\text{Re}(Z_{bb}$'$_{(LF)})$ following (3.29). As for very high frequency, Z_{bb}'$_{(HF)}$ can be approximated by (3.30) and $\text{Re}(Z_{bb}$'$_{(HF)})$ is equal to R_{bb}//R_{dnw} (R_{bb} in parallel with R_{dnw}), as expressed by (3.31).

$$Z_{bb}' = R_{bb}\bullet\frac{1+\omega^2 C_{dnw1}^2 R_{dnw}(R_{dnw}+R_{bb})-j\omega C_{dnw1}R_{bb}}{1+\omega^2 C_{dnw1}^2(R_{dnw}+R_{bb})^2}$$ (3.27)

At very low frequency,

$$\omega^2 C_{dnw1}^2(R_{dnw}+R_{bb})^2 \ll 1 \text{ and } \omega^2 C_{dnw1}^2 R_{dnw}(R_{dnw}+R_{bb}) \ll 1$$

$$Z_{bb}'_{(LF)} \cong R_{bb} \cdot (1 - j\omega C_{dnw1} R_{bb}) \tag{3.28}$$

$$\text{Re}(Z_{bb}'_{(LF)}) \cong R_{bb} \tag{3.29}$$

At very high frequency,

$$\omega^2 C_{dnw1}^2 (R_{dnw} + R_{bb})^2 \gg 1 \quad \text{and} \quad \omega^2 C_{dnw1}^2 R_{dnw}(R_{dnw} + R_{bb}) \gg 1$$

$$Z_{bb}'_{(HF)} \cong \frac{R_{dnw} R_{bb}}{(R_{dnw} + R_{bb})} - \frac{j}{\omega C_{dnw1}} \left(\frac{R_{bb}}{R_{dnw} + R_{bb}} \right)^2 \tag{3.30}$$

$$\text{Re}(Z_{bb}'_{(HF)}) \cong \frac{R_{dnw} R_{bb}}{(R_{dnw} + R_{bb})} \tag{3.31}$$

Unfortunately, Z_{bb}' cannot be measured directly and the RC components associated with the body network cannot be extracted simply following (3.28)~(3.31). The solution to treat this problem is to extract the resistances from $\text{Re}(Y_{44})$ under very high frequency, as given by(3.32). Y_{44} is measured from port-4 (body) with all of the other 3 ports at short state. It can be understood that all of the capacitors become high pass circuits at very high frequency and $\text{Re}(Y_{44})$ can be approximated as two groups of parallel resistors, such as $R_{bb3}//R_{bb2}$ for substrate network and $R_{bb}//R_{dnw}$ for body network, as expressed by (3.32). Then, R_{dnw} can be determined by (3.33) with previously extracted R_{bb2} and R_{bb3} and R_{bb} from $\text{Re}(Y_{42})$ or $\text{Re}(Y_{43})$ at very low frequency, as given by (3.3) or (3.4).

Fig. 3.23 outlines the extraction flow for this new body network model. **Table 3.3 (a)** presents the initial and optimized values of R_{bb2} and R_{bb3}. **Table 3.3 (b)** summarizes a complete set of the resistances extracted according to the flow in **Fig. 3.23** and also the body bias dependence under ZBB, FBB, and RBB. Again, the accuracy of the proposed body network model and the extracted model parameters was verified by a comparison between the measured and simulated Re(Y44) as shown in **Fig. 3.24**. Note that the simulated results indicate a good match with measurement under various body biases, i.e. ZBB(V_{bs}=0), FBB (V_{bs}=0.6V), RBB (V_{bs}= -0.6V).

46

$$\text{Re}(Y_{44(HF)}) \cong \left(\frac{1}{R_{bb}} + \frac{1}{R_{dnw}} \right) + \left(\frac{1}{R_{bb2}} + \frac{1}{R_{bb3}} \right) \tag{3.32}$$

$$R_{dnw} = \frac{1}{\text{Re}(Y_{44(HF)}) - \left(\dfrac{1}{R_{bb}} + \dfrac{1}{R_{bb2}} + \dfrac{1}{R_{bb3}} \right)} \tag{3.33}$$
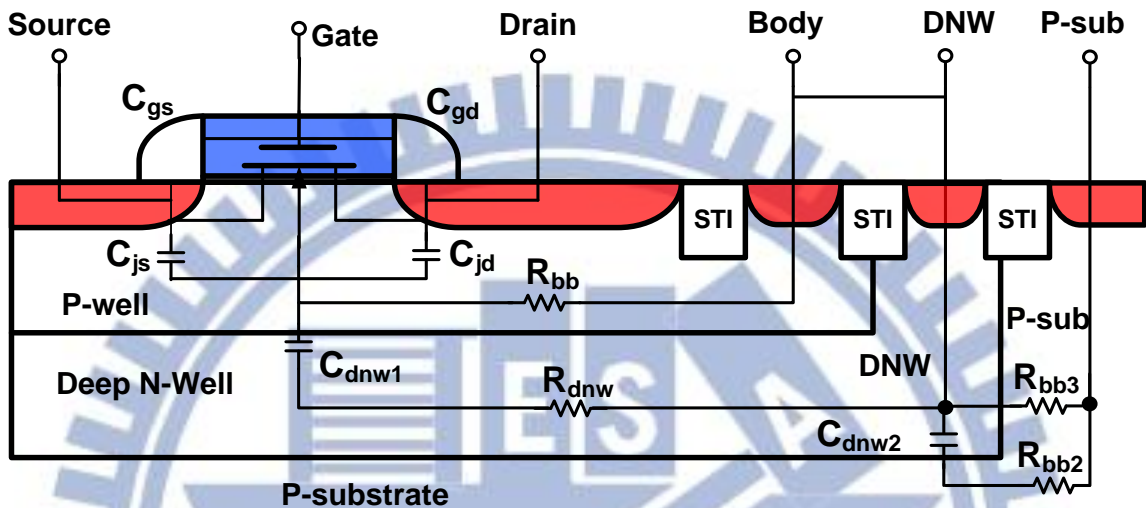
Fig. 3.19 The cross section of 4T MOSFET with deep n-well tied together with p-well body and connected with port-4.
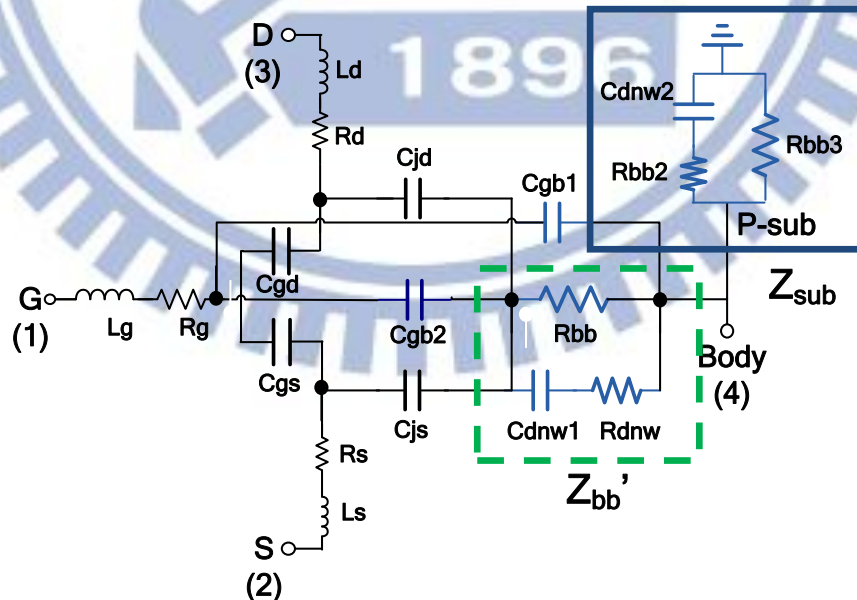
Fig. 3.20 A new body network model proposed for UN65 4-port MOSFET (L65003) in which the deep n-well (DNW) and p-well body (B) are tied together to port-4, and P-sub is connected to ground
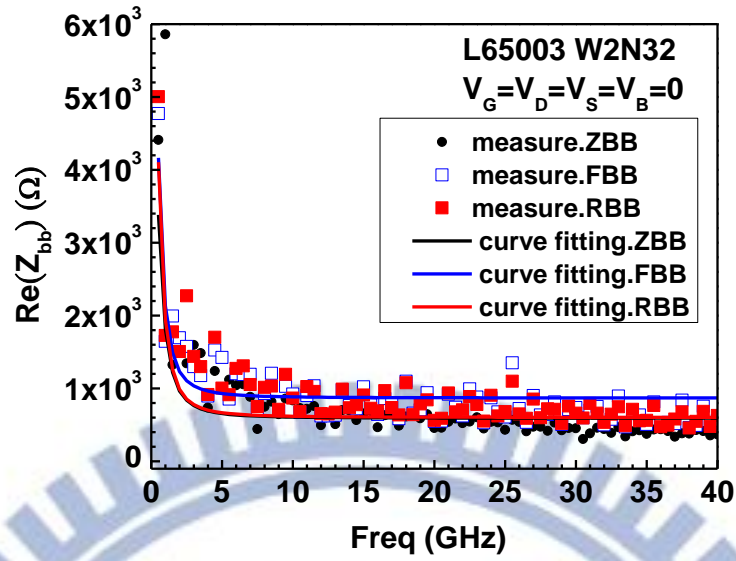
Fig. 3.21 Re(Z_{44})=Re(Z_{sub}) measured from port-4 (body) with all the other 3 ports (1 : G, 2 : D, 3 : S) at open state and under various body biases : ZBB (V_{bs}=0), FBB (V_{bs}=0.6V), and RBB(V_{bs}=-0.6V).

(a)

(b)

(c)
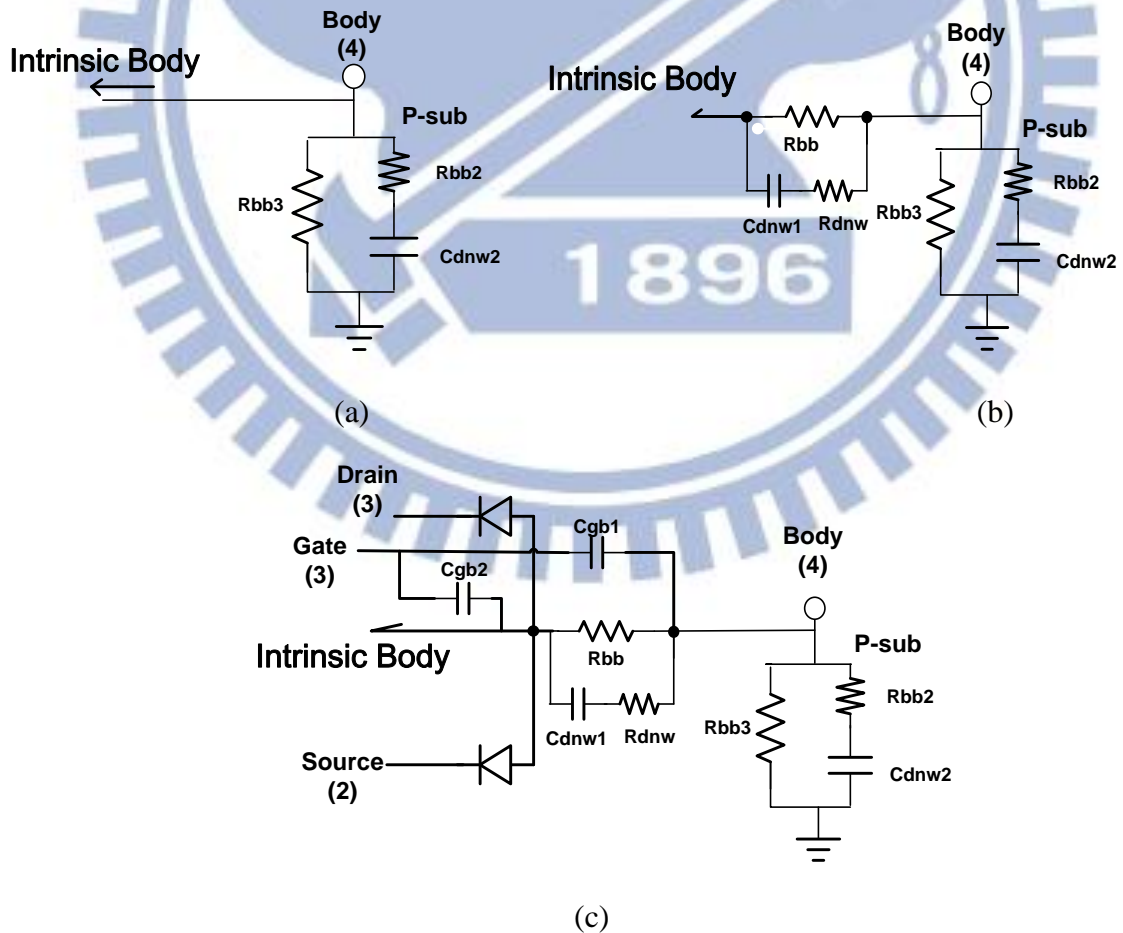
Fig. 3.22 Step by step synthesis of body network model (a) substrate network for deep

n-well/p-substrate (b) p-well body network for p-well/deep n-well and substrate for deep n-well/p-substrate (c) a complete body network model for L65003 4T RFMOSFET

Cjd, Cjs
$$C_{js[0]} : -\frac{Im(Y_{42(LF)})}{\omega} , C_{jd[0]} : -\frac{Im(Y_{43(LF)})}{\omega}$$

Rbb
$$R_{bb[0]} = \frac{Re(Y_{42(LF)})}{-\omega^2 C_{js[0]}(C_{jd[0]} + C_{js[0]})} = \frac{Re(Y_{43(LF)})}{-\omega^2 C_{jd[0]}(C_{jd[0]} + C_{js[0]})}$$

Cdnw
$$C_{dnw1} = \frac{Im(Y_{44}) + Im(Y_{43}) + Im(Y_{42}) + Im(Y_{41})}{\omega} , C_{dnw2} = \frac{Im\left(\frac{1}{Z_{44(LF)}}\right)}{\omega}$$

Rbb2,Rbb3
$$Re(Z_{44}) = R_{bb3} \cdot \frac{1 + \omega^2 C_{dnw2}^2 R_{bb2}(R_{bb2} + R_{bb3}) - j\omega C_{dnw2}R_{bb3}}{1 + \omega^2 C_{dnw2}^2 (R_{bb2} + R_{bb3})^2}$$

Rdnw
$$Re[Y_{44}] = \frac{1}{Re[Z_{bb}]} + \frac{1}{Re[Z_{sub}]} = \left(\frac{1}{R_{bb}} + \frac{1}{R_{dnw}}\right) + \left(\frac{1}{R_{bb2}} + \frac{1}{R_{bb3}}\right)$$
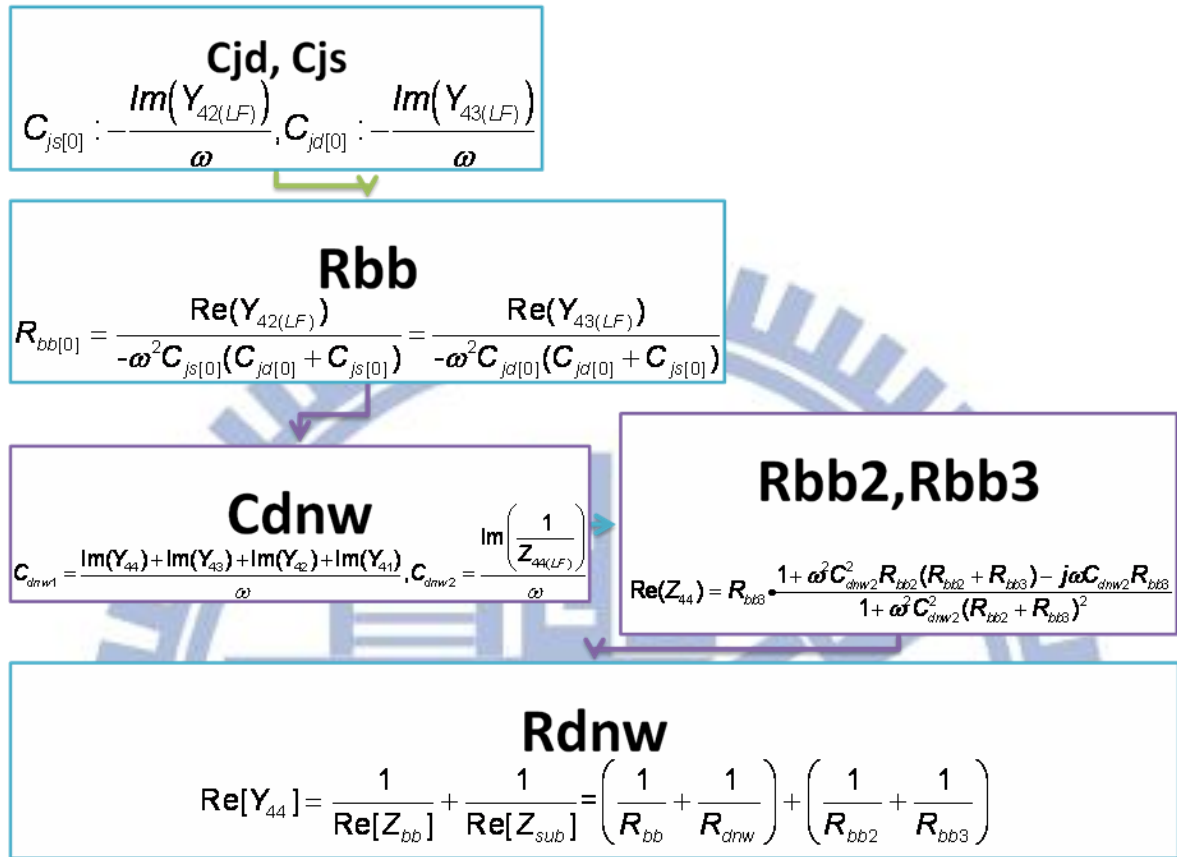
Fig. 3.23 A new body network model parameters extraction flow for 4-port RF MOSFET with equivalent circuit shown in Fig. 3.20

Table 3.3 Resistance parameters extracted for the new body network model
(a) initial and optimized R_{bb2} and R_{bb3}

Zsub	default	optimization
Rbb2	384	664
Rbb3	6741.12	5484

(b) R_{bb}, R_{dnw} R_{bb2} and R_{bb3} after optimization

Optimized parameters	ZBB (Vbs=0V)	FBB (Vbs=0.6V)	RBB(Vbs=-0.6V)
Rbb (Ω)	958	977	842
Rdnw (Ω)	476	202	233
Rbb2 (Ω)	664	874	813
Rbb3 (Ω)	5484	7994	8192
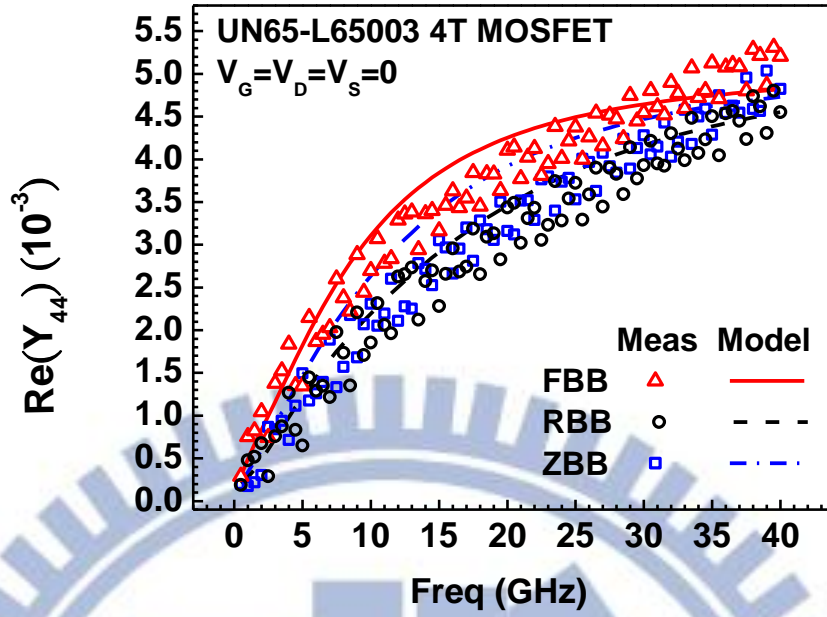
Fig. 3.24 Comparison of measured and simulated $Re(Y_{44})$ using the new body network model and extracted parameters under ZBB ($V_{bs}=0$), FBB ($V_{bs}=0.6V$), and RBB($V_{bs}=-0.6V$).

The final step to complete the extraction flow is the extraction of gate to body capacitances, namely C_{gb1} and C_{gb2} as shown in **Fig. 3.20.** Then the step by step synthesis of the body network model is moved from **Fig. 3.22**(b) to **Fig. 3.22(c)**. In general, gate to body capacitance can be extracted from $-Im(Y_{14})/\omega$ as shown in **Fig. 3.25**. However, the strong frequency dependence revealed in **Fig. 3.25** with a fast fall off in lower frequency region and then saturation to a constant at frequency beyond 25GHz suggests that the gate to body capacitance is composed frequency independent and frequency dependent components, denoted as C_{gb1} and C_{gb2}, respectively. The origin responsible for C_{gb1} and C_{gb2} can be explained by RF MOSFET layout shown in **Fig. 3.26**. The frequency independent component (C_{gb1}) is contributed from gate contact/metal to body contact/metal coupling capacitance. The frequency dependent component (C_{gb2}) comes from gate to channel (body) coupling, which may reveal non-quasi-static effect. According to the measured $-Im(Y_{14})/\omega$ shown in **Fig. 3.25** and the analysis supported by **Fig. 3.26** , C_{gb1} and C_{gb2} can be extracted as follows, given by (3.34) and(3.35).

$$C_{gb1} = \frac{-\mathrm{Im}(Y_{14(HF)})|_{f>25GHz}}{\omega} \qquad (3.34)$$

$$C_{gb2} = \frac{-\mathrm{Im}(Y_{14(LF)})|_{f\ll1GHz}}{\omega} - C_{gb1} \qquad (3.35)$$
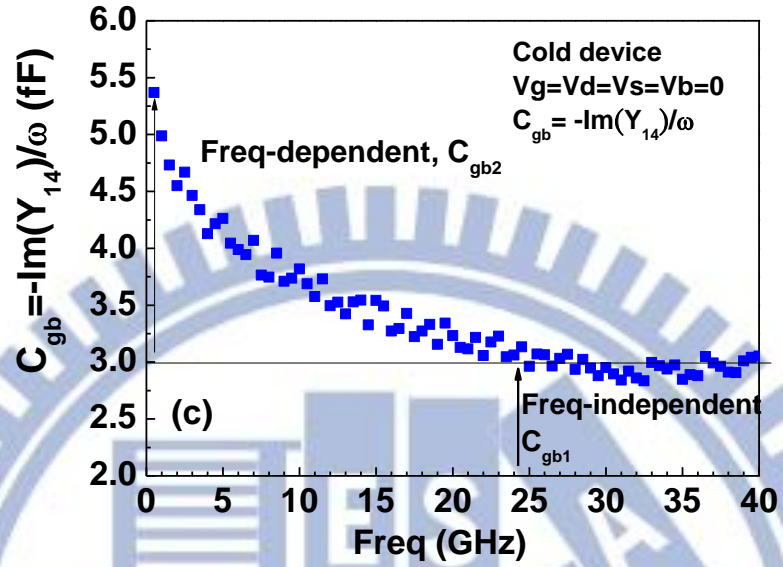
Fig. 3.25 The gate to body capacitances measured from 4-port Y-parameters after openM3 deembedding on 4-port RF MOSFET $-\mathrm{Im}(Y_{14})/\omega = C_{gb} = C_{gb1} + C_{gb2}$
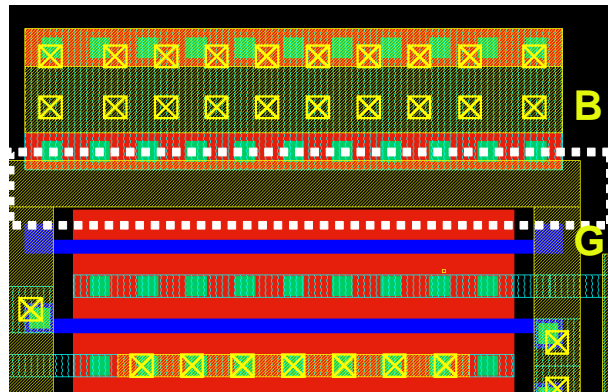
Fig. 3.26 RF MOSFET layout remarked with poly gate fingers, gate contact and metal to contacts, body contacts and metal to contacts. The metals to gate contacts and body contacts will contribute inter-metal coupling capacitance.

3.3 Four-port RF MOSFET Small Signal Equivalent Circuit Development and Analysis

In the following, the small signal equivalent circuits for 4-port RF MOSFET will be drived for different operation regions, such as **off-state**, **linear** region, and **saturation** region. Note that the new body network developed in sec. 3.2 for 4T MOSFET becomes the key component to be adopted to complete the small signal equivalent circuits as required. The accuracy of the simulation by using the small signal equivalent circuits and new body network model specifically for 4-port RF MOSFET will be verified by an extensive comparison with the measured data. Also, the simulation performed by BSIM-4 adopting new body network will be presented for a benchmark with the results from small signal equivalent circuit developed in this work.

3.3.1 Small Signal Equivalent Circuit at Off State

First, the small signal equivalent circuit at **off state** is developed for 4-port RF MOSFET under cold device condition with $V_g=V_d=V_s=V_b=0$. **Fig. 3.27** illustrates the device cross section for 4T MOSFET denoted with the RC elements located at proper regions, e.g. C_{gs}/C_{gd} for the gate capacitances between gate and source/drain, C_{js}/C_{jd} for the junction capacitances between source/drain and p-well body, and C_{dnw1}/C_{dnw2} for the junction capacitances between deep n-well and p-well(body)/p-substrate. Based on the proposed RC elements configuration, the equivalent circuit can be established as shown in **Fig. 3.28**. Note that series RL was deployed at each terminal, i.e. gate, drain, source, and body to account for the parasitic resistance and inductance remained even after short deembedding (M3 instead of M1 for this study). At off state, the channel is turned off due to depletion of free carriers, then C_{gs} and C_{gd} are composed of gate to source/drain overlap capacitance and fringing capacitance. The physical definition and modeling for C_{gs} and C_{gd} will be addressed in sec. 3.4. Regarding C_{gb1} and C_{gb2} introduced in our new body network model, the frequency and layout dependence and the extraction method can be referred to **sec. 3.2.2**. R_{gb} in parallel with C_{gb2} represents a

DC leakage path, which cannot be neglected for UN65 MOSFET with ultra-thin gate oxide to 1.6 nm. The RC parameters of the body network model have been determined in sec. 3.2.2 and the model parameters remained for the 4T MOSFET can be extracted from 4-port Y-parameters at very low frequency given by (3.36)~(3.39). **Fig. 3.29** presents C_{gg}, C_{gd}, and C_{gd} extracted from (3.36)~(3.38). Note that all of the capacitances should be physical elements independent of frequency but the capacitances extracted from $Im(Y_{ij})$ even after an open deembedding reveal significant increase at higher frequency. This frequency dependence suggests the effect from parasitic inductances, which cannot be eliminated using short M3 deembedding used in this work. To overcome this problem, extraction at very low frequency to make the parasitic inductance negligible becomes a compromized solution.

$$C_{gg} = \frac{Im(Y_{11,int})}{\omega}\bigg|_{\omega \ll 1} \tag{3.36}$$

$$C_{gs} = \frac{-Im(Y_{12,int})}{\omega}\bigg|_{\omega \ll 1} \tag{3.37}$$

$$C_{gd} = \frac{-Im(Y_{13,int})}{\omega}\bigg|_{\omega \ll 1} \tag{3.38}$$

$$C_{gb} = \frac{-Im(Y_{14,int})}{\omega}\bigg|_{\omega \ll 1} \tag{3.39}$$

1 : gate (g), 2: source (s), 3: drain (d), 4: body (b)

where, $Y_{ij,int}$ represent the intrinsic Y-parameters achieved after an open deembedding, i.e.

$$Y_{ij,int} = Y_{ij,mea} - Y_{ij,open} \tag{3.40}$$

For 4-port MOSFET, there exist 16 components of transcapacitance in the form of a 4×4 matrix given by (3.41) ,

$$[C_{ij}] = \begin{bmatrix} C_{gg} & C_{gs} & C_{gd} & C_{gb} \\ C_{sg} & C_{ss} & C_{sd} & C_{sb} \\ C_{dg} & C_{ds} & C_{dd} & C_{db} \\ C_{bg} & C_{bs} & C_{bd} & C_{bb} \end{bmatrix}$$ (3.41)

For 4-port devices at off state, the conductance associated with each port becomes zero and the capacitances incorporated in the 4×4 matrix must follow the charge conservation law for the sum of all capacitance at each port, represented by each row or each column in the 4×4 matrix, e.g.

$$\text{Im}(Y_{11,int}) + \text{Im}(Y_{12,int}) + \text{Im}(Y_{13,int}) + \text{Im}(Y_{14,int}) = 0$$

$$\rightarrow \frac{\text{Im}(Y_{11,int}) + \text{Im}(Y_{12,int}) + \text{Im}(Y_{13,int}) + \text{Im}(Y_{14,int})}{\omega} = 0$$ (3.42)

From (3.42), the capacitances associated with port-1, i.e. gate have to follow the conservation law as follows

$$C_{gg} - C_{gs} - C_{gd} - C_{gb} = 0 \rightarrow C_{gg} = C_{gs} + C_{gd} + C_{gb}$$ (3.43)

Note that is valid under ideal condition that all of the parasitic capacitances can be removed to be clean by using open deembedding. The desired perfect deembedding can be approached by open deembedding to the bottom metal, i.e. M1. However, it cannot be achieved in this study due to the test structure limited to open M3 deembedding. Due to the limitation, an additional capacitance, namely C_g is added to (3.44) and given by (3.44)~(3.45).

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} + C_g$$ (3.44)

$$\because C_{gb} = C_{gb1} + C_{gb2}$$

$$\therefore C_{gg} = C_{gs} + C_{gd} + C_{gb1} + C_{gb2} + C_g$$ (3.45)

One more extrinsic parasitic capacitance, namely C_{ds}, which is located between drain and source is deployed in the small signal equivalent circuit to get best fitting to the measured $\text{Im}(Y_{32})$, phase(S_{32}), and phase(S_{23}). C_{ds} can be extracted from $\text{Im}(Y_{32})$ given by (3.46). This C_{ds}

existing at off state is contributed from inter-metal coupling capacitance instead of coupling through the channel between source and drain. Ideally, this C_{ds} can be eliminated through an improved open deembedding, e.g. open M1 deembedding. Unfortunately, this work is limited to open M3 deembedding and an additional C_{ds} cannot be avoided from the equivalent circuit.

$$C_{ds} = \frac{-\text{Im}(Y_{32,int})}{\omega}\bigg|_{\omega \ll 1} \tag{3.46}$$

Fig. 3.30 makes a comparison of C_{ds}=-Im(Y_{32})/ω from measurement and simulation using BSIM-4 and our small signal equivalent circuit. Note that the small signal equivalent circuit without extrinsic C_{ds} leads to under-estimation of C_{ds}=-Im(Y_{32})/ω and the adoption of an appropriate C_{ds} can result in a good match with the measurement.

Table 3.4 summarizes the small signal equivalent circuit model parameters determined for the 4-port RF MOSFET at off state. **Fig. 3.31~ Fig. 3.38** present the 4-port S-parameters from measurement and simulation for this 4-port MOSFET (W2N32) at off state. Note that the simulation by using the small signal equivalent circuit shown in **Fig. 3.28** and model parameters in **Table 3.4** was compared with those calculated by BSIM-4 default model. The results indicate that the small signal equivalent circuit can predict 4-port S-parameters with promisingly good accuracy whereas the simulation uding BSIM-4 default model reveals significant deviation from the measurement, particularly for the components related to the body, i.e. port-4, e.g. Mag(S_{44}), Mag(S_{41}), Mag(S_{42}), and Mag(S_{43}) as shown in **Fig. 3.31** and phase(S_{44}), phase(S_{41}), phase(S_{42}), and phase(S_{43}) as shown in **Fig. 3.35**. Besides S-parameters, Re(Y_{42}), Re(Y_{43}), and Re(Y_{33}) are three more important parameters to verify the body network model. **Fig. 3.39** indicates that small signal equivalent circuit with new body network can accurately predict Re(Y_{42}) and Re(Y_{43}) but that with default body network model reveal large deviation. **Fig. 3.40** presents similar effect from body network model when applied to BSIM-4 for Re(Y_{42}) and Re(Y_{43}) simulation. Interestingly, the impact from body network model on Re(Y_{33}), i.e. the key parameter responsible for output resistance, is relatively

smaller, as shown in **Fig. 3.41.** Again, the new body network model can be applied to both small signal equivalent circuit and BSIM-4 for an accurate simulation. The extensive verification suggests that body network model is the key to determine simulation accuracy for 4-port RF MOSFETs and proves that the new body network proposed in this thesis (**Fig. 3.28**) is the solution to fix the problem with BSIM-4 for 4-port MOSFET simulation.
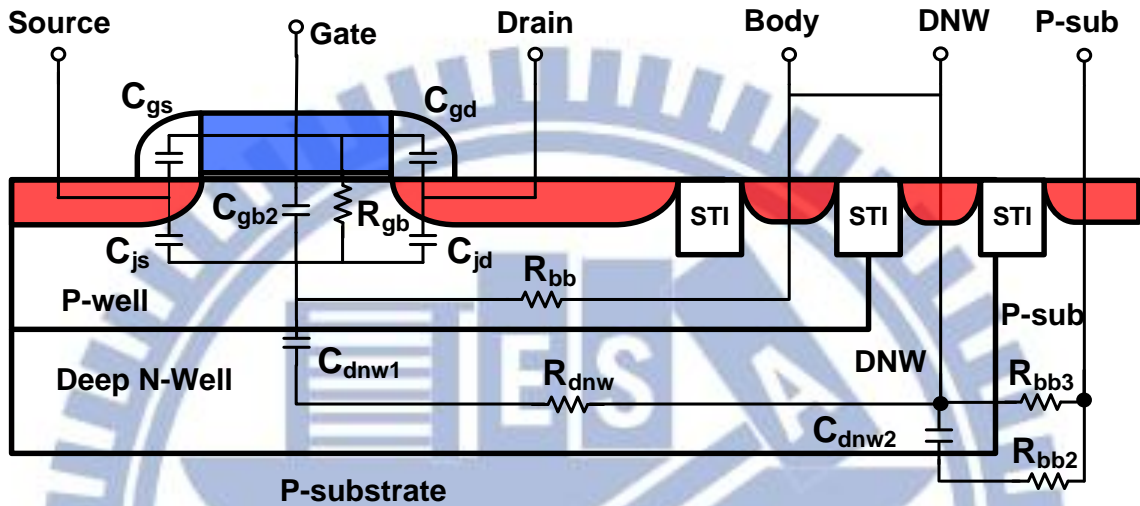
Fig. 3.27 4-port MOSFET device cross section and the representation of RC elements for the equivalent circuit at off state $V_{gs}=V_{ds}=V_{bs}=0$
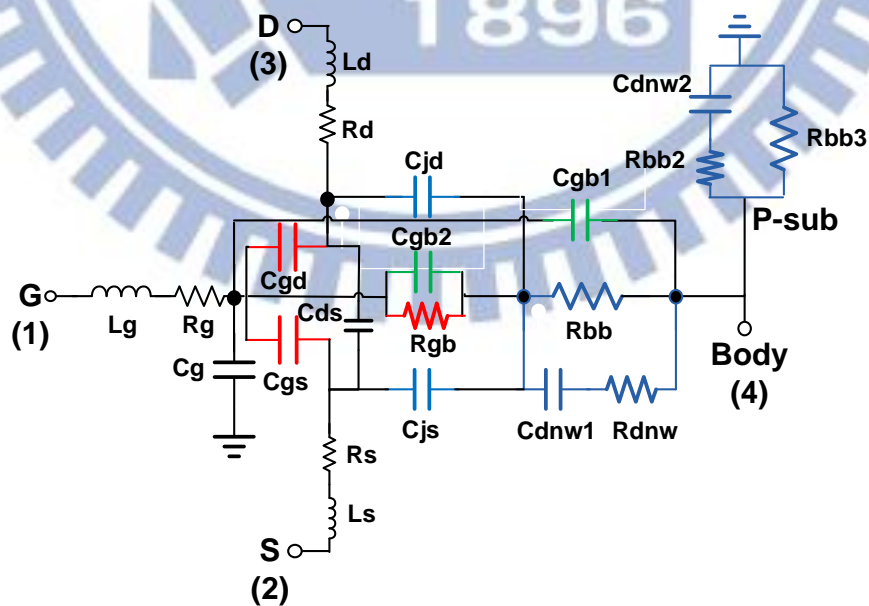
Fig. 3.28 Small signal equivalent circuit with new body network model for 4-port RF MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$
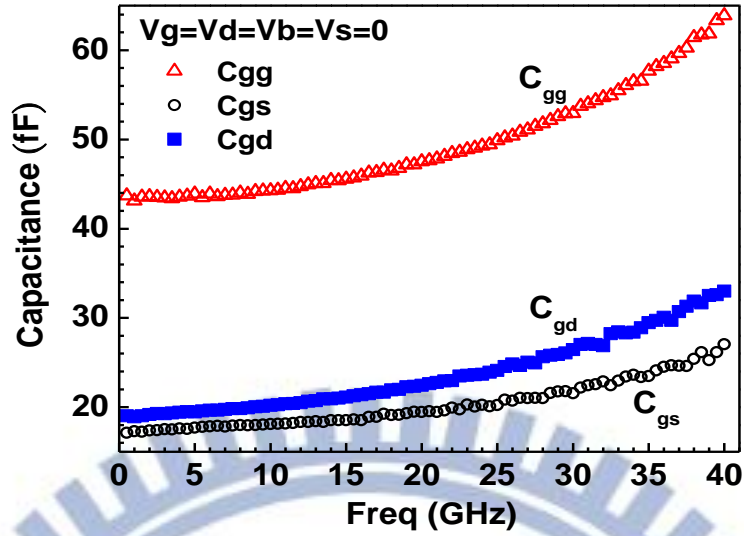
Fig. 3.29 C_{gg}, C_{gs}, and C_{gd} vs. frequency measured from 4-port RF MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$
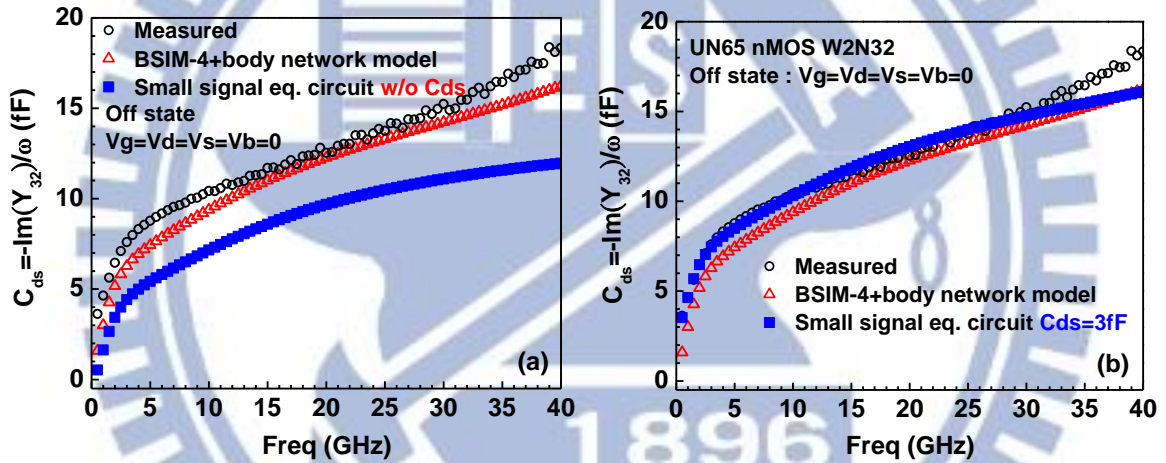
Fig. 3.30 Measured and simulated $C_{ds}=-Im(Y_{32})/\omega$ for 4-port RF MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$. Simulation using BSIM-4 and small signal equivalent circuit (a) without extrinsic C_{ds} (b) with extrinsic $C_{ds}=3fF$

Table 3.4 Small signal equivalent circuit model parameters of 4-port MOSFET at off state

4-port MOSFET model parameters at off state					
Capacitances	(fF)	Resistances	Ω	Inductances	pH
Cgs	17.12	Rg	7.2	Ls	70
Cgd	18.91	Rd	1	Ld	70
Cgb1	2	Rs	1	Lg	70
Cgb2	2.5	Rb	1	Lb	70
Cg	2.1	Rbb	958		
Cds	3	Rbb2	664		
Cjs	18.91	Rbb3	5484		
Cjd	17.12	Rdnw	476		
Cdnw1	18.91	Rgb	518500		
Cdnw2	18.91				

Fig. 3.31 The measured and simulated Mag(S) of Dual gate at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Solid lines : small signal equivalent circuit with body network model.
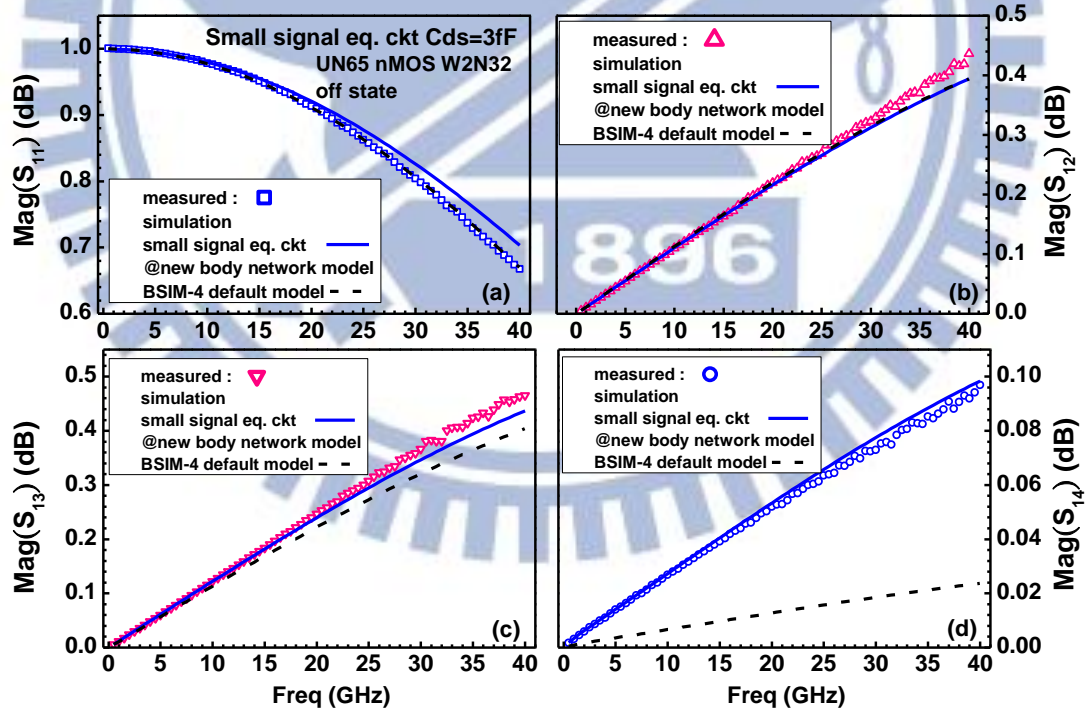
Fig. 3.32 The measured and simulated Mag(S) of Dual gate at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
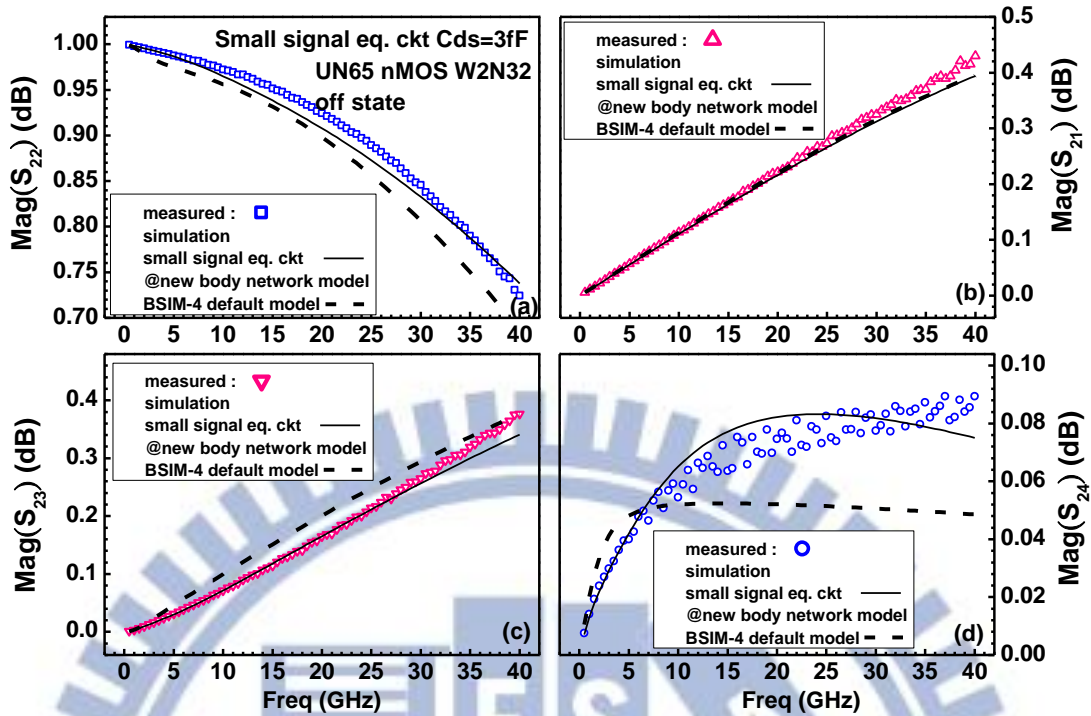
Fig. 3.33 The measured and simulated Mag(S) of 4-port MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) Mag(S_{22}) (b) Mag(S_{21}) (c) Mag(S_{23}) (d) Mag(S_{24}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
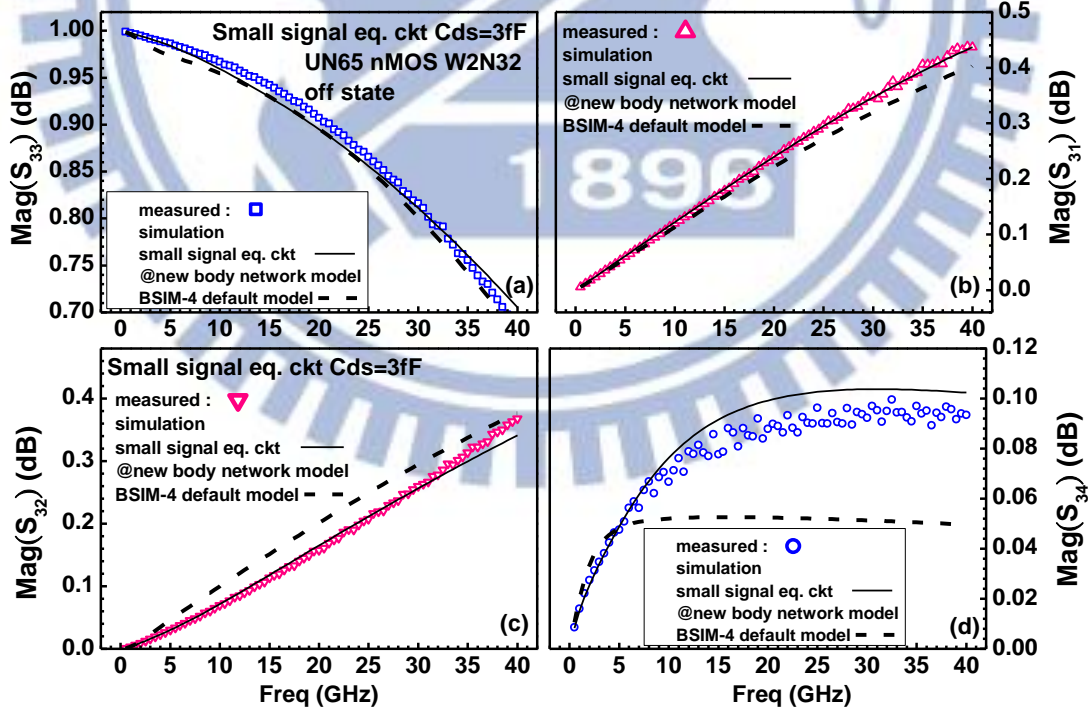
Fig. 3.34 The measured and simulated Mag(S) of 4-port MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) Mag(S_{33}) (b) Mag(S_{31}) (c) Mag(S_{32}) (d) Mag(S_{34}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
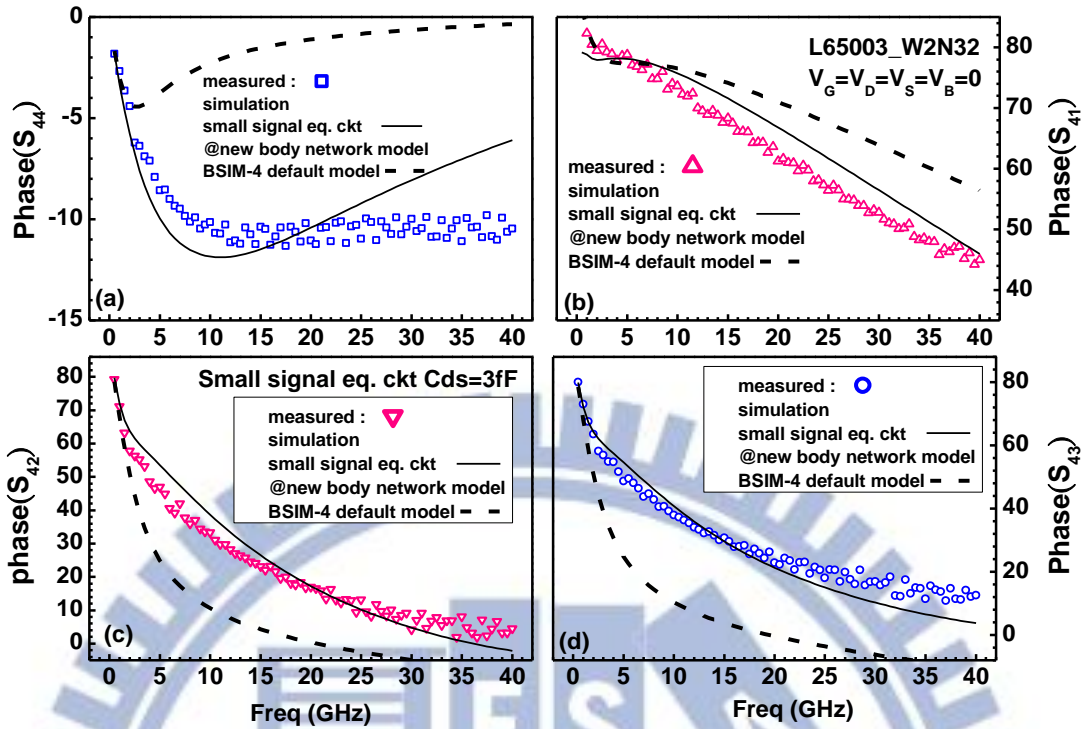
Fig. 3.35 The measured and simulated phase(S) of 4-port MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
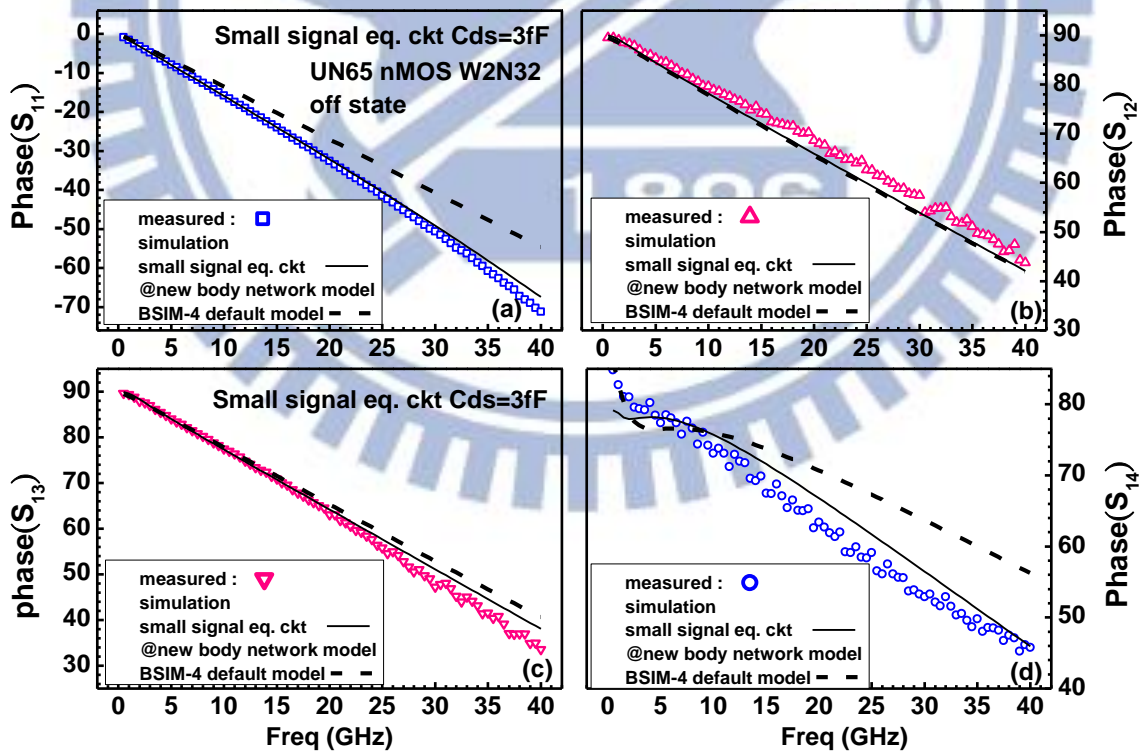
Fig. 3.36 The measured and simulated phase(S) of 4-port MOSFET at off state Vgs=Vds= Vbs=0 (a) phase(S11) (b) phase(S12) (c) phase(S13) (d) phase(S14). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
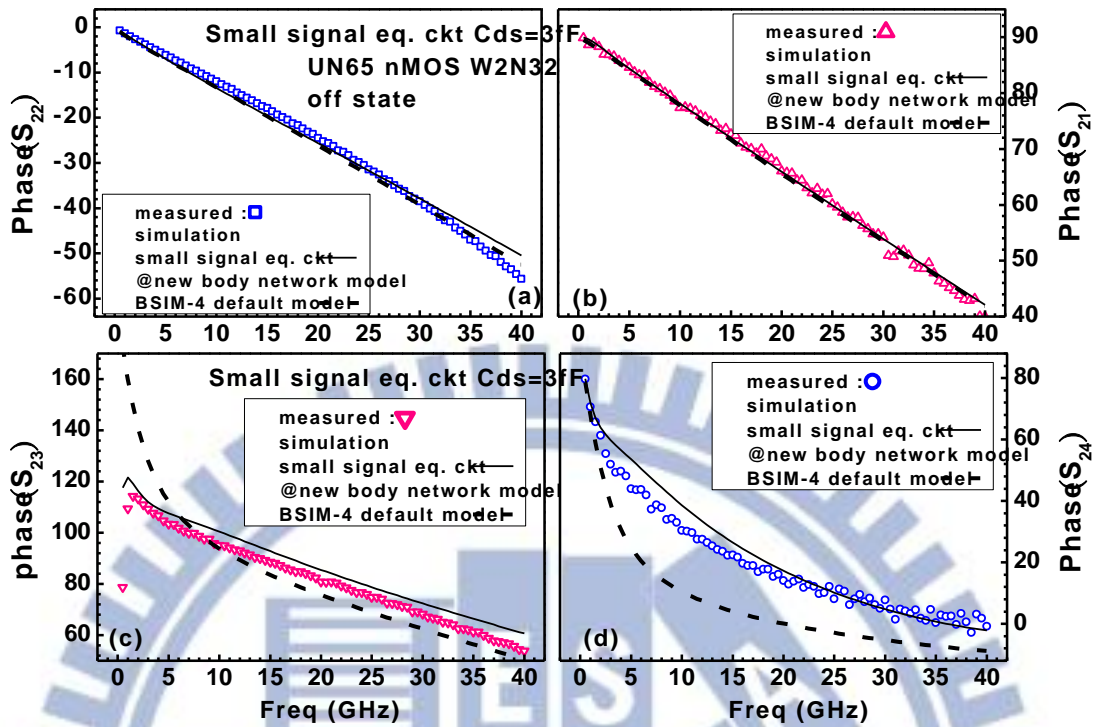
Fig. 3.37 The measured and simulated phase(S) of 4-port MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) phase(S_{22}) (b) phase(S_{21}) (c) phase(S_{23}) (d) phase(S_{24}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
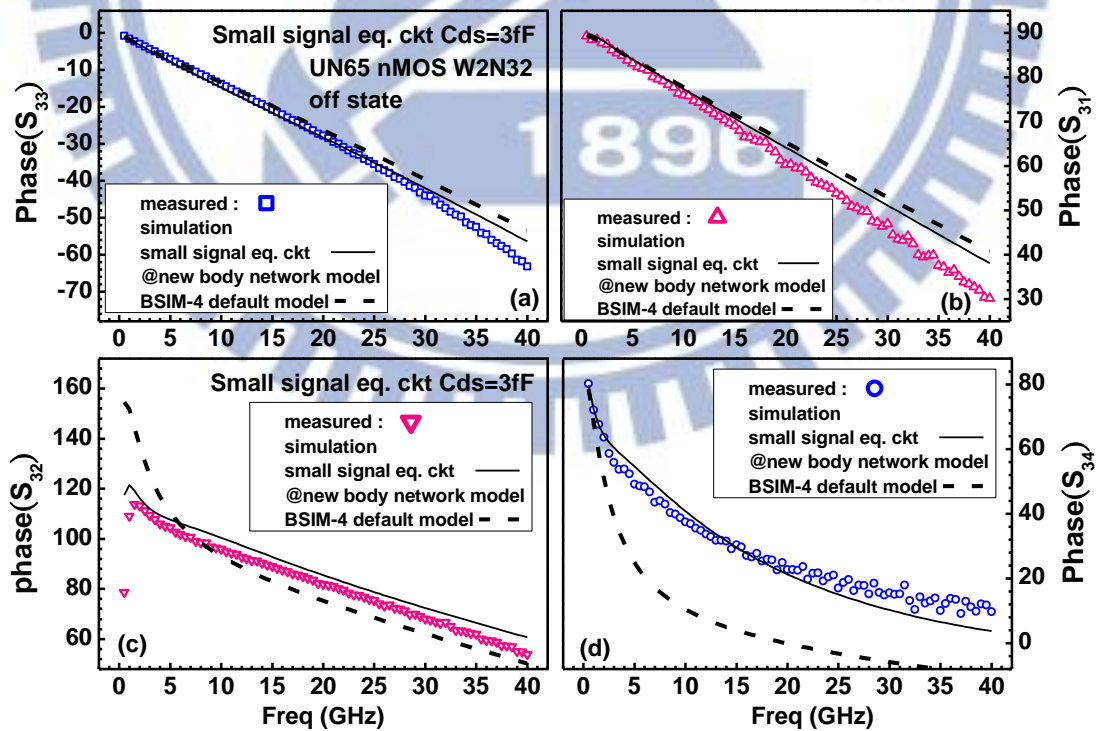
Fig. 3.38 The measured and simulated phase(S) of 4-port MOSFET at off state $V_{gs}=V_{ds}=V_{bs}=0$ (a) phase(S_{33}) (b) phase(S_{31}) (c) phaseS_{32}) (d) phase(S_{34}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
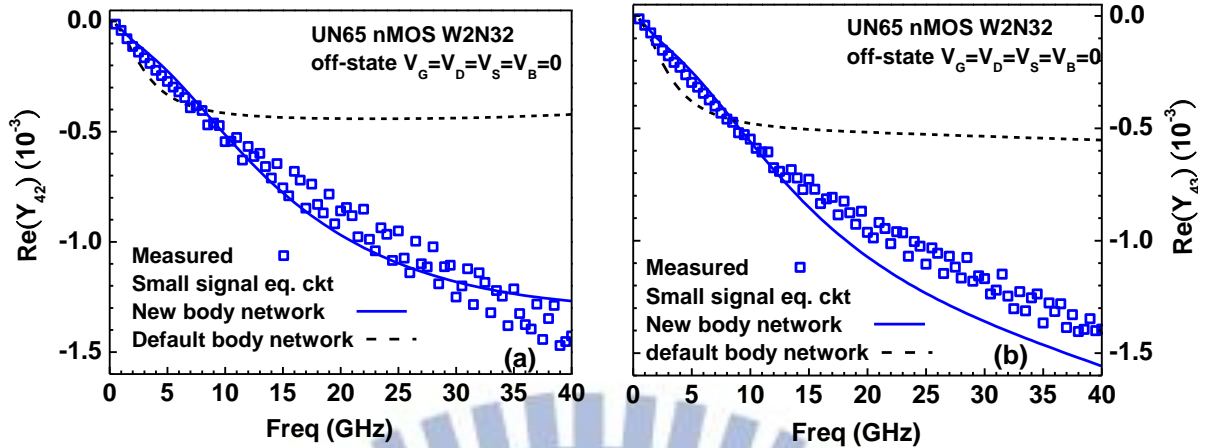
Fig. 3.39 Measured and simulated $Re(Y_{42})$ and $Re(Y_{43})$ for 4-port MOSFET at off state $V_{gs}=V_{ds}= V_{bs}=0$ (a) $Re(Y_{42})$ (b) $Re(Y_{43})$. Simulation by small signal equivalent circuit model. Solid lines : with new body network model. Dash lines : with default body network model
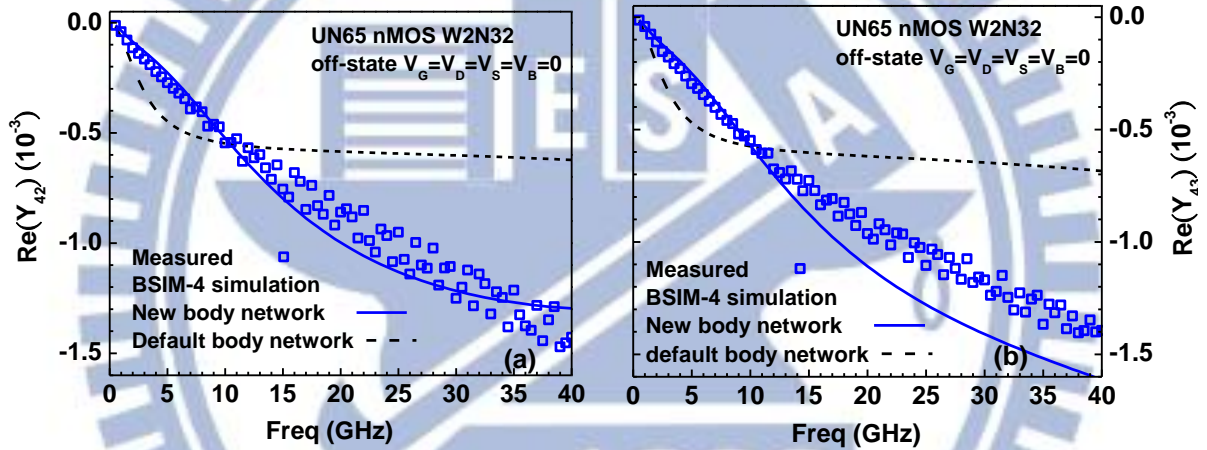
Fig. 3.40 Measured and simulated $Re(Y_{42})$ and $Re(Y_{43})$ for 4-port MOSFET at off state $V_{gs}=V_{ds}= V_{bs}=0$ (a) $Re(Y_{42})$ (b) $Re(Y_{43})$. Simulation by BSIM-4, solid lines : with new body network model, dash lines : with default body network model
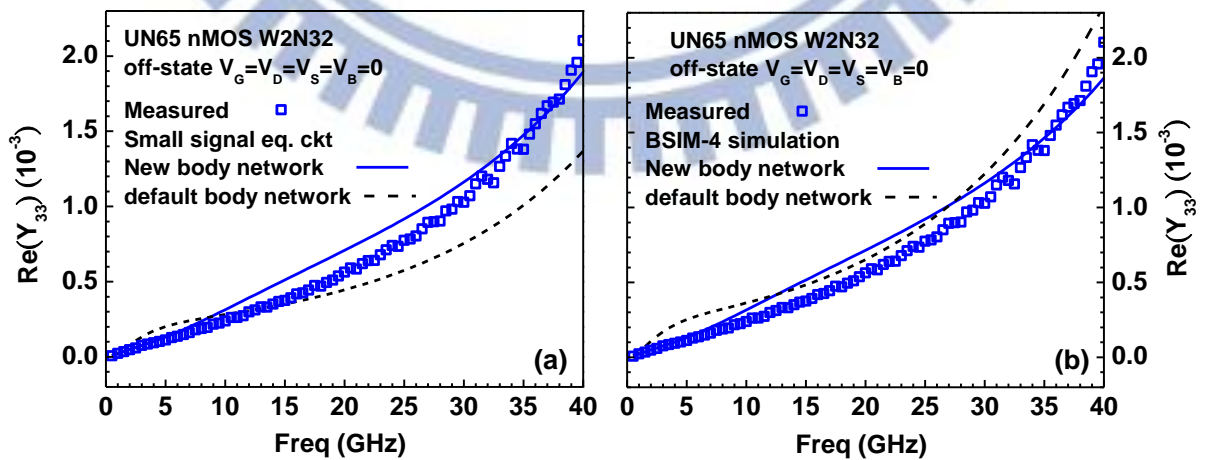
Fig. 3.41 Measured and simulated $Re(Y_{33})$ for 4-port MOSFET at off state $V_{gs}=V_{ds}= V_{bs}=0$ (a) simulation by small signal equivalent circuit (b) simulation by BSIM-4. Solid lines : with new body network model. Dash lines : with default body network model

3.3.2 Small Signal Equivalent Circuit in Linear Region

In this section, small signal equivalent circuit will be derived for 4-port RF MOSFET in linear region. Note that the bias condition for linear region has to follow the criterion of $|V_{gs}| > |V_T|$ and $|V_{ds}| << |V_{gs} - V_T|$ to ensure strong inversion of the channel and linear velocity vs. field under sufficiently low V_{ds}. In this study for UN65 nMOS with V_{dd}=1.0V, the bias condition is specified as V_{gs}=V_{dd} =1.0V and V_{ds}=0 for linear region. Considering the channel conduction driven by inversion carriers, the channel resistance between source and drain is represented by R_{ch} in the device cross section and equivalent circuit as shown in **Fig. 3.42** and **Fig. 3.43**, respectively. Then R_{ch} appears as one additional model parameter compared with those required for off state shown in **Fig. 3.27**and **Fig. 3.28**. According to a simple equivalent circuit analysis on **Fig. 3.43**, R_{ch} can be extracted from $1/Re(Y_{32})$ at very low frequency when all of the capacitors become open circuit, given by (3.47)~(3.48).

At very low frequency,

$$\frac{1}{Re(Y_{32})|_{\omega \ll 1}} \cong R_{ch} + R_d + R_s + \frac{\omega^2 (L_s + L_d)^2}{(R_{ch} + R_d + R_s)^2} \tag{3.47}$$

$$\because \omega^2 (L_s + L_d)^2 \ll 1$$

$$\therefore \frac{1}{Re(Y_{32})|_{\omega \ll 1}} \cong R_{ch} + R_d + R_s \Rightarrow R_{ch} = \frac{1}{Re(Y_{32})|_{\omega \ll 1}} - (R_d + R_s) \tag{3.48}$$

The body network model previously derived for 4-port RF MOSFET at off state can be applied to linear region with an appropriate modification on C_{gb2}, due to formation of inversion channel. Besides necessary change to C_{gb2}, **Fig. 3.44** reveals significant increase of C_{gs} and C_{gd} caused by the raising V_{gs} to well above V_T (V_{gs} =1.0V >>V_T) as compared to those at off state (V_{gs}=0) shown in **Fig. 3.29**.

Table 3.5 summarizes the small signal equivalent circuit model parameters for 4-port RF MOSFET in linear region. It appears that the increase of V_{gs} to strong inversion region leads to increase of C_{gs} and C_{gd} whereas decrease of C_{gb2}, due to shielding effect from inversion carriers.

C_{gs} is larger than C_{gd} by around 5.7% and it can be explained by the difference of finger numbers for source and drain contact in the multi-finger MOSFET with even finger number (N_F=evern : $N_F/2$+1 for source contacts and $N_F/2$ for drain contacts). The channel resistance R_{ch} is determined by (3.48) to be around 7.3 Ω.
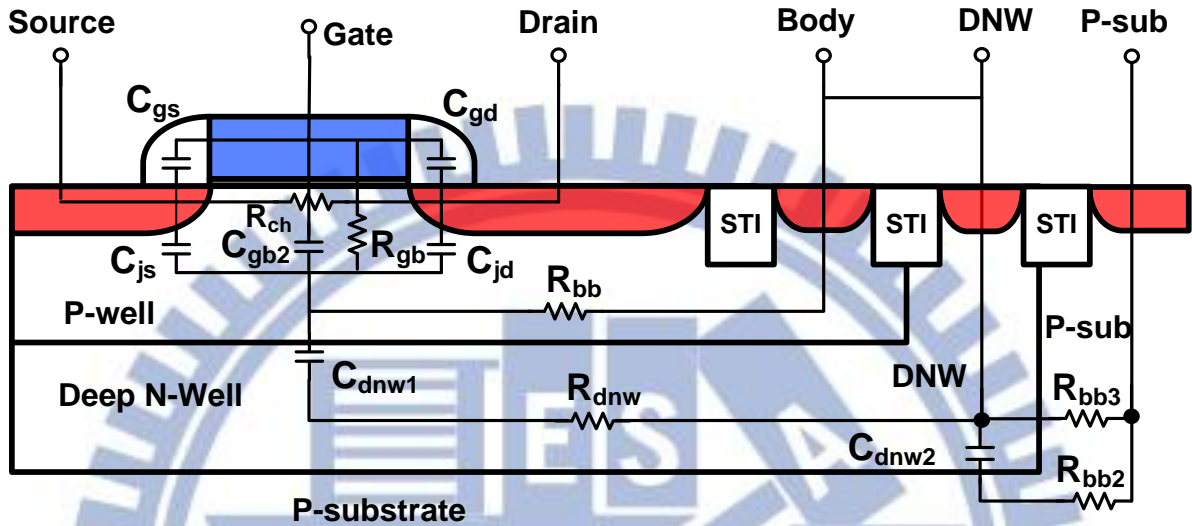
Fig. 3.42 4-port MOSFET device cross section and the representation of RC elements for the small signal equivalent circuit in linear region, V_{gs}=1.0V, V_{ds}=V_{bs} =0
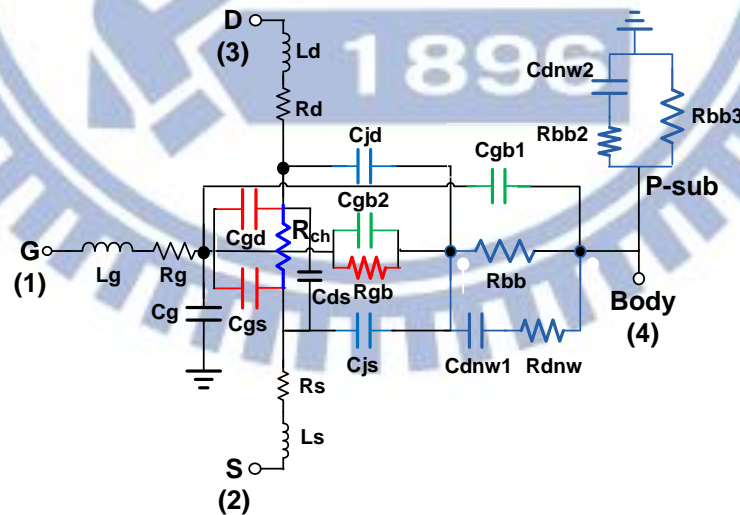
Fig. 3.43 Small signal equivalent circuit with new body network model for 4-port RF MOSFET in linear region, V_{gs}=1.0V, V_{ds}= V_{bs}=0. R_{ch} represents channel resistance of the inversion channel.
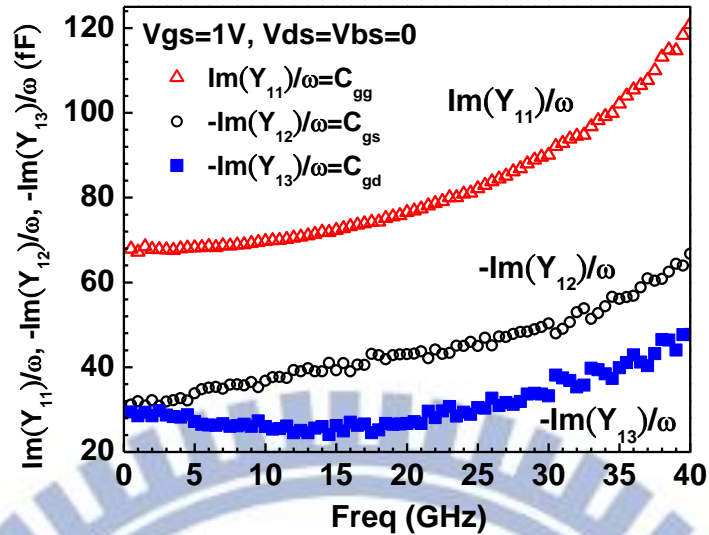
Fig. 3.44 $\mathrm{Im}(Y_{11})/\omega$, $-\mathrm{Im}(Y_{12})/\omega$, and $-\mathrm{Im}(Y_{13})/\omega$ vs. frequency measured from 4-port RF MOSFET under the biases in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0. C_{gg}, C_{gs}, and C_{gd} determined from $\mathrm{Im}(Y_{11})/\omega$, $-\mathrm{Im}(Y_{12})/\omega$, and $-\mathrm{Im}(Y_{13})/\omega$ at very low frequency

Table 3.5 Small signal equivalent circuit model parameters of 4-port MOSFET in linear region (V_{gs}=1.0V, V_{ds}= V_{bs}=0)

4-port MOSFET model parameters in linear region					
Capacitances	(fF)	Resistances	Ω	Inductances	pH
Cgs	31.18	Rg	7.2	Ls	70
Cgd	29.44	Rd	1	Ld	70
Cgb1	2	Rs	1	Lg	70
Cgb2	1.4	Rb	1	Lb	70
Cg	2.1	Rbb	958		
Cds	3	Rbb2	664		
Cjs	18.91	Rbb3	5484		
Cjd	17.12	Rdnw	476		
Cdnw1	18.91	Rgb	518500		
Cdnw2	18.91	Rch	7.3		

According to the model parameters shown in table 3.5 for 4-port MOSFETs in linear region, S- and Y-parameters are simulated. **Fig. 3.45 ~ Fig. 3.52** present the 4-port S-parameters from measurement and simulation for this 4-port MOSFET (W2N32) in linear region under V_{gs}=1.0V and V_{ds}=V_{bs}=0. Note that the simulation by using the small signal equivalent circuit shown in **Fig. 3.43** and model parameters in **Table 3.5** was compared with

those calculated by BSIM-4 default model. The results indicate that the small signal equivalent circuit can predict 4-port S-parameters with promisingly good accuracy whereas the simulation uding BSIM-4 default model reveals large deviation from the measurement, particularly for the components related to the body, i.e. port-4, e.g. Mag(S_{44}), Mag(S_{41}), Mag(S_{42}), and Mag(S_{43}) as shown in **Fig. 3.45** and phase(S_{44}), phase(S_{41}), phase(S_{42}), and phase(S_{43}) as shown in **Fig. 3.49**. Besides S-parameters, Re(Y_{42}), Re(Y_{43}), and Re(Y_{33}) are three more important parameters to verify the body network model. **Fig. 3.49** indicates that the small signal equivalent circuit with new body network can improve simulation accuracy for Re(Y_{42}) and Re(Y_{43}) compared with those simulated by using default body network model. **Fig. 3.54** presents similar effect from body network model when applied to BSIM-4 for Re(Y_{42}) and Re(Y_{43}) simulation. Similar with the condition for off state, the impact from body network model on Re(Y_{33}), i.e. the key parameter responsible for output resistance, is relatively smaller, as shown in **Fig. 3.55.** Again, the new body network model can be applied to both small signal equivalent circuit and BSIM-4 for an accurate simulation in linear region. The verification by extensive data suggests that body network model is the key to determine simulation accuracy for 4-port RF MOSFETs and proves that the new body network proposed for linear region (**Fig. 3.43**) can fix the problem with BSIM-4 for 4-port MOSFET simulation.
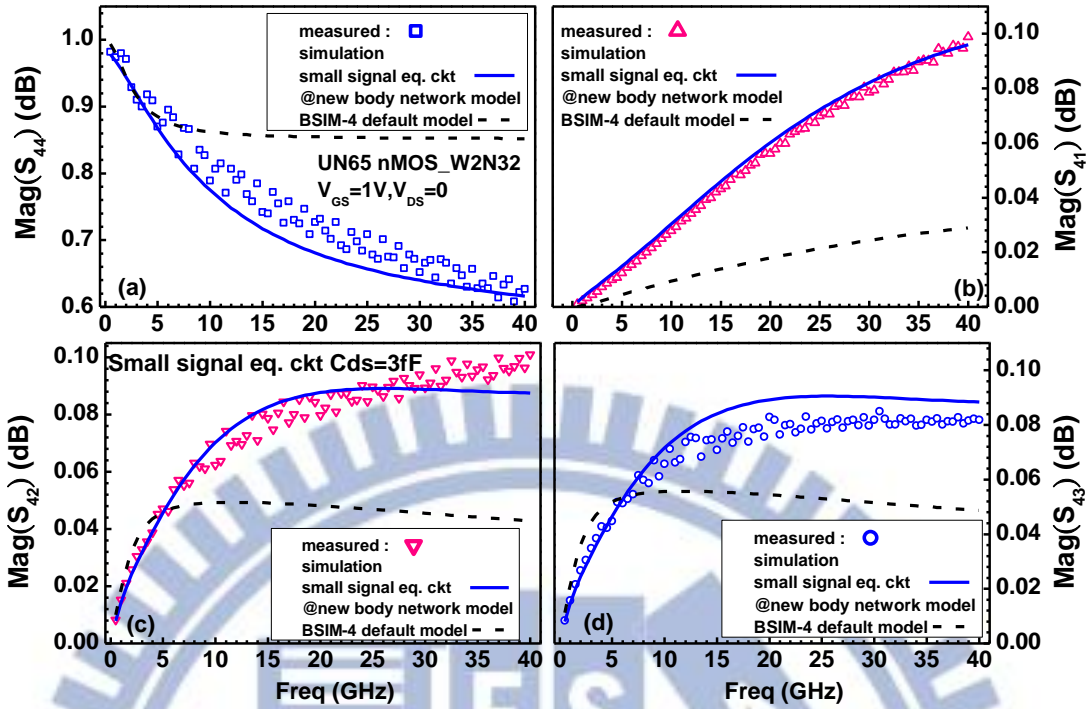
Fig. 3.45 The measured and simulated Mag(S) of 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
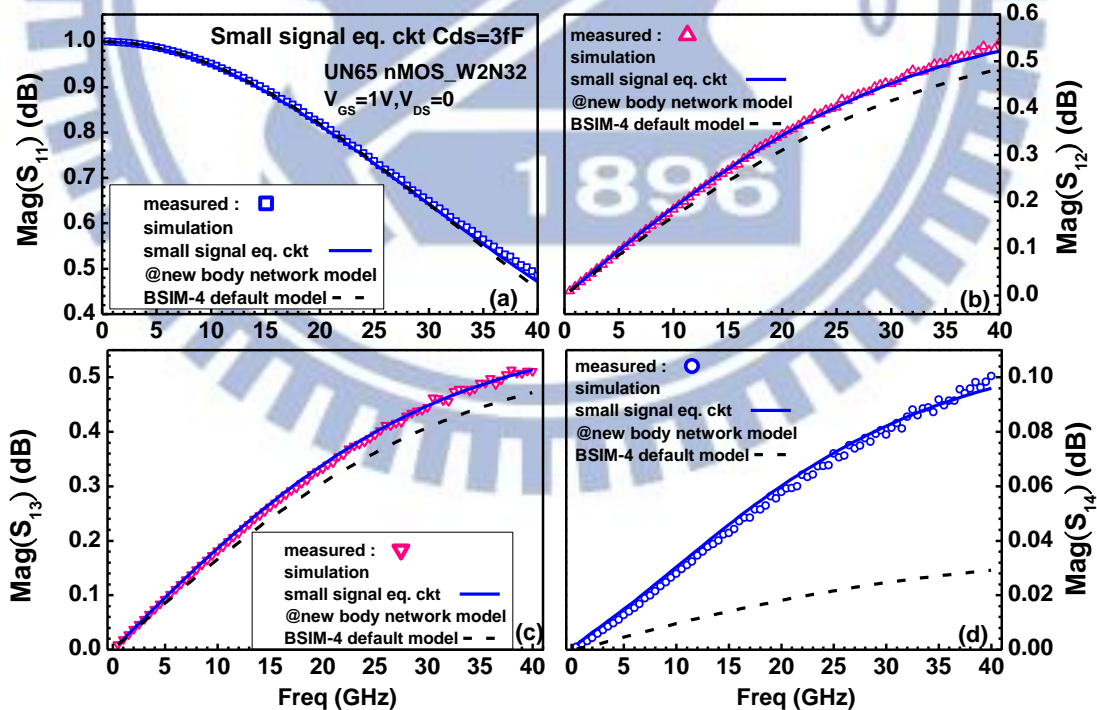
Fig. 3.46 The measured and simulated Mag(S) of 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
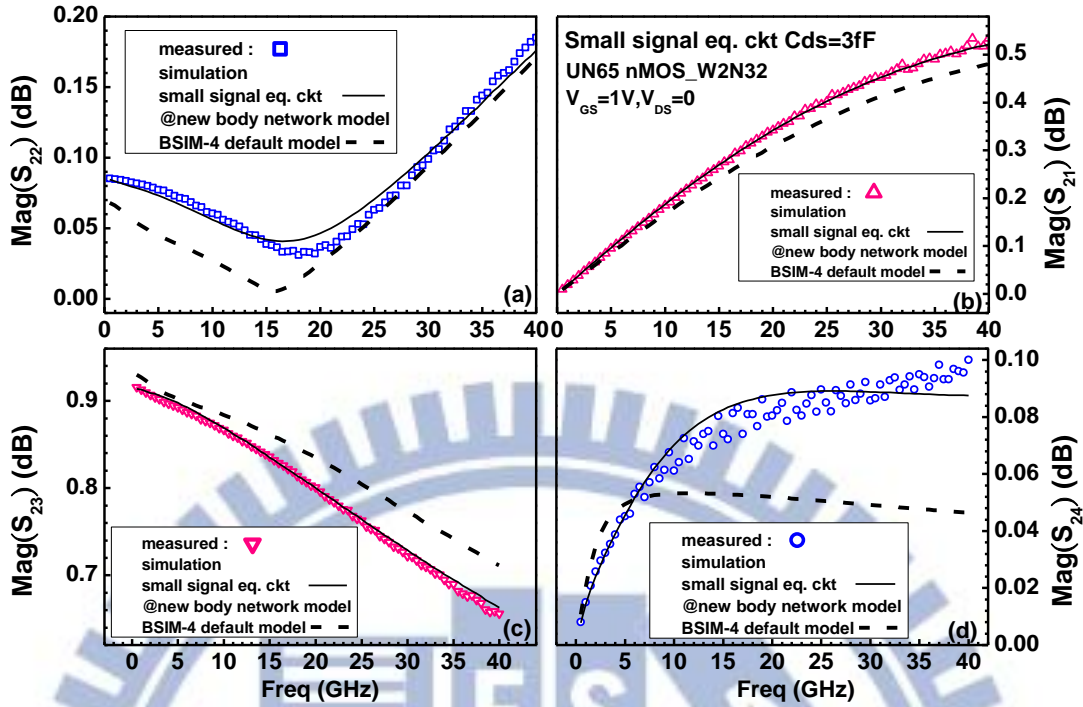
Fig. 3.47 The measured and simulated Mag(S) of 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) Mag(S_{22}) (b) Mag(S_{21}) (c) Mag(S_{23}) (d) Mag(S_{24}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
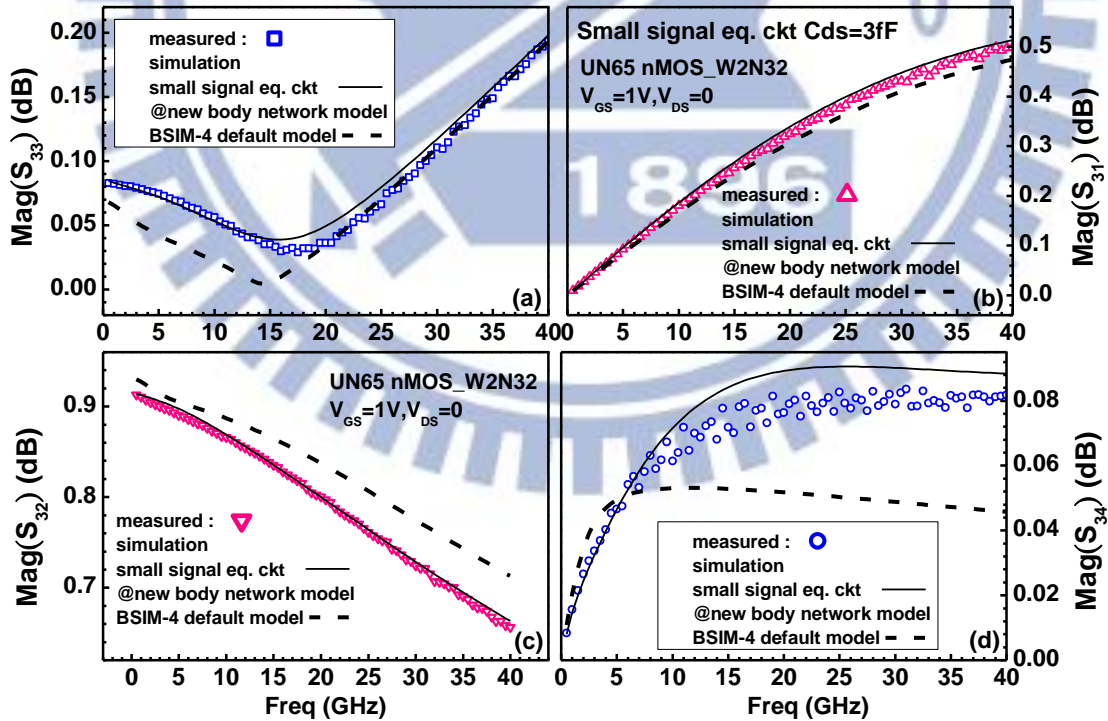
Fig. 3.48 The measured and simulated Mag(S) of 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) Mag(S_{33}) (b) Mag(S_{31}) (c) Mag(S_{32}) (d) Mag(S_{34}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
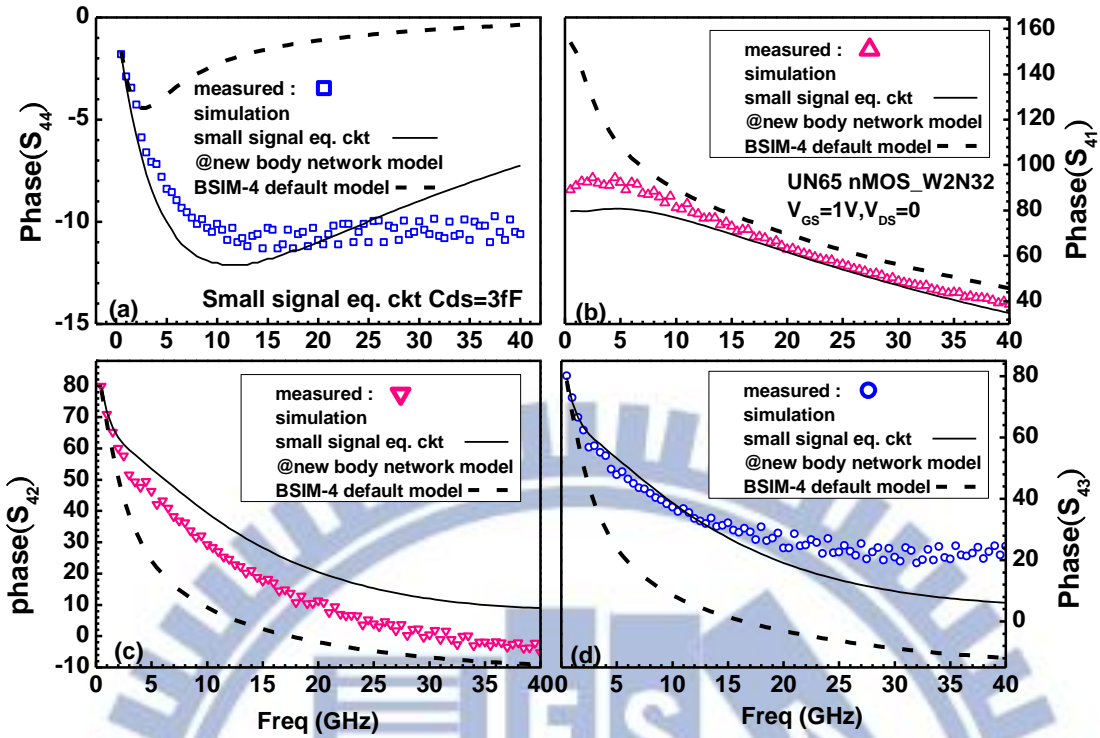
Fig. 3.49 The measured and simulated phase(S) of 4-port MOSFET in linear region $V_{gs}=1.0V$, $V_{ds}=V_{bs}=0$ (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
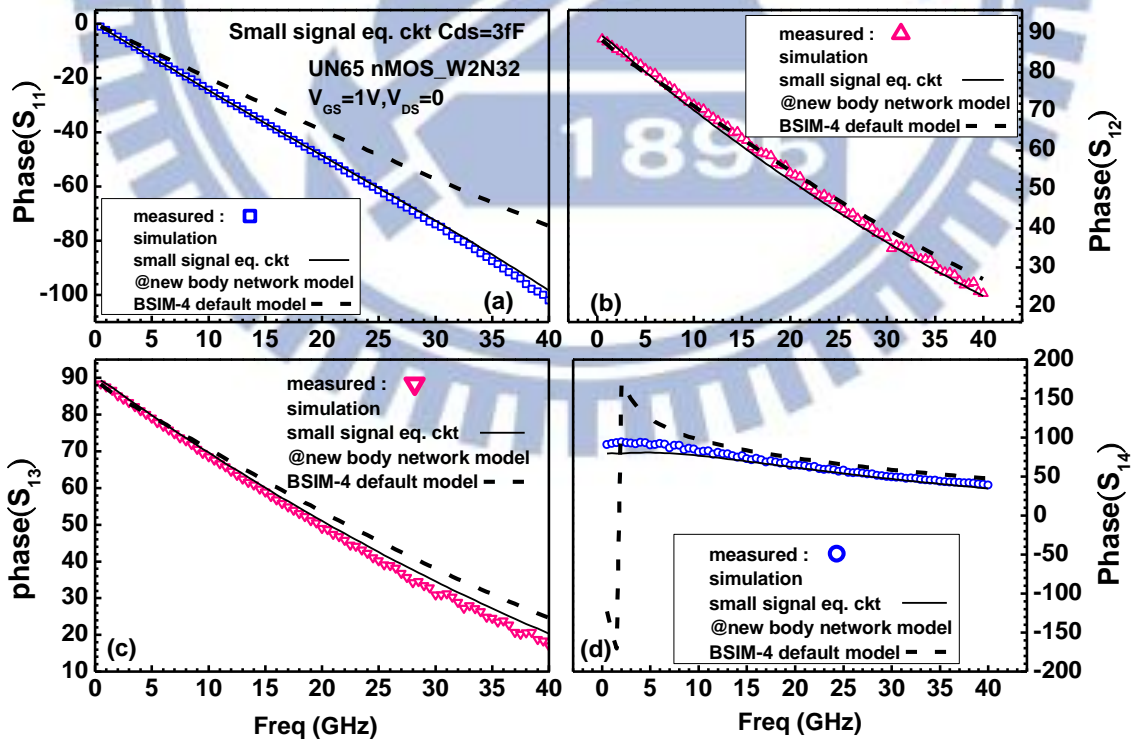
Fig. 3.50 The measured and simulated phase(S) of 4-port MOSFET in linear region $V_{gs}=1.0V$, $V_{ds}=V_{bs}=0$ (a) phase(S_{11}) (b) phase(S_{12}) (c) phase(S_{13}) (d) phase(S_{14}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network
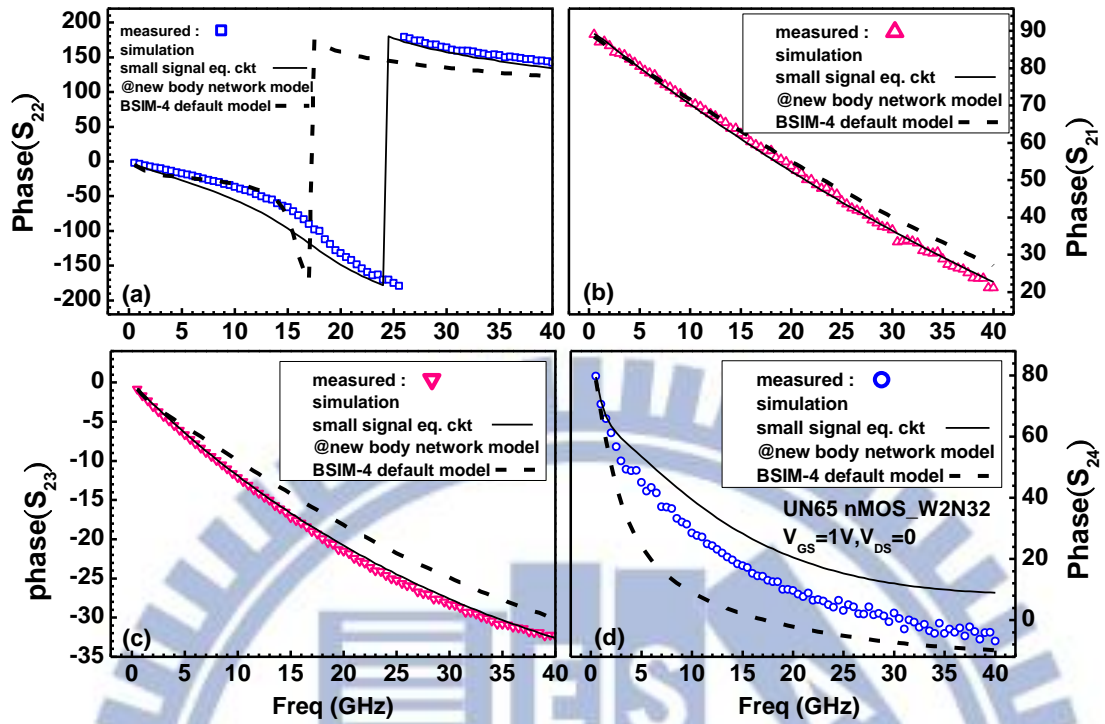
model

Fig. 3.51 The measured and simulated phase(S) of 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) phase(S_{22}) (b) phase(S_{21}) (c) phase(S_{23}) (d) phase(S_{24}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model
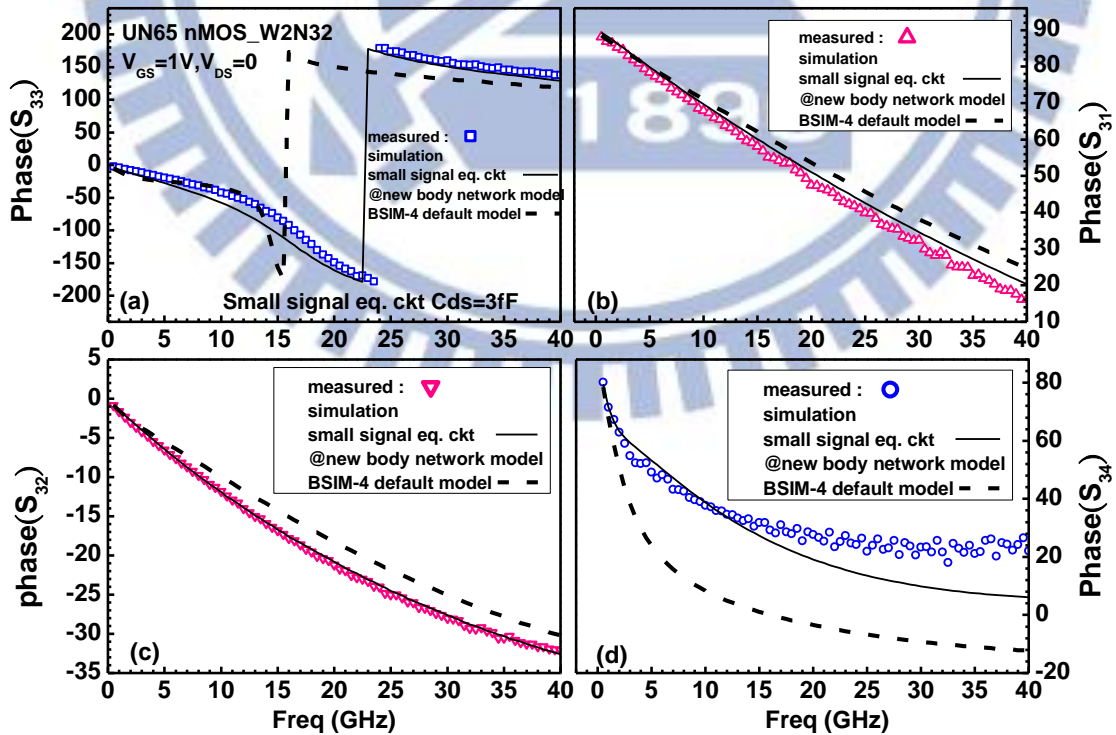
Fig. 3.52 The measured and simulated phase(S) of 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) phase(S_{33}) (b) phase(S_{31}) (c) phaseS$_{32}$) (d) phase(S_{34}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network
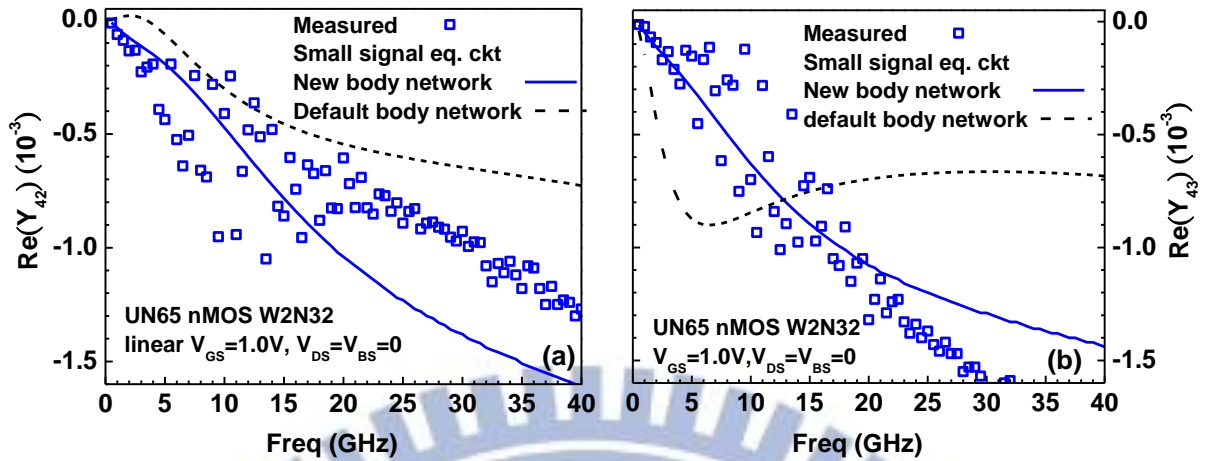
model

Fig. 3.53 Measured and simulated $Re(Y_{42})$ and $Re(Y_{43})$ for 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) $Re(Y_{42})$ (b) $Re(Y_{43})$. Simulation by small signal equivalent circuit model. Solid lines : new body network model. Dash lines : default body network model
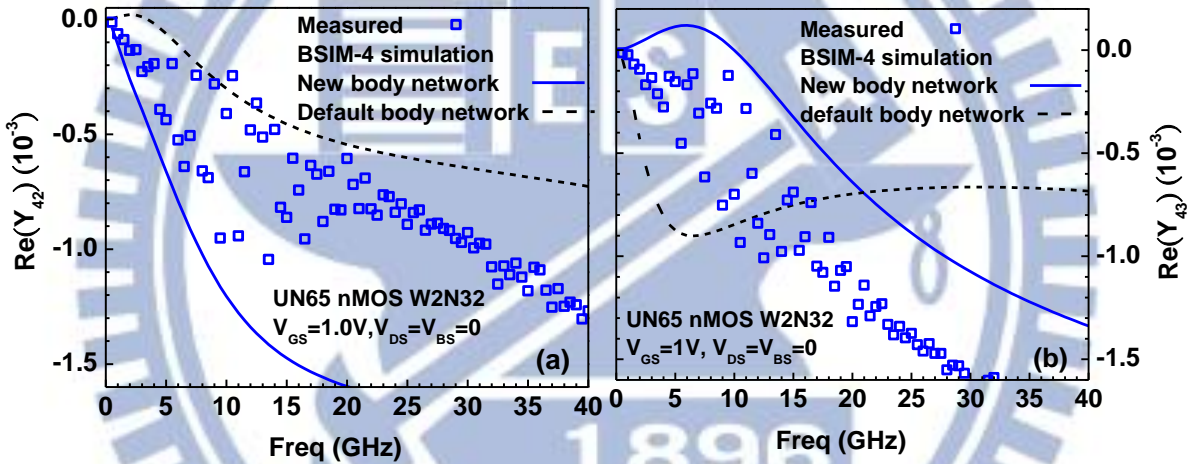
Fig. 3.54 Measured and simulated $Re(Y_{42})$ and $Re(Y_{43})$ for 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) $Re(Y_{42})$ (b) $Re(Y_{43})$. Simulation by BSIM-4, solid lines : with new body network model. Dash lines : with default body network model
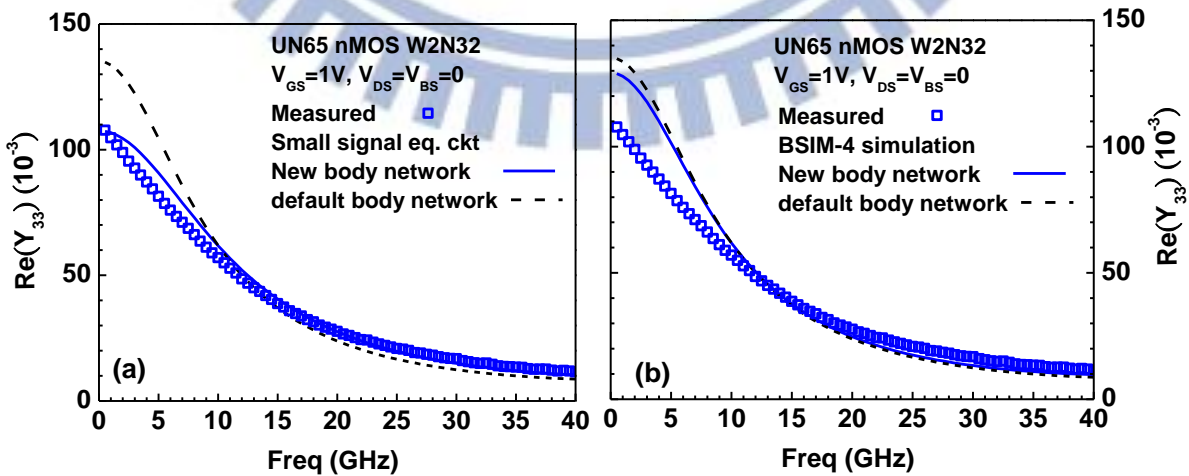
Fig. 3.55 Measured and simulated $Re(Y_{33})$ for 4-port MOSFET in linear region V_{gs}=1.0V, V_{ds}=V_{bs}=0 (a) simulation by small signal equivalent circuit (b) simulation by BSIM-4. Solid

lines : with new body network model. Dash lines : with default body network model

3.3.3 Small Signal Equivalent Circuit in Saturation Region

Finally, the small signal equivalent circuit for 4-port RF MOSFET in saturation region will be developed in this section. Note that the current saturation in short channel devices is dominated by velocity saturation rather than pinch off. Thus, the bias condition responsible for saturation region can be defined by $|V_{gs}| > |V_T|$, $|V_{gs}- V_T| > |V_{ds}| > |V_{dsat}|$, and V_{dsat} is the onset voltage for velocity saturation. In this study for UN65 nMOS with V_{dd}=1.0V, the bias condition is specified as V_{gs}=0.8V and $V_{ds}=V_{dd}$=1.0V for saturation region. Considering the channel conduction is limited by velocity saturation, the channel resistance R_{ch} in linear region is replaced by transconductance g_m and g_{mb} corresponding to gate and body, and output resistance r_o. **Fig. 3.56** illustrates the small signal equivalent circuit proposed for 4-port RF MOSFET in saturation region by adopting g_m, g_{mb}, and r_o along the channel between source and drain. Note that the body network model validated for off state and linear region can be extended to the saturation region when a proper modification is made on some key parameters, e.g. C_{gb1} and C_{gb2}. Again, C_{gs} and C_{gd} are two key parameters for high frequency simulation and can be extracted from measured $-\text{Im}(Y_{12})/\omega$ and $-\text{Im}(Y_{13})/\omega$ after an appropriate open deembedding, as shown in **Fig. 3.57**. The frequency dependence suggests the effect from parasitic inductances, which cannot be eliminated using short M3 deembedding. To overcome this problem, the gate capacitances, C_{gg}, C_{gs}, and C_{gd} are extracted from $\text{Im}(Y_{11})/\omega$, $-\text{Im}(Y_{12})/\omega$, and $-\text{Im}(Y_{13})/\omega$ at very low frequency.
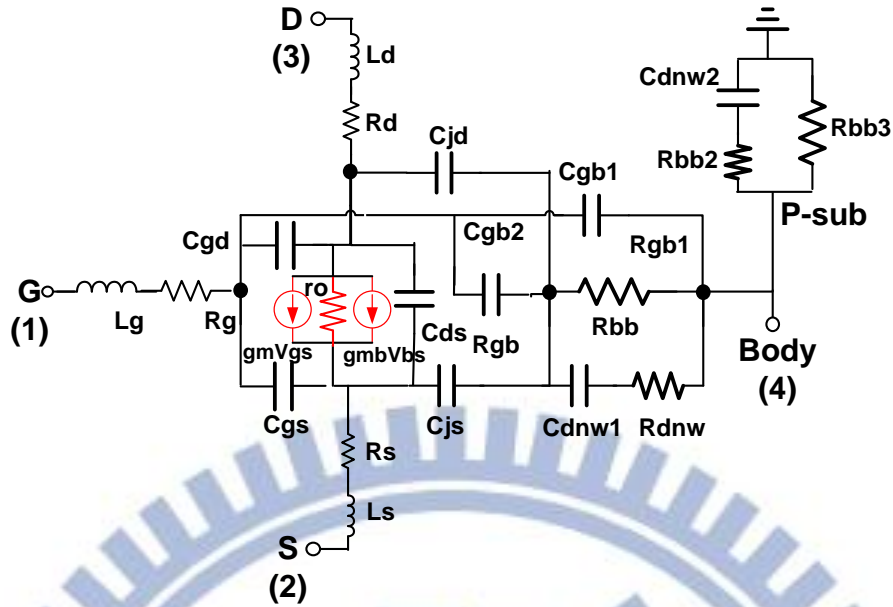
Fig. 3.56 A small signal equivalent circuit for 4-port RF MOSFET in saturation region. g_m, g_{mb}, and r_o are deployed to simulate conduction channel under saturation condition.
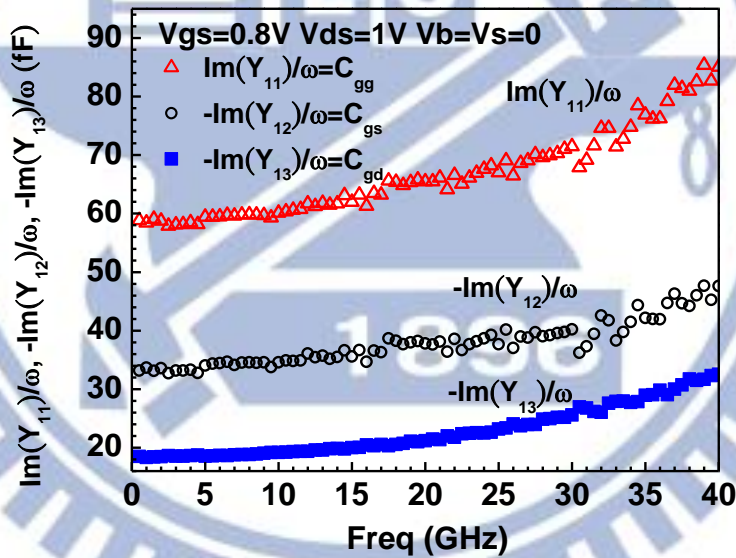
Fig. 3.57 $Im(Y_{11})/\omega$, $-Im(Y_{12})/\omega$, and $-Im(Y_{13})/\omega$ vs. frequency measured from 4-port RF MOSFET in saturation region, $V_{gs}=0.8V$, $V_{ds}=1.0V$, $V_{bs}=0$. C_{gg}, C_{gs}, and C_{gd} determined from $Im(Y_{11})/\omega$, $-Im(Y_{12})/\omega$, and $-Im(Y_{13})/\omega$ at very low frequency.

The extraction flow can be expressed by the iteration flow chart as shown in **Fig. 3.58**. Note that the extraction flow is started with the initial values of g_m and g_{mb} assuming that R_s is negligible and then goes into the optimization flow with extracted r_o and R_s. As a result, the extraction flow is critically dependent on the mentioned four key parameters, such as g_m, g_{mb}, r_o

and R_s.
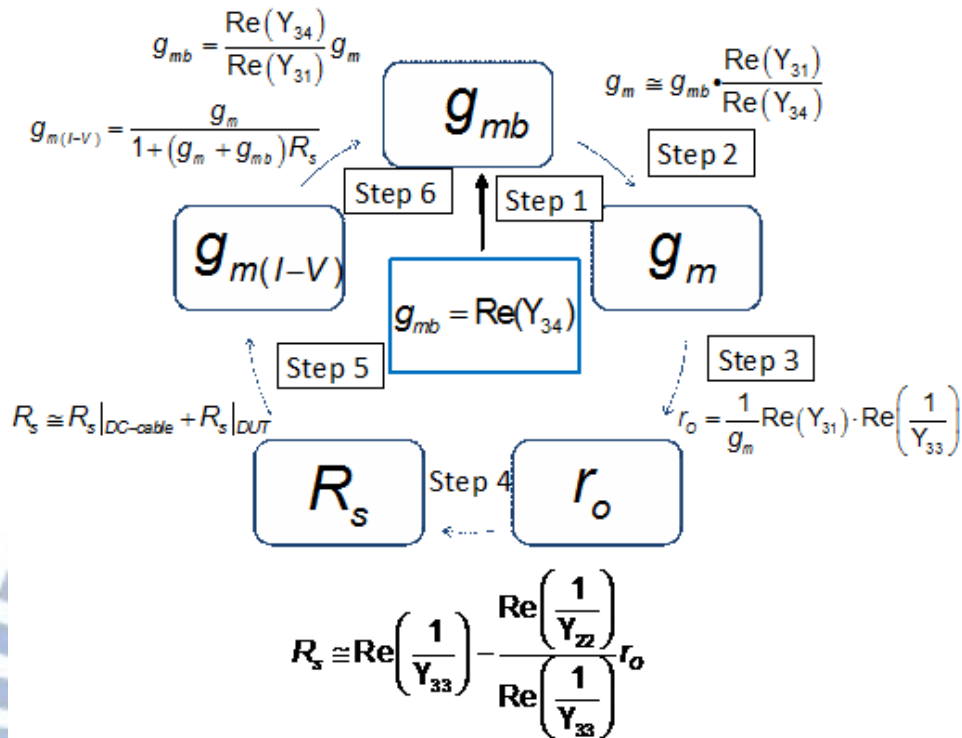
Fig. 3.58 Iteration flow chart for the extraction of gm, gmb, ro, and Rs in 4T RF MOSFETs

Step 1 :

Assume $(g_m + g_{mb})r_o \gg 1$ and $(g_m + g_{mb})R_s \ll 1$,

Then the initial value of gm is determined by $g_{mb} = \text{Re}(Y_{34})$

Step 2 :

The initial value of gm is determined by $g_m \cong g_{mb} \cdot \dfrac{\text{Re}(Y_{31})}{\text{Re}(Y_{34})}$

Step 3 :

The output resistance ro can be extracted from (3.107) with initial gm and measured $\text{Re}(Y_{31})$ and $\text{Re}(1/Y_{33})$.

$$r_o = \frac{1}{g_m}\text{Re}(Y_{31}) \times \text{Re}\left(\frac{1}{Y_{33}}\right)$$

Step 4 :

The source resistance Rs can be extracted from (3.109) with known ro and measured Re(1/Y$_{22}$) and Re(1/Y$_{33}$)

$$R_s \cong \mathrm{Re}\left(\frac{1}{Y_{33}}\right) - \frac{\mathrm{Re}\left(\dfrac{1}{Y_{22}}\right)}{\mathrm{Re}\left(\dfrac{1}{Y_{33}}\right)} r_O$$

Step 5 :

The extrinsic gm associated with I-V can be calculated by intrinsic transcondutance g$_m$ incorporating Rs and Rcable , referring to (3.110) given by

$$g_{m(I-V)} = \frac{g_m}{1+(g_m+g_{mb})R_s}$$

where

$$R_s = R_{s(DUT)} + R_{s(DC\ cable)}$$

Principle of the iteration flow

if calculated $g_{m(I-V)}$ > *measured* $g_{m(I-V)}$

It means that the initial values of gm and g$_{mb}$ are under-estimated then, to increase the initial values of gm and g$_{mb}$, and re-extract r$_o$ and Rs.

Otherwise if $\left(calculated\ g_{m(I-V)} - measured\ g_{m(I-V)}\right) <$ *min. error*

It means that the initial values of gm and g$_{mb}$ are over-estimated.

Then, the next step is to decrease the initial values of g$_m$ and g$_{mb}$, and re-extract r$_o$ and Rs.

The iteration flow can be finished when the difference between the calculated and measured g$_{m(I-V)}$ is less than the specified minimum error, expressed by

$$\left(calculated\ g_{m(I-V)} - measured\ g_{m(I-V)}\right) <\ min.\ error$$

Table 3.6   Iteration flow for g_m and g_{mb} extraction and optimization

Iteration cycles	g_{mb} (A/V)	g_m (A/V)	r_o (Ω)	$R_{s,DUT}$ (Ω)	$g_{m(I\text{-}V)}$ (A/V)
Initial	0.0039	0.0702	99.61538462	-0.69941657	0.068749323
2	0.00395	0.0711	98.35443038	-0.536046905	0.068829516
3	0.004	0.072	97.125	-0.376761481	0.068907885
4	0.00405	0.0729	95.92592593	-0.221409031	0.06898449
5	0.0041	0.0738	94.75609756	-0.069845666	0.069059391
6	0.00415	0.0747	93.61445783	0.078065571	0.069132645
7	0.0042	0.0756	92.5	0.222455111	0.069204304
8	0.00425	0.0765	91.41176471	0.363447251	0.069274421
9	0.0043	0.0774	90.34883721	0.501160503	0.069343044
10	0.00435	0.0783	89.31034483	0.635707934	0.069410221
11	0.0044	0.0792	88.29545455	0.767197468	0.069475998
12	0.00445	0.0801	87.30337079	0.895732182	0.069540417
13	0.0045	0.081	86.33333333	1.021410568	0.06960352
14	0.00455	0.0819	85.38461538	1.144326792	0.069665346
15	0.0046	0.0828	84.45652174	1.264570925	0.069725936
16	0.00465	0.0837	83.5483871	1.382229162	0.069785324
17	0.0047	0.0846	82.65957447	1.497384032	0.069843547
18	0.00475	0.0855	81.78947368	1.610114589	0.069900638
19	0.0048	0.0864	80.9375	1.720496593	0.069956631
20	0.00485	0.0873	80.10309278	1.828602679	0.070011556
21	0.0049	0.0882	79.28571429	1.934502519	0.070065443
22	0.00495	0.0891	78.48484848	2.038262968	0.070118323
23	0.005	0.09	77.7	2.139948208	0.070170222
24	0.00505	0.0909	76.93069307	2.239619879	0.070221169
25	0.0051	0.0918	76.17647059	2.337337203	0.070271188
26	0.00515	0.0927	75.4368932	2.433157104	0.070320305
27	0.0052	0.0936	74.71153846	2.527134314	0.070368545
28	0.00525	0.0945	74	2.619321482	0.07041593
29	0.0053	0.0954	73.30188679	2.709769269	0.070462483
30	0.00535	0.0963	72.61682243	2.798526444	0.070508225
31	0.0054	0.0972	71.94444444	2.885639967	0.070553179
32	0.00545	0.0981	71.28440367	2.971155078	0.070597363

Table 3.6 illustrates an example of the extraction flow based on the data measured from L65003. In this study, the measured $g_{m(I\text{-}V)}$ is 68.5 mA/V and it happens that the 13th cycle with g_m=81 mA/V and R_s=1.02 leads to calculated $g_{m(I\text{-}V)}$ =69.7 mA/V, which approached the measured $g_{m(I\text{-}V)}$ with error 1.2 mA/V, i.e. relative error of 1.2%. Furthermore, the proposed assumptions for this extraction/iteration flow are verified as follows

Step 1 assumption

$$(g_m + g_{mb})r_O \gg 1 \text{ and } (g_m + g_{mb})R_s \ll 1$$

$g_{mb} = 4.5 mA/V, \ g_m = 81 \ mA/V, \ r_O = 86.33\Omega, \ R_s = 1.02\Omega$

$(g_m + g_{mb})r_O = 7.38 < 10 \Rightarrow$ *may introduce certain error from the assumption*

$(g_m + g_{mb})R_s = 0.08721 \ll 1 \Rightarrow$ *valid assumption*

Assumption to derive (A9)~(A12): $\ r_O \gg R_d$

$r_O = 86.33\Omega, \ R_s = 1.02\Omega$

$S/D \ layout \ symmetry \Rightarrow R_d \cong R_s = 1.02\Omega$

$\dfrac{r_O}{R_d} = 84.64 \Rightarrow r_O \gg R_d \Rightarrow$ *valid assumption*

Table 3.7 summarizes the small signal equivalent circuit model parameters for 4-port RF MOSFET in saturation region. It appears that the increase of V_{ds} to saturation region leads to decrease of C_{gd} whereas increase of C_{gs}, due to non-uniform distribution of inversion carriers at source and drain. C_{gs} is larger than C_{gd} by near 80% and it accounts for drain side carriers depletion effect. Note that three key parameters for saturation region, such as g_m, g_{mb}, and r_o are determined by aforementioned extraction flow and the values listed in **Table 3.7** are optimized one for the best fitting to measured I-V and S-parameters.

Table 3.7 Small signal equivalent circuit model parameters of 4-port MOSFET in saturation region (V_{gs}=0.8V, V_{ds}=1.0V, V_{bs}=0)

4-port MOSFET model parameters in saturation region					
Capacitances	**(fF)**	**Resistances**	**Ω**	**Inductances**	**pH**
Cgs	33.16	Rg	6.5	Ls	60
Cgd	18.48	Rd	1	Ld	60
Cgb1	2.5	Rs	1	Lg	70
Cgb2	3.5	Rb	1	Lb	70
Cg	2.1	Rbb	958	**Transconductance**	**mA/V**
Cds	2	Rbb2	664	gm	81
Cjs	22.42	Rbb3	5484	gmb	4.5
Cjd	18.75	Rdnw	476	**Output resistance**	**Ω**
Cdnw1	44.94	Rgb	518500	ro	86
Cdnw2	44.94	Rgb1	500		

According to the model parameters shown in **Table 3.7** for 4-port MOSFETs in

saturation region, S- and Y-parameters can be simulated. **Fig. 3.59 ~ Fig. 3.66** present the 4-port S-parameters from measurement and simulation for this 4-port MOSFET (W2N32) in saturation region under the biases of V_{gs}=0.8V, V_{ds}=1V, and V_{bs}=0. Note that the simulation by using the small signal equivalent circuit shown in **Fig. 3.56** and model parameters in **Table 3.7** was compared with those calculated by BSIM-4 default model. The results indicate that the small signal equivalent circuit can predict 4-port S-parameters with promisingly good accuracy except a few parameters, such as Mag(S_{21}), Mag(S_{22}), Mag(S_{31}), Mag(S_{34}), phase(S_{41}), and phase(S_{24}) with somewhat larger mismatch. However, the simulation using BSIM-4 default model reveals large deviation from the measurement, particularly for the components related to the body, i.e. port-4, e.g. Mag(S_{44}), Mag(S_{41}), Mag(S_{42}), and Mag(S_{43}) as shown in **Fig. 3.59** and phase(S_{44}), phase(S_{41}), phase(S_{42}), and phase(S_{43}) as shown in **Fig. 3.63**. Besides S-parameters, Re(Y_{42}), Re(Y_{43}), and Re(Y_{33}) are three more important parameters to verify the body network model. **Fig. 3.67** indicates that the small signal equivalent circuit with new body network can improve simulation accuracy for Re(Y_{42}) and Re(Y_{43}) compared with those simulated by using default body network model. **Fig. 3.68** presents similar effect from body network model when applied to BSIM-4 for Re(Y_{42}) and Re(Y_{43}) simulation. Similar with the condition for off state, the impact from body network model on Re(Y_{33}), i.e. the key parameter responsible for output resistance, is relatively smaller, as shown in **Fig. 3.69.** Again, the new body network model can be applied to both small signal equivalent circuit and BSIM-4 for an accurate simulation in linear region. The verification by extensive data suggests that body network model is the key to determine simulation accuracy for 4-port RF MOSFETs and proves that the new body network proposed for saturation region (**Fig. 3.56**) can improve the problem with BSIM-4 for 4-port MOSFET simulation.
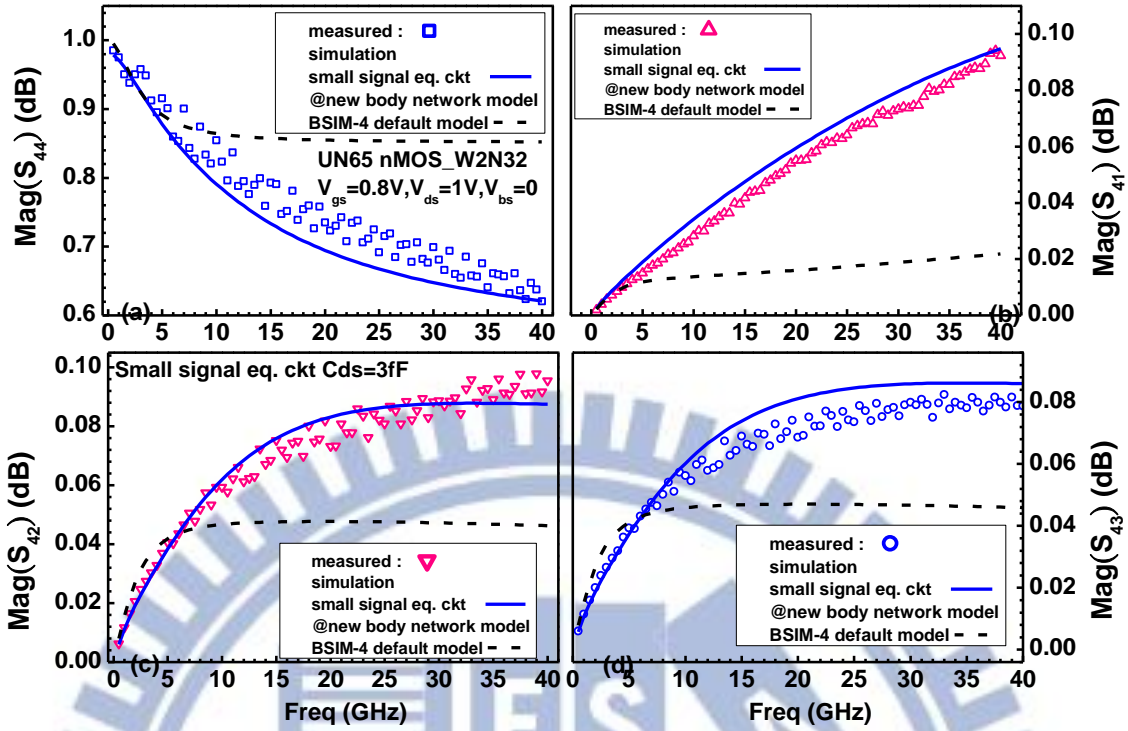
Fig. 3.59 The measured and simulated Mag(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
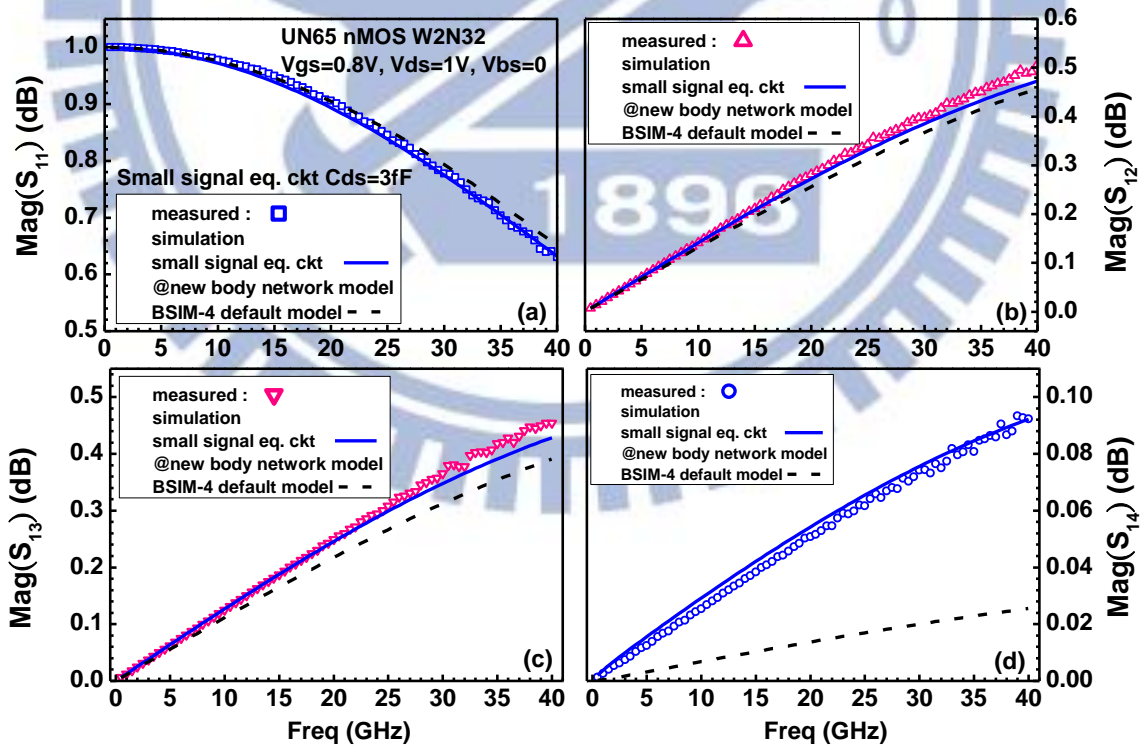
Fig. 3.60 The measured and simulated Mag(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
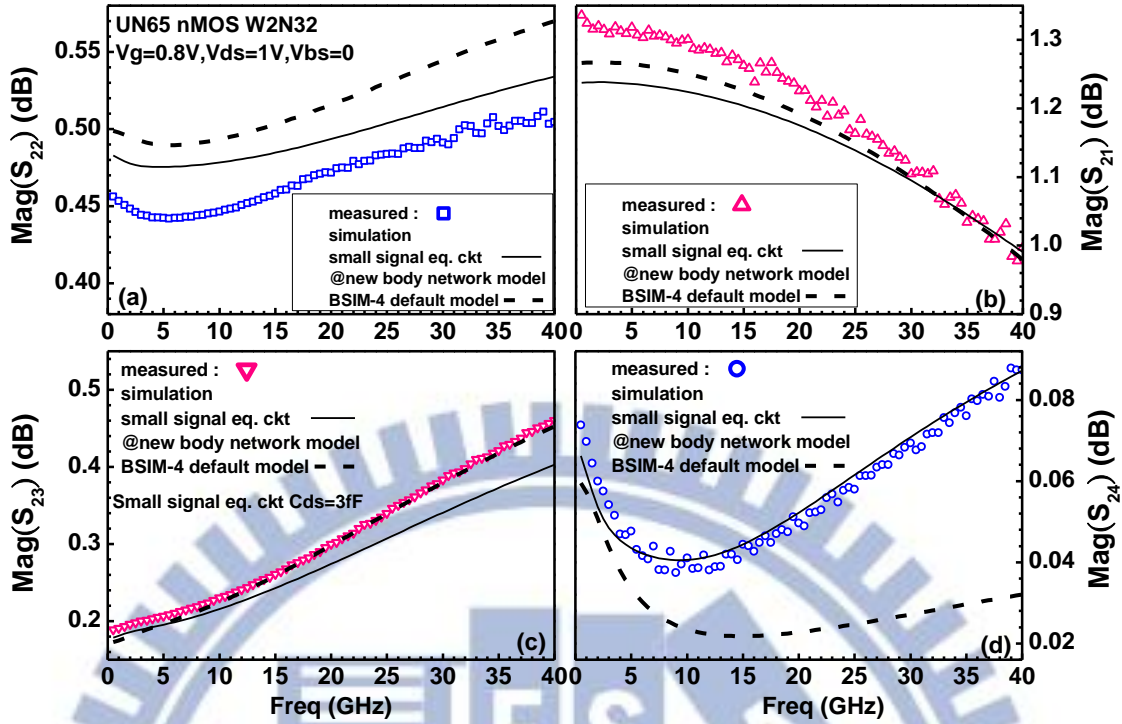
Fig. 3.61 The measured and simulated Mag(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) Mag(S_{22}) (b) Mag(S_{21}) (c) Mag(S_{23}) (d) Mag(S_{24}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
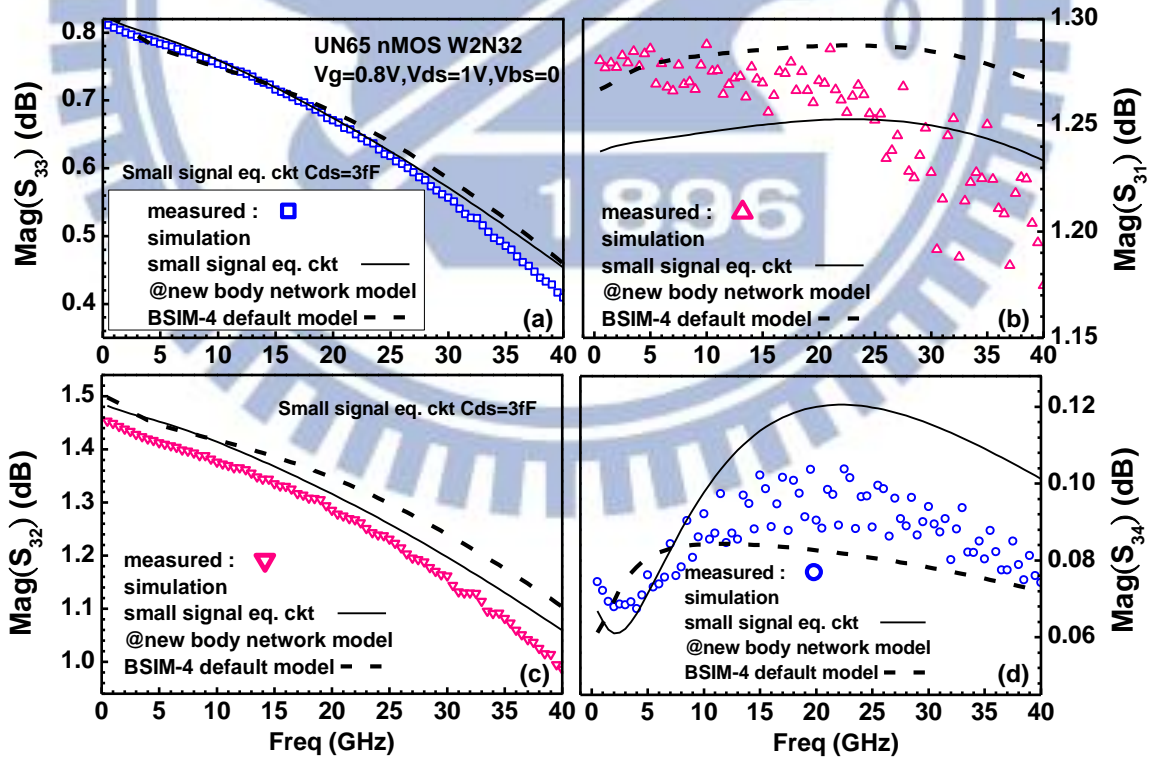
Fig. 3.62 The measured and simulated Mag(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) Mag(S_{33}) (b) Mag(S_{31}) (c) Mag(S_{32}) (d) Mag(S_{34}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
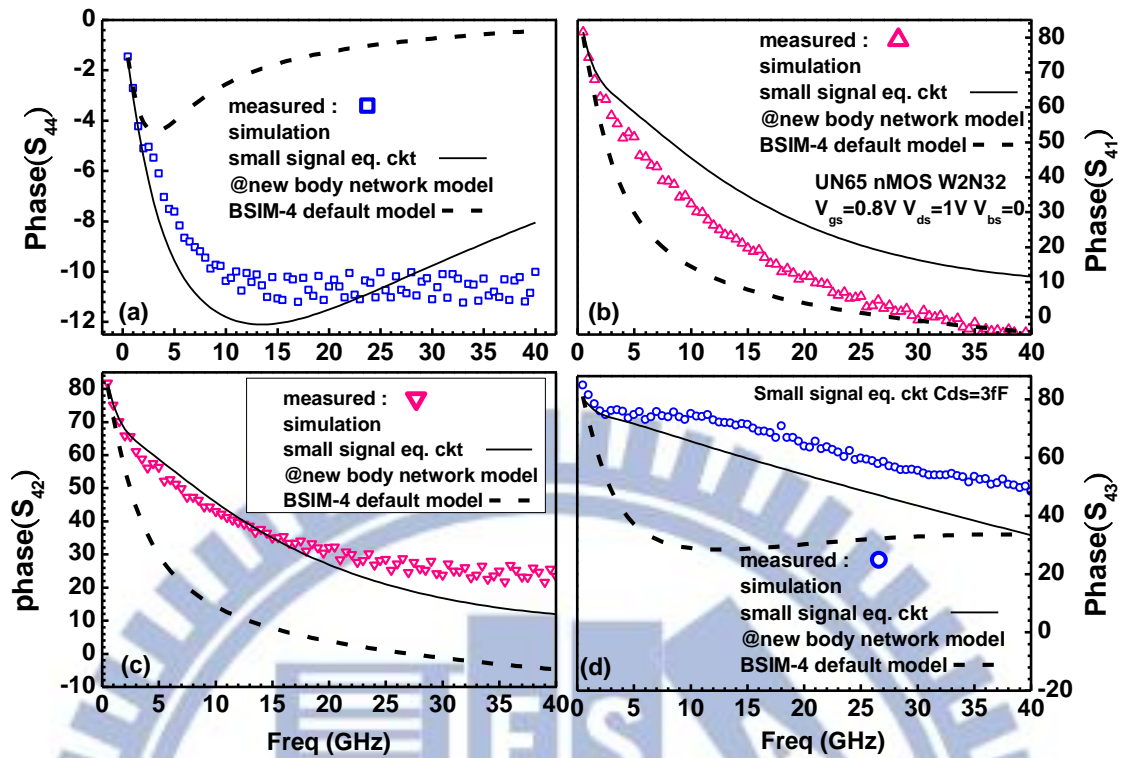
Fig. 3.63 The measured and simulated phase(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
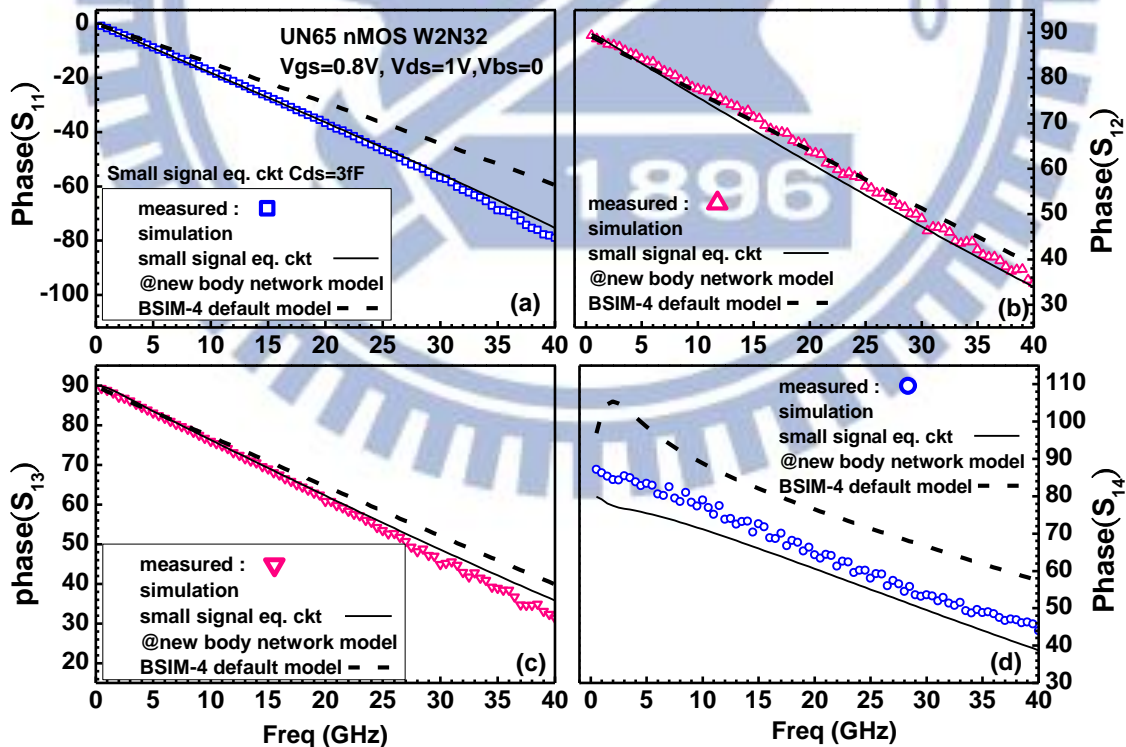
Fig. 3.64 The measured and simulated phase(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) phase(S_{11}) (b) phase(S_{12}) (c) phase(S_{13}) (d) phase(S_{14}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
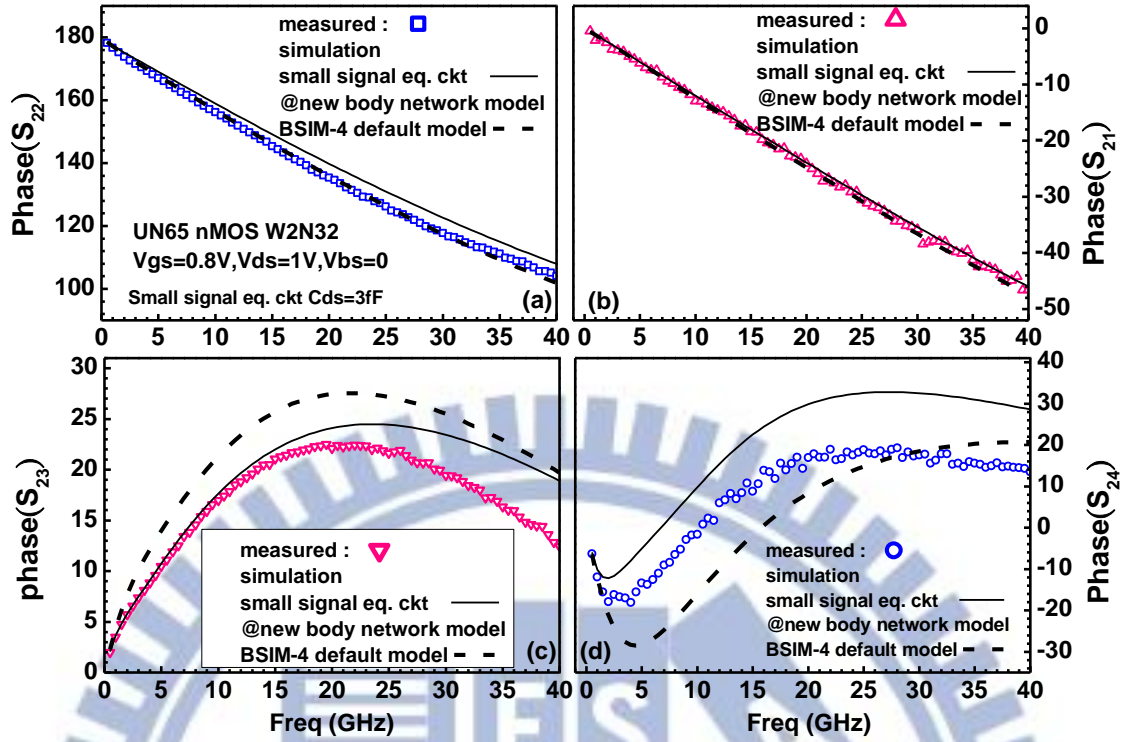
Fig. 3.65 The measured and simulated phase(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) phase(S_{22}) (b) phase(S_{21}) (c) phase(S_{23}) (d) phase(S_{24}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.
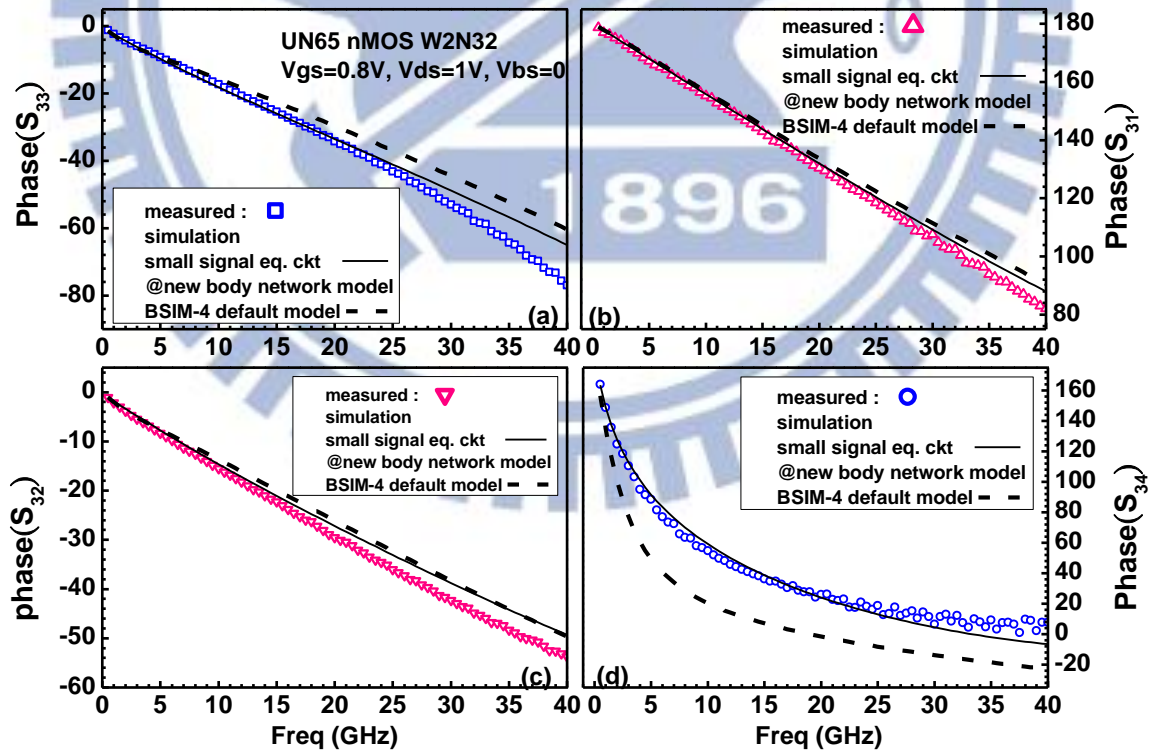
Fig. 3.66 The measured and simulated phase(S) of 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) phase(S_{33}) (b) phase(S_{31}) (c) phase(S_{32}) (d) phase(S_{34}). Solid lines : small signal equivalent circuit with new body network model. Dash lines : BSIM-4 with default body network model.

82
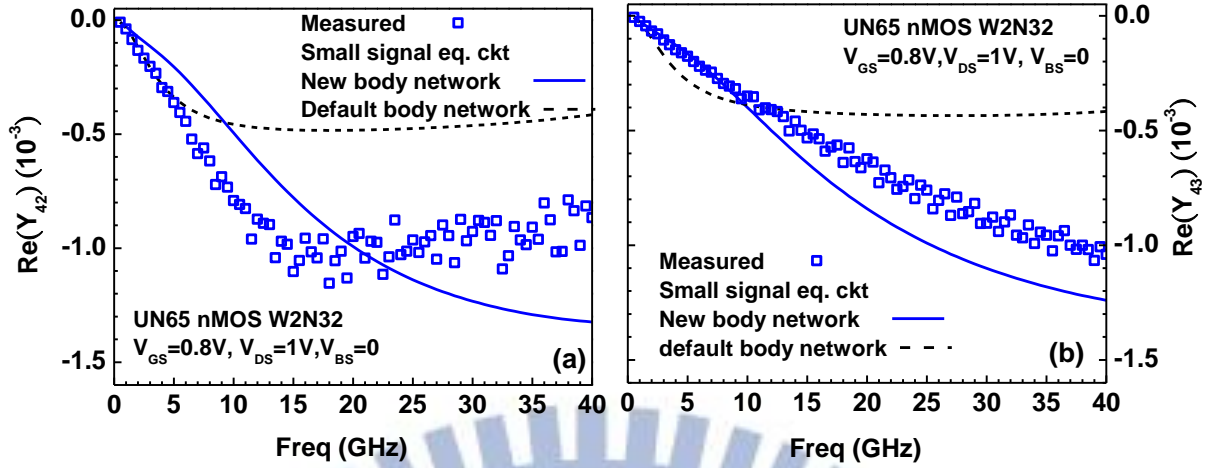
Fig. 3.67 Measured and simulated $Re(Y_{42})$ and $Re(Y_{43})$ for 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) $Re(Y_{42})$ (b) $Re(Y_{43})$. Simulation by small signal equivalent circuit model. Solid lines : new body network model. Dash lines : default body network model
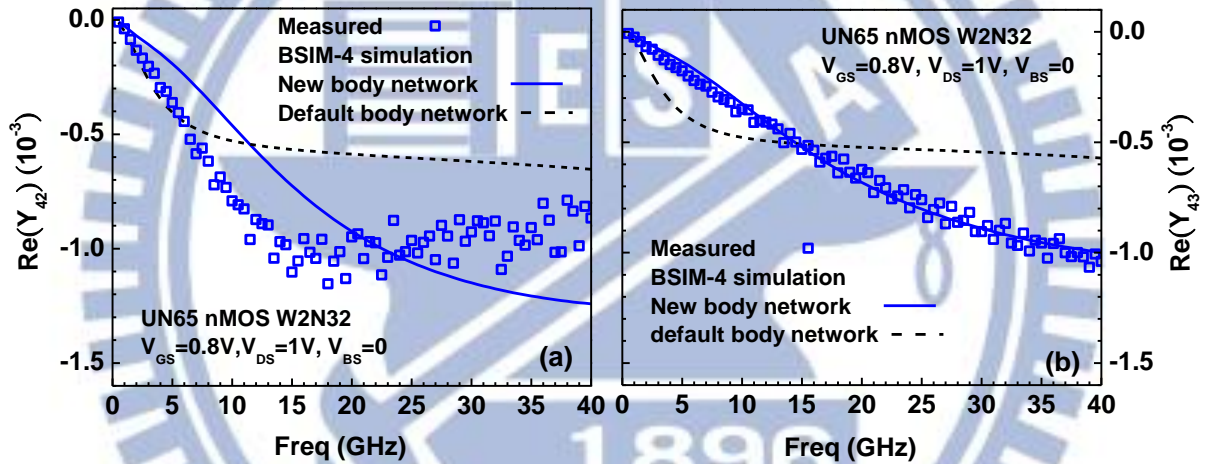
Fig. 3.68 Measured and simulated $Re(Y_{42})$ and $Re(Y_{43})$ for 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) $Re(Y_{42})$ (b) $Re(Y_{43})$. Simulation by BSIM-4. Solid lines : new body network model. Dash lines : default body network model
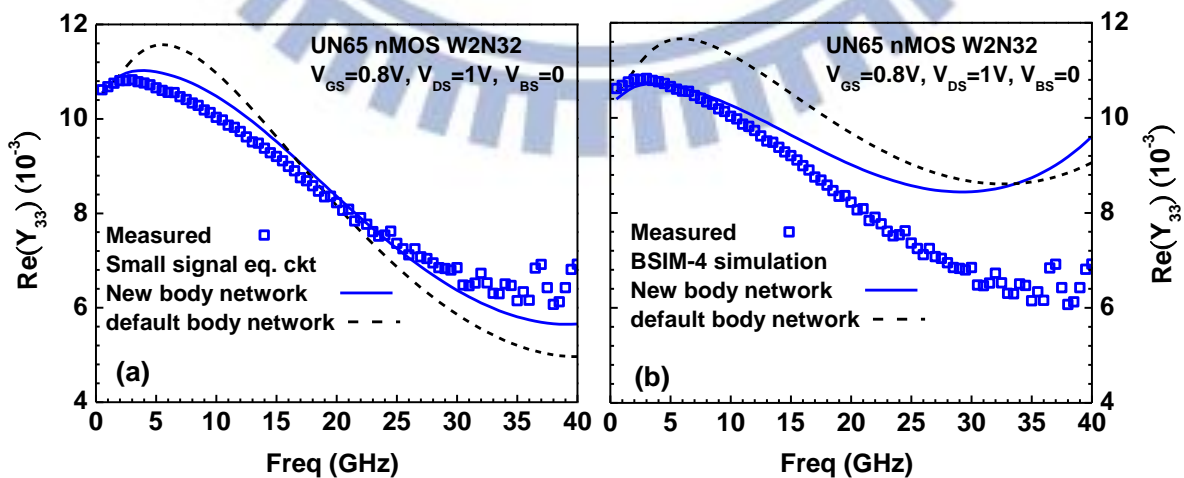
Fig. 3.69 Measured and simulated $Re(Y_{33})$ for 4-port MOSFET in saturation region V_{gs}=0.8V, V_{ds}=1V, V_{bs}=0 (a) simulation by small signal equivalent circuit (b) simulation by BSIM-4.

83

Solid lines : with new body network model. Dash lines : with default body network model

3.4 BSIM-4　with Improved Body Network Model for Four-port RF MOSFET Simulation

BSIM-2,3,4 have been widely used in semiconductor industry as the public domain model for Si based CMOS circuits simulation and design. The core models of BSIM can be classified as I-V model for DC simulation, C-V model for AC/transient/RF simulation, and noise model for RF/analog simulation . The first one, i.e. I-V model incorporates a number of basic and well known models, such as threshold voltage (V_T) model, drain current model including mobility model and velocity saturation, channel charge and subtheshold swing models, gate tunneling model, and body current model. The second one, i.e. C-V model includes gate capacitance model and junction diode model. The last one, i.e. noise model covers flicker noise and thermal noise models. Recently, the most updated BSIM-4 has incorporated the new feature, i.e. layout dependent stress effects into the mobility model [17] , which is indispensable for simulating nanoscale CMOS. In recent work of our research group supervised by Professor Guo, an extensive investigation has been performed to explore layout dependent stress effect on high frequency characteristics and low frequency noise. Lot of innovative and interesting results have been published in IEEE IMS MTT-s, IEEE RFIC symp., SSDM, and most importantly in IEEE Trans. on electron devices **[18-20]** The next step for us to continue the research effort is to implement the layout dependent stress effects in mobility and low frequency noise model, hopefuly an enhancement of BSIM-4 to improve the accuracy for multi-finger MOSFET simulation, which is critical for RF and analog circuit simulation and design.

Besides the core models, parameter extraction methodology is another important building block to facilitate a reliable operation and determine the accuracy and efficiency of the model for simulation and design. Conventionally multiple devices with different dimensions like gate lengths and gate widths are required to realize a complete extraction flow, which is composed of 25 steps defined in BSIM-4 user manual. To meet this purpose, a large chip area is needed to

accommodate sufficient test devices with a broad span of layout dimensions to cover both typical and corner conditions. The mentioned test chips specifically for model parameters extraction can be internally supported in foundry. Unfortunately, the chip area allowed for academic research like ours in the university is very limited and definitely cannot meet the requirement of a complete extraction flow. Due to this restriction, a compromised approach is employed to figure out an optimized model, which can fit the standard device with nominal rule dimension or few devices under small range of splits from the nominal rule.

3.4.1 BSIM-4 I-V Model Calibration and Simulation for 65nm 4-port RF MOSFET with DBB - UN65 L65003

In this thesis, 4-port RF MOSFETs with multi-finger structure and typical gate length have been designed and fabricated using UMC 65nm (UN65) CMOS process in which the physical gate oxide thickness is 1.6 nm and typical gate length on layout is 60 nm. The 4-port test structure is implemented to support 4-terminal (4T) MOSFETs in which the body and source are separated to allow various body biases, such as forward body bias (FBB), reverse body bias (RBB), and zero body bias (ZBB). The freedom of body biases is so call dynamic body biases (DBB) scheme and becomes a potential solution for low voltage and low power design. The controllable V_T shift from DBB, namely dynamic V_T becomes an effective approach to reducing voltage at on-state for low active power and suppressing leakage at off-state. To accurately predict the V_T shift under DBB, the threshold voltage (V_T) model becomes the first important model to be verified.

As shown in (3.49), the V_T model implemented in BSIM-4 incorporates several geometry and bias dependent effects, such as short channel effect (SCE), narrow width effect (NWE), drain induced barrier lowering effect (DIBL), and drain induced threshold voltage shift effect (DITS). Short channel effect (SCE) is generally defined as V_T lowering due to channel length reduction. The basic mechanism responsible for SCE is charge sharing effect from the depletion layer near the source/drain (S/D) junctions. The V_T lowering effect becomes worse when

increasing drain bias and/or reverse body bias, due to increasing depletion layer width and is implemented as DIBL effect, which is a function of drain voltage (V_{ds}) and body bias (V_{bs}). For planar CMOS devices, channel length scaling to deep submicron and further to nanoscale regime, SCE and DIBL become excessively large and lead to extraordinarily high leakage current at off state. To fix this problem, the conventional channel doping technique is no longer valid and non-uniform channel engineering using retrograde channel and halo implantations becomes an effective solution. The former one, i.e. retrograde channel implantation results in vertical non-uniform channel profile and the latter one, i.e. halo implantation creates lateral non-uniform channel profile. The lateral non-uniform channel profile from halo implantation can reduce SCE in sufficiently short devices and keep body effect reasonably low (prevent from excessive increase of body effect) for very long devices. Unfortunately, the lateral non-uniform channel profile with lightly doped central channel and heavily doped halo region near S/D leads to undesired V_T shift when increasing V_{ds} in very long channel devices, which is defined as DITS in BSIM-4 [5]. The mechanism responsible DITS comes from the surface potential variation of the lightly doped channel, which is strongly modulated by drain bias even at subthreshold region [6-7].

$$V_{th} = VTH0 + (K_{1OX} \cdot \sqrt{\Phi_S - V_{bseff}} - K1 \cdot \sqrt{\Phi_S})\sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2OX}V_{bseff} + K_{1OX}\left(\sqrt{1 + \frac{LPEB}{L_{eff}}} - 1\right)\sqrt{\Phi_S} \quad \text{body effect}$$

$$-0.5 \cdot \left[\frac{DVT0W}{\cosh\left(DVT1W \frac{L_{eff}W_{eff}'}{\ell_{tw}}\right) - 1} + \frac{DVT0}{\cosh\left(DVT1 \frac{L_{eff}}{\ell_t}\right) - 1} \right](V_{bi} - \Phi_S) \quad \text{SCE}$$

$$-\frac{0.5}{\cosh\left(DSUB \frac{L_{eff}}{\ell_t}\right) - 1}(ETA0 + ETAB \cdot V_{bseff}) \cdot V_{ds} \quad \text{DIBL}$$

$$-nv_t \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0(1 + e^{-DVTP1 \cdot V_{ds}})}\right) \quad \text{DITS}$$

$$+(K3 + K3B \cdot V_{bseff})\frac{TOXE}{W_{eff}' + W0}\Phi_S \quad \text{NWE}$$

Where   (3.49)

$$\ell_t = \sqrt{\frac{\varepsilon_{Si} \cdot TOXE \cdot X_{dep}}{\varepsilon_{ox} \cdot \eta}}, \quad X_{dep} = \sqrt{\frac{2\varepsilon_{Si}(\Phi_s - V_{bs})}{qNDEP}}$$

$$v_t = \frac{k_B T}{q}$$

(3.50)

The model equation implemented for every individual effect is described as follows. The first term in (3.49) represents the body bias effect of the V_T subject to non-uniform channel doping profiles from retrograde and halo implantations. VTHO is the virgin V_T for ideally long channel device under zero body bias. K1ox represent the first-order body effect coefficient for uniformly doped channel and and K2ox is the second-order coefficient due to vertical non-uniform doping profile from retrograde channel implantation. L_{eff} is the effective channel length, which is different from the gate length on layout. Note that L_{eff} used in I-V model may be different from that used in C-V model. LPEB denotes the length subject to lateral non-uniform doping profile from halo implantation and the larger ratio of LPEB/L_{eff}, i.e. the longer LPEB and/or shorter L_{eff}, will lead to higher V_T and larger body bias effect.

$$VTH0 + (K_{1OX} \cdot \sqrt{\Phi_S - V_{bseff}} - K1 \cdot \sqrt{\Phi_S})\sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2OX}V_{bseff} + K_{1OX}\left(\sqrt{1 + \frac{LPEB}{L_{eff}}} - 1\right)\sqrt{\Phi_S}$$

The second term in (3.49) represents the SCE as a function of L_{eff}, characteristic length ℓ_t, built-in potential V_{bi}, and surface potential Φ_S. Note that the characteristics length ℓ_t defined by (3.50) is determined by the substrate depletion width X_{dep} and electrical equivalent oxide thickness TOXE. The wider X_{dep} and/or thicker TOXE will lead to longer ℓ_t, i.e. smaller ratio L_{eff}/ℓ_t and then worse SCE, i.e. larger V_T lowering due to SCE. On the other hand, the higher channel doping concentration to reduce X_{dep} and/or thinner TOXE can help reduce ℓ_t and suppress SCE.

$$-0.5 \cdot \left[\frac{DVT0W}{\cosh(DVT1W\frac{L_{eff}W_{eff}'}{l_{tw}}) - 1} + \frac{DVT0}{\cosh(DVT1\frac{L_{eff}}{l_t}) - 1}\right](V_{bi} - \Phi_S)$$

DIBL has been known as another form of short channel effects, which becomes worse when increasing V_{ds}. The primary mechanism responsible for DIBL is the source to channel barrier lowering driven by the raised surface potential at drain end, due to drain bias V_{ds}. The third term

in (3.49) represents the DIBL as a function of V_{ds}, effective body bias ($V_{bs,eff}$), L_{eff} and the ratio w.r.t. ℓ_t, i.e. L_{eff}/ℓ_t. This DIBL model assumes the V_T shift as a linear function of V_{ds}. In addition to the linear dependence of V_{ds}, the body bias under reverse condition will increase DIBL effect and resulted V_T lowering.

$$-\frac{0.5}{\cosh(DSUB\frac{L_{eff}}{\ell_t})-1}(ETA0+ETAB\cdot V_{bseff})\cdot V_{ds}$$

The fourth term in (3.49) represents DITS effect as an exponential function of V_{ds} [21]. As mentioned previously, this DITS becomes significant in sufficiently long device and is simulated as a function of L_{eff} as follows. Note that the longer L_{eff} and higher V_{ds} makes the term inside the ℓn approach unity and resulted V_T shift becomes very small. The result looks in contradiction with the expected DITS that is the larger V_T shift associated with longer devices.[22, 23]

$$-nv_t\ell n\left(\frac{L_{eff}}{L_{eff}+DVTP0(1+e^{-DVTP1\cdot V_{ds}})}\right)$$

The last term in (3.49) represent narrow width effect (NWE) for CMOS using LOCOS or inverse narrow width effect (INWE) for modern CMOS devices using STI as the isolation technology[24].

$$(K3+K3B\cdot V_{bseff})\frac{TOXE}{W_{eff}'+W0}\Phi_S$$

Where, TOXE is electrical gate oxide thickness and W_{eff} is the effective channel width.

In older technologies before 0.25um node, the LOCOS adopted as the isolation technique generally leads to narrow width effect, i.e. the narrower width, the higher $|V_T|$. The increase of $|V_T|$ with width scaling is originated from the bird's beak around the LOCOS corner, which contributes additional body charges required for depletion and lead to higher $|V_T|$. As for modern technologies since 0.25um node, the isolation technique has been switched from LOCOS to STI. New feature associated with STI is that 2-dimensional field crowding effect

and gate oxide thinning due to divot near STI top corner results in $|V_T|$ lowering from channel width scaling and it is known as inverse narrow width effect (INWE)[24]. In this study using 65nm CMOS technology (UN65), the width dependence of V_T should follow STI feature, i.e. INWE and the parameter K3 implemented in V_T model of BSIM-4 for width dependence becomes negative to generate V_T lowering with width reduction.

Besides V_T model, mobility model is recognized as one more important model for accurate I-V simulation of MOSFETs. As a matter of fact, the carriers transport in inversion mode MOSFET is a kind of surface conduction instead of bulk transport. The carriers transport along the inversion channel encounters multiple scattering effects, such as phonon scattering, coulomb scattering, and surface roughness sattering. Note that all of three scattering mechanisms are dependent on the normal electric field E_{eff} at gate oxide/Si substrate interface, determined by the gate bias V_{GS} and workfunction or gate overdrive V_{GT}, and gate oxide thickness (TOXE). The effective mobility μ_{eff} is determined by the Matthiessen's rule given by (3.51)-(3.54). Theoretically, the coulomb scattering dominates at low field and the surface roughness scattering becomes the dominant mechanism at high field. Phonon scattering plays a role in the medium field where coulomb scattering and surface roughness scattering become less important. In BSIM-4, the normal field E_{eff} is calculated as a function of effective gate overdrive $V_{gst,eff}$, threshold voltage V_{th}, and electrical gate oxide thickness TOXE given by (3.55) for n-MOSFETs. According to (3.51)-(3.55), the effective mobility μ_{eff} is simulated by the formula with the expression of (8) in which U0 represents the bulk mobility free from surface scattering, UA and UB are first–order and second-order coefficients for surface roughness scattering at higher field, and the last term with UD is proposed to simulate coulomb scattering at very low field. Note that body bias effect is incorporated in the linear term of normal field, i.e. the first order of surface roughness scattering and UC is fitting parameter to adjust body bias effect. For RBB, UC is positive to increase the normal field and surface scattering, and then degrade μ_{eff}. As for FBB, UC

becomes negative to decrease the normal field and suppress the surface scattering, and then enhance μ_{eff}.

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{coul}}} + \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{sr}}} \tag{3.51}$$

$$\mu_{\text{coul}} = AE_{\text{eff}}^{\alpha 1}T^{\alpha 2} \tag{3.52}$$

$$\mu_{\text{ph}} = AE_{\text{eff}}^{-\beta 1}T^{-\beta 2} \tag{3.53}$$

$$\mu_{\text{sr}} = AE_{\text{eff}}^{-\gamma} \tag{3.54}$$

$$E_{\text{eff}} = \frac{1}{6}\frac{(V_{gst,\text{eff}} + 2V_{th})}{TOXE} \tag{3.55}$$

$$\mu_{\text{eff}} = \frac{U0 \cdot f(L_{\text{eff}})}{1 + (UA + UCV_{bseff})\left(\frac{V_{gseff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gseff} + 2V_{th}}{TOXE}\right)^2 + UD\left(\frac{V_{th} \cdot TOXE}{V_{gseff} + 2V_{th}}\right)^2} \tag{3.56}$$

Coulomb scattering

As mentioned previously, V_T and mobility models are fundamental models for accurate simulation of drain current in strong inversion region. Regarding the subthreshold I-V simulation, a unified channel charge density model adapted to both subthreshold and strong inversion regions is proposed to ensure a continuous and smooth transition from the subthreshold to strong inversion. This unified charge density model considering charge layer thickness is express by (3.57),

$$Q_{ch0} = C_{ox,\text{eff}} \cdot V_{gst,\text{eff}} \tag{3.57}$$

where

$$C_{ox,\text{eff}} = \frac{C_{oxe} \cdot C_{cen}}{C_{oxe} + C_{cen}}, \quad C_{cen} = \frac{\varepsilon_{Si}}{X_{DC}} \tag{3.58}$$

$$X_{DC} = \frac{ADOS \times 1.9 \times 10^{-9}\,m}{1 + \left(\frac{V_{gst,\text{eff}} + 4(VTH0 - VFB - \Phi_s)}{2TOXP}\right)^{0.7 \times BDOS}} \tag{3.59}$$

$$V_{gst,eff} = \frac{nv_t \cdot \ell n\left\{1 + \exp\left[\dfrac{m^*\left(V_{gse} - V_{th}\right)}{nv_t}\right]\right\}}{m^* + nC_{oxe}\sqrt{\dfrac{2\Phi_s}{qNDEP\varepsilon_{Si}}}\exp\left[-\dfrac{(1-m^*)\left(V_{gse} - V_{th}\right) - Voff'}{nv_t}\right]} \tag{3.60}$$

Where

$V_{gst,eff}$: *the effective* $\left(V_{gse} - V_{th}\right)$

$$v_t = \frac{k_B T}{q} : \textit{ thermal voltage} \tag{3.61}$$

$$m^* = 0.5 + \frac{\tan^{-1}(MINV)}{\pi} \tag{3.62}$$

$$Voff' = Voff + \frac{VoffL}{L_{eff}} \tag{3.63}$$

where VoffL is used to fit the length dependence of Voff' in MOSFET with non-uniform channel doping profiles.

Then, a unified expression of local charge density distribution function along the direction of channel length (y) is given by (3.64),

$$Q_{ch}(y) = C_{ox,eff} \cdot V_{gst,eff}\left(1 - \frac{V_F(y)}{V_b}\right) \tag{3.64}$$

$$V_b = \frac{V_{gsteff} + 2v_t}{A_{bulk}} \tag{3.65}$$

Taking the proposed $Q_{ch}(y)$, the drain current can be calculated using the integration along the channel from source($y = 0$) to drain($y = L$)and given by (3.66).

$$I_{ds} = I_0\left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off}'}{nv_t}\right) \tag{3.66}$$

$$I_0 = \mu\frac{W}{L}\sqrt{\frac{q\varepsilon_{Si}NDEP}{2\Phi_s}}v_t^2 \tag{3.67}$$

n is the subthreshold swing parameter as a function of capcitances associated with gate oxide C_{oxe}, body depletion width C_{dep}, and interface states C_{IT} ,and channel length L_{eff} / ℓ_t , given by (3.67) and (3.69).

$$n = 1 + NFACTOR \cdot \frac{C_{dep}}{C_{oxe}} + \frac{Cdsc\_Term + CIT}{C_{oxe}} \qquad (3.68)$$

$$Cdsc\_Term = (CDSC + CDSD \cdot V_{ds} + CDSCB \cdot V_{bseff}) \cdot \frac{0.5}{\cosh\left(DVT1\dfrac{L_{eff}}{\ell_t}\right) - 1} \qquad (3.69)$$

Where $Cdsc\_Term$ represents the coupling capacitance between source and drain along the channel. CIT is the capacitance due to interface states. Note that the subthreshold the subthreshold swing determined by n shares the same exponential dependence on channel length as DIBL effect.

In general, the simulation using default model parameters cannot fit the measured I-V characteristics in nanoscale MOSFET, particularly with DBB for our objective in this thesis. Due to the fact, I-V model parameters extraction and optimization is indispensable. First, V_T extraction in both linear and saturation regions is the fundamental work to carry out V_T model calibration. Linear V_T ($V_{T,lin}$) can be extracted from I_{ds}-V_{gs} in linear region ($|V_{ds}|$=0.1V or 0.05V), using maximum g_m ($g_{m,max}$) or constant current (CC) methods. After the extraction of $V_{T,lin}$, the saturation V_T ($V_{T,sat}$) can be determined from I_{ds}-V_{gs} in saturation region ($|V_{ds}|$=V_{dd} =1.0V for UN65), using CC method, according to the same current level corresponding to $V_{T,lin}$. A comprehensive calibration on V_T model requires multiple devices with a wide splits of channel lengths and widths. However, the splits of device dimensions cannot available from our test chip due to limited chip area. The compromised approach is taken to focus the optimized fitting for the multi-finger MOSFET with typical length, i.e. L=60 nm on layout, fixed finger wdith, W_F=2μm, and different finger numbers (N=16 and 32). As mentioned in the beginning, DBB effect is the major topic of our interest and V_T model parameters modification to fit measured V_T under ZBB, FBB, and RBB becomes the first step for I-V model calibration. Following the accurate extraction and simulation of linear and saturation V_T under DBB, the second step is mobility model parameters extraction and calibration based on I_{ds}-V_{gs} in linear region. UD responsible for coulomb scattering at very low field (E_{eff}) is the first parameter to be

extracted. After that, UA and UB contributing to surface roughness scattering at high field can be extracted through a fitting to I_{ds}-V_{gs} in linear region, under higher V_{gs}. Subsequently, UC responsible for V_{bs} effect can be extracted from I_{ds}-V_{gs} under DBB (i.e., ZBB, FBB, and RBB). Note that the mobility model parameters extraction and optimization can be carried out through the best fitting to g_m-V_{gs} in linear region, i.e. the first derivative of I_{ds} w.r.t. V_{gs}, given by $g_m = \partial I_{ds}/\partial V_{gs}$. The third step is DIBL effect related model parameters extraction from I_{ds}-V_{gs} at high V_{ds}, i.e. saturation region. The accuracy of extracted DIBL effect parameters can be verified by the V_T shift from $V_{T,lin}$ to $V_{T,sat}$. Also, DIBL reveals its influence on output resistance R_{out} from I_{ds}-V_{ds} under various V_{gs}. Besides DIBL effect, accurate simulation of I_{ds}-V_{ds} and R_{out} have to take into account of channel length modulation (CLM) effect and substrate current induced body effect (SCIBE). Finally, subthreshold I-V model parameters extraction and calibration is performed and verified by I_{ds}-V_{gs} in semi-log scale, i.e. $\ell og I_{ds} - V_{gs}$. Details of the subthreshold I-V model parameters can be referred to (3.66) ~(3.69).

The mentioned I-V model parameter extraction flow was performed on UN65 multi-finger MOSFET with L=60nm, W_F=2 m, and N=32, namely W2N32.

Table 3.8 presents the extracted model parameters associated with V_T, mobility, and subthreshold current models, under ZBB, FBB (V_{bs}=0.6V), and RBB(V_{bs}=-0.6V), and the comparison with default ones provided by UMC for logic devices. Note that a single set of model parameters for various body biases, such as ZBB, FBB, and RBB is not available from current models in BSIM-4.

Table 3.8 (a)V_T and mobility models parameters extracted from UN65 MOSFET W2N32 under ZBB ((V_{bs}=0), FBB ((V_{bs}=0.6V), and RBB ((V_{bs}=-0.6V) (b) V_T extraction result

(a)

parameter	Default	ZBB (V_{bs}=0V)	FBB (V_{bs}=0.6V)	RBB (V_{bs}=-0.6V)
Vth0	88.1m	88.1m	88.1m	88.1m
K2	36.6m	36.6m	86.6m	36.6m
K1	113m	105m	105m	112m
U0	20.62m	28.42m	30.02m	25.82m
UA	1.29n	1.89n	1.49n	1.59n
UB	2.043a	2.343a	2.843a	2.343a
UC	71.11p	71.11p	71.11p	71.11p
UD	0	8.9125E17	1.035E18	8.9125E17
Voff	-31.9m	-31.9m	-31.9m	-31.9m
VoffL	-4.04n	-4.04n	-4.04n	-4.04n
NFACTOR	1233.9m	1233.9m	1233.9m	1233.9m
CDSC	453.4u	453.4u	453.4u	453.4u
CDSD	0.6m	0.6m	0.6m	0.6m
CDSCB	139.8u	139.8u	139.8u	139.8u

(b)

after calibration	Vt,lin(ZBB)	Vt,sat(ZBB)	Vt,lin(FBB)	Vt,sat(FBB)	Vt,lin(RBB)	Vt,sat(RBB)
Measure	0.3194	0.1413	0.2289	0.08575	0.3561	0.1585
Simulation	0.3143	0.1549	0.2369	0.0722	0.03422	0.17242

In the following, I-V simulation was performed using BSIM-4 with the modified model parameters shown in **Table 3.8**.

Fig. 3.70(a),(b), and (c) present the comparison of simulated and measured I_{ds}-V_{gs} at V_{ds}=0.05V and 1.2V, under ZBB ((V_{bs}=0), FBB ((V_{bs}=0.6V), and RBB ((V_{bs}=-0.6V), respectively. **Fig. 3.71** (a),(b), and (c) indicate simulated and measured g_m-V_{gs} in linear and saturation regions (V_{ds}=0.05V and 1.2V), and under DBB (ZBB, FBB, and RBB). Note that I_{ds}-V_{gs} characteristics indicates excellent match between simulation and measurement. However, g_m-V_{gs} achieved from the first derivative of I_{ds} vs. V_{gs} reveals somewhat deviation from measurement, at very high V_{gs}, particularly large for RBB condition. The results suggest further modification on mobility model parameters under RBB. **Fig. 3.72** (a)~(c) demonstrates I_{ds}-V_{gs} in semi-log scale, i.e. $\ell og I_{ds} - V_{gs}$ from measurement and simulation for a comparison. The results indicate a good fitting in terms of gate swing and V_T shift from $V_{T,lin}$ to $V_{T,sat}$. Finally, the output characteristics, such as I_{ds}-V_{ds} from BSIM-4 simulation and measurement were shown in **Fig. 3.73**. Good match is demonstrated under various V_{gs} and specified body biases, i.e. ZBB (V_{bs}=0), FBB (V_{bs}=0.6V), and RBB (V_{bs}=-0.6V). The promsingly good fitting to the measured I-V and g_m characteristics suggests that I-V model calibration can improve the simulation accuracy for 4-port multi-finger MOSFETs under DBB.
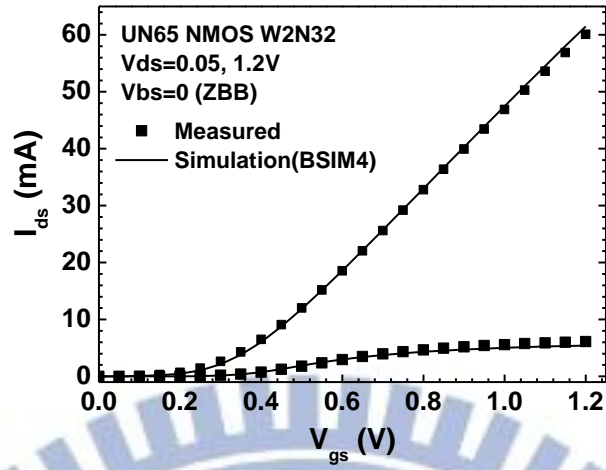
(a)
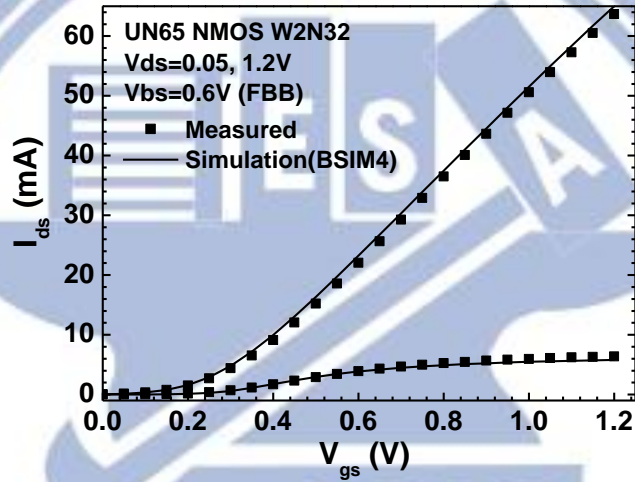
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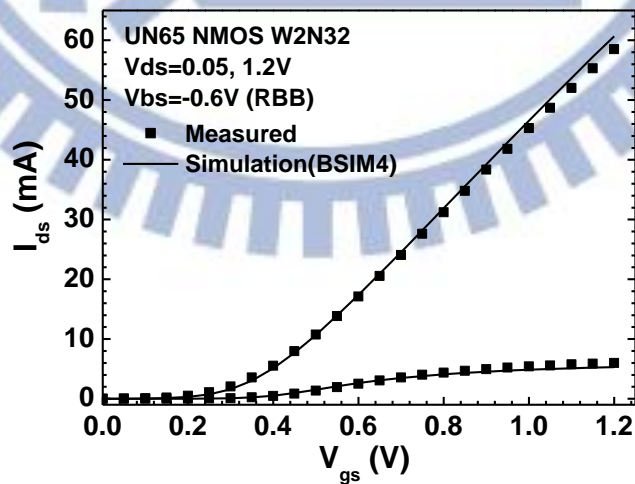
(c)

Fig. 3.70 UN65 NMOS W2N32, measured and simulated I_{ds}-V_{gs} at V_{ds}=0.05V and 1.2V

(a)ZBB : V_{bs}=0V (b) FBB : V_{bs}=0.6V (c) RBB : V_{bs}=-0.6V
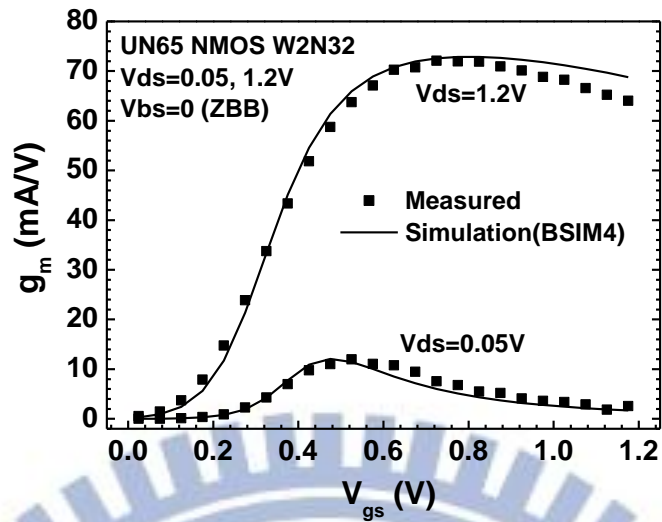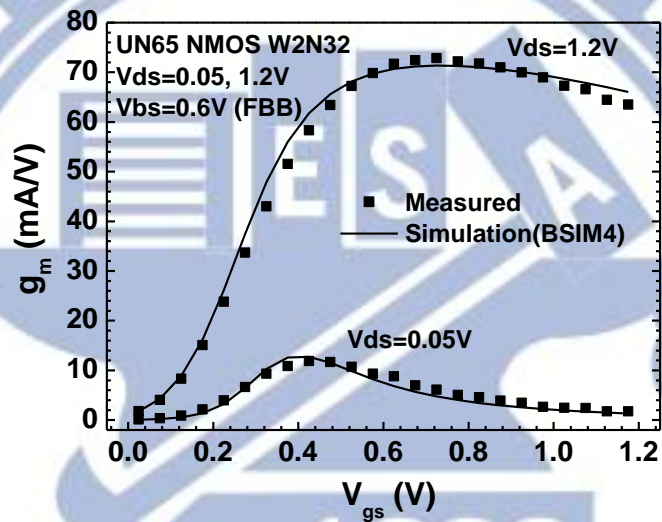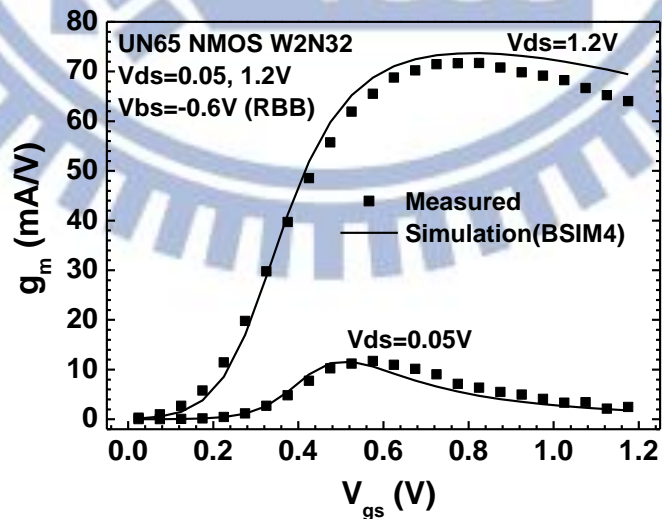
Fig. 3.71 UN65 NMOS W2N32, measured and simulated g_m-V_{gs} at Vd=0.05V and 1.2V

(a)ZBB : V_{bs}=0V (b) FBB : V_{bs}=0.6V (c) RBB : V_{bs}=-0.6V.
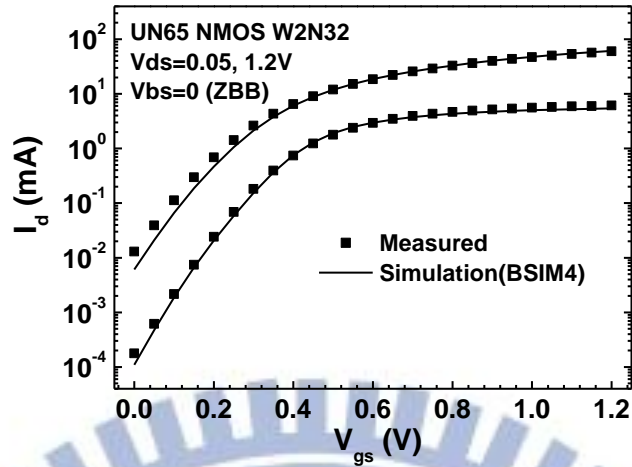
(a)
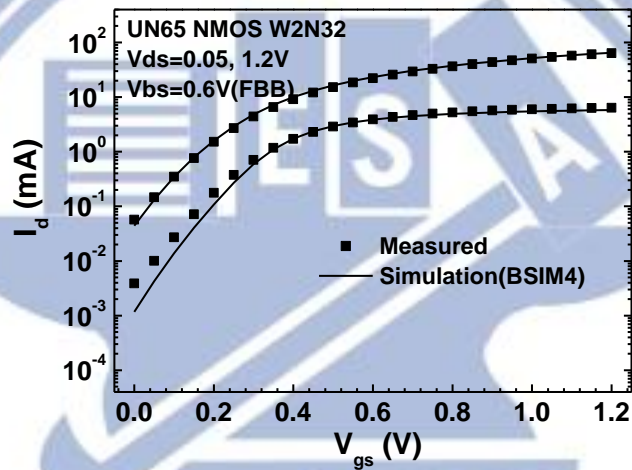
(b)
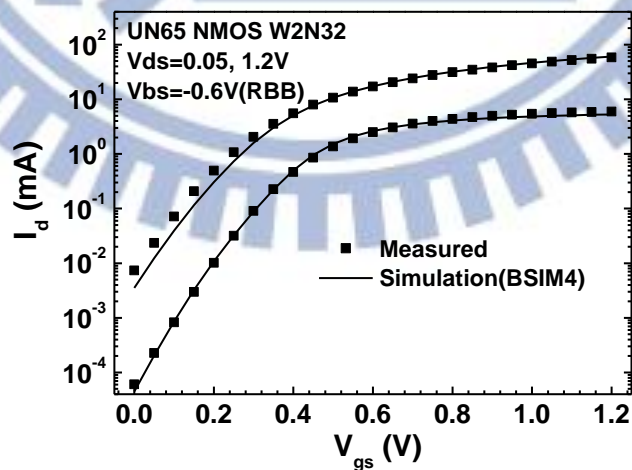
(c)

Fig. 3.72 UN65 NMOS W2N32, measured and simulated $\log(I_{ds})$-V_{gs} at V_{ds}=0.05V and 1.2V

(a)ZBB : V_{bs}=0V (b) FBB : V_{bs}=0.6V (c) RBB : V_{bs}=-0.6V.
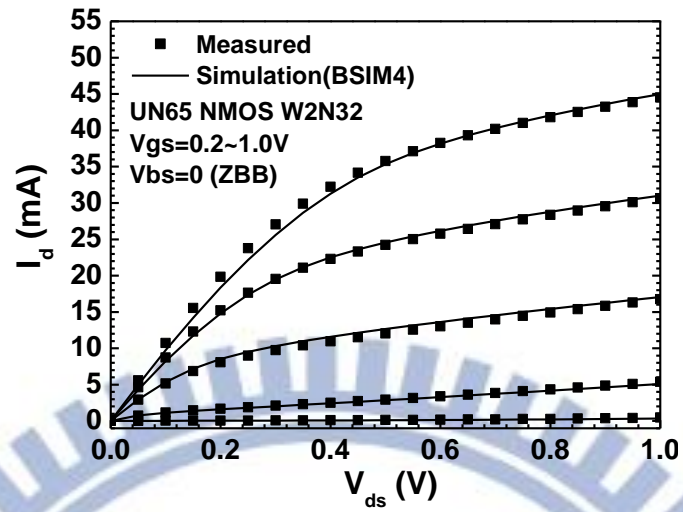
(a)
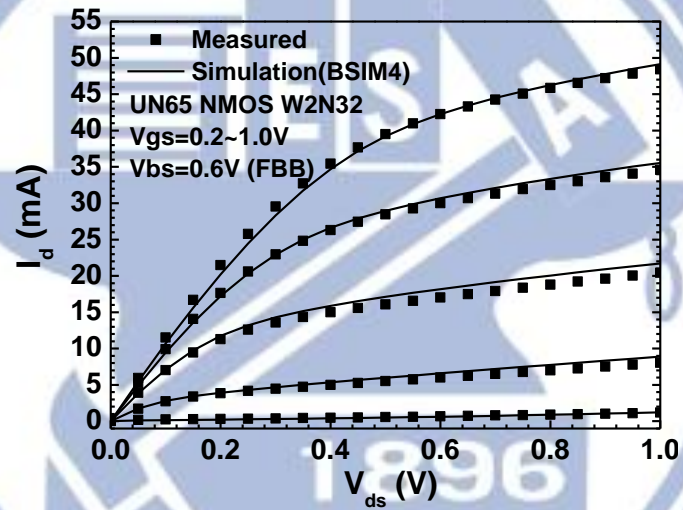
(b)
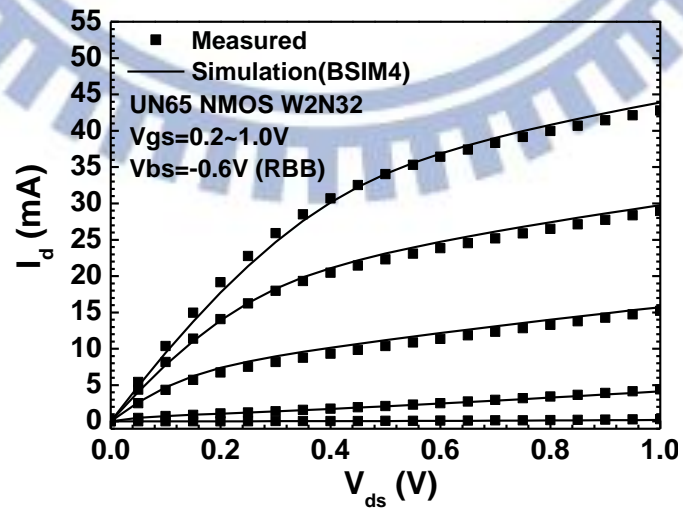
(c)

Fig. 3.73 UN65 NMOS W2N32, measured and simulated I_{ds}-V_{ds} under V_{gs}=0.2~1V, V_{gs}=

0.2V (a)ZBB : V_{bs}=0V (b) FBB : V_{bs}=0.6V (c) RBB : V_{bs}=-0.6V

3.4.2 BSIM-4 C-V Model Calibration and Simulation for 65nm 4-port RF MOSFET with DBB - (UN65 L65003)

As mentioned previously, C-V model in BSIM-4 includes gate capacitance model and junction diode capacitance model [17]. The former one incorporates coupling capacitances originated from the gate electrode of MOSFETs and the latter one is contributed from S/D to body junction depletion or diffusion capacitances. For logic circuits, the gate delay of a CMOS inverter is determined by both categories of capacitance, i.e. gate capacitances and junction capacitances. As for RF and analog circuits, the cut-off frequency f_T serving as the fundamental limitation of operation frequency is determined by gate capacitance, rather than junction capacitance [25]. In this thesis focusing on RF MOSFETs design and modeling, gate capacitance model is the key to determine the simulation accuracy for RF circuits design.

In our recent work, an extensive research effort has been focusing on the analysis of parasitic gate capacitances in nanoscale multi-finger MOSFETs [26, 27]. A comprehensive analysis method has been established for parasitic gate capacitances extraction and modeling, and for accurate simulation of f_T and RF circuit performance [26, 27]. The important insight and conclusion achieved from our work can be summarized as two key points. The first one is that the parasitic capacitances can be classified as extrinsic parasitic and intrinsic parasitic capacitance. The former is contributed from pads, interconnection lines, and lossy substrate, and can be extracted and removed using improved open deembedding method, i.e. openM1 deembedding [27]. The latter consists of gate related fringing capacitances, such as gate sidewall fringing capacitance (C_{of}) and finger end fringing capacitance ($C_{f(poly-end)}$) and cannot be removed using all of the existing open deembedding methods [27]. The second key point is that both extrinsic and intrinsic parasitic capacitances are not scalable with devices scaling and the impact on f_T and other high frequency performance increases dramatically in nanoscale

devices[26, 27].

In BSIM-4, the gate capacitance model is composed of three components, namely intrinsic, overlap, and fringing capacitances. This gate capacitance is originated from the version of BSIM-3.3.2 with some minor revisions and three options are available for BSIM-4, which can be matched with the options from BSIM-3.3.2, shown in **Table 3.9**.

Table 3.9 BSIM-4 capacitance model pptions and matching with BSIM-3.3.2 options

BSIM-4 capacitance model		Matched options in BSIM-3.3.2	
Options	Features	Intrinsic capMod	Overlap/fringing capMod
capMod=0	Simple and piece-wise model	0	0
capMod=1	Single-equation model	2	2
capMod=2	Default of BSIM-4 Single-equation and charge-thickness model	3	2

Before going through the details of three capacitance components, the geometrical parameters of MOSFETs have to be defined to appropriately separate the three components and then simulate each component of capacitance with sufficient accuracy. The geometric parameters include drawn dimensions (length and width) on layout and intrinsic channel dimensions for I-V and C-V modeling. The intrinsic dimensions are denoted as effective channel length and effective channel width. Ideally, a single set of effective channel length and channel width can fit both I-V and C-V models for the same device. However, in practice, different sets of parameters are generally required for I-V and C-V models to achieve respective fitting to the measured I-V and C-V characteristics.

For I-V model, the effective channel length L_{eff} and effective channel widths, denoted as W_{eff} or W_{eff} ' are defined as :

$$L_{eff} = L_{drawn} + XL - 2dL \tag{3.70}$$

$$dL = LINT + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{LWN}} \tag{3.71}$$

$$W_{eff} = W_{drawn} + XW - 2dW \tag{3.72}$$

$$dW = dW' + DWG \cdot V_{gsteff} + DWB\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right) \tag{3.73}$$

or

$$W_{eff}' = W_{drawn} + XW - 2dW' \qquad (3.74)$$

$$dW' = WINT + \frac{WW}{W^{WWN}} + \frac{WL}{L^{WWN}} + \frac{WWL}{L^{WLN}W^{LWN}} \qquad (3.75)$$

where XL and XW represent the offset of gate length and channel width from the drawn dimensions after lithography and etching process. dL represent channel length variation due to S/D lateral diffusion under the gate and dW' is the channel width variation, maybe from bird's beak encroachment for LOCOS or divot and trench top corner rounding for STI. LINT and WINT represent the components of dL and dW', respectively, which are extracted from conventional I-V method **[28]**. Note that dW associated with W_{eff} incorporates gate and body biases dependence with fitting parameters DWG and DWB, respectively.

As for C-V model, the effective channel length and effective channel width, denoted as L_{active} and W_{active} are defined as :

$$L_{active} = L_{drawn} + XL - 2dL \qquad (3.76)$$

$$dL = DLC + \frac{LLC}{L^{LLN}} + \frac{LWC}{W^{LWN}} + \frac{LWL}{L^{LLN}W^{N}} \qquad (3.77)$$

$$W_{active} = \frac{W_{drawn}}{NF} + XW - 2dW \qquad (3.78)$$

$$dW = DWC + \frac{WLC}{L^{WLN}} + \frac{WWC}{W^{WWN}} + \frac{WWLC}{L^{WLN}W^{WWN}} \qquad (3.79)$$

where DLC and DWC are different from LINT and WINT in I-V model and can be bias-dependent variables. It means that L_{eff} and W_{eff} used in I-V model can be different from L_{active} and W_{active} used in C-V model for the same device with specified dimensions. Theoretically, L_{eff} and L_{active} represent the effective channel lengths defined by the metallurgical junctions of S/D lateral diffusion to body. However, the graded S/D junction profile generated by lightly doped S/D (LDD) or S/D extension (SDE) regions makes the effective channel length a strongly bias-dependent parameter and introduces a dramatic difficult to the determination of

L_{eff} and L_{active} from electrical measurement, either I-V or C-V methods. In our previous work, a decoupled C-V method was developed for an accurate extraction of effective channel length and source-and-drain series resistance, simultaneously [29]. The extracted source-and-drain series resistance associated with LDD or DD profiles reveals a strong bias dependence [29].

In BSIM-4, L_{active} is measured and extracted under flatband voltage built at the gate to S/D interface. Additional parameters such as LLC, LWC, LWLC for dL and WLC, WWC, WWLC for dW are introduced as fitting parameters to allow an optimized fitting to devices with various dimensions. Ideally, L_{active} and W_{active} can precisely define the intrinsic channel region contributing intrinsic gate capacitance. Furthermore, **dL** defines the length of S/D lateral diffusion to gate overlap region, which contributes the **overalp capacitance**. Regarding the fringing capacitance, it is a kind of intrinsic parasitic capacitance and cannot be scalable with the channel length scaling. The key parameters governing the fringing capacitance is the gate thickness, gate oxide thickness, and gate to contact spacing, etc [30]. The smaller gate to contact space and the thinner gate oxide will lead to larger fringing capacitance. As for multi-finger MOSFETs widely used in RF circuits, the narrower channel width and simultaneous increase of finger number will increase finger-end fringing capacitance [27]. **Table 3.10** lists the geometrical parameters extracted from UN65 multi-finger MOSFETs for I-V and C-V simulation, respectively. Note that both L_{active} and L_{eff} are shorter than L_{drawn} due to significant CD loss from patterning and etching, i.e. XL (-20nm). Furthermore L_{active} for C-V simulation is smaller than half that of L_{eff} for I-V simulation, due to significantly larger **dL** from DLC >> LINT. The ratio of L_{active} and dL can be used to predict the weighting factor of the intrinsic (channel) capacitance and overlap capacitance in the total gate capacitance. Note that **dL** is not scalable with length scaling and the overlap capacitance will dominate higher ratio with device scaling.

Table 3.10 Geometrical parameters extracted from UN65 multi-finger MOSFET for I-V and C-V simulation

Geometrical parameters for I-V simulation												
W_F (m)	N_F	W_{drawn} (m)	L_{drawn}(m)	XL (m)	LINT (m)	LL	LW	LWL	LLN	LWN	dL (m)	L_{eff} (m)
2.0E-06	32	6.40E-05	6.0E-08	-2.00E-08	-4.0E-09	3.725E-16	-5.00E-16	1.577E-23	1	1	2.205E-09	3.559E-08

Geometrical parameters for C-V simulation												
W_F (m)	N_F	W_{drawn} (m)	L_{drawn}(m)	XL (m)	DLC (m)	LLC	LWC	LWLC	LLN	LWN	dL (m)	L_{active} (m)
2.0E-06	32	6.40E-05	6.0E-08	-2.00E-08	1.237E-08	-5.00E-17	-1.14E-15	-5.00E-23	1	1	1.151E-08	1.699E-08

Besides the effective channel length and effective channel width, gate oxide thickness is one more fundamental parameter for accurate C-V simulation. In BSIM-4, there are three kinds of gate oxide thickness, such as physical gate oxide thickness (TOXP), electrical gate oxide thickness (TOXE), and nominal gate oxide thickness (TOXM). TOXP is the physical thickness of the gate oxide formed on the Si substrate, which is free from poly gate depletion and inversion layer quantization effects. TOXE is the electrical equivalent thickness of the gate oxide at active state, i.e. strong inversion in which additional thicknesses are contributed from the quantum well of inversion layer (W_{inv}) and poly gate depletion (X_{poly}). Note that both W_{inv} and X_{poly} are not scalable with TOXP reduction and their influence increases with device scaling with thinner TOXP. The gate capacitance under strong inversion, represented by k_{ox} $_0$/TOXE is used to calculate the inversion carrier density, which contributes to drain current. TOXM is the gate oxide thickness at which the parameter is extracted as a nominal value and is used in V_T model to allow k1ox and k2ox be tunable with TOXM.

Considering quantum well thickness effect associated with the inversion layer, charge thickness model (CTM) was proposed and implemented as follows to calculate effective oxide capacitance C_{oxeff} from which the inversion carriers and gate charge density can be accurately calculated to simulate the intrinsic channel (gate) capacitance.

According to series capacitance principle, C_{oxeff} is given by

$$C_{oxeff} = \frac{C_{oxp} \cdot C_{cen}}{C_{oxp} + C_{cen}}$$
(3.80)

$$C_{cen} = \frac{\varepsilon_{si}}{X_{DC}}$$
(3.81)

where the inversion charge layer thickness XDC can be formulated as

$$X_{DC} = \frac{ADOS \times 1.9 \times 10^{-9} m}{1 + \left(\dfrac{V_{gst,eff} + 4(VTH0 - VFB - \Phi_s)}{2TOXP} \right)^{0.7 \times BDOS}}$$ (3.82)

Vgst,eff is the effective gate over-drive to realized a unified formula for calculating inversion charge density from weak inversion (subthreshold) region to strong inversion region, as given by (3.80)~(3.82). Note that poly gate depletion effect has been incorporated by the term with NDEP for poly gate doping concentration.

$$V_{gsteff} = \frac{nv_t \cdot \ell n \left\{ 1 + \exp \left[\dfrac{m^*(V_{gse} - V_{th})}{nv_t} \right] \right\}}{m^* + nC_{oxe} \sqrt{\dfrac{2\Phi_s}{qNDEP\varepsilon_{Si}}} \exp \left[-\dfrac{(1 - m^*)(V_{gse} - V_{th}) - Voff'}{nv_t} \right]}$$ (3.83)

$$Voff' = Voff + \frac{VoffL}{L_{eff}}$$ (3.84)

$$V_{gse} = VFB + \Phi_s + q\varepsilon_{Si}NGATE \left(\frac{TOXE}{\varepsilon_{ox}} \right)^2 \left(\sqrt{1 + \frac{2(V_{gs} - VFB - \Phi_s)}{q\varepsilon_{Si}NGATE} \left(\frac{\varepsilon_{ox}}{TOXE} \right)^2} - 1 \right)$$ (3.85)

Then, the inversion charge density can be calculated by

$$q_{inv} = -C_{oxeff} \cdot (V_{gsteff,CV} - \varphi_\delta)_{eff}$$ (3.86)

where φ_δ is employed to simulate body charge thickness by including the deviation of surface potential Φ_S from $2\Phi_B$, i.e. the threshold value for strong inversion

$$\varphi_\delta = \Phi_S - 2\Phi_B$$ (3.87)

$$\Phi_S - 2\Phi_B = v_t \cdot \ell n \left(1 + \frac{V_{gsteff,CV}(V_{gsteff,CV} + 2k_{1ox}\sqrt{2\Phi_B})}{MOIN \cdot k_{1ox}^2 v_t} \right)$$ (3.88)

note that $V_{gsteff,CV}$ is the effective gate-overdrive created for C-V simulation, with major difference from V_{gsteff} in the terms m^* and $Voff'$, given by

$$V_{gsteff,CV} = \frac{nv_t \cdot \ell n \left\{ 1 + \exp \left[\dfrac{m^*(V_{gse} - V_{th})}{nv_t} \right] \right\}}{m^* + nC_{oxe} \sqrt{\dfrac{2\Phi_s}{qNDEP\varepsilon_{Si}}} \exp \left[-\dfrac{(1 - m^*)(V_{gse} - V_{th}) - Voff'}{nv_t} \right]}$$ (3.89)

$$m^* = 0.5 + \frac{\tan^{-1}(MINVCV)}{\pi} \tag{3.90}$$

$$Voff' = VOFFCV + \frac{VOFFCVL}{L_{eff}} \tag{3.91}$$

To ensure charge conservation, terminal charges instead of terminal voltages are used as the state variables. The terminal charges associated with gate, body, source, and drain are formulated as follows. The gate charge Q_g is composed of the mirror charges from the channel charge , accumulation charge Q_{acc}, and body depletion charge Q_{sub}.

$$Q_g = -(Q_b + Q_s + Q_d) \tag{3.92}$$

$$Q_b = Q_{acc} + Q_{sub} \tag{3.93}$$

$$Q_{inv} = Q_s + Q_d \tag{3.94}$$

The total charge is calculated by integrating the charge along the channel as follows. The threshold voltage along the channel is modified due to non-uniform body charge given by (3.95)

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y \tag{3.95}$$

$$Q_c = Q_s + Q_d = W_{active} \int_0^{L_{active}} q_c(y)dy = -W_{active}C_{oxe} \int_0^{L_{active}} (V_{gt} - A_{bulk}V_y)dy \tag{3.96}$$

$$Q_g = W_{active} \int_0^{L_{active}} q_g(y)dy = W_{active}C_{oxe} \int_0^{L_{active}} (V_{gt} + V_{th} - V_{FB} - \Phi_s - V_y)dy \tag{3.97}$$

$$Q_b = W_{active} \int_0^{L_{active}} q_b(y)dy = W_{active}C_{oxe} \int_0^{L_{active}} (V_{th} - V_{FB} - \Phi_s + (A_{bulk} - 1)V_y)dy \tag{3.98}$$

For MOSFETs operating in saturation region, the inversion charges Q_{inv} are partitioned into Q_s and Q_d according to the partitioning ratios *XPART*, such as *XPART*=1, 0.5, and 0 for Q_d / Q_s =0/100, 50/50, and 40/60.

For capMod=2, i.e. the default capacitance model with single equation and charge thickness model (CTM), the inversion channel charges are partitioned as follows

XPART=0.5 (50/50)

$$Q_s = Q_d =$$

$$\frac{-W_{active}L_{active}C_{oxeff}}{2} \cdot \left[(V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{A_{bulk}'V_{cveff,CV}}{2} + \frac{A_{bulk}'^2 V_{cveff,CV}^2}{12 \cdot \left((V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{A_{bulk}'V_{cveff,CV}}{2} \right)} \right]$$

(3.99)

XPART=0 (40/60)

$$Q_s = \frac{-W_{active}L_{active}C_{oxeff}}{2\left((V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{A_{bulk}'V_{cveff,CV}}{2} \right)^2} \cdot \left[\begin{array}{l} (V_{gsteff,CV} - \varphi_\delta)^3 - \frac{4}{3}(V_{gsteff,CV} - \varphi_\delta)^3 (A_{bulk}'V_{cveff,CV}) \\ + \frac{2}{3}(V_{gsteff,CV} - \varphi_\delta)(A_{bulk}'V_{cveff,CV})^2 - \frac{2}{15}(A_{bulk}'V_{cveff,CV})^3 \end{array} \right]$$

(3.100)

$$Q_d = \frac{-W_{active}L_{active}C_{oxeff}}{2\left((V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{A_{bulk}'V_{cveff,CV}}{2} \right)^2} \cdot \left[\begin{array}{l} (V_{gsteff,CV} - \varphi_\delta)^3 - \frac{5}{3}(V_{gsteff,CV} - \varphi_\delta)^3 (A_{bulk}'V_{cveff,CV}) \\ + (V_{gsteff,CV} - \varphi_\delta)(A_{bulk}'V_{cveff,CV})^2 - \frac{1}{5}(A_{bulk}'V_{cveff,CV})^3 \end{array} \right]$$

(3.101)

XPART=1 (0/100)

$$Q_s = \frac{-W_{active}L_{active}C_{oxeff}}{2} \cdot \left[(V_{gsteff,CV} - \varphi_\delta)_{eff} + \frac{1}{2} A_{bulk}'V_{cveff,CV} - \frac{A_{bulk}'^2 V_{cveff,CV}^2}{12 \cdot \left((V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{A_{bulk}'V_{cveff,CV}}{2} \right)} \right]$$

(3.102)

$$Q_d = \frac{-W_{active}L_{active}C_{oxeff}}{2} \cdot \left[(V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{3}{2} A_{bulk}'V_{cveff,CV} - \frac{A_{bulk}'^2 V_{cveff,CV}^2}{4 \cdot \left((V_{gsteff,CV} - \varphi_\delta)_{eff} - \frac{A_{bulk}'V_{cveff,CV}}{2} \right)} \right]$$

(3.103)

As mentioned previously, the intrinsic capacitance is represented by the effective channel length, L_{active}, which is much shorter than the gate length after patterning and etching, i.e. L_{drawn}-XL, and the remaining portion is defined as overlap region, which contributes so called overlap capacitances. Due to the fact that the overlap region is not scalable with the gate length scaling, the overlap capacitance dominates an increasing rate of the total gate capacitance with

device scaling and becomes a key factor governing the gate delay and cut-off frequency for high speed and high frequency design. Accurate overlap capacitance model is essential for accurate simulation of AC and RF performance. However, the critical sensitivity of the overlap region to the S/D lateral diffusion profile from LDD or SDE (S/D extension) and spacer variation complicates the bias dependence and makes the overlap capacitance modelling a challenging work. In BSIM-4, the overlap capacitance model was implemented with a single equation for both accumulation and depletion condition by using smoothing parameters, such as $V_{gs,overlap}$ and $V_{gd,overlap}$ for source and drain sides. Note that the intrinsic capacitances under active mode are non-reciprocal, i.e. $C_{gs} \neq C_{sg}$ and $C_{gd} \neq C_{dg}$ but the overlap capacitances are considered reciprocal, i.e. $C_{gs,overlap} = C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$. The overlap capacitance model implemented for capMod2 is described as follows.

Source side overlap capacitance model with bias dependence is given by

$$\frac{Q_{overlap,s}}{W_{active}} = CGSO \cdot V_{gs} + CGSL \left[V_{gs} - V_{gs,overlap} - \frac{CKAPPAS}{2} \left(-1 + \sqrt{1 - \frac{4V_{gs,overlap}}{CKAPPAS}} \right) \right]$$

(3.104)

$$V_{gs,overlap} = \frac{1}{2} \left(V_{gs} + \delta_1 - \sqrt{(V_{gs} + \delta_1)^2 + 4\delta_1} \right)$$

$$\delta_1 = 0.02V$$

(3.105)

$$C_{gs,overlap} = \frac{-1}{W_{active}} \frac{\partial Q_{overlap,s}}{\partial V_s}$$

(3.106)

Drain side overlap capacitance model with bias dependence is given by

$$\frac{Q_{overlap,d}}{W_{active}} = CGDO \cdot V_{gd} + CGSL \left[V_{gd} - V_{gd,overlap} - \frac{CKAPPAD}{2} \left(-1 + \sqrt{1 - \frac{4V_{gd,overlap}}{CKAPPAD}} \right) \right]$$

(3.107)

$$V_{gd,overlap} = \frac{1}{2} \left(V_{gd} + \delta_1 - \sqrt{(V_{gd} + \delta_1)^2 + 4\delta_1} \right)$$

$$\delta_1 = 0.02V$$

(3.108)

$$C_{gd,overlap} = \frac{-1}{W_{active}} \frac{\partial Q_{overlap,d}}{\partial V_d}$$

(3.109)

where CGSO and CGDO represent bias independent overlap capacitance from heavily doped S/D . GSL and CGDL are bias dependent overlap capacitance from LDD or SDE region. CKAPPAS and CKAPPAD are bias dependent fitting parameters associated with the terms GSL and GDL, respectively.

The gate overlap charge can be calculated according to charge conservation law given by

$$Q_{overlap,g} = -\left(Q_{overlap,d} + Q_{overlap,s} + (CGBO \cdot L_{active}) \cdot V_{gb}\right) \tag{3.110}$$

where CGBO is a model parameter, which represents the gate-to-body overlap capacitance per unit channel length.

Intrinsic channel capacitance and overlap capacitance constitute the intrinsic gate capacitance and another component of gate related capacitance, so called fringing capacitance is a kind of parasitic capacitance. Note that this kind of parasitic capacitance cannot be removed using existing deembedding and is defined as intrinsic parasitic capacitance to be distinguished from the conventionally known extrinsic parasitic capacitance from pads, interconnection lines, and substrate **[26]**. As mentioned previously, the gate related fringing capacitances are composed of two major components, such as gate sidewall fringing capacitance (C_{of}) and finger end fringing capacitance ($C_{f(poly-end)}$). In our recent work, an extensive study has been done based on 3-dimensional (3-D) interconnection simulation (Raphael) and devised deembedding method, C_{of} and $C_{f(poly-end)}$ can be precisely extracted for an accurate determination of intrinsic gate capacitance, inversion carriers density, effective mobility, and intrinsic cut-off frequency f_T **[26]**. Note that the gate sidewall fringing capacitance is so called outer fringing capacitance (C_{of}) and is independent of biases. On the other hand, inner fringing capacitance (C_{if}) is a component of intrinsic channel capacitance and reveals a strong bias dependence. The effect of C_{if} is significant in weak inversion region but becomes negligible in strong inversion region. In our previous work, a 3-D integral model has been developed to accurately simulate C_{of}, which are composed of gate-to-S/D diffusion ($C_{g,Diff}$) and gate-to-contact ($C_{g,CT}$) **[30].** This 3-D integral

model can precisely predict the dependence of device layout and geometry, such as gate length, gate oxide thickness, gate thickness, gate to contact space, and contact dimensions, etc **[27].**

In BSIM-4, the outer fringing capacitance model just follows a simple sidewall capacitance formula derived based on a conformal mapping method **[31]**, as given by

$$CF = \frac{2 \cdot EPSROX \cdot \varepsilon_0}{\pi} \cdot \ell og \left(1 + \frac{4.0e^{-7}}{TOXE} \right) \tag{3.111}$$

where CF represent the outer fringing capacitance per unit width. This simplified formula suggests the larger CF associated with thinner TOXE but cannot predict the dependence of layout and geometrical parameters.

In summary, the capacitances associated with MOSFETs are classified into 4 categories, such as extrinsic parasitic capacitance, fringing capacitances, overlap capacitance, and intrinsic capacitance, as shown in **Fig. 3.74**. The extrinsic parasitic capacitance is contributed from pads, interconnection lines, and substrate and can be removed by an open deembedding. Note that openM1 deembedding is essential to achieving a clean deembedding and approaching the intrinsic MOSFET. However, all of the DUTs with various dimensions require their dedicated openM1 deembedding structures and it leads to much larger chip area. In this thesis, due to limited chip area, openM3 deembedding is a compromised solution to cope with the limitation.
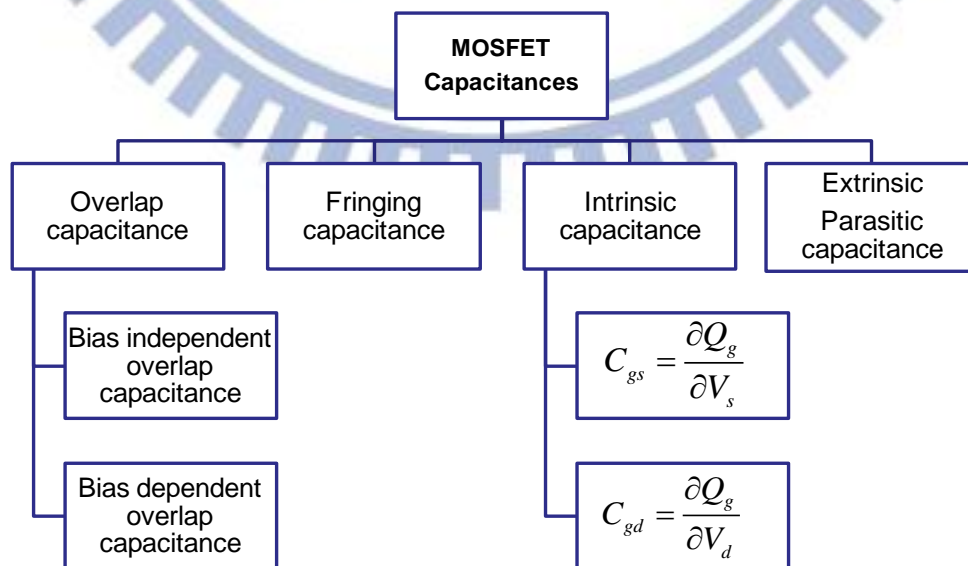
Fig. 3.74 MOSFET capacitances classified into four categories for C-V modeling : extrinsic

parasitic capacitance, fringing capacitance, overlap capacitance, and intrinsic capacitance

Fig. 3.75 illustrates the small signal equivalent circuit for a standard MOSFET after open deembedding. Note that the overlap and fringing capacitances are lumped together with intrinsic capacitance and cannot be removed or extracted by open deembedding. A feasible approach is to turn off the active channel under cold device condition, i.e. $V_g=V_d=V_s=V_b=0$, which is equivalent to turn off the intrinsic capacitance, and then to extract the overlap and fringing capacitances from the measured Y-parameters. According to the 4-port Y-parameters under cold device condition, 4 components of gate related capacitances can be extracted as follows :

$$C_{gg} = \frac{Im(Y_{11})}{\omega} \tag{3.112}$$

$$C_{gs} = -\frac{Im(Y_{12})}{\omega} \tag{3.113}$$

$$C_{gd} = -\frac{Im(Y_{13})}{\omega} \tag{3.114}$$

$$C_{gb} = -\frac{Im(Y_{14})}{\omega} \tag{3.115}$$

$$C_{\delta g} = C_{gg} - C_{gs} - C_{gd} - C_{gb} = \frac{Im(Y_{11})}{\omega} + \frac{Im(Y_{12})}{\omega} + \frac{Im(Y_{13})}{\omega} + \frac{Im(Y_{14})}{\omega} \tag{3.116}$$

$$C_{gd,ext} = C_{gd} - C_{gs} = -\frac{Im(Y_{13})}{\omega} + \frac{Im(Y_{12})}{\omega} \tag{3.117}$$

$$C_{gb} = C_{gb1} + C_{gb2} \tag{3.118}$$

For cold device under ideal condition, the 4 components of gate related capacitances of intrinsic MOSFETs should follow conservation law, i.e. $C_{gg}-(C_{gs}+C_{gd}+C_{gb})=0$ and symmetric S/D feature, i.e. $C_{gs}=C_{gd}$. However, the 4-port Y-parameters measured from practical device, even after open deembedding reveals an offset between C_{gg} and $C_{gs}+C_{gd}+C_{gb}$, as shown in **Fig. 3.76(a)** and represented by $C_{\delta g}$ given by (3.116), and also difference between C_{gs} and C_{gd} denoted as $C_{gd,ext}$ given by (48) and shown in **Fig. 3.76(b)**. Both $C_{\delta g}$ and $C_{gd,ext}$ are considered parasitic capacitances from inter-metal coupling, which cannot be removed by using openM3

deembedding. Regarding cold device at turn-off state, the channel is out of inversion carriers and the gate to body is free from shielding effect. As a result, gate to body capacitance, C_{gb} cannot be negligible. As shown in **Fig. 3.76(c)**, the measured C_{gb} versus frequency indicates a frequency independent component, C_{gb1} in higher frequency region, above 25GHz and a frequency dependent component, C_{gb2} in lower frequency region, below 25GHz. As shown in **Fig. 3.75**, the frequency independent term is implemented as C_{gb1}, contributed from inter-metal coupling between the gate and body contacts. The frequency dependent component is deployed by a parallel RC, i.e. $R_{gb}//C_{gb2}$. in which R_{gb} is one of body resistances.
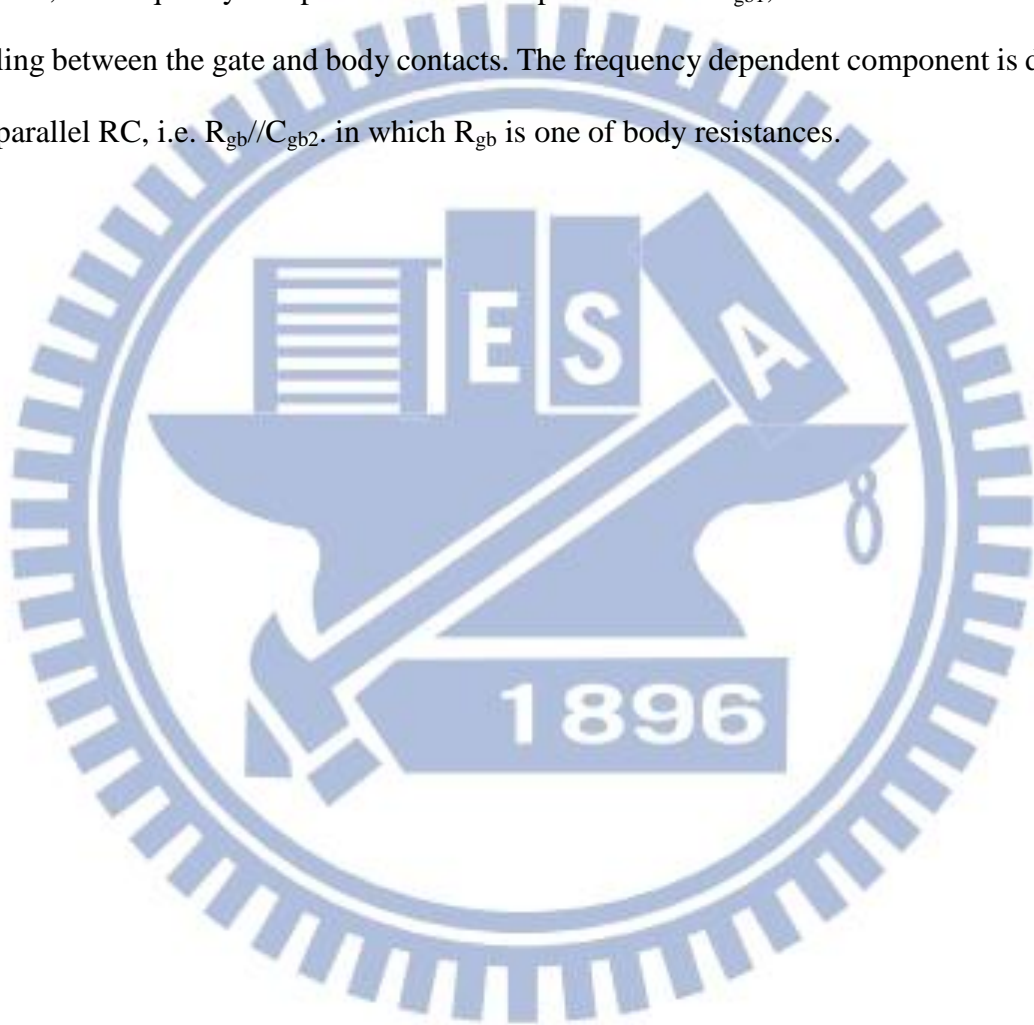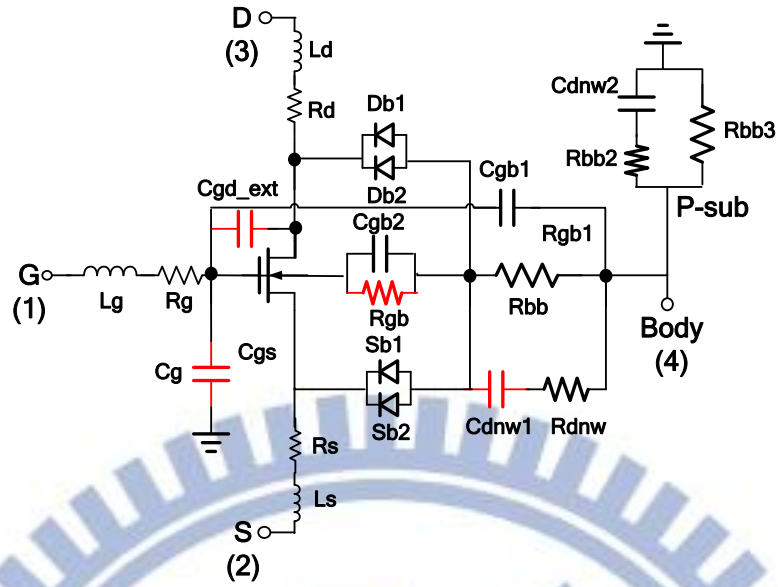
Fig. 3.75 Small signal equivalent circuit of a standard MOSFET after open deembedding
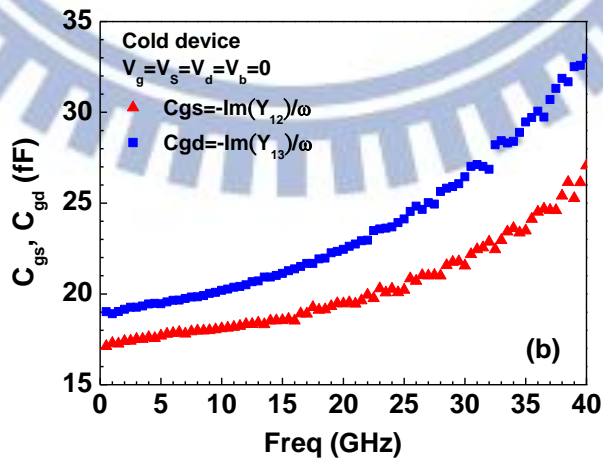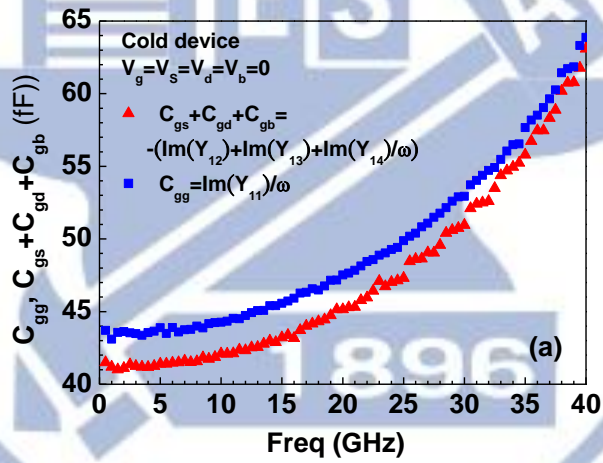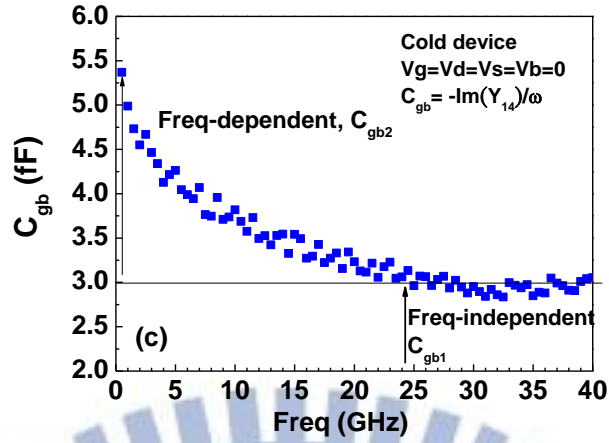
Fig. 3.76 The gate related capacitances extracted from 4-port Y-parameters after openM3 deembedding on 4-port RF MOSFET (a) C_{gg} and $C_{gs}+C_{gd}+C_{gb}$ (b) C_{gs} and C_{gd} (c) $C_{gb}=C_{gb1}+C_{gb2}$

For cold device under turn-off condition, C_{gs} and C_{gd} are contributed from overlap and fringing capacitances and the parameters associated with the overlap and fringing capacitances model can be extracted step by step, according to the flow as shown in **Fig. 3.78**. First, the fringing capacitance C_{of} can be determined from Raphael simulation based on our previous work and 65nm device layout/geometrical parameters **[30]**. The fringing capacitance model parameter, **CF** can be adjusted according to C_{of} from Raphael simulation, shown in **Fig. 3.77**. Then, bias-independent parameters in overlap capacitance model, such as CGSO and CGDO are extracted through an iteration flow to fit C_{gs} and C_{gd} of cold device. As for the intrinsic capacitance model parameters extraction, VOFFCV are NOFF identified as two key parameters governing the gate bias dependent from weak inversion to strong inversion. Finally, bias-dependent parameters in overlap capacitance model, such as CGSL, CGDL, CKAPPAS, and CKAPPAD can be extracted under saturation condition with higher V_{ds}. **Fig. 3.78** illustrates the capacitance model parameters extraction flow as described**. Table 3.11** summarizes the capacitance model parameters extracted from UN65 n-MOSFET (W2N32) with ZBB, FBB, and RBB, and also the default model for a comparison. **Fig. 3.79 (a)~(d)** show a comparison between measurement and simulation for C_{gg}, C_{gs}, C_{gd}, and C_{gb} under ZBB

114

(V_{bs}=0). The results reveals a large deviation from the meaurement by using default C-V model parameters and a good match with measurement when adopting the modified C-V mdoel parameters (**Fig. 3.79**). Similarly, the improved matching with measurement by simulation using the model parameters modified for FBB (V_{bs}=0.6V) and RBB (V_{bs}=0.6V) can be achieved, as shown in **Fig. 3.80** and **Fig. 3.81**.
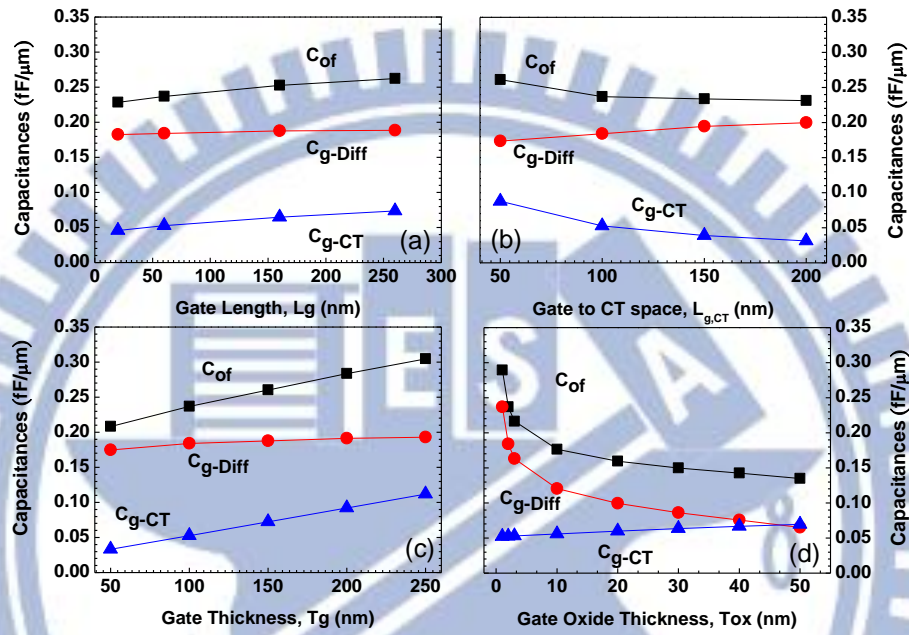
Fig. 3.77 Gate sidewall fringing capacitances, $C_{of}=C_{g,Diff}+C_{g,CT}$ simulated by Raphael for UN65 n-MOSFET (a) C_{of}, $C_{g,Diff}$, and $C_{g,CT}$ vs. L_g (b) C_{of}, $C_{g,Diff}$, and $C_{g,CT}$ vs. $L_{g,CT}$ (c) C_{of}, $C_{g,Diff}$, and $C_{g,CT}$ vs. T_g (d) C_{of}, $C_{g,Diff}$, and $C_{g,CT}$ vs. T_{ox}
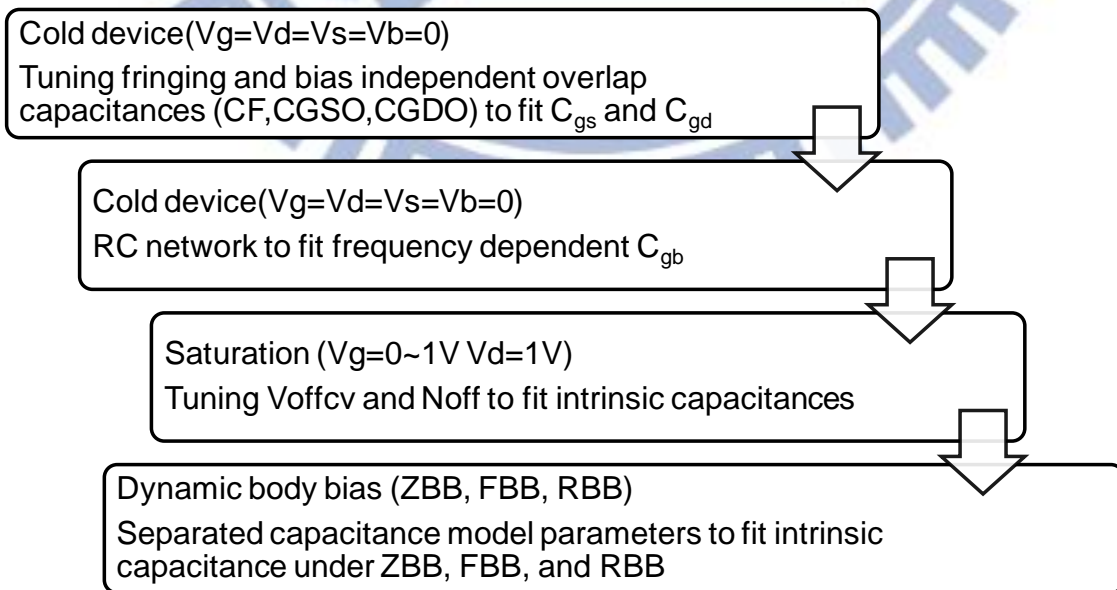
Fig. 3.78 MOSFET capacitance model parameters extraction flow

Table 3.11 C-V model parameters for UN65 n-MOSFET under ZBB, FBB, and RBB, and a comparison with default parameters

CV model parameter	default	ZBB	FBB	RBB
CGSO (F)	52p	36p	26.2p	42.4p
CGDO (F)	52p	54p	60.4p	62p
CGSL (F)	100p	100p	73.3p	96.7p
CGDL (F)	100p	100p	96.7p	91.3p
CKAPPAS	2.7	3.76	1.64	3.7
CKAPPAD	2.7	3.46	1.66	3.7
Noff	2.828	4.428	4.118	4.028
Voffcv	38.84m	172.34m	158.84m	166.84m
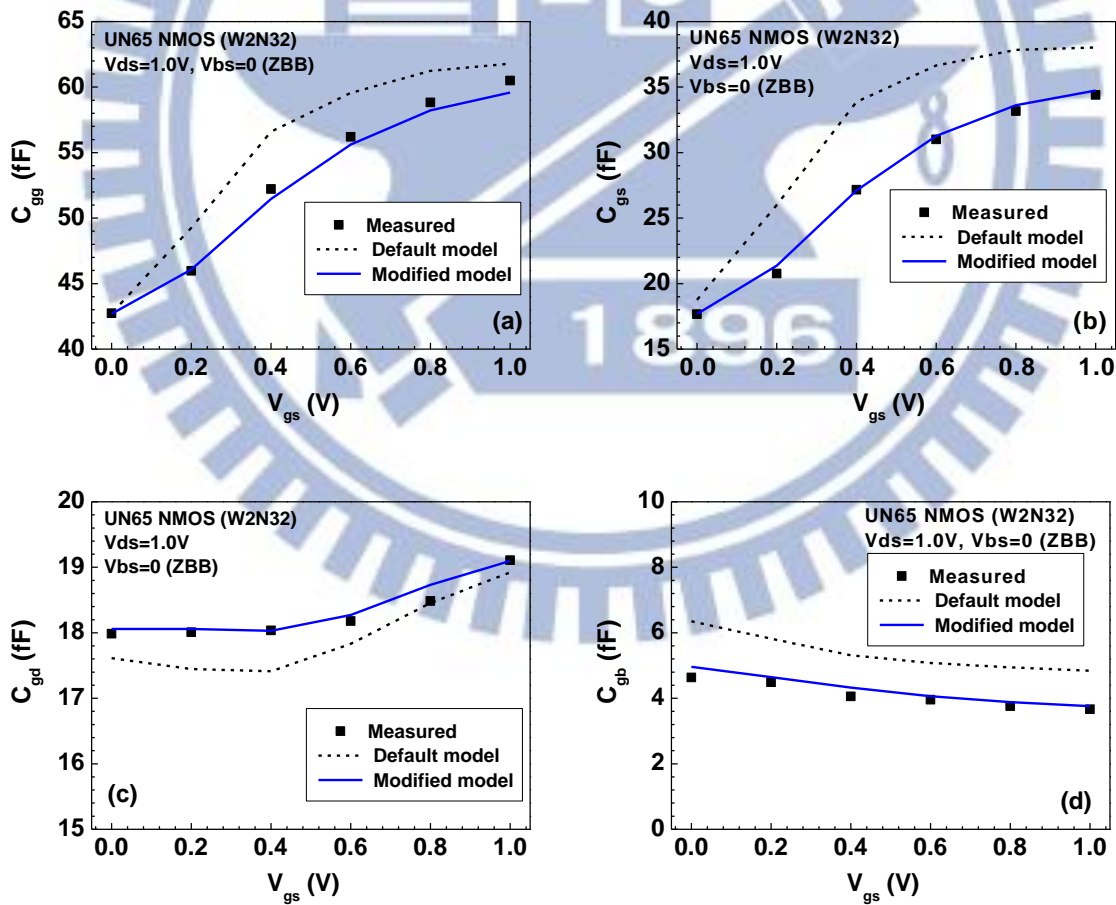
Fig. 3.79 Comparison of measured and simulated gate capacitances under ZBB ($V_{bs}=0$) (a) C_{gg}, (b) C_{gs} (c) C_{gd} and (d) C_{gb}. Simulation using default C-V model parameters (dash line) and modified parameters (solid line).
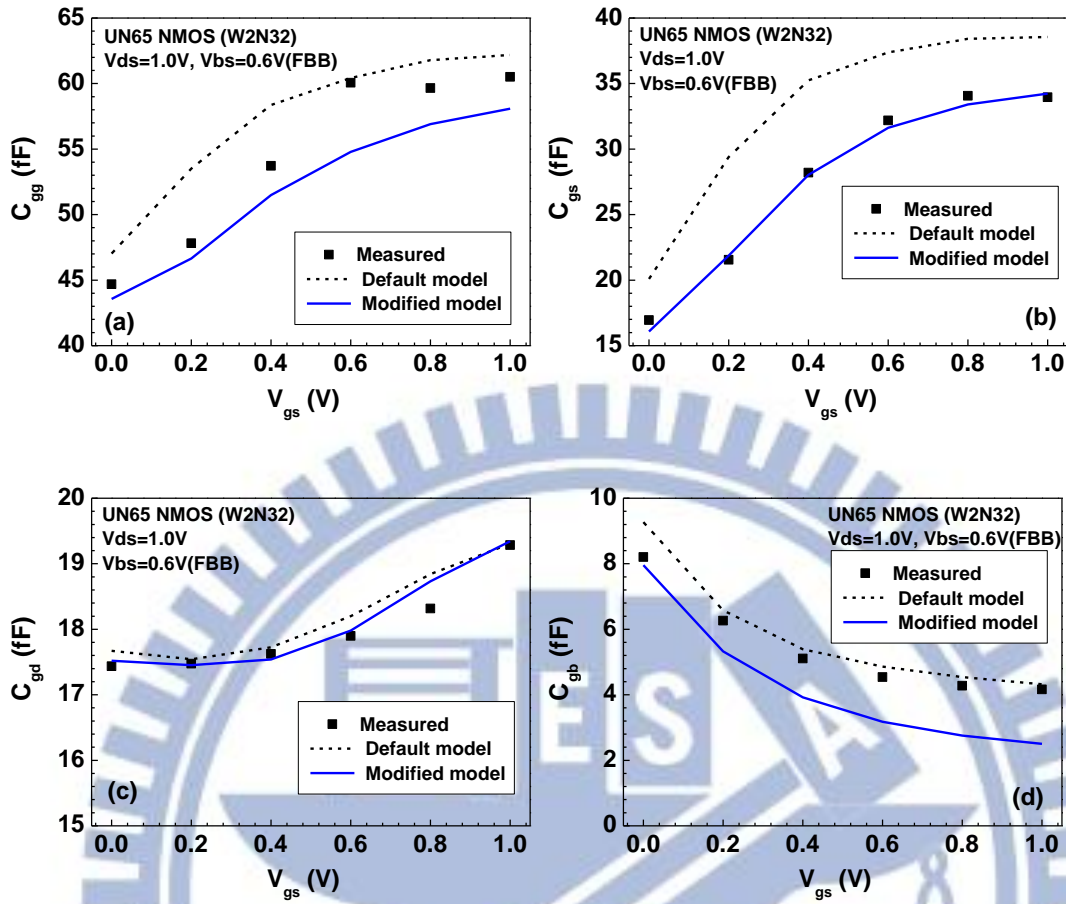
Fig. 3.80 Comparison of measured and simulated gate capacitances under FBB (V_{bs}=0.6V) (a) C_{gg}, (b) C_{gs} (c) C_{gd} and (d) C_{gb}. Simulation using default C-V model parameters (dash line) and modified parameters (solid line).
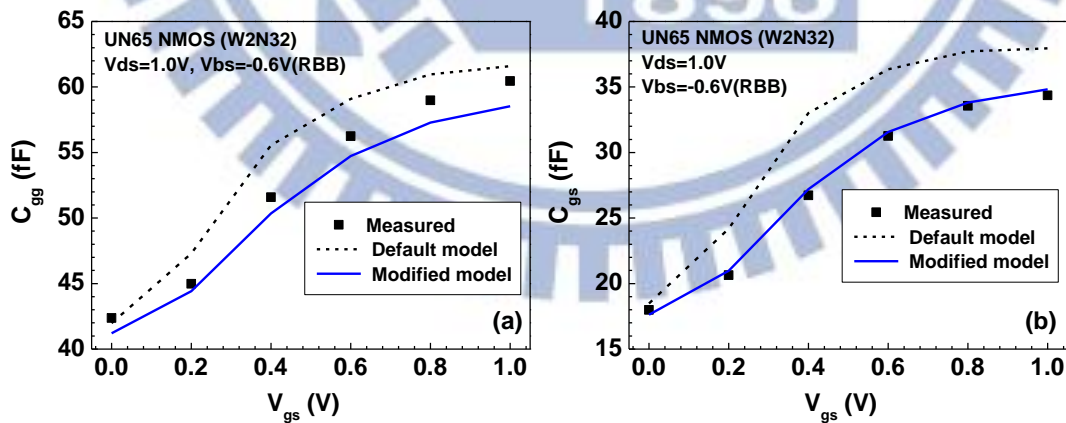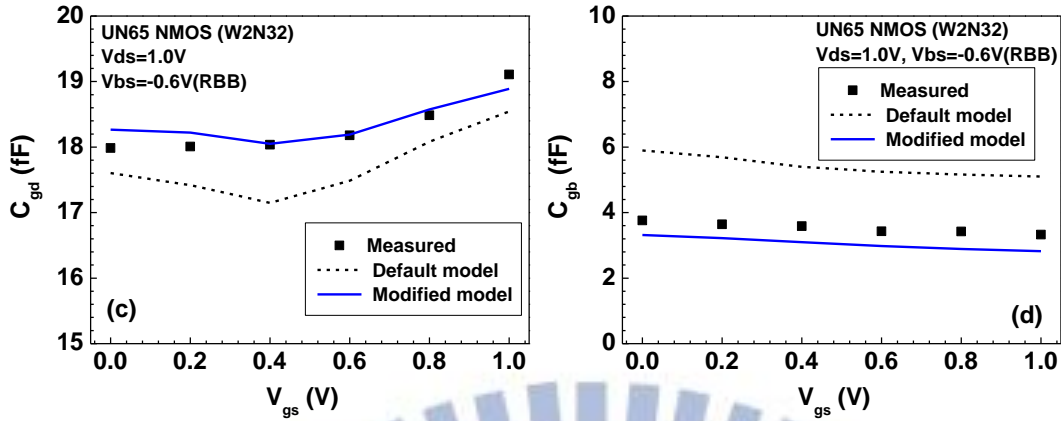
Fig. 3.81 Comparison of measured and simulated gate capacitances under RBB (V_{bs}=-0.6V) (a) C_{gg}, (b) C_{gs} (c) C_{gd} and (d) C_{gb}. Simulation using default C-V model parameters (dash line) and modified parameters (solid line).

3.4.3 RF Performance of 4-port RF MOSFET with DBB – Simulation and Measurement

High frequency simulation was performed using BSIM-4 after mentioned I-V as well as C-V calibration and small signal equivalent circuit model for 4-port RF MOSFET under dynamic body biases, i.e. ZBB (V_{bs}=0), FBB (V_{bs}=0.6V), and RBB (V_{bs}=-0.6V). Note that new body network model developed for small signal equivalent circuit can be implemented in BSIM-4 for a comparison with its default body network model. The transconductance g_m and gate capacitances (C_{gg}, C_{gs}, C_{gd}) have been recognized as the key parameters governing key RF performance parameters, such as f_T and f_{max}. As shown previously in **Fig. 3.79~ Fig. 3.81**, BSIM-4 after C-V calibration can simulation C_{gg}, C_{gs}, C_{gd}, and C_{gb} under ZBB, FBB, RBB with improved accuracy. **Fig. 3.82** illustrates g_m versus V_{gs} at V_{ds} =1.2V, simulated by BSIM-4 and the comparison with measurement. The results indicate that BSIM-4 when adopting new body network model can predict the measured g_m from subthreshold to strong inversion, under ZBB, FBB, and RBB. The increase of g_m driven by FBB is significant at V_{gs} below 0.5V but becomes negligible when increasing V_{gs} to above 0.6V, i.e. strong inversion region. On the other hand, RBB leads to g_m degradation at lower V_{gs}. The FBB and RBB

effect on g_m at sufficiently low V_{gs}, i.e. subthreshold region comes from V_T shift from body biases. However, BSIM-4 simulation reveal a large deviation from g_m measured at V_{ds} =1.0V, as shown in **Fig. 3.83**. This deviation suggests that DIBL effect was over-estimated at V_{ds} =1.0V and a modification on DIBL related model parameters may fix the problem. **Fig. 3.84** presents cut-off frequency f_T versus V_{gs} measured and simulated under ZBB, FBB, and RBB. The result indicates significant enhancement of f_T at $V_{gs} < 0.5V$ when applying FBB and it can be explained by the analytical model for calculating f_T given by (3.119). The increase of g_m caused by FBB can help enhance f_T but the increase of C_{gg} under FBB may degrade the enhancement effect. The experimental data of C_{gg} and C_{gd} shown in **Fig. 3.79 ~ Fig. 3.81** and g_m in **Fig. 3.83** indicate that FBB (or RBB) effect on g_m is much higher than the effect on C_{gg} and C_{gd}, and becomes the dominant factor responsible for f_T enhancement (or degradation). Again, BSIM-4 simulation reveals a large deviation from the measured f_T under FBB and RBB and it suggests the deviation originated from g_m.

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}}$$

(3.119)
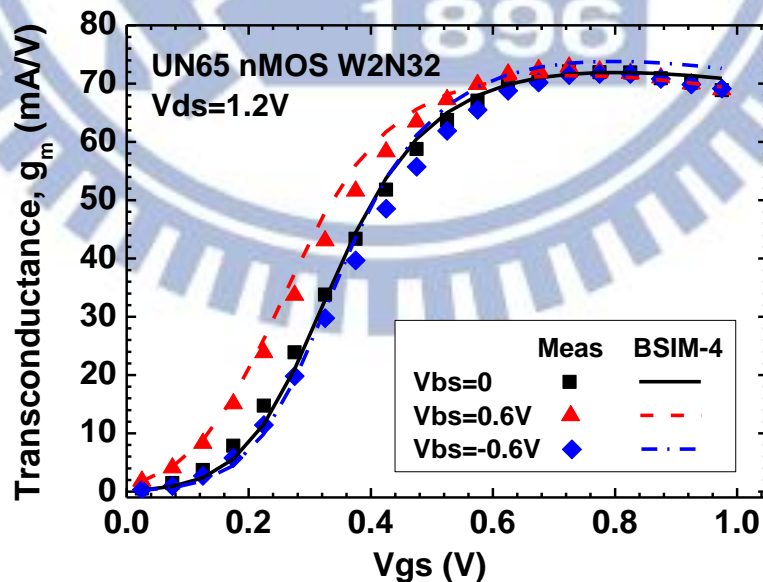
Fig. 3.82 Measured and simulated g_m versus V_{gs} for 4-port MOSFET under V_{ds}=1.2V and dynamic body biases. ZBB: V_{bs}=0, FBB: V_{bs}=0.6V, RBB: V_{bs}=-0.6V. Simulation : BSIM-4 with new body netowork model.
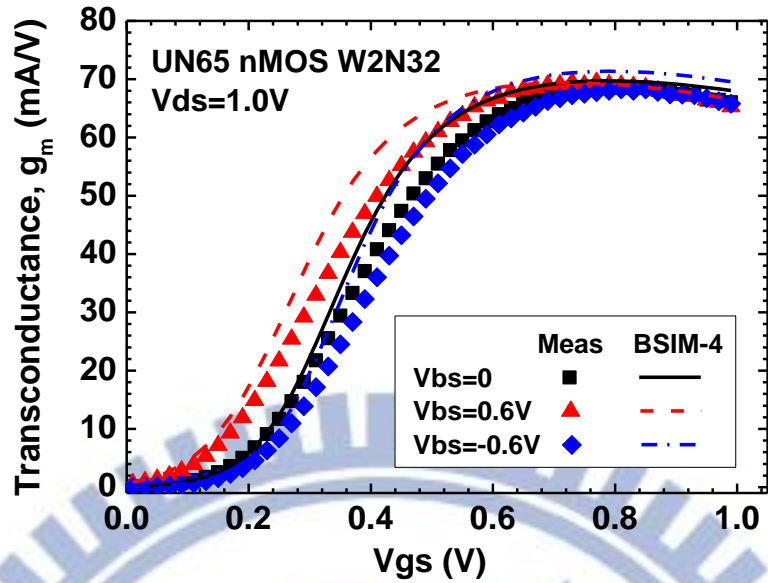
Fig. 3.83 Measured and simulated g_m versus V_{gs} for 4-port MOSFET under $V_{ds}=1.0V$ and dynamic body biases. ZBB: $V_{bs}=0$, FBB: $V_{bs}=0.6V$, RBB: $V_{bs}=-0.6V$. Simulation : BSIM-4 with new body netowork model.
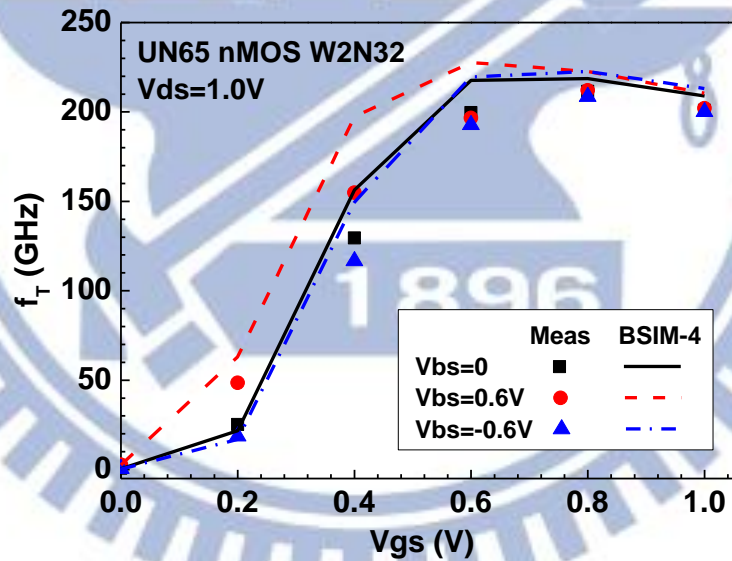
Fig. 3.84 Measured and simulated f_T versus V_{gs} for 4-port MOSFET under $V_{ds}=1.0V$ and dynamic body biases. ZBB: $V_{bs}=0$, FBB: $V_{bs}=0.6V$, RBB: $V_{bs}=-0.6V$. Simulation : BSIM-4 with new body netowork model.

Chapter 4　　　　New Cascode Design

and Modeling for RF Circuits Simulation

4.1　Review of Conventional Cascode Structure for RF Amplifiers

The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer. Compared to a single amplifier stage, this combination may offer the advantages, such as higher input-output isolation, higher input impedance for the lower stage transistor (M1), high output impedance for the upper stage transistor (M2), higher gain or wider bandwidth. In modern circuits, the cascode is generally constructed from two transistors (MOSFETs or BJTs), with the lower stage transistor operating as a common source (or common emitter) and the upper stage transistor as a common gate (or common base). The cascode topology can improve input-output isolation (or reverse transmission) as there is no direct coupling from the output to input. This minimizes the Miller effect and thus contributes to a much wider bandwidth.
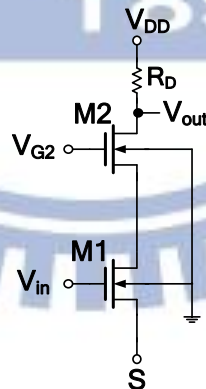
Fig. 4.1 A cascode amplifier with a common source amplifier as the input stage driven by signal source V_{in}.

Referring to **Fig. 4.1** for an example of cascode amplifier with a common source amplifier as the input stage driven by signal source V_{in}. This input stage drives a common gate amplifier as

output stage, with output signal V_{out}. The major advantage of this circuit configuration stems from the placement of the upper transistor (M1) as the load of the lower transistor's (M2) output terminal (drain). Because at operating frequencies the upper transistor's gate (G2 of M2) is effectively grounded, the M2's source voltage and therefore the M1's drain is held at nearly constant voltage during operation. In other words, the upper transistor (M2) exhibits a low input resistance to the lower transistor (M1), making the voltage gain of the M1 very small, which dramatically reduces the Miller feedback capacitance from the M1's drain to gate. This loss of voltage gain is recovered by the upper transistor (M2). Thus, the upper transistor permits the lower transistor (M1) to operate with minimum negative (Miller) feedback, improving its bandwidth. If the upper stage transistor (M2) were operated alone using its source as input node, i.e. common gate (CG) configuration, it would have good voltage gain and wide bandwidth. However, it will be limited to very low impedance voltage drivers due to its low input impedance. Adding the lower transistor (M1) can result in a high input impedance, allowing the cascode to be driven by a high impedance source. Under the condition that the upper transistor (M2) is removed and replaced by an inductive or a resistive load, and the output is taken from the input transistor's drain, i.e. a common-source (CS) configuration, it may offer the same input impedance as the cascode, but the cascode configuration can offer a potentially higher gain and much wider bandwidth.

Better stability is one more advantage achievable from the cascode configuration. Its output is effectively isolated from the input both electrically and physically. The lower transistor has nearly constant voltage at both drain and source and thus there is essentially "nothing" to feed back into its gate. The upper transistor has nearly constant voltage at its gate and source. Thus, the only nodes with significant voltage on them are the input and output, and these are separated by the central connection of nearly constant voltage and by the physical distance of two transistors. Thus in practice there is little feedback from the output to the input. Metal shielding is both effective and easy to provide between the two transistors for even

greater isolation when demanded. This would be difficult in one-transistor amplifier circuits, which at high frequencies would require neutralization.

Table 4.1 summarizes four operation modes, which may exist in a cascode topology according to different combination of M1/M2 operation regions. It is well known that both M1 and M2 operating in saturation region, namely saturation-saturation is the operation mode most favorable for a cascode amplifier.

Table 4.1 Cascode MOSFET operation modes and features

Cascade operation modes	M1	M2	Features
Saturation	Saturation	Saturation	Maximum current and gain for amplifiers
Linear saturation	Saturation (linear)	Linear (Saturation)	Medium current and gain
Linear	linear	linear	Small current and gain
Cut off	Cut off	Cut off	Nearly zero current and gain

According to the circuit schematics of cascode as shown in Fig 4.1, the supply voltage applied to the drain node, namely V_{DD} has to be distributed between two MOSFETs, M1 and M2. It can be easily understood that the increase of gate bias in M1 (V_{G1}) will lead to lower drain voltage (V_{D1}) and may drive M1 into linear region. Under the condition that M1 is driven into linear region, this cascode amplifier will suffer lower current and gain degradation. The increase of V_{DD} may offer higher V_{D1} to keep M1 operate in saturation region but the increase of V_{DD} is limited by junction breakdown and gate oxide breakdown, which impose the worst damage to M2 at off state (i.e., $V_{G2}=0$ for common gate). Due to the limitation to V_{G1} and V_{DS1} available from V_{DD}, it allow limited room for M1 to operate under the optimized bias condition with maximum g_m ($g_{m,max}$).

Based on the basic circuit topology and operation principle as mentioned previously, cascode structure has been widely used in RF circuits, such as mixer, low noise amplifier

(LNA), and power amplifier (PA) attributed to the advantages of less Miller effect, higher output impedance, and better reverse isolation (or transmission leakage). On the other hand, it has been recognized that parasitic RLC elements enforce dramatic impact on RF circuits performance and reducing internal parasitic effect becomes critically important in devices layout for RF circuit design. This fundamental problem motivates our interest in a new cascode design for suppressing internal parasitic effect and improving RF circuit performance.

4.2 New Cascode using Dual Gate MOSFET with Merged S/D Diffusion

The cascode topology using a dual-gate MOSFET attracts increasing interest in recent years and has been adopted in various RF circuits, such as distributed amplifiers (DA) [32], variable gain amplifiers (VGA) **[33]**, low noise amplifiers (LNA) **[34]**, and mixers **[35]**. The dual-gate MOSFET with two separate gates can enable various operation modes via different combination of two independent gate biases applied to M1 and M2 as summarized in **Table 4.1**. The LNA using dual-gate MOSFET published in 2002 JSSC presented around 1.2dB higher gain (maximum available gain, MAG) and 0.7dB lower minimum noise figure (NF_{min}) compared with those achieved by conventional cascode using two individual MOSFETs [34]. The authors concluded the major contribution from the smaller area of the parasitic diode and then the suppression of signal loss through the Si substrate **[34]**. However, a detailed analysis on the parasitic resistances and capacitances associated with the dual-gate MOSFET and the comparison with two separate MOSFETs for conventional cascode is not available from existing publication. A doubly balanced CMOS mixer using dual-gate MOSFET presented in 1999 JSSC reveals major difference in mixing process from that of conventional doubly balanced Gilbert mixer **[35]**. For the conventional one, the LO signal at the drain of the differential pair is zero. However, for dual-gate mixer, the LO signal is required at the drain of the lower MOSFET (M1) to induce mixing action. The principal mixing action of a dual-gate mixer is driven by modulating the transconductance g_m via switching the lower MOSFET

between the linear and saturation region whereas that of the conventional Gilbert mixer is operated by switching between cut-off and active (saturation) region. Due to the fact that transconductance nonlinearity achieved by linear-saturation switching is smaller than that realized by cut-off to active switching, this dual-gate mixer requires higher LO power than Gilbert mixers.

Even though the dual-gate cascode demonstrates some successful examples of RF circuits design in previous work [32]-[35], modeling and parameters extraction appear as more complicated and challenging to the new cascode structure using dual-gate MOSFETs. The major difficulty is originated from the configuration with at least 5 electrodes (terminals) in a dual-gate MOSFET, such as gate of M1 (G1), gate of M2 (G2), source of M1 (S), drain of M2 (D), and body (B) of both. Provided that a separate electrode to deep N-well is requird, it will increase the complexity. A small signal equivalent circuit model published in 2007 RFIC symp. proposed a combination of the conventional hybrid-p model for transistors, external parasitic capacitances, resistances, and inductances (RLC), and a substrate network with a shared node at the resistive node [36]. However, the assumptions of identical capacitances from the gate (and body) to the source (S) and drain (D) in M1 and M2, such as $C_{gs1}= C_{gs2}$ and $C_{gd1}= C_{gd2}$ (and $C_{db1}= C_{db2}$) [36] are absolutely not valid, even for an operation at off state, i.e. zero bias for all nodes. In practical layout for multi-finger MOSFETs used in RF circuits, the metal line routing from the gate to S/D cannot be identical in most frequently used two-port test structure and even four-port test tester. The fact explains why the mentioned assumption cannot be justified. One more problem is that the proposed method requires an extensive optimization using Agilent IC-CAP and this approach may lead to un-physical parameters. Later on, another small signal model was published for dual-gate MOSFET, namely cascode with merged diffusion, trying to fix the mentioned problems by using four-port S-parameters measurement [37]. Unfortunately, the proposed extraction method reveals some fundamental problems, e.g. the direct extraction of inter-stage capacitances, given by C_{gd1}=-Im(Y_{G1G2}

125

+2Y_{G1D})/ω and C_{gs2} =-Im(Y_{G2S})/ω. In fact, the drain(D)/source(S) nodes for M1/M2 are floated so that Y_{G1D} and Y_{G2S} cannot be measured with either one of the nodes at floating state. Moreover, the inter-stage capacitances as extracted indicate similar value with that of in-stage capacitances, such as $C_{gs2} \cong C_{gs1}$ and $C_{gd1} \sim C_{gd2}$ [37] and this result cannot be justified by the device physics for MOSFETs. Recently, an extraction flow for 0.18μm dual-gate MOSEFT modeling was proposed [38]. This method was based on core device model in BSIM-3 for I-V fitting and two-port S-parameters for capacitances and resistances extraction. Unfortunately, the proposed extraction flow exposes a critical problem in capacitances extraction because two-port S-parameters measurement definitely cannot provide sufficient data for dual-gate MOSFET modeling in which RLC parameters associated with at least four ports are required to ensure an accurate modeling. One more basic problem with this method comes from the proposed three-port S-parameters measurement by using two-port vector network analyzer (VNA) [38]. Our previous work on four-port S-parameters measurement and deembedding identified an important principle that four-port reduction to two-port and then followed by two-port deembedding is absolutely different from four-port S-parameters through four-port deembedding and followed by port reduction to two-port S-parameters. According to this principle, the 3×3 matrix composed by three 2×2 matrices from 3 steps of two-port S-parameters measurement definitely cannot be equivalent to 3×3 matrix achieved from truly three-port S-parameters measurement.

All of the mentioned challenges with unknown solutions and obvious problems with the existing methods motivate our interest in this research topic to develop a reliable method for model parameters extraction method and then to establish a small signal equivalent circuit model with sufficient accuracy for dual-gate MOSFETs under various operation conditions.

4.2.1 Comparison between New Cascode and Conventional Cascode Structures

Fig. 4.2(a) and (b) illustrate the layouts generated according to UN65 CMOS design rule for conventional cascode and new cascode, respectively. The conventional cascode as shown in **Fig. 4.2**(a) is composed of two multi-finger MOSFETs, which are originally separated and then stacked in series by additional contacts and metal lines. The new cascode shown in **Fig. 4.2**(b) is built with a dual-gate MOSFET in which every two adjacent gates, i.e. G1/G2 for M1/M2, share the same S/D diffusion region, namely merged S/D. In this way, the lower and the upper MOSFET (M1 and M2) can be stacked together via the merged S/D, without any contacts and metal lines for interconnection. **Table 4.2** summarizes the comparison between the conventional cascode and new cascode in terms of various features, such as transistors and interconnection layout, parasitic capacitances and resistances, junction and chip area, and modeling. The one-by-one comparison forecasts that new cascode using dual-gate MOSFET can yield the advantages of small chip area, smaller parasitic capacitances and resistances attributed to shorter interconnection lines and less contact numbers. However, this new cascode when using single-end gate contact may suffer larger R_g and increase of noise figure. The major challenge to applying new cascode is the difficulty in modeling and simulation accuracy, which is originated from the complicated layout dependent effect, e.g. resistance and capacitances associated with floating node for the merged S/D region. The mentioned challenges motivate our interest in this work.
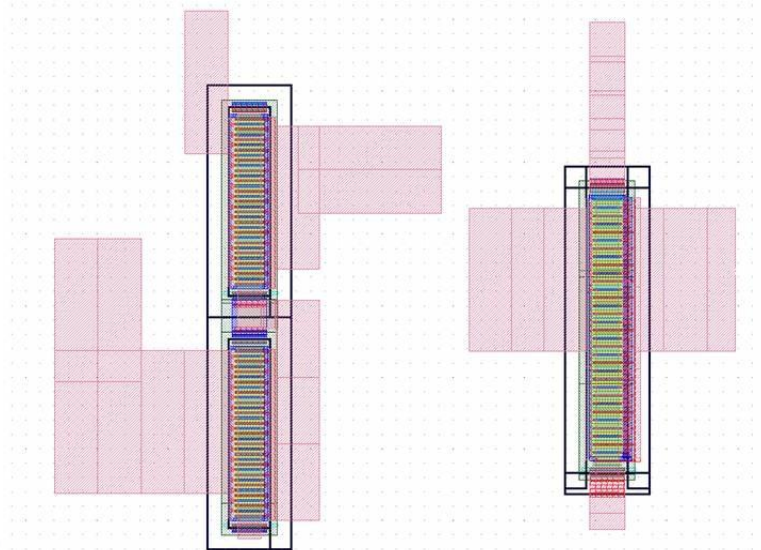
Fig. 4.2 The illustration of cascode layouts (a) conventional cascode with two separate MOSFETs (b) new cascode with dual-gate MOSFET and merged source/drain

Table 4.2 Comparison between conventional cascode and new casode in various features

Cascode structures	New Cascode	Conventional Cascode
Layout	Dual-gate MOSFET with merged S/D	Two separate single MOSFETs stacked with metal line
Interconnection lines	shorter	Longer
Contact number	less	More
Parasitic resistances from interconnect	Smaller	Larger
Parasitic capacitances from interconnect	Smaller	Larger
S/D diffusion area	Smaller	Larger
S/D junction capacitances	Smaller	Larger
Gate contacts layout	Single-end	Two-end
Gate resistance Rg	Larger	Smaller
Chip area	Smaller	Larger
Port number	4~5	3~4
Modeling	More complicated and difficult	Simple and mature
Small signal equivalent circuit model	Problems in parameters extraction method and model accuracy	Ready for single MOSFET

4.2.2 Dual-gate MOSFET Measurement and Deembedding Method

Conventionally, almost all of RF CMOS circuit simulation and design reply on two-port S-parameters and the extracted model for fitting S- and Y-parameters in frequency domain. Basically, two-port characterization and modeling can appropriately fit two-terminal passive devices, such as resistors, capacitors, and inductors. However, this simplified approach generally forces 4-terminal devices lose freedom in bias schemes and available

circuit topologies. MOSFETs given as the most frequently used 4-terminal devices, are generally limited to a 3-terminal configuration in RF circuit layout and design. This 3-terminal configuration, generally formed with body (B) shorted with source (S) to a common ground restricts MOSFET to a common source (CS) topology and non-availability of body biases. As for dual-gate MOSFET for new cascode, the restriction caused by two-port measurement and deembedding imposes significant impact on characterization and parameters extraction for modeling. To fix the mentioned problems, four-port measurement and deembedding become indispensable for dual-gate MOSFET parameters extraction and model development.

There are two kinds of four port test structures supported for high frequency S-parameter measurement. One is constructed with four GSG pads configured orthogonal between every two adjacent pads, namely 4-GSG, as shown in **Fig. 4.3(b)**. Another one is built with two GSGSG pads in parallel with each other, namely 2-GSGSG, illustrate in **Fig. 4.3(c)**. The later one becomes increasingly popular and recommended for the advantage of reduced area and potentially smaller parasitic due to shorter interconnection lines. Basically, the major differences between two structures are summarized as (i) 4-port on wafer calibration methods (ii) RF probes (iii) through pad layout and de-embedding method (iv) interconnection line layout for 4-terminal devices。 For on-wafer calibration in (i), Agilent PNA-L VNA can provide a better solution assisted with a dedicated calibration substrate。Regarding four port on-wafer measurement, NDL RF Lab. can support (i) and (ii). Note that probe correction is generally not employed in substrate calibration and has to be performed separately. Conventionally, 12-error model is selected and the error terms are determined for each pair of probes using SOLT method on LRM substrate. In general, error terms determination is a sophisticated procedure but has a good stability with time. The major concern is contact impedance, which may evolve during the probe correction and has to be corrected at following de-embedding step。As for through pad layout and metal line routing for 4-terminal

MOSFET in (iii) and (iv), dedicated effort is needed to explore an optimized design, which is relatively more challenging for RF MOSFET, a kind of active devices than 4-terminal passive elements like transformers. Four-port test structure like well known two-port structure incorporate multiple parasitic components (R, L, C), which are even more complicated than the two-port structure. **Fig. 4.4** illustrates a simple equivalent circuit for a four-port structure incorporating parasitic impedances and admittances in each individual signal pad to ground and between every two adjacent signal pads. The basic de-embedding structures involve open and short dummy pads. First, open de-embedding for four port structures can be carried out according to a 4x4 Y-parameters matrix calculation. Then, four-port short de-embedding can be carried out according to the calculation of a 4x4 Z-parameters matrix.

Based on the equivalent circuit of 4-port short pads, the parasitic resistances (R) and inductances (L) extraction can be carried out, according to **(4.1)~(4.4)**. **Fig. 4.5(a) and (b)** present R_g, R_d, and R_s, R_b extracted from two-port and four-port short deembedding structures (ShortM3 : top metal to metal-3) as shown in **Fig. 4.3**(a)~(c). Note that The parasitic R extracted from shortM3 indicate that 4-GSG suffers the maximum R at each port whereas 2-GSG can achieve the minimum values. All of the extracted resistances increase with raising frequency in the lower frequency domain, f <10GHz and gradually saturate to a constant when continuously increasing the frequency, well above 10GHz. The increase of R in the domain of f <10GHz suggests the influence of skin effect. **Fig. 4.6(a)** and **(b)** shown the parasitic inductances**,** L_g, L_d, and L_s, L_b extracted from two-port and four-port shortM3 structures. Similarly, the extracted L indicate that 4-GSG suffers the maximum L at each port whereas 2-GSG can keep the minimum values. However, these parasitic L reveal frequency dependence in contrast with that of parasitic resistances, that is all of the extracted L decrease with increasing frequency in f < 5GHz and gradually saturate to a constant when continuously increasing the frequency. The fall-off of parasitic L with increasing frequency suggests capacitive coupling effects, maybe from interconnection lines to the lossy substrate.

$$R_{g,ext} = \text{Re}(Z_{11} - Z_{12}), \ L_{g,ext} = \frac{\text{Im}(Z_{11} - Z_{12})}{\omega} \qquad (4.1)$$

$$R_{s,ext} = \text{Re}(Z_{22} - Z_{12}), \ L_{s,ext} = \frac{\text{Im}(Z_{22} - Z_{12})}{\omega} \qquad (4.2)$$

$$R_{d,ext} = \text{Re}(Z_{33} - Z_{32}), \ L_{d,ext} = \frac{\text{Im}(Z_{33} - Z_{32})}{\omega} \qquad (4.3)$$

$$R_{b,ext} = \text{Re}(Z_{44} - Z_{42}), \ L_{d,ext} = \frac{\text{Im}(Z_{44} - Z_{42})}{\omega} \qquad (4.4)$$

$$R_{N\_ext} = \text{Re}(Z_{12})$$

(a)   (b)   (c)
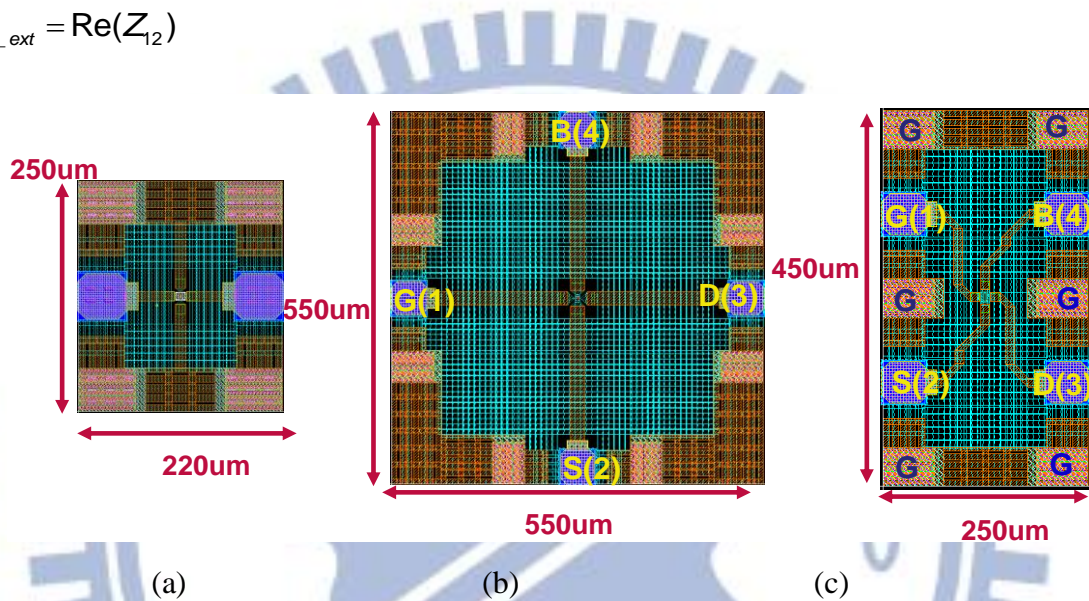
Fig. 4.3 The layouts of 2-port and 4-port test structures for RF MOSFET measurement (a) 2-port tester with two GSG pads in parallel (b) 4-port tester, namely 4-GSG with four GSG pads in perpendicular direction between every two adjacent pads (c) 4-port tester, namely 2-GSGSG with two GSGSG pads in parallel.
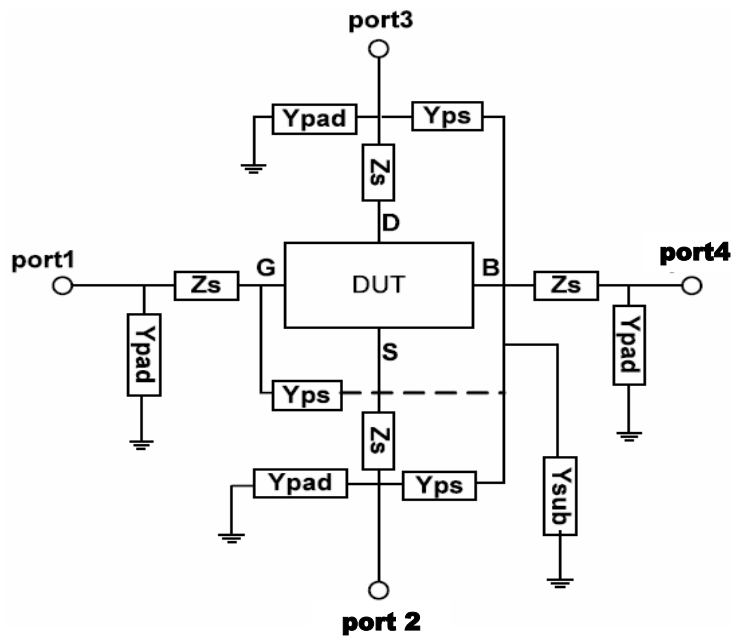
Fig. 4.4 The equivalent circuit for a four-port test structure incorporating parasitic impedances (Zs) and admittances (Ypad, Yps)
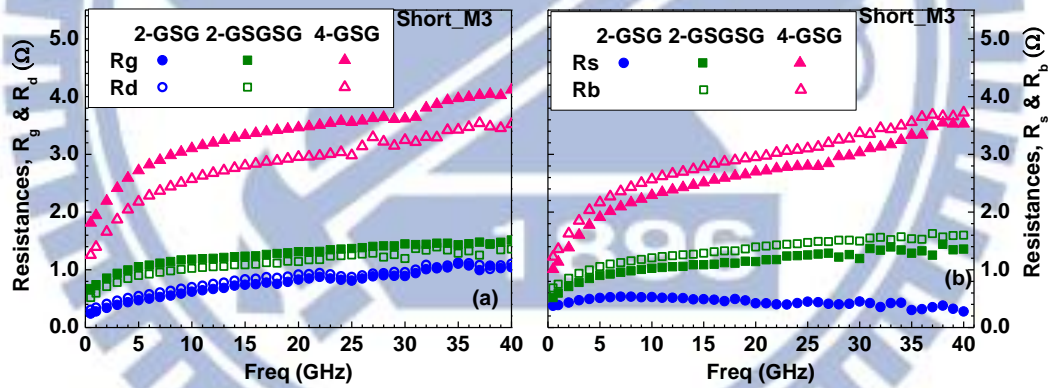
Fig. 4.5 The parasitic resistance extracted from two-port (2-GSG) and four-port (2-GSGSG, 4-GSG) shortM3 deembedding structures (a) R_g and R_d for interconnection lines to gate and drain pads (b)R_s and R_b for interconnection lines to source and body pads
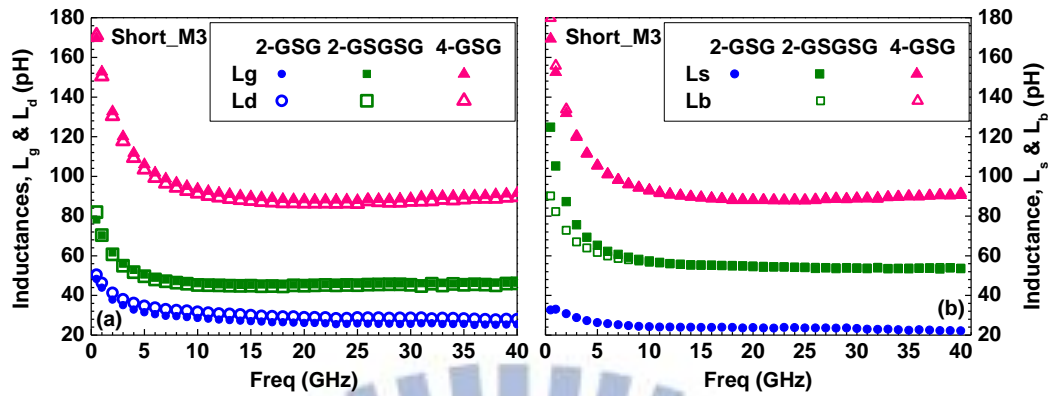
Fig. 4.6 The parasitic inductances extracted from two-port (2-GSG) and four-port (2-GSGSG, 4-GSG) shortM3 deembedding structures (a) L_g and L_d for interconnection lines to gate and drain pads (b) L_s and L_b for interconnection lines to source and body pads

4.3 Dual-gate MOSFET Equivalent Circuit Model and Parameters Extraction Method for New Cascode Simulation

In the following, small signal equivalent circuits will be developed for dual-gate MOSFET under various operation modes, such as off-state under zero bias and active state with both M1 and M2 in saturation region. As mentioned previously, four-port measurement and deembedding are indispensable to enable an accurate characterization and model parameters extraction for dual-gate MOSFET with at least four individual electrodes. Taking a review on the simplified circuit schematics for dual-gate MOSFET shown in **Fig. 4.7(a)**, there are actually five electrodes, such as G1 (gate for M1), G2 (gate for M2), S (source for M1), D (drain for M2), and B (body for M1 and M2). It means that four-port measurement cannot supply RF signal to all of the five electrodes for a complete determination of model parameters associated with every two terminals among the five electrodes. Take **Fig. 4.7**(a) as an example, G1 and G2 are allocated as two separate electrodes to occupy two ports, and the remaining two ports are allocated for S and D. This configuration leaves body (B) without RF port and connected to ground. As a result, all of the model parameters related to the body,

133

such as G1/G2 to B gate capacitance, S/D to B junction capacitances, and body resistances cannot be directly extracted from the 4-port S-parameters measured from this configuration. To overcome this limitation, another test structure with G1 and G2 shorted together to one port, namely common gate cascode, was implemented as shown in **Fig. 4.7(b)** wherein the remaining port can be allocated to the body. In this way, the body network model can be built based on the 4-port S-parameters measured from common gate structure. Based on dual-gate and common-gate structures, a complete extraction flow can be established for off-state and active-state in the following sections.

　　Fig. 4.8(a) illustrates a complete circuit schematics for dual-gate MOSFET with a comprehensive assignment of capacitive, inductive, and resistive components associated with every two terminals among the five electrodes. M1 and M2 represents core devices incorporating channel conductance and capacitances (on or off states), and junction diodes associated with S/B and D/B. C_{g1s} and C_{g2d} represent in-stage gate capacitances associated with G1 to S coupling in M1 and G2 to D coupling in M2. In contrast with the in-stage capacitances contributed from two electrodes in the same device, C_{g1d} and C_{g2s} are cross-stage gate capacitances generated by two electrodes across different devices. C_{g1d} represents the coupling from G1 in M1 to D in M2 and C_{g2s} stems from the coupling from G2 in M2 to S in M1. Besides in-stage and cross-stage capacitances, C_{g1d1} and C_{g2s2} denote the inter-stage gate capacitances, which are contributed from the coupling between gate (G1 and G2) and the floating node in the merged S/D region between M1 and M2. Note that inter-stage capacitances are specific for dual-gate MOSFET and cannot be measured from the 4-port test structure because one of the terminals is floated. It means that C_{g1d1} and C_{g2s2} have to be determined by calculation with all of the other gate capacitances known from 4-port Y-parameters. R_{sd} is series resistance associated with the merged S/D diffusion. **Fig. 4.8 (b)** illustrates the layout of dual-gate MOSFET in which different layers remarked as G1, G2, S, and D can help understand the layout dependence of the mentioned gate related capacitances.
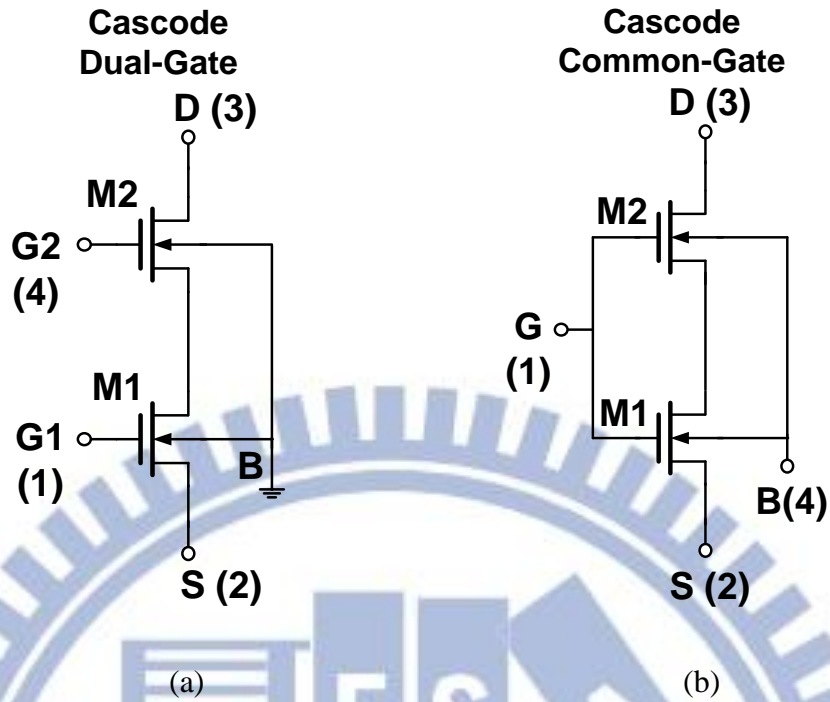
Fig. 4.7 Simplified circuit schematics for (a) dual-gate MOSFET with 4-port assignment as G1 (1), S(2), D(3), G2(4), and body connected to ground (b) common gate structure with G1 and G2 shorted together to port-1 and body to port-4, resulting 4-port assignment : G1/G2 (1), S (2), D(3), and B(4).
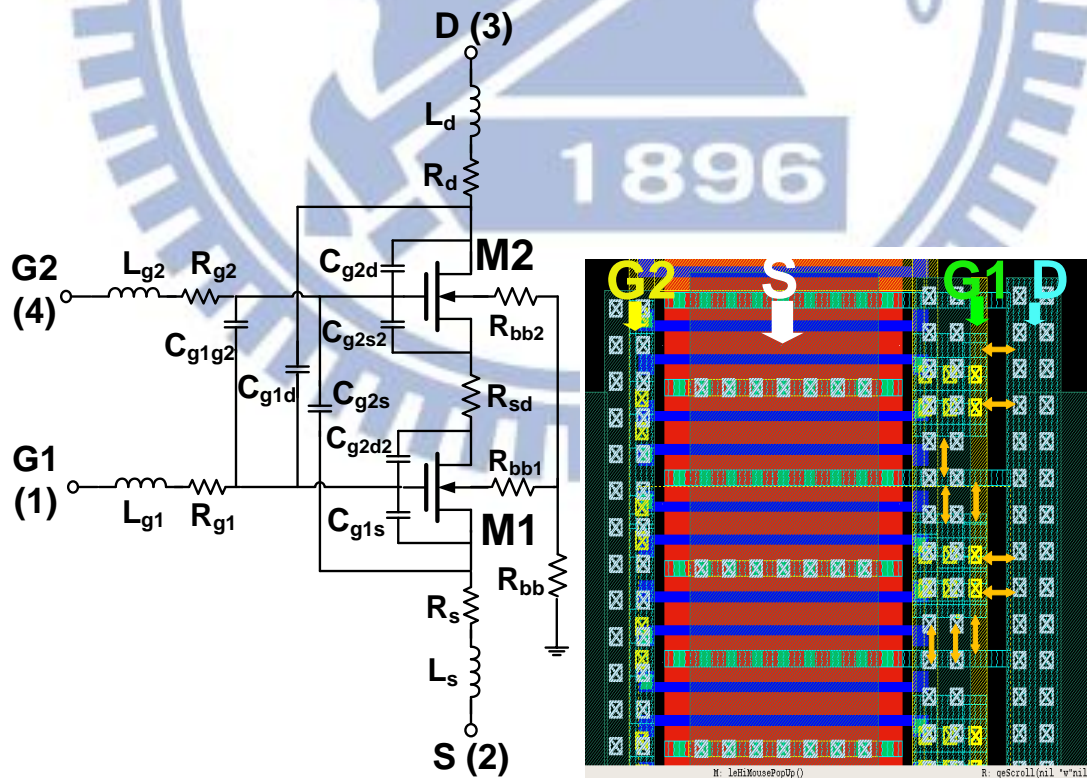
Fig. 4.8 (a) The circuit schematics of dual-gate MOSFET with a detailed assignment of the capacitive, inductive, and resistive components (b) layout of the dual-gate MOSFET

4.3.1 Small Signal Equivalent Circuit Model of Dual-gate MOSFET at Off State

Fig. 4.9 illustrates the small signal equivalent circuit model proposed for the dual-gate MOSFET at off state, i.e. cold device condition with all of the terminals at zero bias. To enable a complete model parameters extraction flow, this small signal equivalent circuit is divided into two parts – one region remarked by solid-line box is the intrinsic device model incorporating all of the gate related capacitances except gate to body capacitances, and the other enclosed by the dash-line box is the body network mode including gate (G1 and G2) to body capacitance (C_{g1b} and C_{g2b}), junction capacitances(C_{js1} and C_{jd2}), and body resistances. First, the model parameters associated with the intrinsic device can be extracted from 4-port Y-parameters measured from the dual-gate test structure with ports assignment shown in **Fig. 4.7**(a). The extraction method is described by (4.5)~(4.11)

All of the gate capacitances except C_{gb} can be extracted from 4-port Y-parameters measured from dual-gate MOSFET as follows

$$C_{gg1} = \frac{Im[Y_{G1G1}]}{\omega}\Big|_{LF} \tag{4.5}$$

$$C_{g1s} = \frac{-Im[Y_{G1S}]}{\omega}\Big|_{LF} \tag{4.6}$$

$$C_{g1d} = \frac{-Im[Y_{G1D}]}{\omega}\Big|_{LF} \tag{4.7}$$

$$C_{gg2} = \frac{Im[Y_{G2G2}]}{\omega}\Big|_{LF} \tag{4.8}$$

$$C_{g2d} = \frac{-Im[Y_{G2D}]}{\omega}\Big|_{LF} \tag{4.9}$$

$$C_{g2s} = \frac{-Im[Y_{G2S}]}{\omega}\Big|_{LF} \tag{4.10}$$

$$C_{g1g2} = \frac{-Im[Y_{G1G2}]}{\omega}\Big|_{LF} \tag{4.11}$$

C_{gb} can be and extracted from $Im(Y_{GB})$ measured from the common gate structure, **Fig.**

4.7(b)

$$C_{gb} = \frac{-Im[Y_{GB}]}{\omega}\Big|_{HF} , C_{g1b} = C_{g2b} = \frac{C_{gb}}{2} \tag{4.12}$$

then, the inter-stage gate capacitances can be calculated from all of other gate capacitances determined from (4.5)~(4.12)

$$C_{g1d1} = C_{gg1} - C_{g1s} - C_{g1d} - C_{g1b} - C_{g1g2} \tag{4.13}$$

$$C_{g2s2} = C_{gg2} - C_{g2d} - C_{g2s} - C_{g2b} - C_{g1g2} \tag{4.14}$$

The junction capacitances associated with S/D to B in M1/M2, namely C_{js1} and C_{jd2} can be extracted from $Im(Y_{BS})$ and $Im(Y_{BD})$ measured from common gate structure, as given by (4.15) and (4.16)

$$C_{js1} = \frac{-Im[Y_{BS}]}{\omega}\Big|_{LF} \tag{4.15}$$

$$C_{jd2} = \frac{-Im[Y_{BD}]}{\omega}\Big|_{LF} \tag{4.16}$$

Note that all of the capacitances, except C_{gb} are extracted from Y-parameters at very low frequency to minimize the effect from parasitic inductances and resistances.

Finally, gate resistances associated with M1 and M2, denoted as R_{g1} and R_{g2} are extracted by Y-method given by (4.17) and (4.18). Note that the conventional Z-method, which has been frequently used in single MOSFET may not be applicable to dual-gate MOSFET. **Fig. 4.10** summarize a complete model parameters extraction flow for small signal equivalent circuit model of dual-gate MOSFET at off state (($V_{G1}= V_{G2}= V_D= V_S= V_B=0$) in which the details of extraction method has been described by (4.5)~(4.18).

$$R_{g1} = \frac{Re(Y_{G1G1})}{[Im(Y_{G1G1})]^2}\Big|_{HF} \tag{4.17}$$

$$R_{g2} = \frac{Re(Y_{G2G2})}{[Im(Y_{G2G2})]^2}\Big|_{HF} \tag{4.18}$$
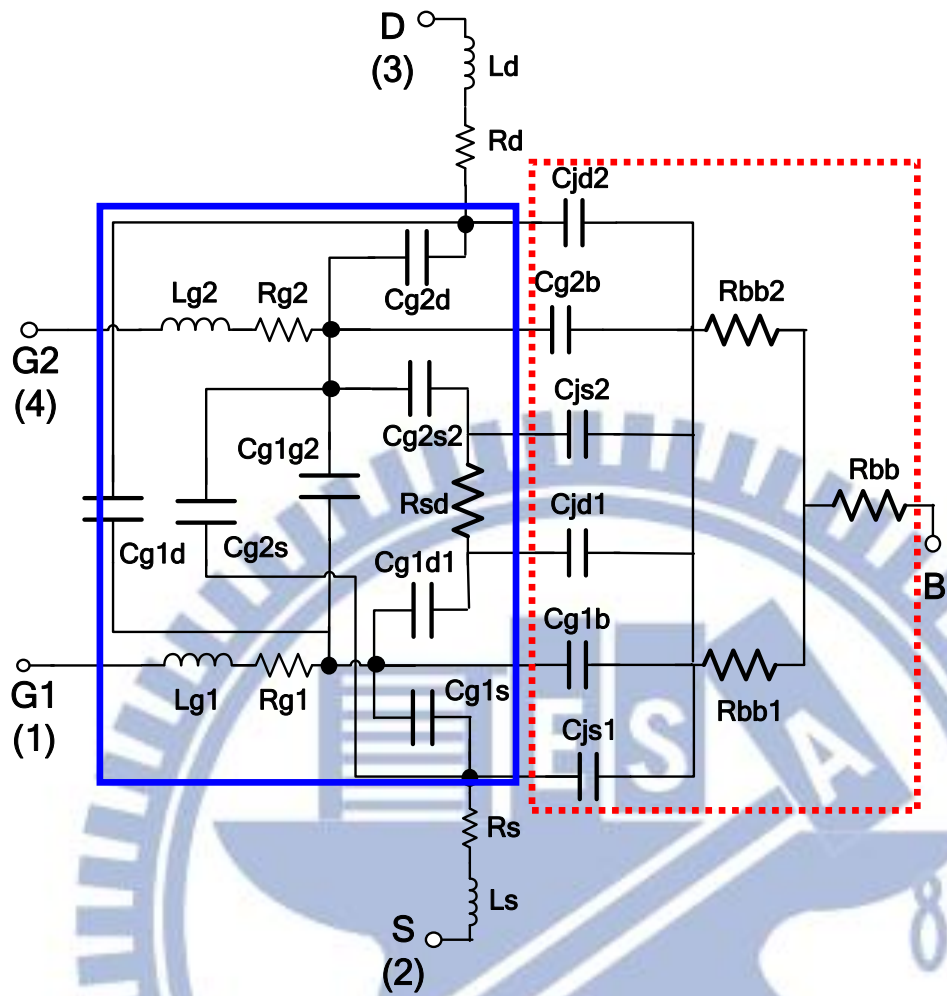
Fig. 4.9 The small signal equivalent circuit model of dual-gate MOSFET at off state : the region remarked by solid-line box is the intrinsic device model excluding body network model and the region enclosed by dash-line box is the body network model
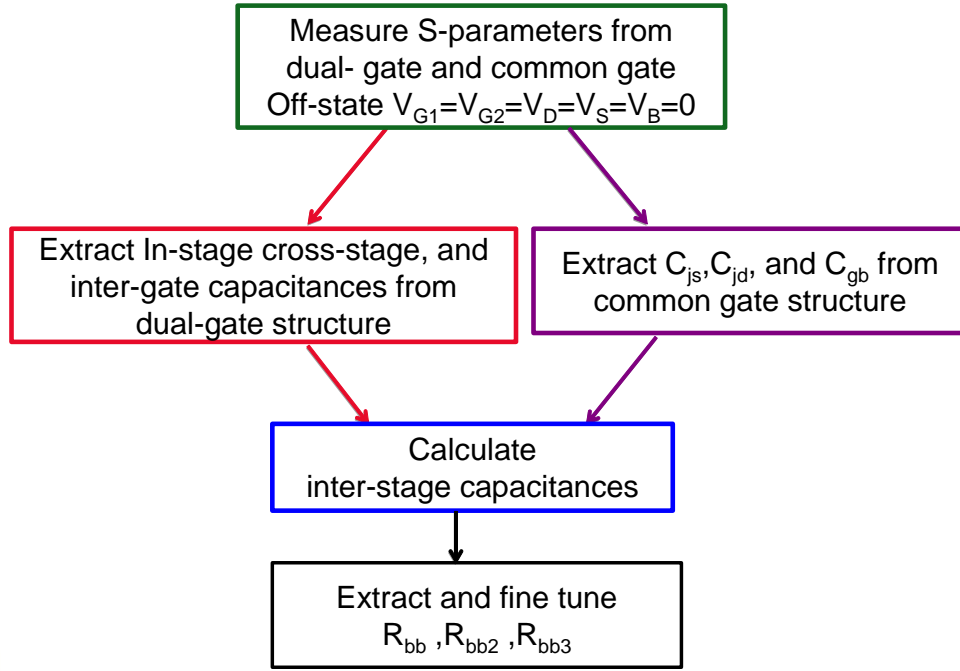
Fig. 4.10 Model parameters extraction flow for small signal equivalent circuit model of dual-gate MOSFET at off state ($V_{G1}= V_{G2}= V_D= V_S= V_B=0$)

In the following the extracted model parameters, such as in-stage capacitances, cross-stage capacitances, inter-gate capacitance, inter-stage capacitance, gate to body capacitance, junction capacitances, and gate resistances will be presented for a detailed discussion. **Fig. 4.11** shows the in-stage gate capacitances C_{g1s} and C_{g2d} extracted from $Im(Y_{G1S})$ and $Im(Y_{G2D})$, which were measured from dual-gate MOSFET at off state and went through 4-port OpenM3 deembedding (short deembedding was not available due to problem with dummy short pads in L65003 for this thesis). It appears that C_{g1s} is larger than C_{g2d}. Taking a review on the layout and cross-section in the same plot, the distance between G1 and S is shorter than that between G2 and D and it explains why C_{g1s} is larger than C_{g2d}. At the same time, C_{gs} and C_{gd} measured from the single MOSFET with the same finger width and number are provided for a comparison. Interestingly, a good match is demonstrated between C_{gs}/C_{gd} and C_{g2d}/C_{g1s} except somewhat larger difference between C_{gd} and C_{g1s} at very high frequency. The increase of capacitances at higher frequency suggests the impact from parasitic inductances and will be verified by simulation as follows. **Fig. 4.12** demonstrates the cross-stage gate capacitances

C_{g1d} and C_{g2s} extracted from $Im(Y_{G1D})$ and $Im(Y_{G2S})$ after 4-port OpenM3 deembedding. Again, the difference between C_{g1d} and C_{g2s}, that is $C_{g1d} \gg C_{g2s}$ can be explained by the device layout in which G1 to D space is indeed shorter than G2 to S distance. Furthermore, the cross-stage capacitances are much smaller than the in-stage capacitances when put in the same scale for a comparison. It means that the gate to S/D coupling across different devices is reduced as compared with those in the same device. **Fig. 4.13** makes a comparison between cross-stage gate capacitances and total gate capacitances C_{gg1} and C_{gg2}. It demonstrates similar trend between M1 and M2 but some differences in the magnitude and ratio, that is $C_{gg1} > C_{gg2}$, $C_{g1d} > C_{g2s}$, $C_{g1d}/C_{gg1} < 25\%$, and $C_{g2s}/C_{gg2} < 15\%$. **Fig. 4.14** indicates the inter-gate capacitances C_{g1g2} extracted from $Im(Y_{G1G2})$ also after 4-port OpenM3 deembedding. As expected, the magnitude is much smaller than in-stage gate capacitances and the weighting factor in the total gate capacitance is around 13~18% over the frequencies 1~40GHz. Again, the increase of C_{gg1}, C_{gg2}, and C_{g1g2} at higher frequency suggests the influence from parasitic inductances at all of the four terminals, which were not eliminated because short deembedding was not available. **Fig. 4.15** presents the inter-stage capacitances C_{g1d1} and C_{g2s2} calculated by (4.13) and (4.14) in which all of the other gate capacitances can be extracted from (4.5)~(4.12) for dual-gate MOSFET. Interestingly, C_{g1d1} and C_{g2s2} show minor difference in the magnitude and nearly the same frequency dependence, i.e. the higher frequency the smaller capacitance, which is in an opposite trend with that of in-stage, inter-gate, and total gate capacitances. At very low frequency, the ratio between the inter-stage capacitances in-stage capacitances, i.e. C_{g1d1}/C_{g1s} and C_{g2s2}/C_{g2d} are around 25~33%. It explains why the total gate capacitance of M1 and M2, i.e. C_{gg1} and C_{gg2} in a dual-gate MOSFET can be effectively reduced as compared to the single MOSFET.

Regarding the gate to body capacitance C_{gb}, which can be extracted from $Im(Y_{GB})$ of common gate cascode structure, the results are shown in **Fig. 4.16** with a comparison with that measured from single MOSFET. The C_{gb} measured from the common gate cascode structure,

denoted as $C_{gb}(G1+G2)$ is around two times that of single MOSFTE, i.e. $C_{gb}(G1+G2) \sim 2C_{gb}$. Note that the major difference happens at very low frequency where $C_{gb}(G1+G2)$ extracted from the common gate structure reveals a drastic increase but that of single MOSFET keeps much more flat with minor increase. It is suspected that the increase of $C_{gb}(G1+G2)$ at very low frequency may be originated from the coupling from the gate through the inter-stage region, i.e. merged S/D diffusion (floating without contacts), then through the junction between merged S/D and body, and eventually to the body. Further effort is required to explore and clarify the mechanism. The layout of dual-gate MOSFET shown in **Fig. 4.17** with the layers remarked for the contacts to gate, drain, body, and deep n-well (DNW) indicates that C_{gb} can be contributed from the inter-metal coupling capacitance via metal-3 (M3) on the gate contacts to metal-4 (M4) on body contacts. **Fig. 4.18**demonstrates the junction capacitances C_{js} and C_{jd} extracted from $Im(Y_{BS})$ and $Im(Y_{BS})$, which were measured from the common gate cascode structure at off state. Again, C_{js} and C_{jd} are very close to each other and both reveal a drastic fall off with increasing frequency. This strong frequency dependence can be explained by body resistance network effect. **Fig. 4.19** makes a comparison of the total gate capacitances between the dual-gate MOSFET, common gate structure, and single MOSFET. The results indicate a close match between $C_{gg1}+C_{gg2}$ for dual-gate MOSFET and C_{gg_CG} for common gate structure. This consistency validates the accuracy of the gate capacitances determined by the extraction method and flow developed in this thesis. One more important point is that the total gate capacitance of dual-gate MOSFET is significantly smaller than twice that of single MOSFET, i.e. $C_{gg1}+C_{gg2} < 2C_{gg}$, as shown in **Fig. 4.19**. This feature manifests the advantage of dual-gate MOSFET in suppressing Miller effect and the benefit in high frequency performance. **Fig. 4.20** demonstrates the comparison of in-stage gate capacitances C_{g1s} and C_{g2d}, between measurement and simulation with and without parasitic inductances. As shown in **Fig. 4.20(a)**, the simulation employing $L_g=L_d=L_s=L_b=70pH$ can predict the increase of C_{g1s} and C_{g2d} at higher frequency and fit the measured data up to 40

GHz. On the other hand, the simulation without parasitic inductances shown in **Fig. 4.20(b)** indicates nearly a constant over the higher frequency up to 40 GHz. The verification by simulation proves the impact from parasitic inductances at higher frequency. **Fig. 4.21(a)** shows the gate resistances R_{g1} and R_{g2} of dual-gate MOSFET, extracted by Y-method given by (4.17) and (4.18). Both R_{g1} and R_{g2} approach a constant at sufficiently high frequency (f >20GHz) and this frequency dependence can be reproduced by simulation as shown in **Fig. 4.21(b)**. In this work, R_{g1} and R_{g2} associated with G1 and G2 of the dual-gate MOSFET are around 15Ω, which is more than two times higher than that of single MOSFET. Referring to **Table 4.2**, Single-end contacts to the multi-finger poly gate fingers is considered the major cause responsible for the dramatic increase of R_g compared to that of standard multi-finger MOSFET in which two-end gate contacts are employed. The higher R_g will impose significant impact on f_{max} and NF_{min}, and an appropriate revision on the gate contacts layout is indispensable to eliminate the impact on mentioned high frequency performance.
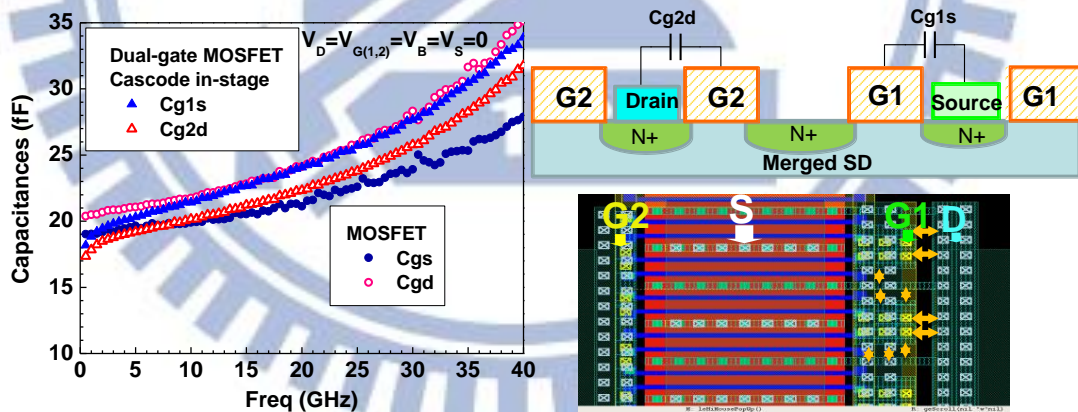
Fig. 4.11 The in-stage gate capacitances C_{g1s} and C_{g2d} extracted from $Im(Y_{G1S})$ and $Im(Y_{G2D})$ of dual-gate MOSFET at off state. C_{gs} and C_{gd} of the standard MOSFET (W2N32) are provided for a comparison.
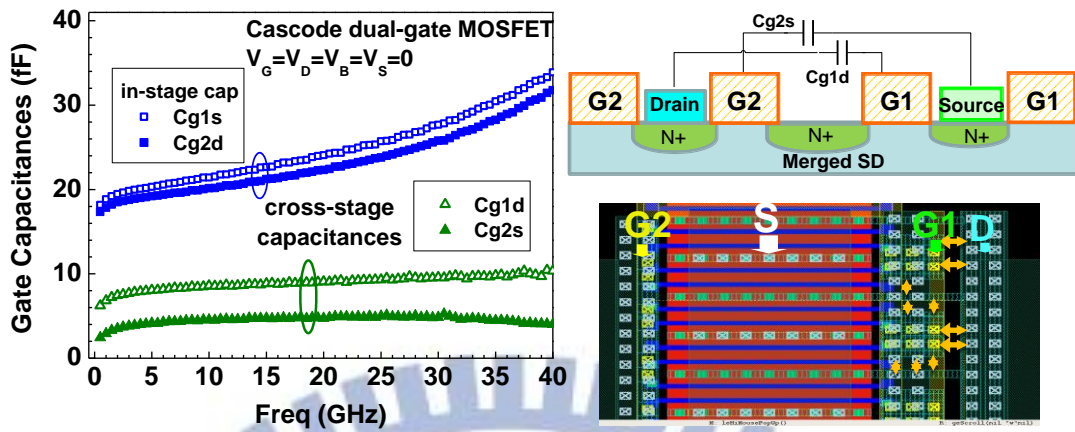
Fig. 4.12 The cross-stage gate capacitances C_{g1d} and C_{g2s} extracted from $Im(Y_{G1D})$ and $Im(Y_{G2S})$ of dual-gate MOSFET at off state. In-stage capacitance C_{g1s} and C_{g2d} of the same device are provided for a comparison.
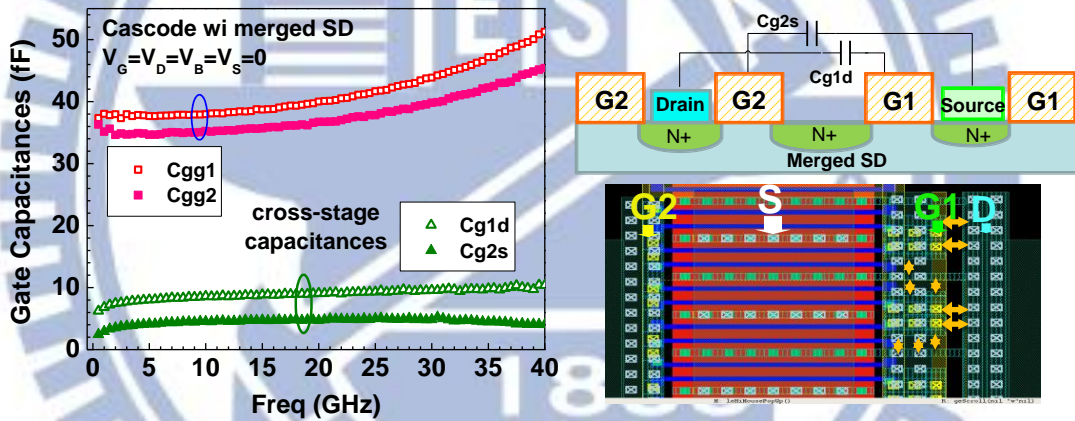
Fig. 4.13 The cross-stage gate capacitances C_{g1d} and C_{g2s} extracted from $Im(Y_{G1D})$ and $Im(Y_{G2S})$ of dual-gate MOSFET at off state. The total gate capacitances C_{gg1} and C_{gg2} associated with G1 and G2 of this dual-gate MOSFET are provided for a comparison.
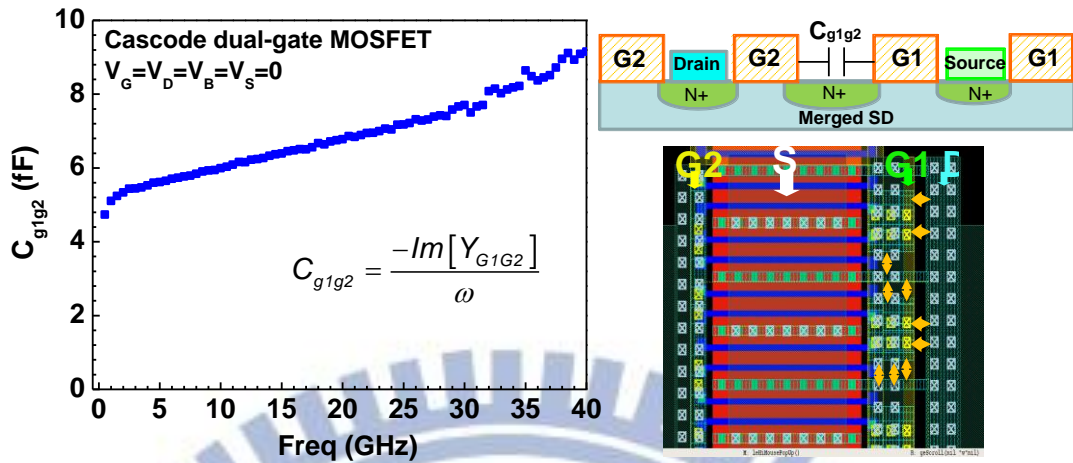
Fig. 4.14 The inter-gate capacitances C_{g1g2} extracted from $Im(Y_{G1G2})$ of dual-gate MOSFET at off state ($V_{G1}= V_{G2}= V_D= V_S= V_B=0$).
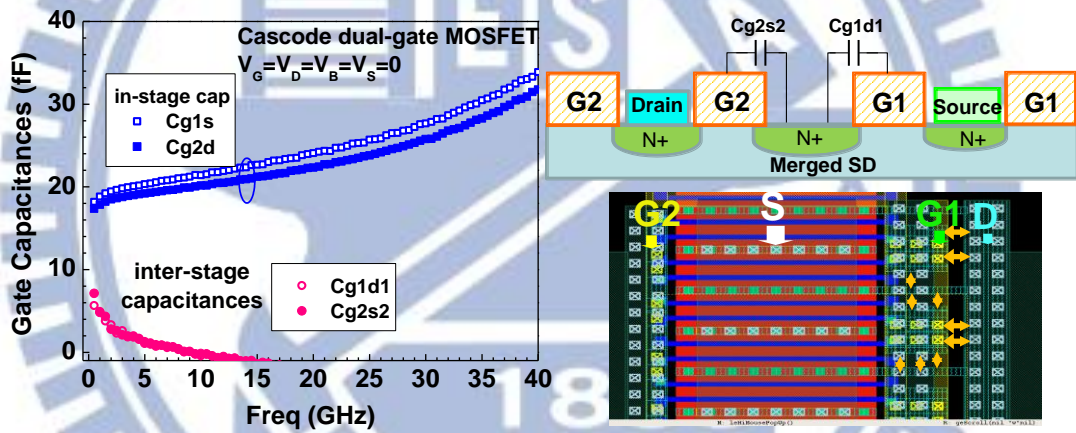
Fig. 4.15 The inter-stage gate capacitances C_{g1d1} and C_{g2s2} calculated by (4.13) and (4.14) with all of the other gate capacitances extracted from (4.5)~(4.12) for dual-gate MOSFET at off state. In-stage capacitance C_{g1s} and C_{g2d} of the same device are provided for a comparison.
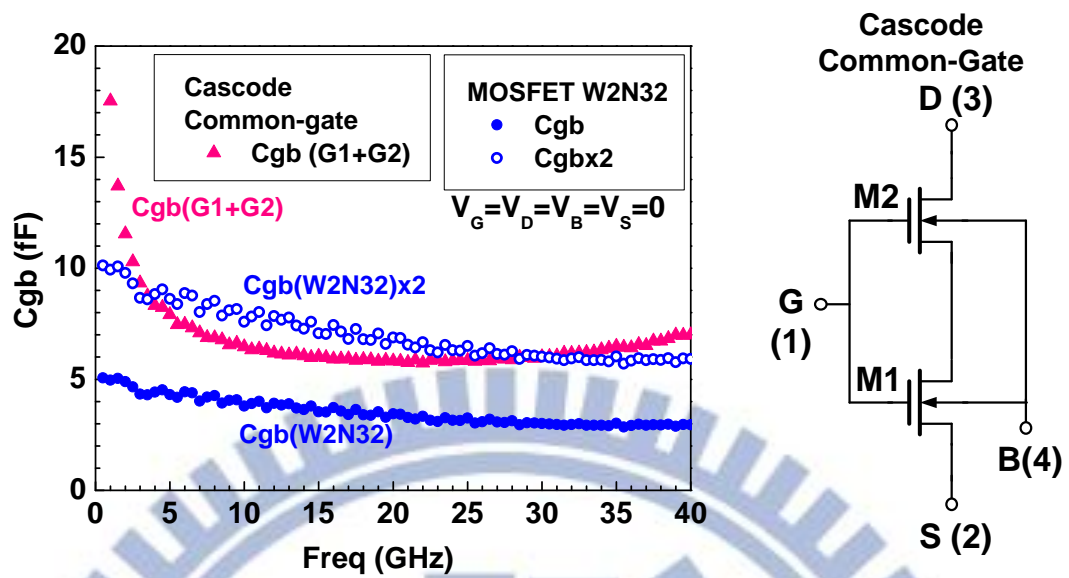
Fig. 4.16 The gate to body capacitance C_{gb} extracted from $Im(Y_{GB})$ of common gate cascode structure at off state($V_G = V_D = V_S = V_B = 0$) and the comparion with C_{gb} measured the standard MOSFET (W2N32).
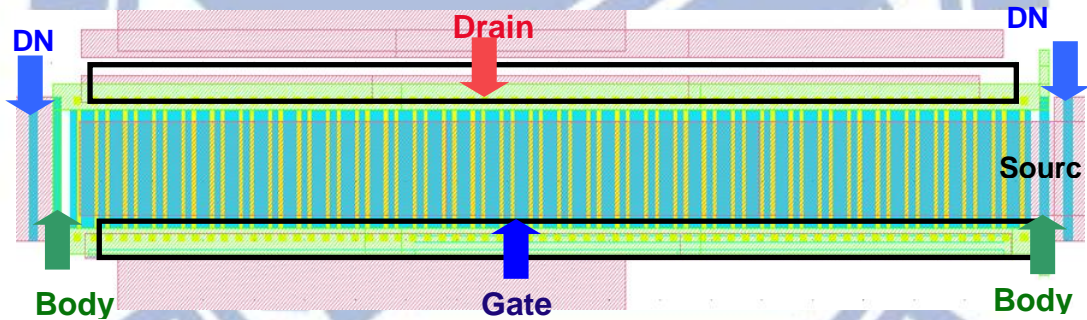
Fig. 4.17 The layout of dual-gate MOSFET with the layers remarked for the contacts to gate, drain, body, and deep n-well (DNW). C_{gb} can be contributed from the inter-metal coupling capacitance : metal-3 (M3) on the gate contacts to metal-4 (M4) on body contacts.

145
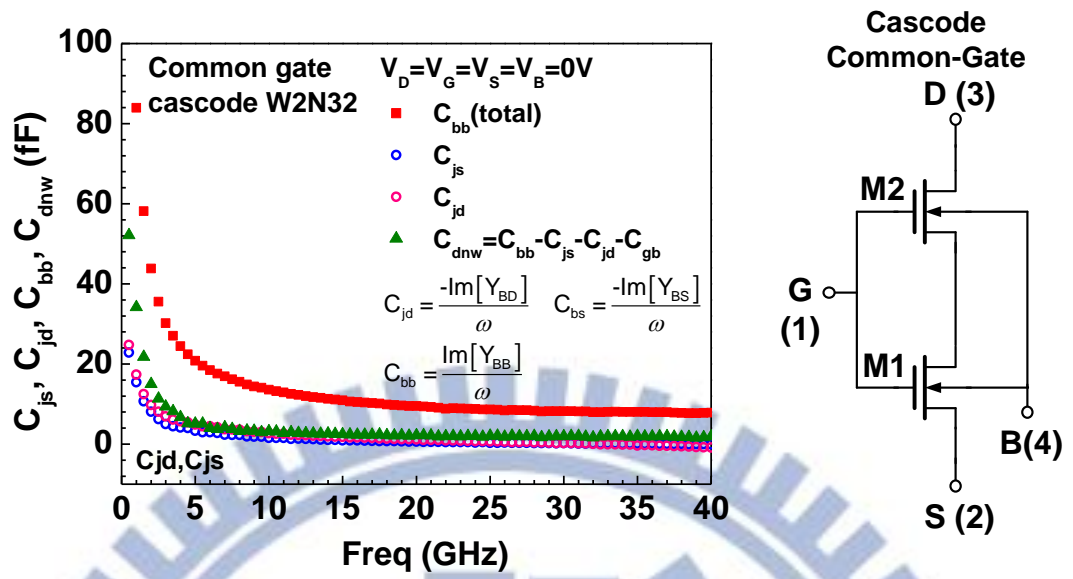
Fig. 4.18 The junction capacitances C_{js} and C_{jd} extracted from $Im(Y_{BS})$ and $Im(Y_{BS})$ of common gate cascode structure at off state.
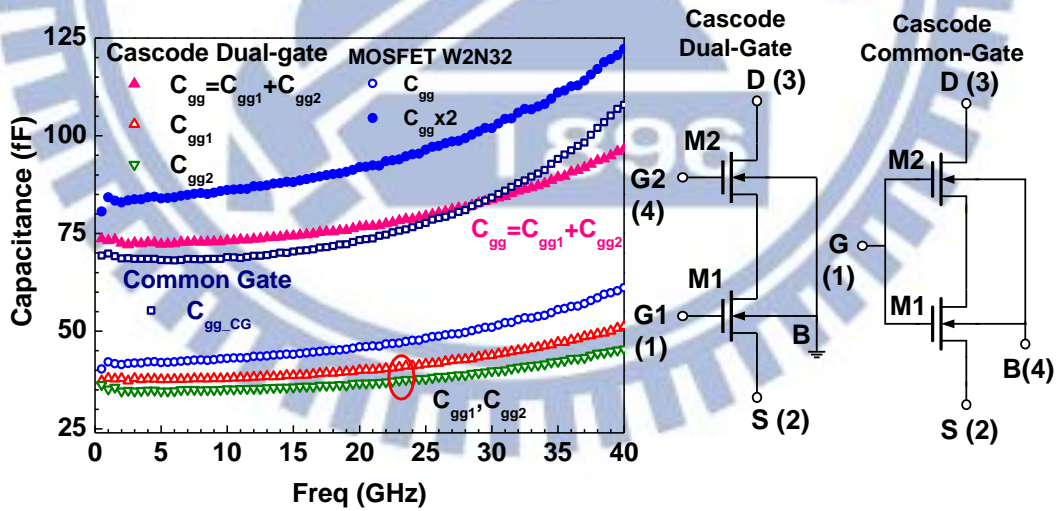
Fig. 4.19 The comparison of total gate capacitances measured from dual-gate MOSFET (C_{gg1} +C_{gg2}), common gate MOSFET (C_{gg_CG}) and single MOSFET at off state.
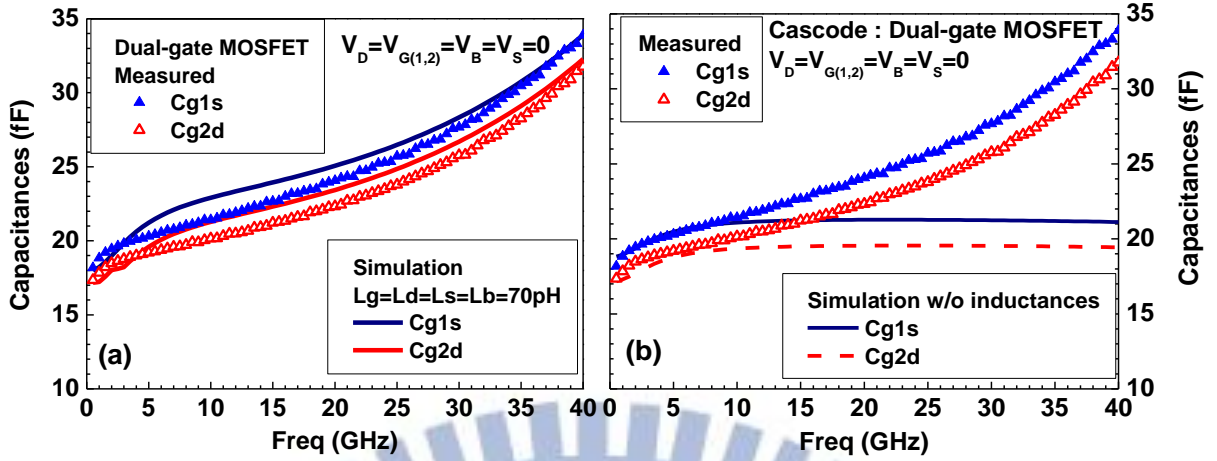
Fig. 4.20 The comparison between the extracted in-stage gate capacitances C_{g1s} and C_{g2d} and those simulated with and without parasitic inductances (a) simulation with $L_g = L_d = L_s = L_b$ = 70pH (b) simulation without inductance.
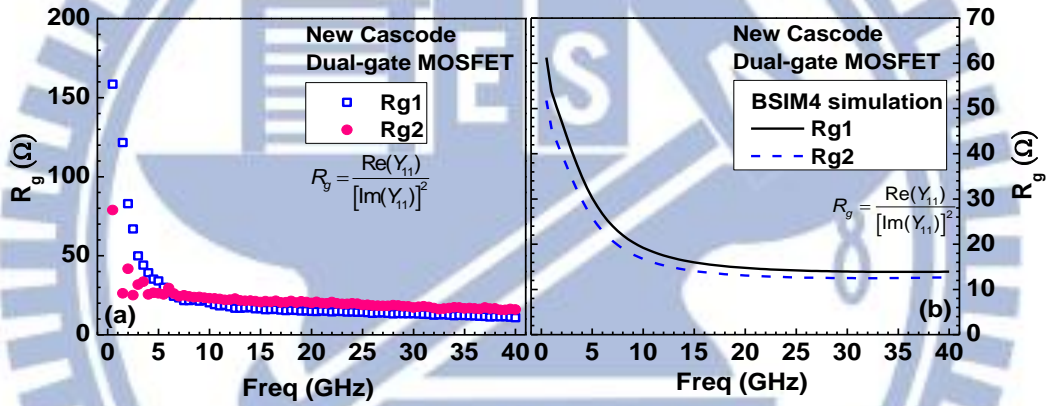
Fig. 4.21 The gate resistances of a dual-gate MOSFET (a) R_{g1} and R_{g2} extracted by Y-method (b) the comparison with simulation (BSIM4).

Table 4.3 summarizes a complete set of small signal equivalent circuit model parameters determined by the extraction method and flow, which have been developed for the dual-gate MOSFET at off state. In the following, an extensive verification on the model accuracy will be carried out through one-by-one comparison between the measurement and simulation by using this small signal equivalent circuit model for all of the 4-port S-parameters after openM3 deembedding. **Fig. 4.22 ~ Fig. 4.25** present the 4-port S-parameters in terms of mag(S_{ij}) (magnitude of S_{ij}) in which i =1, 4, 3, 2 are corresponding to G1, G2, D, and S, respectively. The results demonstrate good match between measurement and simulation over

147

the frequencies up to 40 GHz. As for the phase(S_{ij}) shown in **Fig. 4.26 ~ Fig. 4.29**, a good

match with the measurement can be achieved by simulation for phase(S_{ii}), i=1, 4, phase(S_{4i}),

i=1,3,4, phase(S_{21}), and phase(S_{34}) but leaving the other terms suffering larger deviation. The

mismatch becomes particularly large for phase(S_{42}), phase(S_{24}), phase(S_{31}) and phase(S_{31}),

which are all of the cross-stage parameters. The results suggest required improvement on both

model accuracy and 4-port S-parameters measurement as well as deembedding**.**

Table 4.3 A complete set of small signal equivalent circuit model parameters of dual-gate
MOSFET at off state

Capacitances	fF	Resistances	Ω
C_{g1s}	19.6	R_{g1}	15
C_{g2d}	20.3	R_{g2}	16
C_{g1d}	6.53	R_d	1
C_{g2s}	2	R_s	1
C_{g1g2}	4.35	R_b	1
C_{g1d1}	7.53	R_{bb1}	70
C_{g2s2}	6.24	R_{bb2}	70
C_{jd1}	12	R_{bb}	700
C_{js1}	22.9	R_{sd_diff}	1
C_{jd2}	22.76	Inductances	pH
C_{js2}	12	L_g	70
C_{g1b}	2.5	L_d	70
C_{g2b}	2.5	L_s	70
		L_b	70
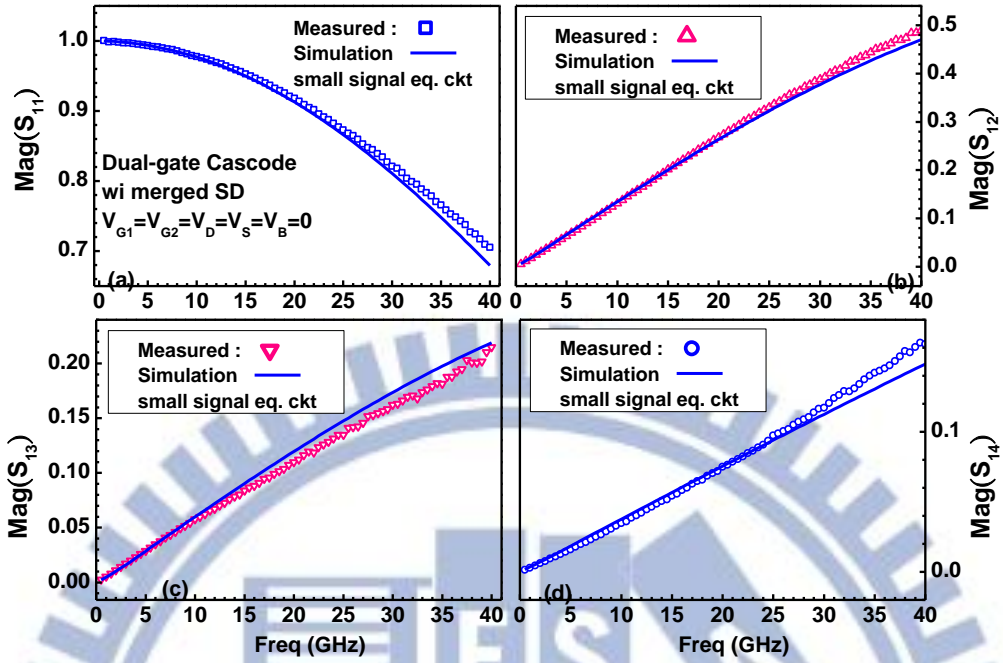
Fig. 4.22 The measured and simulated Mag(S) of dual-gate MOSFET at off state $V_{G1}=$ $V_{G2}=V_D=$ $V_S=$ $V_B=0$ (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
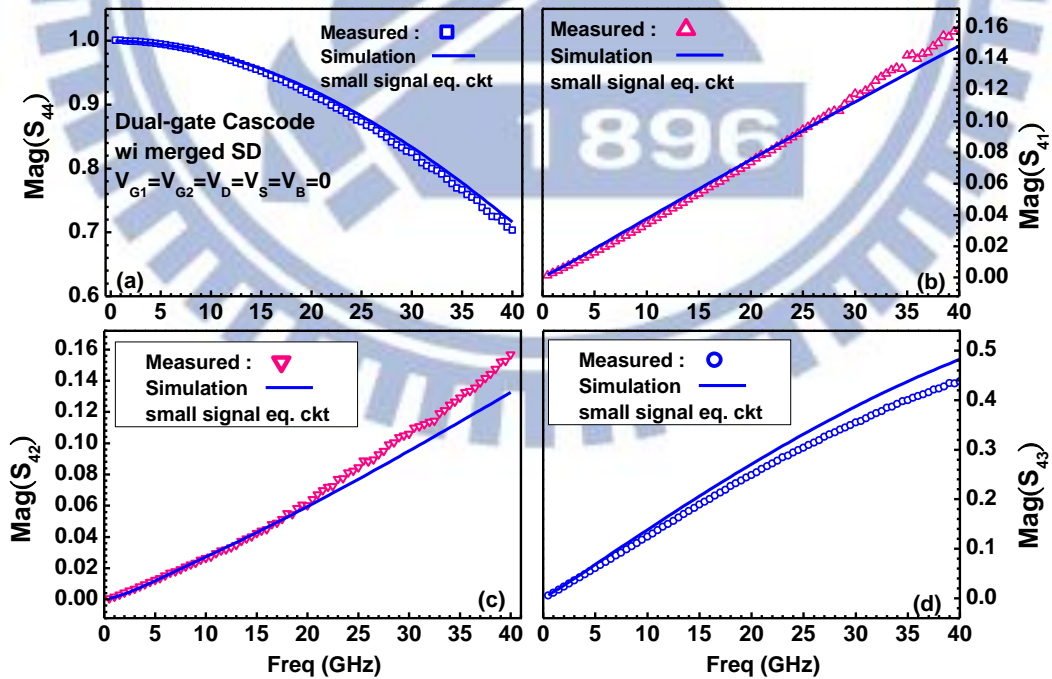
Fig. 4.23 The measured and simulated Mag(S) of dual-gate MOSFET at off state $V_{G1}=$ $V_{G2}=V_D=$ $V_S=$ $V_B=0$ (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
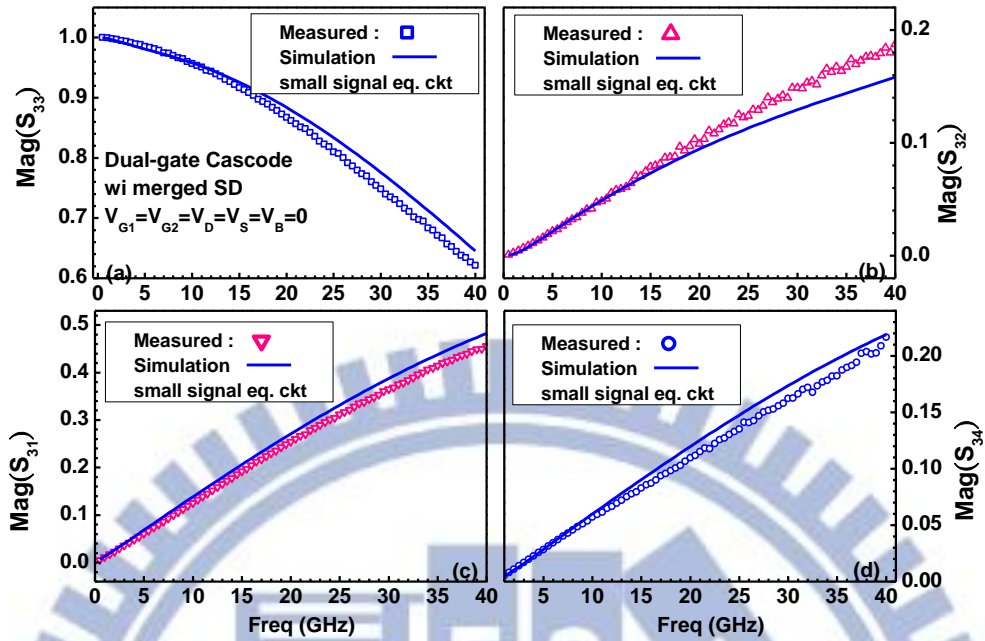
Fig. 4.24 The measured and simulated Mag(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) Mag(S_{33}) (b) Mag(S_{32}) (c) Mag(S_{31}) (d) Mag(S_{34}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

Fig. 4.25 The measured and simulated Mag(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) Mag(S_{22}) (b) Mag(S_{23}) (c) Mag(S_{21}) (d) Mag(S_{24}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

Fig. 4.26 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{11}) (b) phase(S_{12}) (c) phase(S_{13}) (d) phase(S_{14}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

Fig. 4.27 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

151

Fig. 4.28 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{33}) (b) phase(S_{31}) (c) phase(S_{32}) (d) phase(S_{34}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
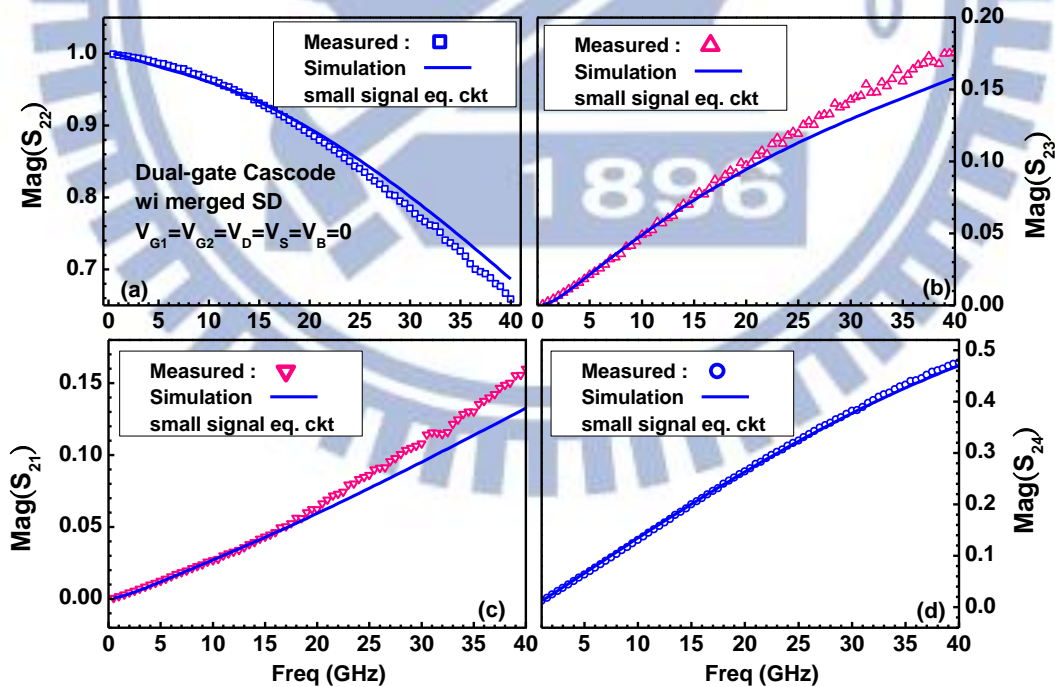

Fig. 4.29 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{22}) (b) phase(S_{24}) (c) phase(S_{23}) (d) phase(S_{21}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

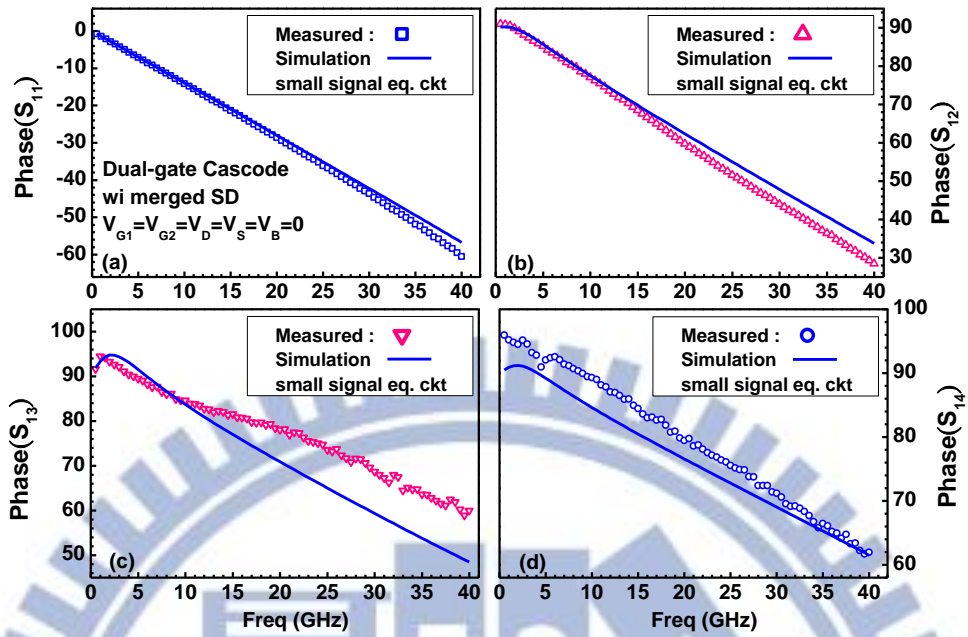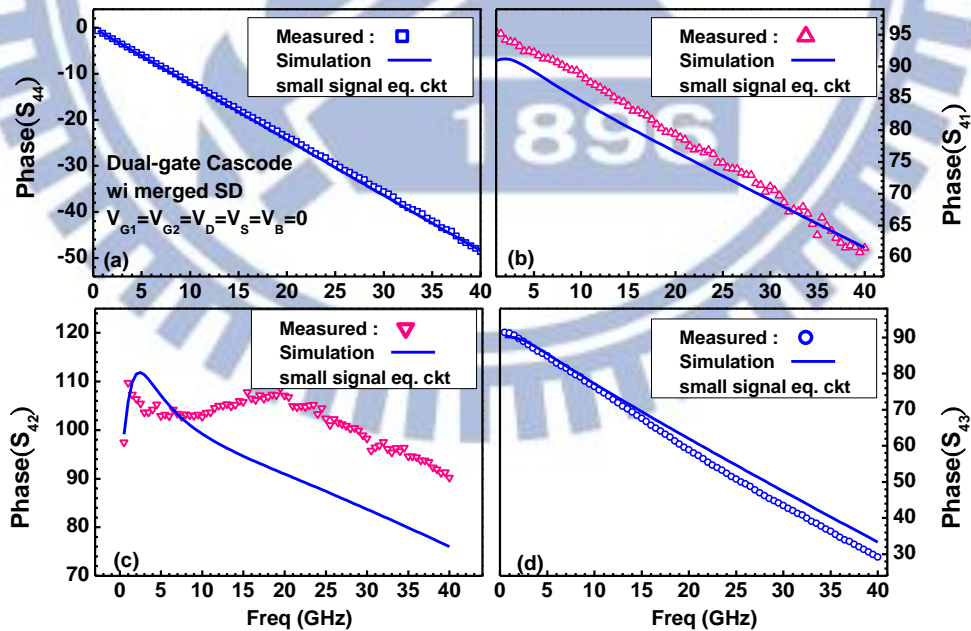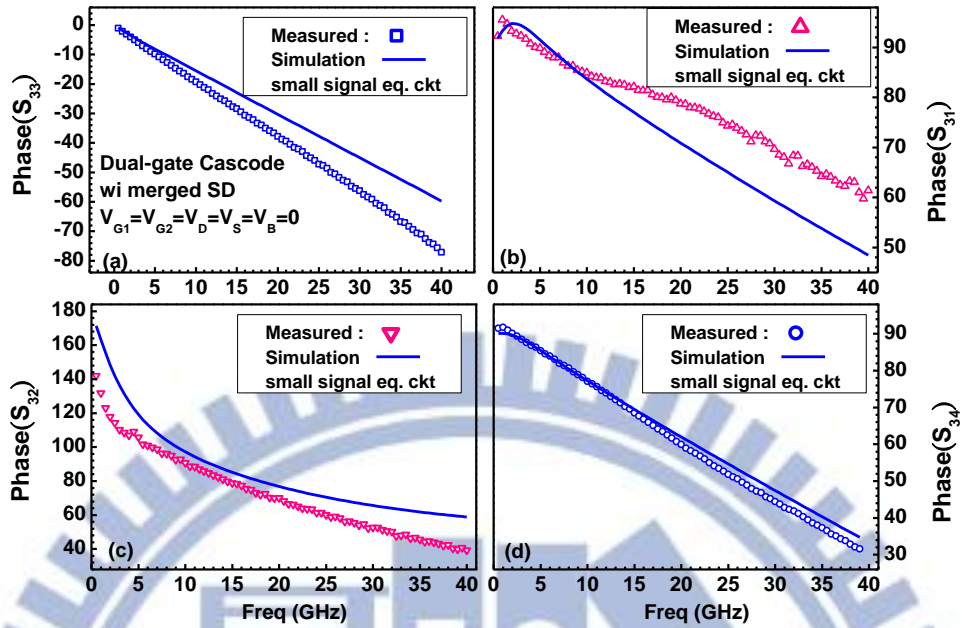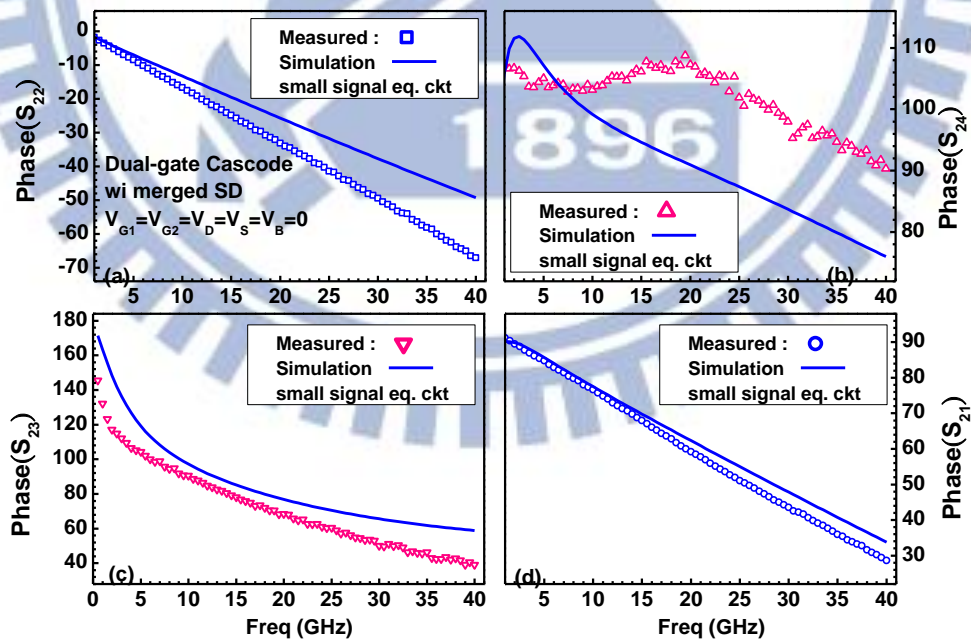### 4.3.2 Small Signal Equivalent Circuit Model of Dual-gate MOSFET at Active State

Referring to **Table 4.1** for the operation modes available for cascode topology, it can be understood that both M1 and M2 operating saturation region, namely saturation- saturation, is the operation mode most favorable for a cascode amplifier. In this section, a small signal equivalent circuit model will be developed and certified for the dual-gate MOSFET at active state, i.e. saturation mode for both M1 and M2.

Fig. 4.30 illustrates the small signal equivalent circuit model proposed for the dual-gate MOSFET at active state. The bias condition for achieving saturation mode for both M1 and M2 is specified as V_{G1}=0.4V, V_{G2}=0.6V, V_D=1.0V, and V_S=V_B=0. Following the extraction method and flow set up for dual-gate MOSFET at off state, the model parameters extraction method can be derived with necessary revision by incorporating transconductances and output resistances, such as g_{m1} and r_{o1} for M1, and g_{m2} and r_{o2} for M2. First, the gate capacitances associated with the core device can be extracted from 4-port S-parameters at active state under the specified bias condition, given by (4.19)~(4.28)

$$C_{gg1} = \frac{Im[Y_{G1G1}]_{active}}{\omega}\Big|_{LF} \tag{4.19}$$

$$C_{g1s} = \frac{-Im[Y_{G1S}]_{active}}{\omega}\Big|_{LF} \tag{4.20}$$

$$C_{g1d} = \frac{-Im[Y_{G1D}]}{\omega}\Big|_{LF} \tag{4.21}$$

$$C_{gg2} = \frac{Im[Y_{G2G2}]_{active}}{\omega}\Big|_{LF} \tag{4.22}$$

$$C_{g2d} = \frac{-Im[Y_{G2D}]_{active}}{\omega}\Big|_{LF} \tag{4.23}$$

$$C_{g2s} = \frac{-Im[Y_{G2S}]}{\omega}\Big|_{LF} \tag{4.24}$$

$$C_{g1g2} = \frac{-Im[Y_{G1G2}]}{\omega}\Big|_{LF} \tag{4.25}$$

C_{gb} can be and extracted from $Im(Y_{GB})$ measured from the common gate structure, **Fig. 4.7(b)**

$$C_{gb} = \frac{-Im[Y_{GB}]_{active}}{\omega}\Big|_{HF}, C_{g1b} = C_{g2b} = \frac{C_{gb}}{2} \tag{4.26}$$

then, the inter-stage gate capacitances can be calculated from all of other gate capacitances determined from (4.19)~(4.26)

$$C_{g1d1} = C_{gg1} - C_{g1s} - C_{g1d} - C_{g1b} - C_{g1g2} \tag{4.27}$$

$$C_{g2s2} = C_{gg2} - C_{g2d} - C_{g2s} - C_{g2b} - C_{g1g2} \tag{4.28}$$

The junction capacitances associated with S/D to B in M1/M2, namely C_{js1} and C_{jd2} can be extracted from $Im(Y_{BS})$ and $Im(Y_{BD})$ measured from common gate structure at active state, as given by (4.29) and (4.30)

$$C_{js1} = \frac{-Im[Y_{BS}]_{active}}{\omega}\Big|_{LF} \tag{4.29}$$

$$C_{jd2} = \frac{-Im[Y_{BD}]_{active}}{\omega}\Big|_{LF} \tag{4.30}$$

Note that the other two junction capacitances in the inter-stage region, i.e. C_{jd1} and C_{js2} cannot be directly extracted from 4-port Y-parameters and have to be calculated based on the bias-dependent junction capacitance model and the voltage drop at the inter-stage region predicted by simulation. Again, all of the capacitances except C_{gb} are extracted from Y-parameters at very low frequency to minimize the effect from parasitic inductances and resistances. The gate resistances associated with M1 and M2, i.e. R_{g1} and R_{g2} are considered weakly dependent on the gate and drain bias and can be approximated by the values at off state as shown in **Table 4.3**.

In the following, the extraction of transconductances and output resistances, such as g_{m1} and r_{o1} for M1, and g_{m2} and r_{o2} for M2, based on $Re(Y_{31}) = Re(Y_{DG1})$ and $Re(Y_{33}) = Re(Y_{DD})$ as follows

$$G_{m(Cascode)} = Re(Y_{DG1})\big|_{LF} \tag{4.31}$$

$$G_{m(Cascode)} = g_{m1} \cdot \frac{g_{m2}r_{o2}}{1 + g_{m2}r_{o2}} \tag{4.32}$$

Assume $g_{m2}r_{o2} \gg 1 \Rightarrow \dfrac{g_{m2}r_{o2}}{1+g_{m2}r_{o2}} \cong 1$

$$G_{m(Cascode)} \cong g_{m1} = Re(Y_{DG1})|_{LF} \qquad (4.33)$$

$$R_{out(Cascode)} = \dfrac{1}{Re(Y_{DD})|_{LF}} \qquad (4.34)$$

$$R_{out(Cascode)} = r_{o2} + r_{o1}(1+g_{m1}r_{o1}) \qquad (4.35)$$

Assume $g_{m2}=g_{m1}$ and $r_{o2}=r_{o1}$ as the initial condition for an iteration cycle to achieve the optimized values for g_{m1}, g_{m2}, r_{o1}, and r_{o2} respectively

$$initial\ condition: r_{o2} = r_{o1}$$

$$\therefore R_{out(Cascode)} \cong r_{o1}(2+g_{m1}r_{o1}) \qquad (4.36)$$

$$r_{o1}(2+g_{m1}r_{o1}) \cong \dfrac{1}{Re(Y_{DD})|_{LF}} \qquad (4.37)$$

The iteration and optimization on r_{o1} and r_{o2} can be performed by best fitting to both $1/Re(Y_{33})$ = $1/Re(Y_{DD})$ and $1/Re(Y_{22}) = 1/Re(Y_{SS})$.

Fig. 4.31 summarize a complete model parameters extraction flow for small signal equivalent circuit model of dual-gate MOSFET at active state ($V_{G1}=0.4V$, $V_{G2}=0.6V$, $V_D=1.0V$, and $V_S=V_B=0$) in which the details of extraction method has been described by (4.19) ~ (4.37). **Table 4.4** summarizes a complete set of small signal equivalent circuit model parameters determined by the extraction method and flow, which have been developed for the dual-gate MOSFET at active state. In the following, an extensive verification on the model accuracy will be carried out through the comparison between the measurement and simulation by using this small signal equivalent circuit model for all of the 4-port S-parameters after openM3 deembedding. First, transcondutance $G_m=Re(Y_{31})$ and output resistance $R_{out}=1/Re(Y_{33})$ are two most important parameters to verify the model accuracy at active state. **Fig. 4.32(a)~(d)** present G_m, R_{out}, and mag(S_{31}) as well as mag(S_{33}) related to the former two parameters. **Fig. 4.33~Fig. 4.36** present the 4-port S-parameters in terms of mag(S_{ij}) (magnitude of S_{ij}) in

which i =1, 4, 3, 2 are corresponding to G1, G2, D, and S, respectively. The results demonstrate good match for mag(S_{ij}), i=1 and 4 but worse deviation for the others, such as mag(S_{ij}), i=2 and 3. As for the phase(S_{ij}) shown in **Fig. 4.37~Fig. 4.40**, a good match with the measurement can be achieved by simulation for most of the parameters, except somewhat larger deviation revealed in phase(S_{13}) and phase(S_{24}), i.e. the cross-stage parameters. This particularly large mismatch happened to those at off state as demonstrated previously. Again, the results suggest required improvement on both model accuracy and 4-port S-parameters measurement as well as deembedding.
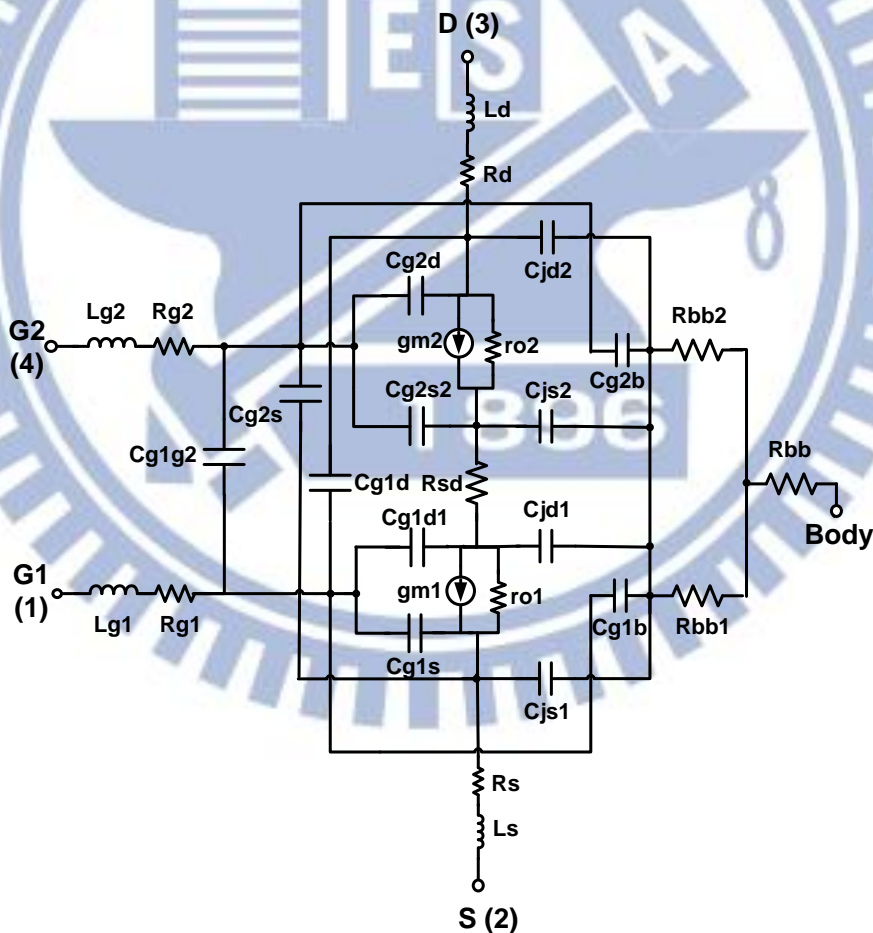
Fig. 4.30 The small signal equivalent circuit model of dual-gate MOSFET at active state. M1 and M2 are operated at saturation mode and the channel conduction is modeled by g_{m1} and r_{o1} for M1 and g_{m2} and r_{o2} for M2.
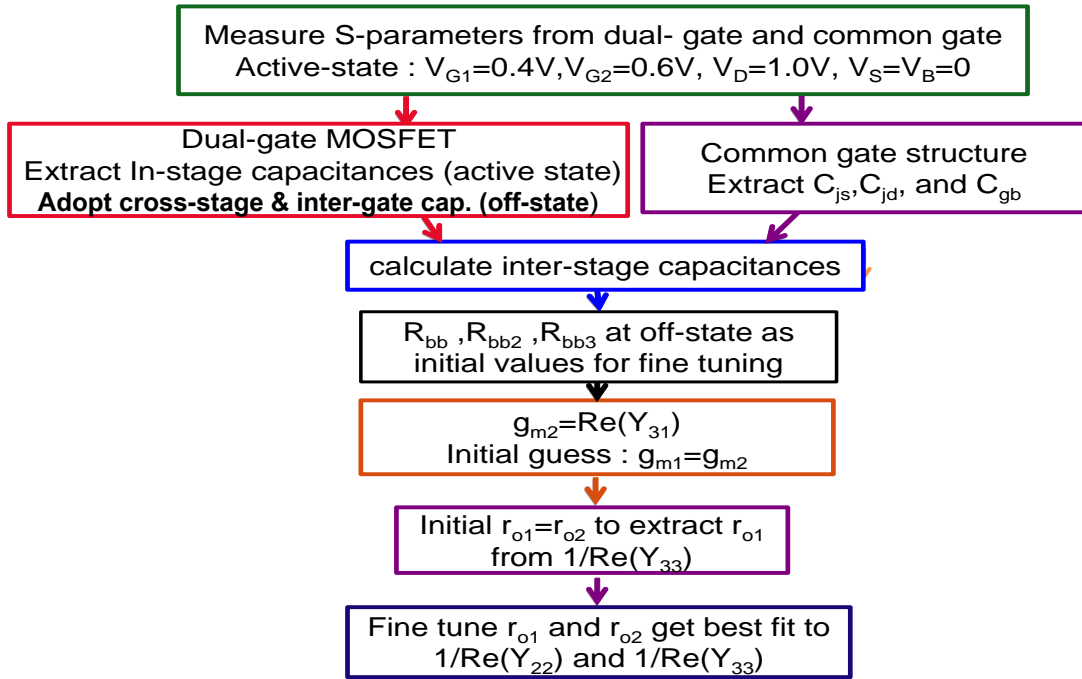
Fig. 4.31 Model parameters extraction flow for small signal equivalent circuit model of dual-gate MOSFET at active state

Table 4.4 A complete set of small signal equivalent circuit model parameters of dual-gate MOSFET at active state(V_{G1}=0.4V, V_{G2}=0.6V, V_D=1.0V, and V_S=V_B=0)

Capacitances	fF	Resistances	Ω	Inductances	pH
C_{g1s}	34.54	R_{g1}	15	L_g	70
C_{g2d}	18.3	R_{g2}	16	L_d	70
C_{g1d}	7.53	R_d	1	L_s	70
C_{g2s}	2	R_s	1	L_b	70
C_{g1g2}	6.35	R_b	1	transconductance	mA/V
C_{g1d1}	6.53	R_{bb1}	70	g_{m1}	20
C_{g2s2}	22.24	R_{bb2}	70	g_{m2}	26
C_{jd1}	8.94	R_{bb}	700	R_{out}	Ω
C_{js1}	22.4	R_{sd_diff}	1	r_{o1}	206
C_{jd2}	17.6			r_{o2}	256
C_{js2}	8.94				
C_{g1b}	2.5				
C_{g2b}	2.5				
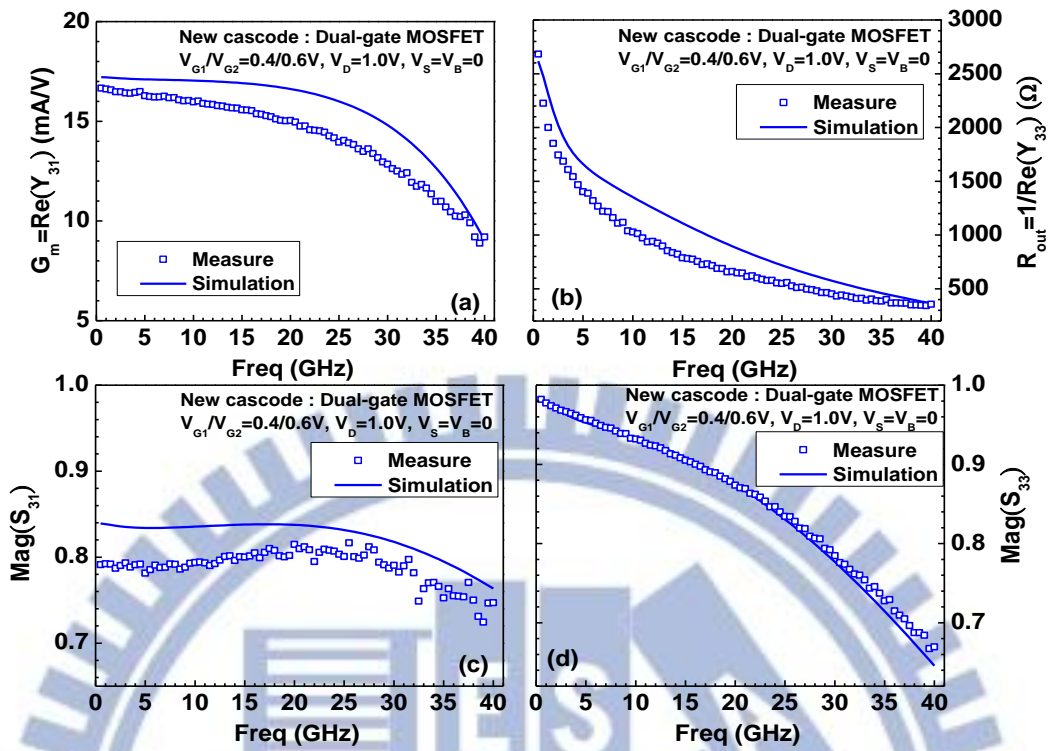
Fig. 4.32 The comparison of measurement and simulation for dual-gate MOSFET at active state V_{G1}=0.4V, V_{G2}=0.6V, V_D=1.0V, V_S= V_B=0 (a) G_m=Re(Y_{31}) (b) R_{out}=1/Re(Y_{33}) (c) Mag(S_{31}) (d) Mag(S_{33}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
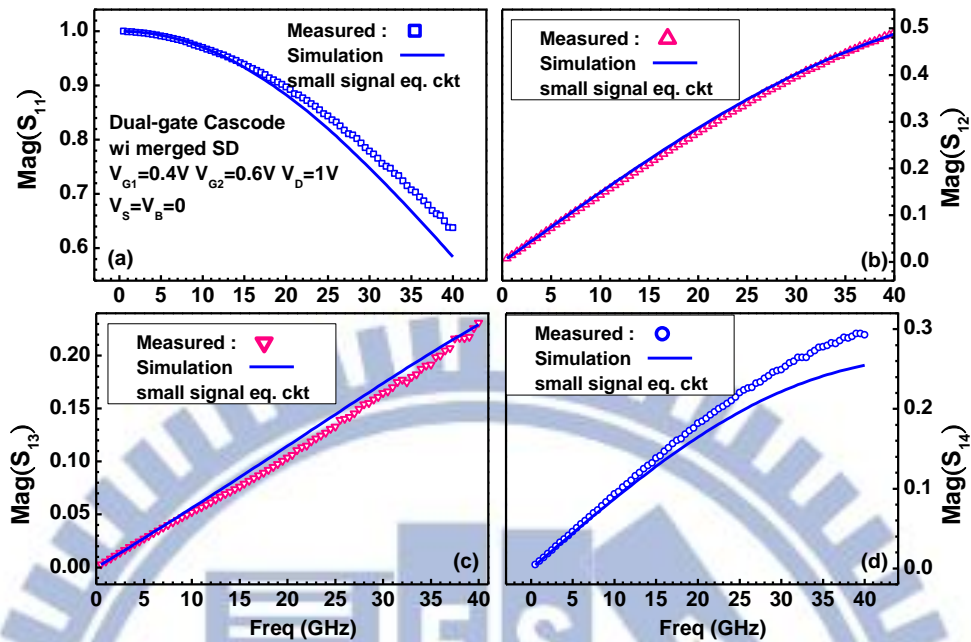
Fig. 4.33 The measured and simulated Mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
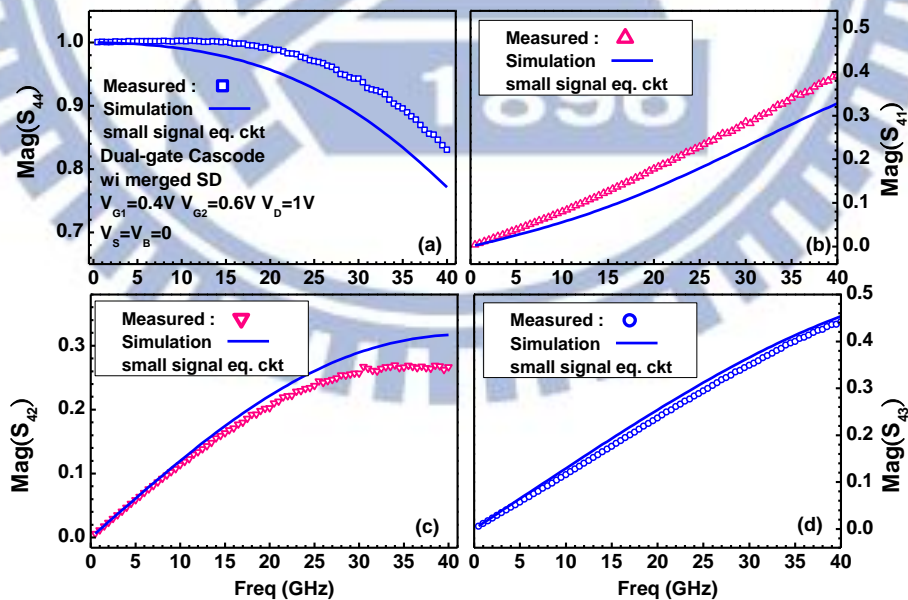
Fig. 4.34 The measured and simulated Mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
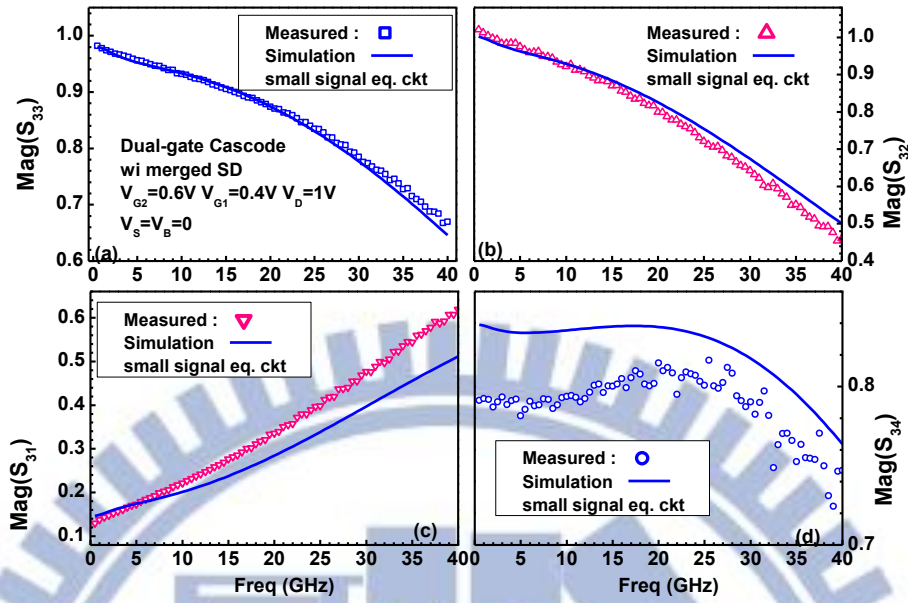
Fig. 4.35 The measured and simulated Mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{33}) (b) Mag(S_{32}) (c) Mag(S_{31}) (d) Mag(S_{34}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

Fig. 4.36 The measured and simulated Mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{22}) (b) Mag(S_{23}) (c) Mag(S_{21}) (d) Mag(S_{24}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
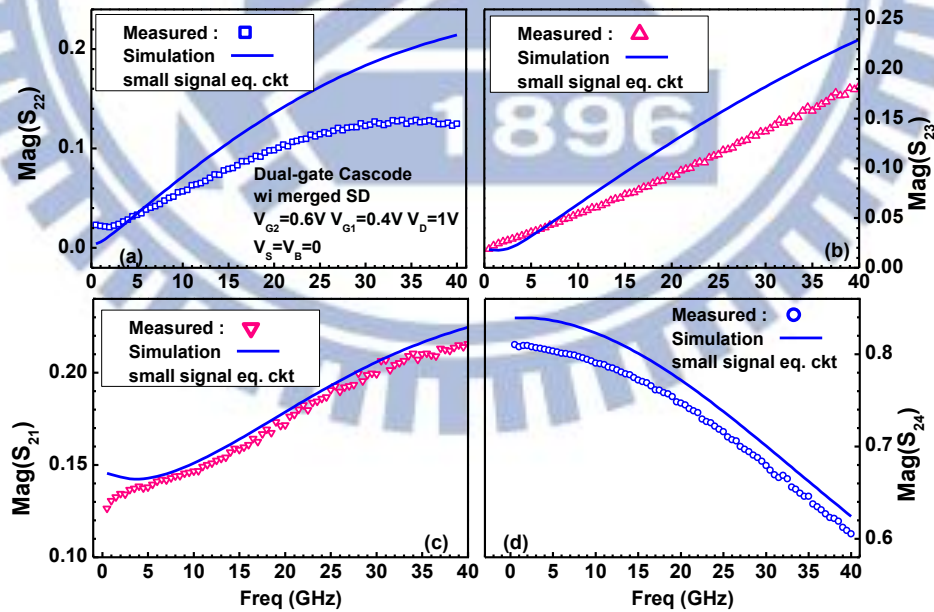
160

Fig. 4.37 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{11}) (b) phase(S_{12}) (c) phase(S_{13}) (d) phase(S_{14}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
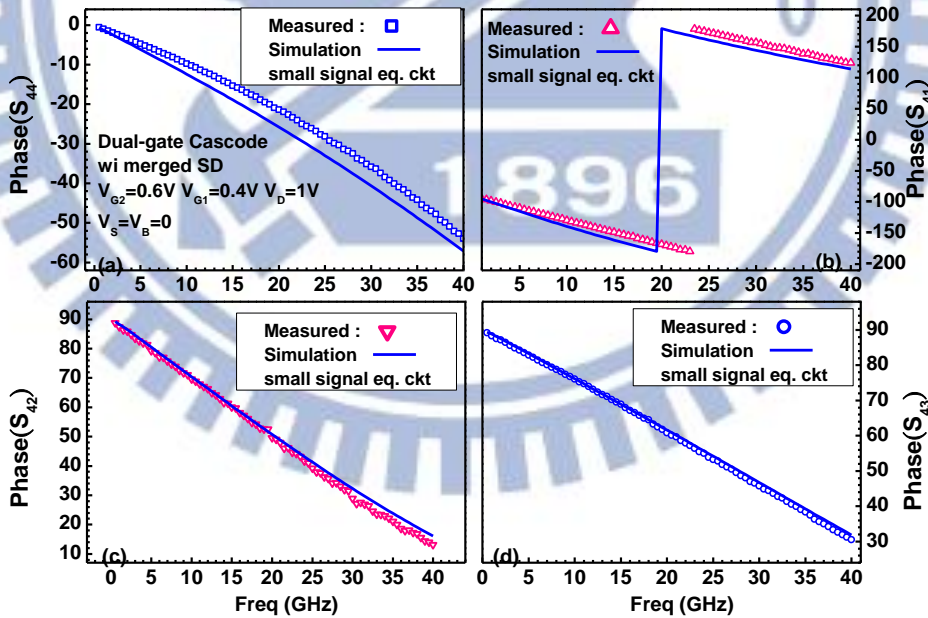
Fig. 4.38 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.
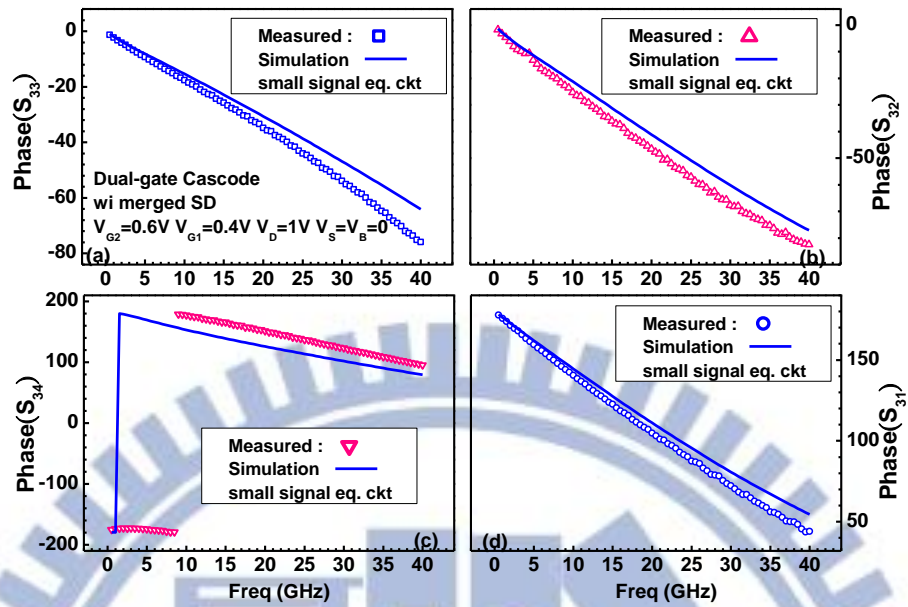
Fig. 4.39 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{33}) (b) phase(S_{31}) (c) phase(S_{32}) (d) phase(S_{34}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

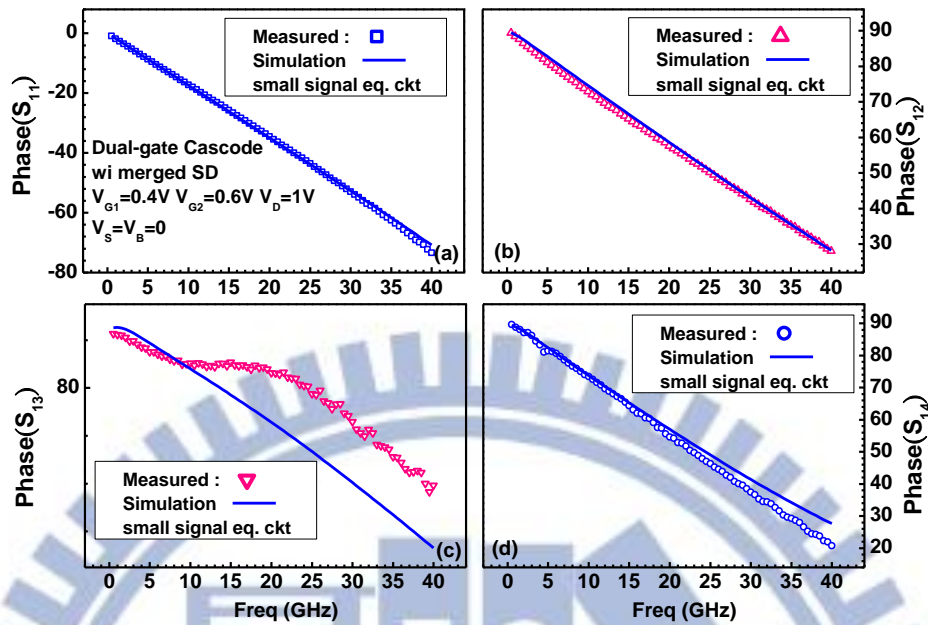**Fig. 4.40** The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{22}) (b) phase(S_{24}) (c) phase(S_{23}) (d) phase(S_{21}). Symbols : measurement. Lines : simulation by small signal equivalent circuit with body network model.

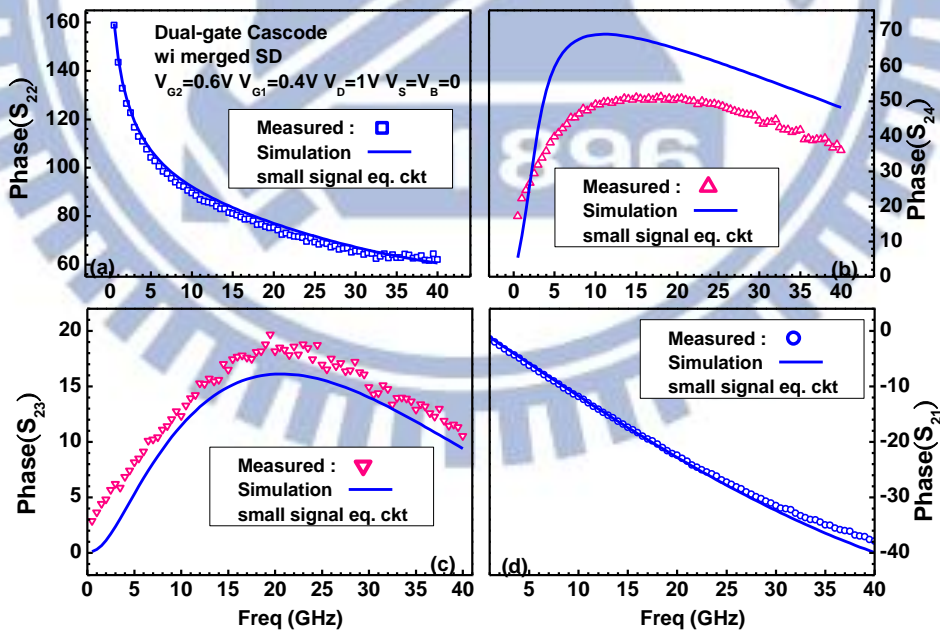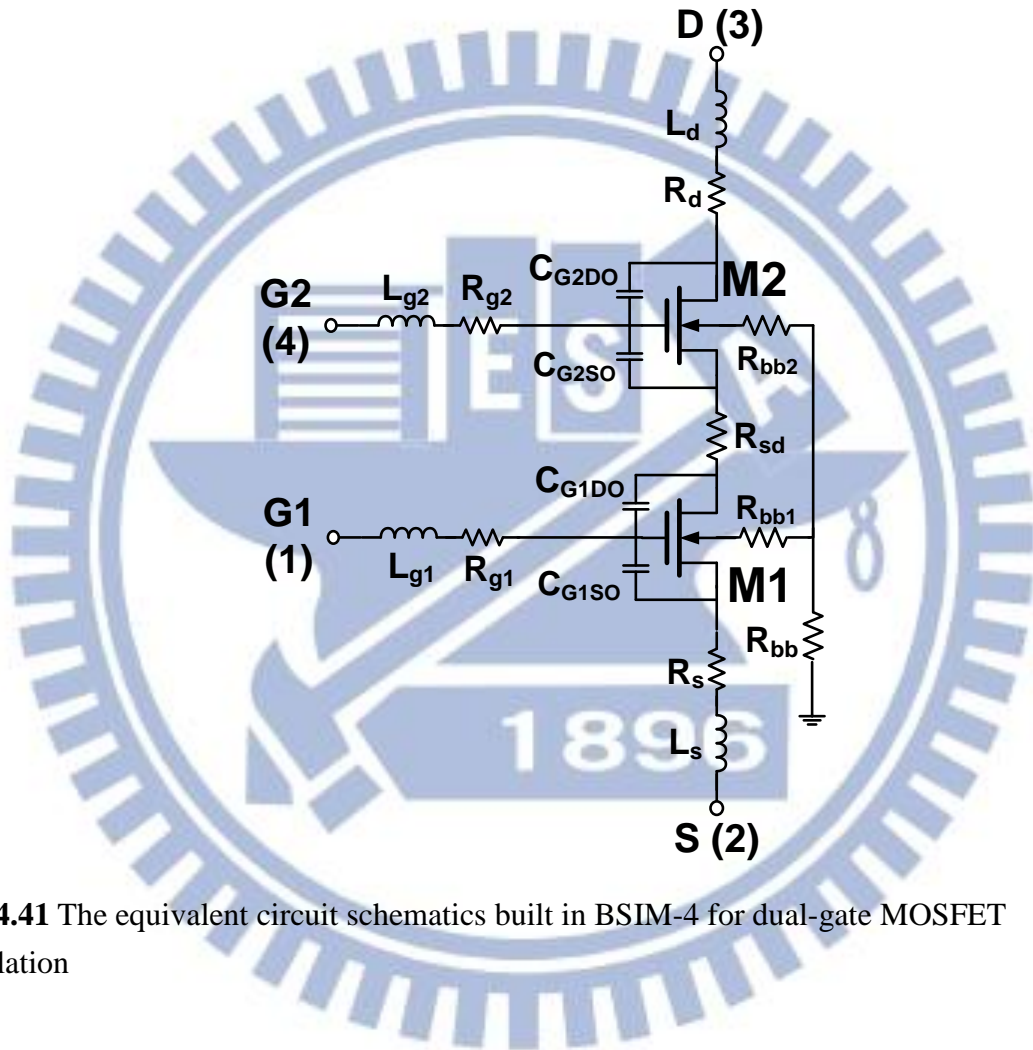## 4.4　Dual-gate MOSFET Simulation by BSIM-4 with Parasitic RLC Parameters

The small signal equivalent circuit models are useful for high frequency simulation at circuit level but reveal the intrinsic limitation in I-V simulation over a full range of bias condition from off state, through linear region, and to saturation region. BSIM-4 is recognized a useful simulation tool to meet the requirement for both I-V and C-V simulation. However, all of the device simulation tools including BSIM-4 are limited to single device and cannot be directly applied to dual-gate MOSFET without any modification. In this thesis, an appropriate modification on BSIM-4 by incorporating parasitic RLC elements, which may be originated from the metal and contact resistances for interconnection lines and and sheet resistance associated with S/D region even without contacts like merged S/D region.

4.4.1　BSIM-4 I-V Simulation for Dual-gate MOSFET

Referring to **Table 4.1** for various operation modes, which can exist in a cascode structure based on different combination of bias conditions applied to M1 and M2. According to a simple circuit schematics of cascode as shown in **Fig. 4.1**, the supply voltage applied to the drain node, i.e. V_{DD} is distributed between M1 and M2. It can be understood that the increase of V_{G1} in M1 will lead to lower drain voltage (V_{D1}) and may drive M1 into linear region. Under the condition that M1 is driven into linear region, this cascode amplifier will suffer lower current and gain degradation. The increase of V_{DD} may offer higher V_{D1} to keep M1 operate in saturation region but the increase of V_{DD} is limited by junction breakdown and gate oxide breakdown, which impose more damage to M2 at off state (i.e., $V_{G2}=0$ for common gate). Due to the limitation to V_{G1} and V_{DS1} available from V_{DD}, it allow limited room for M1 to operate under the optimized bias condition with $g_{m,max}$. In the following, BSIM-4 with I-V model for V_T, mobility, and short channel effects (refer to chapter 3 for more details) is employed to perform I-V simulation for dual-gate MOSFET.

Fig. 4.41 illustrates the equivalent circuit schematics built in BSIM-4 for dual-gate

MOSFET simulation. **Table 4.5** summarized the key model parameters specified in BSIM-4 for I-V, C-V, and high frequency simulation. First, for I-V simulation, the primary difference in the model parameters from those of standard MOSFET is the adoption of series resistance at the merged S/D region, namely $R_{ds,diff}$, which cannot be avoided from dual-gate MOSFET and may have significant impact on current drivability.


Fig. 4.41 The equivalent circuit schematics built in BSIM-4 for dual-gate MOSFET simulation

Table 4.5 The equivalent circuit model parameters of dual-gate MOSFET set up in BSIM-4 for I-V, C-V, and high frequency simulation

| Resistances	Ω	Inductances	pH
R_{g1}	15	L_g	70
R_{g2}	16	L_d	70
R_d	1	L_s	70
R_s	1	L_b	70
R_b	1	BSIM4 C-V model	pF
R_{bb1}	70	CGSO : M1/M2	52/0
R_{bb2}	70	CGDO : M1/M2	0/52
R_{bb}	700	CGSL : M1/M2	100/50
R_{sd_diff}	1	CGDL : M1/M2	50/100

Fig. 4.42 makes a comparison between the measured and simulated I_{DS}-V_{DS} under fixed V_{G2} =1.0V and varying V_{G1} (0.2~1.2V). The results indicate very good match with measurement over the wide range of bias condition and prove BSIM-4 I-V model accuracy after calibration. The I-V characteristics reveals gradual saturation of I_{DS} then g_m degradation when further increasing V_{G1} beyond 0.8V. The result specific to dual-gate MOSFET suggest that the increase of V_{G1} will eventually push M1 into linear region so that the I_{DS} flowing through M1 and M2 is controlled by V_{G2} rather than V_{G1}. To verify the interesting operation schemes specific to dual-gate MOSFET, simulation was performed under different combination of V_{G1} and V_{G2}. **Fig. 4.43**(a) demonstrates simulated I_{DS}-V_{DS} under fixed V_{G2} =1.0V and sweeping V_{G1}. On the other hand, **Fig. 4.43**(b) shows the simulated results under fixed V_{G1}=1.0V and sweeping V_{G2}. **Fig. 4.43**(a) and (b) indicate very different results and justifes the mentioned comments. The I_{DS} saturation and g_m degradation revealed in **Fig. 4.43(a)** under fixed V_{G2} can be solved by exchanging the role of V_{G1} and V_{G2}, as shown in **Fig. 4.43** (b). Similar results are achieved when reducing the fixed gate bias to 0.6V as shown in **Fig. 4.44**. The important conclusion achieved from this verification is that V_{G2} for M2 is the gate bias, which can have effective modulation on I_{DS} even M1 is operated into linear region.
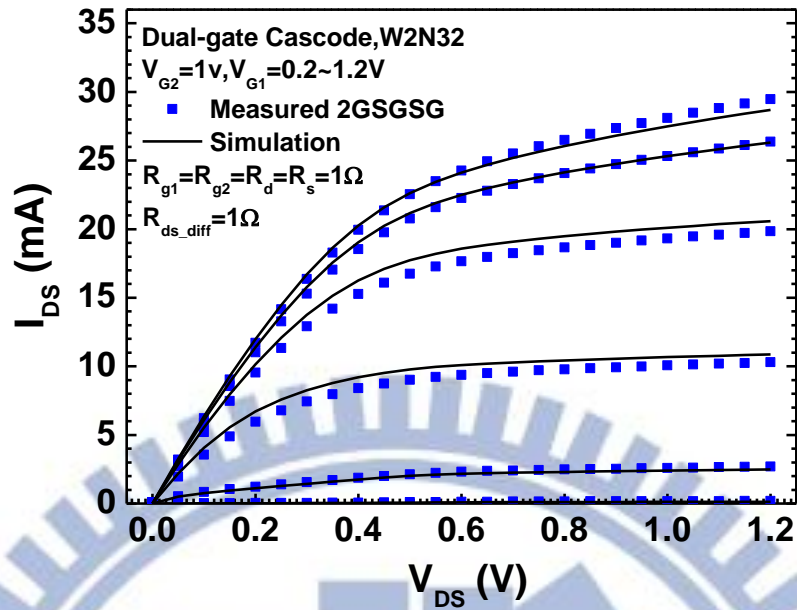
Fig. 4.42 The measured and simulate I_{DS}-V_{DS} of dual-gate MOSFET under V_{G2}=1.0V and varying V_{G1}=0.2~1.2V. R_{g1}= R_{g2}= R_d= R_s=1Ω for 4 terminals, $R_{ds,diff}$=1Ω for merged S/D region. Symbols : measurement. Lines : BSIM-4 simulation.
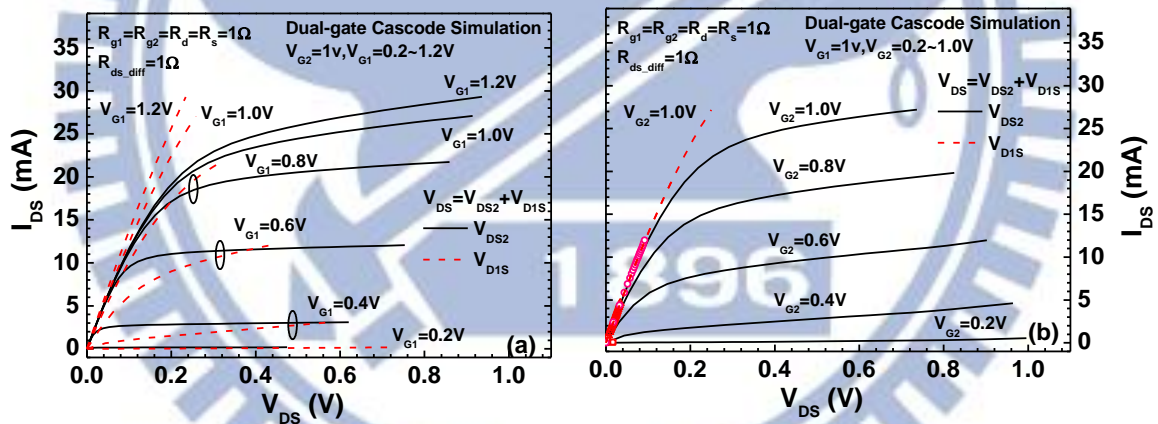
Fig. 4.43 The measured and simulate I_{DS}-V_{DS} of dual-gate MOSFET (a) V_{G2}=1.0V, V_{G1}=0.2~1.2V (b) V_{G1}=1.0V, V_{G2}=0.2~1.0V. R_{g1}= R_{g2}= R_d= R_s=1Ω for 4 terminals, $R_{ds,diff}$=1Ω for merged S/D region. Symbols : measurement. Lines : BSIM-4 simulation.
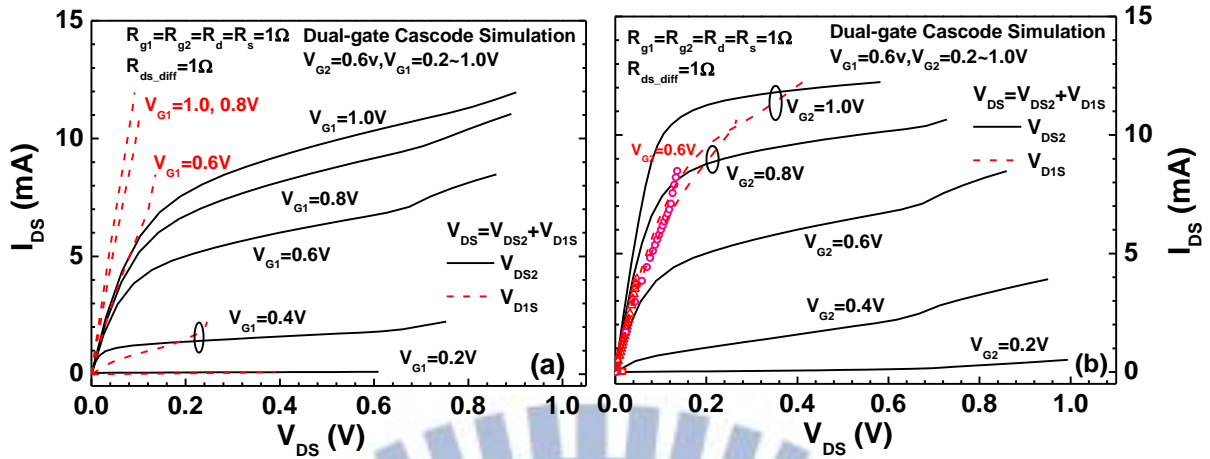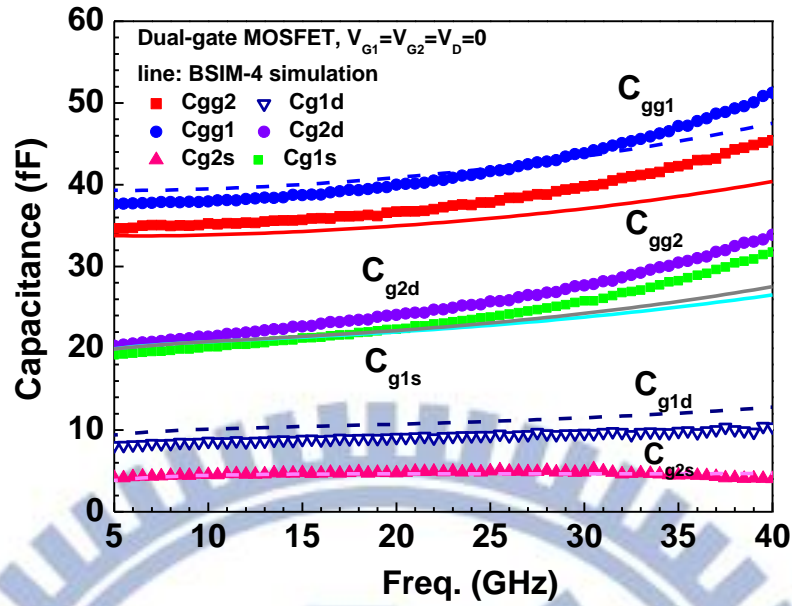
Fig. 4.44 The measured and simulate I_{DS}-V_{DS} of dual-gate MOSFET (a) V_{G2}=0.6V, V_{G1}=0.2~1.0V (b) V_{G1}=0.6V, V_{G2}=0.2~1.0V. R_{g1}= R_{g2}= R_d= R_s=1Ω for 4 terminals, $R_{ds,diff}$=1Ω for merged S/D region. Symbols : measurement. Lines : BSIM-4 simulation.

4.4.2 BSIM-4 C-V Simulation for Dual-gate MOSFET

C-V simulation can be performed by BSIM-4 based on the key model parameters defined in **Table 4.1**. Note that the in-stage gate capacitances including overlap and fringing capacitances can be calculated by C-V model in BSIM-4. However, the cross-stage and inter-stage capacitances specific to dual-gate MOSFET are not available in BSIM-4 C-V model and have to be incorporated via external deployment. **Fig. 4.45** indicate the gate capacitances simulated by BSIM-4 and a comparison with measured data, which were extracted from 4-port Y-parameters. The results show a good match with measurement over a wide range of frequencies up to 40 GHz and justifies C-V model accuracy.
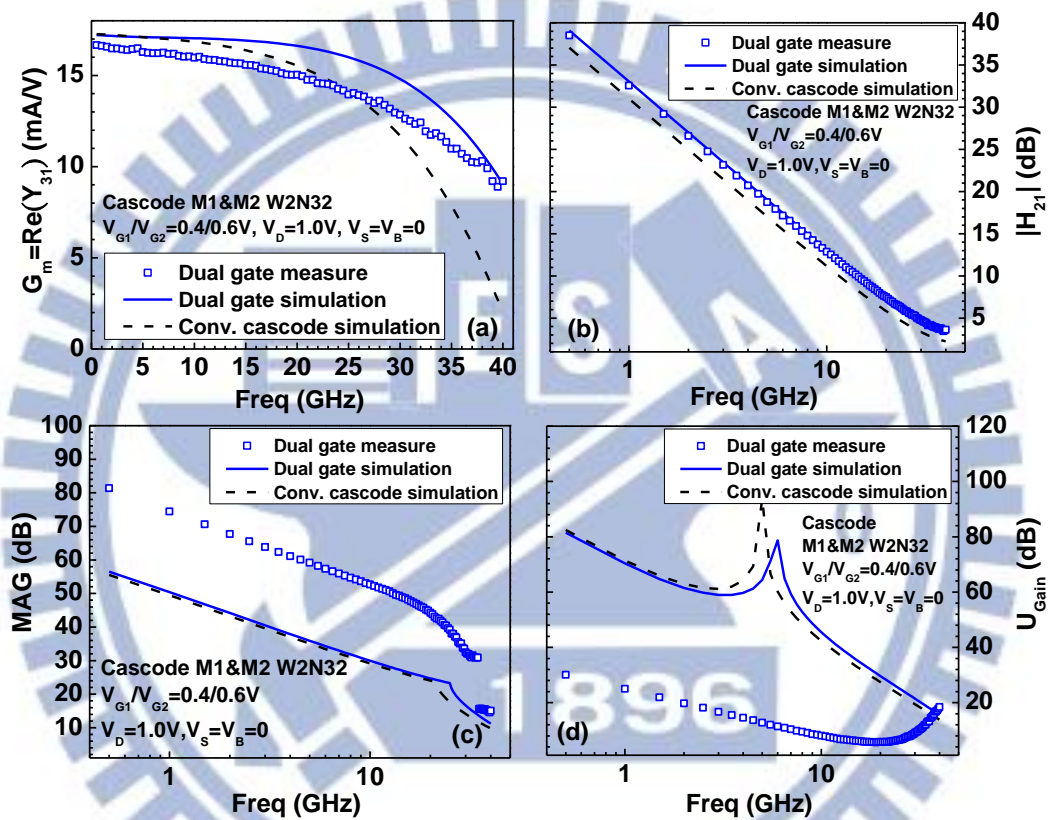
Fig. 4.45 The measured and simulated gate capacitances : in-stage, cross-stage, and total gate capacitances of dual-gate MOSFET. Symbols : measurement. Lines : BSIM-4 simulation.

4.4.3 High Frequency S-parameters Simulation and Comparison with Measurement

In the following, an extensive verification on the model accuracy will be carried out through the comparison between the measurement and simulation by using this small signal equivalent circuit model for all of the 4-port S-parameters after openM3 deembedding. First, four key parameters, such as $G_m=Re(Y_{31})$, H_{21} for f_T, maximum available gain (MAG) and unilateral gain (U) for f_{max} will be demonstrated to verify BSIM-4 simulation accuracy. **Fig. 4.46(a)~(d)** present G_m, H_{21}, MAG, and U for a comparison between measurement and simulation. The good match with measurement justify the model accuracy for dual-gate MOSFET in high frequency simulation. Furthermore, the simulation predicts that new cascode with dual-gate MOSFET can yield improvement on G_m and $f_T(|H_{21}|)$ compared with those of conventional cascode. **Fig. 4.47~Fig. 4.50** present the 4-port S-parameters in terms of mag(S_{ij}) (magnitude of S_{ij}) in which i =1, 4, 3, 2 are corresponding to G1, G2, D, and S, respectively. The results demonstrate good match for mag(S_{ij}), i=1 and 4 but worse deviation for the others, such as mag(S_{ij}), i=2 and 3. As for the phase(S_{ij}) shown in **Fig. 4.51~Fig. 4.54**, a good match with the measurement can be achieved by simulation for most of the parameters,

except somewhat larger deviation revealed in phase(S_{13}) and phase(S_{24}), i.e. the cross-stage parameters. The demonstrated results are for dual-gate MOSFET at off state. As for active state, the results and comparison are presented in **Fig. 4.55~Fig. 4.62**. Again, the results suggest required improvement on both model accuracy and 4-port S-parameters measurement as well as deembedding method**.**

Fig. 4.46 The comparison between measurement and BSIM-4 simulation (a) G_m (b) H_{21}, (c) maximum available gain (MAG) and (d) Unilateral gain of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V
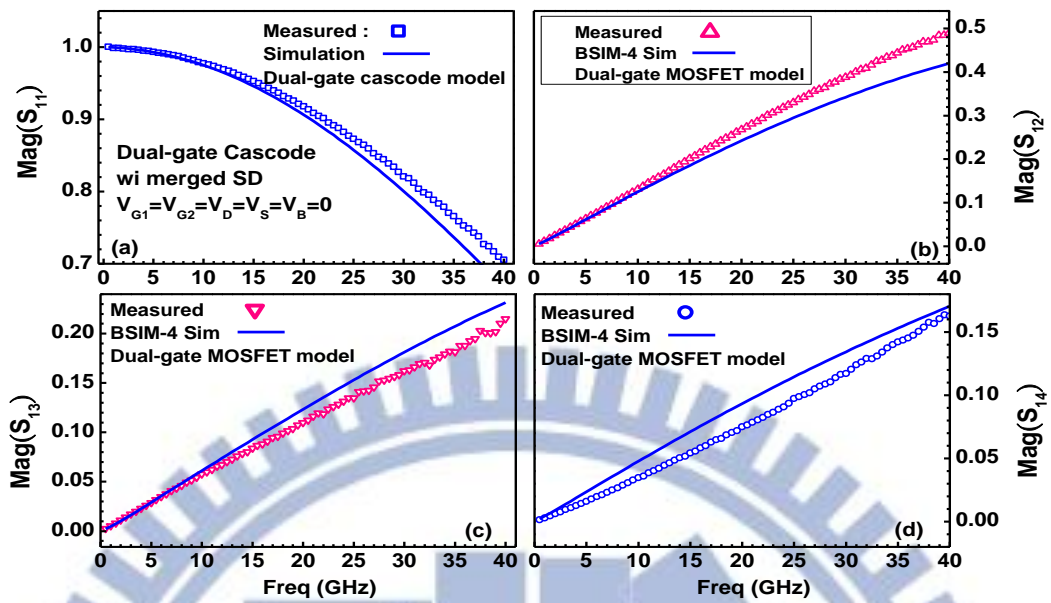
Fig. 4.47 The measured and simulated mag(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D= V_S= V_B=0$ (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Symbols : measurement. Solid lines : BSIM4 simulation.
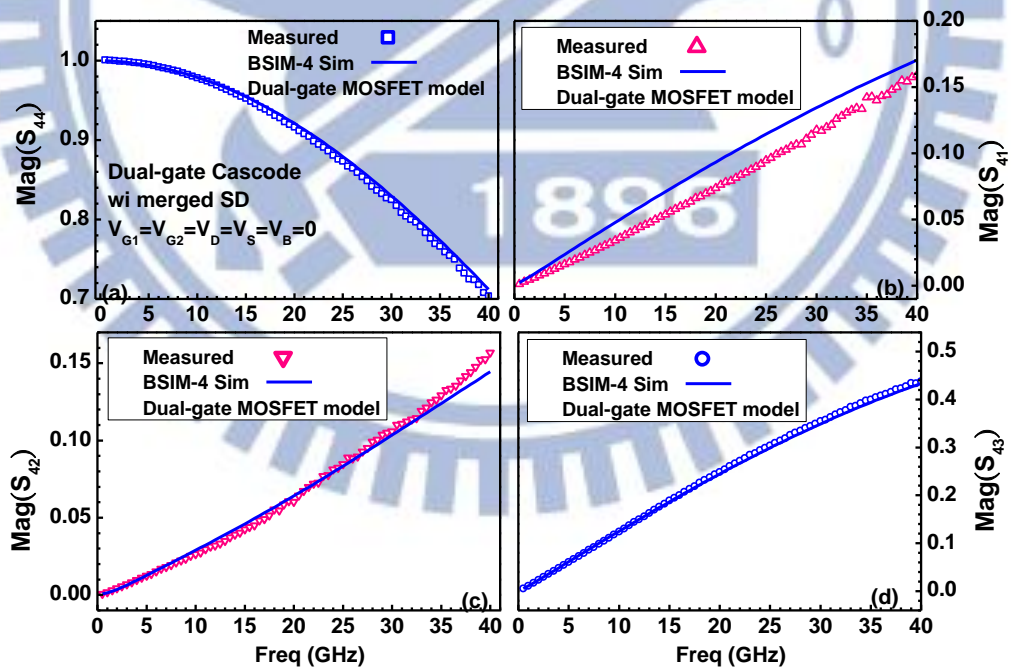
Fig. 4.48 The measured and simulated mag(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D= V_S= V_B=0$ (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Symbols : measurement. Solid lines : BSIM4 simulation.

Fig. 4.49 The measured and simulated mag(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) Mag(S_{33}) (b) Mag(S_{32}) (c) Mag(S_{31}) (d) Mag(S_{34}). Symbols : measurement. Solid lines : BSIM4 simulation.

Fig. 4.50 The measured and simulated mag(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) Mag(S_{22}) (b) Mag(S_{23}) (c) Mag(S_{21}) (d) Mag(S_{24}). Symbols : measurement. Solid lines : BSIM4 simulation.
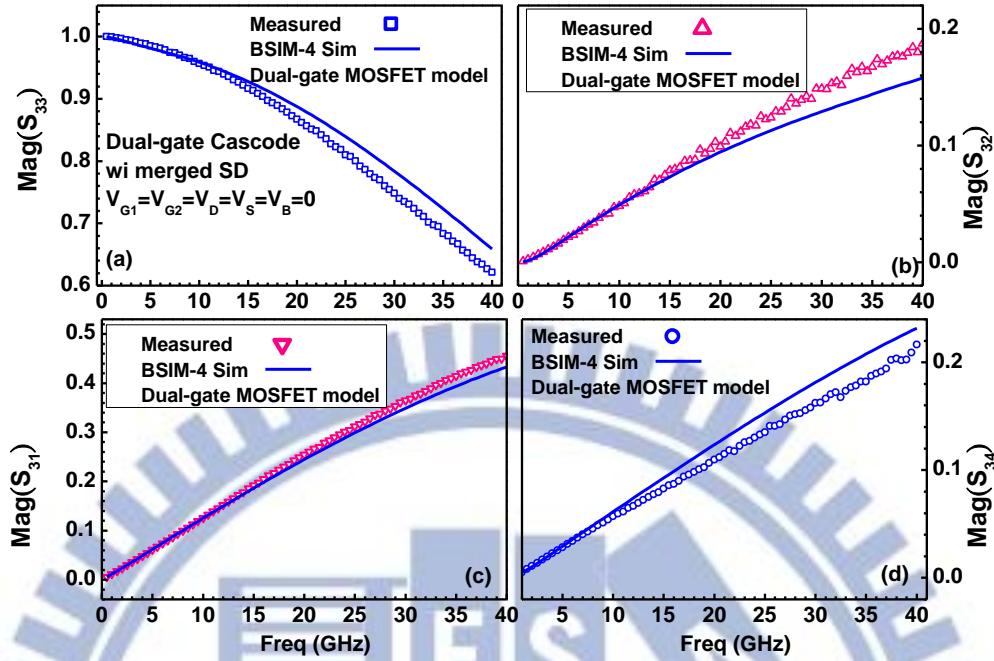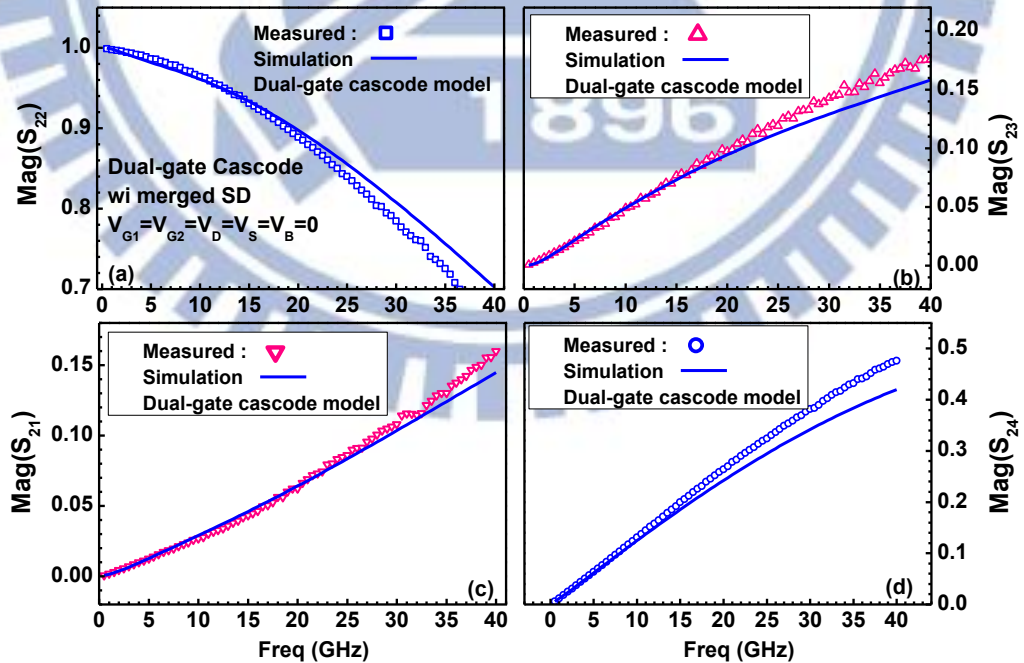
Fig. 4.51 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Symbols : measurement. Solid lines : BSIM4 simulation.

Fig. 4.52 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{11}) (b) phase(S_{12}) (c) phase(S_{13}) (d) phase(S_{14}). Symbols : measurement. Solid lines : BSIM4 simulation.

172

Fig. 4.53 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=$ $V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{33}) (b) phase(S_{31}) (c) phase(S_{32}) (d) phase(S_{34}). Symbols : measurement. Solid lines : BSIM4 simulation.
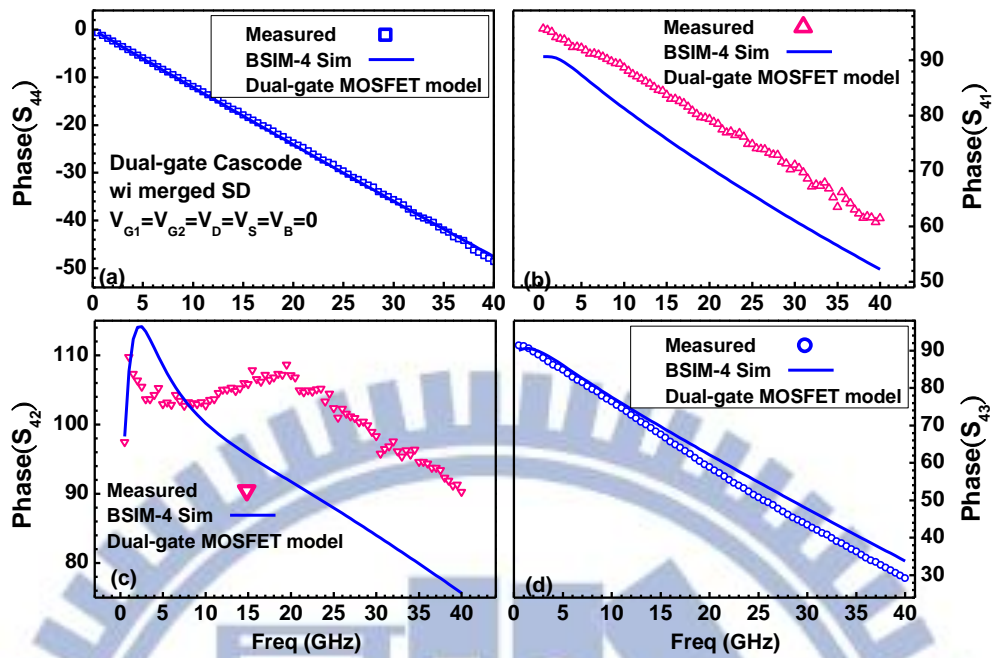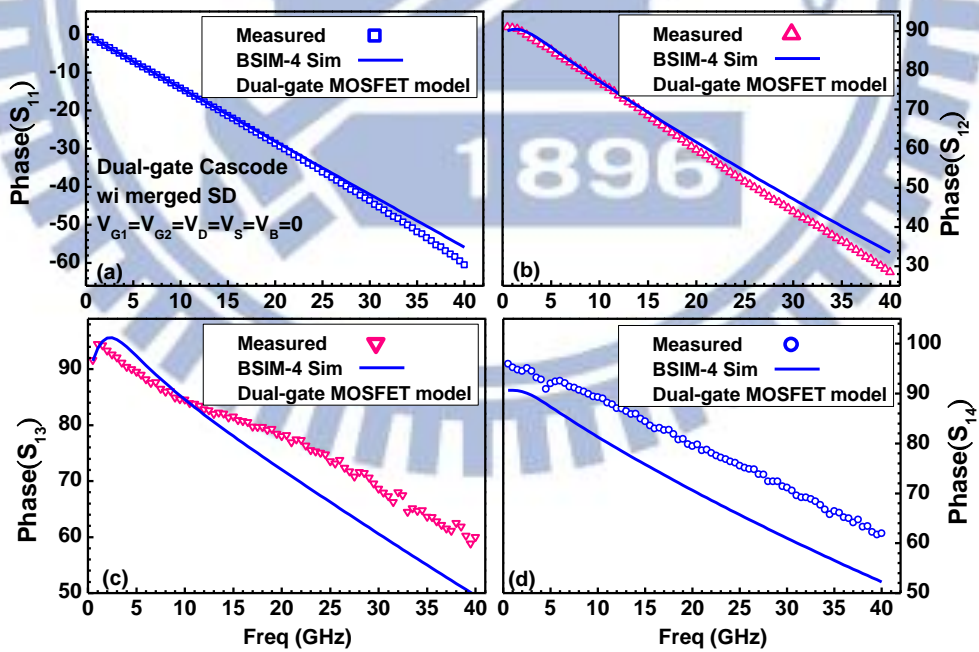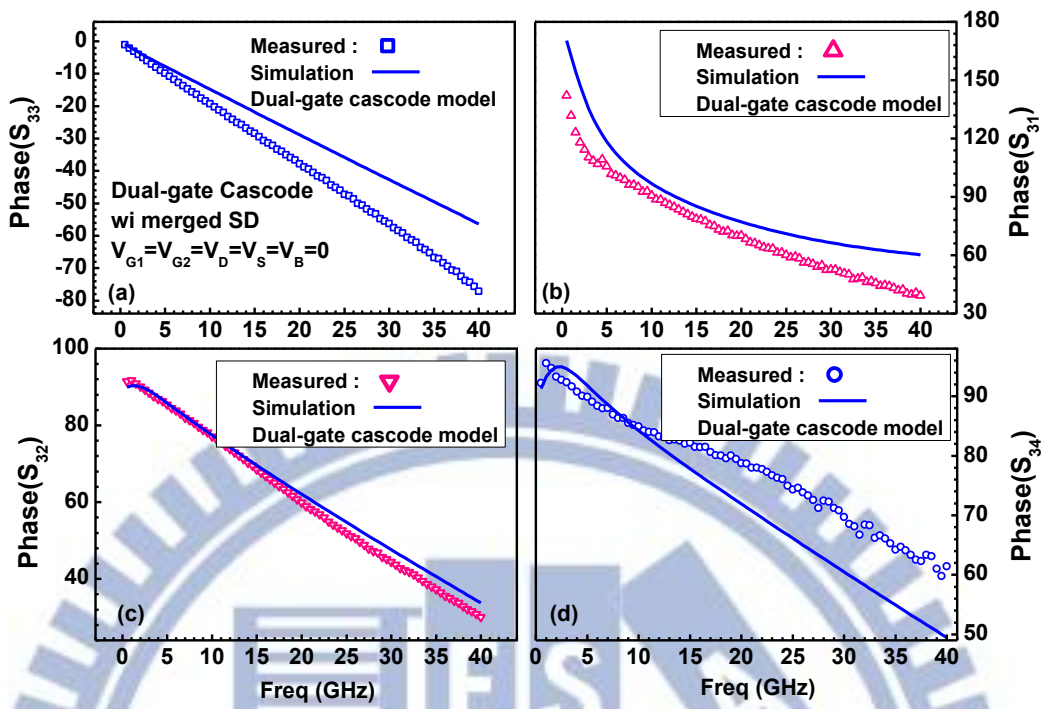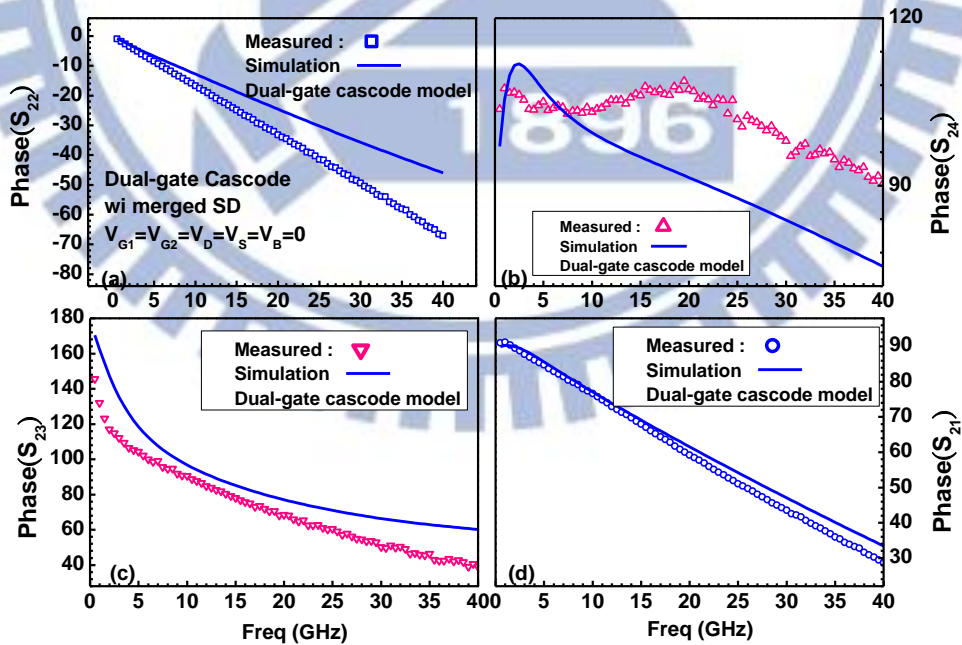

Fig. 4.54 The measured and simulated phase(S) of dual-gate MOSFET at off state $V_{G1}=$ $V_{G2}=V_D=V_S=V_B=0$ (a) phase(S_{22}) (b) phase(S_{24}) (c) phase(S_{23}) (d) phase(S_{21}). Symbols : measurement. Solid lines : BSIM4 simulation.

Fig. 4.55 The measured and simulated mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{11}) (b) Mag(S_{12}) (c) Mag(S_{13}) (d) Mag(S_{14}). Symbols : measurement. Solid lines : BSIM4 simulation.

Fig. 4.56 The measured and simulated mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{44}) (b) Mag(S_{41}) (c) Mag(S_{42}) (d) Mag(S_{43}). Symbols : measurement. Solid lines : BSIM4 simulation.

Fig. 4.57 The measured and simulated mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{33}) (b) Mag(S_{32}) (c) Mag(S_{31}) (d) Mag(S_{34}). Symbols : measurement. Solid lines : BSIM4 simulation.
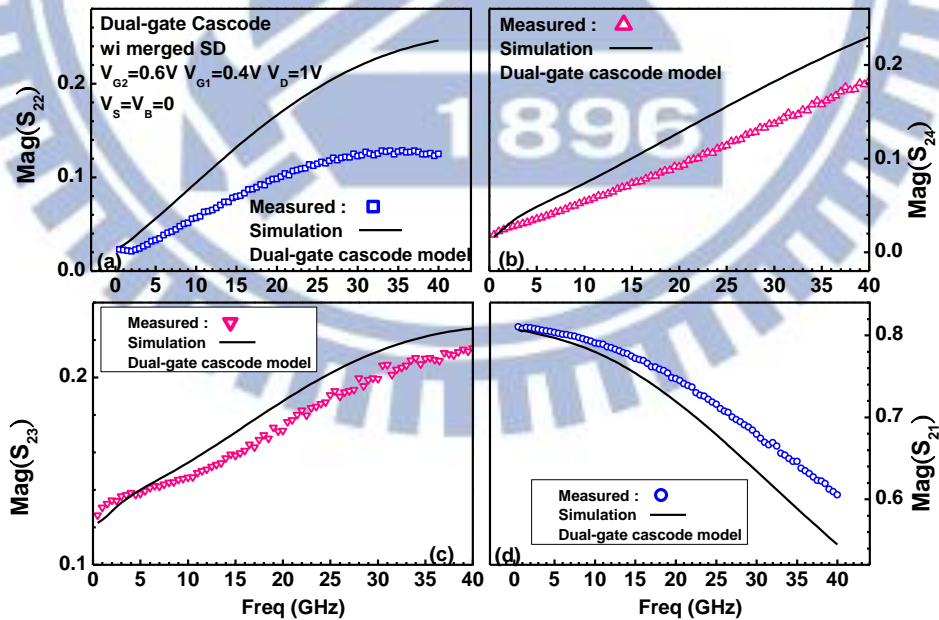
Fig. 4.58 The measured and simulated mag(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) Mag(S_{22}) (b) Mag(S_{23}) (c) Mag(S_{21}) (d) Mag(S_{24}). Symbols : measurement. Solid lines : BSIM4 simulation.
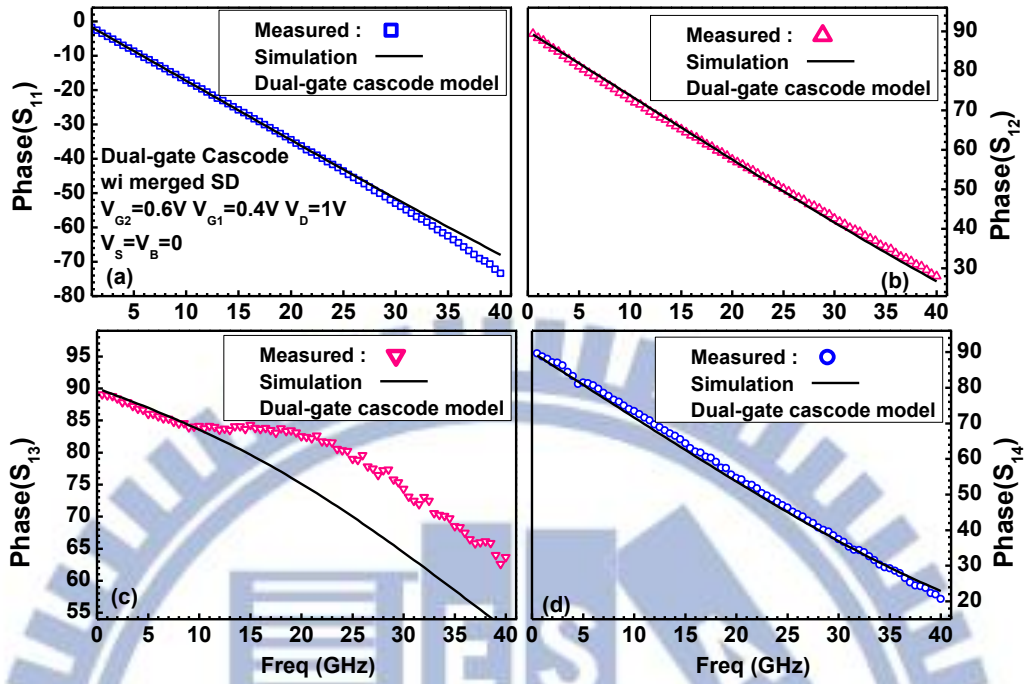
Fig. 4.59 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{33}) (b) phase(S_{31}) (c) phase(S_{32}) (d) phase(S_{34}). Symbols : measurement. Solid lines : BSIM4 simulation.
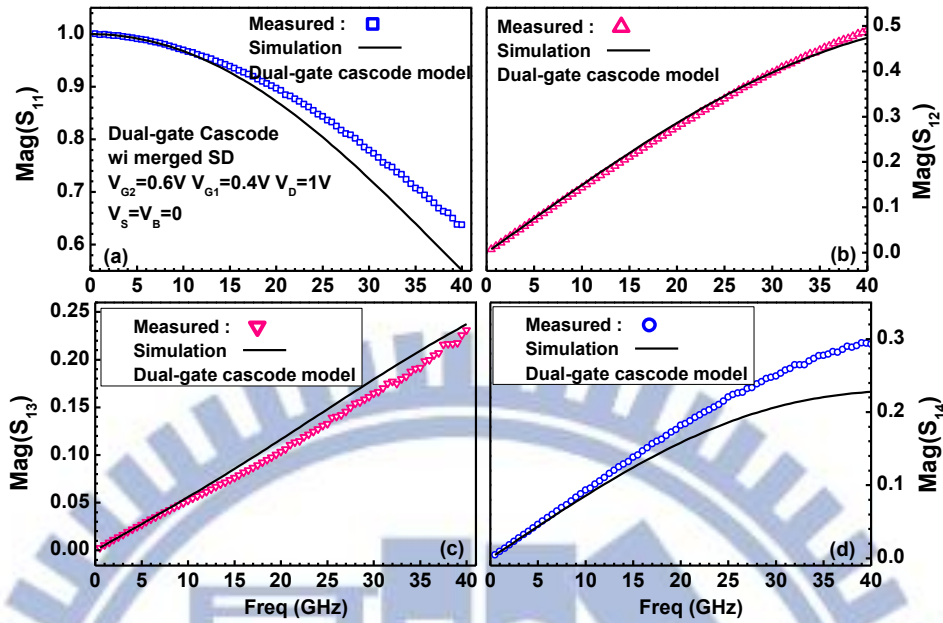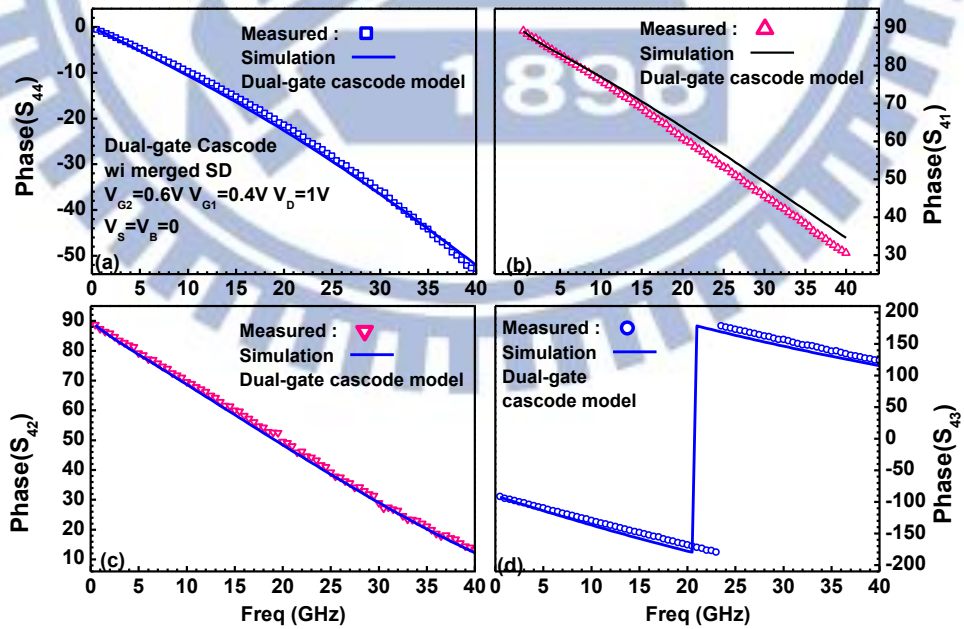

Fig. 4.60 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V   (a) phase(S_{44}) (b) phase(S_{41}) (c) phase(S_{42}) (d) phase(S_{43}). Symbols : measurement. Solid lines : BSIM4 simulation.
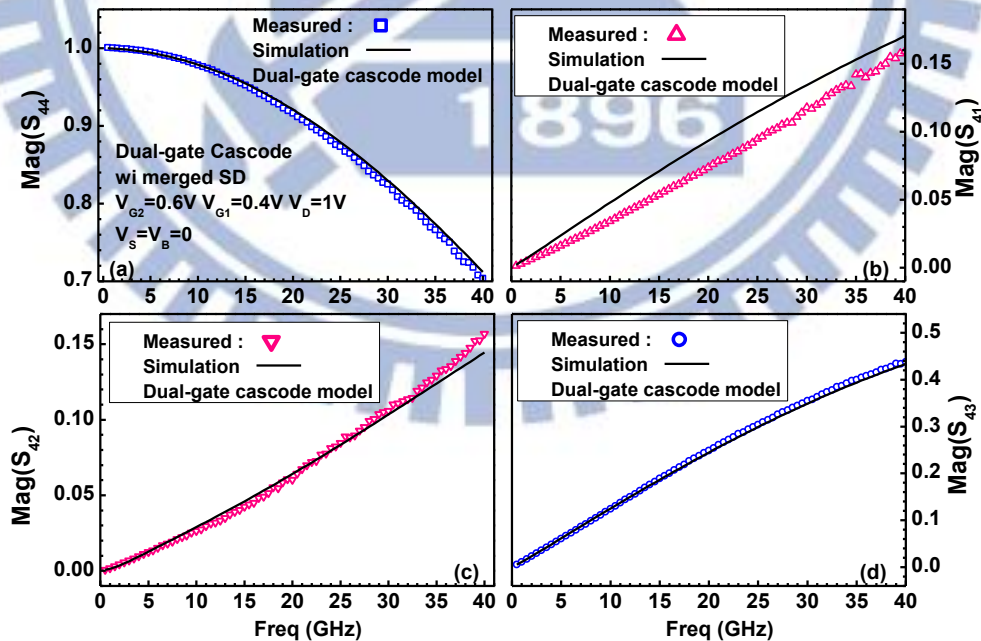
Fig. 4.61 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{22}) (b) phase(S_{24}) (c) phase(S_{23}) (d) phase(S_{21}). Symbols : measurement. Solid lines : BSIM4 simulation.
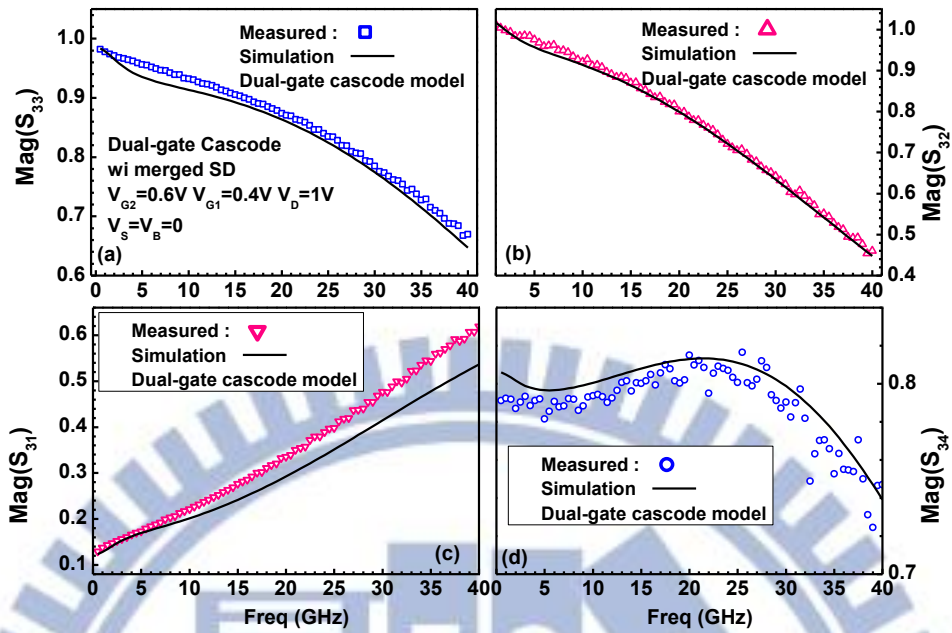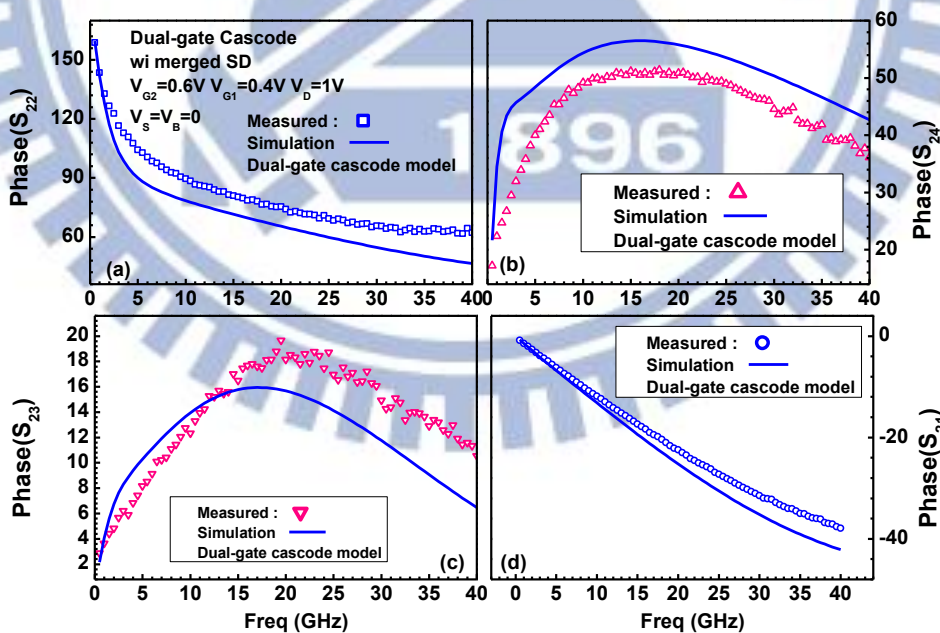

Fig. 4.62 The measured and simulated phase(S) of dual-gate MOSFET at active state V_{G1}=0.4V, V_{G22}=0.6V V_D=1.0V (a) phase(S_{11}) (b) phase(S_{12}) (c) phase(S_{13}) (d) phase(S_{14}). Symbols : measurement. Solid lines : BSIM4 simulation.
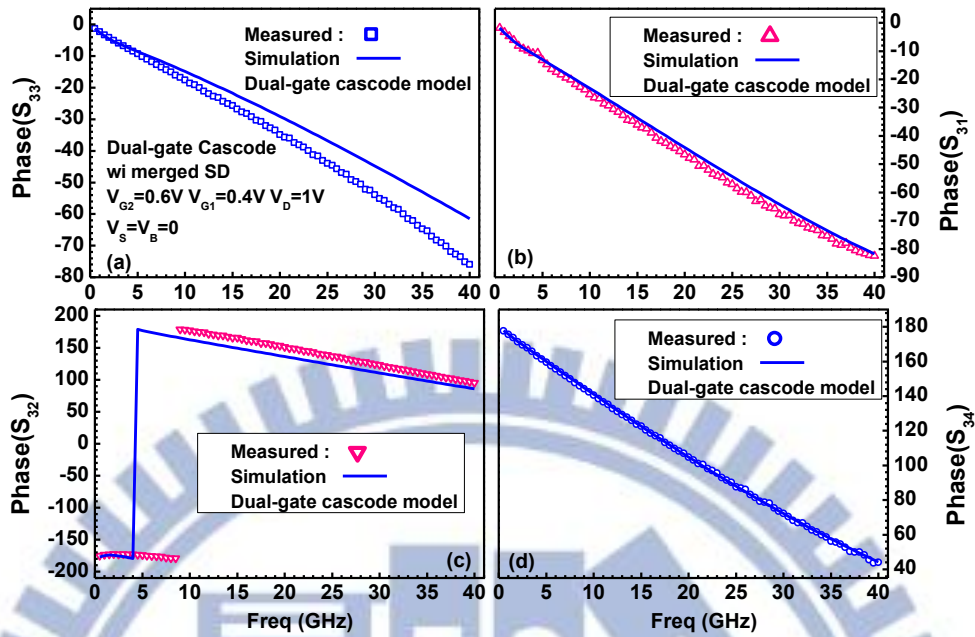
Chapter 5

Conclusions and Future Work

5.1 Conclusions

這次的 body network 可以成功的吻合 40GHz 的資料，並且建立了小訊號等效電路和合併 BSIM4 model 中模擬。我們建立了有物理涵義的 bodynetwork 和萃取流程。

這次研究發現許多人會把 drain 的 $Re(Y_{33})$ (或是 2 port 時的 $Re(Y_{22})$)當作他們驗證 body network 的準確性的依據，這次研究藉由發現到 body network 的精準，可以提升與 body 端有關參數($Re(Y_{43})$、 $Re(Y_{42})$、 $Re(Y_{41})$)的準確性。但不保證 $Re(Y_{33})$ 就一定會準。因為在 2 port 時，大家認為 drain 端和 body 端相連，所以想到改良 body network，但是藉由 4 port 時，我們直接觀察到 body 端，我們可以知道 body 端的結構。我才明白不一定 body 端看到的都準，drain 端看到也會這樣。小訊號等效電路的推導，告訴我們 gm，ro 正是影響 $Re(Y_{33})$ 的重要因子。我們先經由 4 port S 參數中萃取 body resistances，以確認我們的 ro 萃取的值是合理的。

在這論文中 Dual Gate 的研究，我們看到 dual gate 和 conventional cascode 差別沒有很大。而本論文的小訊號等效電路和模型可以應用在 40GHz 的範圍。

5.2 Future work

UN65 中針對 body 和 deep n-well 相連的 MOSFET 分析特性，而創建出新的基板網路，我們可以模擬出準確的的輸出阻抗。為了動態基極偏壓的使用，我對 BSIM4 模型做了矯正。但是我的元件太少了，如果有不同尺寸大小的元件，我的研究才會有實際的應用。除此之外，從不同的 body contact layout 和 deep n-well layout 中，探討雜訊的影響及驗證 body network 的準確性是另一個方向。

探討不同的 body contact layout 和 deep n-well 接線中，量測 4 port s 參數並做比較，這個工作，我希望之後有人可以集中在一顆晶片上完成，這是為了減少製程的變異而帶

來分析上的盲點。

這篇的論文中 dual gate 的研究並不完整，我沒有針對 dual gate 和傳統的 cascode 作特性上的分析，因此希望之後有人能完成這個工作。

Dual gate 和 conventional cascade 要作比較需要另外在畫一個 4-port pad，並其中 2 port 量測 S 參數和雜訊指數，另外 2 port 給予 DC 偏壓。

Dual gate 的研究存在了一些問題，首先在萃取參數上，我使用兩種結構(分離式閘極和共用式閘極)去萃取參數，原本我預計要在 common gate 結構上萃取 body resistances，但是萃取出來的結果帶入模擬，其模擬結果和量測並不吻合。接著在 inter stage capacitances 萃取，在高頻時電容會變成負值。我認為這是因為我的 open de embedding 沒有做好造成的，因為下線面積的限制，我必須使用同一個 open pad，但 dual gate 和 single MOSFET 差異大，這會造成 open de-embedding 產生誤差。另外使用兩種結構萃取參數，元件 layout 的必須盡量相似。除此之外修改元件 layout 使 M1 的閘極電阻更小可以降低雜訊指數，這也是將來可以研究的方向。

最後我把 future work 整理在底下。

1. UN65 的 body network 並無 scalable data 作對照。

2. UN65 沒有做 short de-embedding。

3. 高頻時 Dual gate 的 inter stage capacitances 萃取值不合理。

4. Dual gate 和 conventional cascode 的詳細比較。

5. Dual gate 的 gate resistances 做最佳化。

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