國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

決定高效能蕭特基金氧半場效應電晶體傳輸參數的
新實驗方法

A New Experimental Determination of Transport
Parameters in High Performance Schottky-Barrier
MOSFETs

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2010 年 9 月上旬

決定高效能蕭特基金氧半場效應電晶體傳輸參數的新實驗方法

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摘要

在近年來，蕭特基金氧半場效應電晶體以金屬矽化物取代源極和汲極的方式受到了許多關注，因為它具有優越的 I_{on}/I_{off} 比例及壓制短通道效應的能力，但是蕭特基介面和通道間形成的蕭特基位障卻降低了它的效能。為了減輕蕭特基位障的影響並增進效能，摻雜物隔離式蕭特基金氧半場效應電晶體因而被提出來，且觀察到載子速度的提升，這個現象被認為是擁有強烈的速度過衝機制所導致。然而，這個機制並未對所觀察到的速度增強有一個完整及詳細的探討。因此，對元件做傳輸效率的分析是必要的。

彈道理論可以被用來延伸做為準彈道現象來探討傳輸效率。在本論文裡，我們提出一個名為速度飽和模型的新方法，以實驗量測來研究摻雜物隔離式蕭特基金氧半場效應電晶體的彈道效率以及射入速度。我們一開始先引入摻雜物隔離式蕭特基金氧半場效應電晶體的基本特性，包含元件結構、工業用製程、操作原理以及電性，然後再分別以溫度相依法和速度飽和模型來討論及比較彈道效率。相對於溫度相依法 (Temperature Dependent Method)，透過速度飽和模型，我們獲得了合理的結果。實

驗結果顯示摻雜物隔離式蕭特基金氧半場效應電晶體在通道長度愈短時，會有更高的彈道效率促使它的效能增強，不同於溫度相依法所得的結果。除此之外，我們也用接觸蝕刻停止層型式的應變矽元件做一驗證，結果清楚顯示由於通道的應變力引起低的等效載子質量使其擁有高的射入速度以增進元件的效能。

　　最後，我們得出了幾個結論：（1）隨著通道長度的縮短，摻雜物隔離式蕭特基金氧半場效應電晶體展現其高效能，（2）經由速度飽和模型所決定的彈道效率，應用在摻雜物隔離式蕭特基金氧半場效應電晶體上，顯示出比溫度相依法有更可靠的結果，（3）摻雜物隔離式蕭特基金氧半場效應電晶體，在通道長度縮短下的效能增益是因為彈道效率的強烈增加，（4）接觸蝕刻停止層型式的應變矽元件的效能改善是由於其高的射入速度所引起的。因此，速度飽和模型提供了我們一個比溫度相依法更精確及可靠的彈道傳輸的分析。

A New Experimental Determination of Transport Parameters in High Performance Schottky-Barrier MOSFETs

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Abstract

In recent years, SBMOS with metal-silicided source/drain has received much attention for its better I_{on}/I_{off} ratio and the immunity to short channel effect but has shown a worse performance due to Schottky junction at the silicide and the channel. In order to alleviate the barrier height of S/D Schottky junction and to improve the performance, Dopant-Segregated SBMOS (DSS) is introduced, and a better enhancement on the carrier velocity has also been observed because of the strong velocity overshoot phenomenon. However, it has been not clear on the mechanism of the enhancement in overshoot velocity. Thus, the analysis of the transport efficiency is mandatory.

The ballistic theory has been extended to explore the transport efficiency in quasi-ballistic regime. In this thesis, a new approach called Velocity Saturation Model (VSM), based on experimental measurements, is developed to study the ballistic efficiency, B_{sat}, and injection velocity (v_{inj}) for DSS. We first introduce the basic properties of DSS including structure of device, manufacturing process, operating principle, and electrical characteristics. Then, we discuss and compare the ballistic efficiency extracted by the TDM(Temperature Dependent Method) and VSM respectively. For VSM, we obtain a reasonable relationship of performance, compared to TDM. Moreover, the experimental results showed that the value of B_{sat} is improved with reducing the channel length, resulting in a better enhancement of the performance, but not agreed with the results of TDM. Additionally, the strained-Si device with CESL is further discussed. It demonstrates that the v_{inj} dominates the improvement of the performance since the strained channel induces a low effective mass.

Finally, it was concluded that: (1) with the shrinkage of channel length, the DSS exhibits high performance; (2) the determination of B_{sat} by VSM is applied to DSS, which offers more reliable results than TDM; (3) the enhancement in DSS increases with decreasing channel length because of the increase of the B_{sat}; (4) the improvement of performance in strained-Si device with CESL is induced by high v_{inj}. Consequently, the VSM provides us more accurate and reliable results than the TDM ones.
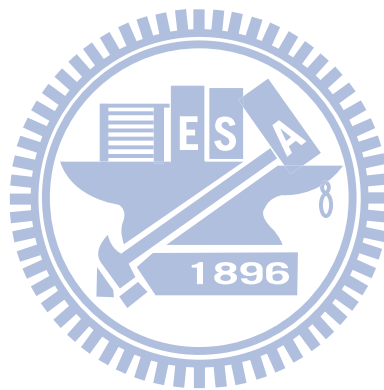
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Chapter 1

Introduction

1.1 Motivation

In the development of modern VLSI devices, many typical structures are investigated for the enhancement of performance. For example, the strained-Si device with SiGe S/D or CESL and high-k/metal gate stack were manufactured in the past decade. They improved the loss of performance, which is induced by short channel effect. The Schottky Barrier MOSFET (SBMOS) is another solution for metal silicide replacing source and drain. It shows good ability on suppressing the short channel effect, and has lower subthreshold swing which induces high I_{on}/I_{off} ratio, but the SBMOS has poor performance because the Schottky barrier height at silicide/channel interface suppresses the transport efficiency of the carrier. This drawback limits the development of SBMOS. In recent years, Tsui et al. [1.1] has provided an available solution for improving performance through the additive process, called Dopant Segregation implantation, being applied prior to the process of source/drain silicidation. The Dopant Segregation (DS) layer is formed at silicide/channel interface, and exhibits the quite high doping concentration. This is called the snowplow effect. This SBMOS with DS layer is termed Dopant-Segregated SBMOS (DSS). The addition of DS layer has succeeded in lowering and narrowing Schottky barrier, and thus raised up the performance. Moreover, low series source/drain resistance induced by modifying Schottky barrier has also been observed.

At present, high velocity over conventional MOSFET has been observed [1.2]. The high velocity leads the high performance. This behavior explained that DSS has more significant velocity overshoot phenomenon than conventional MOSFET does.

But the velocity overshoot phenomenon can not provide us a complete and detailed analysis. Thus, we will use the ballistic theory to discuss the enhancement of velocity as channel length is decreased, and develop a new approach called Velocity Saturation Model (VSM) for the extraction of ballistic efficiency (B_{sat}) and injection velocity (v_{inj}). The higher B_{sat} and v_{inj}, the better performance does. As a result, the VSM provides us a good criterion for the analysis of performance enhancement.

1.2 Organization of the Thesis

This thesis was focused on analysis of transport efficiency in DSS, but we still start from the basic properties. In Chapter 2, we introduce the basic properties of SBMOS including structure, process flow and operating principle. Afterwards, the improvement of DSS in comparison to the SBMOS is demonstrated and discussed.

In Chapter 3, the ballistic theory is introduced. We simply describe the origin of principle and the Temperature Dependent Method (TDM) which is commonly used to determinate B_{sat}. After that we use TDM to discuss the transport efficiency of DSS. In Chapter 4, the VSM has been proposed in detail. The experimental results of DSS by VSM comparing with those of TDM are also discussed. Finally, the conclusions are given in Chapter. 5.
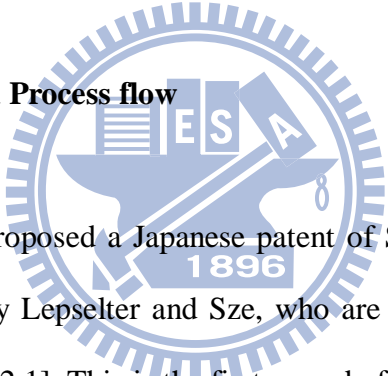
Chapter 2

Performance of Schottky Barrier MOSFET

The Schottky Barrier MOSFET (SBMOS) is formed by metal silicide replacing source/drain in conventional MOSFET. The hetero-junction at silicide/channel interface determines the properties of SBMOS. In this chapter, we first introduce the basic properties of SBMOS. And then, the Dopant-Segregated SBMOS (DSS) as a key issue will be discussed.

2.1 Basic Properties of Schottky Barrier MOSFET

2.1.1 Device Structure and Process flow

In 1966, Nishi, first proposed a Japanese patent of SBMOS, but the first paper for SBMOS is published by Lepselter and Sze, who are the well-known scholars in semiconductor technology [2.1]. This is the first record of PtSi silicide PMOSFET. At that time, SBMOS performed poor performance so that it did not receive much attention. Later in 1984, T. Mochizuki and K. Wise reported a NMOSFET with Schottky source/drain. This device improved the poor performance. Afterwards, the SBMOS attracts much more attention. Several advantages of the SBMOS had been reported repeatedly in the later years as the following:

1. Better for devices scaling down.

2. Low temperature processing for source/drain formation.

3. Better control of short channel effect.

4. Reduced the floating body effect in SOI devices.

5. Reduced the latch-up susceptibility.

A cross section TEM of SBMOS and schematic structure of conventional MOSFET and SBMOS are shown in Figs. 2.1 (a) and (b). The main difference of SBMOS with conventional MOSFET is that metal silicide replaces source/drain of conventional MOSFET. The manufacturing process for SBMOS is simpler than conventional MOSFET and fully compatible with the standard CMOS process.

The schematic process flow for the fabrication of SBMOS is shown in Fig. 2.2. The process starts with a standard isolation process such as STI or LOCOS. Then, the well implantation is applied to adjust V_{th}. Standard lithography and etch technologies are used to form the gate stack, even the novel structures of gate stack such as dual-polysilicon and metal gate/high-k could be applied to SBMOS. A thin sidewall spacer formation is used to define the active operating region. Halo pocket implantation is not necessary because of effective effect of Schottky source/drain barrier controlling short channel effect well. The source/drain extension and deep source/drain implantation are also eliminated.

During the process of silicidation, a dual-silicide exclusion-mask process is used to form source/drain. No mask means that gate stack is treated as hard mask to be patterned for definition of source/drain region. ErSi and PtSi are usually used to form source/drain for n-type and p-type SBMOS respectively. Erbium and Platinum are provided by standard PVD process equipment. During the cycle of thermal silicidation, temperature is very important to be controlled. To avoid breaking active region of device, the maximum temperature required for silicide reaction is less than $600^{o}C$. Finally, the back-end metallization is provided to form the complete device.

2.1.2 Principles of Operation

Although SBMOS has a similar structure with conventional MOSFET, SBMOS exhibits different transport behaviors in operation. Figs. 2.3 and 2.4 show the band diagrams on varied states of operation in p-type and n-type SBMOS respectively. The carrier transport of p-type SBMOS relies on holes injecting into channel at the valence band side, and that of n-type SBMOS relies on electrons injecting into channel at the conduction band side. We consider p-type SBMOS as our discussion in operation.

In Fig. 2.3 (a), we clearly see the difference of band diagram between SBMOS and conventional MOSFET. At the channel edge, SBMOS has a significant barrier, but conventional MOSFET doesn't. At off-state, with V_g applied to 0 volt, the channel barrier raises and stops the carrier transport at the valence band side. But there are still some leakage carrier transporting through the channel on the other side, which means conduction band side for p-type MOSFET. We can clearly understand that the Schottky barrier in SBMOS makes the extra barrier preventing a large number of leakage carrier entering the source. As a result, the I_{off} current on off-state in SBMOS has less magnitude than conventional MOSFET one.

When V_g increases over threshold voltage, the operation of device will be at on-state. A large number of carriers enter the channel and reach to the drain, thus the I_d current raises strongly. In SBMOS, the Schottky barrier at source edge can't make carrier easily pass by. Comparing with conventional MOSFET, the SBMOS should demonstrate less I_d current than conventional MOSFET at on-state. Figs. 2.3 (b) and Fig. 2.4 (b) show that SBMOS has weak I_d current in both n-type and p-type SBMOS.

The loss of performance is due to Schottky barrier at the source edge. In spite of the leakage current decreasing, the SBMOS doesn't show sufficient performance at

on-state. This weakness limits the development of SBMOS, therefore finding a method to enhance the performance of SBMOS is an important course for the development.

2.2 SBMOS with Dopant Segregation Implantation

2.2.1 Device Structure and Process flow

In order to improve performance of SBMOS, many methods are investigated to modify Schottky barrier at silicide/channel interface. One of available methods is the addition of dopant segregation implantation prior to silicidation. This device is termed as Dopant-Segregated SBMOS (DSS). The TEM graph of DSS is shown in Fig. 2.5 (a). It clearly shows the formation of Dopant Segregation (DS) layer at the silicide/channel interface. Due to the addition of DS layer, the band diagram of SBMOS is modified, as shown in Fig. 2.5 (b). The dash line represents the original band diagram of SBMOS, which shows a higher barrier than DSS at silicide/channel interface. The DS layer makes Schottky barrier lower and narrow, and the carrier at the source side can pass the Schottky barrier easily. This behavior results in the enhancement of I_d current at on-state.

Figure 2.6 shows the schematic process flow of DSS from Toshiba. After isolation formation, gate stack is formed by presented technologies, lithography, thermal oxidation, deposition, and anisotropic etching. The process of DSS is also compatible with standard CMOS techniques, after that, a disposable spacer sidewall is formed to define the active region. After deep source/drain implantation, disposable spacer is removed and Offset spacer is deposited. The use of halo implantation eliminates the effect of short channel, and avoids the occurrence of punch through.

Then, dopant segregation implantation and thermal process for silicidation are applied to form DS layer. Finally, a complete device is formed after back-end process.

The DS layer is formed by the snowplow effect, which makes dopant redistribute during thermal cycle of silicidation. Whether dopant redistribution occurs or not is determined by diffusivity and solid solubility of dopant in the silicide and the presence of dopant defects at silicide/si interface. In the case of NiSi phase, Ni atoms are the moving species, supplied by diffusion through the growing silicide layer to Si/Si interface because the covalent bonds between Si atoms are softened by diffusion of Ni atoms. A significant change of volume is involved when silicide is formed. As a result, point defects will be generated in order to partially relieve this stress. Due to the formation of vacancies, the diffusivity of dopant in Si is enhanced and dopants move toward the interface where it piles up between Si and Si. In case of dopant segregation during silicidation, the high density of point defects can lead to a local dopant concentration higher than solid solubility. The SIMS profiles after redistribution of dopant are shown in Fig. 2.7 (a). A large number of dopants concentrated at silicide/Si interface are observed.

2.2.2 The Comparisons with SBMOS

The addition of DS layer enhances the efficiency of carrier transport, which can be understood in previous section. The I_d-V_d characteristic of DSS and the comparison with SBMOS is shown in Fig. 2.7 (b). The performance of DSS shows the significant enhancement, and the leakage current of DSS lower than conventional MOSFET is observed. We can make comparisons of the band diagram in both two devices, as shown in Fig. 2.7 (c).

Figure 2.7 (c) shows the band diagrams of n-type DSS and SBMOS. At off-state,

the hole tries to enter channel, and reaches to the source. The decrease of leakage current by Schottky barrier in valence band formed at drain edge is clearly demonstrated in SBMOS. However, the DSS shows higher Schottky barrier height in valence band than SBMOS, which induces the stronger suppression on leakage current than SBMOS. Consequently, the I_{off} of DSS is lower than that of SBMOS.

At on-state, the electrons are injected into the channel, and are collected by the drain. In SBMOS, the Schottky barrier at source edge at conduction band blocks a large number of electron entering channels. In DSS, the DS layer modifies the Schottky barrier at silicide /channel interface shown in Fig. 2.5 (b). The narrower and lower Schottky barrier thickness and height is generated. Based on quantum effect, the narrower and lower barrier thickness and height enhance the probability of particle tunneling. Consequently, the electron can enter channel by tunneling through Schottky barrier at present. This extra carrier injection raises the performance up, and the performance of DSS shows better result than SBMOS practically.

2.2.3 Advantages of DSS

The performance enhancement by the addition of DS layer in SBMOS is shown in the previous section. Hence, we will show the other advantages in the use of DSS. Fig. 2.8 (a) and Fig. 2.8 (b) show that DSS has better immunity to suppress the short channel effect and DIBL characteristic than conventional MOSFET. As channel length scaling down, these can make the device more stabilized. Furthermore, the series source/drain resistance of DSS less than conventional MOSFET is also observed through the R_{tot}-V_d curve, as shown in Fig. 2.8 (c). This is because DS layer modifies the Schottky barrier at silicide/channel interface, the contact resistance decreases largely. Besides, the low series source/drain resistance is considered to be

one of the reasons enhances the performance of DSS.

Figure 2.9 shows that the I_{on}/I_{off} ratio of DSS is larger than conventional MOSFET. This result corresponds to better performance and lower series source/drain resistance than conventional MOSFET before. For the discussion on performance, the carrier velocity is used for further study. A. Kinoshita first proposes that DSS has the more significant behavior of velocity overshoot in IEDM 2006 [1.2]. Fig. 2.10 (a) and Fig. 2.10 (b) show his experimental results. As channel length scaling down, the difference of velocity in DSS comparing with conventional MOSFET increases strongly. We can see that the velocity in DSS overshoots over saturated velocity (v_{sat}) in the short channel regime. The experimental results provide us an explanation for the performance enhancement, but there is still not a series of complete and detailed discussion. We will discuss it through the ballistic theory in the next chapter.

2.3 Device Preparation and Experimental Setup

2.3.1 Device Preparation

For our experiments, the experimental devices and control devices are needed to be verified clearly. The devices are based on 65nm technology of United Microelectronics Corporation (UMC) in Taiwan. Fig. 2.11 (a) shows the TEM cross-section image of DSS, and Fig. 2.11 (b) depicts the schematic process flow for fabrication. The channel length ranges from 55nm to 1um with width varying from 70nm to 1um, and the largest device with W/L= 10um/10um is used for measurement in capacitance of gate dielectric. The code name LO65-BSRx (x: 1~ c) devices are used for major measurements of characteristic analysis. The pieces of wafer named KPC6607 for DSS and KPC6619 for conventional MOSFET are used.

In the fabrication, the STI isolation is formed first, and so is gate stack with 1.2nm thickness of gate dielectric. The offset spacer is used to define active region. Halo and dopant segregation implantation are applied prior to the formation of disposable spacer which defines source/drain. After disposable is removed, metal silicide (NiPtSi) is formed during thermal cycle of silicidation. Temperature RTP lower than 600 $^{\circ}$C is applied to avoid destroying device.

2.3.2 Experimental Setup

The experimental setup for the current-voltage measurement of devices is illustrated in Fig. 2.12. Both intrinsic and degradation behaviors of the devices can be achieved by this system. Each of the analyzers is connected by the co-axial or tri-axial cable including the semiconductor parameter analyzer (HP 4156C), the low leakage switch mainframe (HP E5250A), the Cascade guarded thermal probe station, and a thermal controller. This facility provides an adequate capability for measuring the low leakage devices I-V characteristic. On the other hand, for precisely measuring of capacitance-voltage characteristic of the devices, LCR Meter (Agilent-HP 4284A) has been added. It provides the testing frequency from 20Hz to 1MHz for AC voltage. These analyzers are controlled by the corresponding software in PC. Therefore, our group developed a control system in HT-Basic language. Through IEEE-488 (GPIB) cable, we can directly give the order to each analyzer. From the above system, the I-V and C-V characteristics of the MOSFET devices can be precisely performed.

2.4 The Discussions of DSS on Performance

2.4.1 Basic Characteristics

The better immunity and lower series source/drain resistance of DSS against conventional MOSFET are shown in Fig. 2.13 (a) and Fig. 2.13 (b), respectively. Fig. 2.14 shows that the I_{on}/I_{off} ratio of DSS provides enhancement of +11% over conventional MOSFET. Fig. 2.15 shows the I_d-V_d characteristics of conventional MOSFET and DSS with channel length ranging from 1um to 55nm. In Fig. 2.16, we can clearly see that the I_d current of DSS demonstrates the enhancement of +15.2% at L= 55nm. Besides, it can significantly be seen that the performance enhancement increases with decreasing channel length. As channel length is down to 0.2um, the enhancement begins to rise rapidly.

The conductance, g_d, is the differential of I_d with respect to V_d. It can be seen as the ability of lifting up I_d with the variation of V_d. Besides, the g_d-V_d curve can be used to define the V_{dsat}, which means the onset of entering saturation region. When V_d reaches V_{dsat}, the I_d current gradually tends to saturation, and I_d current doesn't increase rapidly. As a result, the higher V_{dsat} leads to the later onset of entering saturation region, and I_d current could lift up more highly. In Fig. 2.17, the V_{dsat} is defined by linear extrapolation to x-axis on the g_d-V_d plot.

Figures 2.18 (a) and (b) show the g_d-V_d characteristic of DSS against conventional MOSFET. DSS demonstrates higher g_d at all of ranges and higher V_{dsat} than conventional MOSFET. Consequently, DSS will have a better performance than conventional MOSFET. We can analyze the band diagram in the lateral direction to explain these results. Since the DS layer is added, the Schottky barrier with abrupt gradient is generated at silicide/channel interface. The Schottky barrier triggers carrier

into high energy level state, and thus the transport efficiency will be improved. After carrier entering channel, the high energy state expands the difference between the carrier and the bottom of conduction band. Because of the increasing difference, it will succeed in overcoming the part of scattering mechanism induced by lattice vibration. Therefore, the carrier can pass channel by more easily, and I_d current is late for entering saturation region. As a result, DSS exhibits higher g_d and V_{dsat} than conventional MOSFET.

2.4.2 Analysis on Transport Efficiency

Since the low field mobility decreases seriously at high field, it is commonly believed as the limitation of saturated velocity. In IEDM 2006 [2.2], M. Saitoh utilizes the fixed V_g, V_d and V_{dsat} to maintain the same channel potential profile for inspection of the relation between low field mobility and high field velocity. We also use this experimental setup to observe the difference of the device performance.

As V_d reaches V_{dsat}, the I_d current goes into saturation region, which is termed pinch-off. When V_d continues to increase, the pinch-off point will slide toward the direction of the source, and the increased bias ΔV_d, which is equal to V_d-V_{dsat}, will be applied near drain edge densely. Since the pinch-off occurs, the I_d gain beyond pinch-off with the variation of ΔV_d can be seen as transport efficiency under saturation regime. The scheme is shown in Fig. 2.19.

As mentioned in the previous paragraph, V_{dsat} is a critical parameter to determine I_d. Hence, we could fix V_{dsat} and V_{gov} for estimations of performance between DSS and conventional MOSFET. In Fig. 2.20, high field velocity against low field mobility is plotted at fixed V_{gov}. Exactly, low field mobility is a function of vertical field (refer to V_g) and lateral field (refer to V_d). V_{gov}, the gate overdrive voltage is fixed, thus the

same mobility can be considered to be the same condition of band bending in the channel, which means at the same V_{dsat}. This plot shows these two curve have more significant split with decreasing channel length, but the difference of mobility retains a nearly range.

We can utilize channel band diagram of DSS in lateral direction shown in Fig. 2.21 to explain the discrepancy. At low field, low V_d is applied in the lateral direction which is too small to not help plenty carrier climb over the Schottky barrier, the transport mechanism at Schottky barrier interface is dominated by the tunneling. Thus a little part of carrier overcomes barrier height and goes into high energy state to enhance mobility at low field. As V_d increases into high field regime, a large number of carrier travels easily over Schottky barrier, and then enters channel. The carrier has enough energy to transport through channel, it is considered that the probability of transporting into drain should be larger as channel length decreases due to lower scattering impact. As a result, the difference of high field velocity with respect to DSS and conventional MOSFET increases with decreasing channel length. This enhancement of the velocity will be discussed by ballistic theory in the next two chapters.

(a)

(b)
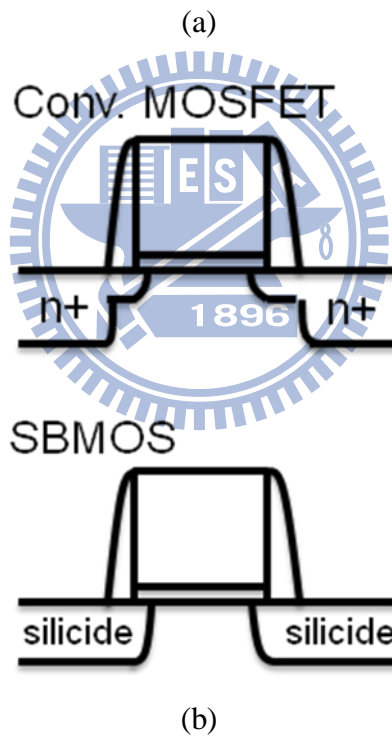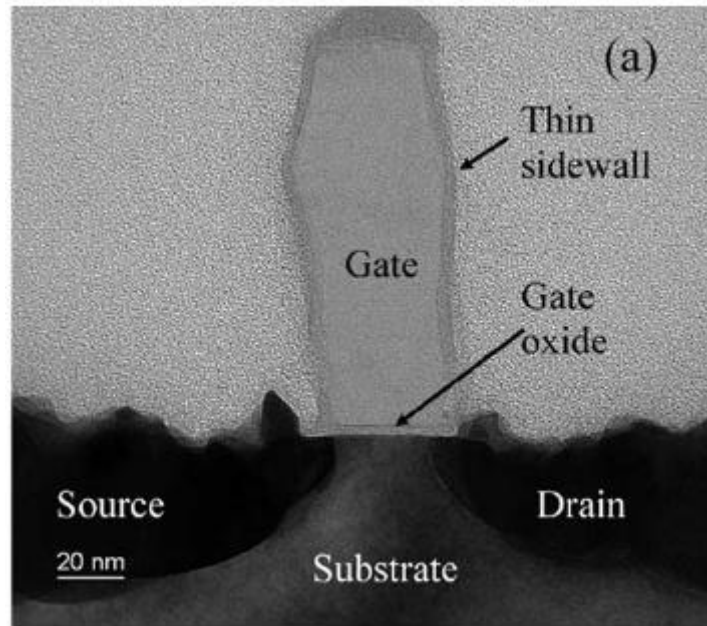
Fig.2.1 (a) TEM graph of SBMOS and (b) schematic structure of conventional MOSFET and SBMOS.

- STI or LOCOS formation
- Well implantation
- Gate stack formation
- Sidewall spacer formation
- Silicidation
- Back-end process

Fig.2.2 The schematic process flow of SBMOS fabrication.
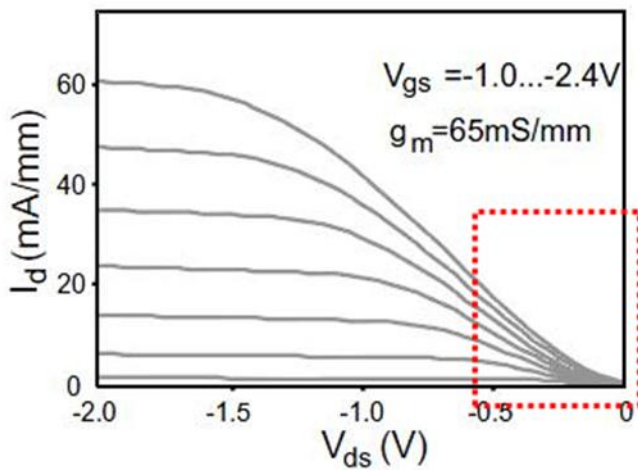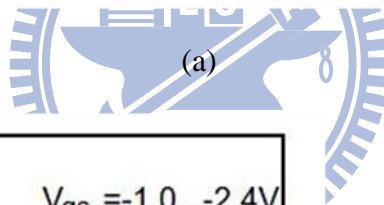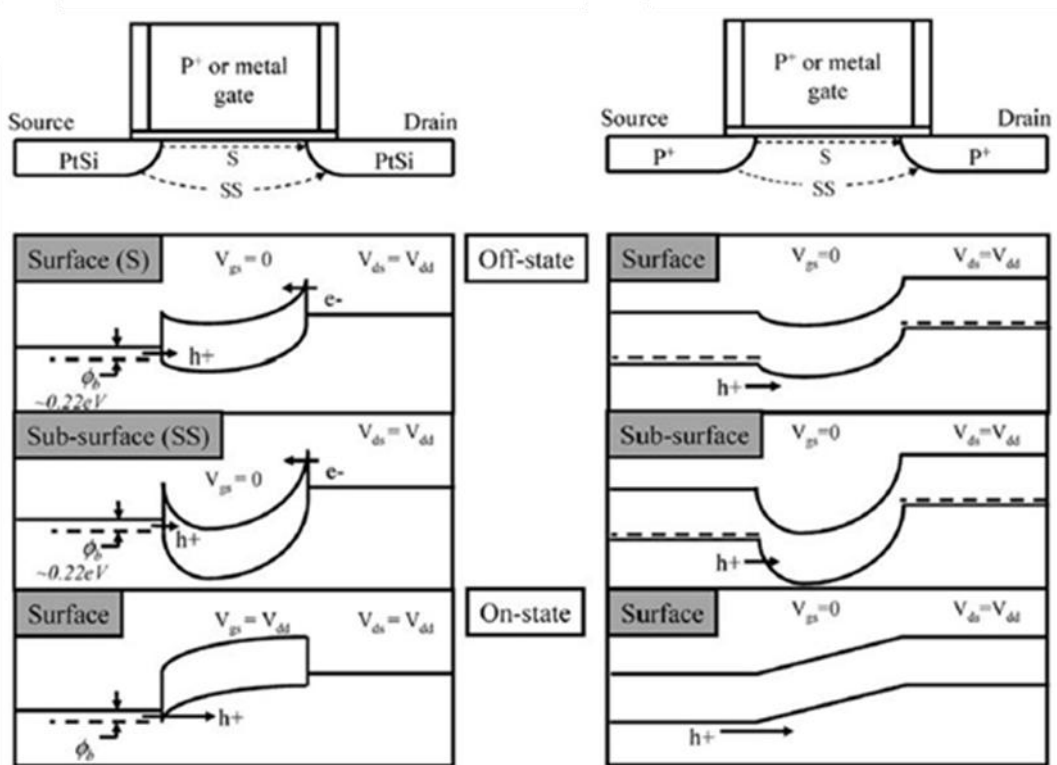
Fig.2.3 (a) The band diagram on the varied state of operation in p-type

SBMOS. (b) The I_d-V_d characteristic at on-state.

(a)

(b)

Fig.2.4 (a) The band diagram on the varied state of operation in n-type SBMOS. (b) The I_d-V_d and I_d-V_g characteristics at on-state.

DS layer

(a)

silicide   Si(n+)   Si(p)

DS layer

(b)

Fig.2.5 (a)TEM graph of DSS. (b) Band diagram of n-type DSS, and the

dash line represents that of SBMOS.

STI Formation
Gate Stack Formation
Disposable Spacer Formation
Deep S/D Implantation
Disposable Spacer Removal
Offset Spacer Formation
Halo I/I

Conv. FET	DSS
Extension I/I	**Dopant Segregation I/I**
Spacer Formation	

NiSi
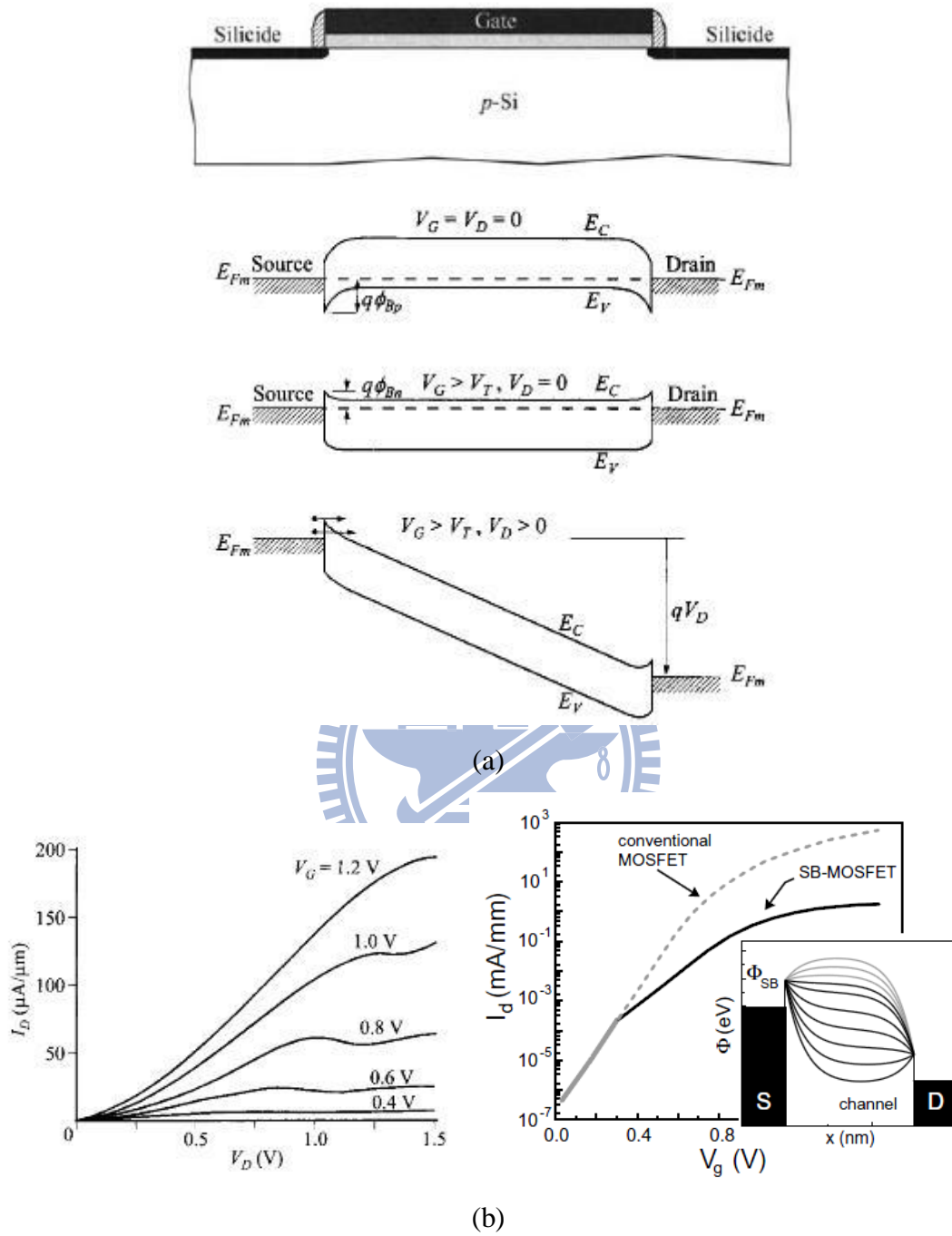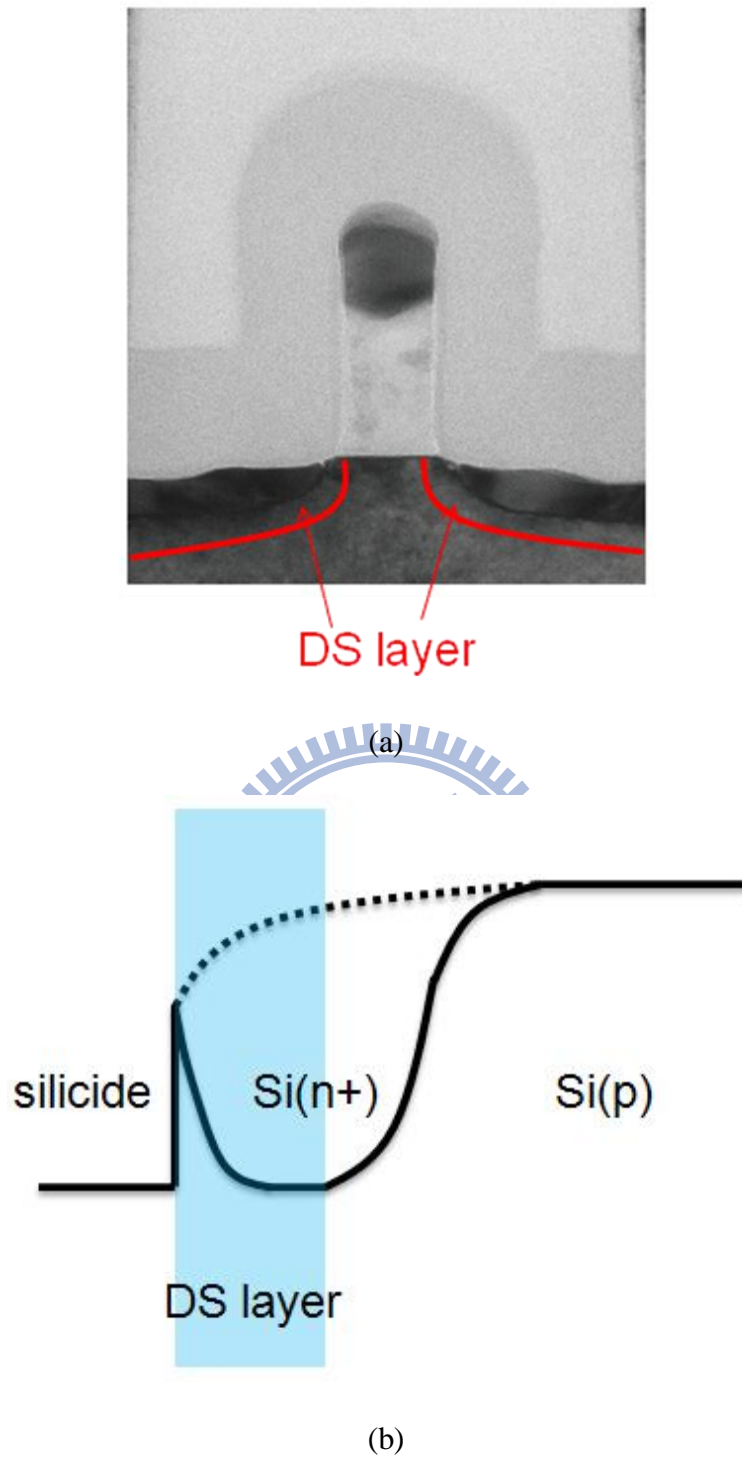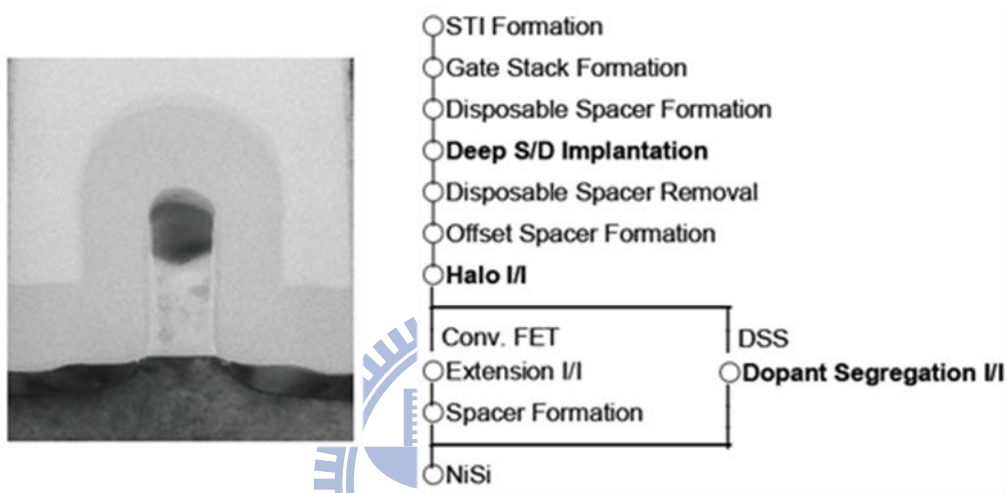
T. Kinoshita et al., IEDM 2006, Toshiba

1896

Fig.2.6   The schematic process flow in DSS fabrication.

(a)

(b)
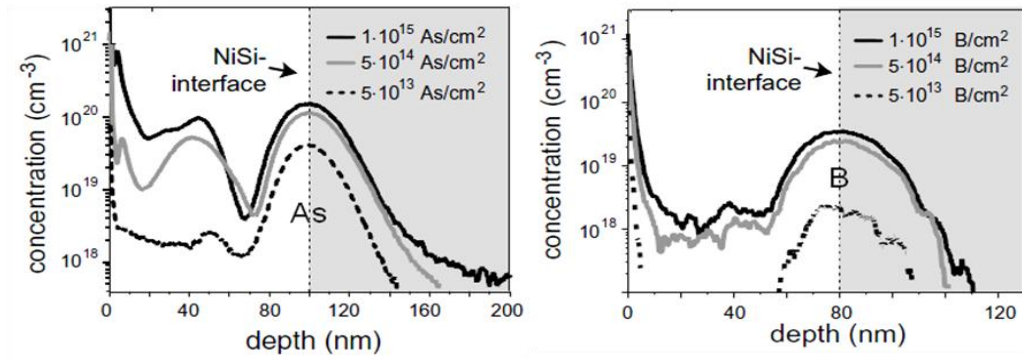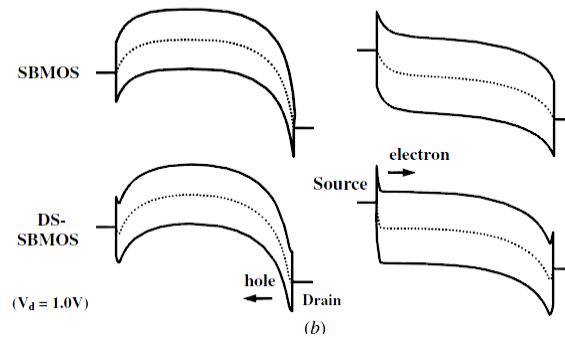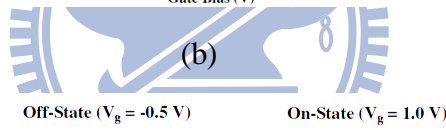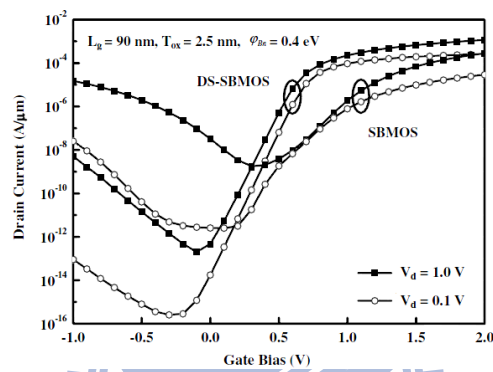
(c)

Fig.2.7 (a) The SIMS profile of doping distribution under snowplow

effect. (b) The performance of DSS comparing with SBMOS.

(c) The difference of band diagram between DSS and SBMOS.

(a)
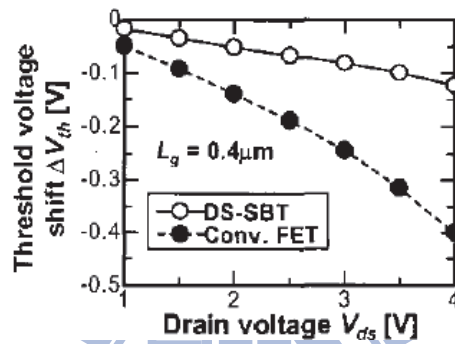
(b)
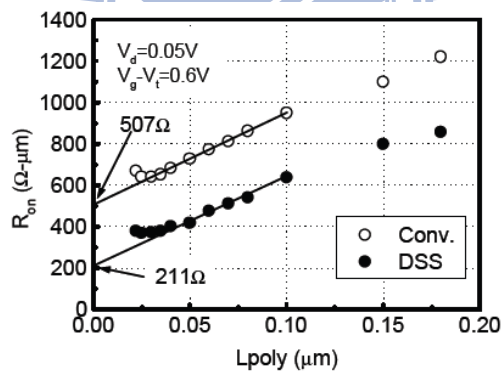
(c)

Fig.2.8 DSS exhibits (a) better immunity of the short channel effect, (b) DIBL characteristic and (c) series source/drain resistance than conventional MOSFET.

Fig.2.9 DSS shows higher I_{on}/I_{off} ratio than conventional MOSFET.

(a)

(b)

Fig.2.10 (a) The enhancement of velocity in DSS in comparison to the conventional MOSFET which increases with reducing channel length. (b) DSS shows more significant behavior of velocity overshoot than conventional MOSFET.

23

(a)

- STI formation
- Gate Stack formation
- Offset Spacer formation
- Halo Pocket implantation
- Dopant Segregation implantation
- Disposable Spacer formation
- S/D implantation
- RTP Annealing
- Disposable Spacer Removal
- NiPt Silicidation
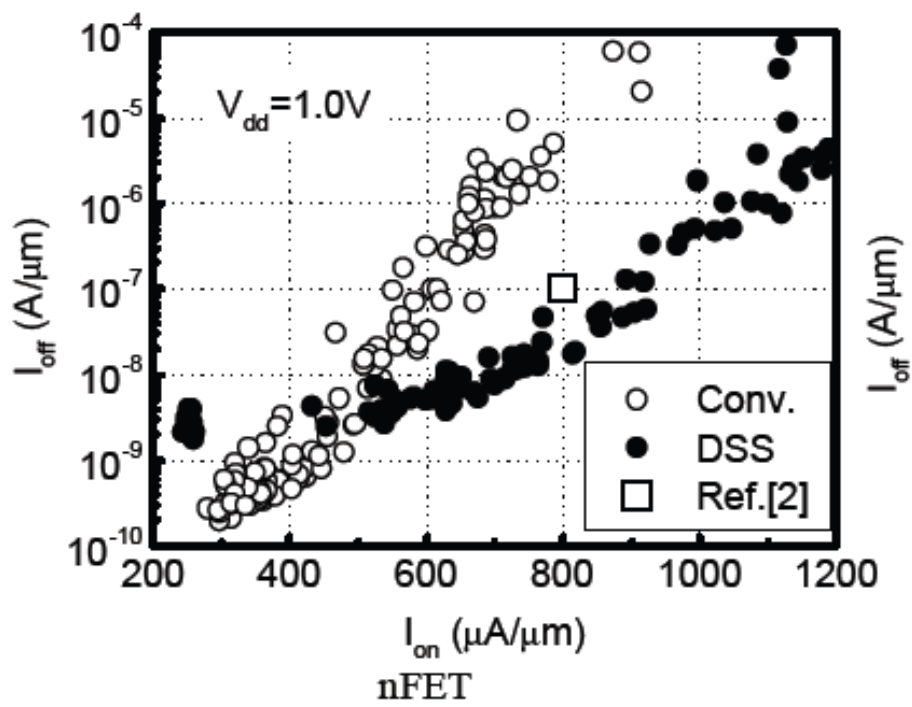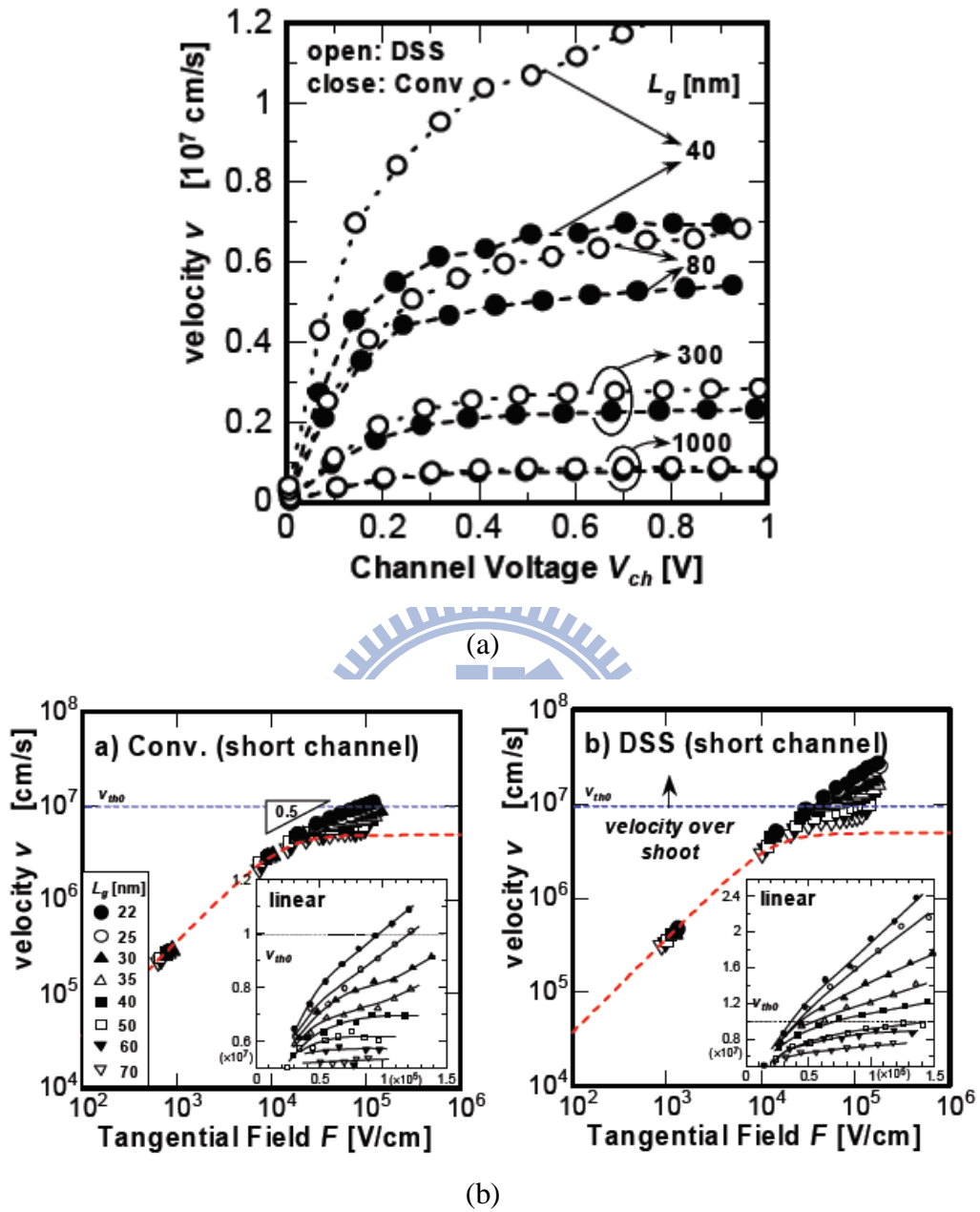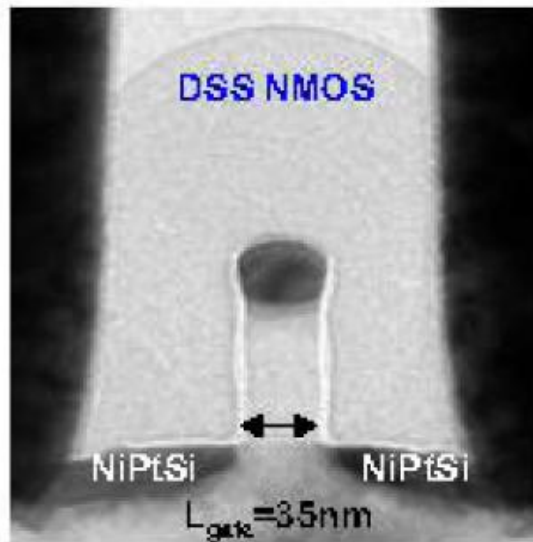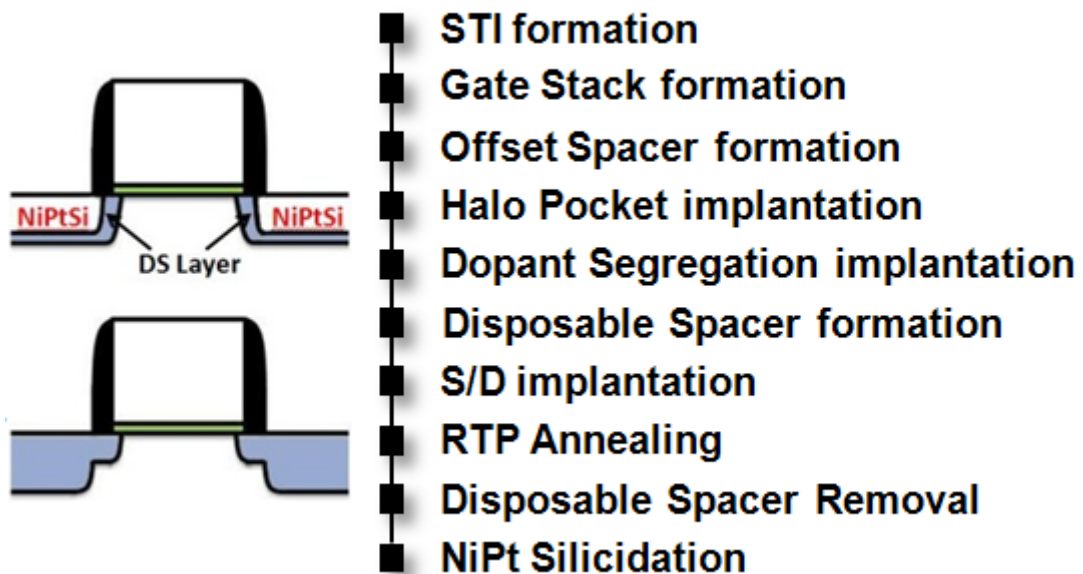
(b)

Fig.2.11 (a) The TEM graph of n-type DSS for our experiments. (b) The schematic process flow of DSS based on 65nm technology node of UMC.
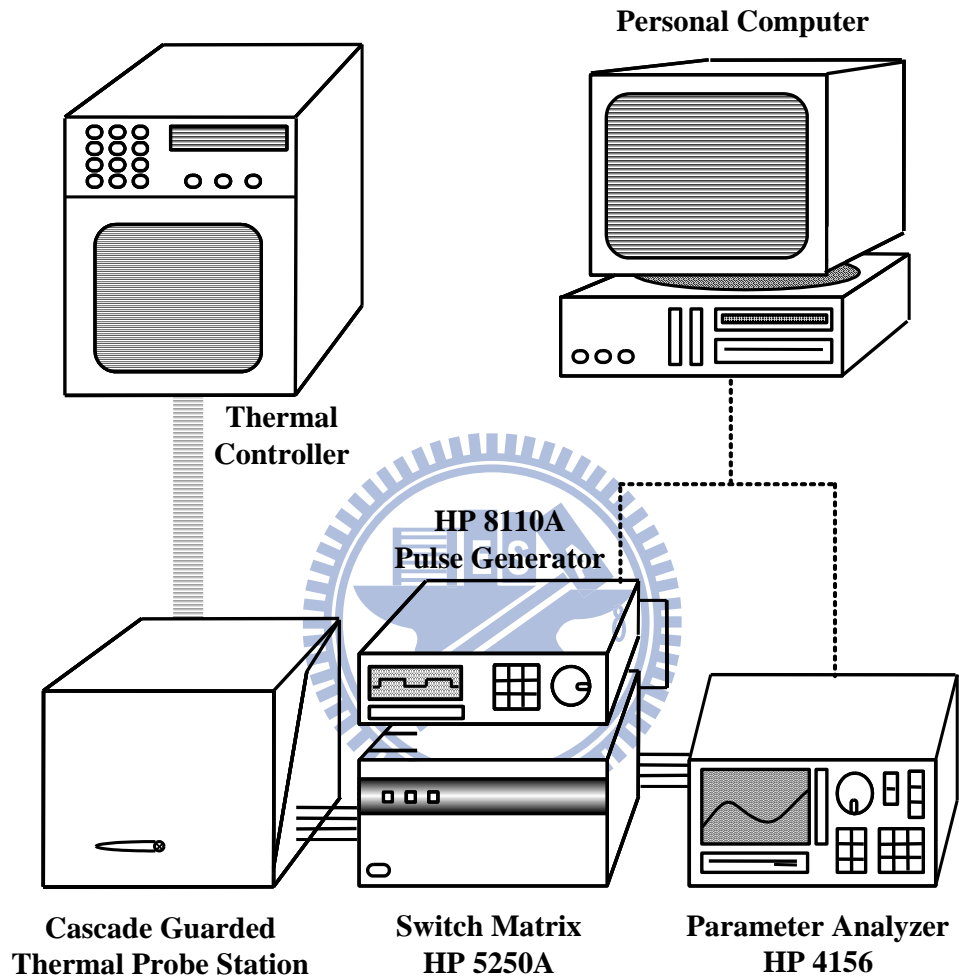
Fig.2.12 The experimental system of current-voltage (I-V) for both
n-type or p-type MOSFET.
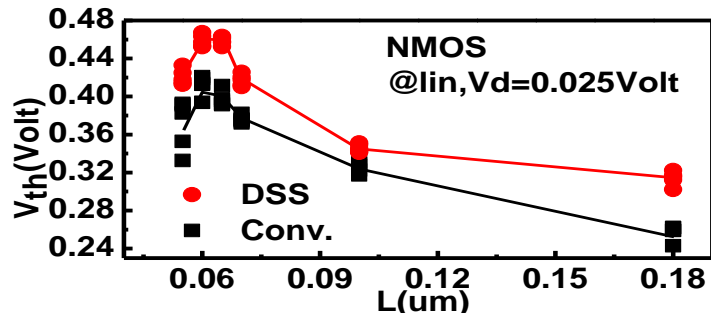
(a)
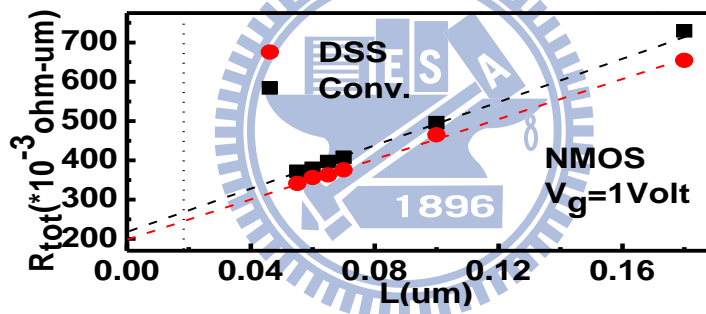
(b)

Fig.2.13 DSS shows the better immunity to short channel effect and the lower series source/drain resistance than conventional MOSFET one.
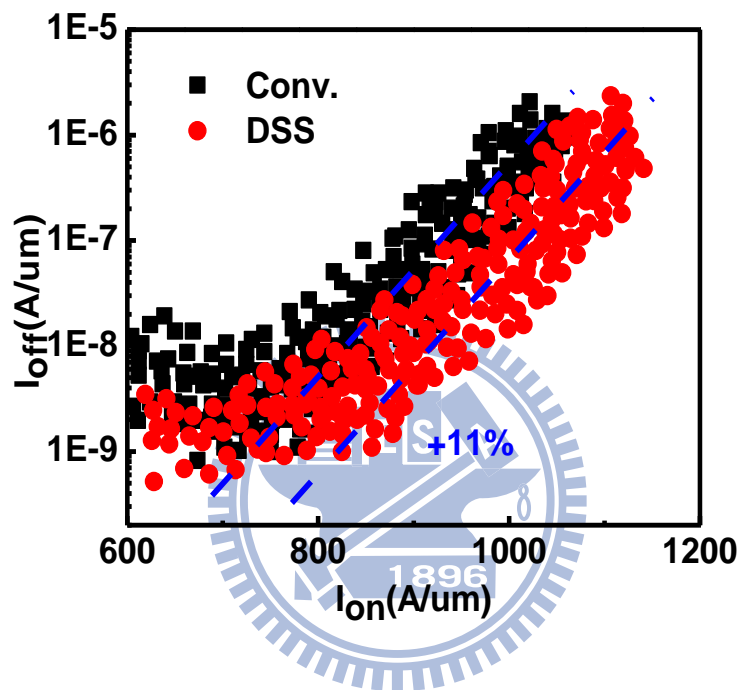
Fig.2.14 I_{on}/I_{off} ratio of DSS shows 11% enhancement over conventional
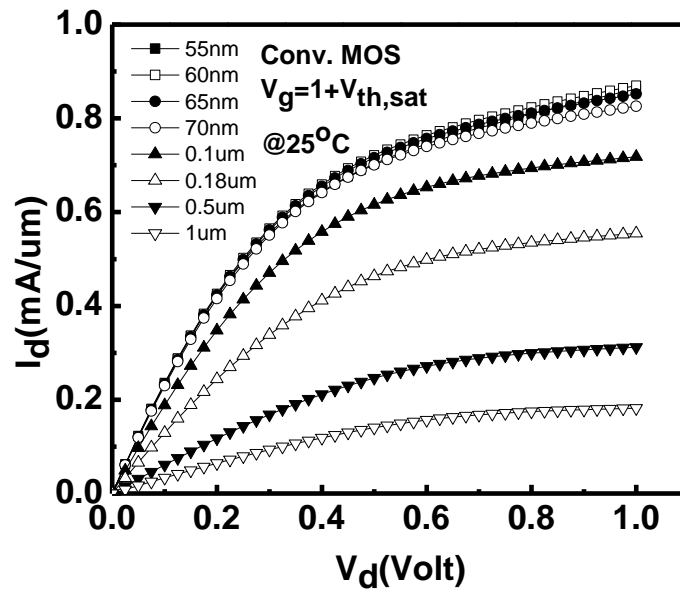
MOSFET.

(a)
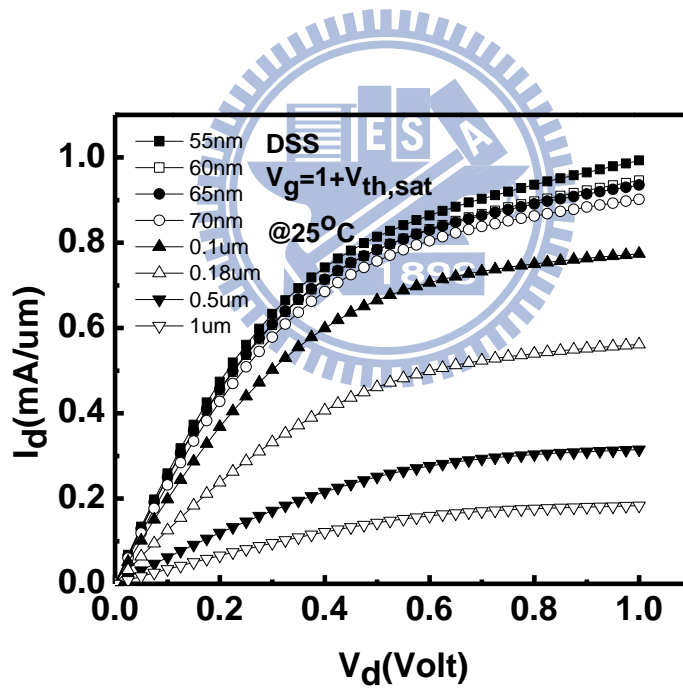
(b)

Fig.2.15 I_d-V_d characteristics of (a) conventional MOSFET and (b) DSS.

(a)
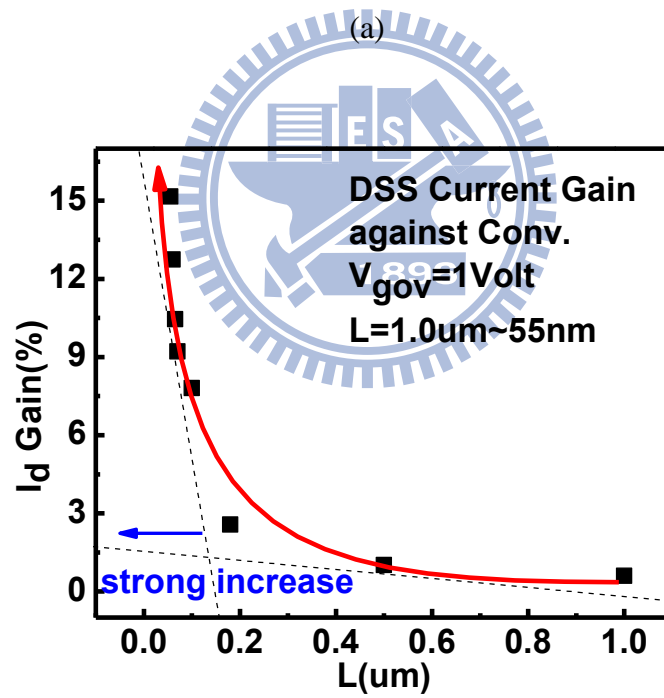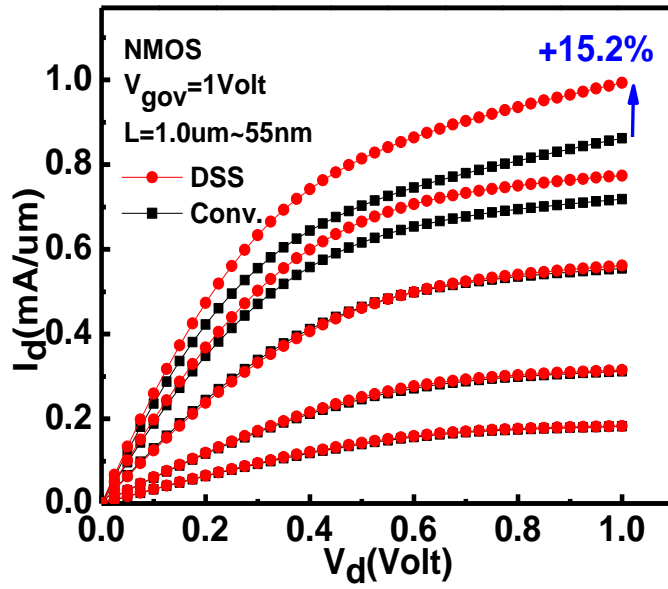
(b)

Fig.2.16 (a) I_d-V_d characteristic of DSS comparing to conventional MOSFET, and (b) DSS shows strong enhancement under short channel regime.
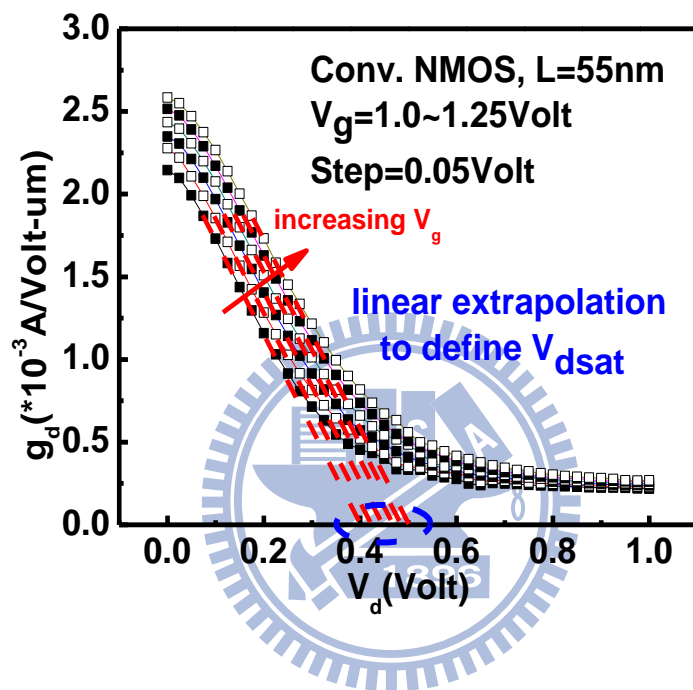
Fig.2.17 V_{dsat} is defined by linear extrapolation to x-axis from g_d-V_d curve.

(a)

(b)
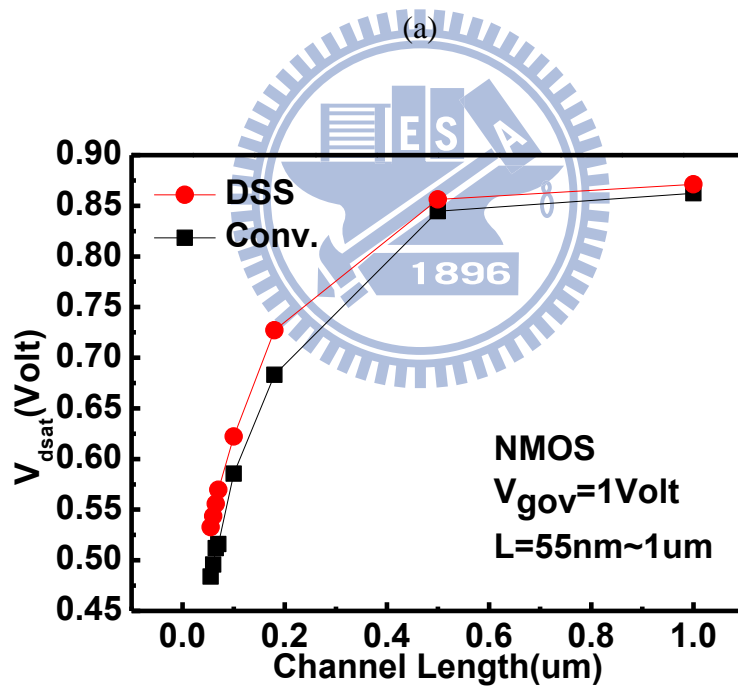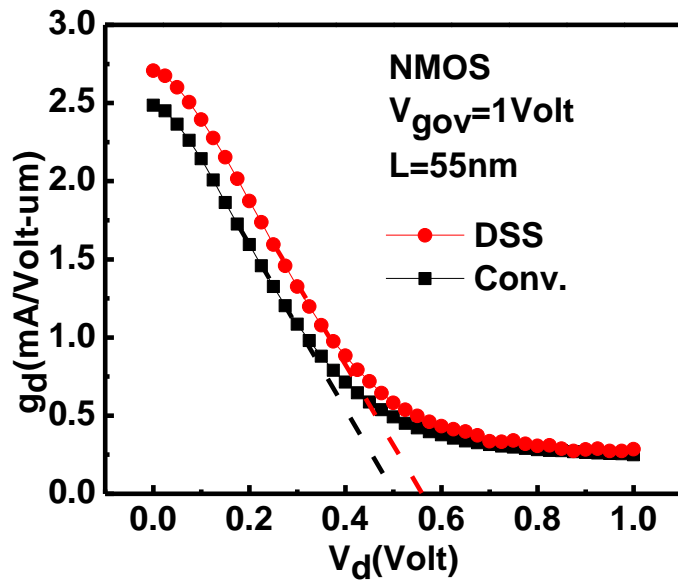
Fig.2.18 (a) g_d-V_d characteristics of conventional MOSFET and DSS. (b) V_{dsat} of DSS shows larger value than that of conventional MOSFET.
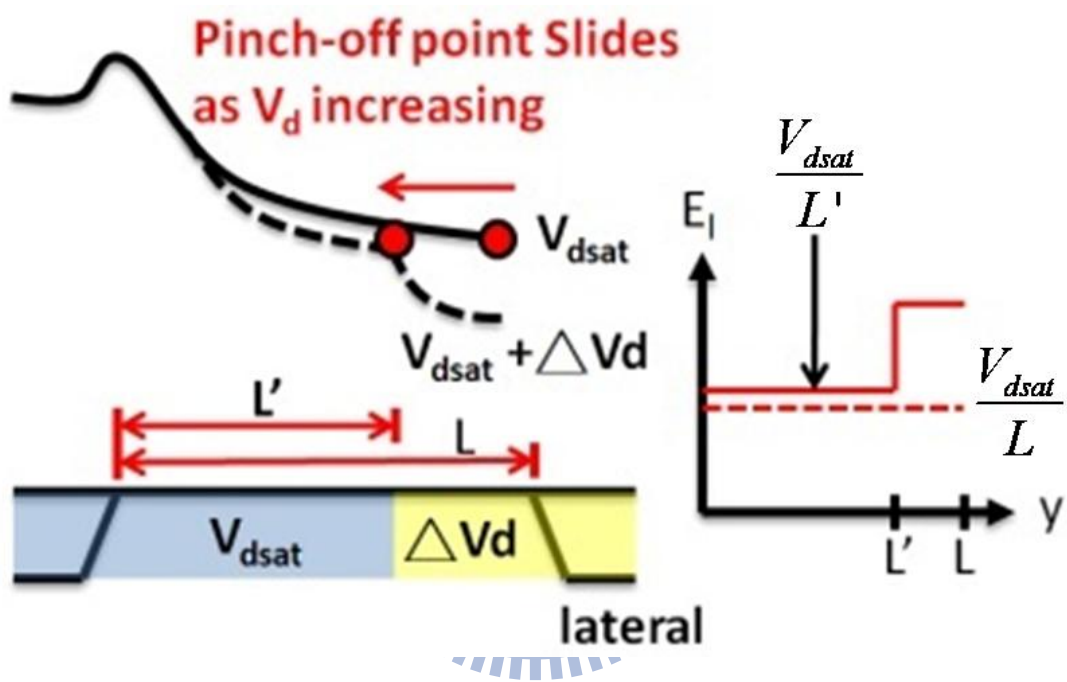
Fig.2.19 Band diagram on channel along the lateral direction.
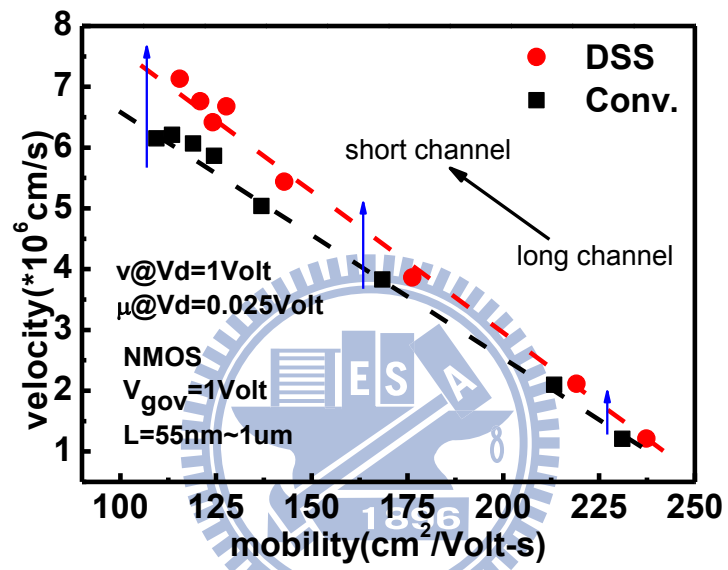
Fig.2.20 The plot of high field velocity versus low field mobility at fixed V_{gov}.
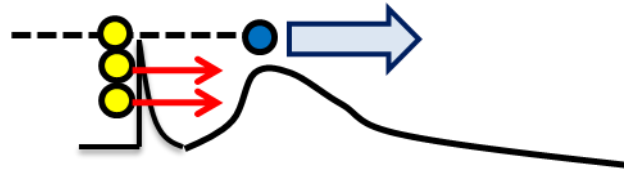
(a)
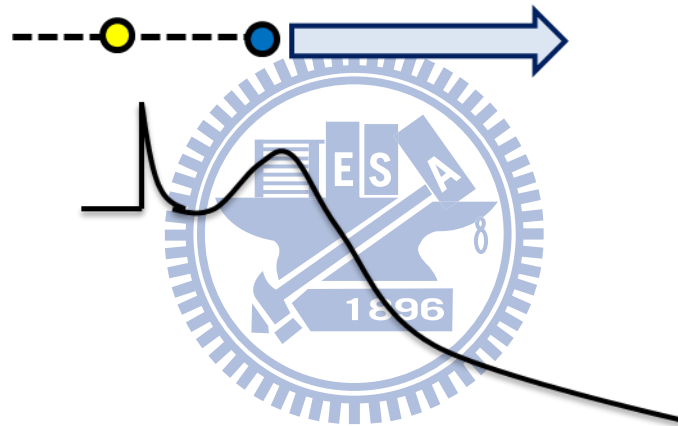
(b)

Fig.2.21   Channel band diagrams of DSS operated at (a) low field and (b)
high field.

Chapter 3

Fundamentals of Ballistic Transport Theory

Semiconductor devices have been scaled down to the nano-scale region, and entered the quasi-ballistic regime. Because of the physical limitations of carrier transport, the drift-diffusion model for describing carrier transport becomes less significant in the nano-scale MOSFET. From the quasi-ballistic toward ballistic region, Natori brought up a new insight for modeling the carrier transport phenomenon, which is called ballistic theory or backscattering theory in 1994 [3.1]. Later in 1997, Lundstrom developed the complete theorem to explain the physical meaning of the ballistic transport phenomenon in nano-scale MOSFET [3.2].

3.1 Introduction of Ballistic Theory

3.1.1 Backscattering Principle and Current Transport Model

In ballistic theory, we treat the moving carriers as the quantum wave. This kind of wave goes through channel from the source to the drain. When the waves move toward the channel, they bomb into a non-negligible quantum barrier which leads to transmission and reflection in quantum mechanics. In saturation region of MOSFET, the channel barrier is like the shape of hills. The length ℓ is called critical length, which means the potential drops $k_B \cdot T$ from the edge of source to channel, where k_B is the Boltzmann constant and T is the temperature in Kelvin coordinates. In the critical length, the carrier suffers from strong resistance induced by the scattering mechanism. Thus, the longer ℓ results in the carrier suffers from the stronger scattering mechanism. The scattering mechanism in the channel is brought by

impurity scattering, lattice vibration, and surface roughness. The mean-free-path λ of carrier in the channel means the expected length of carrier transporting through channel. The longer λ responds to the better transport efficiency. As a result, when the carrier enters channel, the probability of reaching drain is determined by the relation of ℓ and λ. We can define the backscattering coefficient r_c, in which the probability of the carrier bounced back to source, as following:

$$r_c = \frac{\ell}{\ell + \lambda} = \frac{1}{1 + \lambda/\ell} \qquad (3.1)$$

On the other hand, it also can be represented the probability of the carrier passing through channel. The ballistic efficiency, which called B_{sat} is given by:

$$B_{sat} = \frac{1 - r_c}{1 + r_c} \qquad (3.2)$$

In 1997, Lundstrom presented a simple scattering model based on the ballistic theory for carrier transport. Under the operation, the two-section model is shown in Fig. 3.1 (a). The source is treated as a reservoir of carriers which injects a flux a_s into the channel, and the flux a_D represents the carriers which succeeded to be collected by drain. We can more clearly see the mechanism of carrier transport in Fig. 3.1 (b).

The fraction t_s means the source flux which transmits across the barrier at source/channel interface, and enters the channel. The fraction t_c of flux, which injects into the channel, and exists in drain, represents the transport efficiency of carrier. Thus, the fraction r_c, which means the backscattering coefficient, is defined as $r_c = 1 - t_c$. The flux a_s before injecting into channel can be written by:

$$a_s(0) = n(0, z) \cdot v_{inj} \qquad (3.3)$$

where v_{inj} is the injection velocity in the lateral direction and n is the density of carrier in the source reservoir. Then, the Eq. 3.3 links up t_s and r_c, and we can rearrange the equations as the following:

$$a_s(0) = a_s t_s + a_s t_s r_c \tag{3.4}$$

$$1 = t_c + r_c \tag{3.5}$$

Through the transmission of fraction t_c, a_D can be represented by:

$$a_D = a_s t_s t_c \tag{3.6}$$

Substituting Eq. 3.4 and Eq. 3.5 into Eq. 3.6, and integrating a_D with respect to the channel width. We can obtain the I_d equation under the ballistic theory.

$$I_d = q \cdot W \cdot \int_0^W a_D dz = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot v_{inj} \cdot \left(\frac{1 - r_c}{1 + r_c} \right) \tag{3.7}$$

The I_d equation also can be written as:

$$I_d = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot v_{inj} \cdot B_{sat} \tag{3.8}$$

This equation represents the transport efficiency of carrier in the channel, which provides us a simple current expression without invoking the unpredictable mobility. In the ultimate of ballistic theory, the B_{sat} tends to 1 and I_d will be fully controlled by v_{inj}.
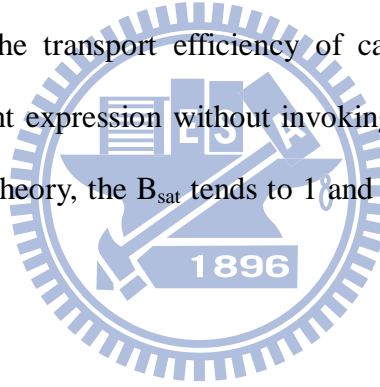
3.1.2 Injection Velocity

The maximum value of velocity under classical thermal equilibrium is simply defined as thermal velocity, $v_{T0} = \sqrt{\dfrac{2k_BT}{\pi m^*}}$. The random velocity can exceed this thermal limit due to quantum mechanism effect, and this behavior is induced by degeneracy of carrier. Thus, the average carrier energy is triggered to the high energy state, and the carrier will have higher velocity than thermal velocity. The ballistic theory assumes the thermal velocity on carrier degeneracy to be the injection velocity (v_{inj}). As a result, the v_{inj} is given by:

$$v_{inj} = v_{T0} \cdot \frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)} = \sqrt{\frac{2k_BT}{\pi m^*}} \cdot \frac{\Im_{1/2}(\eta_F)}{\ln(1+e^{\eta_F})} \qquad (3.8)$$

$$\eta_F = \left(E_F - E_n\right)/k_BT \qquad (3.9)$$

where $\Im_{1/2}$ is the Fermi-Dirac integral.

When the operation is in the weak inversion, Eq. 3.8 is reduced to $v_{inj} = v_{T0}$. The simulation result of Eq. 3.8, considering the occupation of single valley in band structure, is shown in Fig. 3.2 (a). The v_{inj} demonstrates the significant trend with respect to the surface density. When gate bias continues to increase beyond the threshold voltage, the strong accumulation of inversion charge will raise surface density up. As a result, the behavior, which v_{inj} exceeds v_{T0}, is observed.

Besides, we have found another approximate equation for expressing the v_{inj} under the state of degeneracy. The equation is given by:

$$v_{inj} = \frac{8\hbar}{3m^*} \cdot \sqrt{\frac{C_{ox}(V_g - V_{th})}{2\pi q}} \qquad (3.10)$$

Fig. 3.2 (b) shows the result of v_{inj} versus n_s, which is based on Eq. 3.10.

3.2 Ballistic Efficiency with Temperature Dependent Properties

3.2.1 Temperature Dependent Parameters

The ratio of λ and ℓ is the important element for determination of B_{sat}, and is a function of temperature. From Eq. 3.8, we can see that the v_{inj} is also dependent on temperature. Thus, Chen developed a model with respect to temperature for calculating r_c or B_{sat} [3.3]. Through rearranging Eq. 3.1 and Eq. 3.7, the I_d equation can be rewritten by:

$$I_d = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot v_{inj} \cdot \left(\frac{\lambda/\ell}{2 + \lambda/\ell} \right) \tag{3.11}$$

where $\left(\dfrac{\lambda/\ell}{2 + \lambda/\ell} \right)$ is equal to B_{sat}.

In Eq. 3.11, there are several parameters which are related to temperature, and we list those below.

1. Injection velocity, v_{inj}

$$v_{inj} = \sqrt{\frac{2k_B T}{\pi m^*}} \cdot \frac{\Im_{1/2}(\eta_F)}{\ln(1 + e^{\eta_F})} \propto T^{\frac{1}{2}} \tag{3.12}$$

2. Critical length, ℓ

$$\ell \approx \frac{k_B \cdot T}{q} \cdot \frac{L}{V_d} \propto T \tag{3.13}$$

where L is channel length.

3. mean-free-path, λ

At first, we need to know the relation between v_{inj} and λ. This relation can be derived from the Einstein relation, and is given by:

$$\lambda = \frac{2\mu_0 \cdot k_B T/q}{v_{inj}} \tag{3.14}$$

And, the μ_0 is also a function of temperature.

$$\mu_0 \propto T^{-1.5} \tag{3.14}$$

As a result, we have found the relation with respect to temperature.

$$\lambda = \frac{2\mu_0 \cdot k_B T/q}{v_{inj}} \propto T^{-1} \tag{3.15}$$

4. threshold voltage, V_{th}

The relation of V_{th} and temperature will be calculated by the practical measurements.

3.2.2 Derivation and Application of Temperature Dependent Current Equation

Eq. 3.12, Eq. 3.13, Eq. 3.15 and $V_{th}(T)$ are replaced in Eq. 3.11, and we differentiate I_d equation with respect to temperature.

$$\frac{\partial I_d}{\partial T} = I_d \cdot \left\{ \frac{1}{v_T} \cdot \frac{\partial v_T}{\partial T} + \frac{2 + \lambda/\ell}{\lambda/\ell} \cdot \frac{\partial}{\partial T} \left(\frac{\lambda/\ell}{2 + \lambda/\ell} \right) + \frac{1}{V_g - V_{th}} \cdot \frac{\partial}{\partial T} \left(V_g - V_{th} \right) \right\}$$

$$\rightarrow \frac{\partial I_d}{\partial T} = I_d \cdot \left\{ \left(\frac{1}{2} - \frac{4}{2 + \lambda/\ell} \right) \cdot \frac{1}{T} + \frac{1}{V_g - V_{th}} \cdot \frac{\partial}{\partial T} \left(V_g - V_{th} \right) \right\} \tag{3.16}$$

Then, Eq. 3.16 can be simplified as the following:

$$\frac{\partial I_d}{\partial T} = I_d \cdot \alpha \tag{3.17}$$

And, we rearrange the α equation from Eq. 3.16 and Eq. 3.17. The equation can be obtained as below.

$$\frac{\lambda}{\ell} = \left\{ 0.5 - \alpha \cdot T + \frac{1}{V_g - V_{th}} \cdot \frac{\partial (V_g - V_{th})}{V_g - V_{th}} \right\} \tag{3.18}$$

Afterward, the Eq. 3.17 and Eq. 3.18 will be used to calculate the B_{sat} and r_c in different devices, which is generally called Temperature Dependent Method (TDM).

In the beginning of using TDM, we need to calculate α by measurements. Fig. 3.3 shows the relation of I_d and T, and the parameter α which means the slope of the

curve is calculated. Then, substitute α into Eq. 3.18, we can find the ratio of λ and ℓ, and B_{sat} will be calculated through Eq. 3.11.

In the paper that Chen proposed, the Id equation with considering series source/drain resistance can be rewritten by:

$$I_d = W \cdot C_{ox} \cdot (V_g - V_{th} - 0.5 \cdot I_d \cdot R_{SD}) \cdot v_{inj} \cdot B_{sat} \qquad (3.19)$$

where $I_d \cdot R_{SD}$ is the voltage consumption induced by series source/drain resistance.

Figure 3.4 shows that the B_{sat} and r_c in conventional MOSFET at L= 65nm are calculated by TDM. As temperature increases, the B_{sat} decreases due to the strong thermal scattering. Fig. 3.5 shows the results of v_{inj}, r_c and λ with respect to gate bias, which are calculated by TDM.

3.3 Experimental Results

3.3.1 Ballistic Efficiency

In this section, we use the TDM to calculate B_{sat}, the ballistic efficiency, and compare the results of DSS with that of conventional MOSFET. Fig. 3.6 and Fig. 3.7 show the results of B_{sat} with respect to temperature in conventional MOSFET and DSS, respectively. The same trend with increasing temperature, both devices demonstrate the behavior of decreasing B_{sat}. But we also observe some values of B_{sat} in conventional MOSFET at L= 1um is lower than 0. This means that all carriers could not be injected into channel even on on-state operation. Actually, we have the data of I_d, which is greater than 0. Thus, the negative B_{sat} calculated by TDM is observed, and we will discuss it in the next chapter.

Besides, we can find that the B_{sat} of DSS is slightly higher than that of

conventional MOSFET. Fig. 3.8 provides us a more clear result of B_{sat} with respect to channel length at the fixed temperature, and demonstrates that DSS has higher B_{sat} in all range. At L= 1um, the B_{sat} difference between DSS and conventional MOSFET is the highest, and the difference decreases with decreasing channel length.

3.3.2 The Ratio of Mean-Free-Path and Critical Length

The ratio λ / ℓ is calculated by Eq. 3.11. Because the ratio is proportional to B_{sat}, we will obtain the result of λ / ℓ versus channel length approaching that of B_{sat} versus channel length. Fig. 3.9 and Fig. 3.10 show the results of λ / ℓ with respect to temperature in conventional MOSFET and DSS, respectively.

Moreover, we continues to calculate the estimated value of λ which is obtained by Eq. 3.14. In Eq. 3.14, there are two unknown parameters at present, which are μ_0 and v_{inj}. The low field mobility μ_0 is calculated by g_d method as shown below.

$$I_{d,lin} = W \cdot C_{ox} \cdot \left(V_g - V_{th}\right) \cdot \mu \cdot \frac{V_d}{L}$$

$$\rightarrow g_d = \frac{\partial I_{d,lin}}{\partial V_d} = \frac{W}{L} \cdot C_{ox} \cdot \left(V_g - V_{th}\right) \cdot \mu$$

$$\rightarrow \mu = \frac{g_d \cdot L}{W \cdot C_{ox} \cdot \left(V_g - V_{th}\right)} \tag{3.20}$$

where C_{ox} is the capacitance of gate dielectric which is estimated by split-CV measurement. And through the I_d equation, the v_{inj} can be obtained after B_{sat} and C_{ox} are calculated.

Thus, λ versus channel length which is calculated by TDM will be obtained, as shown in Fig. 3.11. DSS demonstrates the higher value than conventional MOSFET from long channel region to short channel region. In the long channel region, the

difference between DSS and conventional MOSFET is the largest. As channel length decreases, the difference gradually disappears.

3.3.3 Injection Velocity

We can calculate v_{inj} once B_{sat} and C_{ox} are found. The v_{inj} is treated as an important performance criterion. From the I_d equation, we understand that the higher v_{inj} may lead to higher I_d. Besides, the v_{inj} will dominate the I_d current when B_{sat} approaches one.

The result of v_{inj} is shown in Fig. 3.12. We first look at the curve of conventional MOSFET. The curve doesn't show the uniform trend with respect to channel length. We need to see the equation of v_{inj}. In Eq. 3.12, we observe that the v_{inj} is not a function of channel length, and is only dependent on temperature, the effective mass and the level of carrier degeneracy. This conclusion is consistent with the curve of conventional MOSFET in our measurement.

Then, we see the curve of DSS. It was found that the curve is strongly dependent on the channel length. When channel length decreases, the v_{inj} has a significant trend which is rising up. This point receives our attention because the abnormal trend of v_{inj} may be induced by the model errors in TDM. We suppose that one or two temperature dependent models are not suitably applied in DSS, which results in the wrong v_{inj} estimation. Because of the model errors, the TDM can't be applied to the case of DSS. Thus, the estimations including B_{sat}, λ and v_{inj} are needed to be calculated by another way.
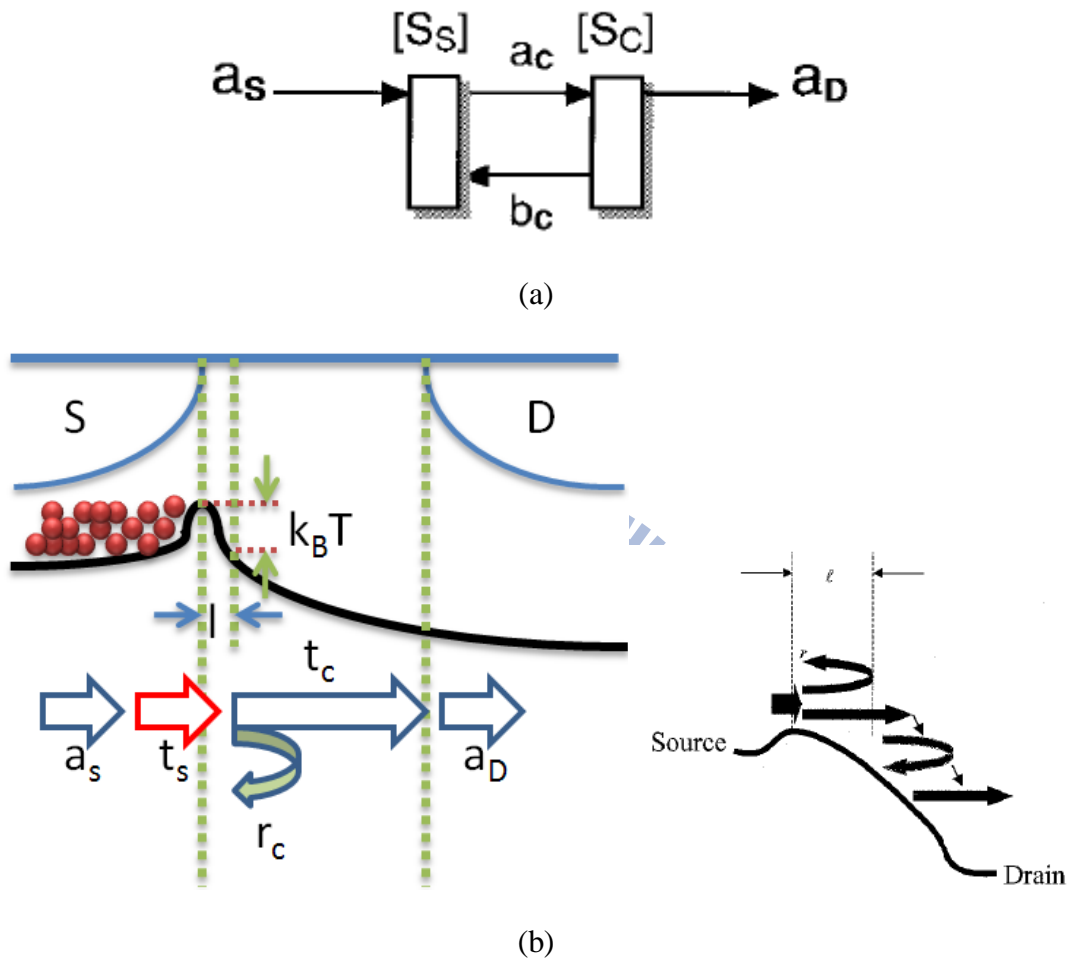
Fig.3.1 (a) The two-section model for backscattering theory. (b) The schematic graph of carrier transport in the lateral band diagram.
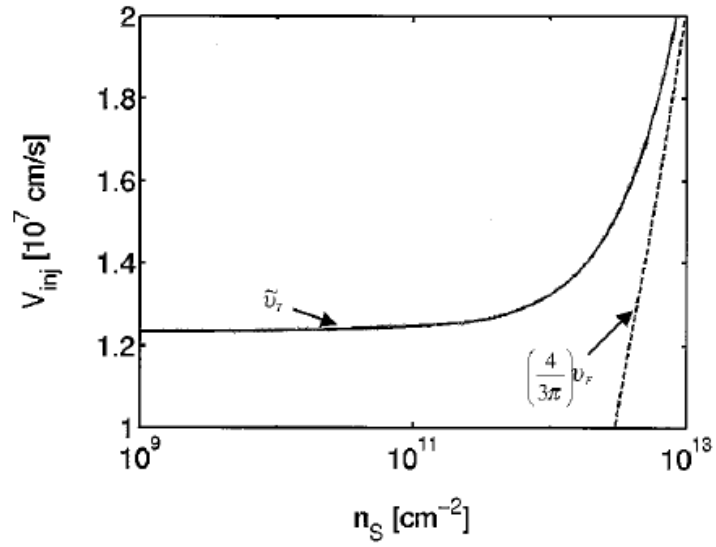
(a)
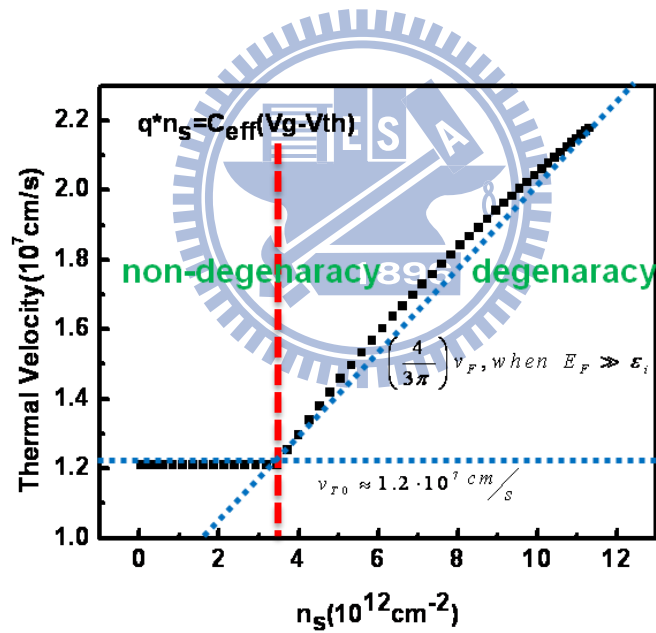
(b)

Fig.3.2 (a) The result of simulation and (b) that of approximate equation

on v_{inj} versus surface density.
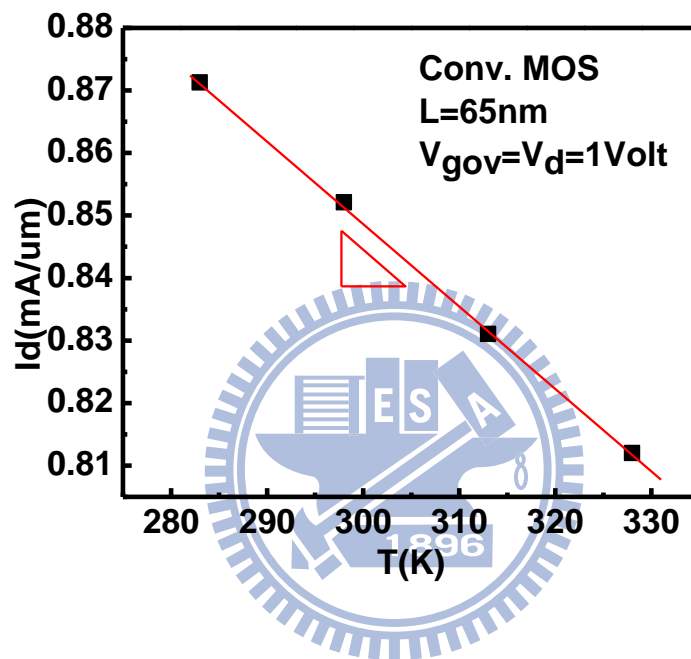
Fig.3.3 The relation between I_d current and temperature is used for TDM.
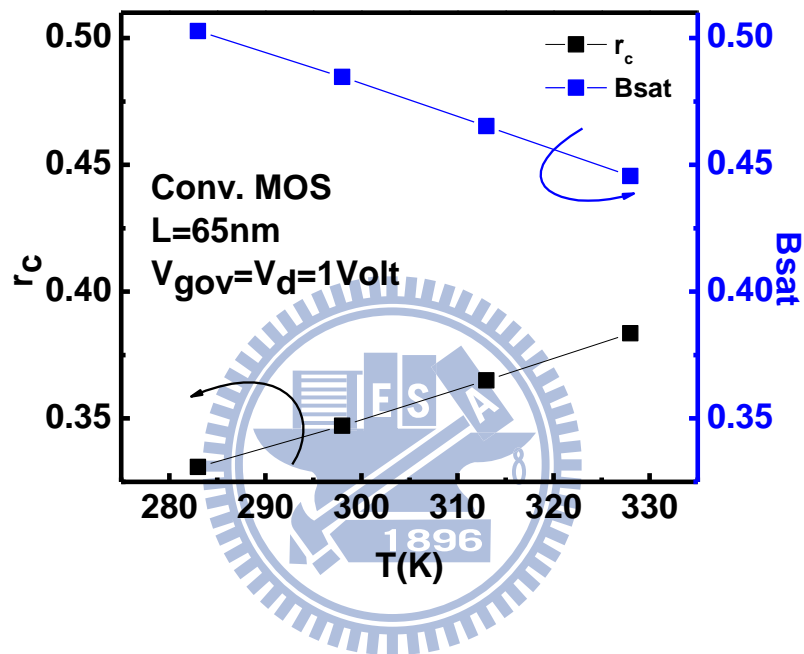
Fig.3.4 The B_{sat} and r_c in conventional MOSFET at L= 65nm are calculated by TDM.
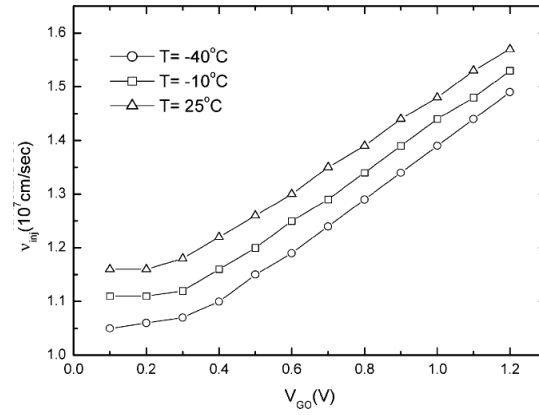
(a)
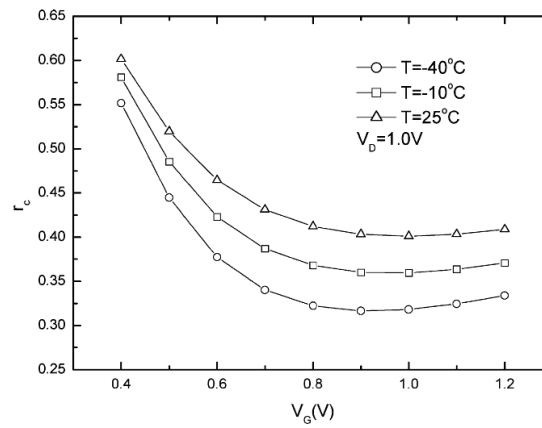
(b)
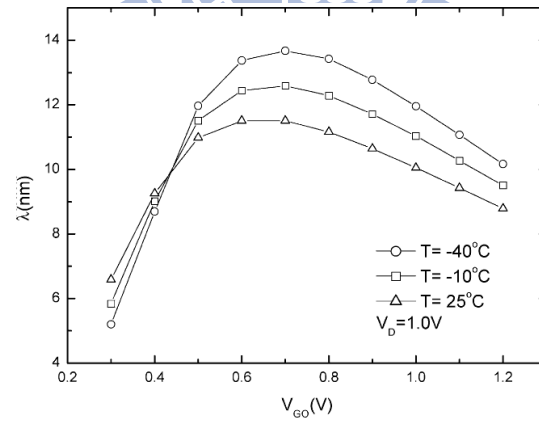
(c)

Fig.3.5 The related parameters are calculated by TDM. (a) v_{inj}. (b) r_c.

(c) λ.
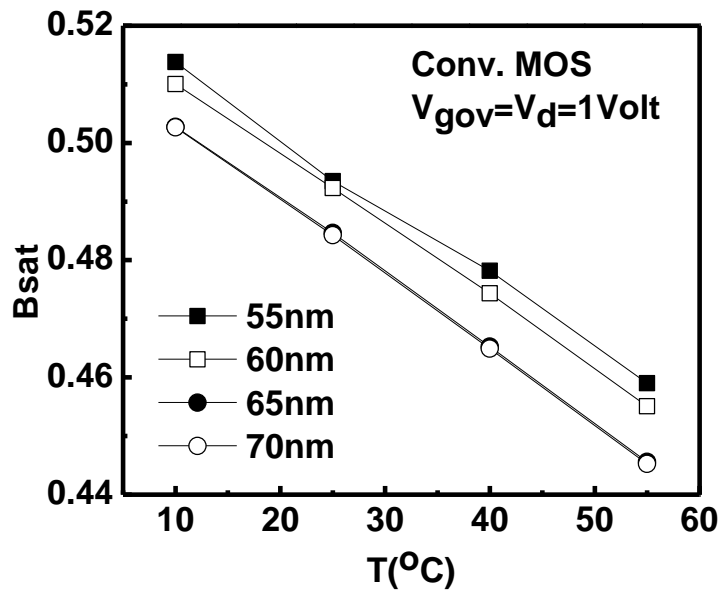
(a)
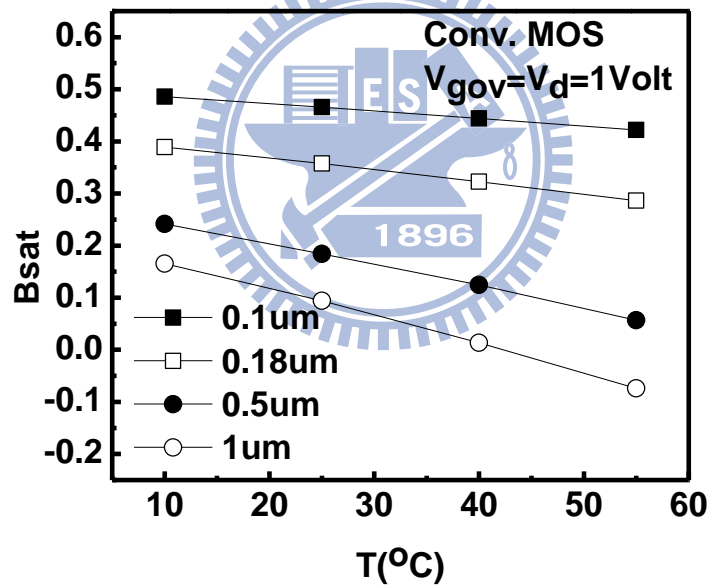
(b)

Fig.3.6 B_{sat} versus temperature in conventional MOSFET in the range of

(a) 55nm to 70nm and (b) 0.1um to 1um.
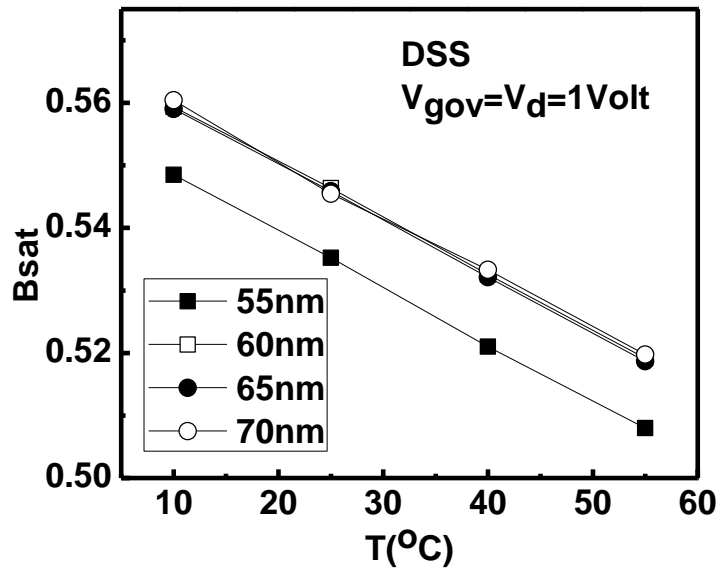
(a)
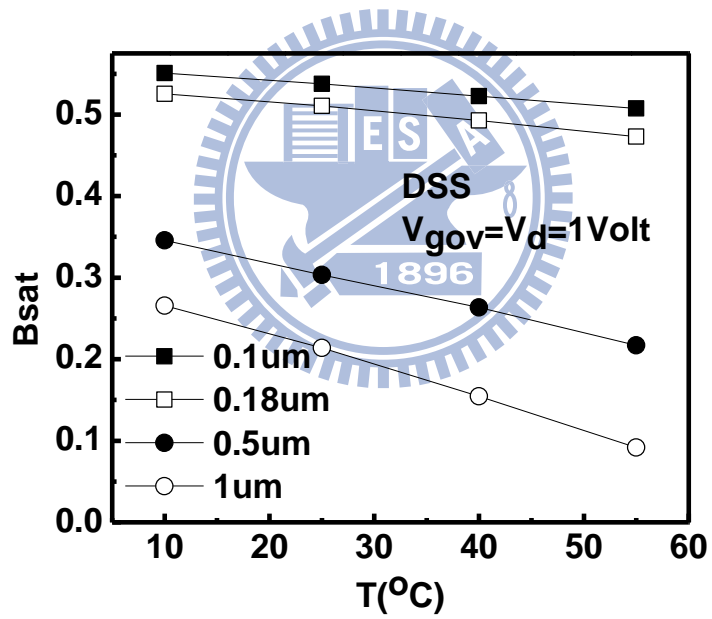
(b)

Fig.3.7 B_{sat} versus temperature in DSS in the range of (a) 55nm to 70nm
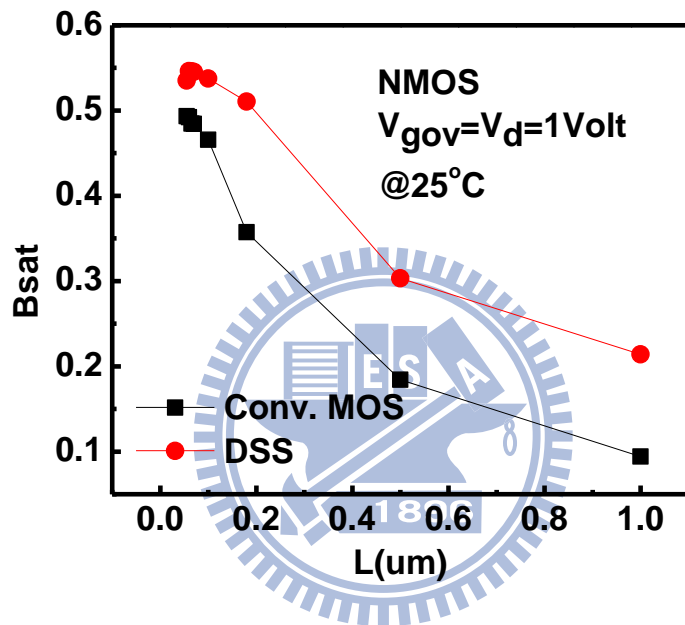
and (b) 0.1um to 1um.

Fig.3.8 The result of B_{sat} versus channel length in DSS and conventional

MOSDET, which is calculated by TDM.
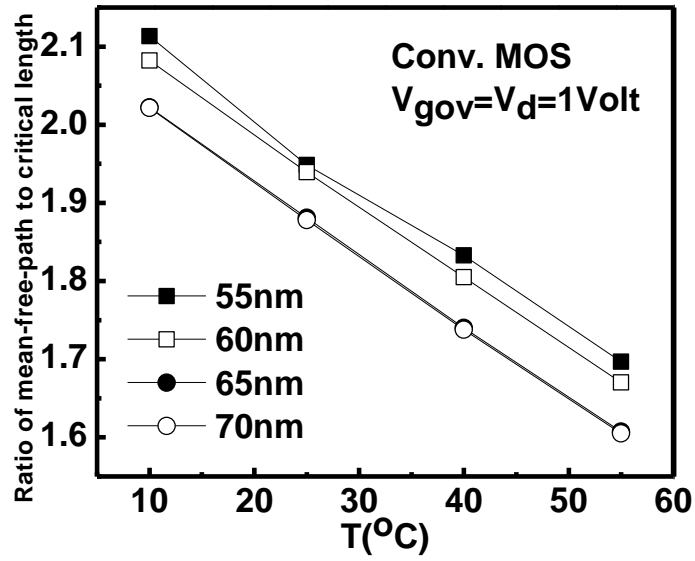
(a)
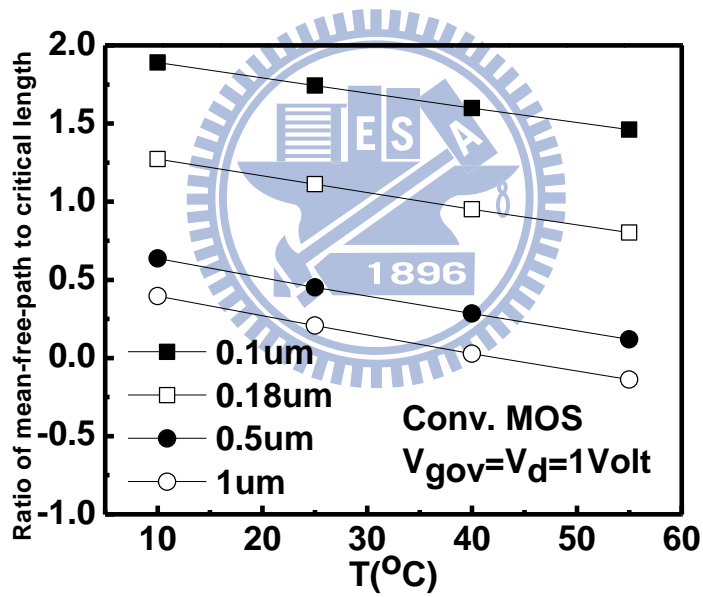
(b)

Fig.3.9 The ratio of mean-free-path and critical length in conventional MOSFET in the range of (a) 55nm to 70nm and (b) 0.1um to 1um.
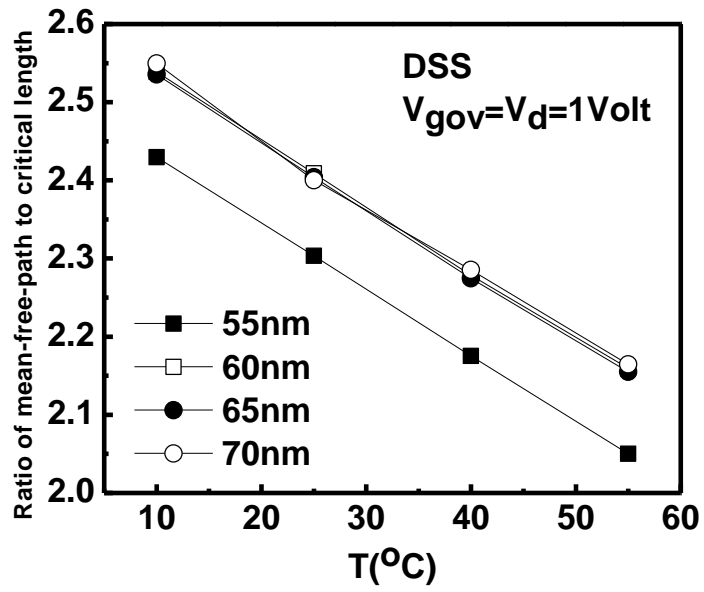
(a)
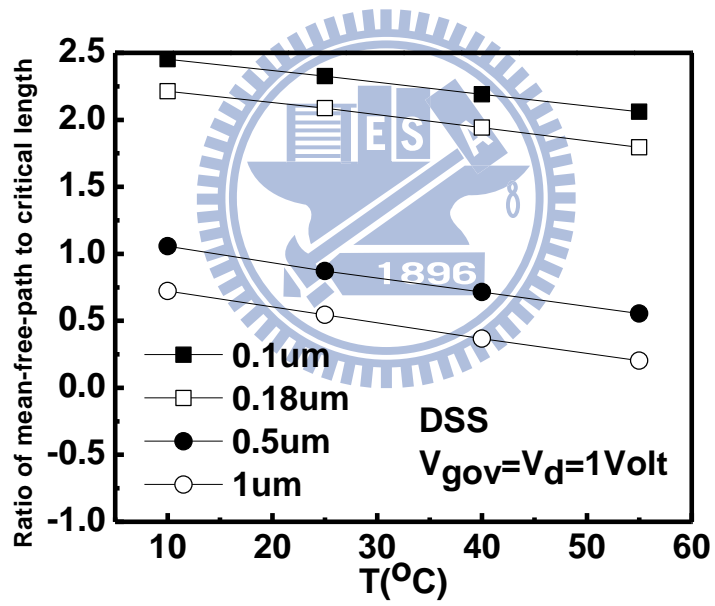
(b)

Fig.3.10 The ratio of mean-free-path and critical length in DSS in the range of (a) 55nm to 70nm and (b) 0.1um to 1um.
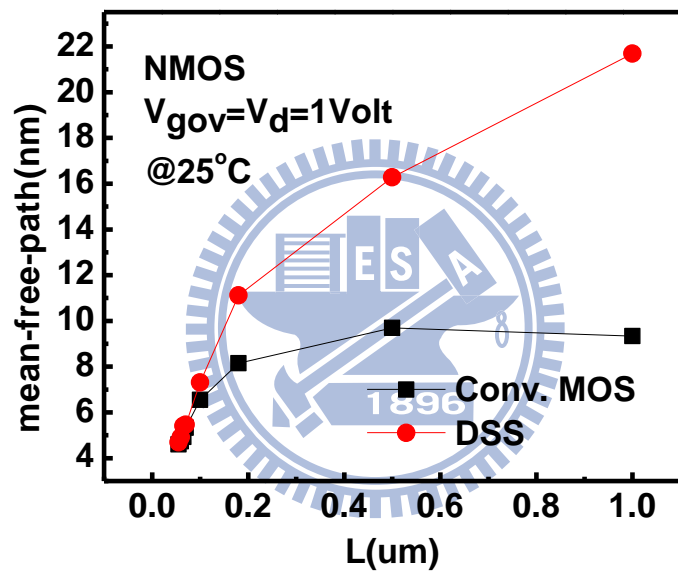
Fig.3.11 The result of the mean-free-path versus channel length in DSS and conventional MOSFET, calculated by TDM.
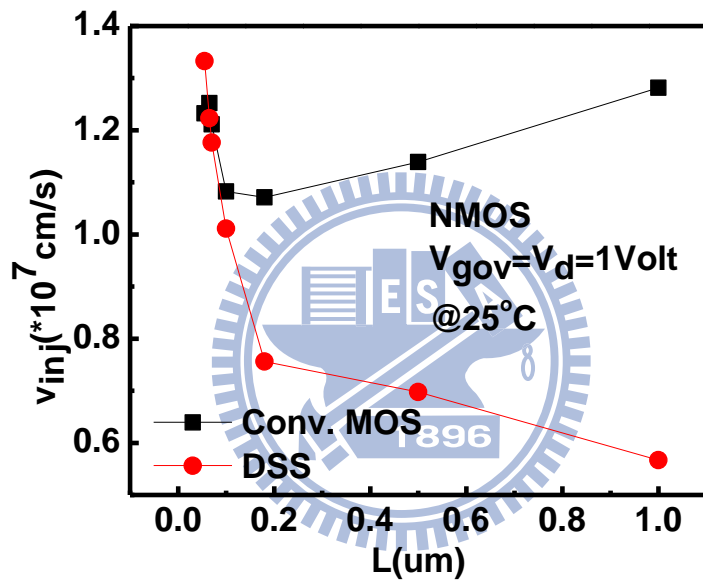
Fig.3.12 The result of v_{inj} versus channel length in DSS and conventional

MOSFET, calculated by TDM.

Chapter 4

Ballistic Efficiency in the Velocity Saturation Regime

As channel length decreases, the phenomenon of velocity saturation gradually impacts the performance of MOSFET. When carrier velocity in channel reaches the limit of velocity saturation, a continuous V_d bias does not longer raise I_d up. On the other hand, the ballistic theory refers to the ballistic efficiency (B_{sat}) under quasi-ballistic regime. The higher B_{sat} makes performance better as channel length decreases. The behavior of B_{sat} in short channel region is in contrast to that of velocity saturation phenomenon. Thus, it needs a unity, which can effectively describe those at the same time. We start our concepts with the equation of velocity saturation.

4.1 The Equations under Velocity Saturation

4.1.1 The Empirical Equation

In 1967, Caughey and Thomas presented an empirical equation called velocity model, which describes the carrier velocity with respect to the electric field [4.1]. The parameters of the equation consists of low field mobility μ, saturated velocity v_{sat} and electric field E_ℓ in the lateral direction. The equation is given by:

$$v = \frac{\mu \cdot E_\ell}{\left[1 + \left(\dfrac{E_\ell}{E_c}\right)^\beta\right]^{\frac{1}{\beta}}} \tag{4.1}$$

where $\beta = 1$ for hole or $\beta = 2$ for electron and E_c represents the critical field which is defined as below.

$$E_c = \frac{v_{sat}}{\mu} \tag{4.2}$$

Figure 4.1 shows the result from the velocity model. In the model, the v_{sat} is set the fixed value of 9.5×10^6 cm/s for hole and that of 1.1×10^7 cm/s for electron. When the E_ℓ increases, and is comparable to even greater than E_c, v_{sat} will dominate the equation. We can survey this behavior from the operation in the linear region. In the linear region, the v is related to E_ℓ with the constant value μ, which is defined as the low field mobility. Thus, the Eq. 4.1 reduces to $v = \mu \cdot E_\ell$. As the E_ℓ increases over the E_c, the denominator of Eq. 4.1 demonstrates the significance. When the E_ℓ tends to infinity, the Eq. 4.1 will be rewritten as below.

$$v \approx \mu \cdot E_c = v_{sat} \qquad\qquad (4.3)$$

The Eq. 4.3 shows clearly that the v_{sat} dominates the carrier velocity. As a result, the velocity model succeeds in representing the velocity saturation phenomenon by using the analytical equation.

But we confuse the definition of the critical field, which is given in Eq. 4.2. The μ is usually used in the linear region. When the device is operated in the saturation region, the mobility will degrade strongly, and be less than μ. However, in Eq. 4.2, the μ used under velocity is equal to v_{sat}, this estimation of the E_c seems to be inaccurate. Thus, we propose the modified velocity model, which improves this problem and is used to the calculation of the B_{sat} in the next section.

4.1.2 The Modified Velocity Model

The definition of E_c, which is given in Eq. 4.2, makes us confused. When the device is operated in the saturation, the μ, which is applied in the linear region suitably, is used. Thus we need to define the E_c as another form. In general, the E_ℓ is given by:

$$E_\ell = \frac{V_d}{L} \tag{4.4}$$

We can see that the E_ℓ is proportional to V_d. However, the V_{dsat}, which is introduced in Ch. 2, has the same behavior contrasting to the E_c. When V_d reaches V_{dsat}, the I_d current gradually tends to saturation, and I_d current doesn't increase rapidly, neither does the v in Eq. 4.1. Consequently, we can utilize the V_{dsat} to define the E_c. The form of E_c is rewritten as the following.

$$E_c = \frac{V_{dsat}}{L} \tag{4.5}$$

On the other hand, this form needs to be consistent with the velocity saturation. Thus, we can rearrange Eq. 4.5 by another form, which is given by:

$$E_c = \frac{v_{sat}}{\gamma} \tag{4.6}$$

where $\gamma = v_{sat} \cdot L / V_{dsat}$ calculated by Eq. 4.5 and Eq. 4.6.

From the comparison of Eq. 4.6 and Eq. 4.2, the E_c is no longer defined by μ, and is dependent on the new factor γ, which is related to V_{dsat}. Except modifying the E_c, we have another important target, in which the velocity model can be used in calculating B_{sat}. Thus, we need to add a fraction n into the velocity model to fit the experimental value. We will discuss the reason by adding the factor into the velocity model in the next section. The modified velocity model is given by:

$$v = \frac{\mu \cdot E_\ell}{1 + \frac{E_\ell}{n \cdot E_c}} \tag{4.7}$$

where n is termed the fitting factor, which is determined by fitting the experimental value. When V_g increases, the I_d will increase, and it needs the higher value of n to fit the experimental value of I_d. Thus the n is a function of V_g.

In Fig. 4.2, the same motivation on v with varied V_g is observed, and we should believe that the modified velocity model can describe the curve of carrier velocity

with varied E_ℓ. Fig. 4.3 shows the curve of carrier velocity calculated by measurement comparing to the original velocity model and the modified velocity model. The black line with closed black square represents the result of measurement. In this line, we mark the E_c with different velocity model. The opened black square represents the E_c defined by the original velocity model, and the closed red circle represents the E_c defined by the modified velocity model. In short channel region, the E_c of the modified velocity model is less than that of the velocity model. As channel length increases, both E_c is increasing. We see that the E_c of the original velocity model is out of our measurement range. This means that the carrier velocity is yet dominated by velocity saturation phenomenon. Keep an eye on the curve of measured velocity, the curve demonstrates the behavior of saturation mechanism at the curve tail. This behavior means that the E_c should be in the measured range. And we can obtain the reasonable E_c in the range from the modified velocity model. Besides, the curve of the modified velocity model, which has the same terminal value with that of measurement through the fitting factor n is applied, also shown in Fig. 4.3. For the model of calculating B_{sat} we developed, the fitting procedure is the most critical point due to eliminate the errors during the derivation of the current equation.

Besides, the relation of V_{dsat} and channel length is shown in Fig. 4.4, we can observe that V_{dsat} is lower with decreasing channel length because higher lateral field induces early occurrence of velocity saturation mechanism. Moreover, the curve of DSS exhibits slower decrease of V_{dsat} to expand the performance difference against conventional MOSFET.

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4.2 Ballistic Efficiency with the Velocity Saturation Properties

4.2.1 Derivation of Id Equation with Velocity Saturation

In the previous section, we have developed the modified velocity model to calculate B_{sat}. Then, we start to derive the I_d equation based on the modified velocity model. The orientation of coordination is defined in Fig. 4.4 (a). The modified velocity model consists of Eq. 4.6 and Eq. 4.7 can be represented by:

$$v = \frac{\mu \cdot E_\ell}{1 + \dfrac{\gamma \cdot E_\ell}{n \cdot v_{sat}}} \tag{4.8}$$

Substitute Eq. 4.8 into the conventional I_d equation, we will obtain the differential equation of I_d with voltage consumption due to series source/drain resistance, which is given by:

$$I_d = W \cdot C_{ox} \cdot (V_g - V_{th} - m \cdot V) \cdot \frac{\mu \cdot \partial V / \partial y}{1 + \dfrac{\gamma \cdot \partial V / \partial y}{n \cdot v_{sat}}} \tag{4.9}$$

where $m \cdot V$ means the voltage consumption due to series source/drain resistance.

After rearranging the Eq. 4.9, we integrate the equation with respect to y and V.

$$I_d = \left[W \cdot C_{ox} \cdot (V_g - V_{th} - m \cdot V) \cdot \mu - I_d \cdot \frac{\gamma \cdot \mu}{n \cdot v_{sat}} \right] \cdot \frac{\partial V}{\partial y} \tag{4.10}$$

$$\rightarrow \int_0^L I_d \cdot \partial y = \int_0^{V_d} \left[W \cdot C_{ox} \cdot (V_g - V_{th} - m \cdot V) \cdot \mu - I_d \cdot \frac{\gamma \cdot \mu}{n \cdot v_{sat}} \right] \partial V \tag{4.11}$$

where the integral range of y is from 0 to L and that of V is from 0 to V_d.

Further, we obtain the equation of I_d as below.

$$I_d = \frac{W \cdot C_{ox} \cdot (V_g - V_{th} - 0.5m \cdot V_d) \cdot \mu \cdot V_d}{L + \frac{\gamma \cdot \mu}{n \cdot v_{sat}} \cdot V_d} \tag{4.12}$$

The following is to derive the I_d equation for calculating B_{sat}. The symbol $V_{d,q\text{-}sat}$ means the drain bias applied under quasi-ballistic regime. We will find $V_{d,q\text{-}sat}$ by differentiating Eq. 4.12 with respect to V_d.

$$\left. \frac{\partial I_d}{\partial V_d} \right|_{V_{d,q-sat}} = 0$$

$$\rightarrow V_{d,q-sat} = \frac{2}{m} \cdot (V_g - V_{th}) \cdot \left[1 + \sqrt{1 + \frac{2 \cdot \gamma \cdot \mu \cdot (V_g - V_{th})}{m \cdot n \cdot v_{sat} \cdot L}} \right]^{-1} \tag{4.13}$$

After replacing $V_{d,q\text{-}sat}$ into Eq. 4.12, the I_d equation with velocity saturation phenomenon under quasi-ballistic regime is obtained.

$$I_{d,q-sat} = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot n \cdot v_{sat} \cdot \frac{\sqrt{1 + \frac{2 \cdot \gamma \cdot \mu \cdot (V_g - V_{th})}{m \cdot n \cdot v_{sat} \cdot L}} - 1}{\sqrt{1 + \frac{2 \cdot \gamma \cdot \mu \cdot (V_g - V_{th})}{m \cdot n \cdot v_{sat} \cdot L}} + 1} \tag{4.14}$$

Then, Eq. 4.14 can be simplified as shown below.

$$I_{d,q-sat} = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot n \cdot v_{sat} \cdot B_{sat} \tag{4.15}$$

where $n \cdot v_{sat}$ represents the injection velocity v_{inj} is a function of V_g.

Moreover, we hope that we can calculate accurate experimental value by removing the voltage consumption due to series source/drain resistance. Below, we rewrite the forms of E_ℓ, E_c and the carrier velocity v which is calculated at the source/channel interface.

$$E_\ell = \frac{V_d - V_{Rsd}}{L} \tag{4.16}$$

$$E_c = \frac{V_{dsat} - V_{Rsd}}{L} \tag{4.17}$$

$$v = \frac{I_d}{W \cdot C_{ox} \cdot (V_g - V_{th} - 0.5 \cdot V_{Rsd})} \tag{4.18}$$

where V_{Rsd} is the voltage consumption due to series source/drain resistance. The V_{Rsd} can be calculated by the following equation.

$$V_{Rsd} = I_d \cdot R_{sd} \tag{4.19}$$

Finally, we rearrange the fully equations to calculate B_{sat} in Fig. 4.4 (b). Those equations are called Velocity Saturation Model (VSM).
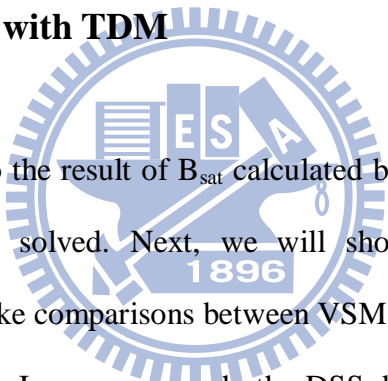
4.2.2 The Procedure of Calculating Bsat Through VSM

Consequently, we use the VSM to calculate the B_{sat}. The procedure of operation is shown in Fig. 4.5. For the beginning of calculation, we need the measured data including I_dV_g, I_dV_d and CV characteristics of the device. The I_dV_g characteristic is used for determining the V_{th} in the saturation region, and the CV characteristic is applied to calculate the C_{ox} value. We find a curve of device performance from I_dV_d characteristic. The V_g equal to $V_{dd}+V_{th}$ is applied to it for the reference between different devices. And, the terminal I_d current on the I_d curve is considered the $I_{d,q\text{-}sat}$ in the Eq. 4.15.

The μ is determined by g_d method at low field on the I_dV_d characteristic, and the v can be calculated by the Eq. 4.18. After the μ and the v are known, the modified velocity model can be applied to fit the terminal I_d value on I_d curve. Note that the Eq. 4.15 is formed by substituting $V_{d,q\text{-}sat}$, which is the V_d value at the maximum I_d value into I_d equation, thus the n is reasonably used to fit the terminal value, which is the maximum I_d value on the curve. Finally, the n is found at $V_g = V_{dd}+V_{th}$.

Because n is known, we will obtain the B_{sat} value from the Eq. 4.15. Fig. 4.6 shows the relation of v_{inj} and B_{sat} with respect to V_{gov}, which means V_g-V_{th}. The v_{inj} increases with increasing V_{gov}. This behavior is the same as that calculated by the TDM. The carrier degeneracy leads to raise the v_{inj} up. When the v_{inj} reaches the v_{sat}, the B_{sat} will decrease. The decrease is considered that the carrier suffers from the strong thermal scattering mechanism, and it suppresses the transport efficiency. As a result, the velocity saturation phenomenon demonstrates the significance in the VSM.

4.3 Experimental Results

4.3.1 The Comparison with TDM

In Chap. 3, we refer to the result of B_{sat} calculated by TDM, and there are some confusing problems to be solved. Next, we will show the experimental result determined by VSM, and take comparisons between VSM and TDM. At first, we need to have a notion about DSS. In some research, the DSS demonstrates the behavior of source side hot carrier. The behavior is induced because the carrier in source of DSS has larger energy than that of conventional MOSFET. When the carriers are injected into the channel, the carrier with high energy generates the early impact ionization. Some experiments have confirmed this specific behavior of DSS [4.4] [4.5].

Figure 4.7 shows the B_{sat} result calculated by VSM. We can see that the difference between DSS and conventional MOSFET increases with decreasing channel length. This figure demonstrates the reverse trend comparing to Fig. 3.8. But Fig. 4.7 seems to be a more reasonable result than Fig. 3.8 calculated by TDM. We then come back to inspect the performance enhancement of DSS against conventional MOSFET. In Fig. 2.16, The I_d gain of DSS contrasting to conventional MOSFET

increases as channel length decreases. When the carrier with high energy in DSS enters channel, the carrier suffers from the resistance of lateral scattering which will be less than the carrier in conventional MOSFET. The carrier with high energy can suppress the more scattering phenomenon, and help the transport efficiency rise up. As channel length decreases, the suppression should demonstrate the significance. Thus, the B_{ast} difference of Fig. 4.7 can respond to the performance enhancement of Fig. 2.16. The larger B_{sat} difference causes the larger performance enhancement.

Then, we examine the result of v_{inj} in DSS and conventional MOSFET. The v_{inj} can be found when the B_{sat} and the capacitance C_{ox} were known. Fig. 4.8 shows the v_{inj} results calculated by VSM and TDM. Between these two methods for calculation, it shows the significant difference in the same device. Regarding to the curve of conventional MOSFET, they show an approximate trend by applying different methods. They show a significant different trend with respect to DSS. In Ch. 3, we illustrate the unreasonable point in the v_{inj} result of DSS by applying TDM, the v_{inj} is a function of channel length. However, the v_{inj} of DSS calculated by VSM has an approximate trend with the v_{inj} of conventional MOSFET. This is reasonably explained that both two devices are operated under the same Si bulk well. Before the carrier enters the channel, the v_{inj} is the only function of V_{gov}. When these two devices are biased in the some gate overdrive, they should have the near values consequently. These devices demonstrates that the v_{inj} is the approximate value of 1.5×10^7 cm/s under $V_{gov} = V_d = V_{dd} = 1$ Volt.

Moreover, we have calculated the mean-free-path λ and the critical length ℓ by VSM. When the B_{sat} and the v_{inj} have been calculated by VSM, we can find these two parameters by replacing B_{sat} and v_{inj} into Eq. 3.11 and Eq. 3.15. The estimations of λ and ℓ are shown in Fig. 4.9 (a) and Fig. 4.9 (b), respectively. In Fig. 4.9 (a), the λ degrades as channel length decreases due to the more serious scattering

phenomenon.

The λ of DSS shows the higher value than that of conventional MOSFET, and the slower rate of λ degradation in DSS is observed. This behavior relates to the better suppression on scattering phenomenon in DSS, which induces the larger λ. Besides, the lower ℓ of DSS is also observed. We can draw a schematic plot of band diagram to describe the condition in the lateral direction, as shown in Fig. 4.10. At the interface of DS layer, the carrier goes into high energy state from the abrupt potential drop. The carrier with high energy in DSS overcomes the main resistance due to scattering phenomenon more easily, and then will have longer distance in transporting, which means the longer λ. As a result, the DSS demonstrates the higher transport efficiency in quasi-ballistic regime, which means the higher B_{sat}.

And, we can create an equation of linking up B_{sat} and V_d at the fixed V_{gov}. According to the concept of ballistic theory, we must obey the rule, in which the v_{inj} is a function of V_{gov}, and not a function of V_d. Thus, the fixed n should be applied at the fixed V_{gov} with varied V_d. The schematic plot describes the rule, shown in Fig. 4.11 (a). And Fig. 4.11 (b) shows the $1/B_{sat}$ results with respect to $1/V_d$. To connect the $1/B_{sat}$ point with different $1/V_d$ can obtain a straight line, which intersect the y-axis. The equation of the B_{sat} can be formed by:

$$B_{sat} = \left[\frac{1}{B_f} + \theta \cdot \frac{1}{V_d} \right]^{-1} \tag{4.20}$$

where θ is the slope of the straight line and B_f is the extreme value of B_{sat}.

The B_f of 0.54572 in DSS and that of 0.46882 in conventional at L= 55nm are calculated.

4.3.2 Applications to the Strained-Si Device

Finally, we use VSM to calculate the B_{sat} and the v_{inj} of strained-Si device. The CESL type strained-Si device is used. The basic phenomenon of strain effect means that structure variation induced channel strain leads to lower effective mass in carrier transport, and raises the device performance up. Fig. 4.12 (a) and Fig. 4.12 (b) show the results of v_{inj} and B_{sat}, respectively. We can see that the v_{inj} of strained-Si device has higher value than other two devices, and the B_{sat} of strained-Si device demonstrates the approximate value contrasting to conventional MOSFET. Between the CESL type strain-Si device and conventional MOSFET, there is no structure variation at source/channel interface. Thus, the carrier in them doesn't raise PE up prior to entering channel, they demonstrates less B_{sat} than DSS. However, the strain effect provides lower effective mass for carrier transport, which induces higher v_{inj} than DSS and conventional MOSFET. As a result, the high v_{inj} of CESL type strained-Si device dominates the performance enhancement against conventional MOSFET.
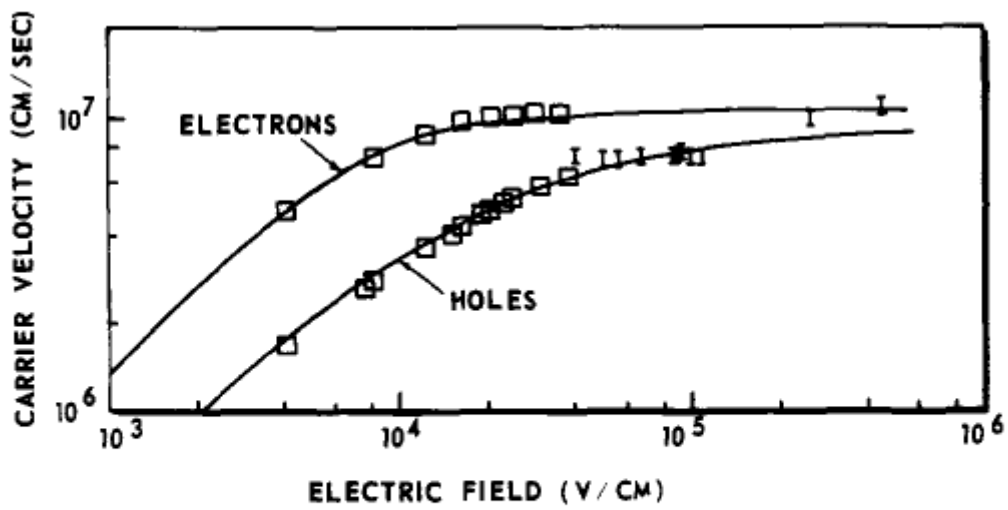
	v_m cm/s	ε_c V/cm	β
Holes	9.5×10^6	1.95×10^4	1
Electrons	1.1×10^7	8×10^3	2

Fig. 4.1   The curve of carrier velocity with respect to electric field and

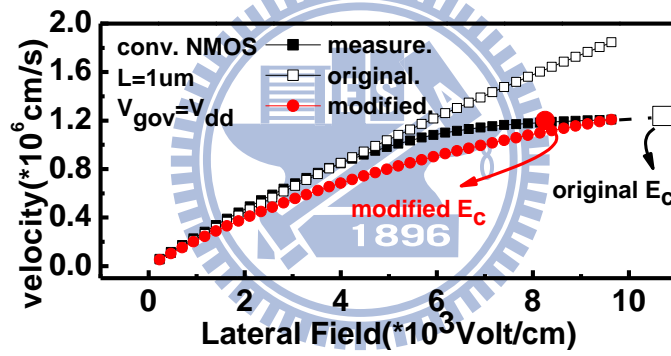the empirical equation is applied on the plot.

	E_c	V_g	μ	V_{dsat}	n	RESULT
Original equation $v=\dfrac{\mu\cdot E_\ell}{1+\dfrac{E_\ell}{E_c}}$	$\dfrac{v_{sat}}{\mu}$		$\searrow$			
Modified equation $v=\dfrac{\mu\cdot E_\ell}{1+\dfrac{E_\ell}{n\cdot E_c}}$	$\dfrac{V_{dsat}}{L}$		$\nearrow$	$\nearrow$	$\nearrow$	$E_C\nearrow$ $\to v\nearrow$

Fig. 4.2 The comparisons between the original and the modified

velocity saturation equation for a varying V_g.
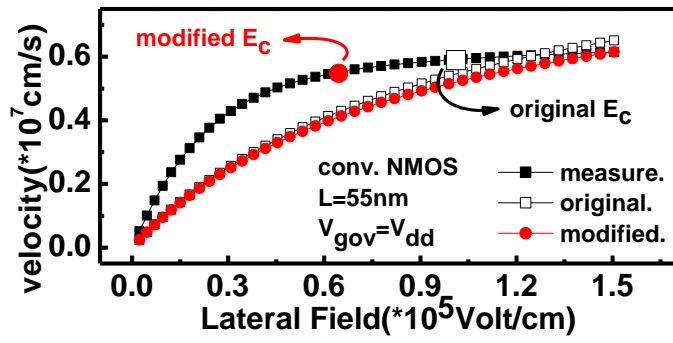
(a)

(b)

Fig. 4.3   The curve of carrier velocity in calculated by measurement comparing to the original velocity model and the modified velocity model in (a) short channel region and (b) long channel region.
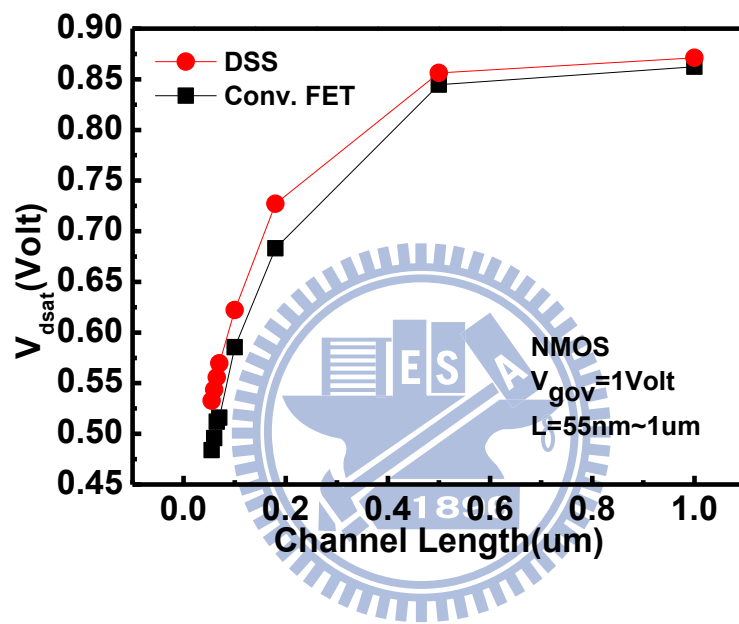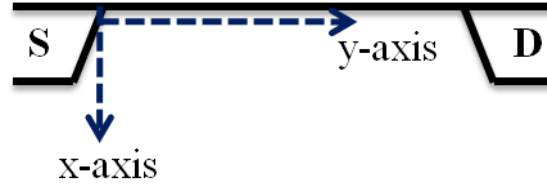
Fig. 4.4   The plot of V_{dsat} versus channel length with respect to DSS

and conventional MOSFET.

(a)

$$I_d = W \cdot C_{ox} \cdot (V_g - V_{th} - 0.5 \cdot V_{R_{SD}}) \cdot v \qquad (1)$$

$$v = \frac{\mu \cdot E_\ell}{1 + \dfrac{E_\ell}{n \cdot E_C}} \quad ; E_\ell = \frac{V_d - V_{R_{SD}}}{L} \quad ; E_c = \frac{V_{dsat} - V_{R_{SD}}}{L} \quad (2)$$

$$I_{d,q-sat} = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot n \cdot v_{sat} \cdot B_{sat} \qquad (3)$$

$$v_{sat} = 1.07 \cdot 10^7 \; \frac{cm}{s} \quad \text{for NMOS, Silicon channel}$$

$$8.7 \cdot 10^6 \; \frac{cm}{s} \quad \text{for PMOS, Silicon channel}$$

n : *fitting factor,* $V_{R_{SD}}$: *voltage consumption by S/D series resistance*

(b)

Fig. 4.5   (a) The orientation of coordinates in the MOSFET device. (b)

The rearrangement of equations applied in the VSM.
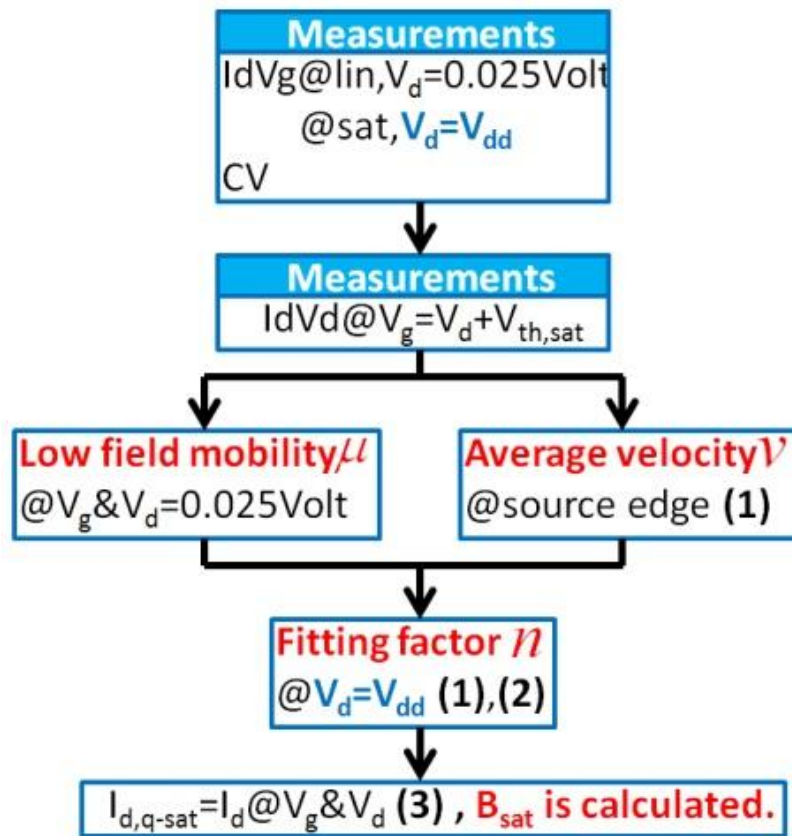
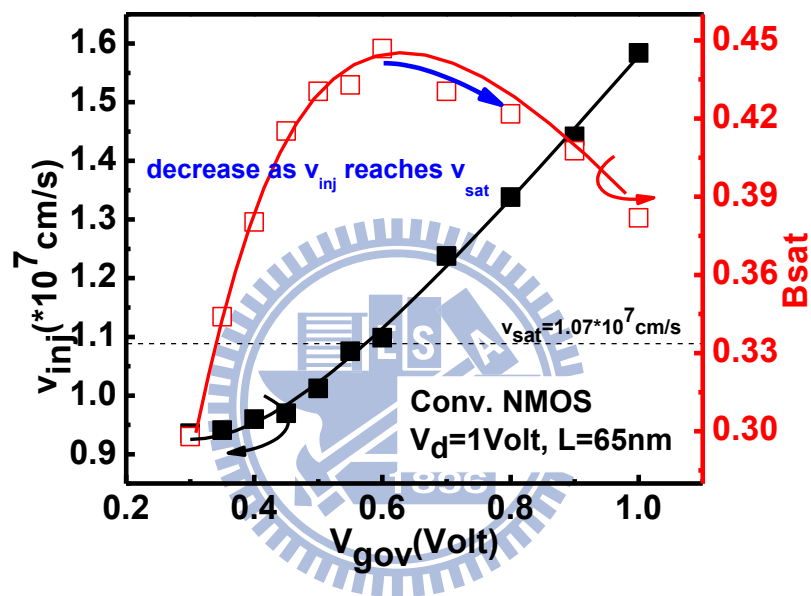Fig. 4.6   The procedure of using VSM to calculate B_{sat}.

Fig. 4.7   The relation of v_{inj} and B_{sat} with a varying V_{gov}.
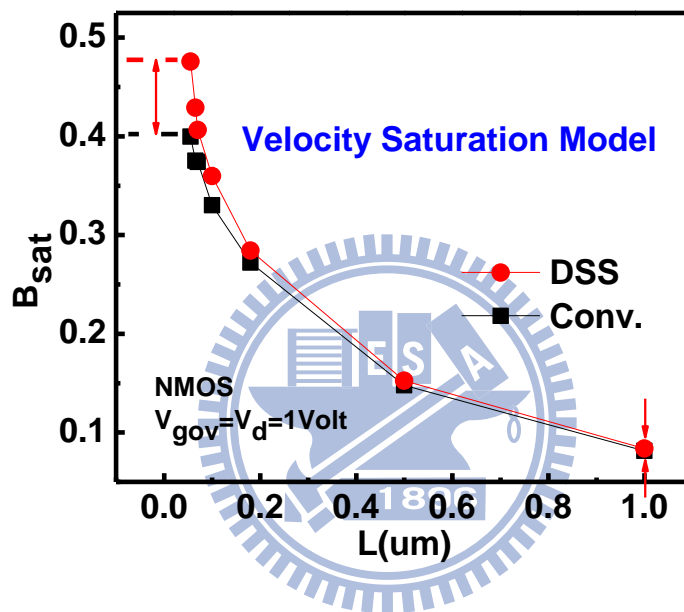
Fig. 4.8   The B_{sat} is calculated by the VSM with respect to channel

length.
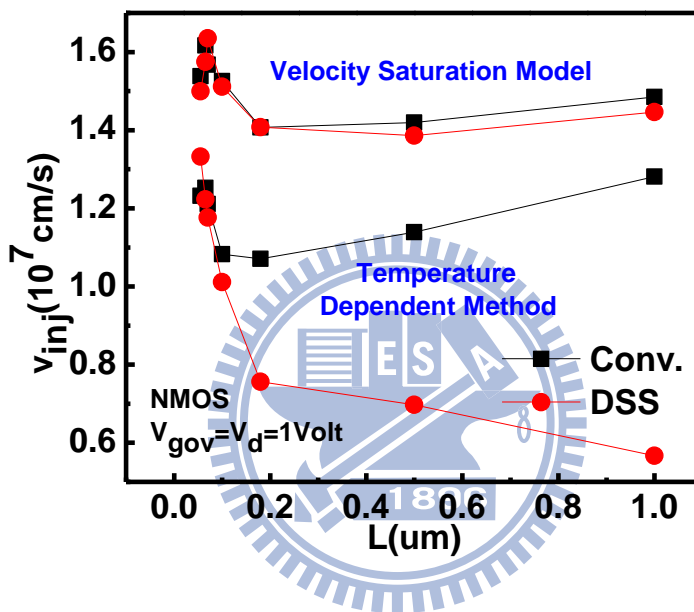
Fig. 4.9   The v_{inj} calculated by VSM in comparison to that by TDM.

(a)
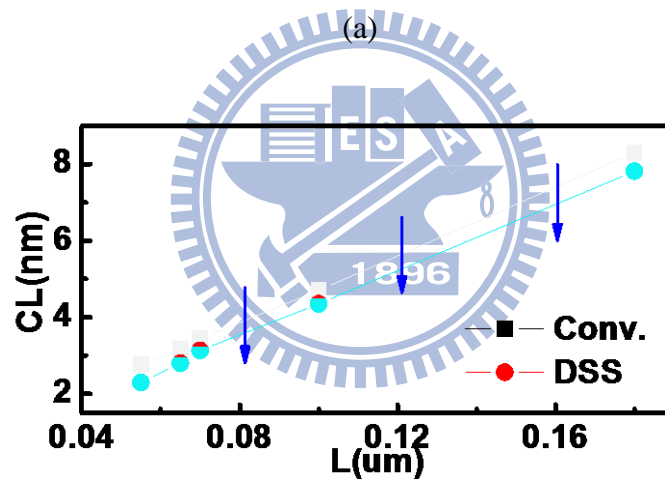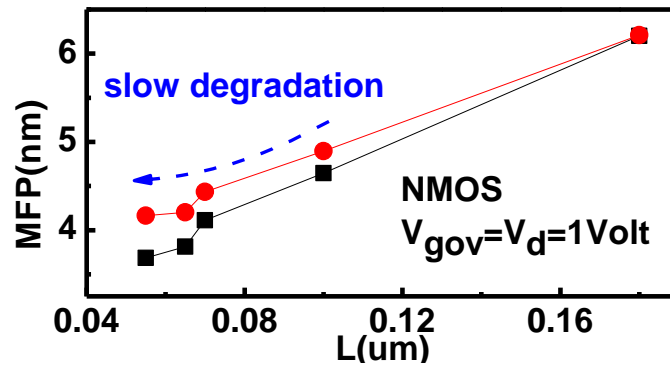
(b)

Fig. 4.10   (a) The mean-free-path and (b) the critical field are calculated

by VSM in comparison to TDM.
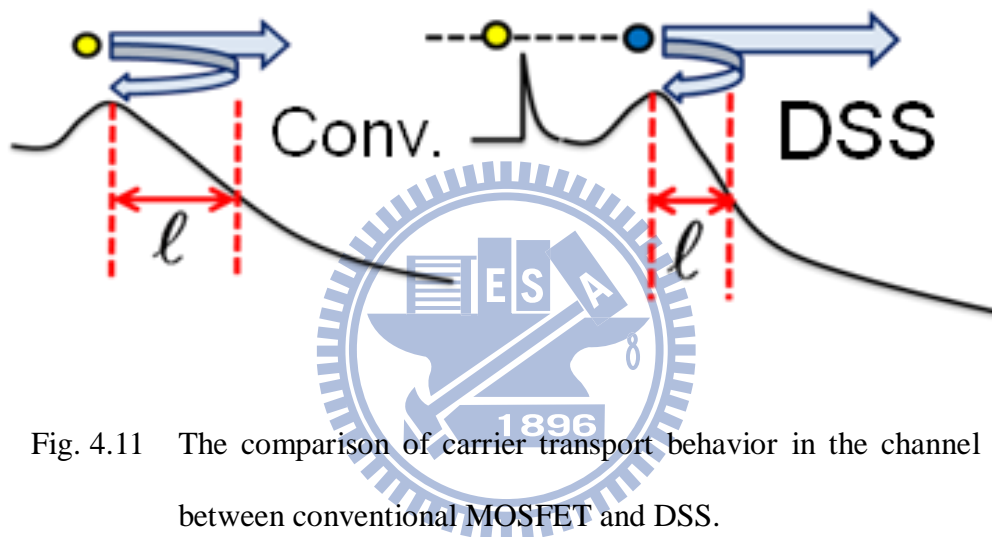
Fig. 4.11   The comparison of carrier transport behavior in the channel

between conventional MOSFET and DSS.

(a)
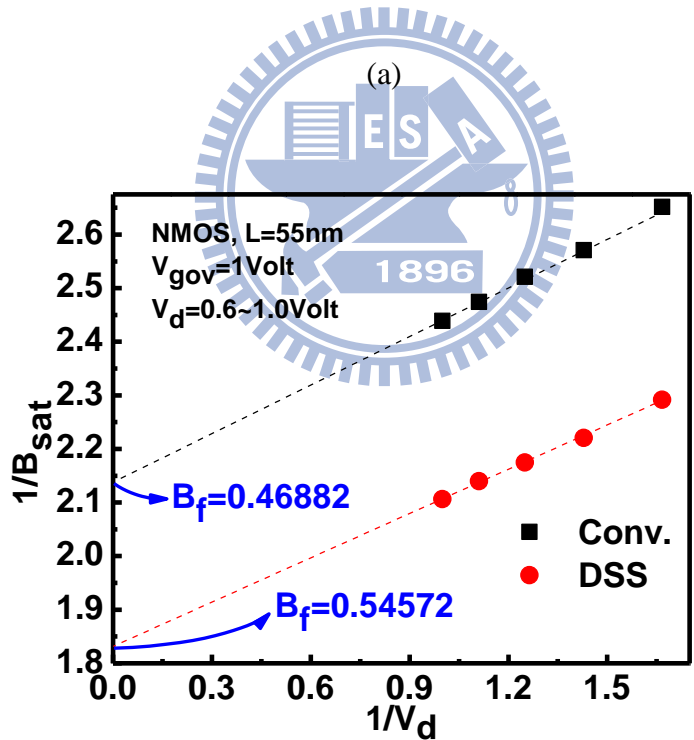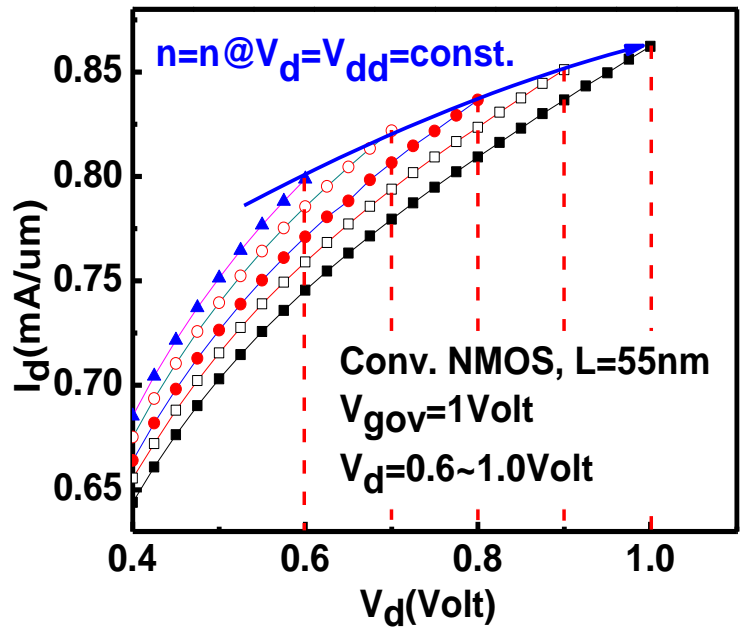
(b)

Fig. 4.12 (a) The rule needs to be obeyed at a fixed V_{gov}. (b) The extreme value of B_{sat}, which is defined by B_f, is calculated by VSM.

(a)

(b)

Fig. 4.13   The CESL type strained-si device is added for discussion about the v_{inj} and the B_{sat}.

Chapter 5

Conclusions

In recent years, much effort has been focused on the performance enhancement study of Schottky-Barrier MOSFET. However, none has been provided on the study of its transport characteristics. The study of this work is to mainly develop a method which can be used to determine the two major transport parameters, the ballistic efficiency, B_{sat}, and injection velocity (v_{inj}).
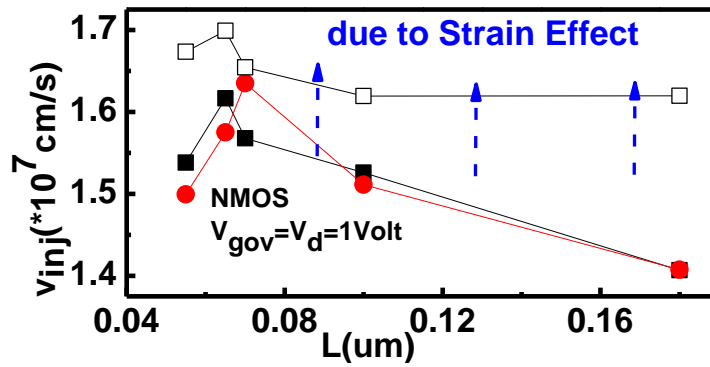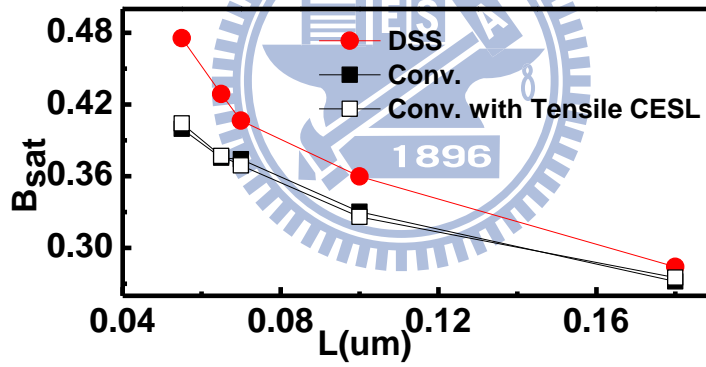
First, an advanced SB-MOSFET with Dopant-Segregated(DSS) source/drain has been made. It was found that the DSS exhibits a driving current gain over 15.2% and overall gain of 11% in the I_{on}/I_{off} characteristics in comparison to the conventional MOSFETs.

Then, based on the understanding of device physics, we develop a new experimental approach called Velocity Saturation Model (VSM) with velocity saturation phenomenon. The drain current equation of VSM is described by:

$$I_{d,q-sat} = W \cdot C_{ox} \cdot (V_g - V_{th}) \cdot n \cdot v_{sat} \cdot B_{sat}$$

where v_{inj} is redefined as $n \cdot v_{sat}$. B_{sat} decreases when v_{inj} exceeds saturated velocity (v_{sat}), which indicates the velocity saturation phenomenon. From VSM approach, we obtain reasonable values of B_{sat} and V_{inj}, compared to TDM ones. Moreover, the experimental results showed that the accuracy of B_{sat} is improved by reducing the channel length, resulting in a better enhancement of the performance, but not agreed with the results of TDM. .

In addition, the strained Si device (CESL type) has also been studied by using the same approach. By applying VSM, it was found that the enhancement of performance in strained-Si device with CESL is caused by v_{inj} but not B_{sat} as shown in Fig. 4.12.

Finally, the comparison between DSS and conventional MOSFET has been summarized in Fig. 5.1.

DEVICE		Conv.	DSS
Q_{inv}	V_{th}	-	HIGH
	R_{sd}	HIGH	LOW
Velocity		SLOW	FAST
Ballistic view	v_{inj}	-	-
	B_{sat}	LOW	HIGH
	λ	SHORT	LONG
	ℓ	LONG	SHORT
I_d		-	GOOD

Fig. 5.1　　The summary of critical parameters in DSS.

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