國立交通大學

電子工程學系 電子研究所

碩士論文

寬頻一進二出放大器設計

Wideband Splitter Amplifier Design

研 究 生：黃瀞瑩

指導教授：胡樹一 教授

中 華 民 國 一〇〇 年 七 月

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摘要

由於積體電路的元件設計和系統整合皆已經發展相當成熟，接收器陣列是未來主流之一。如果把一組接收器系統比擬為一雙眼睛，那麼接收器陣列就像是蒼蠅的複眼，不但可以接收到更微弱的訊號，還可以增加接收訊號的廣度;在一個超寬頻的接收器系統當中，由於接收的訊號太寬，必須先經由功率分配器輸出多路訊號之後再做切割與降頻，以提供較低頻且窄頻的訊號給後級的類比數位轉換器處理。然而，傳統的功率分配器大多使用由被動式元件組成的多階項功率分配器來達到寬頻的效果（例：威爾金森功率分配器）。此種功率分配器雖然不消耗功率，卻會佔用相當可觀的面積，無法順利做成接收器陣列。此外，被動式功率分配器在寬頻的應用之下在隔絕度上有很大的限制，如果使用在對於輸出訊號獨立性要求特別高的系統當中，通常需要外接其他元件才能夠達到足夠的隔絕度，實用性上不是很高。為了更進一步的改善傳統被動式功率分配器在面積消耗和寬頻之下隔絕度的限制，在此提出結合主動式元件的功率分配兼放大器。利用主動式元件本身具有良好的隔絕度，輸出獨立性極高的兩路訊號，更能夠以積體電路來取代原本需要極大面積的被動式功率分配器。

Wideband Splitter Amplifier Design

Student: Ching-Ying Huang Advisor: Dr. Shu-I Hu

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ABSTRACT

Since the developments of the IC components design and system integration have been quite mature, receiver array is one of mainstream in the future. If we compare a receiver system to eyes, the receiver array would be the compound eyes of the flies which can catch weaker signals and possess the more extensive range. However, it requires power dividers to split out multiple signals; Multi-section Wilkinson power divider is one of the most common power dividers which can reach wideband achievement. Although such passive power divider does not consume any DC power, it requires considerable area. Besides, Wilkinson power divider has a severe limit to isolation in the wideband application. Inevitably we have to add other device to achieve enough isolation while a system demanding of particularly independence between two output signals. This solution is not that efficient. In order to overcome the area consumption and isolation limit problems, we report the active splitter amplifiers integrating active devices. Active power dividers can provide two highly independent signals by employing active device which has good isolation in itself, and reduce area to an IC size.

Tables of Contents

Chapter1 Introduction

1.1 The Motivation and Research Development

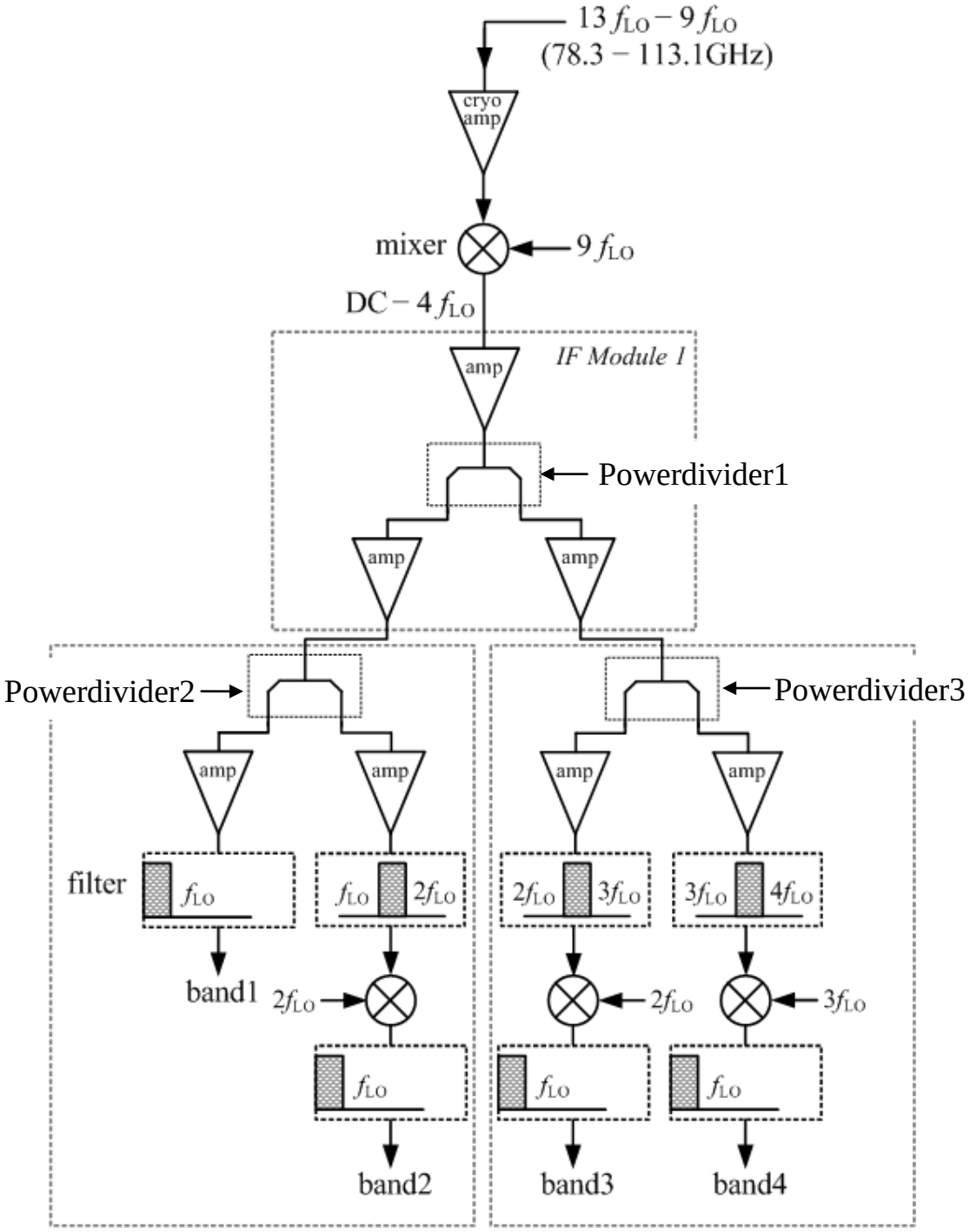

Fig. 1

Fig.1 shows a W-band receiver system configuration. The 78.3-113.1GHz band signal is received and this signal will be down conversion to DC-34.8GHz by a mixer. After being split to two paths by a passive power divider, which has the operating frequency band in DC-34.8GHz, the two signals are amplified relatively and then go through powerdivider2 and 3, which's operating frequency band are in DC-17.4GHz and 17.4-34.8GHz. After the two signals are divided to four ways, all of them will be amplified once again and encounter low-pass and band-pass filters with different operating frequency band: DC-8.7GHz, 8.7-17.4GHz, 17.4-26.1GHz, 26.1-34.8GHz. The four filters extract four sets of frequency band, and the three higher frequency sets will be down conversion to DC-8.7GHz eventually. Because the received signals has too wide band, the receiver system employs power dividers and filters to split and cut signals for four sets in different frequency band. The ultimate goal is to provide narrow band signal for backward analog-to-digital converter, which can only deal with DC-8.7GHz band presently.

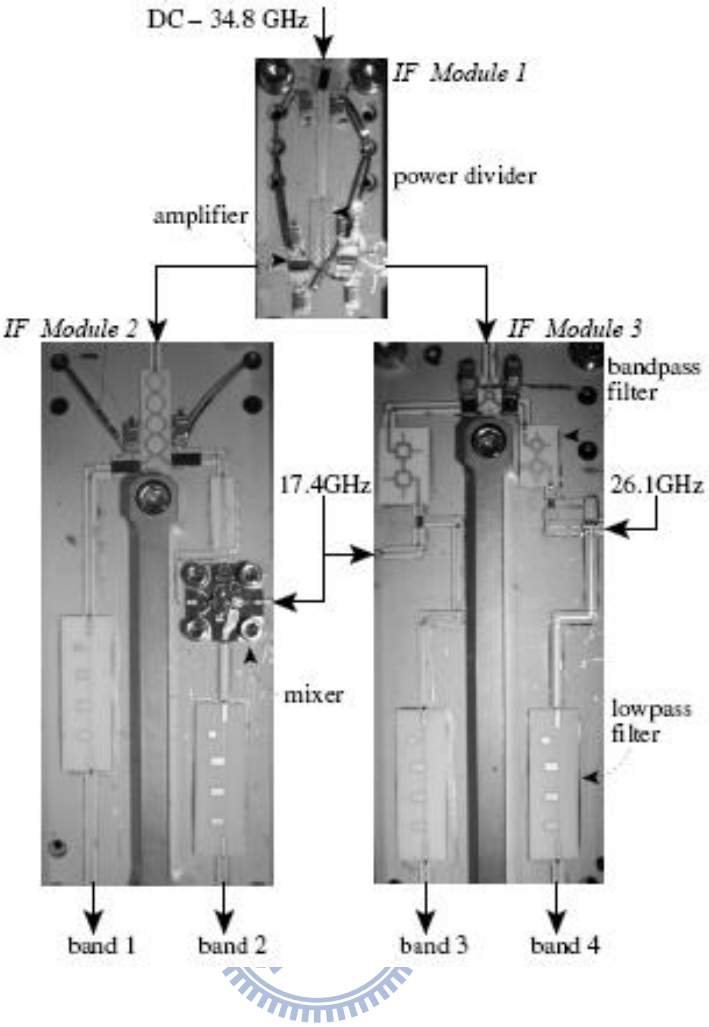

Fig. 2

Fig.2 is the entity picture of the receiver system. The photo shows that the three multi-sections Wilkinson power dividers engage quite considerable area. If now we take the replace of passive power dividers by active power dividers, which has only the size as same as ICs, the whole area will be reduced greatly so that we can integrate the system to an IC and further fabricate the receiver array. The receiver array can not only catch weaker signals but also extend the function range. For example, if more receivers are placed in the camera lens, the camera can obtain higher sensitization and wide-angle. As a matter of course, we will receive a natural vivid picture.

1.2 Passive Power Divider Analysis

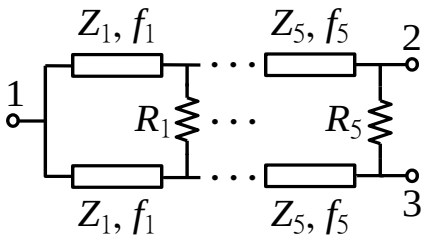

Fig. 3(a)

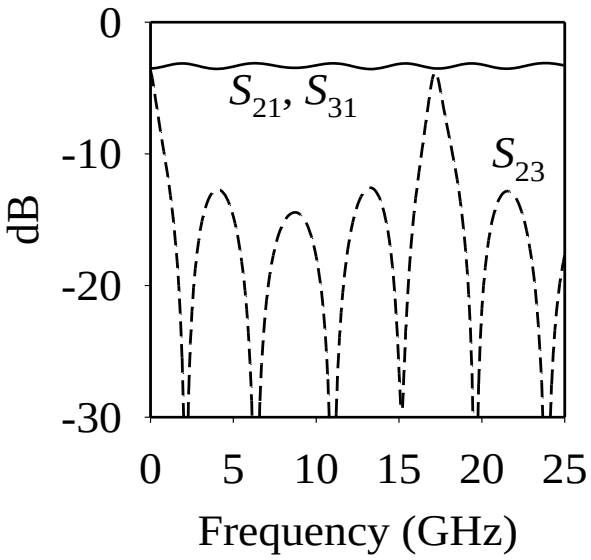

Fig. 3(b)

The Wilkinson power divider has been widely used for splitting the input power into two output signals of the same magnitude and phase and, with modifications, multiple octave bandwidth can be achieved [1], [2]. For applications that require even wider bandwidth, however, this type of passive circuit will be struggling to deliver the intended performance. As shown in Fig. 3(a), a five-section DC–17GHz Wilkinson power divider using ideal transmission lines. The impedance and frequency of the quarter-wave sections are $Z_{1\sim5}$ = 90, 55, 60, 60, 60Ω, and $f_{1\sim5}$ = 8.5, 8.6, 8.7, 8.8, 8.9GHz. The resistance $R_{1\sim5}$ = 120, 200, 330, 330, and 180Ω. As shown in Fig. 3(b), this Wilkinson power divider exhibits a good 3dB power division (S_{21}, S_{31} are about -3dB), and small input and output reflection coefficients. Though isolation (S_{23}) between the output ports is below -15dB in the middle of the frequency range, it deteriorates rapidly while approaching DC or 17GHz.

In this receiver system, the isolation of power dividers is one of the most important considerations. The main reason is that the following stage is four filters with different operating frequency band. The signal which is not in the band will reflect in quantity and leak to another output port while the isolation of the power divider is not good enough. Due to a phase difference between original signal and leaking signal, the output amplitude has a variation in shape of sine wave. This variation will bring about a problem of dynamic range to the next stage. The input power is very likely saturated so that influences the whole receiver's efficiency. In order to avoid such circumstance, the original method is to add a distributed amplifier, which has good isolation in itself, following each power divider. However, it's not a practical solution.

Active power dividers, on the other hand, show promise for meeting the wideband design specifications, and its compactness makes it even more appealing. For instance, a 1–10GHz active power divider using 0.13μm CMOS process for phase array application has been demonstrated [3]. In this paper, by re-examining the constraining factors, we like to further extend the bandwidth of the active power divider while at the same time keep improving the circuit's performance. Details regarding this DC–20GHz active power divider using the more common 0.18μm CMOS process will be presented in the following section.

Chapter2 Traditional Distributed Amplifier

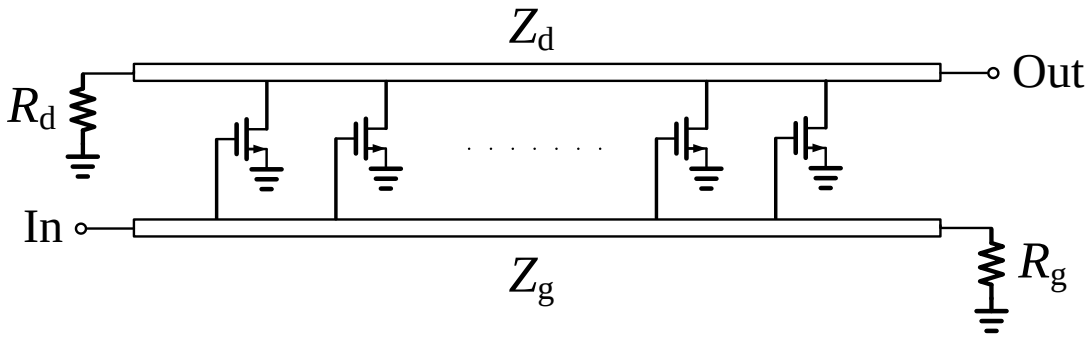

Fig. 4(a)

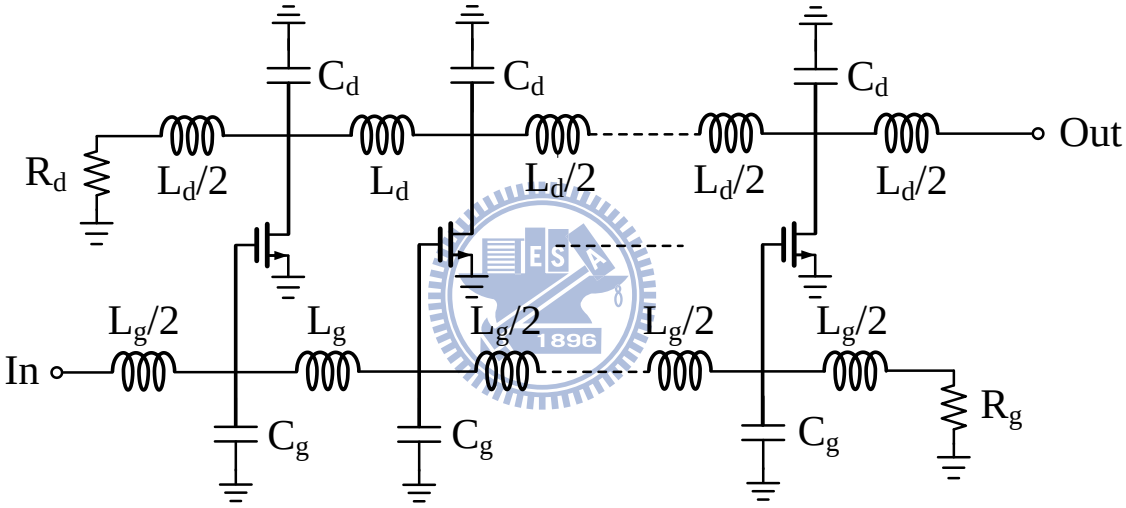

Fig. 4(b)

Distributed amplification, which was originally invented by Percival in 1936 and further developed by Ginzton et al. in 1948, has been widely used as a circuit topology for broadband amplifier design. Distributed amplifiers are constructed from two transmission lines that connect the drain and gate terminals of several field-effect transistors (FETs), as depicted in Fig. 4(a). The two lines are coupled by transconductances of the FETs. The equivalent gate and drain transmission lines are essentially loaded constant-k lines, where the parasitic resistances of FET's are considered the dominant loss factors.

In CMOS, transmission lines are normally constructed using micro-strip lines or ladder-lumped LC elements, as shown in Fig. 4(b). The distribution of the parasitic capacitors of transistors and series inductors is equivalent to a low-pass filter topology so that to achieve wideband amplification, providing the gain and good input and output matching over a large bandwidth. However, this structure provides a relatively low gain due to its paralleled gain cells and large artificial-line losses at high frequency. The characteristic impedance and cutoff frequency of the artificial transmission lines can be expressed as

$$Z_0 = \sqrt{\frac{L_{in}}{C_{in}}} = \sqrt{\frac{L_{out}}{C_{out}}} \quad (1)$$

$$f_T = \frac{1}{\pi\sqrt{L_{in}C_{in}}} = \frac{1}{\pi\sqrt{L_{out}C_{out}}} \quad (2)$$

By properly choosing the transistor sizes and the inductance values, the impedances of input and output transmission lines are able to match 50-Ω, offering low input and output return losses.

An RF signal applied at the input travels down the gate line to the terminated end, where it is absorbed. As the signal goes down the gate line, each transistor is excited by the traveling voltage wave and transfers the signal to the drain line through its transconductance. If the phase velocity on the gate line and drain line add in the forward direction as they arrive at the output. The waves traveling in the reverse direction are not in phase. And any uncancelled signal is absorbed by the drain-line termination. A simplified equivalent circuit of a MOSFET arrived at from typical S-parameter measurements at microwave

frequency is shown in Fig. 4(c). r_i is the effective input resistance between the gate and source terminals and C_{gs} is the gate-to-source capacitance. r_o and C_{ds} are the drain-to-source resistance and capacitance respectively. C_{dg} is the drain-to-gate capacitance and g_m the transconductance.

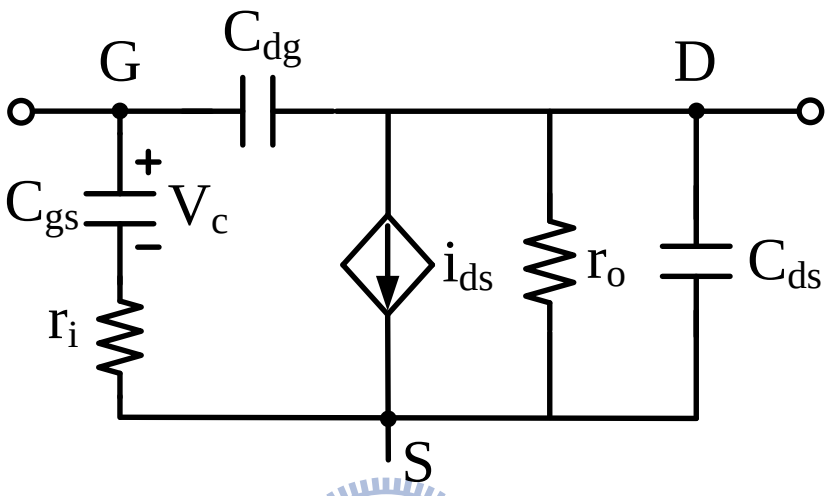

Fig. 4(c)

Theoretically, the artificial-line composed by LC networks will be more and more like the realistic transmission line and the gain should increase by adding more LC-networks which is the gain cell in the mean time. However, there are two principal limitations to gain increasing: the series metal losses from the on-chip inductors as well as the frequency response of the transistors due to the finite input gate resistance and output resistances though the gain-bandwidth product has been superior to other amplification structures. Notice that the distributed architecture consumes higher DC power because of the paralleled gain cells.

Chapter3 DC-20GHz splitter amplifier

3.1 Architecture Analysis

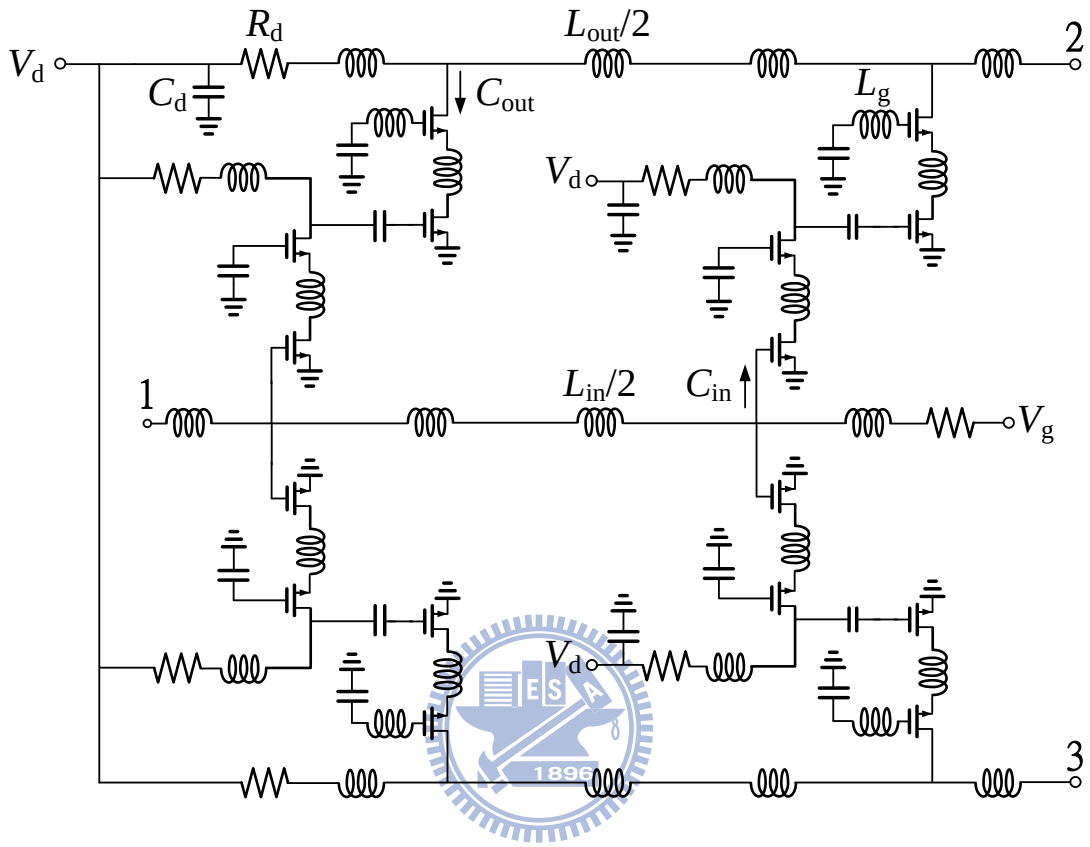

Fig. 5(a)

Fig. 5(a) is the Schematic of the DC–20GHz active power divider where port 1 on the left is for input while ports 2 and 3 on the right are for output. Each gain cell is made of two cascade transistor circuits. Not all the gate biases for the transistors are indicated here.

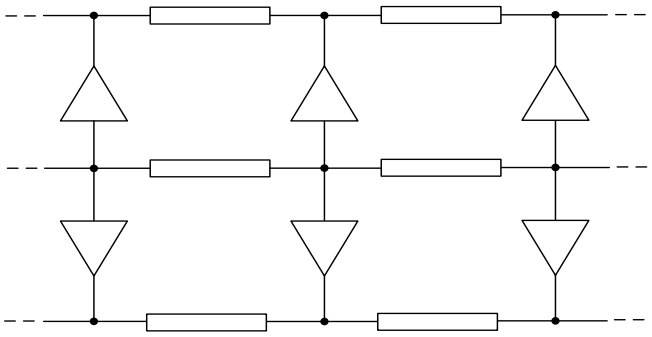

Fig. 5(b)

As shown in Fig. 5(a), the splitter amplifier circuit is made of three parts. The first is the input artificial transmission line where L_{in} is the lumped spiral inductor and C_{in} is the input capacitance of each gain cell; the second part is the gain cell itself which contains two cascode transistor stages; the third is the output artificial $L_{out}C_{out}$ artificial transmission line. For simplicity, the finite series resistance and shunt admittance of all these lines are not included in the circuit schematic. As is well known, the system impedance Z_0 of an infinite-length LC line is

$$Z_0 = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2}{\omega_0^2}\right)} \qquad (3)$$

with the cutoff frequency ω_0 defined as $\omega_0 = 2\sqrt{LC}$ **[4]**. Therefore, compared with the conventional single-input single-output distributed amplifier, the adding of the other parallel transistor stage along the input transmission line may require the use of larger lumped inductors so as to maintain the same system impedance, but this halves the available bandwidth from 20GHz to 10GHz. In our circuit design, on the contrary, we opt for the use of smaller transistors to relieve this bandwidth constraint while keep the input impedance to be still 50Ω.

With smaller input transistor, each gain cell is now composed of two cascode stages for providing sufficient amplification [5], [6]. The inductor L_g allows the output resistance of the gain cell to be slightly negative, thus compensates for the loss of the output transmission line at high frequency [7]. Bandwidth of the output transmission line is limited at high frequency by its cutoff frequency $\omega_H = 2\pi f_H = \omega_0 = 2/\sqrt{L_{out}C_{out}}$ With L_{out} = 0.65nH and

C_{out} = 140fF, we have f_H = 33GHz. With the two output lines terminating at a common C_d = 11.4pF, the corresponding low frequency point is $\omega_L = 2\pi f_L = 2/R_dC_d$. For R_d = 45Ω, the corresponding f_L (now 0.62GHz) can be further reduced through the use of large off-chip bypass capacitor. Position of the loading resistor R_d has been oriented to avoid the use of off-chip inductor.

As shown in Fig. 5(b), this circuit is based on the distributed amplification construction. Therefore, the input and output impedance and cut-off frequency are decided by input and output transmission lines where the splitter amplifier reach wideband purpose. The input and output transmission lines must possess the same phase delay to ensure the signals amplified by different gain stages keeping in construction interference.

3.2 Loss Compensation Topologies

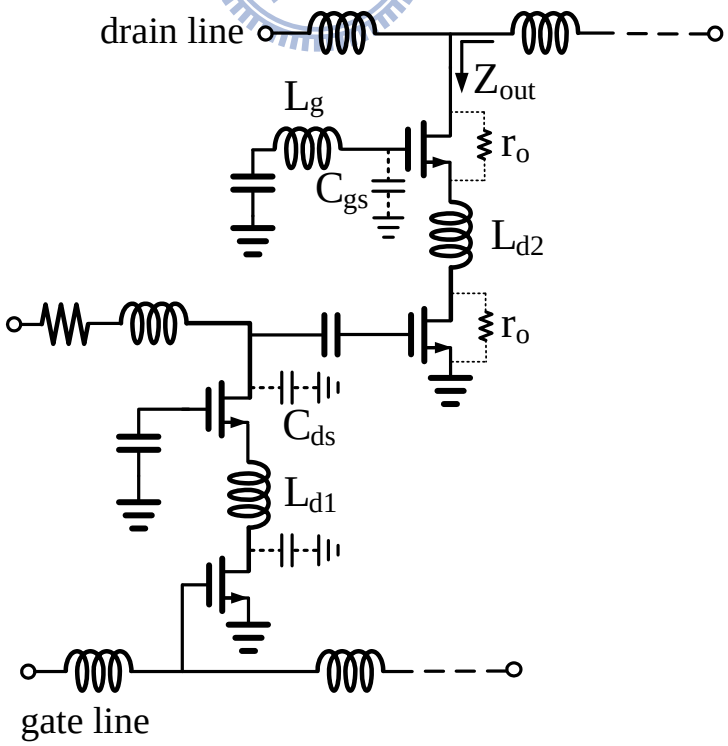

Fig. 6

As predicted in the chapter of distributed amplifiers analysis, there are two principal limitations to gain increasing: the series metal losses from the on-chip inductors as well as the frequency response of the transistors due to the finite input gate resistance and output resistances. To maintain enough gain in high frequency, the gain stage brings to two loss compensation topologies. First method is cascading two cascode pairs of transistors as shown in Fig. 6. Cascode pair series two paralleled resistances r_o. In the traveling wave point view, the signals leaking through the parasitic resistance path decreases while the shunt impedance is larger, as a result of decreasing loss.

In addition to cascade pair of transistors, it introduces gain peaking inductors (L_{d1}, L_{d2}, L_g). L_{d1} and parasitic capacitor C_{ds} produce a short path in a specific frequency to avoid the signal leaking out through the C_{ds} path and passes through the amplified stage more completely. Similarly L_g and parasitic capacitor C_{gs} produce a short path in a specific frequency to avoid the signal leaking out through the C_{gs} path. Furthermore, L_g operates as negative resistance for it decreasing the real part of the output impedance that causes the loss of the drain artificial line. However, the stability is lost when the real part of Z_{out} becomes negative. L_{d2} controls the amount of the negative resistance to maintain stability.

3.3 Manufacturing in CMOS Process

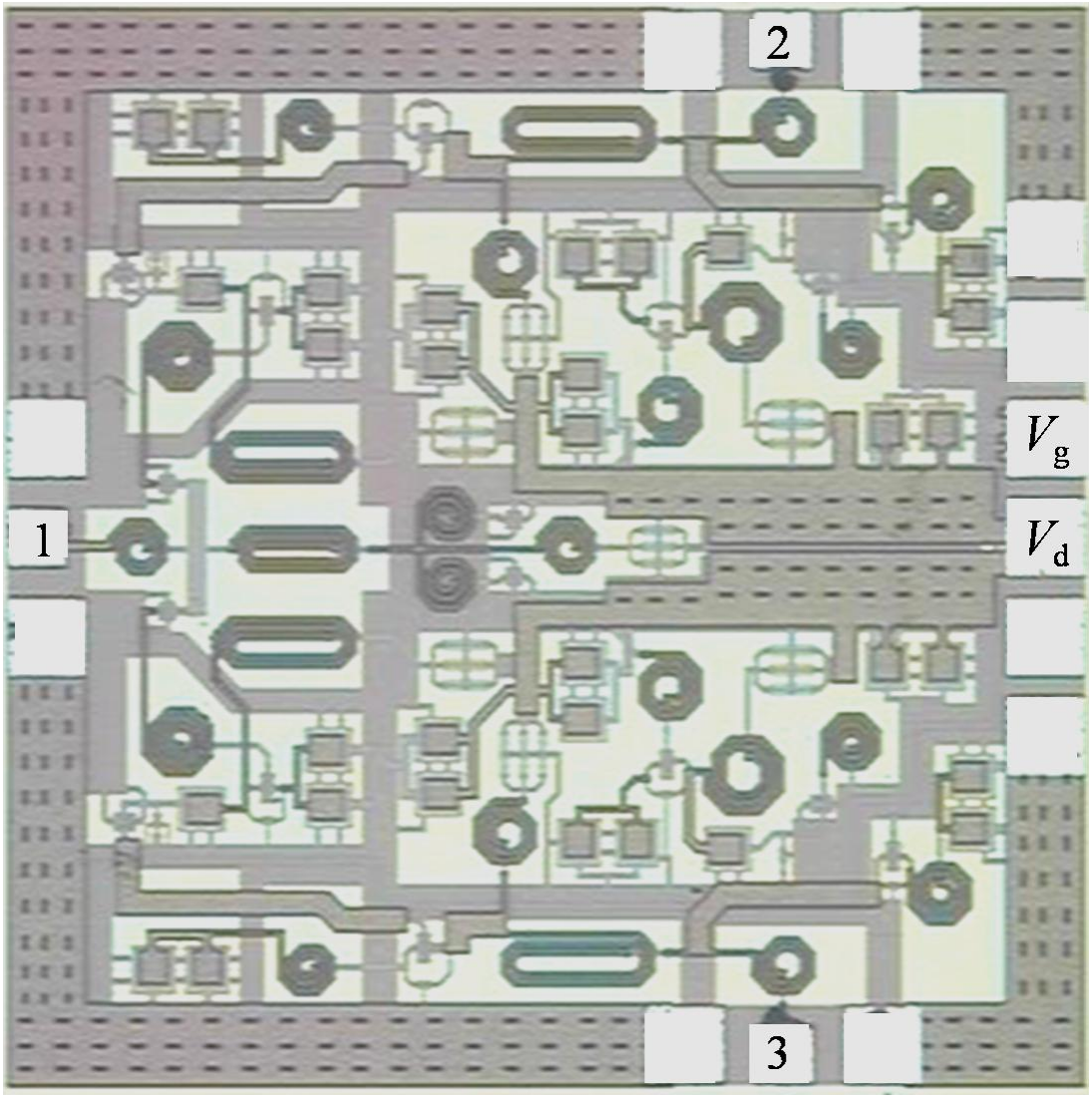

Fig. 7

Fig. 7 shows the photograph of the divider circuit, which is fabricated using commercial 0.18μm CMOS process and the chip size is 1.1×1.1mm^2. To ensure identical outputs, the circuit layout is arranged to be symmetrical. With supply voltage V_d = 2.5Volt and I_d = 64Amp, the total power consumption is 160mWatt; the gate bias voltage V_g is 0.8Volt with negligible current in this case.

3.4 The Simulated and Measured Results

(1) Simulated S-parameters: V_{DD}=2.5 Volt, V_g=0.8 Volt, P_{DC}=120mW

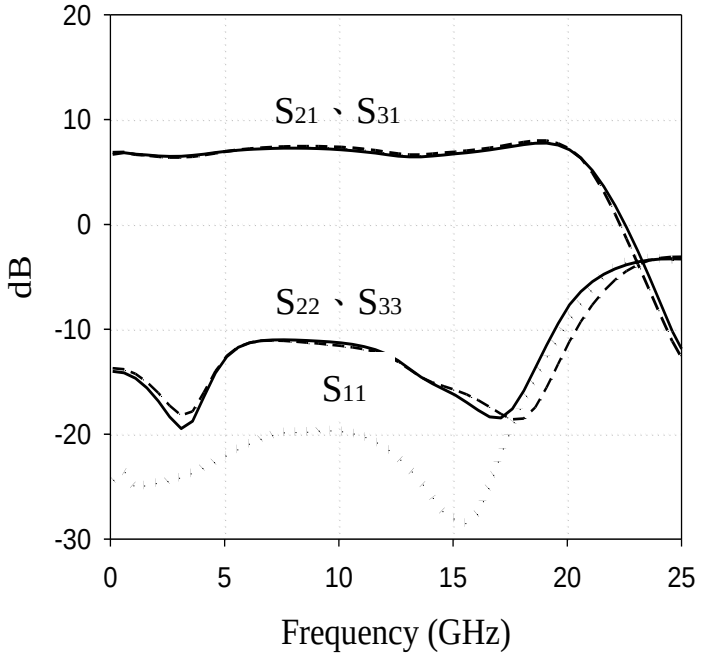

Fig. 8(a)

(2) Measured S-parameters: V_{DD}=2.5 Volt, V_g=0.8 Volt, P_{DC}=160mW

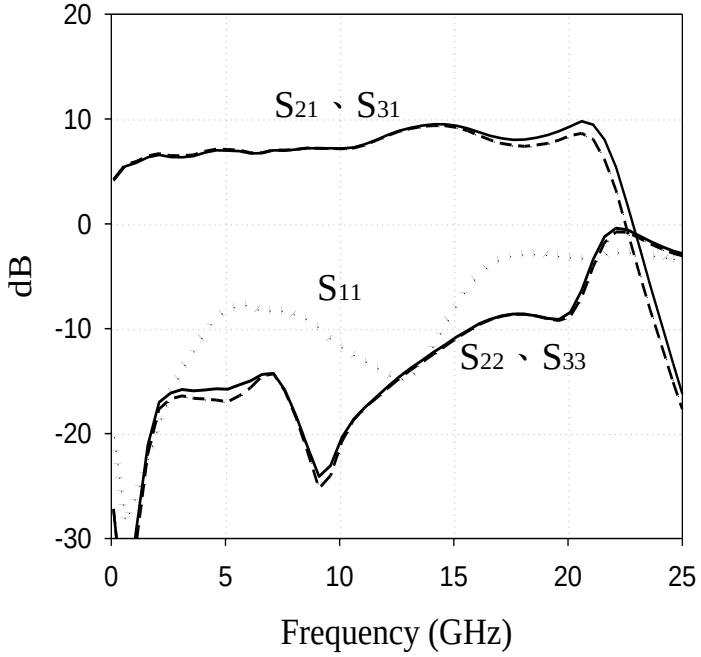

Fig. 8(b)

(3) Isolation (S_{23})

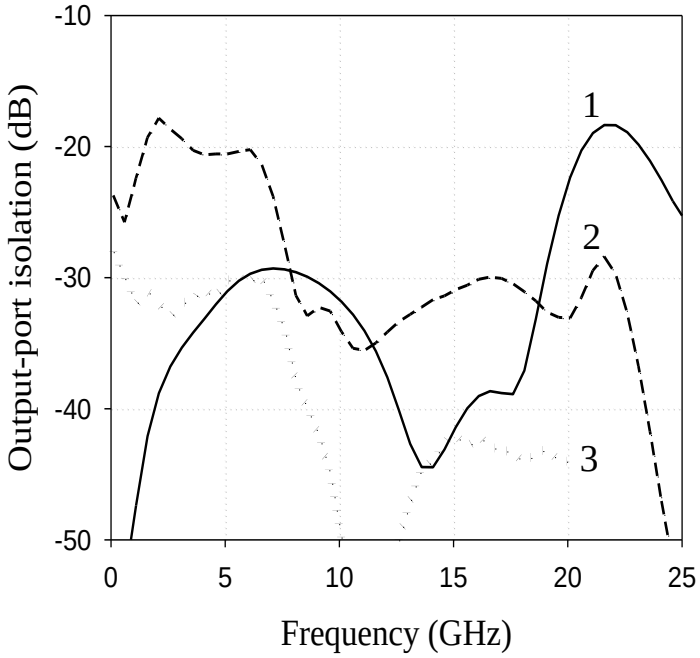

Fig. 8(c)

(4) Measured phase of S_{21} ans S_{31}

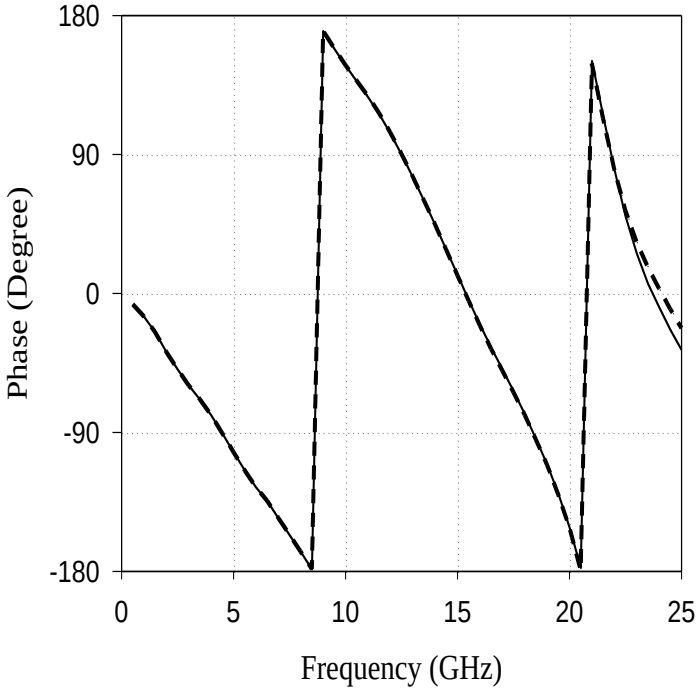

Fig. 8(d) The solid curve is $\angle S_{21}$; dashed curve is $\angle S_{31}$

(5) Measured group delay of S_{21} and S_{31}

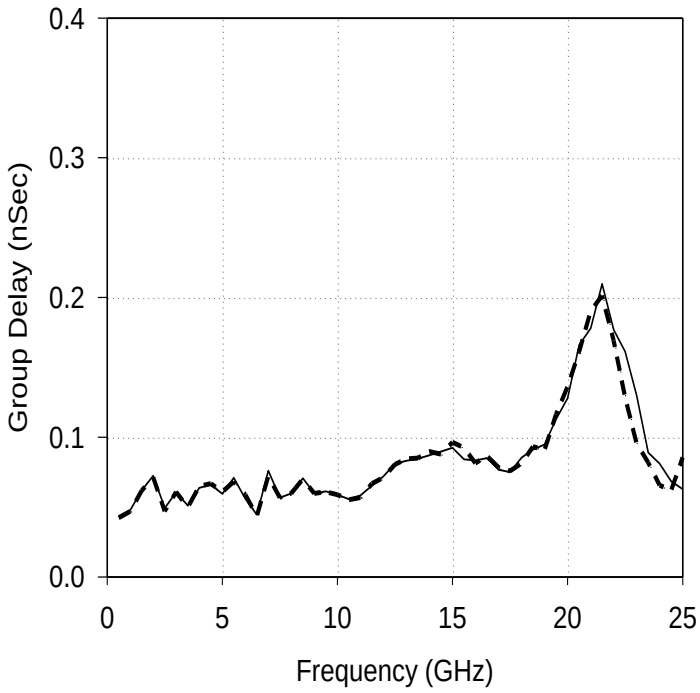

Fig. 8(e)

The solid curve is the group delay out of port 2; dashed curve is out of port 3.

(6) Noise figure

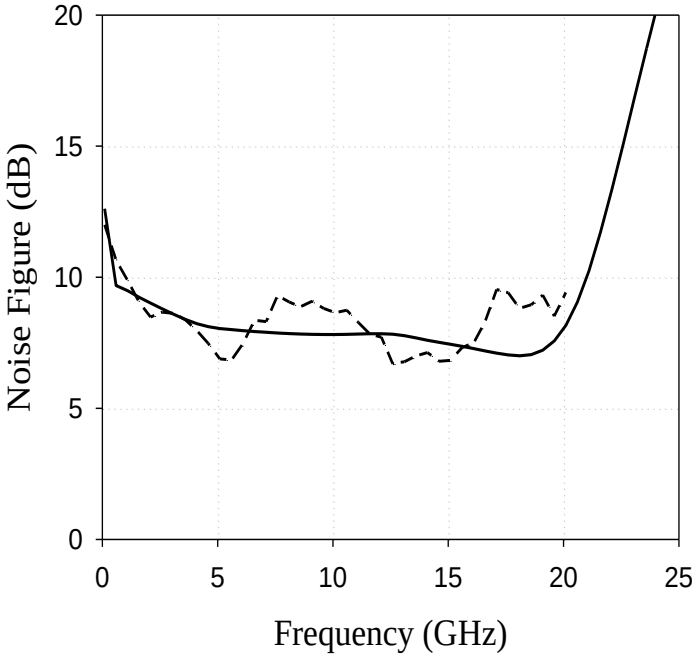

Fig. 8(f) Solid curve: the simulated result; Dashed curve: the measured result.

(7) Measured magnitude imbalance

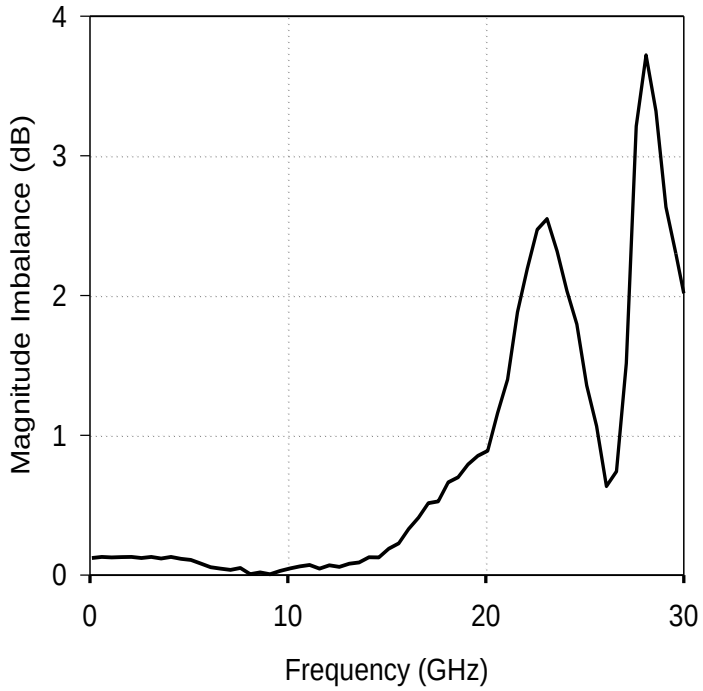

Fig. 8(g)

(8) Measured phase imbalance

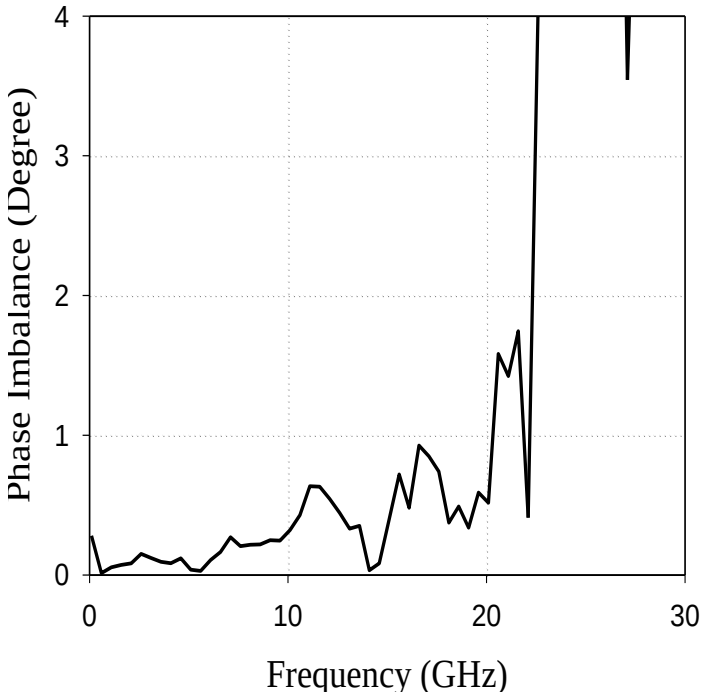

Fig. 8(h)

Fig. 8(a) shows the simulated results. The flat gain is about 7dB and the input and output return losses are below -10dB in the whole bandwidth. Fig. 8(b) shows the on-wafer measured *S*-parameters. The flat gain is about 7.5dB and the input and output return losses are below -10dB in the whole bandwidth.

Validity of this circuit's wideband performance is vindicated by the overlapping S_{21} and S_{31} curves in DC–20GHz. The degradation of S_{23} for frequency below 7GHz is due to the finite impedance of C_d. When a 100pF off-chip bypass capacitor is added, isolation between output ports will be better than 30dB in DC–20GHz as shown in Fig. 8(c). The solid curve #1 is the simulated results, The dashed curve #2 is the measured output port isolation S_{23} without off-chip capacitor on the drain bias pad; the dotted curve #3 is with 100pF off-chip capacitor.

Fig. 8(d) shows the phase of S_{21} and S_{31}. Fig. 8(f) is the noise figure, which is around 8dB across the whole bandwidth but is increasing for frequency below 2GHz. If a resistive feedback scheme is used to replace the 50Ω input loading resistor R_g, the low-frequency noise figure can be reduced [7]**.** Fig. 8(g) and Fig. 8(h) show the magnitude and phase discrepancy of the two output ports where the magnitude imbalance is defined as the absolute value of $20\cdot\mathrm{Log}(|S_{21}/S_{31}|)$, and the phase imbalance in degree is defined as the absolute value of $\angle(S_{21}/S_{31})$.

(9) Linearity

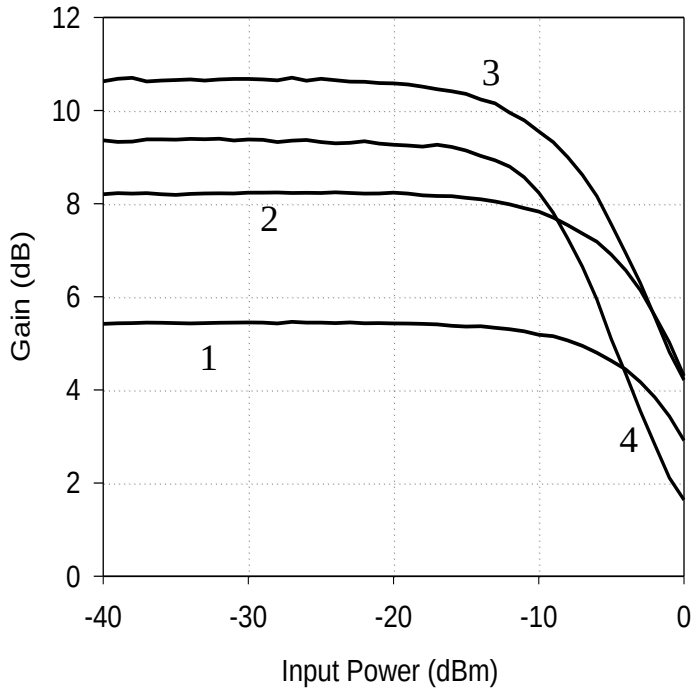

Fig. 9

Fig. 9 #1-#4 is the gain relatively, or more exactly, S_{21}, versus the input power at 0.7, 10, 15, and 20GHz, and their input-referred 1dB compression point is -3.7, -6.3, -10, and -10.5dBm, respectively.

3.5 Conclusion

A DC–20GHz active power divider using 0.18μm CMOS process has been designed and measured here. It has two identical outputs with superb isolation in between, and good matching for the input and output ports. The averaged noise figure is 8dB and the input-referred 1dB compression point is -10dBm at 15GHz. A further improvement of its noise performance and linearity will be our design goals in the near future.

Chapter4 DC-40GHz Splitter Amplifier

4.1 Architecture Analysis

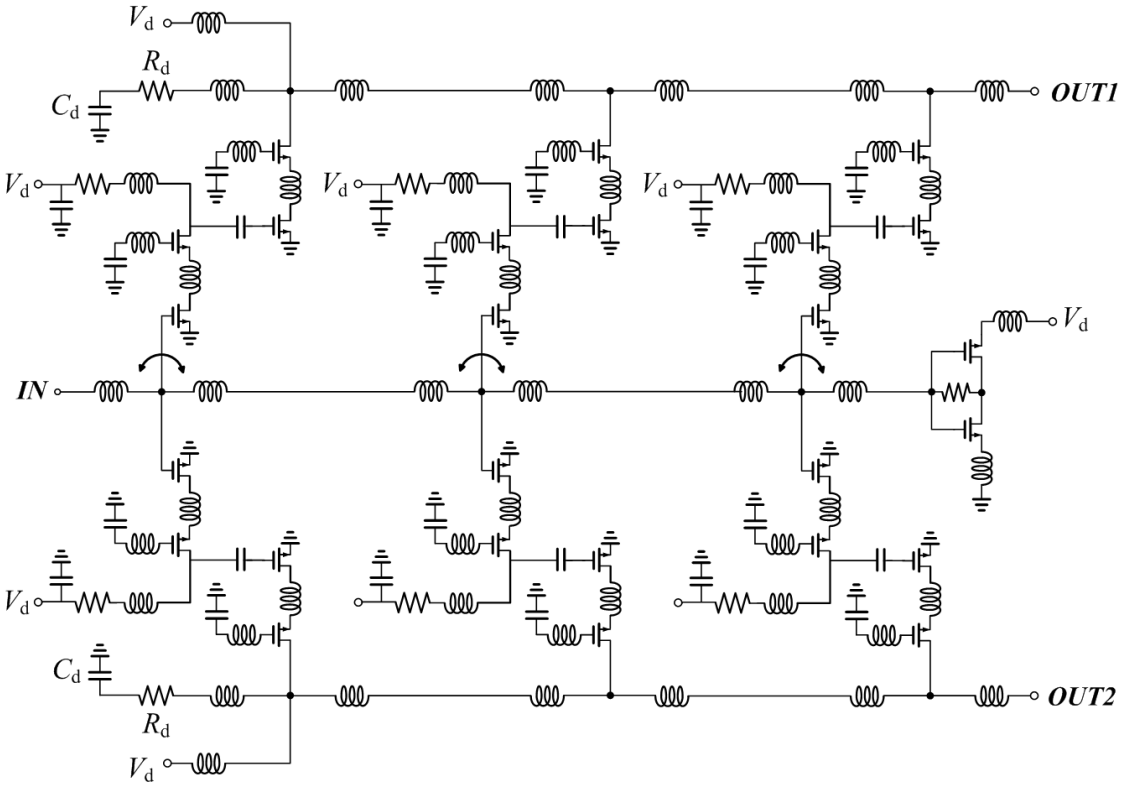

Fig. 10

The DC-40GHz splitter amplifier has the similar architecture to the DC-20 GHz splitter amplifier based on the distributed amplification. This circuit involves three amplification stages to achieve higher gain. The principle improvements are extending input matching bandwidth by using the coupling inductors and decreasing noise figure at low frequency by current reuse replacing of 50-Ω resistance .

4.2 Coupling Inductors

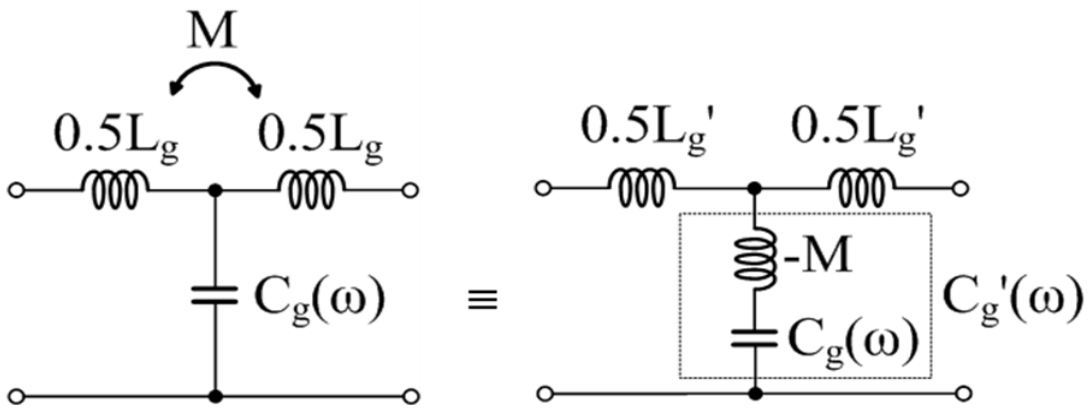

Fig. 11

Begin from the T-networks of L_g and parasitic capacitor C_g , which is shown as Fig. 11., the equivalent circuit would be like the left side of the equal sign while assigning M-value to the coupling magnitude. The equivalent L-value and C-value are

$$C_g'(\omega)=\frac{C_g(\omega)}{\left[1+\omega^2 M * C_g(\omega)\right]} \quad , \quad L_g'(\omega)=0.5L_g+M$$

$$f_g'(\omega)=\frac{1}{\pi\sqrt{L_g' C_g'(\omega)}}=\frac{1}{\pi\sqrt{L_g C_g(\omega)*\left(1-\frac{2M}{L_g}\right)}}$$

Once the M-value is positive (M > 0), the denominator in the frequency formula will decrease and $f_g'(\omega)$ obtain the bigger value. It definitely means that the bandwith has been broad and solve the input bandwidth limitaion caused by twice parasitic capaitors. Moreover, using the coupling inductors can reach the inductance in samller size, minimizing the area.

4.3 Current-Reuse Termination

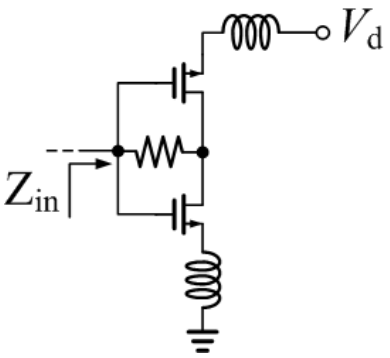

Fig. 12(a)

The gate termination adopts a current reuse replacing of a simple 50-Ω resistance while current reuse can provide a 50-Ωinput impedance in whole band. Current reuse consist of a PMOS and a NMOS transistors with a feedback resistance. The big resistance value will be plus into the denominator of noise formula so that the noise figure is able to decline.

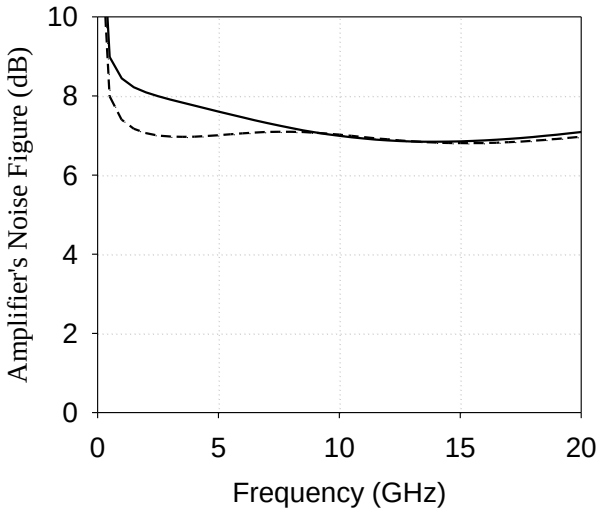

Fig. 12(b)

Solid curve: simple 50-Ωresistance; dashed curve: current reuse

As shown in Fig. 12(b), noise figure can decrease effectively below 5GHz band. Another advantage of using current reuse is that it can provide gate voltage for transistors without adding another set of voltage so as to promote integrity.

4.4 Manufacturing in CMOS Process

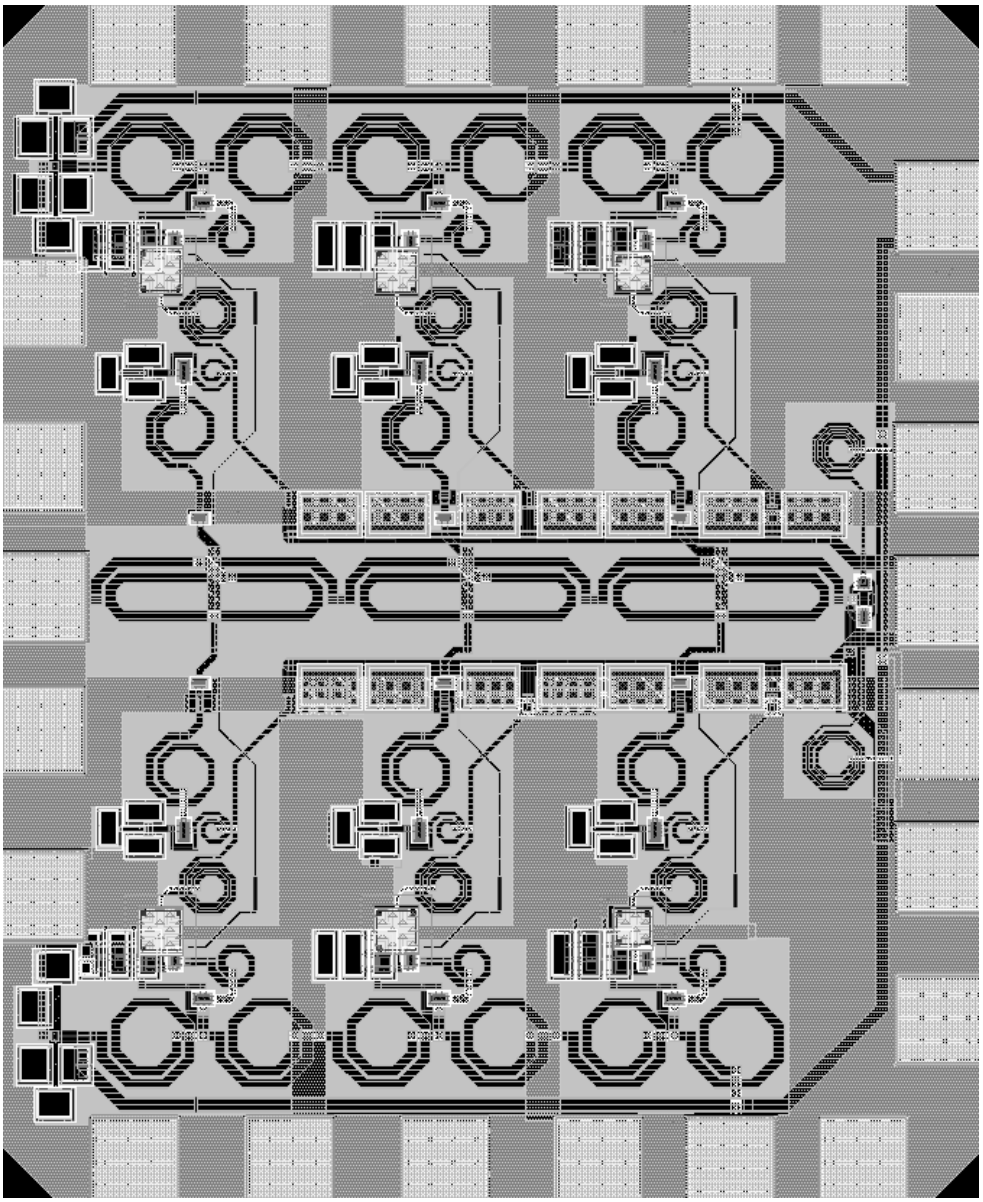

Fig. 13

Fig. 13 shows the photograph of the divider circuit, which is fabricated using commercial 90*n*m CMOS process and the chip size is $0.8\times0.98\text{mm}^2$. The layout has differences at coupling inductors and DC-bias metal line. With supply voltage V_d = 2Volt and I_d = 50Amp, the total power consumption is 100mWatt; the gate bias voltage V_g is 0.8Volt with negligible current in this case.

4.5 The Simulated and Measured Results

(1) S-parameters: V_{DD}=1.5 Volt, V_g=0.65 Volt, P_{DC}=70mW

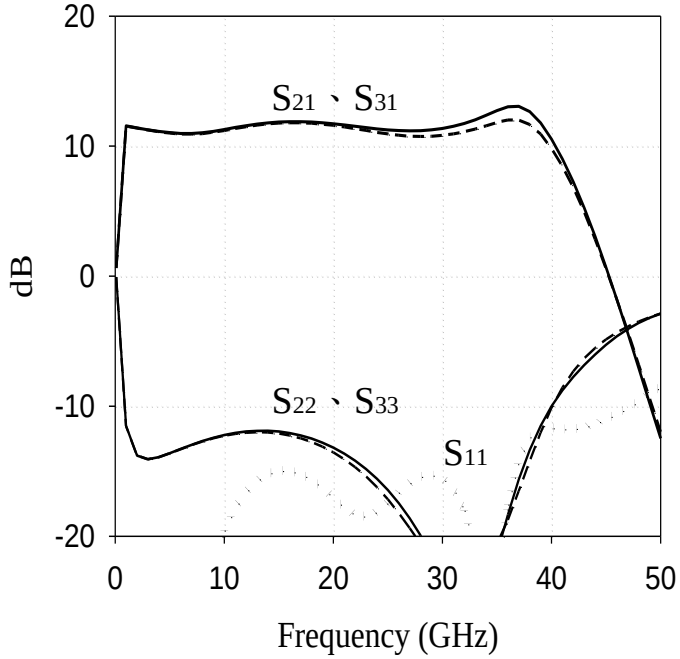

Fig. 14(a)

(2) Measured S-parameters: V_{DD}=2 Volt, V_g=0.8 Volt, P_{DC}=100mW

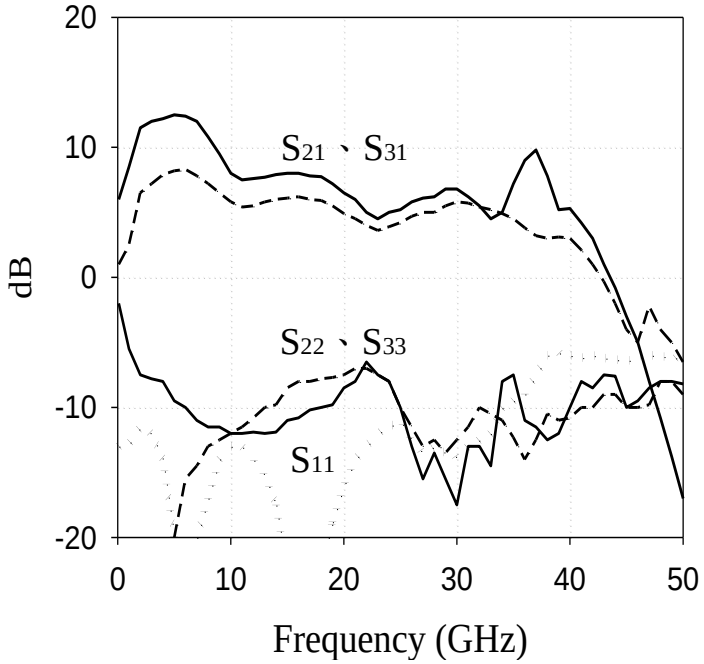

Fig. 14(b)

(3)Simulated Isolation (S_{23}):

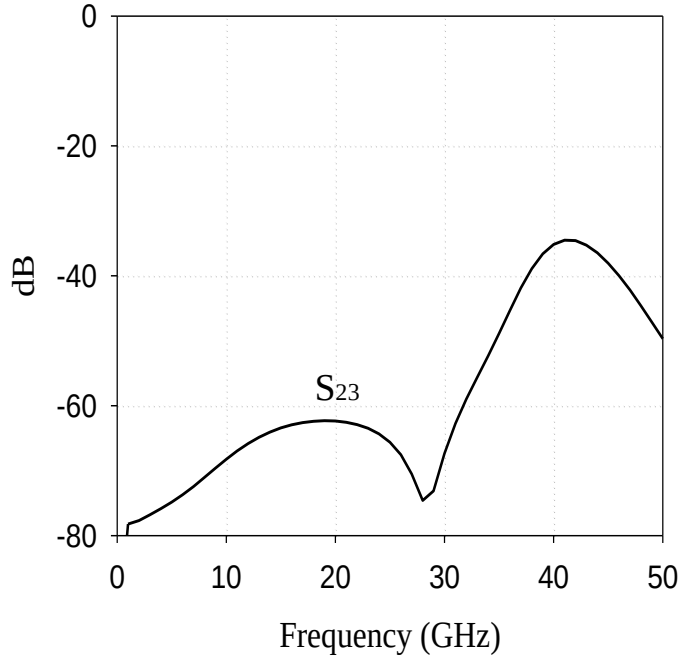

Fig. 14(c)

(4) Simulated Noise Figure :

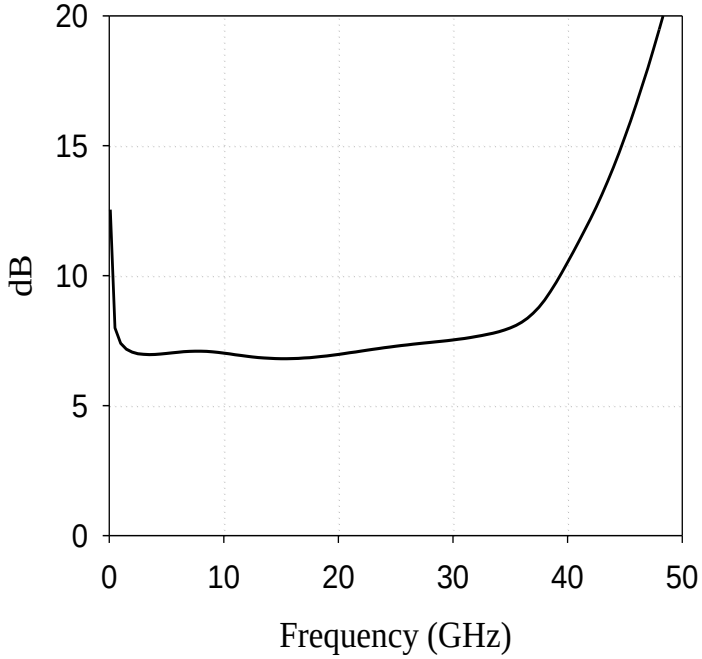

Fig. 14(d)

Chapter5 The Measurement Concerns

The measure items include S-parameters, noise figure and P1dB. It needs 4-ports measurement system as shown in Fig. 15(a). The DC-block capacitor between network analyzer and probe has been considered in simulation. The range is 0.1-20GHz with 201points, sampling 128 times. Input power is -20 dBm. The network analyzer type is HP 8510C.

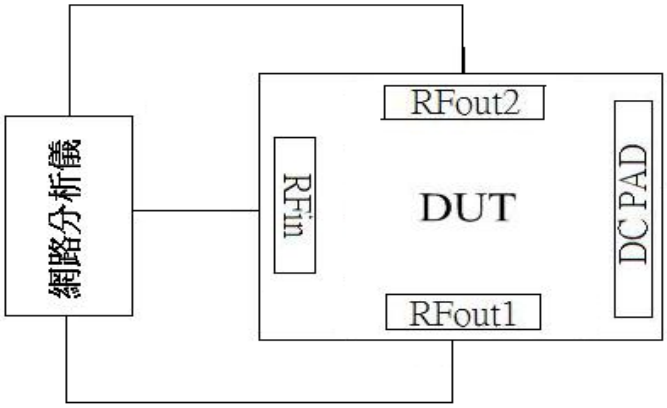

Fig. 15(a)

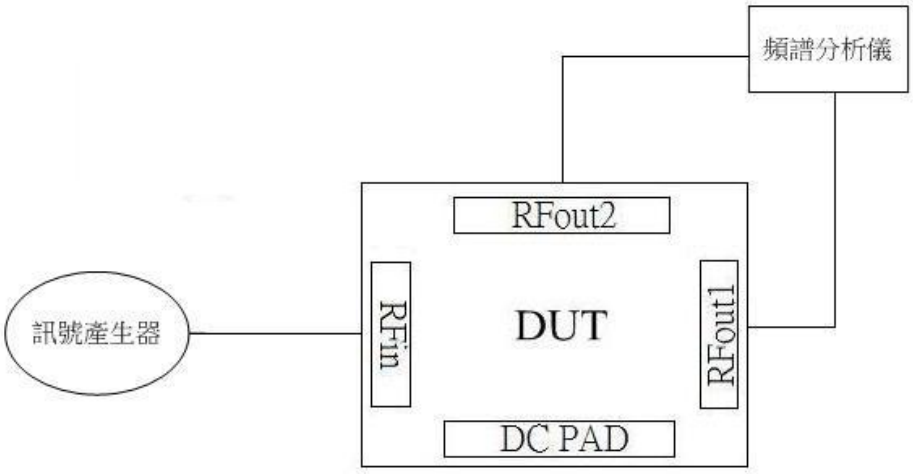

Fig. 15(b)

As shown in Fig. 15(b), the input port connects the signal generator Agilent E8247C. By sweep the input signals and observe the graph on the network analyzer, we can find out the P1dBs corresponding frequency.

Chapter6 References

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