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博 士 論 文

新型PHINES和PREM快閃記憶體及氮化矽型發光電晶體之研究

Investigation of Novel PHINES and PREM Flash Memories and Silicon-Nitride Based Light Emitting Transistor

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摘要

在本論文中，我們研究兩種新型非揮發性快閃記憶體架構：PHINES (Programming by hot Hole Injection Nitride Electron Storage)和 PREM (Programmable Resistor with Erase-less Memory)。另外我們也研究一種新式的氮化矽型發光電晶體 (Silicon-Nitride based Light Emitting Transistor：SiNLET)。我們將介紹並討論這些元件的結構、操作原則及元件特性。

在第二章中，我們架構了一種新型的 PHINES 記憶胞。PHINES 是使用氮化矽缺陷捕捉儲存的元件結構。抹除(Erase)是利用 Fowler-Nordheim 電子注入提昇臨界電壓(threshold voltage)的方式，程式化(Program)是利用帶對帶穿遂產生之熱電洞注入以降低局部臨界電壓的方式。PHINES 可達成一個記憶胞儲存二位元、低功率抹除與程式化、高的寫入抹除次數(Endurance)及好的資料保持力(Retention)。以外，PHINES 記憶胞可以被編排在 NOR 型和 NAND 型陣列中，並可同時使用於編碼快閃記憶體(Code flash memory)和資料存取快閃記憶體(Data flash memory)的應用。在第三章中，我們引進一種新型的帶對帶穿遂電流讀取方式(BTB sensing scheme)和一種改良的 NAND 型陣列。PHINES 記憶胞使用帶對帶穿遂電流讀取方式後，將可以排除二位元間的相互干擾(2-bit interaction)，並且在二位元操作時，得到非常大的操作空間和非常好的元件特性。在第四章中，我們將討論 PHINES 記憶胞在微縮時的挑戰。PHINES 記憶胞顯示出非常好的微縮能力。在 NAND 型陣列架構下，一位元與二位元儲存的 PHINES 記憶胞分別可以微縮到十五奈米和三十奈米世代。

在第五章中，我們發表了一種應用於系統單晶片的新型 PREM 快閃記憶胞。PREM 結合了一種新式 “無抹除”的操作法和超薄氧化矽中漸進式崩潰的特性。在 CMOS 標準製程中，其製程完全不需額外的光罩或只需一道額外的光罩。PREM 記憶胞具有多次寫入(Multi-time programming)、多值記憶(Multi-level cell)、非揮發性、和低壓操作的特性，並且具有很好的可靠度。

在第六章中，我們研發了一種新式的氮化矽型發光電晶體。此三端電致發光元件是使用 SONOS 型元件結構，而且製程與 CMOS 元件製程相容。光子的產生是介由 Fowler-Nordheim 電子注入、帶對帶穿遂產生之熱電洞注入、及載子經由氮化矽缺陷捕捉與再結合等機制綜合所造成。氮化矽型發光電晶體的元件等效面積只有 0.616μm^2，適合於顯示器與光通訊等的應用。

Investigation of Novel PHINES and PREM Flash Memories and Silicon-Nitride Based Light Emitting Transistor

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Abstract

In this dissertation, we investigate two novel non-volatile flash memory architectures named PHINES (Programming by hot Hole Injection Nitride Electron Storage) and PREM (Programmable Resistor with Erase-less Memory). We also study a novel Silicon-Nitride Based Light Emitting Transistor (SiNLET). The cell structures, operation principles, and device performances are introduced and discussed.

In chapter 2, we construct a novel PHINES memory cell. PHINES uses a nitride trapping storage cell structure. Fowler-Nordheim injection is performed to raise Vt in erase while programming is done by lowering a local Vt through band-to-band tunneling induced hot-hole injection. Two-bits-per-cell feasibility, low power program/erase, good endurance, and good data retention are demonstrated. PHINES cells can be arranged in NOR-type and NAND-type array for both code and data flash applications. In chapter 3, a novel BTB sensing scheme and a modified NAND-type array are introduced. PHINES cell with BTB sensing scheme can eliminate the issue of 2-bit interaction, and a large operation can be obtained in 2-bits-per-cell operation. In chapter 4, the scaling challenges of PHINES cell are discussed. PHINES memory cell shows high scalability, and 15nm generation for 1-bit-per-cell storage and 30nm generation for 2-bit-per-cell storage are feasible in NAND-type array architecture.

In chapter 5, a novel non-volatile memory cell named PREM is proposed for

SOC applications. PREM combines a novel ìerase-lessî algorithm and the progressive breakdown of ultra-thin oxide. No extra mask is needed with CMOS standard process. MTP (multi-time programming), MLC (multi-level cell), non-volatility, and low voltage operation are realized. Good reliability is demonstrated.

In chapter 6, a novel silicon-nitride based light-emitting transistor (SiNLET) is investigated. This three-terminal electroluminescence device uses a SONOS-type structure, and its process is compatible to standard CMOS devices. Photons are generated by Fowler-Nordheim electron tunnel-injection, band-to-band tunneling induced hot-hole injection, and carrier trapping/recombination via nitride traps. SiNLET with an effective device area of 0.616 μm^2 is demonstrated for display and optical communication purposes.

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Chapter 1

Introduction

1.1 An Overview of Mass Storage Flash Memory Technologies

Today, flash memory has come of age as a mainstream memory product, and its technologies and markets will become more diversified. It can be classified into two major markets: code storage application and data storage application (see Fig.1.1). NOR-type flash memory [1.1] is most suitable for code storage application, such as cellular phone, PC bios, and DVD player. NAND-type flash memory [1.2] has been targeted at data storage market, which is an emerging application such as PDA, memory cards, multi-media audio, and digital still camera. Fig.1.2 discloses the memory market, and flash memory share increased rapidly in the last few years.

Conventional NOR-type and NAND-type flash memories use the same floating gate structure as shown in Fig.1.3. Table 1.1 shows the ITRS roadmap [1.3] for flash memory cells. NOR-type flash memory cell has good visibility into 90nm and 65nm generation. Current projection shows that scaling continues at 45nm node but is challenged to meet the goal of 50% cell size shrinkage [1.1,1.4]. NOR-type flash memory has two scaling limiters. One is the non-scalability of tunnel oxide and inter-poly ONO due to reliability concerns. The other is caused by the channel hot electron programming, which requires an internal voltage of more than 8V, and imposes the limit of the cell gate length [1.4]. Besides, the process complexity increases dramatically to shrink the memory cell size, which makes the cost ineffective. NAND-type flash memory cell meets another scaling limitation caused by floating gate interference. Vt shift is caused by the Vt change and capacitive coupling of the adjacent cells. It is very likely that the practical limit of NAND-type flash memory is at 30nm technology node [1.5].

Instead of the process scaling, one important innovation in cost reduction is multi-level cell (MLC) operation. Although MLC operation can double the memory density [1.6], scaling limitations of conventional floating gate memory cell mentioned above are coming in the near future. Accordingly, several new memory concepts are under investigating to maintain Mooreís law as shown in Table 1.2. Nitride trapping storage flash memory [1.7] and nano-crystal flash memory [1.8] are evolutionary approaches, and their processes are compatible to the standard CMOS process. FeRAM [1.9], MRAM [1.10], PRAM [1.11], and Polymer [1.12] memory architectures are revolutionary approaches with new materials. Although many efforts and resources have been devoted to develop these memory cells, most emerging

memories still have reliability problems, and are not commercially available for fabricating yet except for the nitride trapping flash memory.

1.2 Introduction of SONOS Flash Memory Cell

SONOS flash memory cell (Fowler-Nordheim tunnel program by electron and direct tunnel erase by hole [1.7]) has been proposed for years. As shown in Fig.1.4, the carriers are stored in the traps of the nitride layer between the top and the bottom oxides. SONOS cell offers several advantages over conventional floating gate memory cells: simple process, ease of manufacturing, no erratic bit, not sensitive to oxide defects, and no floating gate coupling effect. However, the cell retention is an issue due to the thin bottom oxide. Besides, its large cell size ($6F^2$) and slow program/erase speed limit its applications. Recently, SONOS cell has evolved into a 2-bits-per-cell storage architecture (NROM [1.13]) by utilizing the localized charge trapping effect of nitride. Localized trapping nitride trapping storage memory cell enables a memory cell to hold twice as much data as the standard memory cell, without compromising device endurance, performance or reliability.

NROM flash memory cell structure is shown in Fig.1.5, and the operation principle is shown in Table 1.3. NROM programs its memory cell by channel hot electron injection as conventional NOR-type floating gate memory does, which is suitable for code storage applications. Erase is done by band-to-band tunneling induced hot-hole injection. A novel ìreverse read schemeî [1.13] is introduced to realize physically 2-bits-per-cell operation. NROM holds 2 physical bits in one cell above the source and drain junction, which is more reliable alternative to MLC solutions in the floating gate memory cell. MLC products suffer from performance and reliability concerns when detecting between multiple charge levels. Although NROM cell has many advantages over conventional floating gate memory cells, it can only be applied to code storage application due to its high power consumption and slow program speed in program operation. Previous works [1.14-1.15] reveal that reliability issues including read disturb, over erasure and cell retention after cycling are major challenges. Besides, 2-bit interaction effect resulted from the reverse read scheme also limits the device scalability [1.16]. In this dissertation, we construct a novel nitride trapping storage memory cell. The memory cell does not suffer 2-bit interaction issue and shows great performance for the candidate of next generation flash memory technology.

1.3 Introduction of Embedded Flash Memory Technologies

The requests for high performance system combining CMOS devices and embedded flash memories have increased for SOC applications (smart cards, cellular

communications, automotiveÖ). However, the integration of CMOS devices and conventional floating gate flash memories shows difficulties in terms of complex process and high cost. Besides, high periphery voltages, large current pumper, and high voltage transistors are necessary to operation the memory cell, which will consume active area, complicate the process, and increase die cost as shown in Fig.1.6. Although several memory cells [1.17-1.19] have been proposed for embedded applications, the device scalability and/or cell reliability are still issues. These memory devices also face scaling challenges due to the non-scalable gate stack for the consideration of cell retention. Therefore, the development of a high performance memory cell with non-volatility, low voltage operation, good reliability, high-density storage, good scalability, and simple process (CMOS compatible) is essential for embedded markets. In this dissertation, we report a novel embedded flash memory cell and its process is compatible to CMOS devices. The memory performance and array architecture are discussed.

1.4 Introduction of Light Emitting Devices

Electrical wires meet a fundamental limitation of aspect ratio, and capacitive coupling, which reduces the bit rate. Below 0.13um, interconnect delay starts to dominate over gate delay in Si CMOS. The scaling limitations of electrical wires give an opportunity for optical interconnects. Optical interconnection avoids the issue of aspect ratio. They can replace global wires to provide high data rates. III-V based optical devices are widely accepted due to its direct bandgap and high photon emission efficiency. Silicon is not considered as a good light-emitting source due to its indirect bandgap induced low emission efficiency.

Although silicon optical devices suffer lower light emission efficiency, their applications are numerous (see Fig.1.7) due to the ease of integration in CMOS-based ultralarge scale integrated circuit (ULSI) as shown in Fig.1.8. Silicon light emitting devices can also be used in massively parallel optical interconnects and cross connects for microprocessor and digital-signal processor applications. Traditionally, silicon LEDs have been regarded as a difficult candidate for light emission since they suffer low light emitting efficiency due to the indirect band-gap of silicon. Recently, many attempts including p-n diodes [1.21], MIS diodes [1.22], and nanocrystal LEDs [1.23] have shown that light emission from silicon materials is readily obtained.

1.5 Organization of this Dissertation

In this dissertation, a novel PHINES (Programming by hot Hole Injection Nitride Electron Storage) flash memory cell is investigated. PHINES uses the nitride storage cell structure. PHINES cell, with its superior reliability, 2 bits-per-cell storage and low

power operation, can meet the need of both code and data storage applications. Chapter 2 will discuss the cell structure, operation principles, array architecture, and reliability characteristics. In chapter 3, a novel BTB sensing scheme and a new modified NAND-type array are introduced to eliminate the issue of 2-bit interaction. Chapter 4 discusses the scaling challenges of PHINES memory cell.

In chapter 5, we construct another novel non-volatile flash memory cell named Programmable Resistor with Erase-less Non-Volatile Memory (PREM). PREM can realize multi-time programming, multi-level cell operation, non-volatility, and low voltage operation, and can meet some applications in SOC and embedded areas.

In chapter 6, we develop a novel Silicon-Nitride based Light-Emitting Transistor (SiNLET) with high light emission efficiency, low current consumption and a small device area. The fabrication process of SiNLET is compatible to CMOS technology. SiNLET demonstrates its high feasibility for the application of optical interconnects in ULSI.

Finally, a conclusion will be given in chapter 7.

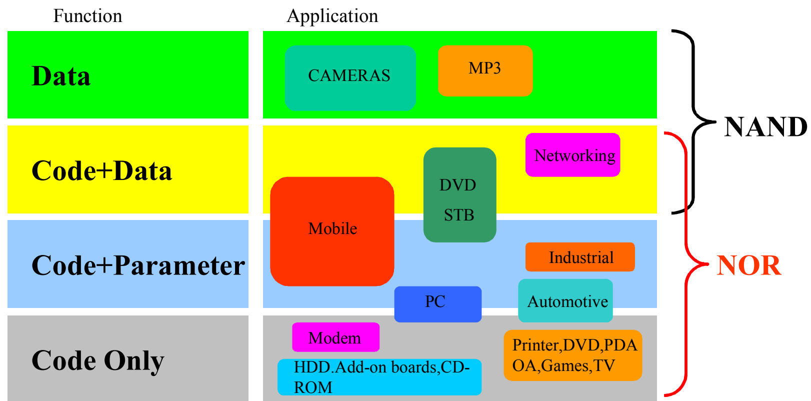


Fig.1.1 Major applications of flash memories (refer to Web Feet Inc. 2003).

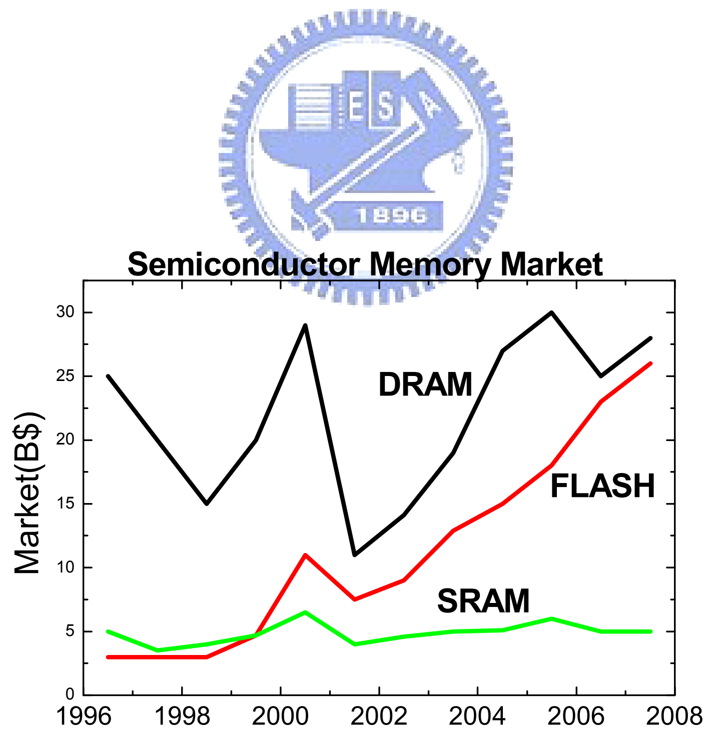


Fig.1.2 Forecast of memory market share (refer to Web Feet Inc. 2003).

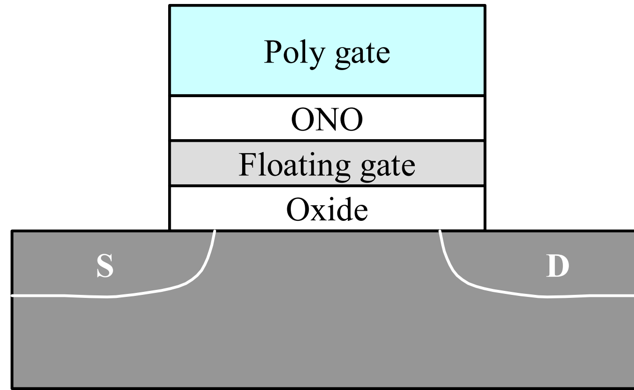


Fig.1.3 The cell structure of a floating gate flash memory cell.

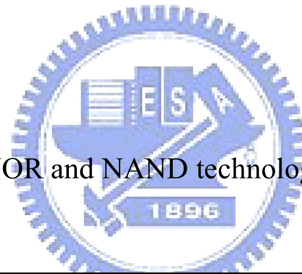


Table 1.1 NOR and NAND technology roadmap in ITRS 2002.

Year		2001	2004	2007	2010	2013
Technology node (nm)		130	90	65	50	35
NOR	Cell Size (F^2)	10	10	11 ~14	12 ~15	13 ~16
	Cell Size (μm^2)	0.16	0.081	0.053	0.034	0.018
NAND	Cell Size (F^2)	5.5	5.5	4.5	4.5	4.5
	Cell Size (μm^2)	0.093	0.045	0.019	0.011	0.006

Table 1.2 Summary of emerging non-volatile memories.

Transistor Vt shifts	Charge Displacements	Resistance Change
1. Floating gate 2. Nitride trap 3. Nano-crystal	1. Crystalline Ferroelectric 2. Polymer Ferroelectric	1. Magnetic: GMR or MJT 2. Phase Change 3. Polymer ionic transport

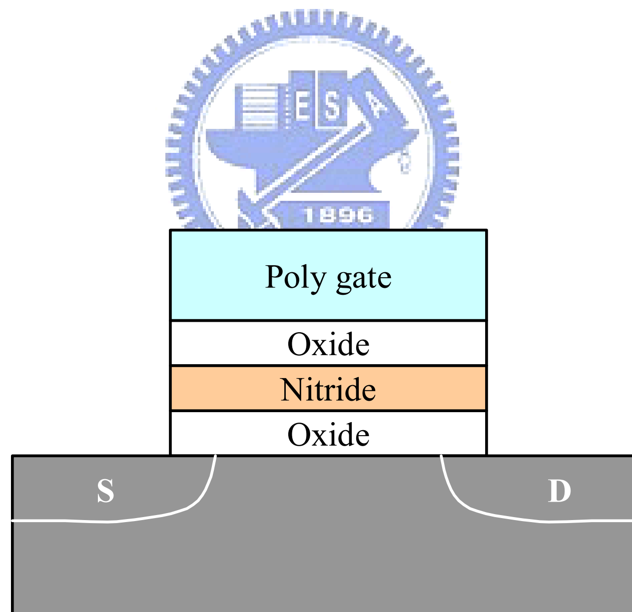


Fig.1.4 The cell structure of a nitride storage flash memory cell.

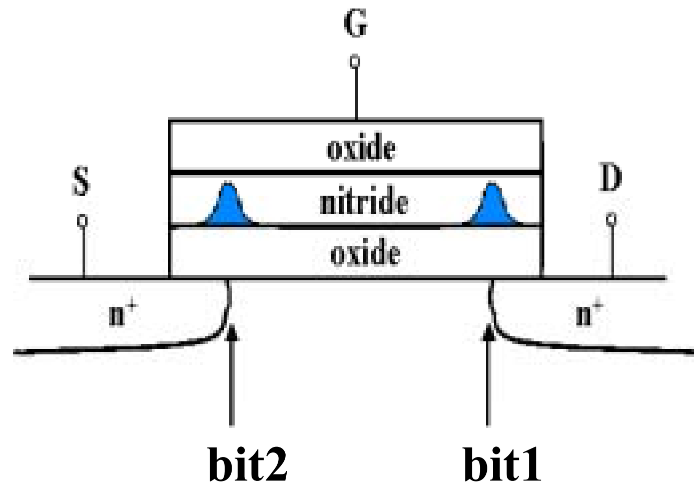


Fig.1.5 Schematic representation of a NROM cell with physically 2-bits storage. The shaded area in the nitride layer represents stored charges.

Table 1.3 Operation bias conditions of a NROM cell.

		Program	Erase	Read
Bit 1	Vg	11V	-3V	2.5V
	Vd	5V	8V	0V
	Vs	0V	0V	>1.5V
Bit 2	Vg	11V	-3V	2.5V
	Vd	0V	0V	>1.5V
	Vs	5V	8V	0V

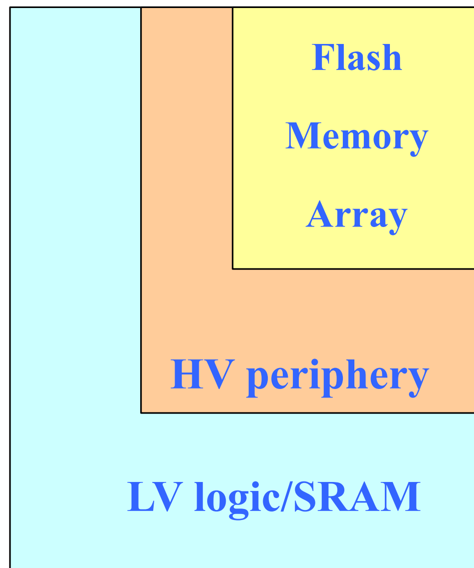


Fig.1.6 Schematic representation of the chip architecture with embedded flash memory array, high voltage periphery control circuit, and low voltage logic circuit.

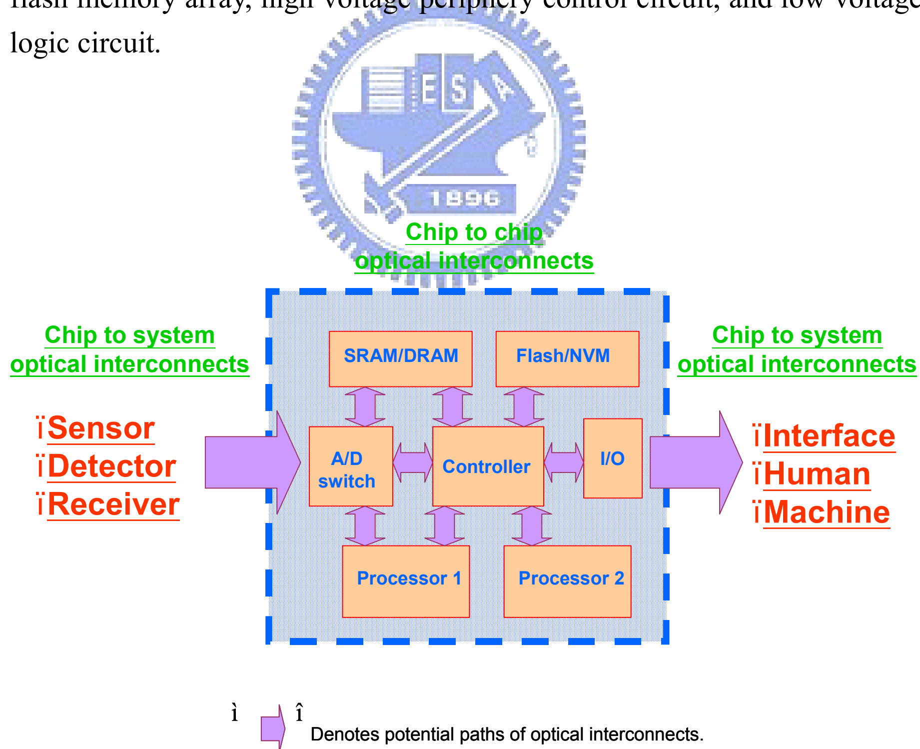


Fig.1.7 Illustration of applications and insertion of optical interconnections.

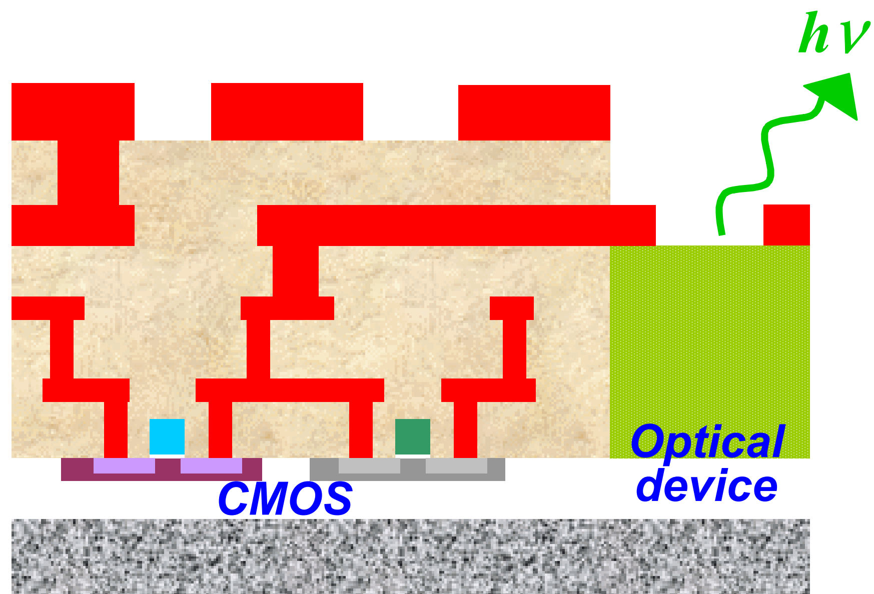


Fig.1.8 Illustration of integration of CMOS and silicon optical devices.

Chapter 2

PHINES Flash Memory Cell with Low Power Program/Erase, Backward-Read Scheme and 2-bit-per-cell Storage

2.1 Introduction

Interest in nitride based localized trapping storage flash memory cells has revived for 2-bits-per-cell operation, which can double the memory density [2.1-2.3]. Besides, they also show better scalability since charges are stored in the nitride traps rather than a poly-silicon floating gate in conventional flash memory cells. Nitride storage memories do not have floating gate induced drain turn-on and coupling issues that are believed to be the scaling limitations of conventional floating gate memories [2.4,2.5]. Various operation schemes were proposed based on the nitride-storage cell structure. SONOS flash memory with modified Fowler-Nordheim-tunneling programming by electrons and direct-tunneling erasing by holes was proposed long time ago [2.6]. The absence of erratic bits and low power operation make SONOS a good candidate for next generation flash technology. However, the cell retention is still an issue now [2.7]. Besides, its large cell size ($6F^2$ per bit [6]) and slow program/erase speed limits its applications. Recently, NROM cell with channel-hot-electron (CHE) programming and band-to-band tunneling induced hot-hole (BTBT HH) erasing [2.2] has demonstrated excellent intrinsic cell performance. NROM cell is suitable for code flash applications, and CHE programming is widely accepted in NOR-type architecture. In spite of many advantages, previous works [2.8-2.13] reveal that reliability issues including read disturb, over erase, and cell retention after cycling are major challenges of NROM cell. C.T. Swift et al proposed to use uniform tunneling for erasing [2.3] instead of the hot-hole injection to reduce the stress of high energetic holes in the erase operation. However, for mass storage and data flash applications, CHE programming is still not suitable due to its high power consumption.

Here, a novel flash memory cell named PHINES (Programming by hot Hole Injection Nitride Electron Storage) [2.1] is investigated. PHINES uses the nitride storage cell structure and can be arranged in both NOR-type and NAND-type array for code and data flash applications. The operation principles, cell characteristics, and cell reliability will be studied and characterized in this chapter.

2.2 PHINES Cell Structure

PHINES memory cell is a NMOSFET with an ONO stack as the gate dielectric

(Fig.2.1). The test single cell is arranged in a virtual-ground array as shown in Fig.2.2, which is free of field isolation. The key cell parameters are listed in Table 2.1. The gate length and gate width are 0.19μm and 0.14μm, respectively. The thickness of each ONO layer is 9nm, 6nm, and 6nm from top to bottom. The top oxide and bottom oxide are formed by thermal oxidation while nitride is performed by CVD deposition. A double poly technology, novel low-temperature dielectric film fill-in and planarization process is introduced to form a sufficiently thick insulating layer between the local buried-diffusion (BD) bit-lines and the word-lines (WLs) [2.14]. Figure 2.3 (a) and (b) show the TEM pictures of the cell, in which the X-pitch and Y-pitch are 0.33μm and 0.28μm, respectively.

2.3 PHINES Cell Operation Condition, and Cell Characteristics

2.3.1 PHINES Cell Operation Condition

PHINES cell uses gate FN electron injection (negative gate-to-substrate bias) and BTBT HH injection as the erase and program methods, respectively. Schematic representations of PHINES cell operation are shown in Fig.2.4. The bias conditions are given in Table.2.2. Figure 2.5 shows the erasing characteristics and the Vt saturates after 1ms. As shown in Fig.2.6 (a), electrons are injected from the gate via tunneling through the top oxide (path 1) in the erase operation. Some of the tunnel electrons are captured by the nitride traps (path 2, either deep traps or shallow traps), while the others will inject into the substrate (path 3). Electrons in the shallow traps will easily be drawn out due to the high electric field (path 4) and only electrons in deep traps remain in the nitride. Accordingly, the erase saturation may be caused by the limited amount of deep nitride traps, and cell Vt will saturate while all deep traps are filled with electrons. PHINES cell does not have an over-erasure problem due to the self-convergent behavior of FN injection, which can improve the uniformity and tighten the Vt distribution of the erased cells.

The program of a PHINES cell is done by lowering the local Vt through edge BTBT HH injection. Fig.2.6 (b) shows the band structure of PHINES cell during program operation. Figure 2.7 shows the program characteristics of the two bits. In Fig.2.7 (a), bit-1 is programmed to a low Vt, while bit-2 is in the erased state. Bit-2 is subsequently programmed in Fig.2.7 (b). Since the program is performed by bit-by-bit and shot-by-shot tracking, a verification step is applied after each program shot to well control the program behavior of each bit. The program of each bit stops as its Vt or current passes the program verification. Over-program induced leakage current in the low Vt state between two columns can be suppressed, and a narrow Vt distribution of the program cells can be achieved. Read of PHINES cell is performed by a

backward-read scheme as shown in Table 2.2. To read bit-1 (bit-2), a source (drain) bias is applied to reduce the channel potential near bit-2 (bit-1). The IV characteristics of each state are shown in Fig.2.8.

2.3.2 The Charge Distribution

In Fig.2.9, the charge pumping technique [2.15] is utilized to monitor the charge variation in the nitride. The open circles and solid circles represent the initial and erased conditions. The Vt shift after erase is around 2.5V. The solid up-triangles and down-triangles represent the charge distribution in nitride after 1μs and 200μs programming. After FN electron erasing and hot-hole programming, a tail of charge pumping current (Icp) is observed. The turn-on Vt (Vgh) of the Icp tail is proportional to the number of storage holes in a programmed bit while the amount of the Icp tail is proportional to the length of the programmed holes in the channel region. As program time increases, the increase of Icp in the portion of $1V<Vgh<3.5V$ represents that hot holes are injected into the nitride from junction edge toward channel wherein a bit is programmed.

2.3.3 2-bit Interaction Effect

Two-bit interaction effect is a unique phenomenon in physical 2-bit storage memory cell, which is caused by the interaction between bit-1 and bit-2 during backward read operation. Similar to NROM cell [2.16], PHINES cell suffers 2-bit interaction effect and operation Vt window reduction due to the channel current sensing and the backward read scheme. Fig.2.10 (a) shows the program characteristics. In the initial state (condition A), two bits are in high Vt states. Figure 2.10 (b) and (c) illustrate the channel potential of condition A during read operation. As bit-1 is intentionally programmed to a low Vt state, a slight Vt decrease is observed in bit-2 (condition B in Fig.2.10 (a)), which induces Vt window reduction. Fig.2.10 (d) and (e) illustrate the channel potential of condition B (bit-1 is in a low Vt state while bit-2 is in a high Vt state). In condition B, as bit-1 is read (see Fig.2.10 (d)), a high read Vd is used to pull down the channel potential near bit-2, and a low Vt of bit-1 is thus sensed. To read bit-2 (see Fig.2.10 (e)), the high read Vd and the local/narrow electron distribution of bit-2 after bit-1 programming will enhance the Drain-Induced-Barrier-Lowering (DIBL) effect and lower the channel potential. Compared to the condition A (Fig.2.10 (c)), a lower Vt of bit-2 is obtained, and a reduced Vt operation window is caused. Since the Vt of bit-2 is very sensitive to the programmed condition of bit-1, we name this phenomenon ì2-bit interaction effectî.

Device simulation is used to characterize the effects of cell parameters on the Vt operation window. The definitions of the simulated cell parameters are descried in

Fig.2.11. As shown in Fig.2.12 and Fig.2.13, three parameters will dominate the Vt window of a PHINES cell: read Vd, the length of the residual electron distribution, and the density of the stored electrons. In Fig.2.12, as the length of the residual electron distribution decreases (the length of the programmed hole distribution increases), Vt window increases under a fixed read Vd and, in other words, read Vd can be reduced to maintain a constant Vt window. Besides, higher stored electron density can also increase Vt window without increasing the read bias as shown in Fig.2.13. A narrower electron distribution, a higher electron density, and a lower read Vd could suppress the DIBL effect enhanced Vt reduction and enlarge the Vt window.

Accordingly, 2-bit interaction effect can be suppressed by optimizing the charge profiles and the operation schemes. As mentioned in Section 2.3.1, PHINES can determine the stored electrons via erase operation and well control the injected amount of holes to modulate the length of residual electrons via program and program verification, separately. Although we can suppress Vt window reduction via better operation algorithms and carrier injection processes to manage the charge distribution, the 2-bit interaction effect cannot be eliminated completely in the backward read scheme. Besides, 2-bit interaction effect will get worse in the next generation due to the enhanced DIBL in a scaled device. In chapter 3, a novel BTB-PHINES memory cell and BTB-sensing (band-to-band sensing) scheme are developed to solve this issue completely.

2.3.4 PHINES Cell Endurance and Vt Operation Window

Figure 2.14 and Fig. 2.15 show the P/E cycling endurance of 1-bit-per-cell and 2-bits-per-cell operation, respectively. The Vt window is almost unchanged up to 10K P/E cycles. A slight window closure is observed after 100K cycles. This phenomenon is widely observed in flash memory cells, which should result from the stress-induced bottom/top oxide degradation [2.17]. The Vt operation window of 1-bit-per-cell and 2-bit-per-cell operation is around 2V and 1.2V, respectively.

2.3.4 PHINES Cell Performance

The electrical performance of a PHINES cell is summarized in Table 2.3. Program can be finished within 200μs and erase can be done in 2ms. Vt-windows of 2V and 1.2V are obtained for 1-bit-per-cell and 2-bits-per-cell operation. Since the program current is less than 50nA/bit, high programming rate can be achieved by parallel programming. Besides, FN-erase also consumes extremely low current (10fA/cell). Both program and erase are low power operations, which makes it suitable for mass storage (data flash) applications.

2.4 PHINES Cell Reliability

2.4.1 Data Retention

Fig.2.16 shows the data retention characteristics of three program/erase states. Vt loss is less than 0.5V and 0.2V for high-Vt bits and low-Vt bits, respectively, after 150C, 168 hours bake in 10K P/E cycled cells. Fig.2.17 shows the temperature effect on data retention in a high Vt state. Three storage temperatures are compared: 25C, 85C, and 150C. Excellent data retention is observed. In previous studies [2.18], hot electron injection tends to fill traps with shallower energy in a stressed oxide film. We also use this characterization method to monitor the characteristics of electrons in the nitride traps. High Vt state charge loss behavior of two electron injection techniques (FN injection and substrate hot electron injection) is compared in Fig.2.18. Two devices are stressed by constant voltage stress (Vg=-24V, Vd=Vs=Vb=0V) for 1000s. After stress, hot-hole injection is performed to lower the Vt of the devices. Finally, FN injection and substrate hot electron (SHE) injection are used to inject electrons into two devices to raise Vt to 5V, respectively. Vt shift is measured in the high temperature condition (150C). As shown in Fig.2.18, the device with FN electron injection shows less charge loss than the device with SHE injection. It is surmised that hot electrons in SHE will jump over the oxide barrier and are randomly captured by deep and shallow traps of nitride as shown in Fig.2.19 (a). Electrons in shallower traps will easily escape during a storage period and charge loss is observed as shown in Fig.2.19 (b). However, tunnel electrons by FN injection tend to stay in deep traps of nitride since electrons in shallow traps will be drawn out by high electric field as shown in Fig.2.20 (a). According to the Frenkel-Poole model, electrons in deeper traps have longer emission time and good data retention is obtained accordingly as shown in Fig.2.20 (b).

2.4.2 Read Disturbance

Read disturbance is another reliability issue of flash memory devices. As the device is in a low Vt state, continuously reading the device will induce disturbance due to the high channel current and hot electron injection. Vt will increase and the read current will degrade accordingly. We also evaluate the read disturbance characteristics of a PHINES cell. As shown in Fig.2.21, the read condition (Vg=3V, Vd=1.6V, and Vs=0V to read Bit-2) is applied to the device while two bits are both at low Vt states (Vt is around 2V). The Vt shifts of both bits are measured. Vt drift of 0.2V is observed in Bit-1 by continuous read of 10000s while there is almost no disturbance in Bit-2. The reason is that a high voltage is applied on the drain, which induces hot electron injection at the drain side. Accordingly, the Vt of Bit-1 increases

due to hot electron injection and no Vt shift is observed in Bit-2. Likewise, continuously reading Bit-1 (Vg=3, Vd=0, and Vs=1.6V) will cause hot electron injection at the source side, which will cause read disturbance in Bit-2.

Read disturbance is a potential scaling issue due to enhanced hot carrier effect in a scaled device [2.19]. Higher substrate doping concentration, shorter channel length and cycling induced damages will degrade read disturbance and the only solution is to reduce read Vd. In section 2.3.3, the effects of read Vd, length of residual electron distribution and density of stored electrons have been discussed. As shown in Fig.2.12, read Vd can be reduced without degrading the Vt window by optimizing the length of the residual electron distribution. PHINES can determine the stored electrons via erase verify step and well control the injected amount of holes to modulate the length of residual electrons via program verify step, separately. Accordingly, by managing electron profile, hole profile and stored electron density, a large Vt window and reduced read disturbance (by lowering read Vd) can be realized in future scaled devices.

2.5 PHINES Array Architecture

2.5.1 PHINES Operation in Virtual Ground Array (NOR-type) Architecture

PHINES cells can be arranged in the virtual ground array (NOR-type) as shown in Fig.2.22. In NOR-type array architecture, the cells are connected in parallel. Fig. 2.22 (a), (b) and (c) show the array erase, program and read operations, respectively. In array erase operation, a negative bias (-9V) and a positive bias (10V) are applied on the selected WLs and P-well, respectively. Electron injection via Fowler-Nordheim tunneling from the gate is used to erase the selected cells to high Vt states. In order to program PHINES cells in a high-density virtual ground array, a technique to inhibit the program disturbance in the adjacent cell is necessary. As shown in Fig.2.22 (b), to program the bit-1 in cell-A, a positive bias (5V), a grounded bias, and a negative bias (-7V) is applied on the BL2, BL1, and the selected WL, respectively. The program disturbance of the adjacent cell-B sharing the same bit-line (BL) and word-line (WL) is inhibited by properly biasing the unselected BL3 (ex: 3V). The programming behavior of cell-A and disturbance behavior of cell-B and cell-C are shown in Fig.2.23. The channel potential of cell-A and cell-B are plotted in Fig.2.24. Dramatic reduction of hot-hole injection by an inhibitive BL bias is due to a less lateral electric field [2.20]. Likewise, in cell-C sharing the same BL, but a different WL, grounding the unselected WL reduces the program disturbance because of the less vertical field. Fig.2.22 (c) shows the operation condition of the backward read scheme in array operation. To read the bit-1 in cell-A, a positive bias (3V) is applied on the selected

WL. Another positive bias (1.6) is applied on BL1 with grounded BL2. The channel current of the selected cell is sensed to determine the storage state of bit-1. To program and read the storage state of bit-2, similar operations can be applied by interchanging the role of BL1 and BL2.

2.5.2 PHINES Operation in NAND-type Array Architecture

PHINES cells can be also arranged in NAND-type array. In NAND-type array architecture, one NAND string contains 32 memory cells and 2 select-transistors (SLG1 and SLG2) that are arranged in series as shown in Fig.2.25 [2.21]. Fig.2.25 (a), (b) and (c) show the array erase, program, and read operations, respectively. In array erase operation as shown in Fig.2.25 (a), a negative bias (-9V) and a positive bias (10V) are applied on the selected WLs and P-well, respectively. Electron injection via Fowler-Nordheim tunneling from the gate is used to erase the selected cells to high Vt states. Fig.2.25 (b) shows the array program operation. To program bit-1 of the selected WL (WL3), a positive bias (5V), a grounded bias, and a negative bias (-7V) are applied on the drain, source, and the selected WL, respectively. The non-selected WLs are turned on (10V), which serves as pass transistors to pass the drain and source voltages. To read bit-1 of the selected WL (WL4) as shown in Fig.2.25 (c), a positive bias (1.6V), a grounded bias, and another positive bias (3V) are applied on the source, drain, and the selected WL, respectively. The non-selected WLs also serve as pass transistors to pass the read current, and the storage state of bit-1 is determined accordingly. To program and read the storage state of bit-2, similar operations can be applied by interchanging the role of the source and the drain.

2.6 Conclusion

A novel flash memory cell named PHINES (Programming by hot Hole Injection Nitride Electron Storage) is investigated. PHINES uses a nitride trapping storage cell structure. Channel FN erasing is performed to raise Vt while programming is done by lowering local Vt through band-to-band hot-hole injection. PHINES cell uses backward read scheme with low power program/erase operation, and physically 2-bits storage is achieved. The 2-bit interaction effect and the effects of charge profile on Vt operation window are also studied and characterized. PHINES cell also shows good retention, and cell reliability can be arranged in both NOR-type and NAND-type array architectures for code flash and data flash applications. PHINES can be a promising candidate for future flash EEPROM technology.

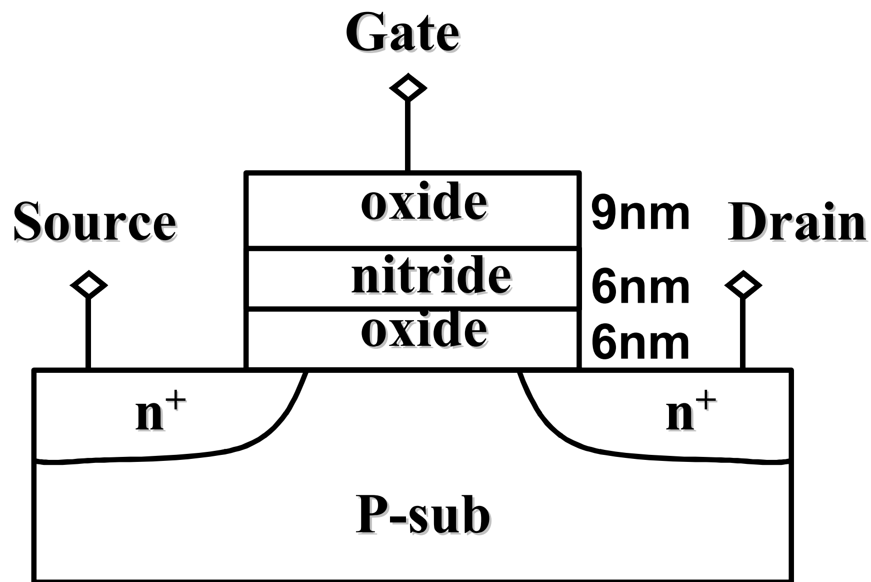


Fig.2.1 Schematic representation of the PHINES cell structure.

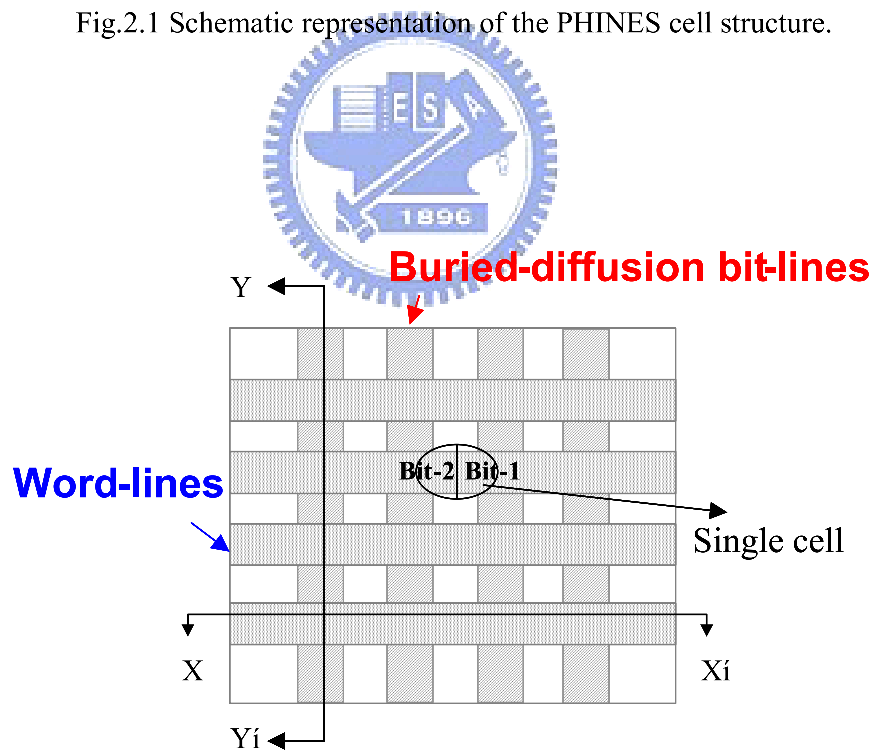


Fig.2.2 The array architecture of the test single cell.

Table 2.1 Key PHINES cell parameters.

Design rule	0.13μm
Gate Length	0.19μm
WL Width	0.14μm
BL Width	0.14μm
Unit Cell Area	0.092μm²
Unit Bit Area	0.046μm²
Bottom Oxide	6nm
Nitride	6nm
Top Oxide	9nm

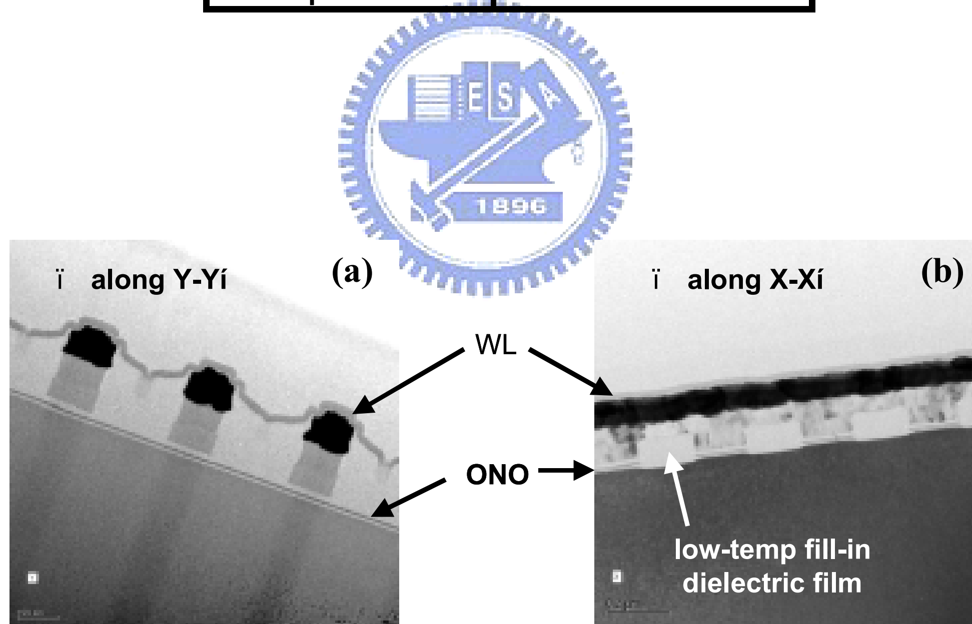


Fig.2.3 TEM pictures of a PHINES cell along (a) Y-Yí and (b) X-Xí (refer to Fig.2.2).

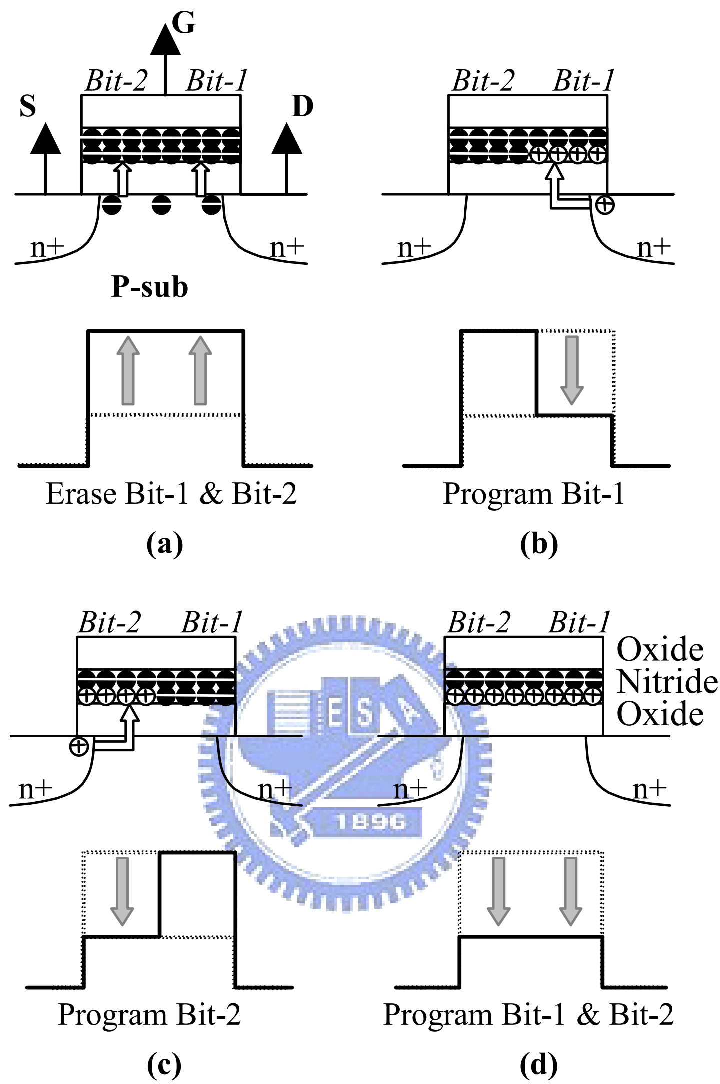


Fig.2.4 Schematic representation of the storage charges in a PHINES cell (top) and the channel surface potential (bottom) with two-bits storage. (a) Bit-1 and Bit-2 in erased states. (b) Bit-1 in a programmed state and Bit-2 in an erased state. (c) Bit-1 in an erased state and Bit-2 in a programmed state. (d) Bit-1 and Bit-2 in programmed states.

Table 2.2 Physical mechanisms and bias conditions of PHINES operation. Please refer to Fig.2.1 for the corresponding terminals and Bit-1 and Bit-2 in a PHINES cell.

		Program (BTBT HH)	Erase (-Vg FN)	Read (Backward)
Bit-1	Vg	-7V	-9V	3V
	Vd	5V	F	0V
	Vs	0V	F	1.6V
	Vb	0V	10V	0V
Bit-2	Vg	-7V	-9V	3V
	Vd	0V	F	1.6V
	Vs	5V	F	0V
	Vb	0V	10V	0V

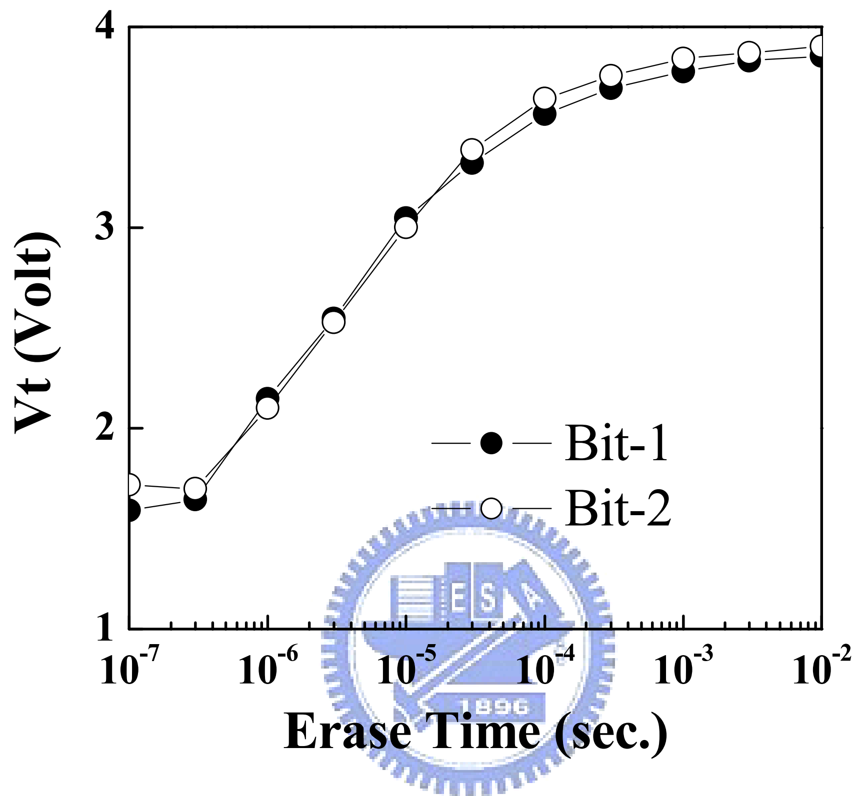


Fig.2.5 Negative FN erase characteristics of a PHINES cell. Threshold voltage (Vt) is defined as the applied gate voltage at which the drain current is 1μA.

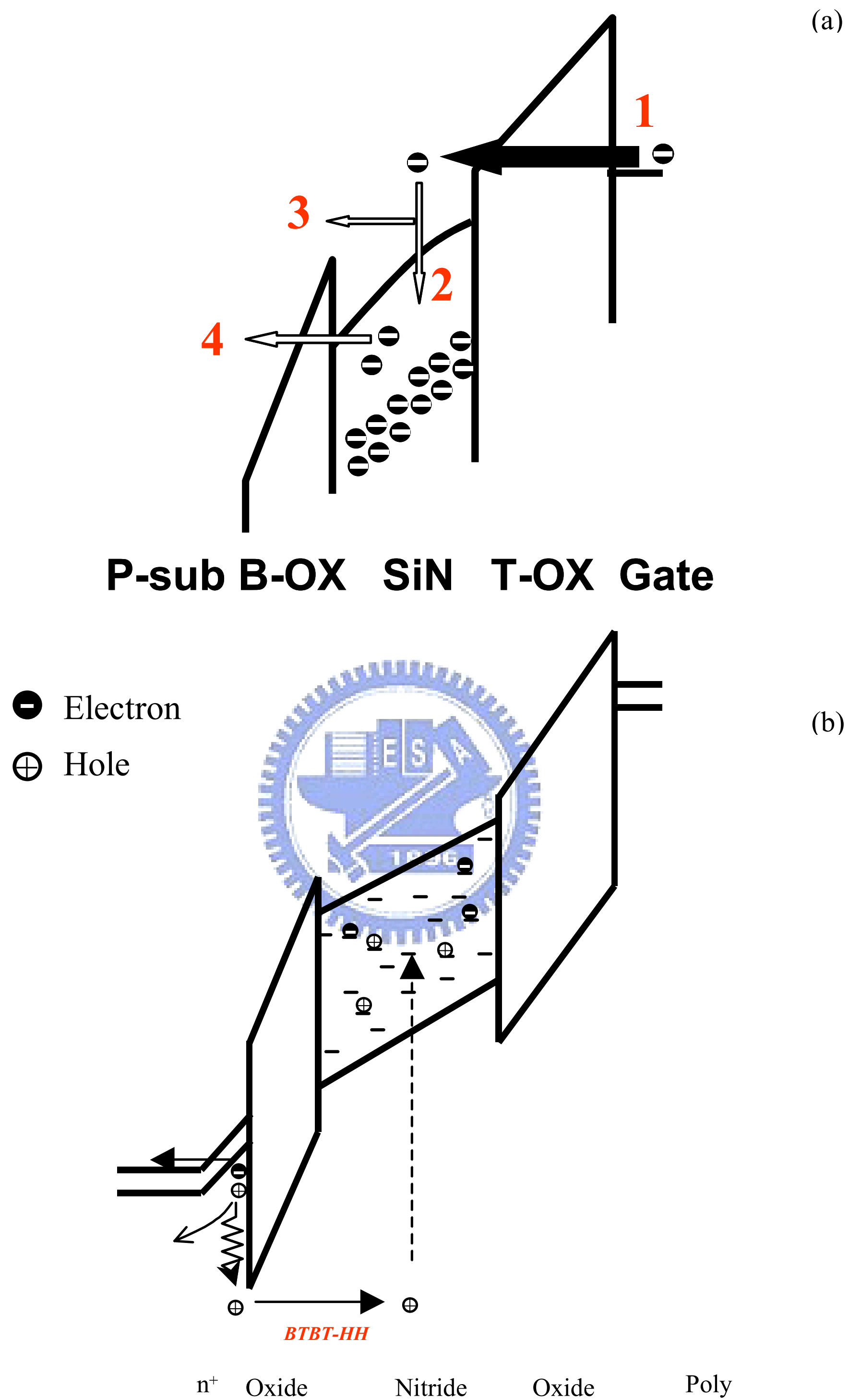


Fig.2.6 Schematic representation of the band structure and the electrical field during (a) negative FN injection and (b) BTBT HH injection in PHINES erase and program operation, respectively.

Bit-1 Program Bit-2 Program

Fig.2.7 Programming characteristics of a PHINES cell. (a) Bit-1 is programmed to a low Vt while bit-2 is maintained at a high Vt. (b) Bit-2 is programmed to a low Vt while bit-1 is maintained at a low Vt.

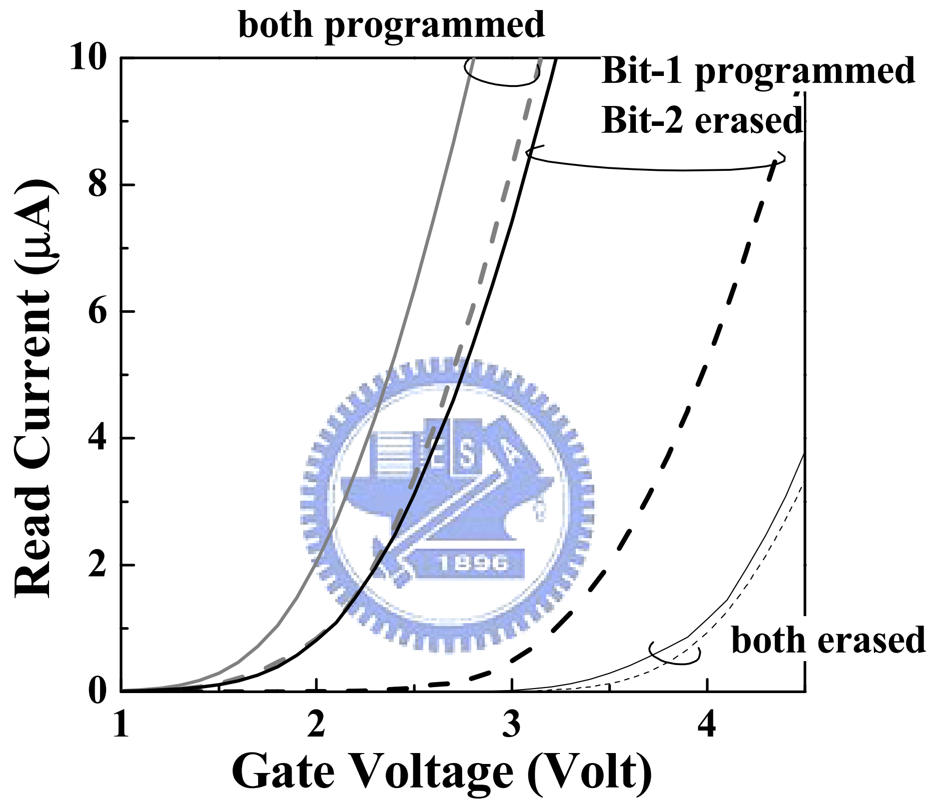


Fig.2.8 IV characteristics of 3 cell states (both bits are erased, one bit is programmed and the other bit is erased, both bits are programmed). Solid line represents the IV of Bit-1 and dash line represents the IV of Bit-2. The cells are fresh cells.

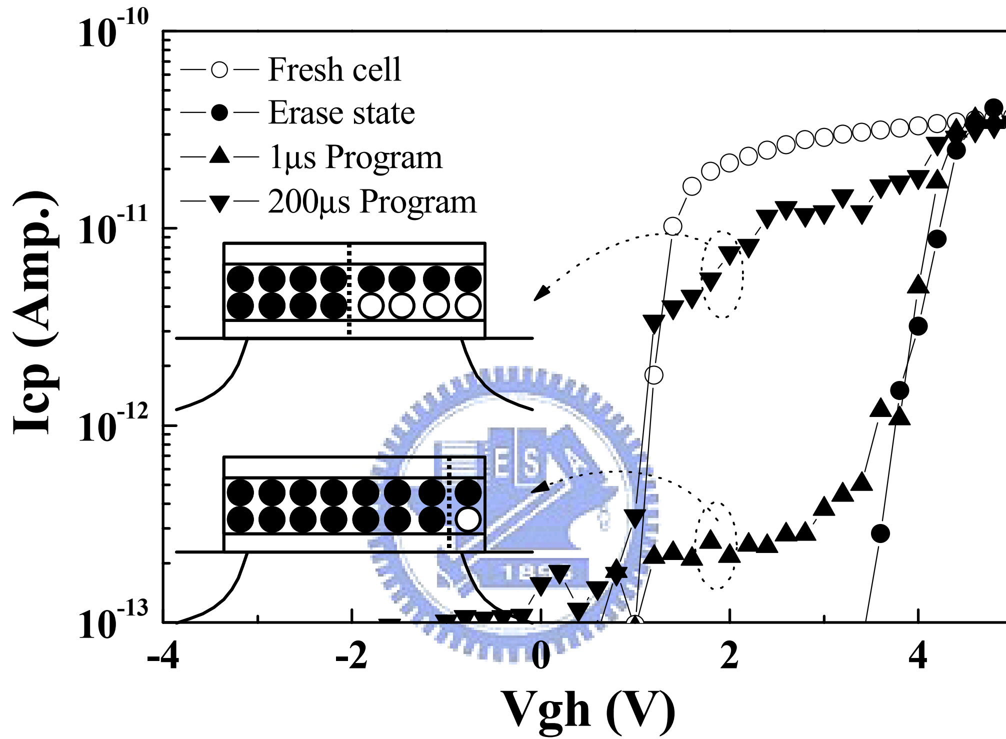


Fig.2.9 The measured charge pumping current (Icp) versus the high-level gate pulse (Vgh). The low level gate pulse is ñ4V. The open circles and solid circles represent the initial and erased state conditions, respectively. The solid up-triangles and down-triangles represent the charge distribution in nitride after 1μs and 200μs programming, respectively.

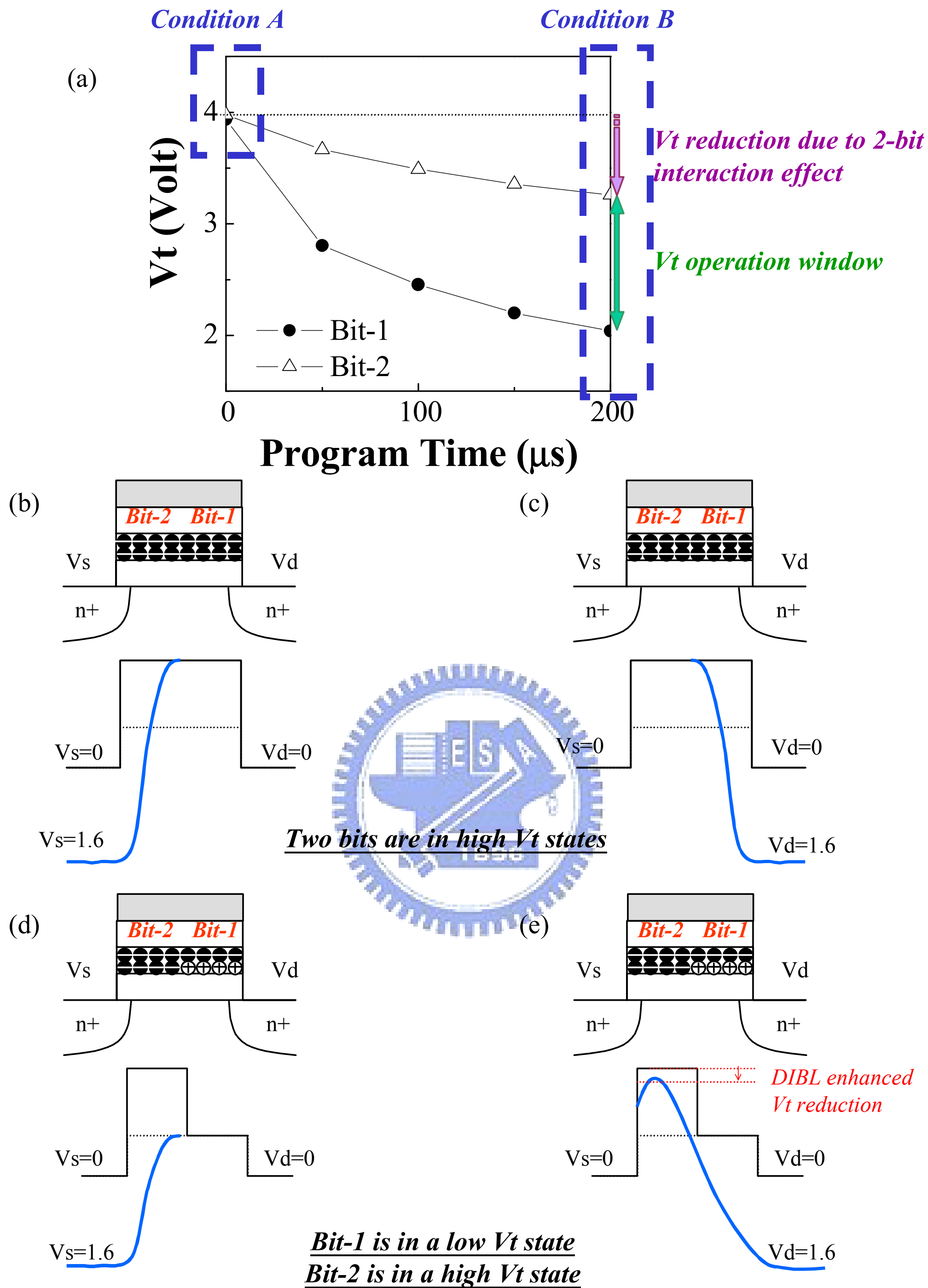


Fig.2.10 (a) The program characteristics of a PHINES cell. Condition A shows that two bits are both in high Vt states. Condition B shows that bit-1 is in a low Vt state and bit-2 is in a high Vt state. (b) Illustration of the channel potential in bit-1 read (condition A). (c) Illustration of the channel potential in bit-2 read (condition A). (d) Illustration of the channel potential in bit-1 read (condition B). (e) Illustration of the channel potential in bit-2 read (condition B).

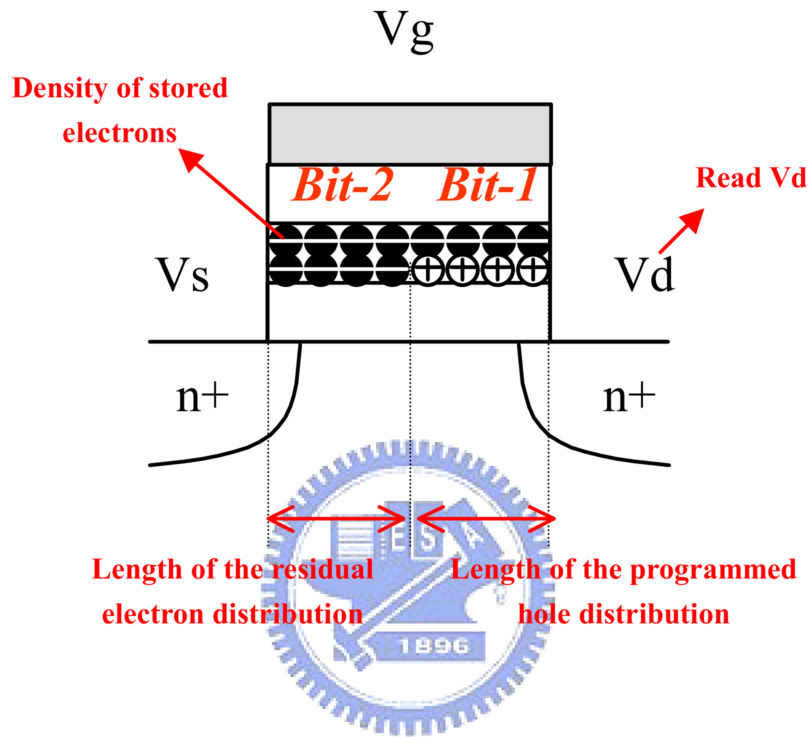


Fig.2.11 Definitions and descriptions of the simulated cell parameters.

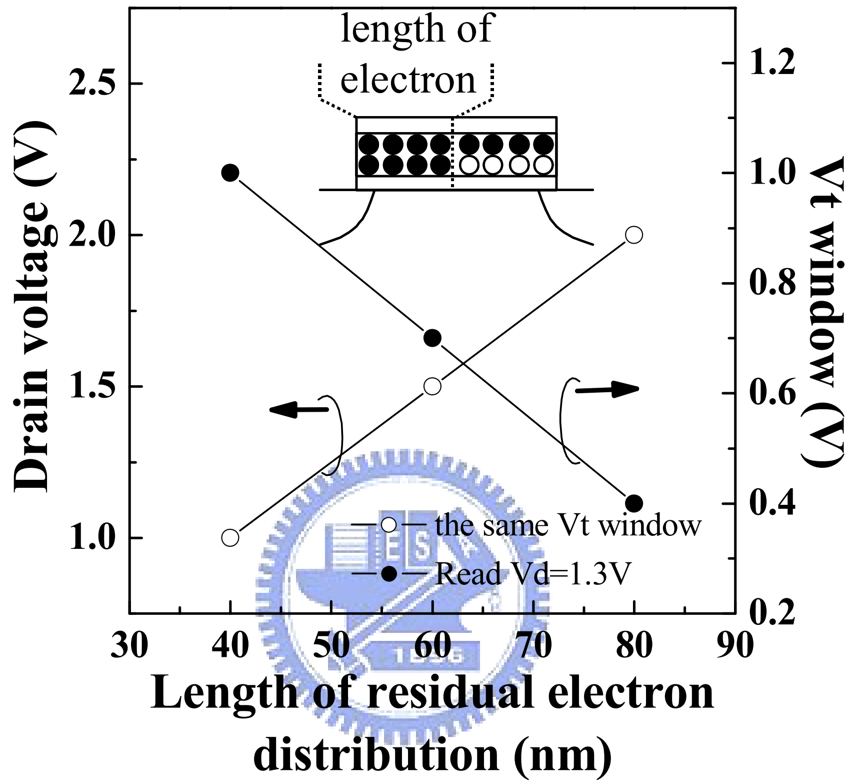


Fig.2.12 Simulated length of the residual electron distribution versus read Vd and Vt window with a programmed hole distribution of 60nm. Open symbols represent the minimum required Vd for the 0.8V Vt window and solid symbols represent the window with a read drain bias of 1.3V.

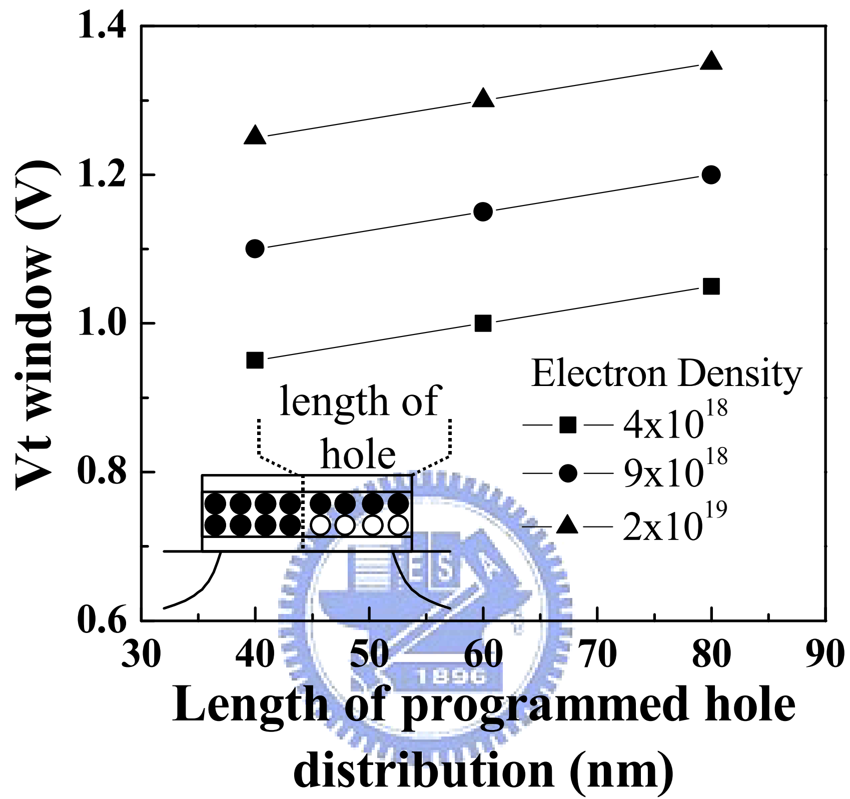


Fig.2.13 Simulated Vt windows versus the length of the programmed hole distribution with various electron densities and a residual electron distribution of 40nm.

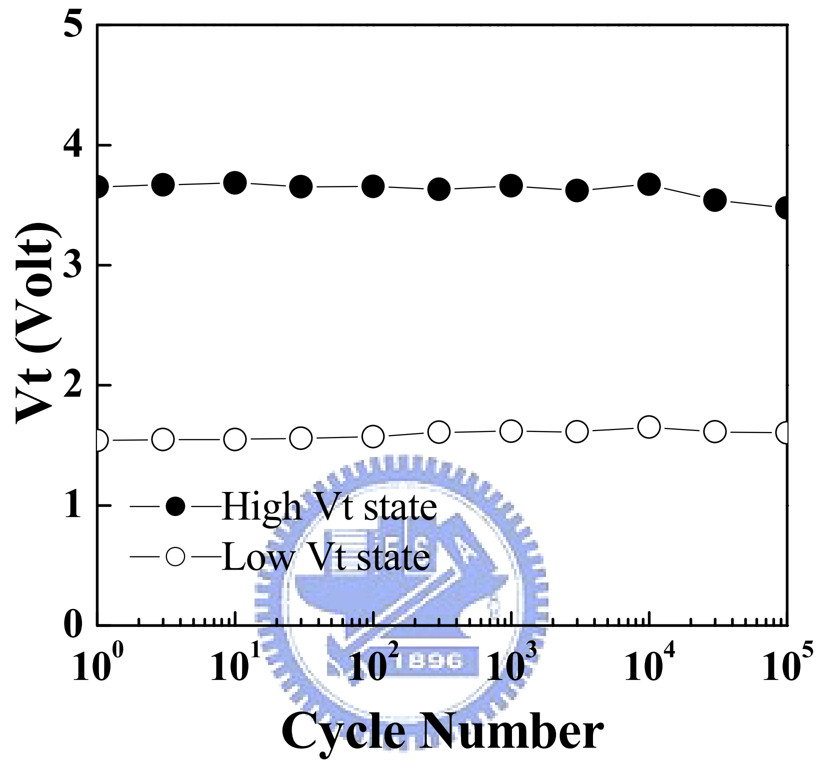


Fig.2.14 Endurance behavior of 1-bit-per-cell operation.

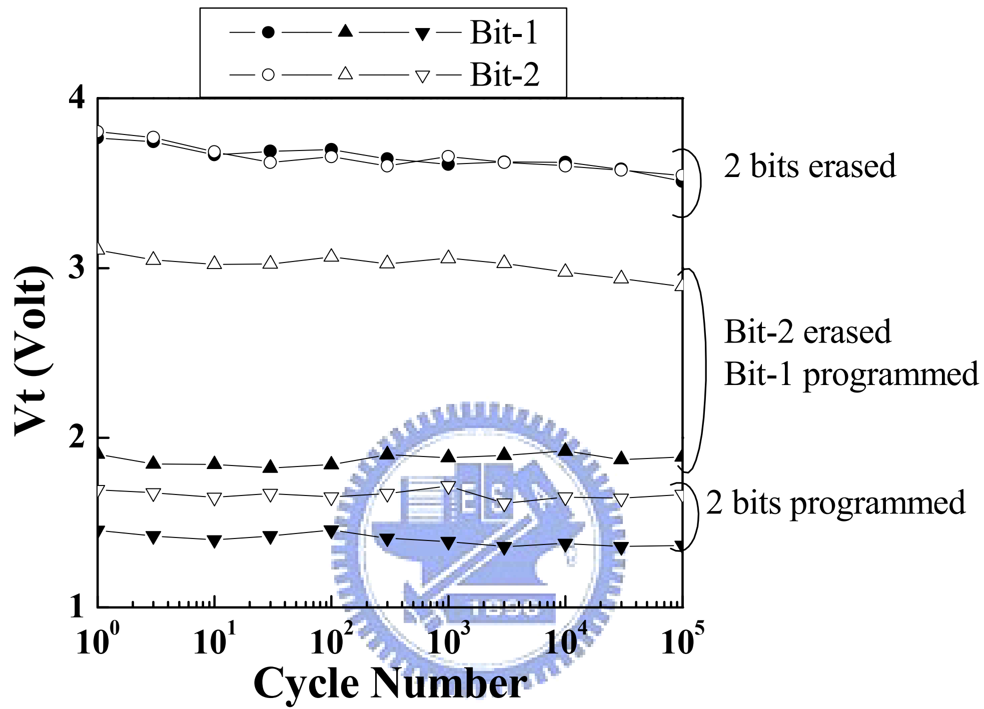


Fig.2.15 Endurance behavior of 2-bits-per-cell operation. The cycle is repeated by erase => bit-1 program => bit-2 program. Circles represent that both bits are in high Vt states. Up-triangles represent that bit-1 is in a low Vt state and bit-2 is in a high Vt state. Down-triangles represent that both bits are in low Vt states.

Table 2.3 The electrical performance of a PHINES cell. The Vt window in the table denotes the initial operation window, which does not include the charge loss, read disturbance, and other reliability margins.

Program Current	$< 5\text{x}10^{-8}$ A/bit
Erase Current	$<10^{-14}$ A/bit
Program Time	200μs/page
Erase Time	2 ms/sector
Vt Window - 1 Bit	2 Volts
Vt Window - 2 Bit	1.2 Volts

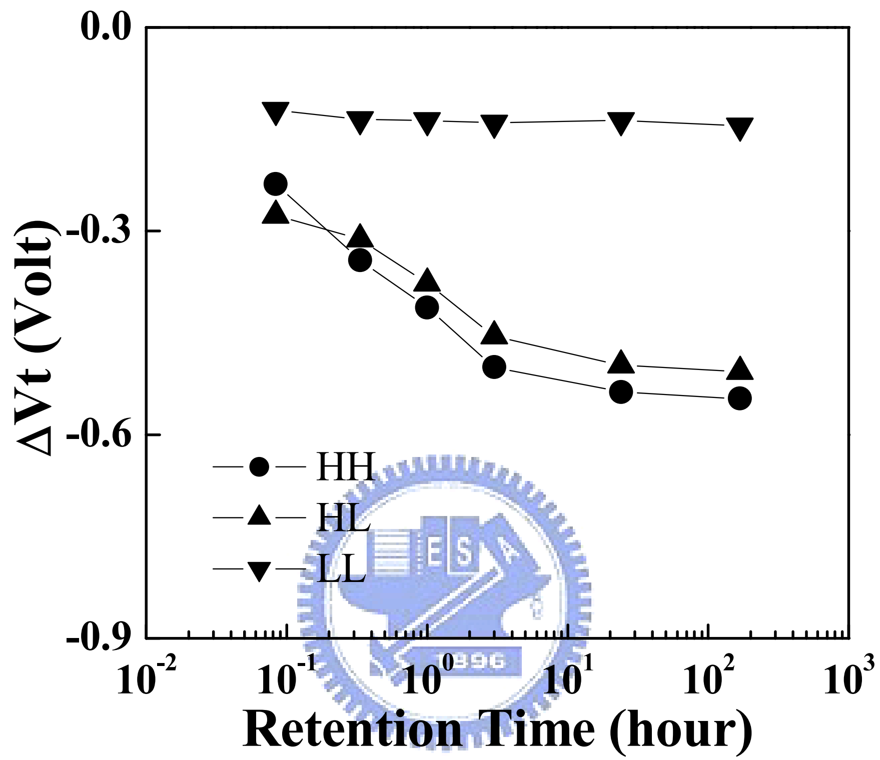


Fig.2.16 Data retention (Vt loss) of three program/erase states. The storage temperature is 150C. The cells are 10K P/E cycled.

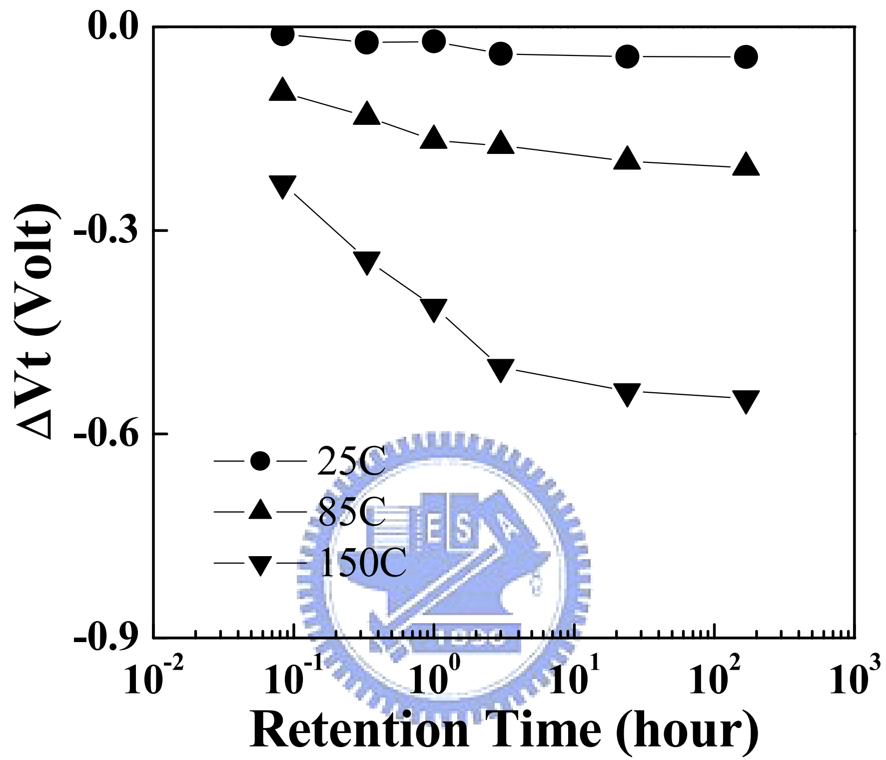


Fig.2.17 The temperature effect on data retention in high Vt states. The cells are 10K P/E cycled.

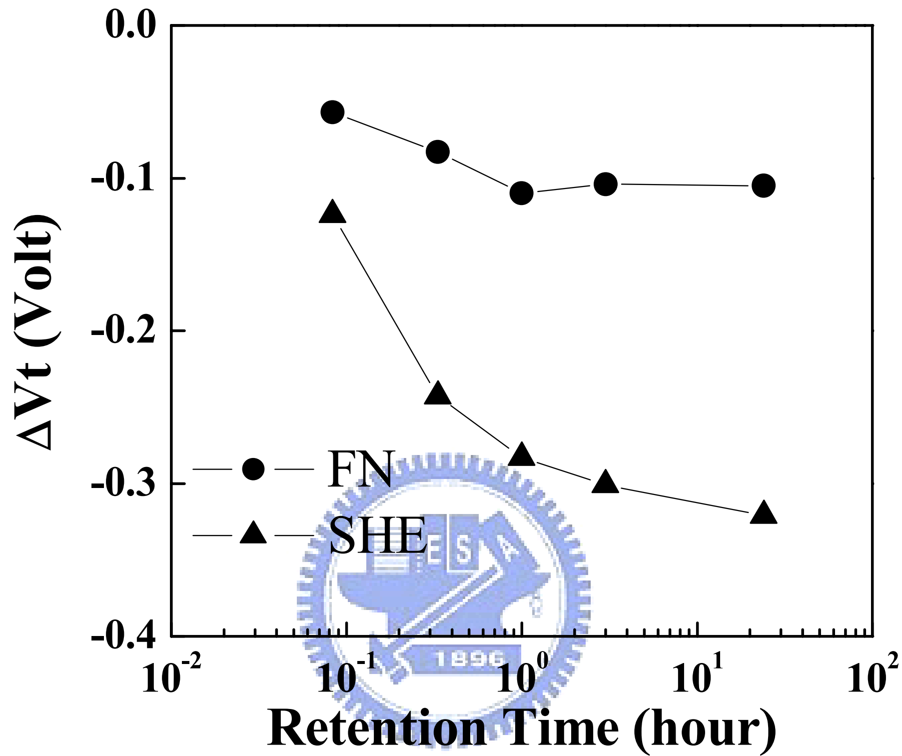
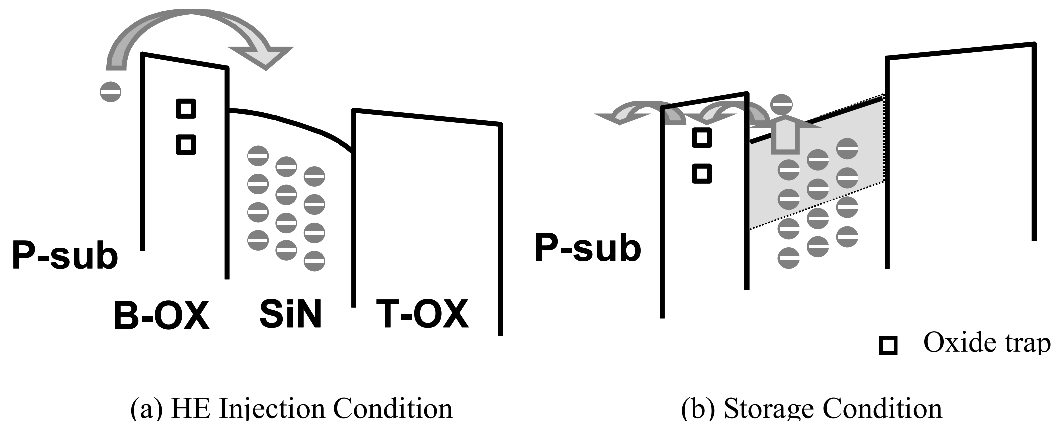
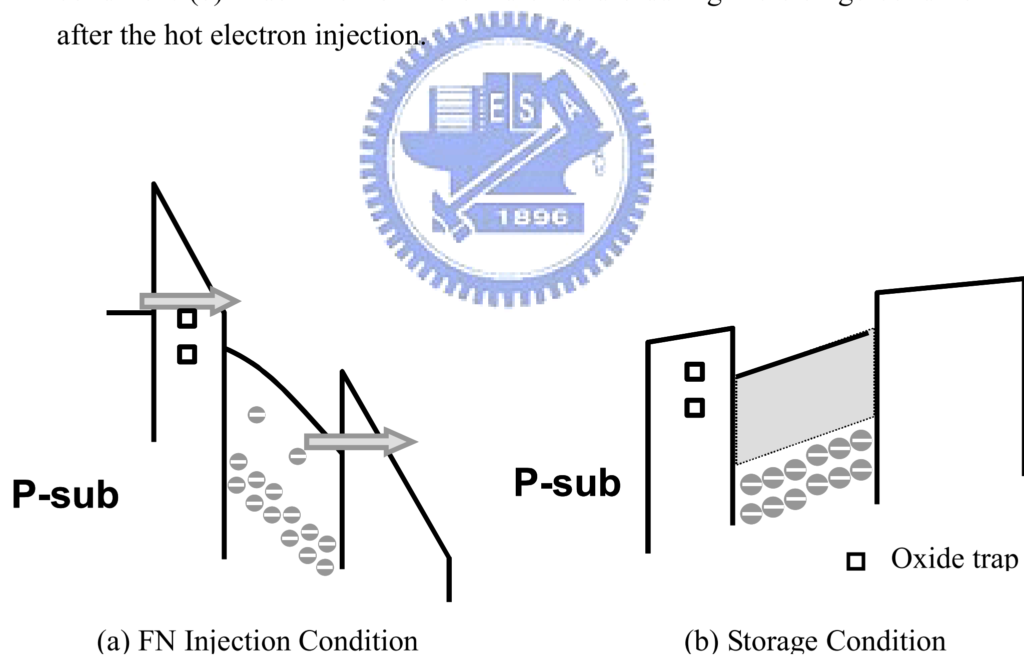


Fig.2.18 Effects of electron injection methods on the charge loss at the storage temperature of 150C. After stress of Vg=-24V for 1000s, two devices are conditioned to high Vt states (Vt=5V) by two electron injection methods and Vt shift is measured. Two electron injection methods are FN (Vg=-8V, Vb=10V) injection and SHE injection (Vg=2V, Vs=Vd=0V, V_{PWELL}=-6V, V_{NWELL}=-7V).



(a) HE Injection Condition (b) Storage Condition

Fig.2.19 (a) Illustration of the band structure in the hot electron injection condition. (b) Illustration of the band structure during the storage condition after the hot electron injection.



(a) FN Injection Condition (b) Storage Condition

Fig.2.20 (a) Illustration of the band structure in Fowler-Nordheim injection condition. (b) Illustration of the band structure during the storage condition after Fowler-Nordheim injection.

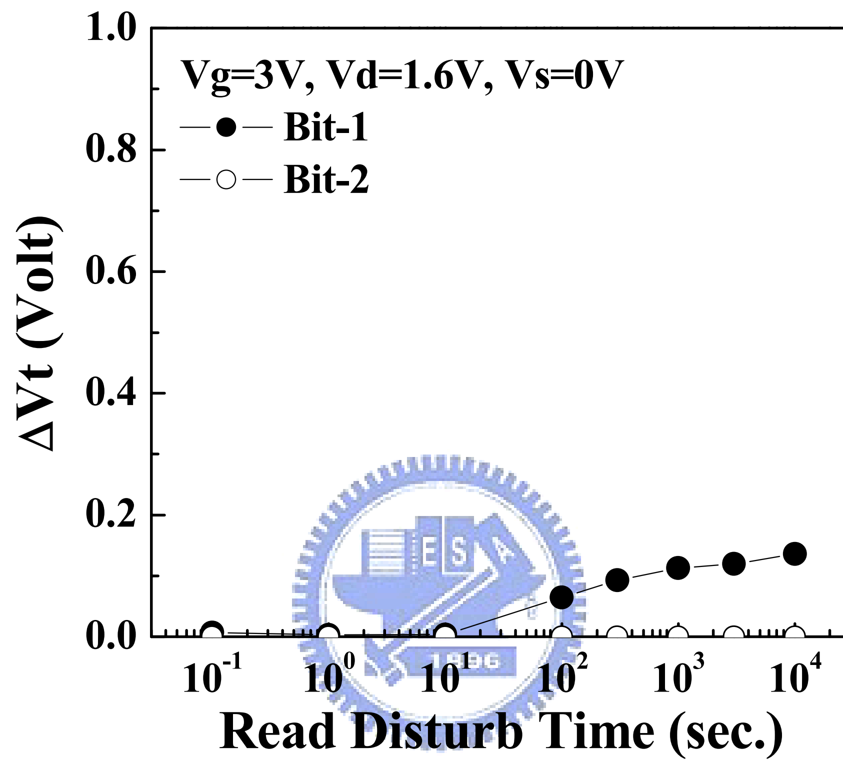


Fig.2.21 Read disturbance characteristics of a PHINES cell.

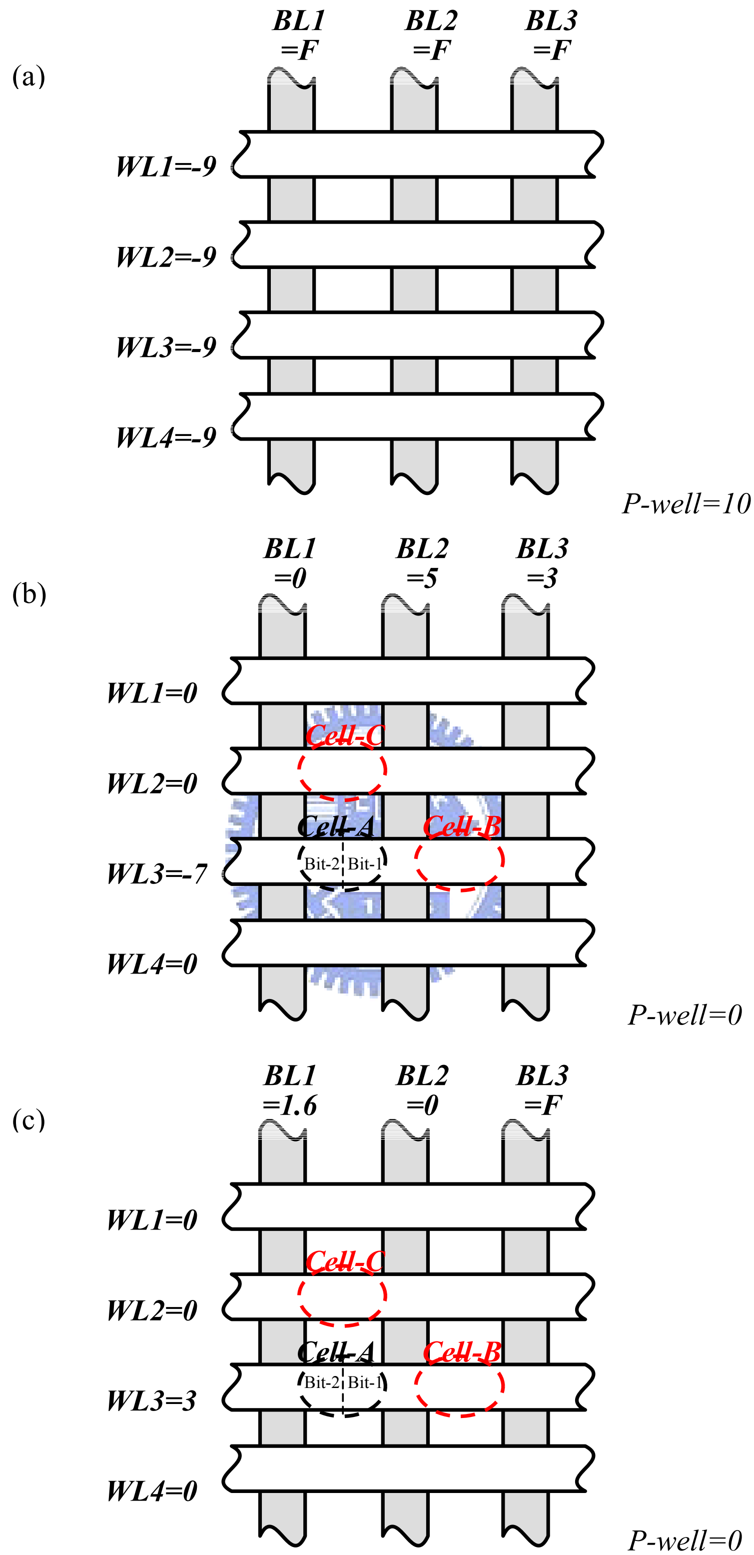


Fig.2.22 PHINES (a) erase, (b) program, and (c) read operations in a virtual ground (NOR-type) array architecture.

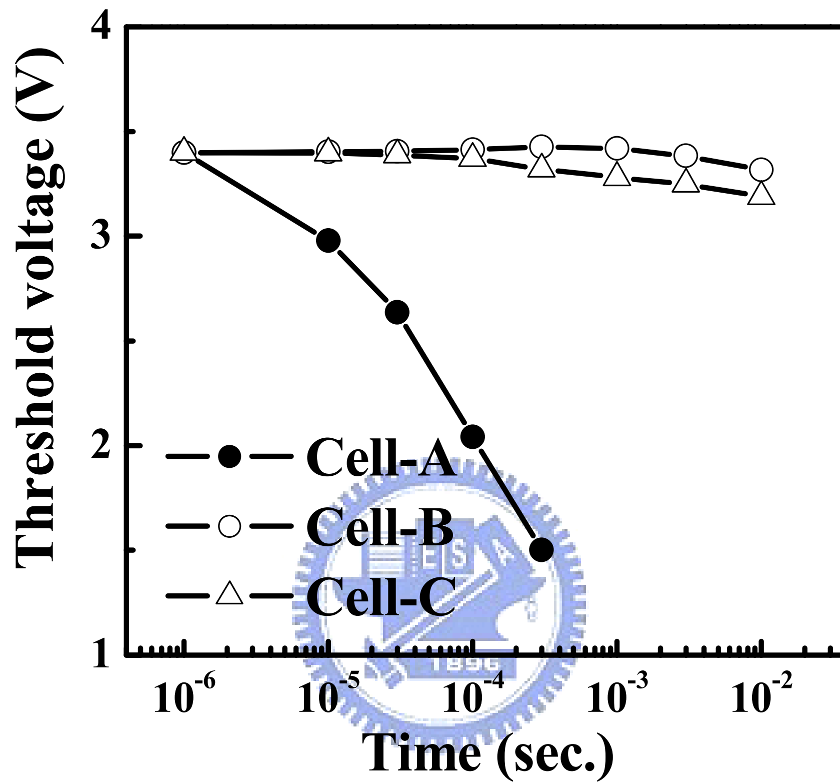


Fig.2.23 The program behavior of cell-A and the disturbance behavior of cell-B and cell-C.

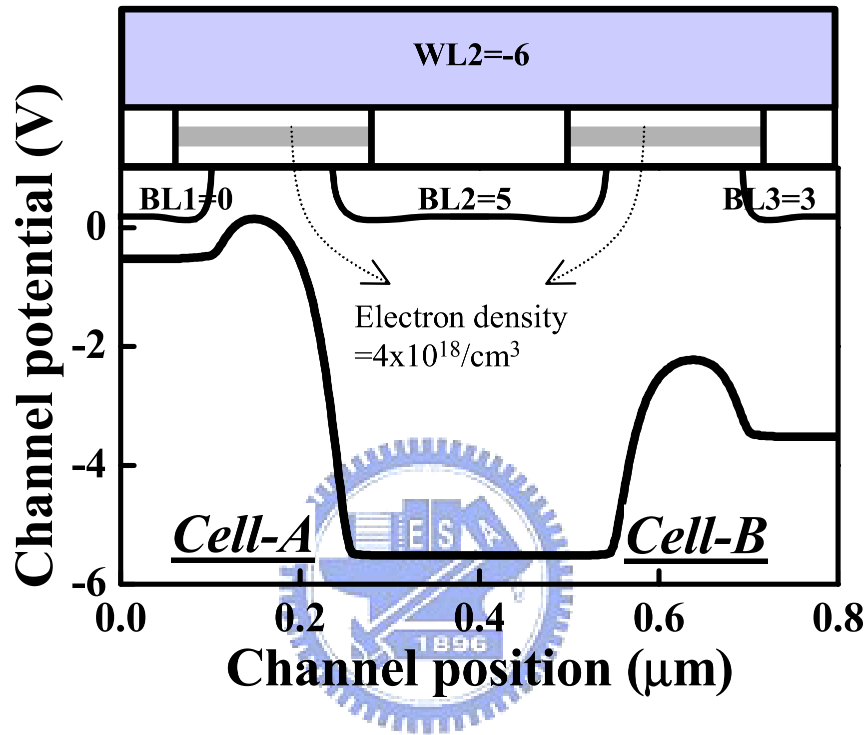


Fig.2.24 The simulated channel potential of cell-A and cell-B.

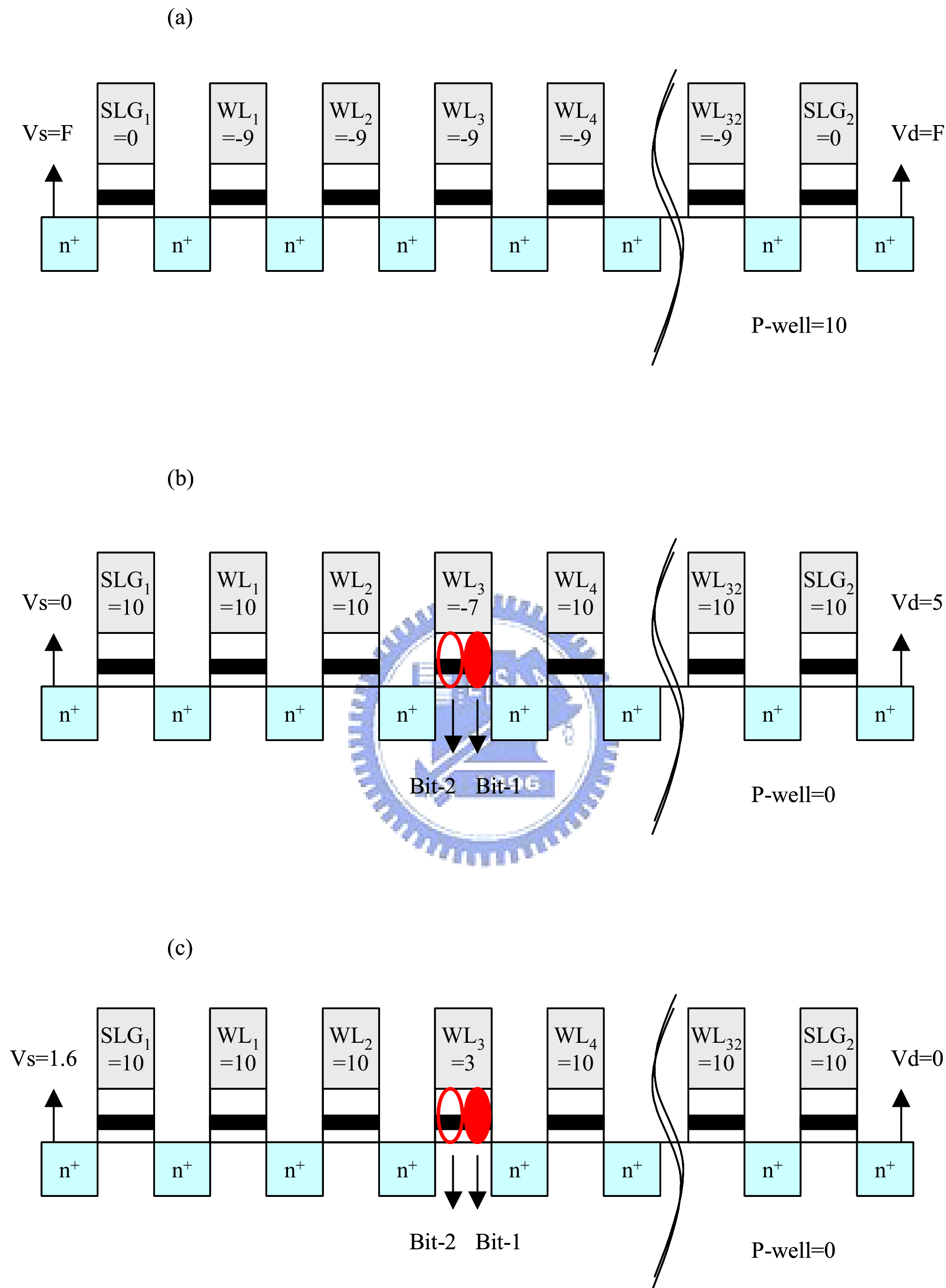


Fig.2.25 PHINES (a) erase, (b) program, and (c) read operations in a NAND-type array architecture.

Chapter 3

A novel BTB-PHINES Flash Memory Cell with BTB Sensing Scheme and modified NAND-type Architecture

3.1 Introduction

Recently, the market of NAND-type flash memory [3.1-3.4] has been growing rapidly due to the applications of digital still cameras, personal digital assistants, and portable videos/audios. However, conventional NAND-type floating gate memory meets a scaling limitation of floating gate capacitance interference [3.2, 3.3], and the scaling limitation is at around 30nm CMOS generation [3.3]. SONOS-type nitride trapping storage flash memory cell (FN tunnel program by electrons and direct tunnel erase by holes) arranged in NAND array [3.3, 3.4] is proposed to overcome the issue of floating gate coupling. Besides, SONOS cell reduces the stack height due to the absence of floating gate and inter-poly dielectric, and provides nearly planar cell array. However, conventional SONOS cell can only perform 1-bit-per-cell storage, and the bad cell retention, the slow program speeds, and the slow erase speeds are still issues until now [3.4].

As mentioned in chapter 2, we propose a PHINES nitride storage flash memory cell [3.5] with physically 2-bits-per-cell storage, good reliability, simple process, and low power operation for mass storage applications. PHINES can be operated in both NOR-type and NAND-type array. Although NAND-type PHINES memory architecture can target the growing data flash market, it suffers 2-bit interaction effect and operation window reduction due to the backward read scheme. In this chapter, we construct a novel BTB-PHINES memory architecture based on conventional PHINES program and erase operation. Better cell retention, no 2-bit interaction, large operation window, and a high programming throughput (>10MB/s) can be realized. The main features of BTB-PHINES memory cell are: (1) BTB current sensing scheme, and (2) a modified NAND-type array architecture.

3.2 PHINES Operation with BTB Sensing Scheme

3.2.1 BTB-PHINES Memory Operation

Fig.3.1 illustrates BTB-PHINES cell structure and the erase/program/read operations. BTB-PHINES utilizes an oxide/nitride/oxide trapping storage structure similar to the conventional PHINES introduced in chapter 2. In this chapter, the gate length/width of the test pattern is 0.14/0.14μm. The ONO thickness is 9, 6, and 6nm

from top to down. Fig.3.2 shows the characteristics of 2-bits erase that is done by FN electron injection from the gate (see Fig.1 (a)). Fig.3.3 shows the characteristics of 2-bits program that is done by local BTBT HH injection from the source (or drain) junction (see Fig.3.1 (b)). Read utilizes a novel technology of BTB current sensing scheme (see Fig.3.1 (c)). Program and read use the same mechanism and the band structures are compared in Fig.3.4. In the program operation as shown in Fig.3.4 (a), a higher junction bias (>4V) provides a higher lateral field and high energetic holes for hot-hole injection. In read operation as shown in Fig.3.4 (b), a lower junction bias (lower lateral field) and a higher gate bias are adopted to provide sufficient sensing current. A lower junction bias and lateral field will not accelerate the holes, and the BTB current is generated without hot-hole injection. BTB-PHINES cell also performs physically 2-bits-per-cell operation via hole/electron trapping storage above source and drain junctions.

3.2.2 Two-Bit Interaction Effect

In the conventional channel current sensing (backward read scheme), the storage states of two bits will affect the channel current as discussed in chapter 2. Two bits will interact to each other and operation window is degraded (see Fig.2.7 and Fig.2.10). To overcome this issue, we introduce a novel technology of BTB current sensing scheme. As shown in Fig.3.3 (a), the sensing current of bit-2 will not be affected by the programmed state of bit-1. Two bits will not affect each other in the BTB sensing scheme, since BTB current is generated locally between the source (or drain) junction, and P-well as shown in Fig.3.1 (c). By using BTB-sensing scheme, a large operation window is obtained and a high on/off current ratio is maintained as the channel length scales (see Fig.3.5). Although BTB-sensing scheme provides lower sensing current (~100nA/bit) than the channel current sensing scheme (>1uA/bit as shown in Fig.2.8), the sensing current and the cell performance can still be compatible to the NAND-type floating gate memory cell with MLC (multi-level cell) operation and data flash specifications [3.6].

3.3 Modified NAND-type Array Architecture with BTB-PHINES Memory Operation and BTB Sensing Scheme

Different to the channel current sensing scheme, BTB-sensing scheme cannot be performed in the virtual ground array. As shown in Fig.3.6, the bit-2 of cell-A and the bit-1 of cell-B will be selected and sensed at the same time if the sensing biases are applied on BL3 (2V) and WL2 (-10V). Therefore, BTB-sensing scheme in the virtual ground array will lose the capability of 2-bits-per-cell storage and the advantage of ultra-high storage density. To realize BTB-sensing scheme, BTB-PHINES memory

operation, and 2-bits-per-cell storage, we construct a novel modified NAND-type array as shown in Fig.3.7 (a). Fig.3.7 (b), (c), and (d) show the cross sectional schematics of the array erase, program, and read operation. In the modified NAND-type array, there are 32 cells arranged in series with 2 select-transistors (SLG1 and SLG2). The key feature of the modified NAND-type array is that the source of SLG1 and the drain of SLG2 are shorted to the same metal bit-line (BL). Sector erasing, page programming, and parallel sensing are introduced. To program/read Bit-1 of the selected word-line (WL), a negative bias is applied on the selected WL and a positive bias is applied on the selected BL. SLG1 and SLG2 are turned on and off, respectively. The WLs between SLG1 and the selected WL are applied with a pass voltage (10V) to serve as pass gates while the others are grounded. Accordingly, Bit-1 can be simultaneously read and programmed by BTB current sensing, and BTB-HH injection, respectively. Similarly, Bit-2 can be read/programmed by interchanging the role of SLG1 and SLG2.

3.4 Cell Performances and Reliability

3.4.1 Cell Performances

Fig.3.8 and Fig.3.9 compare the program speed and IV curves in various gate lengths (Lg). The gate Length shows no influence on the program speed and IV curves due to the local effects of HH injection and BTB current sensing, which means that BTB-PHINES memory can sustain larger process induced Lg variations. Besides, a high programming speed (<60μs) and a low programming current (≦100nA/cell) are realized because only around 200 holes are needed to change the storage state of each bit. Fig.3.10 shows the temperature dependence of sensing current. Weak dependence is observed due to that the dominant mechanism of BTB current is tunneling as shown in Fig.3.4 (b). Besides, fresh cells and cycled cells show similar temperature dependence.

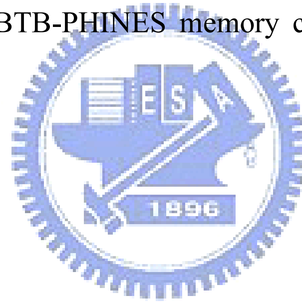
3.4.2 Cell Endurance, Retention, and Disturbances

Fig.3.11 shows the cell endurance of 2-bits-per-cell operation. A large operation window is maintained until 10K cycles. Fig.3.12 shows the cell retention, and the storage temperature is 150C. Almost no charge loss and charge gain can be obtained in a 1-cycled cell. Although a slight charge loss and charge gain are observed in the erased and the programmed cells after 10K cycles, respectively, the large operation window guarantees good cell retentivity. Fig.3.13 shows the characteristics of read disturbance in the non-selected cells (pass transistors). The dominant disturbance is the gate stress (Vg=10V or 12V with Vd=Vs=Vb=0V). Almost no disturbance is

observed in the non-selected cells. Fig.3.14 shows the characteristics of read disturbance in the selected cells (Vg/Vd/Vs=-10/2/F). Although a little current degradation is observed in the erased states, the performance is 1 to 2 orders of magnitude better than the required product specification. Compared to 1-cycled cells, 10K-cycled cells show more degradation in the erased state.

3.5 Conclusion

We propose a novel NAND-type BTB-PHINES nitride trapping storage flash memory cell featuring physically 2-bits-per-cell storage, high-density storage, low power operation, and simple process. BTB-PHINES memory cell eliminates the 2-bit interaction effect by using the local BTB-sensing scheme. Accordingly, a large memory operation window and good cell performance can be obtained. Besides, a novel modified NAND-type array architecture is designed for BTB-PHINES operation. Fast cell programming (≦60μs) can be achieved by a low programming current (≦100nA/cell), which realizes a high programming throughput. The sensing current shows weak temperature dependence, and good cell reliability is demonstrated. These characteristics make BTB-PHINES memory cell suit mass storage and data flash applications.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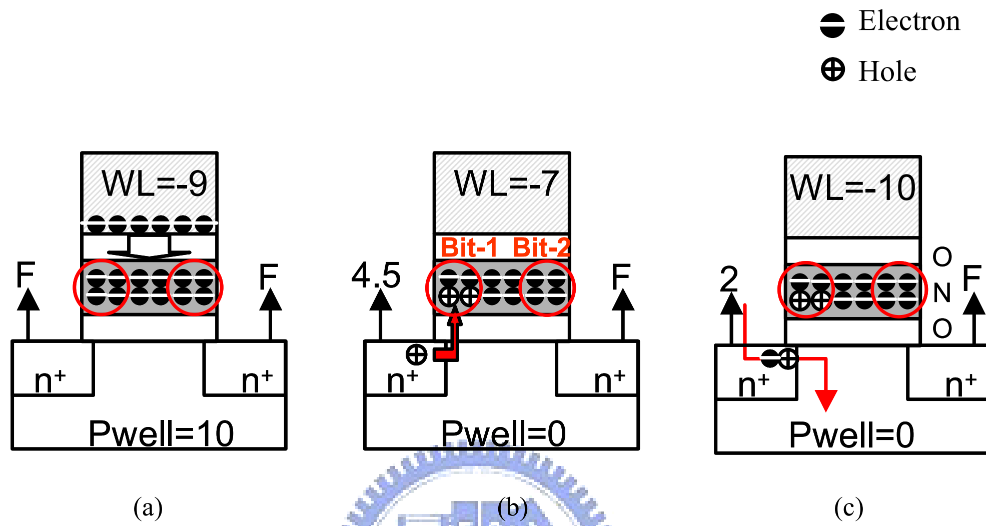


(a) (b) (c)

Fig.3.1 Schematic representations of PHINES cell operations. (a) 2 bits are erased by FN electron injection. (b) Bit-1 is programmed by BTBT HH injection. (c) Bit-1 is read via sensing the BTB current. Bit-2 can be programmed and sensed by interchanging the role of the source and the drain.

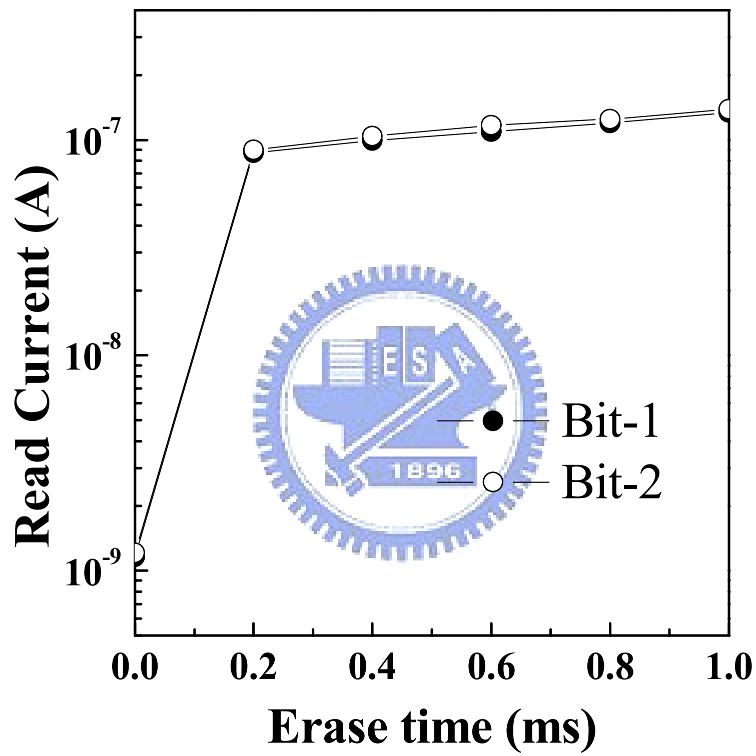


Fig.3.2 Two-bits-per-cell erasing characteristics.

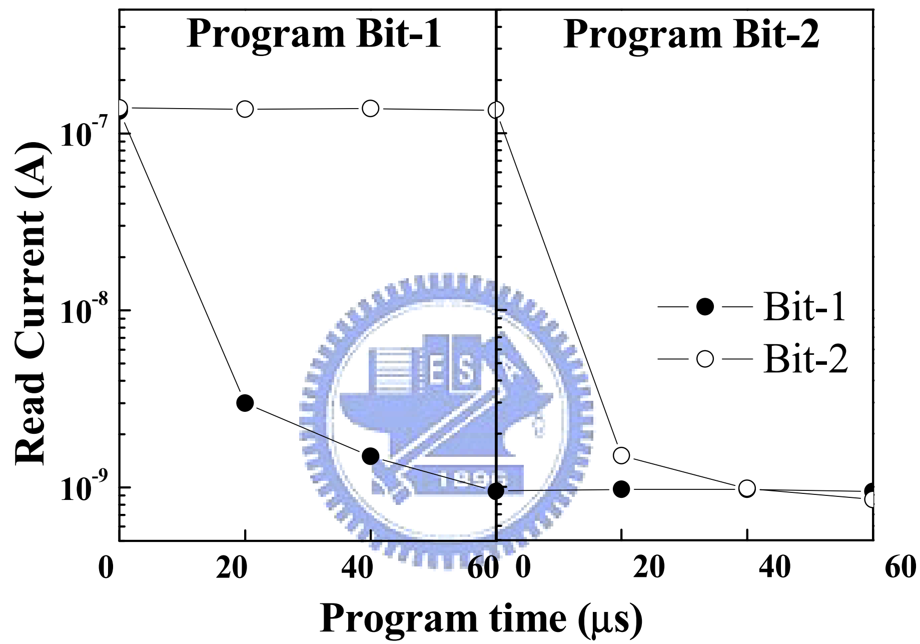


Fig.3.3 Two-bits-per-cell programming characteristics. (a) Bit-1 is programmed while Bit-2 is in an erased state. (b) Bit-2 is sequentially programmed while Bit-1 is in a programmed state.

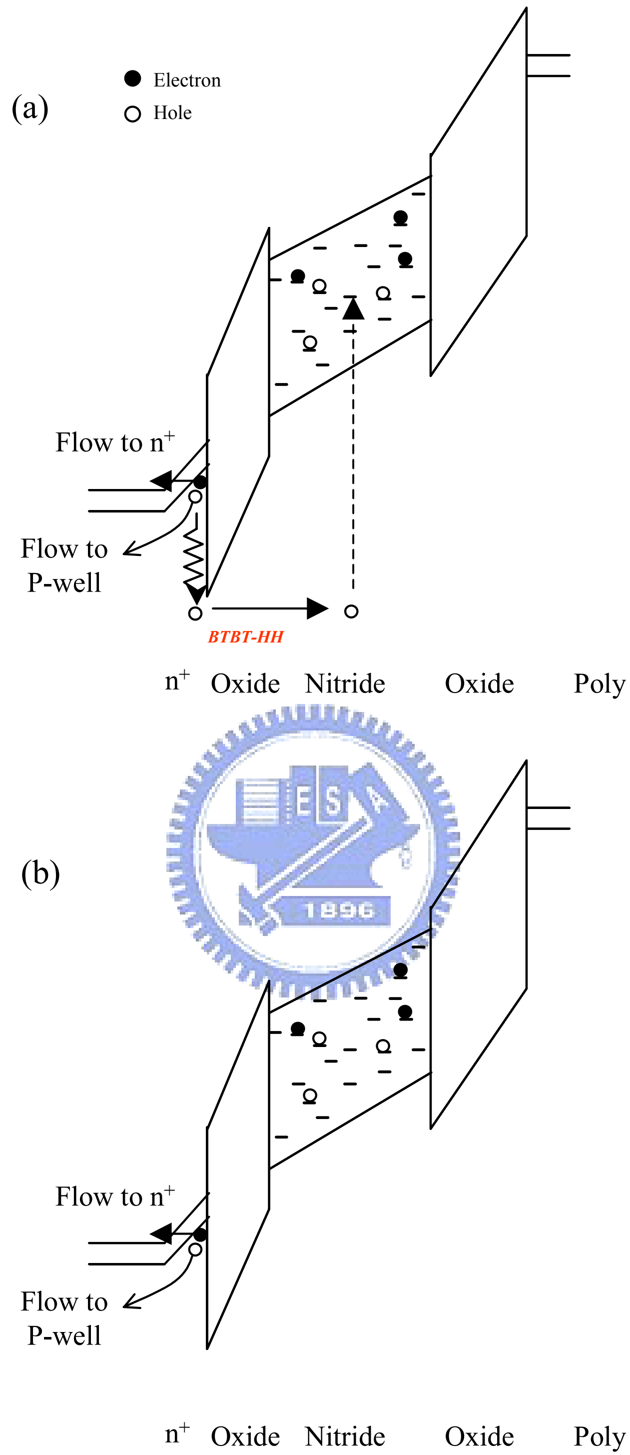


Fig.3.4 Band structures of (a) BTB-PHINES program operation and (b) BTB-PHINES read operation.

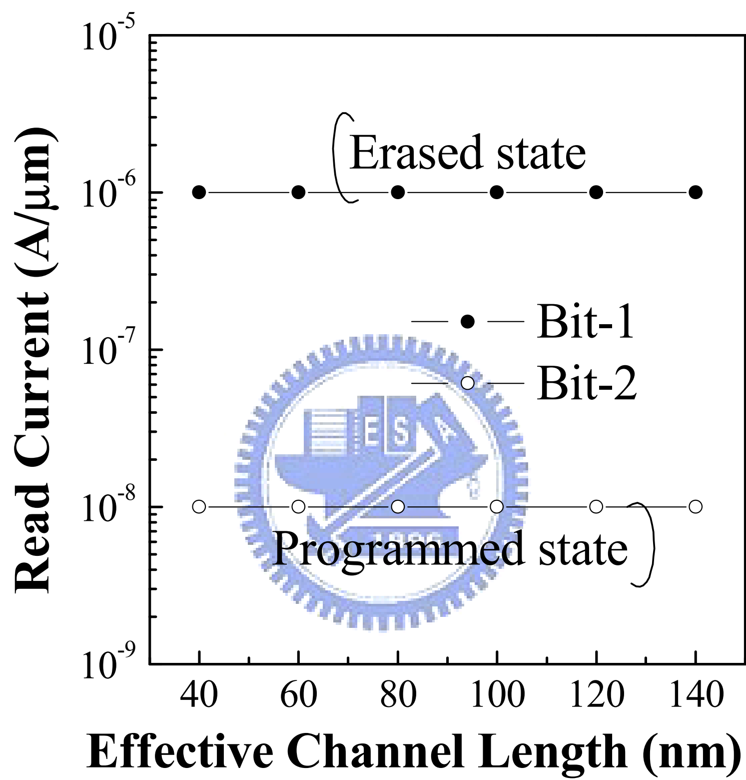


Fig.3.5 Simulated read current in different channel lengths.

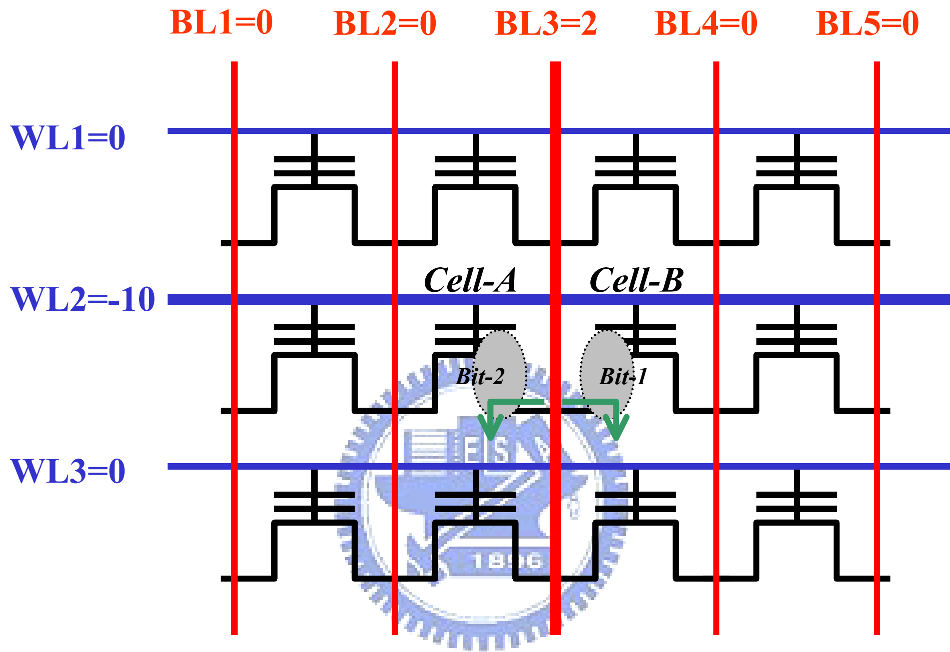
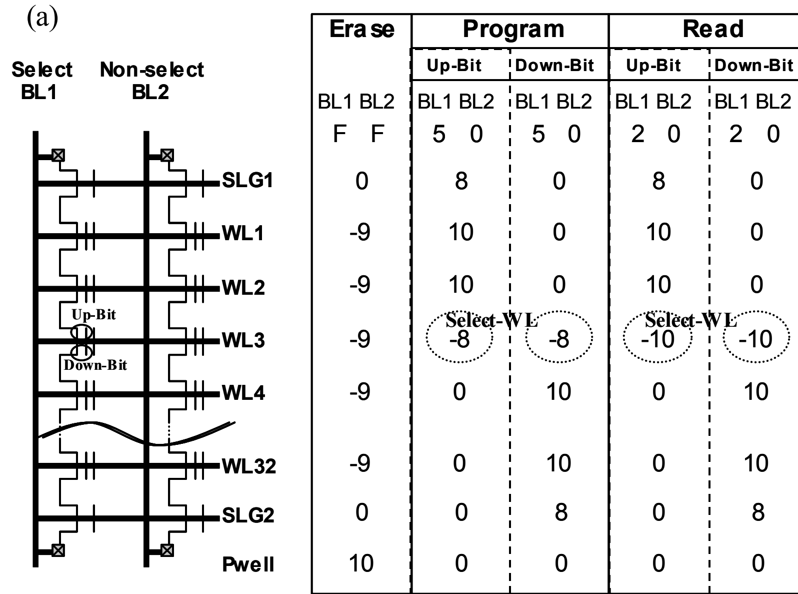


Fig.3.6 Schematic representation of BTB sensing scheme in the virtual ground array.



	Erase	Program Up-Bit	Program Down-Bit	Read Up-Bit	Read Down-Bit
	BL1 BL2	BL1 BL2	BL1 BL2	BL1 BL2	BL1 BL2
	F F	5 0	5 0	2 0	2 0
SLG1	0	8	0	8	0
WL1	-9	10	0	10	0
WL2	-9	10	0	10	0
WL3	-9	-8	-8	-10	-10
WL4	-9	0	10	0	10
WL32	-9	0	10	0	10
SLG2	0	0	8	0	8
Pwell	10	0	0	0	0

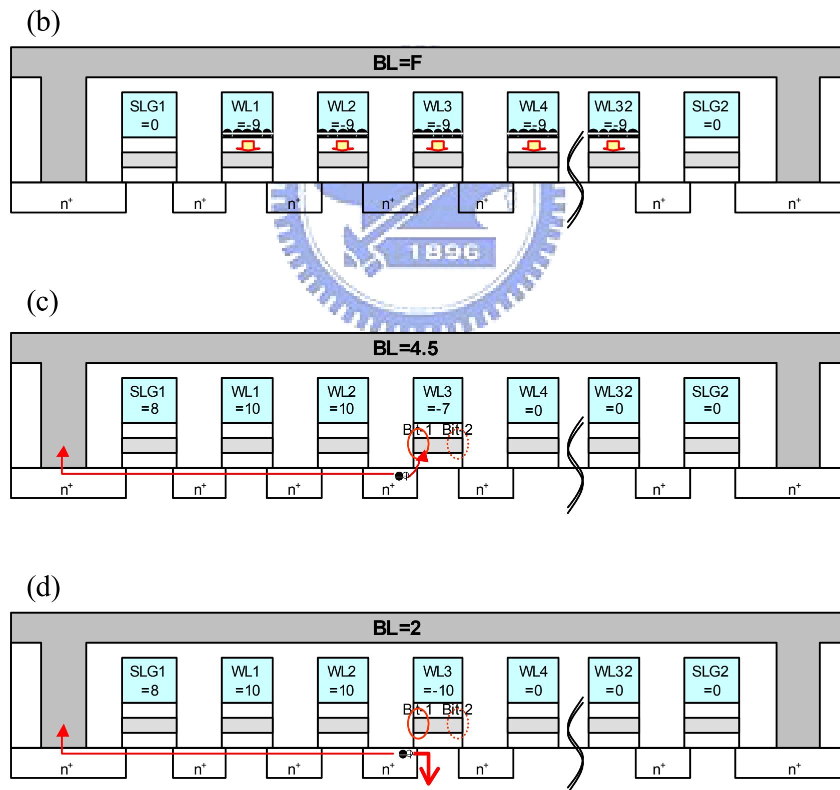


Fig.3.7 (a) The modified NAND-type array architecture and the operation conditions. (b) The cross sectional schematics of the array and the erase operation. (c) The cross sectional schematics of the array and the program operation. (d) The cross sectional schematics of the array and the read operation.

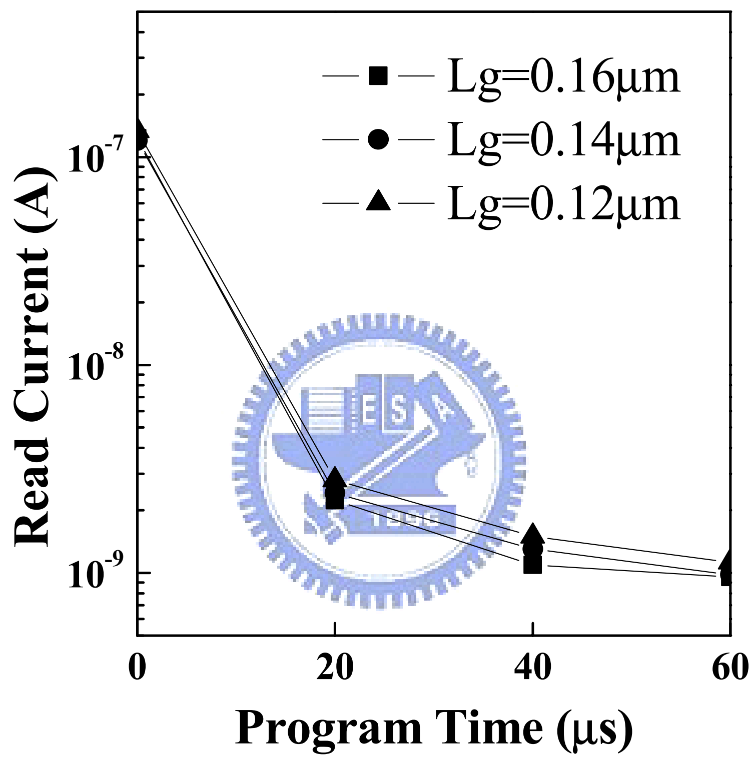


Fig.3.8 The program characteristics in three different gate lengths.

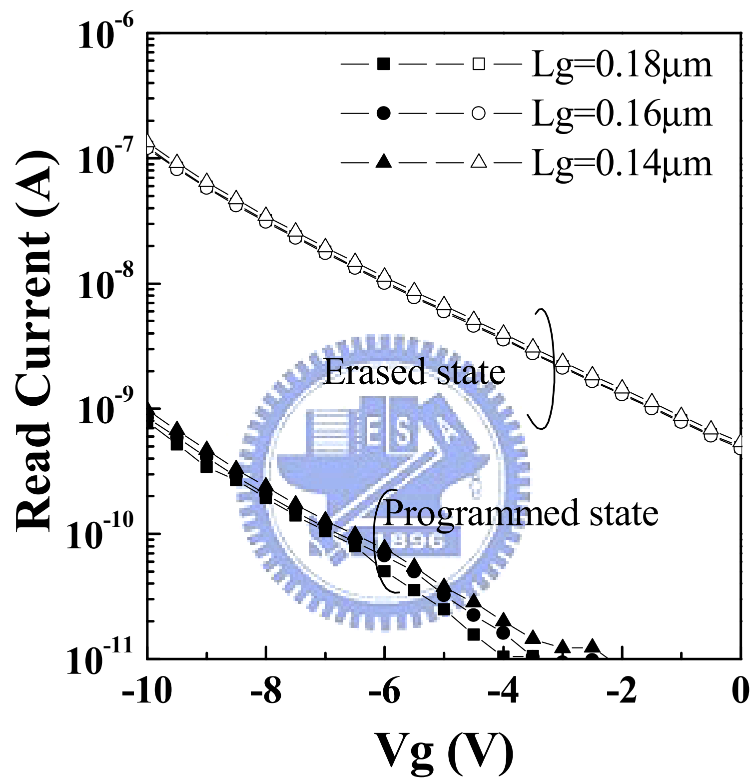


Fig.3.9 The IV characteristics in three different gate lengths.

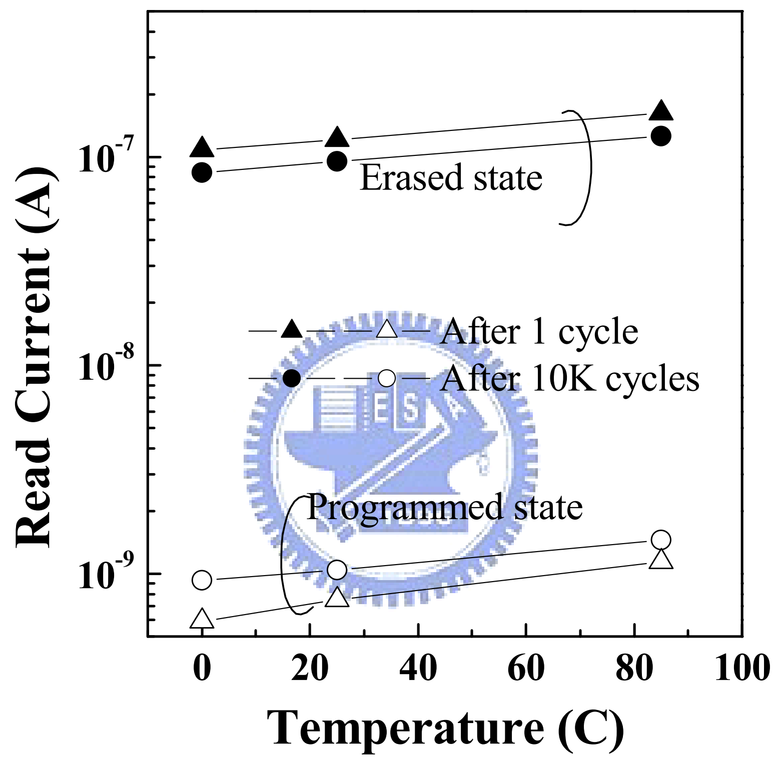


Fig.3.10 The temperature dependence of the read current in 1 cycled and 10K cycled cells.

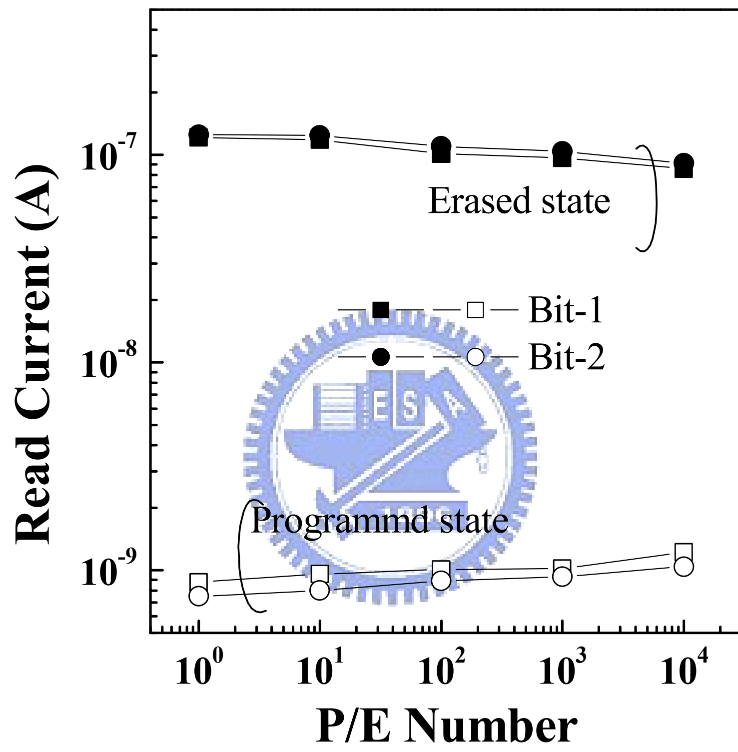


Fig.3.11 The cell endurance of 2-bits-per-cell operation.

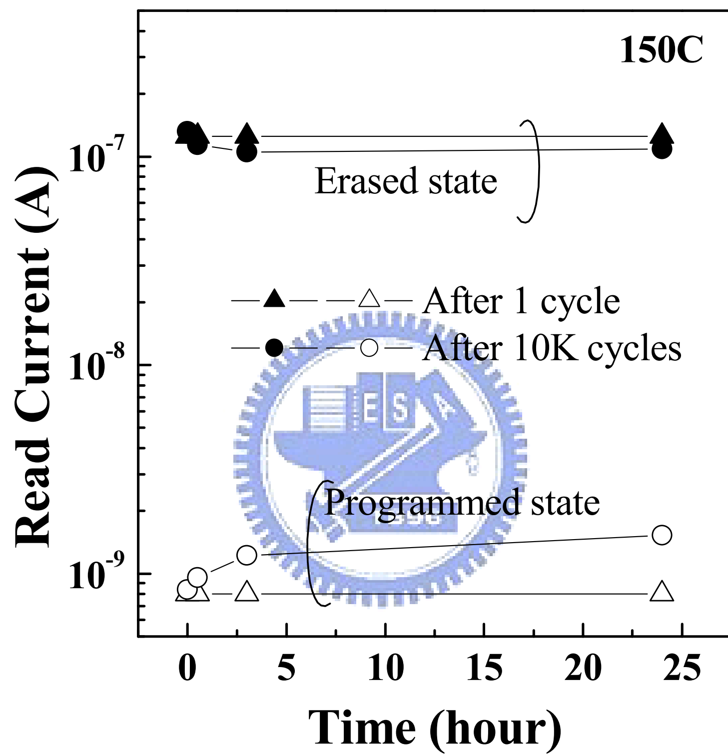


Fig.3.12 The cell retention characteristics of 1-cycled and 10K-cycled cells. The storage temperature is 150C.

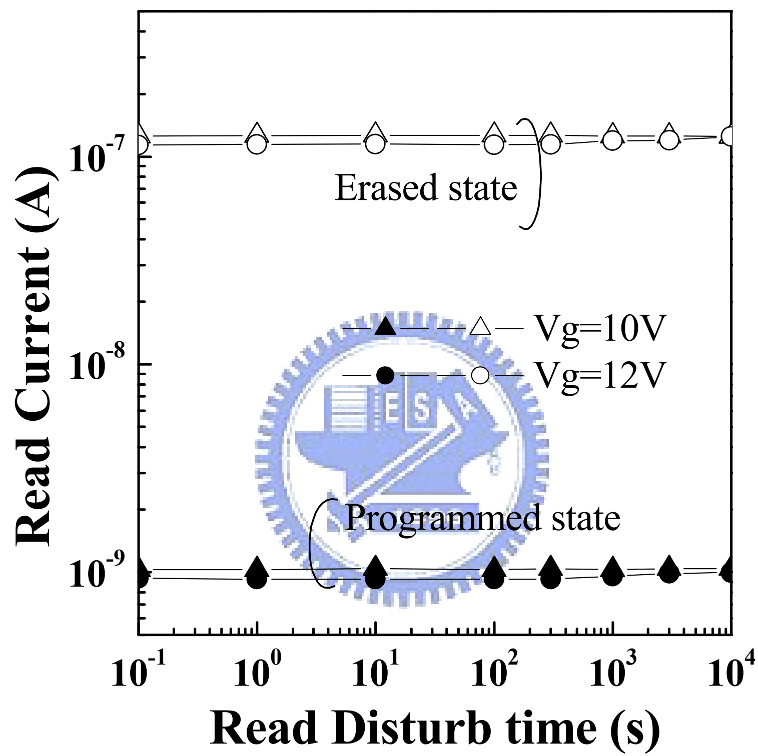


Fig.3.13 The read disturbance characteristics of the non-selected cells that serve as the pass transistors (Vg=10V or 12V, Vs=Vd=0).

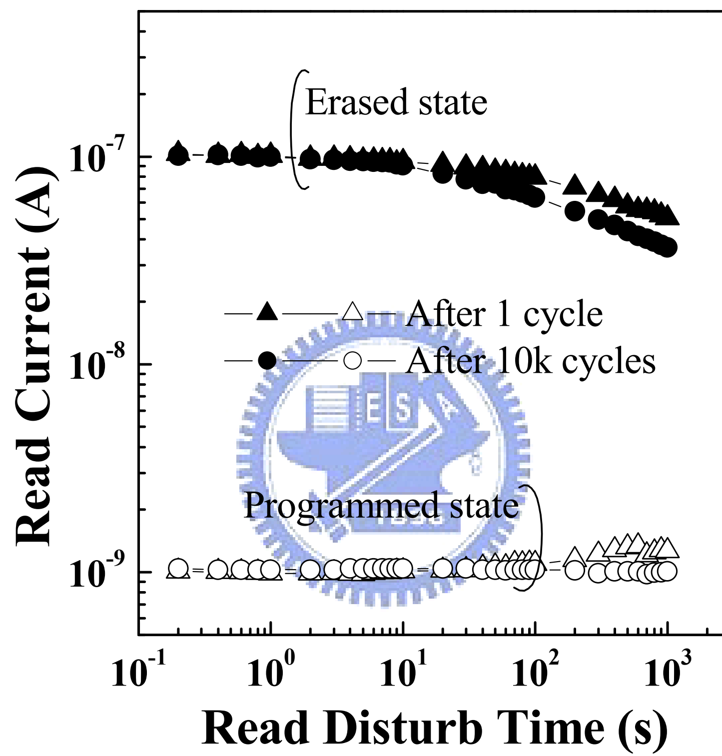


Fig.3.14 The read disturbance characteristics of the selected cells (Vg/Vd/Vs=-10/2/F). One-cycled and 10K-cycled cells are compared.

Chapter 4

Evaluation of Device Scalability of PHINES Flash Memory Cell

4.1 Introduction

According to the previous studies [4.1], conventional floating gate memories cannot maintain Moore's Law (the memory density has doubled every generation) and face scaling challenges at around 30nm CMOS generation. NOR-type floating gate memory cell suffers several critical limitations [4.2] including active area reduction, junction breakdown, cell punch, maintaining narrow Vt distribution in MLC, and non-scalable tunnel oxide and inter-poly dielectric layer. NAND-type floating gate memory cell faces the scaling challenges of floating gate interference, a lower GCR coupling ratio, few storage carriers, and less tolerant charge loss in MLC operation. Although several approaches using non-floating gate structure including SONOS memory cell [4.3], PRAM [4.4], MRAM [4.5], and FRAM [4.6] are proposed for future scaling, they uses new materials, and the reliability and the uniformity are still issues until now.

In chapter 2 and chapter 3, we propose a novel PHINES memory cell. PHINES memory uses nitride traps for carrier storage and does not suffer floating gate interference. In this chapter, the scaling challenges of 1-bit and 2-bit PHINES cells will be discussed.

4.2 Scaling Limitation of a 1-Bit PHINES Cell with Backward Read Scheme

In 1-bit PHINES memory architecture, channel current sensing and backward read scheme are adopted due to its higher sensing current (see chapter 2). Fig.4.1 shows the storage conditions of a 1-bit PHINES cell. Fig.4.2 shows the NAND array architecture and the bias conditions of 1-bit PHINES operation. One string contains 32 memory cells and 2 select-transistors (SLG1 and SLG2) that are arranged in series. The source of each memory string is connected to Vs and the drain of each memory string is shorted to its own metal bit-line (BL).

Although 1-bit PHINES cell does not have the scaling issue of floating gate interference, it still faces several scaling challenges. The first one is that the reduced number of storage carriers in a scaled device as shown in Fig.4.3. In 10nm CMOS generation, less than 10 storage carriers may be obtained (Vt window=2.5V, storage electron density=$1\text{x}10^{19}$ cm^{-3}), which induces distribution, variation, and reliability issues. Although thinner ONO thickness and larger operation window can be used to increase the storage carriers, worse cell retention is still suffered. Another scaling

challenge is the issue of inter-WL leakage/breakdown. As shown in Fig.4.4, a negative bias on the selected WL and a positive bias on the pass WL are essential for PHINES program and read operations. The high voltage drop between the selected and non-selected WLs may induce the inter-WL leakage/breakdown as the WL spacing scales. Although a thinner ONO thickness, lower cell Vt, and a smaller operation window can be used to suppress this issue, it will be a problem after 15nm generation. The other scaling challenge is the degraded cell punch and junction breakdown in a scaled device, which reduces the injection efficiency of hot holes. Fig.4.5 (a) and (b) compare the paths of punch leakage current in a NOR-type and a NAND type array during the program operation, respectively. Since the cells are arranged in parallel in NOR-type array, the dominant leakage current is the punch current in the non-selected WLs (Vg/Vd/Vs=0/5/0). In the NAND-type array with series cells, the punch leakage current is dominated by the selected string itself (Vg/Vd/Vs=-5/5/0). Fig.4.6 compares the cell punch current in a NOR-type and a NAND-type array. NAND-type PHINES memory cell shows better scalability and can reduce the punch current by the high negative bias on the selected WL. NOR-type PHINES cell suffers tough scaling challenges due to plenty of leakage paths without the suppression of negative gate voltages. Fig.4.7 shows the punch current of NAND-type PHINES in various channel lengths. A shallower junction depth, a higher gate voltage on the selected WL, and a lower BL voltage can suppress the cell punch without degrading the junction breakdown. The requirement of programming at 15nm generation without cell punch and reduced carrier injection efficiency can be achieved by an optimized operation condition and substrate/junction doping. As a result, 1-bit PHINES suffers the scaling challenges of few storage carriers, inter-WL leakage/breakdown, and cell punch beyond 15nm generation.

4.3 Scaling Limitation of a 2-Bit PHINES Cell with BTB Sensing Scheme

Although backward read scheme and BTB sensing scheme can both realize 2-bits-per-cell storage, we adopt BTB current sensing scheme in 2-bit-per-cell operation since it does not have severe 2-bit interaction effect, and its larger operation window can serve high performance and good reliability. Fig.3.7 shows the proposed modified NAND-type array architecture and array operation for 2-bit PHINES operation. Compared to 1-bit PHINES architecture (NAND-type), the key feature of 2-bit PHINES is that the source of SLG1 and the drain of SLG2 are shorted to the same metal BL.

The first scaling challenge of 2-bit PHINES memory cell is the charge distribution of a programmed bit as shown in Fig.4.8. Two-bits-per-cell operation will fail, as the charge distribution is wider than half of the effective channel length. In

Fig.4.9, we use charge-pumping technique [4.7] to profile a programmed bit. The characterized device is ECD=0.17um with an effective channel length of 0.095um extracted from the TSUPREME-4 simulation. After FN electron erasing and hot-hole programming, a tail of charge pumping current (Icp) is observed. The turn on Vt (Vgh) of the Icp tail is proportional to the number of storage holes in a programmed bit while the amount of the Icp tail is proportional to the length of the programmed holes in the channel region. As shown in Fig.4.9, the Icp of the tail is around 1.3pA and the total Icp is around 11pA. Accordingly, the length of a programmed bit should be around 11nm ((1.3pAx0.095um)/11pA=0.011um). Therefore, the scaling limit of the effective channel length is around 20nm with 2-bit operation. The other scaling challenge of 2-bit PHINES is the 2-bit interaction effect. Although BTB sensing scheme shows less 2-bit interaction effect than channel current sensing scheme in long channel devices, we still observe that the electrons in an erased bit will affect the BTB current of the adjacent programmed bit in a scaled device. The 2-bit interaction ratio is shown in Fig.4.10 (a). Fig.10 (b) shows the illustration of 2-bit interaction in BTB sensing scheme. The 2-bit interaction effect increases dramatically beyond 30nm generation (effective channel length=20nm). Fig.4.11 shows the storage carriers per bit in 2-bits-per-cell operation. Less than 10 storage carriers per bit may be obtained in 15nm CMOS generation. As a result, 2-bit PHINES suffers scaling challenges of the distribution of a programmed bit, 2-bit interaction effect, and few storage carriers beyond 30nm generation.

4.4 Conclusion

Table 4.1 compares PHINES and floating gate technologies. PHINES technology can achieve compatible performance and bit size to floating gate technologies for most data flash memory applications. PHINES memory cell shows high scalability, and 15nm generation for 1-bit-per-cell storage and 30nm generation for 2-bit-per- cell storage are feasible in NAND-type array architecture.

n+ n+

(a)

n+ n+

(b)

Fig.4.1 The storage conditions of a 1-bit PHINES memory cell: (a) erased state, and (b) programmed state.

Select BL1 Non-select BL2

	Erase	PGM	Read
	BL1 BL2	BL1 BL2	BL1 BL2
	F F	4.5 0	0 1.5
SLG1	0	8	8
WL1	-9	10	8
WL2	-9	10	8
WL3	-9	-7 (Select-WL)	2 (Select-WL)
WL4	-9	0	8
WL32	-9	0	8
SLG2	0	0	8
Vs	F	0	1.5
Pwell	10	0	0
	FN electron injection	BTB HH injection	Channel current sensing

Fig.4.2 The NAND-type array architecture and bias conditions of 1-bit PHINES operation with channel current sensing scheme.

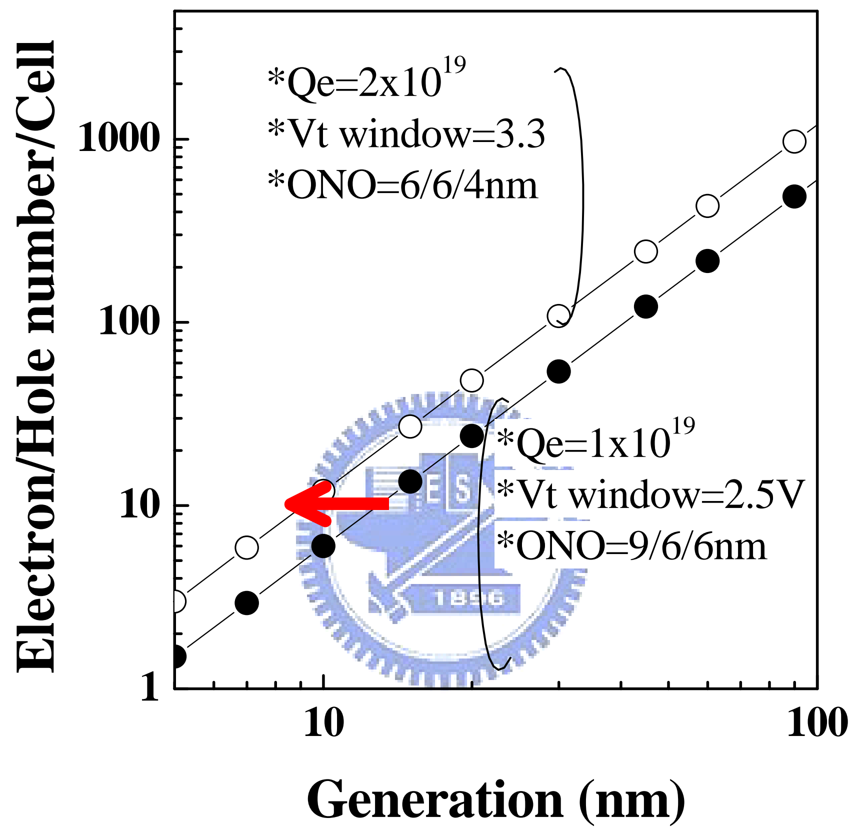


Fig.4.3 Number of storage carriers in a 1-bit PHINES cell.

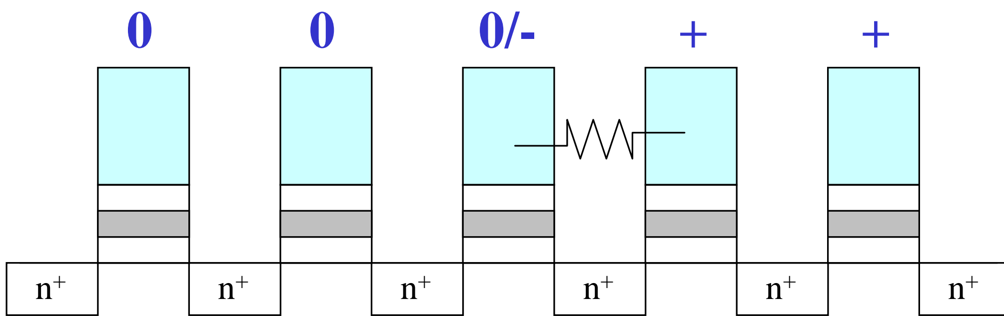


Fig.4.4 Cross sectional representation of PHINES cells arranged in NAND-type array.

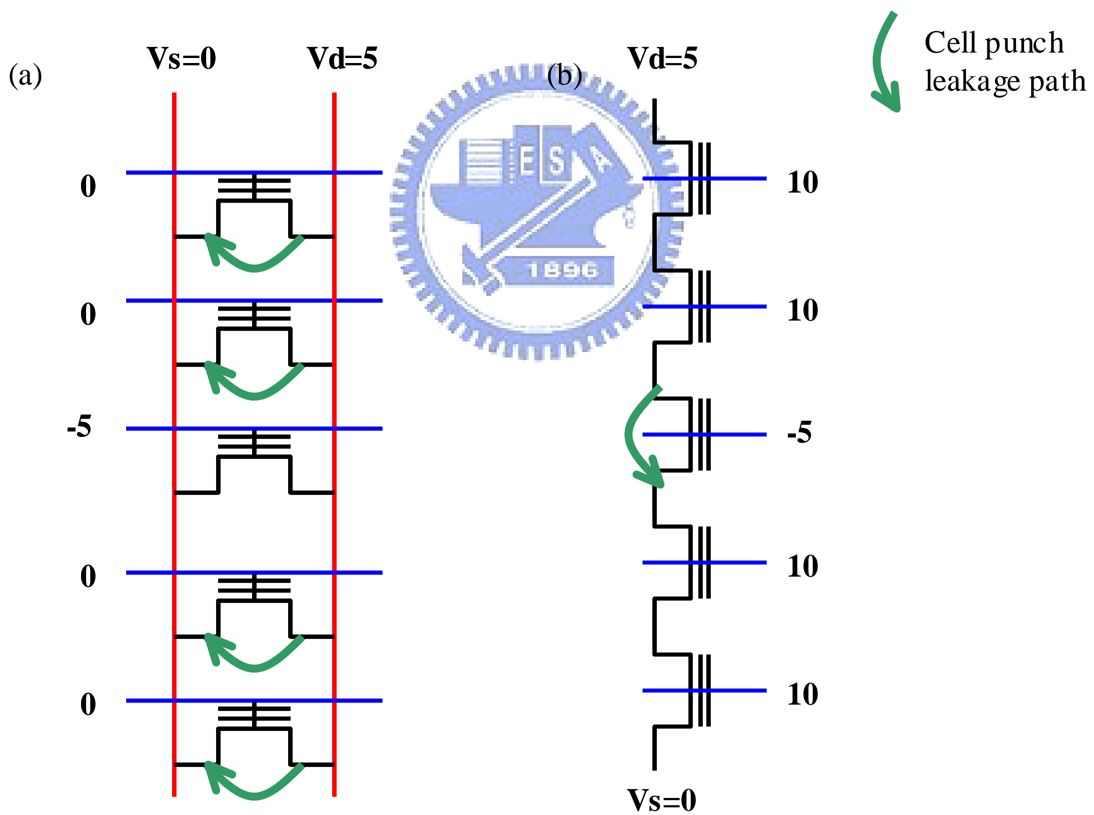


Fig.4.5 The paths of punch leakage current in (a) a NOR-type and (b) a NAND type array during the program operation.

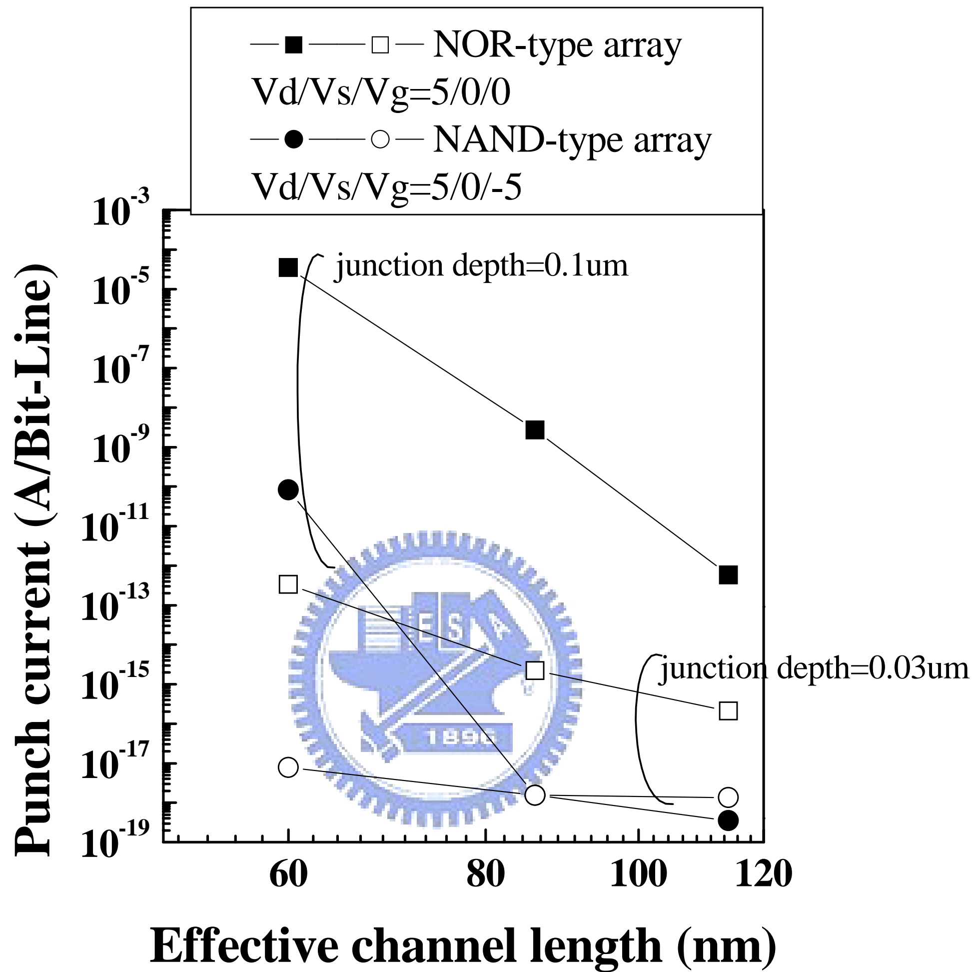


Fig.4.6 The simulated punch leakage current in (a) a NOR-type and (b) a NAND type array during the program operation. In our calculations, there are 64 parallel WLs and leakage paths within one BL in a NOR-type array in our calculation. Two junction depths are also compared. Solid symbols and open symbols represent the junction depth of 0.1um and 0.03um, respectively.

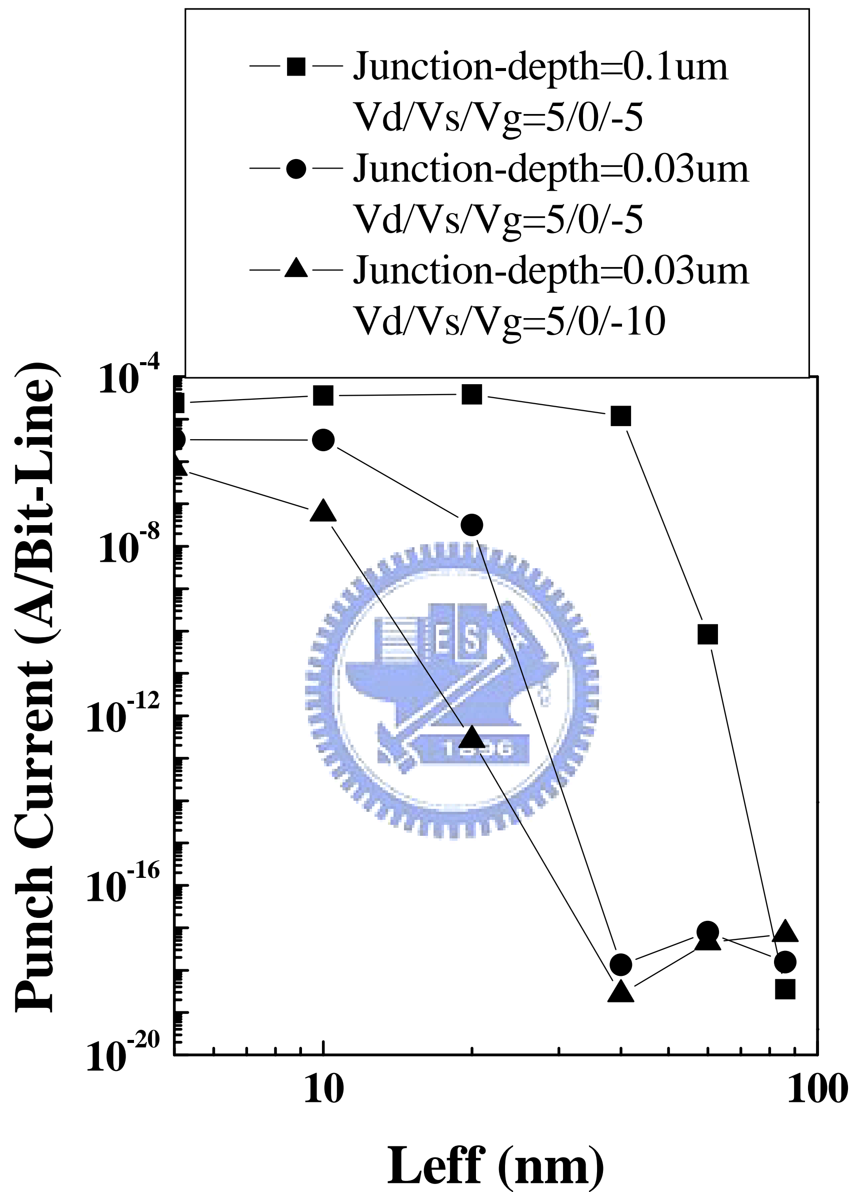


Fig.4.7 The simulated punch leakage current in a NAND-type array during the program operation. Two junction depths (0.1um and 0.03um) and two bias conditions (Vd/Vs/Vg=5/0/-5 and 5/0/-10) are compared.

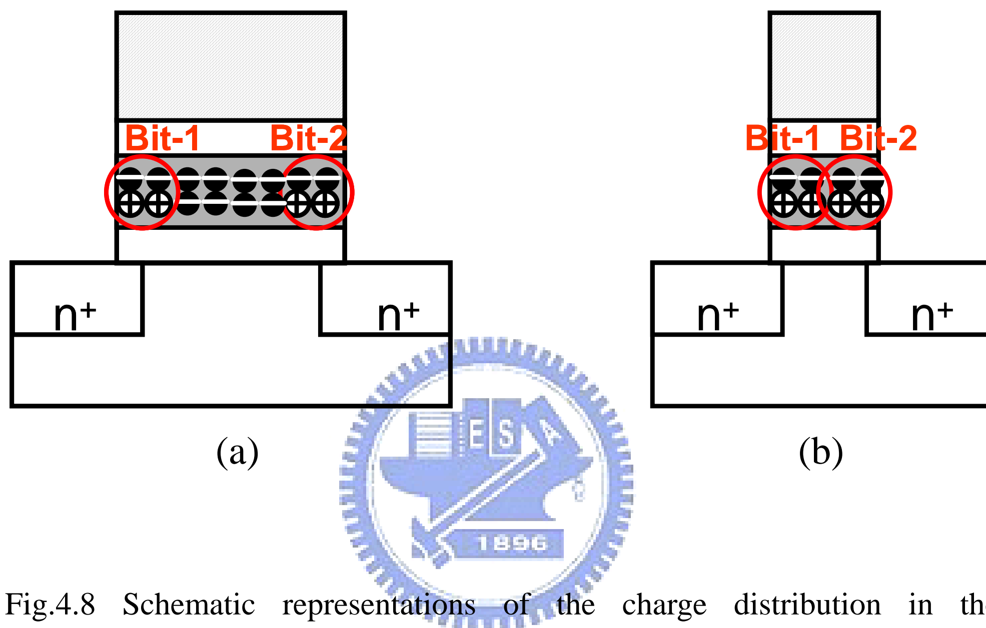


Fig.4.8 Schematic representations of the charge distribution in the 2-bits-per-cell PHINES operation: (a) long channel device with isolated two programmed bits. (b) short channel device with coupled two programmed bits.

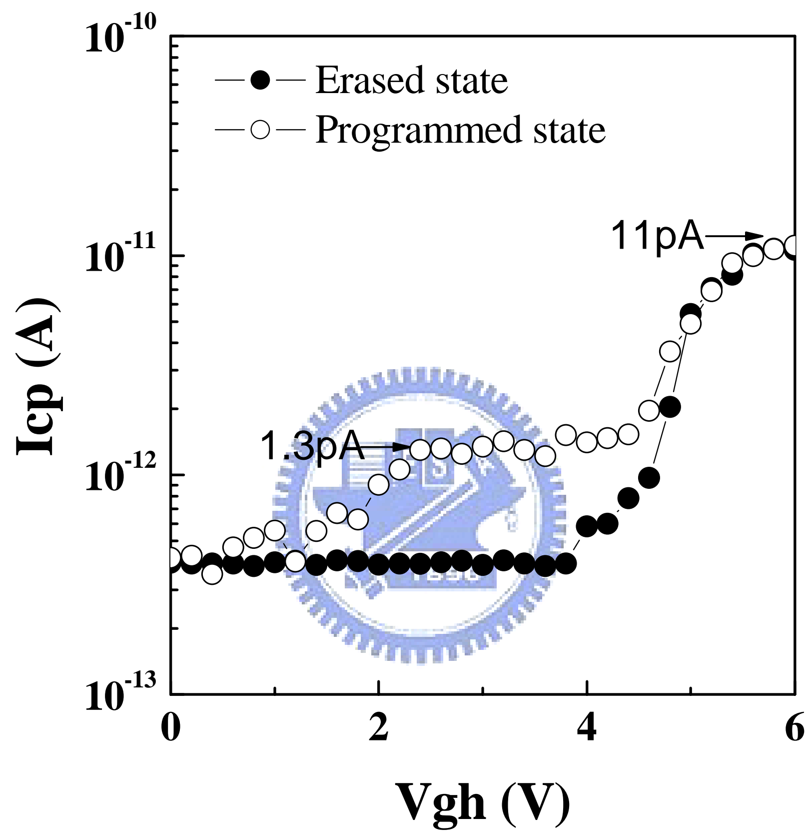
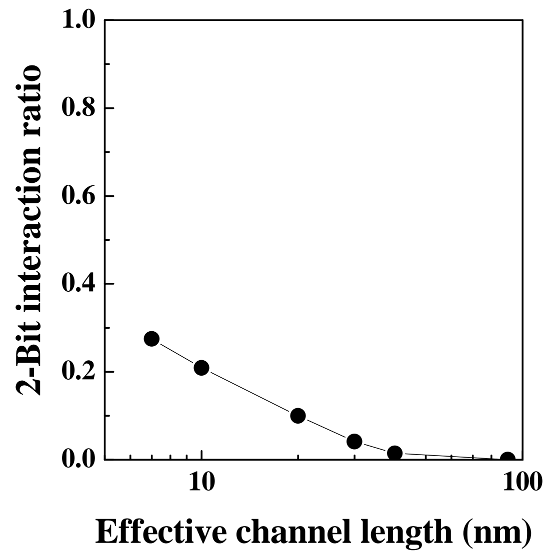
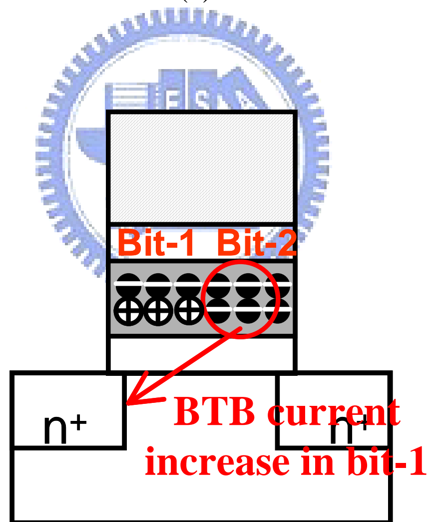


Fig.4.9 Charge pumping characteristics of a PHINES cell.



(a)



(b)

Fig.4.10 (a) The 2-bit interaction ratio of a PHINES cell with BTB sensing scheme. (b) Illustration of 2-bit interaction in BTB sensing scheme. Electrons in bit-2 (erased state) will increase the BTB current of the programmed bit-1 in a scaled device.

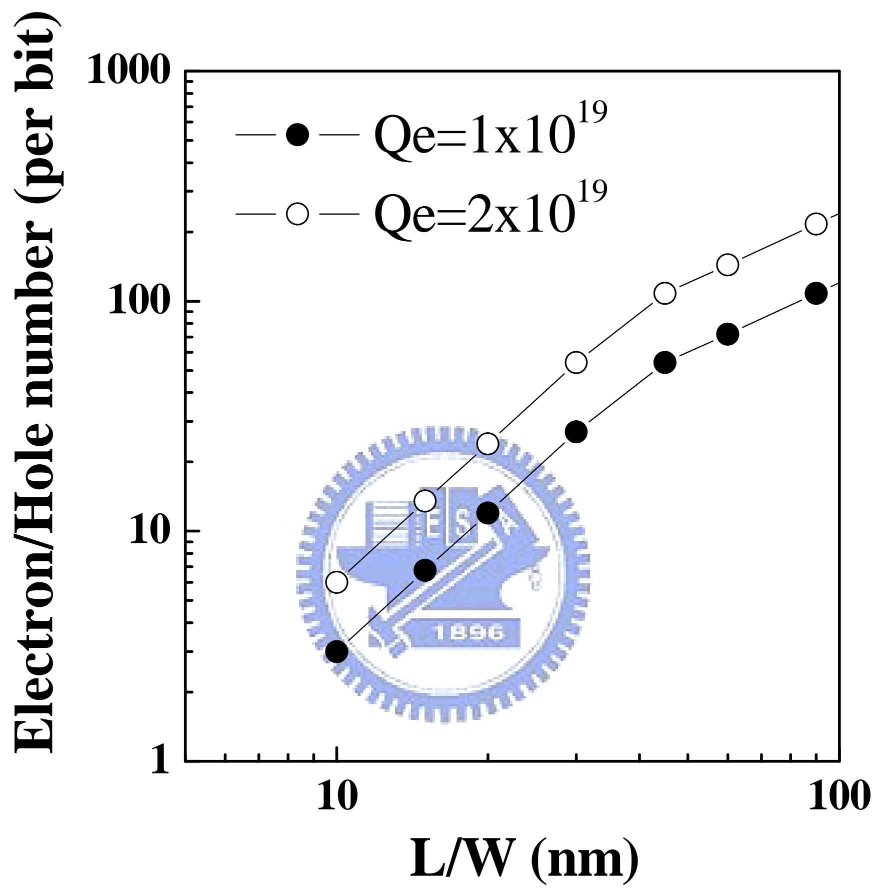


Fig.4.11 Number of storage carriers per bit in a 2-bit PHINES memory cell with BTB sensing scheme.

Table 4.1 The comparison table of PHINES and floating gate technologies.

Data flash	FG		PHINES	
Storage	Floating gate		Nitride	
Array	NAND	NAND	NAND	Modified NAND
Sensing	Channel current	Channel current	Channel current	BTB current
Bit/cell	1 (SLC)	2 (MLC)	1	2
Bit size	$4.6F^2$	$2.3F^2$	$4.6F^2$	$2.3F^2$
Sensing current	$\sim 10^{-6}A$	$\sim 10^{-7}A$	$\sim 10^{-6}A$	$\sim 10^{-7}A$
Scalability	~30nm	~30nm	~15nm	~30nm
Scaling limit	•FG coupling •# of carriers •GCR	•FG coupling •# of carriers •GCR	•# of carriers •Inter-WL leakage •Punch/JBD	•PGM profile •2-bit interaction

Chapter 5

Programmable Resistor with Erase-less Non-Volatile Memory (PREM) for SOC and Embedded Flash Applications

5.1 Introduction

The stand-alone Diode Programmable Read Only Memory (DPROM) has been proposed as an economical one-time programmable memory device [5.1]. DPROM uses antifuse cell structure with gate oxide between n+ polysilicon gate and p+ diffusions. The oxide breakdown serves as the storage node. The cell is unprogrammed when the gate oxide is intact and the cell is programmed when the applied stress voltages break down the gate oxide. In addition, three-dimensional one-time-programmable (3D-OTP) memory technology [5.2-5.3] is demonstrated for high density and low cost ROM applications. The memory cell utilizes vertical polysilicon diodes with an antifuse [5.1]. The cells can be stacked above read/write transistors and above another, and its 3D architecture enables very high packing density. However, the applications of the conventional antifuse memory are limitied since it can perform only one-time programming and it also suffers testing issues.

In advanced CMOS devices, oxide breakdown behavior of an ultra-thin oxide (<2nm) is quite different from that in a thicker one [5.4-5.7]. Fig.5.1 compares the breakdown evolutions in a 1.4nm oxide MIS diode and a 2.2nm oxide MIS diode. The breakdown in the 1.4nm oxide MIS diode (Fig.5.1 (b)) is evolved in a progressive way, and the leakage current increases gradually with stress time.

Here, we construct a novel non-volatile memory cell named Programmable Resistor with Erase-less Non-Volatile Memory (PREM). PREM is arranged in antifuse structure and utilizes the progressive breakdown of an ultra-thin oxide layer for memory storage. Compared to the conventional OTP antifuse memory, PREM can realize MTP (multi-time programming), MLC (multi-level cell), non-volatility, and low voltage operation. Only one extra or none mask is needed with CMOS standard process. PREM is proposed and studied for SOC applications.

5.2 Cell Structure and Characteristics

5.2.1 PREM Cell Structure

As shown in Fig.5.2, PREM utilizes an anti-fuse cell structure [5.1] and the novel mechanism of progressive breakdown in an ultra-thin oxide for memory storage and operation. Fig.5.3 shows typical IV characteristics of a fresh and a stressed cell. The

cells are stressed at a high program voltage while the read current are measured at a low read voltage of 1.3V. The program voltage will ìtriggerî the progressive oxide breakdown, and the read current between the gate and the n+ diffusion increases. The diode formed between the gate and the n+ diffusion can sustain high reverse bias, which eliminates the leakage current in the negative gate voltage (Vg). Fig.5.4 shows the program voltage dependence of the read current evolution in PREM cells. The breakdown evolution rate shows strong dependence of stress biases, which means that the program speed and the current evolution can be well controlled by the stress voltage and the stress time interval.

Table 4.1 discloses the PREM operation parameters. Only one extra or none mask is needed with CMOS standard process to realize PREM cell. The operation voltages of PREM are less than ±3V, which does not need high-voltage transistors and high-voltage processes. General I/O devices can serve the operation requirements.

5.2.2 MLC Operation Principles

PREM can realize MLC to increase the memory density. Fig.5.5 shows the program algorithm of MLC. Since the oxide breakdown is evolved in a progressive way, the read current can be programmed to any desired level by repeating the program and program verification. Fig.5.6 (a) shows an example of 2-bits-per-cell storage with 3 reference current levels and 4 storage levels. Fig.5.6 (b) shows an example of 3-bits-per-cell storage with 7 reference current levels and 8 storage levels. Fig.5.6 (c) shows an example of 4-bits-per-cell storage with 15 reference current levels and 16 storage levels. MLC operation demands precise control of program speed and current evolution, which can be optimized by the stress voltage and stress time interval since the breakdown evolution rate shows strong dependence of stress biases as show in Fig.5.4.

5.2.3 MTP Operation Principles

Fig.5.7 shows the program algorithm of PREM to realize MLC. According to the designed set of reference currents, the cell is repeated by the programming and program verification until the read current reaches the desired level. Fig.5.8 shows the exemplary illustrations of cell distributions and Fig.5.9 shows the behavior of a PREM cell to realize MTP operation. For the 1st program operation with reference current ref-1, the read current is stressed to the desired level (higher than ref-1) where a bit is stored in (Fig.5.8 (a) and Fig.5.9 (a)). To perform the 2nd programming step (Fig.5.8 (b) and Fig.5.9 (b)), the reference level is switched to ref-2 that is higher than the read current of all cells. The data are reset by changing the reference level without an ìeraseî in conventional operation of flash memories. Following, program voltages

are applied to program the selected cells to another specific level (higher than ref-2) where the data of ì1î are programmed while the others are remained at ì0î state. Fig.5.8 (c), and Fig.5.9 (c) show the 3rd programming. No erase is performed in the operation. Instead, PREM switches reference level to reset the stored data, and we name this operation scheme ìErase-less Algorithmî. Although PREM can only realize MTP due to the limited increase of the read current, the cell performance is much better than the conventional antifuse memory that can only achieve one-time programming.

5.2.4 MLC+MTP Operation Principles

PREM can also combine the algorithms of MTP and MLC to meet the required applications. In Fig.5.10, 2-bits-per-cell storage is demonstrated with at least 5 programming times. However, it is a tradeoff between the number of allowed programming times and the number of stored bits. If a higher memory density (more storage bits) is performed, it will reduce the number of allowed programming times. The choice of MTP or MLC depends on the required applications.

5.3 PREM Array Architecture

Fig.5.11 (a) and Fig.5.11 (b) illustrate the array architecture for PREM operation and anti-fuse cell structure. The word-lines (WLs) are P+-polysilicon. The bit-lines (BLs) are n-type diffusions separated by deep trenches. N^-/N^+ diffusions are chosen for BLs where N^- is utilized to reduce the junction leakage and the N^+ is used to decrease the bit-line resistance. An ultra-thin oxide of 15nm isolates the BLs and WLs. Only one extra or none mask is needed with CMOS standard process to realize PREM cells. Besides, the area of the crossing point cell of $4F^2$ is feasible and less than $2F^2$/bit can be achieved by using MLC operation.

The array program operation is shown in Fig.5.12. Device A is the selected cell for programming, and device B and device C are non-selected cells. In device A, programming is done by applying a high positive voltage (2.5V) to the selected WL (WL2) and a high negative voltage (-2.5V) to the selected BL (BL2). The high oxide field and stress current will trigger the progressive breakdown and device A is programmed accordingly. In unselected cells, an inhibit WL bias (-2.5V) and an inhibit BL bias (2.5V) are applied on the non-selected BLs and WLs, respectively. No tunnel current will flow through device B (low oxide field) and device C (reverse biased) to trigger programming and progressive breakdown.

The array read operation is shown in Fig.5.13. Device A is the selected cell for reading, and device B and device C are non-selected cells. In device A, read is done by applying a positive voltage (1.3V) to the selected WL (WL2) and grounding

the selected BL (BL2). Accordingly, Device A is forward biased, and the BL current is sensed to verify the storage state. In the unselected cells, an inhibit WL bias (0V) and an inhibit BL bias (1.3V) are applied on the non-selected BLs and WLs, respectively. No sensing current will flow through device B (low oxide field) and device C (reverse biased).

5.4 Disturbances and Cell Retention

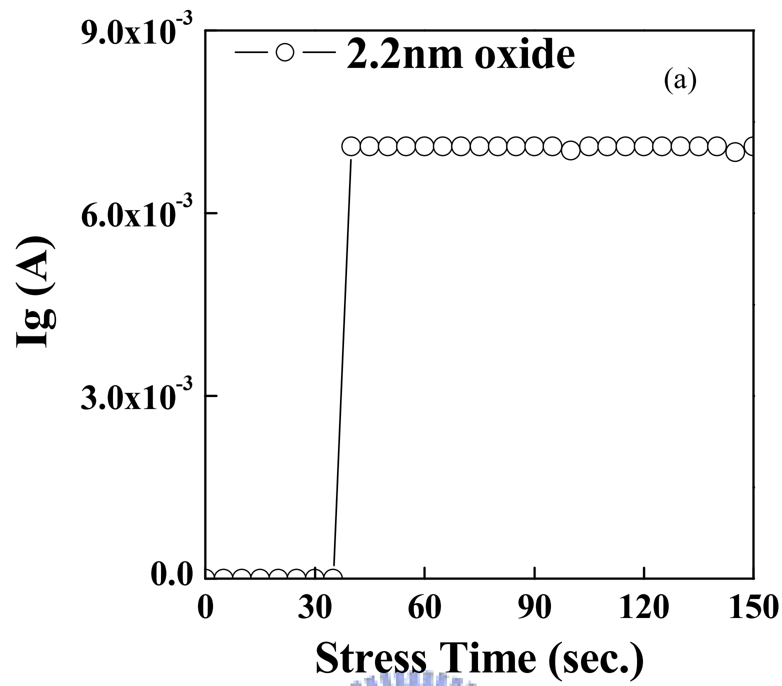
Fig.5.12 shows the distribution of the disturbed cells (device C) during device A programming. Fig.5.14 (a) and (b) show the disturbance behavior of device B and device C, respectively, and no program disturbance is observed for 1000 seconds (~100x programming time). The characteristics of read disturbance in 4 programmed-levels are shown in Fig.5.15 and no read disturbance is observed for 10^4 seconds. Fig.5.16 shows the cell retention of PREM at a high temperature of 150C. No retention degradation is observed in 3 programmed-levels. PREM shows excellent reliability characteristics, and retention results without program and read disturbance.

5.5 Scalability and Applications

PREM also shows high scalability as shown in Fig.5.17. The program characteristics of 1.4nm and 1.2nm oxide are compared. The current evolution of thinner film shows less noisy and better controllability. As shown in Fig.5.18, PREM can be easily integrated with advanced logic circuits and SRAM for SOC applications. Besides, PREM can be also as a standalone high-density storage device. Table 4.2 compares PREM and other embedded memories. PREM can meet some applications in SOC, embedded flash memory, and high-density storage areas.

5.6 Conclusion

A novel non-volatile memory cell named PREM (Programmable Resistor with Erase-less Memory) is proposed and characterized. Instead of the conventional ìeraseî operation, PREM adjusts the reference level to reset the data. By utilizing the progressive breakdown of ultra-thin oxide and the new ìErase-lessî operation, PREM can realize MTP and/or MLC. Only one extra or none mask is needed with CMOS standard process. No degradation of cell retention, no program disturbance, and no read disturbance are observed, and the cell reliability is guaranteed. PREMís low voltage operation, high scalability, and simple process are superior for SOC or very low cost and high-density storage applications.



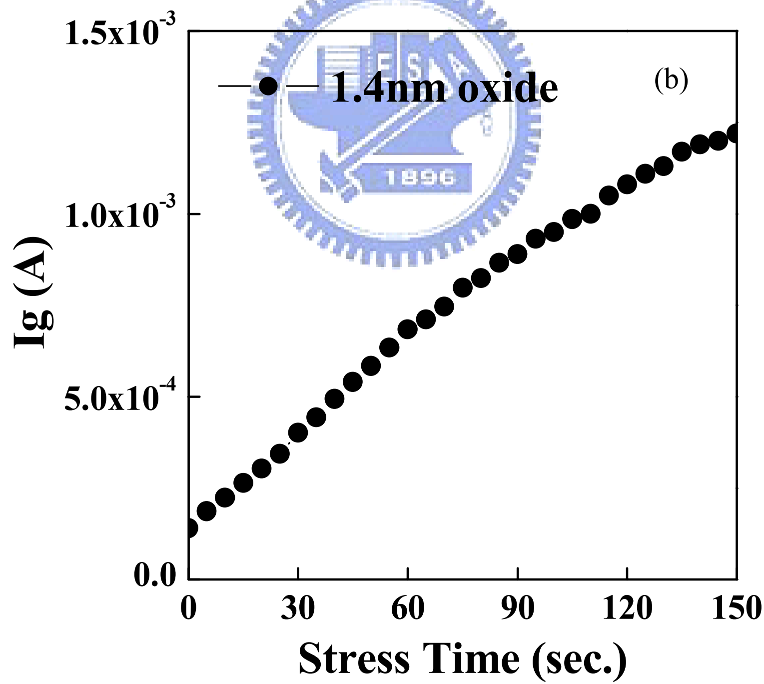


Fig.5.1 (a) The breakdown behavior of a MIS diode with a 2.2nm oxide. (b) The breakdown behavior of a MIS diode with a 1.4nm oxide.

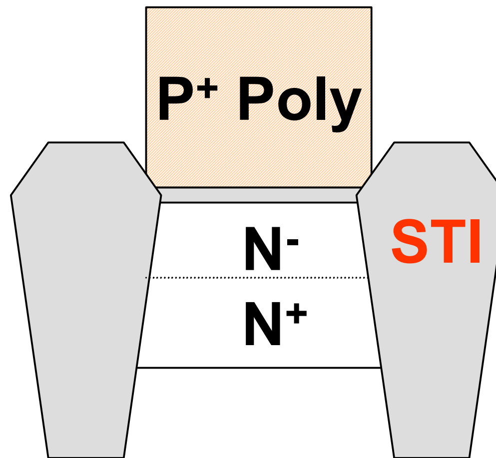


Fig.5.2 Illustration of the PREM cell structure.

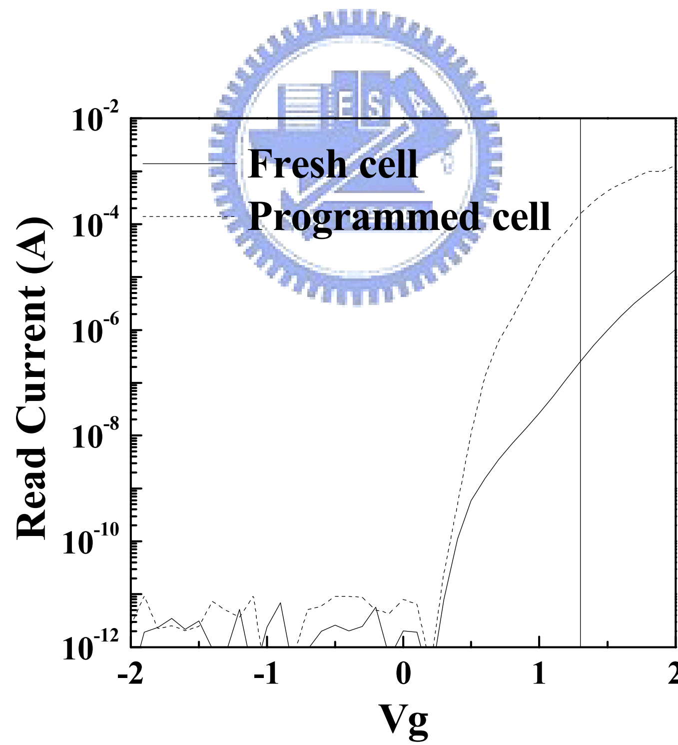


Fig.5.3 The IV characteristics of a fresh and a programmed cell (Vg=1.3V).

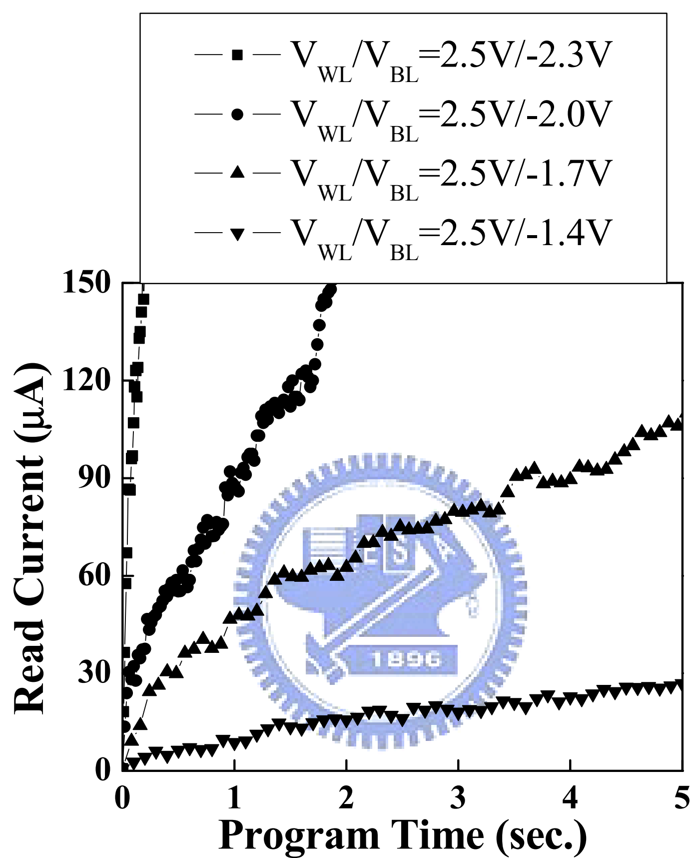


Fig.5.4 The program voltage dependence of the read current evolution in PREM cells. Four program voltages are compared: V_{WL}/V_{BL}=2.4V/-2.4V, 2.2V/-2.2V, 2.0V/-2.0V and 1.8V/-1.8V.

Table 5.1 PREM cell parameters and program/read bias conditions.

Test pattern		P-poly/oxide/N-diffusion MIS diode
Dielectric		Oxide
Physical thickness		1.4nm
Cell area		2μm^2
Program	Selected Word-line (WL)	$+V_{PGM}$ (<+2.5V)
	Selected Bit-line (BL)	$-V_{PGM}$ (>-2.5V)
	Un-selected Word-lines	-2.5V
	Un-selected Bit-lines	2.5V
Read	Selected Word-line (WL)	1.3V
	Selected Bit-line (BL)	0V
	Un-selected Word-lines	0V
	Un-selected Bit-lines	1.3V

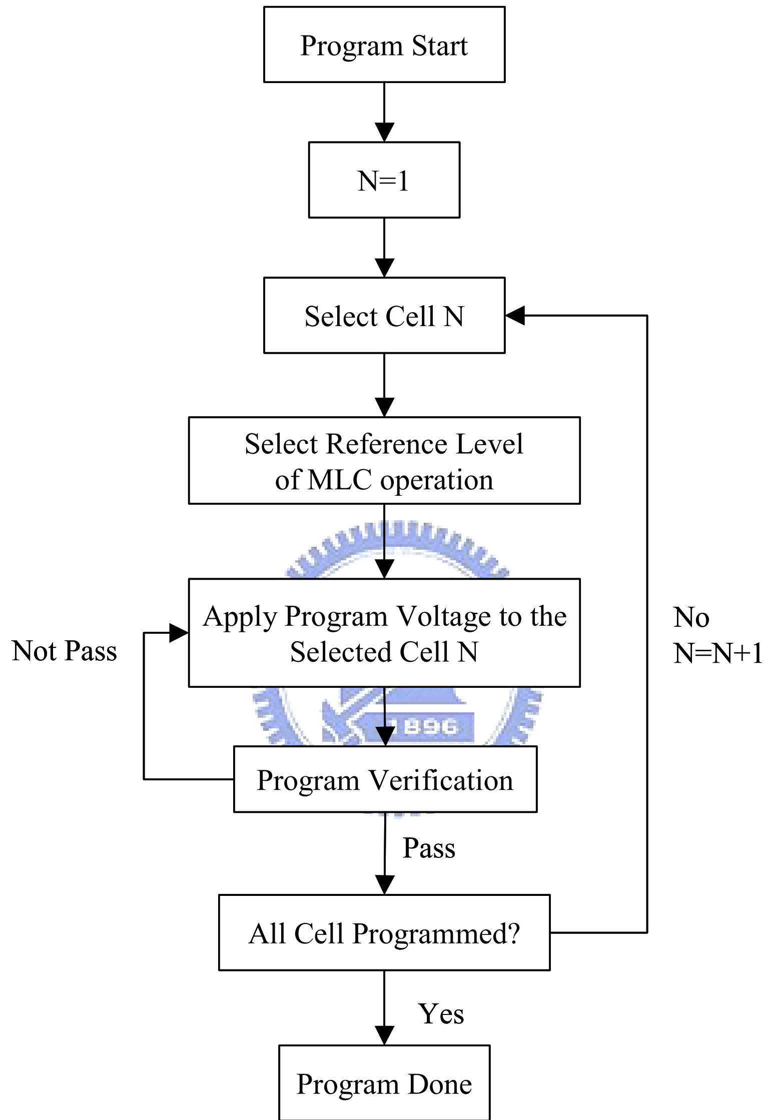
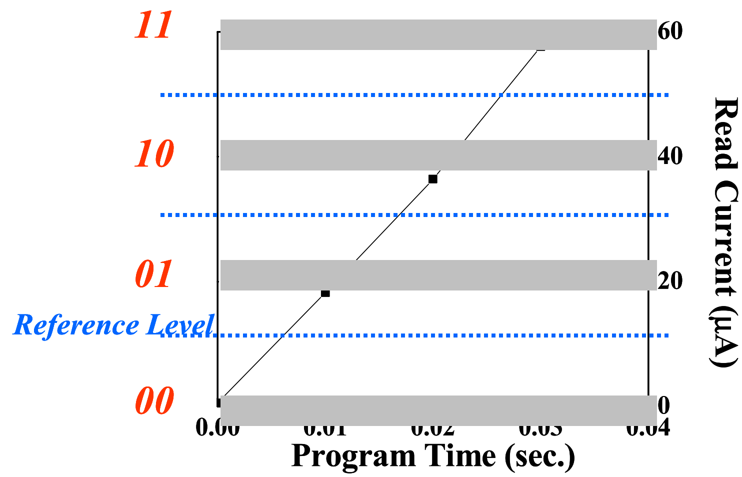
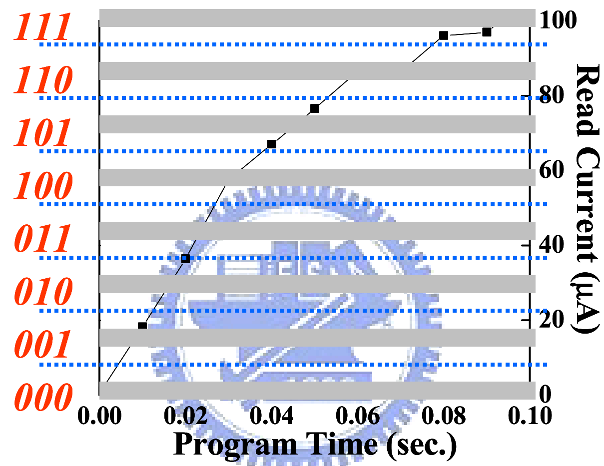


Fig.5.5 MLC program algorithm of a PREM cell.





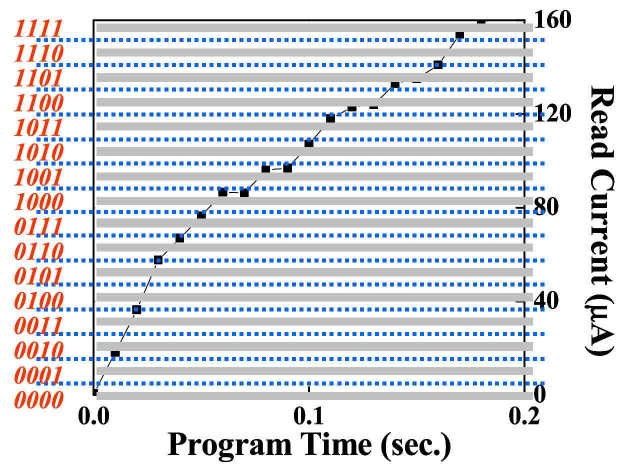


Fig.5.6 An exemplary illustration of a PREM cell to realize MLC operation. (a) 2-bits-per-cell storage. (b) 3-bits-per-cell storage. (c) 4-bits-per-cell storage.

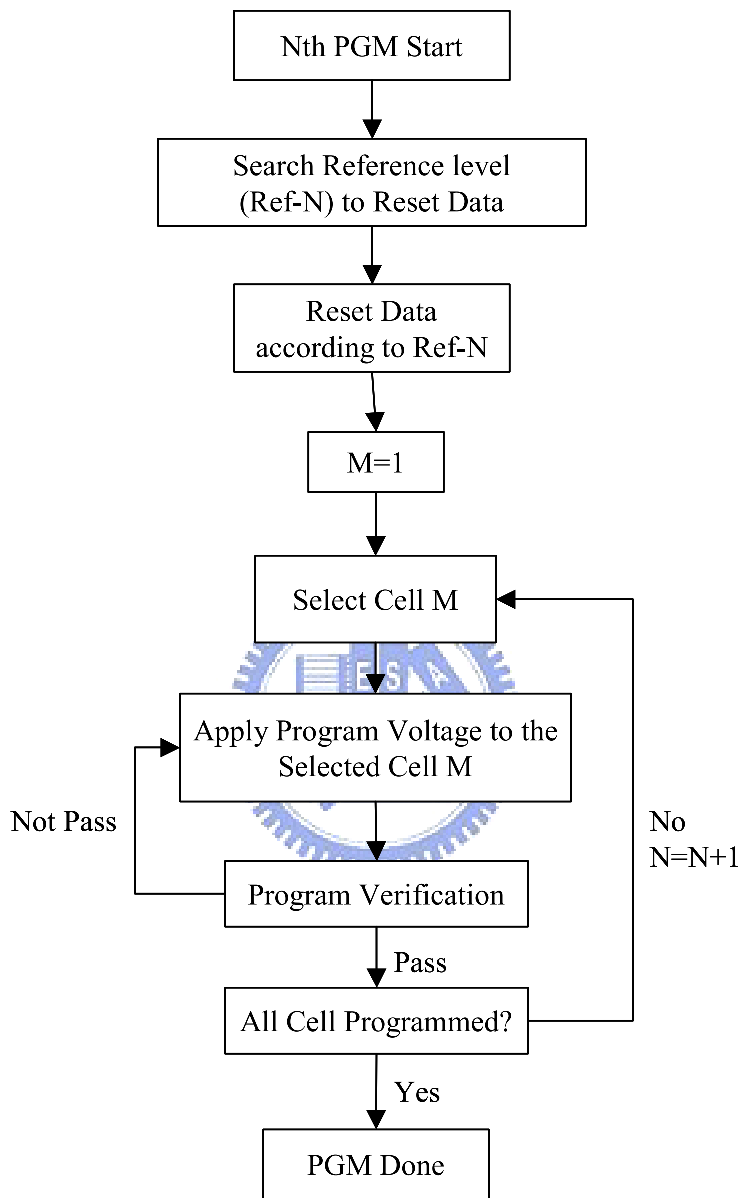


Fig.5.7 MTP program algorithm of a PREM cell

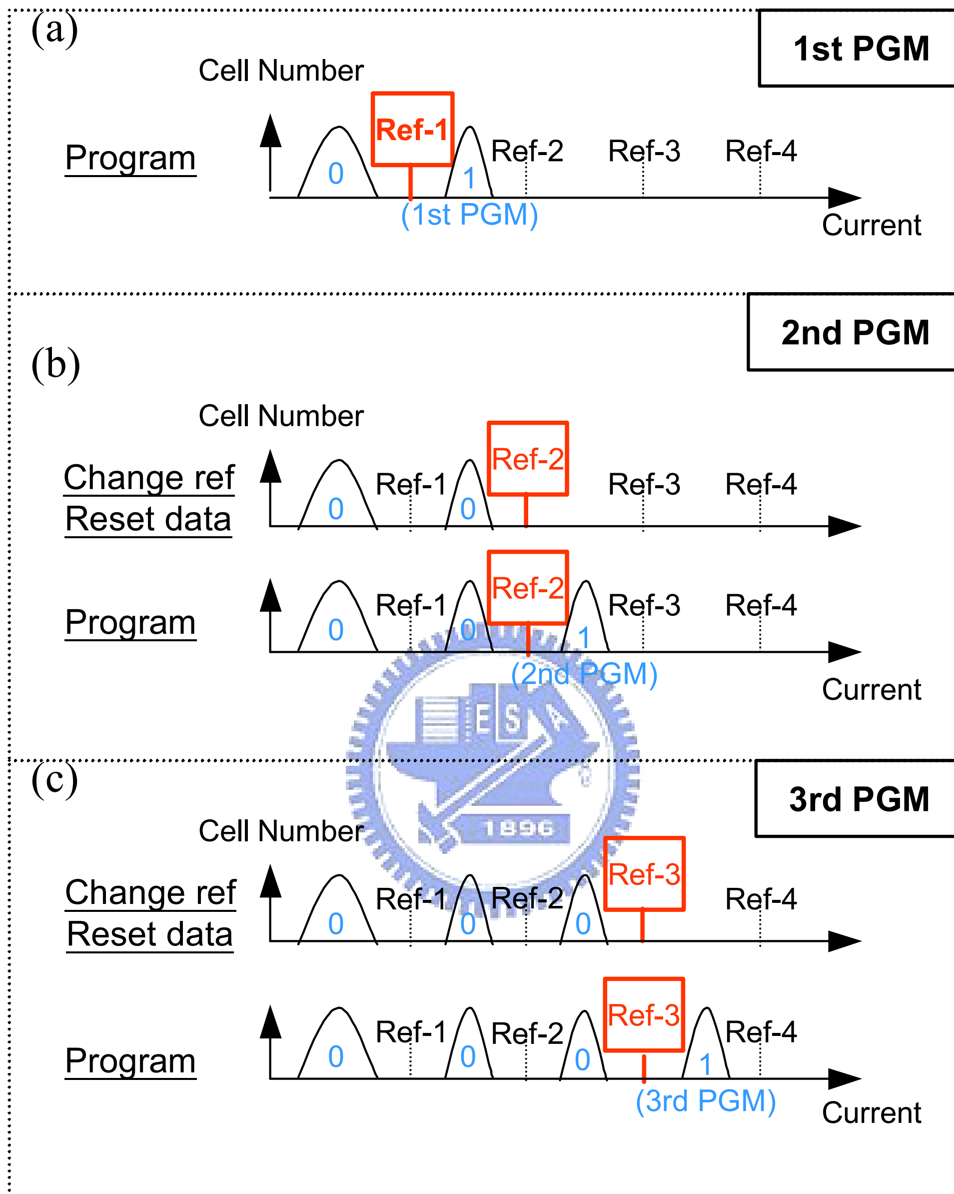


Fig.5.8 Illustration of cell distributions in (a) the 1st, (b) the 2nd, and (c) the 3rd program sequence.

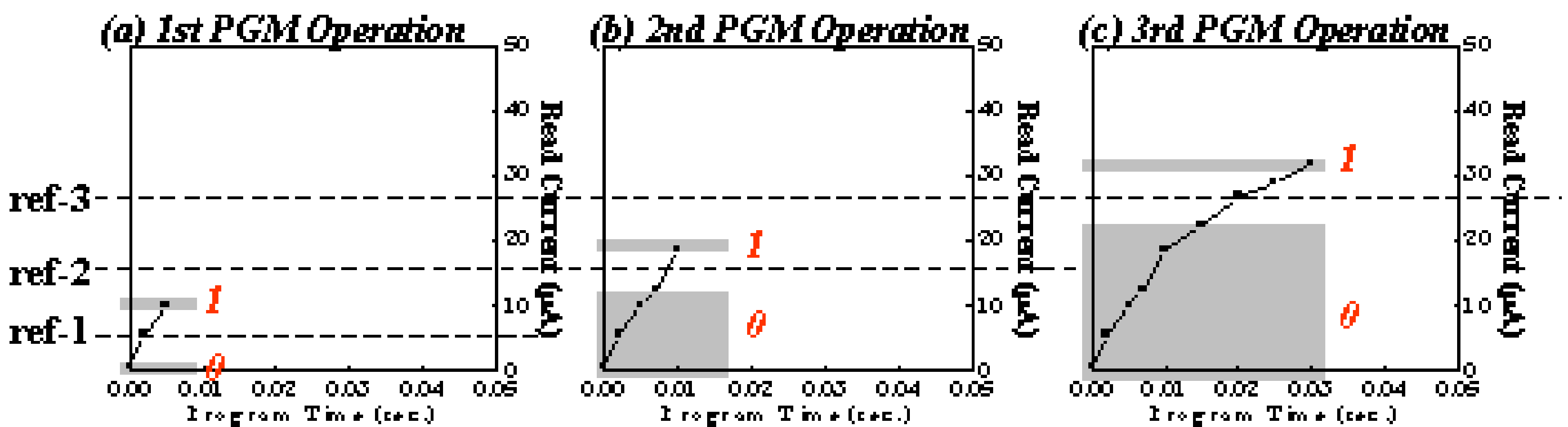


Fig.5.9 An exemplary illustration of a PREM cell to realize MTP. (a), (b), and (c) represent the schematic representations of the 1st, the 2nd, and the 3rd time program (PGM) operations. Ref-1, ref-2, and ref-3 are the reference currents for each time program operation.

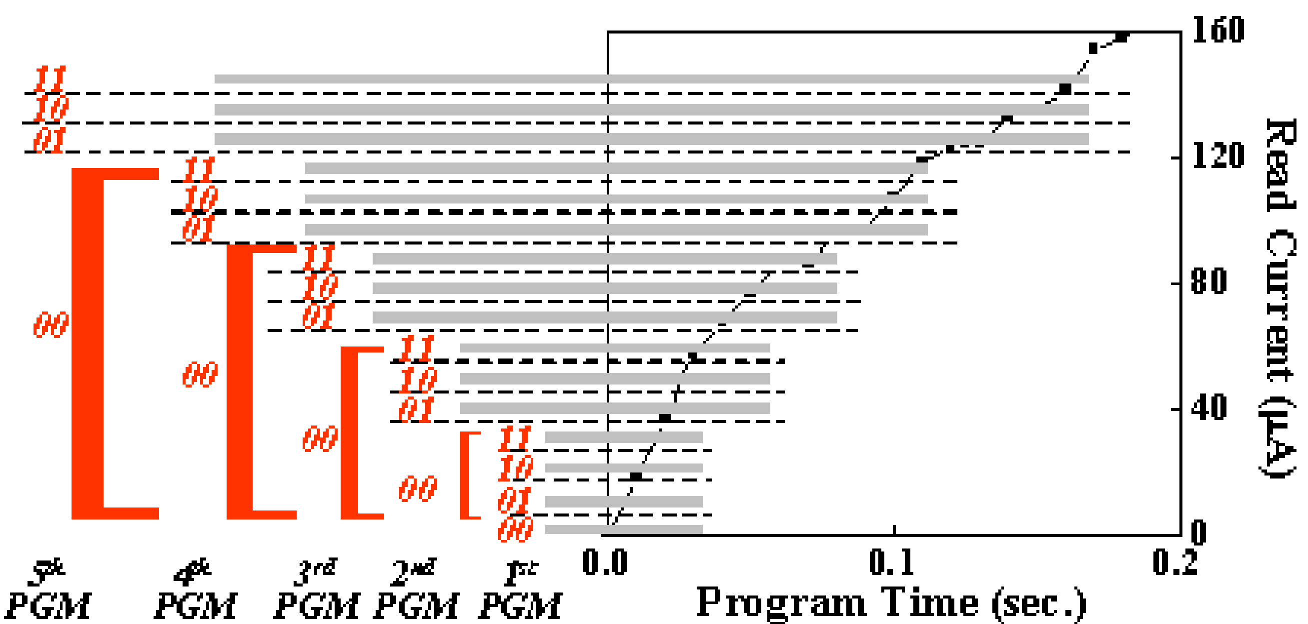


Fig.5.10 An exemplary illustration of a PREM cell to realize MTP+MLC (2-bits-per-cell storage with at least 5 programming times).

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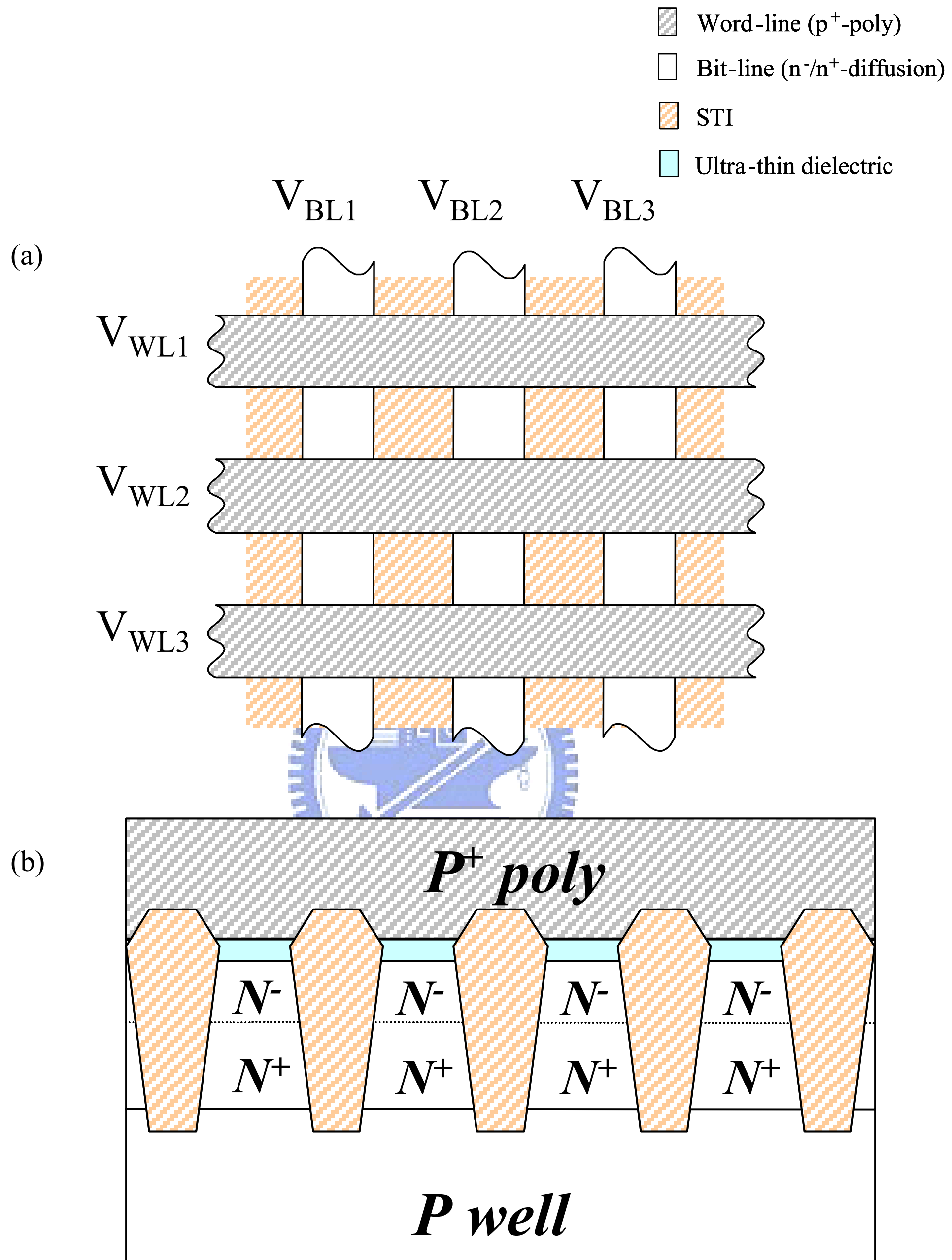

Fig.5.11 (a) Schematic representation of PREM array architecture. (b) Schematic representation of PREM cell structure. As small as $4F^2$/cell is feasible.

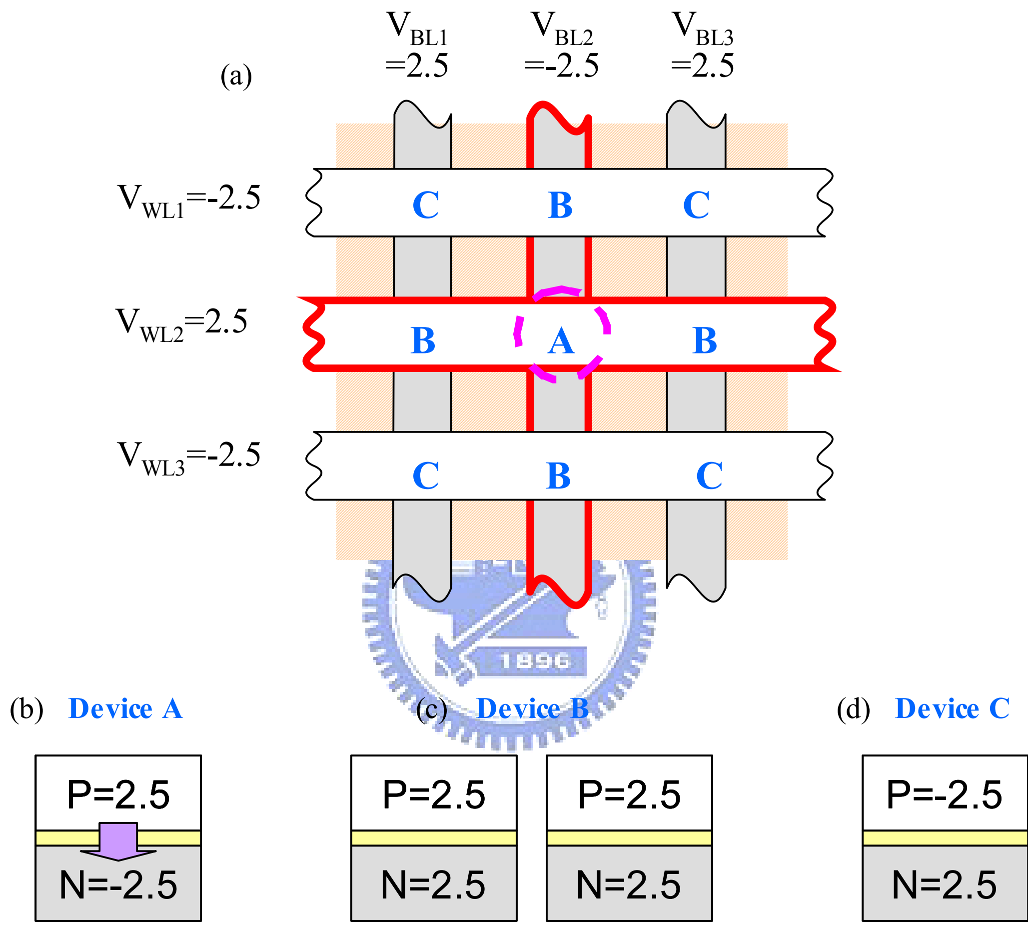

Fig.5.12 (a) The array program condition and distribution of selected device A, non-selected device B and non-selected device C. The single cell bias condition of (b) device A, (c) device B, and (d) device C.

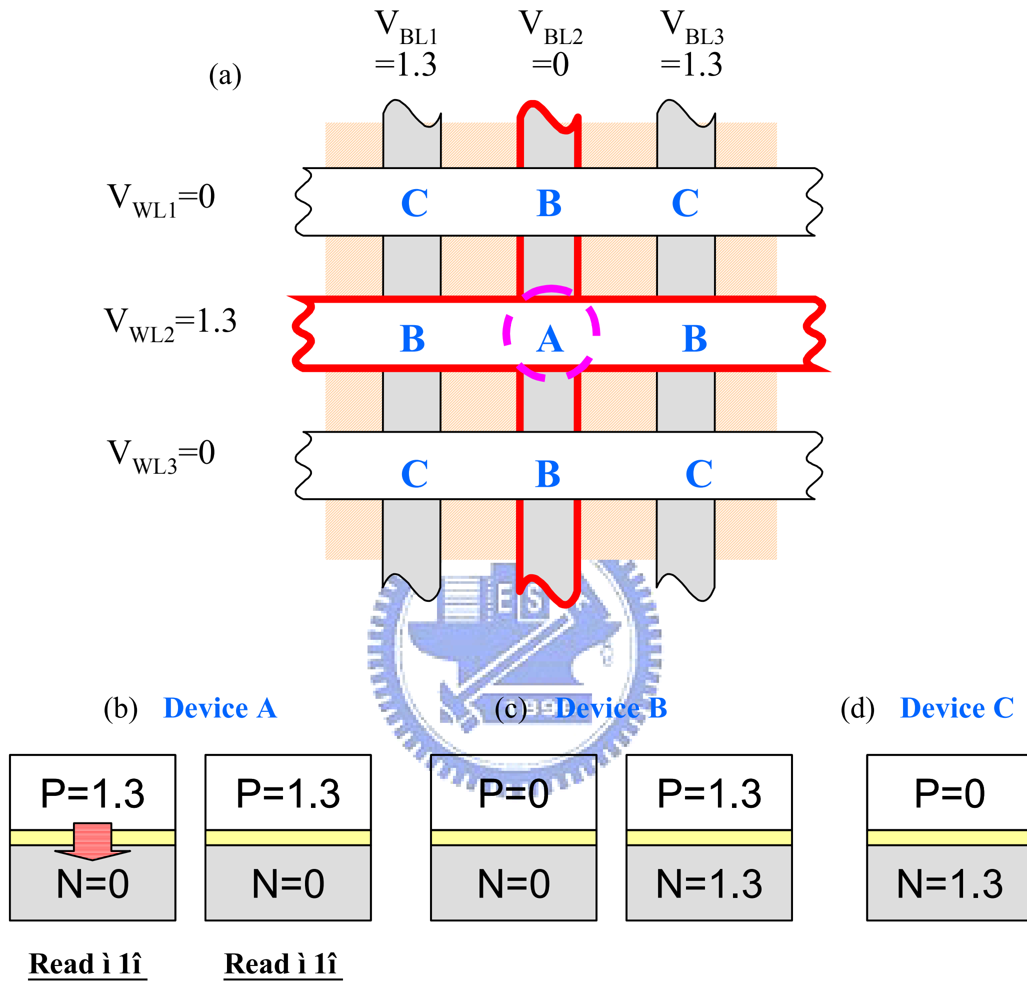

Fig.5.13 (a) The array read condition and distribution of selected device A, non-selected device B and non-selected device C. The single cell bias condition of (b) device A, (c) device B, and (d) device C.

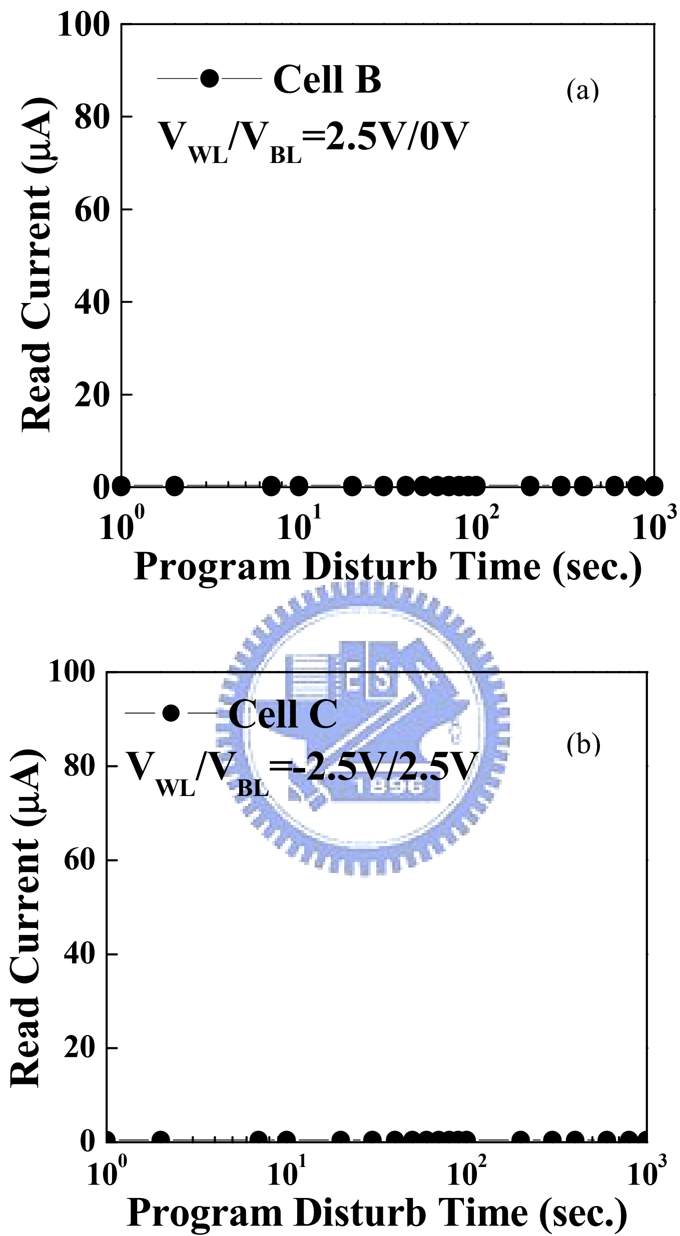

Fig.5.14 The program disturbance characteristics of (a) device B, and (b) device C at the temperature of 25C.

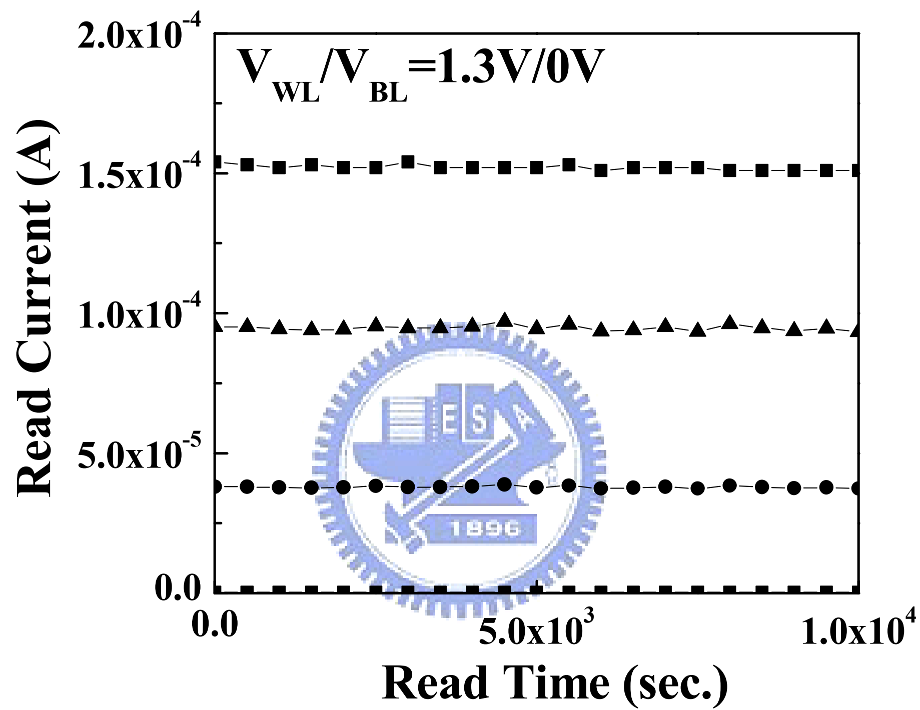

Fig.5.15 The read disturbance characteristics of four programmed levels. The disturbance condition is V_{WL}/V_{BL}=1.3V/0V at the temperature of 25C.

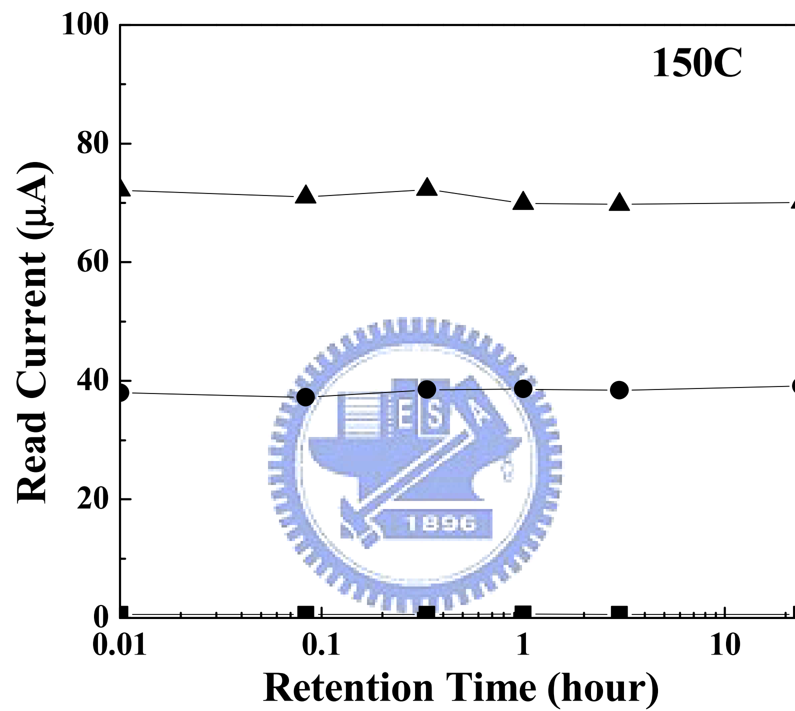

Fig.5.16 The cell retention characteristics of three programmed levels. The bake temperature is 150C.

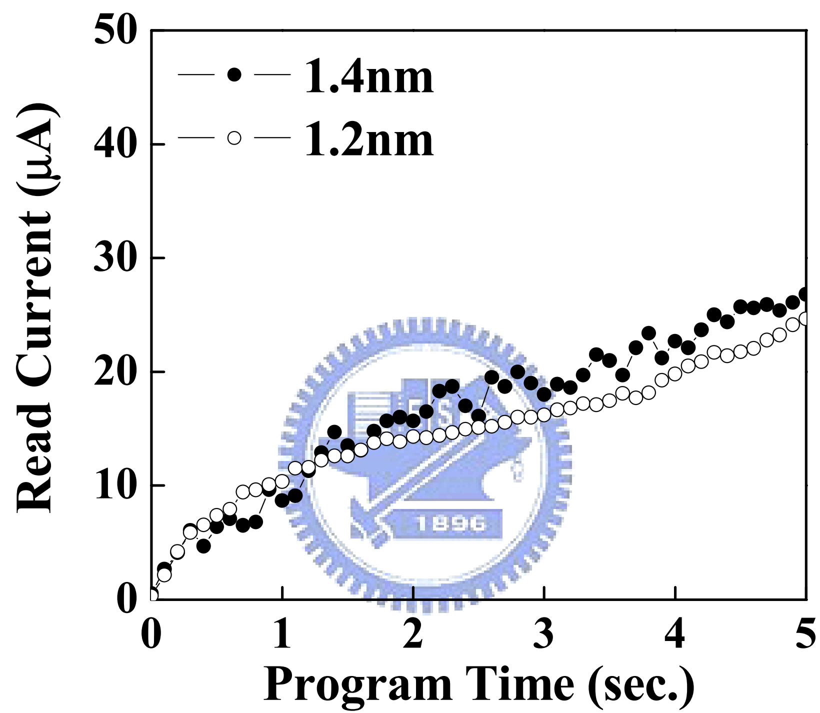

Fig.5.17 The program behavior of two PREM cells with 1.4nm and 1.2nm oxide films.

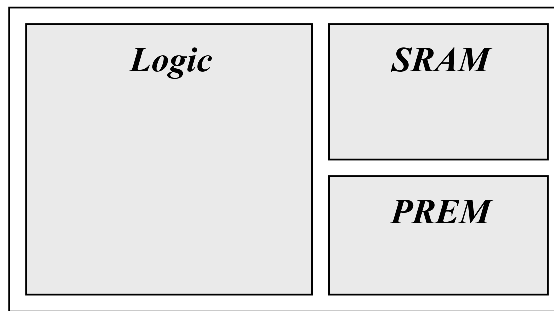

Fig.5.18 The illustration of logic circuits with embedded SRAM and PREM for SOC applications.

Table 5.2 Summary of embedded memory cells.

Memory	Floating gate memory (embedded)	Oxide-BD OTP	SRAM	PREM
Process	Complex	Simple	Simple	Simple
	Not CMOS compatible	CMOS compatible	CMOS compatible	CMOS compatible
Volatility	Non-volatile	Non-volatile	Volatile	Non-volatile
Operation Voltage	High	Low	Low	Low
	Need HV transistors	General I/O transistors	CMOS transistors	General I/O transistors
Program cycles	100k	1	∞	10~100
Cell size	1T	1T	4~6T	1T
Bit/cell	1~2	1	1	1~4

Chapter 6

A novel Silicon-Nitride based Light-Emitting Transistor (SiNLET) for Display and Optical Communications

6.1 Introduction

Recently, light emission from heterojunction bipolar light-emitting transistors (HBLET) has received much attention for optical interconnects [6.1-6.2]. HBLET uses the graded base layer of InGaP/GaAs heterojunction for the radiative recombination, and the modulations of light emission in phase with the base current modulated in transistor operation at 1MH$_Z$ are demonstrated. HBLET can possibly overcome the speed limitation of conventional electrical interconnects; however, its process is incompatible to standard CMOS devices, which narrows the applications. Although silicon-based light-emitting devices suffer lower light emission efficiency due to the in-direct band-gap of silicon, their applications are numerous due to the ease of integration in silicon-based ultralarge scale integrated circuit (ULSI). Many attempts including p-n diodes [6.3], MIS diodes [6.4-6.6], porous silicon [6.7], and nanocrystal LEDs [6.8-6.10] have been reported for electro-optics applications based on silicon technologies.

In this chapter, we develop a novel silicon light-emitting transistor called SiNLET (Silicon-Nitride based Light-Emitting Transistor), which is based on standard silicon process, triple-well technology and a SONOS-type device structure. The optical and electrical properties are characterized. Here, we only demonstrate the main idea of SiNLET. The ONO thickness, device size, operation condition, and manufacturing process have not been optimized.

6.2 SiNLET Device Structure and Operation Principles

6.2.1 SiNLET Device Structure

As shown in Fig.6.1, SiNLET uses a poly-silicon/oxide/nitride/oxide/ silicon-substrate structure for light emission and contains three terminals: poly, n^+ junction, and p-well. The ONO thickness is 9nm, 7nm and 6nm from top to down. Bottom oxide and top oxide use thermal oxidation and nitride uses CVD deposition. The layout of the test device is shown in Fig.6.2 and the effective device area of light emission is around $0.616\mu m^2$.

6.2.2 SiNLET Operation Principles

The bias condition of SiNLET is shown in Fig.6.1, and the band diagram is illustrated in Fig.6.3. As we apply a negative bias (Ve=-16V) on the poly and a positive bias (Vh=5.8V) on the n^+ junction with a grounded P-well (Vc=0), electrons (FN-E) will inject into the nitride from the poly via Fowler-Nordheim tunneling. Meanwhile, band-to-band tunneling induced hot holes (BTBT-HH) from the n^+ junction will also inject into the nitride via jumping over the bottom oxide barrier. As shown in Fig.6.3, FN-E and BTBT-HH will be captured by nitride traps or recombine with the trapped carriers. Photons will be emitted by the energy relaxation process via carrier scattering, carrier trapping and carrier recombination [6.5].

6.2.3 Light Spectrum and CCD Image

Fig.6.4 (a) and (b) show the light spectrum and CCD image of SiNLET, respectively. SiNLET shows peak intensity at the wavelength of around 700nm (~1.8eV), and its light spectrum contains infrared ray and visible ray (1100nm ~ 400nm). To further investigate the detail of SiNLET, the light spectrums of several bias conditions and device structures are compared. As shown in Fig.6.4, if we just apply a negative bias on the poly with FN-E supply only, no light emission is observed. Similar result is obtained as we only supply BTBT HH without electron injection. When a MOS structure without nitride traps is used to replace the SONOS structure, we still donít observe light emission (see Fig.6.4 (a) and (c)).

Fig.6.5 compares the light spectrums of a reverse-biased junction and a forward-biased junction. In the reverse-biased junction, a shorter wavelength and lower current consumption are obtained, which results from the scattering, trapping, and recombination of high energetic electrons and holes via nitride traps. In contrast, the forward-biased junction functions as a pure p-n-junction LED, and shows peak intensity at around 1000nm. The photon energy is around 1.2eV, which should be caused by the electron/hole pair recombination in the bulk substrate via silicon band-gap. Table 5.1 summarizes the results of light emission in various bias conditions and device structures. High energetic electrons, hot holes and nitride traps (quantum dots for carrier scattering, trapping and recombination) are essential for SiNLET to emit high energetic photons.

6.3 Electrical and Optical Properties

Fig.6.6 (a) and Fig.6.7 (a) show the light spectrum of SiNLET operated in different Ve and Vh. Higher Ve or Vh shows larger output light intensity due to the increased input vertical and lateral electrical field. Fig.6.6 (b) and Fig.6.7 (b) show the supply current from the n^+ junction to the p-well (Ih=-Ic), which is induced by band-to-band tunneling. In the normal operation condition, the current from the poly

is negligible ($Ie<10^{-13}$ A/μm^2). High light emission efficiency can be achieved by a low supply current (<10^{-7}A/μm, compare to p-n junction in Fig.6.5) in SiNLET.

SiNLET can function as a three-terminal light-emitting transistor as shown in Fig.6.8. The poly (Ve) and n^+ junction (Vh) serves as the Source and the Drain to supply electrons and holes, respectively. The control voltage (Vc) in the p-well can control the lateral electrical field to modulate the output light intensity, which serves as the Gate. Fig.6.9 shows the output light intensity versus the supply current, and they have nearly linearly dependence. Fig.6.10 shows the output light intensity as a function of Vc. Fig.6.11 demonstrates the characteristics of output light intensity as a function of input Ve and Vh. The threshold voltage of Vc is around 2V to switch SiNLET. Fig.6.12 shows the voltage stress effect on SiNLET. After continuously stress for 10 hours, a little degradation of light intensity is observed, which should result from the stress induced deterioration of the ONO film. The wavelength of peak intensity after electrical stress is still 700nm.

6.4 Conclusion

We have reported a novel SiNLET with high light emission efficiency and low current consumption (<10^{-7}A/μm) in a small device area (~0.616μm^2), and its process is compatible to standard CMOS. SiNLET shows peak intensity at around 700nm, and its light spectrum contains infrared and visible light. SiNLET can modulate the output light intensity by controlling the input voltages, and functions as a light-emitting transistor. SiNLET can be integrated with CMOS devices easily as shown in Fig.6.13 and has demonstrated its high feasibility for the application of optical interconnects in ULSI.

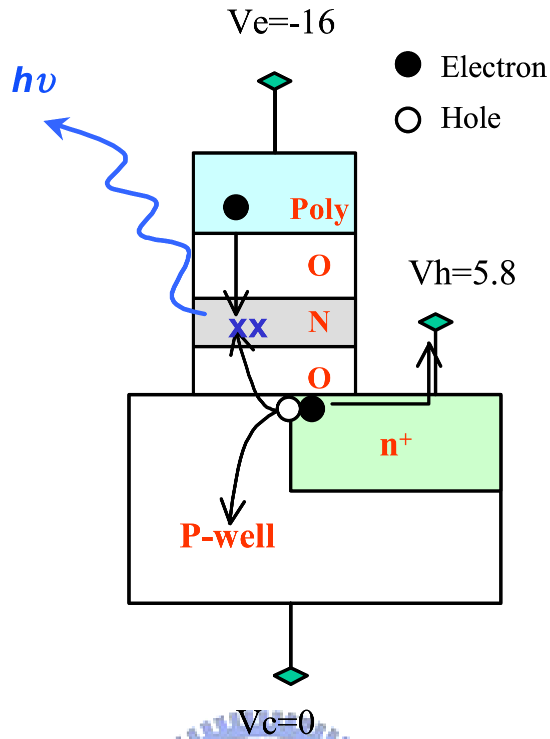

Fig.6.1 The device structure of SiNLET. ONO thickness is 9, 7, and 6nm from top to down.

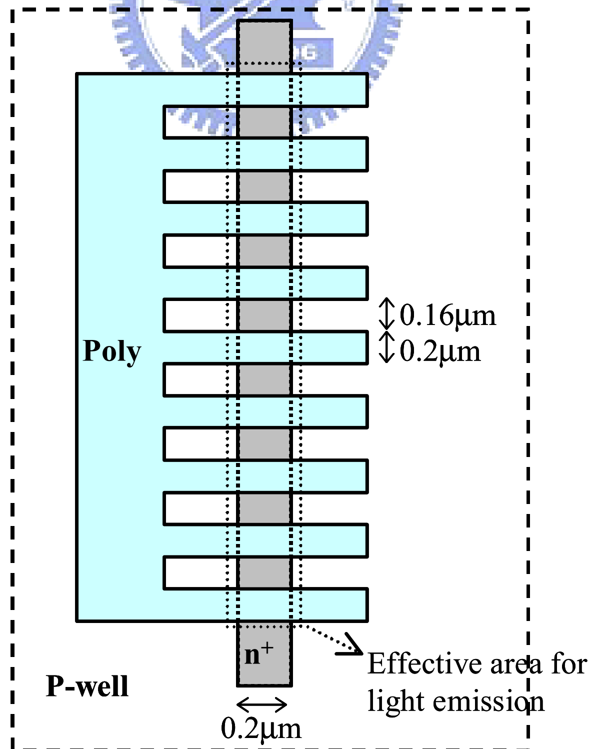

Fig.6.2 Layout of SiNLET test device.

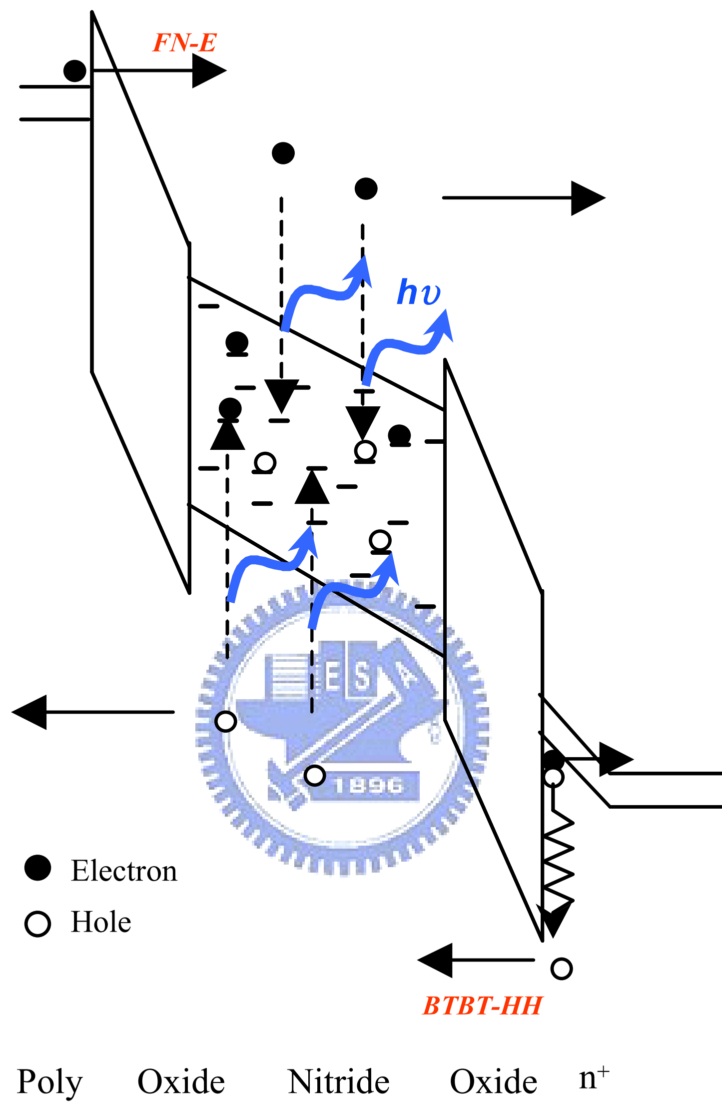

Fig.6.3 Schematic representation of the band diagram of SiNLET in the operation condition of light emission.

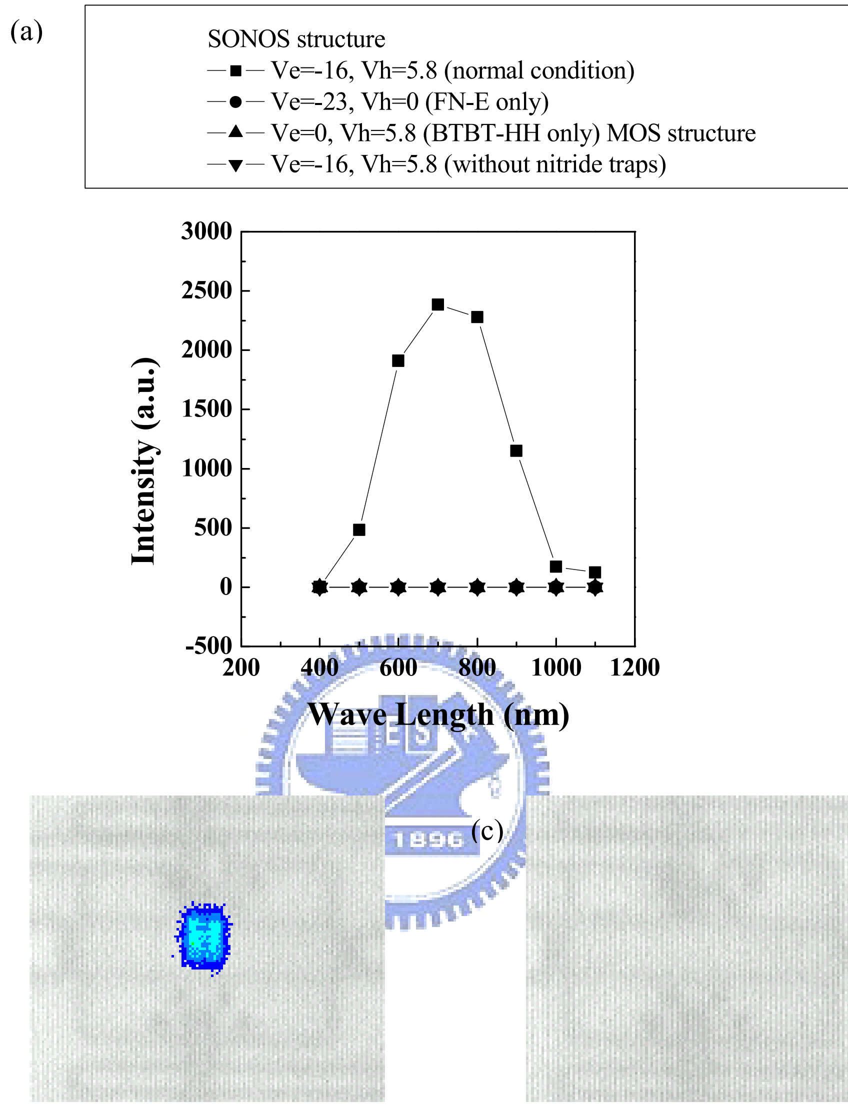

Fig.6.4 (a) Light spectrum of various bias conditions and device structures. Squares represent the spectrum of the normal operation condition of SiNLET. Circles and up-triangles represent the spectrum with FN-E supply only and BTBT-HH supply only in SONOS structure, respectively. Down-triangles represent the spectrum of the normal operation condition in MOS structure (oxide thickness is 18nm). (b) CCD image of SiNLET in the normal operation condition. (c) CCD image of MOS structure in the normal operation condition (Vc/Ve/Vh=0/-16/5.8).

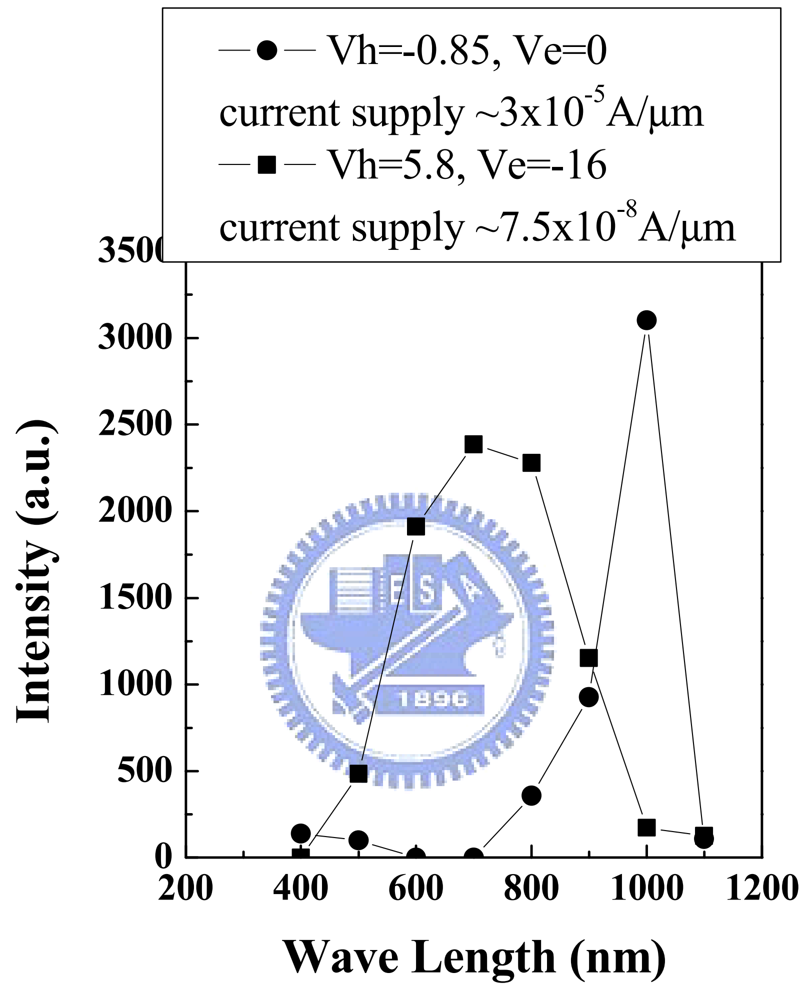

Fig.6.5 Light spectrum of SiNLET in the operation condition of forward-biased junction (circles) and reverse-biased junction (squares). Reverse-biased junction shows shorter wavelength and higher photon energy, and the supply current is 3 orders less than the forward-biased junction.

Table 6.1 Summary of various test-bias conditions and test-device structures in Fig.5.4 and Fig.5.5.

	Normal condition	Electron only	Hot hole only	Without nitride	Forward junction
Vh	5.8	0	5.8	5.8	-0.85
Ve	-16	-23	0	-16	-16 or 0
Vc	0	0	0	0	0
Structure	SONOS	SONOS	SONOS	MOS	SONOS
Photon Emission	O	X	X	X	O
Peak intensity	700nm				1000nm

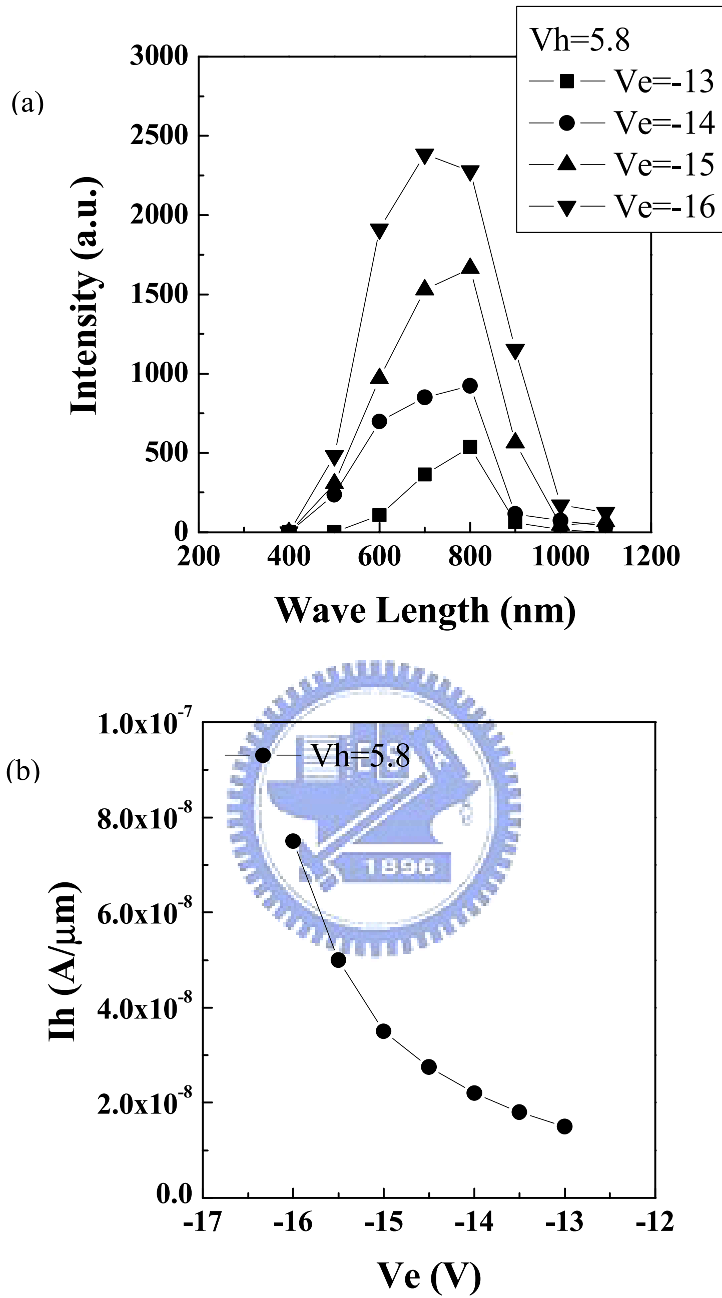

Fig.6.6 (a) Light spectrum of SiNLET in various Ve (Vh=5.8V). Higher Ve shows larger intensity. The peak intensity is at 700~800nm in all conditions. (b) The supply current (Ih) versus the operation voltage of poly (Ve) with a constant Vh of 5.8V. In all bias conditions, the current at n^+ junction is equal to p-well (Ih=Ic) and the current at the poly (Ie) is negligible.

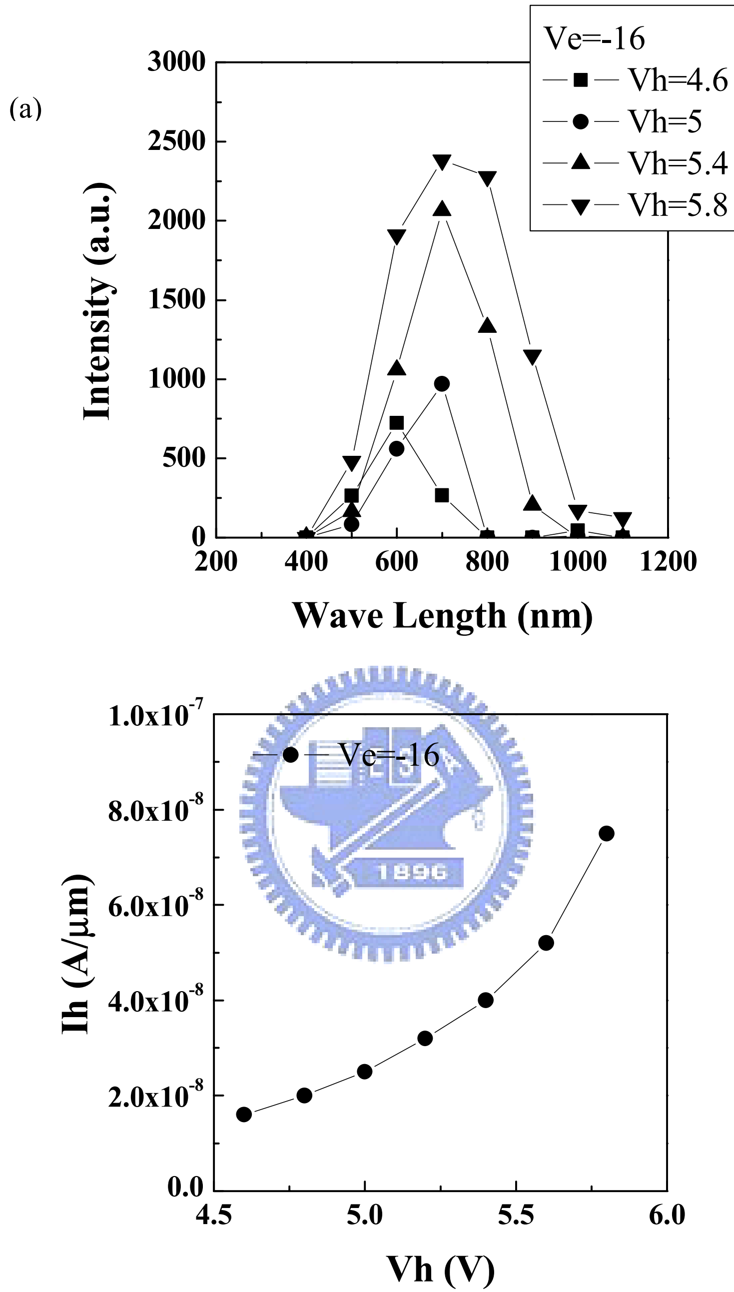

Fig.6.7 (a) Light spectrum of SiNLET in various Vh (Ve=-16V). Higher Vh shows larger intensity. The peak intensity is at 600~700nm in all conditions. (b) The supply current (Ih) versus the operation voltage of n^+ junction (Vh) with a constant Ve of -16V. In all bias conditions, the current at n^+ junction is equal to p-well (Ih=Ic) and the current at the poly (Ie) is negligible.

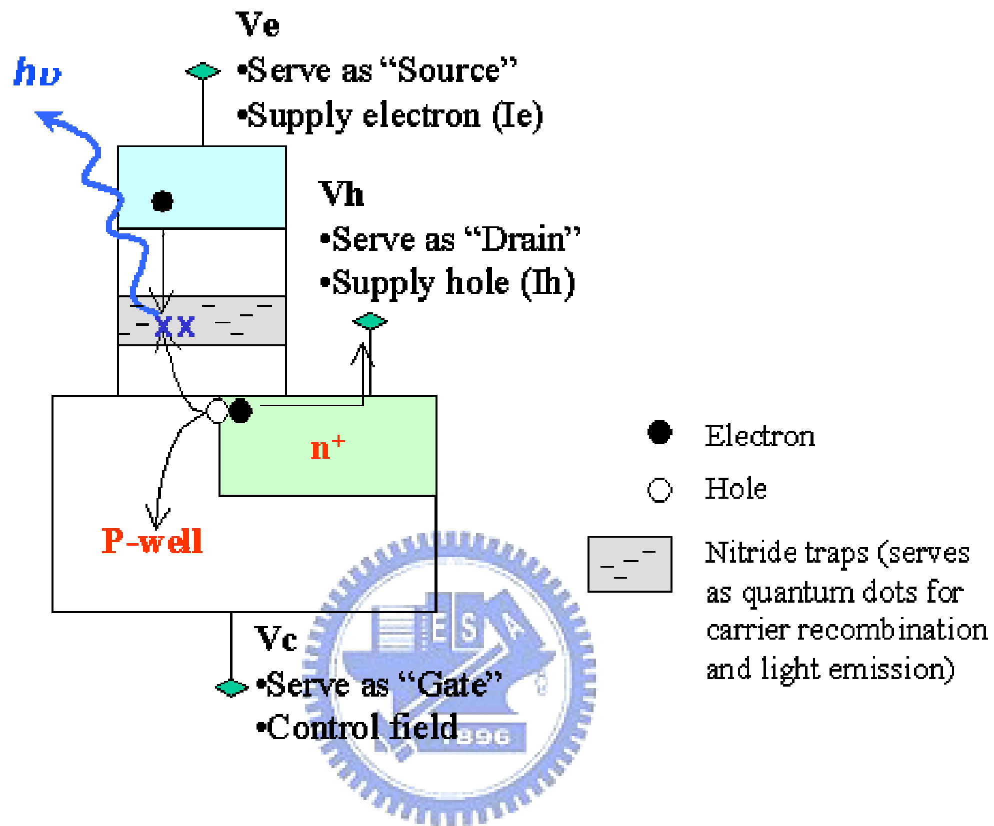

Fig.6.8 Schematic illustration of SiNLET to function as a three-terminal transistor. The poly supplying electrons serves as the Drain. The n^+ junction supplying holes serves as the Source. The p-well controlling the lateral field serves as the Gate. The nitride traps serve as quantum dots for carrier trapping and recombination.

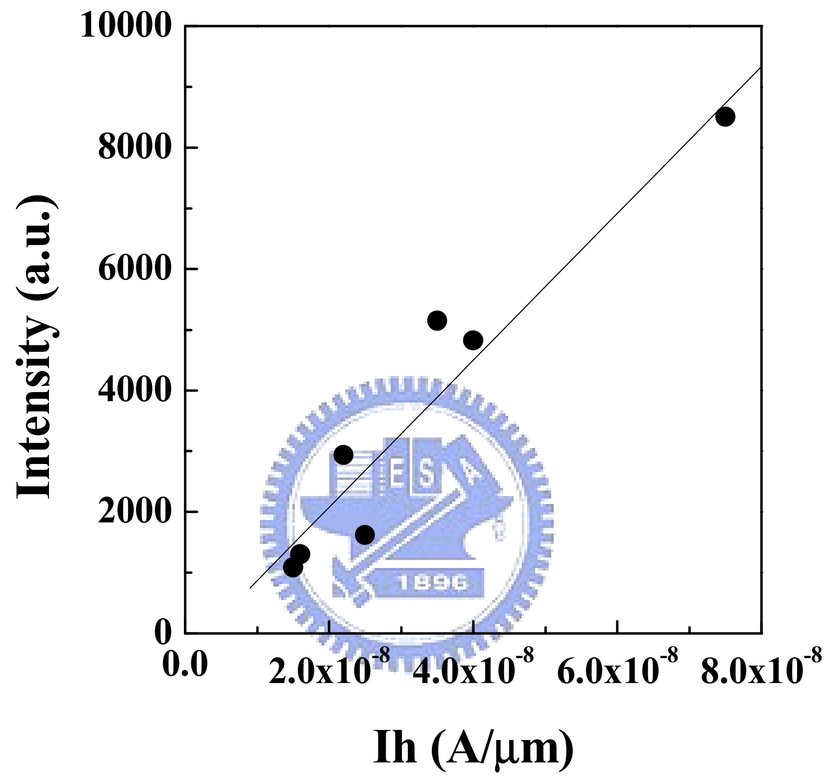

Fig.6.9 The supply current density versus output light intensity. The data are extracted from Fig.5.6 and Fig.5.7.

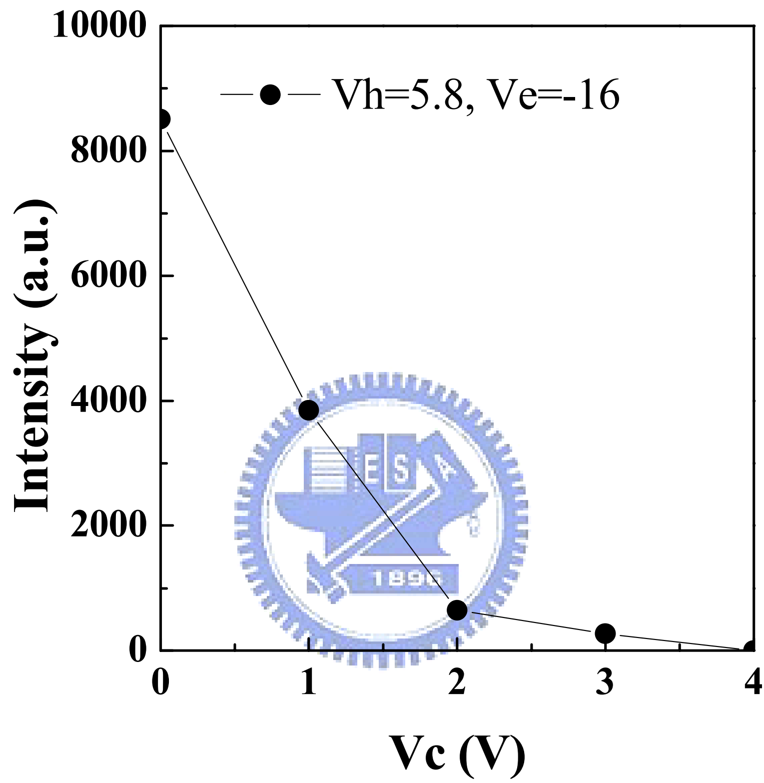

Fig.6.10 The light intensity as a function of Vc (Vh=5.8V, Ve=-16V). The threshold voltage of Vc is around 2V to switch SiNLET.

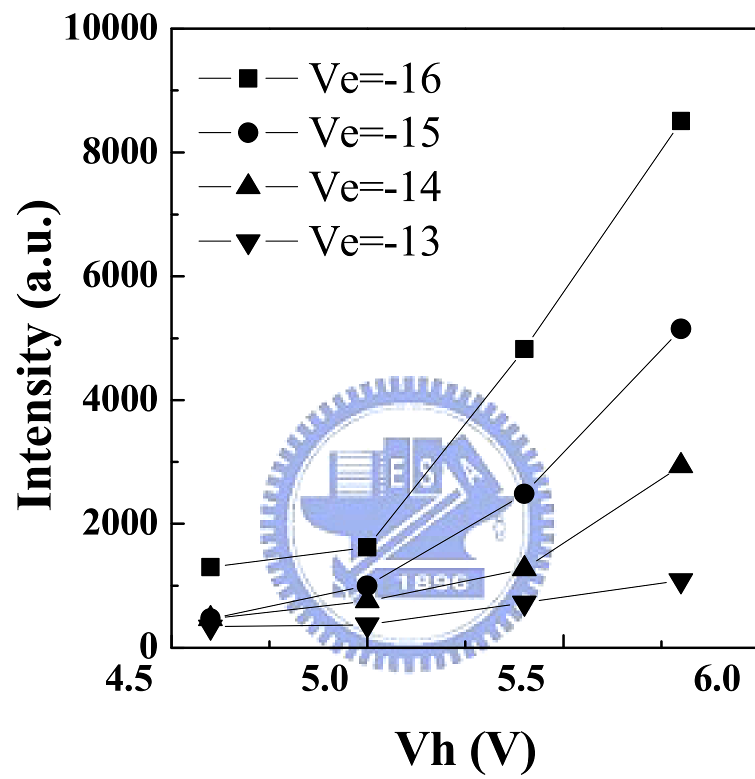

Fig.6.11 The light intensity as a function of Ve and Vh (Vc=0V).

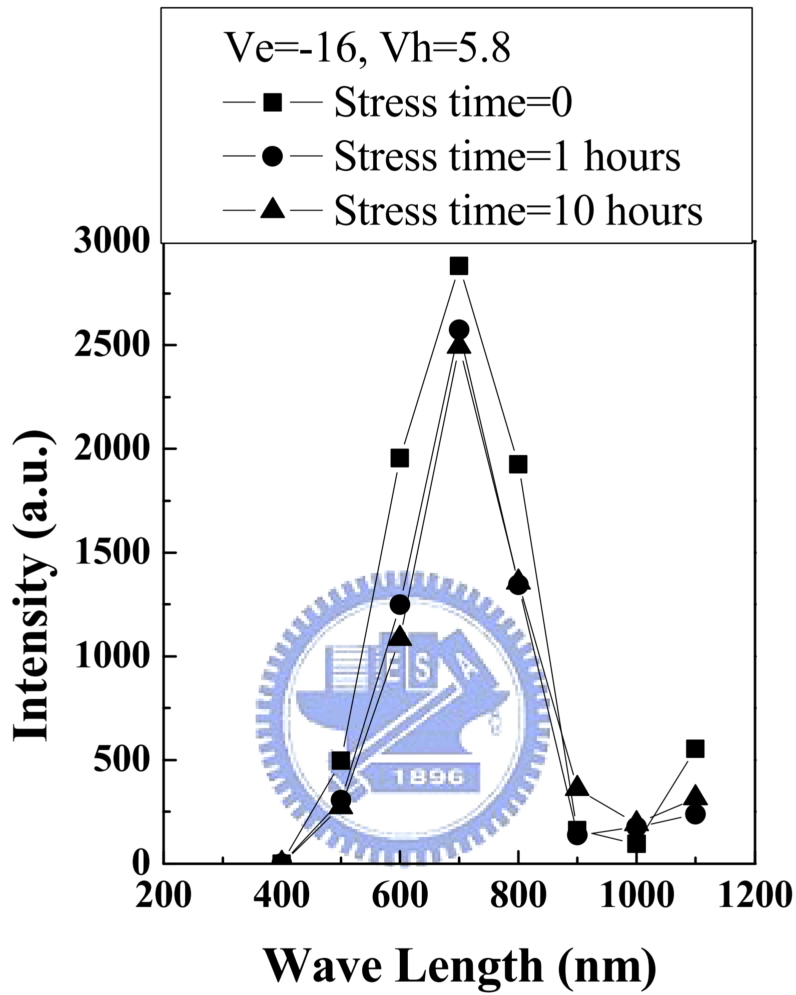

Fig.6.12 The light spectrum before and after stress. The stress condition and light emission measurement condition are both Vc/Ve/Vh=0/-16/5.8V.

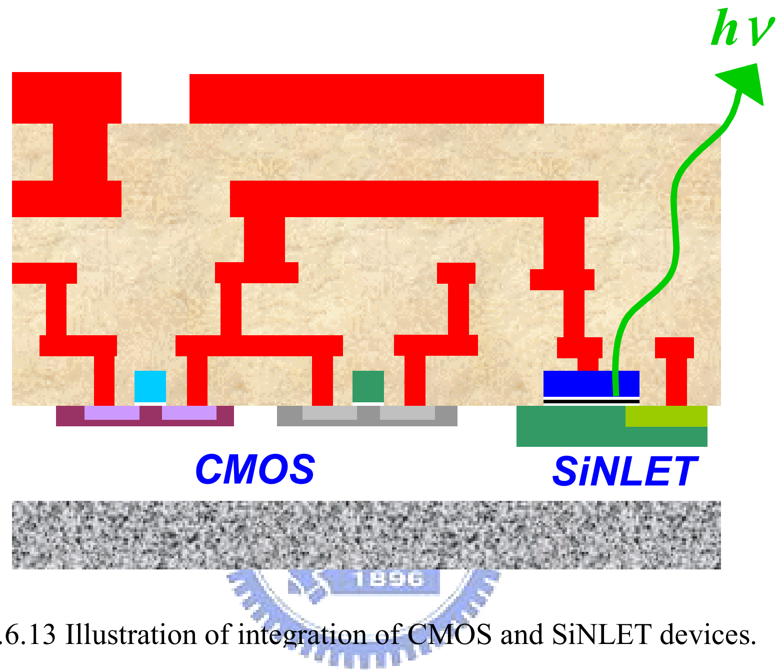

Fig.6.13 Illustration of integration of CMOS and SiNLET devices.

Chapter 7

Conclusion

We investigated a novel flash memory cell named PHINES (Programming by hot Hole Injection Nitride Electron Storage). PHINES uses a nitride trapping storage cell structure. Channel FN erasing is performed to raise Vt while programming is done by lowering local Vt through band-to-band hot-hole injection. PHINES uses backward read scheme with low power program/erase operation, and physically 2-bits-per-cell storage is achieved. PHINES cell also shows good retention and cell reliability and can be arranged in both NOR-type and NAND-type array architectures for code flash and data flash applications.

However, PHINES cell suffers the issue of 2-bit interaction due to the backward read scheme. Two-bit interaction effect caused by the local storage carriers and the DIBL will result in the reduction of the Vt operation window. The effects of the charge profile on the Vt operation window are also studied and characterized. Although a narrower electron distribution, higher electron storage density, better program/erase algorithms, and a lower read-Vd can be used to increase the operation window, 2-bit interaction effect can not be eliminated completely and will get worse in a scaled device. To overcome this issue, a novel BTB sensing scheme and a new modified NAND-type array are introduced in chapter 3. Since BTB current is generated locally between the drain (or source) and P-well, the sensing currents of two bits are independent and will not affect each other. BTB-PHINES eliminates the 2-bit interaction effect and a large operation window can be obtained by BTB sensing scheme. We also construct a novel modified NAND-type array to realize 2-bits-per-cell operation and high-density storage. BTB-PHINES memory cell demonstrates a fast cell programming speed (≦60μs) with a low programming current (≦100nA/cell), and a high programming throughput can be achieved. Besides, the sensing current shows weak temperature dependence, and good cell reliability is demonstrated.

In chapter 4, we compare the scaling challenges of PHINES and floating gate technologies. PHINES technology can achieve compatible performance and bit size to floating gate technologies for most data flash memory applications. According to our evaluations, 1-bit PHINES suffers the scaling challenges of few storage carriers, inter-WL leakage/breakdown, and cell punch beyond 15nm CMOS generation. Two-bit PHINES suffers scaling challenges of the distribution of a programmed bit, 2-bit interaction effect, and few storage carriers beyond 30nm generation. Compared

to the conventional floating gate memory cells, PHINES memory cell shows high scalability, and 15nm generation for 1-bit-per-cell storage and 30nm generation for 2-bits-per-cell storage are feasible in NAND-type array architecture.

In chapter 5, a novel non-volatile memory cell named PREM (Programmable Resistor with Erase-less Memory) is constructed for SOC and embedded flash memory applications. Instead of the conventional ì eraseî operation, PREM adjusts the reference level to reset the data. By utilizing the progressive breakdown of ultra-thin oxide and the new ì Erase-lessî operation, PREM can realize MTP and/or MLC. Only one extra or none mask is needed with CMOS standard process. No degradation of cell retention, no program disturbance, and no read disturbance are observed, and the cell reliability is guaranteed. PREMís low voltage operation, high scalability and simple process are superior for SOC or very low cost and high-density storage applications.

In chapter 6, we reported a novel SiNLET (Silicon-Nitride based Light-Emitting Transistor) with high light emission efficiency and low current consumption ($<10^{-7}$A/μm) in a small device area (~0.616μm^2). This three-terminal electroluminescence device uses a SONOS-type device structure, and its process is compatible to standard CMOS devices. Photons are generated by Fowler-Nordheim electron tunnel-injection, band-to-band tunneling induced hot-hole injection, and carrier scattering/trapping/recombination via nitride traps. SiNLET shows peak intensity at around 700nm, and its light spectrum contains infrared and visible light. SiNLET can modulate the output light intensity by controlling the input voltages, and functions as a light-emitting transistor. SiNLET has demonstrated its high feasibility for the application of optical interconnects in ULSI.

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Vita

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博士論文題目:

新型 PHINES 和 PREM 快閃記憶體及氮化矽型發光電晶體之研究

Investigation of Novel PHINES and PREM Flash Memories and Silicon Nitride-Based Light Emitting Transistor

Publication List

(A) Journal Papers:

3 點 A 類國際性期刊(長文)

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