國立交通大學

電子工程學系 電子研究所

碩士論文

應用於微瓦特動態電壓與頻率調節系統設計中近/次臨界電壓具製程電壓溫度能力之感測器

Near-/Sub-threshold PVT Sensors for Micro-Watt DVFS System Design

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摘　　要

在本篇論文中，我們將目標放在設計並實現一個應用於微瓦特動態電壓與頻率調節系統設計中具製程電壓溫度能力之感測器。其中包含自動補償全數位之製程電壓溫度感測器、多臨界電壓互補式金屬氧化層半導體(MTCMOS)之交換式電容直流-直流轉換器、具數位溫度補償之低電壓鎖相迴路頻率產生器、動態電壓與頻率調節系統。主要的研究成果如下：

1. 提出了一個可以操作在近臨界/次臨界電壓的全數位溫度感測器，具備有高精準度、電壓小、耗電低、自動補償等優點。
2. 提出了一個利用可調性脈衝寬度產生器去自動補償溫度感測器受電壓製程影響且可以操作在近臨界/次臨界電壓的數位溫度感測器，具備有高精準度、電壓小、耗電低等優點。
3. 在本篇論文中提出了一個可應用於微瓦特系統中具製程電壓溫度感知的動態電壓與頻率調節系統。本系統透過交換式電容直流-直流轉換器可以提供非常穩定直流電源，產生不同的電壓位準透過動態電壓轉換電路做電

壓調節。並且透過溫度感測器在不同溫度下選擇不一樣的電壓，可有效的減少功率消耗和維持系統運作的穩定度。

4. 一個新的架構用於提升交換式電容直流-直流轉換器在低負載時的能量效益和電壓穩定度被提出。

5. 在本篇論文中提出一個具數位溫度補償之低電壓鎖相迴路頻率產生器，可以透過除頻器去調節輸出頻率，以及用溫度去補償最壞情況下頻率無法鎖住的問題。

Near-/Sub-threshold PVT Sensors for Micro-Watt DVFS System Design

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ABSTRACT

The goal of this research is to design and implement PVT sensors for micro-watt DVFS system design. It includes the design of self-calibration all-digital PVT sensors, MTCMOS switched capacitor (SC) DC-DC converter, temperature compensation for low-voltage digital assist PLL, and dynamic voltage and frequency scaling system. The major contributions are as below:

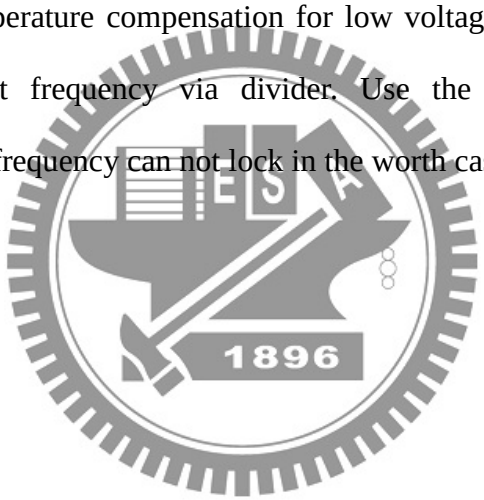
1. A near-/sub-threshold all-digital process, voltage, and temperature sensor is proposed and integrated to the DVFS control for micro-watt system applications. The sensor is proposed for high accuracy, ultra-low voltage, low power, and self-calibration portable applications.

2. A self-calibration near-/sub-threshold all-digital temperature sensor with adaptive pulse width generator is proposed. The sensor is proposed for high accuracy, ultra-low voltage, low power, and self-calibration portable applications.

3. A PVT-aware DVFS for micro-watt system is proposed. The system through the switched capacitor (SC) DC-DC converter can provide a very stable DC power supply. It generates different voltage levels which are suitable for SoC integrated regulator applications.

4. A novel connect scheme for improving power efficiency and reducing voltage variation of switched capacitor (SC) DC-DC converter which generates ultra low voltage is proposed.

5. Proposed a temperature compensation for low voltage digital assist PLL can modulate output frequency via divider. Use the temperature sensor to compensate the frequency can not lock in the worth case.



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Chapter 1 Introduction

1.1 Motivation of the Thesis

Wireless microsensor network (WSN) technology creates enormous possibility to have a positive impact on our near future life [1.1]-[1.2]. Advances in ultra-low voltage (ULV) circuit design have recently demonstrated capabilities compatible with wireless body area sensor networks (WBASNs) needs. An important application of WBAN is the vital sensor network shown in Fig1.1. Sensor nodes that measure biomedical signals such as electrocardiogram, blood pressure, and etc, are small pieces either attached on or implanted into a human body. They use a battery with as thin and light characteristics as possible. Most of them do not have the ability to last for a long time. As a result, the demand for low power has been critical in a WBAN. For the health-care purpose, it makes sense when the observation period could last for days to weeks. Therefore, the ultra-low power wireless sensor node (WSN) is the most crucial design target to achieve.

Figure 1.1. Sensor network of WBAN.

The power reduction is an important design issue for the WBAN. For ultra-low power circuit design, transistors will operate in near/sub-threshold region [1.3]. Lowering the supply voltage and frequency is one of the attractive approaches to reduce power consumption.

Furthermore, dynamic voltage and frequency scaling (DVFS) shown in Fig.1.2, achieves extremely efficient energy saving by adjusting system supply voltage and frequency depending on workload monitor [1.4]. Because if this reason, there are many previous researches about DVFS power management for digital systems such as RISC, DSP and Video Code.

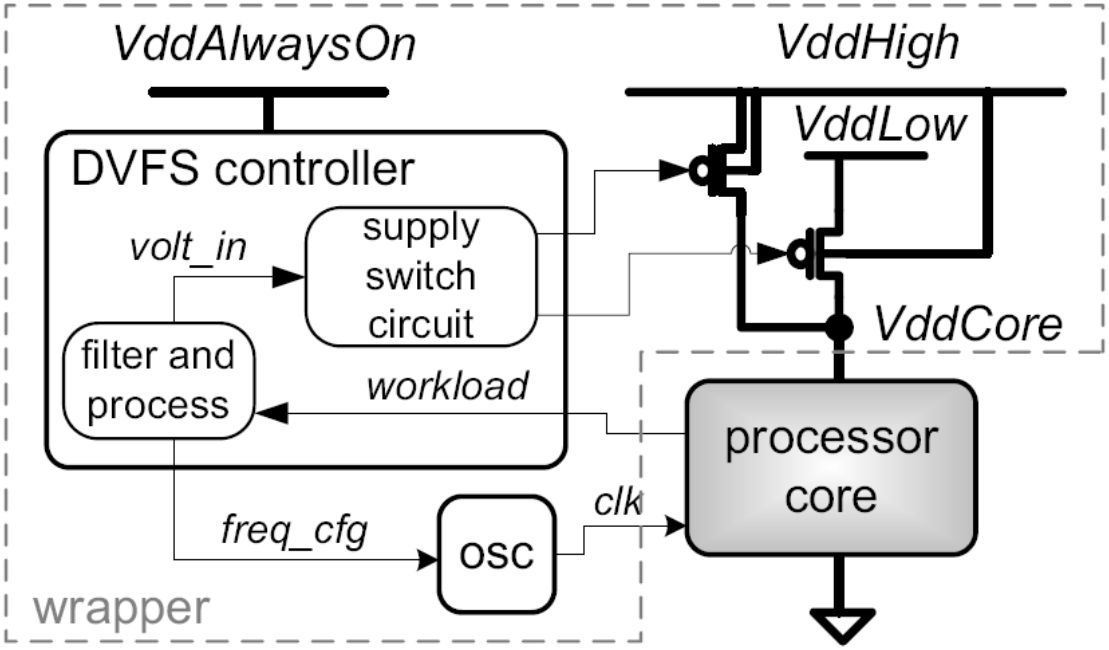


Figure 1.2 Dynamic voltage and frequency scaling systems.

As we continue to reduce the voltage until the transistor get into the near/sub-threshold voltage, circuits will become more sensitive to PVT variations than super threshold. Thus, minimizing energy dissipation and improving variation immunity are far more important rather than operating frequency. Thus, a process, voltage, and temperature (PVT) aware subthreshold clocking design is essential to solve the one last puzzle in ULV circuits.

Since wearable sensors are intended to be worn on the body, miniaturization and minimal weight are important [1.5], [1.6]. Energy harvesting and 3D integration have the potential to solve above mentioned challenges. Energy harvesting [1.7] can exploit the external environment as a source of energy for sensor nodes operating over a full lifetime; while 3D integration [1.8], [1.9] can stack more die connected with a very high packing density of one chip. Through-silicon via (TSV) technology, however, led to higher power density that is much worse hot spot issues. Thus, a PVT-aware micro-watt DVFS system for energy harvesting is also essential.

1.2 Research Goals and Major Contributions

The goal of this research is to design and implement PVT sensors for micro-watt DVFS system shown in Fig.1.3. It includes the design of self-calibration all-digital PVT sensors, MTCMOS switched capacitor (SC) DC-DC converter, temperature compensation for low-voltage digital assist PLL, and dynamic voltage and frequency scaling system.

The major contributions of this thesis are list as follow:

1. A near-/sub-threshold all-digital process, voltage, and temperature sensor is proposed and integrated to the micro-watt DVFS system. The sensor is proposed for high accuracy, ultra-low voltage, low power, and self-calibration portable applications.

2. A self-calibration near-/sub-threshold all-digital temperature sensor with adaptive pulse width generator is proposed. The sensor is proposed for high accuracy, ultra-low voltage, low power, and self-calibration portable applications.

3. A novel connect scheme for improving power efficiency and reducing voltage variation of switched capacitor(SC) DC-DC converter which generates ultra low voltage is proposed.

4. To proposed a temperature compensation for low voltage digital assist PLL can modulate output frequency via divider. Use the temperature sensor to compensate the frequency can not lock in the worth case.

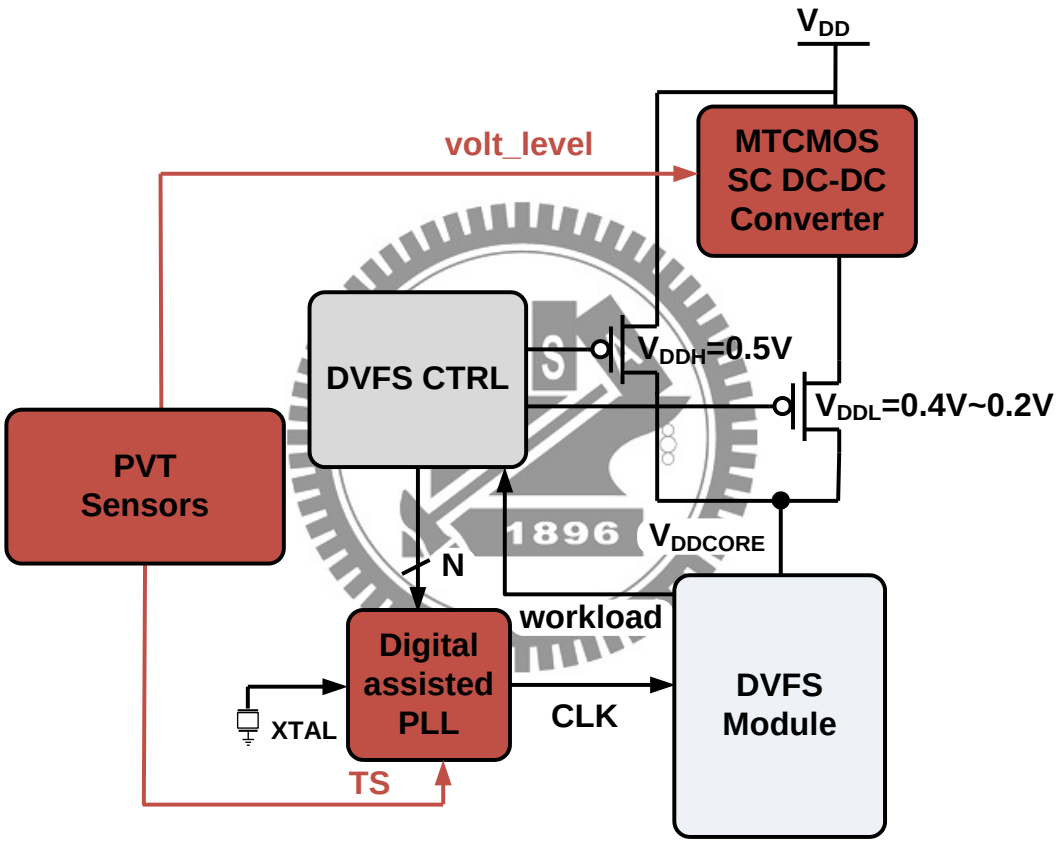


Figure 1.3 Proposed PVT sensors for micro-watt DVFS system.

1.3 Thesis Organization

The organization of the thesis is as bellow: Previous of conventional process, voltage, and temperature sensors are introduced in the Chapter 2. The detail circuits of conventional process, voltage, and temperature sensors are introduced. The

shortcomings of conventional PVT sensors are introduced. The applications of PVT sensors are also introduced.

The organization of the thesis is as below. The Chapter 1 is an introduction and motivations for research. Then, in chapter 2, introduces an overview of conventional process, voltage, and temperature sensors. The detail circuits of conventional process, voltage, and temperature sensors are introduced in this chapter and which also includes the shortages of conventional PVT sensors and the applications of PVT sensors.

In chapter 3, we have as following ideas. First, proposed fully on chip and fully digital PVT sensors. Second, we presented novel FDC technique for PVT sensors, and it can reduce power and area. Also at the same time, it improves temperature linearity in near/sub-threshold region.

The self-calibration all-digital PVT sensors and the self-calibration temperature sensor with adaptive pulse width compensation are proposed in Chapter 4. We use all-digital circuit to replace the traditional PVT sensors which can reduce power consumption and area. And to propose self-calibration technology does not require additional circuitry to achieve high accuracy.

PVT sensors for micro-watt DVFS system is introduced in the final chapter. We combine with previous proposed PVT sensors and DVFS system to control the output voltage of SC DC-DC converter for achieving the reduction of power consumption in different PVT variation. And use PVT sensors to compensate the output frequency of low voltage PLL can not lock in the worth case.

Chapter 2 Previous of Process, Voltage, and Temperature sensors

This chapter introduces the overview of PVT sensors in power management system. The conventional process sensor design would be demonstrated in Section 2.1. The conventional voltage sensor circuit evolution would be introduced in Section 2.2. Section 2.3 introduces the temperature sensor circuit evolution. Section 2.4 introduces the power management system for PVT sensors applications. Finally, Section 2.5 is the summary.

2.1 Conventional Process Sensor

Technology scaling beyond 90 nm is causing higher level of process variations, which changes the design paradigm from deterministic to probabilistic.

Fig. 2.1 shows a process monitor circuit [2.1]. The circuit consists of a current reference circuit, I_{R1} generator, and circuits to generate temperature insensitive V_{Output}. The current I_{R1} in Fig. 2.1 is given by

$$I_{R1} = \frac{V_{GS1}}{R_1} \tag{2.1}$$

The current I_{MP4} is determined by the I_{R1} and the ratio of the transistor MP2 and MP4. Therefore, V_{Output} is given by

$$V_{Output} = R_4 I_{R4} + V_{R3} = R_4 (\frac{V_{R3}}{R_3} - I_{R2} \frac{\beta_{MP4}}{\beta_{MP2}}) + V_{R3} \tag{2.2}$$

Where β is the transistor aspect ratio.

From the loop “Lx” in Fig. 2.1

$$V_{R2} + V_{GS3} = V_{R3} + V_{GS4} \tag{2.3}$$

$$\frac{\beta_{MP3}}{\beta_{MP2}} R_2 + V_{GS3} = V_{R3} + V_{GS4} \tag{2.4}$$

If transistor MN3 and MN4 are in subthreshold region, V_{R3} is obtained by solving the (2.4) using the current mirror relationships among I_{R1}, I_{MP3}, and I_{MP4}, and it is given by

$$V_{R3} = \frac{\beta_{MP3}}{\beta_{MP2}} \frac{R_2}{R_1} V_{GS1} + V_T \ln\left(\frac{\beta_{MN4}}{\beta_{MN3}} \frac{\beta_{MP3}}{\beta_{MP4}}\right) \tag{2.5}$$

By substituting (2.1) and (2.5) in (2.2), V_{Output} is obtained as follows:

$$V_{Output} = C_1 V_{GS1} + C_2 V_T \tag{2.6}$$

where

$$C_1 = \left(\frac{R_4}{R_3} + 1\right) \frac{R_2}{R_1} \frac{\beta_{MP3}}{\beta_{MP2}} - \frac{R_2}{R_1} \frac{\beta_{MP4}}{\beta_{MP2}} \tag{2.7}$$

$$C_2 = \left(\frac{R_4}{R_3} + 1\right) \ln\left(\frac{\beta_{MN4}}{\beta_{MN3}} \frac{\beta_{MP3}}{\beta_{MP2}}\right) \tag{2.8}$$

In [2.2], V_{GS1} is given by

$$V_{GS1} \approx V_{GS1}(T_0) + K_G\left(\frac{T}{T_0} - 1\right) \tag{2.9}$$

where

$$K_G = K_T + V_{GS}(T_0) - V_{th}(T_0) \tag{2.10}$$

where V_T is the thermal voltage, K_T is the temperature coefficient for threshold voltage (typical value is 0.3 V), and T_0 is the room temperature.

Substituting (2.10) in (2.6) to find temperature independent V_{Output}, taking partial derivative with respect to temperature, and setting it zero

$$\frac{\partial V_{Output}}{\partial T} = 0 \tag{2.11}$$

Solving (2.11), the condition nullifying the temperature coefficient V_{Output} of is given by

$$\frac{C_1}{C_2} = -\frac{V_T(T_0)}{K_G} \tag{2.12}$$

However, from (2.12), the temperature coefficient is affected by the large [threshold-voltage variation in different process corner and it leads significant variation of reference voltage. Therefore, the circuit is not suitable for a voltage-reference circuit but is suitable for a process-variation monitoring circuit. Fig. 2.2 demonstrates linear variation of the reference voltage according to process corner conditions. The reference voltage is not affected by temperature and supply voltage variations as shown in Fig. 2.2.

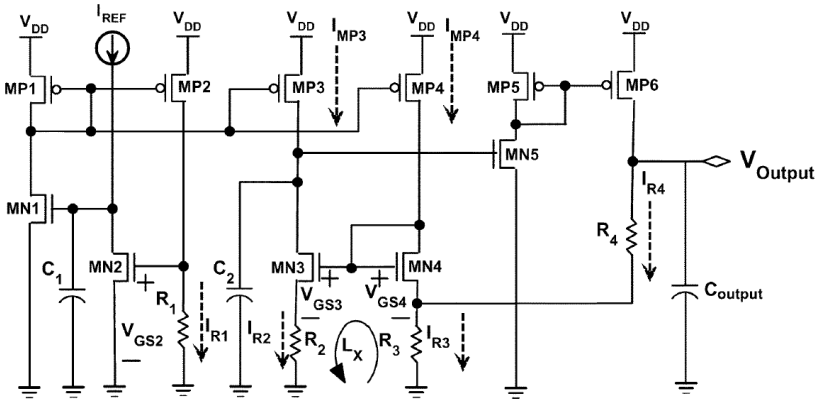


Figure 2.1. Process monitoring circuit.

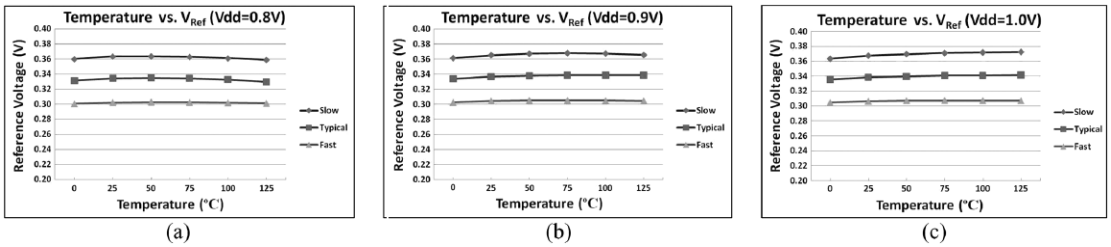


Figure 2.2. Process dependence of reference voltage (output) in different temperatures and supply voltages: (a) V_{DD} = 0.8 V; (b) V_{DD} = 0.9 V; (c) V_{DD} = 1.0 V.

2.2 Voltage Sensor Circuit Evolution

Advanced systems (automobiles, medical and other electronic devices) have come to use multiple sensors in recent years, and the number is expected to increase even more in the future. The basic structure of the sensors includes a sensing element and electronic circuits. User requirements for sensors have become more and more demanding, including the need for high performance and lower cost.

Therefore, there are four major problems in predicting the analog type sensors of the near future. The first issue, from an economic perspective, is the difficulty of shrinkage due to loss of accuracy. The second problem involves greater sophistication of, for example, self-correction and self-diagnostics. The third issue is environmental durability. The fourth problem relates to improving reliability.

Research on digitalization of sensor circuits has become energized as efforts are made to resolve these problems. To realize digital sensing, the weak signal from the element must be analog-to-digital (A/D) converted at an early stage within the sensor chip, so an A/D converter (ADC) is required. A successive approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

2.2.1 Successive Approximation Analog-to-Digital Converter

The successive-approximation (SA) ADC is one of the most popular architectures for data-acquisition applications, especially when high-resolution, low power and medium speed are required. In some applications such as wireless sensor nodes, designing low power and low energy ADC is one of the major challenges. For SAADC, the dominant power dissipation sources are the comparator and the

switching in the DAC capacitor array. Traditional successive-approximation ADC architecture is shown in Fig2.3.

The successive approximation ADC circuit typically consists of four chief subcircuits:

1. A sample and hold circuit (S/H) to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive approximation register subcircuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and do the same test, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

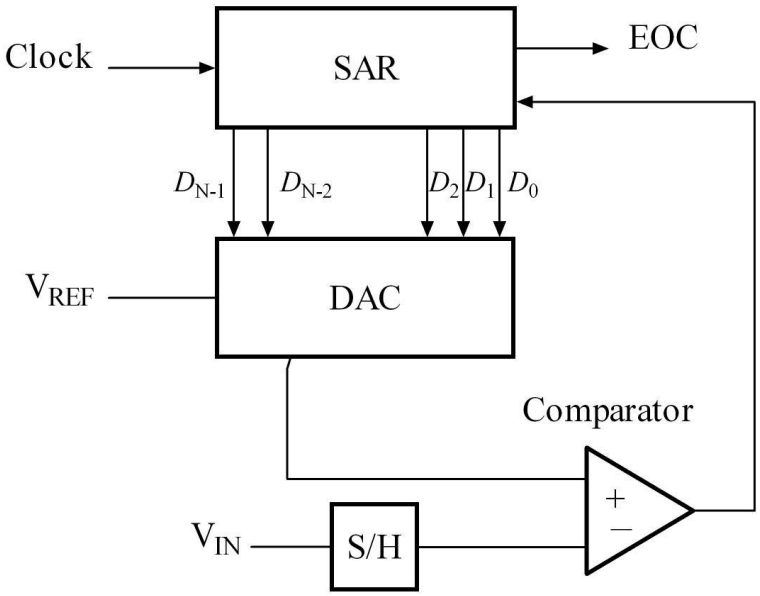


Figure 2.3 Successive Approximation ADC Block Diagram

2.2.2 All-Digital Analog-to-Digital Converter

The general schematic of all-digital ADC is shown in Fig 2.4. The multi oscillators (f_0, $2f_0$, ... 2^Nf_0) are employed to be corresponding to the quantization levels (q, 2q, 2^Nq) in the conventional ADC, Fig2.5 . According to the input voltage, one of these oscillators is selected and pass through constant time pulse ($T_S=l/f_0$) to the counter. The switching block is a combinational logic circuit as shown in Fig 2.4, which is used to pass the equivalent frequency required. The input voltage controls the selective block.

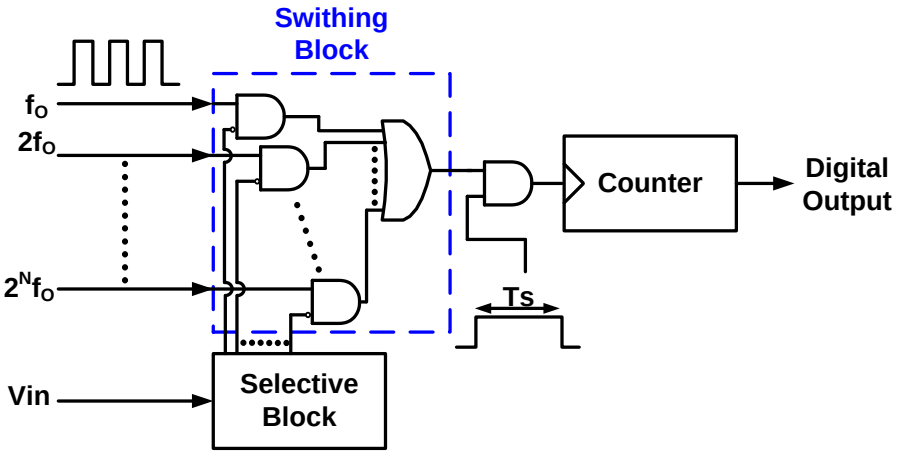


Figure 2.4 The general all-digital ADC.

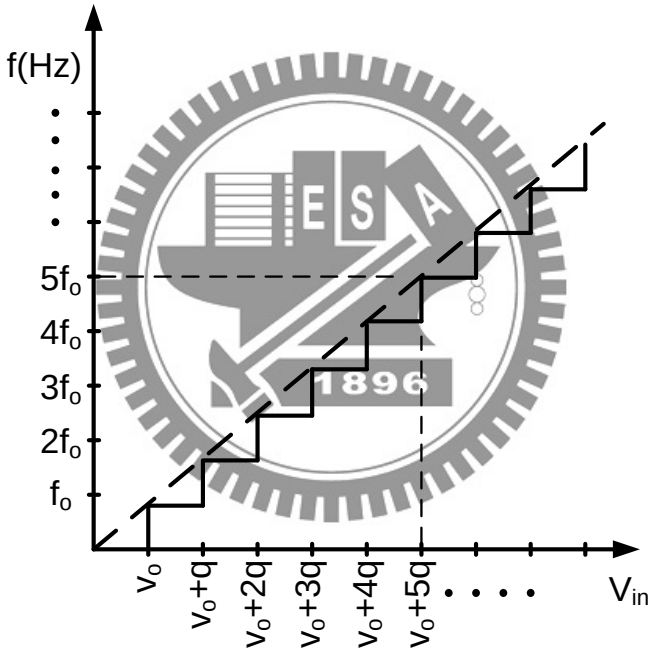


Figure 2.5 Quantization levels of ADC.

In the last approach, the number of gates will be dramatically high. Therefore, to minimize the hardware complexity, a new circuit was presented [2.3] as shown in Fig2.6. In the circuit, the input voltage is converted to frequency (voltage controlled oscillator) using only one oscillator. This clock signal is passing through constant duration pulse (Ts) to count, as shown in Fig2.6. In this circuit, if the supply voltage (control terminal) is changed from V_O to V_O+q, where q is the quantization voltage,

the output frequency of the VCO will be less or equal f_O. (fo=l/Ts, where T, is time of conversion). Therefore, the counter will count 0's, (no positive/negative edge will be counted). At the second quantization level (2q), the frequency output must be 2fo. Only two pulses will be memorized in the counter during the Ts pulse. The relation between the input voltage and its equivalent frequency is shown in Fig 2.5.

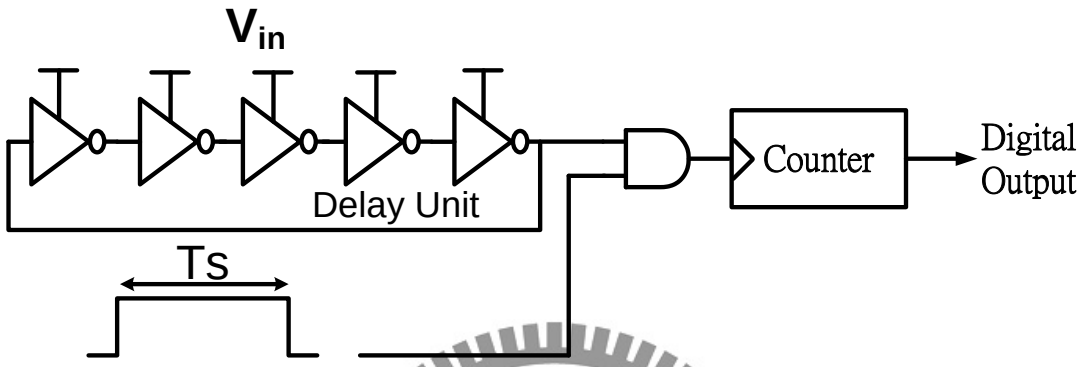


Figure 2.6 All-digital voltage to frequency converter ADC.

The digital voltage-to-time conversion technique, can be employed as controlled circuit. The basic block and timing diagram of this controlled circuit are shown in Fig2.7. The inverter steps within the gate delay pulse group are P1, P2, P3,..., which are steady states (1,0,1,...). Measurement process starts with the rise of pulse PA, then the P1, P2, P3, ... are going to invert. Due to the propagation delay time, there is an overlap between two 1's or 0's as shown in Fig 2.8. When pulse PB starts to rise, the number of inverters in which its outputs have changed due to PA is equal the measurement time. Table 2.l illustrates the XOR gate outputs for 4-stage delay line, the 0's output logic means that position of the overlap between two l's logic. This 0's logic will be cached at Y_1 at level V_1 of the input, at Y_2 at level V_2, and so on, where ($V_1<V_2<V_3<V_4<V_5$).

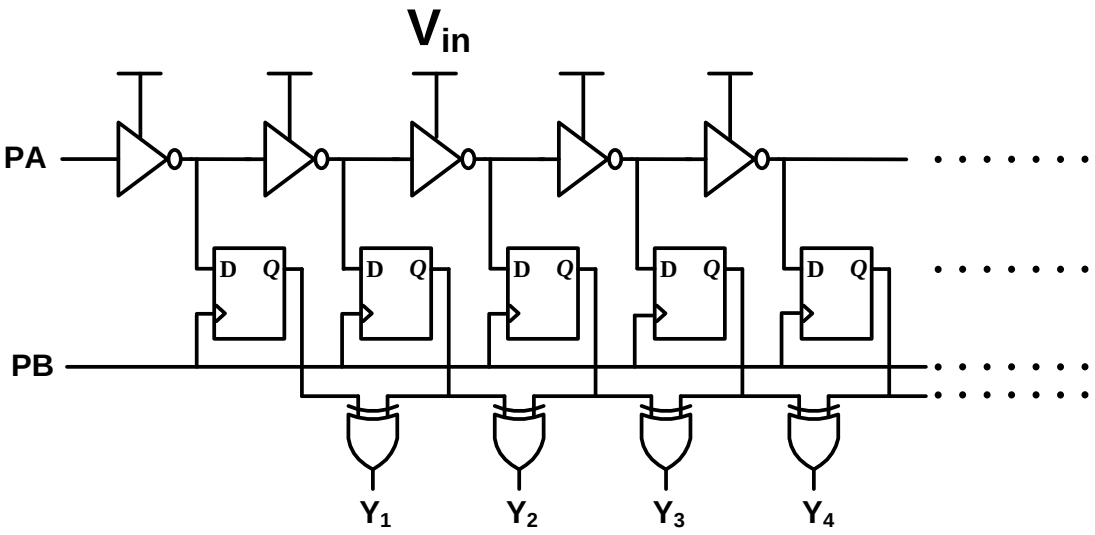


Figure 2.7 Voltage to time conversion concept using digital circuit.

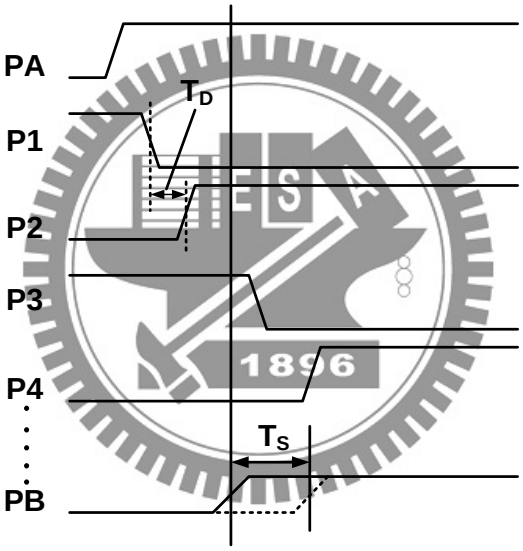


Figure 2.8 Voltage to time conversion wave signals.

Table 2.1 The output of voltage-to-time conversion ADC ($T_{D1} > T_{D2} > T_{D3} > T_{D4} > T_{D5}$)

V_{in}	Delay Time	Output			
		Y_1	Y_2	Y_3	Y_4
V_1	T_{D1}	0	1	1	1
V_2	T_{D2}	1	0	1	1
V_3	T_{D3}	1	1	0	1
V_4	T_{D4}	1	1	1	0
V_5	T_{D5}	1	1	1	1

2.3 Temperature Sensor Circuit Evolution

In recent years, numerous portable electronic products have been launched to the market with considerable market growth. With process scaling down continuously, this high level of integration also introduces the problem of self-heating, which is the result of increased power density. Low cost, low power, high-performance temperature sensors are therefore becoming increasingly important for applications from power consumption control to thermal monitoring, so as to enhance performance and reliability. The important applications of smart temperature sensors include:

1) The power consumption control in VLSI chips, such as CPU and chip sets.

2) The thermal compensation in single-chip systems and micro systems with built-in sensors.

3) The environment temperature monitors in automatic fabrication factories.

4) The temperature control of consumer electronics, such as automobiles and home electronics. Kim et al. [2.4] use temperature Sensor for Mobile DRAM Self-refresh Control.

2.3.1 Analog Temperature Sensor

Several different implementations of on-chip temperature sensors have been reported in the last ten years. With the use of bipolar transistors for temperature sensing, and advanced techniques including chopping circuit, dynamic element matching and sigma-delta ADC for noise suppression and cancellation, Pertijs et al. [2.5] developed an on-chip temperature sensor with a 3σ inaccuracy of ±1℃at the expense of increased circuit complexity.

With the use of three CMOS transistors for temperature sensor was presented in [2.6]. The three-transistor temperature sensor shows in Fig. 2.9, which utilizes the

temperature characteristic of the threshold voltage, shows highly linear characteristics at a power supply voltage of 1.8 V. The conditions of this temperature sensor are defined as follows.

1) All transistors operate in the saturation region.

2) The output voltages of each node are equal.

3) The sinking currents at each node are equal.

The temperature is obtained by measuring V_{OUT}, where the two currents, I_{OUT1} and I_{OUT2}, have the same value. When the substrate bias effect of the transistor M2 is neglected to simplify the calculation, their I_{DS}-V_{GS} characteristics and the operating conditions are

$$I_{DS1} = \frac{\beta_1}{2}(V_{GS1} - V_{T1})^2 \tag{2.13}$$

$$\beta_1 = \mu_{eff1} C_{OX} \frac{W_1}{L_1} \tag{2.14}$$

$$I_{DS2} = \frac{\beta_2}{2}(V_{GS2} - V_{T2})^2 \tag{2.15}$$

$$\beta_2 = \mu_{eff2} C_{OX} \frac{W_2}{L_2} \tag{2.16}$$

$$I_{DS3} = \frac{\beta_3}{2}(V_{GS3} - V_{T3})^2 \tag{2.17}$$

$$\beta_3 = \mu_{ef3} C_{OX} \frac{W_3}{L_3} \tag{2.18}$$

$$I_{DS1} = I_{DS2} = I_{DS3} \tag{2.19}$$

$$V_{OUT1} = V_{GS1} \quad , \; V_{OUT2} = V_{GS2} + V_{GS3} \tag{2.20}$$

$$V_{OUT1} = V_{OUT2} \tag{2.21}$$

After solving (2.16) - (2.18) for each transistor's respective V_{GS}, the results are applied to $V_{GS2}$and V_{GS3} in (2.20). Then, I_{DS2} and I_{DS3} are also substituted for (2.13)&(2.14) using (2.19). Finally, (2.21) is solved against V_{GS1} and we get

$$V_{OUT1} = V_{GS1} = \frac{V_{T2} + V_{T3} - (\sqrt{\beta_1/\beta_2} + \sqrt{\beta_1/\beta_3})V_{T1}}{1 - (\sqrt{\beta_1/\beta_2} + \sqrt{\beta_1/\beta_3})} \propto T \tag{2.22}$$

$$\frac{dV_{OUT1}}{dT} = a\left(\frac{dV_{T2}}{dT} + \frac{dV_{T3}}{dT}\right) - b\frac{dV_{T1}}{dT} \tag{2.23}$$

Where

$$a = \frac{1}{1 - (\sqrt{\beta_1/\beta_2} + \sqrt{\beta_1/\beta_3})}$$

$$b = \frac{\sqrt{\beta_1/\beta_2} + \sqrt{\beta_1/\beta_3}}{1 - (\sqrt{\beta_1/\beta_2} + \sqrt{\beta_1/\beta_3})}$$

Since $\sqrt{\beta_1/\beta_2} + \sqrt{\beta_1/\beta_3}$ can be assumed as constant, the variables and in (2.23) also become constant. Therefore, the output voltage corresponds to the temperature coefficients of the transistor threshold voltages.

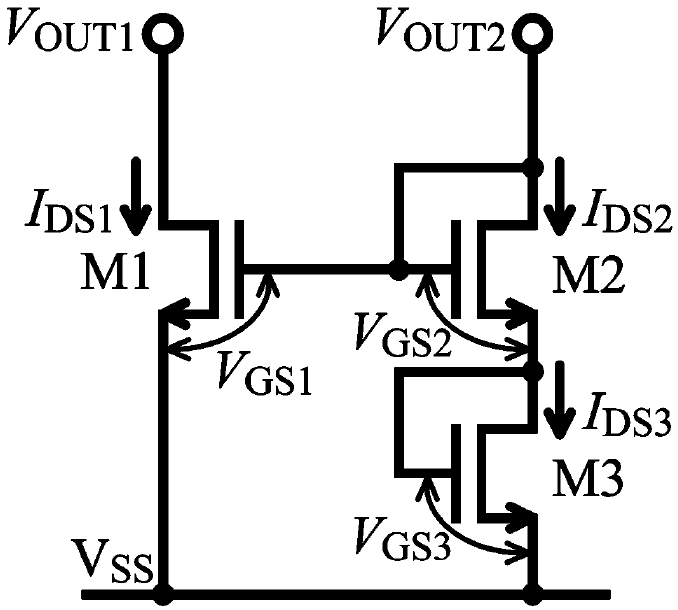


Figure 2.9 Conventional three-transistor temperature sensor.

Fig. 2.10 shows the characteristics at 1.8V and 1V supply voltages, where the intersections of and correspond to the operating points of this sensor. This method shows highly linear characteristics at a power supply voltage of 1.8V or more, which enables us to define the operating conditions well above twice the threshold voltage. But the linearity diminishes after scaling down the supply voltage to 1V using a 90-nm CMOS process. Because the temperature coefficient of the operating point's current at a 1V supply voltage is steeper than the coefficient at a 1.8V supply voltage, the operating point's current at high temperature becomes quite small and the output voltage goes into the subthreshold region or the cutoff region.

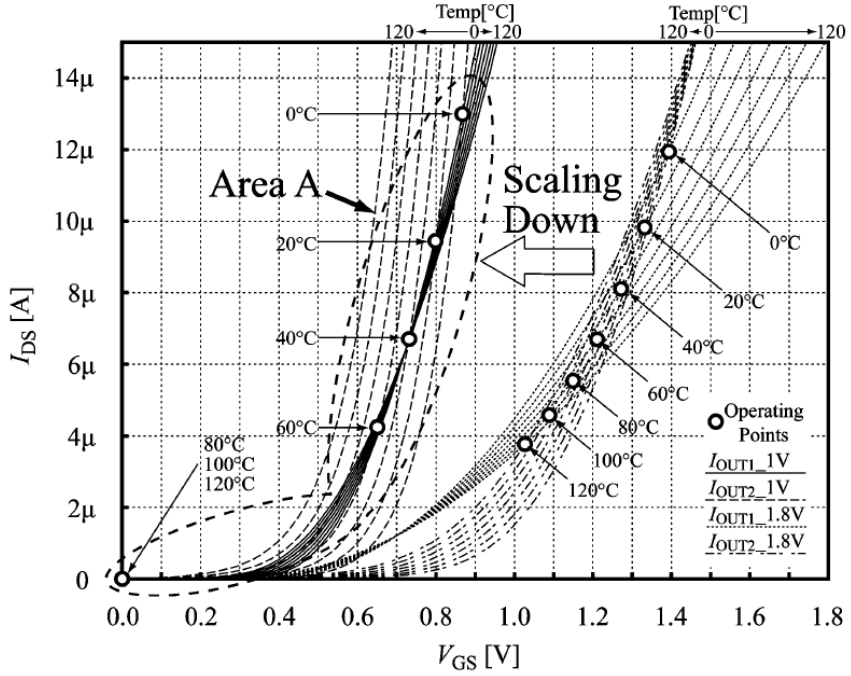


Figure 2.10 Operating-point comparison of three-transistor temperature sensor on I_{DS}-V_{GS} curves at 1.8- and 1.0-V supply voltage.

To improve linearity at a 1V supply voltage, an accurate four-transistor temperature sensor was designed in [2.7] shows in Fig. 2.11, and developed for thermal testing and monitoring circuits in deep submicron technologies. Note that to operate the additional transistor in the saturation region, an extra bias voltage V'_{GS0} is required.

Of course, the bias voltage generation circuit must not possess temperature dependency, and, in some cases, this circuit becomes larger than the temperature sensor itself.

In addition, the W/L ratio of the transistors $M0'$ and $M1'$ should be as small as possible so that the current I'_{OUT1} remains small. However, the smaller W/L ratio requires a longer channel, so it occupies larger chip area. Consequently, there is a tradeoff between the current consumption and the chip area.

The $I'_{DS} - V'_{GS}$ characteristics and the operating conditions of both the proposed four-transistor sensor is the following:

$$V'_{OUT1} = \sqrt{\frac{2I'_{DS2}}{\beta'_2}} + V'_{T2} + \sqrt{\frac{2I'_{DS3}}{\beta'_3}} + V'_{T3} \propto T \tag{2.24}$$

$\sqrt{\frac{2I'_{DS2}}{\beta'_2}} + \sqrt{\frac{2I'_{DS3}}{\beta'_3}}$ can be assumed as a constant value. Thus, (2.24) shows that the output voltage is mainly proportional to the temperature characteristics of the threshold voltage ($M2'$ and $M3'$).

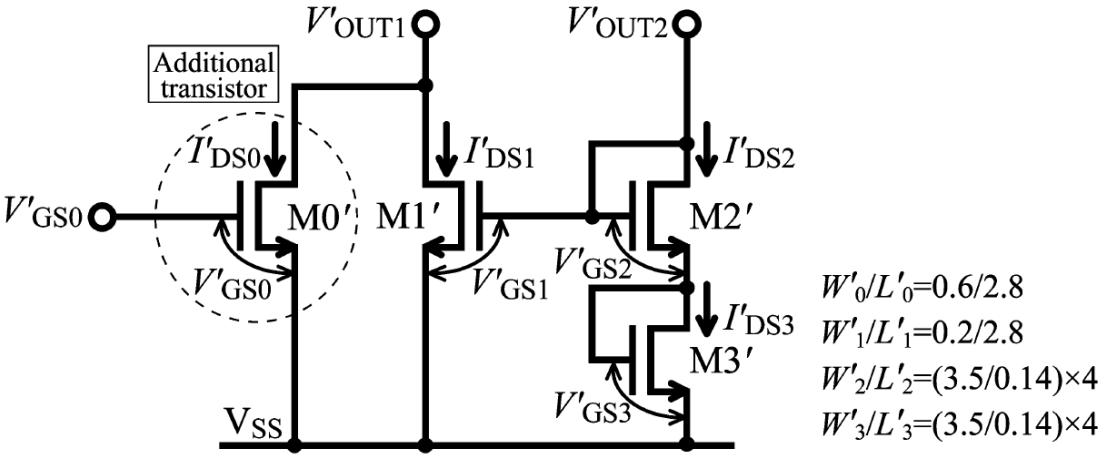


Figure 2.11 Four-transistor, voltage output, temperature sensor.

The output current of four- transistor temperature sensor is more high linearity with high temperature than conventional three-transistor circuit shows in Fig 2.12.

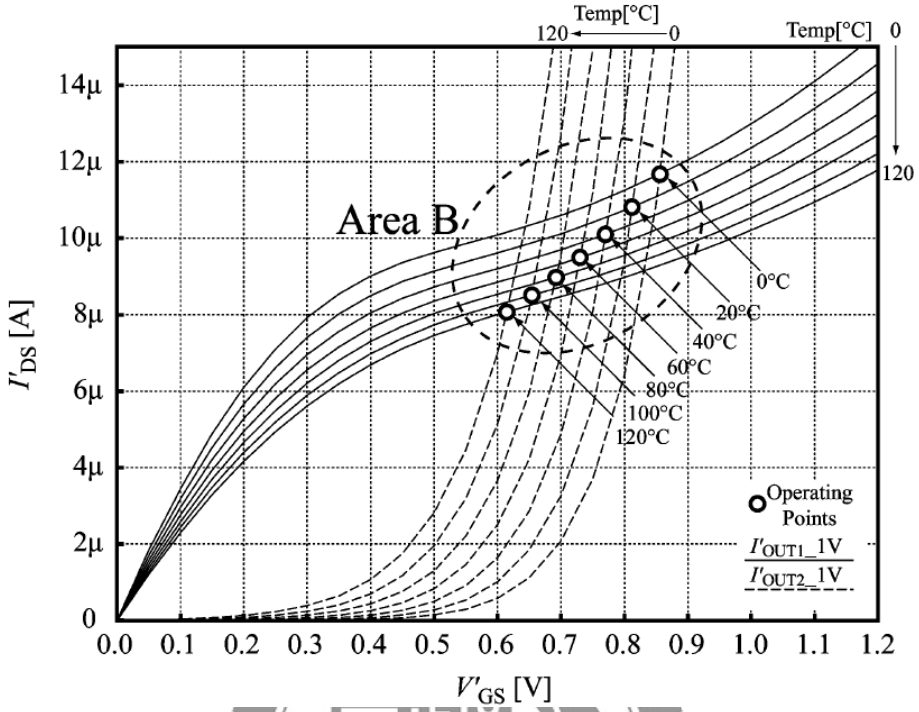


Figure 2.12 Operating points of four-transistor temperature sensor.

2.3.2 Time-to-Digital Based Temperature Sensors

In the late 20th century, analog-to-digital converters (ADCs) were gradually integrated into analog thermal sensors by IC designers to compose the so-called intelligent or smart temperature sensors. The typical block diagram of the conventional smart temperature sensor is depicted in Fig. 2.13 [2.8]. The sensor consumes more power, and large area, so another version of all-digital temperature sensor which is based on time-to-digital converters instead of ADCs was presented in [2.9]-[2.15].

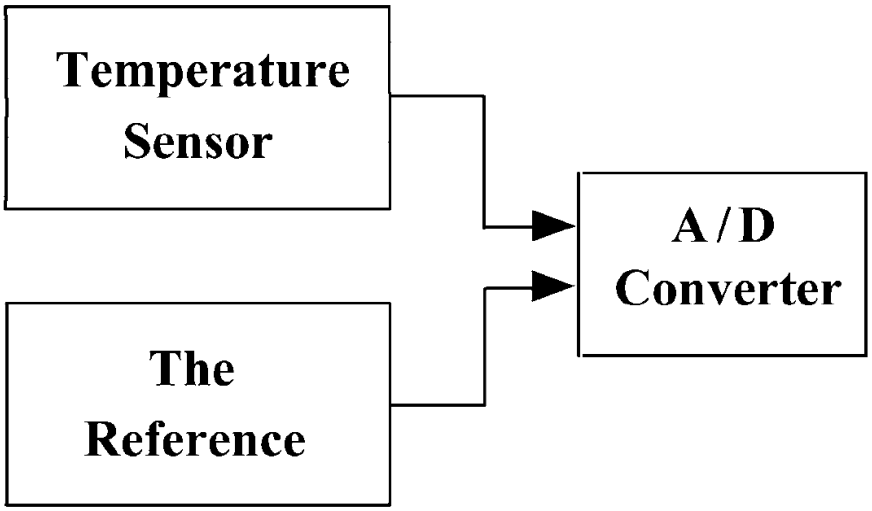


Figure 2.13 Conventional digital output of temperature sensor.

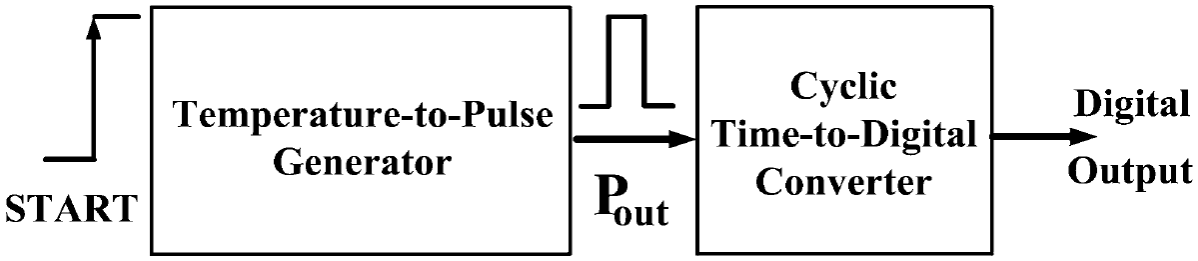


Figure 2.14 Block diagram of the time-to-digital temperature sensor.

The temperature sensor composed of temperature-to-pulse generator and cyclic time-to-digital converter, shows in Fig 2.14. Temperature-to-pulse generator, it can generate a pulse width is linear to temperature variation. A simple circuit utilizing gate delays to generate the thermally sensitive pulse is shown in Fig. 2.15. The START signal is delayed a certain amount of time by the delay line composed of even number of inverter. The high-to-low and low-to-high propagation delay time for an inverter can be expressed as [2.16]

$$t_{PHL} = \frac{2C_L V_{TN}}{K_N (V_{DD} - V_{TN})^2} + \frac{C_L}{K_N (V_{DD} - V_{TN})} \cdot \ln\left(\frac{1.5V_{DD} - 2V_{TN}}{0.5V_{DD}}\right) \quad (2.25)$$

$$t_{PHL} = \frac{-2C_L V_{TP}}{K_P (V_{DD} + V_{TP})^2} + \frac{C_L}{K_P (V_{DD} + V_{TP})} \cdot \ln\left(\frac{1.5V_{DD} + 2V_{TP}}{0.5V_{DD}}\right) \quad (2.26)$$

Where $k_N = \mu_N C_{OX}(W/L)_N$, $k_P = \mu_P C_{OX}(W/L)_P$ and C_L are the transconductance parameters and effective load capacitance of the inverter. Note that we assume square-law behavior for the CMOS devices and thereby ignore the effects of velocity saturation. For an inverter with equivalent NMOS and PMOS, the propagation delay can be derived as

$$t_P = \frac{t_{PLH} + t_{PHL}}{2} = \frac{(L/W)C_L}{\mu C_{OX}(V_{DD} - V_T)} \ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right) \quad (2.27)$$

Where

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{km}, \quad km = -1.2 \sim -2.0 \quad (2.28)$$

$$V_T(T) = V_T(T_0) + \alpha(T - T_0), \quad \alpha = -0.5 \sim -3.0 mv/°k \quad (2.29)$$

As the temperature increases, the mobility (μ) and the threshold voltage (V_T) will both decrease. In the case of V_{DD} much larger than V_T, the thermal effect of the propagation delay will be dominated by the mobility. That is, the thermal coefficient of the propagation delay will become positive. The major problem of the simple temperature-to-pulse generator is that the width of the output pulse at the lower bound of the measurement range is usually much larger than zero. This will cause a large DC offset at the smart temperature sensor output. The second delay line with thermal compensation for temperature sensitivity reduction is inserted in the lower transmission path of the START signal to reduce the width offset of the output pulse, which is shown in Fig. 2.16. The width offset of the output can be easily reduced by adjusting the number of delay cells in delay line 2.

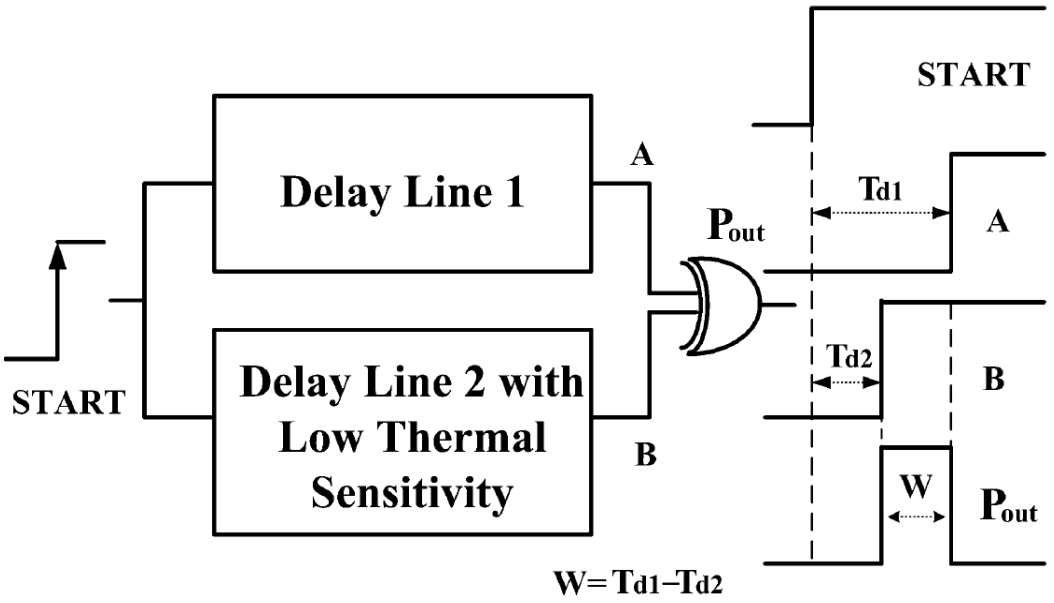


Figure 2.15 Temperature-to-pulse generator.

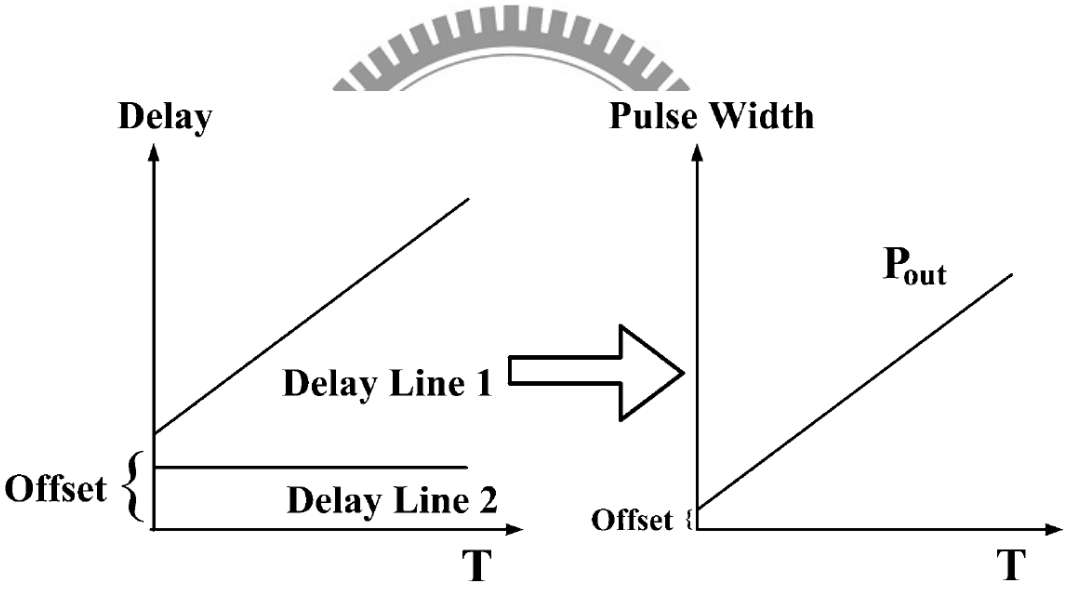


Figure 2.16 Width offset reduction accomplished by delay line 2.

As shown in Fig. 2.17, a simple thermal compensation circuit is used to reduce the sensitivity of the inverter in delay line2. The diode connected transistors P1, N1, and P3 serve as the core of the thermal compensation circuit. Since P1, P3, and N1 are all diode connected, they will operate in saturation if bias current is flowing. Thus, we have

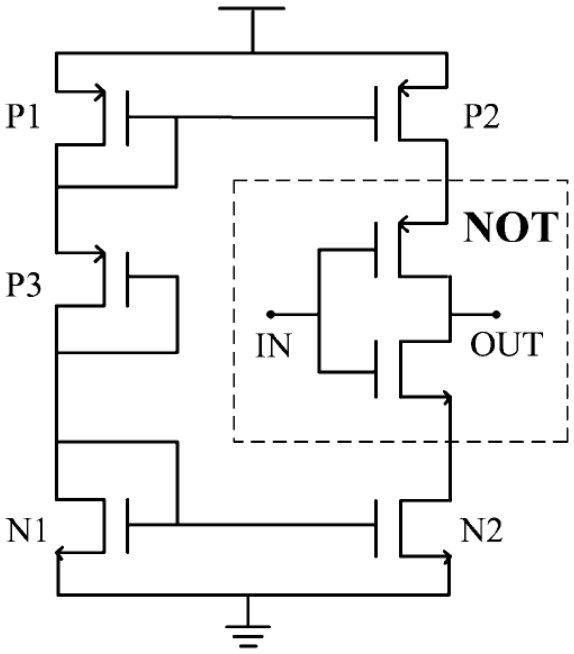


Figure 2.17 Delay cell is used in delay line 2.

$$I_{DP3} = \frac{1}{2}\mu C_{OX}(\frac{W}{L})(V_{GSP3} - V_T)^2(1+\lambda V_{GSP3}) \quad (2.30)$$

By substituting (2.28) and (2.29) into (2.30), the equation becomes

$$I_{DP3} = \frac{1}{2}\mu_0 C_{OX}(\frac{W}{L})(\frac{T}{T_0})^{km}[V_{GSP3} - V_T(T_0) - \alpha(T - T_0)]^2(1+\lambda V_{GSP3}) \quad (2.31)$$

When the temperature is higher than 200K, a significant plateau effect can be observed for the difference between mask channel length and effective channel length. The thermal sensitivity of channel length modulation term $(1+\lambda V_{GSP3})$ will be neglected in the following deviations since it is much smaller than those of mobility and threshold voltage over the temperature range we are interested.

To get the minimum thermal sensitivity, let $\frac{\partial I_{DP3}}{\partial T} = 0$

$$\frac{\mu_0 \cdot C_{OX} \cdot km}{2T_0}\left(\frac{W}{L}\right)\left(\frac{T}{T_0}\right)^{km-1}\left[V_{GSP3} - V_T(T_0) - \alpha(T - T_0)\right]^2(1 + \lambda V_{GSP3})$$

$$= \alpha \cdot \mu_0 \cdot C_{OX}\left(\frac{W}{L}\right)\left(\frac{T}{T_0}\right)^{km}\left[V_{GSP3} - V_T(T_0) - \alpha(T - T_0)\right](1 + \lambda V_{GSP3})$$

After simplification, we have

$$V_{GSP3} = V_T(T_0) + \alpha(T - T_0) + 2\frac{\alpha \cdot T}{km} \tag{2.32}$$

The sizes of transistors P1 and N1 are adjusted to make the gate-to-source voltage of P3 fit the requirement stated in (2.32) as closely as possible. The conduction current of transistor P3 can be found by substituting (2.32) back into (2.31) to yield

$$I_{DP3} = \frac{1}{2}\mu_0 C_{OX}\left(\frac{W}{L}\right)\left(\frac{T}{T_0}\right)^{km}\left[\frac{2\alpha T}{km}\right]^2(1 + \lambda V_{GSP3}) \tag{2.33}$$

When $km = -2$, the drain current will become totally thermal independent

$$I_{DP3} = \frac{1}{2}\mu_0 C_{OX}\left(\frac{W}{L}\right)(\alpha T_0)^2(1 + \lambda V_{GSP3})$$

Through the help of the current mirrors (P1, P2) and (N1, N2), the drain current of the inverter will be kept thermally insensitive as well, as will the propagation delay of delay line 2. This greatly reduces the design difficulty and enhances the tolerance to process variation.

Finally, the cyclic time-to-digital converter, shows in Fig 2.18, it convert the pulse width of temperature-to-pulse generator to digital output code.

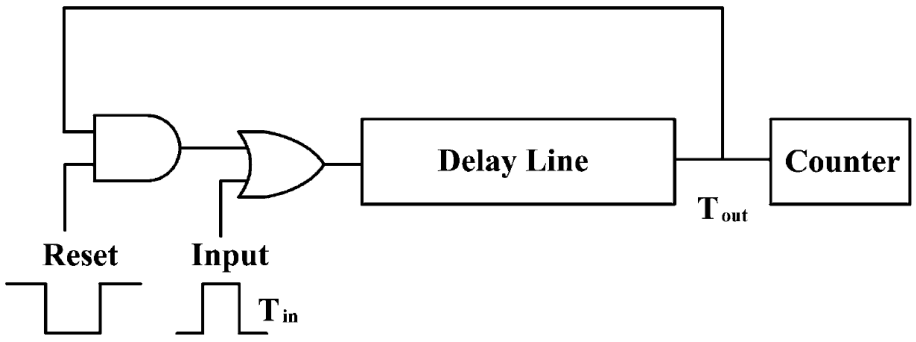


Figure 2.18 Block diagram of the cyclic TDC.

2.3.3 Dual-DLL-Based All-Digital Temperature Sensors

With process scaling down continuously, PVT variation will be a big problem about Time-to-digital based temperature sensors. A new type DLL-based all-digital temperature sensor [2.17] was presented. It has two improvements. First, it removes the effect of process variation on inverter delays via calibration at one temperature point, thus, reducing high volume production cost. Second, we used two fine-precision DLLs, one to synthesize a set of temperature-independent delay references in a closed loop, the other as a TDC to compare temperature-dependent inverter delays to the references. The use of DLLs simplifies sensor operation and yields a high measurement bandwidth (5kS/s) at 7bit resolution, which could enable fast temperature tracking.

We execute calibration and delay normalization using the circuit of Fig. 2.19. It contains an open-loop delay line, and a DLL that synthesizes temperature-independent-delay references. This reference-DLL (R-DLL) is locked to a crystal oscillator x(t): each delay cell in the R-DLL has constant delay $\Delta 0$. MUX-1 taps a node in the R-DLL delay line: if the N-th cell's output is tapped, the delay from input x(t) to output d(t) of the R-DLL is $D_{DLL} = N\Delta_0$. This is our delay reference independent of temperature and process. N can be altered to produce different reference delays. In the open-loop line, if the M-th cell's output is tapped by MUX-2, the delay between input x(t) and output c(t) is varies with temperature and process.

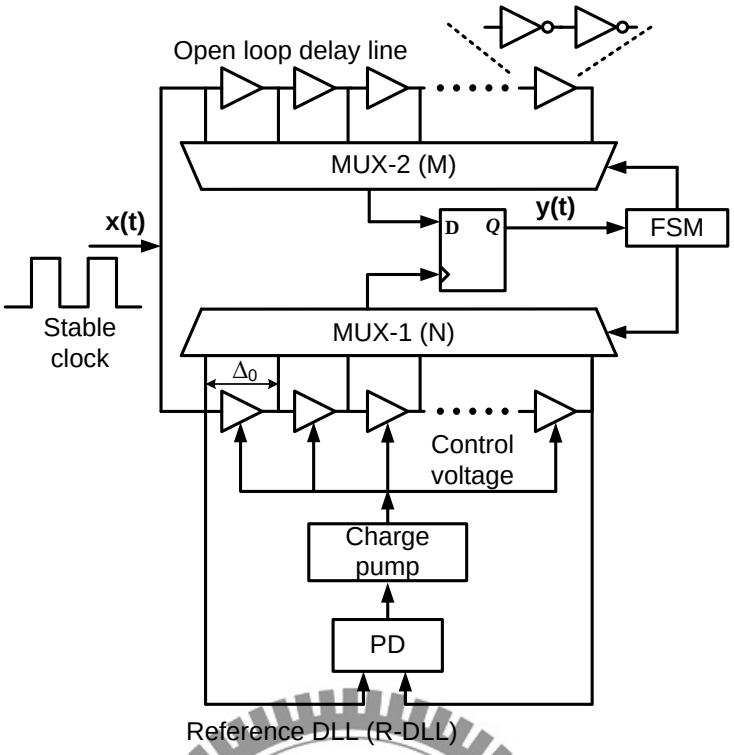


Figure 2.19 Basic architecture of DLL-based CMOS digital temperature sensor.

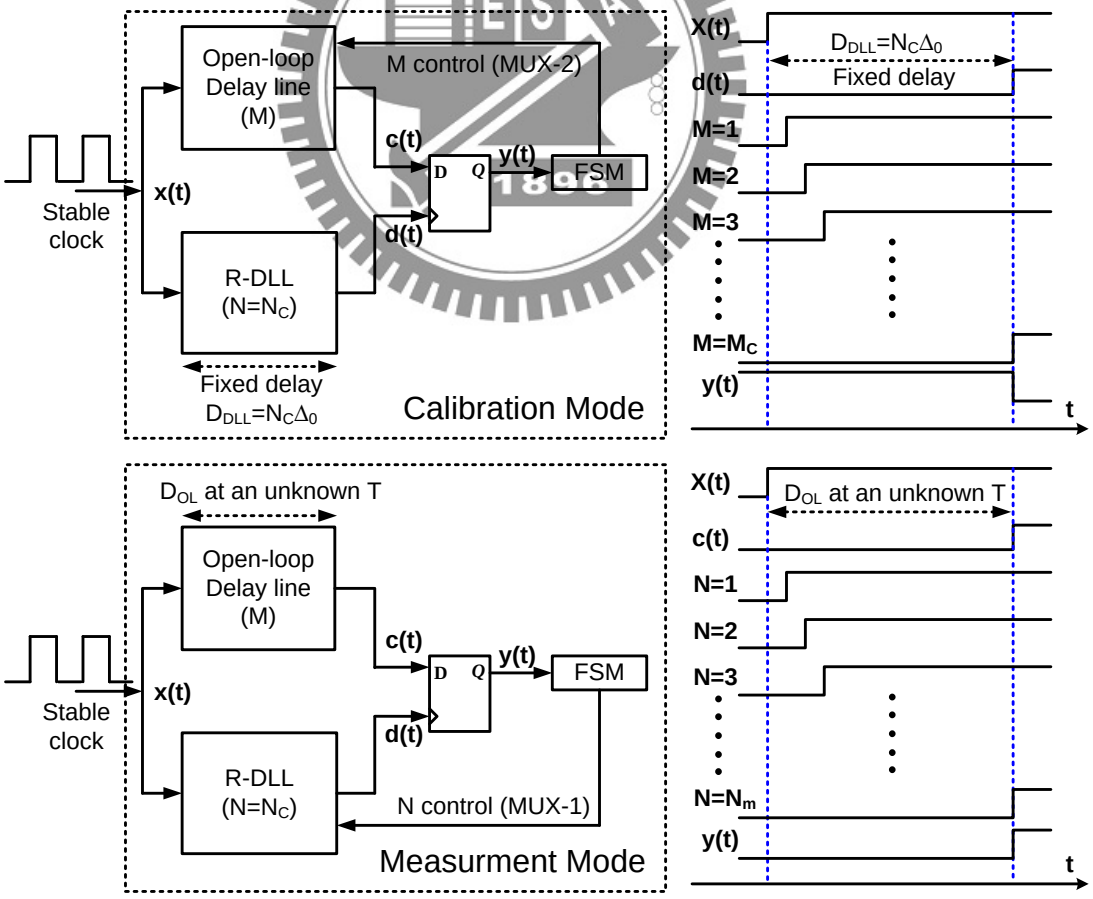


Figure 2.20 Calibration mode (top) and measurement mode (bottom).

In calibration mode at temperature T_C, we set $N = N_C$ to fix the reference delay at $D_{DLL} = N_C\Delta_0$. We then increase M (MUX-2 setting) until D_{OL} equals D_{DLL} at $M = M_C$. This comparison of D_{OL} to D_{DLL} to find their lock at $M = M_C$ is done via the bang-bang phase detector in the middle of Fig. 2.19. Then the M_C value is corresponding to process corner.

Once 1-point calibration is complete, the sensor enters measurement mode. Temperature T is unknown, thus, D_{OL} of the hardwired open-loop line is an unknown delay, which the M-DLL measures by varying the reference delay D_{DLL} of the R-DLL (bottom of Fig. 2.20). MUX-1 setting N is varied until DDLL equals D_{OL} at N = Nm. Nm is a digital output that faithfully represents T. Nm corresponds to the normalized delay seen earlier. Fig. 2.21 shows the implemented architecture.

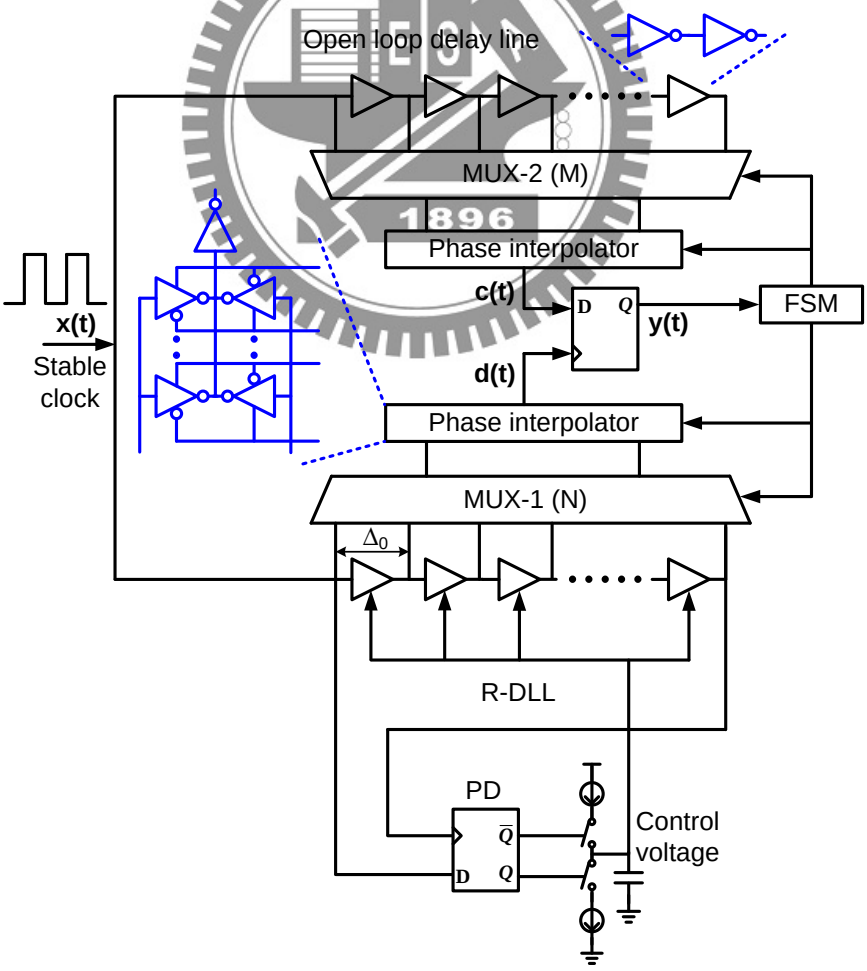


Figure 2.21 DLL-based CMOS all-digital temperature sensor.

2.4 PVT Sensors Applications

The important applications of temperature sensors include:

1) The temperature control of consumer electronics, such as automobiles and home electronics.

2) The power consumption control in VLSI chips, such as CPU and chip sets;

3) The environment temperature monitor in automatic fabrication factories;

4) The temperature control of 3D-ICs.

5) The temperature compensation of clock skew in synchronous digital circuit.

2.4.1 CMOS Temperature Sensor with Ring Oscillator for Mobile DRAM Self-refresh Control

Low-power mobile DRAM can adjust its self-refresh period according to internal temperature to minimize data retention current during power-down mode [2.4]. Usually, the leakage characteristic of a DRAM cell becomes worse at high temperature than at low temperature. Hence, for a conventional DRAM with no self-refresh control scheme, the interval for self-refresh operation must be determined by the hottest temperature condition. This means that data retention current is wasted at low temperature due to too early refresh of memory cells. Moreover, if a local clock signal to determine the self-refresh interval is generated by a ring oscillator as conventional DRAMs do, the wasted data retention current tends to be further increased at low temperature because the oscillation frequency of the oscillator increases as temperature decreases. This situation is described by the upper curve in Fig. 2.22 showing the dependency of the oscillation frequency of a ring oscillator on temperature variation. On the other hand, if we can measure the temperature using a temperature sensor, the self-refresh period can be adjusted adaptively based on this

measured temperature. That is, the period can be set long at low temperature and short at high temperature, as seen by the lower curve in Fig. 2.22

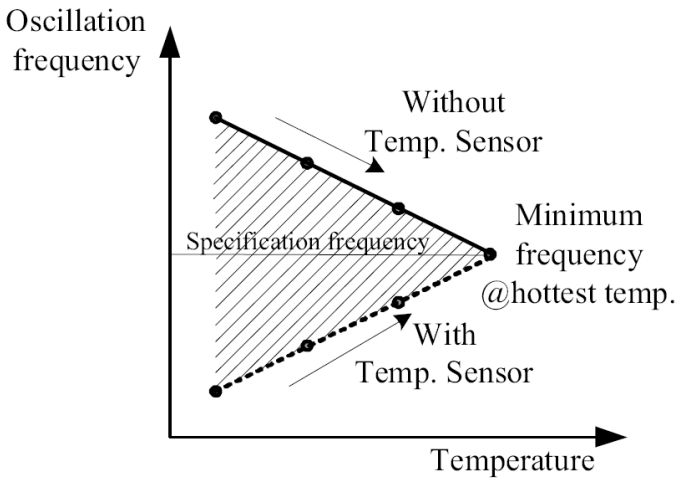


Figure 2.22. The oscillation frequency of ring oscillator with and without temperature-driven control scheme for self-refresh of DRAM

Fig. 2.23 depicts the circuit implementation of the self-refresh control scheme for a mobile DRAM with a temperature sensor.

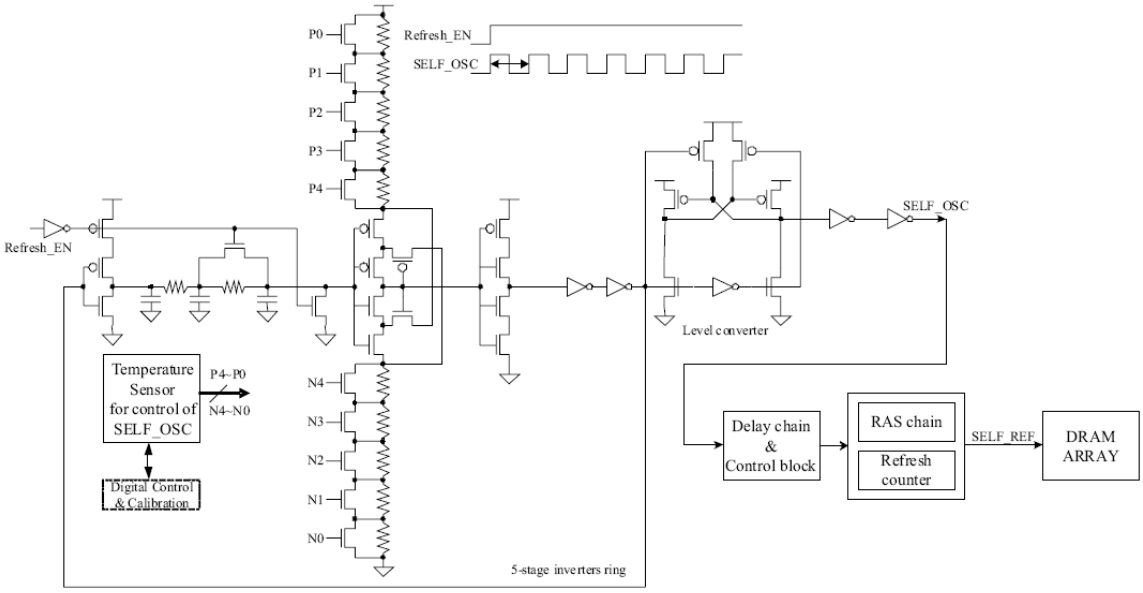
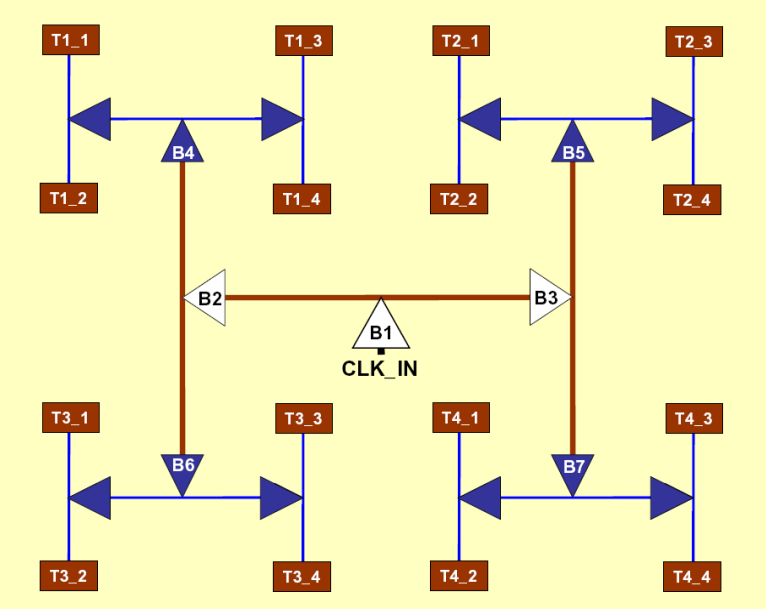


Figure 2.23. Circuit diagram of DRAM self-refresh control scheme with temperature sensor

2.4.2 Thermally Robust Clocking Schemes for 3D Integrated Circuits

3D integration of multiple active layers into a single chip is a viable technique that greatly reduces the length of global wires by providing vertical connections between layers. However, dissipating the heat generated in the 3D chips possesses a major challenge to the success of the technology and is the subject of active current research. Since the generated heat degrades the performance of the chip, thermally insensitive/adaptive circuit design techniques are required for better overall system performance. A thermally adaptive 3D clocking scheme that dynamically adjusts the driving strengths of the clock buffers to reduce the clock skew between terminals [2.18].

For the synchronous part of a 3D chip, which may be distributed across layers, skewless clock signal is of utmost importance for the accuracy and speed of operation of a design. Since the clock network spans over most parts of the chip and thereby gets exposed to as diverse temperature range as occurs across the chip, the effect of temperature is very pronounced in clock trees. Fig. 2.24 shows an H-tree for a single layer of a 3D chip where we can see that for a number of physically close terminals the clock signals traverse through entirely different temperature zones to reach the terminals which can lead to significant skew between these terminals.



$\Delta T(^oC) \rightarrow$	0	20	40	60	80
Skew (ps) $\rightarrow$	0	26.5	57.7	102.0	160.0

Figure 2.24.Temperature effect on rising edge skew between buffers T3_4 and T4_2.

Fig. 2.25 implements the via topology clock tree with the clock buffers on a single layer and using interlayer vias the clock signals from the terminals of the clock tree are passed to all other layers.

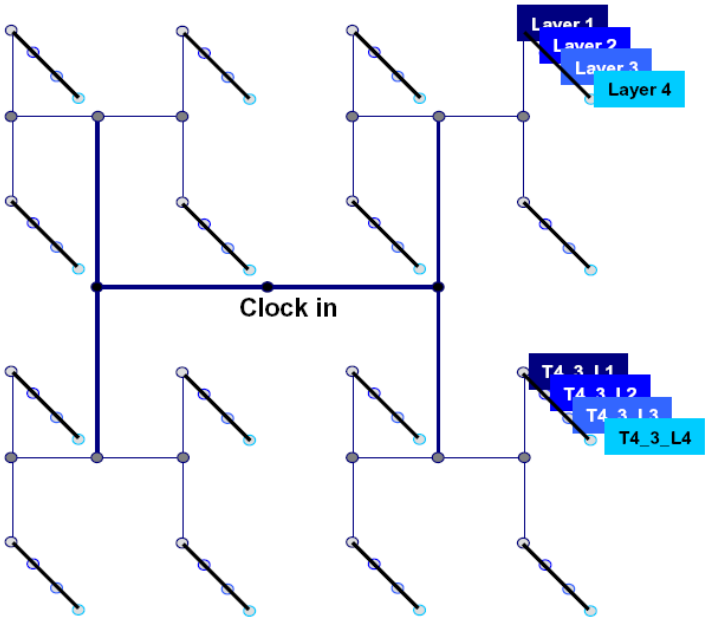


Figure 2.25. 3D clock tree with via.

An adaptive circuit scheme was presented to reduce the variation of the clock skew with temperature gradient in the 3D design in Fig. 2.26. The temperature sensors sense the ambient temperatures and convert the temperatures to voltages that are processed by a wave shaping circuitry and finally used for dynamically changing the driving strengths of the clock buffers to reduce the overall skew.

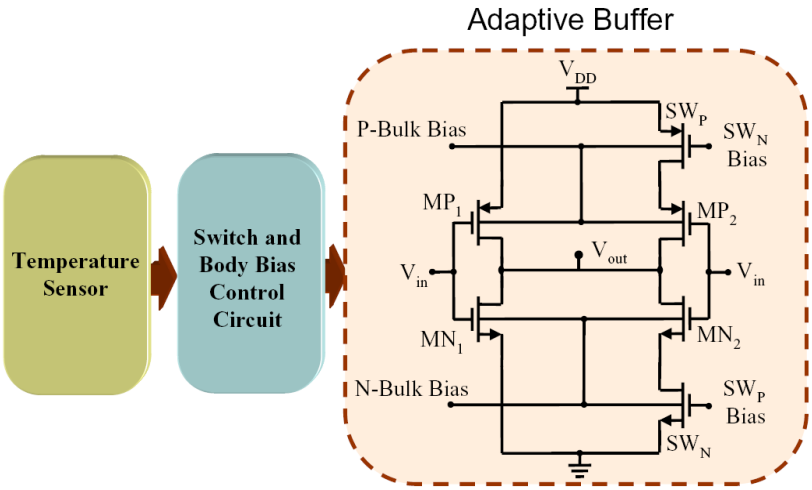


Figure 2.26. Thermally adaptive buffer schematic.

2.4.3 A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on VLSI Systems

A novel design method to minimize the leakage power during standby mode using a novel adaptive supply voltage and body-bias voltage generating technique for nanoscale VLSI systems [2.19]. The minimum level of V_{DD} and the optimum body-bias voltage are generated for different temperature and process conditions adaptively using a lookup table method based on the PVT monitoring and controlling systems shows in Fig 2.27. The process, voltage, and temperature (PVT) variations are monitored and controlled independently by their own dedicated systems shows in Fig 2.28. The subthreshold current as well as gate-tunneling and band-to-band-tunneling currents are monitored and minimized adaptively by the

optimally generated body-bias voltage.

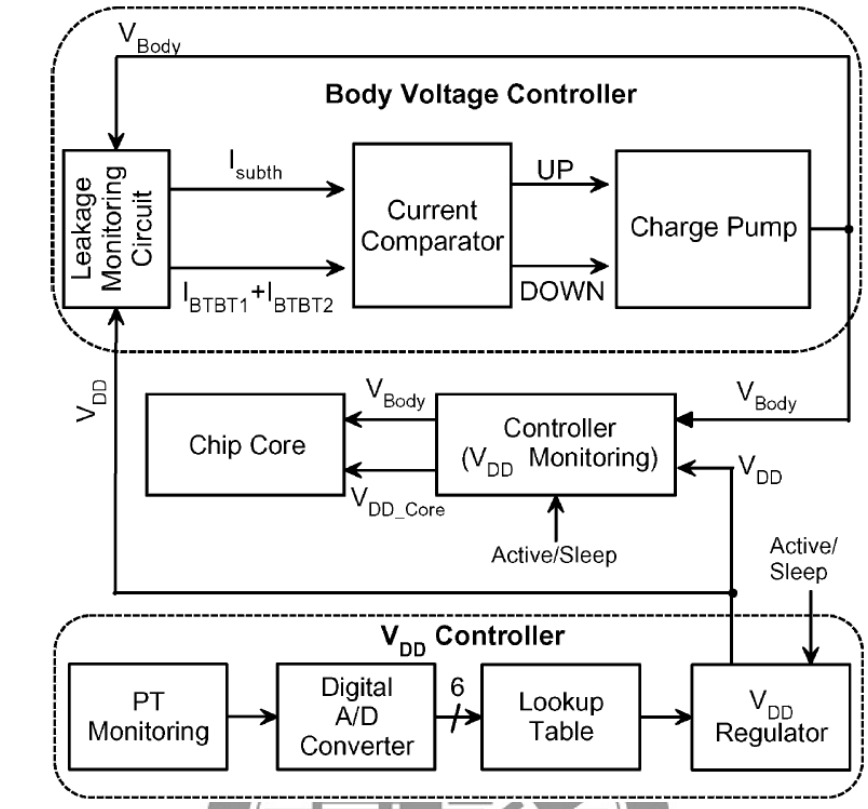
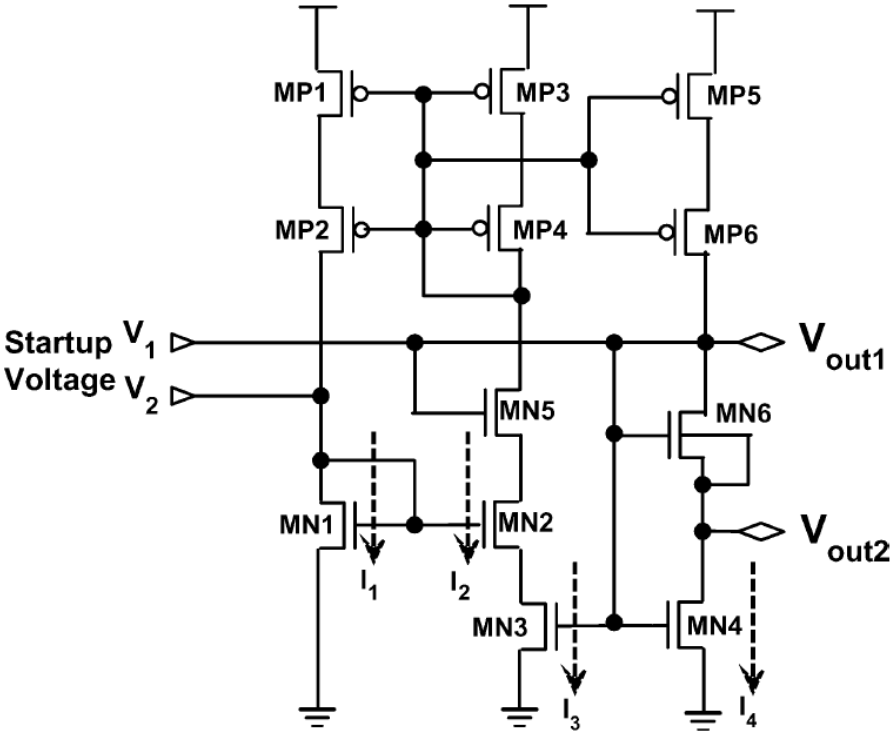
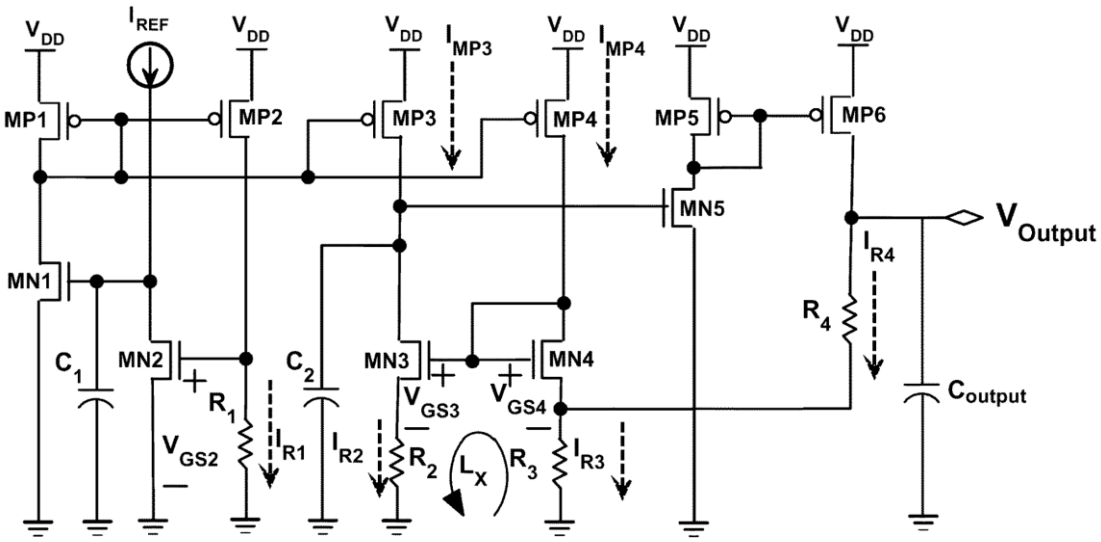


Figure 2.27. Block diagram of V_{DD} and V_{BODY} control system



(a)



(b)

Figure 2.28. (a) Temperature monitoring circuit. (b) Process monitoring circuit.

2.5 Summary

Process, voltage, and temperature variability has become a fundamental challenge in nanometer technologies. This trend is driven by: a) Moore's law, which governs the exponential growth of transistors in ICs, b) the low-power requirements of mobile devices (i.e., Vdd < 0.5V), and c) the shrinking geometries of advanced CMOS technologies reaching the sub-nanometer dimensions. Therefore, understanding PVT variability is a key to successfully designing ultra-low-power multi-million-gate systems on-a-chip. In this chapter introduces the previous of PVT sensors in power management system. Conventional on-chip PVT sensors that measure PVT variability are described in this chapter.

Chapter 3 Fully On-Chip Process, Voltage, and Temperature Sensors

The past 20 years have seen enormous growth in the capability and ubiquity of digital integrated circuits. Today, it sometimes seems difficult to buy any product without them—even greeting cards have chips in them. In a short review paper like this, it is unfortunately impossible to mention (let alone describe) all of the great work that was done and published in the VLSI Circuits Symposium during this period. Time-to-Digital-Converter (TDC) is usually used to replace analog circuit. Its applications are gradually expanding such as a phase comparator of all-digital-PLL [3.1], [3.2], PVT sensors circuit [2.9]-[2.14], jitter measurement [3.3], modulation circuit and demodulation circuit as well as a TDC-based ADC [3.4]. The TDC will play more important role in nano-CMOS era because it is well-matched to implement with fine digital CMOS process; it consists of mostly digital circuits and as the switching speed increases, its performance is improved.

However, TDC converters are adopted in [3.5]. As a result, hundreds of inverters were required to obtain enough pulse delay to achieve sufficient temperature resolution. A DLL based temperature sensor has problems of occupying large area, consuming high power. In order to solve these problems, the frequency-to-digital converter (FDC) based smart PVT sensors are proposed in this chapter. The proposed FDC exhibits simple and efficient feature in the process of measuring PVT variation and converting it to digital value. Compared to previous work, the proposed PVT sensors are small-area, low-power, and high performance.

3.1 Time to Digital Converter (TDC) Architecture

A Time-to-Digital-Converter (TDC) is to measure the interval time between two signals, and its time resolution of several pico seconds is achieved when it is implemented with advanced CMOS process. The next will introduce two types of TDC architecture.

3.1.1 Basic TDC Architecture

Fig. 3.1 shows configuration of a basic TDC, where the reference CLK passes through a buffer line which consists of an inverter chain, and the delayed reference CLK signals are fed into Flip-Flops as their data input. Also the measured signal is fed into Flip-Flops as their clock signal. We obtain the outputs of the Flip-Flops as a thermometer code, according to the rise-edge-timing interval between the reference CLK and the measured signal, and the encoder transforms it into a binary code. Its time resolution is given as the gate delay T_d.

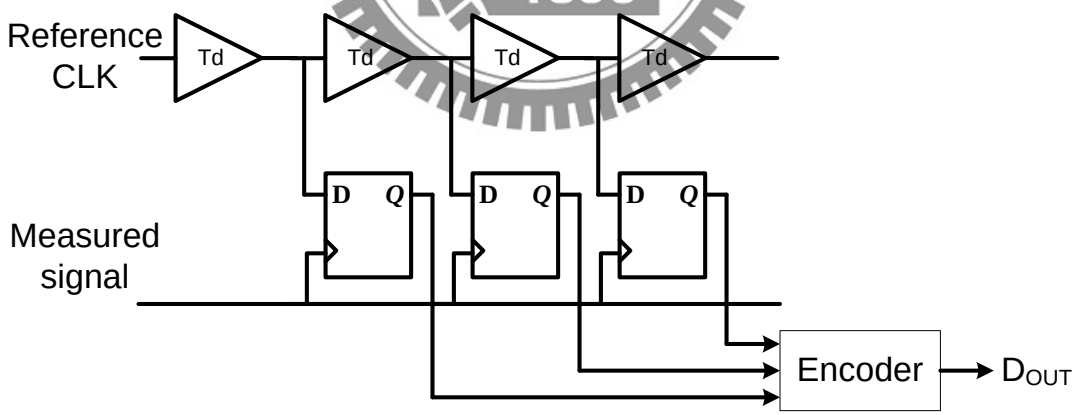


Figure 3.1 A basic TDC architecture.

3.1.2 Vernier Delay Line TDC Architecture

Fig. 3.2 shows a vernier delay line TDC which uses two delay lines: one is for the reference CLK with the buffer delay of T_{d1}. and the other is for the measured signal

with the buffer delay of T_{d2}. Its time resolution is given by $T_{d1} - T_{d2}$ (gate delay difference) which can be smaller than the basic TDC, but note that it uses 2N buffers (N buffers of T_{d1} and N buffers of T_{d2}) for the input range from 0 to $N(T_{d1} - T_{d2})$. A new calibration method for a Vernier-based time-to-digital converter (TDC) was presented [3.6]. The method eliminates the need for accurate external sources typically used for TDC calibration. Simulation and experimental results using a field programmable gate array platform indicate that the method can successfully be employed to calibrate high-resolution TDCs with reasonable accuracy.

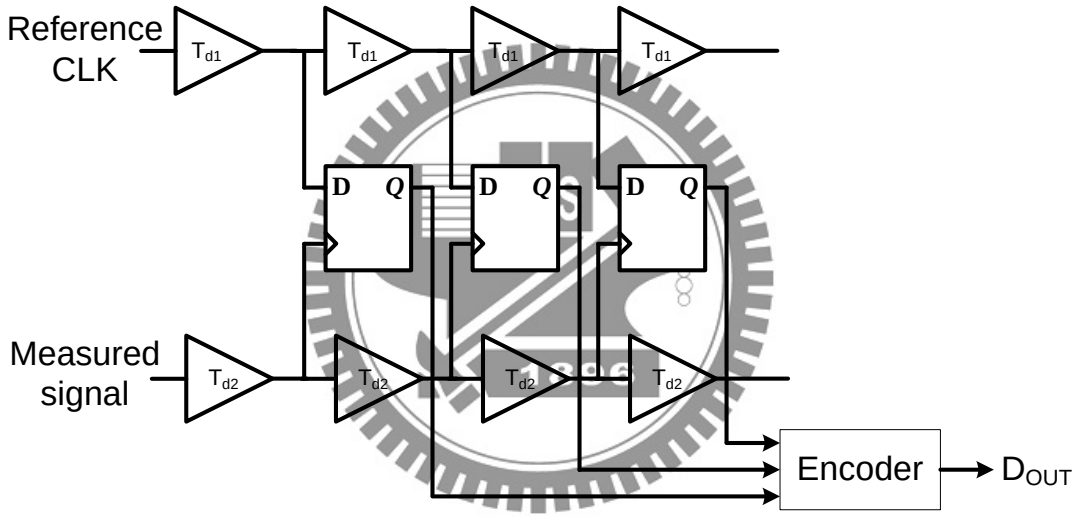


Figure 3.2 A vernier delay line TDC.

3.2 Frequency to Digital Converter (FDC)

A TDC based PVT sensors have problems of occupying large area, consuming high power. In this thesis, we propose frequency-to-digital converter (FDC) based PVT sensors with small area, low-power, and high-resolution. Fig. 3.3 shows the proposed frequency-to-digital converter (FDC) exhibits simple and efficient feature in the process of measuring PVT variations and converting it to digital value. PVT variations are measured by the frequency difference between the PVT variations

sensitive oscillator (PVTSO). The PVTSO are constructed from ring oscillators using a current starved delay cell.

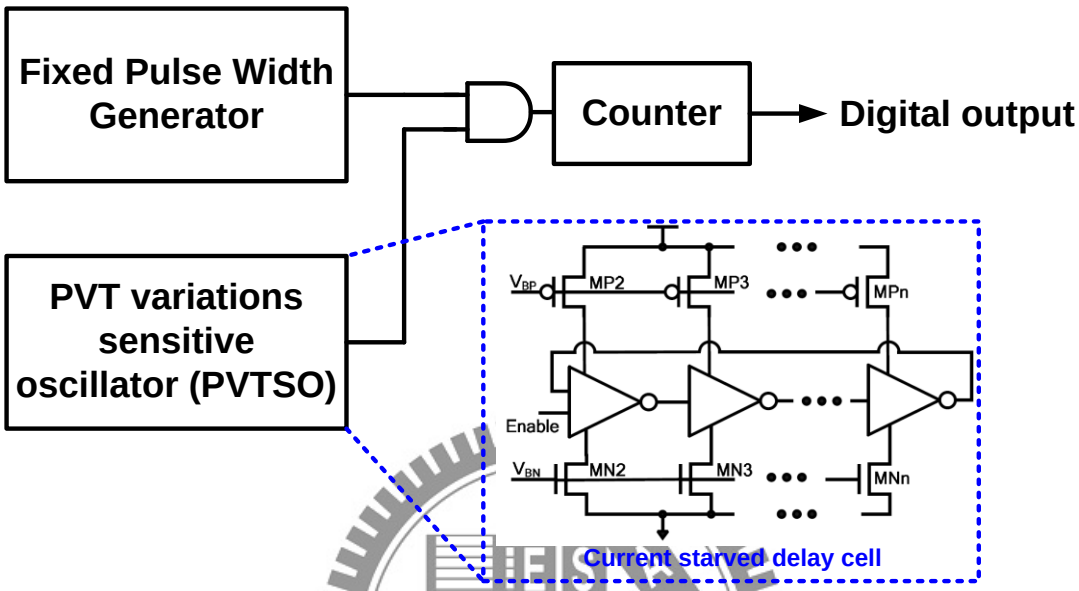


Figure 3.3 Frequency-to-digital converter (FDC) Architecture.

3.3 Fixed Pulse Width Generator

The proposed fixed pulse generator generates a pulse signal width independent of PVT variation. The detail schematic of the fixed pulse generator is drawn in Fig. 3.4. It is composed of D-type flip-flop, counter and comparator. When START signal rises, over a delay time (Td1), the output of D-type flip-flop also rises. When “result” signal rises, over a delay time (Td2), the output of D-type flip-flop will be reset to 0. The delay time Td1 and Td2 both affected by similar PVT variation, so it can be removed. From the above description, the output pulse signal width (W) is invariant from PVT variation. The simulation result of fixed pulse generator shows in Fig. 3.5. The circuit output pulse width is independent of PVT variation.

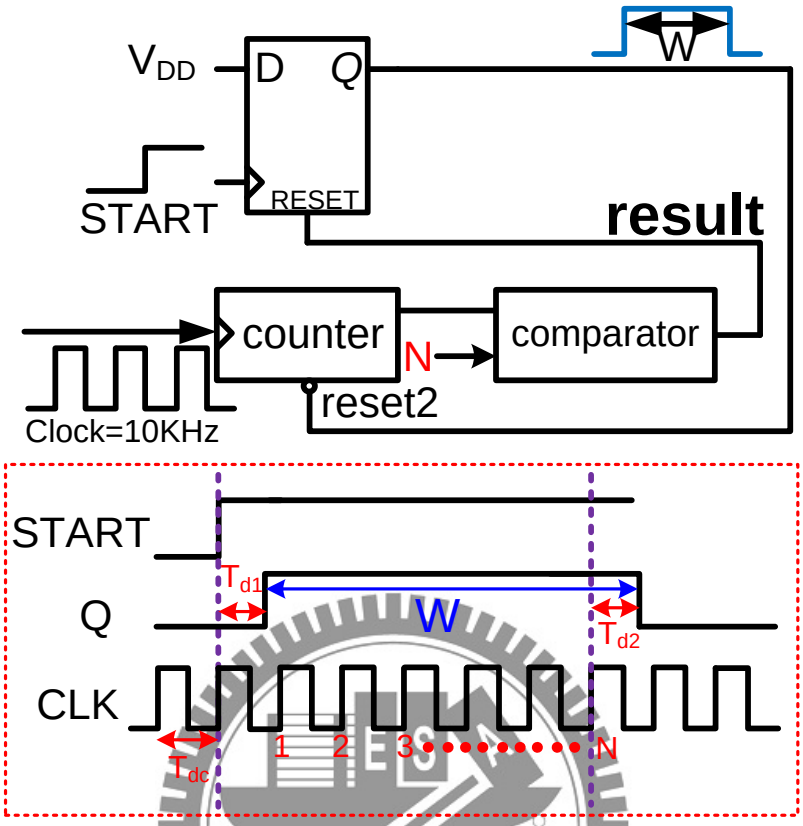


Figure 3.4 Fixed pulse generator block diagram and wave form.

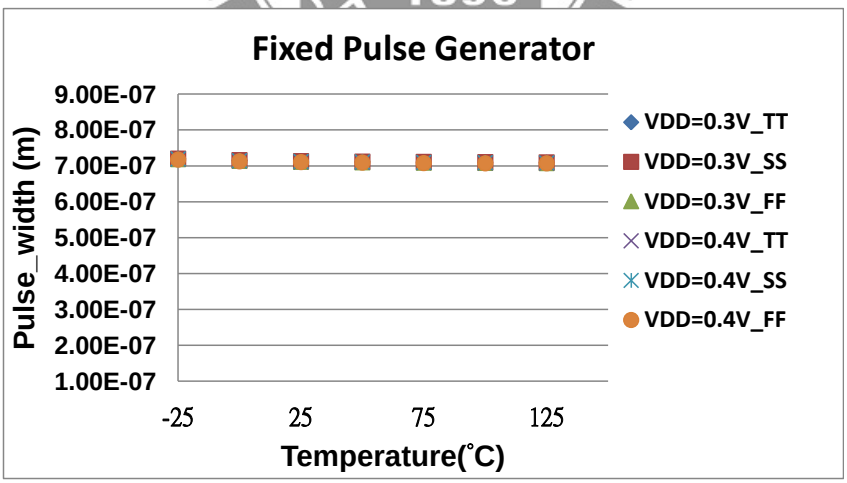


Figure 3.5 simulation result of fixed pulse generator.

3.4 Zero Temperature Coefficient Point Application – Process Sensor

A low power all-digital FDC-based process sensor circuit is proposed, and the circuit used ZTC characteristic to design. Section 3.4.1 introduces the effect of PVT variation in CMOS circuits. Section 3.4.2 introduces ZTC bias point of a MOS transistor. The architecture of all-digital process sensor and simulation results are presented in section 3.4.3.

3.4.1 PVT variation effects in CMOS circuits

In deeper submicron CMOS circuits design, PVT variations problem is more and more critical. In this section, the PVT variation effects are revealed.

MOS Current Equation in saturation mode

$$I_{DSAT} = I_{D0}\left(\frac{V_{GS} - V_T}{V_{DD} - V_T}\right)^{\alpha};$$

$$I_{D0} = (W/L)\frac{\mu_0}{[1+\theta(V_{GS}-V_T)][1+V_{DSSAT}/(E_C L)]} C_{OX} V_{D0}[V_{DD} - V_T - (\eta/2)V_{D0}];$$

$$\alpha = \frac{1}{\ln(2)}\ln\left(\frac{2V_{D0}[V_{DD} - V_T - (\eta/2)V_{D0}]}{V_{Da}[V_{DD} - V_T - \eta V_{Da}}\right);$$

$$V_{DSSAT} = E_{CL}\left\{\sqrt{1+\frac{2}{E_{CL}}\left(\frac{V_{GS}-V_T}{\eta}\right)} - 1\right\};$$

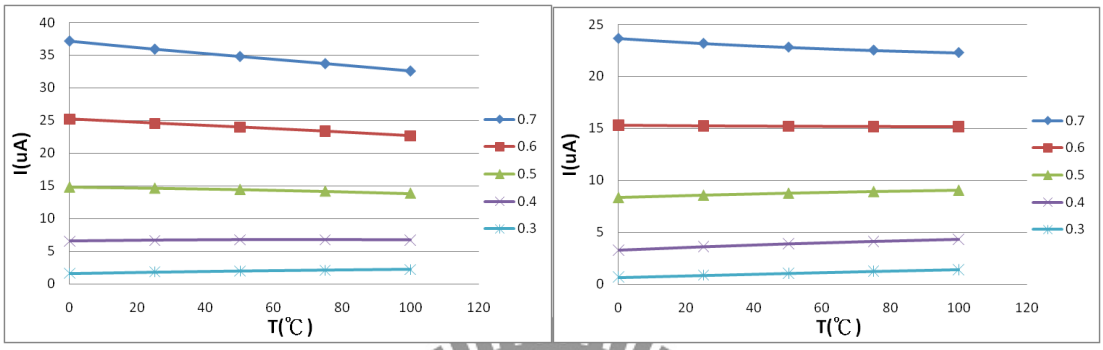
$$V_{D0} = V_{DSSAT}\,|_{V_{GS}=V_{DD}};\quad V_{Da} = V_{DSSAT}\,|_{V_{GS}=(V_{DD}+V_T)/2};$$

Figure 3.6 MOS current equation in saturation mode

MOS current varied with temperature, process, and voltage. Fig. 3.6 shows MOS current equations in saturation mode [3.7]. In the equations, I_{DSAT} is varied with

supply voltage (for V_{DD}), temperature (for mobility and V_T), and process (for W, L, C_{OX} and V_T). In different PVT situations, I_{DSAT} makes gate delay an inconstant value.

Fig. 3.7 is I_D – Temperature plot with supply voltage 0.5V, 0.4V, 0.3V. The current variation caused by temperature gets 26.5% difference at 0.3V. Temperature variation should be taken care while low supply voltage configurations are used.



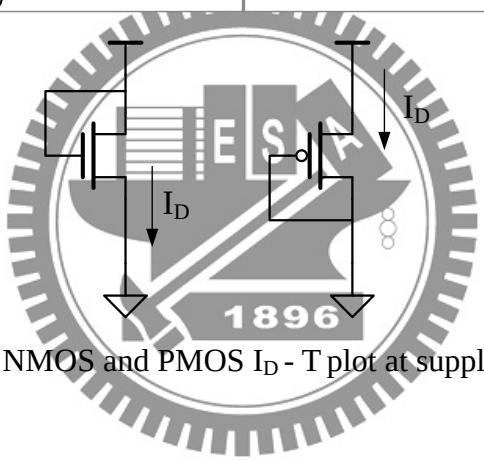


Figure 3.7 UMC90 NMOS and PMOS I_D - T plot at supply voltage 0.3~0.7V.

3.4.2 Zero Temperature Coefficient Point

Mutual compensation of mobility and threshold voltage temperature variations may result in a zero temperature coefficient (ZTC) bias point of a MOS transistor. The ZTC effect has been used in many applications, for instance, voltage reference circuits and temperature sensor.

The n-channel transistor drain current equation

$$I_d = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{gs} - V_T)^2 \qquad (3.1)$$

The carrier mobility and the threshold voltage decrease with temperature. Make a partial differential on both side of (3.1) equation, and at the ZTC point $(\partial I_d)/(\partial T) = 0$.

We can find the bias voltage such that the drain current I_d would not vary with temperature T

$$V_{GS} = V_T(T_1) + \left[2\mu_n \frac{\partial V_T / \partial T}{\partial \mu_n / \partial T} \right] \Big|_{T = T_1} \tag{3.2}$$

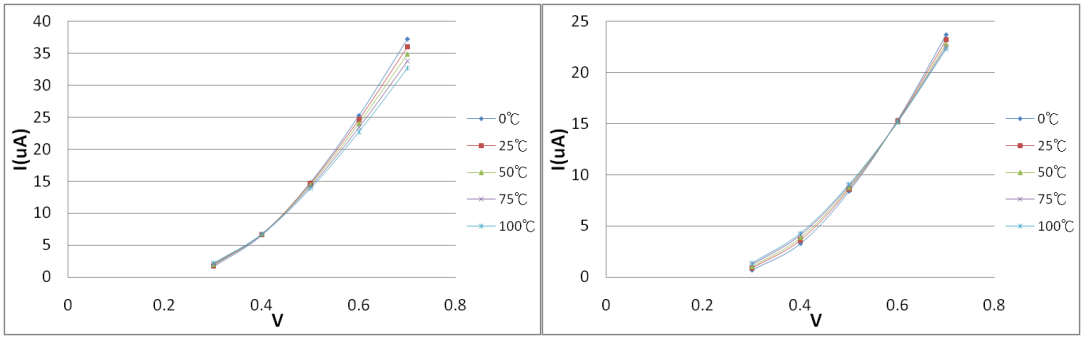


Figure 3.8 ZTC points of UMC90 NMOS and PMOS transistor are at about 0.4V and 0.6V.

In Fig. 3.8, in UMC90 process, the ZTC points of NMOS and PMOS are at about 0.4V and 0.6V respectively. With the ZTC point, one may be able to create a logic gate with almost constant delay at a specific voltage point. The application of ZTC point is in the next section that a ring oscillator's period varies less with temperature.

3.4.3 ZTC Point Application – Process Sensor

A ZTC application is shown in this section. Although the NMOS and PMOS's ZTC point are at different V_{GS}, with proper sizing, there is a V_{GS} point that the ring oscillator's period would vary less with temperature in process corners FF, TT, SS. In Fig. 3.9, at 0.5V, NMOS I_D decreases with T, PMOS I_D increases with T. The PMOS and NMOS mutual current compensation results in a ring oscillator's period are constant.

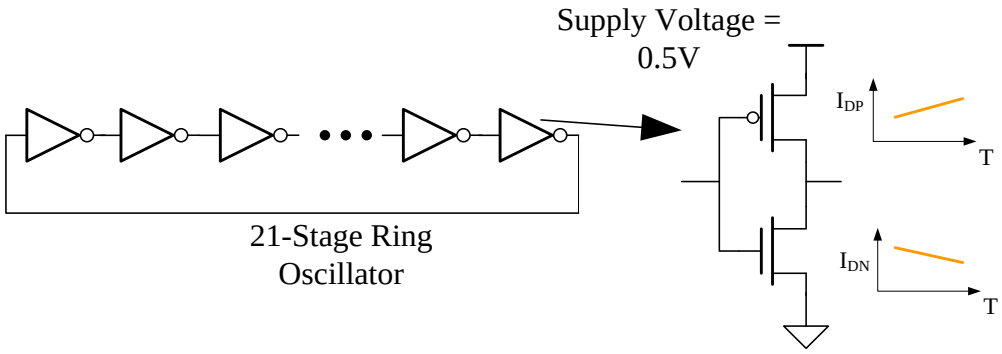


Figure 3.9 At 0.5V, NMOS I_D decreases with T, PMOS I_D increases with T.

Fig. 3.10 is the testing result of a ring oscillator's frequency, at 0.5V, in process corners FF, TT, and SS. The NMOS and PMOS's width/length both are 120nm/90nm. Fig. 3.11 is the process monitor circuit, it can detect process variation in different corner. Finally, I use counter to convert the ring oscillator's frequency to 4-bit digital output. The output value will change with process variation, and the simulation result shows in Fig. 3.12.

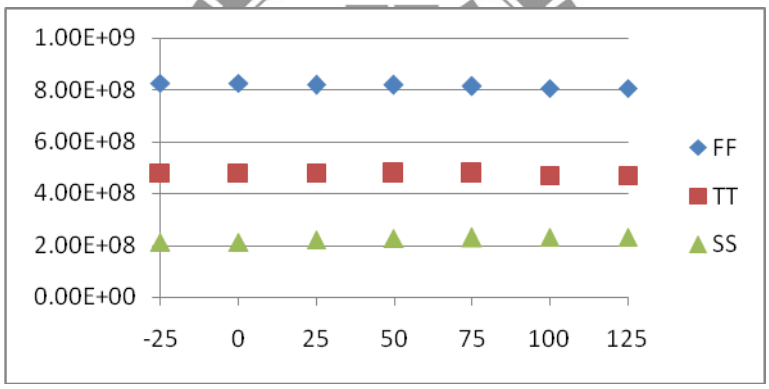


Figure 3.10 Ring oscillator's frequency – temperature plot in corners FF, TT, SS.

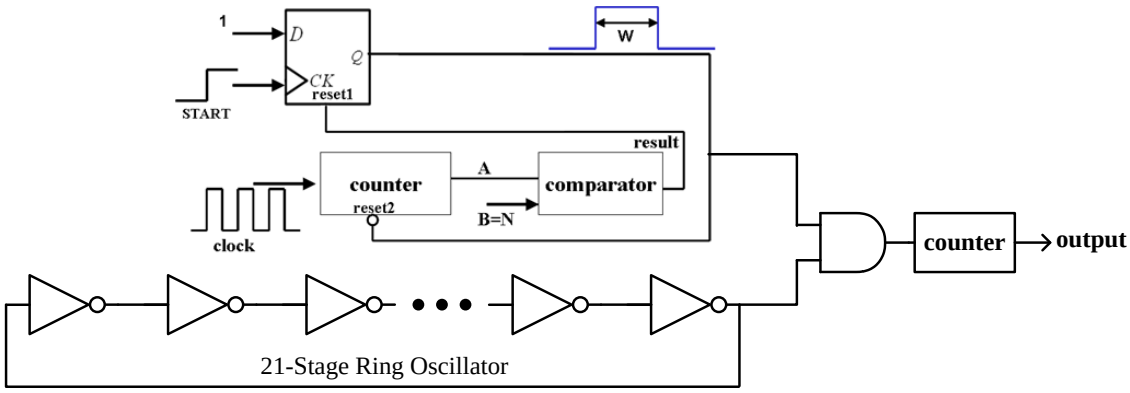


Figure 3.11 Process Monitor circuit.

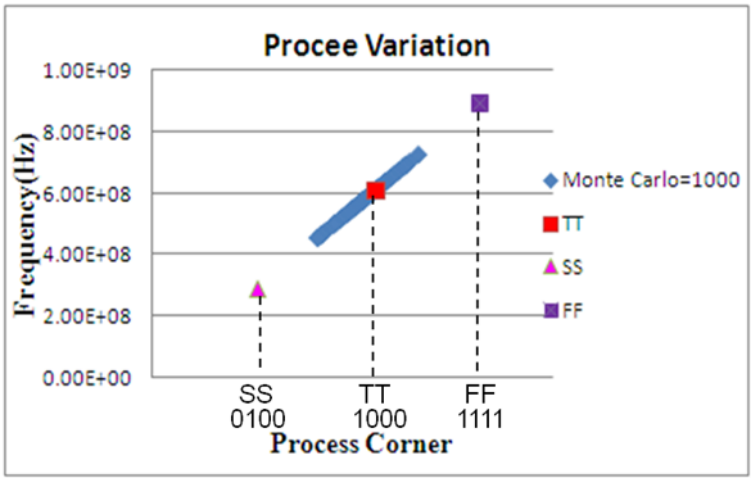


Figure 3.12 Ring oscillator's frequency with process variation.

3.5 A Fully Digital Voltage Sensor Using A New Delay Element

The conventional ADC, however, consists of conventional op amplifier. Cascode architecture of conventional op amplifier did not have enough headroom, so it is difficult to design at sub-1V.

One way to overcome the challenge of the low-power and low-voltage design is to process the signal in time-domain. In time-based ADC converter, the input analog voltage is converted to time or phase information. Thus, digital ADC circuit was presented in [2.3]. The circuit can replace conventional analog ADCs, and it can reach low-power, low-voltage, and small area. However, the digital ADC is not accuracy with PVT variation. Therefore, a novel fully digital ultra-low voltage sensor using a new delay element circuit is proposed to improve accuracy.

The proposed voltage sensor with 0.5V voltage reference is presented in this paper, shows in Fig. 3.13. It converts input voltage to 5-bit digital code V[4:0]. The proposed voltage sensor consists of current starved inverters, flip-flops, and XOR gate. The

control bit is from process monitor, and it can reduce the voltage sensor output error. The control bit can compensate process variation, and Table 3.1 represents the V[4:0] with different voltage. The quantization step of voltage sensor is about 50mv.

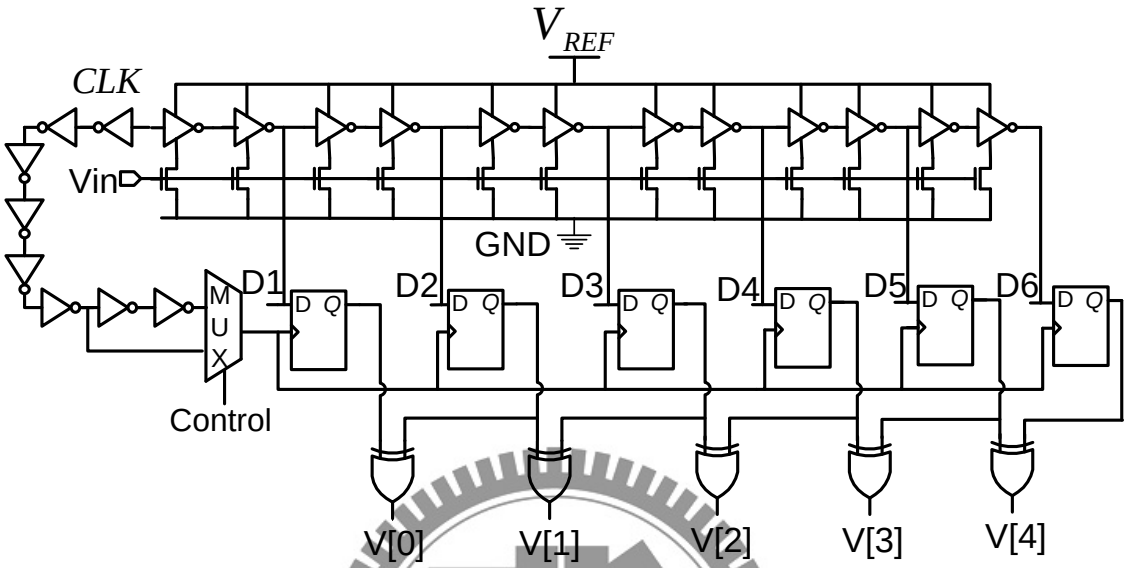


Figure 3.13 A fully digital voltage sensor.

Table 3.1 Voltage Sensor Digital Code Table

V_{in}	Digital Code				
	V[0]	**V[1]**	**V[2]**	**V[3]**	**V[4]**
0.3	1	0	0	0	0
0.35	0	1	0	0	0
0.4	0	0	1	0	0
0.45	0	0	0	1	0
0.5	0	0	0	0	1

3.6 Fully On Chip Ultra-Low Voltage Temperature Sensor

The proposed temperature sensor, it shows in Fig. 3.14. The bias current generator shows in Fig. 3.15, and N1, N2 transistors operate in weak inversion region. Alpha-power subthreshold drain current *(I_{D_SUB})* [3.7] can be expressed as follows:

$$I_{D\_SUB} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{(V_{GS}-V_{th})/mV_T} \times (1-e^{-V_{DS}/V_T}) \quad (3.3)$$

Assume $V_{DS}>>V_T$, The term of $(1-e^{-V_{DS}/V_T})$ can be ignored. Simplification of the formula can be expressed based on the following:

$$I_{IN} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{(V_{GS1}-V_{th})/mV_T} \quad (3.4)$$

$$I_{OUT} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{(V_{GS2}-V_{th})/mV_T} \quad (3.5)$$

Assume

$$I_O = \mu_0 C_{OX} \frac{W}{L}(m-1) \quad (3.6)$$

P_1 and P_2 are current mirror.

$$\frac{I_{P1}}{I_{P2}} = \frac{W_{P1}/L_{P1}}{W_{P2}/L_{P2}} = \frac{I_{IN}}{I_{OUT}} \quad (3.7)$$

Simplification (3.4) and (3.5) into (3.8) and (3.9), the equation becomes

$$V_{GS1} = mV_T \times \ln\left(\frac{I_{IN}}{I_{ON1}}\right) + V_{th} \quad (3.8)$$

$$V_{GS2} = mV_T \times \ln\left(\frac{I_{OUT}}{I_{ON2}}\right) + V_{th} \quad (3.9)$$

And

$$\frac{I_{ON1}}{I_{ON2}} = \frac{W_{N1}/L_{N1}}{W_{N2}/L_{N2}} \quad (3.10)$$

Combine (5)-(8) into (9), the equation becomes

$$I_{OUT} = \frac{V_{GS1} - V_{GS2}}{R}$$

$$= \frac{mV_T \times \ln\left(\frac{I_{IN} \times I_{ON2}}{I_{OUT} \times I_{ON1}}\right)}{R} = \frac{mV_T}{R} \times \ln\left(\frac{W_{p1}W_{N2} / L_{P1}L_{N2}}{W_{P2}W_{N1} / L_{P2}L_{N1}}\right) \quad (3.11)$$

If, $L_{P1} = L_{P2} = L_{N1} = L_{N2}$

$$I_{OUT} = \frac{mV_T}{R} \times \ln\left(\frac{W_{p1}W_{N2}}{W_{P2}W_{N1}}\right) \quad (3.12)$$

The output current of the bias current generator is proportional to temperature, as described in equation (3.12). The output current is used to charge the inverters, so the frequency of ring oscillator is also proportional to temperature. All of above mentioned characteristics have perfect linearity. The fixed pulse generator generates a pulse signal width independent of PVT variation. The ring oscillator output and fixed pulse through 2-AND gate, and the output frequency digital code connects to “clock” pin of counter, and the counter can be positive edge triggered generating the corresponding digital output T[9:0]. The output T[9:0] represents the corresponding environmental temperature, and T[9:0] will be adjusted by proposed PV sensor to reduce the error caused by PV variation.

When the supply voltage is 0.5V~1V, a voltage regulator was presented to generate output voltage below 0.5V. Thus, the output of voltage reference provides a voltage source to temperature sensor. The simulation result with process and voltage variation is shows in Fig. 3.16.

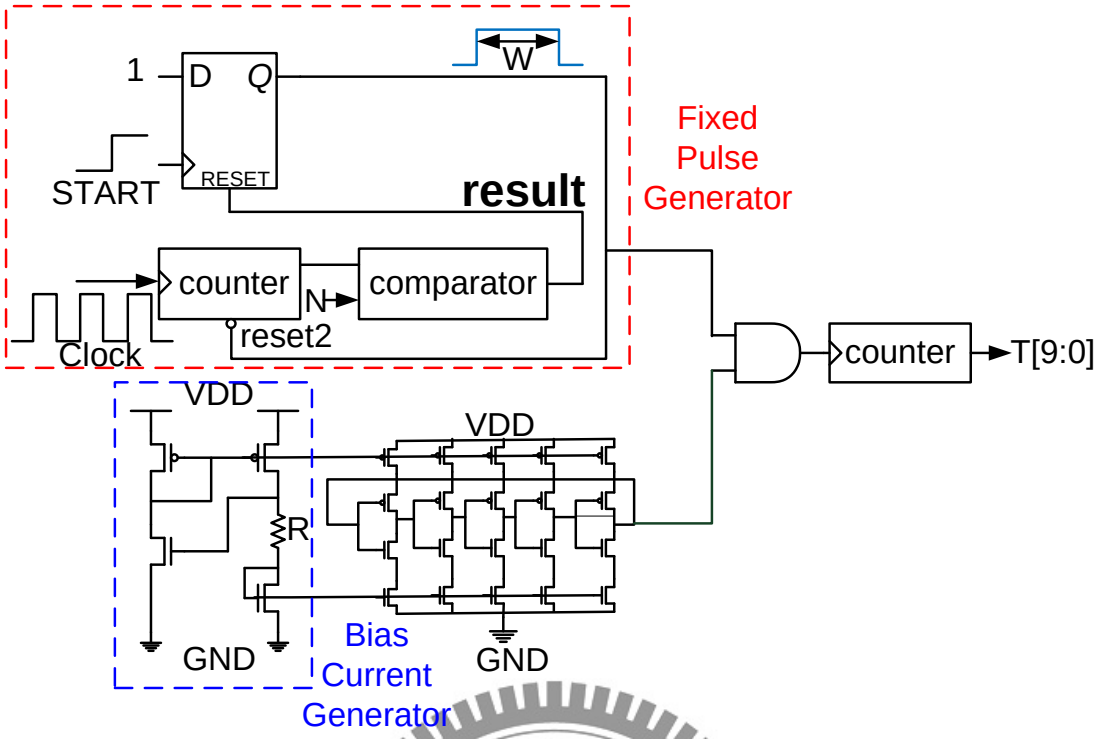


Figure 3.14 Proposed fully on chip temperature sensor.

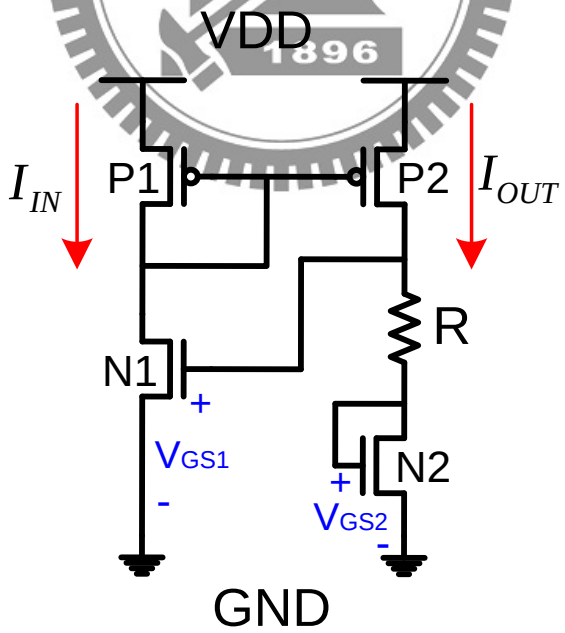
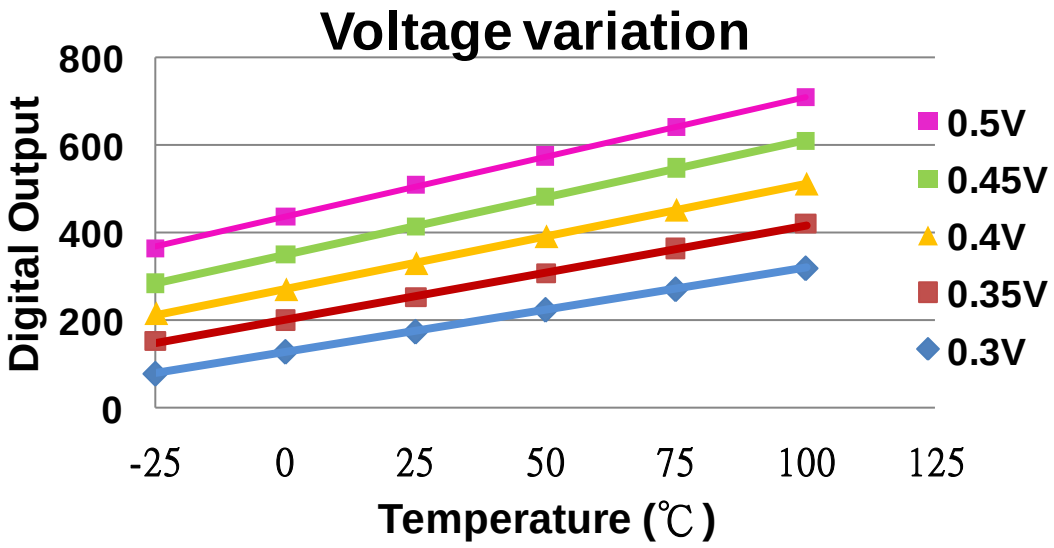
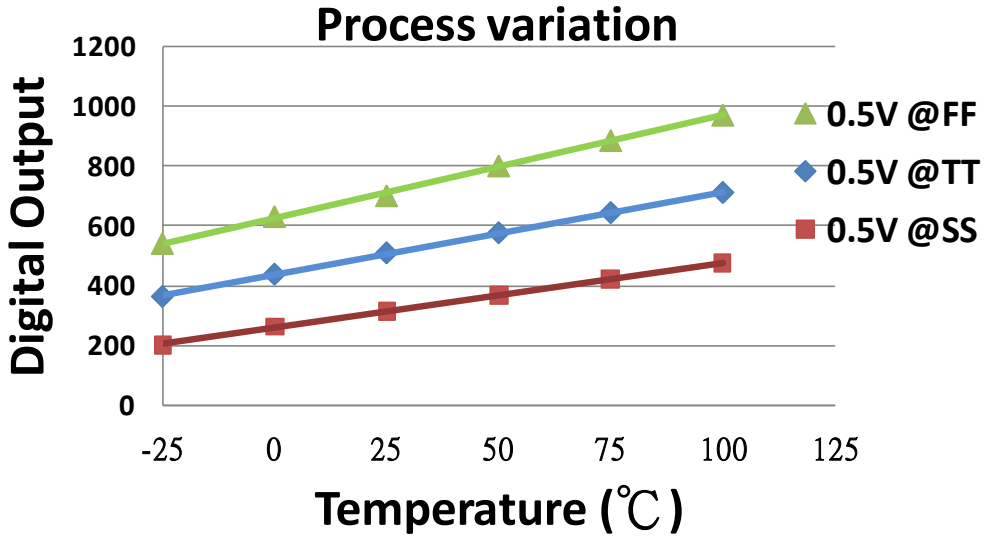


Figure 3.15 Bias current generator.



(a)



(b)

Figure 3.16 (a) Simulation result of temperature sensor with voltage variation. (b) Simulation result of temperature sensor with process variation.

3.7 1-point Calibration Method of Proposed Temperature Sensor

Fig. 3.16 shows the simulation result of temperature sensor with process and voltage variation. We choose 1-point calibration (a.k.a linear calibration) method to compensate the output of this sensor. The calibration selects one point in the range of

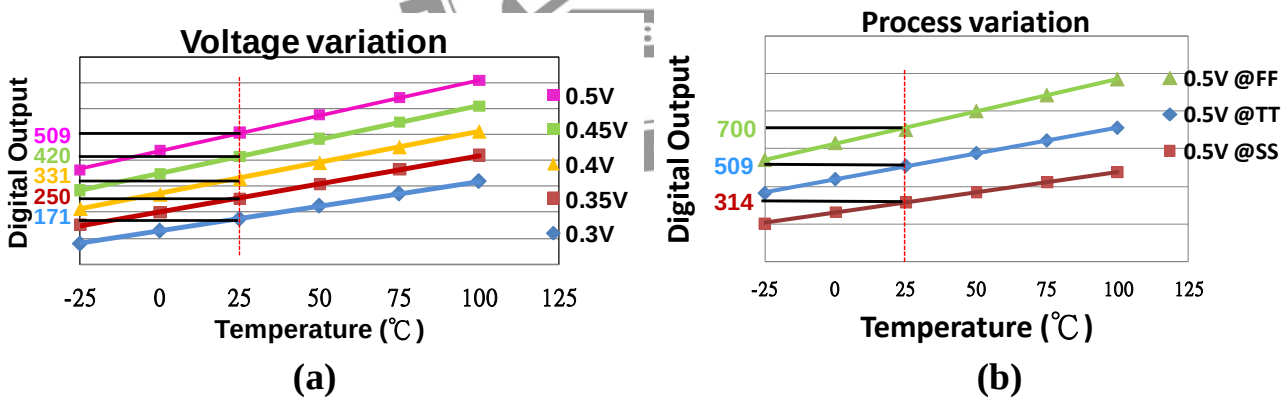
a data logger or chart recorder and setting it to give an identical reading as the same point.

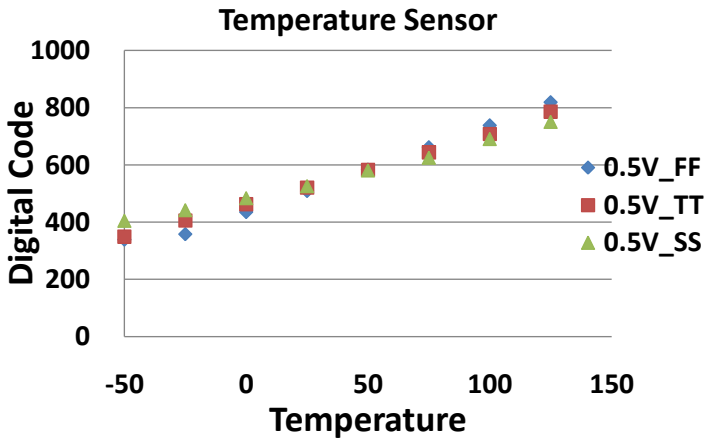
Frequency of ring oscillator varies with both voltage and process shows in Fig 3.17(a)-(b). Proposed sensor calibrates out the process dependency with a frequency measurement at one temperature. First, we record the digital output D(25℃,TT)=509 at 25℃ and TT corner from Fig 3.17. Then we measure digital output D(25℃,P) at 25℃ and unknown process corner P. Then we record the difference P_0 between D(25℃,P) and D(25℃,TT).

$$P_0 = D(25℃, P) - D(25℃, TT) = D(25℃, P) - 509 \tag{3.13}$$

Finally, we measure digital output D(T,P) at an unknown temperature T and unknown process corner P. Through the 1-point calibration, the digital output D_C(T,P) shows in Fig.3.17(c) can be expressed as

$$D_C(T, P) = D(T, P) - P_0 \tag{3.14}$$





(c)

Figure 3.17 (a) Simulation result of temperature sensor with voltage variation.

(b) Simulation result of temperature sensor with process variation.

(c) 1-point calibration method of proposed temperature sensor.

1-point calibration method hardware implementation of the proposed scheme is introduced to compensate for the voltage and process variations on the impact of temperature. The proposed calibration circuit is shown in Fig. 3.18.

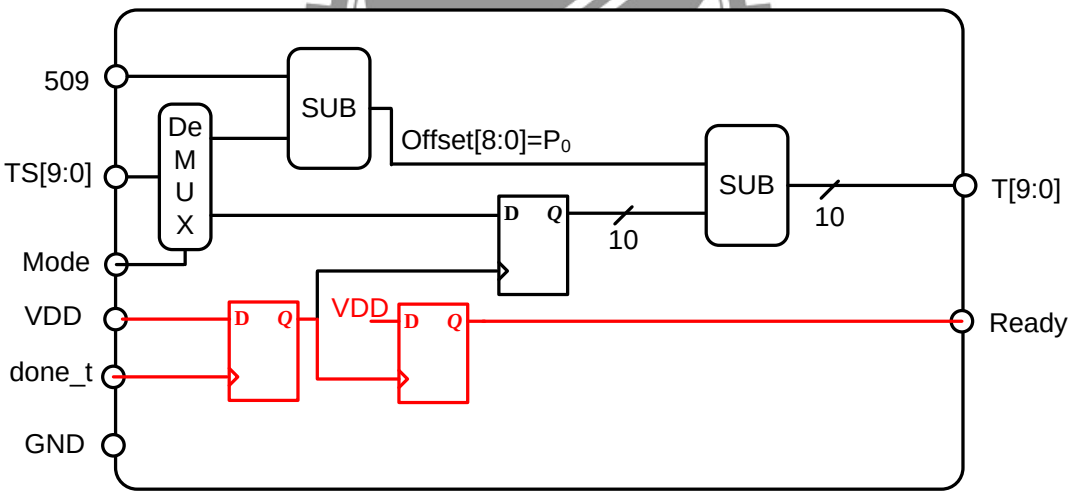


Figure 3.18 1-point Calibration Method of Temperature Sensor.

3.8 Conclusion and Simulation Results

From the previous section, we proposed a fully on chip ultra-low power PVT sensors in Fig. 3.19. The sensor without analog-to-digital converter (ADC) or bandgap reference is proposed for high accuracy, ultra-low power, and wide voltage

range portable applications. Conventional temperature sensors rely on ADCs for digital output code conversion. The proposed temperature sensor generates a clock frequency proportional to the measured temperature, and converts the frequency into a corresponding digital code T[9:0]. A voltage sensor and process sensor are proposed to compensate temperature sensor. The sensor was designed in a 65nm CMOS technology. It operate over a wide voltage range from 0.3V~1V. The power consumption is under 3.7μW at 0.3V and a sample rate of 10k samples/sec. The temperature error is merely -0.8~0.8℃ shows in Fig. 3.20.

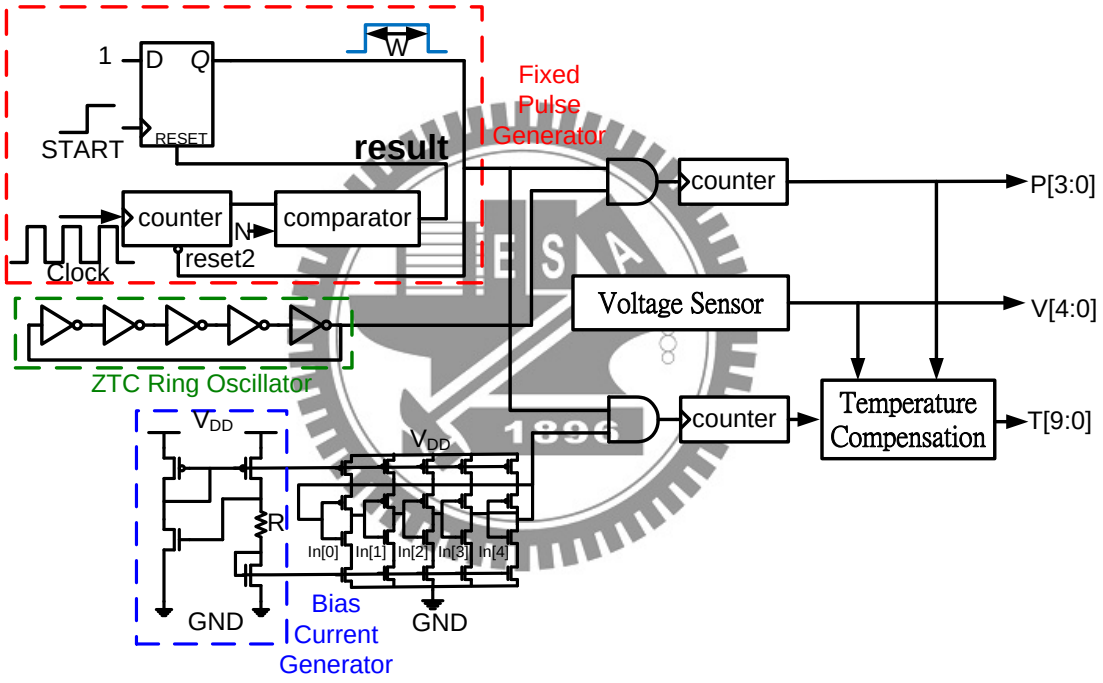


Figure 3.19 Proposed fully on chip PVT sensors

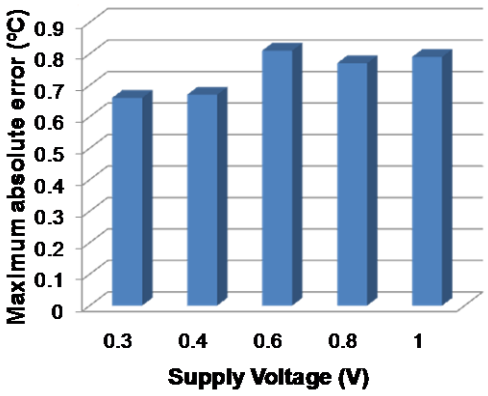


Figure 3.20 Maximum absolute error of proposed temperature sensor.

3.9 Summary

A process, voltage, and temperature (PVT) sensor without a voltage/current analog-to-digital converter (ADC) or bandgap reference is proposed for high accuracy, low power, and wide voltage range portable applications. Conventional temperature sensors rely on voltage/current ADC for digital output code conversion. The proposed temperature sensor generates a clock frequency proportional to the measured temperature, and converts the frequency into a corresponding digital code. The generated digital code is still under the influence of PVT variations. Two distinct sensors for voltage and process monitoring are also proposed to enhance temperature sensor environmental variation immunity. The property of zero temperature coefficient (ZTC) bias point is used to remove temperature effect. It is capable of operating over a wide voltage range within 0.3V~1V. The power consumption is no more than 3.7W at 0.3V supply voltage and a high sample rate of 10k samples/sec. The temperature error is merely -0.8~0.8℃.

A comparison chart between this work and previously presented temperature sensors is shown in Table 3.2. In Table 3.2, the main characteristics, such as operation supply voltage, power, error, temperature range, sensor type, process technology, and conversion rate are compared.

Table 3.2 Temperature sensor comparisons

Sensor	Supply(V)	Power(μW)	Error(℃)	Sensor Type	CMOS Technology	Conversion rate (samples/s)
[2.7]	3.0	4.5	-0.6~+0.6	Temp-to-Pulse	0.35um	10
[2.9]	3.0	10	-0.7~+0.9	Temp-to-Pulse	0.35um	10k
[2.10]	1.0	25	-1.0~+0.8	Analog Voltage	90nm	4
Fully on chip PVT sensors	**0.3~1**	**3.7@0.3V**	**-0.8~+0.8**	**Temp-to frequency**	**65nm**	**10k**

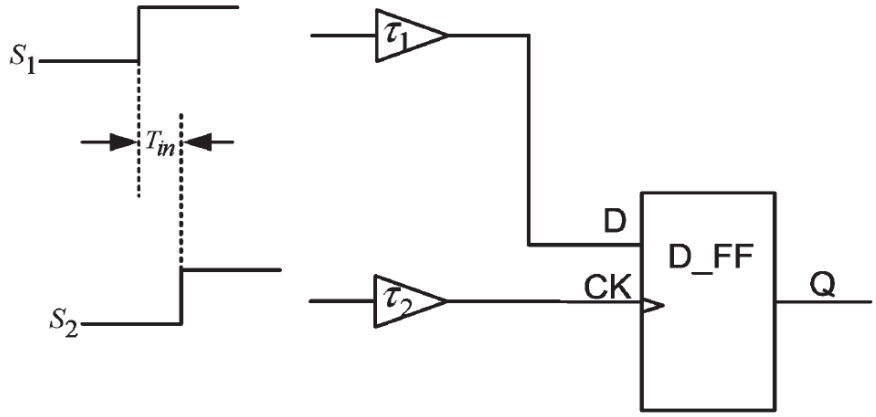
Chapter 4 Self-Calibration Method for Subthreshold All-Digital PVT Sensors

4.1 Previous TDC Calibration Method

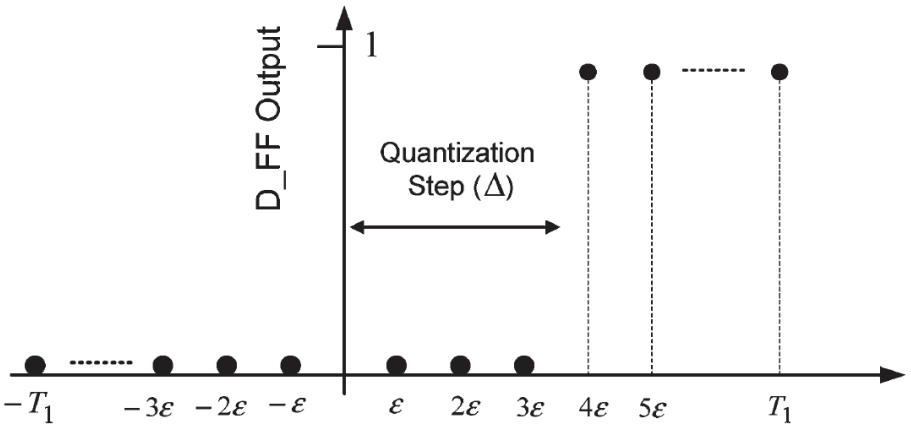
To calibrate a TDC, first, the duration of each quantization level is determined. Then, the actual characteristic curve representing the TDC is constructed based on the estimated size of each quantization level. The measurement error of the TDC is determined from its characteristic curve and compensated accordingly. Various TDC calibration methods have been proposed in the literature; the dominant methods are given here.

4.1.1 Direct Calibration

The concept of direct calibration is shown in Fig. 4.1, in which two signals with a precise delay difference of T_{in} are externally generated and applied to one stage of a Vernier-based TDC containing two buffers with delays of τ_1 and τ_2 and a D flip flop. If the input time interval Tin is increased in small steps ε over a sufficiently long interval of $(-T_1,+T_1)$, the output of the flip-flop generates a stream of "0"s and "1"s. Assuming an ideal D flip-flop, the difference between the total number of "0"s and "1"s divided by two determines the size of the quantization step, which is equal to $\Delta = \tau_2$-τ_1, where $\tau_2 > \tau_1$. The accuracy of this calibration method is highly dependent on the size and precision of ε.



(a)



(b)

Figure 4.1 (a) Typical setup for direct calibration of an arbitrator.

(b) Calibration result for an arbitrator with a quantization step of $\Delta = 4\varepsilon$.

4.1.2 Improved Direct Calibration Based on Added Noise

To ensure proper calibration of modern TDCs using the direct calibration method, ΔT has to be in the range of femtoseconds. This requirement can be alleviated to some extend by adding noise with a standard deviation of σ_{noise} to ΔT. Assuming that the standard deviation of the TDC delay elements are much lower than σ_{noise}, the sum of ΔT and the noise creates a set of time events that follow Gaussian distribution with a mean value of ΔT and a standard deviation of σ_{noise}. The addition of noise in this method increases the standard deviation of the quantization step and facilitates its

measurement. Using additive temporal noise, Levine and Roberts [4.1] reported TDC calibration down to 5 ps. This method requires an on-chip noise source with a relatively large standard deviation, which may not be easy to implement.

4.1.3 Indirect Calibration

The differences between the quantization steps of a VDL-based TDC can be determined through an indirect calibration method [4.2]. To illustrate this method, assume two periodic signals of S_1 and S_2 with periods of T_1 and T_2, where T_2 is slightly larger than T_1. The time difference between the rising edges of S_1 and S_2 is incremented by $\varepsilon = T_2 - T_1$ in every cycle. If one cycle of S_1 is observed over time, it can be seen that the rising edges of S_2 are uniformly distributed over that particular cycle of S_1. It can be shown that it takes a total number of $N = T_1/\varepsilon$ cycles for a rising edge of S_2 to sweep one full cycle of S_1. The difference between the rising edges of S_1 and S_2 can be considered as an input time interval that extends by $\varepsilon = T_2 - T_1$ in every cycle. Such a sequence of time events includes a total number of $N = T_1/\varepsilon$ distinct input intervals. Fig. 4.2 shows a two-stage Vernier-based TDC and its equivalent circuit in which two delay lines are replaced with a single delay line where $\Delta_1 = \tau_{12} - \tau_{11}$ and $\Delta_2 = \tau_{22} - \tau_{21}$. If a sequence of equally likely time events is applied to the circuit shown in Fig. 4.2(b), the outputs of the flip-flops can be represented by

$Q1 = 1$ and $Q2 = 1$ for $Tin < \Delta 1$ (4.1)

$Q1 = 0$ and $Q2 = 1$ for $\Delta 1 < Tin < \Delta 1 + \Delta 2$ (4.2)

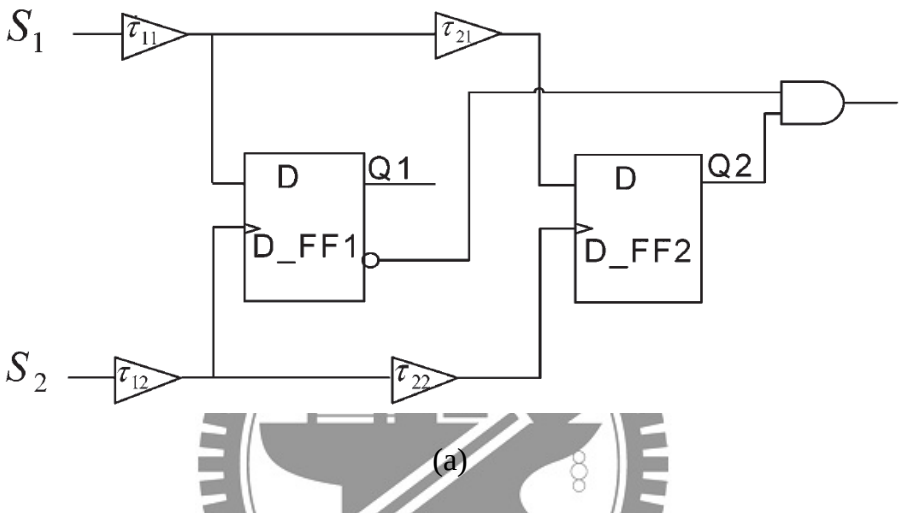
$Q1 = 0$ and $Q2 = 0$ for $Tin > \Delta 1 + \Delta 2$ (4.3)

The output of the AND gate in Fig. 4.2(b) remains high for all events falling in the range of $\Delta_1 < T_{in} < \Delta_1 + \Delta_2$ and becomes zero for the rest of the events. The fraction of time for which the output of the AND gate becomes high is equal to Δ_2/T_1, which repeats in each cycle of T_2. Therefore, the frequency of the AND gate output in Fig.

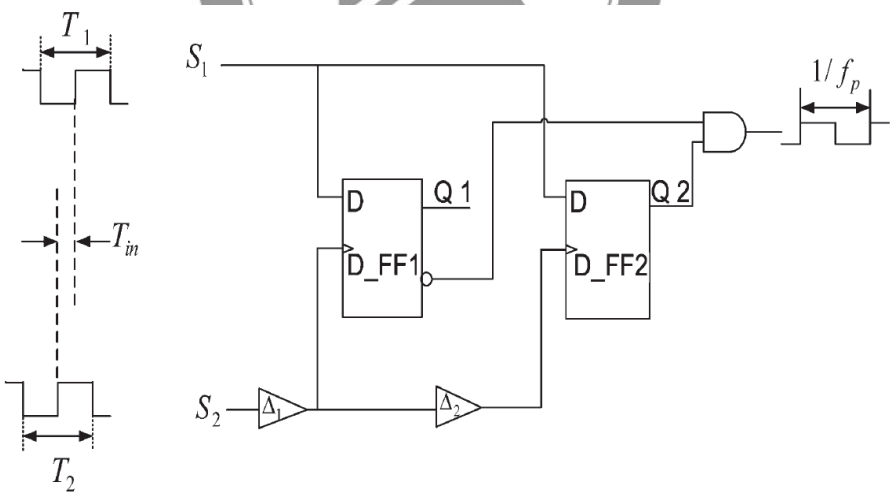
4.2(b) can be expressed by

$$f_p=\Delta_2 \; ; \; T_1 \times f_2=\Delta_2 \times f_1 \times f_2 \tag{4.4}$$

From (4.4), the quantization step of Δ_2 is determined through the measurement of f_p. To accurately calibrate a TDC with this method, the reference signals of S_1 and S_2 have to be very low jitter signals that are precisely aligned to generate accurate time events. These requirements are difficult to achieve in practice.



(a)



(b)

Figure 4.2 (a) Portion of a conventional VDL-based TDC. (b) Equivalent circuit containing a single delay line with an added AND gate for calibration.

4.1.4 Statistical Linearity Calibration

In [4.3], a statistical method of calibration is proposed, in which an independent ring oscillator is used to generate a sequence of equally likely time events within one period of a reference clock. If this sequence of events is applied to a TDC, it can be shown that the probability of hitting a specific code in the TDC is proportional to the duration of the time that leads to that particular code. Assuming the duration of D_C for code "c," the probability of hitting this code is equal to Pc = Dc/TR, where TR represents the period of the reference clock. For N cycles of the event sequence applied to the TDC, code "c" is expected N_C times, where N_C is given by

$$N_C = N \times P_C = \frac{N \times D_C}{T_R} \tag{4.5}$$

If the actual number of hits for code "c" is counted in a calibration phase, the estimated duration of the code D_C can be calculated from

$$D_C = \frac{N_C \times T_R}{N} \tag{4.6}$$

Where N_C represents the actual number of hits.

The estimated durations of the codes can be used to construct a TDC characterization curve and calibrate the TDC accordingly. To implement this calibration method, the frequencies of the on-chip oscillator and the reference clock have to be adjusted to prevent coherency between them. Coherency between these signals limits the number of time events and can adversely affect the uniformity of the time events leading to inaccurate calibration. Even without coherency between the oscillator and the reference clock, the periods of these signals have to be carefully adjusted [4.4] to ensure the generation of proper time events for calibration. In general, in addition to an on-chip oscillator, dedicated circuitries are needed to properly control the period of the oscillator to perform TDC calibration in this method.

4.2 Proposed Self-Calibration Method for Subthreshold All-Digital PVT Sensors

Today's microprocessors increasingly need on-chip temperature sensors for thermal and power management. Since these sensors do not take part in the main computing activity but rather play the auxiliary, albeit important, role of temperature monitoring, their presence in terms of area, power, and design effort should be minimal, thus, all-digital sensors are desired. This Section presents a self-calibration method for proposed all-digital PVT sensors. The proposed method eliminates the need for accurate external sources typically used for TDC calibration in section4.1.

4.2.1 Subthreshold All-Digital Temperature Sensor

A fully on chip high-resolution, and low-power CMOS is proposed in section 3.8, and the sensor using frequency-to-digital converter based on PVT variation sensing.

However, the proposed temperature sensors in section 3.8 cannot be integrated with other systems because they occupy large area. The bias current generator in Fig 3.14 accounted for most of the area of the proposed PVT sensors. In order to solve this problem, the new frequency-to-digital based all-digital small-area, and low-power PVT sensors are proposed shown in Fig. 4.3. Using temperature sensitive ring oscillator (TSRO) take the place of bias current generator, the TSRO circuit can reduce more power and area than bias current generator.

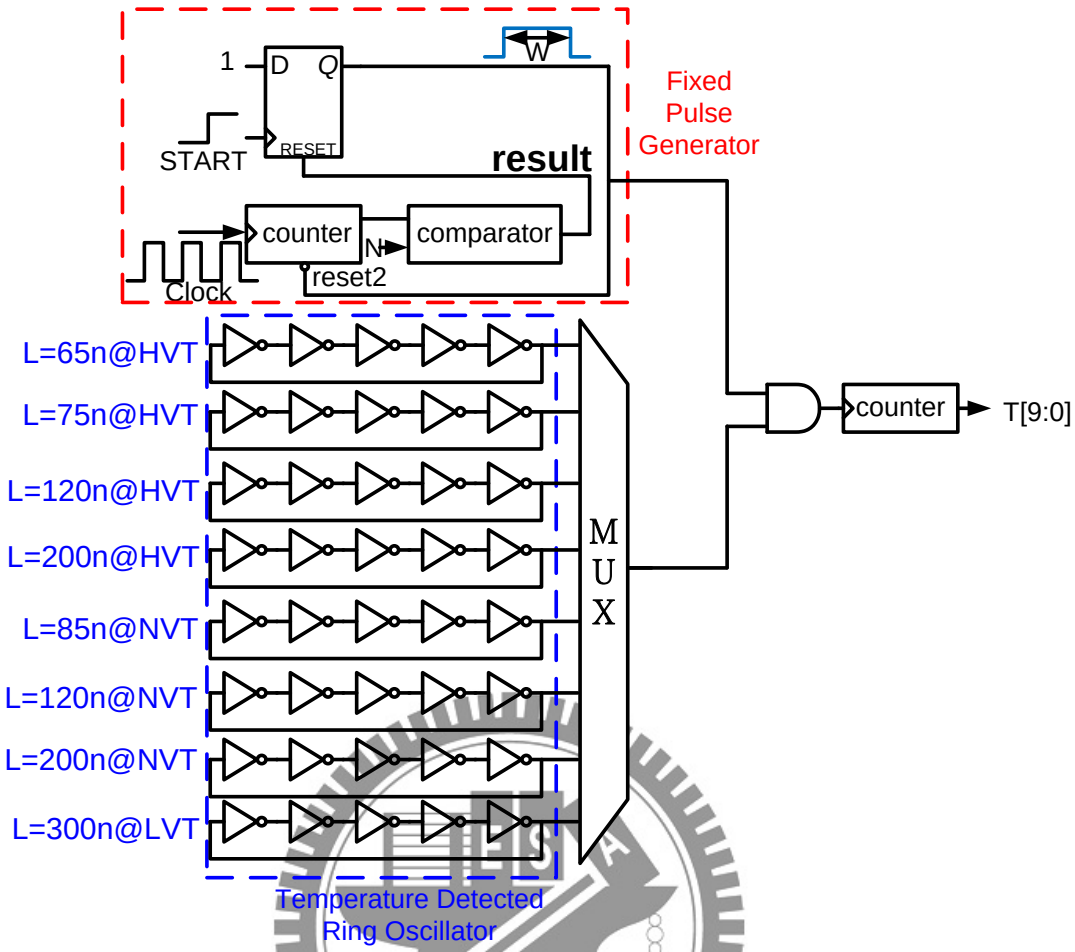


Figure 4.3 Proposed all-digital temperature sensor.

The temperature sensor shows in Fig. 4.3, and all ring oscillators operate in weak inversion region. Alpha-power subthreshold drain current (I_{D_SUB}) [3.7] can be expressed as follows:

$$I_{D\_SUB} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{(V_{GS}-V_{th})/mV_T} \times (1-e^{-V_{DS}/V_T}) \quad (4.7)$$

Assume $V_{DS} >> V_T$, The term of $(1-e^{-V_{DS}/V_T})$ can be ignored. Simplification of the formula can be expressed based on the following:

$$I_{D\_SUB} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{(V_{GS1}-V_{th})/mV_T} \quad (4.8)$$

Where

$$V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0) \tag{4.9}$$

Then

$$I_{D\_SUB} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{[V_{GS1} - V_{th}(T_0) - \alpha(T-T_0)]/mV_T} \tag{4.10}$$

Assume T_0=0℃, then

$$I_{D\_SUB} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times e^{[V_{GS1} - V_{th}(0)]/mV_T} \times e^{-\alpha T/mV_T} \tag{4.11}$$

Where $e^{-\alpha T/mV_T}$ is constant K_C. When $V_{GS} \approx V_{th}(0)$, $\left|[V_{GS} - V_{th}(0)]/mV_T\right| << 1$

Using Taylor series,

$$e^{[V_{GS1} - V_{th}(0)]/mV_T} \approx 1 + \frac{[V_{GS} - V_{th}(0)]/mV_T}{1} = 1 + \frac{K_A}{T} \tag{4.12}$$

$$I_{D\_SUB} = \mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 \times (1 + \frac{K_A}{T}) \times K_C \tag{4.13}$$

Where $V_T \propto T$ and $\mu_0 \propto T^{-1}$, then

$$\mu_0 C_{OX} \frac{W}{L}(m-1)(V_T)^2 = K_B T \tag{4.14}$$

$$I_{D\_SUB} = K_b T \times (1 + \frac{K_A}{T}) \times K_C \tag{4.15}$$

$$I_{D\_SUB} = K_B K_C T + K_A K_B K_C \propto T \tag{4.16}$$

$$f_{OSC} = \frac{I_{D\_SUB}}{V_{DD} \times C_L} \propto T \tag{4.17}$$

When $V_{GS} \approx V_{th}(0)$, then the frequency of the ring oscillator in Fig. 4.4 is proportional to temperature, as described in equation (4.17). Using this characteristic, we can adjust CMOS length to change the V_{th} value in corresponding supply voltage. By adjusting the V_{th}, the frequency of the ring oscillator is proportional to temperature in corresponding supply voltage.

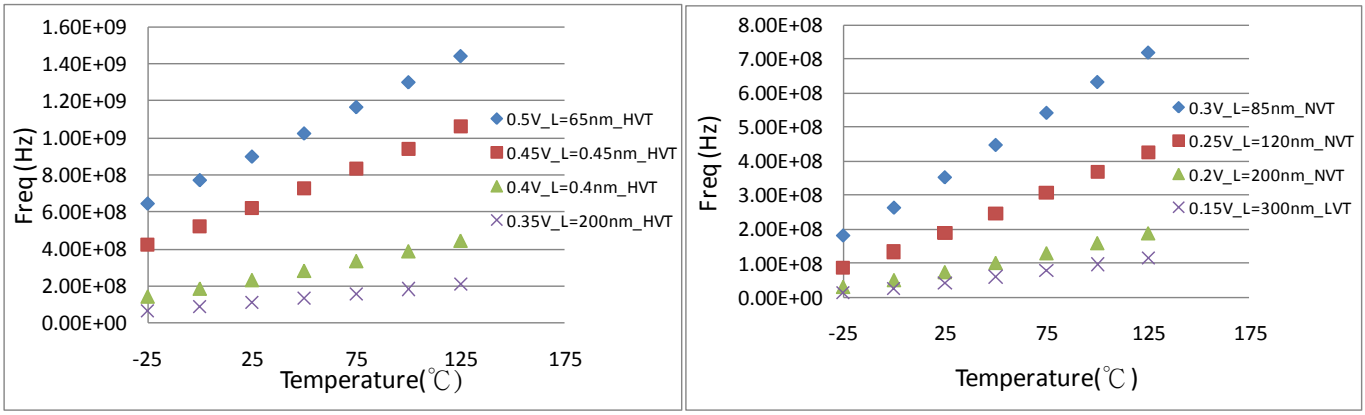


Figure 4.4 Simulation result of proposed temperature sensor in different supply voltage.

4.2.2 Self-Calibration for Subthreshold All-Digital PVT Sensors

Fig. 4.4 and Fig. 4.5show the digital output of temperature sensor with process and voltage variation, and we use process and voltage sensors to compensate temperature. The architecture of proposed all-digital self-calibration PVT sensors shows in Fig. 4.6. Self-calibration method hardware in Fig. 4.6 implementation of the proposed scheme is introduced to compensate for the voltage and process variations on the impact of temperature. The proposed self-calibration circuit is shown in Fig. 4.7, and simulation results shows in Fig. 4.8.

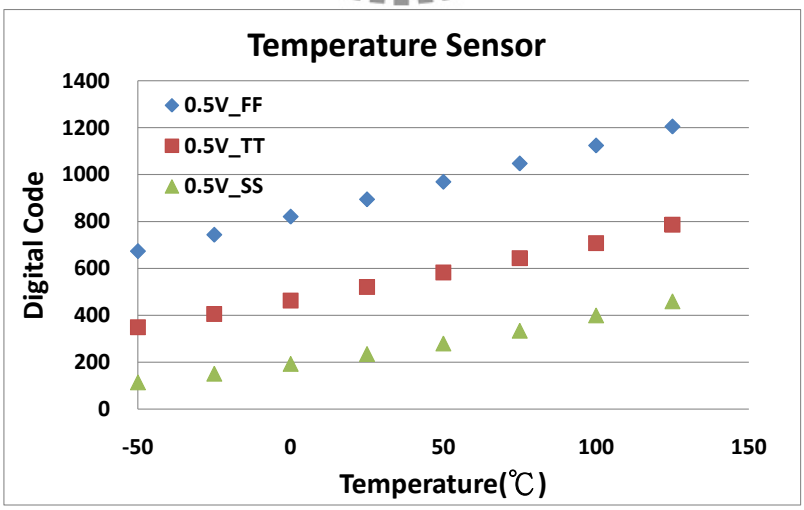


Figure 4.5 Simulation result of temperature sensor in different process corner.

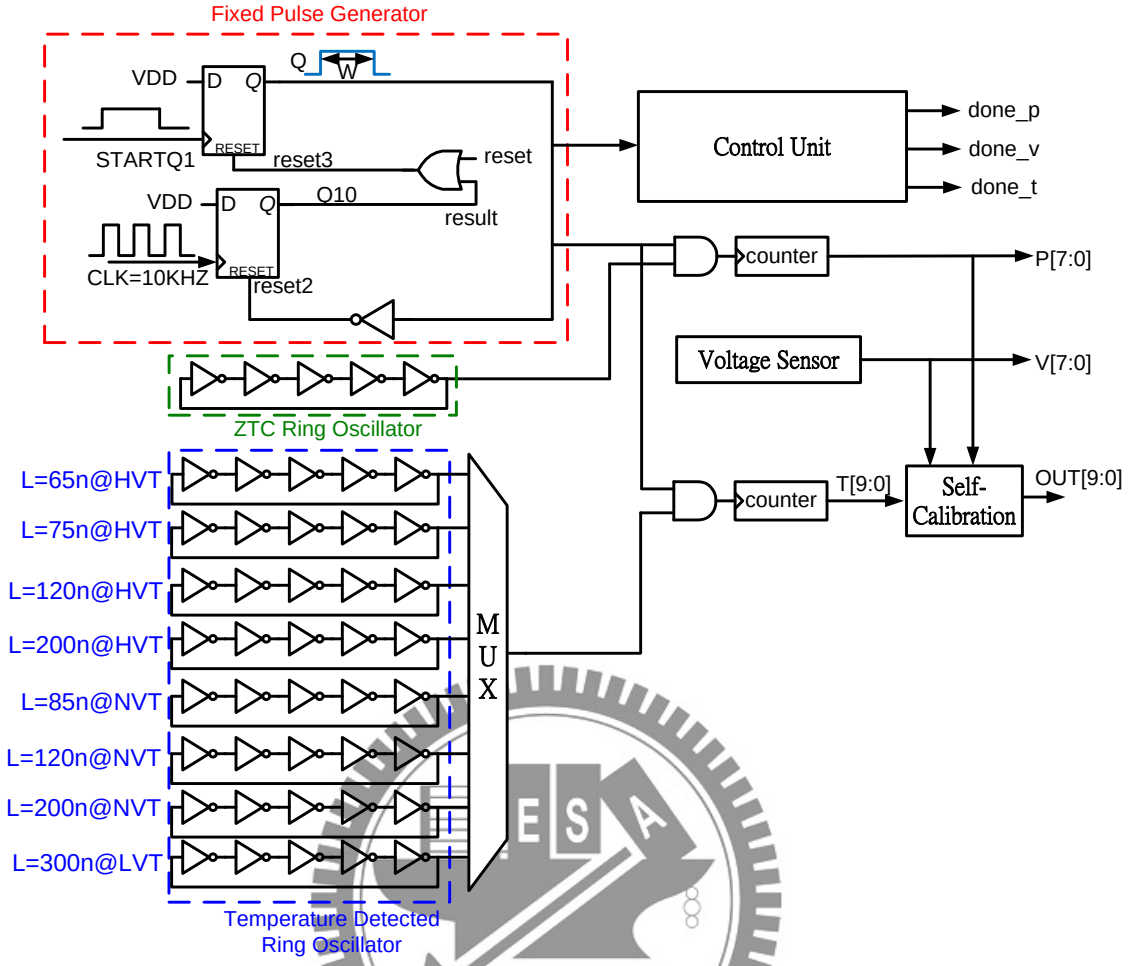


Figure 4.6 Proposed all-digital self-calibration PVT sensors.

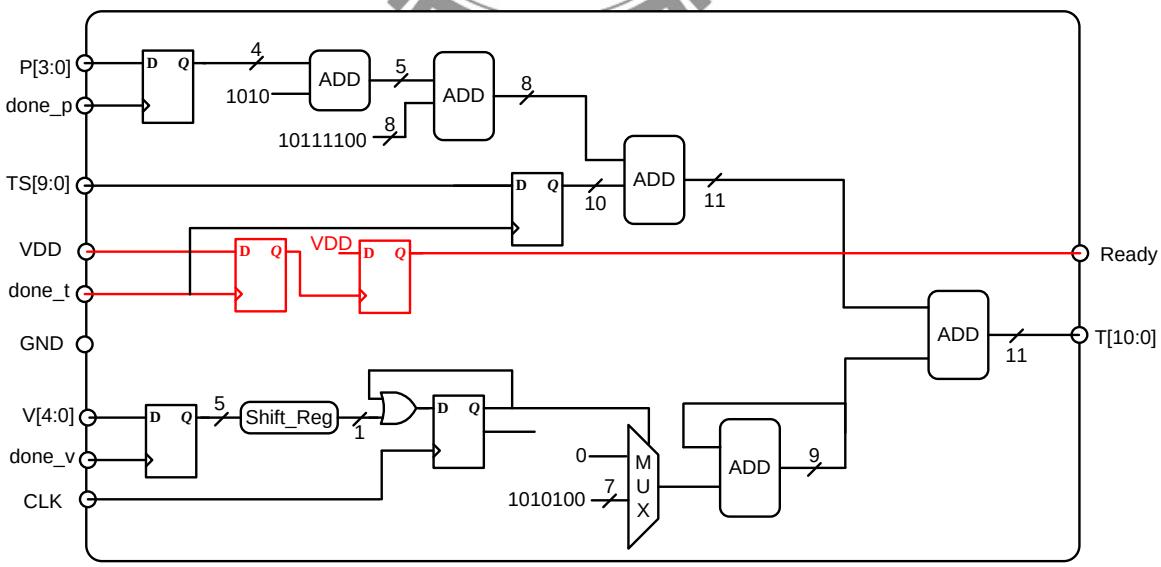


Figure 4.7 Self- Calibration circuit of all-digital PVT Sensors.

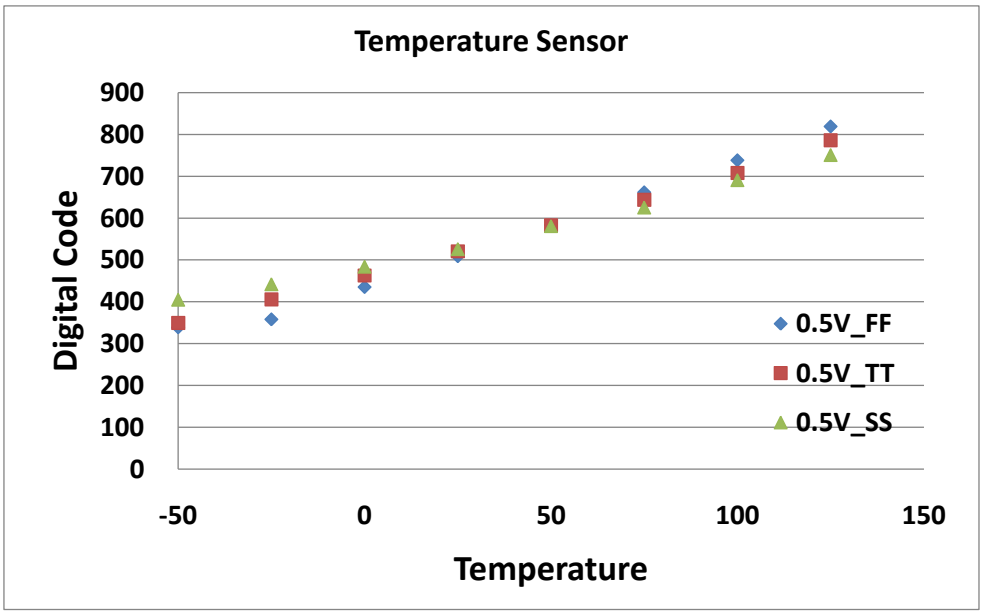


Figure 4.8 Simulation results of calibration of temperature sensor in different process corner.

4.2.3 Post-Layout Simulation Results

A FDC-based subthreshold all-digital PVT sensor is proposed in Fig. 4.9. The PVT sensors without an analog-to-digital converter (ADC) or bandgap reference is proposed for medium accuracy, ultra-low power, small area applications. The proposed temperature sensor generates a clock frequency proportional to the measured temperature, and converts the frequency into a corresponding digital code T[9:0]. A voltage sensor and process sensor are proposed to compensate temperature sensor. The voltage sensor and process sensor used ZTC point to design. The sensor was designed in a 65nm CMOS technology. Layout view of the PVT sensor is shown in Fig. 4.9. The chip area of the 10-bit sensor is merely 840um^2 .The power consumption is under 0.7326μW at 0.3V and a sample rate of 10k samples/sec. The temperature error is merely -3.0~3.0℃.

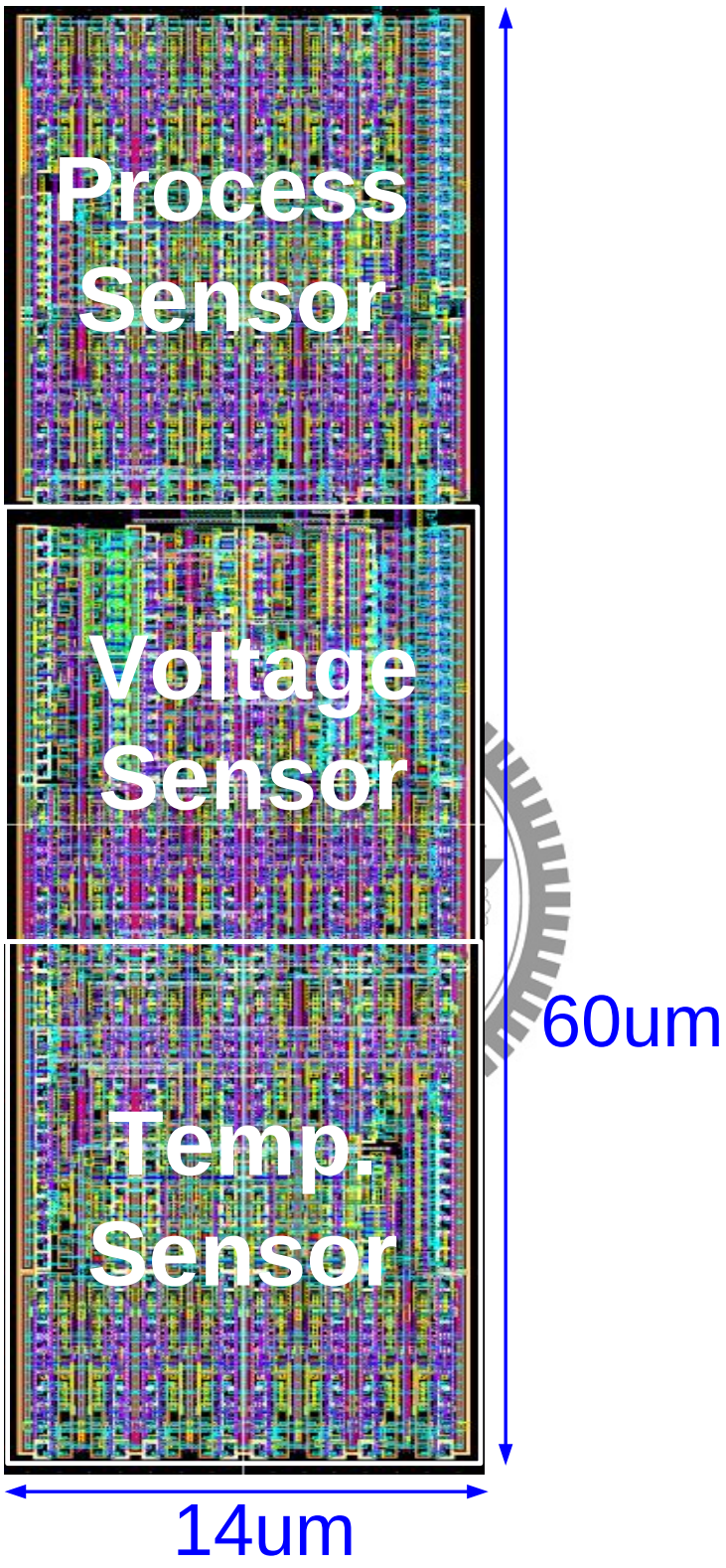


Figure 4.9 Layout views of the all-digital PVT Sensors

4.3 Ultra-Low Voltage All-Digital Temperature Sensor with Adaptive Pulse Width Compensation

4.3.1 Architecture of All-Digital Temperature sensor with Adaptive Pulse Width Compensation

We report on an all-digital CMOS temperature sensor for microprocessor application, which also exploits temperature-dependent frequency of ring oscillator with the FDC-based framework of Fig. 4.10. It, however, has two improvements over prior art of [4.5]. First, we use FDC-based architecture to reducing power and area, and improving the linearity of digital output (instead of TDC-based temperature sensor of [4.5]). The use of FDC-based temperature sensor operation and yields a high measurement bandwidth (10k/s) at 10bit resolution, which could enable fast temperature tracking. Second, it removes the effect of process and voltage variation on frequency of ring oscillator via self-calibration (instead of 1-point and 2-point calibration of [4.5]), thus, reducing high volume production cost. We use an adaptive pulse width generator to generate a pulse width change with process and voltage variation.

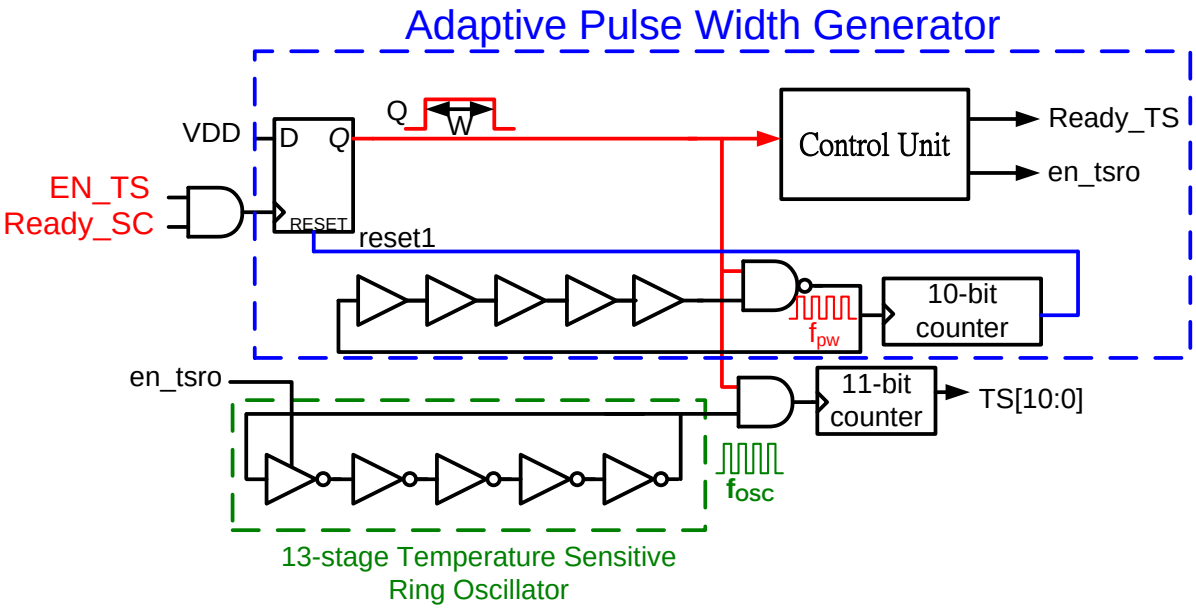


Figure 4.10 Architecture of FDC-based CMOS all-digital temperature sensor.

The self-calibration is enabled by our observation that the frequency of ring oscillator can be separated into a temperature-only-dependent part and a process-only-dependent part. The frequency, f_{OSC}, of a CMOS ring oscillator with equal PMOS and NMOS strengths in subthreshold region can be expressed as

$$f_{OSC} = \frac{\mu_0 C_{OX} \frac{W}{L} (m-1)(V_T)^2 \times e^{(V_{GS}-V_{th1})/mV_T}}{V_{DD} \times C_L} \tag{4.18}$$

Temperature-dependent parameters are the mobility, μ_0, thermal voltage, V_T, and threshold voltage, V_{th}, so to the first order, $f_{OSC} \propto T^{\alpha}$ (α:constant) accounts for temperature dependence of f_{OSC}. To highlight this, eq. (4.18) can be rewritten as

$$f_{OSC}(T,P) = T^{\alpha} G(P) \tag{4.19}$$

Where G(P) is the function of process variations. G(P) varies only with process variation. T^{α} varies only with temperature (α varies slowly with doping level, so it can be regarded as a constant in a given technology).

The sensor uses adaptive pulse width generator to eliminate the process variation.

The pulse width can be expressed as

$$W = \frac{N}{f_{PW}} \tag{4.20}$$

Where, N is generated by the counter.

The frequency, f_{PW}, of a CMOS ring oscillator shows in Fig. 4.10 in linear region can be expressed as

$$f_{PW} = \frac{\mu_0 C_{OX} \frac{W}{L} V_{DS} \times (V_{GS} - V_{th2} - \frac{1}{2} V_{DS})}{V_{DD} \times C_L} \tag{4.21}$$

According eq.(4.18)(4.20)(4.21), the digital output T[10:0] can be express as

$$T[10:0] = W \times f_{OSC} = \frac{N}{f_{PW}} \times f_{OSC}$$

$$= N \times \frac{V_{DD} \times C_L}{\mu_0 C_{OX} \frac{W}{L} V_{DS} \times (V_{GS} - V_{th2} - \frac{1}{2} V_{DS})} \times \frac{\mu_0 C_{OX} \frac{W}{L} (m-1)(V_T)^2 \times e^{(V_{GS} - V_{th1})/mV_T}}{V_{DD} \times C_L}$$

$$= N \times \frac{(m-1)(V_T)^2 \times e^{(V_{GS} - V_{th1})/mV_T}}{V_{DS} \times (V_{GS} - V_{th2} - \frac{1}{2} V_{DS})}$$

Where

$$V_{DS} = V_{GS} = V_{DD} \tag{4.22}$$

Then

$$T[10:0] = N \times \frac{(m-1)(V_T)^2 \times e^{(V_{DD}-V_{th1})/mV_T}}{V_{DD} \times (\frac{1}{2}V_{DD} - V_{th2})}$$

$$= N \times (m-1)(\frac{K}{q})^2 \times T^2 \frac{e^{(V_{DD}-V_{th1})/mV_T}}{V_{DD} \times (\frac{1}{2}V_{DD} - V_{th2})} \quad (4.23)$$

Where $N \times (m-1)(\frac{K}{q})^2$ is constant K_m, and $V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0)$

Then

$$T[10:0] = K_m \times T^2 \frac{e^{(V_{DD}-V_{th1}(0)+\alpha T)/mV_T}}{V_{DD} \times (\frac{1}{2}V_{DD} - V_{th2}(0) - \alpha T)} \quad (4.24)$$

Where $e^{(\alpha T / mV_T)}$ is constant K_a

When $V_{DD} \approx V_{th_1}(0)$ and $V_{DD} \approx 2V_{th_2}(0)$, then eq. (4.23) can be rewritten as

$$T[10:0] = K_m \times T^2 \times K_a \frac{1}{V_{DD} \times (-\alpha T)} = \frac{K_m \times T^2 \times K_a}{V_{DD} \times (-\alpha T)} = K \times T \quad (4.25)$$

Where $K = \frac{K_m \times K_a}{V_{DD} \times (-\alpha)}$

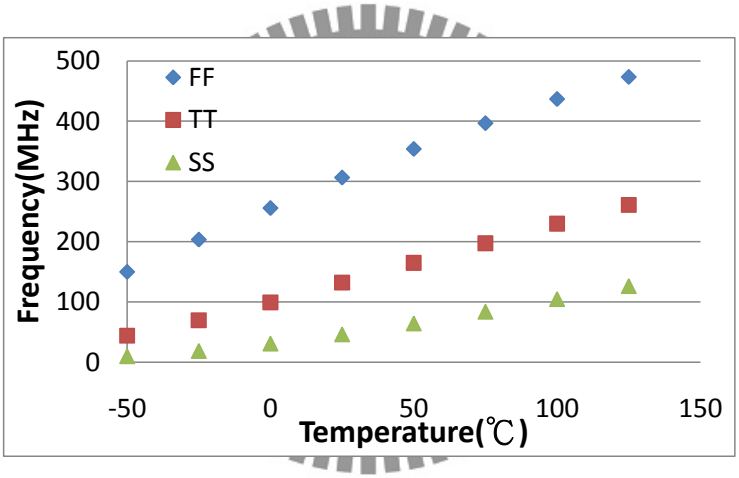
Process dependency G(P) disappeared due to the separation of variables. Digital output T[10:0] is a function of T only, so it is reproducible across all process corners, serving as a good temperature representation. This is the foundation of our sensor operation with self-calibration.

4.3.2 Post-Layout Simulation Results

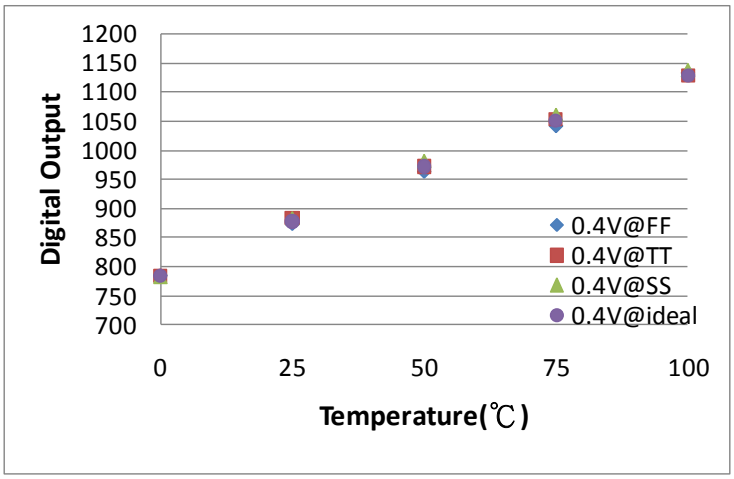
Simulations validate this approach. Using TSMC standard 65nm CMOS technology,

the simulation results shows in Fig. 4.11. Fig. 4.11(b) shows digital output T[10:0] remains almost the same across corners after self-calibration method. The measurement error over 0℃~ 100℃ is within -2℃~2.5℃ shows in Fig. 4.12(c), which demonstrates good process immunity for the proposed sensor. The effective resolutions for all test chips spread over 0.25℃.

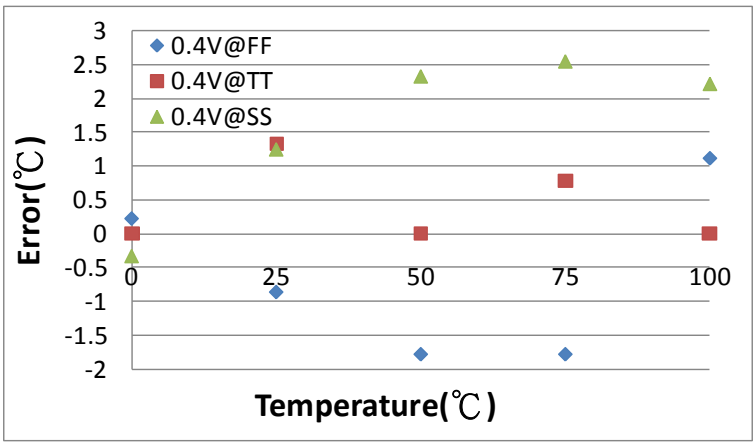
Layout view of proposed all-digital temperature sensor is shown in Fig. 4.12. The chip area of the 10-bit sensor is merely 832um^2 .The power consumption is under 0.23μW at 0.3V and a sample rate of 10k samples/sec. The temperature error is merely -3.0~3.0℃.



(a)



(b)



(c)

Figure 4.11 (a) Simulated frequency of ring oscillator in different process corner.

(b) Digital output of sensor after self-calibration method.

(c) Simulated output error for 0℃~100℃.

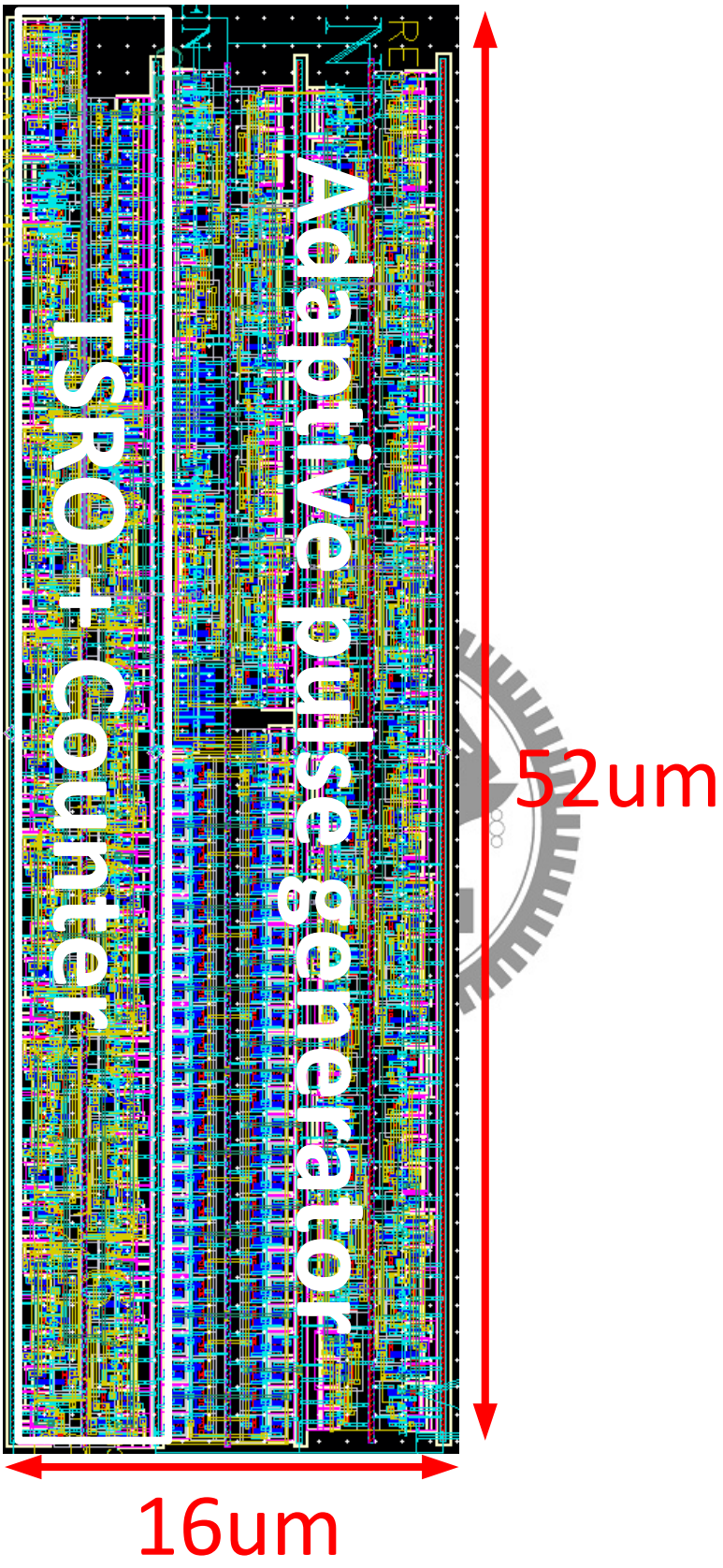


Figure 4.12 Layout views of the all-digital temperature sensor with adaptive pulse width compensation.

A comparison chart between this work and previously presented temperature sensors is shown in Table 4.1. In Table 4.1, the main characteristics, such as operation supply voltage, power, error, temperature range, sensor type, process technology, and conversion rate are compared.

Table 4.1 Temperature sensor comparisons

Sensor	Supply(V)	Power(μW)	Error(℃)	Sensor Type	CMOS Technology	Conversion rate (samples/s)
[2.7]	3.0	4.5	-0.6~+0.6	Temp-to-Pulse	0.35um	10
[2.9]	3.0	10	-0.7~+0.9	Temp-to-Pulse	0.35um	10k
[2.10]	1.0	25	-1.0~+0.8	Analog	90nm	4
Fully on chip PVT sensors	0.3~1	3.7@0.3V	-0.8~+0.8	FDC-Based	UMC 65nm	10k
All-digital PVT sensors	0.2~0.5	0.7326@0.3V	-3.0~+3.0	FDC-Based	UMC 65nm	10k
Temperature sensor with APWG	0.4	0.23@0.4V	-1.5~+1.5	FDC-Based	TSMC 65nm	50k

4.4 Summary

This chapter provides two kinds of self-calibration temperature sensors. One is uses voltage and process sensors to enhance temperature sensor environmental variation immunity. Another method is uses adaptive pulse width generator to enhance temperature sensor environmental variation immunity.

The temperature sensor with process and voltage compensation has only 0.723μW power consumption at 0.3V supply voltage and a high sample rate of 10k samples/sec. The temperature error is -3.0~3.0℃. The temperature sensor with adaptive pulse width generator has only 0.23μW power consumption at 0.4V supply voltage and a high sample rate of 50k samples/sec. The temperature error is -3.0~3.0℃.

Chapter 5 PVT Sensors for Micro-Watt DVFS System Design

In micro-watt systems, dynamic voltage and frequency scaling (DVFS) serve as an effective method to reduce power through voltage and frequency scaling in response to varying workload requirements. This system requires multiple on-chip voltage domains and adaptive frequency generator. A switched capacitor (SC) dc–dc converter is a good choice for multiple voltage domains. In addition, SC DC-DC converter can minimize the number of off-chip components and does not require any inductors. On the other hand, a low-voltage PLL is a good choice for adaptive frequency generator.

PVT variation has enormous influence for SC DC-DC convert and low-voltage PLL in ultra-low voltage which causes output voltage and frequency could not achieve the target value. So we use the proposed PVT sensors in Chapter 3 and 4 to improve the influence of circuit in PVT variation. For above reasons, we present PVT sensors for micro-watt DVFS system.

In section 5.1, we describe the architecture of proposed PVT sensors for micro-watt DVFS system. The previous work of conventional sc DC-DC converter is shown in section 5.2. The proposed multi-threshold voltage sc DC-DC converter is shown in section 5.3. The results are simulated in TSMC and UMC 65nm standard CMOS technology and are shown in section 5.4. In section 5.5, we describe the architecture of proposed temperature compensation technique for low-voltage digital assisted PLL. And the results are simulated in TSMC 65nm standard CMOS technology and are shown in section 5.5. Finally, we will conclude the proposed PVT sensors for micro-watt DVFS system in section 5.6.

5.1 PVT Sensors for Micro-Watt DVFS System Design

Fig. 5.1 shows the PVT sensors for micro-watt DVFS system which consists of the PVT sensors, PVT-aware MTCMOS SC DC-DC converter, and temperature compensation technique for low-voltage digital assist PLL. The SC DC-DC converter uses PVT sensors to adjust output supply voltage in different environmental variation. Low-voltage PLL uses temperature sensor to compensate the output frequency.

The micro-watt DVFS system contains logic to estimate the workload (indicated by *workload*) by the FIFO utilization and stall duration of the DVFS Module. The workload information is filtered and processed with configurable FIR and IIR filters. Frequency and voltage scaling are performed by incrementing or decrementing the clock frequency and voltage based on the workload information.

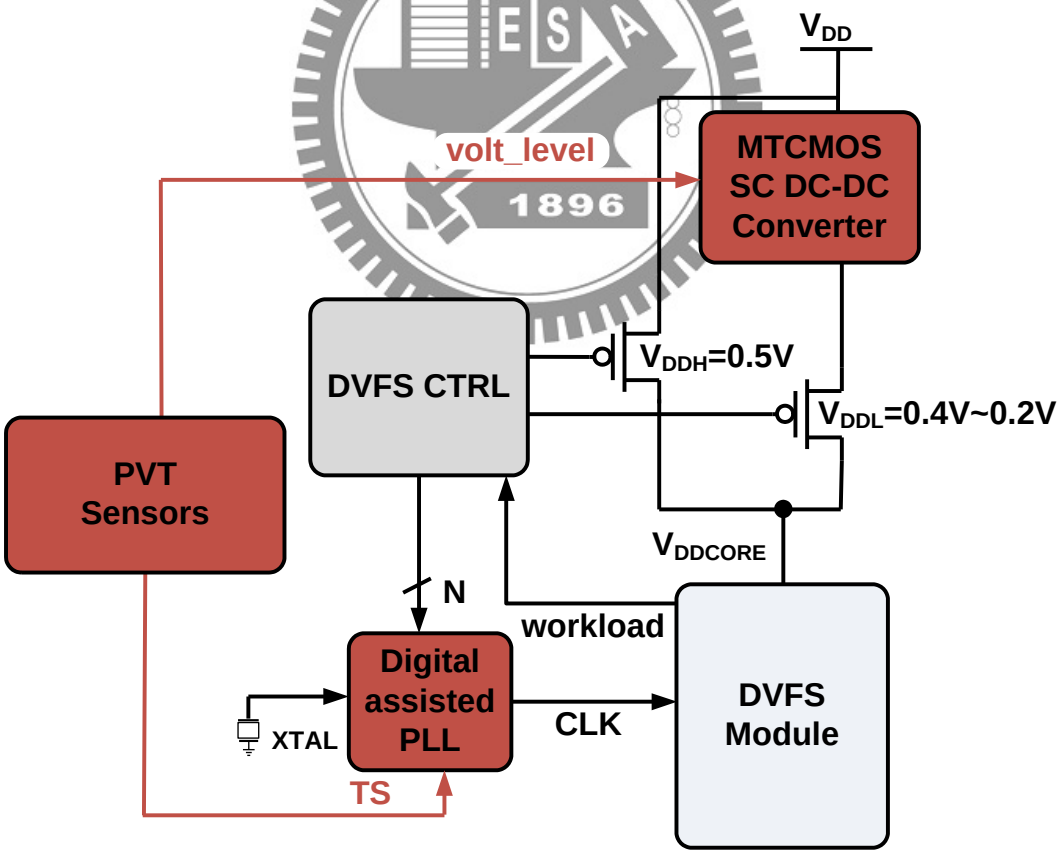


Figure 5.1 PVT sensors for micro-watt DVFS system.

5.2 Switched Capacitor DC-DC Converter

DVFS systems often require multiple on-chip voltage domains. A switched capacitor (SC) DC-DC converter is a good choice for such battery operated systems because it can minimize the number of off-chip components and does not require any inductors. Compared to commonly use linear regulators for on-die voltage conversion, SC converters can provide 15%–30% higher efficiencies when the output voltage delivered is less than half the input voltage.

5.2.1 Conventional SC DC-DC Converter

Fig. 5.2 shows the architecture of the SC DC-DC converter [5.2]. At the core of the system is the switch matrix which contains the charge-transfer capacitors, and the topology, charge-transfer switches. A suitable topology is chosen depending on the reference voltage V_{ref}, which is set digitally. The digital reference is converted to an analog value using an on-chip charge redistribution digital-to-analog converter. A pulse frequency modulation (PFM) mode control is used to regulate the output voltage to the desired value. A dynamic comparator clocked by the signal *clk* is used for this purpose. When the output voltage V_O is above V_{ref}, the switches are all set to the Φ_1 mode. When V_O falls below V_{ref}, the comparator triggers a Φ_2 pulse, which charges up the output load capacitor C_{load}. The nonoverlapping clock generator block prevents any overlap between the Φ_1 and Φ_2 ON phases. Typical waveforms of these phases are shown in the inset in Fig. 5.2. Bottom-plate parasitics of the on-chip capacitors significantly affect the efficiency of the converter. A divide-by-3 switching scheme was employed to mitigate the effect due to bottom-plate parasitic and improve efficiency. The switching losses are scaled with change in load power by the help of an automatic frequency scaling block. This block changes the switching frequency as the load power delivered changes, thereby reducing the switching losses at low load.

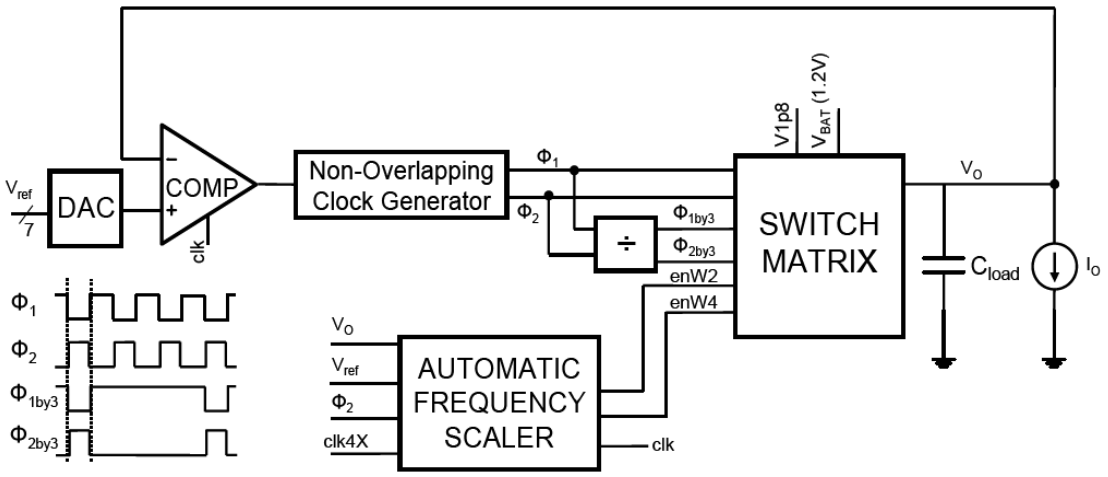


Figure 5.2 Architecture of the switched capacitor DC-DC converter system.

5.2.2 Switch Matrix

The operation of switched capacitor matrix is able to provide five different common phases and gain phases, with the gain being the ratio of the output voltage V_{out} to the input voltage V_{in}. The equivalent circuits of these conversion phases are shown in Fig. 5.3 [5.3].

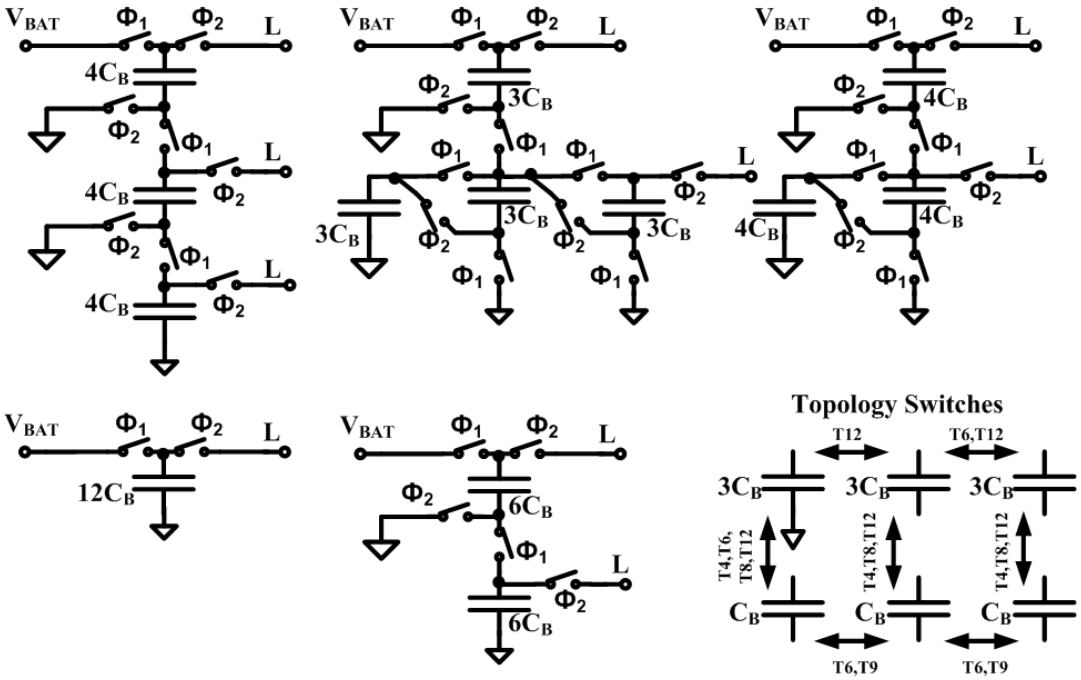


Figure 5.3 Topologies used to generate a wide range of load voltages from a 1.2V supply.

In these configurations, there are four gain configurations referred as buck stages

whose gains are less than 1 and one gain configuration referred as unit gain with gain equal to 1. According to the input and the output, the DC-DC converter is divided to step-down type or buck type converter ($V_{out}<V_{in}$).

While the converter is clocked and the gain setting is chosen, the switched capacitor matrix is switched between the common phase and the chosen gain phase to transfer charges from the input to the output to keep the chosen output voltage. The gain configuration of 1/2 is used as an example to explain the implementation of gains through the switched capacitor matrix. The equivalent circuit of gain configuration of 1/2 is shown in Fig. 5.4[5.4] below. The flying capacitor C_f is used to store and transfer energy, and capacitor C_h is the hold capacitor for the output.

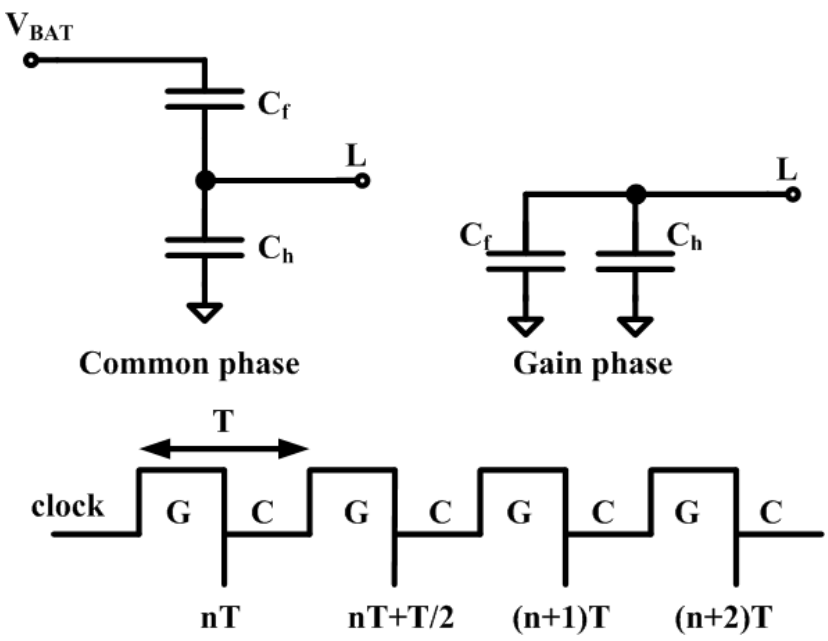


Figure 5.4 Equivalent circuit of the gain configuration with gain of 1/2.

At time nT, the switched capacitor stays at the end of the gain phase, and the charges in the capacitors C_h and C_f are

$$Q_{ch}(nT) = C_h \times V_{out}(nT) \tag{5.1}$$

$$Q_{cf}(nT) = C_f \times V_{out}(nT) \tag{5.2}$$

At time nT+(T/2), the charge pump stays at the end of the common phase, the charges in the capacitors Ch and Cf are

$$Q_{ch}(nT + \frac{T}{2}) = C_h \times V_{out}(nT + \frac{T}{2}) \tag{5.3}$$

$$Q_{cf}(nT + \frac{T}{2}) = C_f \times [V_{in} - V_{out}(nT + \frac{T}{2})] \tag{5.4}$$

According to the theory of charge conversation, we have

$$Q_{ch}(nT + T/2) - Q_{cf}(nT + T/2) = Q_{ch}(nT) - Q_{cf}(nT) \tag{5.5}$$

Solving Equation (5.1)-(5.5) results in

$$V_{out}(nT + T/2) = \frac{C_f}{C_h + C_f} V_{in} + \frac{C_h - C_f}{C_h + C_f} V_{out}(nT) \tag{5.6}$$

$$Q_{ch}(nT + \frac{T}{2}) = C_h \times \frac{C_f}{C_h + C_f} V_{in} + C_h \times \frac{C_h - C_f}{C_h + C_f} V_{out}(nT) \tag{5.7}$$

$$Q_{cf}(nT + \frac{T}{2}) = C_h \times \frac{C_f}{C_h + C_f} V_{in} - C_f \times \frac{C_h - C_f}{C_h + C_f} V_{out}(nT) \tag{5.8}$$

At time nT+T, the charge pump is switched back to the gain phase. According to the theory of charge conservation, the total charges in the capacitors C_h and C_f are

$$Q_{total}(nT + T) = Q_{ch}(nT + T/2) + Q_{ch}(nT + T/2) \tag{5.9}$$

So the output voltage at time nT+T is

$$V_{out}(n+1)T = \frac{Q_{total}}{C_h + C_f} = aV_{in} + bV_{out}(nT)$$

$$= \frac{2C_hC_f}{(C_h + C_f)^2}V_{in} + \frac{(C_h - C_f)^2}{(C_h + C_f)^2}V_{out}(nT) \quad (5.10)$$

According to Equation (5.10), we can have

$$V_{out}(nT + 2T) = aV_{in} + bV_{out}(nT + T)$$

$$= aV_{in} + b[aV_{in} + bV_{out}(nT)] = a(1+b)V_{in} + b^2V_{out}(nT) \quad (5.11)$$

$$V_{out}(nT + 3T) = aV_{in} + bV_{out}(nT + 2T)$$

$$= aV_{in} + b[a(1+b)V_{in} + b^2V_{out}(nT)] \quad (5.12)$$

$$= a(1+b+b^2)V_{in} + b^3V_{out}(nT)$$

According to Equation (5.11) and (5.12), we can have

$$V_{out}(nT + kT) = a(1+b+b^2+...+b^{k-1})V_{in} + b^kV_{out}(nT)$$

$$= a\frac{1-b^k}{1-b}V_{in} + b^kV_{out}(nT) \quad (5.13)$$

Where k=0,1,2…. ,because of b<1,we can have

$$\lim_{k\to\infty} V_{out}(nT + kT) = \frac{aV_{in}}{1-b}$$

$$= V_{in}\frac{2C_hC_f}{(C_h + C_f)^2}\frac{1}{1 - \frac{(C_h - C_f)^2}{(C_h + C_f)^2}} = \frac{V_{in}}{2} \quad (5.14)$$

5.2.3 Conventional Bandgap Voltage Reference

The traditional bandgap voltage reference, as shown in Fig. 5.5, is the combination of a voltage that is proportional to absolute temperature (PTAT) and a voltage that is complementary to absolute temperature (CTAT). The CTAT is traditionally generated from a diode (or diode-connected BJT). The current through the pn-junction of a diode has a dependence on temperature which is well-characterized and predictable.

The PTAT current is generated, as seen in Fig. 5.5, by BJTs Q_1 and Q_2, resistor R_1, the op amplifier and the current sourcing FETs M_1 and M_2. The op amplifier feedback loop sets the currents through M_1 and M_2 to the same value. As Q_1 and Q_2 have emitter areas that differ by a factor of n, their temperature response will differ. The BJTs will sink the same amount of current, but a PTAT current will flow through R1. This current is added to the CTAT generator, Q_3, through M_3. The size of M_3 and the ratio of R_2 to R_1 are chosen so that the PTAT current is translated into a PTAT voltage that is equal to the CTAT voltage of Q_3. This produces an almost temperature independent reference voltage (neglecting 2nd-order-and-above effects). The temperature dependence of the current through the pn-junction of the diode is naturally CTAT. The PTAT characteristic used to null the CTAT behavior is created by scaling the inherent thermal voltage of a BJT (VT). The reference voltage of a traditional BVR can be described in equation (5.15).

$$V_{REF} = V_{BE1} + \frac{R_2}{R_1} V_T \ln n \tag{5.15}$$

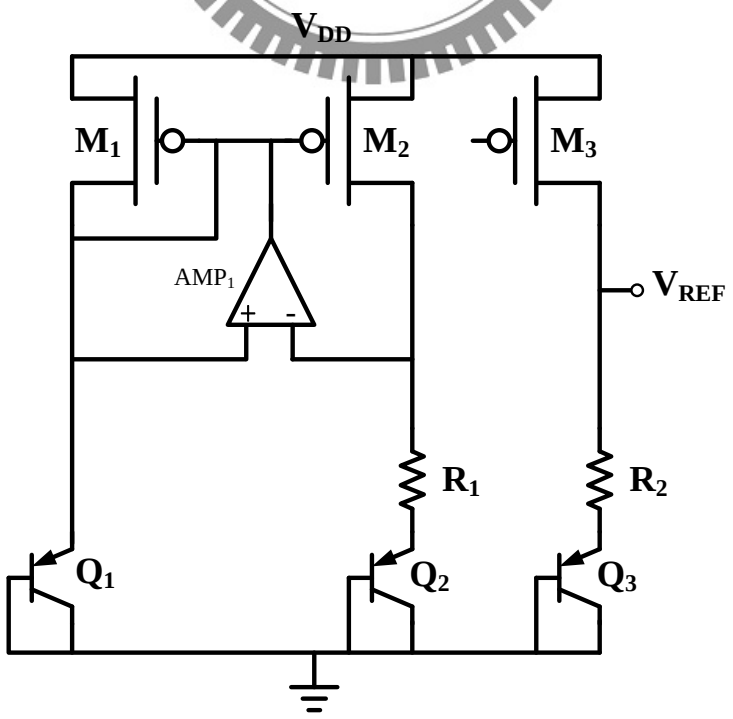


Figure 5.5 Conventional CMOS bandgap voltage reference.

5.1.4 Automatic Frequency Scaling

To minimize gate-switching losses, the circuit automatically adjusts the switching frequency depending on the load power demand. The automatic frequency scaling (AFS) block that performs the frequency selection is shown in Fig. 5.6 [5.2]. An additional comparator called the overload comparator is used in the AFS block. The reference voltage of the overload comparator is set to V_{ref}-V_{off}, where V_{off} is an offset voltage (~20mV) which again is set digitally. When the DC-DC converter, operating in steady state, cannot supply the desired load power at a given switching frequency, V_O begins to fall below V_{ref}. As V_O falls below V_{ref}–V_{off}, the overload comparator triggers the *go_up* signal. This signal is used to double the switching frequency which in turn doubles the width of the charge-transfer switches. At low load powers, the switching frequency is brought down using a counter mechanism. If the number of Φ_2 pulses for every 4 *clk* cycles is found to be less than 3, the *go_down* signal is triggered which halves the switching frequency and the width of the charge-transfer switches. The signals *enW2* and *enW4* determine the switching frequency. When only *enW2* is high, 2X the minimum clock frequency is used and when *enW4* is high, 4X the minimum clock frequency is used. The signals *enW2* and *enW4* are fed into the switch matrix to suitably size the charge-transfer switches. While the PFM mode control effectively reduces the frequency of Φ_2 pulses as load power decreases, the AFS block helps in bringing down the overall system switching frequency together with the width of the charge-transfer switches, thereby reducing the switching losses in the gate-drive and the control circuitry. The entire control circuitry is digital and consumes no static power, which is a critical feature to achieve good efficiency at ultra-low load power levels. It is extremely scalable in terms of complexity to suit the load power and voltage demands of the target application.

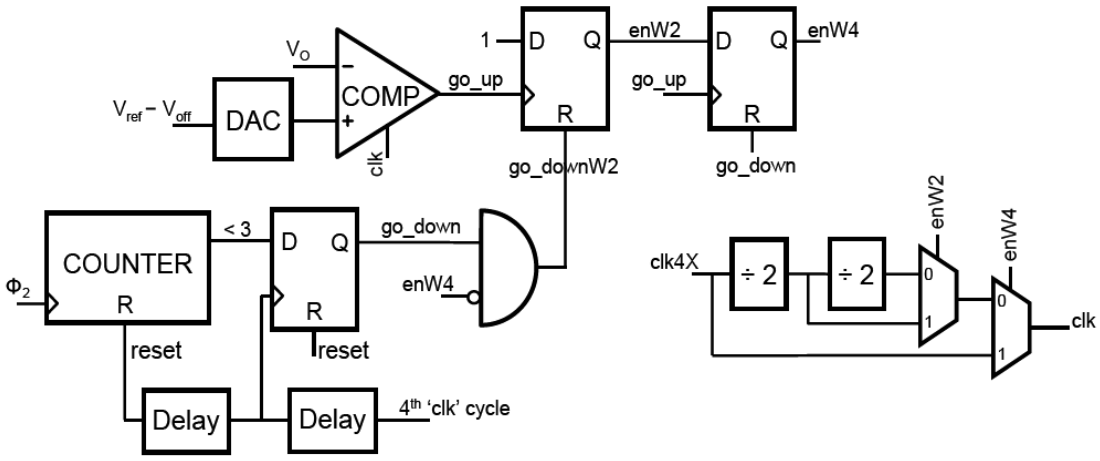


Figure 5.6 Automatic frequency scaling circuit.

5.2.4 Efficiency Analysis

Efficiency of a power converter is a key metric for battery operated electronics and energy starved systems. The principal efficiency loss in the SC DC-DC converter is shows in Fig. 5.7 [5.6].

i) Conduction Loss in transferring charge from battery to load

This is a fundamental loss mechanism which arises from charging a capacitor through a switch. To minimize conduction loss, different topologies (Fig. 5.7) are switched in to reduce the difference between the no-load voltage (VNL) of a topology and V_O. Assuming that a load voltage less than 600mV is being supplied by the T8 topology, conduction loss imposes a limit on the maximum efficiency that can be achieved to $\eta_{lim} = V_O/0.8$. By switching to the T6 topology, this efficiency limit can be improved to $\eta_{lim} = V_O/0.6$.

ii) Loss due to bottom-plate parasitic capacitors

The second main contributor to efficiency loss after the linear conduction loss is that due to parasitic bottom-plate capacitors. The loss due to bottom-plate parasitic

occurs because of the energy stored in the parasitic capacitors being dumped to ground every cycle. This loss is more pronounced if on-chip capacitors are used. Common capacitors in CMOS processes may have up to 20% parasitic at the bottom-plate. On top of these losses are the switching and control losses. The efficiency achievable in a switched capacitor system is in general smaller than which can be achieved in an inductor based switching regulator with off-chip passives. Further, multiple gain settings and associated control circuitry is required in a SC DC–DC converter to maintain efficiency over a wide voltage range.

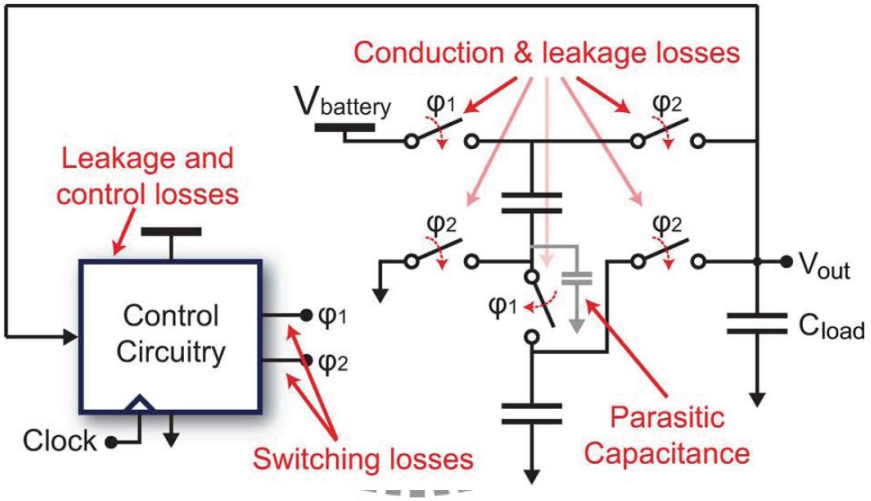


Figure 5.7 Energy loss mechanisms in a switched capacitor DC–DC converter.

iii) Gate-drive Loss

The energy expended in switching the gate capacitances of the charge-transfer switches every cycle can be approximately given by

$$E_{SW} = nC_{ox}WLV_{BAT}^{2}$$

where n is the number of switches used, C_{ox} is the gate-oxide capacitance per unit area, W and L are the width and length of the charge-transfer switches. The width of each switch is however proportional to the charge-transfer capacitance and the

frequency of switching. This is because the resistance of the switches needs to be low enough to allow settling of the charge-transfer capacitors within the time period of switching.

To minimize the gate-switching loss, depending on the location of the charge-transfer switch and the topology in use, either only a PMOS or an NMOS switch is used instead of a transmission gate comprising both PMOS and NMOS devices.

iv) Power loss in the control circuitry

The power lost in the control circuitry is of specific concern while delivering ultralow load power levels. The control circuitry does not consume any static power (no analog bias currents) other than the subthreshold leakage currents in the digital circuitry.

The overall efficiency can be expressed in a more compact form where the pre-factor is due to the linear efficiency. The 2nd term in the denominator is due to the bottom-plate parasitic loss. The next term is due to gate-drive switching loss, and the 4th and 5^{th} terms are due to switching and leakage loss in the control circuitry.

The efficiency of the SC converter with change in load voltage while delivering 100 μW to the load from a 1.2 V supply is shown in Fig. 5.8 The converter was able to achieve 70% efficiency over a wide range of load voltages. An increase in efficiency of close of 5% can be achieved by using divide-by-3 switching.

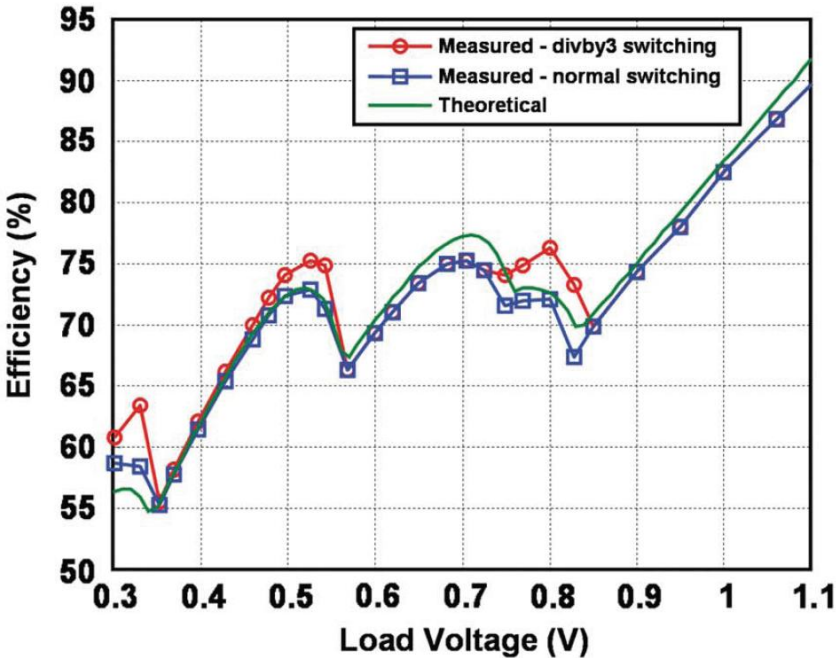


Figure 5.8 Efficiency plot with change in load voltage.

5.3 Multi-threshold CMOS SC DC-DC Converter

5.3.1 Architecture of Multi-threshold CMOS SC DC-DC Converter

To realize the full energy savings of subthreshold operation, a DC-DC converter supplying ultra-low voltages at high efficiencies is essential. Since the power consumption of the micro-watt load circuits drops exponentially at subthreshold voltages, the DC-DC converter was designed to deliver a maximum of 100μA of load current. This reduced load power demand makes switched capacitor DC-DC conversion an ideal choice for this application. The switched capacitor (SC) DC-DC converter is based on [5.2], and makes use of 15 pF of total on-chip charge transfer (flying) capacitance to provide fix load voltages 200~300mV.

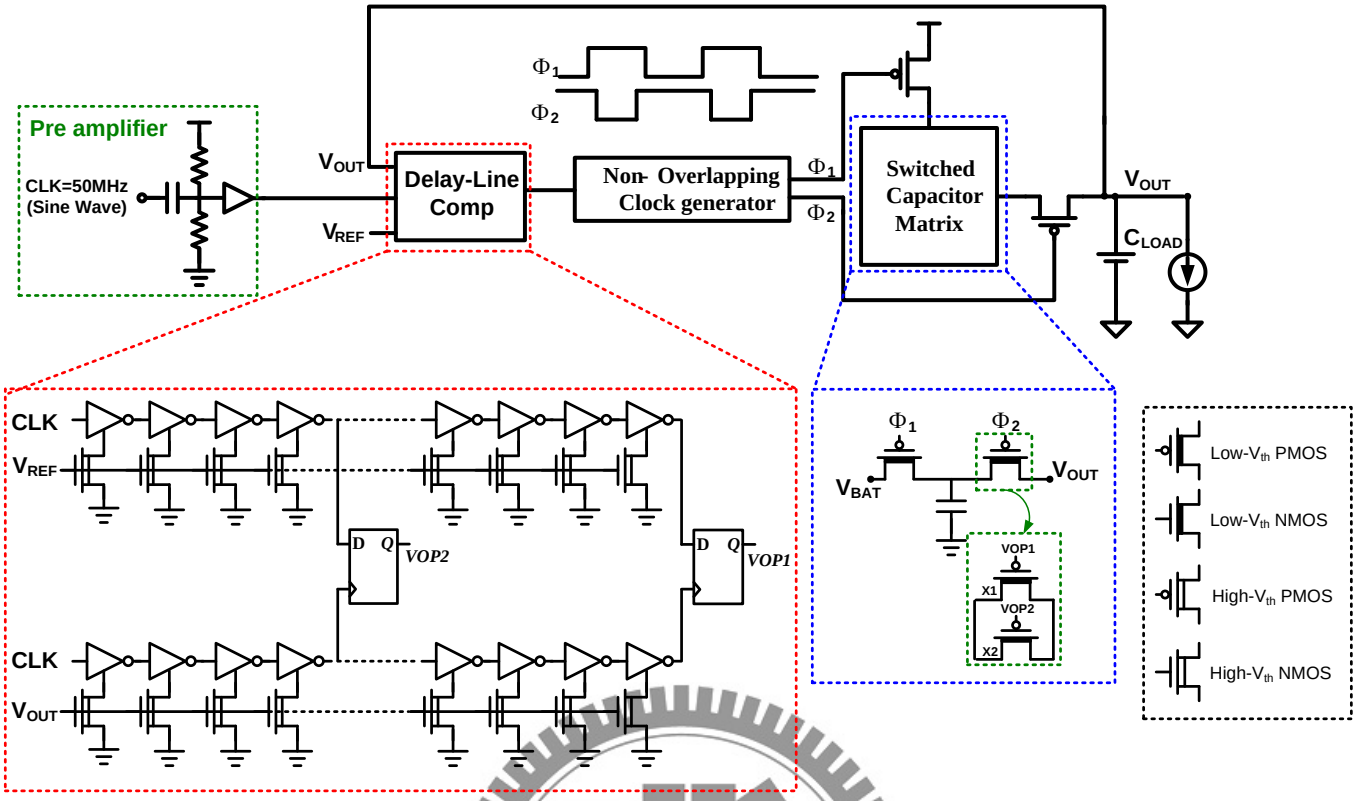


Figure 5.9. Architecture of switched capacitor DC-DC converter

Fig. 5.9 shows the architecture of the DC-DC converter. The converter uses a pulse frequency modulation (PFM) mode of control to regulate the output voltage. A TDC-based comparator clocked by the signal *clk* is used for this purpose. When the output voltage V_{OUT} is above V_{REF}, the switches are all set to the Φ_1 mode. When V_{OUT} falls below V_{REF}, the comparator triggers a Φ_2 pulse, which charges up the output load capacitor C_{load}. The non-overlapping clock generator block prevents any overlap between the Φ_1 and Φ_2 ON phases. A PFM mode control is crucial to achieving high efficiency for the extremely low power system being built. The switch matrix block contains the charge transfer switches and the charge transfer capacitors.

The external voltage input to the system is 0.5V. The gain setting at no-load provides a voltage ratio output of the input voltage. The switching losses in the converter are dominated by the energy expended in turning the charge transfer switches ON and OFF. The switch widths are designed such that the charge transfer

capacitors just settle at the end of a charge transfer cycle. In order to scale switching losses with load power, the charge transfer switches have adjustable widths which are enabled by the signals *VOP1, VOP2* as shown in the inset of Fig. 5.10.

The signals VOP1, VOP2 are generated by comparator. When the difference voltage between V_{OUT} and V_{REF} is larger, both the signals *VOP1, VOP2* are set to 1. While V_{OUT} is below V_{REF}, *VOP1* is set to 0. When next cycle, the V_{OUT} is still below V_{REF}, *VOP2* is set to 0. This helps to decrease the switching power, leading to an increase in efficiency at lower load power levels.

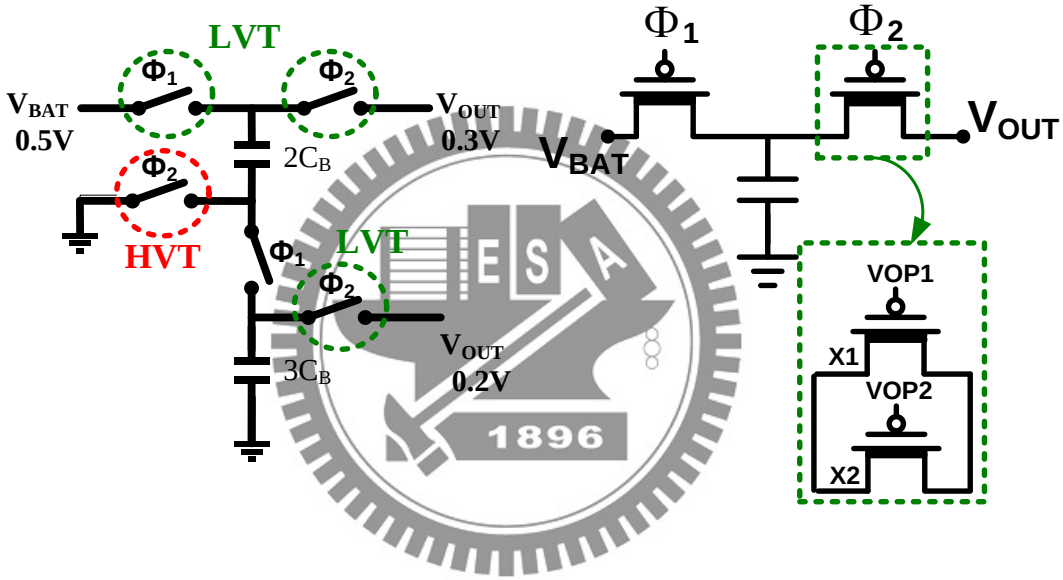


Figure 5.10. Switch matrix and simplified representation of the switch size control.

The efficiency of DC-DC converter is shown in Fig. 5.11. The converter was able to achieve >60% over a load current range from 10μA to 100μA. However, at very low load power levels (sub-5μW), leakage and other fixed losses in the control circuitry reduce the efficiency of the switched capacitor DC-DC converter [5.5].

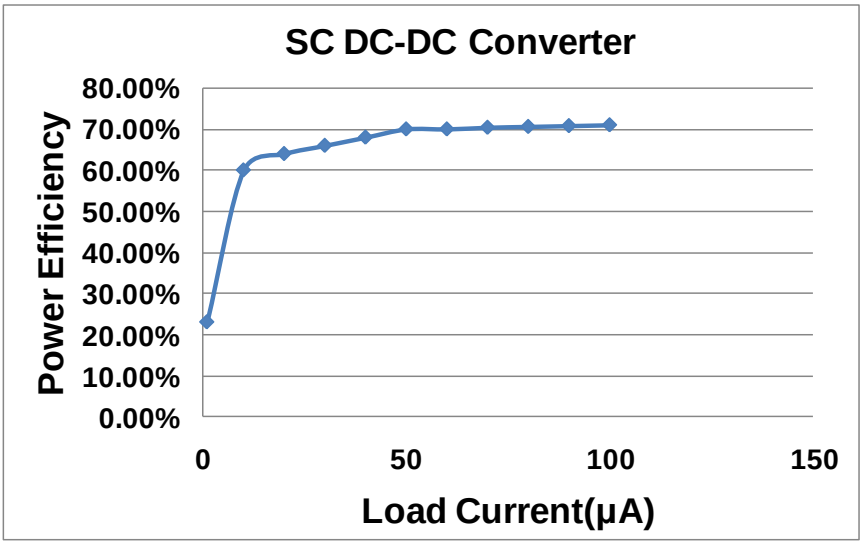


Figure 5.11. DC-DC converter efficiency while delivering 300 mV

5.3.2 Delay Line Comparator

As we know, operating speed of the circuit depends on its supply voltage. Higher supply voltage makes the circuit working faster than the lower supply voltage one. Thus, a comparator can be implemented through this characteristic. Fig. 5.12 shows the circuit of comparator, it composed of two stack-inverter chain and two D Flip-Flop. One of the two stack-inverter chain was connected to V_{REF} as stack nmos gate voltage. The other one was connected to V_{OUT} as stack nmos gate voltage. The two inverter chains input a clock signal (CLK) at the same time. When V_{REF} is greater than V_{OUT}, the below one has slower speed than above one. Therefore, while DFF triggered, Data is still 1, the signal *VOP1* is 1. On the other hand, when V_{REF} is less than V_{OUT}, the above inverter chain one has slower speed than below one. Thus, Data will ready before clock trigger DFF. The signal *VOP1* is 0, which means V_{OUT} is greater than V_{REF}.

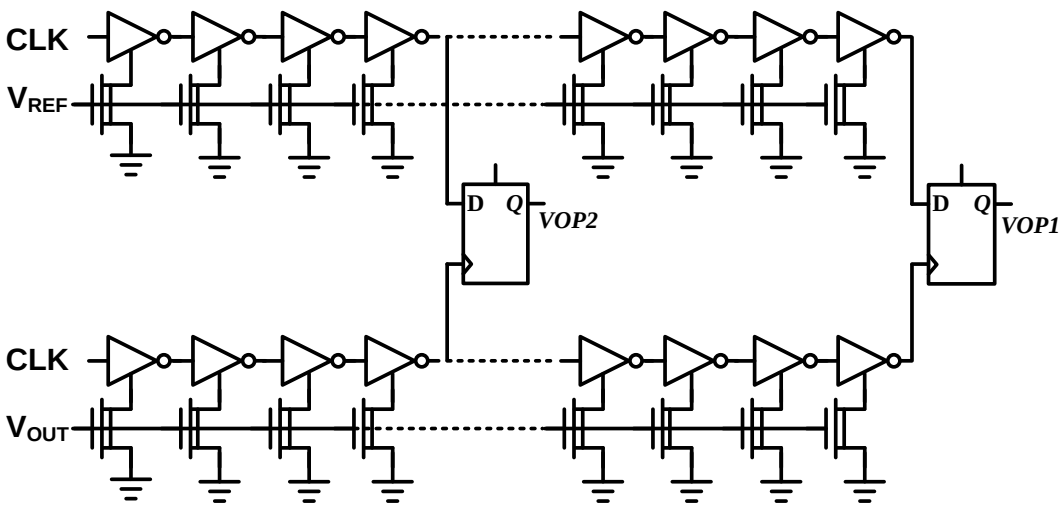


Figure 5.12. Delay line comparator

In Fig. 5.12, there is another signal named *VOP2*. The difference between *VOP1* and *VOP2* is the number of stack-inverter chain. It raised more inverter as a longer inverter chain. This target is to differentiate the degree of the difference voltage between V_{REF} and V_{OUT}. While V_{REF} is much greater than V_{OUT}, the delay of longer inverter chain which connected to V_{REF} is still shorter than connected to V_{OUT} one, even though it passed more inverter gate. Hence, when both the two signal *VOP1* and *VOP2* is 1, it presents the degree of the difference voltage between V_{REF} and V_{OUT} is large. So it need increased the width of switch in switch matrix to make the voltage transmit faster. The proposed comparator can compare 5mv voltage difference.

5.3.3 Subthreshold Voltage Reference

The traditional BVR(bandgap voltage reference) shows in Fig. 5.13 performance suffers as the supply voltage is lowered. The ability of the op amplifier to properly function as an error generator is reduced as the Input Common Mode Range (ICMR) of the op amplifier is degraded with a lower supply voltage when high loop gain is desired. This inhibits the reference's ability to match the PTAT and CTAT currents, resulting in a less accurate reference. The use of diodes to produce CTAT and PTAT

current outputs is impractical at low voltages, as the built-in voltage of a pn-junction is around 700mV and that severely limits the lower limit of the supply voltage; especially considering that all MOSFETs in the circuit are normally designed to have enough voltage headroom to operate in their saturation region.

A low power and low voltage subthreshold voltage reference is proposed and shown in Fig. 5.13. This design makes use of the weak inversion region of MOSFET operation to allow for an extremely low supply voltage with commensurate low power expenditure. Layout size is also reduced compared to the conventional BVR. The proposed subthreshold voltage reference is comprised of a bias network, a CTAT voltage generator, and a PTAT voltage generator that combine to produce the output reference voltage. As such, the drain current of a PMOS transistor operating in weak inversion can be modeled as,

$$I_D = I_{D0}\frac{W}{L}exp(\frac{V_{SG}-|V_{th}|}{nV_T}) \tag{5.16}$$

Where n is a slope factor (usually 1~2), and V_T is the thermal voltage. Solving for V_{SG} and including its temperature dependence yields,

$$V_{SG}(T) = V_{th}(T) + nV_T\, ln(\frac{I_D(T)}{I_{D0}(W/L)}) \tag{5.17}$$

Equation (5.17) consists of a near-linear term with respect to temperature and a non-linear term with respect to temperature; much like the model of a BJT. The near-linear component comes from V_{th}. Although this component isn't exactly linear, it can be approximated with a linear function in the temperature range we are using. The proposed reference circuit in Fig. 5.13 has components to cancel both the linear (first order) and non-linear (second order and above) temperature behavior. To

generate a simple low voltage and low powered PTAT voltage, a diode connected NFET was used. Fig. 5.14 shows the simulated gate-to-source voltage of M8 and the source-to-gate voltage of M6 as the temperature is swept from -40 ℃ to 100 ℃. As shown in Fig. 5.14, the source-to-gate voltage of M6 is CTAT and the gate-to-source voltage of M8 is PTAT. The CTAT source-to-gate voltage of M6 is applied to transconductance device M7 and the resulting current through M7 is CTAT. By scaling the sizes of M7 and M8 appropriately, when the CTAT current of M7 is passed through M8, the resulting gate-to-source voltage on M8 is (ideally) independent of temperature. The matching of the CTAT to PTAT characteristics is improved through the feedback mechanism present in M1-M5.

As shown in Fig. 5.15, the proposed subthreshold voltage reference shows a reference voltage of 319 mV with a 500 mV supply. The maximum variation in the output voltage is 711.78 μV or 2.2ppm/℃, over a -50℃ to 100℃ range. A variation of 121 μV, or 0.38ppm/℃, was demonstrated in the -50℃ to 100℃ range.

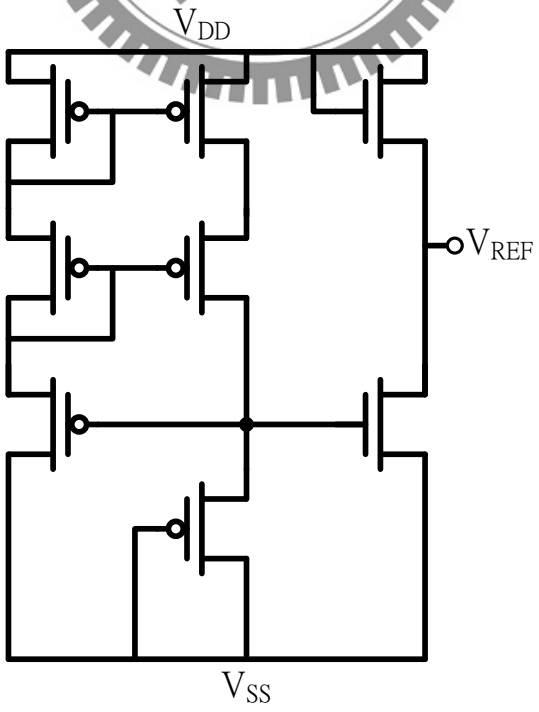


Figure 5.13. Proposed Bandgap Voltage Reference (BVR).

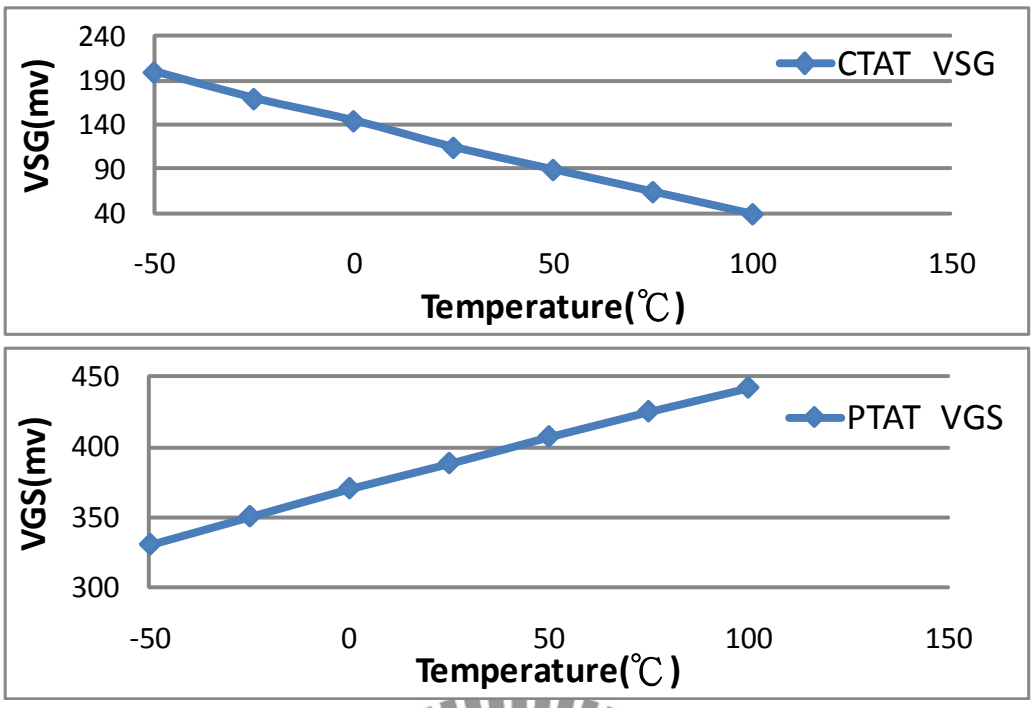


Figure 5.14. Simulated temperature dependence of an NFET and PFET.

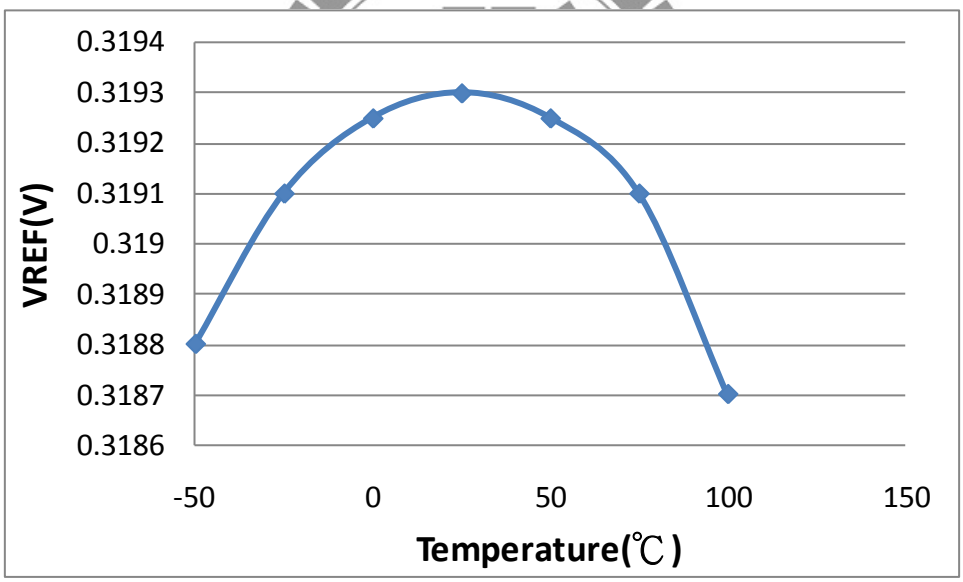


Figure 5.15. Simulated V_{REF} versus temperature.

5.3.4 Variable Voltage Reference Generation by DAC

In section 5.3.3, the subthreshold voltage reference can only output a fixed voltage 319 mV with a 500 mV supply. So this section proposed a variable voltage reference is generated by resistor-string DAC in Fig. 5.16. The decoder selects the output voltage for variable voltage reference. Fig. 5.17 and Table 5.1 are shown the Variable

voltage reference generation with temperature variation.

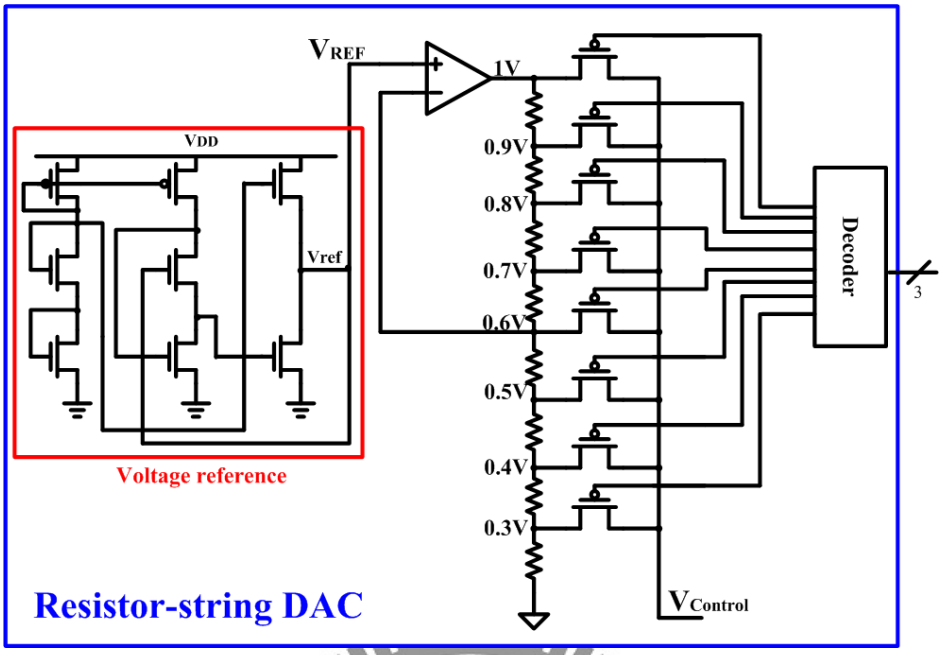


Figure 5.16 Resistor-string DAC for variable voltage reference generation.

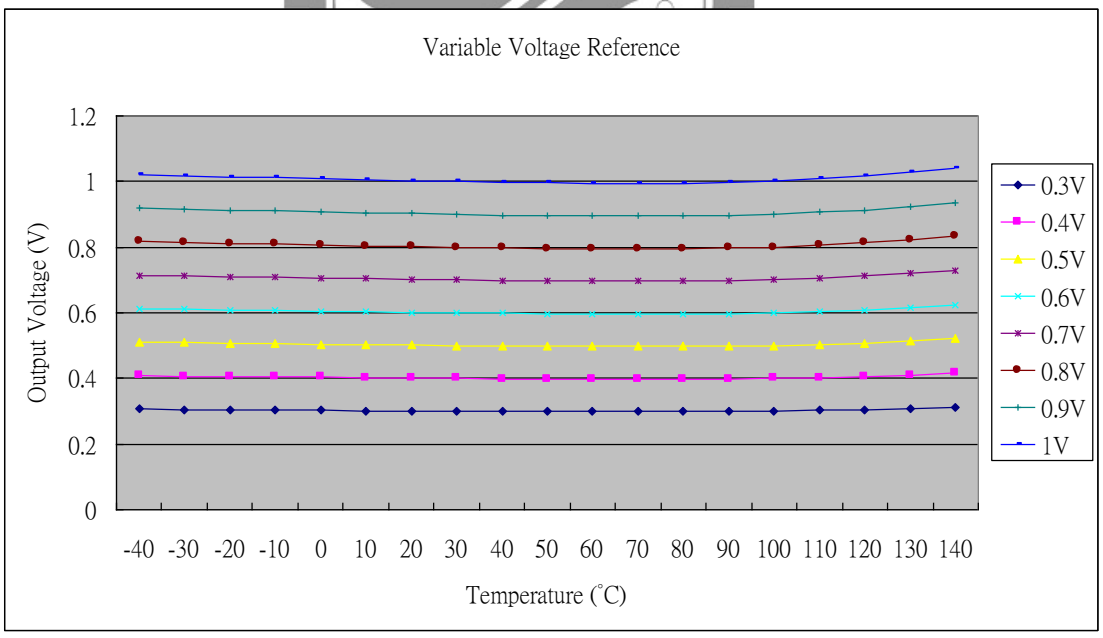


Figure 5.17 Variable voltage reference generation with temperature variation.

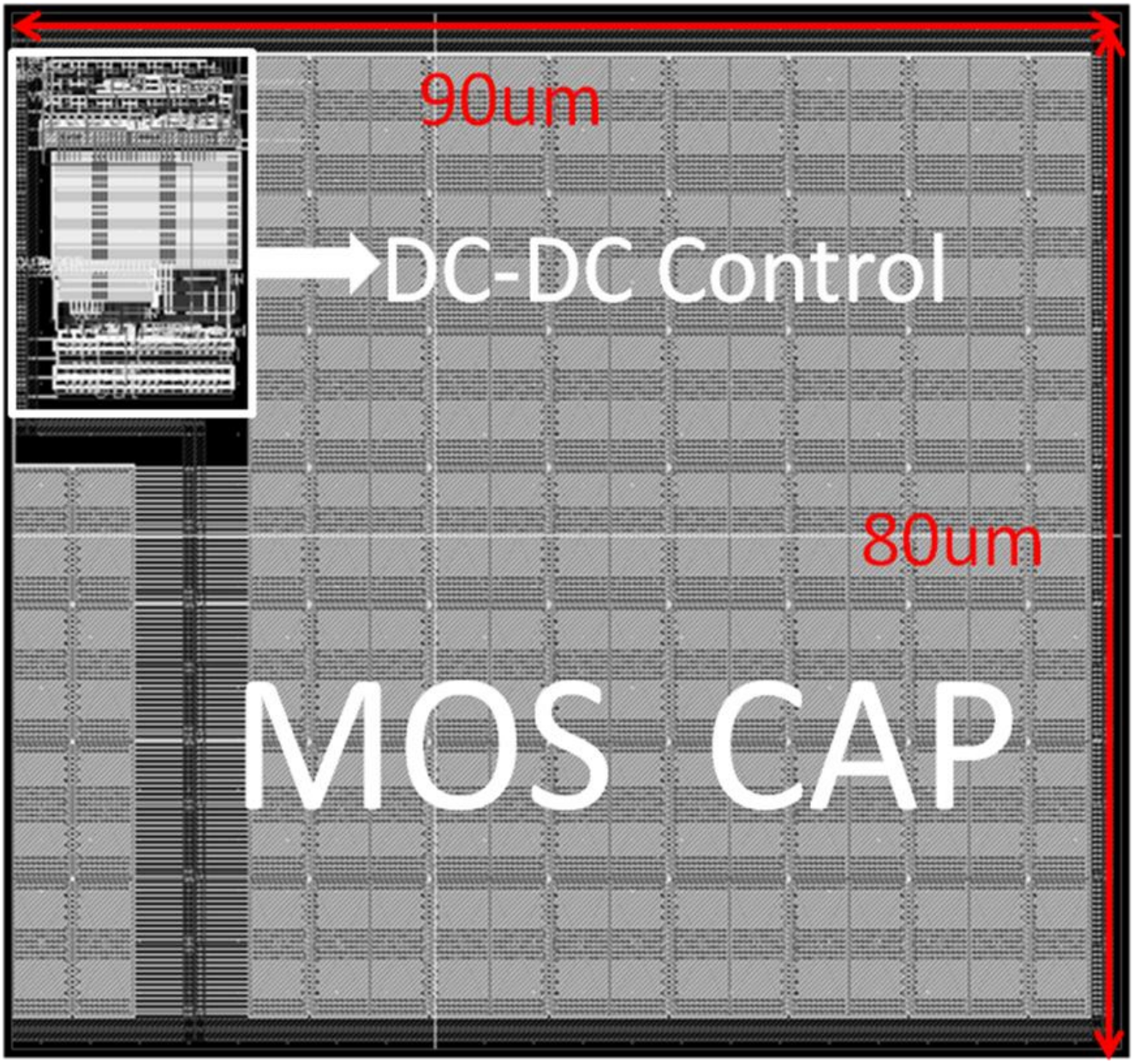
Table 5.1 Temperature variation				
Temperature	**-40° C**	**30° C**	**140° C**	**Variation**
1V	1.02	1.0	1.04	0.04V
0.9V	0.92	0.9	0.94	0.04V
0.8V	0.82	0.8	0.83	0.03V
0.7V	0.71	0.7	0.73	0.03V
0.6V	0.61	0.6	0.62	0.02V
0.5V	0.51	0.5	0.52	0.02V
0.4V	0.41	0.4	0.42	0.02V
0.3V	0.31	0.3	0.31	0.01V

5.4 Post-Layout Simulation Results

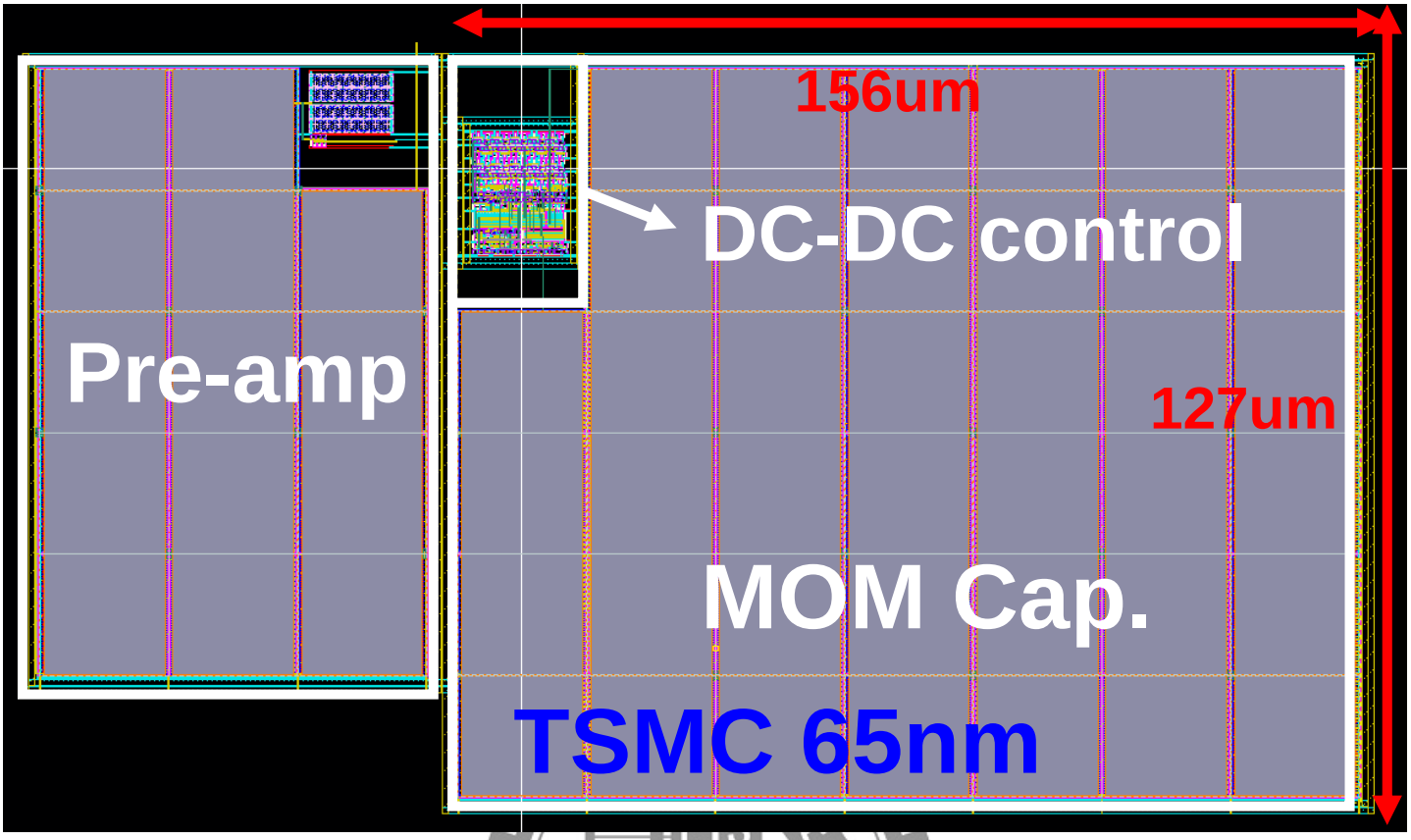
5.4.1 Layout

Layout view of the MTCMOS SC DC-DC converter with MOS capacitors in UMC 65nm standard CMOS technology is shown in Fig. 5.18(a). The area of MOS capacitors is smaller but has serious current leakage than other capacitors, so it has low power efficiency in very light load condition.

Layout view of the MTCMOS SC DC-DC converter with MOM capacitors in TSMC 65nm standard CMOS technology is shown in Fig. 5.18(b). The current leakage of MOM capacitors is small, so it has high power efficiency in light or heavy load condition.



(a)



(b)

Figure 5.18 Layout view of the SC DC-DC converter. (a) with MOS capacitor in UMC 65nm CMOS tech. (b) with MOM capacitor in TSMC 65nm CMOS tech.

5.4.2 The Layout of the power MOS

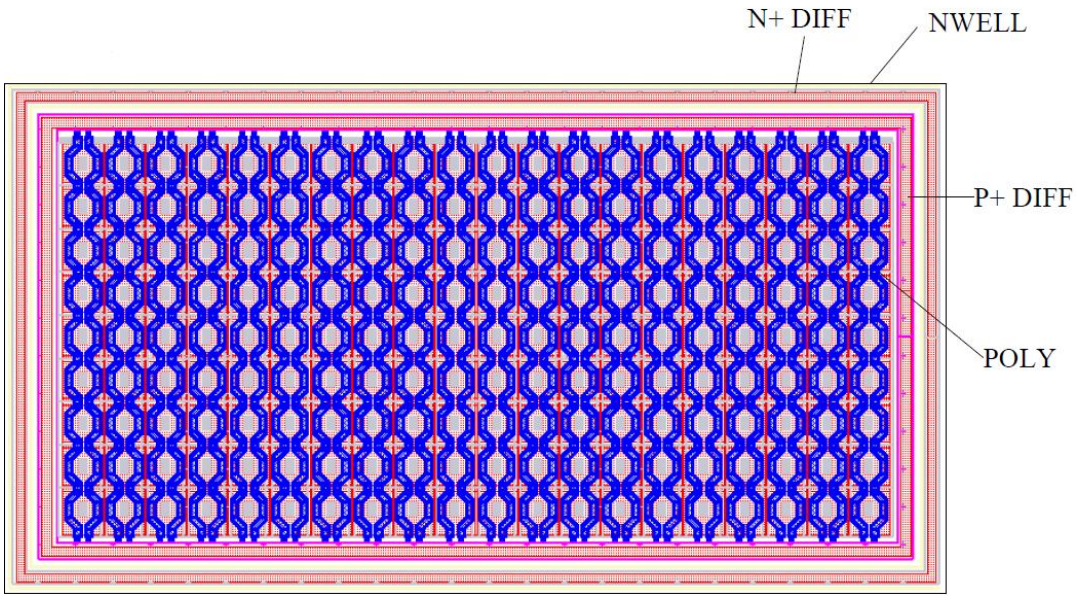
From layout view of SC DC-DC converter, we knows that the size of power MOS may be one thousand (1000um) in the maximum current loading. The huge size causes different layout for some purpose.

In Fig. 5.19, the poly-silicon is drawn as a beehive in order to get better electro-Static Discharge (ESD) protection. In this kind of layout, the drain and source will be an octagon, improving the point discharge effect in the rectangle. The causation of the electro-Static Discharge can be listed as four kinds of type: human

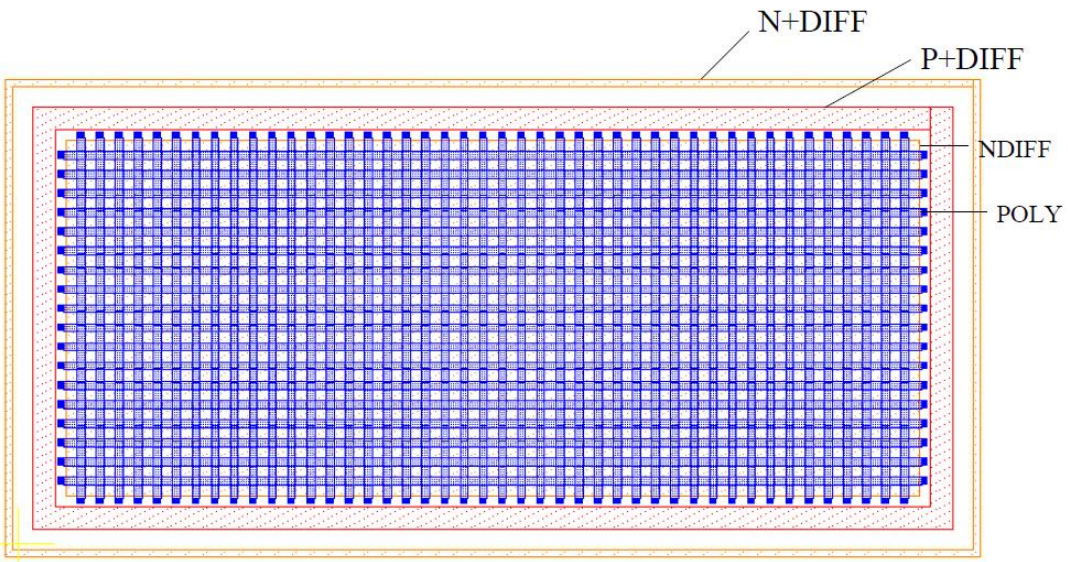
body model, machine model, charged device model and field induced model.

The human model and machine model are caused by the external static electricity. Therefore, we usually make some protection between the core and the pad. In the output ping, we usually use an output stage with large size to push the external load. The large size output stage which can endure large current is also a good discharge path of the static electricity. Therefore, we draw the layout as Fig. 5.19(a) to make the power MOS as an output stage with better ESD protection.

However, the layout as Fig. 5.19(b) will save more area. Fig. 5.20 shows the equivalent MOS of Fig. 5.19(a) and (b) in the same area. The layout as Fig. 5.19(a) will produce 30 equivalent MOS and the layout as Fig. 5.19(b) will produce 49 equivalent MOS.

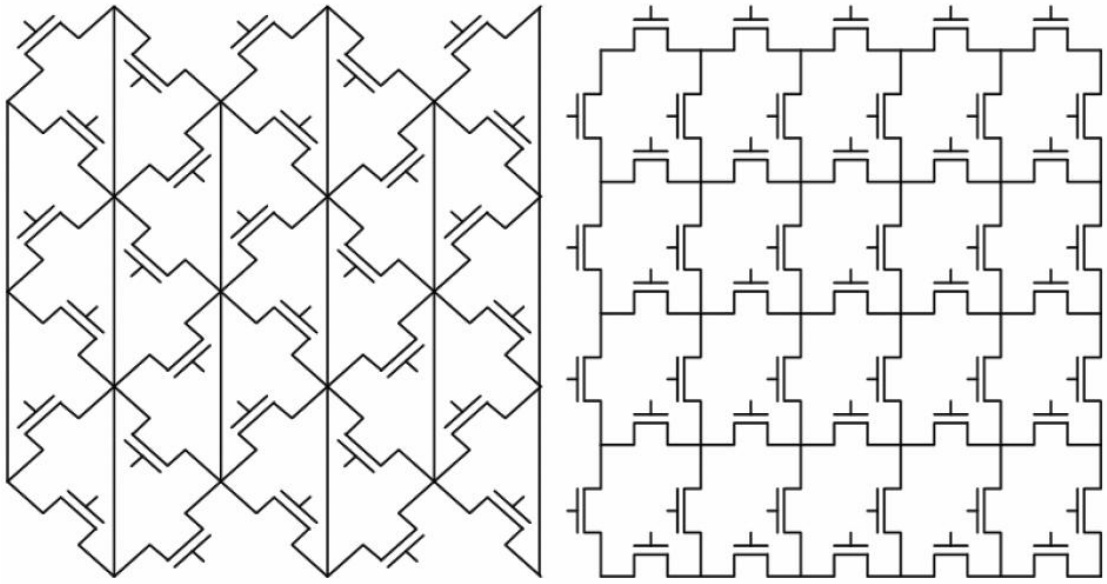


(a)



(b)

Figure 5.19 The layout of the Power MOS (a) with better ESD protection (b) with better efficiency of area.



(a) (b)

Figure 5.20 The equivalent MOS of layout in Fig. 5.18(a) and(b).

5.4.3 Post-Simulation Results

The transient response of SC DC-DC converter is shown in Fig.5.21. The converter was able to achieve >60% over a load current range from 10μA to 100μA. The converter has small voltage variation, because the proposed delay-line based comparator can detect 5mv voltage variation. The comparison of switched capacitor DC-DC converter is shown in Table 5.2.

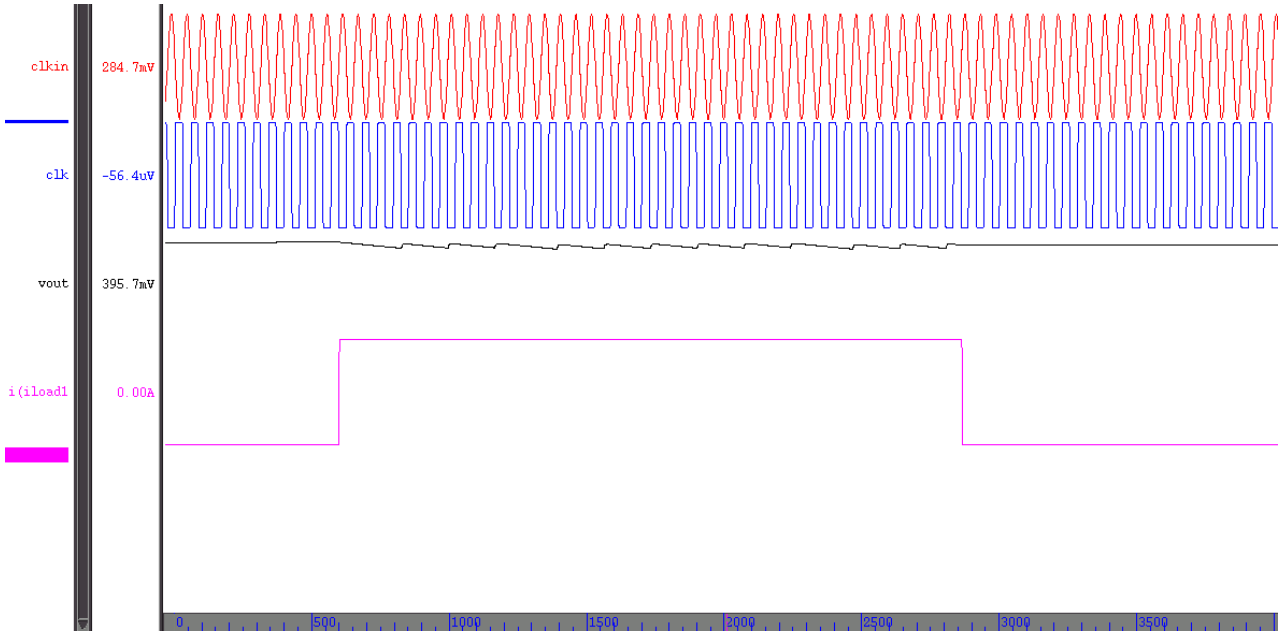
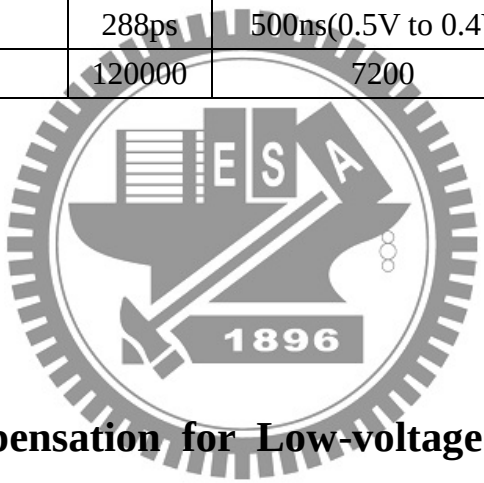


Figure 5.21 The transient response of SC DC-DC converter.

Table 5.2 Comparison of [5.2], [5.5] and proposed switched DC-DC conberter.				
	Ref.[5.2]	Ref.[5.5]	This work (MOS Cap.)	This work (MOM Cap.)
Technology	0.18μm	65nm	UMC 65nm	TSMC 65nm
Input Voltage	1.2V	0.5V	0.5V	0.5V
Output Voltage	0.3~1.1V	0.3V	0.2~0.4V	0.2~0.4V
Variation ΔV_{OUT}	8%	10%	4%	4%
MAX Load Current	400uA	400uA	70uA	80uA
Power Efficiency	75%@(1.2V to 0.5V)	75%	70%@(0.5V to 0.4V) 60%@(0.5V to 0.2V)	78%@(0.5V to 0.4V) 64%@(0.5V to 0.2V)
Switch Cap.	0.6nF	600pF	30pF(MOS Cap.)	30pF(MIM. Cap.)
Response time	540ps	288ps	500ns(0.5V to 0.4V)	450ns(0.5V to 0.4V)
Area(μm^2)	750000	120000	7200	21280



5.5 Temp. Compensation for Low-voltage Digital Assisted PLL

A conventional phase lock loop (PLL) is a control system that tries to generate an output signal whose phase is related to the phase of the input "reference" signal. A phase-locked loop circuit compares the phase of the input signal with a phase signal derived from its output oscillator signal and adjusts the frequency of its oscillator to keep the phases matched.

The architecture of PLL is shown in Fig. 5.22. A phase detector (PFD) compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the VCO frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency at the other input. This input is called the reference and is often derived from a crystal oscillator, which is very stable in frequency.

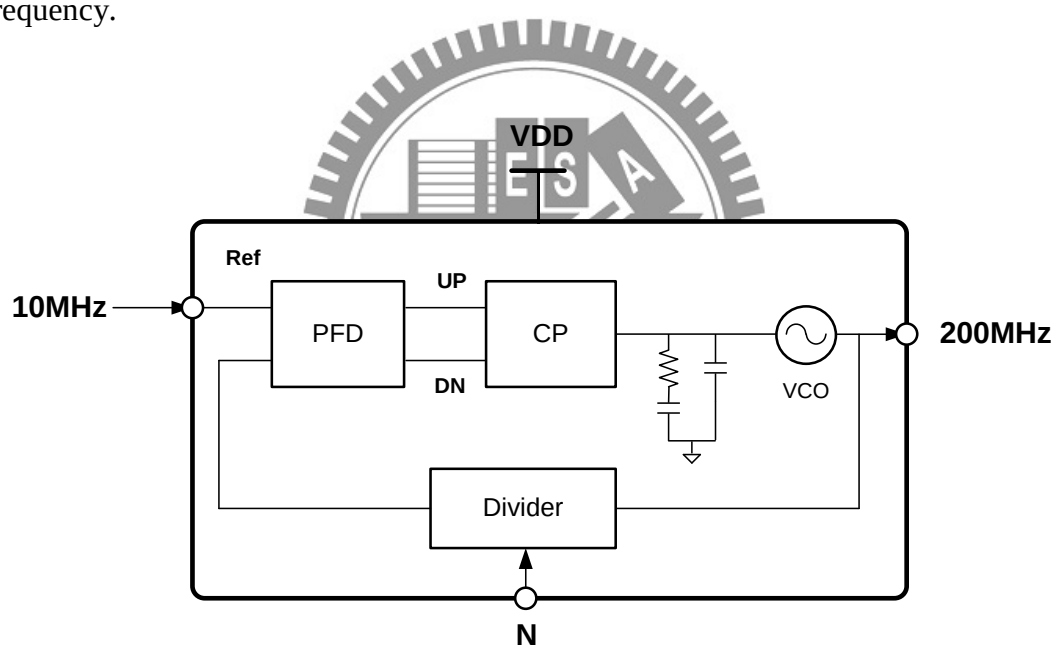


Figure 5.22 Architecture of phase lock loop (PLL).

When we reduce the supply voltage to near/ sub-threshold region ($V_{DD} \leqq 0.5V$), the VCO output frequency range does not cover desired frequency in FF, 0.55V, 100℃ and SS, 0.45V, 0℃. The VCO output frequency shows the simulation result as below Fig. 5.23.

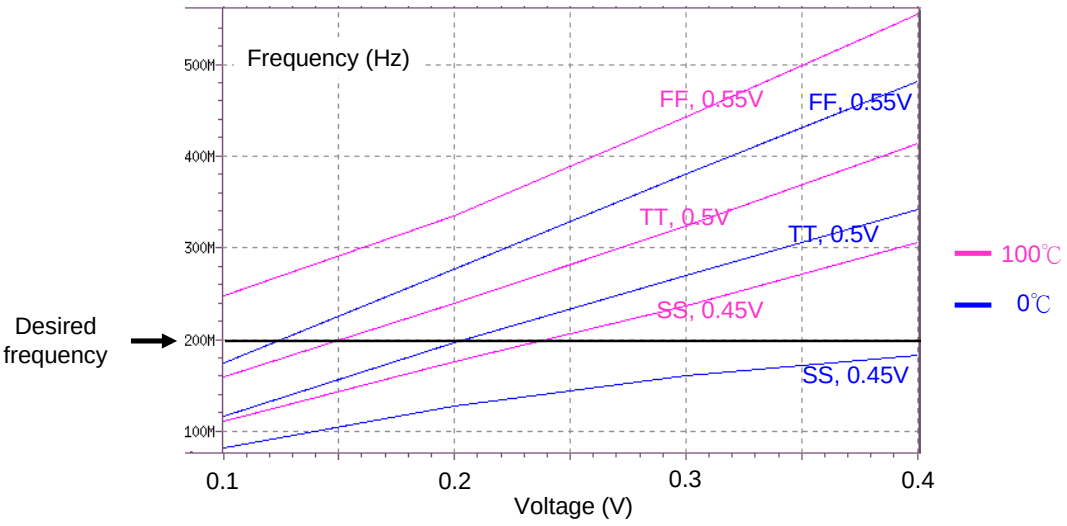


Figure 5.23 Simulation results of VCO output frequency in different environment condition.

Because of above problem, we use temperature sensors to compensate the VCO output frequency. The architecture of proposed temperature compensation for low-voltage digital assisted PLL is shown in Fig. 5.24. The VCO output frequency with temperature compensation shows the simulation result as below Fig. 5.25. From the above simulation results, the VCO output frequency can cover desired frequency range after temperature compensation.

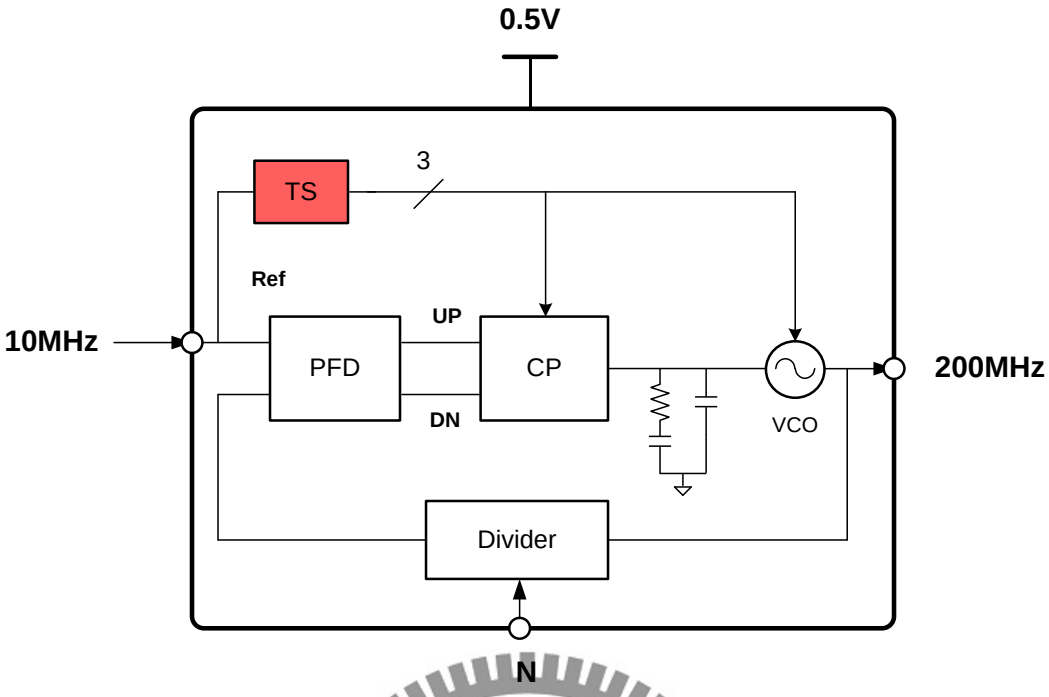


Figure 5.24 Architecture of proposed temp. compensation for low-voltage digital assisted PLL.

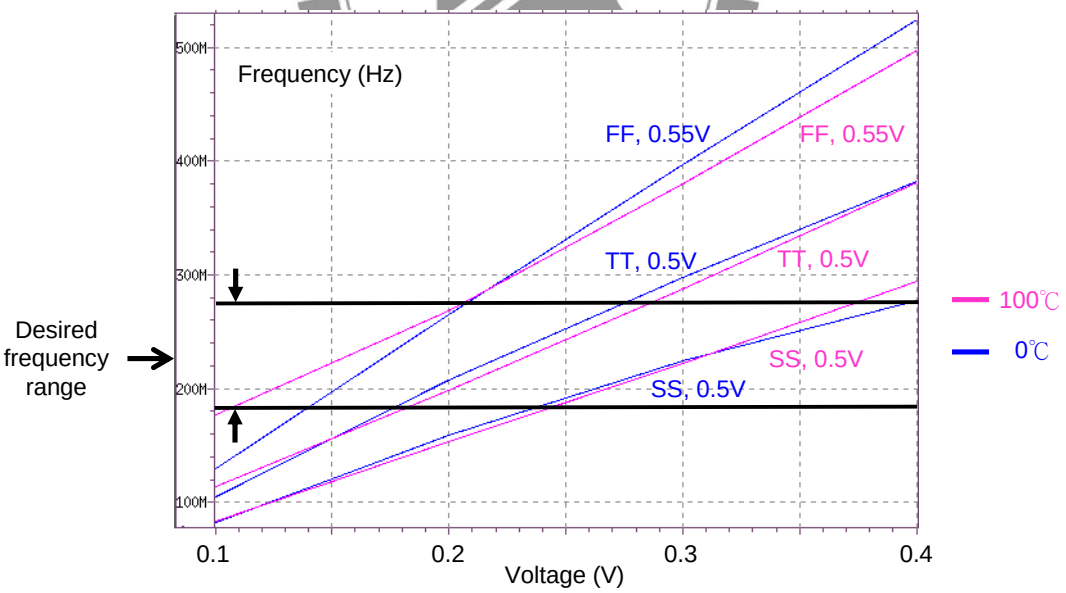


Figure 5.25 Simulation results of VCO output frequency in different environment condition with temperature compensation.

5.6 Summary

This chapter presents circuits that enable dynamic voltage and frequency scaling (DVFS) for micro-watt system to reduce both dynamic and leakage power dissipation. The system consists of the MTCMOS SC DC-DC converter, and temperature compensation technique for low-voltage digital assist PLL. The SC DC-DC converter uses PVT sensors to adjust output supply voltage in different environmental variation. Low-voltage PLL uses temperature sensor to compensate the output frequency.

For MTCMOS SC DC-DC converter, we improve the output voltage variation and power efficiency by using delay-line based comparator and multi-threshold CMOS technology. For low-voltage digital assisted PLL, we use temperature sensor to compensate VCO output frequency in worse case.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

In this thesis, we proposed a 1-point calibration near-/sub-threshold PVT sensor in Chapter 3. A self-calibration near-/sub-threshold digital PVT sensors and a self-calibration near-/sub-threshold digital temperature sensor with adaptive pulse width generator are proposed in Chapter 4. In Chapter 5, we proposed a multi-threshold CMOS switched capacitor (SC) DC-DC converter with 70% power efficiency and 4% voltage variation for micro-watt DVFS system design. We also proposed a temperature compensation for low-voltage digital assisted PLL; it can generate output frequency cover our desired frequency in any environment condition.

The research results of Chapter 3, Chapter 4, and Chapter5 are applied to PVT sensors for micro-watt DVFS system design.

The PVT sensors micro-watt DVFS system can provides process, voltage, and temperature value, dynamically varying clock frequency and supply voltage level. The DVFS control can reduce total energy consumption in sleep mode.

6.2 Future Work

Wireless medical microsensors are usually with two different operating modes: *Low-Power Mode* and *Performance Mode* because the well-known signals of the main characteristics of cardiac activity, e.g. heart rate and ECG, are at a very low rate. More than 99% operating time of sensor nodes are operating in *low-power mode* to record various physiological signals throughout its life time while only less than 1% operating time in *performance mode* to process and transmit real-time informative

cardiovascular parameters to a host. This *low-power-mode*-dominated scenario is capable of further reducing total energy consumption if dynamic voltage scaling (DVS) technique is applied. The benefit of DVS technique is attributed to the quadratic savings in active CV_{DD}^2 energy. In this work, an on-chip switched capacitor(SC) DC-DC converter which can deliver desired supply voltage for each operating mode is integrated with proposed asynchronous 8T SRAM-based FIFO. Device in *low-power mode* and *performance mode* will perform sub-threshold operation and near-threshold operation respectively.

A robust near-/sub-threshold SRAM-based FIFO for WBAN applications is shown in Fig. 6.1(a). To achieve high reliability and extend battery working time, ULV dual-port SRAM-based FIFO is applicable. The conventional dual-port SRAM fails to perform reliable subthreshold operation because of read disturb induced read static noise margin (RSNM) degradation. Plenty of subthreshold SRAMs have been implemented to overcome the degradation. However, threshold voltage shift due to random doping fluctuations and processing variation causes SRAM reliability getting worse. In addition, the reduction of signal level directly hurts the noise margin of memory. As technology scaling, the smaller I_{on}-I_{off}-ratio limits the sharing elements like SRAM. All of the ULV effects are considered in 2Kb proposed 8T SRAM cell, shown in Fig. 6.1(b), in this work.

Besides a near-/sub-threshold memory is required, a novel switched capacitor (SC) DC-DC converter and smart dynamic voltage scaling controller are proposed. The schematic views of them are shown in Fig. 6.2(a) and Fig. 6.2(b), respectively. The SC DC-DC converter uses a pulse frequency modulation (PFM) mode of control to regulate the output voltage. When the output voltage V_L is above V_{ref}, the switches are all set to the Φ_1 mode. When V_L falls below V_{ref}, the comparator triggers a Φ_2 pulse, which charges up the output load capacitor C_{LOAD}. The non-overlapping clock

generator block prevents any overlap between the Φ_1 and Φ_2 ON phases. The power efficiency of DC-DC converter is no less than 70% over a load current range from 10μA to 100μA. Following a request for a voltage switch (where the signal *MODE* changes), correct operation of the FIFO is guaranteed by sending a *stall* request before the actual switching of voltage. Stalling prevents processor operation during the period when the voltage supply is not completely connected. The stored data in FIFO are preserved within the internal circuits. When stalling is finished, a confirmation signal (*stall_done*) is transmitted back to the supply switch circuit. Finally, the stall signal is released after the new voltage supply is fully connected.

Thermal issues are fast becoming major design constraints in subthreshold systems. Temperature variations adversely affect system reliability and prompt worst-case design. A dynamic temperature management (DTM) techniques uses to target average-case design and tack the temperature issue at runtime. A novel digital temperature sensor and dynamic temperature management mechanism are proposed. The schematic views of them are shown in Fig. 6.3(a) and Fig. 6.3(b), respectively.

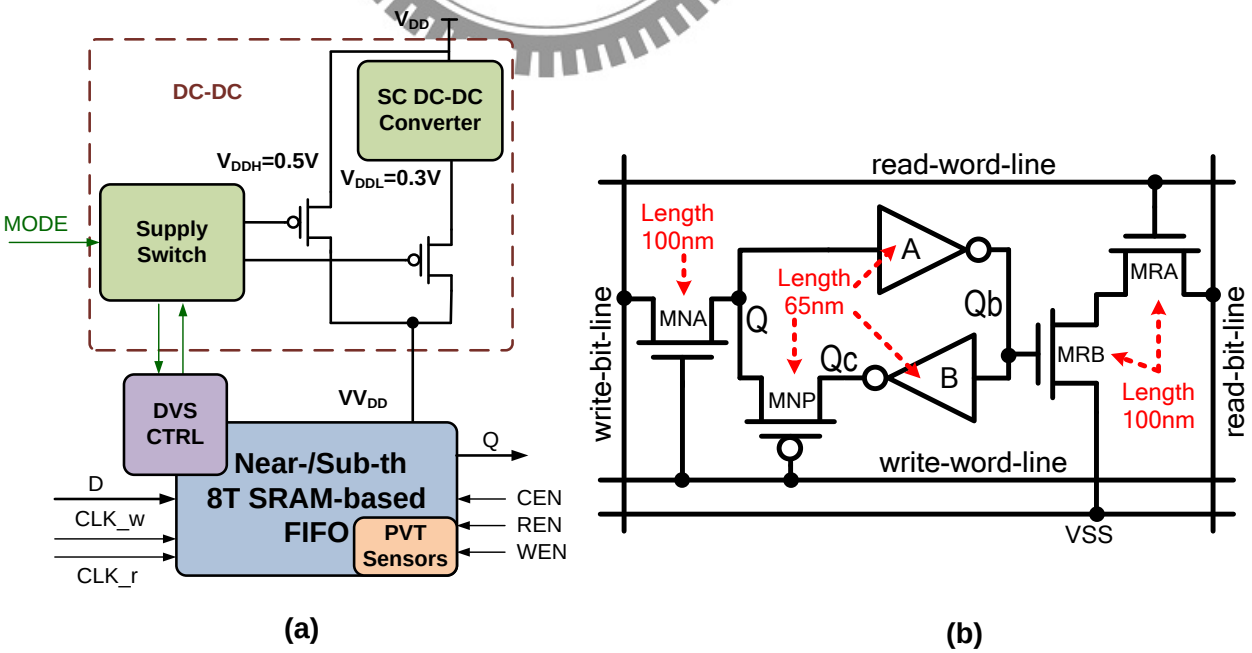
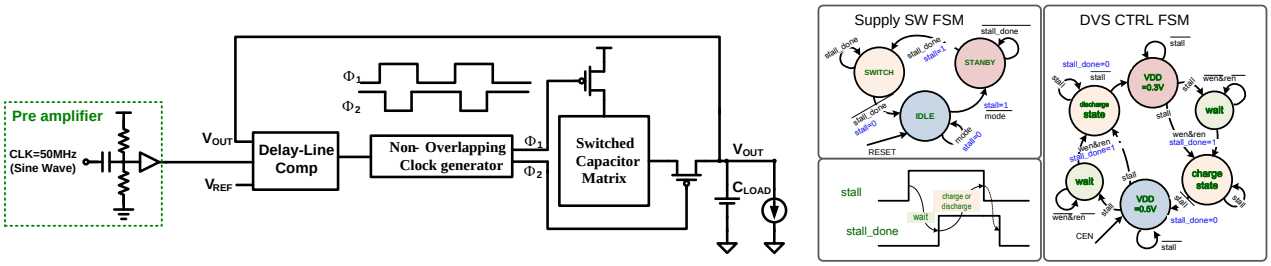
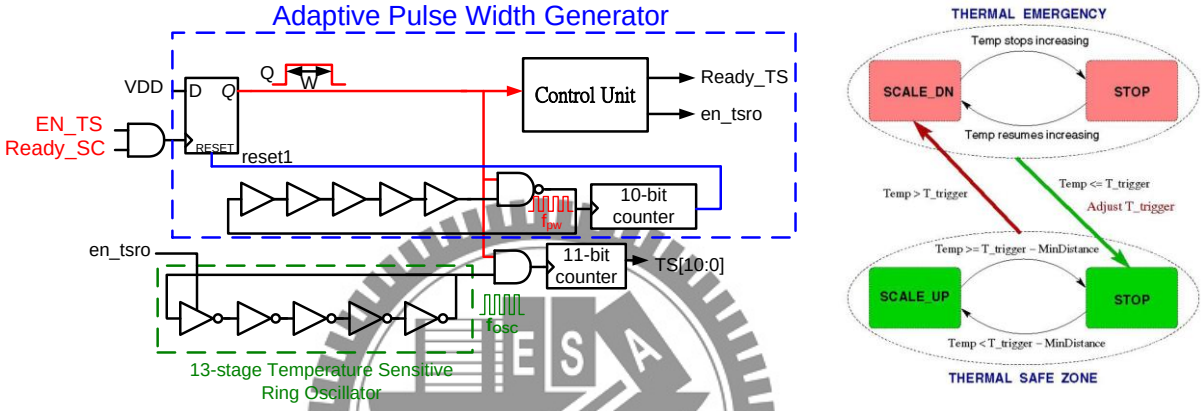


Figure 6.1 (a) Block diagram of Near/Sub- threshold FIFO memory. (b) Proposed 8T Near/Sub-threshold SRAM cell.



(a) (b)

Figure 6.2 (a) ULV MTCMOS SC DC-DC converter. (b) Smart dynamic voltage scaling converter.



(a) (b)

Figure 6.3 (a) Self-calibration temperature sensor with adaptive pulse width generator. (b) DTM algorithm.

Bibliography

[1.1] J. Y. Yu, C. C. Chung, W. C. Liao, C. Y. Lee, “A sub-mW Multi-Tone CDMA Baseband Transceiver Chipset for Wireless Body Area Network Applications,” *ISSCC Tech. Digest*, pp. 364-609, February 2007.

[1.2] J. Y. Yu, W. C. Liao, and C. Y. Lee, “An MT-CDMA Based Wireless Body Area Network for Ubiquitous Healthcare Monitoring,” *IEEE BioCAS*, November 2006.

[1.3] D. Markovic, C. C. Wang, L. P. Alarcon, L. T. Tsung, J. M. Rabaey, "Ultralow-Power Design in Near-Threshold Region," in *Proceedings of the IEEE* , vol.98, no.2, pp.237-252, Feb. 2010

[1.4] W. H. Cheng and B. M. Baas, ” Dynamic Voltage and Frequency Scaling Circuits with Two Supply Voltages,” in IEEE Int’l Symp. Circuits and Systems, pp. 1236-1239, June 2008.

[1.5] B. H. Calhoun, J. Bolus, S. Khanna, A. D. Jurik, A. C. Weaver, T. N. Blalock, ”Sub-threshold operation and cross-hierarchy design for ultra low power wearable sensors,” in *IEEE Int’l Symp. Circuits and Systems*, pp. 1437-1440, May 2009.

[1.6] B. H. Calhoun, S. Khanna, R. Mann, and J. Wang, ”Sub-threshold circuit design with shrinking CMOS devices,” in *IEEE Int’l Symp. Circuits and Systems*, pp. 2541-2544, May 2009.

[1.7] J. A. Paradiso and T. Starner, ”Energy scavenging for mobile and wireless electronics,” in *IEEE Pervasive Comput.*, vol. 4, no.1, pp. 18-27, 2005.

[1.8] T. Vucurevich, ”The long road to 3D integration: are we there yet?,” in *3D Architecture Conference*, Keynote Speech, 2007.

[1.9] X. Dong and Y. Xie, ”System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs),” in *Asia and South Pacific Design Automation Conf.*, pp. 234-241, Jan. 2009.

[2.1] K.K. Kim and Y.B Kim, “A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems”, *IEEE Trans. VLSI Systems*, vol. 17, no. 4, pp. 517-528, April 2009.

[2.2] R. Jacob Baker, *CMOS: Circuit Design Layout, and Simulation*. New York: Wiley-Interscience, 2005.

[2.3] M. A. Farahat , F. A. Farag, and H. A. Elsimary, “Only digital technology analog-to-digital converter circuit,” *IEEE Trans.* I*nternational Midwest Symposium on Circuits and Systems*, Vol.1, pp. 178-181, Dec. 2003.

[2.4] C. K. Kim, B. S. Kong, C. G. Lee, and Y. H. Jun, “CMOS Temperature Sensor with Ring Oscillator for Mobile DRAM Self-refresh Control,” *IEEE Trans.*

Circuit and System, pp.3094-3097, May. 2008.

[2.5] M. A. Pertijs, A. Niederkorn, M. Xu, B. McKillop, A. Bakker, and J.H. Huijsing, "A CMOS smart temperature sensor with a 3σinaccuracy of ±0.1℃from -5℃ to125℃," *IEEE J. Solid-State Circuits*, vol.40, no. 12, pp. 2805–2815, Dec. 2005.

[2.6] V. Székely, Cs. Márta, Zs. Kohári, and M. Rencz, "CMOS sensors for on-line thermal monitoring of VLSI circuits," *IEEE Trans. VLSI Syst.*, vol. 5, no. 3, pp. 270–276, Sep. 1997.

[2.7] M. Sasaki, M. Ikeda, K. Asada, "A Temperature Sensor With an Inaccuracy of -1/+0.8 ℃ Using 90-nm 1-V CMOS for Online Thermal Monitoring of VLSI Circuits," *IEEE Trans. Semiconductor manufacturing*, vol. 21, no. 2, pp. 201–208, May 2008.

[2.8] A. Bakker and J. H. Huijsing, "CMOS smart temperature sensor - an overview," in *Proc. IEEE Sensors*, vol. 2, Jun. 2002, pp. 1423–1427.

[2.9] P. Chen, C. C. Chen; C. C. Tsai, W. F. Lu, "A Time-to-Digital-Converter-Based CMOS Smart Temperature Sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, PP1642-1648, August 2005.

[2.10] C. C. Chen, A. W. Liu, Y. C. Chang, P. Chen, "An accurate CMOS delay-line-based smart temperature sensor for low-power low-cost systems," *Meas. Sci. Technol.*, vol. 17, no. 4, pp. 840–846, Apr. 2006.

[2.11] T. T. Nguyen, S. Kwansu, S. W. Kim, "A Delay Line with Highly Linear Thermal Sensitivity for smart temperature sensor," *IEEE Trans. Circuit and System*, pp.899-902, Aug. 2007.

[2.12] P. Chen, M. C. Shie, Z. Y. Zheng, Z. F. Zheng, C. Y. Chu, "A Fully Digital Time-Domain Smart Temperature Sensor Realized With 140 FPGA Logic Elements", *IEEE Trans. Circuit and system*, vol. 54, no. 12, pp. 2661–2668, December 2007.

[2.13] P. Chen, K. M. Wang, Y. H. Peng, Y. S. Wang, C. C. Chen, "A Time-Domain SAR Temperature Sensor with -0.25℃~+0.35℃ Inaccuracy for On-Chip Monitoring," *ESSCIRC*, pp.70-73, Sept. 2008.

[2.14] M. K. Law, A. Bermak, "A Time Domain Differential CMOS Temperature Sensor with Reduced Supply Sensitivity," *IEEE Trans. Circuit and system*, pp.2126-2129, May 2008.

[2.15] Yi Ren, C.Wang, and H. Hong, "An All CMOS Temperature Sensor for Thermal Monitoring of VLSI Circuits," *IEEE ICTD*, pp. 1-5, April 2009.

[2.16] T. A. Demassa and Z. Ciccone, *Digital Integrated Circuits*. New York: Wiley, 1996.

[2.17] K. Woo, S. Meninger, T. Xanthopoulos, E. Crain, Ha. Dongwan, Ham. Donhee, "Dual-DLL-based CMOS all-digital temperature sensor for microprocessor thermal monitoring," *IEEE ISSCC*, pp. 68–69, Feb. 2009.

[2.18] M. Mondal, A. J. Ricketts, S. Kirolos, T. Ragheb, G. Link, N. Vijaykrishnan, Y. Massoud, "Thermally Robust Clocking Schemes for 3D Integrated Circuits," *IEEE DATE*, pp. 1–6, April 2007.

[2.19] K.K. Kim and Y.B Kim, "A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems," *IEEE Trans. VLSI Systems*, vol. 17, no. 4, pp. 517-528, April 2009.

[3.1] R.B.Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, P. T. Balsara, "1.3V 20p Time-to-Digital Converter for Frequency Synthesis in 90-nm CMOS", *IEEE Trans. CAS II*, pp.220-224, Mar.2006.

[3.2] C. M. Hsu, M. Z. Straayer, M. H. Perrott, "A Low-Noise, Wide-BW 3.6GHz Digital ΔΣ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *ISSCC*, pp.340-617, Feb. 2008.

[3.3] K. Nose, M. Kajita, M. Mizuno, "A 1-ps Resolution Jitter Measurement Macro Using Interpolated Jitter Oversampling," *IEEE J. Solid-State Circuits*, pp.2911-2920, Dec. 2006.

[3.4] T. Komuro, "ADC Architecture Using Time-to-Digital Converter," *IEICE* vol. J90-C, April 2007.

[3.5] P. Chen, C. .C Chen, Y. H. Peng, K. M. Wang, Y. S. Wang, "A Time-Domain SAR Smart Temperature Sensor With Curvature Compensation and a 3σ Inaccuracy of −0.4°C~+0.6°C Over a 0°C to 90°C Range," IEEE J. Solid-State Circuits, pp.600-609, Feb. 2010.

[3.6] R. Rashidzadeh, M. Ahmadi, W. C. Miller, "An All-Digital Self-Calibration Method for a Vernier-Based Time-to-Digital Converter," *IEEE Trans. Instrumentation and Measurement*, vol.59, no.2, pp.463-469, Feb. 2010.

[3.7] K. A. Bowman, B. L. Austin, J. C. Eble, X. Tang, and J. D. Meindl, "A Physical Alpha-Power Law MOSFET Model," *IEEE J. Solid-State Circuits*, vol. 34, no.10, pp. 1410-1414, Oct. 1999.

[4.1] P. M. Levine and G. W. Roberts, "A high-resolution flash time-to-digital converter and calibration scheme," in *IEEE Int. Test Conf.*, pp. 1148–1157, Feb. 2004.

[4.2] V. Gutnik and A. Chandrakasan, "On-chip picosecond time measurement," in *Proc. IEEE VLSI Circuits Dig. Tech. Papers*, pp. 52–53, May. 2000.

[4.3] J. Rivoir, "Fully-digital time-to-digital converter for ATE with autonomous calibration," in *Proc. IEEE Int. Test Conf.*, pp. 1–10, Oct. 2006.

[4.4] J. Rivoir, “Statistical linearity calibration of time-to-digital converters using a free-running ring oscillator,” in *Proc. 15th Asian Test Symp.*, pp. 45–50, Nov. 2006.

[4.5] P. Chen, C. .C Chen, Y. H. Peng, K. M. Wang, Y. S. Wang, “A Time-Domain SAR Smart Temperature Sensor With Curvature Compensation and a 3σ Inaccuracy of −0.4°C~+0.6°C Over a 0°C to 90°C Range,” IEEE J. Solid-State Circuits, pp.600-609, Feb. 2010.

[5.1] W. H. Cheng and B. M. Baas, “Dynamic voltage and frequency scaling circuits with two supply voltages,” *IEEE Asian Solid-State Circuits Conference*, pp.1236-1239, Nov. 2007.

[5.2] Y. K. Ramadass and A. P. Chandrakasan, “Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications,” *IEEE PESC*, pp. 2353–2359, June 2007.

[5.3] J. Kwong, Y. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, A. P. Chandrakasan, “A 65nm Sub-Vt Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter,” *IEEE ISSCC*, pp.318-616, Feb. 2008.

[5.4] Mengzhe Ma, ” Design of High Efficiency Step-Down Switched Capacitor DC/DC Converter,” *Thesis of Oregon State University*, Jun. 2003.

[5.5] J. Kwong, Y. K. Ramadass, N. Verma and A. P. Chandrakasan, “A 65nm Sub-Vt Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter,” *IEEE J. Solid-State Circuits*, vol.44, pp.115-126, Jan. 2009.

[5.6] A.P. Chandrakasan, D. C. Daly, D. F. Finchelstein, J. Kwong, Y. K. Ramadass, M. E. Sinangil, V. Sze, N. Verma, "Technologies for Ultradynamic Voltage Scaling," in *Proceedings of the IEEE*, vol.98, no.2, pp.191-214, Feb. 2010.

[5.7] M. Anis, S. Areibi, M. Mahmoud, and M. Elmasry, “Dynamic and leakage power reduction in MTCMOS circuits using an automated efficient gate clustering technique,” in *39th Design Automation Conference*, 2002.

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PUBLICATIONS

Shi-Wen Chen, Ming-Hung Chang, Wei-Chih Hsieh, and Wei Hwang, "Fully On-Chip Temperature, Process, and Voltage Sensors" in *IEEE Int'l Symp. Circuits and Systems*, *ISCAS*, Jan. 2010. (Accepted)

PATENTS

1. Shi-Wen Chen, Ming-Hung Chang, Wei-Chih Hsieh, and Wei Hwang, "Fully On-Chip Temperature, Process, and Voltage Sensors" US/TW Patent Pending (pending)

2. Shi-Wen Chen, Shang-Yuan Lin Ming-Hung Chang, Wei-Chih Hsieh, and Wei Hwang, "Ultra-Low Voltage All-Digital Temperature Sensor With Adaptive Pulse Width Compensation" US/TW Patent Pending (submitted)

3. Shi-Wen Chen, Ming-Hung Chang, Wei-Chih Hsieh, and Wei Hwang, "MTCMOS Switched Capacitor DC-DC Converter with Delay Line Comparator" US/TW Patent Pending (submitted)