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電子工程學系　電子研究所碩士班

碩　士　論　文

低溫多晶矽製程之畫素記憶體電路暨數位類比轉換器電路設計與實現

Design and Realization of Pixel Memory Circuit and Two-Direction Cyclic D/A Converter in LTPS Technology

研 究 生：陳思翰　　(Szu-Han Chen)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一００年八月

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ABSTRACT (CHINESE)

近年來，有越來越多關於低溫複晶矽 (low temperature polycrystalline silicon, LTPS) 薄膜電晶體 (thin-film transistors, TFTs)的研究。這是因為這種技術已被廣泛地使用於可攜帶式系統產品中，例如數位相機、行動電話、筆記型電腦等。跟傳統的非晶矽 (amorphous silicon) 薄膜電晶體比起來，低溫複晶矽薄膜電晶體的電子遷移率約大了一百倍。這也是為什麼低溫複晶矽技術很適合用來將驅動電路整合於顯示器之周邊區域。藉由系統面板 (System-on-Panel, SOP) 之應用，可以實現輕薄、巧小且高解析度的顯示器。

由於綠能科技的興起，各式各樣的電子產品對於低功耗的需求越來越大，而這些新穎的電子產品常常伴隨著大量 LCD 面板的使用，因此出現了嵌入式畫素記憶體這樣的研究題目與方向，目的就是希望能夠降低 LCD 面板功率的消耗，進而使搭載這些 LCD 面板的電子產品能減少功率的耗損，以符合世界對於綠色產品日漸嚴格的標準。

此外，由於系統面板的發展，越來越多研究是將 LCD 面板的驅動電路(driving circuit)整合在面板上，而數位至類比轉換器在整個驅動電路中可以說是很重要的一環。其中循環式的數位至類比轉換器(cyclic DAC)比起其他的數位至類比轉換器，像是電阻式數位至類比轉換器(R-string DAC)、電流控制式數位至類比轉換器(current-steering DAC)等，擁有較小的功率消耗，也符合了前文所說對於低功

耗的需求。

在本篇論文之中，首次提出了設計於玻璃基板上之數位時間調變嵌入式畫素記憶體電路以及雙向循環式數位類比轉換器電路，其中畫素記憶體電路已經在三微米低溫複晶矽薄膜電晶體製程下成功被驗證。利用此畫素記憶體電路，可以將面板的平均功耗降低；而所提出的雙向循環式數位類比轉換器電路可以將八位元的數位訊號，經由開關電容(switch capacitor)的切換，轉換成對應的類比值，而比起傳統的電阻式數位至類比轉換器電路，擁有較小的面積，也就是意味著擁有較小的功耗。這兩種電路未來將可以被整合在面板上，帶來更便利性的應用。

Design and Realization of Pixel Memory Circuit and Two-Direction Cyclic D/A Converter in LTPS Technology

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ABSTRACT (ENGLISH)

In recent year, there are more and more researches on the low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs). That is because the wide use on the portable system such as digital camera, mobile phone, notebook and so on. Compared to the conventional amorphous silicon TFTs, the electron mobility of LTPS TFTs is about 100 times larger. That's why LTPS technology is suitable to integrate the driving circuits on peripheral area of display. By realizing the System-on-Panel (SOP) applications, slim, compact, and high-resolution display can be achieved.

The demand of low power has boosted for various electronic products because of the development of green technology. These fancy electronic products usually accompany large use of LCD panels. The research topics and directions of embedded pixel memory prompt in order to lower the power consumption of LCD panels. Further, to lower the power consumption of electronic products which contain these LCD panels in order to satisfy the world standard of green products.

Besides, the development of SOP urges more and more researches about the integration of driving circuit on the glass substrate. D/A converter (DAC) is an essential part for the whole driving circuit. Cyclic DAC has smaller power consumption than some other kind of DAC, like R-string DAC, current-steering DAC and so on.

In this thesis, a proposed on-panel digital time-modulation embedded pixel memory circuit and a two-direction cyclic DAC designed and implemented with the TFTs on glass substrate has been proposed in a 3-μm LTPS process. Also, the pixel memory circuit has been successfully verified. The average power consumption can be reduced with this pixel memory circuit. The propose two-direction cyclic DAC circuit can convert 8-bit digital signal into corresponding analog value with switching of the switch capacitor circuit. The cyclic DAC has smaller area rather than conventional cyclic DAC, which means lower power consumption. These two kinds of circuit can be integrated in the active matrix LCD (AMLCD) panels.

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Chapter 1

Introduction

1.1 Motivation

1.1.1 LCD Industry and LTPS Technology [1], [2]

The liquid-crystal display (LCD) industry has shown rapid growth in several market areas, such as notebook computers, monitors, mobile equipment, mobile telephones, TVs and so on. When it comes to high-speed communication networks, the emerging portable information tools are expected to grow in following on the rapid development of display technologies. Thus, the development of higher specification is demanded for LCD as an information display device. Moreover, the continual growth in network infrastructures will drive the demand for displays in mobile applications and flat panels for computer monitors and TVs. The specifications of these applications will require high-quality displays that are inexpensive, energy-efficient, lightweight, and thin.

Amorphous silicon (a-Si) thin-film transistors (TFTs) are widely used for flat-panel displays. However, this low field-effect mobility (ability to conduct current) property limits their application only as pixel switching devices; they cannot be used for complex circuits. However, the polycrystalline Si (poly-Si) TFTs from excimer laser annealing (ELA) process relatively exhibits higher electron and hole mobility functions than the conventional ones. The field-effect mobility of the poly-Si TFTs is about 100 times of the a-Si.

The high driving ability of poly-Si TFTs allows the integration of various circuits such as display drivers. For example, to date the function of the external ICs which is used for driving the pixel directly is integrated onto the peripheral of the glass

substrate. It leads to a lighter and thinner display and because this technology relaxes the limit in pitch between connection terminals, it's suitable for high resolution display. Moreover, high driving ability of poly-Si can provide larger aperture ratio because poly-Si TFTs can drive the same current as a-Si TFTs but only occupy small space.

There are two kind of process, including high-temperature and low-temperature poly-Si (HTPS and LTPS) TFTs. The process temperature for high-temperature poly-Si can be as high as 900°C so it needs more expensive quartz substrates, and the profitable substrate size is limited to around 6 inch (diagonal). And that size limit constraint to its applications. The process temperature for low-temperature poly-Si (LTPS) TFTs is less than 600°C, which would allow cheaper glass substrates. This makes possible direct-view large-area displays—for example, UXGA (ultra extended graphics array) monitors of up to 15.1 inch (diagonal) with a resolution of 1600 x 1200 pixels.

In addition, LTPS TFTs can be used to manufacture complementary metal oxide semiconductors (CMOSs) in the same way as in crystalline silicon metal oxide semiconductor field-effect transistors (MOSFETs). Figure 1.1 shows the cross sectional structure of a LTPS TFT CMOS. That allows the circuit design in LTPS process.

LTPS TFT performance is extremely improved in recent year because of the technology like ELA, ion doping and oxide formation. For those reasons above, LTPS technology has been applied successfully to not only small-sized displays, but also medium- and large-screen products. It is the base for high performance TFTs for active matrix liquid crystal displays.

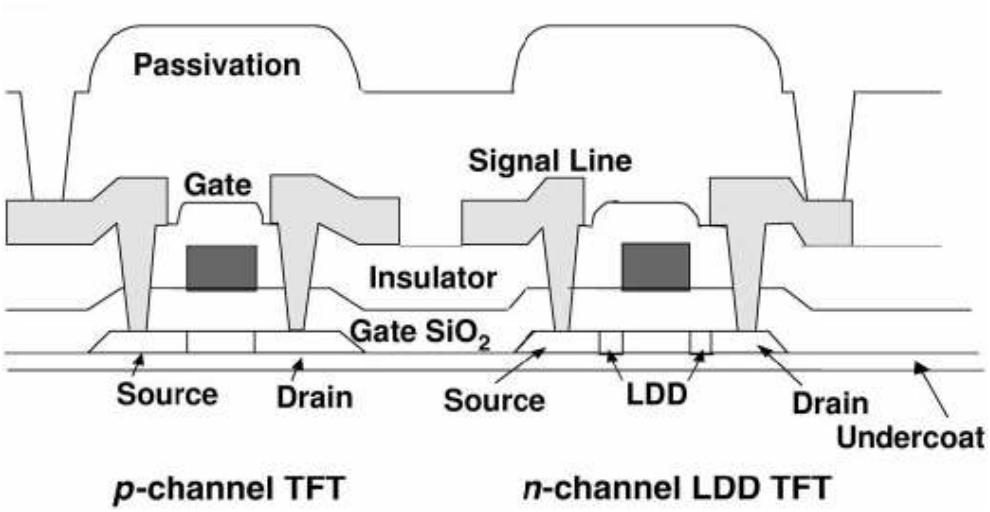


Figure 1.1 Schematic cross-section view of the structure of a LTPS complementary metal oxide semiconductor (CMOS). (LDD: lightly doped drain)

1.1.2 The Advantages of the System-on-Panel LTPS TFT-LCD Displays [3], [4], [5]

In recently, there are more and more practical uses for LTPS TFT technology of forming a part of display circuits on the glass substrate. It has many merits for display such as compact, high reliable, high resolution and so on. Because of this property, LTPS TFT-LCD technology is widely used for mobile displays. Figure 1.2 shows the system integration roadmap of LTPS TFT-LCD [3], [4], [5].

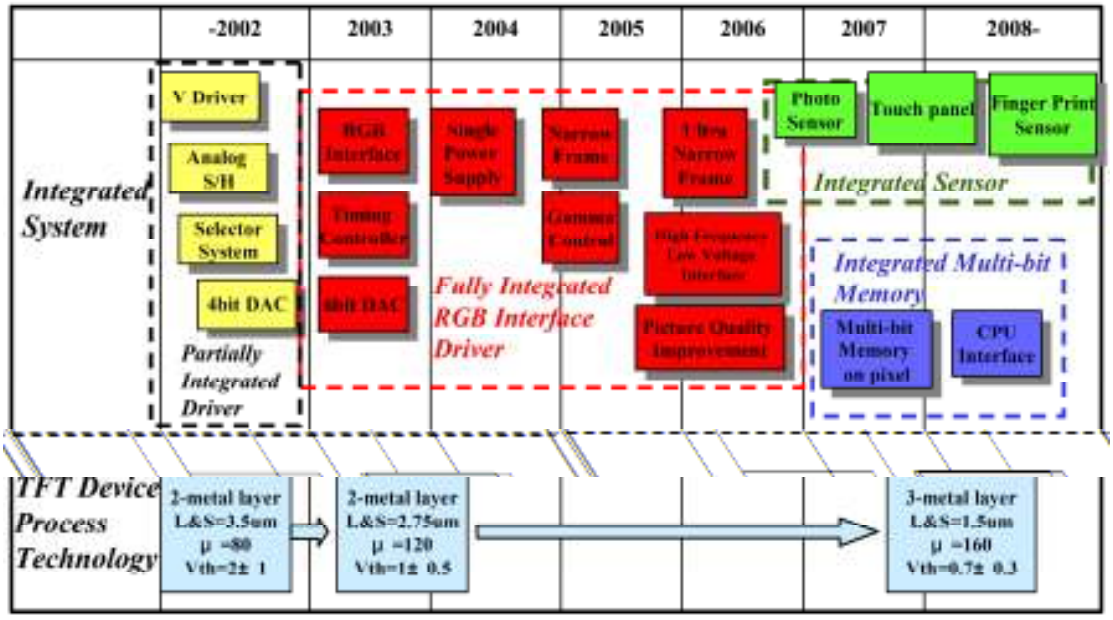


Figure 1.2 System integration roadmap of LTPS TFT-LCD.

The main advantage of the LTPS TFT-LCD is the elimination of TAB-ICs (tape-automated bonding integrated circuits). For a-Si TFT-LCDs, TAB-ICs are connected to the left and bottom side as the Y driver and the X driver, respectively. However, integration of the Y and X drivers with LTPS TFTs requires PCB (printed circuit board) connections on the bottom of the panel only. The PCB connection pads in LTPS TFTs have size reduction than TAB-ICs connection in a-Si TFT-LCDs. In addition, the most common failure mechanism of TFT-LCDs is the disconnection of the TAB-ICs. By using LTPS TFTs, this kind of effects can be therefore decreased significantly. For this reason, the reliability and yield of the manufacturing can be improved. Also, because the TAB-IC pitch (spacing between connection pads) limits display resolution to 130 ppi (pixels per inch), decreasing the number of TAB-IC connections by using LTPS TFTs can achieve a high-resolution display. A higher resolution of up to 200 ppi can be achieved by LTPS TFT-LCDs. Therefore, the SOP technology can effectively relax the limit on the pitch between connection terminals to be suitable for high-resolution display. Furthermore, because three sides of the display are now available without TAB-ICs [1], LTPS technology allows more flexibility in the design of the display system. Figure 1.3 shows a comparison of a-Si and LTPS TFT-LCD modules. The 3.8” SOP LTPS TFT-LCD panel has been manufactured successfully and it is shown in Figure 1.4.

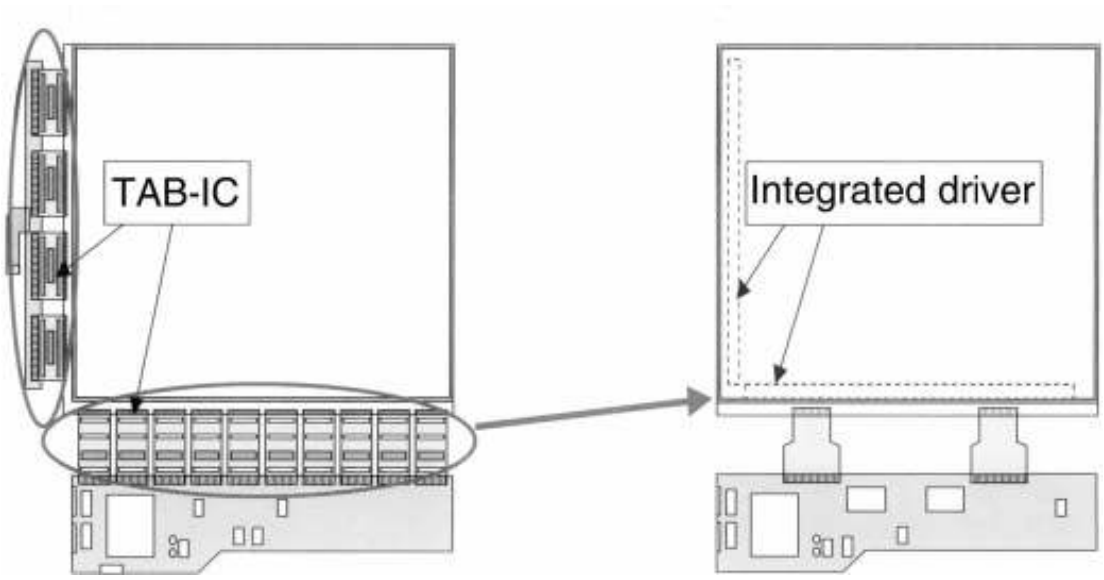


Figure 1.3 Comparison of (a) an amorphous silicon TFT-LCD module and (b) a low-temperature polycrystalline silicon TFT-LCD module.

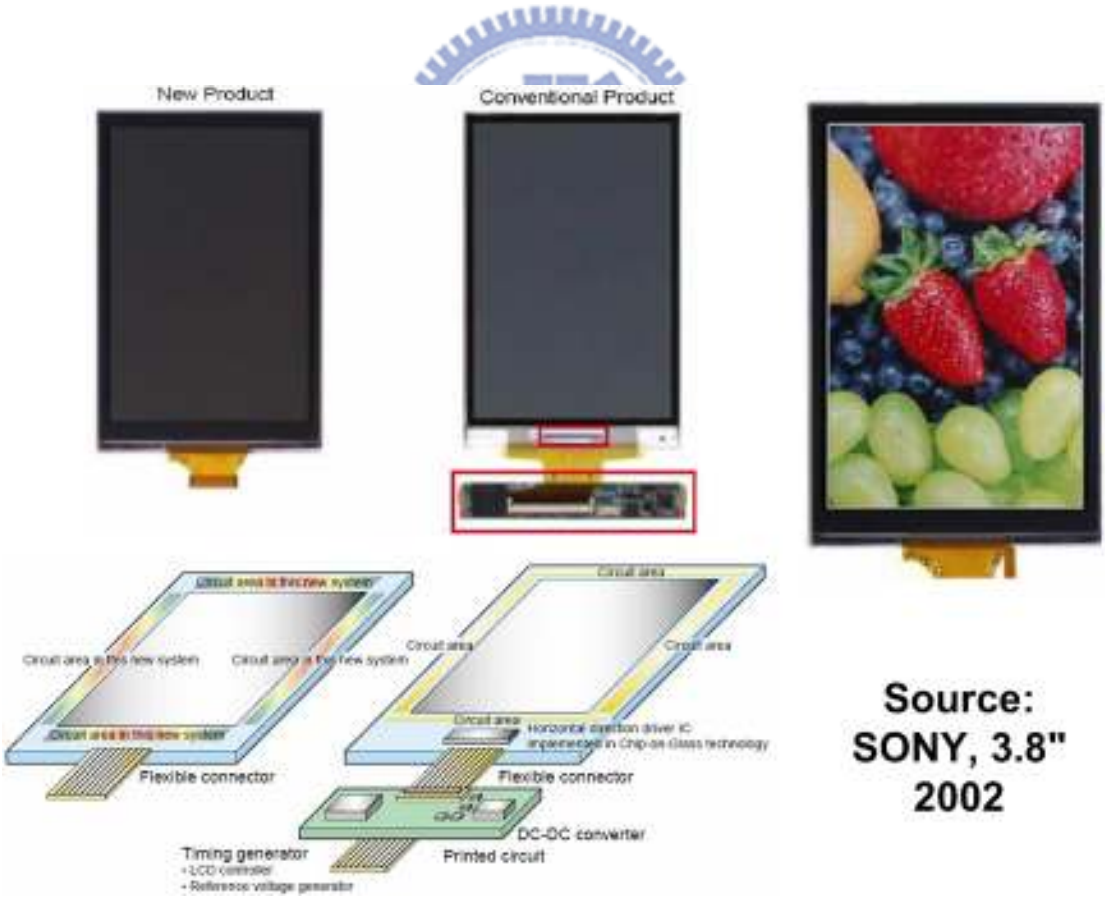


Figure 1.4 The comparison of new SOP technology product and conventional product. The new 3.8” SOP LTPS TFT-LCD panel has been manufactured by SONY corp. in

2002.

Figure 1.5 shows there are three kinds of peripheral circuits of the array panel including signal processor, display driver, and gate driver. The signal processor can capture and process the photo sensor signals, and then convert them to a suitable form for display. The converted signals are sent to the display driver and the captured images can be displayed. Last, the gate driver controls both the pixel TFT and the sensor circuit. Application to color image capturing has been realized by successively capturing through red, green, and blue (RGB) color filter, and then synthesizing their captured image.

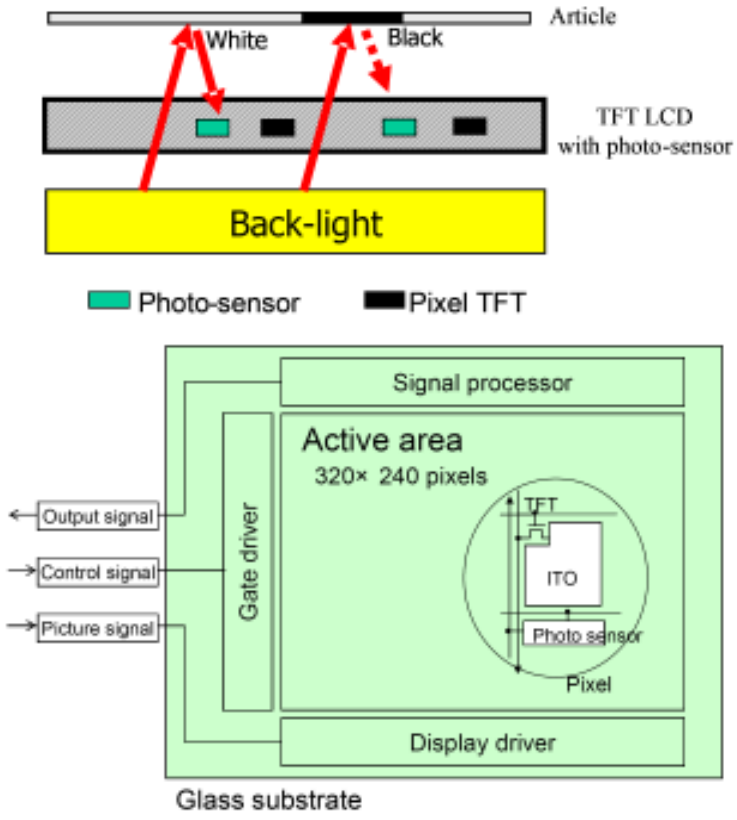
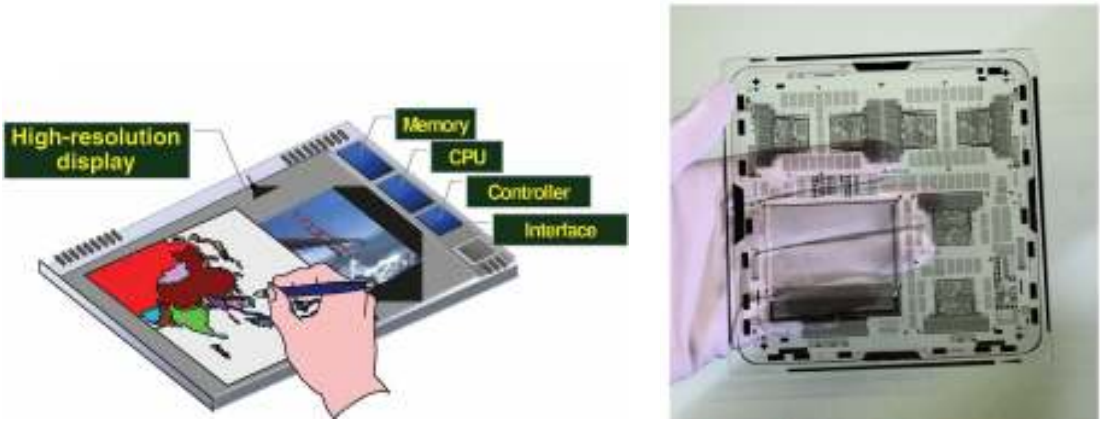


Figure 1.5 The principle and structure of the photo-sensing display.

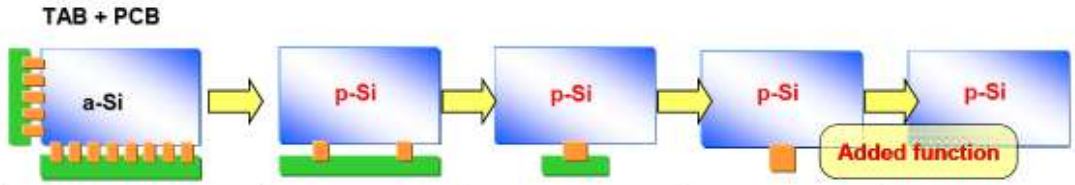
In the end, it may be possible to integrate the keyboard, CPU, memory, and display into a single “sheet computer”. The schematic illustration of the “sheet computer” concept and a CPU with an instruction set of 1-4 bytes and an 8-bit data bus on glass substrate are shown in Figure 1.6, respectively. Figure 1.7 shows the

roadmap of LTPS technologies leading toward the realization of sheet computers. Finally, all of the necessary function will be integrated in LTPS TFT-LCD.



(a) (b)

Figure 1.6 (a) The "sheet computer" concept and (b) a CPU with an instruction set of 1-4 bytes and an 8-bit data bus on glass substrate.



Year	'98~ 01	'02~ 04	'05~ 07	'08~
Generation	1st Gen .	2nd Gen .	3rd Gen.	4 th Gen.
Mobility(cm2/Vs)	100	150		300~500
Integrated function	LCD Driver	D/A converter Pixel memory	DC/DC Converter Digital I/F Photo-sensor	DSP/CPU Frame memory
Key technology Design rule	ELA, I/D 4-5μ m	Flat-ELA C/H Dry 3μ m	Fine lithography S tepline Dry 1.5μ m	Crystallization Planarization <1μ m

Figure 1.7 The roadmap of LTPS technologies leading to sheet computers.

1.1.3 Low Power Issue in LCDs [7]

The market for mobile SOP LCDs, including poly-Si TFT LCDs whose circuit integration levels are relatively low, has been rapidly expanding because SOP-LCDs have advantages of high resolution, narrow picture frames, low power consumption, and highly reliable electrical terminal connections. For example, 2.2- to 2.4-inch QVGA-format ones began to be used in mobile-phone terminals. Figure 1.8 shows the

trends in mobile SOP-LCDs [7]. As the circuit-integration level progressed, the driving voltage and design rule should be decreased for low-power consumption and a narrow picture frame. However, the power consumption of SOP driver circuit tends to be higher than that of silicon ICs because poly-Si TFTs have higher threshold voltages and lower mobility, and are fabricated with a larger design rule. This tendency increases as circuit integration progresses. Therefore, power reduction in SOP driver circuit is one of the major challenges to expand the SOP-LCD market further.

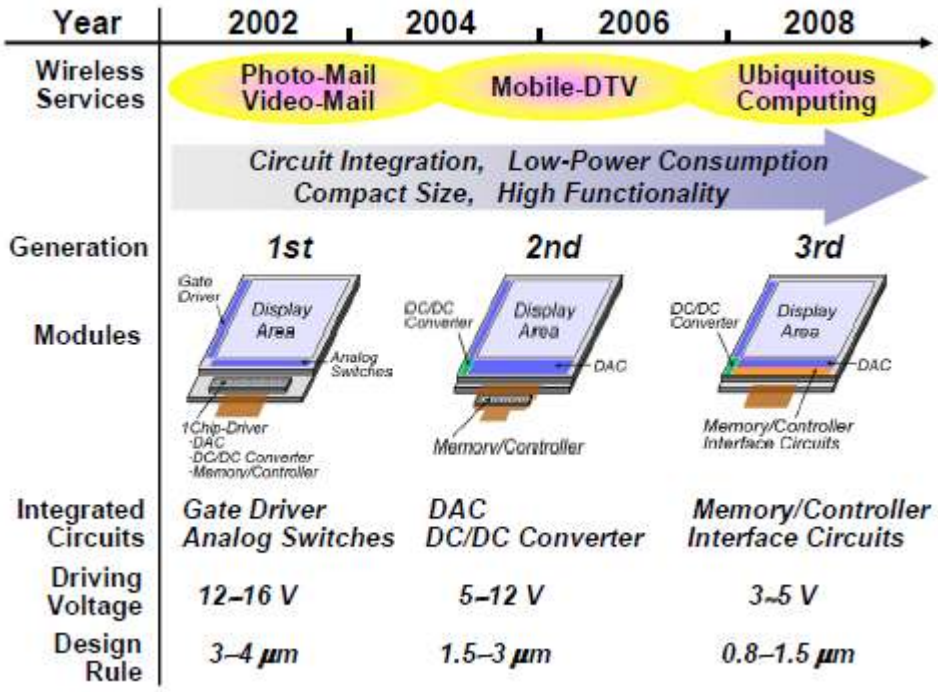


Figure 1.8 Trends in mobile SOP LCDs.

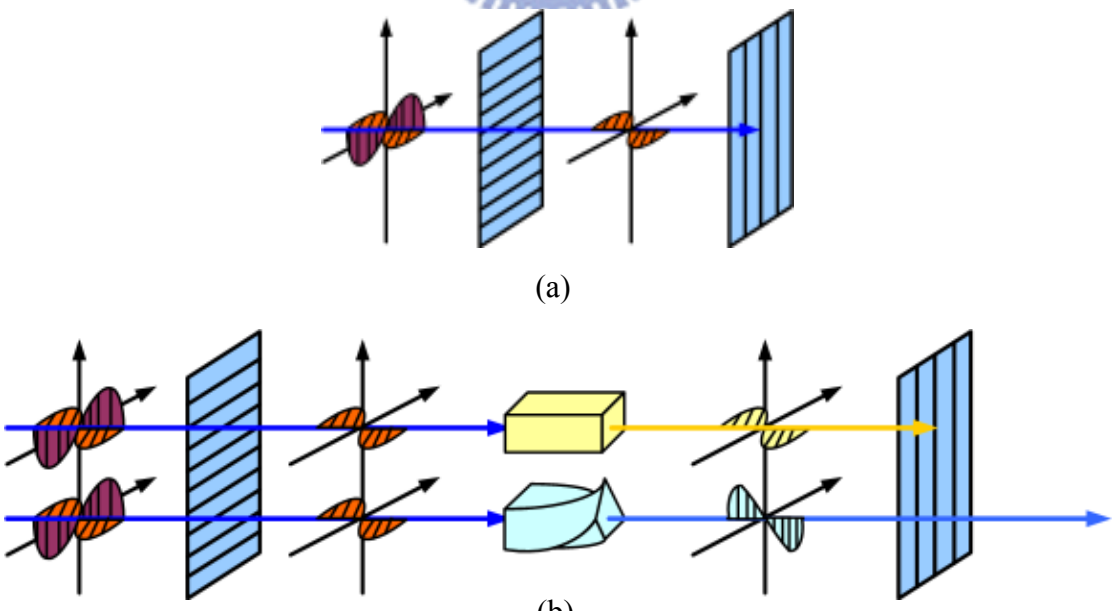
1.1.4 Summary

LTPS technology has many advantages such as high resolution, large size, low-cost, higher mobility than a-Si process. This technology is thus suitable for SOP-LCD applications. With SOP-LCD, it may be possible to integrate the keyboard, CPU, memory, and display into a single “sheet computer”. However, power issue is an important issue in SOP-LCD applications. Therefore, power reduction in SOP driver circuit has become one of the major challenges and research topics.

1.2 Background Knowledge of Thin-Film Transistors Liquid Crystal Displays

1.2.1 Brief Introduction of Liquid Crystal Displays [8], [9]

There are many kinds of liquid crystal. The twist of liquid crystals can be controlled by the electric field that is applied across it, liquid crystals are used as a switch that passes or blocks the light. The polarizer can block or pass the specific light by changing the phase of the polarizer. There are two polarizers including the first polarizer called *polarizer* and the second polarizer called *analyzer*. If the couple of polarizers have 90° phase error, the light can be blocked which is shown in Figure 1. (a). But if we twist the liquid crystal molecule by applying the specific electric field across it, the light still can pass the polarizer. This is because the direction of liquid crystal molecules varies with electric field and it can guide the light along the long axis, shown in Figure 1. (b).



(a)

(b)

Figure 1.9 (a) A couple of polarizers with 90° phase error. (b) A couple of polarizers with liquid crystals.

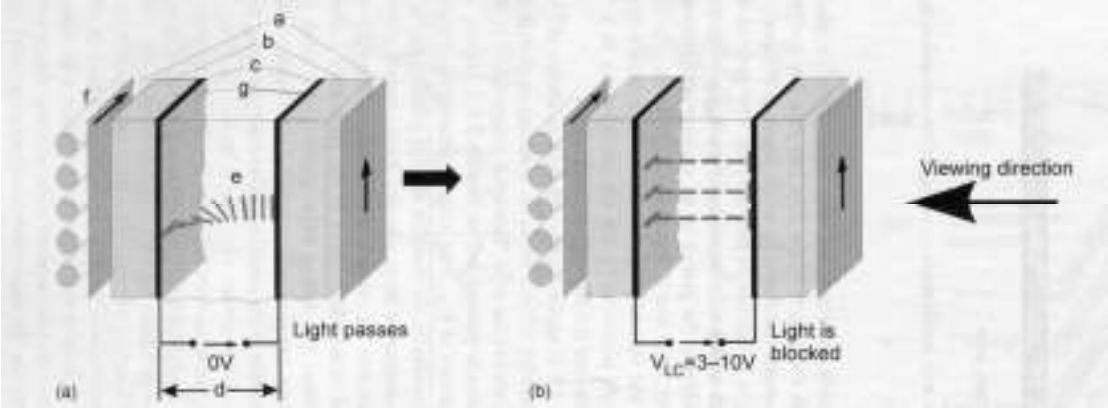


Figure 1.10 The structure of a TN-LCD (a) while light is passing, and (b) while light is blocked. a: polarizer; b: glass substrate; c: transparent electrode; g: orientation layer; e: liquid crystal; f: illumination.

In Figure 1.1 (a), it shows a pixel of a transmissive twisted nematic LC-cell without voltage applied. The white backlight *f* passes the polarizer *a*. The light leaves it linearly polarized in the direction of the lines in the polarizer. In this case, the analyzer is crossed with polarizer. The light can pass the analyzer without applied voltage and the pixel appears white. This operation is called the *normally white* (NW) *mode*.

If a voltage V_{LC} of the order of 10 V is applied across the cell, as shown in Figure 1.1 (b), all molecules aligned parallel to the electric field. In this situation, the wave is polarized in the same direction as at the input. Therefore, the analyzer blocks the light and the pixel appears black. This is called the *normally black* (NB) *mode*.

1.2.2 Liquid Crystal Display Module Structure

The cross section structure of TFT-LCD panel is shown in Figure 1.11. There are two parts of liquid crystal filled in the center of LCD panel including TFT array substrate and color filter substrate. A backlight module contains an illuminator and a light guilder because liquid crystal molecule cannot light by itself. Usually this part

consumes the most power of the system. There are a polarizer, a glass substrate, a transparent electrode and an orientation layer in TFT array substrate. In color filter substrate, it is composed of an orientation layer, a transparent electrode, color filters, a glass substrate and a polarizer. Transparent electrodes can control the directions of liquid crystal molecules in each pixel by voltage supplied from TFT on the glass substrate. Color filters contain three original colors, red, green, and blue (RGB). The degree of light called “gray level” can be well controlled in each pixel covered by color filer to get more than million kinds of colors.

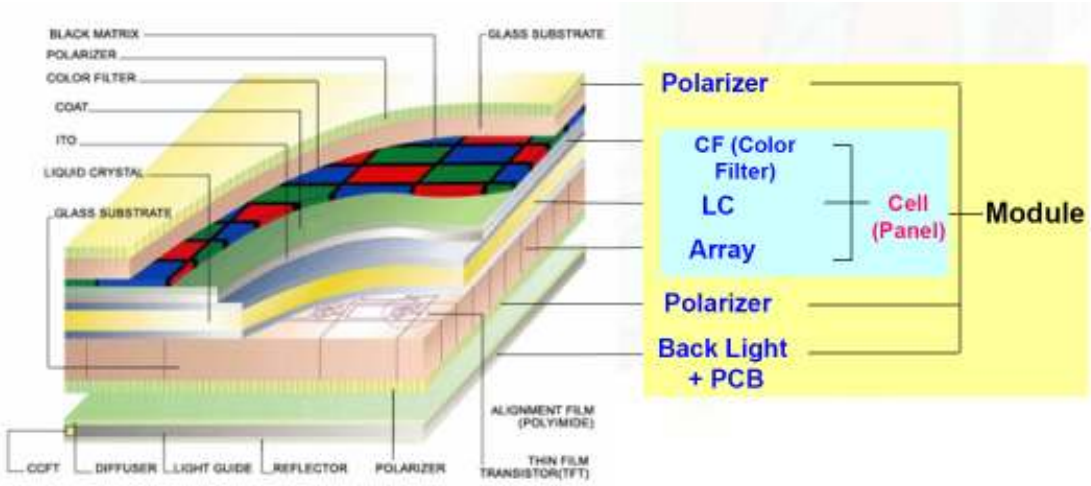


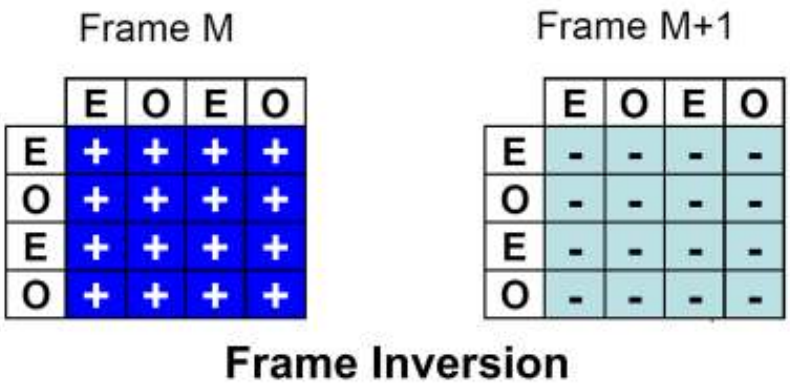
Figure 1.11 The cross section structure of TFT-LCD panel.

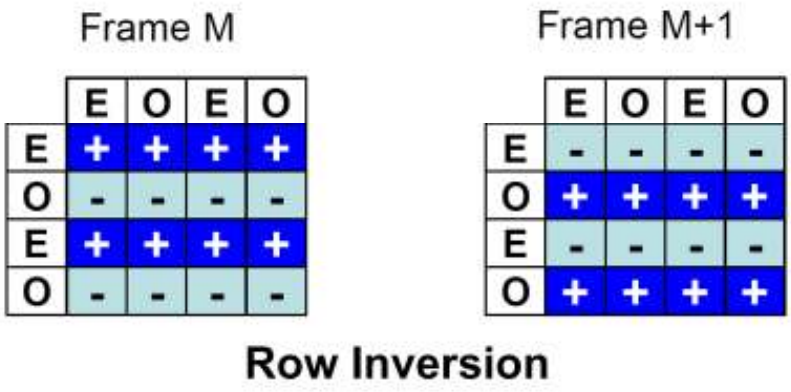
1.2.3 Driving Method [10]

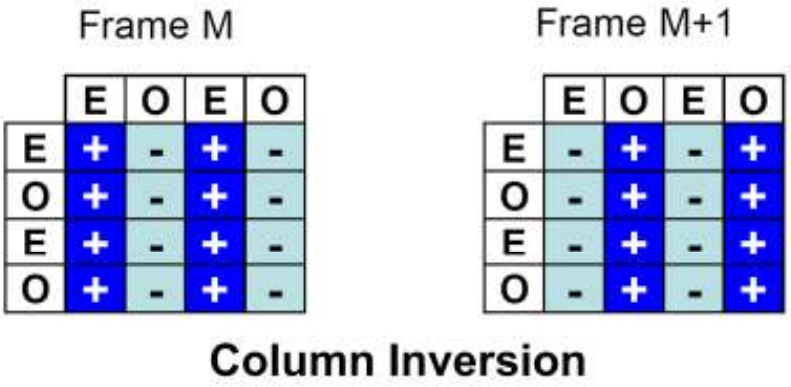
Liquid crystal molecules need to do inversion because the DC blocking effect and the DC residue (stick image) will be appeared under a fixed voltage in the long period. Therefore, the electric field polarity should be inversed every period to avoid the destruction of liquid crystals. The torque caused by electric filed is related to the magnitude of electric filed instead of the polarity of electric filed. Therefore, the polarity of electric filed would not affect the twisting of the liquid crystal molecules. If

the electric field across liquid crystals is changed into two polarities (positive and negative) with the same magnitude alternately, the frame picture can still be kept on the same gray level. If electric field is higher than common mode voltage the polarity is called positive polarity, otherwise it is called negative polarity. By this way, the liquid crystal molecules can avoid defection under the applied voltage with same magnitude. From the description above, the polarity inversions of LCD panel can be divided into four general types: frame inversion, row inversion, column inversion, and dot inversion which are shown in Figure 1.4 [10]. Dot inversion is the major driving method of LCD panel because by this method, we can achieve to higher quality image due to the reduction in both horizontal and vertical cross-talk. The flicker of image also can be reduced due to the spatial averaging of pixels. But the price of this method is an increase of the power consumption due to the line inversion component. This method is also incompatible with common voltage modulation.

Based on the operational type of common mode voltage, the driving method can also be classified into DC modulation driving and AC modulation driving which are shown in Figure 1.13. DC modulation driving method would keep its common voltage on a constant level. However, the common mode voltage of AC modulation driving method is not a constant level, is a period voltage. DC modulation driving method can eliminate the crosstalk and flicker; however, this driving method will cause more power consumption. AC modulation driving method can lower the power dissipation in data driver, but only frame and row inversion are available for this driving method.







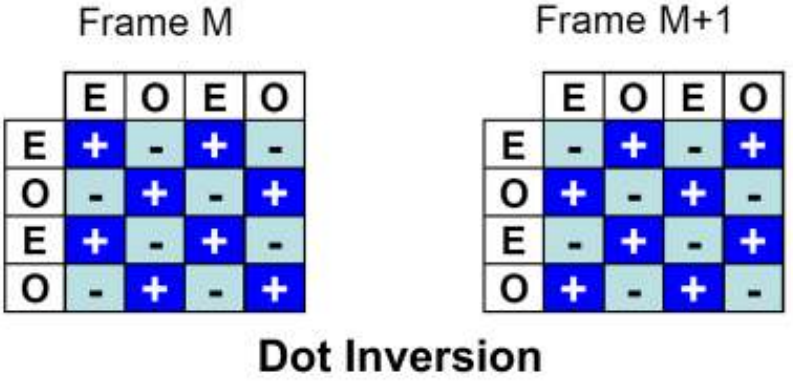
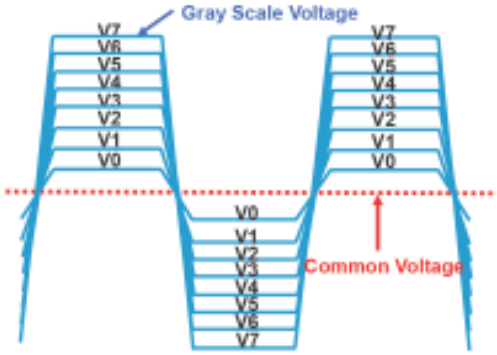
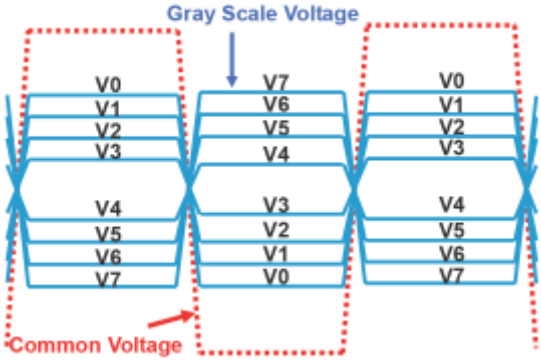


Figure 1.4 The polarity inversions of TFT-LCD panel.



(a)



(b)

Figure 1.5 (a) The operation waveform of DC modulation driving method and (b) the operation waveform of AC modulation driving method.

1.3 Thesis Organization

The fundamentals and realization of the time-modulation pixel memory are discussed in chapter 2. Then, the concept and simulation results of the two-direction cyclic DAC are discussed in chapter 3. In the last chapter, the conclusions of this thesis and the future work are stated.

Chapter 2

Fundamentals and Realization of Time-modulation Pixel Memory

2.1 Introduction

2.1.1 Embedded Pixel Memory

The LCD frame can be separated into normal mode and still mode. The normal mode is that the frame of LCD is changing continuously. The still mode means that the frame of the LCD is static. However, conventional LCD driver produces data and sends it into pixel through data line even these data are all the same because it is a static frame. The concept of the embedded pixel memory is that the LCD is driven by only the pixel circuit when displaying a still image. This means that no charging current to the data line, which has a large load capacitance, is required. And only a small charging current to the pixel capacitor is necessary. This results in an ultra-low-power operation. Figure 2.1 shows the basic concept of pixel memory technology [3].

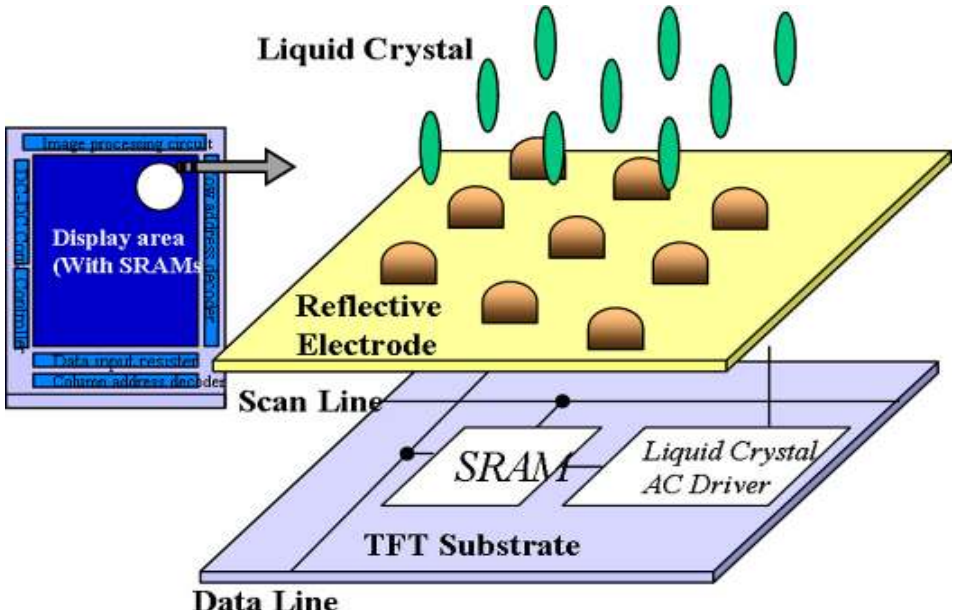


Figure 2.6 Basic concept of pixel memory technology.

Figure 2.2 shows the power consumption trend of an LCD driver with various resolutions [3]. With this pixel memory technology with reflective color LCD technology, a very attractive display having an ultra-low-power characteristic as well as high image quality can be realized. Also, it has low-cost property because the frame memory is integrated in the display. The total power consumption of an LCD module is actually dominated by the lighting system such as a frontlight and a backlight. Therefore this pixel memory technology should be applied to a reflective LCD or a transflective LCD. In a reflective LCD, the pixel memory circuit can be effectively integrated under the reflective pixel electrode without any optical loss. The power consumption remains very low in most case. However, the LCD requires a frontlight system when it is used in a very low ambient light environment, which results not only in a high consumption of power but also degrades the image quality even in a normal environment. In a transflective LCD, the above problem relating to the image quality can be solved. A backlight system can be used instead of a frontlight for very low ambient light conditions. Also, it can have two different operating modes in normal ambient light conditions; an ultra low power mode which is operated by the pixel memory circuit without a backlight, and a high picture quality mode which is operated by the pixel memory or conventional driver circuit with the backlight turned on. The drawback is that the transmissive aperture area is limited to some level, according to the display specifications and the process technology.

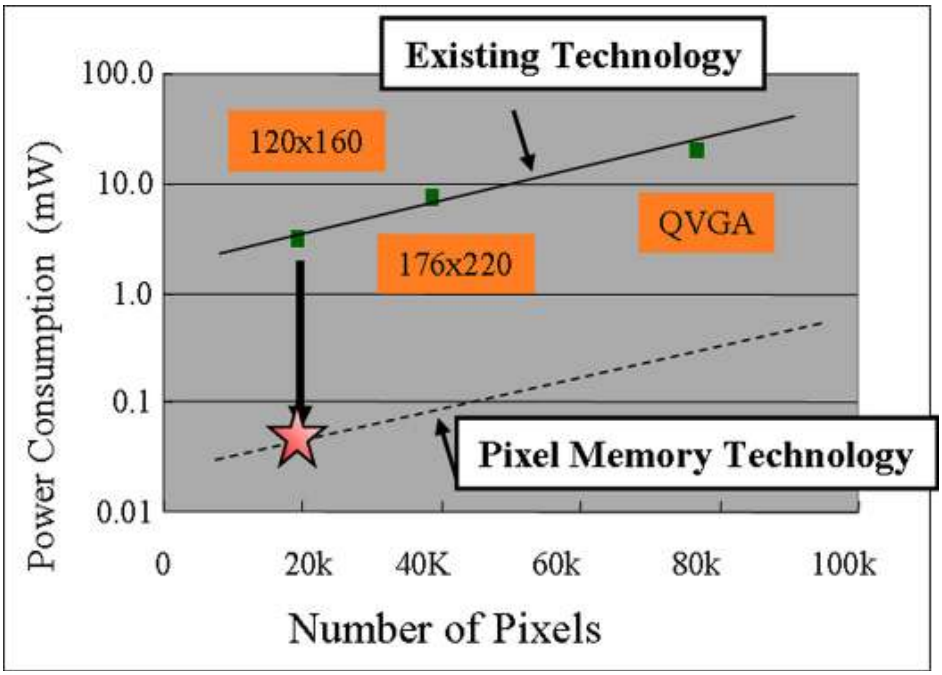


Figure 2.2 Power consumption trend of an LCD driver.

2.1.2 Fundamentals of the 1-bit Digital Pixel Memory [11], [12], [13]

Recently, several researches were introduced to reduce the power consumption of the low-temperature polycrystalline silicon (LTPS) TFT LCDs for small size and portable electronic equipments. These are focused on the reducing the driving frequency of LCD panel for low power consumption in the still image. Since the embedded memory circuits using LTPS TFTs in the pixel can display the still image without driving the data line from the data driver. There are two memory types to memorize the video data for display the still image in the pixel. One is using a dynamic memory. And the other is using a static memory circuit as shown in Figure 2.3, its pixel consist of pixel switch, one latch contain the digital data to express still image, and two switched to select binary data of latch. Since each pixel have either black or white, this panel was able to display 1-bit RGB(8 color) image in still mode. Figure 2.4 shows the operation of this pixel from normal mode to still mode. At normal mode, Cont1 and Cont2 are low to cut the electrical path between pixel electrode and latch (SRAM1) and this pixel is driven as conventional pixel. In pre-still

mode, all latches in the panel ate programmed and memorized their own data. Then, in still mode, data driver and gate driver are turned off and pixel is driven by contained data in latch. Cont1, Cont2 and common electrode signals are alternated to reverse the voltage polarity applied at LC in every frame time. Therefore, driver circuits on the glass substrate and the controller IC consume almost nothing and its panel only consumes little power to drive control signals (Cont1 and Cont2) and power caused by leakage current in the latch in the still mode.

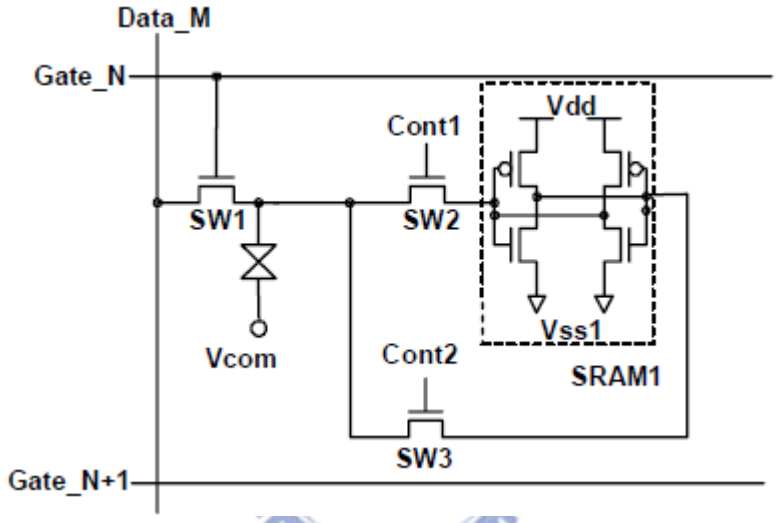


Figure 2.3 Schematic diagram of static memory embedded pixel.

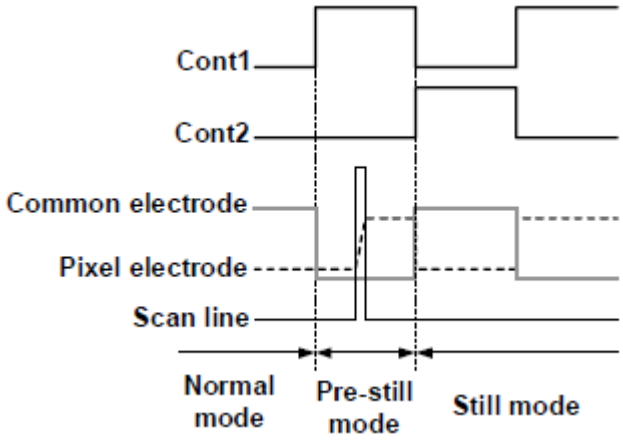


Figure 2.4 Timing chart from normal mode to still mode.

2.1.3 Fundamentals of the Digital Area-modulation Pixel Memory [14], [15]

The basic concept of the area-modulation is that dividing one pixel into binary

weighted area and controlling each divided area to be black or white. With dividing the pixel into six parts, this panel was able to display 6-bit RGB(64 color) image in still mode. Figure 2.5 shows the schematic diagram of this 6-bit area-modulation pixel memory [15]. This pixel memory circuit contains one latch, a 6-bit DRAM and two TFTs as controlling transistors.

Figure 2.6 shows the time diagram of the control signals. At normal mode, POLA and POLB are low to cut the electrical path between pixel electrode and latch (SRAM1) and this pixel is driven as conventional pixel. In pre-still mode, all latch in the panel ate programmed and memorized their own data. S0~S5 turns on in turns to store the corresponding digital data into the DRAM. Then, in still mode, data driver and gate driver are turned off and pixel is driven by contained data in latch. S0~S5, POLA, POLB and common electrode signals are alternated to reverse the voltage polarity applied at LC in every frame time. Therefore, driver circuits on the glass substrate and the controller IC consume almost nothing and its panel only consumes little power in the still mode.

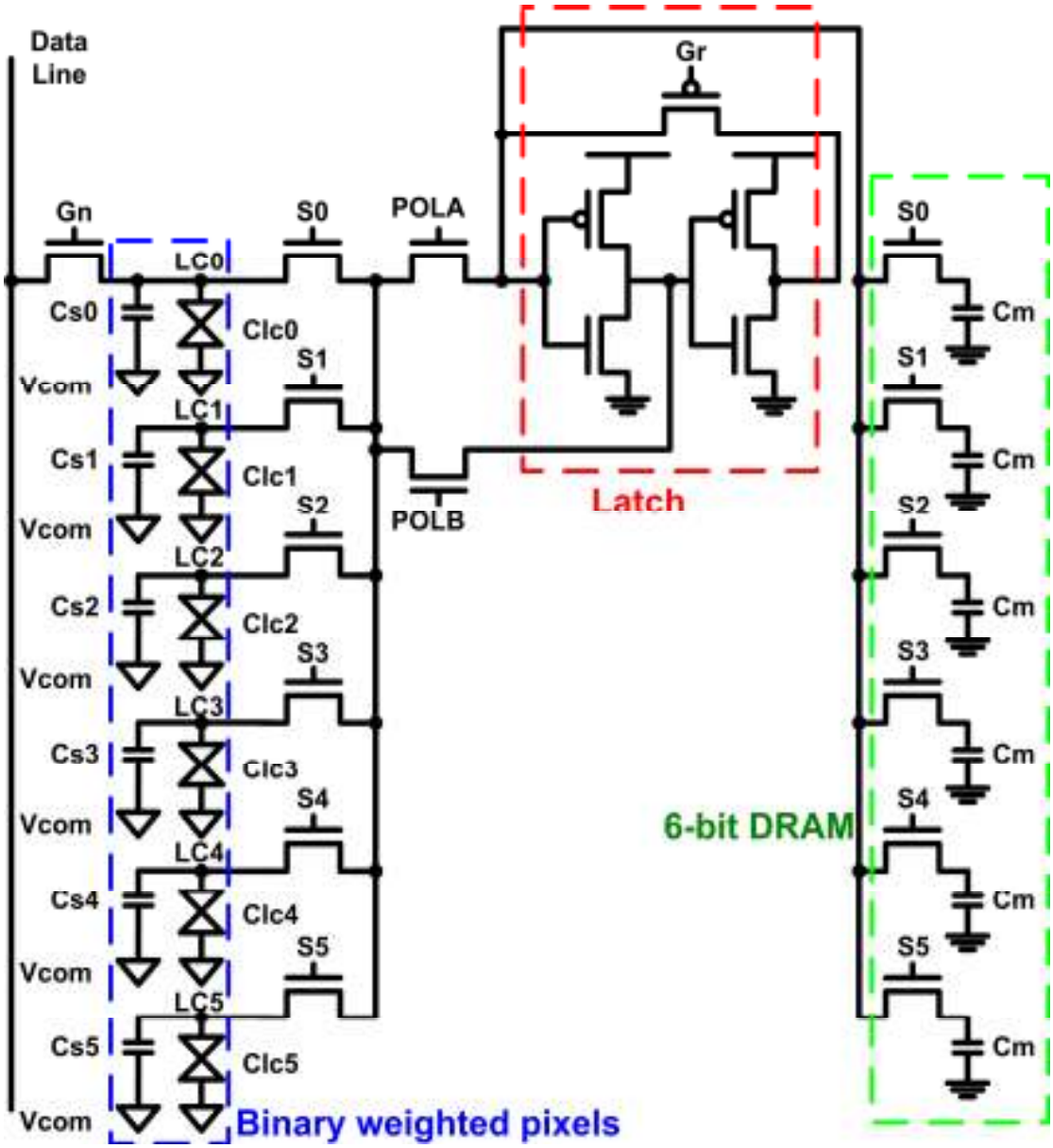


Figure 2.5 Schematic diagram of area-modulation pixel memory.

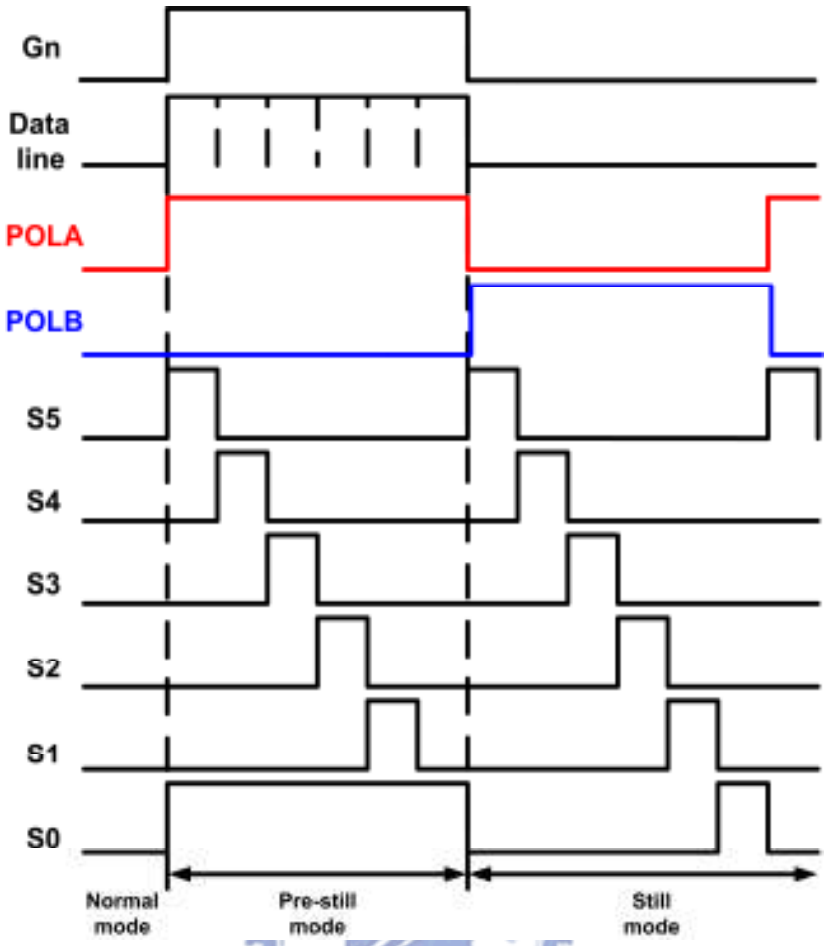


Figure 2.6 Time diagram of the control signals.

2.2 Circuits Implementation on Glass Substrate

2.2.1 Concept of Time-modulation [16]

This section explains basic concept of the time-modulation way for the embedded digital pixel memory. Figure 2.7 illustrates the main idea that how the time-modulation is used to build up the memory circuit. Except for the area-modulation that mentioned on 2.1.3 can produce different gray levels by dividing one pixel into several areas which is binary weighted and control each area to brighten or not, the time-modulation is another way to produce gray levels. When the high voltage is given to the pixel electrode for different time width in a constant time interval, it can be observed that different time width that the pixel electrode is given to high voltage, the different gray level that the pixel will show.

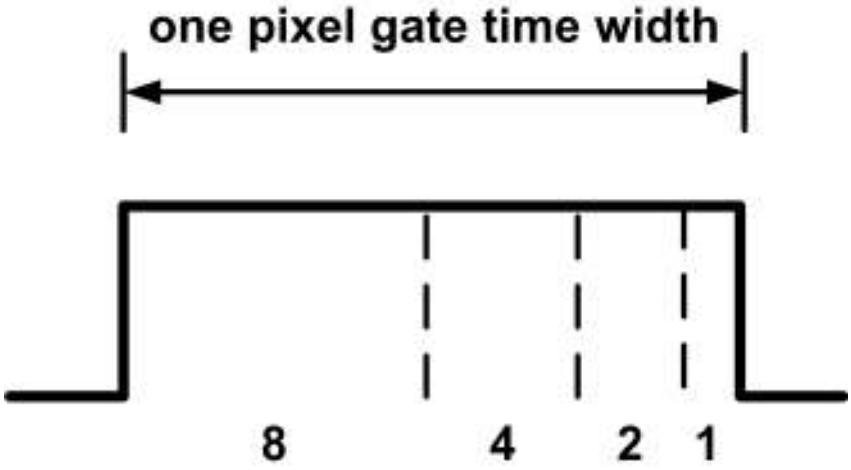


Figure 2.7 Concept of time-modulation.

Based on this concept, the gate time width that is opened for one pixel to read the data for data line is designed to be divided into binary weighted, 8:4:2:1, for 4-bit. By controlling each time interval voltage high or not, the different gray levels can be mixed. In this work, we design the pixel memory based on 2.8" QVGA TN LCD. The frame time of this LCD is 16.7ms, so the gate line time width is 16.7ms/320 = 52μs.

2.2.2 Design of 4-bit Digital Time-modulation Pixel Memory

This section presents the design of the 4-bit time-modulation pixel memory circuit which is embedded for each pixel. Figure 2.8 shows the schematic diagram of the pixel memory which contains a latch, a 4-bit DRAM and two switches, M2, M3, deciding whether to do inversion or not. This design is similar to the area-modulation design; however, this design does not have to divide the pixel into several parts which can decrease the aperture for the LCD panel. Figure 2.9 shows the control signal with time-modulation for this design. In pre-still mode, the control signals (i.e. S0~S3) turn on the switches of DRAM (i.e. M8~M11) in turns to store the corresponding digital value for each time interval into the 4-bit DRAM with M2 on and M3 off. Then, at the next cycle, the pixel goes into the still mode which means M1 is off and the pixel memory circuit has to produce the time-modulation digital signal for the Lc node

without providing data from driving circuit.

In still mode, when inversion is needed, M3 will turn off and M2 will turn on. In that case, the digital data stored in DRAM will produce an inverting digital data through one inverter (i.e. M4 and M5) at node Lc. And because control signals (S0~S3) can turn on the switches of DRAM for corresponding time width (i.e. 8:4:2:1) due to the concept of time-modulation technique, the inverting data will be produced at Lc node for corresponding time width. The latch can lock up the digital value in case the value stored in DRAM might be changed when the switch of DRAM is turned on. This design is based on AC modulation driving method. When doing the inversion, Vcom will be 5V; otherwise, it will be 0V.

With M2, M3 turns on alternatively, the pixel memory circuit can do normal operation and inversion without reading the data from driving circuit. The size of these switches is shown in Table 2.1. For a smaller area, it's better to design the size of switch as small as possible, but in this design, the switch size of DRAM (i.e. M8~M11) is designed larger (m=5) to make sure the switch has smaller resistance while reading or writing digital data from DRAM.

Name	Type	Size	Fin (m)
M1	nTFT	3μm/3 μm	1
M2	nTFT	3μm/3 μm	1
M3	nTFT	3μm/3 μm	1
M8~M11	nTFT	3μm/3 μm	5
Cm	Cap	0.6pF	

Table 2.1: Transistor dimensions of the switches used in the pixel memory circuit.

The capacitance value of DRAM is also important in this design. When there is a

digital value change, there might be the charge redistribution between Cm and Clc. For example, there is a digital value “1” at node Lc and the value should be changed to “0” in the next cycle because the second capacitance of DRAM stores the digital value “0” as shown in Figure 2.10. The charge on the Cm and Clc will redistribute and if the value of Cm is too small, the latch might lock up with wrong digital value and the digital value stored in DRAM might be changed. In addition, lager capacitance can diminish the effect from clock feed-through. When the control signals (S0~S3) swing, there might be some voltage coupling on capacitance of DRAM. If the capacitance value of DRAM is large enough, the voltage coupling from clock can be ignored. For the reasons above, the larger capacitance of DRAM can prevent data changed from charge redistribution and clock feed-through; however, larger capacitance also brings smaller aperture for the pixel and that will be a trade off whiling designing the value of capacitance. From simulation, it can be found that the value of DRAM capacitance must be larger than 0.5pF, or this pixel memory circuit will not work in still mode. To take Cm=0.3pF as an example, it can be observed that the digital value is wrong in still mode as shown in Figure 2.11. That is because the digital data stored in DRAM are changed due to the charge redistribution with too small Cm. So in this design, Cm is designed to be 0.6 pF to make sure there is no effect from charge redistribution and make the area of the pixel memory circuit as small as possible.

A test pattern and its simulation timing chart are shown in Figure 2.12. The test pattern is given as “l010” for 4 bits. The Lc node is shown as “0101” when M3 is on which means the inversion has been done successfully. By such simulation, this circuit is successfully verified. In the pixel memory design, the data stored by digital memory is more reliable than analog memory. And proposed time-modulation memory has a smaller area than area-modulation pixel memory.

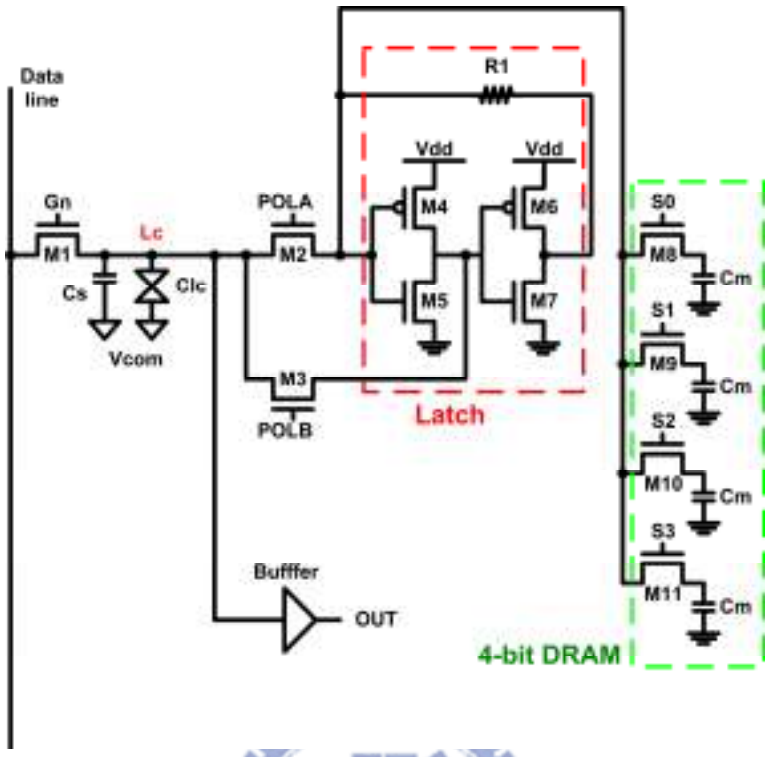


Figure 2.8 Schematic diagram of time-modulation pixel memory.

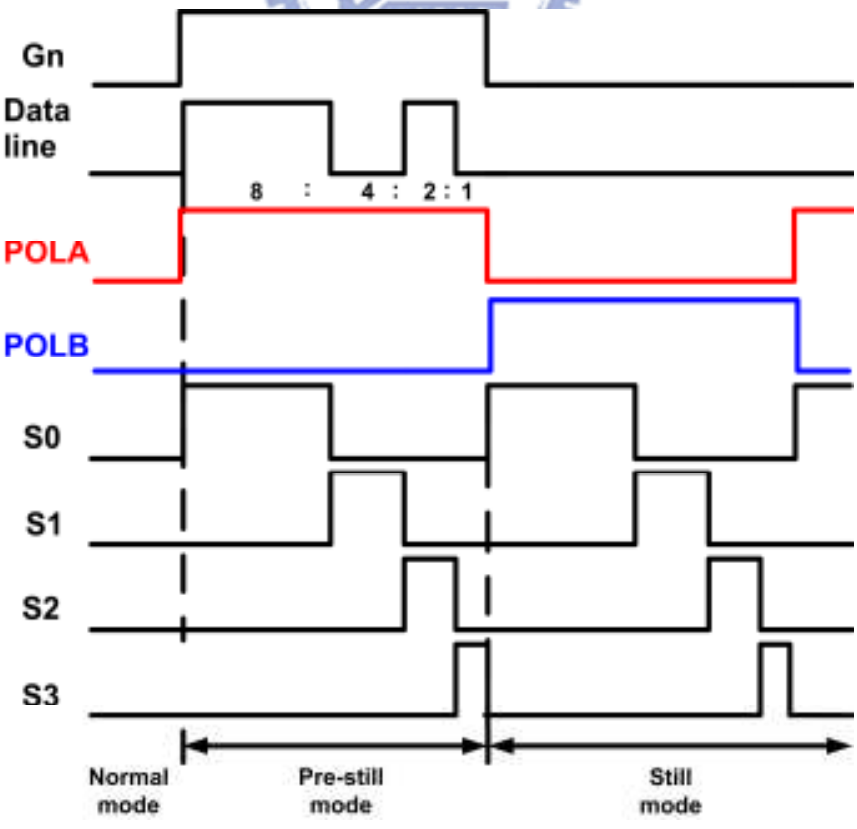
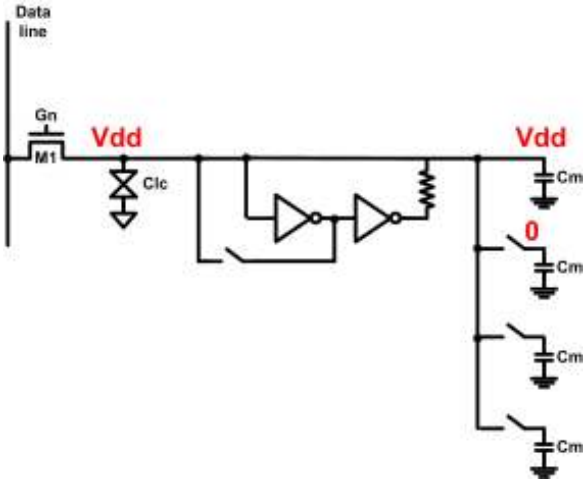
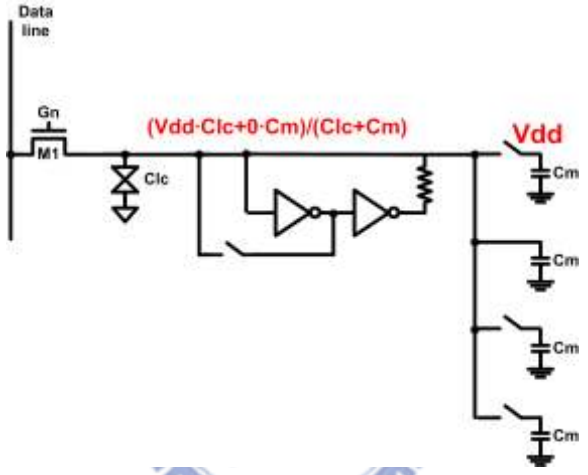


Figure 2.9 Time diagram of the control signals.



(a)



(b)

Figure 2.10 (a)S0 turns on with the digital data “1” for the first cycle in still mode and (b) S1 turns on with the digital data “0” for the second cycle in still mode and there is a charge redistribution.

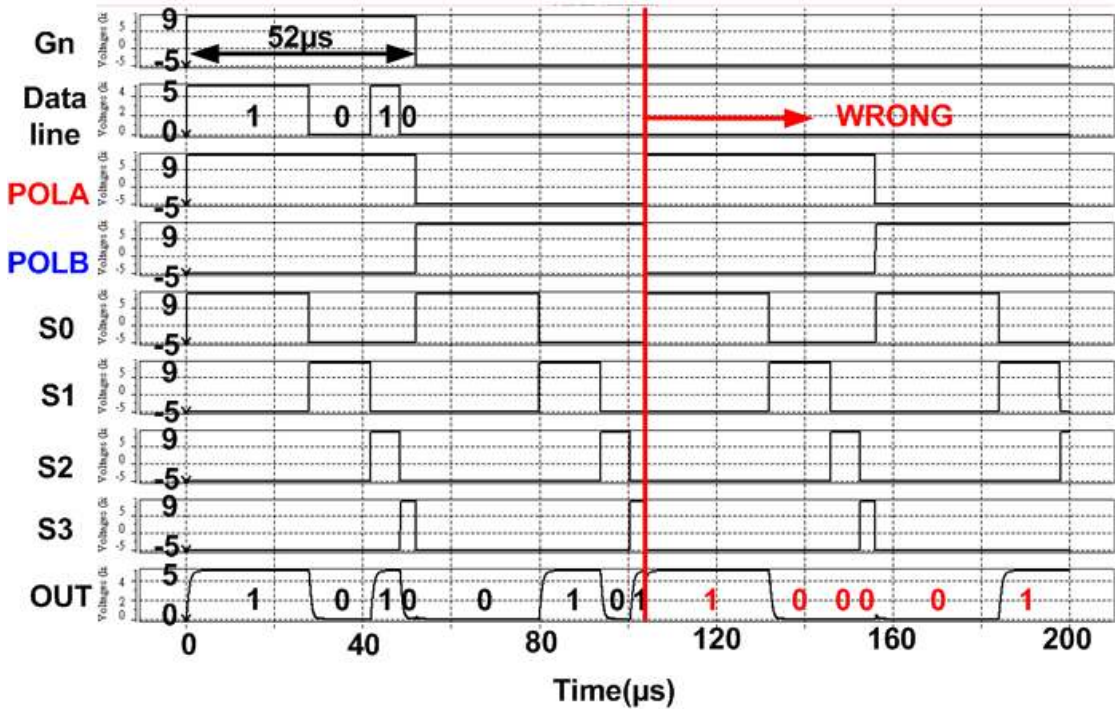


Figure 2.11 Time diagram of the simulation with Cm=0.3pF.

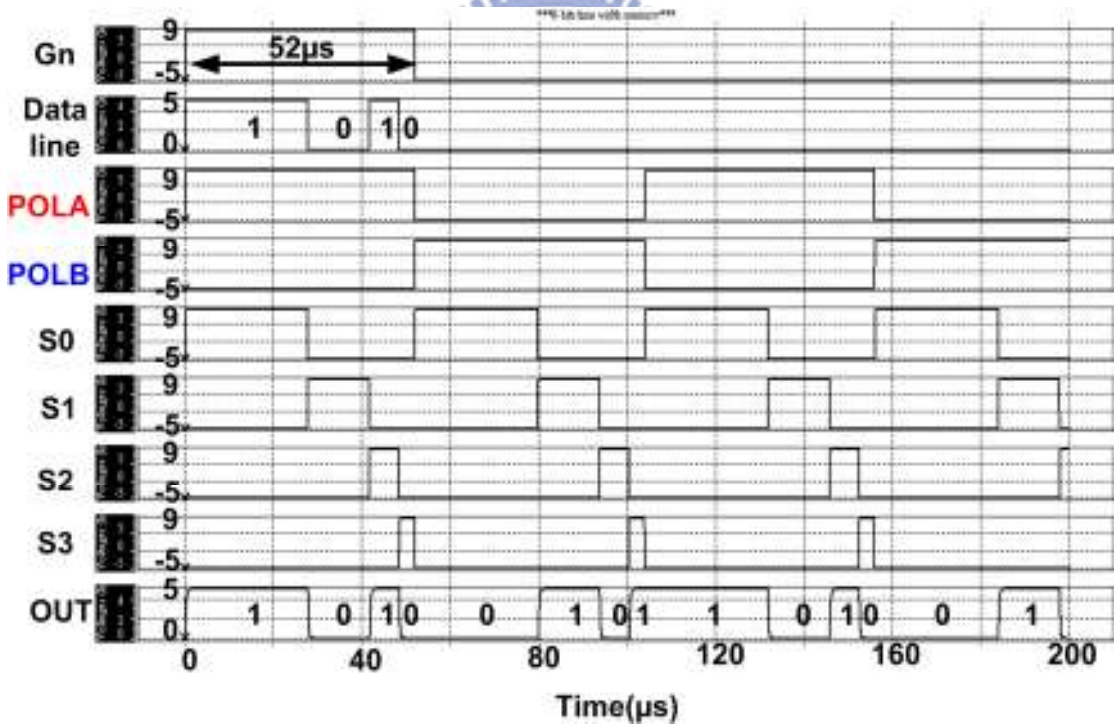


Figure 2.12 Time diagram of the simulation with Cm=0.6pF.

2.2.3 Discussions

According to simulated results, the power consumption of the proposed circuit in still mode is 0.24 μW per pixel. The scan driver and data driver are not included in the proposed circuit for power consumption simulation due to the limited resource, such

as chip area. However, by storing the frame data and generating its corresponding inversion data to refresh the static image without activating the data driver circuit, the power consumption of the proposed circuit can be reduced.

Also, the aperture for the LCD panel in the proposed circuit is higher because the occupied area from complicate routing for each binary-weighted pixel can be further decreased. The area impact is one of the most important issues in the proposed circuit. Since the time-modulation technique is utilized in the proposed circuit, the desired gray levels can be displayed by applying high or low logical voltage on the pixel in different time widths in a fixed time period. Therefore, the pixel is not needed to be divided in a binary weighted way as mentioned in area-modulation, which means the occupied area from complicate routing for each binary-weighted pixel can be further decreased, and the aperture for the LCD panel can be increased in the proposed circuit.

2.2.4 Summary

In this section, the concept of pixel memory circuit has been described. A 4-bit time-modulation pixel memory is designed and simulated in 3-μm LTPS technology. A 4-bit test pattern is given and the inversion can be done with the pixel memory circuit without the LCD driving circuit.

2.3 Experimental Results

2.3.1 Layout Considerations

The chip performance is often affected by the layout. At first, in order to reduce the sensitivity to process variation on capacitances of DRAM, the layout of these capacitances is aligned closely For the same reason, the switches layout is also put together to diminish the distortion or other errors caused by the process variation.

Figure 2.13 shows the photo of the fabricated 4-bit time-modulation digital pixel memory in a 3-μm LTPS. To prevent the parasitic capacitance of measurement equipment, about 10p, this layout adds a buffer for the output LC node.

The test chip size is 306μm x 465μm. It contains DRAM, switches, Clc and buffer. Then, the measured results will be discussed detailed in the next section.

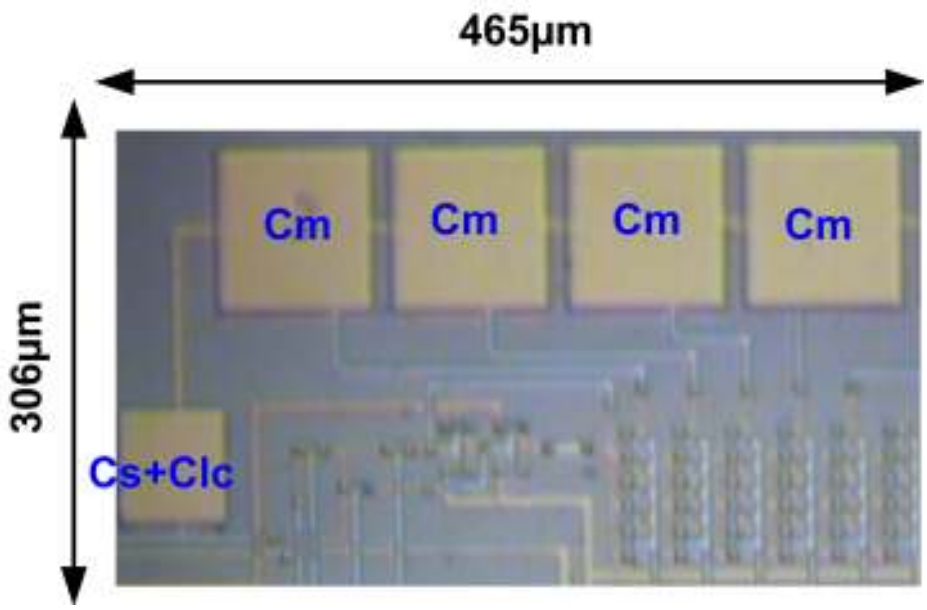


Figure 2.13 Photo of the fabricated 4-bit time-modulation digital pixel memory in a 3-μm LTPS.

2.3.2 Measurement Setup

The measurement setup is shown in Figure 2.14. Keithley4200 Dual Pulse Generator can produce clock signal waveform, which is high to 9V and low to -5V. It can also edit the waveform when to rise or fall down so that it can produce both

periodic and non-periodic waveform. Gn, data signal, S0~S3 are produced by it.

GPS 4303 DC Power Supply is a DC power supply which can provide separated pairs of power supply and ground where the supply voltage Vdd is 5 V and ground Vss is 0 V.

Agilent 81110A is pulse/pattern generator which can provide a pair of non-overlapping clock signals which is square waveform. It needs 81110A to generate POLA and POLB. To synchronize these two 81110A and Keithley4200, Agilent 33220A Function/arbitrary waveform generator is needed to be a reference clock. By connecting these three machines with one reference clock signal, these three machines can produce synchronized signal waveform.

SDO603A Oscilloscope shown in Figure 2.14 is a digital phosphor oscilloscope using to detect and display the signal waveforms.

The pixel memory circuit is designed on glass substrate and all of its input/output signals are bounded to the flexible printed circuit (FPC) pads and then connected to the PCB (printed circuit board) at the right hand side of Figure 2.14.

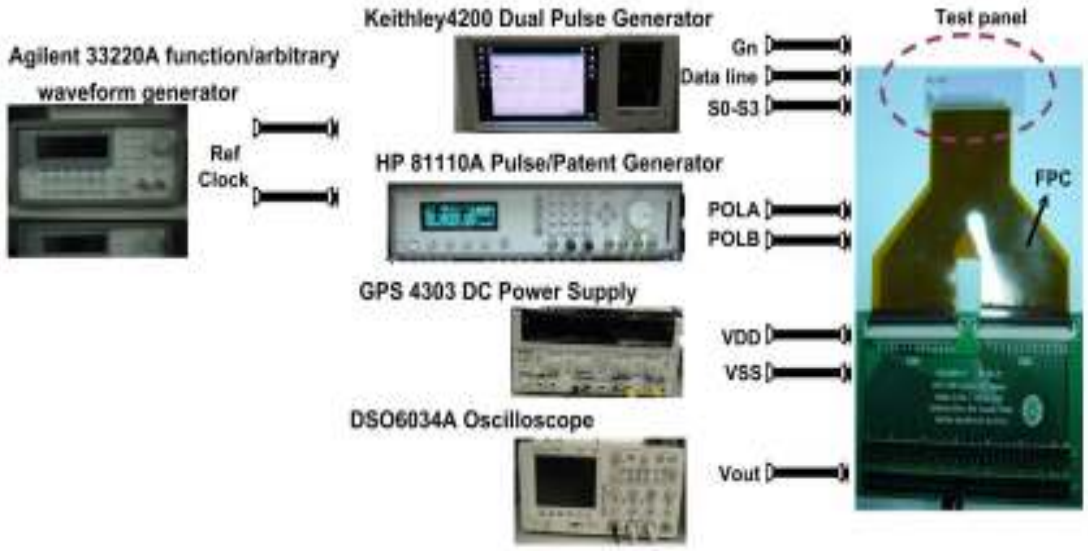
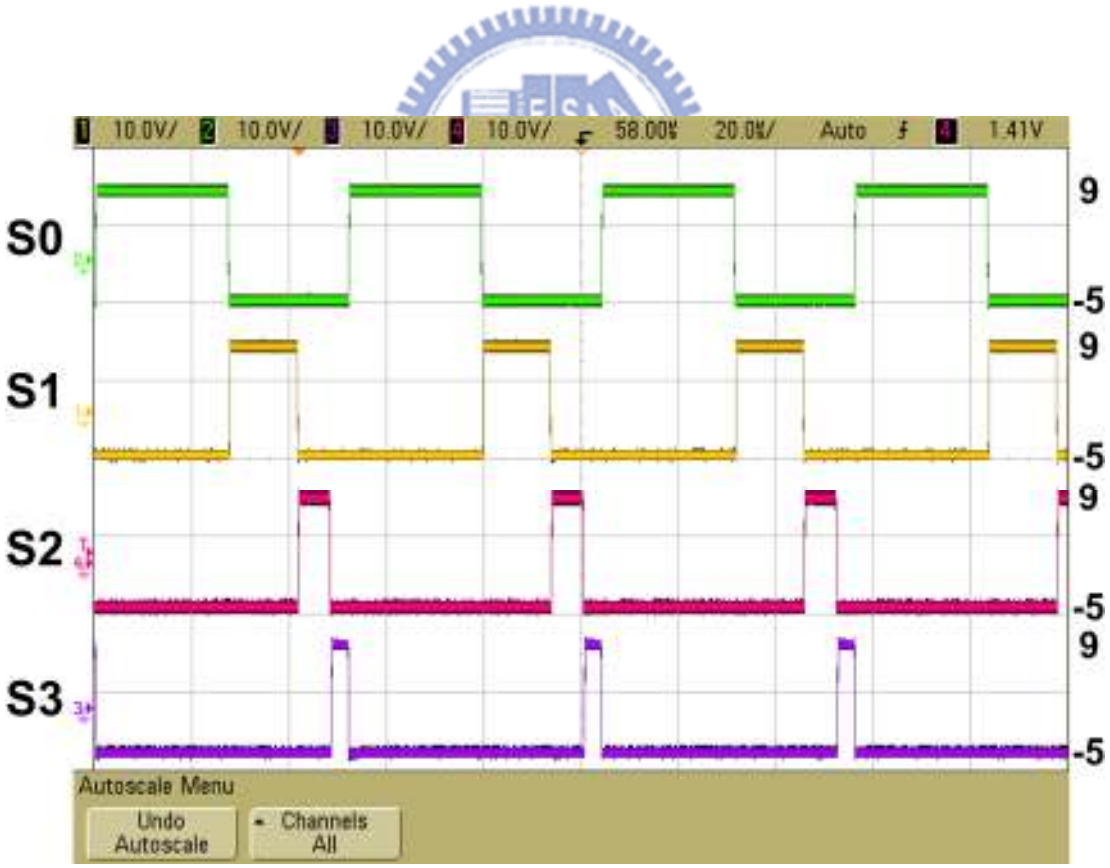


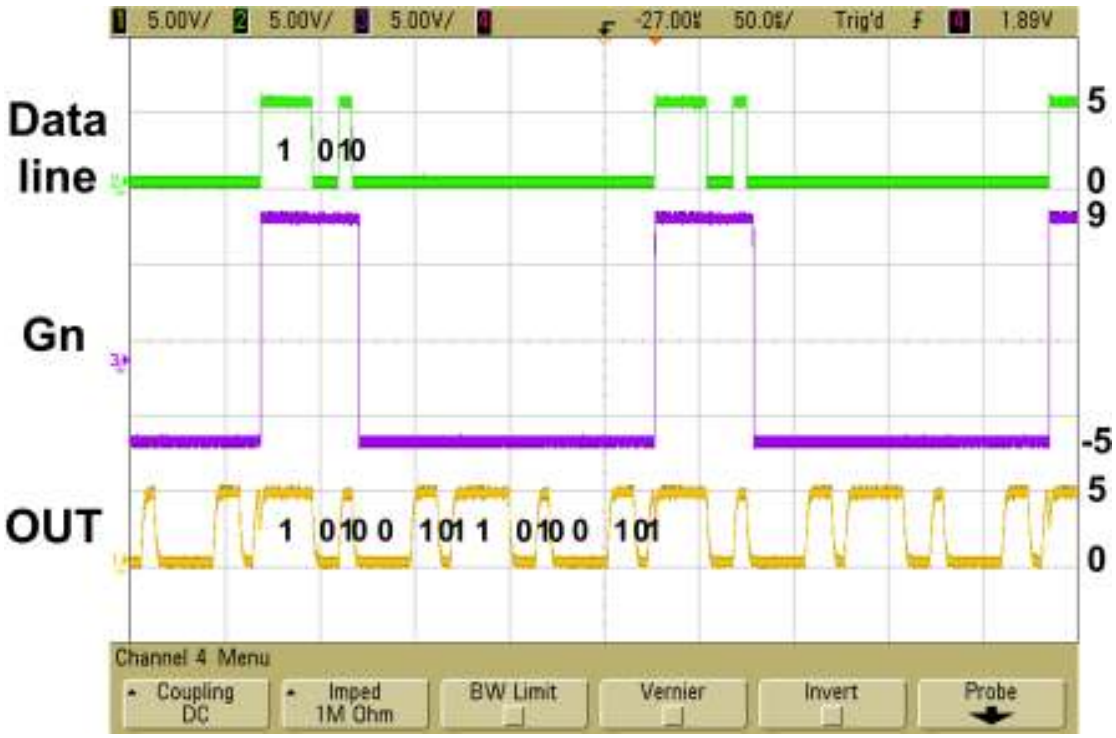
Figure 2.14 The measurement setup illustration for Pixel Memory Circuit.

2.3.3 Measured Results of the 4-bit Time-modulation Pixel Memory Circuit

Figure 2.15 (a) shows S0 and S1 and Figure 2.15 (b) shows S2 and S3. In order to follow the concept of time-modulation, the duty cycle of S0 is twice of S1, and duty cycle of S2 is twice of S3. During Gn is on, data line produces the test pattern "1010". Because large parasitic capacitance of measurement equipment will affect node LC, a buffer is added to LC node for measurement. As a result, output of buffer, buffer_out represents the waveform of LC node. Figure 2.15 (c) shows Gn, data line and buffer_out. LC node can do inversion by itself as Gn is off to show the pattern "1010", "0101" alternatively.



(a)



(b)

Figure 2.15 Measured result of the 4-bit time-modulation pixel memory (a) S0, S1, S2 and S3 (b) data line, Gn and buffer_out.

2.4 Summary

A 4-bit time-modulation pixel memory is designed, simulated and verified in 3-μm LTPS technology. A 4-bit test pattern is given and the inversion can be done with the pixel memory circuit without the LCD driving circuit. The power consumption of the proposed circuit in still mode is 0.24 μW per pixel. The measurement results show the pixel memory circuit can display 4-bit digital data and its inversion data on LC node alternatively when Gn is closed.

Thus, the proposed time-modulation pixel memory circuit has been successfully designed and realized in a 3-μm LTPS technology, and that is suitable to be further integrated with display panel to reduce the power consumption.

Chapter 3

Fundamentals and Realization of Two-direction Cyclic Digital-to-Analog Converter

For the first time, the cyclic digital-to-analog converter (DAC) is simulated in 3-μm LTPS process as a part of the LCD driving circuit. The concept of the cyclic DAC used in LCD driving circuit is described in the following section. Also, the design for each block of cyclic DAC is discussed in this chapter. Finally, the performance of the cyclic DAC designed in 3-μm LTPS process can be discussed from simulation. In this work, the DAC is designed for the driver of the 2.8" QVGA TN LCD mentioned in chapter 2. That means the DAC should convert the digital codes into analog value in 52μs. To take the time for buffer into account, the DAC needs to convert one bit per 4 μs.

3.1 Introduction

3.1.1 LCD Panel Data Driving Circuit [17]

In Figure 3.1, there are several blocks which consists the data driver including shifter register, data latch, level shifter, digital-to-analog converter (DAC) and analog output buffer [16]. For the first three parts, they can process the digital data from video signal so that they are classified as digital architectures. Shifter register (S/R) and data latch manage to transit and store the RGB signals. The level shifter (L/S) is applied to translate the RGB signal to a higher level voltage.

For the other two parts, the DAC can convert the digital data into analog signal which makes LCD pixel display with different gray levels and analog output buffer has the ability to drive the large RC load in LCD panel. So the DAC and output buffer are classified as analog architectures. There are many types of structure for DAC. The pros and cons for each structure of DAC will be discussed in the next section.

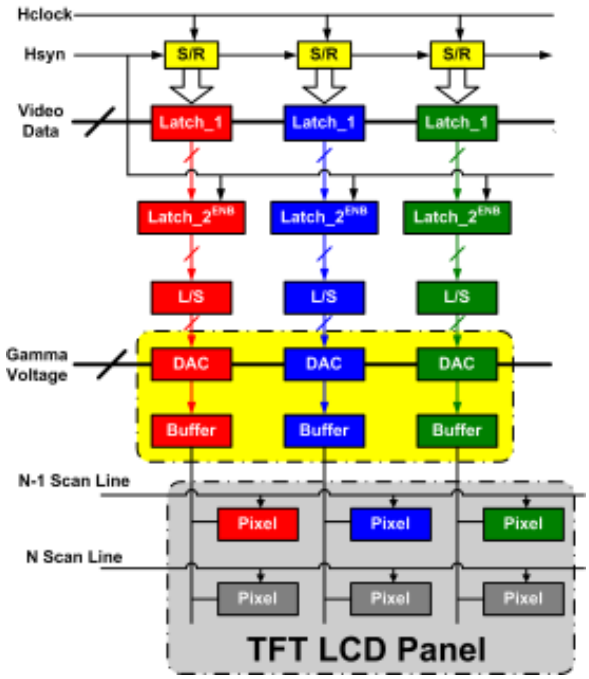


Figure 3.1 The basic diagram of data driver circuit.

3.1.2 Digital-to-Analog Converters [18], [19]

Digital-to-Analog (DAC) circuit takes an important role in data driving circuit as mentioned in last section. There are many types of structure for the DAC circuit. In this section, the pros and cons of these DAC circuits are illustrated and discussed.

R-String DAC with Switch Array Decoding

The R-string DAC circuit is a conventional DAC used in LCD data driving circuit. This structure is simple and easy for gamma correction design. A 6-bit R-string DAC circuit is shown in Figure 3.2. However, it needs larger area for the switch array as the resolution of DAC goes higher. The larger area means the power also goes higher when the area of switch array is becoming larger and larger due to the high resolution DAC. In addition, because of the huge switch array, the loading at the output node (Vout) is also becoming larger which means more power is needed to drive the load at the same speed.

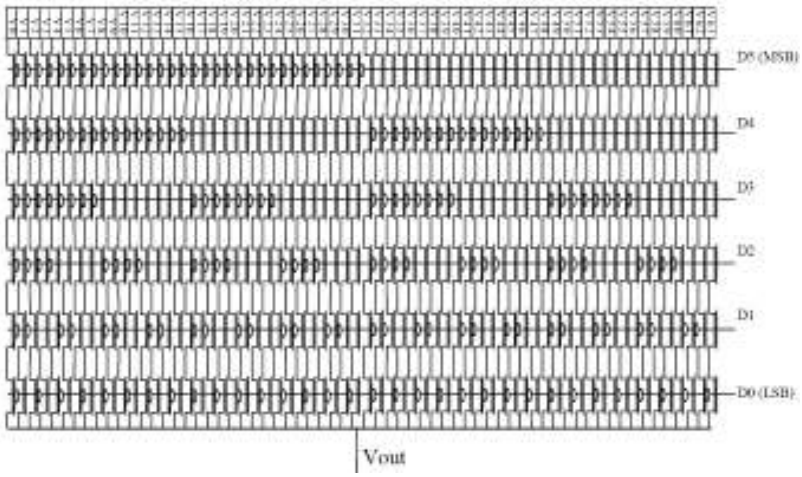


Figure 3.2 A 6-bit R-string DAC with switch array decoding.

Current-Steering DAC

The concept of current-steering DAC is to switch currents to either the output or to ground, as shown in Figure 3.3. The output current is the combination of binary weighted currents which are determined by input digital codes. This output current can be converted to a voltage through a resistor (R_F). This type of DAC can operate at high frequency because of its current type; however, this structure might suffer from large glitches due to timing skews. In addition, due to the current mode operation, it might consume lot of power.

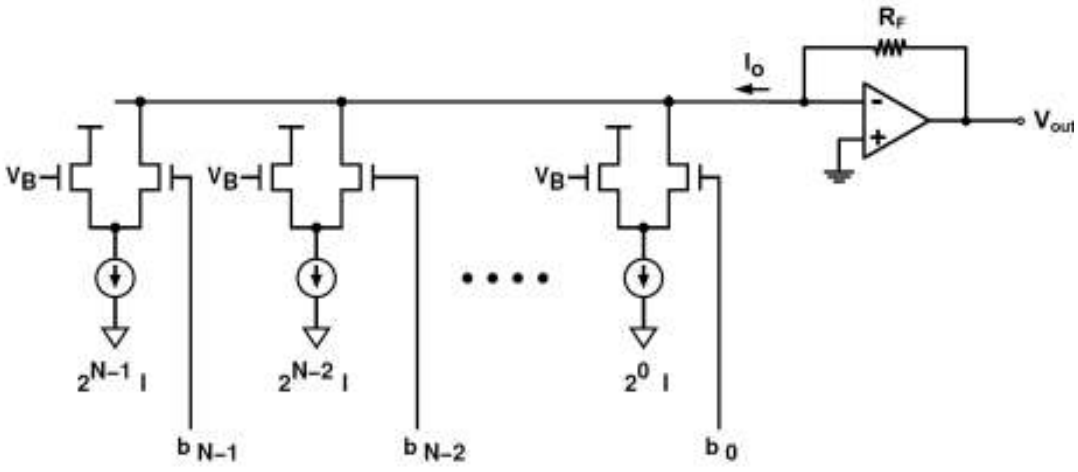


Figure 3.3 The current-steering DAC.

Charge-Redistribution DAC

The concept of the charge-redistribution DAC is using the switch capacitor (SC) circuit to convert digital codes to analog output. There is one kind of charge-redistribution DAC shown in Figure 3.. In this circuit, there are two phases in operation. For first phase (ϕ_1), all capacitor bottom plates are connected to a reference voltage and top plates are connected to ground. For the second phase (ϕ_2), capacitor bottom plates are connected to a reference voltage or ground according to input digital code. This circuit structure has some advantages like the process matching for capacitor is better than resistor string and this charge-redistribution DAC can save more power because it has no DC path in the circuit.

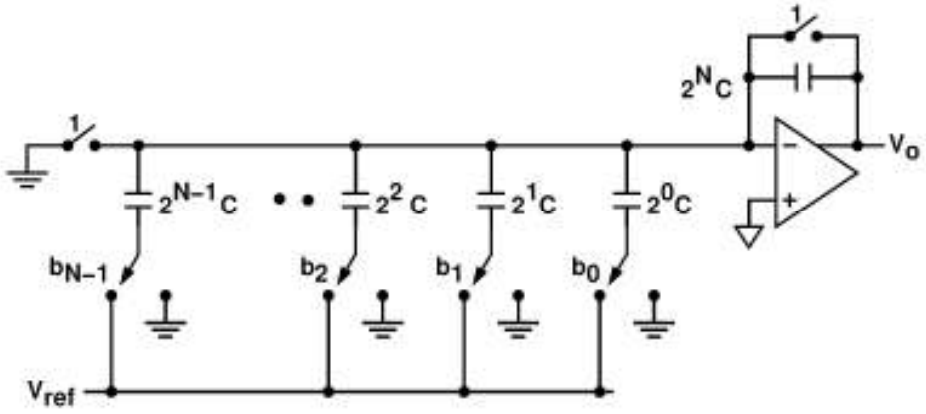


Figure 3.4 The charge-redistribution DAC.

In recent years, due to the digital gamma control, a linear DAC became possible. The digital gamma control was generalized for satisfying both higher resolution and RGB independent gamma control in high-performance application. That makes the linear DAC like current-steering DAC and charge-redistribution DAC are possible to be used as the LCD data driving circuit.

In this work, a cyclic DAC is simulated as the LCD data driving circuit. It is a kind of charge-redistribution DAC with serial operation. It is very attractive that the area of DAC is independent of its resolution because the architecture converts one bit at a time. However, it needs non-negligible conversion time, so this problem must be

solved using single output over two DACs or pipelining operation.

3.1.3 Summary

From the description above, the characteristics about many kinds of the DAC circuits can be summarized to a table, as shown in Table 3.2. There are many characteristics of those DAC in this table, like: operation speed, power consumption, area, and the complexity of design and layout.

For the low power consideration and small area purpose, the cyclic DAC (i.e. serial type charge-redistribution DAC) is designed and simulated in 3-μm LTPS process.

Circuit Type	Process Technology	Number of Bits	Settling Time	Power	Area
R-DAC with binary-tree decoder [22]	0.35μm	10	3μs	N/A	0.2× 1.26mm^2 for 4 channels
Charge-redistribution DAC	0.35μm	10	7μs	4μA/Channel	1704×262 mm^2 for 420 channels
Charge-redistribution DAC (Serial type) [20]	N/A	12	15μs	5μA/Channel	16.5× 0.9mm^2 for 420 channels

Table 3.2 The comparisons table of different kinds of the digital-to-analog converter.

3.2 Circuits Implementation on Glass Substrate

3.2.1 Circuit Description [20], [21]

The cyclic technique is based on the serial DAC shown in Figure 3.5. The conversion begins with both capacitors discharged and is accomplished serially by considering the least significant bit b_0 first. If this bit is a one, S2 is closed momentarily charging C2 to VREF; if it is a zero, C2 is left discharged. Switch S1 is then closed momentarily giving a voltage VOUT of

$$V_{out} = [\frac{b_o V_{REF}}{2}] \tag{3.1}$$

Leaving the charge on C1, the pre-charging of C2 is repeated, this time considering the next least significant bit b_1. After redistribution, the output voltage is

$$V_{out} = \frac{b_0 V_{REF}}{4} + \frac{b_1 V_{REF}}{2} \tag{3.2}$$

This repetitive procedure has the effect as the nth redistribution of driving the existing charge on C1 by two and adding a charge of

$$\frac{b_i V_{REF}}{2} \tag{3.3}$$

So that for an n-bit D/A conversion

$$V_{out} = \sum_{i=0}^{n-1} \frac{b_i 2^i V_{REF}}{2^n} \tag{3.4}$$

where N is the bit numbers.

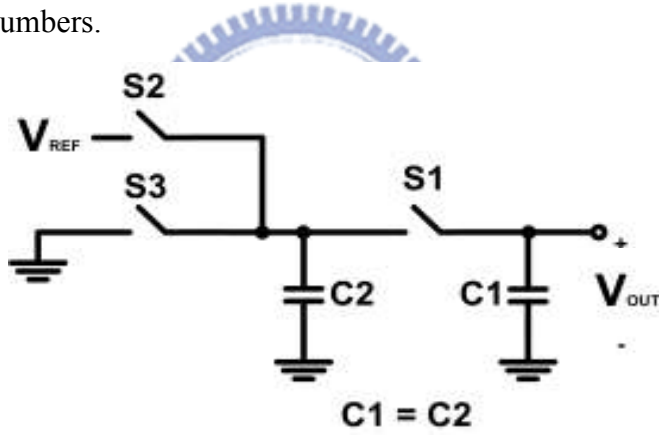
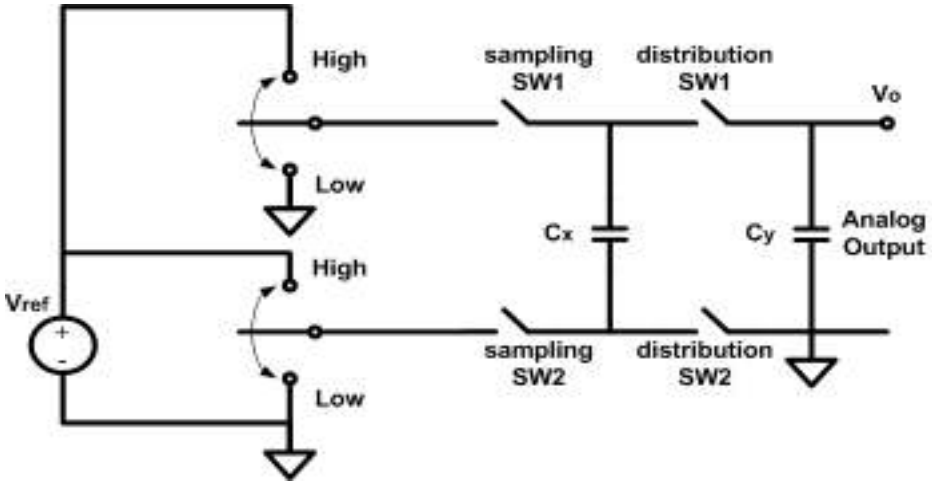


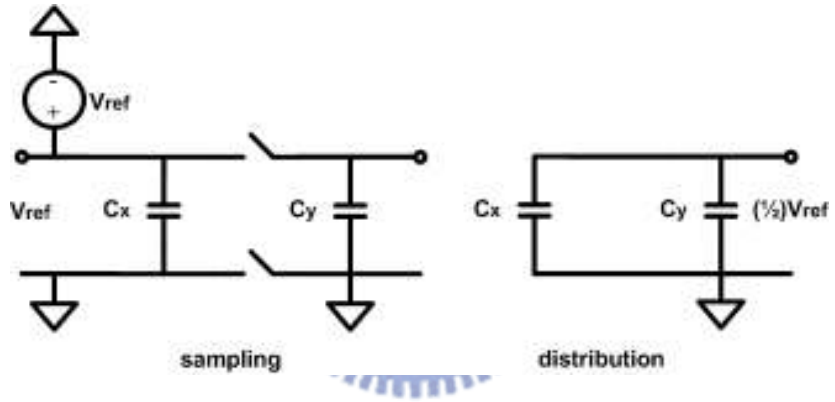
Figure 3.5 Concept of serial charge-redistribution DAC.

The basic concept of the two-direction cyclic DAC is that only one DAC could convert digital data into upper and lower analog value. The sign bit of digital data is needed to switch the mode of the cyclic DAC to decide converting upper or lower. Figure 3.6 shows the basic concept of two-direction cyclic DAC. When the sign bit of digital data is “0”, Cx will sample the positive Vref or zero, which depends on the digital data is “1” or “0”, on it and redistribute the charge in the next cycle. Figure 3.6 (b) shows how the DAC works when the sign bit of digital data is “0”. But when the sign bit of digital data is “1”, Cx will sample the negative Vref or zero, which depends

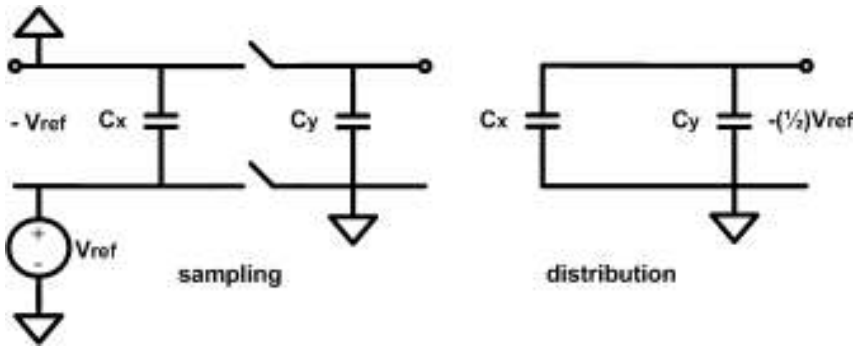
on the digital data is “1” or “0”, on it and redistribute the charge in the next cycle. Figure 3.6 (c) shows how the DAC works as the sign bit of digital data is “1”.



(a)



(b)



(c)

Figure 3.6 (a)The basic concept diagram of two-direction cyclic DAC, (b)operation when sign bit=”0” and (c)operation when sign bit=”1”.

Figure 3.7 shows how the concept of the two-direction DAC is implemented. A negative feedback operational amplifier is used to integrate the analog voltage on Vo

node. At the same time, due to the negative feedback configuration, two inputs of the operational amplifier is virtual short to the AC ground. As the concept mentioned, when the sign bit of digital data is “1”, Cx will sample the negative Vref or zero, and when the sign bit of digital data is “0”, Cx will sample the positive Vref or zero. Sampling switches and distribution switches close in turns to integrate the targeted analog value on output of operational amplifier, Vo.

The Vref of this two-direction cyclic DAC is designed to be 4V and from the equation 3.4, for an 8-bit D/A conversion,

$$V_{out} = \sum_{i=0}^{7} \frac{b_i 2^i V_{REF}}{2^8} \tag{3.5}$$

From equation 3.5, the output waveform under the 8-bit code 11111111 (255) is shown in Figure 3.8. In Figure 3.8, if the sign bit bn is ‘0’, the DAC would convert the digital code to analog data in up direction; however, if the sign bit bn is ‘1’, the DAC would convert the digital code to analog data in down direction.

Because the 8-bit data should be converted in 52μs, which is the gate time width of the pixel in 2.8" QVGA, the conversion time of the 8-bit data is designed to be 32 μs which means that it takes 4 μs to convert one bit. With the reason of that, the operation frequency of the switch should be 250 kHz.

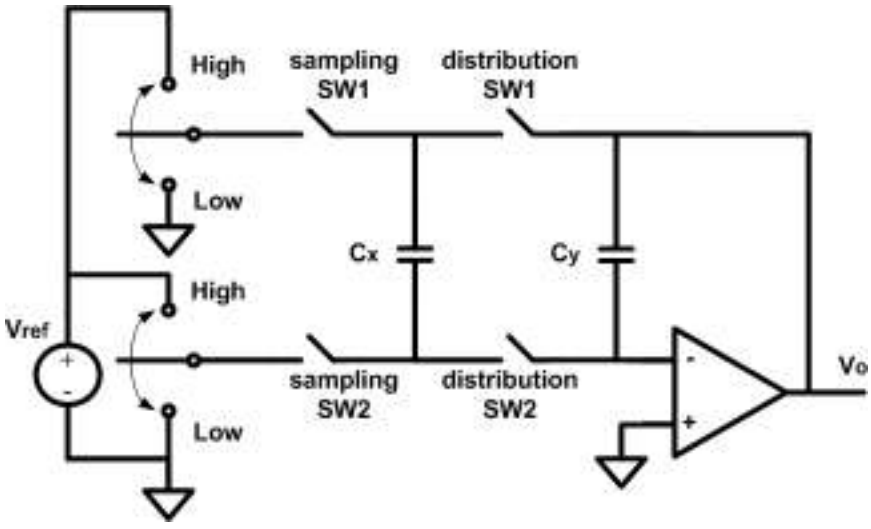
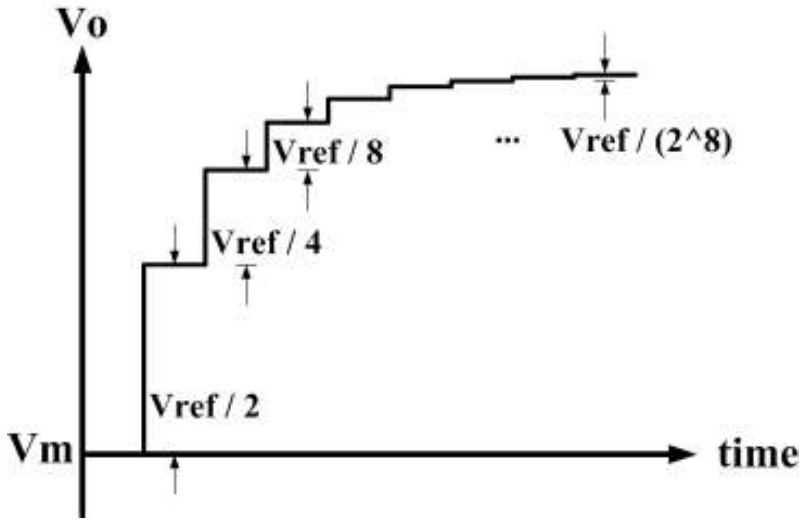
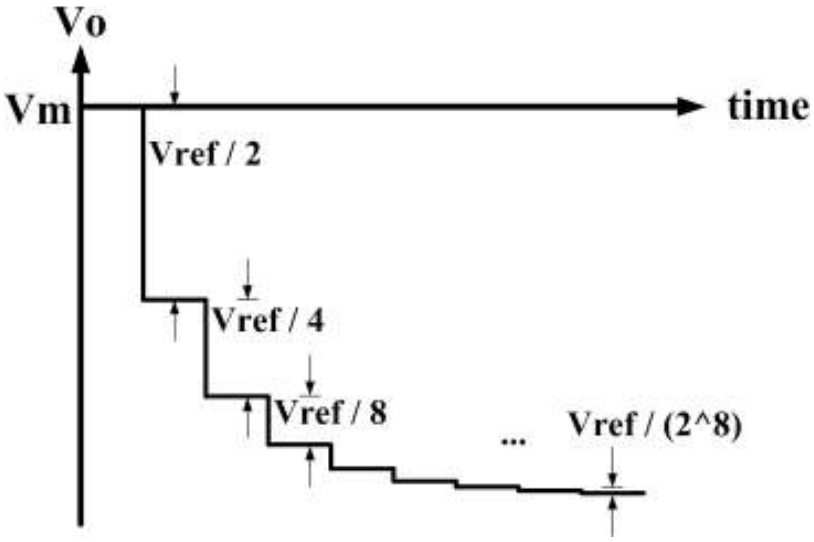


Figure 3.7 Implementation of two-direction cyclic DAC with Op amplifier.



(a)



(b)

Figure 3.8 (a)The output waveform with input codes 011111111 and (b) output waveform with input codes 111111111.

3.2.2 Design of the Control Circuit and Switches

To fulfill the design shown in Figure 3.7, the clock signal and the controlling circuit is needed as shown in Figure 3.9. The reset signal makes sure the output of the operational amplifier is as same as two inputs of operational amplifier to the AC ground before every 8-bit input data. Ctrl1 and Ctrl2 are designed to decide the sampling configuration with sign bit (i.e. bn) and data bits (i.e. bi). Cx must be equal to Cy, so that the redistribution process can divide the voltage by exact two. The

output of the buffer is vo node.

The switches are designed as complementary Switch (Transmission Gate). The schematic of complementary switch is shown in Figure 3.10. This switch consists of one pTFT switch and one nTFT switch. These switches are used to prevent Vt drop from input voltage Vin to output voltage Cout. The two control signals (i.e. Clk and Clk_b) can turn the switch fully ON or OFF. The on-resistance (when the switch is fully ON, so that input = output) is given by the formula:

$$R_{on} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})_n (V_{DD} - V_{T,n}) - [\mu_n C_{ox}(\frac{W}{L})_n - \mu_p C_{ox}(\frac{W}{L})_p]V_{in} - \mu_p C_{ox}(\frac{W}{L})_p |V_{T,p}|} \quad (3.6)$$

And the relation between accuracy and RC time constant of switch is given by:

$$t_s = RC \ln(\frac{1}{\varepsilon}) \quad (3.7)$$

where t_s is sampling time and ε is the accuracy. Because the switch should be operated at 250 kHz, for the 0.1% accuracy, the time constant $R_{on}C$ should be less than 0.29 μs.

The controlling circuit is aimed for controlling the cyclic DAC circuit to sample positive Vref, negative Vref , or zero with the digital values of sign bit (i.e. bn) and data bits (i.e. bi). If bn = ’0’, bi = ‘1’, then Ctrl1 = ‘0’ and Ctrl2 = ‘1’. The DAC circuit will sample a V_m^+ - V_m, positive Vref. If bn = ’0’, bi = ‘0’, then Ctrl1 = ‘1’ and Ctrl2 = ‘1’. The DAC circuit will sample a V_m^+ - V_m^+, zero value. However, If bn = ’1’, bi = ‘1’, then Ctrl1 = ‘1’ and Ctrl2 = ‘0’. The DAC circuit will sample a V_m - V_m^+, negative Vref. If bn = ’1’, bi = ‘0’, then Ctrl1 = ‘1’ and Ctrl2 = ‘1’. The DAC circuit will sample a V_m^+ - V_m^+, zero value. Table 3.2 shows the truth table of the controlling circuit.

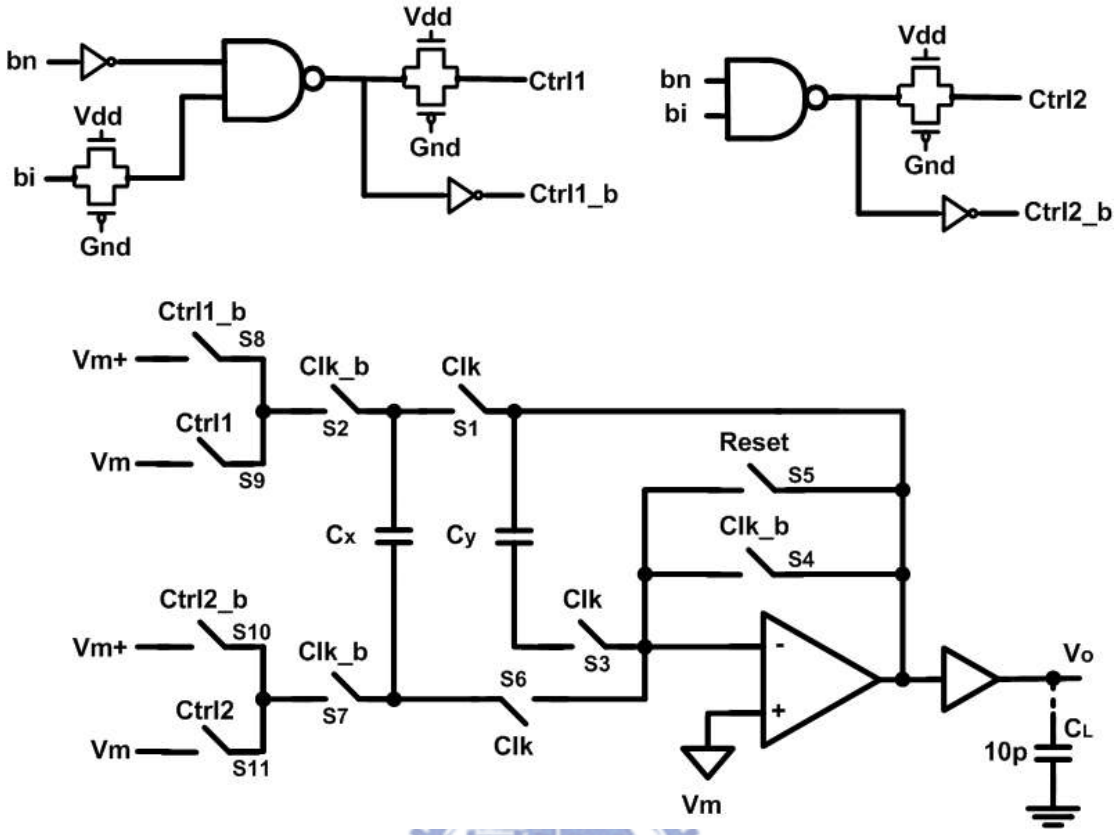


Figure 3.9 Circuit implementation of two-direction cyclic DAC.

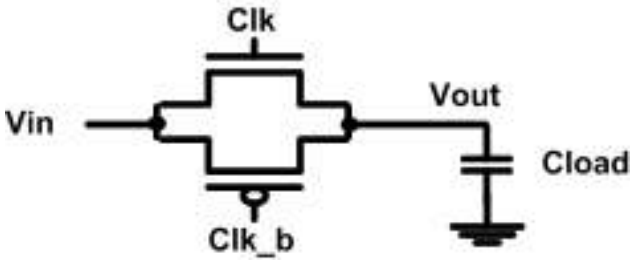


Figure 3.10 Analog complementary Switch.

bn	bi	Ctrl1	Ctrl1_b	Ctrl2	Ctrl2_b	Sampling Voltage
0	0	1	0	1	0	zero
0	1	0	1	1	0	positive Vref
1	0	1	0	1	0	zero
1	1	1	0	0	1	negative Vref

Table 3.2 The truth table of the controlling circuit.

3.2.3 Design of the Operational Amplifier Circuit

In order to achieve an N-bit linearity, requirements on opamp can be determined. In the cyclic DAC circuit, for the open loop of the opamp, the static error ε_S is given:

$$\varepsilon_S = \frac{1}{A_o} \cdot \frac{1}{\alpha} \tag{3.8}$$

where $\alpha = \frac{C_x + C_y}{C_x + C_y + C_p}$, C_p denotes the parasitic capacitance associated with the opamp's negative input and $C_x = C_y$. The DC gain is given by:

$$A_o > \frac{1}{\varepsilon_S} \cdot \frac{1}{\alpha} \tag{3.9}$$

When it comes to the speed requirement for the opamp, the dynamic error is given by:

$$\varepsilon_D = \exp(-\alpha \cdot 2\pi \cdot GBW \cdot t_S) \tag{3.10}$$

where t_s is the transition time. The required GBW can be found from:

$$GBW > \frac{f_c}{\pi \cdot \alpha} \ln\left(\frac{1}{\varepsilon_D}\right) \tag{3.11}$$

where $t_s = \frac{1}{2 \cdot f_c}$. By choosing $\varepsilon_D = \varepsilon_S = 0.05\%$, the DC gain should be larger than 66 dB and the GBW of the opamp is about $3 \times f_c = 750\ kHz$.

Figure 3.11 shows the topology of the opamps used in the cyclic DAC. Compared to a single-stage amplifier, a two-stage amplifier can achieve much higher gain, and larger output swing requirement. The single-ended two-stage configuration consists of a telescopic first stage followed by a common-source second stage. In this design, in order to enlarge the output swing, the M9 and M10 are added as the level shifter between the first and second stage. To ensure closed-loop stability, the parasitic pole created by the second stage in a two-stage amplifier needs to be pushed beyond its closed-loop bandwidth. The parasitic pole is located approximately at g_{m6}/C_L, where g_{m6} is the transconductance of M6, and C_L is the effective load capacitance

at node vo. The standard miller compensation has a pole-splitting effect, which moves one pole to a lower frequency and the other to a high frequency. n this work, the Miller compensation technique with nulling resistor (i.e. R_C) is adopted as frequency compensation circuit, which can provide a negative zero as

$$z = \frac{1}{(\frac{1}{g_{m6}} - R_C)C_C} \tag{3.12}$$

If R_C is greater than $\frac{1}{g_{m6}}$, the zero would move into the left half-plane (LHP), which can provide positive phase shift at high frequency region and consequently to improve the phase margin of this output buffer. The simulated frequency response is shown in Figure 3.12.

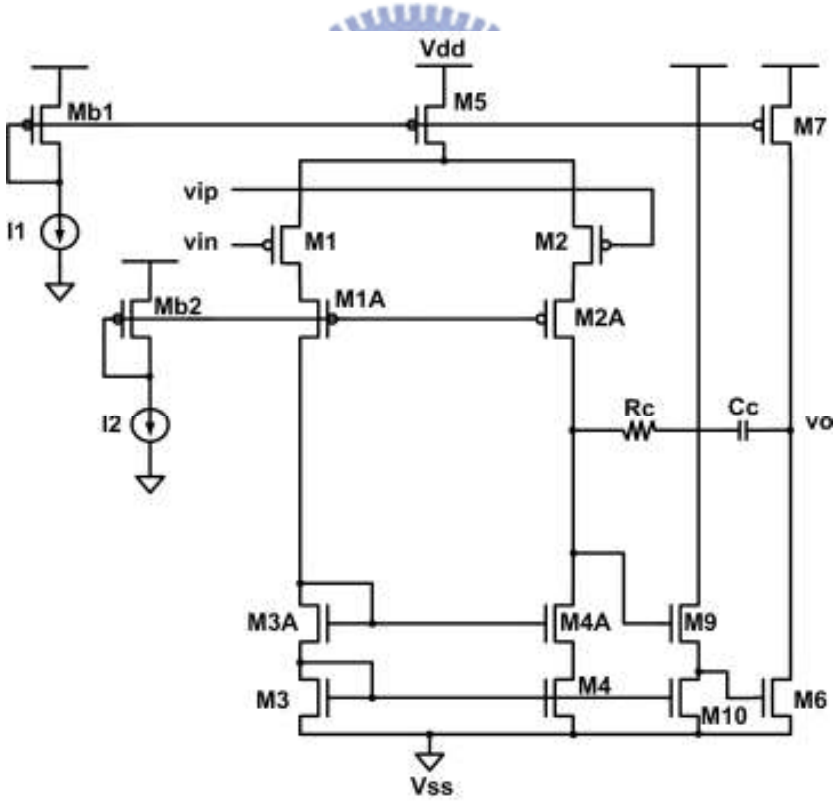


Figure 3.11 Circuit design of the single-ended two-stage operational amplifier on glass substrate in a 3-μm LTPS technology.

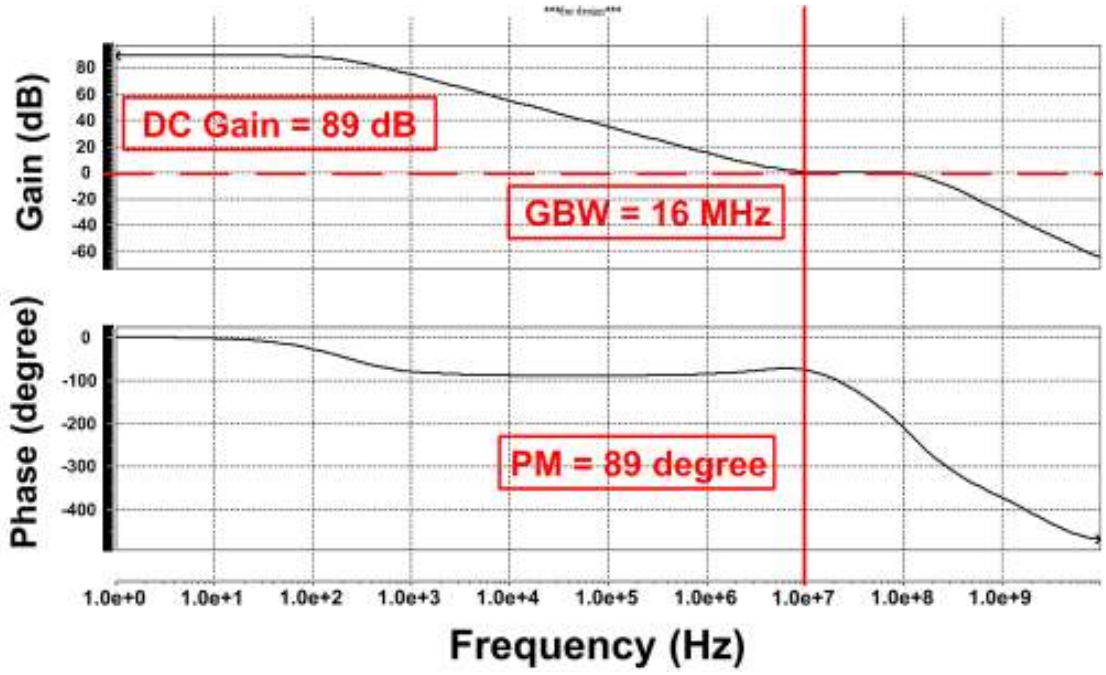


Figure 3.12 The simulated frequency response of the single-ended operational amplifier in open-loop condition.

3.2.4 Simulation

According to previous sections in this chapter, we can get whole architecture of this 8-bit two-direction cyclic DAC (as shown in Figure 3.9). This two-direction cyclic DAC has four voltage sources: V_{DD} = 10 V, V_{SS} = 0 V, V_m = 5 V, and V_m^+ = 7 V. That means $V_{REF} = V_m^+ - V_m$ = 2 V. This two-direction cyclic DAC has been successfully simulated in 3-μm LTPS technology. The simulation result of this DAC, assigned a series of digital input codes 11111111 (255) at 250-kHz operation frequency. Except for the first cycle, which is called 'reset cycle', there are still eight cycles needed to obtain the target analog conversion data. In Figure 3.13, it shows the simulation when the sign bit bn is '0'. The cyclic DAC with codes 011111111 can convert the digital codes to analog data in up direction. However, in Figure 3.14, it shows the simulation when the sign bit bn is '1'. The cyclic DAC with codes 111111111 can convert the digital codes to analog data in down direction. The average power consumption of the

cyclic DAC is 95.63801 μW and the average drive current per channel is 4.7657 μA.

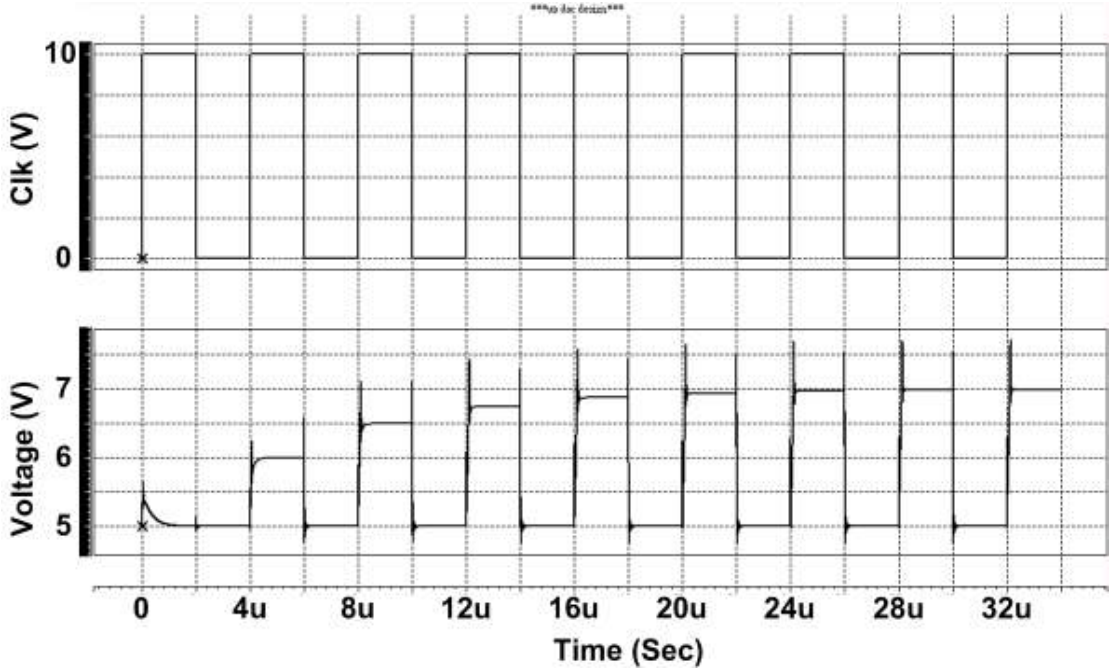


Figure 3.13 The simulation result of this 8-bit cyclic DAC with input codes 011111111 in 3-μm LTPS technology.

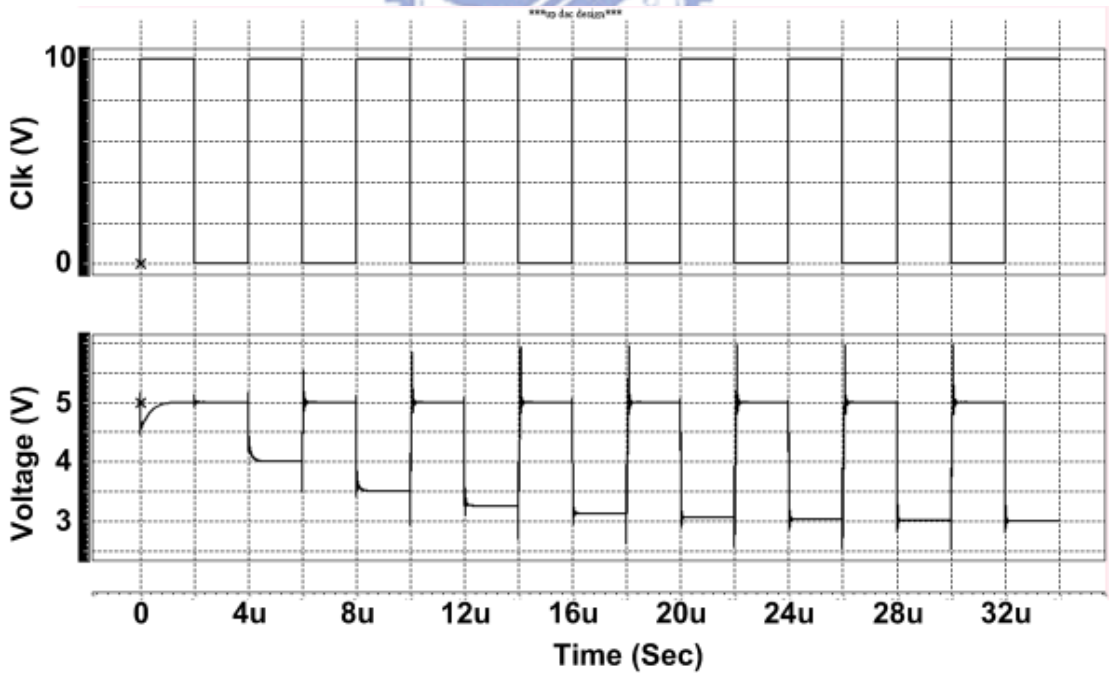
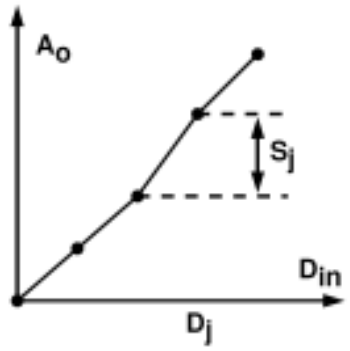


Figure 3.14 The simulation result of this 8-bit cyclic DAC with input codes 111111111 in 3-μm LTPS technology.

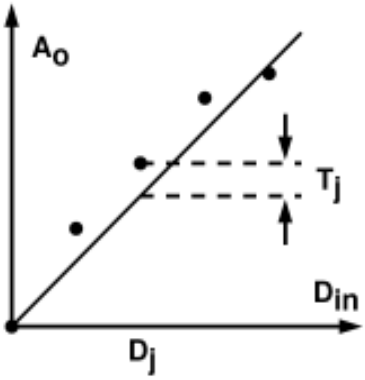
The linearity is an important specification of the data converter circuits except offset error and gain error. The linearity of the DAC depends on the deviation of the transfer curve from the ideal straight-line transfer curve. There are two factors to evaluate this kind of non-linearity, including differential nonlinearity (DNL) and integral nonlinearity (INL). The step size for the ideal DAC "Δ" is defined as least significant bit (1 LSB) in the data converter. The definitions of DNL and INL are shown in Figure 3.15.



$$DNL(D_j) = \frac{S_j - \Delta}{\Delta} \quad (LSB)$$

$$\Delta = \frac{A_{FS}}{2^N}$$

(a)



$$INL(D_j) = \frac{T_j}{\Delta} \quad (LSB)$$

$$\Delta = \frac{A_{FS}}{2^N}$$

(b)

Figure 3.15 (a)The definition of the differential non-linearity (DNL) and (b)the definition of the integral non-linearity (INL).

From the definition of the linearity above, the DNL and INL of cyclic DAC with codes 011111111 are shown in Figure 3.16. The maximum DNL is 0.35 LSB and the maximum INL is 0.55 LSB. However, when it comes to the cyclic DAC with codes 111111111, the DNL and INL are shown in Figure 3.17. From this figure, the

maximum DNL is 0.35 LSB and the maximum INL is 0.4 LSB.

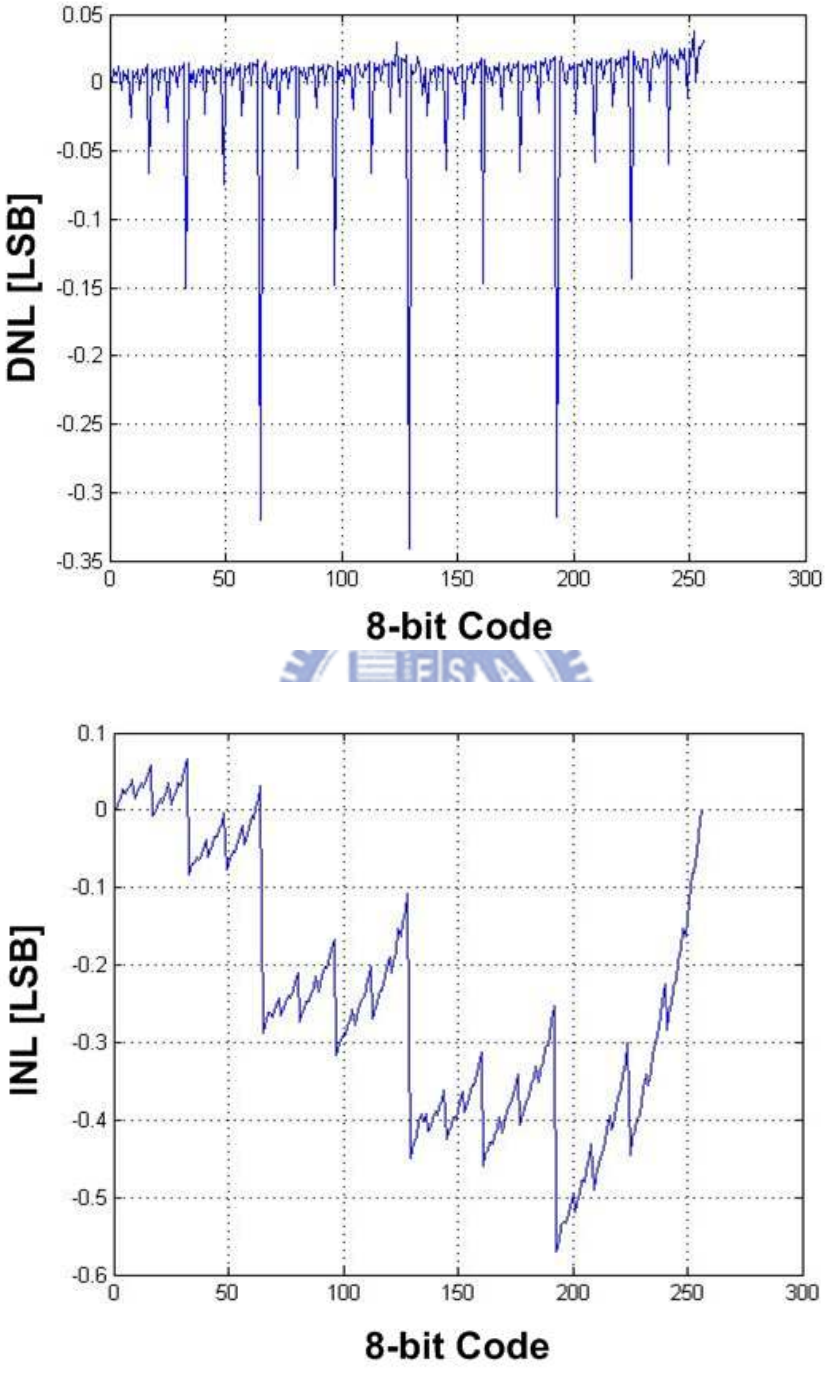


Figure 3.16 Simulated DNL and INL with input codes 011111111.

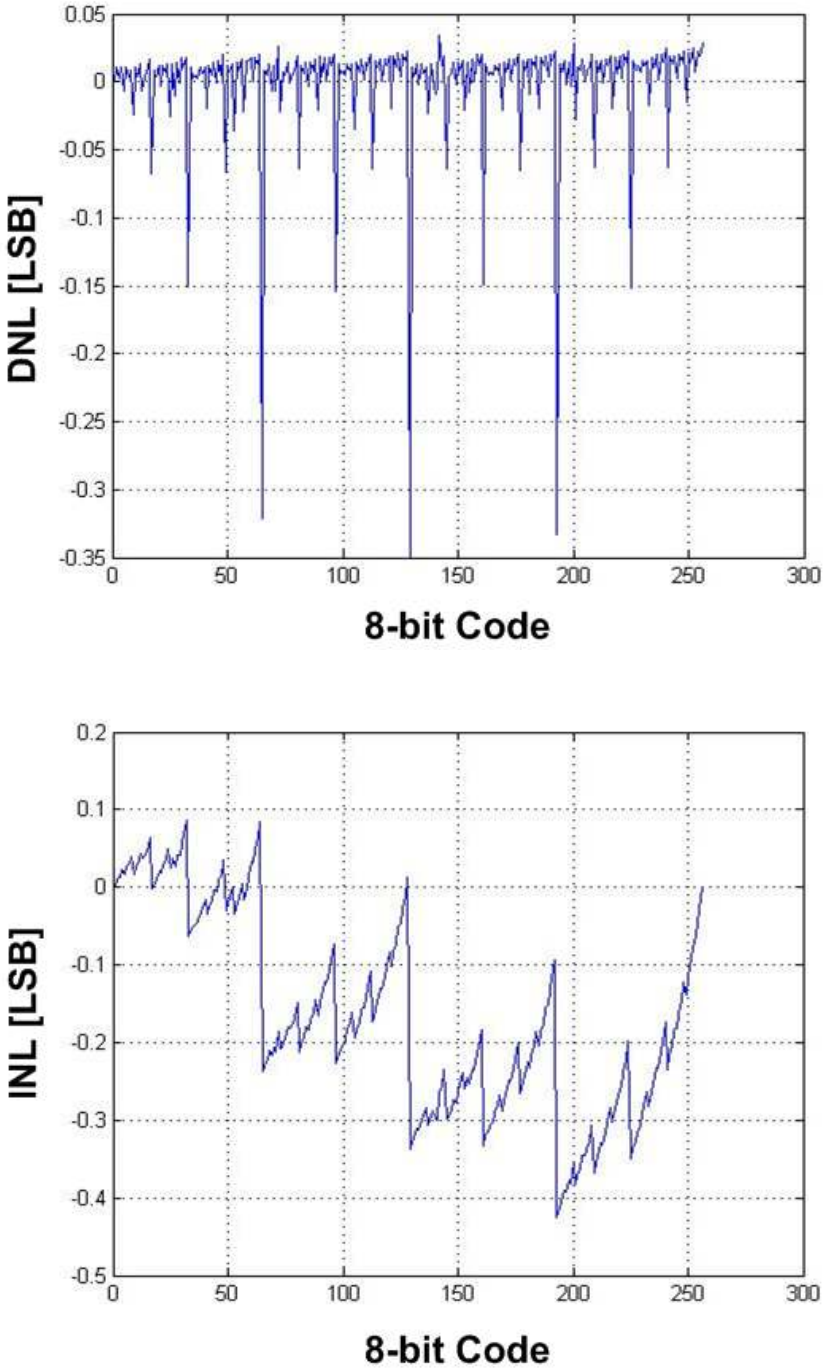


Figure 3.17 Simulated DNL and INL with input codes 111111111.

3.2.5 Summary

In this chapter, a speed and power efficient two-direction 8-bit cyclic DAC with 4 μs conversion time per bit has been has been successfully simulated in 3-μm LTPS technology for column drivers. The simulation results are shown above. The performance summary is shown in Table 3.1. This simple structure cyclic DAC shows

the capability of low power driver ICs for 2.8” QVGA TN LCD.

Parameter	*Performance*
# of bits	**8**
Accuracy (DNL/INL)	**0.35 LSB/0.55 LSB @ 250 kHz**
Speed	**4 μs/bit~2 μs/bit**
Power	**95.63801 μW**
Technology	**3-μm LTPS**

Table 3.3 Performance summary for cyclic DAC.

Chapter 4

Conclusions and Future Works

4.1 Conclusions

In chapter 2, a novel 4-bit time-modulation pixel memory is designed, simulated and verified in 3-μm LTPS technology. This pixel memory circuit allows the pixel display 4-bit digital data without the LCD driver circuit. That means the pixel memory circuit can display 4-bit digital data and its inversion data when gate driver and data driver of LCD are off. This pixel memory is suitable to be further integrated with display panel to reduce the power consumption.

In chapter 3, an 8-bit two-direction cyclic DAC for on-panel data driver has been simulated. This cyclic DAC has been successfully simulated in 3-μm LTPS technology. This cyclic DAC can be implemented with one opamp and two capacitors with clock controlling circuit. By using serial type charge-redistribution technique, the power efficiency of DAC can be achieved while using in a LCD driver circuit. Also, two-direction technique allows one cyclic DAC per one channel. The circuit configuration does not change with the input data. That makes the DAC more robust and has the smaller area.

4.2 Future Works

For the function verification, the size of the pixel memory circuit is overdesigned, so the size should be scaled down to be suitable for high resolution application. By scaling down the size, the power of the pixel memory circuit can be reduced.

And the two-direction cyclic DAC could be combined with digital gamma

control to perform DAC with gamma correction as shown in Figure 4.1 and integrated on the glass substrate.

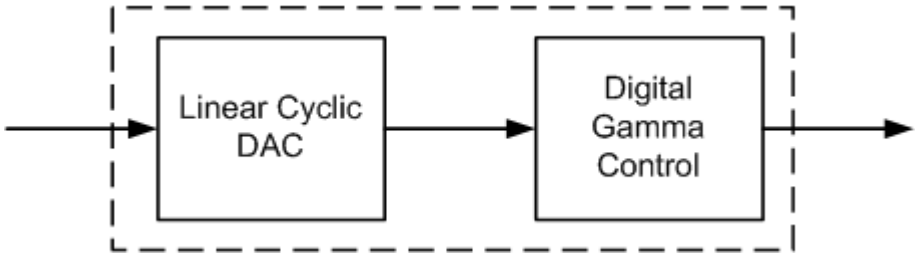


Figure 4.1. DAC block with gamma correction.

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