

# 國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

高效能高頻功率放大器使用控制電路調整基極  
電壓之研究

The logo of National Tsing Hua University is a circular seal. It features a central emblem with a book and a torch, surrounded by the university's name in Chinese characters and the year '1896' at the bottom.

**The Study of High Efficiency RF Power Amplifier with  
Adaptive Body Bias Control Circuit**

研究生：李佳芸

指導教授：荊鳳德 教授

中華民國九十九年七月

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## 摘要

本論文探討如何設計高效率的CMOS射頻功率放大器。我們將討論如何使用控制電路調整基極電壓來提升低輸入功率時的PAE。此差動功率放大器是使用TSMC 0.18um CMOS製程並經由ADS momentum做EM模擬分析。在此設計一個操作5.3GHz的功率放大器，並有最大輸出功率為27.9dBm，最大線性功率為26dBm，最大輸出PAE為34.3%，退後最大輸入功率12dB的PAE為12.2%的模擬結果。

# **The Study of High Efficiency RF Power Amplifier with Adaptive Body Bias Control Circuit**

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## Abstraction

Design of high Efficiency CMOS RF Power Amplifier will be investigated in this thesis. We will discuss how to use the adaptive body bias control circuit to enhance the PAE when the low input power is implemented. The differential power amplifier is implemented using TSMC 0.18um CMOS process. The EM simulation results with ADS momentum. A design 5.3GHz power amplifier have the post simulation results  $P_{out, sat}$  is 27.9dBm,  $P_{1dB}$  is 26dBm and the transducer gain is 19.3dB. PAE, Max is 34.3% PAE@12dB  $P_{in}$  back-off is 12.2%.

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99年7月

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# Chapter I

## Introduction

### 1.1 Background

Wireless Local-Area Network has three kinds of standard which are IEEE802.11a, IEEE802.11b and IEEE802.11g. The application of IEEE 802.11b is on web mail and internet browse with lower transfer rate and IEEE 802.11a is for media image wireless transmission with higher transfer rate. Due to the frequency and modulation technique differences between IEEE 802.11a and 802.11b the standard of IEEE802.11g comes out for products compatible.

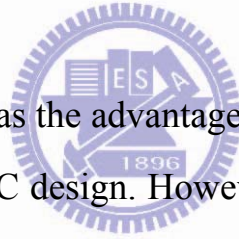
This research uses CMOS technology for high integration trying to achieve good linearity, high efficiency, high output power and comply the specification of IEEE802.11a which has 5150-5250MHz, 5250-5350MHz, 5725-5825MHz and injection power 40mW, 200mW and 800mW respectively.[14]

## 1.2 Research Motivation

Power amplifier is a key building block in radio frequency circuits that needs high breakdown voltage for large output power and low loss passive components for impedance transformation. Besides, for highly integrated circuit many researches trying to use CMOS technology rather than GaAs process. To lower down the enormous power consumption of the power amplifier in radio frequency and get higher efficiency is also a substantial subject.

Based on the above-mentioned problems, we try to use some circuit design skills such as differential structure, cascode structure, power combine technique and adaptive body bias to give solution for CMOS process limitation.

CMOS technology has the advantage of reducing integration costs; hence it is widely apply to IC design. However, CMOS is poor at current drive and large associated parasitic capacitances which lead to reduce usefulness in high frequency analog circuits.



### 1.3 CMOS Limitation

Although CMOS is widely use and many RF blocks can also have good performance. There are still have some blocks operate in a better efficiency by using III-V process and power amplifier is one of them. The reasons of CMOS aren't suit for making PAs are the following.

#### 1.3.1 Breakdown Voltage in CMOS Process

In recently, process scaling is the trend of integrated circuit that can improve transconductance and increase  $f_T$ . However, process scaling will lead to the electric field in the oxide become more significant and the critical field that could induce oxide breakdown as an insulator.

The electric field in the oxide is related to the voltage across the oxide by the thickness of the oxide and the relationship equation as


$$E_{ox} = \frac{V_{ox}}{t_{ox}} \quad \text{Eq.1-1}$$

Therefore, in order to keep the electric field in the oxide below the critical field, the voltage difference voltage across the oxide must be kept below the corresponding maximum voltage for the transistors still operate in normal function.

#### 1.3.2 CMOS Transconductance

The MOS transistors available in the CMOS process are used as thansconductance devices which mean an input voltage signal would generate an output current. In the saturation region for n-type MOSFET, the output current is related to input voltage by

$$I_D \cong \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \text{Eq.1-2}$$

And the transconductance of CMOS process is

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{\frac{2 \mu_n C_{ox} \frac{W}{L} I_D}{1 + \lambda V_{DS}}} \quad \text{Eq.1-3}$$

If we neglect the channel length modulation coefficient, the Eq. can rewrite as

$$g_{m, \text{MOSFET}} \cong \frac{\partial I_D}{\partial V_{GS}} = \frac{2 I_D}{V_{GS} - V_T} = \frac{2 I_D}{V_{\text{overdrive}}} \quad \text{Eq.1-4}$$

In Bipolar process, and the transconductance is

$$g_{m, \text{BJT}} \cong \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T} \quad \text{Eq.1-5}$$

The  $V_T$  is thermal voltage, it's about 25-mV at the room temperature.

In Eq.1-2, the MOS device is a square law relation with respect to its input signal; drive voltage  $V_{GS}$ . Typically, the over-drive voltage is about 200-mV of CMOS process [6]. Compare the denominator of Eq.1-4 and Eq.1-5, we can discover that BJT has larger amplification ability than CMOS process.

In order to solve the problem of poor current drive capability, one way is to increase  $V_{GS}$  that is increasing input signal to generate more current. The other way is to enlarge device size for the accommodation of parameter  $W$ . However, increasing the amplitude of the input signal will also consume more power in creating the input signal.

## Chapter II

### Research Contents and Methods

#### 2.1 Introduction

In this chapter, some of background information will be provided both on transmitters and power amplifiers. In order to integrate a linear or non-linear system power amplifier in a transmitter that attempts to satisfy a cellular standard or others specifications, transmitter architecture is amenable to power amplifier integration must be used. High efficiency and good linearity are among the important characteristics of a base station power amplifier used in numerous of the communication applications.

In general, PA can be put into two different types; one is the transistors nominally in its amplifying mode and act as a current sources and the other one is the transistors act as switches. These two types have several different sub-classes, which are used to identify the topology used in a particular implementation.

The several problems relate to CMOS process was introduced in last chapter which include oxide breakdown, poor transconductance and large device sizes. Overall select amplifying-mode classes or parasitic problems with CMOS process will face the issues and cause the efficiency drop down. Therefore, several methods will be introduced to solve the problems in circuit design skills.

## 2.2 The Basic Knowledge of Power Amplifier

Power amplifiers are used in the transmit chain of communication systems; the main purpose is to amplify the signal to the desired power level. The desired power level is determined by the communication system specification. For base-stations used in cellular systems, the magnitude of the transmitted power can be on the order of tens to hundreds of watts. However, the transmitted power of the portable wireless communication devices is often significant less; it will vary from tens to hundred milliwatts and in cordless systems from hundreds of milliwatts to a few watts in cellular system. However, the losses in the transmit medium such as air, it must be high enough such that the amount of power that the receiver is able to sense is adequate to recover the desired signal.

The power amplifier should be able to amplify and transmit signals. The most common unit is used to described the output power magnitude is dBm which is the output power in dB referenced to 1-mW. That is, the output power in dBm is given by

$$P_{dbm} = 10 \log \frac{P_{out}}{1mW} \quad \text{Eq.2-1}$$

Where  $P_{out}$  is defined in watts, thus 1-W is equivalent to 30dBm; and 0.1-W is equivalent to 20dBm. The power that needs to deliver to its load should need taken from the source which is the power of the pre-amplifier to output stage amplifier. In the case of portable unit, this will be the battery. In essence, the power amplifier converts the DC power from the battery into radio frequency power delivered to the load.



Unless the power conversion is lossless otherwise the power amplifier will consume power what it should delivers.

The way to represent how much power is consumed by a power amplifier changing the DC to RF power conversion is known as the PA's efficiency, given by

$$\eta = \text{efficiency} = \frac{\text{Power Delivered to load}}{\text{Power Drawn from Supply}} \quad \text{Eq.2-2}$$

The power efficiency is one of the key characteristic used to judge a power amplifier's performance. Because of power amplifiers in portable applications are driven from a source with finite amount of available energy and the higher power efficiency can lead to the longer battery lifetime.

Furthermore, we must know more detail about the final stage Pas, there are variations on the metric that give us more information about the power amplifier. The drain efficiency is defined as

$$\eta_D = \text{drain efficiency} = \frac{\text{Power Delivered to Load}}{\text{Power Consumed in Final Stage}} \quad \text{Eq.2-3}$$

The drain efficiency is the ratio between the radio frequency output power and the DC power consumed. This tells us how efficient the final stage, often referred to as the power stage.

When we inspect the PA implementation more close to real situation, we usually use power added efficiency to describe it. Because of the power need to drive the PA is not only including DC power but also power source. The power deliver to the PA should be taken into account and the efficiency given that

$$\begin{aligned}
& \text{PAE} = \text{Power Added Efficiency} \\
& = \frac{(\text{Power Delivered to Load}) - (\text{Power Delivered to PreAmp})}{\text{Power Drawn from Supply}} \\
& = \eta_D \cdot \left(1 - \frac{1}{G}\right) \qquad \text{Eq.2-4}
\end{aligned}$$

The PAE is a more practical measure parameter accounts for the power gain of the amplifier. The power added efficiency which can see from upper formula that must less than drain efficiency except the power gain getting higher. Therefore, if the power gain is not enough than more stages should be added .The power amplifier must deliver a large amount of power to the antenna while consuming a minimum amount of power. In general, in order to maximize the power added efficiency, the magnitude of the input power should also be quite small. The smaller the size of the input, the less power consumed by the previous stage in providing the required signal drive.

The specification of power amplifier calculated based on the link budget of the entire transceiver. Table 2.1 lists the typical PA performance.

**Table 2.1 lists the typical PA performance. [6]**

Output Power	+20 to +30 dBm
Efficiency	30% to 60%
IMD	-30dBc
Supply Voltage	3.8 to 5.8 V
Gain	20 to 30dB
Output Spurs and Harmonics	-50 to 70dBc
Power control	On-Off or 1-dB Steps
Stability Factor	>1

Some of the key specifications in the power amplifier design are its frequency of operation, output power level, power gain, efficiency and power consumption. Traditionally, all the impedance of any RF block is

terminated to  $50\Omega$ , especially to aid in the testing. However, sometime it

not only to conform to antenna of typical intrinsic impedance used  $50\Omega$ .

Since the load impedance are different and the power gain and voltage gain would not be the same.

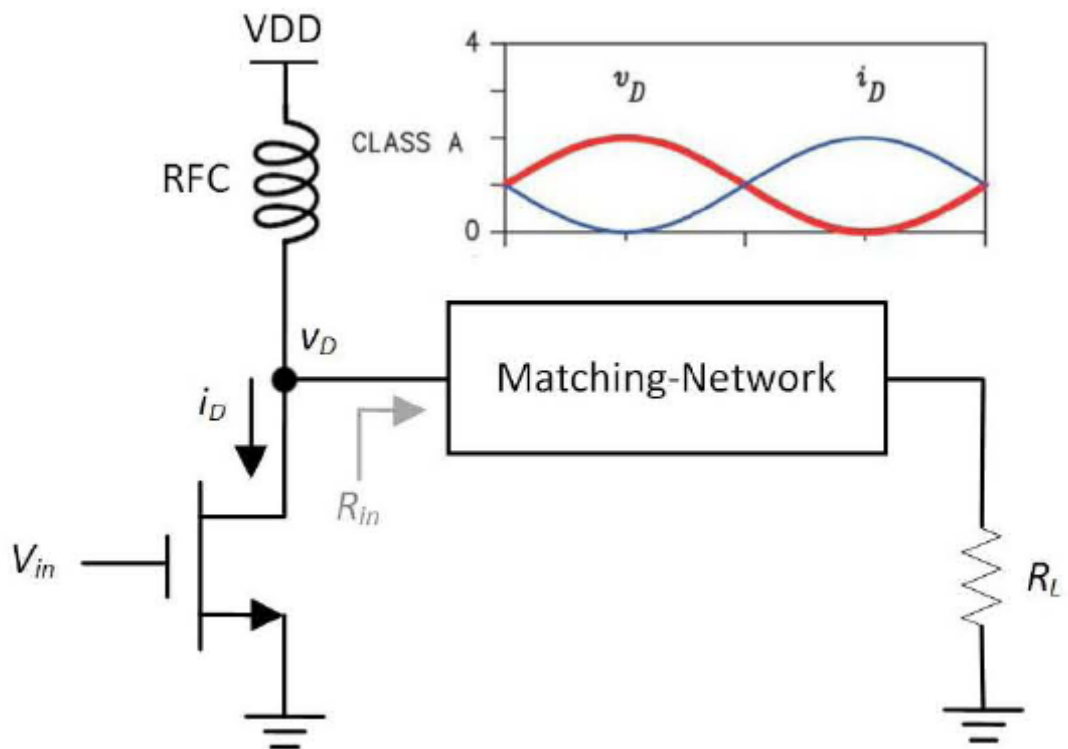
## 2.3 Different Classes Implementation of Power Amplifier

Generally speaking, PAs can be separated to two different categories; one is in its amplifying mode and the other is acting as a switch. The amplifying mode device normally acts as a current source and works as linear class of power amplifier. The switching mode category is referred to as the nonlinear power amplifier. And sometimes, we can use the dc bias condition to classify the linear or nonlinear mode of PAs. In general, RF power amplifiers can be specified as class A, B, C, D, E and F that different kinds of power amplifier classes have different transistors conduct cycle. [7]

The generation of significant power for power amplifiers depends on the standards of wireless communication. Each application has its own requirements for operating frequency, bandwidth, power, efficiency, linearity and cost. Besides, power amplifier is not only a simple linear amplifier which operate in small signal, on the other hand, power amplifier operate in large signal and has different properties comparing to traditional operating amplifier.

The phrase “linear” is just a concept to describe how output signal close to the input signal, as stated earlier, this just identifies the group of PAs in which the device is intended to operate in its amplifying region. For amplification of amplitude-modulated signals, the quiescent current can be varied in proportion to the instantaneous signal envelope. Since the devices are meant to operate in their amplifying region, it should be apparent that there exist some relationship between the magnitude of

input and output, regardless how linear that is. And the relationship between linearity and efficiency are mutual trade off [8] [9]. The linearity is direct proportional to conduct angle which means that the longer the conduction cycle the better linearity a PA has. However, the average power is consumed even when no signal is applied that will lead to lower efficiency.



**Figure 2-1 Basic Class-A implementation**

The above description describes the group of PAs known as Class-A PAs and the device conducts current for entire input sinusoid cycle. The amplifying device is biased in such a way that it always remains in its amplification region, even under maximum input signal conditions. The bias voltage is set to keep the device still operate in saturation region even when the swing of input signal reaches the maximum the gate

voltage should over threshold voltage. The output voltage swings around its bias point; in general is the supply voltage,  $V_{DD}$ . On the ideal situation, the maximum amplitude of the output swing is just  $V_{DD}$  which can help us determine the peak efficiency of the Class-A configuration. If we consider that

$$I_o = \text{average current} \quad \text{Eq2-5}$$

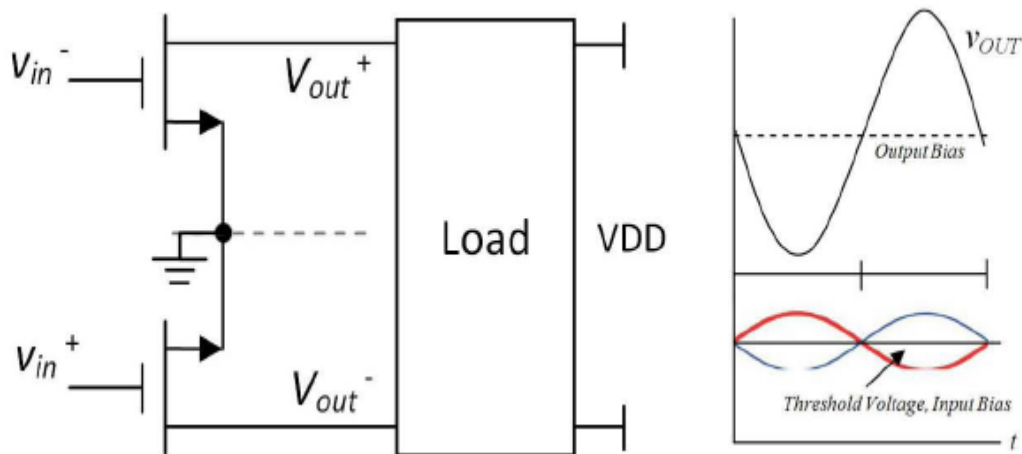
And the peak efficiency is given by

$$\eta = \frac{\frac{1}{2}V_{DD}I_D}{V_{DD}I_D} = 50\% \quad \text{Eq2-6}$$

As we can see that the peak efficiency of class-A PA is 50%. As a result, class-A PAs are used in applications which require low power, high linearity or high gain.

If the bias condition is going to change and make PAs not always operate in saturation region which introduce the idea of class-B PAs. Class-B PAs sometimes also called push-pull output stage. In standard implementations, two amplification devices are used and used differential input to maintain the original waveform. Each of the devices has only half sinusoidal period that is to say the conducting angel is only half of the class-A PAs. The efficiency of this implementation is greater than that of the class-A implementation and the theoretical peak efficiency of the class-B PAs is given by

$$\eta = \frac{\pi}{4} = 78\% \quad \text{Eq.2-7}$$



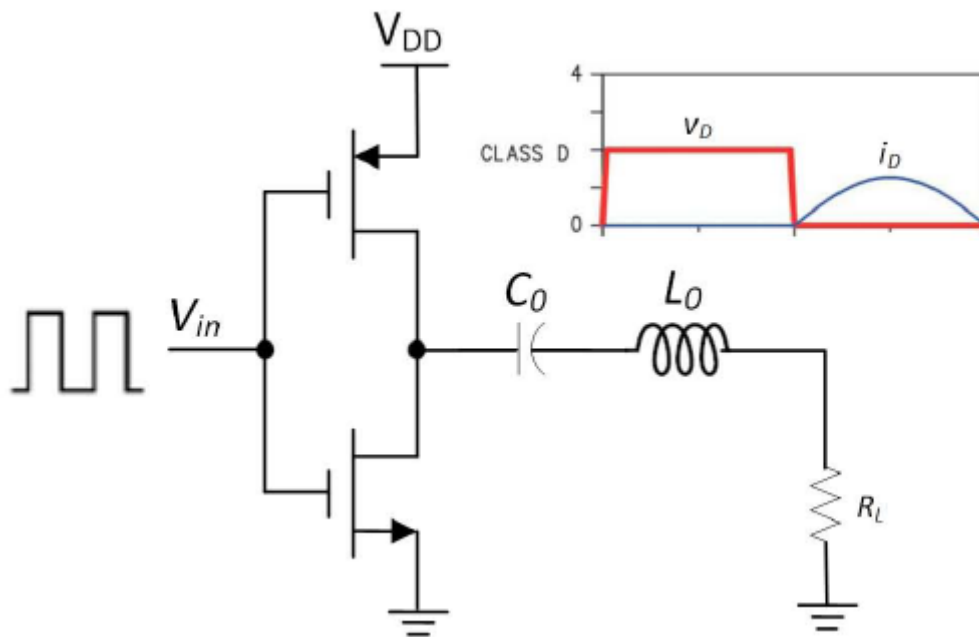
**Figure 2-2 Basic Class-B implementation**

Although the efficiency will enhance by using class-B implementation the linearity will degrade at the same time. And sometime if the gain through the devices is not exactly the same, the output will not be smooth sinusoid. Therefore, the issue of mismatch between two devices occurs no matter the parameter of threshold voltage or mobility difference. Crossover distortion is the existences of dead-zone during the devices turn on by turns leading to output signal distortion which also decreasing the linearity.

In order to gain better linearity we should obtain the balance between class-A and class-B configurations and this is the reason of class-AB generation. The power amplifier is now based such that it is on for more than half the cycle. In this case, the problem of dead-zone is avoided because there is a portion when both devices in a push-pull implementation are on [6] [7]. In narrowband RF implementations, class-B and class-AB PAs can also be implemented using a single device adding an RF filter at the output to extract the fundamental frequency

component of the output waveform. Normally, a single device would induce a problem that the device would be off for part of the input cycle and generate a chopped and thus become extreme distortion of output waveform while the input power is large. However, through the use of narrowband RF filters, the component of the output waveform at the fundamental frequency can be extracted and the amount of distortion can be reduced.

The group of “Nonlinear” PAs is also known by a more descriptive name: waveform shaping-mode or switch mode PAs. For RF PAs, the two classes of switched mode PAs which have received the most attention are class-D and class-E PAs.



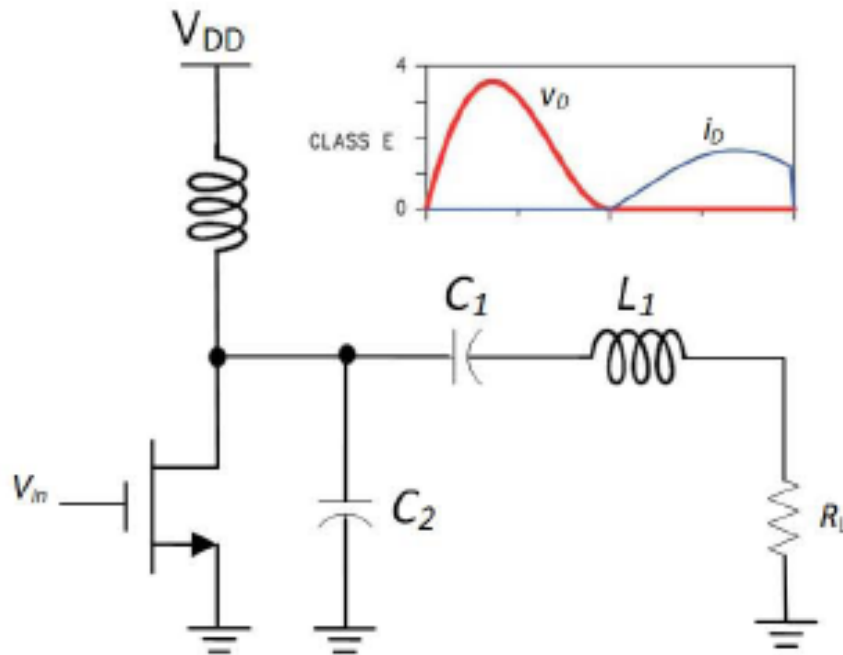
**Figure 2-3: Class-D implementation**

The class-D architecture is similar to what is used in a bridge DC-DC converter [10]. In the style of DC-DC converter, the devices acting as switches change the polarity of the input voltage onto the load



and the resulting output is averaged to create an output voltage that is some fraction of the input voltage, depending on the duty cycle of the switching. If the implementation of the switch is assumed to be ideal, then no on-resistance and the output voltage will be zero exactly when the switch is closed the ideal maximum efficiency of the power stage can be 100%, as no power will be consumed in the transistor.

The class-E PA, is also used the idea of soft switching in order to further reduce power consumption by the device in the switched-mode PA. This class of power amplifier has also been recently implemented in a CMOS implementation [11] [7] [10]. Basically, the class-E power amplifier tries to force the voltage on the output node becoming zero voltage at the instant that the switch is closed, so there is ideally no time at the transition when both the output voltage and current are non-zero. Not only is that but also there is no  $CV^2$  energy loss from the output capacitance discharging as the switch is turned on. In order to account for timing errors in the switching instants, the slope of the output voltage waveform should also be zero at the instant of that the switch closes. Because of any timing error when the switch closes, the power consumed attribute to any overlap in the output current and voltage waveforms will be minimal; since the slope of the output voltage at the correct instant is zero, the value of the output voltage at instants close to the output voltage will be very small to improve the drain efficiency. So, an ideal class-E power amplifier consists of a single supply voltage  $V_{dd}$ , an RF choke inductor  $L_{dc}$ , a switch with a parallel capacitor  $C_p$ , a resonant circuit  $L_o$ - $C_o$ , and a load  $R_L$ , or intrinsic impedance  $50\text{-}\Omega$ .



**Figure 2-4: Class-E implementation**

And like the class-D PA, the theoretical efficiency of the class-E power amplifier is 100%, again, practical considerations, especially in CMOS limitations, have limited the efficiency to about 50%[11], although GaAs implementation have reached close to 60% efficiency[10].

## 2.4 General Technique for Power Amplifier Design

There are two useful ways that can apply on power amplifier design. One way is differential structure and the other way is cascode structure. These two methods are commonly used to improve the overall performance of CMOS power amplifier.

### 2.4.1 Differential Structure

Differential topology can immune the common mode signal and prevent any noise that might exist on the power supply impacting the circuit performance. Differential structure, usually add on the transistors with equal load impedance on both sides of the drain. According to superposition, the gain distributed by common-mode and differential-mode could be separated. And the result of CMRR is significant large.

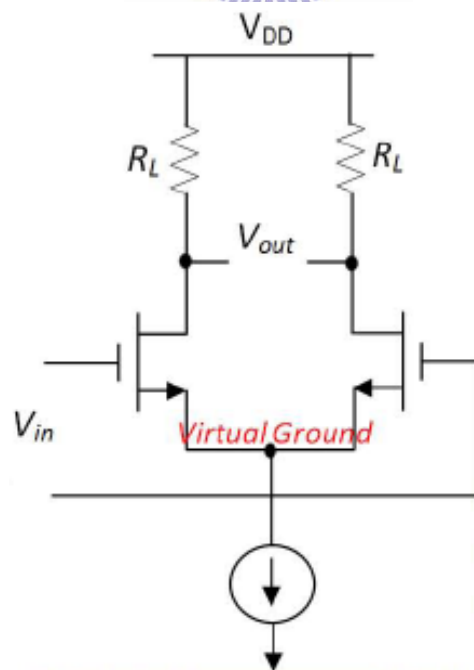


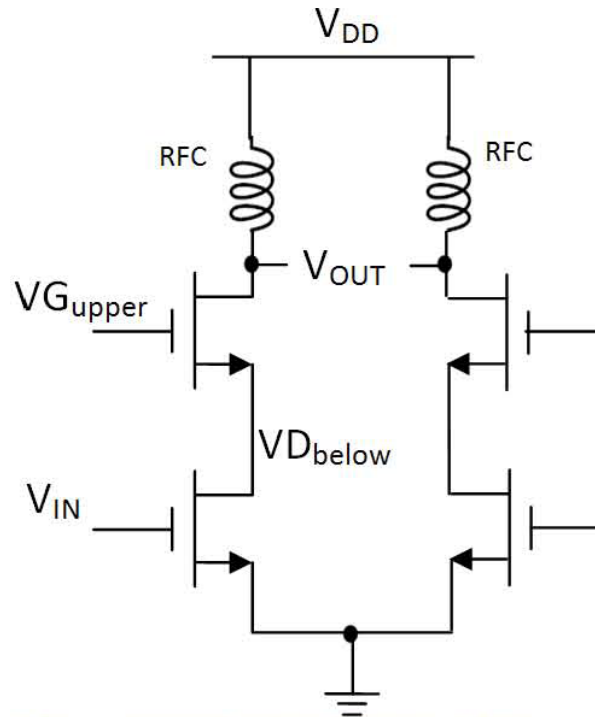
Figure2-5 the differential structure with the tail current source

For the common source amplifier which is shown in figure 2-5, due to the large output impedance of the tail current source, the node common to the sources of the two transistors acts like a virtual ground for differential signal and a virtual open-circuit for common-mode circuits [6].

Owing to the low-resistivity substrate, signal may travel through one block to another block elsewhere on the chip [12]. These signals will show up as a common-mode signal on the substrate terminal of the devices in another block. In order to ensure the impact of those signal is reduced, the implementation of all blocks, especially noise that deal with small signals or those that are extremely sensitive should use differential structure. The current tail offers the same magnitude as single-ended implementation thus each side of differential pair receives half of the original current. Under this situation, each side provides half power of the original single-ended implementation. Although the maximum voltage swing doesn't change the output current become half of the tail current. Summing the powers of each side delivers the full desired power to the load.

#### **2.4.2 Cascode Structure**

The cascade topology is generally used in amplifiers with differential structure. This structure successfully enhances the output resistance comparing to single-transistor gain stage. Besides, the cascode configuration also reduces the impact of Miller effect and enhances the isolation of amplifier that makes impedance matching getting easier.



**Figure 2-6 The cascode structure**

In other words, there is no direct connection between the output node and the input node. This is extremely beneficial in the design of a power amplifier, as the impact of oxide breakdown is greatly reduced. If the bias of the gate of the cascode device is set appropriately, the maximum stress on the oxide of the cascode device is

$$V_{ox(max)} = V_{out(max)} - VG_{upper} \quad \text{Eq.2-8}$$

The  $VG_{upper}$  is the bias voltage on the gate of the cascode upper device. In the case of the single device stage, the maximum oxide stress is

$$V_{ox(max)} = V_{out(max)} - V_{IN(max)} \quad \text{Eq.2-9}$$

This places a severe limitation on the available output voltage swing. In the case of the cascode structure, the oxide stress on the lower device is now limited to

$$V_{ox} = VD_{below} - V_{IN} \quad \text{Eq.2-10}$$

That may cause some problems, depending on the voltage excursion of the cascode node voltage. As stated earlier, the maximum stress on the oxide occurs when the input voltage and the drain voltage getting maximum value.

The cascode node voltage achieves its' maximum value when the minimum of input signal provided and the transistors shut off. There is no current flow into upper device so does the lower device has no charging to the drain capacitance. Therefore, the maximum voltage on the cascode node will be limited to

$$VD_{below(max)} = VG_{upper} - V_t \quad \text{Eq.2-11}$$

The maximum voltage stress across the oxide of the lower device is

$$V_{ox(max)} = VG_{upper} - V_t - V_{in(min)} \quad \text{Eq.2-12}$$

That is a much more reasonable limit than in the single-ended case. The maximum output voltage is now increased to

$$V_{out(max)} = VG_{upper} + V_{ox(max)} \quad \text{Eq.2-13}$$

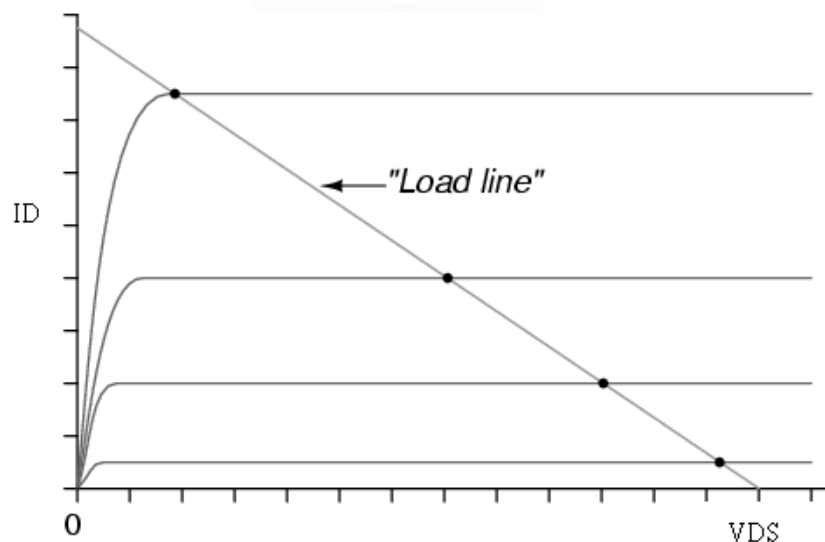
Where  $V_{ox(max)}$  is the maximum voltage the oxide can sustain without damaging the oxide. It is apparent that the maximizing the bias voltage of the cascode device will allow for the cascade device will allow for the largest possible output swing, reducing the amount of current that needs to be drawn from the supply in order to deliver required output power, which can lower down the current inducing hot effect. Furthermore, the smaller the sizes of the output devices, the lesser the pre-amplification stages must provide in order to deliver the required output power [13].

## Chapter III

### Design Theories of Two Stages Power Amplifier

#### 3.1 The Concept of Power Amplifier Circuit Design

For power amplifier circuit design, given the required output power and linearity requirement, therefore the transistors are sized to provide the necessary load gain. Load-line theorem can be used to approximately estimating the optimum impedance and transistor sizes. Parallel enough fingers of transistors to achieve the power goal.

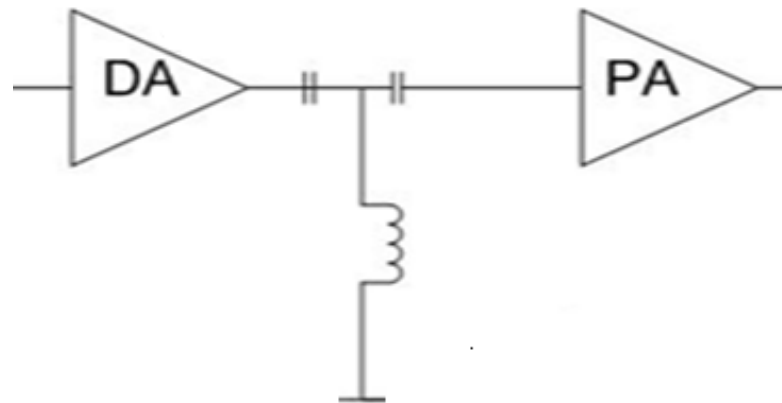


**Figure 3-1 load-line diagram**

The cascode structure we have introduced in chapter 2.4.2 can provide about double value of  $V_{DS}$  will not changing the optimum load impedance because of the upper transistor is nothing but a source follower. In this reason the load line should not become flat by enhancing the maximum sustain voltage.

The stability is also a very important issue to power amplifier, when the transistor numbers are large to offer enough current and get enough output power, the gate resistance is lower down and the input impedance will easy to become negative and lead to oscillate. The stability factor should larger than one and so does the mu factor to make sure the power amplifier is stable. Usually, we will add an RC parallel circuit or using source degeneration method to improve the stability.

In order to transducer the max output power for two stage power amplifier adding a matching network to do the conjugate matching between the load resistance and second stage optimum impedance is necessary. The inter-stage matching has the same situation doing conjugate matching between the second stage input impedance and first stage optimum impedance. In order to avoiding dc disturbance between two stages therefore the inter-stage matching is adopted by T model.



**Figure 3-2 two stage power amplifier with inter-stage matching**

Apparently, for decreasing the input reflection the impedance matching network between source load and first stage input impedance is also required, the lesser coefficient of  $S_{11}$  the smaller loss when input



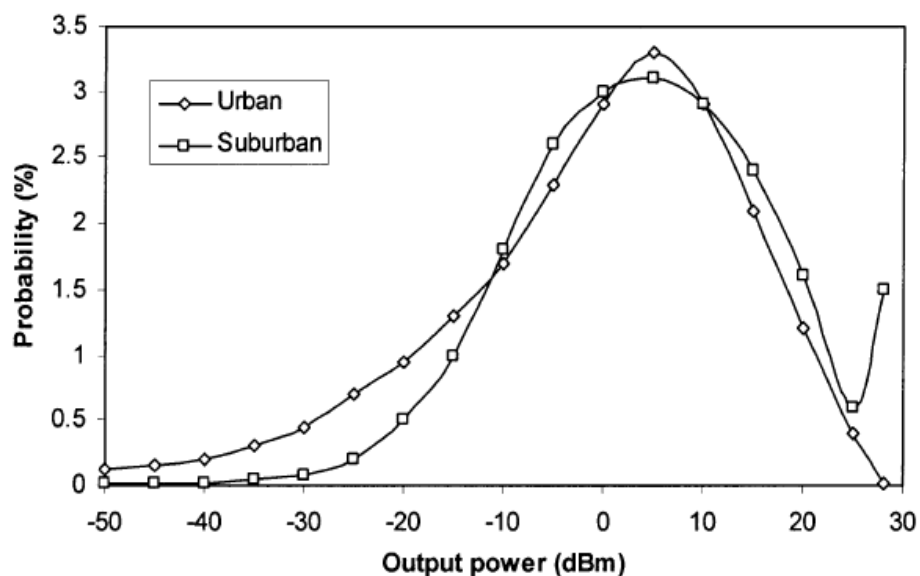
signal transmit to the main circuit.

### 3.2 The Concept of Power Amplifier PAE Enhancement at Power

#### Back-off

The saturation power is a very important index in power amplifier, the larger the saturation power the farer communication distance it provided.

However, one inherent problem of power amplifier is that conventional PA designs achieve maximum efficiency only at a single power level, around the peak output power. As the power is back off from the peak, the efficiency drops sharply. The need of conserving battery power and to mitigate interference to other users necessitates the transmission of power levels well below the peak output power. Transmitters only use peak output power when absolutely necessary.



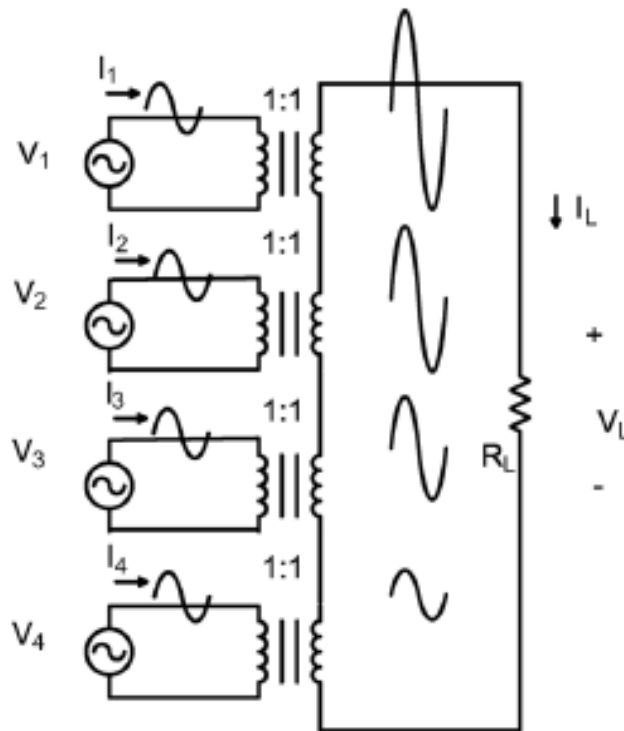
**Figure 3-3 probability curves for transmit power level in urban and suburban environment (IS-95CDMA) [15]**

Dynamic Load Modulation is an attractive approach to enhance the efficiency that we can see from figure 3-4. At the peak power, every individual amplifier is on. Now the load, output swing of each active amplifier and RF power seen by each amplifier is:

$$R = \frac{1}{4} \cdot R_L \quad \text{Eq.3-1}$$

$$V_{\text{output}} = A \cdot V_{\text{input}} = g_m \cdot \frac{1}{4} \cdot R_L \cdot V_i = V_o \quad \text{Eq.3-2}$$

$$P_{\text{peak}} = N \cdot P_{\text{unit\_peak}} = 4 \cdot \frac{1}{2} \cdot \frac{V_o^2}{\frac{1}{4} R_L} = 8 \frac{V_o^2}{R_L} \quad \text{Eq.3-3}$$



**Figure 3-4 conceptual diagram of transformer based power combining amplifier at peak power mode [16]**

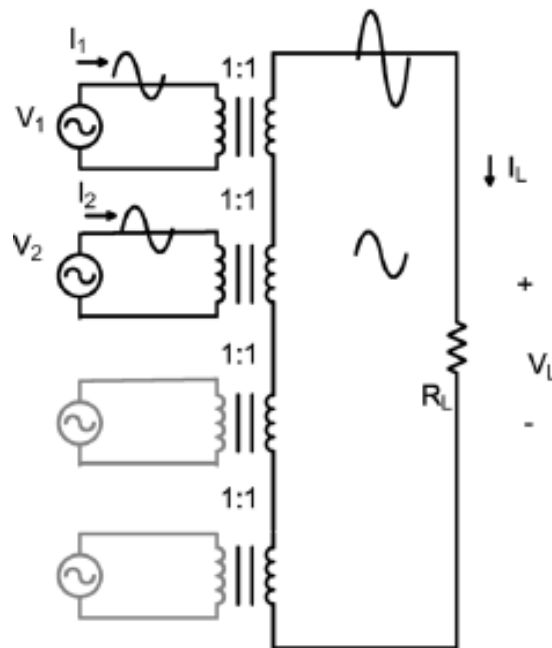
As peak output is not need, input drive is reduced to lower output power. When power is 2.5dB back off, input swing reduced to  $3/4 \cdot V_i$ . As

a result, the output swing of each individual amplifier is  $3/4 \cdot V_o$ . Therefore, the efficiency of each amplifier as well as that of the power combined amplifier drop rapidly. However, if one amplifier is turned off, efficiency could be greatly enhanced. When the operating power amplifier numbers drop to three then the load, output swing of each active amplifier and RF power seen by each amplifier is:

$$R = \frac{1}{3} \cdot R_L \quad \text{Eq.3-4}$$

$$V_{\text{output}} = A \cdot V_{\text{input}} = g_m \cdot \frac{1}{3} \cdot R_L \cdot \frac{3}{4} V_i = V_o \quad \text{Eq.3-5}$$

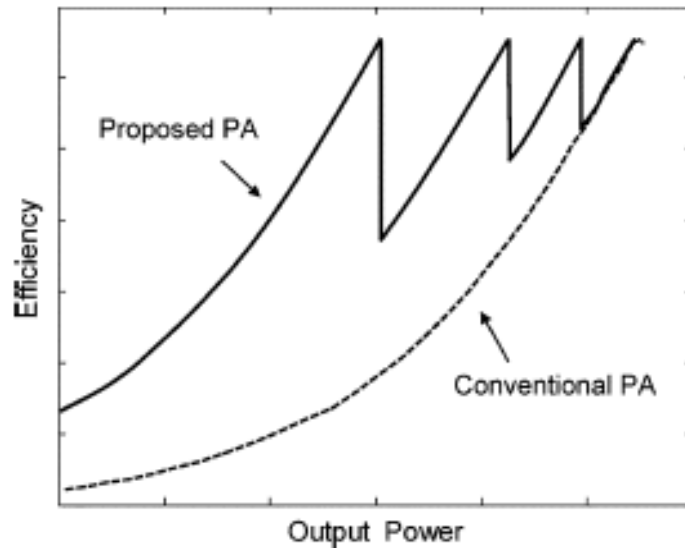
$$P_{\text{out}} = N \cdot P_{\text{unit\_peak}} = 3 \cdot \frac{1}{2} \frac{V_o^2}{\frac{1}{3} R_L} = \frac{9}{2} \frac{V_o^2}{R_L} = \frac{9}{16} P_{\text{peak}} \quad \text{Eq.3-6}$$



**Figure 3-5 conceptual diagram of transformer based power combining amplifier at power back-off mode [16]**

As shown in figure 3-5, the input signal can be reduced from 2.5dB,

6dB to 12dB power back off that turn off one to three power amplifier individually. And the proposing structure greatly enhanced the efficiency as figure 3-6 shown.



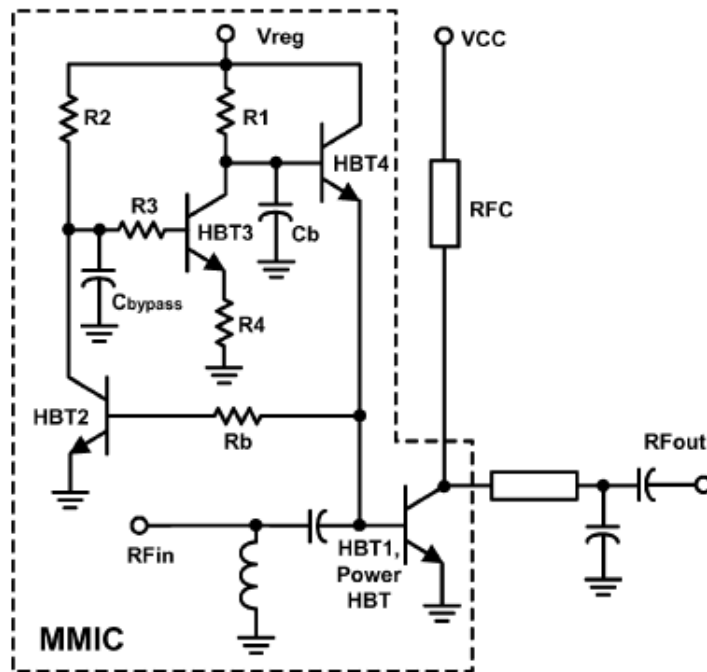
**Figure 3-6 comparison of efficiency between the PA based on proposed power combining transformer and the conventional PA.**

[16]

The idea of adaptively biased power amplifier is to change the device's operating point and improve the power added efficiency. Traditional Class AB power amplifier is difficult to exhibit high efficiency at the low output power level and high linearity at the high output power level. The adaptive bias power amplifier tries to lower down the quiescent current at the low output power level whereas to increase the quiescent current at the output power level.

Figure 3-7 shows the adaptive bias control circuit. Transistor HBT2 will sense the input power and the collector currents increase with the

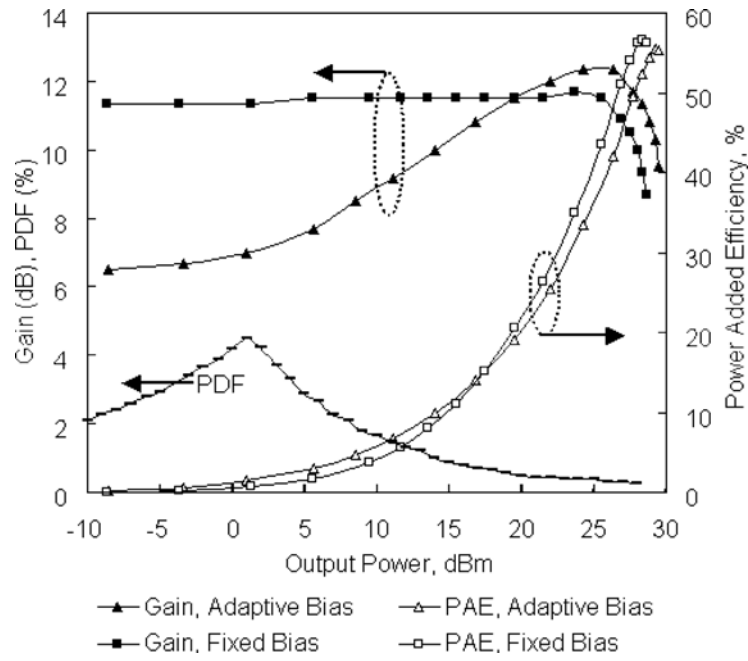
function of the input power. Therefore, the collector current increases so that base voltage of the HBT3 decreased. Then, the decreased  $I_{C3}$  increases the base voltage of the HBT4 such that the emitter current of  $I_{E4}$  decreased and the collector current of HBT1 to decrease. Thus, the quiescent current is a function of input power.



**Figure 3-7 schematic diagram of the adaptive bias control circuit**

[17]

As we can see from the figure 3-8, the gain is 6.5dB for the low output power and increases to 12.3dB at the output power of 24dBm. The power added efficiency is higher than fix bias mode during the output power -3dBm to 17dBm.

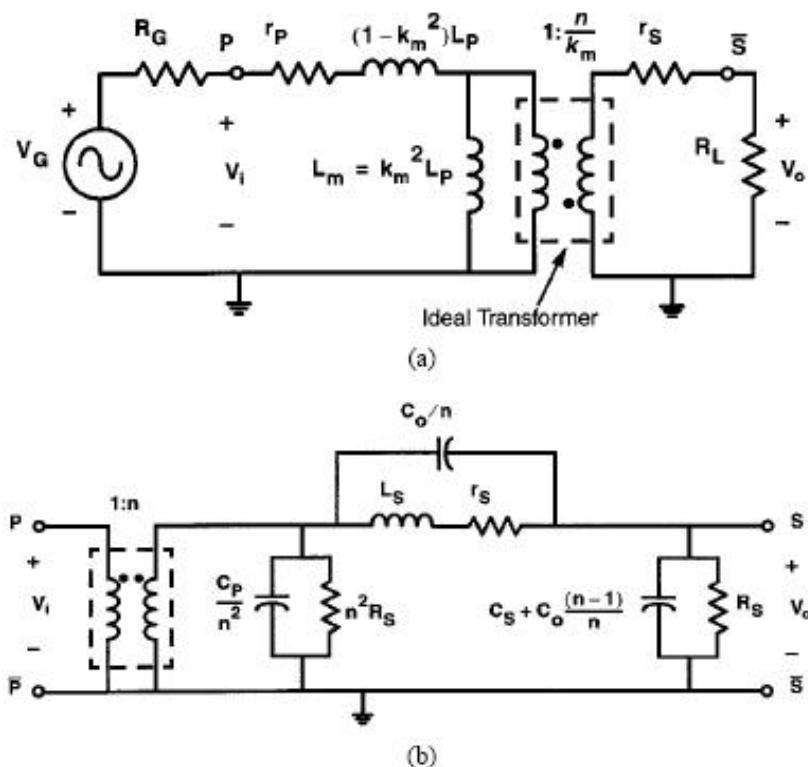


**Figure 3-8 measured gain and power-added efficiency of the power amplifier with the adaptive bias and the fixed bias circuit [17]**



### 3.3 The Design of Output Power Combiner

Typically, the operation of a passive transformer is based upon the mutual inductance between two or more conductors, or windings. By magnetically coupling two inductors, we can create a simple coupling transformer and equivalent circuit model shown in figure 3-9.



**Figure3-9 transformer equivalent model (a) Low frequency model (b) High frequency model [18]**

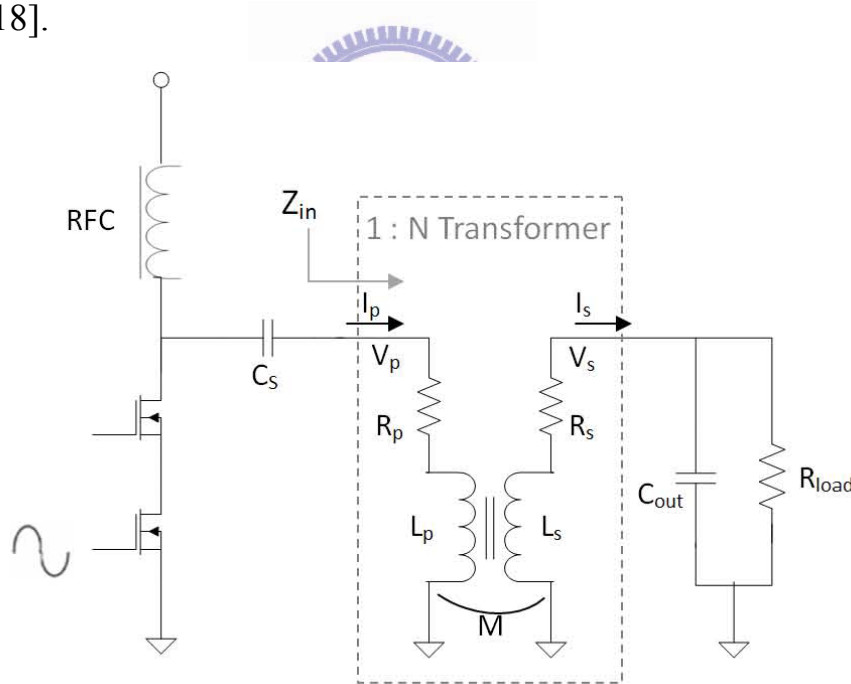
By using transformer, we can try to improve the quality factor of inductor to make the performance better. There are many variable topologies of transformer; it makes circuit design more creative by using monolithic transformer. There are also some special transformer feedback techniques applying in novelty circuit.

$$n = \frac{V_s}{V_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}} \quad \text{Eq.3-7}$$

The parameter of  $L_p$  and  $L_s$  are self-inductances of the primary and secondary loops. The strength of the magnetic coupling between windings is indicated by the  $k$  factor, as

$$k = \frac{M}{\sqrt{L_p L_s}} \quad \text{Eq.3-8}$$

$M$  is the mutual inductance between the primary and secondary windings. The self-inductance of a given winding is the inductance measured at the transformer terminals when all other windings are open circuited [18].



**Figure 3-10 schematic of the cascade PA with a 1: N transformer**

The magnetic-coupled transformer shown in figure 3-10 can be modeled with equivalent series resistors,  $R_p$  and  $R_s$ , and the equivalent net inductance,  $L_p$  and  $L_s$ . Take into the equivalent net inductance,  $L_p$  and  $L_s$ ,



from the primary and secondary winding. Take into the effect of the induced voltage through mutual coupling and neglect the equivalent series resistance, from the KVL can write the matrix from as

$$\begin{bmatrix} V_p \\ V_s \end{bmatrix} = \begin{pmatrix} j\omega L_p & -j\omega M \\ j\omega M & -j\omega L_s \end{pmatrix} \begin{bmatrix} I_p \\ I_s \end{bmatrix} \quad \text{Eq.3-9}$$

$$V_p = Z_{in} I_p = (R_{in} + jX_{in}) I_p \quad \text{Eq.3-10}$$

$$V_s = Z_{out} I_s = I_s / Y_{out} = I_s / (G_{load} + j\omega C_{out}) \quad \text{Eq.3-11}$$

The  $Z_{in}$  is the input resistance and  $R_{load}$  is the output resistance, which is typically 50-Ω. From the Eq.3-10 and Eq.3-11, the input impedance of the transformer is given by

$$Z_{in} = \frac{V_p}{I_p} = R_{in} + jX_{in} = j\omega L_p + \frac{\omega^2 M^2}{Z_{out} \left( 1 + \frac{j\omega L_s}{Z_{out}} \right)} \quad \text{Eq.3-12}$$

Now, rationalization the

$$Z_{in} = j\omega L_p + \frac{\omega^2 M^2}{Z_{out} \left( 1 + \frac{j\omega L_s}{Z_{out}} \right)} = j\omega L_p + \frac{\omega^2 M^2 (Z_{out} - j\omega L_s)}{(Z_{out}^2 + \omega L_s^2)} \quad \text{Eq.3-13}$$

And we can use eq.3-8 into the eq.3-13 as

$$Z_{in} = j\omega L_p + \frac{\omega^2 k^2 L_p L_s (Z_{out} - j\omega L_s)}{(Z_{out}^2 + \omega L_s^2)} \quad \text{Eq.3-14}$$

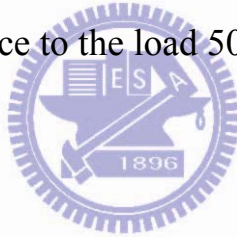
To minimize passive losses in the above equation, and use Eq.3-7

$$Z_{in, opt} = j\omega L_p(1 - k^2) + \frac{k^2}{N^2} R_{load} \quad \text{Eq.3-15}$$

If the magnetic coupling between windings is less leakage of the magnetic flux, and we can write Eq. 3-16 as

$$R_{in, opt} \cong \frac{k^2}{N^2} \cdot R_{load} \quad \text{Eq.3-16}$$

Eq.3-11 shows the correlation between the magnetic coupling and the self-inductance of the primary and secondary windings. We can try to use the relationship Eq.3-16 described to do the output matching. The turn ratio  $N$  of the transformer is the parameter that we have to design to match the optimum impedance to the load  $50\text{-}\Omega$ .



## Chapter IV

### Simulation and Measurement Results

#### 4.1 Proposed Design

As we mentioned at Chapter 3.2, the way of improving adaptive body bias is to modulate the quiescent current. It depends on the required output power, or the unnecessary DC power consumption will be reduced the power efficiency.

BJT can use the method of adjusting the adaptive bias circuit to modulate the power cells' base current and change the power cells' collector current. The only way of changing CMOS transistor is by changing the bias point. So that we try to adjust the body-bias as changing the bias point. As we can see from the Eq.4-1, the threshold voltage increases when the body bias connects to negative bias voltage, therefore the quiescent current will lower down.

$$V_{TN} = V_{TO} + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}) \quad \text{Eq.4-1}$$

In order to sense the different amplitude of input power and change the quiescent current of power amplifier. Rectifier is a way that we usually come up with to modulate the AC signal to DC bias.

Figure 4-1(a) (b) are a conventional voltage doubler rectifier with positive and negative input and the node voltages are marked.

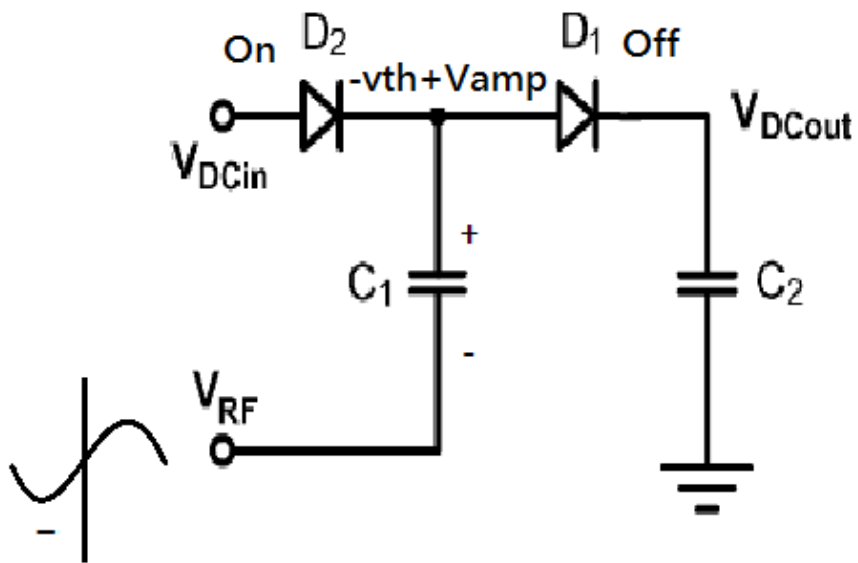


Figure 4-1 (a) conventional voltage doubler rectifier with

negative phase input

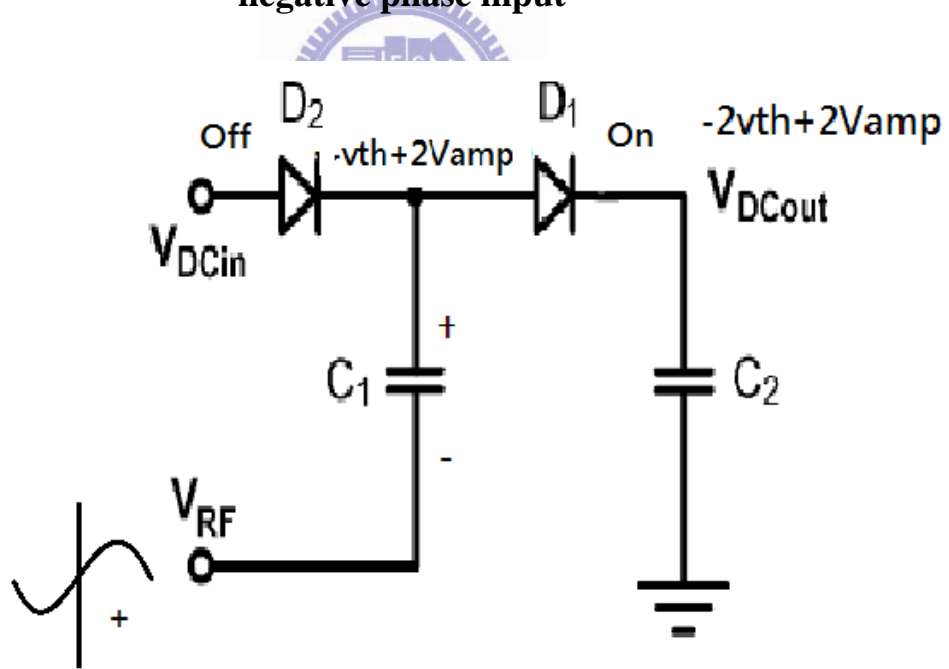
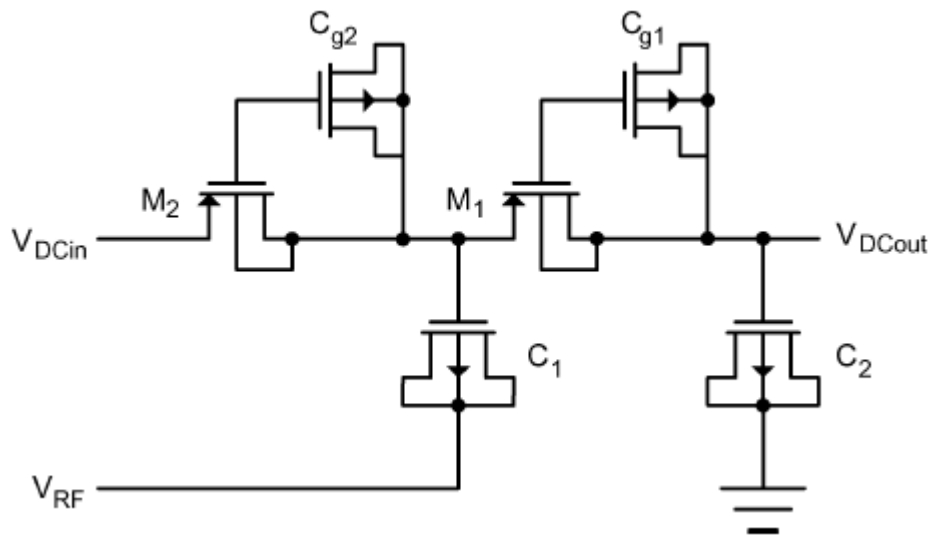


Figure 4-1 (b) conventional voltage doubler rectifier with

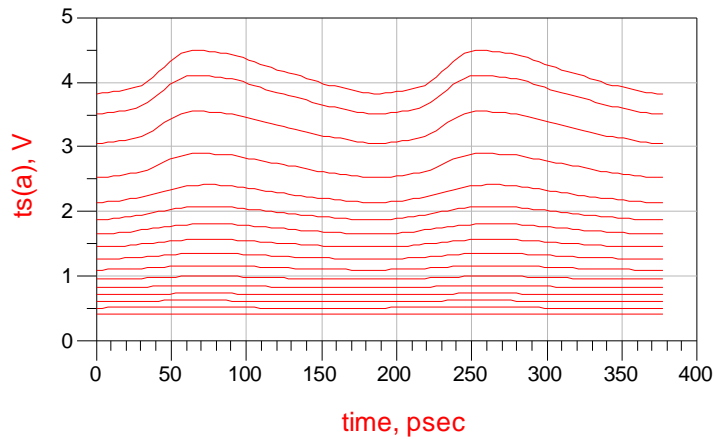
positive phase input

Since the conventional voltage doubler rectifier has  $2V_{th}$  drop that decrease the efficiency of the rectifier. Therefore the floating gate voltage doubler which I implemented in this design can compensate the threshold voltage drop. The gate of the diode-tied transistor and the gate of the MOS capacitor are connected together to form a high-impedance node to trap charges in the floating gate. The charge in the floating gate is therefore fixed which results in a fixed voltage bias across the MOS capacitor. The charges that are trapped inside the floating gate device act as a gate-source bias to passively reduce the effective threshold voltage of the transistor [19].



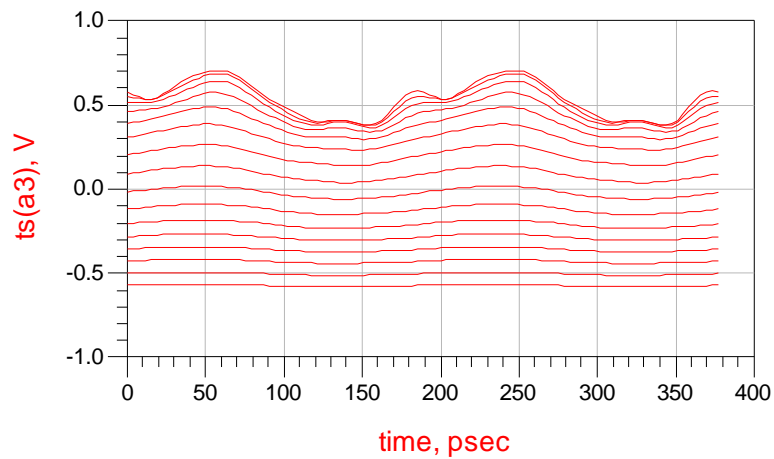
**Figure 4-2 floating gate voltage doubler rectifier [19]**

The input signal change into positive voltage as figure 4-3 and it should be change to negative voltage. Therefore, the negative voltage should add a voltage divider and change the voltage from positive to negative. We implement a NMOS as a voltage divider and bypass capacitor to stable the voltage.



**Figure 4-3 the voltage wave form after signal transform by floating gate voltage doubler rectifier**

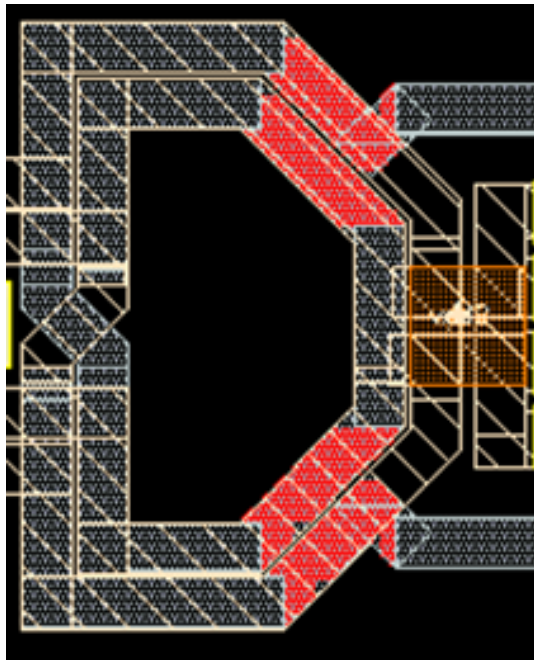
Figure 4-4 shows the voltage waveform modulate by NMOS voltage divider which is very stable when transistor operate at active region with large  $R_{on}$  and the waveform is going to tremble when the transistor operate in triode region.



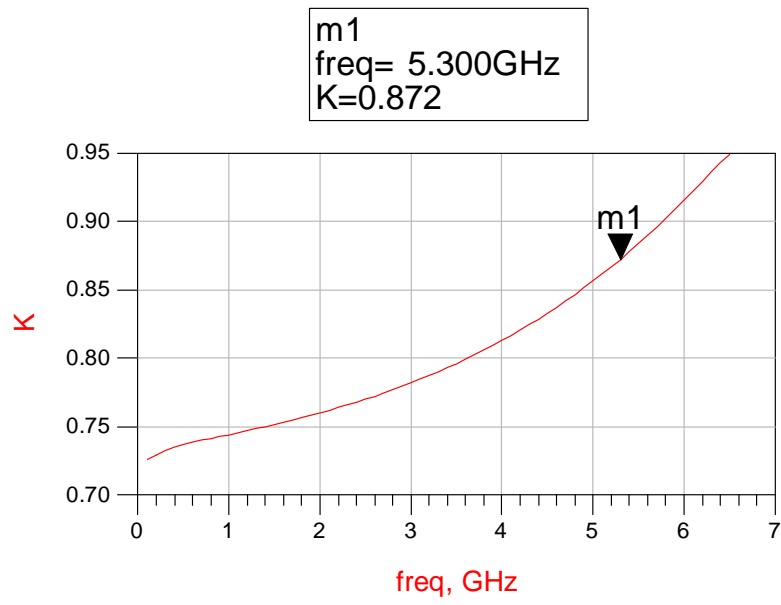
**Figure 4-4 the voltage waveform modulate by NMOS voltage divider**

## 4.2 Output Impedance Matching Network

We have introduced the output impedance matching network at chapter 3.3. The transformer structure was shown as figure 4-5. In order to increase the ability of enduring high current, I try to parallel the primary coil. Besides, using sidewall coupling the coupling factor can't reach that high value which is only about 0.5~0.6. Therefore, I try to overlap primary and secondary coils to increase coupling factor and figure 4-6 displayed the coupling factor increased successfully.



**Figure 4-5 transformer structure**



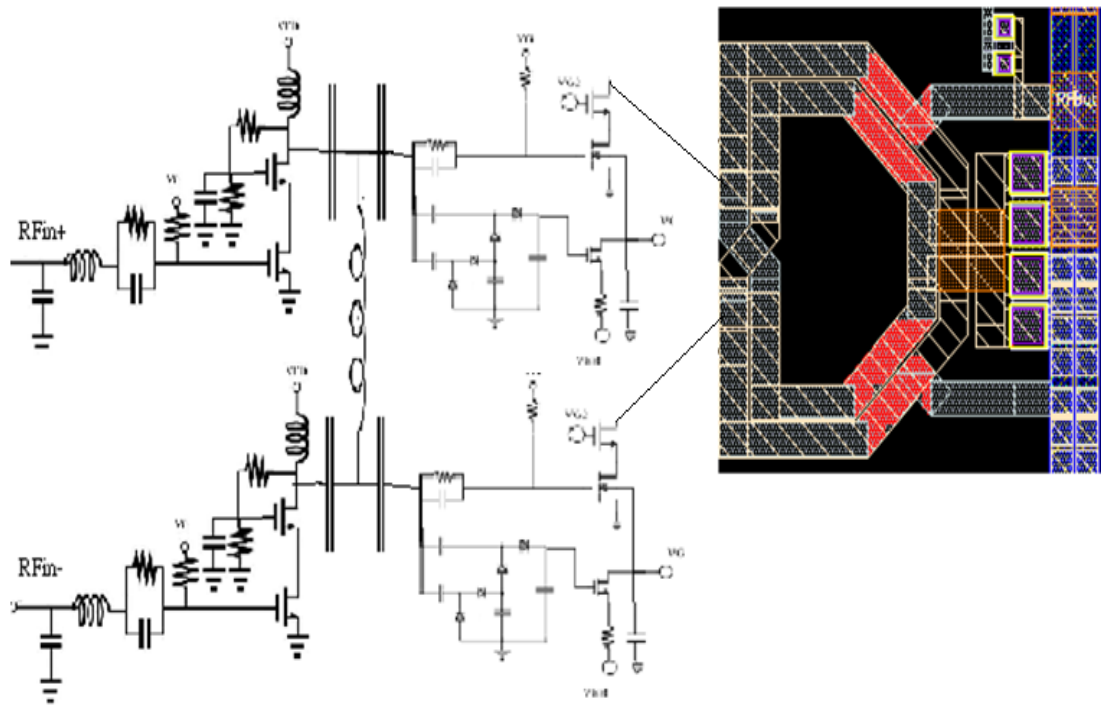
**Figure 4-6 transformer coupling factor**





### 4.3 Simulation Result of Overall Circuit

Figure 4-7 is the proposed power amplifier structure, and it can be separated into two stages. The drive amplifier of the first stage is very important to linearity and gain, the power amplifier of the second stage decides how much power that a PA can transmit.



**Figure 4-7 proposed power amplifier**

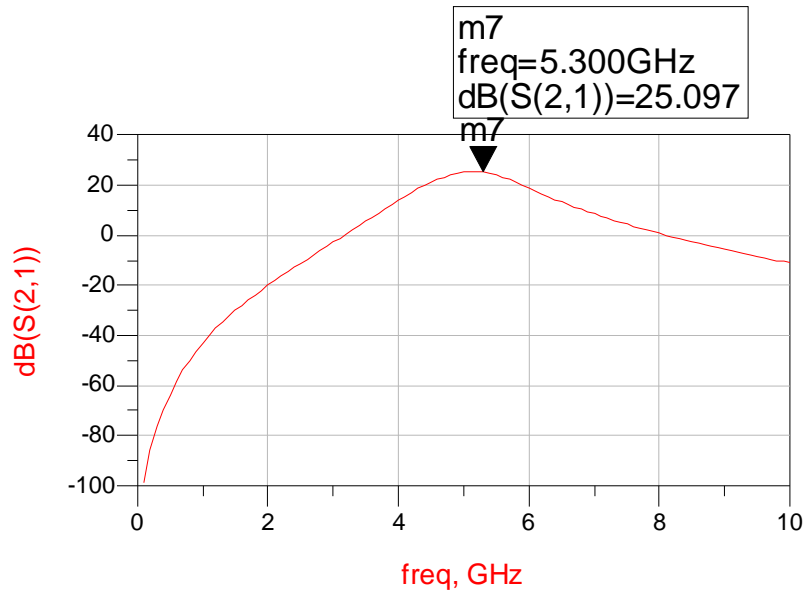


Figure 4-8 pre-simulation gain

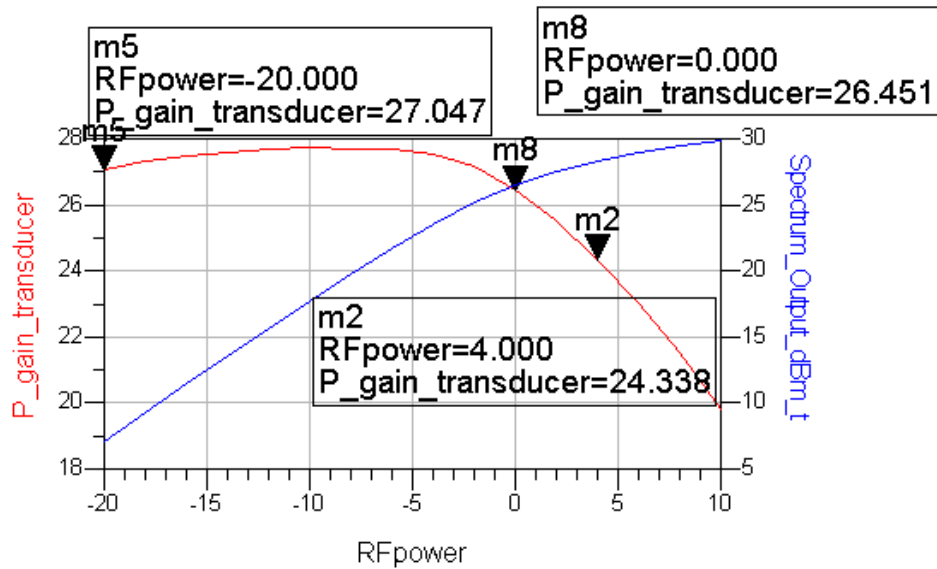
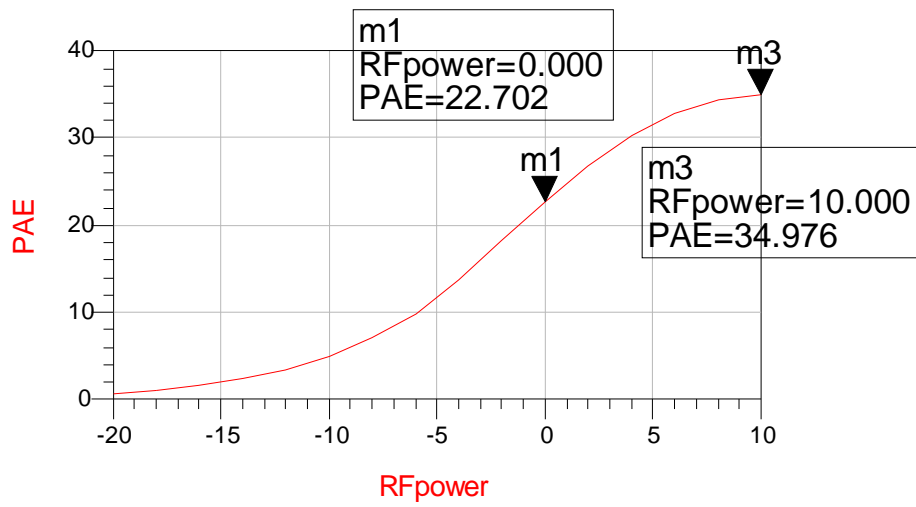
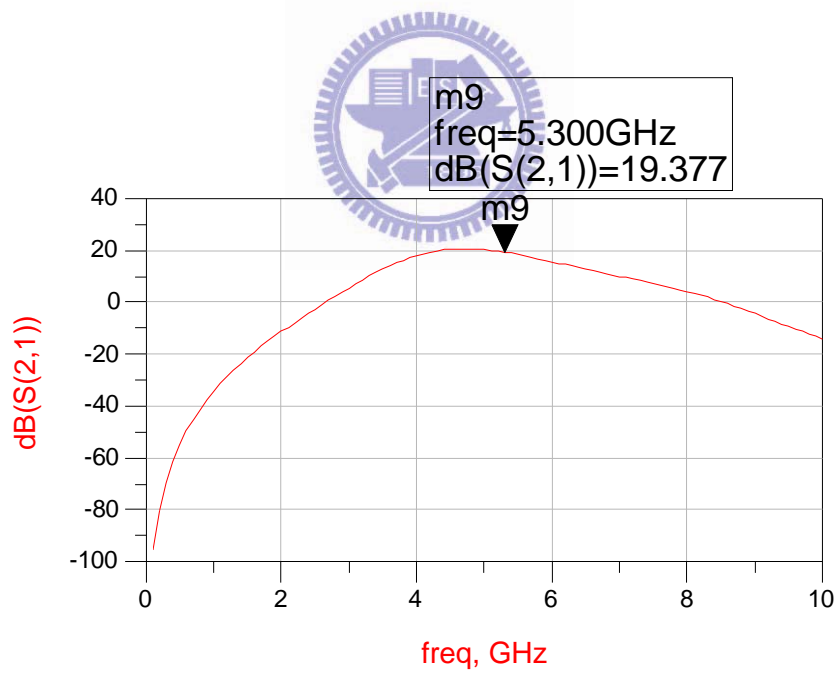


Figure 4-9 pre-simulation transducer gain and output power



**Figure 4-10 pre-simulation PAE**



**Figure 4-11 post-simulation gain**

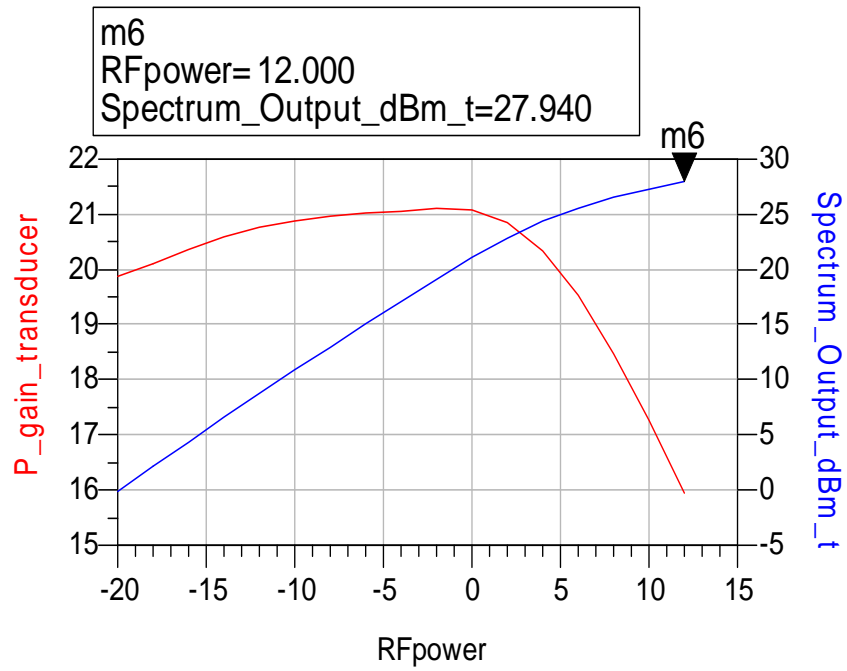


Figure 4-12 post-simulation transducer gain and output power

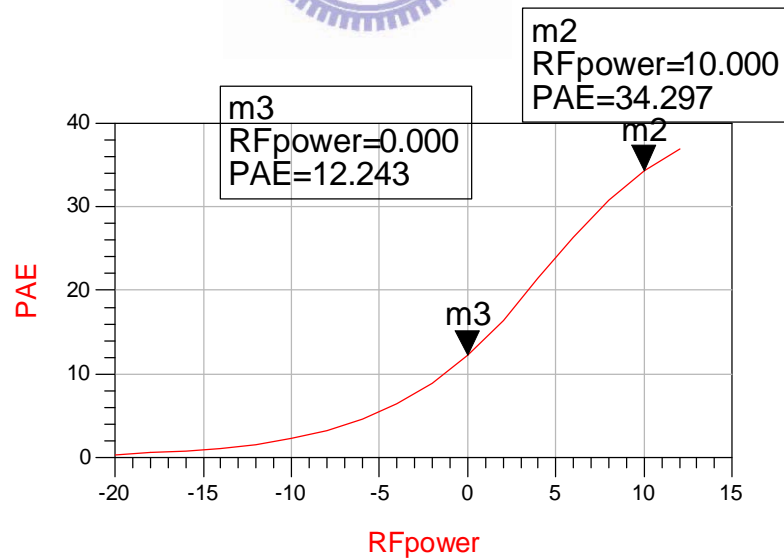


Figure 4-13 post-simulation PAE

**Table 4.1 the comparisons with others literatures**

Ref	process	Freq (GHz)	P <sub>1dB</sub> (dBm)	Max. P <sub>out</sub> (dBm)	Power gain(dB)	PAE (%)	PAE@12dB P <sub>in</sub> back-off (%)
1	0.18um CMOS	2.4	21.4	22.3	10.6	33	10
2	0.18um CMOS	5	20.5	22	12	44	6
3	0.18um CMOS	5.25	21.8	24.1	22	21	11
4	0.13um CMOS	2.4	24	27	17.5	30	9
5	0.25um CMOS	2.45	20	22	11.2	28	4
Pre-sim	0.18um CMOS	5.3	26.45	29.2	25	34.9	22.7
Post-sim	0.18um CMOS	5.3	26	27.94	19.3	34.3	12.2

#### 4.4 Measurement Results

Because of the measurement environment can not set differential signal directly and the loss of the balun is too large that can not be ignored, the S parameter can not measure under this condition. Therefore, I can not get the S parameter measurement results and only received power spectrum picture.

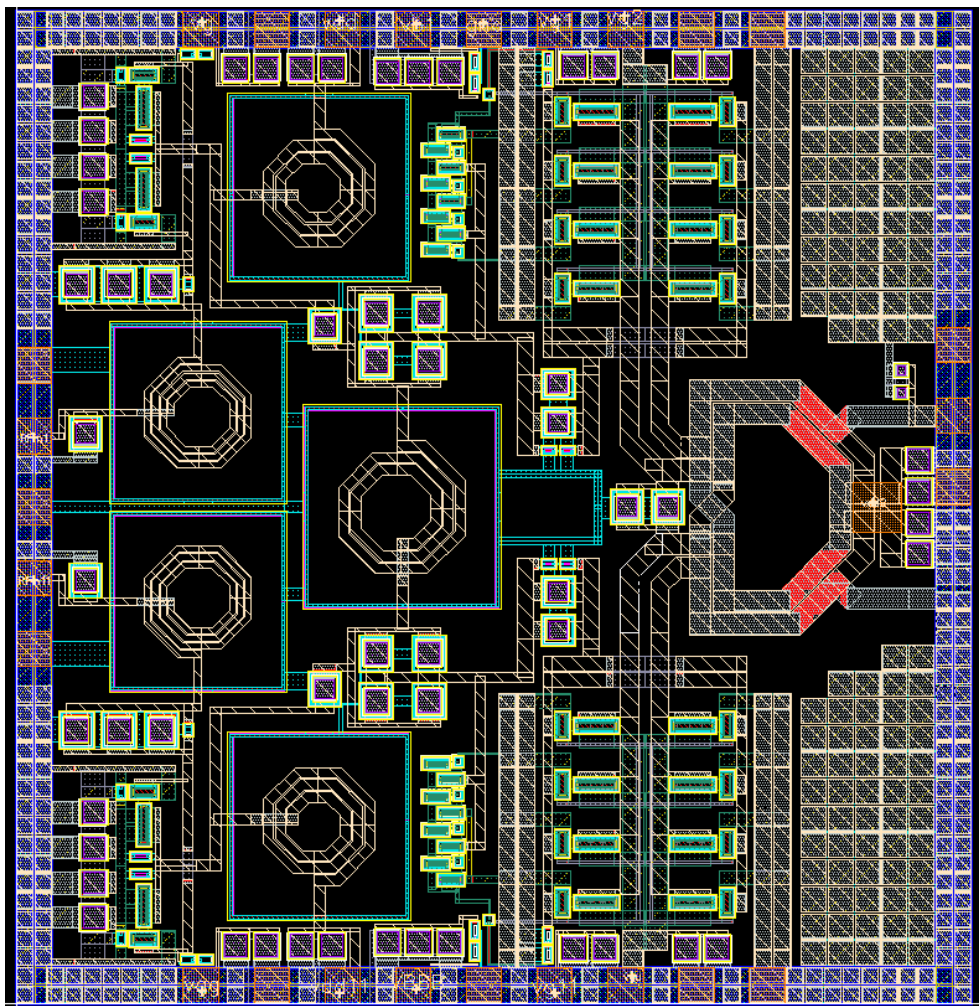
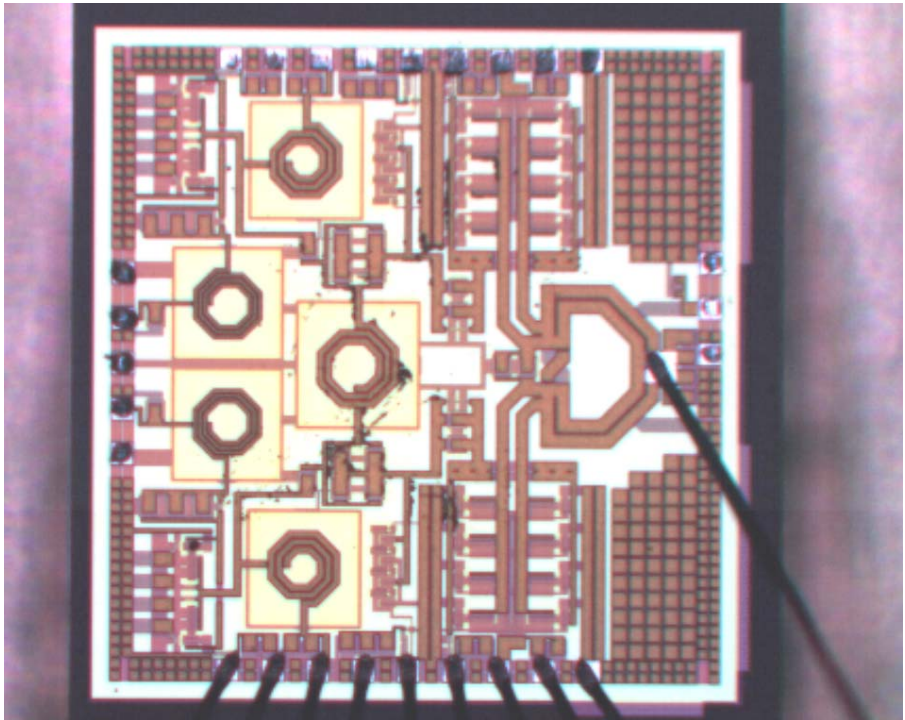
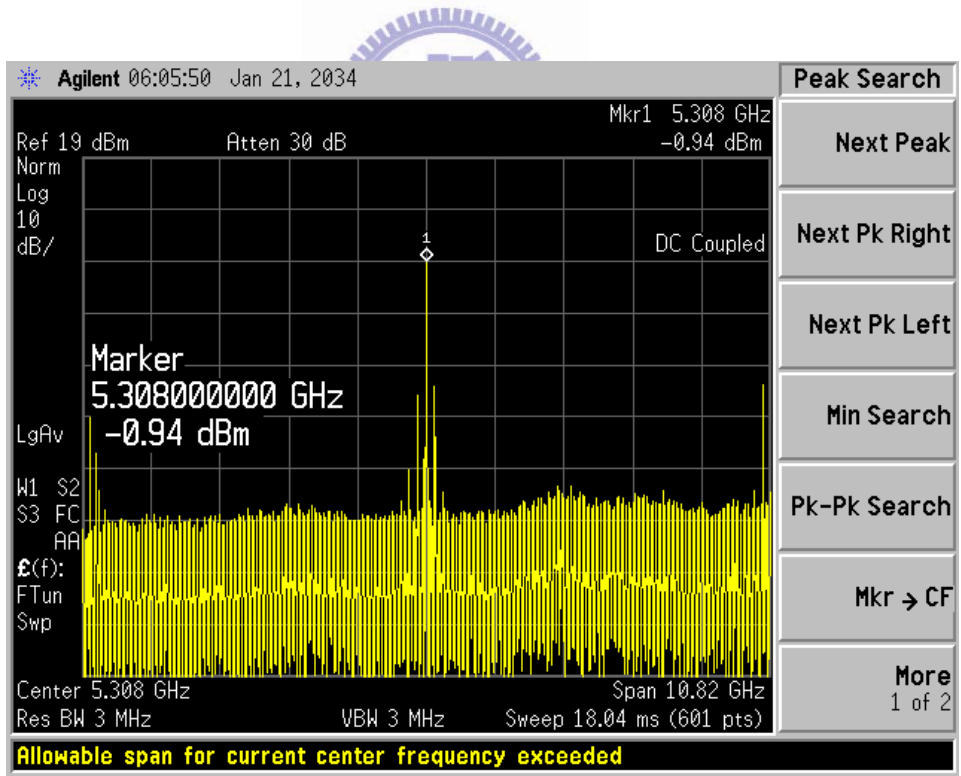


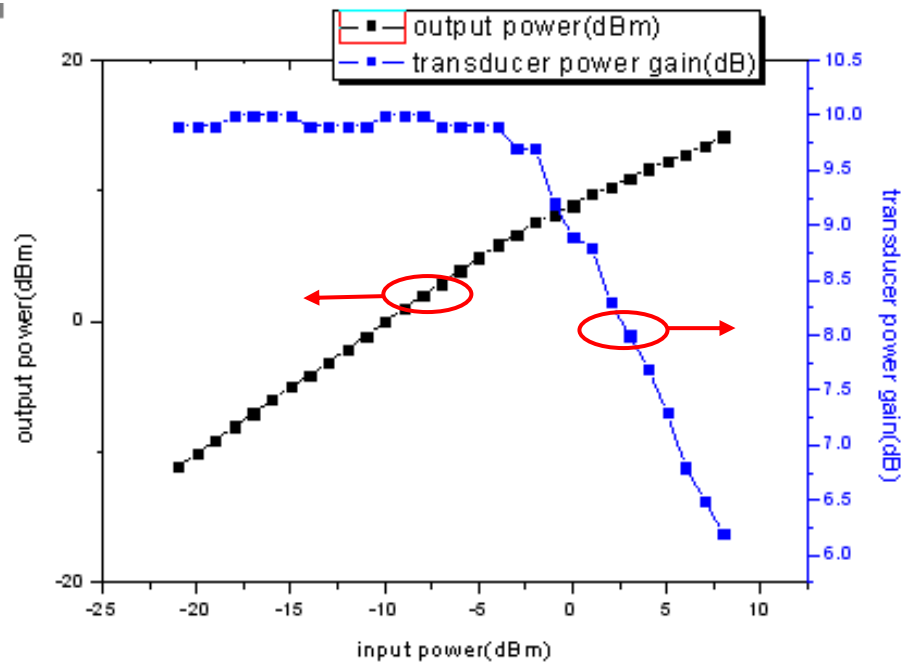
Figure 4-14 Layout



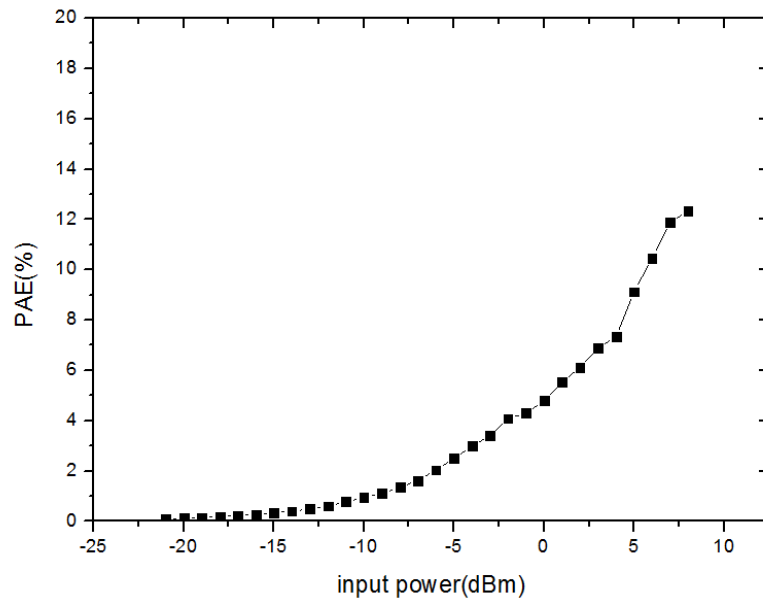
**Figure 4-15 Microphotograph**



**Figure 4-16 Power Spectrum**



**Figure 4-17 Measured Output power and transducer gain**



**Figure 4-18 Measured PAE**

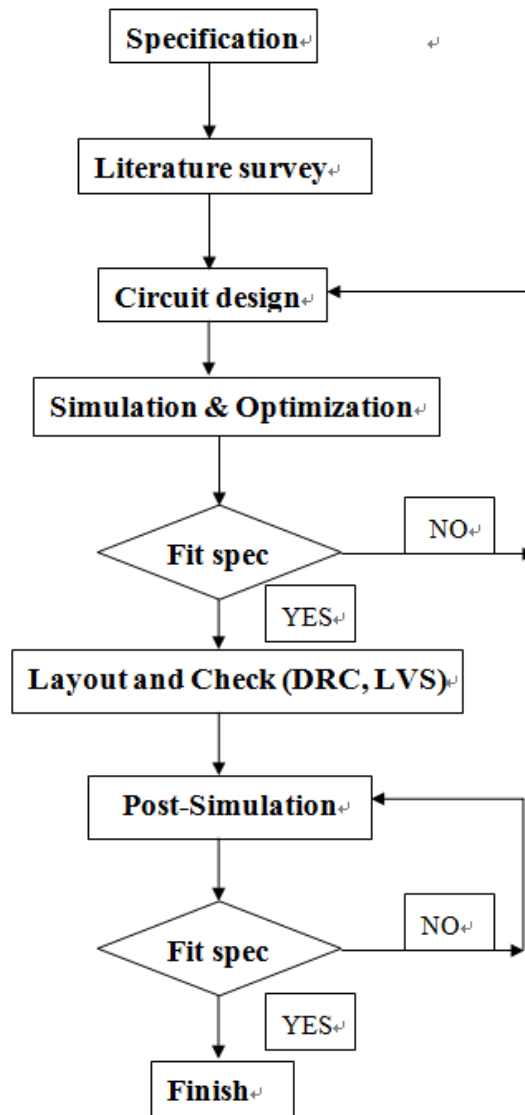


# Chapter V

## Design Flow

### 5.1 Design Flow

The simulation software ADS designer is used to design the circuit. ADS momentum is used to do EM simulation. After the layout of circuit is finished, DRC & LVS & LPE is done to check the correction for the design.



## Chapter VI

### Future Work

#### 6.1 Conclusion and Summary

Although the designed two-stage CMOS class-AB power amplifier exhibits good linearity and maximum efficiency, it still suffers serious efficiency degradation when operated at low output power levels. Therefore, detect the input power level to lower down unnecessary DC power waste can improve the power added efficiency. Sensing the input power by rectifier and using NMOS voltage divider to change positive DC level to negative DC level to control the body bias and then achieve the target of enhancing PAE.

#### 6.2 Future Works

Comparing with pre-simulation that we can find the post-simulation performance decreased a lot. Because of power amplifier has to parallel a lot of transistors to transfer high enough output power and that would increase the difficulty of layout and so does the long connecting metal line will give rise to the extra parasitic RLC decreasing the performance. This power amplifier performance may improve by doing good ground plane such as ground mesh other than strip line to decrease the inductance.

Using asymmetric device to increase the break down voltage and change differential structure to single ended structure to reduce the loss of non-ideal transformer will probable increase PAE.

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