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應用鎳矽化物與鍺於新穎結構複晶矽薄膜電晶體之研究

Applications of Ni-Silicidation and Germanium for Novel Structures of Polycrystalline Silicon Thin-film Transistors

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摘　　要

此論文製作多種高效能新結構複晶矽薄膜電晶體，研究鎳矽化物與鍺在閘極工程、源極/汲極工程、通道結晶與非揮發記憶體上之應用。

首先我們提出一種新自我對準蕭特基(Schottky)位能障源極與歐姆接觸(ohmic contact)基極結構(SSOB)，我們使用不對稱 p 型接面源極 / n 型接面汲極結構與自我對準鎳矽化物來形成蕭特基位能障源極與歐姆接觸基極結構，此結構能有效抑制複晶矽薄膜電晶體浮接基體效應(Floating-Body Effect)。和傳統複晶矽薄膜電晶體相比，實驗結果顯示此蕭特基位能障源極與歐姆接觸基極結構之複晶矽薄膜電晶體(SSOB-TFTs)具有較高的輸出阻抗(output resistance)、較少的臨界電壓變化(threshold voltage variation)、改善的次臨界特性(subthreshold characteristics)和較大的崩潰電壓(breakdown voltage)。然後我們首次成功發展出具完全自我對準鎳矽化物(fully Ni-salicided)於源極/汲極和閘極之 n 型通道與 p 型通道複晶矽薄膜電晶體(FSA-TFTs)，和傳統複晶矽薄膜電晶體相比，實驗結果顯示此完全自我對準鎳矽化物(fully Ni-salicided)於源極/汲極和閘極之 n 型通道與 p 型通道複晶矽薄膜電晶體(FSA-TFTs)具有較高的導通/關閉電流比(Ion/Ioff

current ratio)、改善的次臨界特性(subthreshold characteristics)、較少的臨界電壓下降(threshold voltage roll-off)、較低的源極/汲極寄生電阻(parasitic S/D resistance)、較高的閘極電容和較大的場效應電子遷移率(field-effect mobility)。另外我們亦研究發展出新穎鎳矽化物引發橫向結晶技術於對稱式垂直通道複晶矽薄膜電晶體(NSILC-VTFTs)，兩階段的鎳矽化物引發橫向結晶技術(NSILC)包含第一階段:爐管 500°C 12 小時退火和第二階段的 700°C 60 秒快速熱退火(RTA)，此新穎結晶技術可以加強結晶大小、改善結晶品質並抑制鎳金屬的累積污染。元件製作完全無經過氨電漿後處理，此新穎鎳矽化物引發橫向結晶技術於對稱式垂直通道複晶矽薄膜電晶體(NSILC-VTFTs)具有陡峭的次臨界擺動(subthreshold swing)和相當高的場效應電子遷移率(field-effect mobility)。

接著我們首次成功發展製作出自我對準堆疊矽/鍺 T 型閘極結構之複晶矽薄膜電晶體(Si / Ge T-gate TFTs)，此新結構之閘極靠源極/汲極兩邊具有較厚之閘極氧化層，此設計能有效地降低汲極的垂直與橫向電場而不需要額外的光罩、輕摻雜汲極(lightly doped drain)、間隙壁(spacer)或副閘極(sub-gate)等製程和結構。和傳統複晶矽薄膜電晶體相比，實驗結果顯示此堆疊矽/鍺 T 型閘極結構之複晶矽薄膜電晶體(Si / Ge T-gate TFTs)具有較低的關閉電流(off-state leakage current)、較高的導通/關閉電流比(Ion/Ioff current ratio)與較飽和的輸出特性(output characteristics)。

在論文的最後，我們成功發展製作出具鍺奈米微晶粒之非揮發複晶矽薄膜記憶體(poly-Si TFT nonvolatile Ge-NCs memories)，此鍺奈米微晶粒是利用低壓化學氣相沉積系統在 370°C 下直接沉積在氧化層上來完成。此外，我們應用適當的浮接基體效應(Floating-Body Effect)來提高寫入/抹除效率。實驗結果顯示此鍺奈米微晶粒之非揮發複晶矽薄膜記憶體(poly-Si TFT nonvolatile Ge-NCs memories)具有高的寫入/抹除效率、長的電荷儲存持久性、低的閘極和汲極干擾與良好的寫入/抹除忍受力。

Applications of Ni-Silicidation and Germanium for Novel Structures of Polycrystalline Silicon Thin-film Transistors

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ABSTRACT

In this thesis, applications of Ni-silicidation and Germanium in gate engineering, source/drain engineering, channel crystallization and nonvolatile memories for fabricating high performance new structures of polycrystalline silicon thin-film transistors (poly-Si TFTs) have been investigated.

First, we have developed a new self-aligned Schottky barrier source and ohmic body contact (SSOB) method that can effectively suppress the floating-body effect in poly-Si TFTs. Experimental results show that the SSOB-TFTs give higher output resistance, less threshold voltage variation, improved subthreshold characteristics, and larger breakdown voltage compared with conventional TFTs.

Second, the n-channel and p-channel fully Ni-self-aligned silicided (fully Ni-salicided) source/drain and gate poly-Si TFTs (n-channel and p-channel FSA-TFTs) have been successfully are successfully developed and fabricated for the first time. Experimental results show that the FSA-TFTs give increased Ion/Ioff current ratio, improved subthreshold characteristics, less threshold voltage roll-off, low parasitic

S/D resistance, high gate capacitance and larger field-effect mobility compared with conventional TFTs.

Next, the novel symmetric vertical channel poly-Si TFTs fabricated by Ni-silicide induced lateral crystallization technology (NSILC-VTFTs) are successfully developed and demonstrated. Two step NSILC (1_{th} step: 500°C, 12hr and 2_{th} step: RTA 700°C, 60-sec; without NH_3 plasma treatment) has been introduced to enhance the grain size and improve the crystal integrity through secondary crystallization. The NSILC-VTFTs after two step NSILC treatment show a steep subthreshold swing (S.S.) of 180 mV / dec and max field effect mobility μ = 553 cm^2 / V-s with L_{eff} = 0.6μm and gate oxide = 500Å.

Then, we have successfully developed and fabricated the self-aligned Si / Ge T-gate poly-Si thin-film transistors (Si / Ge T-gate TFTs) with a thick gate oxide at the gate edges near the source and drain for the first time. The thick gate oxide at the gate edges effectively reduces the drain vertical and lateral electric fields without additional mask, lightly doped drain (LDD), spacer, or sub-gate bias. Experimental results show that the Si / Ge T-gate TFTs have low off-state leakage currents, improved Ion / Ioff current ratio, and more saturated output characteristics compared with conventional TFTs.

Finally, we have successfully developed and fabricated the poly-Si thin-film transistor (poly-Si TFT) nonvolatile Ge nanocrystals (Ge-NCs) memories for the first time. The pure Ge-NCs trapping layer was directly deposited by low-pressure chemical vapor deposition (LPCVD) at 370°C. In addition, a programming/erasing scheme adopting appropriate floating body effect was proposed. Results show that the new poly-Si TFT nonvolatile Ge-NCs memories have high programming/erasing efficiency, long charge retention time, less gate and drain disturbance, and good endurance characteristics.

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Chapter 1

Introduction

1.1 Overview of Polycrystalline Silicon Thin-Film Transistors

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many potential applications including pixel driving elements of active matrix organic light emitting diode (AM-OLED), and integrated peripheral driving circuits and addressing elements of active-matrix liquid crystal displays (AMLCDs) [1.1]-[1.4]. Recently, poly-Si TFTs are very attractive for system on top of the panel (SOP) as devices performances improve further [1.5]. The degree of circuit integration will continue to increase as device performances improve further. The entire system will include memories, such as SRAM and nonvolatile FLSAH Memories, solar cells, and touch sensors as well as driver circuits for AMLCDs [1.6]-[1.8].

Poly-Si TFTs have the potential advantages of silicon-on-insulator (SOI) MOSFETs such as simple fabrication process, good device-to-device isolation, high circuit density, and high device performance as well as the possibility to be applied in vertical 3-D integration. Poly-Si TFTs technology has been receiving more attention because it is a promising mean of achieving 3-D integration, which has been utilized in various 3-D circuits [1.9]-[1.11]. In addition, poly-Si TFTs have been used as the driving devices for pixel, if they can have nonvolatile memories function, then they are very attractive for 3D integration of active devices and SOP application in the future.

However, grain boundaries of poly-Si material cause trap and tail states which put strong influences on device characteristics including an increase in threshold voltage (V_{TH}), decrease in mobility, increase in off-state leakage current, decrease in on-state current, poor subthreshold characteristics and degradation in device reliability[1.12] [1.13]. The trap states in the grain boundaries is though to be associated with the presence of dangling and strained bounds [1.14] To solve these problems, some crystallization methods have been introduced to enlarge the grain size. Poly-Si thin film with large crystalline grains can be obtained using a variety of techniques: rapid thermal annealing (RTA) [1.15], solid phase crystallization (SPC) [1.16], laser crystallization (LC) [1.17] and the relatively new metal-induced lateral crystallization (MILC) [1.18]-[1.20] of amorphous silicon (a-Si). Because crystallization of poly-Si channel plays a main role in carrier mobility and uniformity of poly-Si channel, a robust crystallization method is required for poly-Si TFTs in future various applications.

Moreover, these traps also enhance valence-band carriers jump to conduction band via trap-assisted thermionic emission or trap-assisted thermionic field emission, resulting in large leakage current even under off-state operation [1.21], [1.22]. In order to increase the reliability and reduce the leakage current, poly-Si TFTs with offset gated, lightly doped drain (LDD), gate-overlapped LDD, floating gate spacer, air cavities, or field-induced drain (FID) structures have been suggested to reduce the electric field near the drain [1.23]-[1.29].

In the thin-film transistors, the output characteristics exhibit an anomalous increase of current in the saturation regime, often called “kink” effect due to an analogy with silicon-on-insulator (SOI) devices [1.30]-[1.32]. This phenomenon can be attributed to the floating-body effect [1.33] and the avalanche multiplication enhanced by grain boundary-traps [1.31]. In the floating-body thin-film devices, the

improved parasitic BJT effect can be achieved by using deep salicidation and fully silicided source/drain structure [1.34], [1.35]. Several structures such as lateral body terminal (LBT) [1.36], low-barrier body-contact (LBBC) [1.37], and Schottky body contact [1.38] have been reported in order to reduce the kink current.

With the increasing demand for portable systems, it is desirable to have high performance integrated circuits with high integration density, low power consumption, and low voltage operation. Traditionally, this has been achieved by device scaling. However, with the current state-of-the-art technology, the achievable integration density using a conventional approach has almost reached its saturation point. In order to provide a revolutionary breakthrough in circuit compactness, three-dimensional (3-D) VLSI technology has become an important topic in research [1.11]. In order to apply poly-Si TFTs in the 3D integration of active devices and SOP application in the future, nonvolatile memories function in poly-Si TFTs has become an important topic in research. Recently, nonvolatile memory devices using Ge, Si and metal nanocrystals (Ge-NCs, Si-NCs and M-NCs) as floating gate (FG) have been widely studied because of its excellent memory performance and high scalability. Some methods to form various NCs have been introduced in past including the thermal annealing of trapping materal and dielectric mixture, the oxidation of SiGe or SiM_X and Si or Ge ion implantation [1.39]-[1.41].

In summary, the technologies of poly-Si TFTs will become more and more important in future applications including 3D integration of active devices and SOP. More researches investigate the related new technologies and underlying mechanisms in thin-film devices with scaling down dimension are worthy to study. Various materials will be applied for fabricating high-performance thin-film devices.

1.2 Applications of Metal-Silicidation in Poly-Si TFTs

Recently, metal-silicidation procedures have been widely used in VLSI technology. These metal-silicides, such as Ti, Co, Pt, and Ni, have been introduced into integrated circuits for many processes properties including low resistivity, good adhesion, low contact resistance, low contamination to devices, no metal-compound formation, minimum silicon consumption, ease of pattern definition, high barrier height for Schottky devive applications [1.42].

It is well known that nickel monosilicide (NiSi) has several advantages over titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$) [1.43], [1.44]. These advantages include a low thermal budget. NiSi is typically formed between 400 ^{o}C and 600°C, as compared to above 800°C for a low-resistance $TiSi_2$ [1.43]. The resistance of the narrow $TiSi_2$ lines increases significantly when the linewidth is below 200–300 nm [1.45]. $CoSi_2$ extends the linewidth down to ~ 100 nm [1.46]. NiSi has a low resistance in narrow lines for further reduction in the linewidth [1.43]. The formation of NiSi consumes less Si compared with $TiSi_2$ and $CoSi_2$, which is important in forming contacts to ultra-shallow source/drain junctions. Between 200 ^{o}C and 350 ^{o}C, several phases of Ni-rich Ni silicide, such as trinickel silicide (Ni_3Si) and dinickel silicide (Ni_2Si), are formed at the Ni / Si interface [1.47], [1.48]. Between 400 ^{o}C and 600 ^{o}C, the stable phase formed at the interface is NiSi. Above 700 ^{o}C, Ni disilicide ($NiSi_2$) is formed [1.49], [1.50]. The Ni-rich phases formed below 400 ^{o}C, such as Ni2Si and Ni3Si, have much higher resistance than NiSi. Above 700°C, $NiSi_2$ is formed, which also has a higher resistance than NiSi. Therefore, the temperature window for forming a low-resistance NiSi is limited to 400 ^{o}C ~ 600 ^{o}C.

Moreover, NiSi has a lower-temperature than $TiSi_2$ and $CoSi_2$, making it suitable for the lower-temperature poly-Si TFTs fabrication. A self-aligned top-gate poly-Si

TFT using Ni-silicide layers have been studied in the past [1.51]-[1.53]. To simplify the fabrication process of the poly-Si TFT and to reduce parasitic S/D resistance using Ni silicide as ohmic contact layers of the source/drain electrodes. Besides, a fully silicided S/D poly-Si TFTs (FSD TFTs) with ultrashort S/D extension (SDE) structure was developed. Because of the implant-to-silicide (ITS) technique, different to the process of salicide TFTs, the dopants can be implanted into the silicide region without damage the poly-Si region, and then, activated and diffused out quickly from silicide to the interface of silicide/poly-Si at about 600°C by rapid thermal annealing (RTA). Therefore, the activation thermal budget for FSD TFTs is less than that for the conventional and salicide TFTs [1.54].

1.3 Applications of Germanium in Poly-Si TFTs

It is easy to incorporate germanium with silicon to become $Si_{1-X}Ge_X$ alloy. Essentially, $Si_{1-X}Ge_X$ cannot only lower the process thermal budget but also promotes the carrier mobility. Poly-$Si_{1-X}Ge_X$ TFTs have been found to have higher mobility than similarly processed poly-Si TFTs [1.55]. P-channel TFTs with good device characteristics can be fabricated in poly-$Si_{1-X}Ge_X$, films [1.56]. The use of relatively inexpensive glass substrates further reduces manufacturing cost; however, it places tighter constraints on the thermal-budget allowance for a TFT fabrication process, due to problems associated with glass shrinkage and warpage. The fabrication of high-performance poly-Si TFT's typically requires high- temperature (≥600°C) and/or long-time anneals, which makes it incompatible with large area glass substrates. This problem can be solved through the use of silicon-germanium ($Si_{1-X}Ge_X$) films, which can be deposited and crystallized at lower temperatures than Si films. Dopants can be activated at lower temperatures in $Si_{1-X}Ge_X$ than in Si [1.57], [1.58]; therefore, a lower

thermal budget can be used to fabricate poly- $Si_{1-X}Ge_X$ TFTs compared to poly-Si TFTs, to realize CMOS circuits on large-area glass substrates. Poly-$Si_{1-X}Ge_X$ TFTs fabricated using low-temperature solid phase crystallization (LT-SPC) have been demonstrated [1.56]. For LT-SPC applications, $Si_{1-X}Ge_X$ is particularly advantageous, as it requires substantially shorter annealing cycles than required for the crystallization of Si. Hence, $Si_{1-X}Ge_X$ seems to be a potential material for the active layer of a TFT [1.59].

Furthermore, vertical 3D integration of devices using thin film transistors (TFTs) is a promising means of achieving three-dimensional (3-D) integration. Unfortunately, TFT performance is typically substantially worse than that of bulk devices. Variation in device performance is introduced by the random distribution of grains in the device [1.60], since the grain size is on the order of the device size. To achieve large grain TFTs with a control over the location of the grain is therefore highly desirable. Lateral solid-phase crystallization using a seeding agent to precisely nucleate the grains is an extremely promising means of achieving this. Metal induced crystallization has been studied in the past, using metals such as nickel [1.61]. Unfortunately, the integration of such a process into a CMOS technology is problematic due to the deleterious effect of nickel on device performance [1.62]. A metal-contamination-free technique to achieve lateral crystallization could be integrated into a standard CMOS process. A technique to achieve lateral crystallization through the use of germanium seeding has been proposed [1.63]. This technique is free of metallic seeding agents and is therefore easily integrated into a CMOS technology. Additionally, the technique performs extremely well for small devices, making it very promising for next generation VLSI applications. The process has been used to fabricate high-performance TFTs suitable for 3-D integration applications.

1.4 Motivation

1.4.1 From the Perspective of Poly-Si TFTs Characteristics Enhanced by Applying Ni-Silicidation in Gate Engineering, Source/Drain Engineering, and Channel Crystallization

. The output characteristics exhibit an anomalous current increase in the saturation regime, often called "kink" effect [1.64], [1.65] due to an analogy with silicon-on-insulator (SOI) devices [1.66]. This phenomenon can be attributed to the floating-body effect [1.67] and the avalanche multiplication enhanced by grain boundary-traps [1.68]. The avalanche multiplication is caused by the high drain electric field and the presence of grain boundaries and traps enhances the kink effect in poly-Si TFTs [1.68]. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return, particularly in n-channel TFTs [1.33]. Several structures such as lateral body terminal (LBT) [1.36], low-barrier body-contact (LBBC) [1.37], and Schottky body contact [1.38] have been reported in order to reduce the kink current. Among these structures, Schottky barrier MOSFETs (SB-MOSFETs) are thought to have some advantages over conventional MOSFETs, such as the reduction of parasitic resistance and capacitance, and the immunity to the short channel [1.69], latch-up, or silicon-on- insulator floating-body effects [1.70].

In the floating-body thin-film devices, the improved parasitic BJT effect can be achieved by using deep salicidation and fully silicided source/drain structure [1.34], [1.35]. Due to low hole field-effect mobility, p-channel TFTs have lower on-state current compared with n-channel TFTs. Nevertheless, the p-channel TFTs have some advantages, such as low off-state leakage current, slight floating-body effect and kink effect, weak drain impact ionization and high hot carrier reliability. In addition, the

thin-channel poly-Si TFTs have the improved device characteristics such as small leakage current and suppressed floating-body effect compared with the thick-channel poly-Si TFTs [1.71]. Thin channel film also leads to increased source and drain parasitic resistance. The parasitic S/D resistances become increasingly a serious issue in the thin-channel poly-Si TFTs and SOI devices. Several methods such as self-aligned silicide, selective tungsten-clad and metal-replaced junction technology were proposed to reduce parasitic S/D resistance for thin-channel SOI devices and poly-Si TFTs [1.72]-[1.75]. Furthermore, silicided and metal gates have a higher capacitance than poly-Si gates due to the elimination of poly-Si depletion [1.76]. The field-effect mobility and on-state current can be improved by reducing parasitic S/D resistance and increasing gate capacitance [1.74], [1.75]. In the Chapter 2 and 3, application of Ni-salicidation for suppression of floating-body effect and parasitic BJT effect in poly-Si TFTs were demonstrated and investigated.

However, the application of poly-Si TFTs is mainly limited in low-temperature flat-panel display. Conventional poly-Si TFTs suffer from serious poor device characteristics and device-to-device variations resulted from the grain boundaries in the channel region. It is believed that electrical characteristics of the poly-Si TFTs can be improved if the poly-Si grain size can be enhanced and the number of grain boundaries in the channel can be reduced. Metal-Induced-Lateral-crystallization (MILC) technology has been studied in the past to achieve large and regular poly-Si grain from amorphous silicon [1.18]-[1.20]. In addition, vertical thin film transistors (VTFTs) are suitable for high density 3-D integration since their channel length are determined by the thicknesses of SiO_2 or poly-Si films instead of the photolithographic limitation. Many works had been devoted to developing and studying VTFTs [1.77], [1.78]. In Chapter 4, application of Ni-silicide induced lateral crystallization for novel symmetric vertical channel poly-Si TFTs were investigated.

1.4.2 From the Perspective of Poly-Si TFTs Characteristics Enhanced by Applying Germanium in Gate Engineering and Nonvolatile Memories

The large OFF-state leakage current and device instability of poly-Si TFTs are hindrances to the high-performance and high reliability circuit applications. It is well known that the dominant mechanism of the OFF-state leakage current is the field emission via grain boundary traps due to a high electric field in the drain depletion region. The leakage current is increased with increasing gate and drain voltages which enhance the field emission via grain boundary traps in the depletion region near the drain [1.79], [1.80]. In order to increase the reliability and reduce the leakage current, poly-Si TFTs with offset gated, lightly doped drain (LDD), gate-overlapped LDD, floating gate spacer, air cavities, or field-induced drain (FID) structures have been suggested to reduce the electric field near the drain [1.23]-[1.29]. In Chapter 5, application of novel self-aligned Si / Ge T-gate for suppression of OFF-state leakage current in poly-Si TFTs were proposed and demonstrated.

In addition, nanocrystal floating-gate memories offer a number of potential advantages over FLASH devices, including improved scalability, retention, and cyclability, as well as lower voltage operation. In these devices the floating gate is composed of discrete, electrically-isolated particles (rather than a continuous film as in conventional FLASH) [1.81]. Recently, nonvolatile memory devices using Ge or Si nanocrystals (Ge-NCs or Si-NCs) as floating gate (FG) have been widely studied because of its excellent memory performance and high scalability. Ge has smaller bandgap and similar electron affinity compared with Si. Nonvolatile memory devices using Ge-NCs instead of Si-NCs have superior retention properties [1.39]. In addition, Ge/Si-NCs have been reported to possess superior charge retention capability than Ge or Si-NCs [1.82]. In Chapter 6, application of new Ge-NCs for poly-Si TFT

nonvolatile memories with low temperature annealing were proposed and studied.

1.5 Thesis Organization

This thesis is organized as follow:

In Chapter 1, the overview of poly-Si TFTs and applications of Ni-silicidation and germanium in poly-Si TFTs are described.

In Chapter 2, a self-aligned Schottky barrier source and ohmic body contact (SSOB) method was proposed to contact the body terminal of poly-Si TFTs and form the silicided source applicable to technologies that incorporate self-aligned silicide cladded junctions. The new structure provides a very effective body contact to suppress all undesirable floating-body effects. Various device parameters such as subthreshold characteristics, output characteristics, and breakdown voltage are compared with conventional poly-Si TFTs.

In Chapter 3, the n-channel and p-channel fully Ni- self-aligned silicided (fully Ni-salicided) source/drain and gate poly-Si thin-film transistors (n-channel and p-channel FSA-TFTs), whose source/drain and gate layer are completely silicided with Ni, have been successfully fabricated on a 40-nm thick channel layer. The low-resistance fully Ni-salicided source/drain and gate allow a significant recovery of the intrinsic characteristics of thin-channel TFTs. We found that the measured characteristics of FSA-TFTs significantly suppressed floating-body and parasitic BJT effects. Threshold voltage (V_{TH}) difference between in-situ n^+ doped gate and undoped gate n-channel FSA-TFTs was also discussed in this chapter.

In Chapter 4, the novel symmetric vertical channel poly-Si TFTs fabricated by Ni-silicide induced lateral crystallization technology (NSILC-VTFTs) were investigated. The NSILC-VTFTs were fabricated by combining NSILC process and

vertical poly-Si channel. The NSILC-VTFTs are S/D symmetric devices and equivalent to dual-gate devices. In the dual-gate devices, a n^+ floating region is included in the channel region between S/D. The Ni-accumulation and grain boundaries induced from S/D sides can be centralized in the n^+ floating region. The dual-gate structure is employed to eliminate the grain boundaries perpendicular to the current flow in the channel. In this work, the effects of grain boundaries in the vertical channel and n^+ floating region crystallized by NSILC or MILC processes are studied. The NSILC-VTFTs can eliminate metal contaminations on source and drain region due to the limited Ni source from Ni-silicided seeding window arranged on source and drain contact holes. When the device L_{mask} and W_{mask} are scaled down, the probability of the channel region in NSILC-VTFTs to cover grain boundaries in the length and width direction decreases significantly. The NSILC-VTFTs with small L_{mask} and W_{mask} have better device performance and higher uniformity. Furthermore, we have discovered that amorphous silicon was crystallized by two steps: first step lateral crystallization at 500°C for 12hr and second step rapid thermal annealing (RTA) at 700°C for 60-sec, the grain size of the resulting poly-Si can be significantly enhanced and device characteristics can be further improved. In order to investigate the impact of grain boundaries in the vertical channel and n^+ floating region, all the devices were fabricated without further NH_3 plasma treatment. The measured results show the NSILC-VTFTs without NH_3 plasma treatment have high field-effective mobility, small subthreshold swing (S.S.), and low off-state leakage current.

In Chapter 5, the novel self-aligned Si / Ge T-gate poly-Si TFTs (Si / Ge T-gate TFTs) were proposed and demonstrated. The Si / Ge T-gate was formed by selective wet etching of Ge gate layer. The Ge regions etched at the gate edges were refilled by low-pressure chemical vapor deposition tetraethoxysilane (LPCVD TEOS) oxide in the passivation process. The thick gate oxide layer at the gate edges and the

passivation oxide layer were deposited simultaneously in passivation process. The thick gate oxide at the gate edges effectively reduces the drain vertical and lateral electric fields without additional mask, LDD, spacer, and sub-gate bias. The lateral electric field within the channel can be lowered by using the lateral selective etching of Ge within the gate stack at the gate edges without extra fabrication cost in the Si / Ge T-gate TFTs. The Si / Ge T-gate TFTs have a reduced OFF-state leakage current at negative voltages, an improved ON / OFF current ratio, and a smaller drain conductance in saturation due to a reduced impact ionization at the drain end of the channel compared with conventional TFTs.

In Chapter 6, the new poly-Si TFT nonvolatile Ge-NCs memories with low temperature annealing were proposed. The Ge-NCs embedded in oxide were formed by low-pressure chemical vapor deposition (LPCVD) at 370°C [6.10]. The size and density of Ge-NCs can be easily controlled by GeH_4 deposition time and flow rate. Furthermore, the programming / erasing (P/E) characteristics of thin film nonvolatile memory devices (SOI and TFTs) with floating body effect have been investigated. We find that drain voltage is the key point to improve P/E efficiency in thin film nonvolatile memory devices. The mechanism is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the thin film devices. The drain voltage needs to adjust with different gate length and different channel thickness. We can reduce the applied drain voltage to achieve higher P/E efficiency by this floating body effect compared with bulk memory devices.

Finally, conclusions as well as recommendation for further research are given in Chapter 7.

Chapter 2

Suppression of the Floating-Body Effect in Poly-Si Thin-Film Transistors with Self-Aligned Schottky Barrier Source and Ohmic Body Contact Structure

2.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are key devices in active-matrix liquid crystal displays (AMLCDs). Due to the relatively-large field-effect mobilities in both n- and p-channel devices, poly-Si TFTs can be used to incorporate the integrated driving circuits in AMLCDs [2.1]. Recently, poly-Si TFTs are suitable for the pixel driving elements of active matrix organic light emitting diode (AM-OLED) [2.2], and the driving TFTs with a high output resistance are desirable.

However, the output characteristics exhibit an anomalous current increase in the saturation regime, often called "kink" effect [2.3], [2.4] due to an analogy with silicon- on-insulator (SOI) devices [2.5]. This phenomenon can be attributed to the floating- body effect [2.6] and the avalanche multiplication enhanced by grain boundary-traps [2.7]. The avalanche multiplication is caused by the high drain electric field and the presence of grain boundaries and traps enhances the kink effect in poly-Si TFTs [2.7]. The added drain current enhances impact ionization which leads to a premature breakdown in return [2.6]. Several structures such as lateral body

terminal (LBT) [2.8], low-barrier body-contact (LBBC) [2.9], and Schottky body contact [2.10] have been reported in order to reduce the kink current. However, LBT needs additional terminal for the body bias; LBBC needs additional implantation processes and thicker channel thickness for the body contact; and the high forward bias turn on voltage of Schottky diode was reported using Schottky body contact. Among these structures, Schottky barrier MOSFETs (SB-MOSFETs) are thought to have some advantages over conventional MOSFETs, such as the reduction of parasitic resistance and capacitance, and the immunity to the short channel [2.11], latch-up, or silicon-on- insulator floating-body effects [2.12].

In this chapter, we have developed a self-aligned Schottky barrier source and ohmic body contact (SSOB) method for contacting the body terminal of poly-Si TFTs and forming the silicided source applicable to technologies that incorporate self-aligned silicide cladded junctions. The new structure provides a very effective body contact to suppress all undesirable floating-body effects. Various device parameters such as subthreshold characteristics, output characteristics, and breakdown voltage are compared with conventional poly-Si TFTs.

2.2 Experiment

The key processes to fabricate the SSOB-TFTs are shown in Fig. 2.1 First, a 50-nm or 100-nm amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafers. Next, the a-Si layer was then recrystallized by solid phase crystallization (SPC) at 600°C for 24-hr. After the active region patterning, a 50-nm gate oxide layer was deposited by high-density plasma chemical vapor deposition at 350°C. Subsequently, a 150-nm in-situ n^+ doped a-Si layer and a 150-nm Si_3N_4 hard mask layer were deposited by

LPCVD. After defining gate electrode, the remaining oxide on source/drain regions was removed by diluted HF. A mask was used to perform the n^+ drain-side implantation with P^+ to dose 5×10^{15} cm^{-2} and energy 18 keV for channel thickness = 50-nm (energy 30 keV for channel thickness = 100-nm) (Fig. 2.1a). A 250-nm oxide sidewall spacer was formed by deposition and etching of TEOS oxide. A similar mask was used to perform the p^+ doped body-contact BF_2 implantation with dose 5×10^{15} cm^{-2} and moderate energy 35 keV for channel thickness = 50-nm (energy 50 keV for channel thickness = 100-nm). This implantation serves to form a p^+ junction below the Schottky barrier source for ohmic body contact and also improves the conductivity at the bottom of the source for better body current collection simultaneously (Fig. 2.1b). Meanwhile, only source- side oxide spacer was removed by buffered oxide etch (BOE). After removing the photoresist of body-contact mask, the Si_3N_4 hard mask layer was then selectively etched in a hot phosphoric acid bath. A second 25-nm oxide sidewall spacer was again formed by deposition and etching of TEOS oxide. Dopants were activated by rapid thermal annealing (RTA) at 750°C for 20-sec. A Ni film of about 10-nm was deposited by sputtering after a dilute HF-dip and then Ni-salicidation was carried out at 500°C for 30-sec by one-step RTA in the N_2 ambient. Unreacted Ni was removed in $H_2SO_4 : H_2O_2$ solution. The Schottky barrier source was formed by the Ni-salicidation (Fig. 2.1c). After contact and metallization processes, the resultant poly-Si TFT with SSOB was shown in Fig. 2.1d. Conventional devices with self-aligned n^+ source/drain and without Ni-salicidation were also fabricated to serve as control ones. No further hydrogenation (NH_3 plasma treatment) procedures were implemented after sintering at 400 °C for 30 min.

2.3 Results and Discussion

2.3.1 n^+ Drain - p^+ Source Poly-Si TFTs Structure

Figure 2.2 shows the measured transfer characteristics of the n^+ drain - p^+ source poly-Si TFTs without Ni-salicidation. The limited drain current is caused by tunneling current between the inversion layer and the p^+ source [2.13]. When gate voltage is increased, the drain current is limited by the p^+ source.

The measured transfer characteristics of the conventional and the SSOB-TFTs with W / L = 50μm / 5μm are shown in Fig. 2.3. The off-state leakage currents in the conventional TFTs are slightly higher than that in the SSOB-TFTs. The SSOB-TFTs and conventional TFTs are the approximate on-state currents. Figure 2.3 also displays that the threshold voltages V_{TH} (defined as $I_D = W / L \times 100nA$) of SSOB-TFTs are more stable than these of conventional TFTs at small $V_{DS} = 0.5V$ and large $V_{DS} = 5V$. Since the hole accumulation at the channel increases the body potential and lowers the junction barrier at the source region, a large number of hole carrier may be collected by the source. The leakage current is the sum of the electron current by field-emission at the drain region and the hole current caused by p-n forward bias at source [2.8]. With this ohmic body contact, the hole accumulation in the body and parasitic bipolar effects can be eliminated, resulting in a stable V_{TH} [2.9], [2.14] and lower off-state leakage current in the SSOB-TFTs [2.15]. The benefit of the SSOB-TFTs also can be found on subthreshold swing (S.S.). The S.S. of the conventional and the SSOB-TFTs are about 1230 mV/dec. and 1100 mV/dec., respectively. We believe that it may be due to the shallow silicided source junction and p^+ junction in the SSOB-TFTs.

The measured output characteristics of the conventional and the SSOB-TFTs are shown in Fig. 2.4. The kink effect of the SSOB-TFTs is considerably reduced compared with the conventional TFTs. Under high drain voltage, excessive holes are accumulated at the body region and the drain breakdown is reduced by the floating-body effect in the conventional TFTs [2.16], [2.17]. This hole accumulation

causes a profound kink effect, which in turn deteriorates the output characteristics and induces parasitic bipolar transistor action [2.18], [2.19]. Since the SSOB-TFTs effectively collect the hole current generated by impact ionization, the floating-body effect is significantly suppressed and breakdown voltage is increased.

2.3.2 p^+ Drain - n^+ Source Poly-Si TFTs Structure

Figure 2.5 demonstrates the output characteristics of the p^+ drain - n^+ source poly - Si TFTs without Ni-salicidation. The output characteristics exhibit a turn-on voltage of the drain-diode [2.20]. The drain voltage offset is approximately 0.5V~0.6V. The drain voltage offset is considered to arise from the barrier formed between the p^+ drain and n^+ inversion layer.

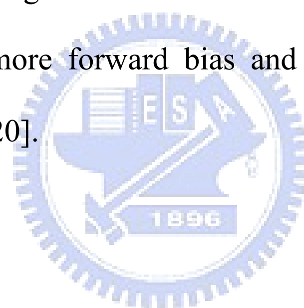
To prove asymmetric S/D embedded in our SSOB structure, devices were measured again with interchanged S/D, i.e., Schottky drain TFTs with Schottky barrier drain and n^+ source. Figure 2.6 shows the transfer characteristics of the Schottky drain and the SSOB-TFTs with W / L = 50μm / 5μm. Notably, the subthreshlod and on-state transfer characteristics for both devices are almost the same, except for gate-induced-drain-leakage (GIDL)-like currents when V_G was at negative bias. Normally, GIDL-like currents were often found for Schottky drain TFTs due to holes tunneling to the channel from drain metal silicide [2.21]. The GIDL-like currents become significant at the stronger accumulation region and higher drain voltage in the Schottky drain TFTs. This GIDL-like current can be three-order of magnitude reduced by the n^+ drain in the SSOB-TFTs.

The measured output characteristics of the Schottky drain TFTs and the SSOB-TFTs are shown in Fig. 2.7. The kink effect of the SSOB-TFTs is considerably reduced compared with the Schottky drain TFTs. Figure 2.7 also indicates that the output characteristics of the Schottky drain TFTs have a small finite drain voltage

offset (V_D offset < 0.5V) which is considered to arise from the Schottky barrier formed between the Schottky barrier drain and n^+ inversion layer [2.22]. The low breakdown voltage (V_D ~ 15 V) and kink-like current for Schottky drain TFTs may result from the inherent p-i-n diode forward biased at $V_D > 0V$.

2.3.3 SSOB-TFTs at Different Negative Source Voltage

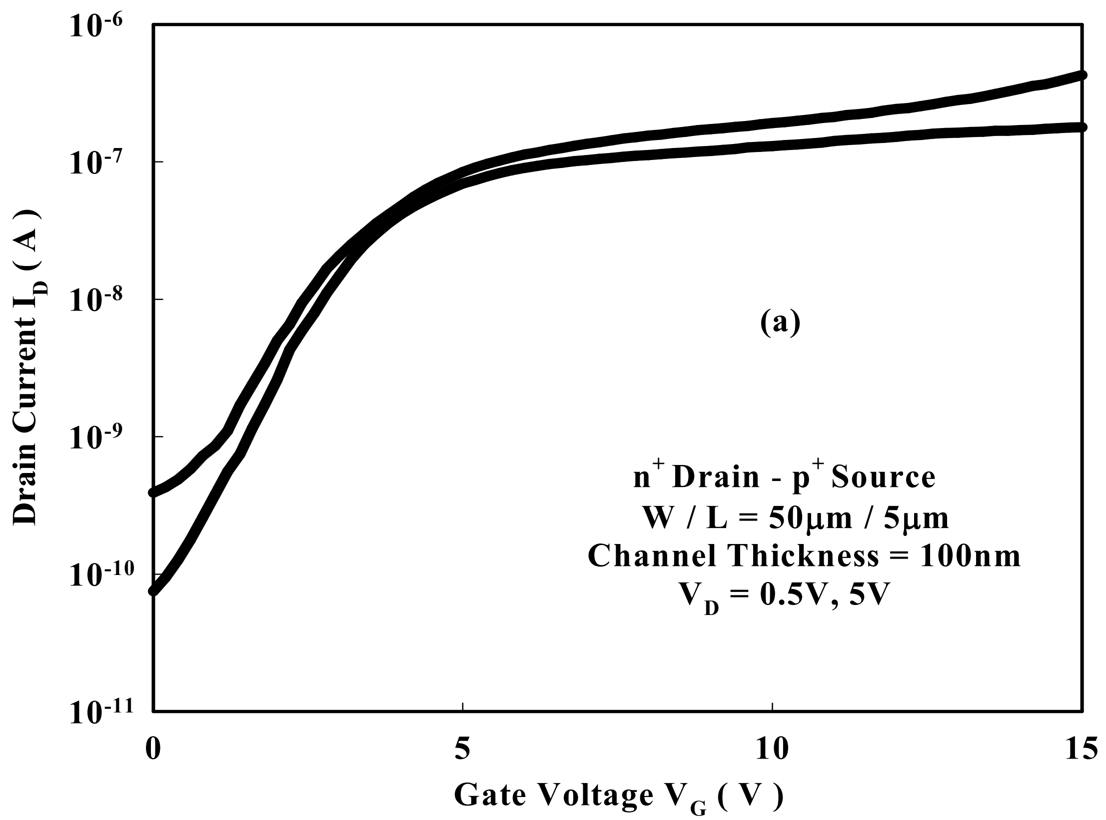
The measured output characteristics of the conventional and the SSOB-TFTs at different negative source voltage are shown in Fig. 2.8 and Fig. 2.9 with channel thickness = 100-nm and channel thickness = 50-nm, respectively. The kink effect of the SSOB-TFTs is considerably reduced compared with the conventional TFTs at different negative source voltage. When the source voltage is more negative, the source to body junction is more forward bias and kink effect is more serious in conventional TFTs [2.19], [2.20].



2.4 Summary

We have developed a self-aligned SSOB structure for poly-Si TFTs to provide an effective body contact and suppress the floating-body effect. The GIDL-like currents occurred in the Schottky drain TFTs are reduced by the SSOB-TFTs. This SSOB-TFTs show reduced kink effect and increased breakdown voltage and are suitable for driving circuit application for high voltage gain.

Fig. 2.1 The key processes of the SSOB-TFTs, (a) n^+ drain-side implantation, (b) p^+ body-contact implantation, (c) Ni-salicidation and Schottky barrier source formation, (d) The poly-Si TFTs with SSOB after contact and metallization processes.



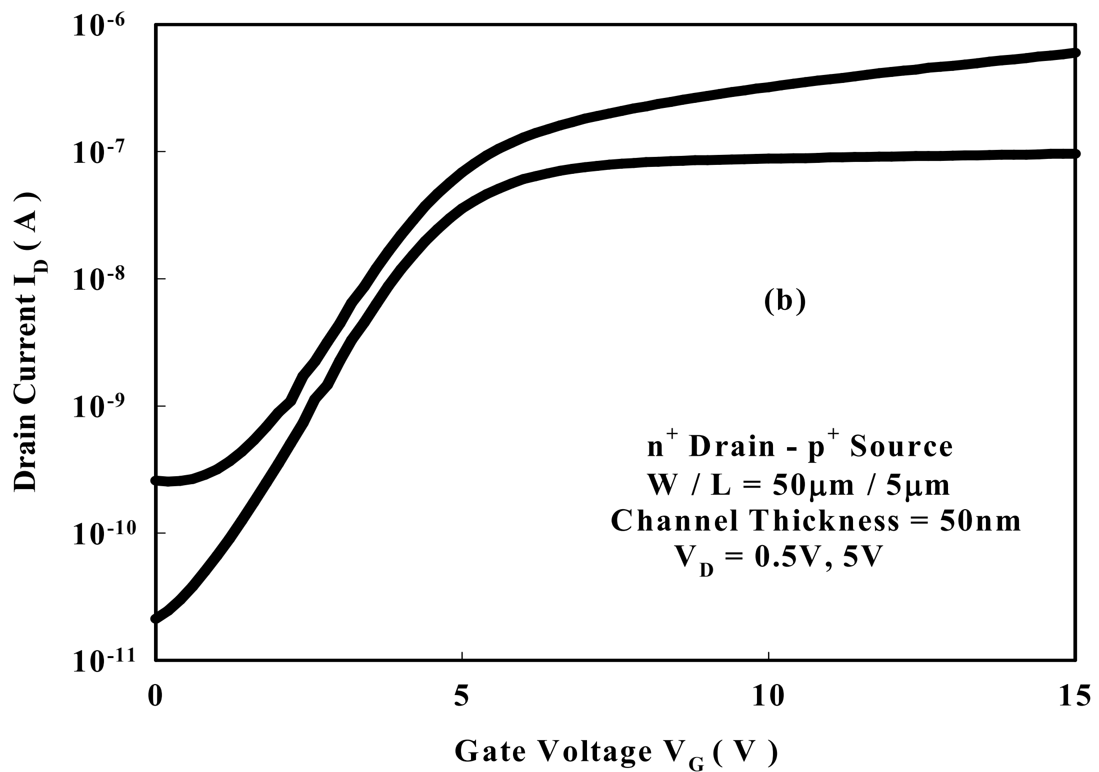
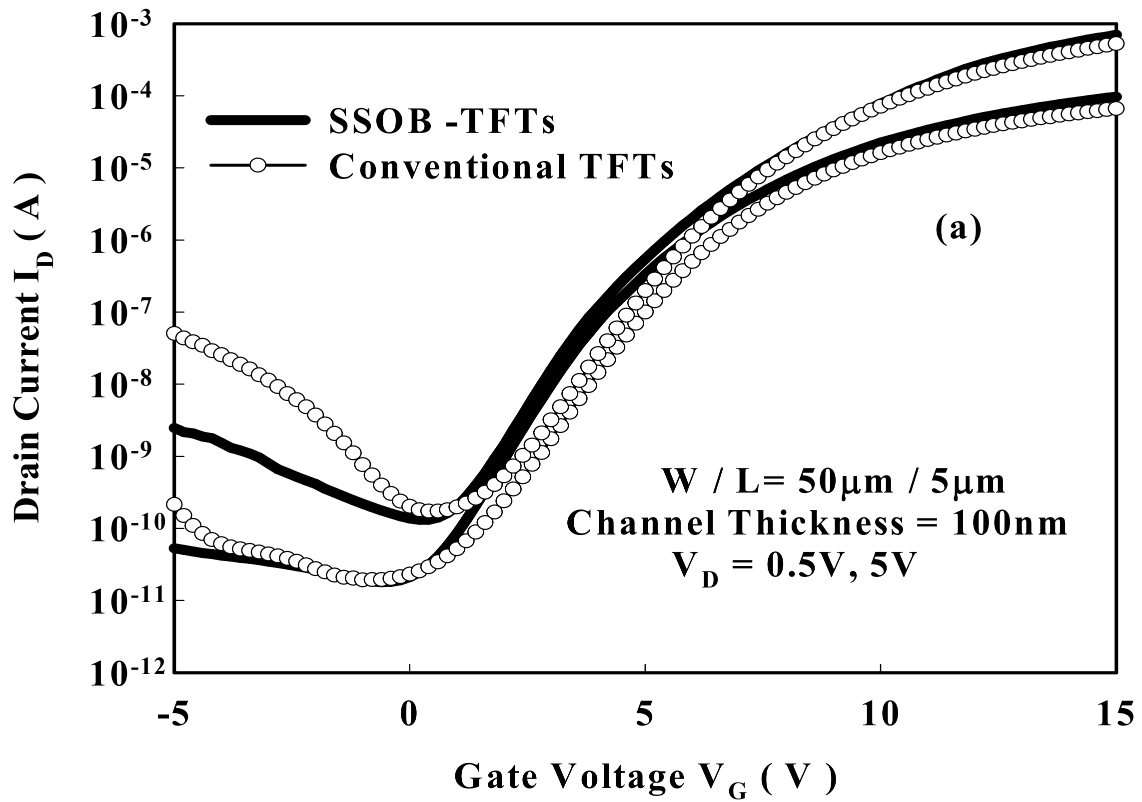


Fig. 2.2 The transfer characteristics of the n^+ drain - p^+ source poly - Si TFTs with channel thickness (a) 100nm and (b) 50nm before Ni salicidation. When gate voltage is increased, the drain current is limited by the p^+ source.



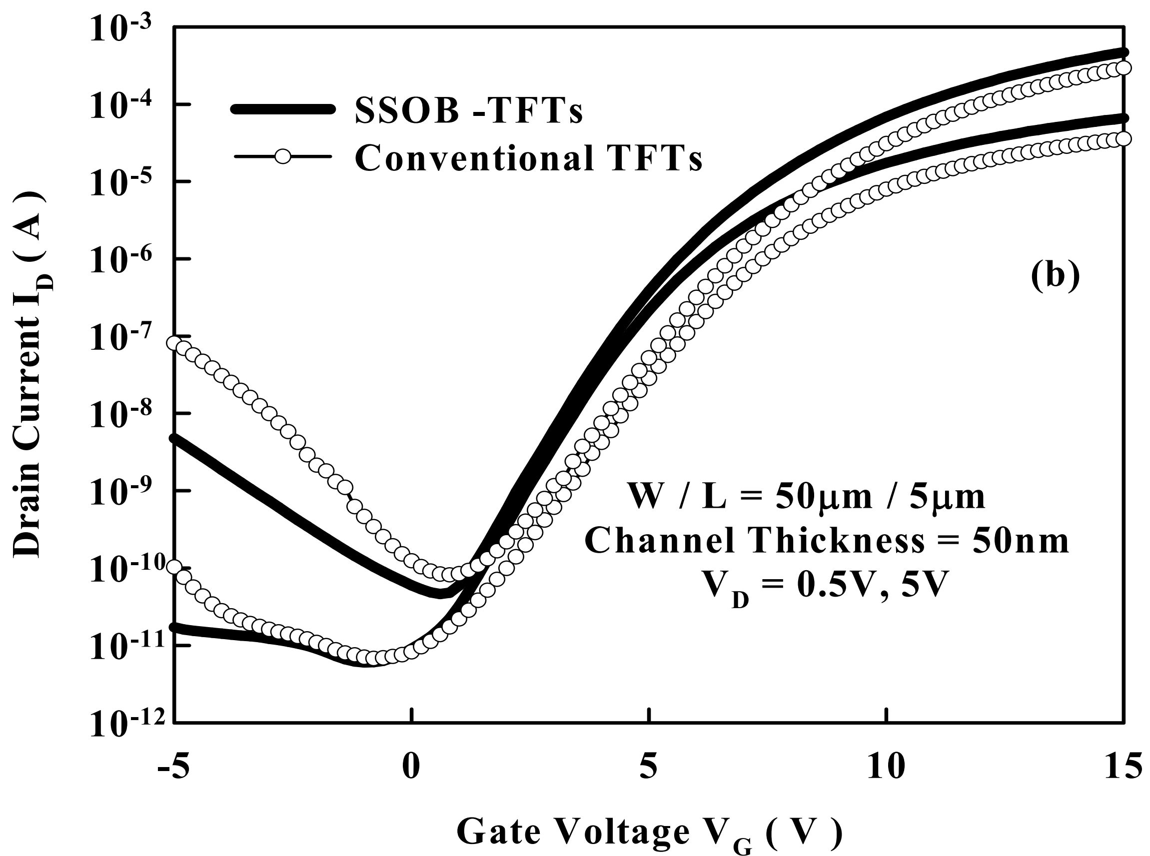
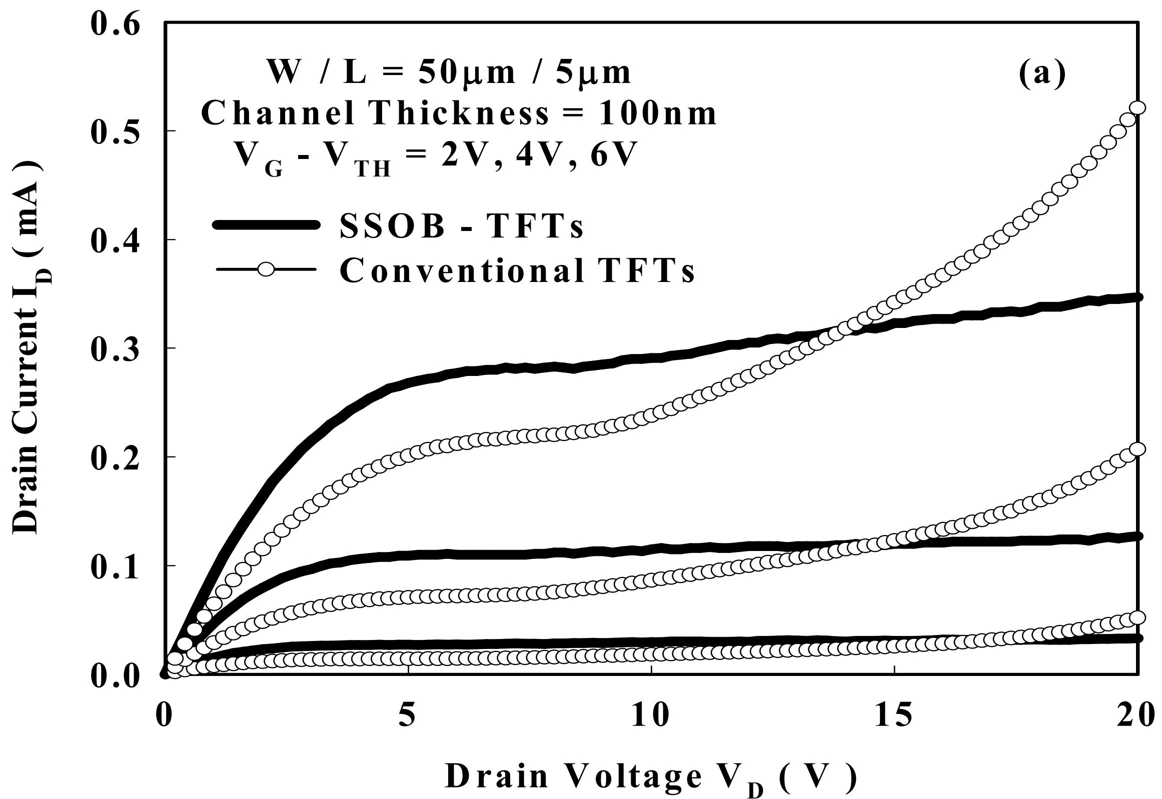


Fig. 2.3 The transfer characteristics of the conventional and the SSOB - TFTs with channel thickness (a) 100nm and (b) 50nm. The SSOB-TFTs give low leakage currents and improved subthreshold characteristics compared with conventional TFTs.



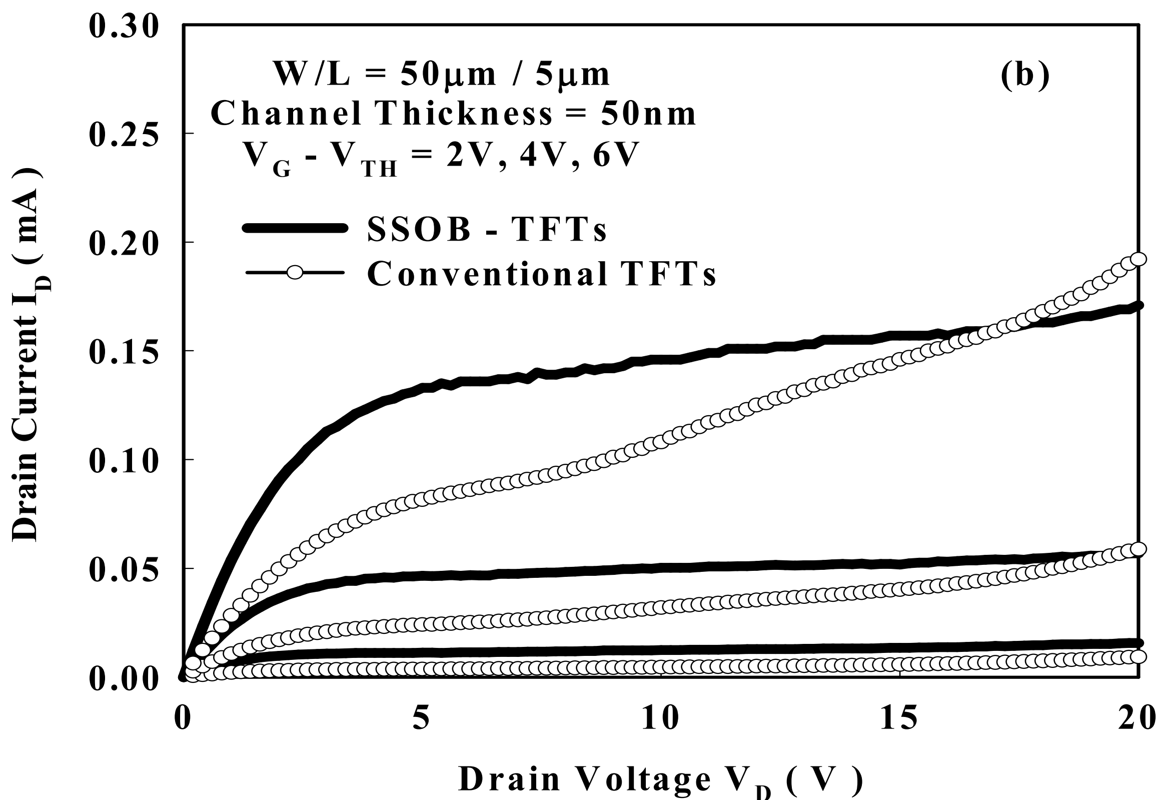


Fig. 2.4 The output characteristics of the conventional and the SSOB - TFTs with channel thickness (a) 100nm and (b) 50nm. Compared with conventional TFTs, SSOB-TFTs give reduced kink effect and increased breakdown voltage.

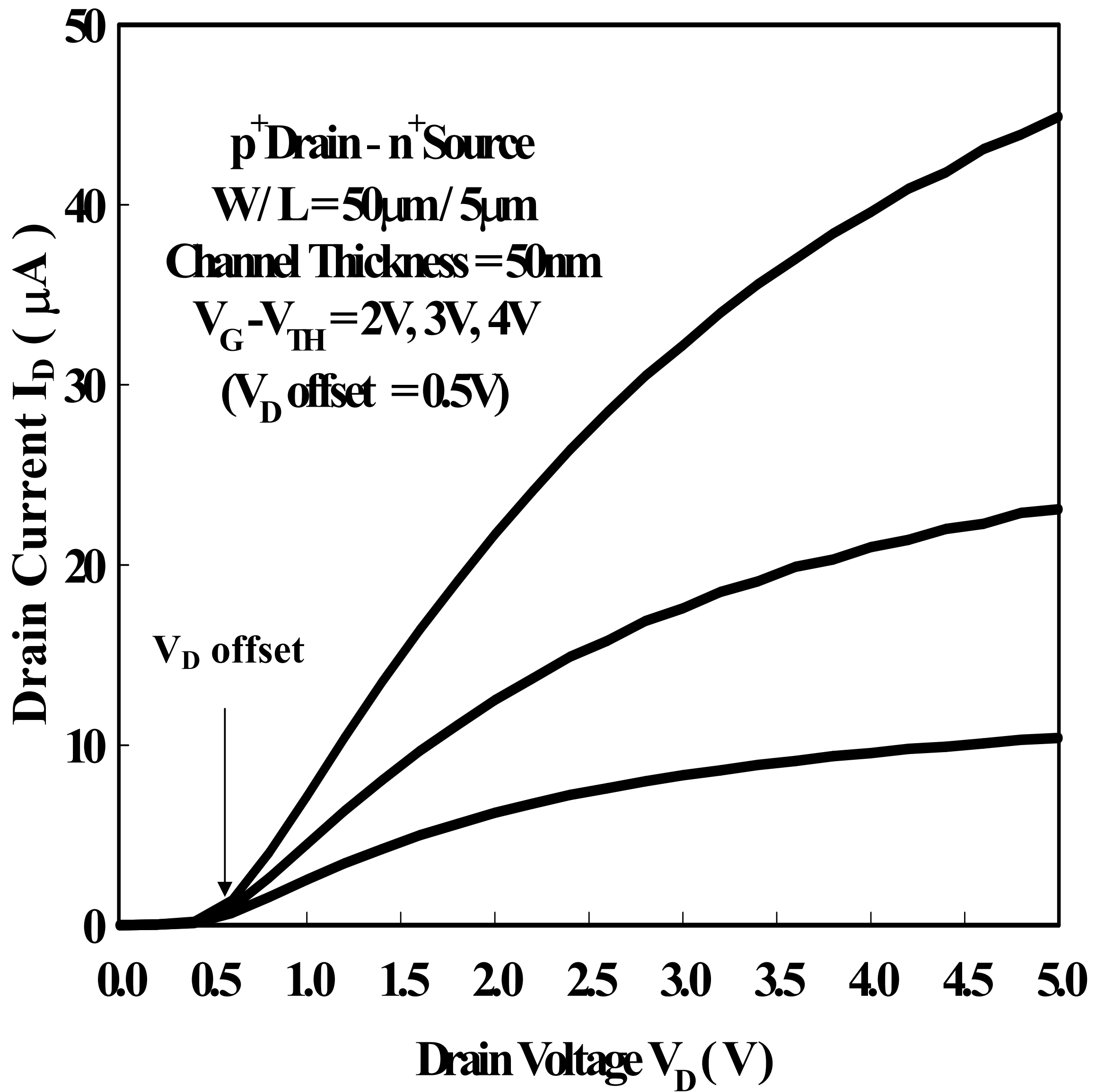


Fig. 2.5 The output characteristics of the the p^+ drain - n^+ source poly - Si TFTs with channel thickness 50nm before Ni salicidation. The drain voltage offset is approximately 0.5V.

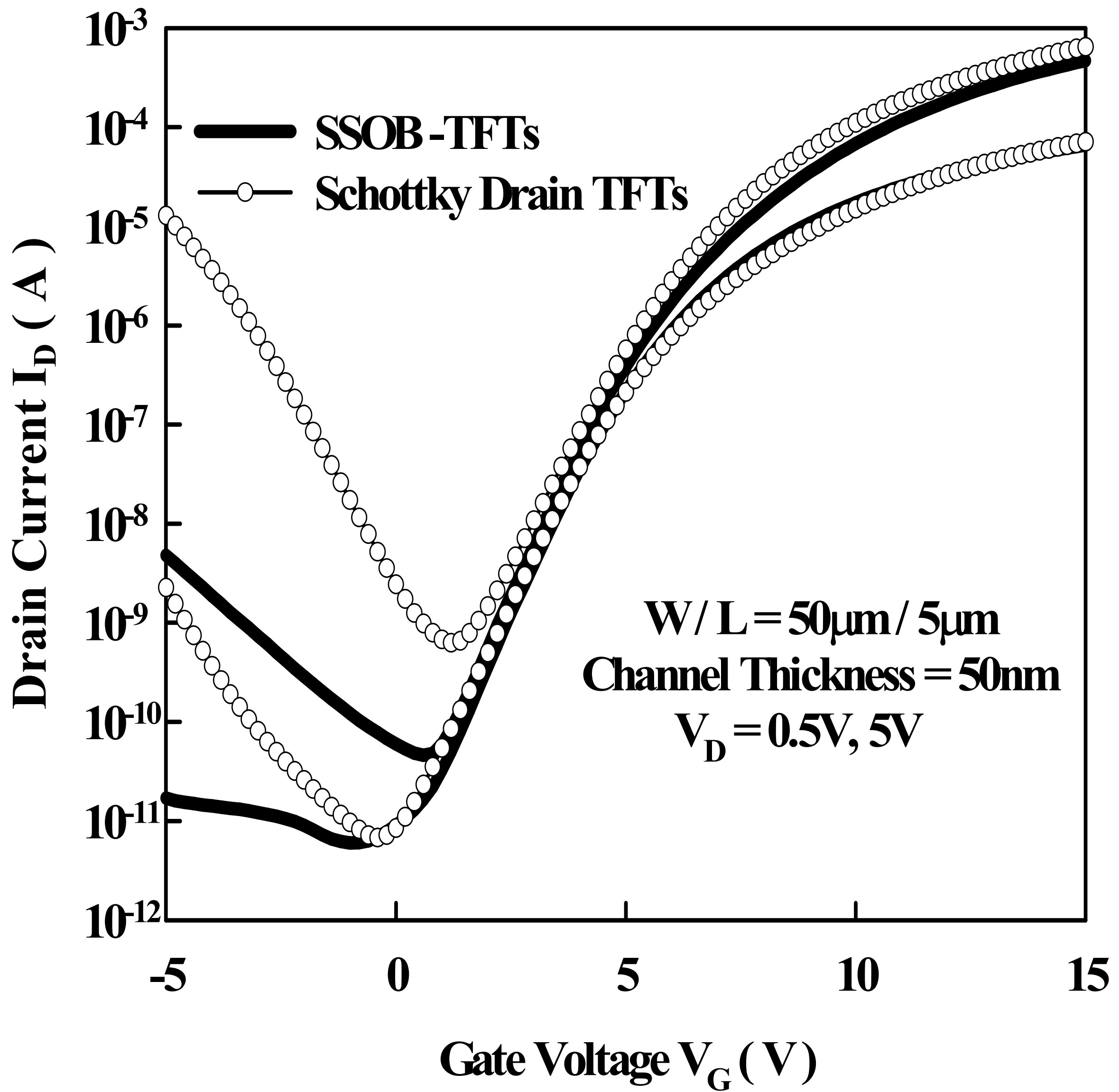


Fig. 2.6 The transfer characteristics of the Schottky drain and the SSOB - TFTs with channel thickness 50nm. The large GIDL-like current is due to Schottky barrier drain.

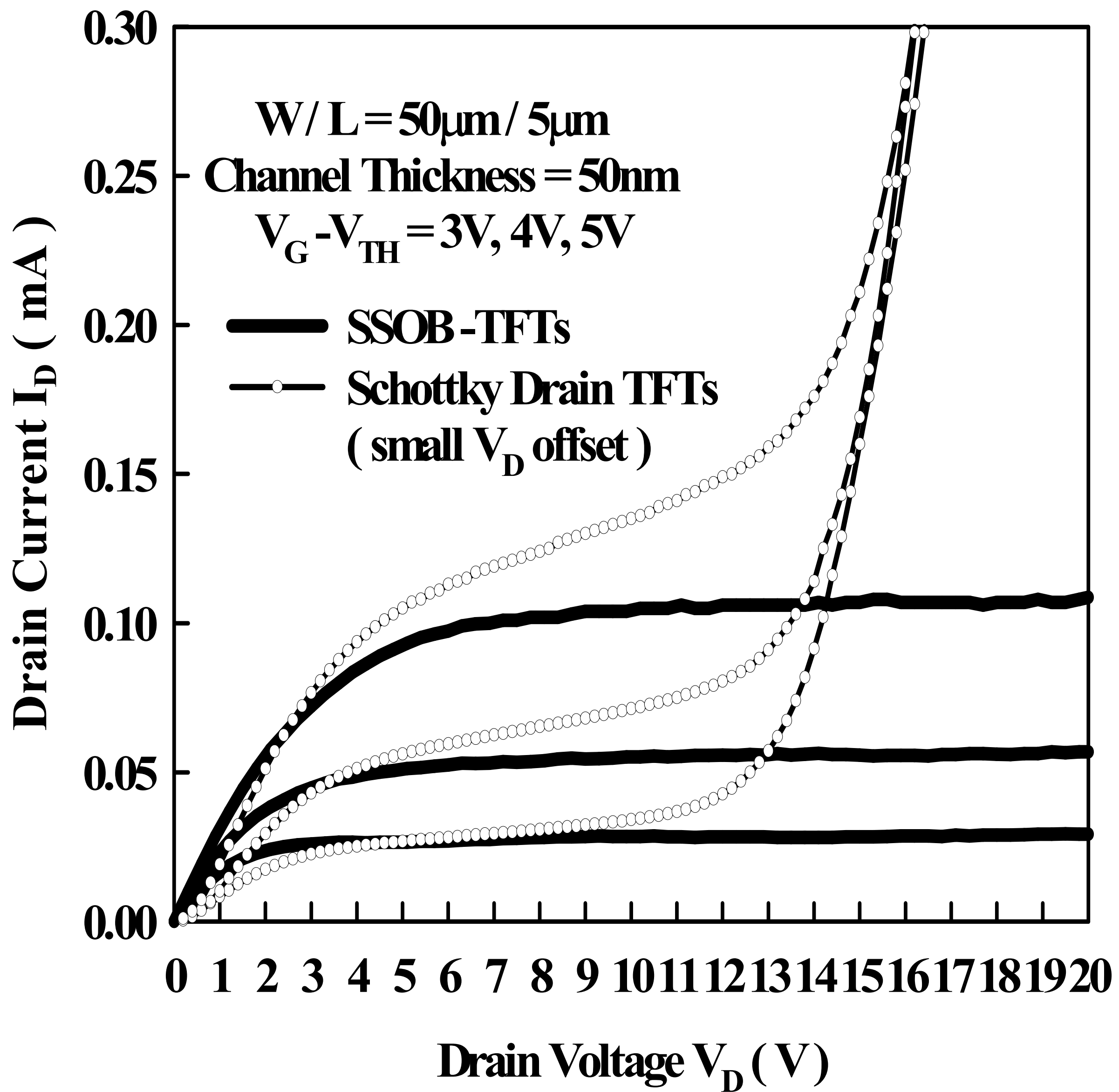


Fig. 2.7 The output characteristics of the Schottky drain and the SSOB - TFTs with channel thickness 50nm. The Schottky drain TFTs have a small drain voltage offset (< 0.5V).

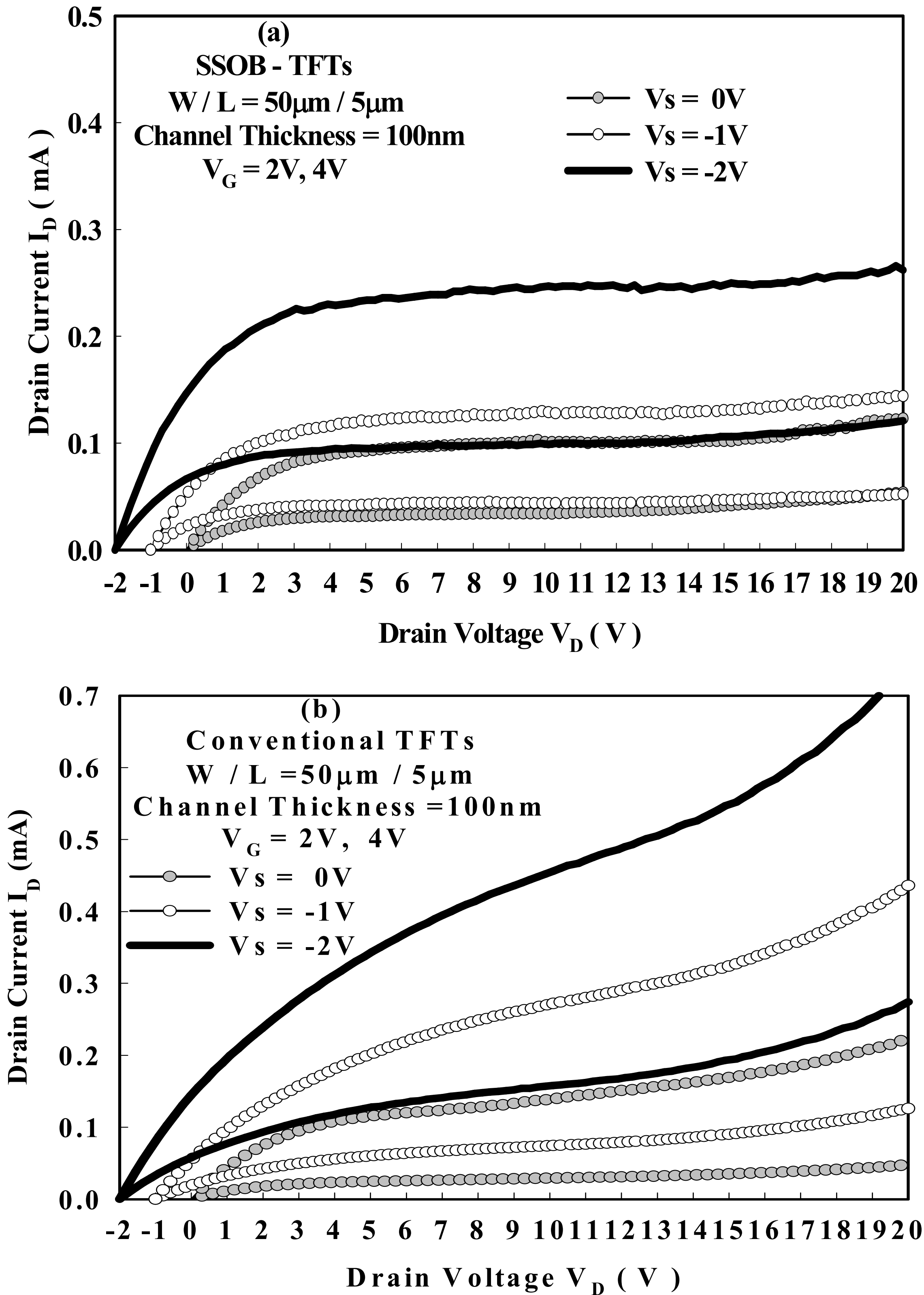
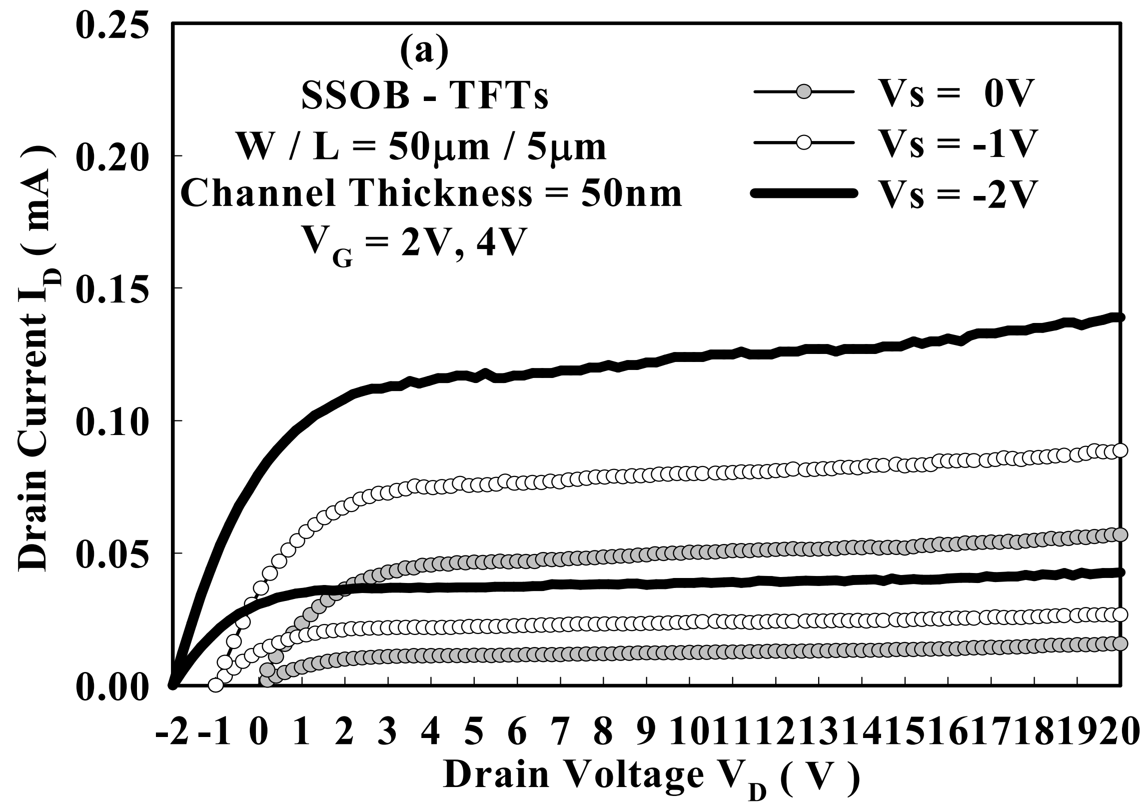


Fig. 2.8 The output characteristics of (a) the SSOB - TFTs and (b) the conventional TFTs with channel thickness 100nm at different negative source voltage. When the source voltage is more negative, the source to body junction is more forward bias and kink effect is more serious in conventional TFTs.



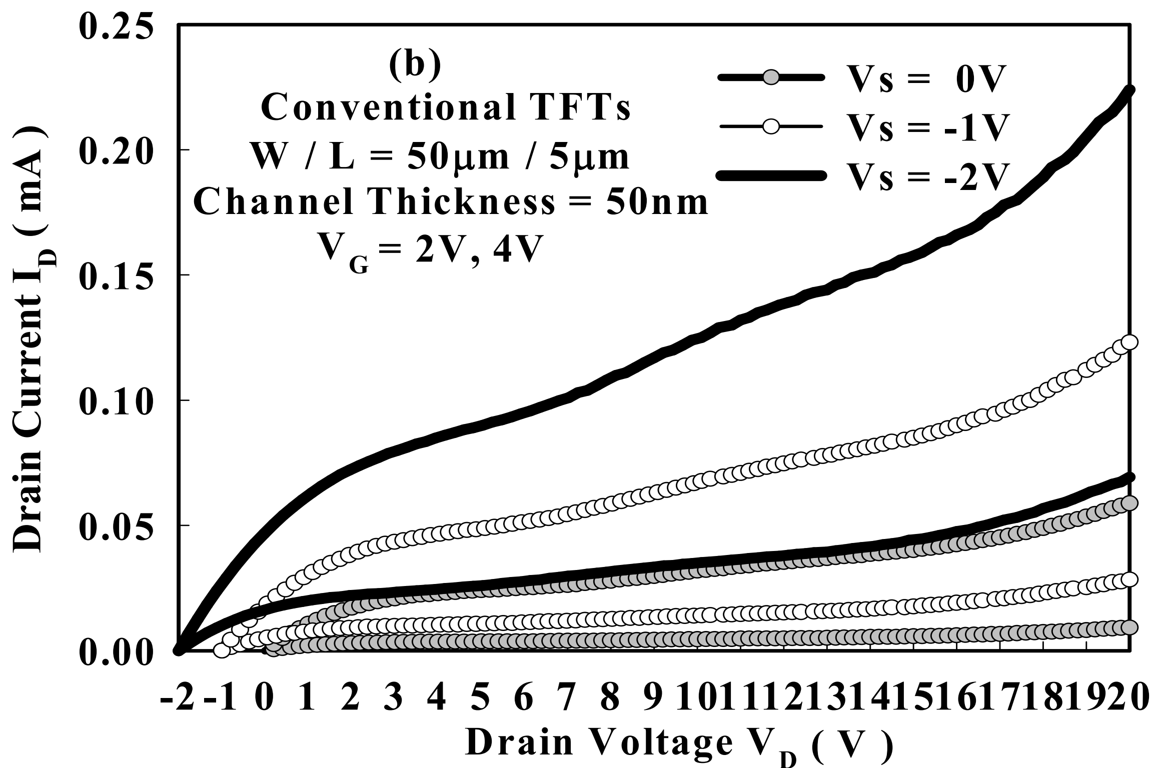


Fig.2.9 The output characteristics of (a) the SSOB - TFTs and (b) the conventional TFTs with channel thickness 50nm at different negative source voltage. When the source voltage is more negative, the source to body junction is more forward bias and kink effect is more serious in conventional TFTs.

Chapter 3

Characteristics of n-Channel and p-Channel Fully Ni-Self-Aligned Silicided S/D and Gate Poly-Si Thin-Film Transistors

3.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many potential applications including 3D integration high density flash memories, pixel driving elements of active matrix organic light emitting diode (AM-OLED), and integrated peripheral driving circuits and addressing elements of active-matrix liquid crystal displays (AMLCDs) [3.1]-[3.4].

However, the output characteristics exhibit an anomalous increase of current in the saturation regime, often called "kink" effect due to an analogy with silicon-on-insulator (SOI) devices [3.5]-[3.7]. This phenomenon can be attributed to the floating-body effect [3.8] and the avalanche multiplication enhanced by grain boundary-traps [3.6], particularly in n-channel TFTs. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return [3.8]. In the floating-body thin-film devices, the improved parasitic BJT effect can be achieved by using deep salicidation and fully silicided source/drain structure [3.9], [3.10].

Due to low hole field-effect mobility, p-channel TFTs have lower on-state current compared with n-channel TFTs. Nevertheless, the p-channel TFTs have some

advantages, such as low off-state leakage current, slight floating-body effect and kink effect, weak drain impact ionization and high hot carrier reliability. In addition, the thin-channel poly-Si TFTs have the improved device characteristics such as small leakage current and suppressed floating-body effect compared with the thick-channel poly-Si TFTs [3.11]. Thin channel film also leads to increased source and drain parasitic resistance. The parasitic S/D resistances become increasingly a serious issue in the thin-channel poly-Si TFTs and SOI devices. Several methods such as self-aligned silicide, selective tungsten-clad and metal-replaced junction technology were proposed to reduce parasitic S/D resistance for thin-channel SOI devices and poly-Si TFTs [3.12]-[3.15]. Furthermore, silicided and metal gates have a higher capacitance than poly-Si gates due to the elimination of poly-Si depletion [3.16]. The field-effect mobility and on-state current can be improved by reducing parasitic S/D resistance and increasing gate capacitance [3.14], [3.15].

In this chapter, the n-channel and p-channel fully Ni- self-aligned silicided (fully Ni-salicided) source/drain and gate poly-Si thin-film transistors (n-channel and p-channel FSA-TFTs), whose source/drain and gate layer are completely silicided with Ni, have been successfully fabricated on a 40-nm thick channel layer [3.17]. The low-resistance fully Ni-salicided source/drain and gate allow a significant recovery of the intrinsic characteristics of thin-channel TFTs. We found that the measured characteristics of FSA-TFTs significantly suppressed floating-body and parasitic BJT effects. Threshold voltage (V_{TH}) difference between in-situ n^+ doped gate and undoped gate n-channel FSA-TFTs was also discussed in this chapter.

3.2 Experiment

Figure 3.1 shows the main fabrication process steps of FSA-TFTs. First, a 40-nm

amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafers. Next, the a-Si layer was then crystallized by solid phase crystallization (SPC) at 600°C for 24-hr. After the patterning of active region, a 50-nm tetraethoxysilane (TEOS) gate oxide layer was deposited by LPCVD. Subsequently, a 50-nm a-Si gate layer and a 100-nm Si_3N_4 layer as the hard mask were deposited by LPCVD. The a-Si gate layers were divided into in-situ n^+ phosphorus doped gate or undoped gate in n-channel FSA-TFTs. The a-Si gate layer was undoped gate in p-channel FSA-TFTs. Due to experimental equipment limitation, the p-channel FSA-TFTs with in-situ p^+ boron doped gate were not fabricated in our experiments.

After defining gate electrode, the self-aligned source/drain implantation were used to form the n^+ / p^+ with P^+ / BF_2^+ to dose 5×10^{15} cm^{-2} for n-channel / p-channel (Fig.3.1a). Dopants were activated by furnace at 600°C for 12-hr. A 150-nm TEOS oxide was deposited and etched to form the sidewall spacer. Then, the Si_3N_4 hard mask layer was selectively etched in a hot phosphoric acid bath (Fig.3.1b). A Ni film of about 40-nm was deposited by sputtering and then fully Ni-salicidation was carried out at 500°C~550°C for 30~60-sec by one-step rapid thermal annealing (RTA) in the N_2 ambient. The fully Ni-silicided source/drain and gate were formed by the fully Ni-salicidation process (Fig.3.1c). After contact and metallization processes, NH_3 plasma treatments were implemented after sintering at 400 °C for 30-min. Conventional devices with self-aligned n^+ source/drain and without Ni-salicidation were also fabricated to serve as control ones.

3.3 Results and Discussion

3.3.1. Fully Ni-Salicidation Process

The cross-sectional transmission electron microscopy (TEM) micrographs of FSA-TFTs are shown in Fig.3.2. The gate and source/drain of FSA-TFTs were fully Ni-salicided and no silicide was observed on the sidewall TEOS spacer (Fig.3.2a and Fig.3.2b). In our study, we used thick enough Ni film (about 40-nm) to achieve the fully Ni-salicided TFTs. According to the volume ratio of Ni-silicidation, a typical 30~40-nm thick Ni film can completely convert the 50nm-thick poly-Si gate to fully Ni-silicided gate. We chose 40-nm thick Ni film and one-step RTA at 500°C~550°C for 30~60-sec to formed the FSA-TFTs. It was found that threshold voltage V_{TH} values of FSA-TFTs with fully Ni-silicided gate formed by RTA 500°C or 550°C for appropriate time are almost identical. In order to form fully Ni-salicided TFTs, the time of RTA must be long enough. The process key point is the balance of spacer length and RTA conditions. In the Fig.3.2c, the lateral diffusion length of Ni-silicidation is smaller than spacer length and the S/D n^+ or p^+ junction can be left to avoid formation of the Schottky barrier junction. When the Ni-silicided edge is too close to the S/D n^+ or p^+ junction edge with too high RTA temperature and too long RTA time, an abnormally high off-state leakage current (I_{OFF}) and gate-induced-drain leakage (GIDL)-like current occur [3.18], [3.19]. Hence, it is important to find out the balance of spacer length and RTA conditions.

3.3.2 n-Channel FSA-TFTs

The measured transfer characteristics and field-effect mobility of the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm are shown in Fig.3.3 and Fig.3.4 respectively. The on-state currents and field-effect mobility in the FSA-TFTs are higher than those in the conventional TFTs. The off-state leakage currents of FSA-TFTs are lower than those of the conventional TFTs. The on-state currents are significantly degraded by the parasitic S/D resistance in short-channel

conventional TFTs. The field-effect mobility plotted in Fig.3.4 is obtained from the channel conductance. For the conventional TFTs with short channel length of 0.8 μm, the field-effect mobility is seriously decreased when gate voltage $V_G > 2.5$ V, but it is not found in short channel FSA-TFTs. The high field-effect mobility of FSA-TFTs can be kept at large gate voltage. This improvement is due to the fully Ni-salicided source/drain and gate structure, which has smaller parasitic S/D resistance, higher capacitance and superior scalability than the conventional TFTs with poly-Si gates [3.16]. The advantage of FSA-TFTs also can be found on subthreshold swing. We believe that it is due to the higher gate capacitance and the fully silicided source/drain in the FSA-TFTs.

The measured output characteristics of the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm are shown in Fig.3.5. Under high drain voltage, the accumulation of holes in the body causes a profound kink effect and induced parasitic BJT action which results in decreased drain breakdown voltage by the floating-body effect in the conventional TFTs [3.20]-[3.23]. Salicidation is a well known method to suppress the floating-body effect because the silicide layer near the source/drain junction works as a sink and an effective lifetime killer for holes [3.9], [3.10]. The reduced kink effect and increased drain breakdown voltage of FSA-TFTs strongly support that floating-body and parasitic BJT effects are significantly suppressed by the fully-silicided source/drain structure.

In order to prove that parasitic S/D resistance can be greatly reduced by the fully Ni-salicided process, the parasitic resistance R_P of (a) n-channel FSA-TFTs with in-situ doped gate, (b) n-channel FSA-TFTs with undoped gate and (c) n-channel conventional TFTs, in the linear region, is extracted by plotting measured on state resistance (R_{ON}) versus gate length (L_G), as shown in Figs.3.6. With different gate bias, the relationship between R_{ON} and L can be expressed by several straight lines

that extend to merge at a characteristic length Lo representing the accumulation channel in LDD (and S/D) area and have a residual value of a gate-voltage independent parasitic resistance R_P [3.12]. The R_P of FSA-TFTs with in-situ doped gate and undoped gate is about 437 Ω and 372 Ω respectively. The Lo of FSA-TFTs with in-situ doped gate and undoped gate are near 0 μm. The R_P of conventional TFTs is extracted by the same method and is about 5.78 kΩ. The on-state currents and field-effect mobility are greatly improved by reducing R_P in the n-channel FSA-TFTs.

Figure 3.7 displays the on / off current ratio (I_{ON} / I_{OFF}) of the n-channel conventional and the n-channel FSA-TFTs with W =10μm. The on-state current is defined as drain current (I_D) at V_G = 10.0 V, V_{DS} = 3.0 V and the off-state current is defined as minimum drain current (I_{min}) at V_{DS} = 3.0 V. The I_{ON} / I_{OFF} (10^8~10^9) can be increased with scaling down channel length in FSA-TFTs. Because the threshold voltage of FSA-TFTs with in-situ doped gate is smaller than this of FSA-TFTs with undoped gate, the I_{ON} / I_{OFF} of FSA-TFTs with in-situ doped gate is larger than this of FSA-TFTs with undoped gate. The I_{ON} / I_{OFF} (10^6~10^7) of conventional TFTs is limited with scaling down channel length. The enhancement of off-state leakage currents is observed in short-channel conventional TFTs. The off-state leakage currents of the conventional TFTs are increasing with scaling down channel length. This enhanced off-state leakage currents is the amplification of gate-induced-drain leakage (GIDL) currents by the parasitic BJT in short-channel devices due to the floating-body effect and strong impact ionization [3.24]. Since the FSA-TFTs effectively suppress the floating-body effect, the enhancement of GIDL currents are eliminated and off-state leakage currents are almost the same in both long and short channel devices.

Figure 3.8 shows the extracted threshold voltage V_{TH} of the n-channel conventional and the n-channel FSA-TFTs with different gate lengths (defined as I_D =

W / L × 100 nA at V_{DS} = 0.5 V). The roll-off of V_{TH} is greatly improved in FSA-TFTs. With this fully Ni-salicided structure, the floating-body and parasitic BJT effects can be suppressed, resulting in a stable V_{TH} and lower off-state leakage current in FSA-TFTs [3.9], [3.10], [3.25], [3.26]. Figure 3.8 also shows the V_{TH} difference between in-situ n^+ doped gate and undoped gate FSA-TFTs. This V_{TH} difference is observed with additional P^+ dopants in the in-situ n^+ doped gate FSA-TFTs. The silicidation induced segregation of the impurities from poly-Si to the silicide interface is determined that sub-monolayer segregation of the dopants causes a change in the apparent NiSi workfunction shift [3.16].

Furthermore, we also used thin Ni film (about 15-nm) to form partially salicided TFTs with in-situ doped 50-nm-thick poly-Si gate. The partially salicided TFTs were form by RTA 500°C for 60-sec and RTA 550°C for 30-sec. Figure 3.9 displays the extracted V_{TH} roll-off of the n-channel FSA-TFTs with in-situ doped gate and n-channel partially salicided TFTs with in-situ doped gate. We find that the V_{TH} roll-off of partially salicided TFTs with in-situ doped gate is significantly influenced by the different RTA conditions and the FSA-TFTs have more positive and stable V_{TH} compared with partially salicided TFTs. In the partially salicided TFTs, higher RTA temperature results in more positive V_{TH} and partially Ni-silicided gate results in unstable and unexpected V_{TH} with different RTA condition. It is also found that short channel (L = 0.8μm) partially salicided TFTs have the approximate V_{TH} near the V_{TH} of short channel FSA-TFTs.

Figure 3.10 illustrates the relationship of V_{TH} shift versus V_{DS} for the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm. The reference drain voltage is 0.5V. The enhanced V_{TH} shift is observed in conventional TFTs at large drain voltage. The reduced V_{TH} shifts of FSA-TFTs strongly support that floating-body and parasitic BJT effects are significantly suppressed by the

fully-silicided source/drain structure [3.10].

3.3.3 p-Channel FSA-TFTs

The measured transfer characteristics and field-effect mobility of the p-channel conventional and the p-channel FSA-TFTs with W / L = 10μm / 0.8μm are shown in Fig.3.11 and Fig.3.12 respectively. In short channel p-channel TFTs, the on-state currents and field-effect mobility of the FSA-TFTs are higher than those of the conventional TFTs. The off-state leakage currents of FSA-TFTs are identical to these of the conventional TFTs. The electrical characteristics improvements of p-channel FSA-TFTs are similar to n-channel FSA-TFTs except improvement of off-state leakage currents. The on-state currents are significantly limited by the parasitic S/D resistance in short-channel conventional TFTs. For the conventional TFTs with short channel length of 0.8 μm, the field-effect mobility is seriously degraded when gate voltage $V_G > -9.0V$, but it is not found in short channel FSA-TFTs. The high field-effect mobility of p-channel FSA-TFTs is due to the fully Ni-salicided source/drain and gate structure, which has smaller parasitic S/D resistance, higher capacitance and superior scalability than the conventional TFTs with poly-Si gates [3.16]. The p-channel FSA-TFTs also show improved subthreshold characteristics.

The measured output characteristics of the p-channel conventional and the p-channel FSA-TFTs with W / L = 10μm / 0.8μm are shown in Fig.3.13. Obviously FSA-TFTs exhibit larger driving currents than conventional TFTs in short channel devices. The high driving currents of FSA-TFTs can be attributed to the fully Ni-salicided source/drain and gate structure. The short channel FSA-TFTs have more saturated output characteristics and increased drain breakdown voltage compared with conventional TFTs. In p-channel TFTs, it strongly supports that parasitic BJT effects are significantly suppressed by the fully-silicided source/drain structure [3.10].

The parasitic resistance R_P of (a) p-channel FSA-TFTs with undoped gate and (b) p-channel conventional TFTs, in the linear region, is extracted by plotting measured on state resistance (R_{ON}) versus gate length (L_G), as shown in Figs.3.14. The R_P of FSA-TFTs with undoped gate is about 387 Ω and the Lo of FSA-TFTs with undoped gate is near 0 μm. The R_P of conventional TFTs is about 8.80 kΩ. The on-state currents and field-effect mobility are significantly improved by reducing R_P in the p-channel FSA-TFTs [3.14], [3.15].

Figure 3.15 displays the on / off current ratio (I_{ON} / I_{OFF}) of the p-channel conventional and the p-channel FSA-TFTs with W =10μm. The on-state current is defined as drain current (I_D) at V_G = -15.0 V, V_{DS} = -3.0 V and the off-state current is defined as minimum drain current (I_{min}) at V_{DS} = -3.0 V. The I_{ON} / I_{OFF} (10^8~10^9) can be increased with scaling down channel length in FSA-TFTs. It is not like n-channel conventional TFTs, the I_{ON} / I_{OFF} (10^7~10^8) of p-channel conventional TFTs is increased with scaling down channel length. The enhancement of off-state leakage currents is not observed in short-channel p-channel conventional TFTs due to slight floating-body effect and weak hole drain impact ionization.

Figure 3.16 displays the extracted threshold voltage V_{TH} of the p-channel conventional and the p-channel FSA-TFTs with different gate lengths (defined as I_D = W / L × 10 nA at V_{DS} = -0.5 V). The V_{TH} roll-off is greatly improved in FSA-TFTs. The threshold voltage absolute values $|V_{TH}|$ of FSA-TFTs are smaller than conventional TFTs due to improved S.S. in FSA-TFTs. We believe that the stable V_{TH} and improved S.S. of the p-channel FSA-TFTs result from the fully Ni-silicided gate and S/D structure.

3.4 Summary

We have developed the n-channel and p-channel fully Ni-self-aligned silicided S/D and gate poly-Si thin-film transistors. In n-channel TFTs, the FSA-TFTs show reduced kink effect, increased drain breakdown voltage, stable V_{TH} roll-off, improved S.S., low parasitic S/D resistance, higher field-effect mobility and increased on /off current ratio. The p-channel FSA-TFTs were also fabricated with improved devices performance. The parasitic resistance of S/D and gate is greatly reduced and allows it possible to recover the intrinsic characteristics of thin-channel TFTs. The FSA-TFTs with low thermal budget fully Ni-salicidation processes are proved to be a very promising structure with low parasitic S/D resistance and high gate capacitance ability for 3D integration applications and high-performance driver circuits in the AMLCDs.

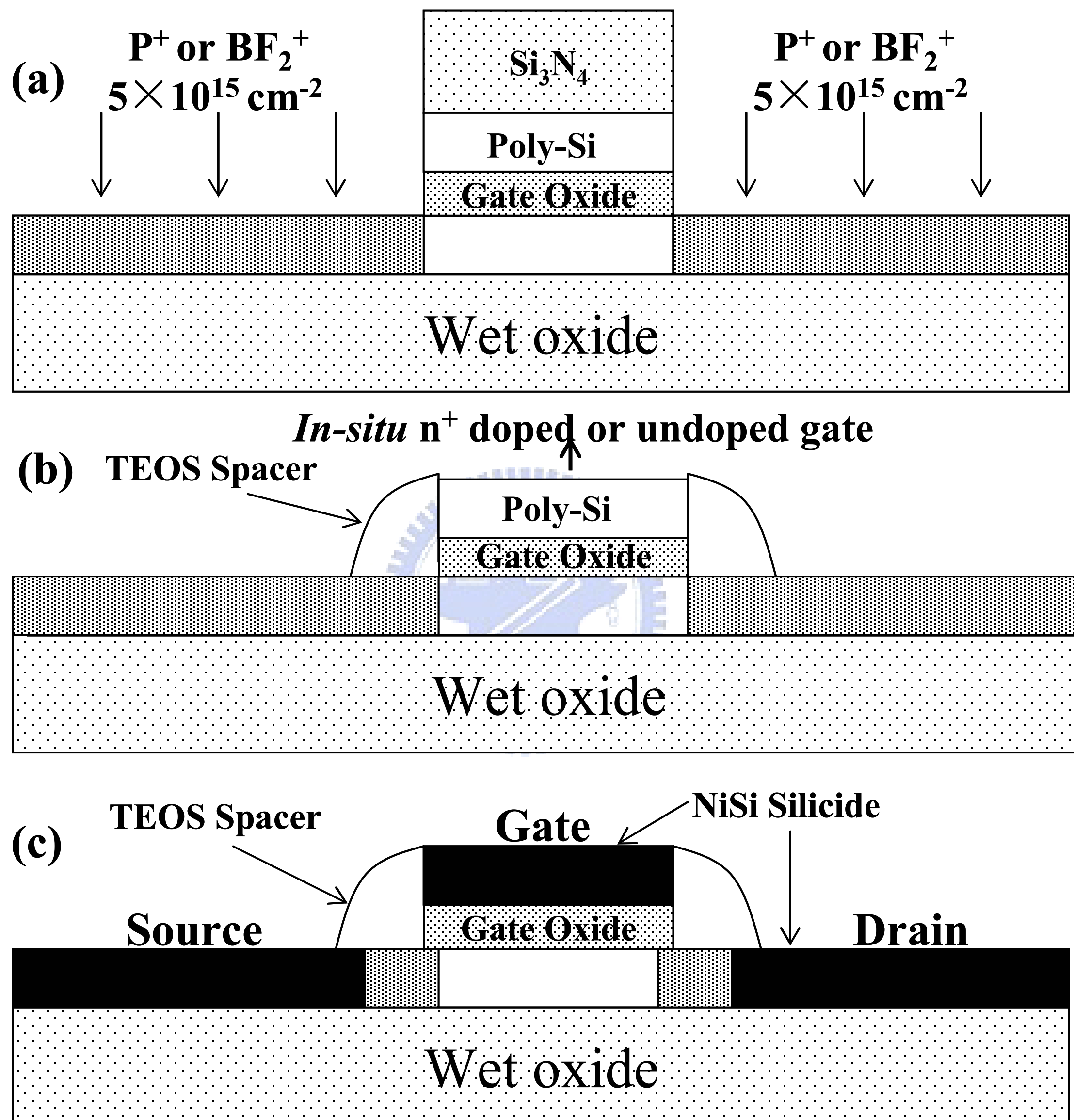


Fig. 3.1 The main process flow of FSA-TFTs.

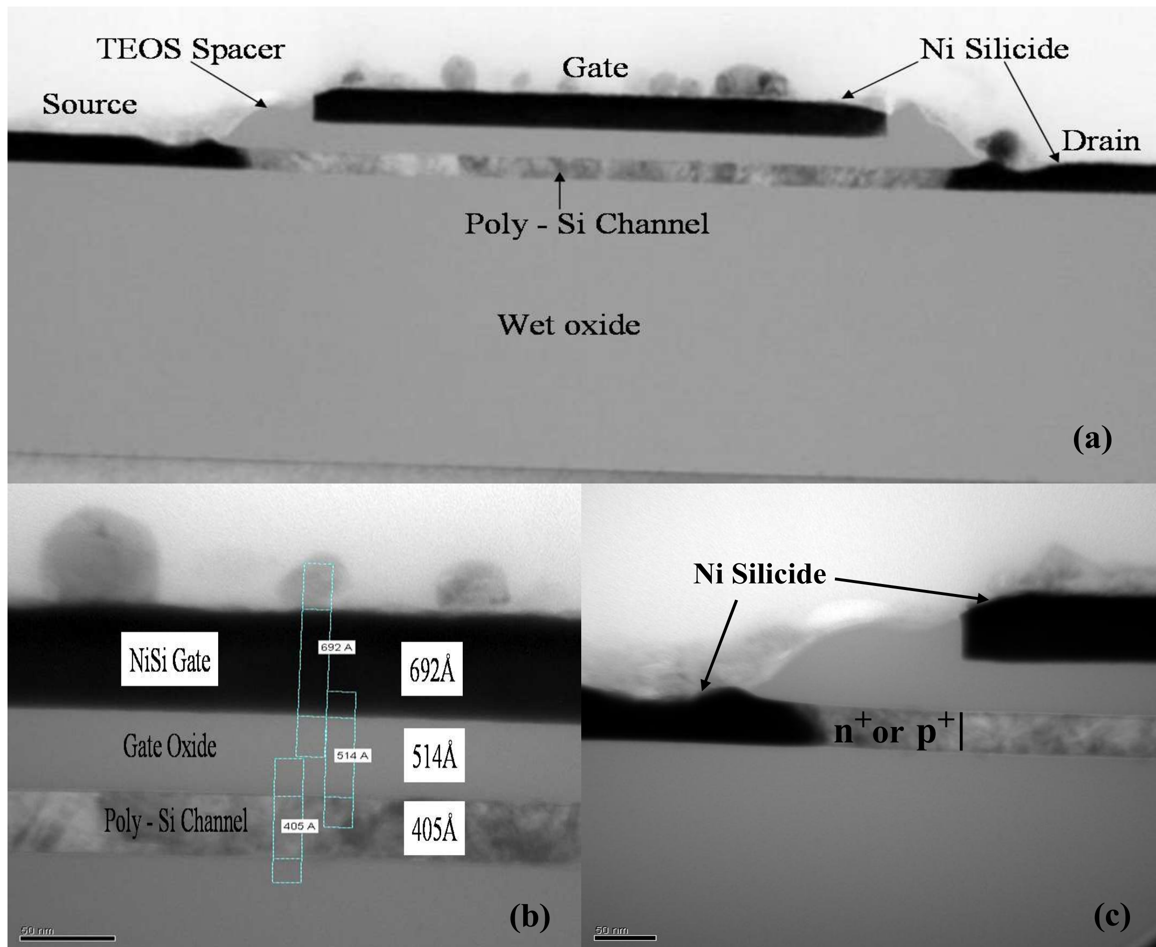


Fig. 3.2 The cross-sectional transmission electron microscopy (TEM) micrographs of FSA-TFTs with gate length = 0.8μm and channel thickness = 40nm.

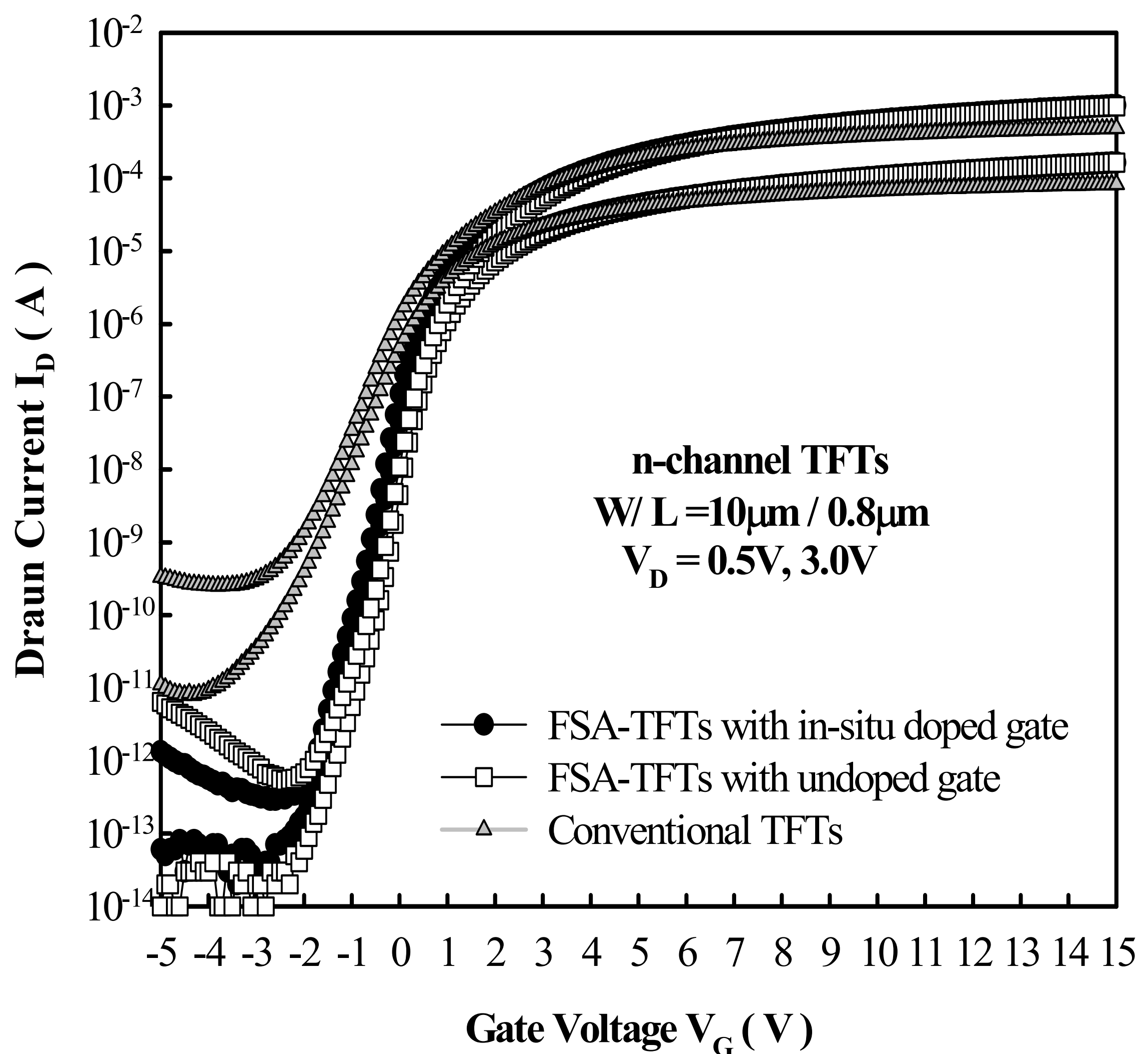


Fig. 3.3 The measured transfer characteristics of the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm.

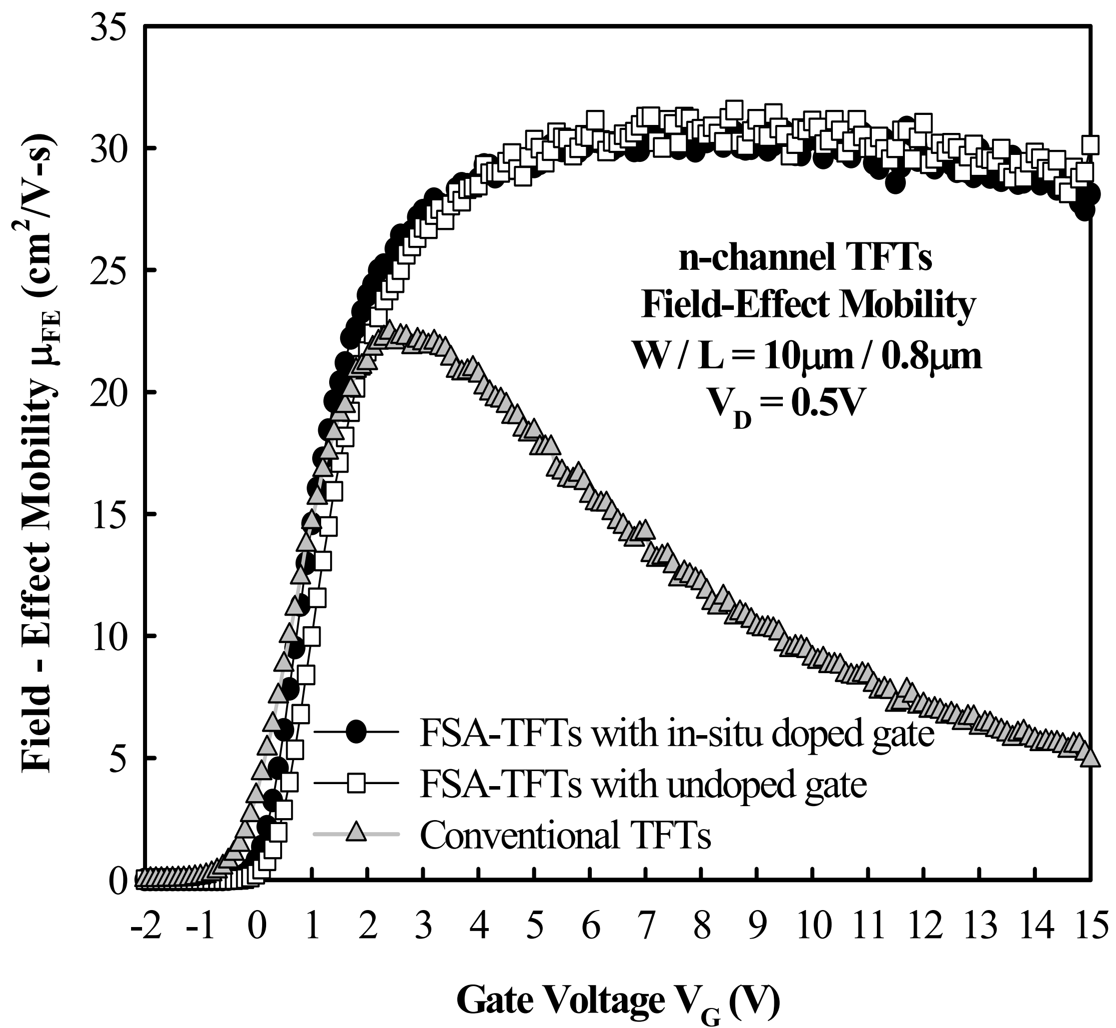


Fig. 3.4 The field-effect mobility of the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm.

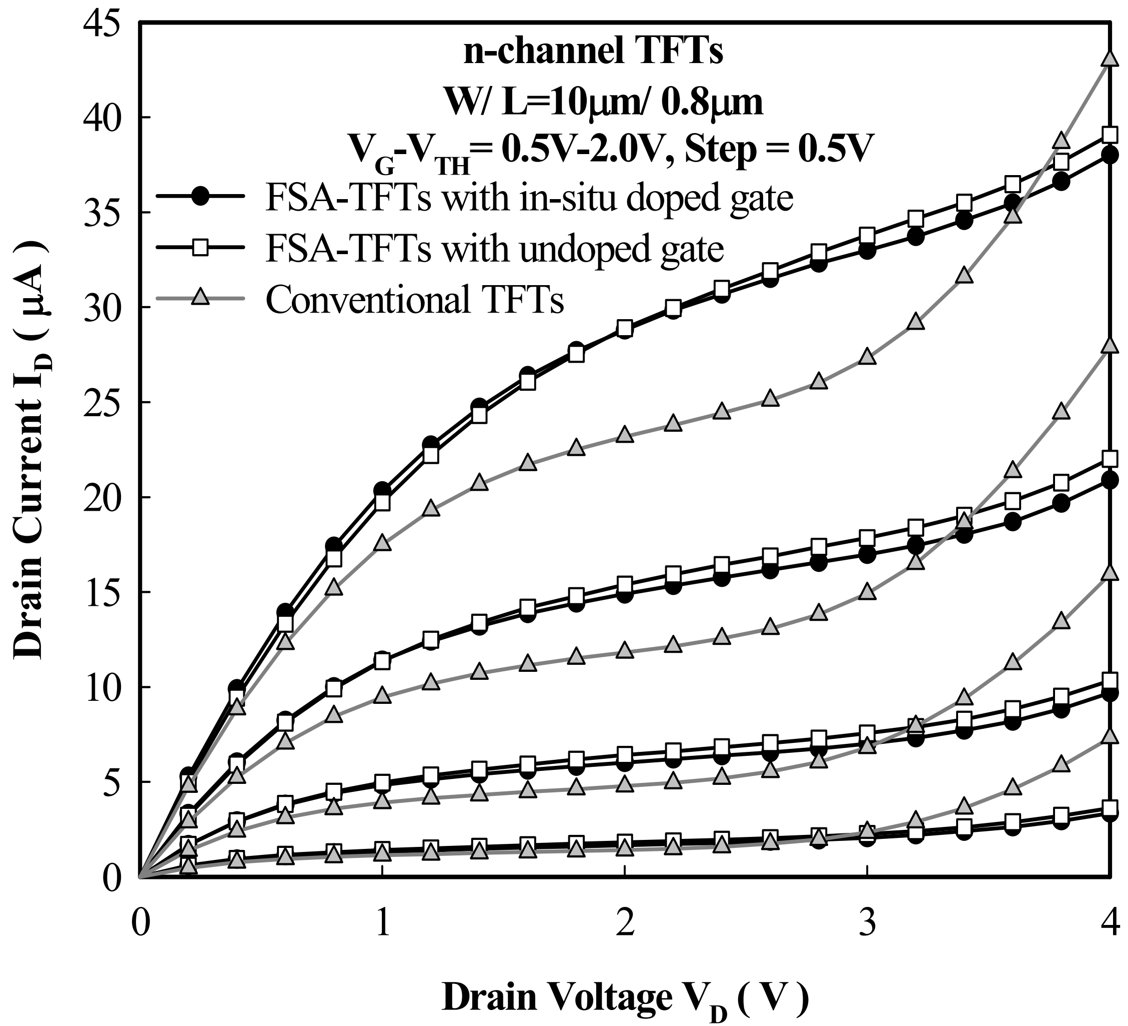


Fig. 3.5 The measured output characteristics of the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm.

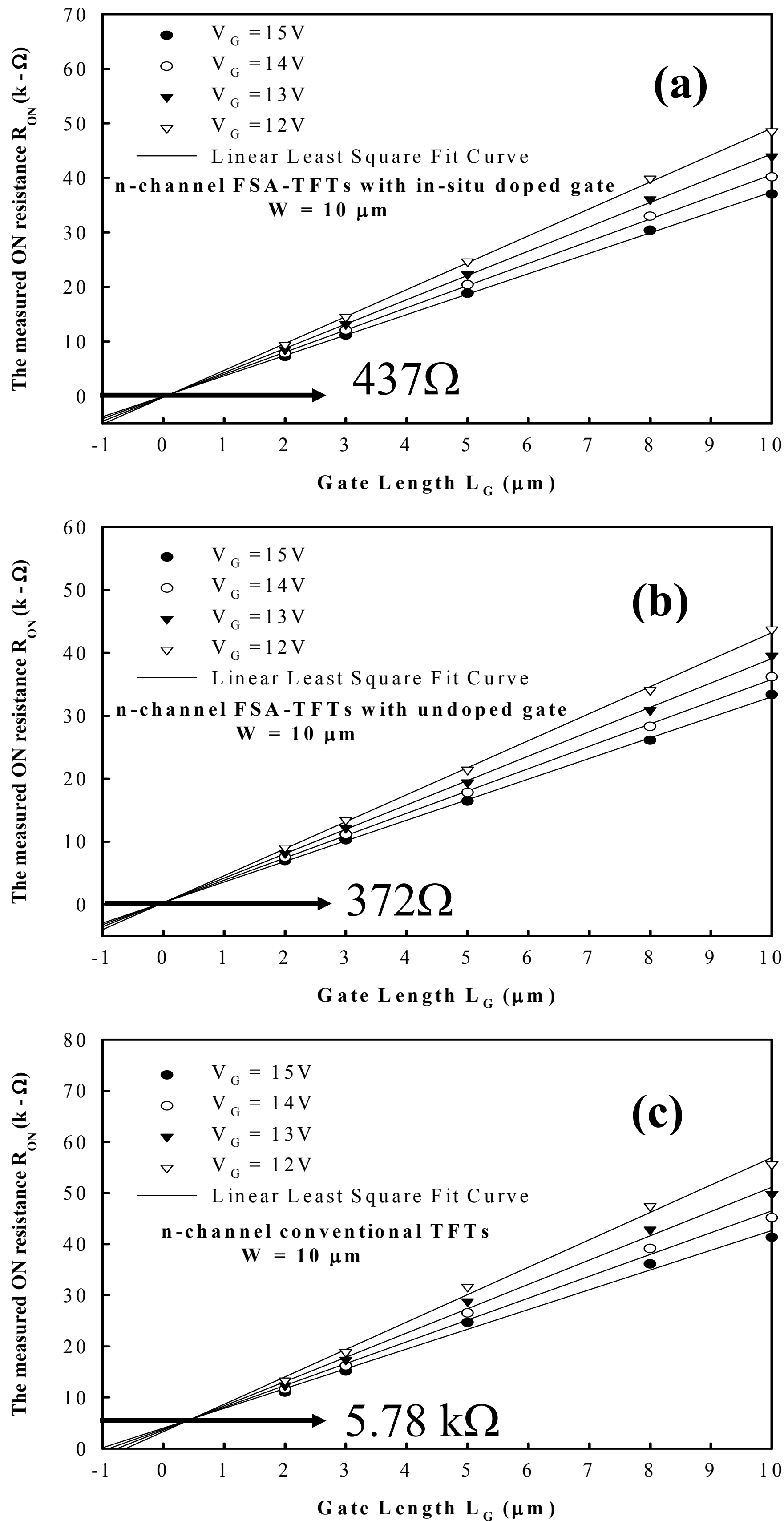


Fig. 3.6 The parasitic resistance R_P of (a) n-channel FSA-TFTs with in-situ doped gate, (b) n-channel FSA-TFTs with undoped gate and (c) n-channel conventional TFTs, in the linear region, is extracted by plotting measured on state resistance (R_{ON}) versus gate length (L_G).

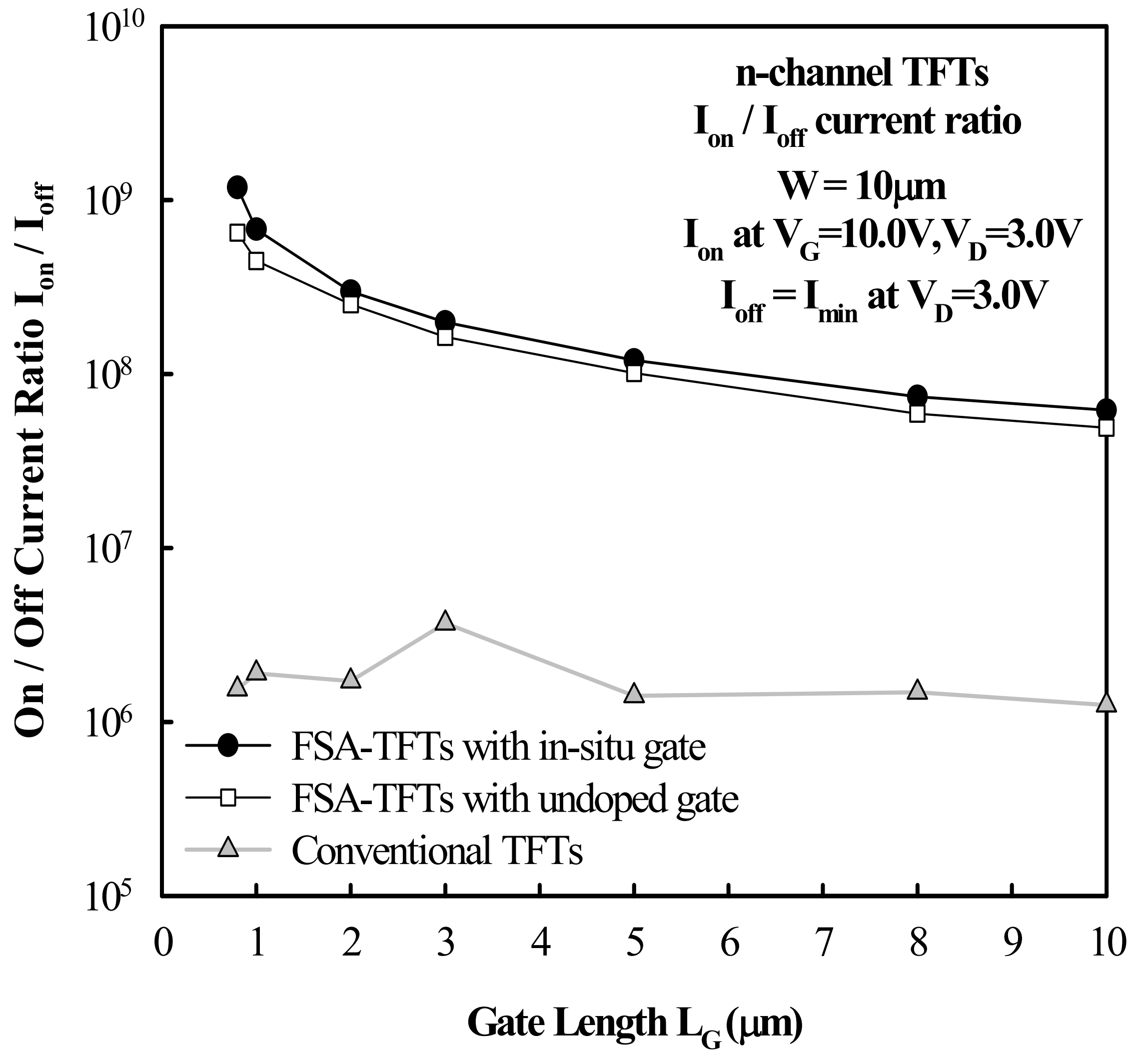


Fig. 3.7 The on / off current ratio (I_{ON} / I_{OFF}) of the n-channel conventional and the n-channel FSA-TFTs with W =10μm. The on-state current is defined as drain current (I_D) at V_G = 10.0 V, V_{DS} = 3.0 V and the off-state current is defined as minimum drain current (I_{min}) at V_{DS} = 3.0 V.

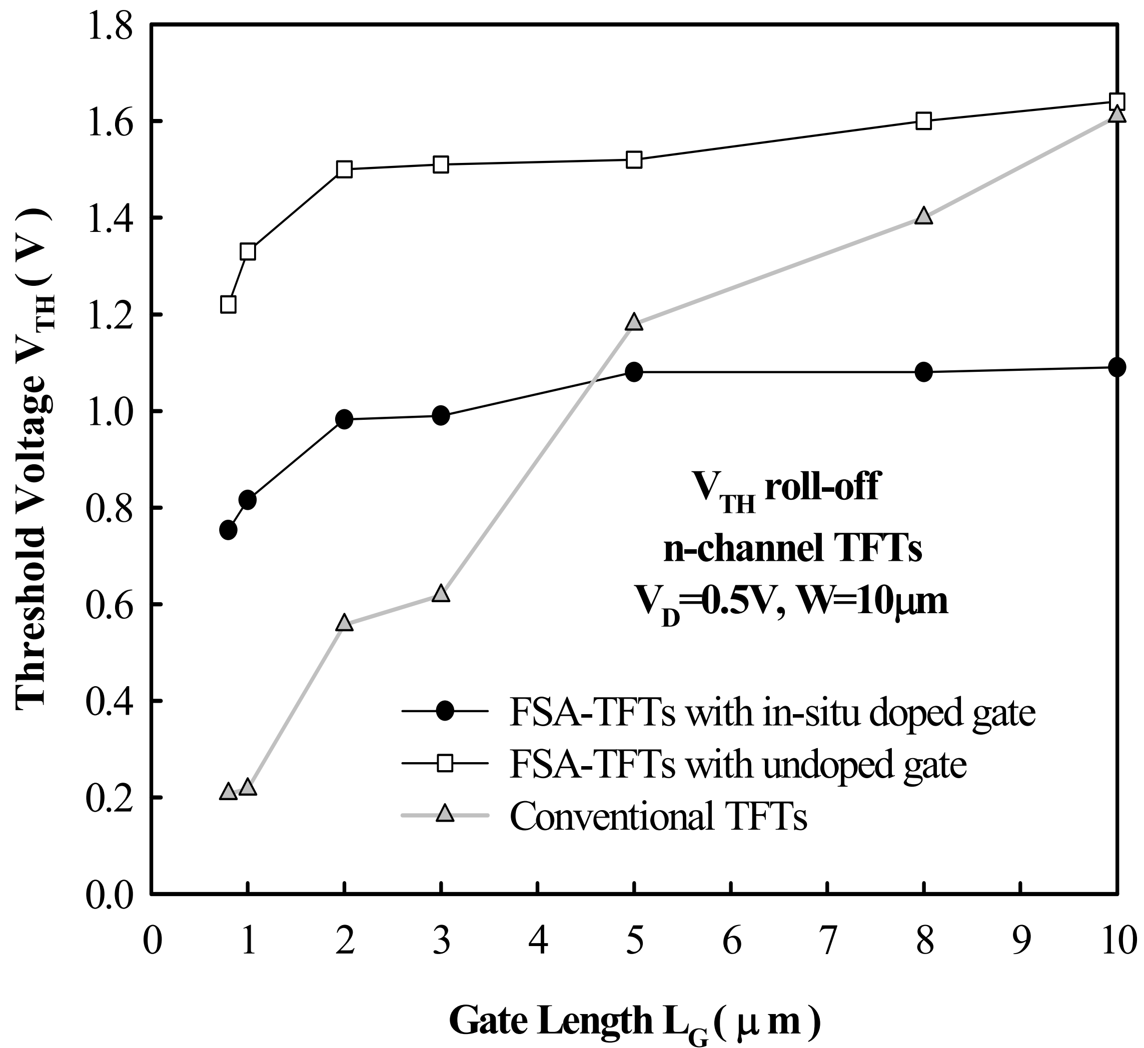


Fig. 3.8 The extracted threshold voltage V_{TH} of the n-channel conventional and the n-channel FSA-TFTs with different gate lengths (defined as $I_D = W / L \times 100$ nA at $V_{DS} = 0.5$ V).

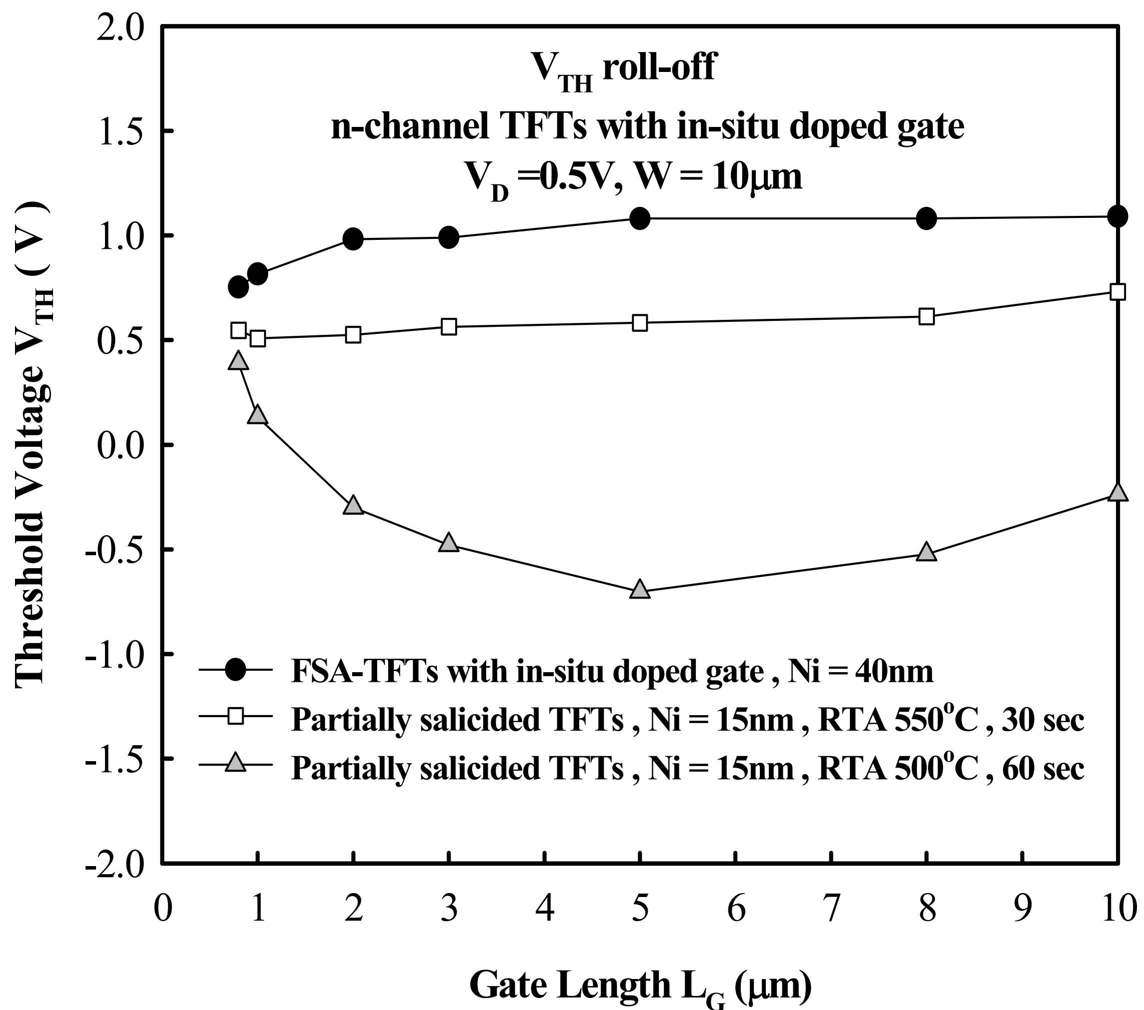


Fig. 3.9 The extracted V_{TH} roll-off of the n-channel FSA-TFTs with in-situ doped gate and n-channel partially salicided TFTs with in-situ doped gate. The partially salicided TFTs were form by RTA 500°C for 60-sec and RTA 550°C for 30-sec.

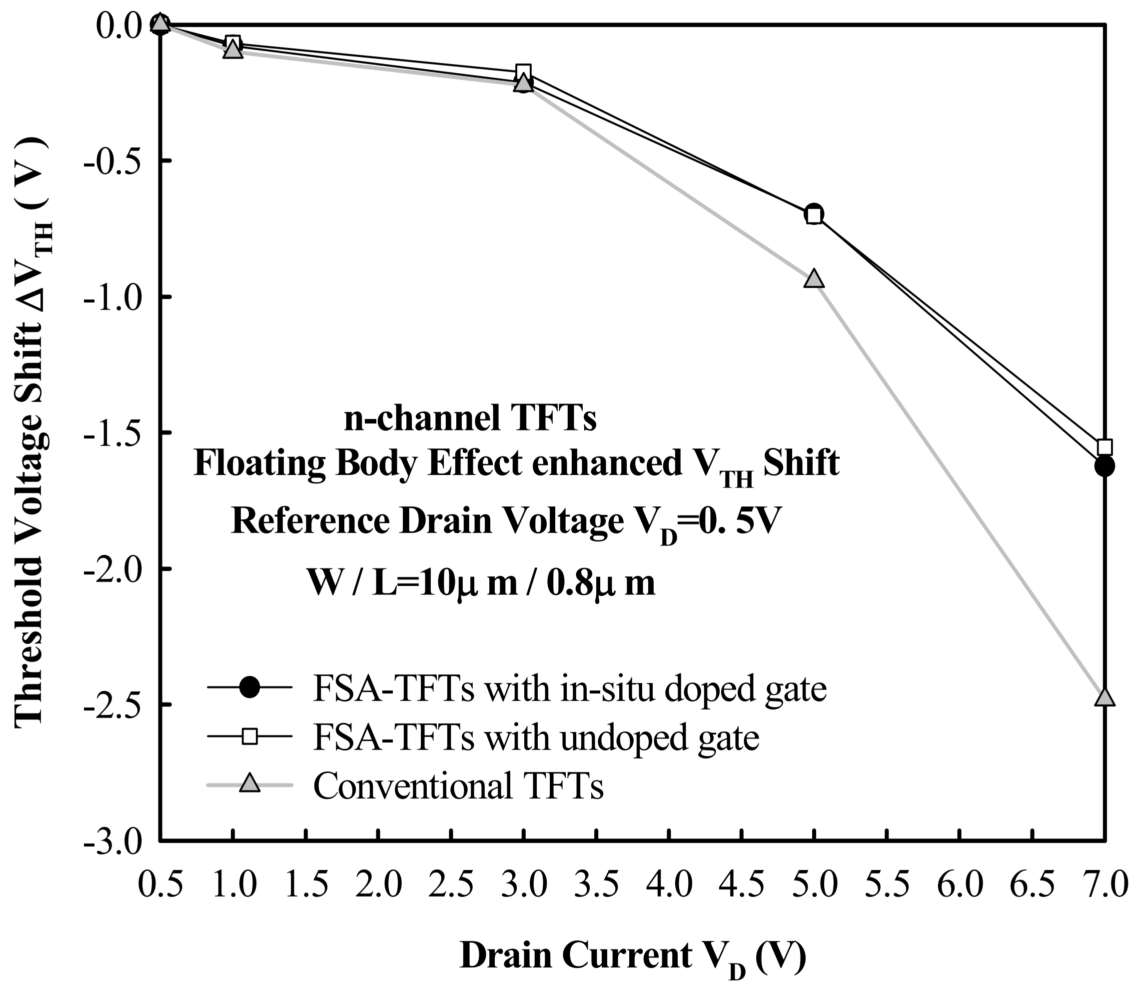


Fig. 3.10 Threshold voltage shift (ΔV_{TH}) versus drain voltage V_{DS} characteristics for the n-channel conventional and the n-channel FSA-TFTs with W / L = 10μm / 0.8μm. The reduced V_{TH} shift for the n-channel FSA-TFTs exhibits suppressed floating body effect.

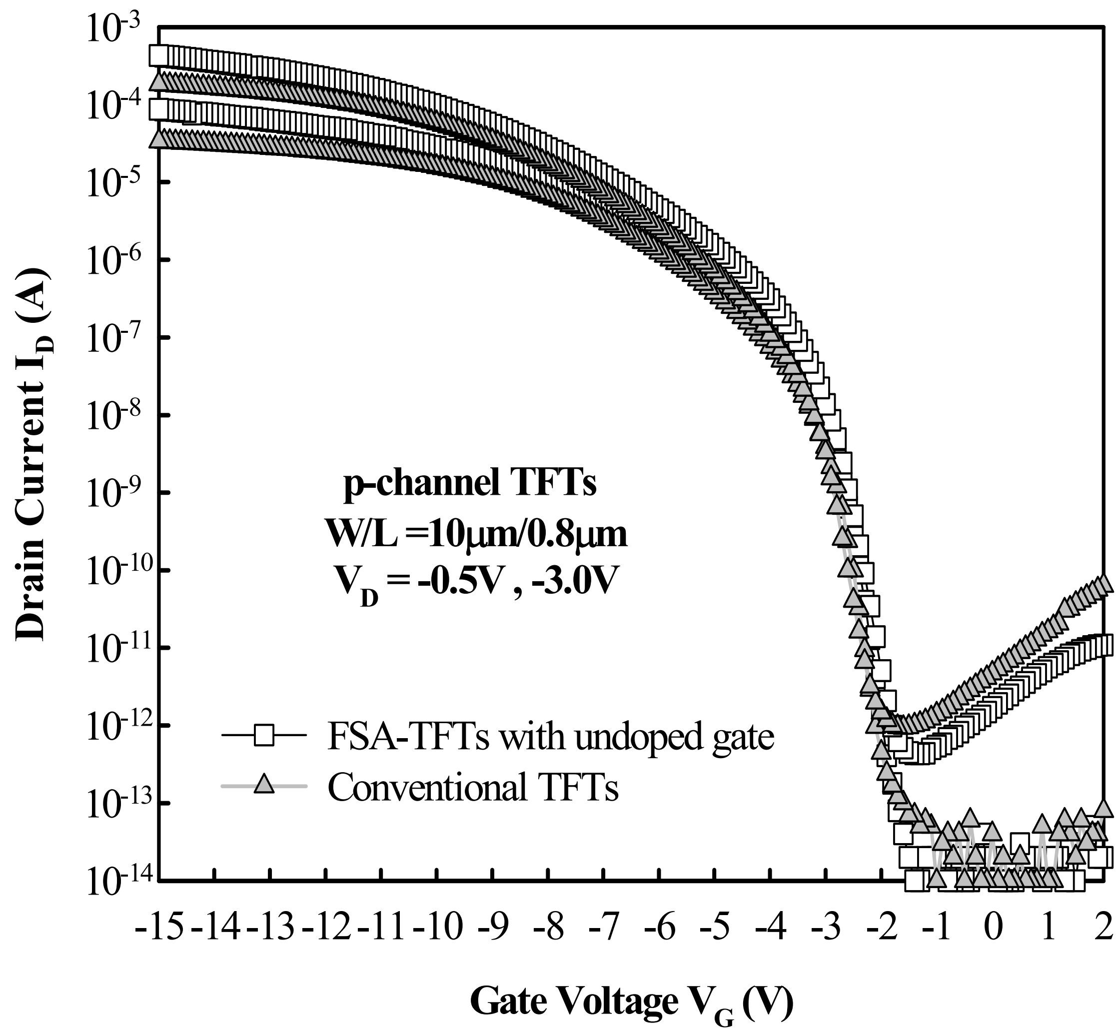


Fig. 3.11 The measured transfer characteristics of the p-channel conventional and the p-channel FSA-TFTs with W / L = 10μm / 0.8μm.

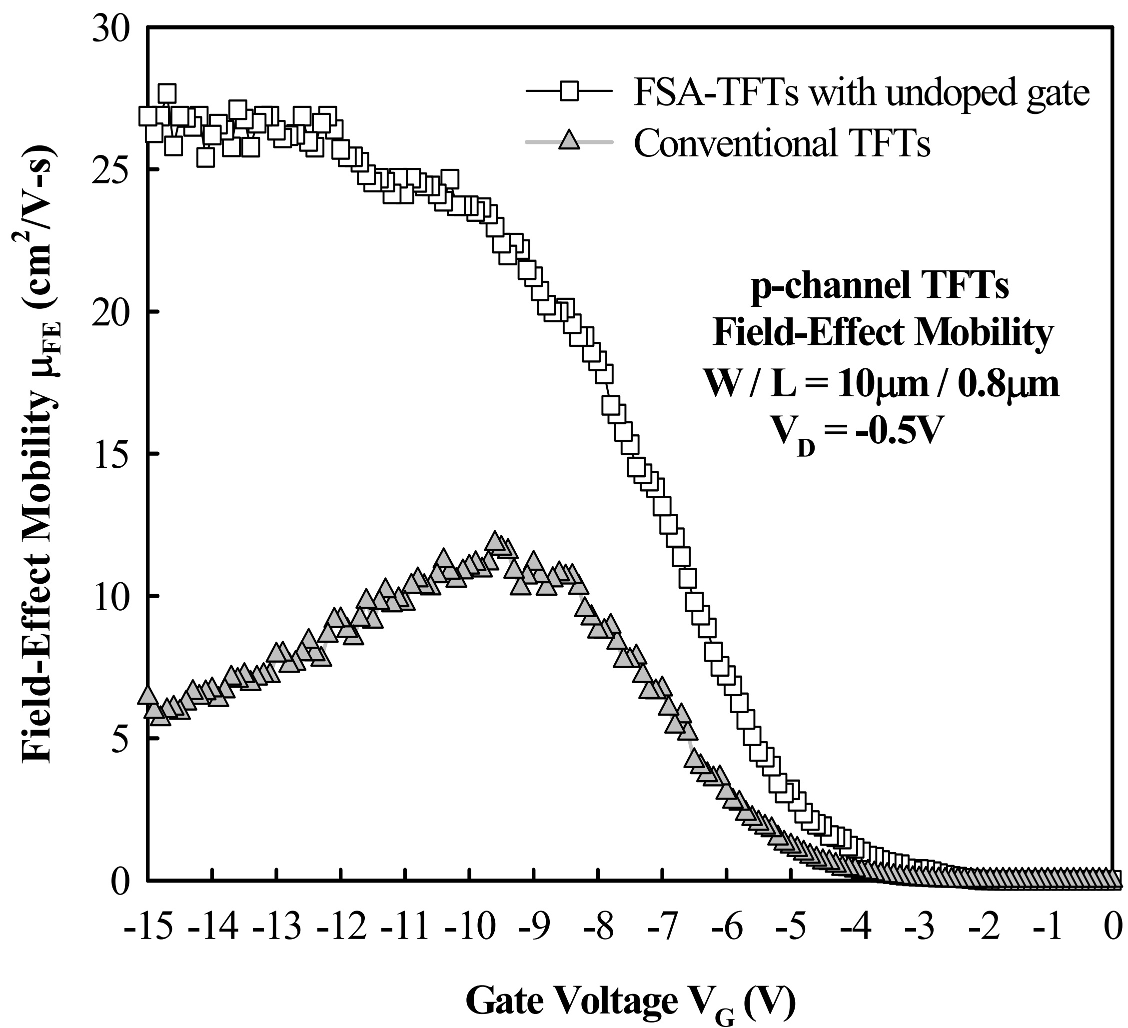


Fig. 3.12 The field-effect mobility of the p-channel conventional and the p-channel FSA-TFTs with W / L = 10μm / 0.8μm.

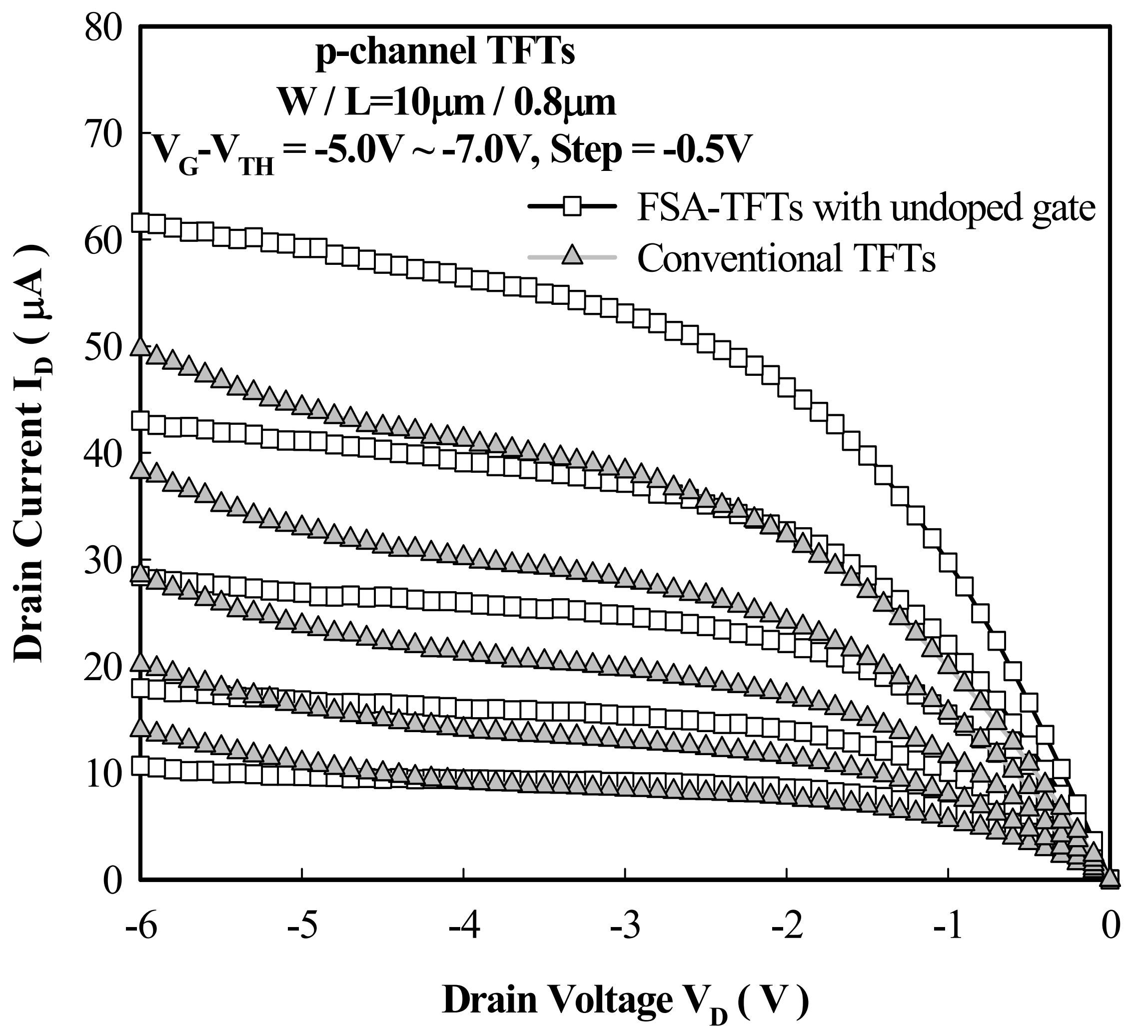
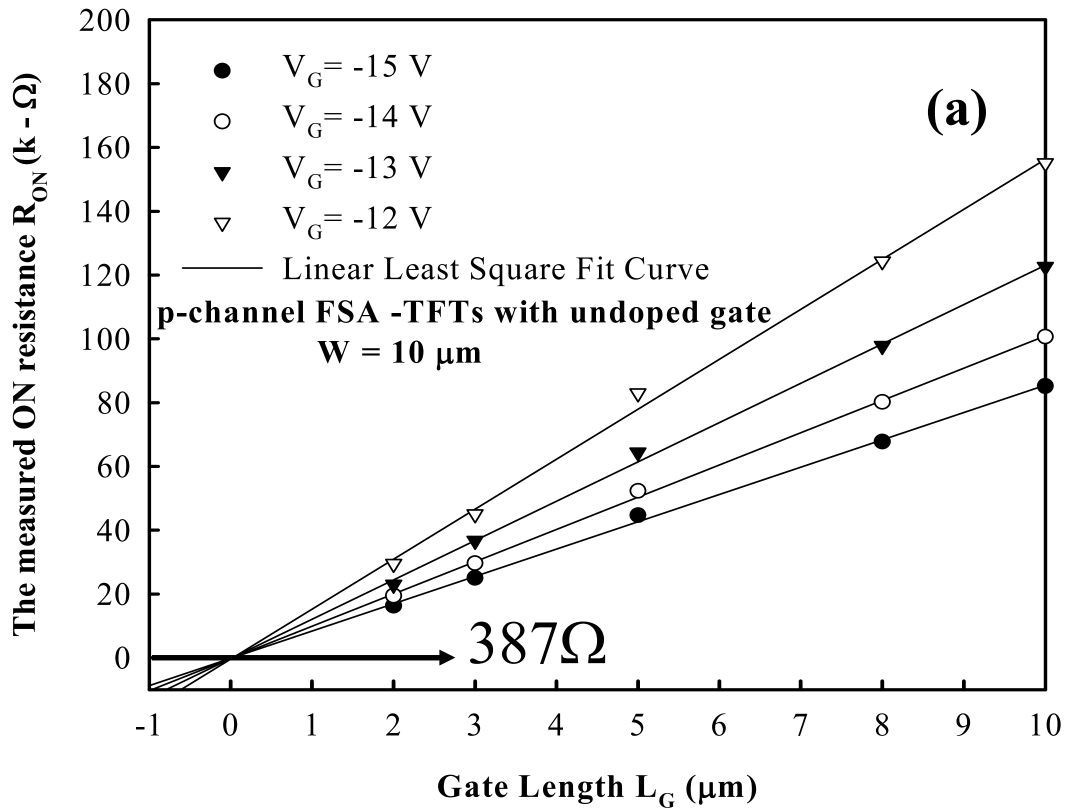


Fig. 3.13 The measured output characteristics of the p-channel conventional and the p-channel FSA-TFTs with W / L = 10μm / 0.8μm.



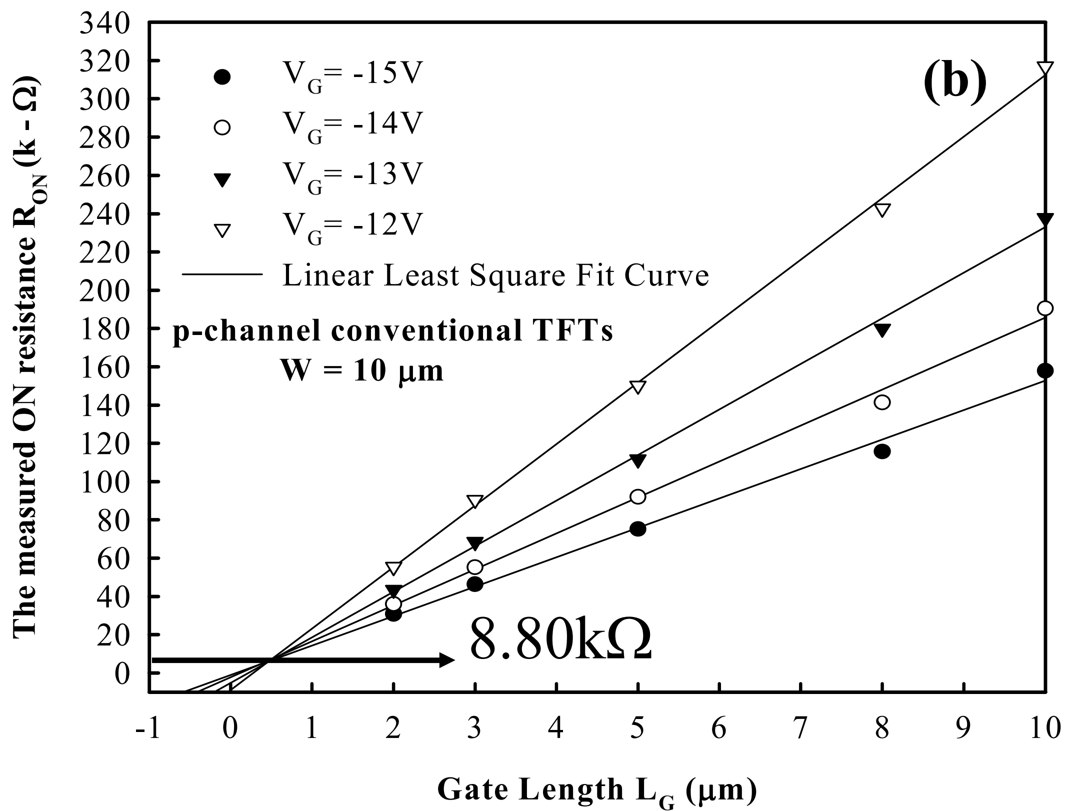


Fig. 3.14 The parasitic resistance R_P of (a) p-channel FSA-TFTs with undoped gate and (b) p-channel conventional TFTs, in the linear region, is extracted by plotting measured on state resistance (R_{ON}) versus gate length (L_G).

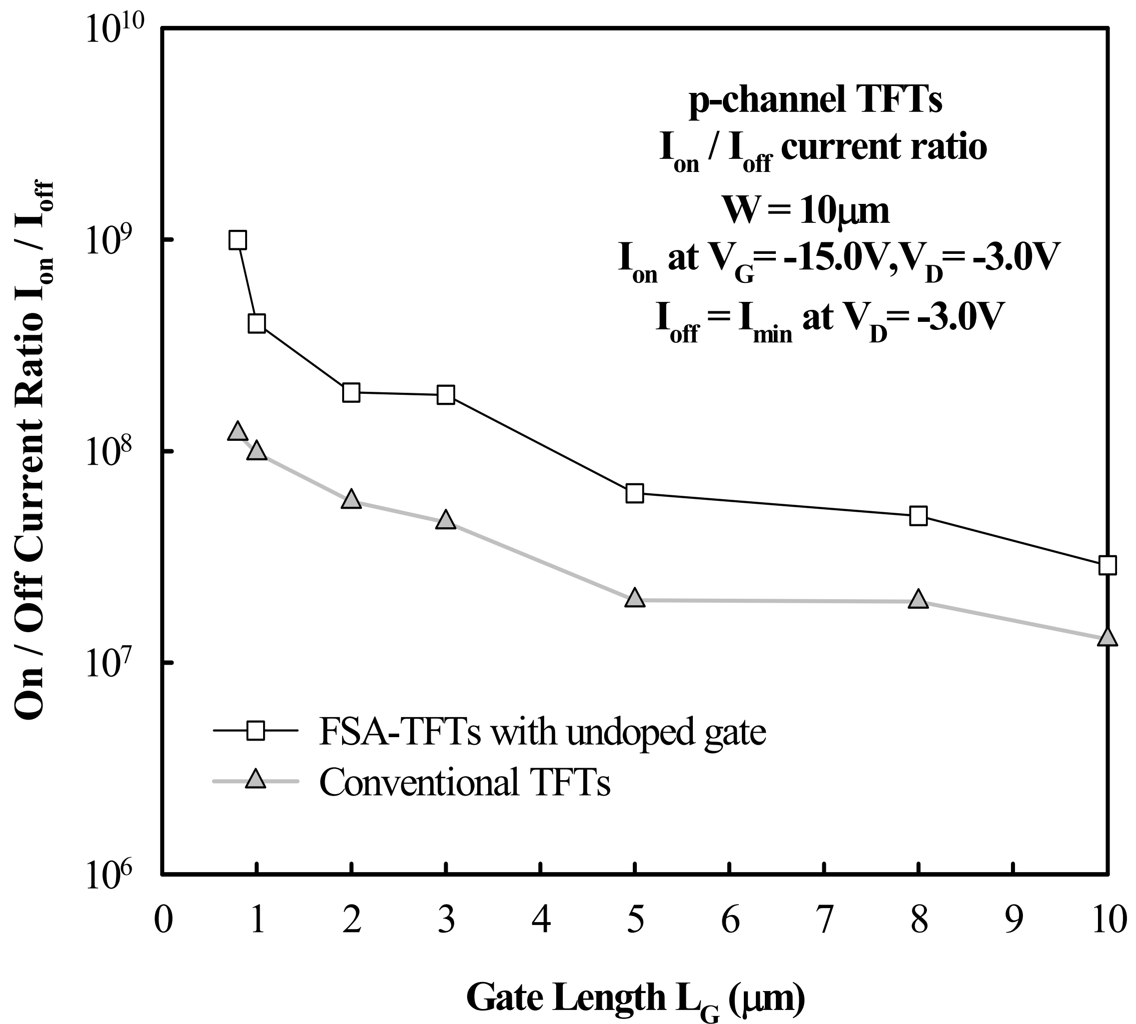


Fig. 3.15 The on /off current ratio (I_{ON} / I_{OFF}) of the p-channel conventional and the p-channel FSA-TFTs with W =10μm. The on-state current is defined as drain current (I_D) at V_G = -15.0 V, V_{DS} = -3.0 V and the off-state current is defined as minimum drain current (I_{min}) at V_{DS} = -3.0 V.

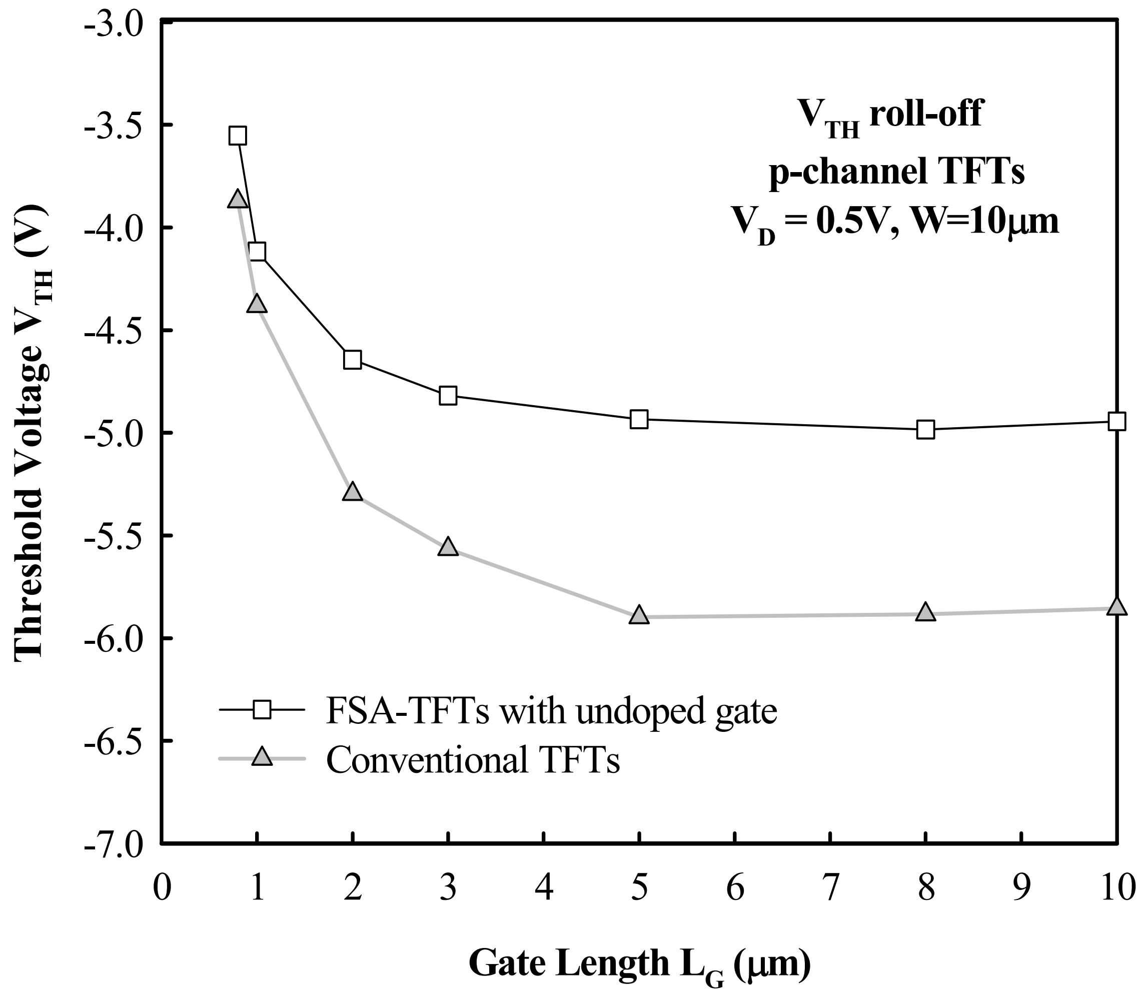


Fig. 3.16 The extracted threshold voltage V_{TH} of the p-channel conventional and the p-channel FSA-TFTs with different gate lengths (defined as $I_D = W / L \times 10$ nA at $V_{DS} = -0.5$ V).

Chapter 4

Novel Symmetric Vertical n-Channel Poly-Si Thin-Film Transistors Fabricated by Ni-Silicide Induced Lateral Crystallization Technology

4.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have the potential advantages of silicon-on-insulator (SOI) MOSFETs such as simple fabrication process, good device-to-device isolation, high circuit density, and high device performance as well as the possibility to be applied in vertical 3-D integration. Recently, poly-Si TFTs technology has been receiving more attention because it is a promising mean of achieving 3-D integration, which has been utilized in various 3-D circuits [4.1]-[4.3].

However, the application of poly-Si TFTs is mainly limited in low-temperature flat-panel display. Conventional poly-Si TFTs suffer from serious poor device characteristics and device-to-device variations resulted from the grain boundaries in the channel region. It is believed that electrical characteristics of the poly-Si TFTs can be improved if the poly-Si grain size can be enhanced and the number of grain boundaries in the channel can be reduced. Metal-Induced-Lateral-Crystallization (MILC) technology has been studied in the past to achieve large and regular poly-Si grain from amorphous silicon [4.4]-[4.6]. In addition, vertical thin film transistors (VTFT's) are suitable for high density 3-D integration since their channel length are

determined by the thicknesses of SiO_2 or poly-Si films instead of the photolithographic limitation. Many works had been devoted to developing and studying VTFTs [4.7], [4.8].

We have successfully developed and fabricated the novel symmetric vertical n-channel poly-Si TFTs fabricated by Ni-silicide induced lateral crystallization technology (NSILC-VTFTs). The NSILC-VTFTs were fabricated by combining NSILC process and vertical poly-Si channel. The NSILC-VTFTs are S/D symmetric devices and equivalent to dual-gate devices. In the dual-gate devices, a n^+ floating region is included in the channel region between S/D. The Ni-accumulation and grain boundaries induced from S/D sides can be centralized in the n^+ floating region. The dual-gate structure is employed to eliminate the grain boundaries perpendicular to the current flow in the channel [4.9], [4.10].

In this chapter, the effects of grain boundaries in the vertical channel and n^+ floating region crystallized by NSILC or MILC processes are studied. The NSILC-VTFTs can eliminate metal contaminations on source and drain region due to the limited Ni source from Ni-silicided seeding window arranged on source and drain contact holes. When the device L_{mask} and W_{mask} are scaled down, the probability of the channel region in NSILC-VTFTs to cover grain boundaries in the length and width direction decreases significantly [4.3]. The NSILC-VTFTs with small L_{mask} and W_{mask} have better device performance and higher uniformity. Furthermore, we have discovered that amorphous silicon was crystallized by two steps: first step lateral crystallization at 500°C for 12-hr and second step rapid thermal annealing (RTA) at 700°C for 60-sec, the grain size of the resulting poly-Si can be significantly enhanced and device characteristics can be further improved [4.11]-[4.13]. In order to investigate the impact of grain boundaries in the vertical channel and n^+ floating region, all the devices were fabricated without further NH_3 plasma treatment. The

measured results show the NSILC-VTFTs without NH_3 plasma treatment have high field-effective mobility, small subthreshold swing (S.S.), and low off-state leakage current.

4.2 Experiment

Figures 4.1 show the key process flows of NSILC-VTFTs and MILC-VTFTs. First, bare silicon covered with 5500 Å-thick SiO_2 was used as the glass substrate. A 2500 Å-thick polysilicon thin film was deposited for gate by low pressure chemical vapor deposition (LPCVD). After gate patterning, a 1000Å oxide undercut was etched to form gate offset region. A 500Å-thick TEOS gate oxide thin film was deposited by LPCVD and then a 500Å-thick a-Si was deposited by LPCVD to form S/D and channel active region.

After the active region patterning, a 4000Å low temperature passivation oxide was deposited by HDPCVD (high density plasma chemical vapor deposition) at 350^oC. Next, Ni-offset mask pattern was formed in the contact hole region. A stacked 100Å/100Å TiN/Ni thin film was deposited on the contact hole of the devices. We used two methods to complete channel poly-Si crystallization process: one is conventional MILC process; another is our new NSILC process. The MILC-VTFTs were fabricated without RTA Ni-silicidation processes. In the NSILC-VTFTs, the Ni-silicidation of NSILC was achieved by RTA (rapid thermal annealing) at 450^oC for 30-sec before lateral crystallization. Next, the residue Ni was removed by H_2SO_4 : H_2O_2 solution (Fig.4.1a). Both methods were crystallized by first step lateral crystallization at 500^oC for 12-hr (Fig.4.1b). Table 4.1 shows the split table of the devices. In order to investigate the impact of grain boundaries in the vertical channel and n^+ floating region crystallized by one step NSILC or MILC processes,

NSILC-VTFTs and MILC-VTFTs were crystallized by only first step lateral crystallization (500°C for 12-hr). The channel active region of conventional TFTs was crystallized by solid phase crystallization (SPC) at 600°C for 24-hr. In order to investigate the effects of secondary grain crystallization by two steps NSILC and RTA processes. The NSILC-VTFTs (RTA) were crystallized by two steps: first step lateral crystallization (500°C for 12-hr) and second step RTA (700°C for 60-sec).

After removing the low temperature oxide, the 15kev, $5x10^{15}$ cm^{-2} As^{+} self-aligned n^{+} S/D ion implantations were performed (Fig.4.1c). Dopants were activated by RTA at 580°C for 60-sec. After passivation, contact, and metallization processes, all the devices were fabricated without NH_3 plasma treatment for studying influences of grain boundaries in the vertical channel and n^{+} floating region (Fig.4.1d).

4.3 Results and Discussion

4.3.1 Devices Structure and TEM Results

Figure 4.2 displays the schematic device cross-section structure of NSILC-VTFTs. The NSILC-VTFTs are equivalent to dual-gate device structures. In this work, the effective channel length of NSILC- VTFTs is defined by 2 × total thickness of poly-Si gate and gate oxide (poly-Si gate thickness = 2500 Å and gate oxide thickness = 500Å). The effective channel length of NSILC-VTFTs is about 0.6μm. In the dual-gate devices, a n^{+} floating region was included in the channel region between S/D. Applying the dual-gate structure can suppress the electrical field in the drain depletion region, significantly reducing the leakage current of the NSILC-VTFTs, increasing the Ion / Ioff current ratio [4.9], [4.14].

The plan view optical microscope microphotograph of NSILC-VTFTs is shown in Fig.4.3. The length of n^{+} floating region is defined by the mask channel length (L_{mask}).

The mask channel width (W_{mask}) is equal to effective channel width of NSILC-VTFTs. The NSILC-VTFTs with different L_{mask} and W_{mask} have different device performance due to the effects of grain boundaries in the vertical channel and n^+ floating region.

Figures 4.4 show (a) transmission electron diffraction (TED) pattern of vertical poly-Si channel in NSILC-VTFTs and (b) cross-section transmission electron microscope (TEM) microphotograph of NSILC-VTFTs. The integrity of the vertical poly-Si channel is verified by the TED pattern as shown in Fig. 4.4(a). The dots in TED pattern confirm that single crystal is locally achieved. In the Fig.4.4 (b), the gate oxide thickness and channel thickness are both 500Å. The poly-Si gate thickness and undercut depth of gate offset region are 2500Å and 1000 Å respectively. The undercut depth of gate offset region is designed by the total thickness of gate oxide and channel (500Å + 500Å = 1000Å) for the purpose of n^+ S/D top edge and poly-Si gate bottom edge in the same horizontal level. In the NSILC-VTFTs, the off-state leakage current can be reduced by the self-aligned undercut gate offset without additional masking step, which makes the fabrication simple and easy [4.8].

4.3.2 Ni Accumulation in Floating Region after MILC and NSILC Processes

Figures 4.5 display (a) the plan view optical microscope microphotograph of test key after MILC process at 500°C for 24-hr and (b) the plan view optical microscope microphotograph of test key after NSILC process at 500°C for 12-hr. The excess Ni accumulation of grain boundaries is found in the MILC process but it is not found in the NSILC process. The length of poly-Si crystallized by NSILC process at 500°C for 12-hr is about 20μm. In the devices, the Ni-accumulation and grain boundaries induced from S/D sides can be centralized in the n^+ floating region. Figures 4.6

indicate (a) the plan view optical microscope microphotograph of MILC-VTFTs after annealing at 500°C for 12-hr and (b) the plan view optical microscope microphotograph of NSILC-VTFTs after annealing at 500°C for 12-hr. The excess Ni accumulation of the n^+ floating region is found in the MILC-VTFTs but it is not found in the NSILC-VTFTs. Compared with MILC-VTFTs, the NSILC-VTFTs can eliminate metal contaminations on source and drain region due to the limited Ni source from Ni-silicided seeding window arranged on source and drain contact holes.

4.3.3 Comparison of NSILC-VTFTs, MILC-VTFTs, and Conventional TFTs

Figure 4.7 shows the transfer characteristics of conventional TFTs and NSILC-VTFTs. The effective channel length of NSILC-VTFTs is 0.6μm. The W_{mask} / L_{mask} of conventional TFTs and NSILC-VTFTs is 0.8μm / 0.8μm. The NSILC-VTFTs have smaller S.S., higher on-state current, and lower off-state leakage current compared with conventional TFTs. It is believed that electrical characteristics of NSILC-VTFTs can be improved due to larger poly-Si grain size and less number of grain boundaries in the channel.

Figure 4.8 exhibits the transfer characteristics of MILC-VTFTs and NSILC-VTFTs. The W_{mask} / L_{mask} of MILC-VTFTs and NSILC-VTFTs is 0.8μm / 0.8μm. The NSILC-VTFTs have smaller S.S., and lower off-state leakage current compared with MILC-VTFTs. The poor electrical characteristics of MILC-VTFTs are due to the excess Ni accumulation in the n^+ floating region and this phenomenon can be eliminated in NSILC-VTFTs. It is believed that the limited Ni source from Ni-silicided seeding window arranged on source and drain contact holes.

Table 4.2 is summary of measured devices parameters for NSILC-VTFTs, MILC-VTFTs, and conventional TFTs. The NSILC-VTFTs have lower threshold

voltage (V_{TH}), smaller S.S., higher field effect mobility, and larger Ion / Ioff current ratio compared with conventional TFTs and MILC-VTFTs.

4.3.4 NSILC-VTFTs with Constant L_{mask} and Different W_{mask}

Although the grain sizes are enhanced substantially by this novel NSILC process, electrical characteristics of NSILC-VTFTs are still influenced by grain boundaries when channel region and n^+ floating region cover the multiple poly-Si grains [4.12]. In this section, we study the effect of grain boundaries and provide a device design guideline. The transfer characteristics of NSILC-VTFTs with constant L_{mask} = 0.8μm and different W_{mask} are shown in Fig.4.9. The S.S. characteristics and off-state leakage current of NSILC-VTFTs can be improved by decreasing W_{mask}. Table 4.3 is the summary of measured devices parameters from NSILC-VTFTs with constant L_{mask} =0.8μm and different W_{mask}. The field effect mobility can be improved significantly with W_{mask} scaling down. The NSILC-VTFTs with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the smallest S.S., highest field effect mobility, and largest Ion / Ioff current ratio. When the W_{mask} is reduced, the probability of the channel region to cover grain boundaries in the width direction decreases significantly. Therefore, the reduction of W_{mask} is more important for getting a single grain TFT in our work.

The illustration of Ni induced lateral crystallization in wide channel width (W_{mask}) and narrow channel width (W_{mask}) is shown in Fig.4.10. When crystallized W_{mask} is wide, multiple grains can grow side by side leaving one or more grain boundaries in the region. In narrow W_{mask}, there is a higher probability that only one of those grains will grow and occupy the entire channel region. Therefore, it is desirable to use narrow devices [4.15], [4.16].

The same electrical results are also discovered in long L_{mask}. Figure 4.11 shows the transfer characteristics of NSILC-VTFTs with constant L_{mask} =10μm and different

W_{mask}. The S.S. characteristics and off-state leakage current of NSILC-VTFTs with constant L_{mask} =10μm can be improved by decreasing W_{mask}. Figure 4.12 exhibits the transfer characteristics of NSILC-VTFTs with W_{mask} = 5μm and NSILC-VTFTs with multi-channel W_{mask} = 0.8 × 5 μm. The L_{mask} is 10μm. The NSILC-VTFTs with multi-channel W_{mask} = 0.8 × 5 μm have improved S.S. characteristics, off-state leakage current, and on-state current. The electrical characteristics can be improved significantly with W_{mask} scaling down, although L_{mask} is long.

4.3.5 NSILC-VTFTs with Constant W_{mask} and Different L_{mask}

Figure 4.13 displays the transfer characteristics of the NSILC-VTFTs with constant W_{mask} = 0.8μm and different L_{mask}. The S.S. characteristics and on-state current of NSILC-VTFTs with constant W_{mask} = 0.8μm can be improved by decreasing L_{mask}. Summary of measured devices parameters from NSILC-VTFTs with constant W_{mask} = 0.8μm and different L_{mask} is shown in Table 4.4. The S.S. characteristics and field effect mobility can be improved significantly with L_{mask} scaling down. The NSILC-VTFTs with W_{mask} / L_{mask} = 0.8μm / 0.8μm have smallest S.S., highest field effect mobility, and largest Ion / Ioff current ratio. The length of n^+ floating region is defined by L_{mask}. The n^+ floating region is one part of effective channel region between S/D. When the L_{mask} is increasing, the series resistance of n^+ floating region is increasing. It is believed that the probability of n^+ floating region to cover grain boundaries in the length direction decreases with reducing L_{mask}. The poor electrical characteristics of NSILC-VTFTs with long L_{mask} is due to the large series resistance and more grain boundaries in the n^+ floating region.

With device scaling, it is possible to fabricate the entire vertical channel region of NSILC-VTFTs in a single grain. In summary, the NSILC-VTFTs with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the best performance.

4.3.6 Comparison of NSILC-VTFTs and NSILC-VTFTs (RTA)

Figure 4.14 displays the transfer characteristics of the NSILC-VTFTs and NSILC-VTFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 0.8μm. The NSILC-VTFTs (RTA) have steeper S.S., and larger on-state current compared with NSILC-VTFTs. The second step RTA is performed on the NSILC-VTFTs to further improve the device characteristics. Secondary grain crystallization by the second step RTA is the process responsible for the grain size enhancement and crystal integrity improvement [4.11]-[4.13].

In this chapter, the reduction of W_{mask} is more important for getting a single grain TFT. The transfer characteristics of the NSILC-VTFTs (RTA) with constant W_{mask} = 0.8μm and different L_{mask} are shown in Fig.4.15. The NSILC-VTFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the smallest S.S. and the largest on-state current. When the L_{mask} is decreasing, the series resistance of n^+ floating region is decreasing. The high on-state current of NSILC-VTFTs (RTA) with short L_{mask} is due to the low series resistance in the n^+ floating region.

Table 4.5 is summary of measured devices parameters from NSILC-VTFTs (RTA) with constant W_{mask} = 0.8μm and different L_{mask}. The S.S. characteristics and field effect mobility can be improved significantly with L_{mask} scaling down. The NSILC-VTFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the smallest S.S., the highest field effect mobility. The second step RTA can be utilized to enhance the grain size significantly in both the length and the width direction. Furthermore, the NSILC-VTFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 5μm have the lowest Ioff current and largest Ion / Ioff current ratio. The grain size of the n^+ floating region can be enhanced by the second step RTA and the grain boundary induced leakage current can be suppressed by the secondary grain crystallization [4.12]. The NSILC-VTFTs (RTA)

are equivalent to dual-gate device structures. It can suppress the electrical field in the drain depletion region, significantly reducing the leakage current of the, increasing the Ion / Ioff current ratio [4.9], [4.14]. In the NSILC-VTFTs (RTA), the off-state leakage can be improved by increasing appropriate L_{mask}. The poor electrical characteristics of NSILC-VTFTs with a long L_{mask} =10μm is due to the large series resistance in the n^+ floating region.

4.4 Summary

The novel symmetric vertical channel poly-Si TFTs fabricated by NSILC technology have been proposed to fabricate the high performance TFTs. The NSILC-VTFTs have the symmetric S/D structure without additional MILC window mask. NSILC process can reduce metal contaminations and improve poly-Si TFTs characteristics. One step NSILC (500 ^{o}C, 12-hr) is controlled to study the effects of grain boundaries on the vertical channel and n^+ floating region. The NSILC-VTFTs with small W_{mask} and L_{mask} have improved device characteristics due to less poly-Si grain boundaries. Two step NSILC (1_{th} step: 500°C, 12-hr and 2_{th} step: RTA 700°C, 60-sec.) has been introduced to enhance the grain size and improve the crystal integrity through secondary recrystallization. Significant improvements in TFT performance have been observed even for large devices with multiple grains in the channel. The novel NSILC-VTFTs without NH_3 plasma treatment have good S.S. characteristics, low off-state leakage current and high field-effective mobility.

MILC-VTFTs

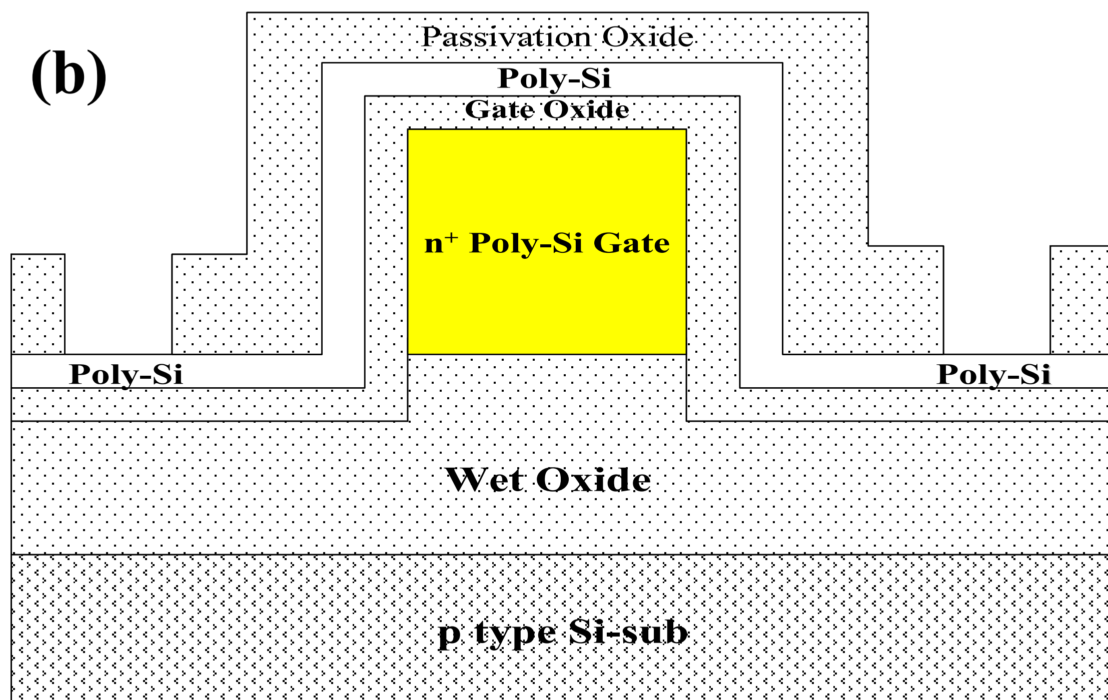
(a)

NSILC-VTFTs

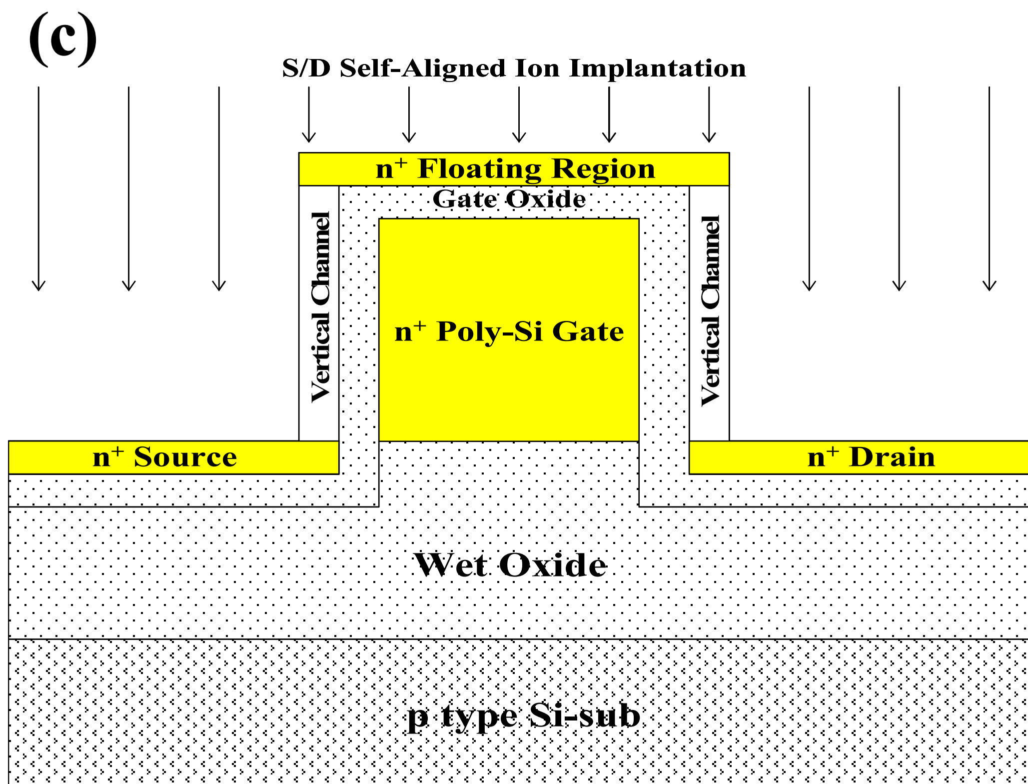
TiN
Ni
Passivation Oxide
a-Si
Gate Oxide
TiN / Ni
n^+ Poly-Si Gate
TiN
Ni
a-Si
TiN
Ni
a-Si
Wet Oxide
p type Si-sub

Passivation Oxide
a-Si
Gate Oxide
NiSi
n^+ Poly-Si Gate
NiSi
a-Si
a-Si
Wet Oxide
p type Si-sub

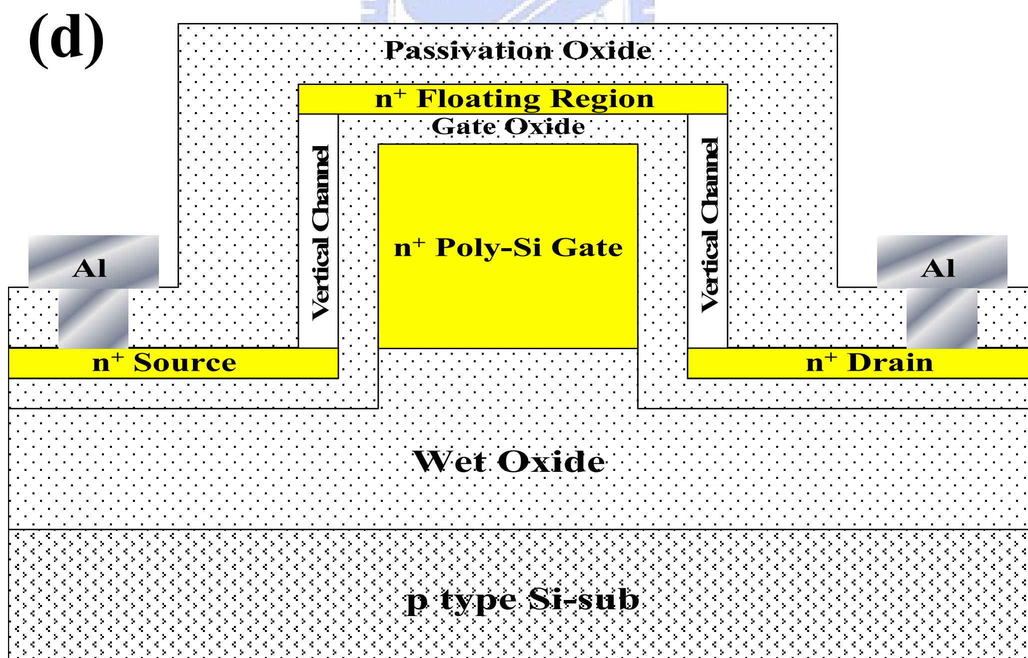
(a) The MILC-VTFTs were fabricated without RTA Ni-silicidation processes. In the NSILC-VTFTs, The Ni-silicidation of NSILC was achieved by RTA at 450 °C for 30 sec before lateral crystallization. Unreacted Ni was removed in H_2SO_4 : H_2O_2 solution after RTA Ni-silicidation processes.



(b) Crystallized poly-Si after NSILC and MILC at 500 °C for 12hr.



(c) S/D self-aligned ion implantation after removing passivation oxide.



(d) Dopants were activated by RTA at 550°C for 30-sec. After passivation, contact, and metallization processes, all the devices were fabricated without NH_3 plasma treatment for studying influences of grain boundaries in the vertical channel and n^+ floating region.

Fig. 4.1 The key process flows of NSILC-VTFTs and MILC-VTFTs.

Table 4.1 The split table of the devices. The NSILC-VTFTs and MILC-VTFTs were only crystallized by first step lateral crystallization (500°C for 12hr). The NSILC-VTFTs (RTA) were crystallized by first step lateral crystallization (500°C for 12hr) and second step RTA (700°C for 60sec). In order to investigate the impact of grain boundaries in the channel crystallized by NSILC or MILC processes, no further NH_3 plasma treatment procedure was implemented in our experiment.

Devices \ Conditions	Gate Oxide Thickness	Channel Thickness	Poly-Si Gate Thickness	Undercut Distance	First Step Lateral Crystallization	Second Step RTA	NH_3 Plasma
NSILC-VTFTs	500Å	500Å	2500Å	1000Å	500°C, 12hr		
NSILC-VTFTs (RTA)	500Å	500Å	2500Å	1000Å	500°C, 12hr	700°C, 60 sec	
MILC-VTFTs	500Å	500Å	2500Å	1000Å	500°C, 12hr		
Conventional TFTs	500Å	500Å	2500Å				

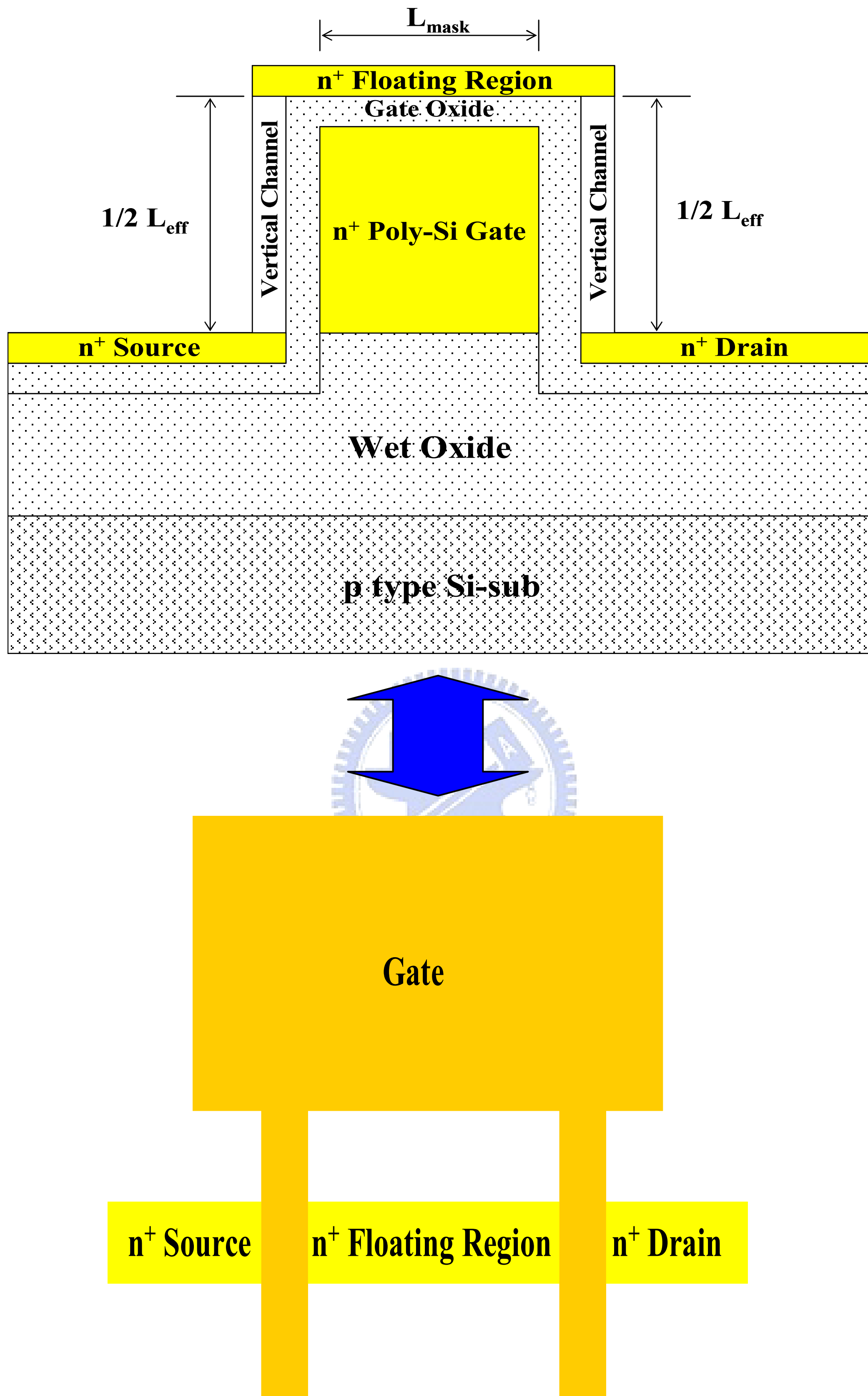


Fig.4.2 The schematic device cross-section structure of NSILC-VTFTs. The NSILC-VTFTs are equivalent to dual-gate device structures. The effective channel length of NSILC-VTFTs is defined by thickness of poly-Si gate and gate oxide.

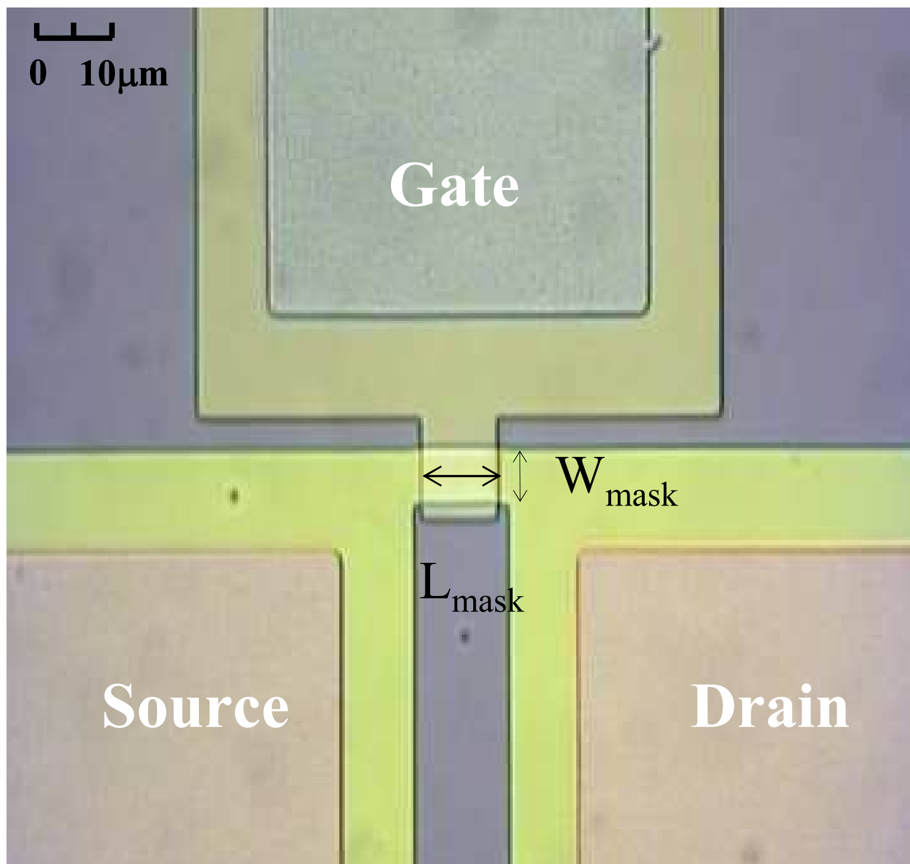


Fig. 4.3 The plan view optical microscope microphotograph of NSILC-VTFTs. The length of n^+ floating region is defined by the mask channel length (L_{mask}). The mask channel width (W_{mask}) is equal to effective channel width of NSILC-VTFTs.

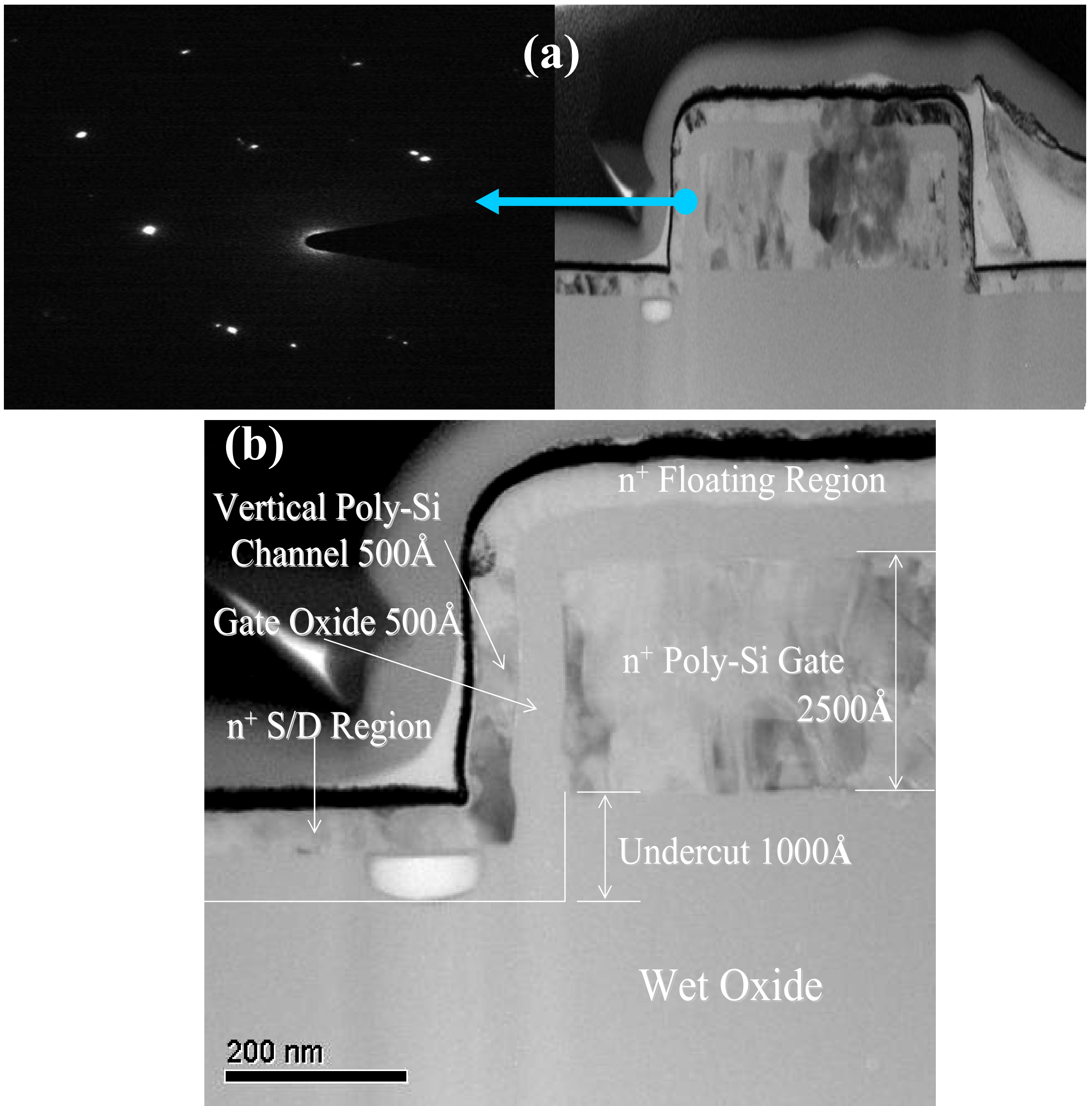
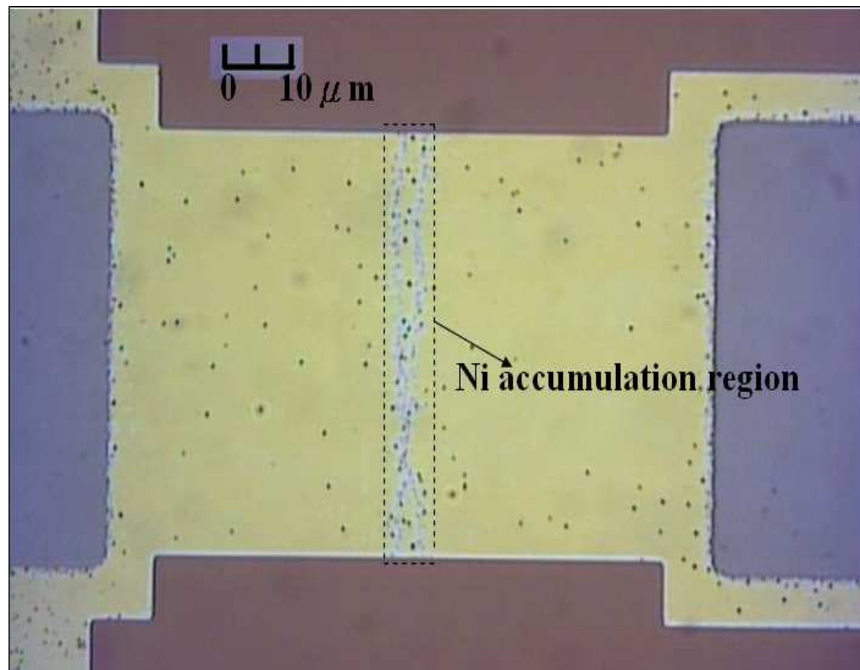
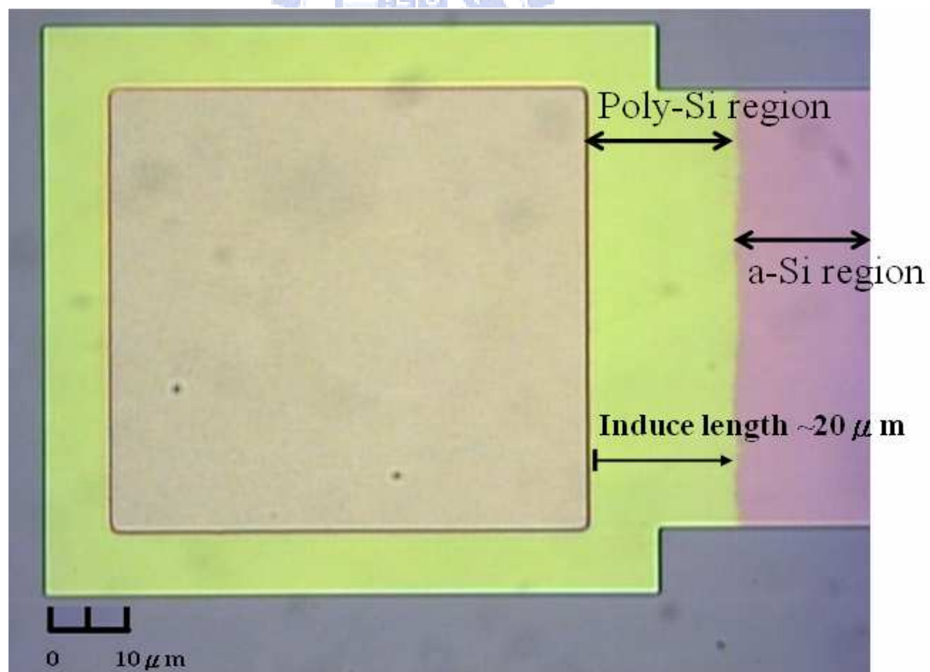


Fig.4.4 (a) The transmission electron diffraction (TED) pattern of vertical poly-Si channel in NSILC-VTFTs and (b) cross-section transmission electron microscope (TEM) microphotograph of NSILC- VTFTs. The gate oxide thickness and channel thickness are both 500Å. The undercut depth of poly-Si gate is 1000Å.

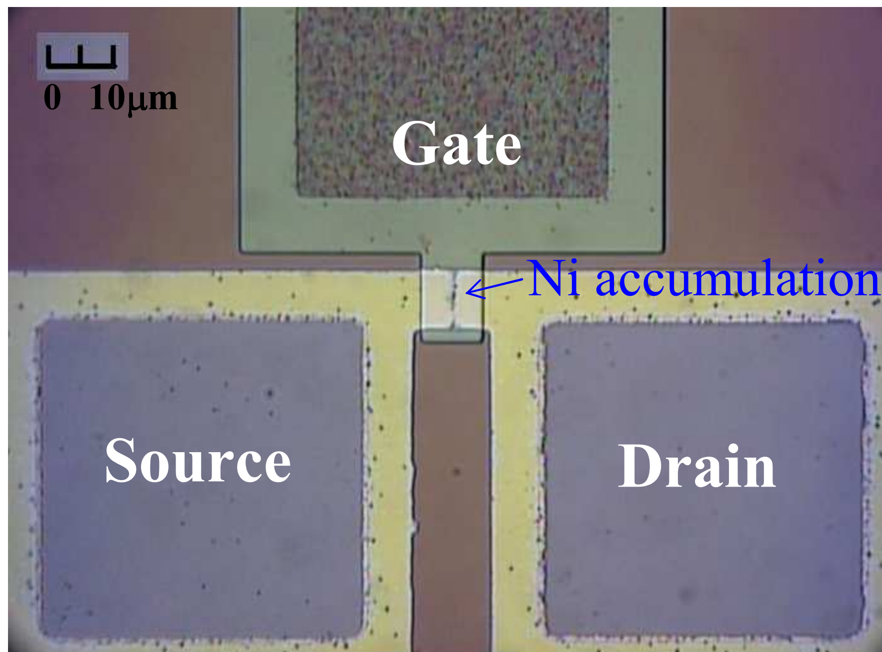


(a) MILC, 500°C, 24hr

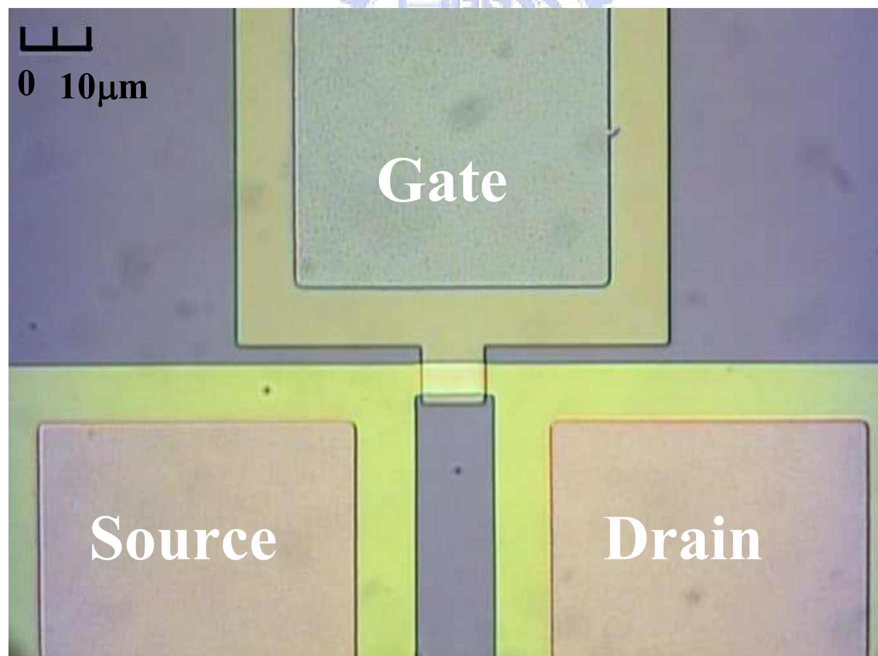


(b) NSILC, 500°C, 12hr

Fig. 4.5 (a) The plan view optical microscope microphotograph of test key after MILC process at 500°C for 24hr and (b) the plan view optical microscope microphotograph of test key after NSILC process at 500°C for 12hr. The Ni accumulation of grain boundaries is found in the MILC process but it is not found in the NSILC process.



(a) MILC-VTFTs



(b) NSILC-VTFTs

Fig.4.6 (a) The plan view optical microscope microphotograph of MILC-VTFTs after annealing at 500°C for 12hr and (b) the plan view optical microscope microphotograph of NSILC-VTFTs after annealing at 500°C for 12hr. The Ni accumulation of the n^+ floating region is found in the MILC-VTFTs but it is not found in the NSILC-VTFTs.

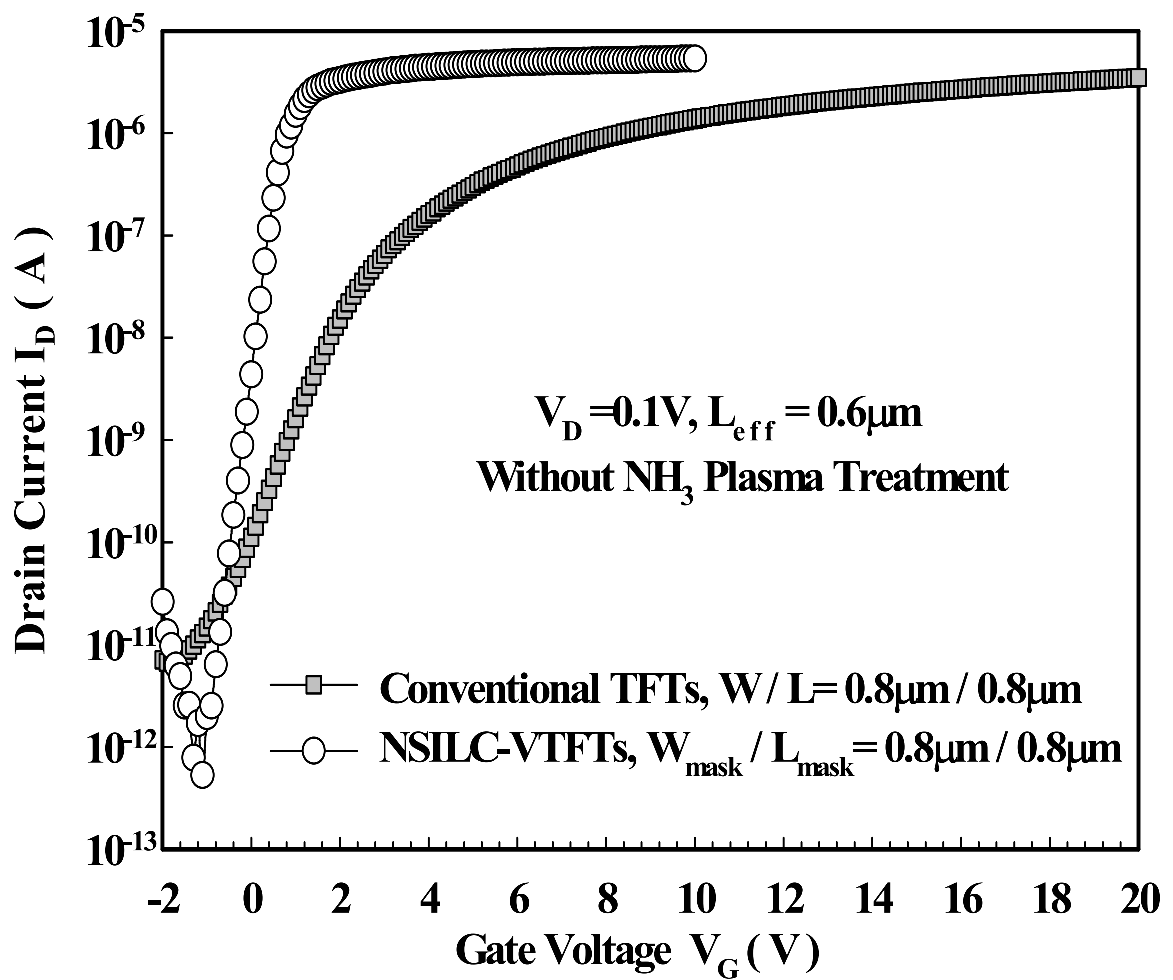


Fig.4.7 The transfer characteristics of conventional TFTs and NSILC-VTFTs. The effective channel length of NSILC-VTFTs is 0.6µm.

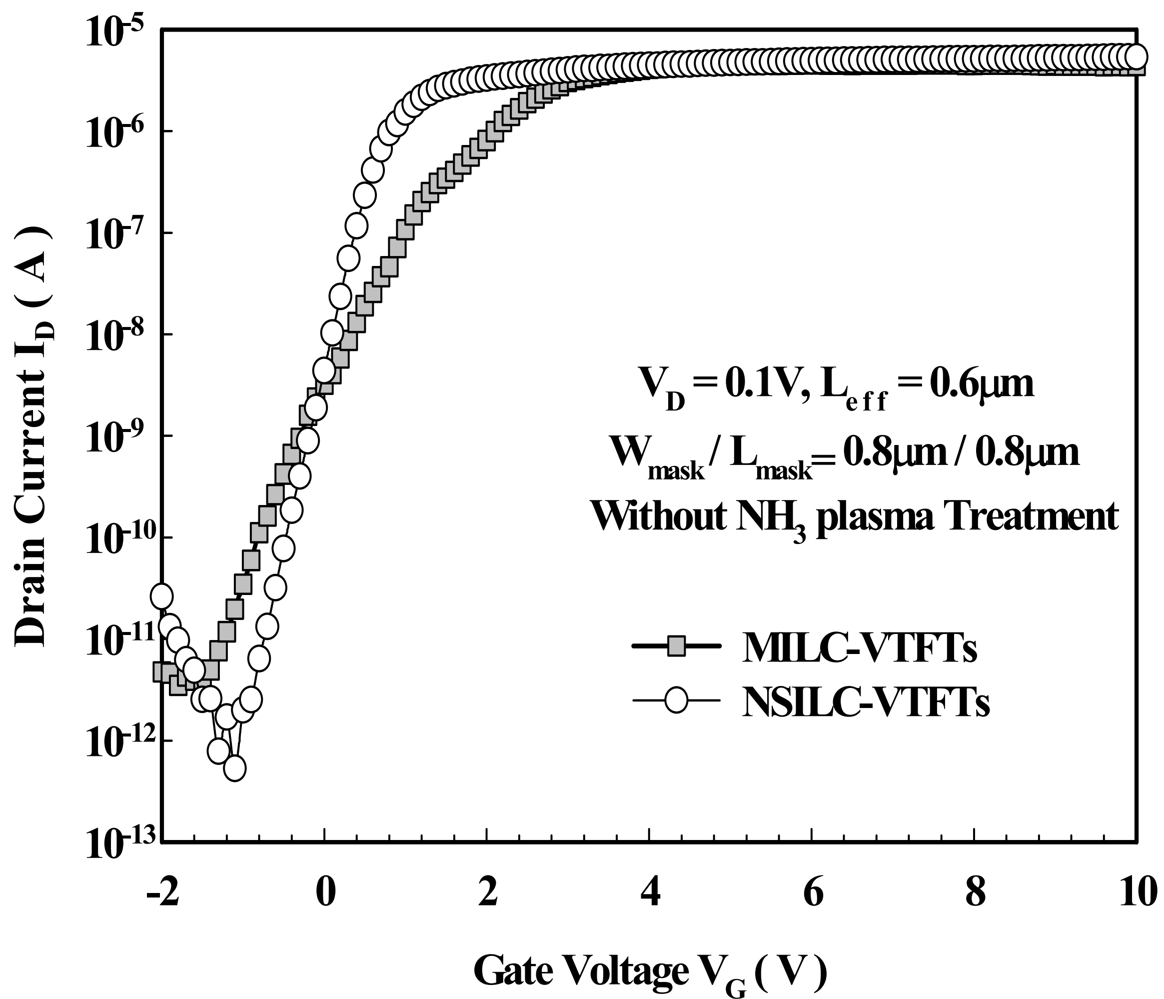


Fig.4.8 The transfer characteristics of MILC-VTFTs and NSILC-VTFTs. The effective channel length of MILC-VTFTs and NSILC-VTFTs is 0.6μm

Table 4.2 The summary of measured devices parameters for NSILC-VTFTs, MILC-VTFTs, and conventional TFTs.

W_{mask} / L_{mask} (μm / μm)	Threshold Voltage V_{TH} (V)	Subthreshold Swing S.S. (mV/dec)	Field Effect Mobility μ (cm^2/V-s)	Ion / Ioff Ioff @ V_{DS}=0.1V Ion @ V_{GS}=10V
0.8 / 0.8 NSILC-VTFTs L_{eff}= 0.6 μm	0.095	222	355	1.01×10^7
0.8 / 0.8 MILC-VTFTs L_{eff}= 0.6 μm	0.328	560	271	1.15×10^6
0.8 / 0.8 Conventional TFTs	1.776	996	40.9	2.02×10^5

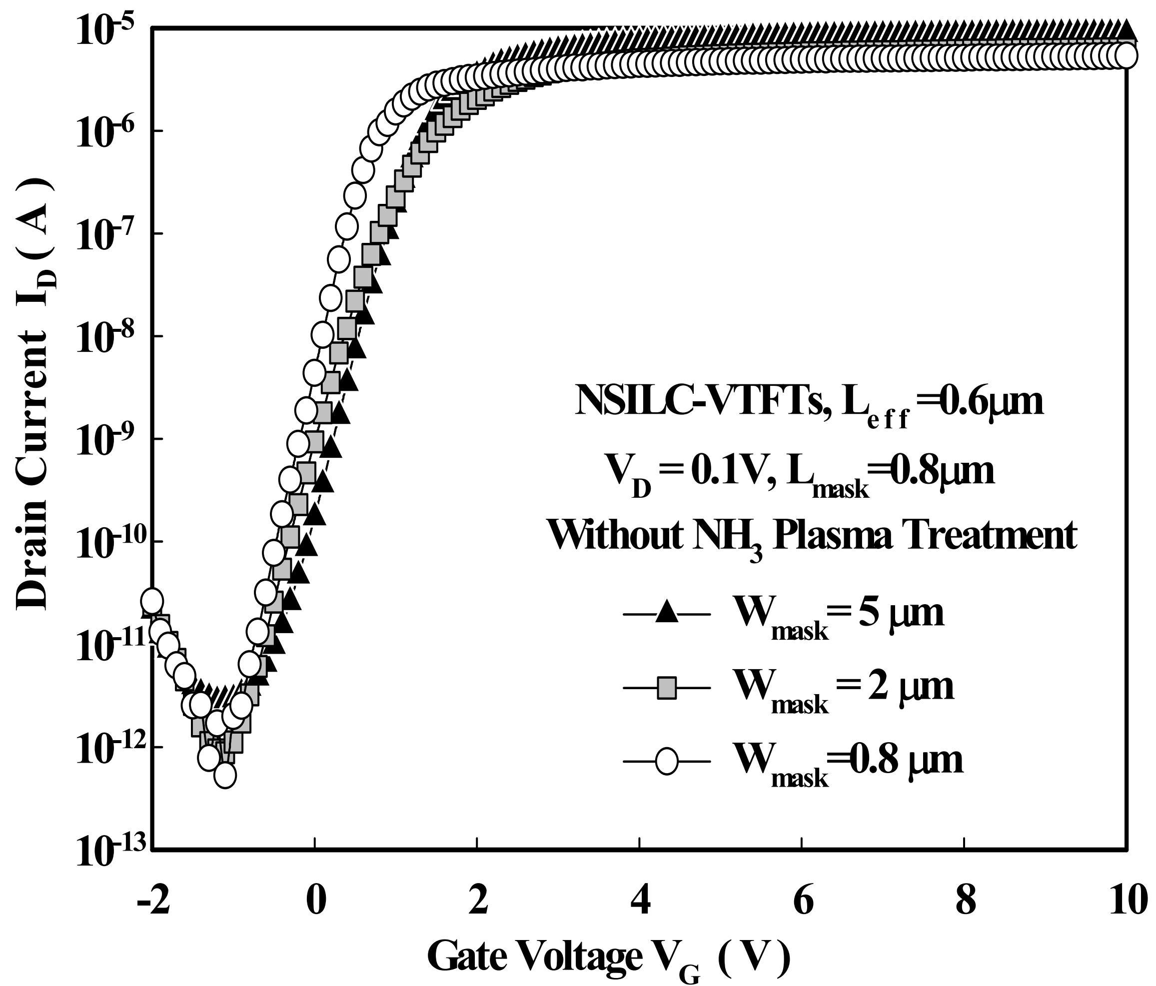


Fig.4.9 The transfer characteristics of NSILC-VTFTs with constant L_{mask} = 0.8μm and different W_{mask}. The effective channel length of NSILC-VTFTs is 0.6μm.

Table 4.3 The summary of measured devices parameters from NSILC-TFTs with constant L_{mask} = 0.8μm and different W_{mask}. The effective channel length of NSILC-VTFTs is 0.6μm.The NSILC-TFTs with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the highest field effect mobility.

NSILC-VTFTs W_{mask} / L_{mask} (μm / μm) L_{eff}=0.6μm	Threshold VoltageV_{TH} (V)	Subthreshold Swing S.S. (mV/dec)	Field Effect Mobility μ (cm^2/V-s)	Ion/Ioff Ioff @V_{DS}=0.1V Ion @V_{GS}=10V
0.8/0.8	0.095	222	355	1.01×10^7
2/0.8	0.362	236	135	7.15×10^6
5/0.8	0.532	239	74.4	3.08×10^6

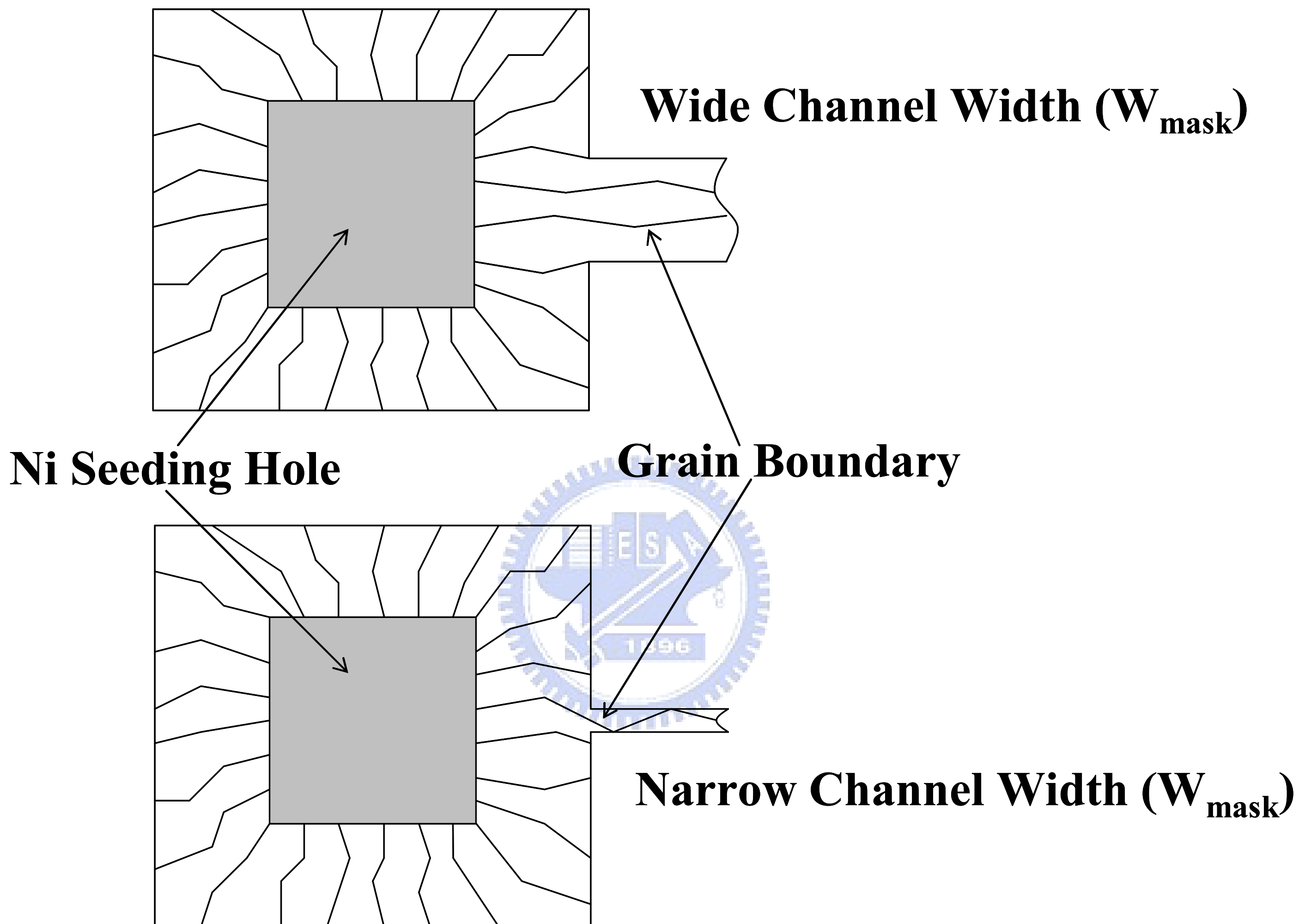


Fig.4.10 The illustration of Ni induced lateral crystallization in wide channel width (W_{mask}) and narrow channel width (W_{mask}).

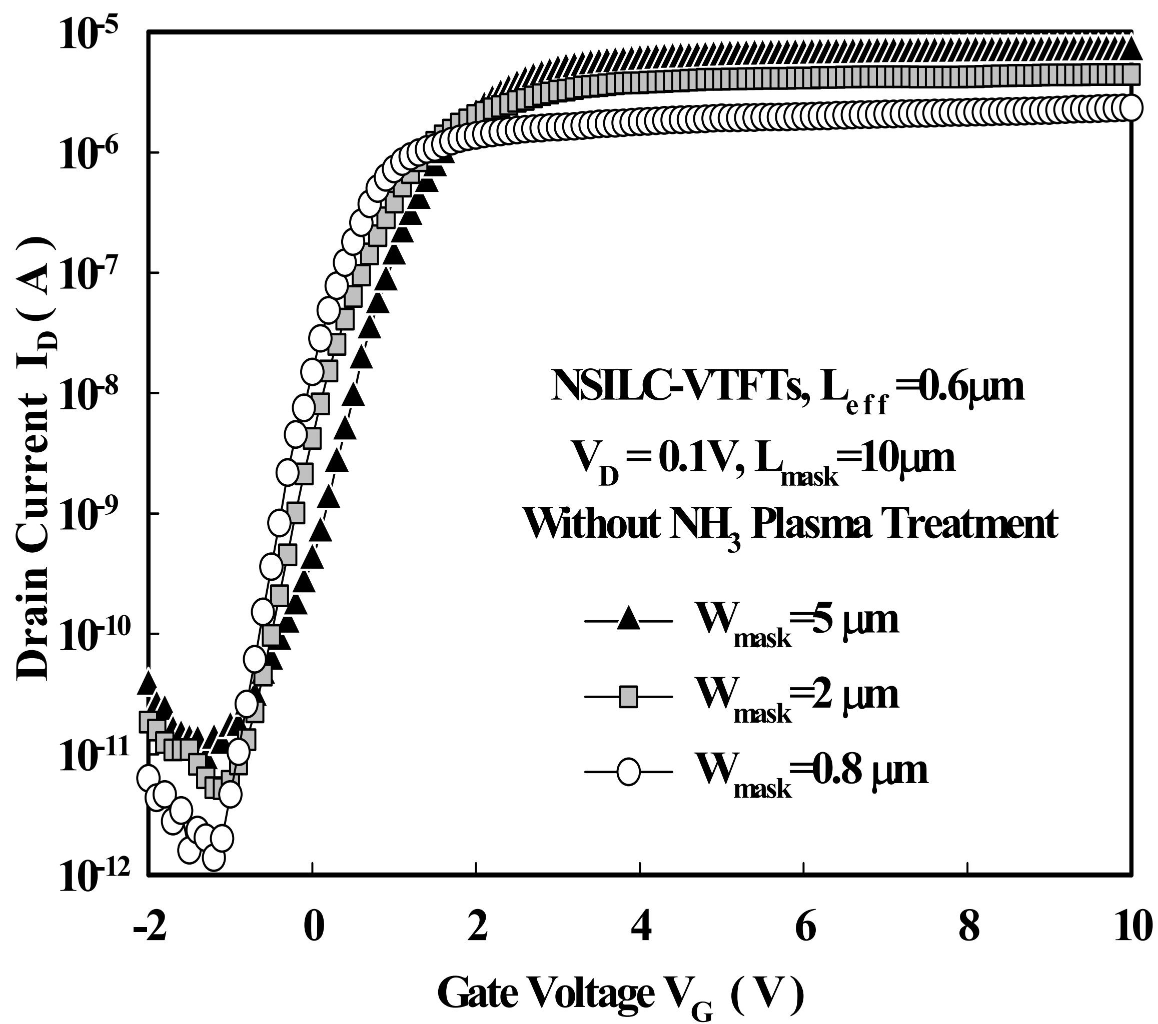


Fig.4.11 The transfer characteristics of NSILC-VTFTs with constant L_{mask} =10μm and different W_{mask}. The effective channel length of NSILC-VTFTs is 0.6μm.

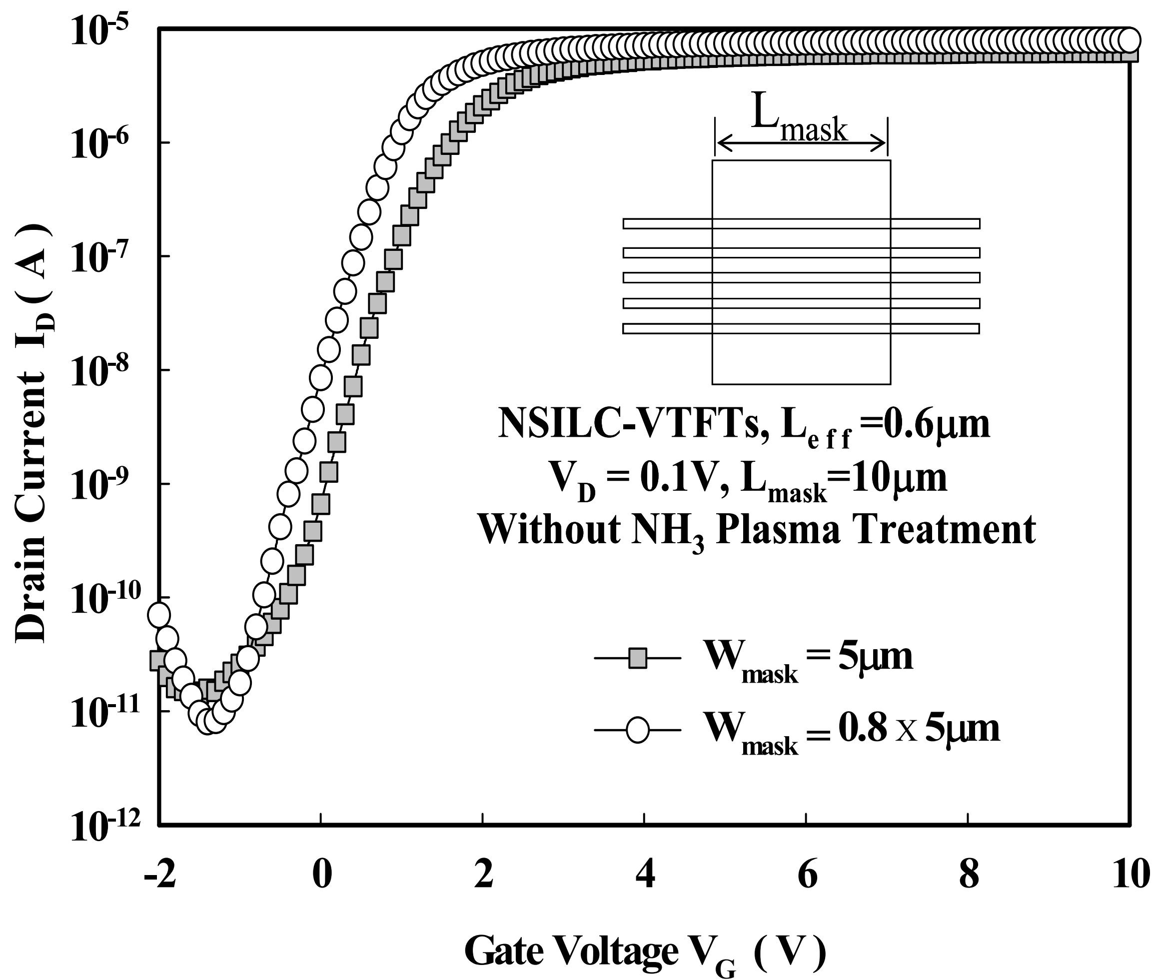


Fig.4.12 The transfer characteristics of NSILC-VTFTs with W_{mask} = 5μm and NSILC-VTFTs with multi-channel W_{mask} = 0.8 × 5 μm. L_{mask} is constant = 10μm. The effective channel length of NSILC-VTFTs is 0.6μm.

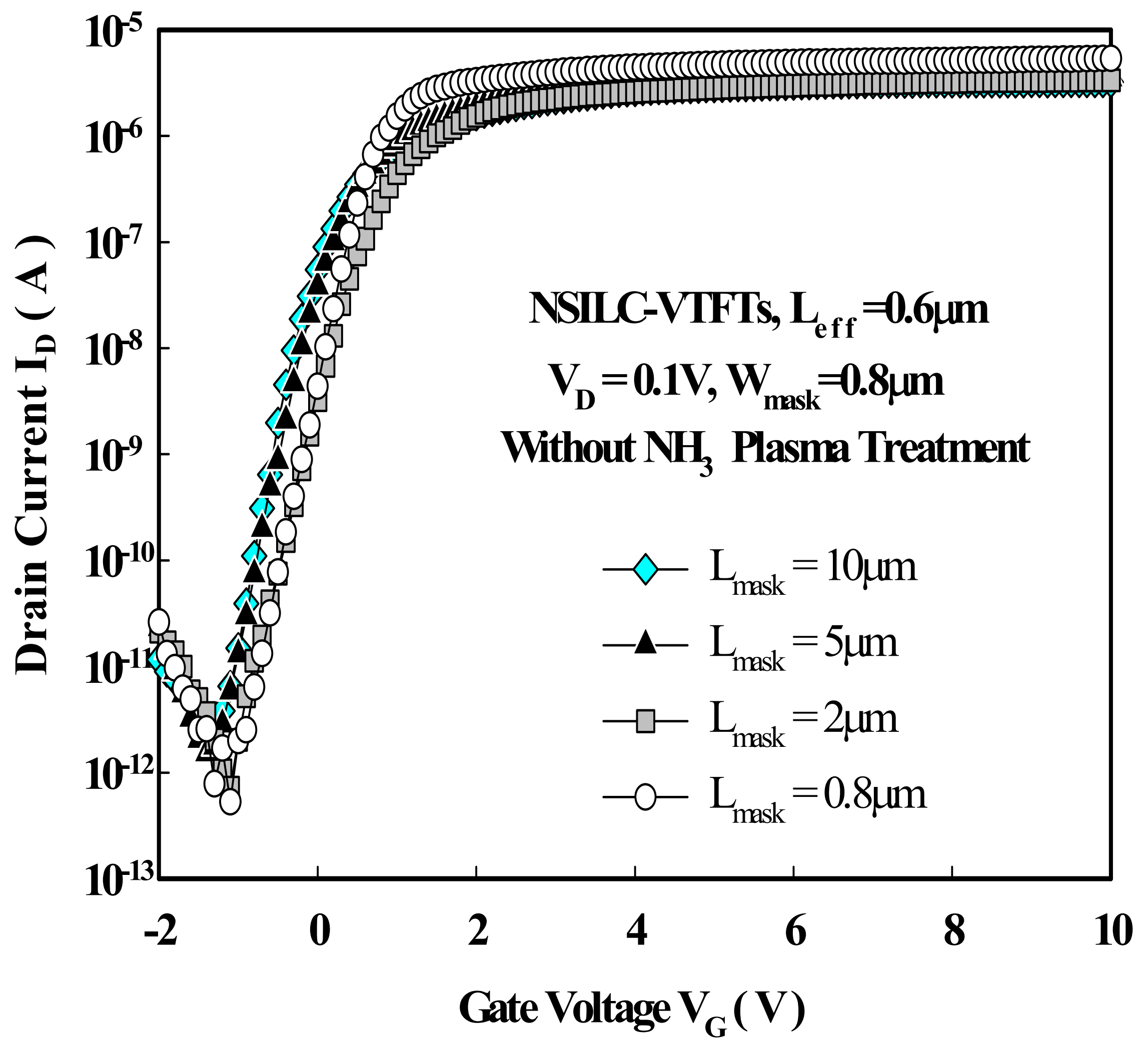


Fig.4.13 The transfer characteristics of the NSILC-VTFTs with constant W_{mask} = 0.8μm and different L_{mask}. The effective channel length of NSILC-VTFTs is 0.6μm.

Table 4.4 The summary of measured devices parameters from NSILC-TFTs with constant W_{mask} = 0.8μm and different L_{mask}. The effective channel length of NSILC-VTFTs is 0.6μm.The NSILC-TFTs with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the highest field effect mobility.

NSILC-VTFTs W_{mask} / L_{mask} (μm / μm) L_{eff}=0.6μm	Threshold VoltageV_{TH} (V)	Subthreshold Swing S.S. (mV/dec)	Field Effect Mobility μ (cm^2/V-s)	Ion/Ioff Ioff @ V_{DS}=0.1V Ion @ V_{GS}=10V
0.8/0.8	0.095	222	355	$1.01x10^7$
0.8/2	0.151	236	133	$4.65x10^6$
0.8/5	-0.207	241	133	$2.2x10^6$
0.8/10	-0.295	280	131	$1.05x10^6$

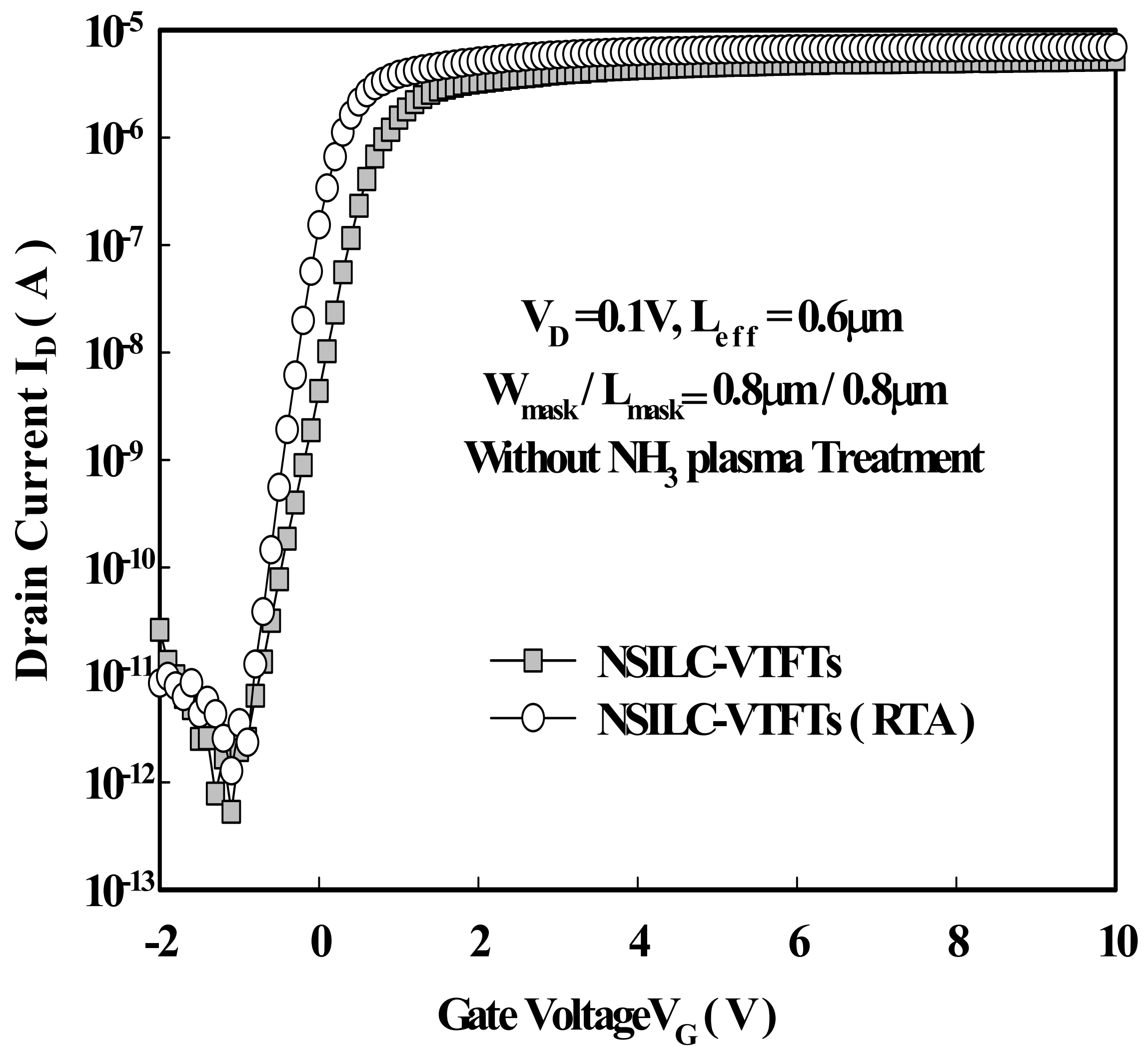


Fig.4.14 The transfer characteristics of the NSILC-VTFTs and NSILC-VTFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 0.8μm. The effective channel length is 0.6μm.

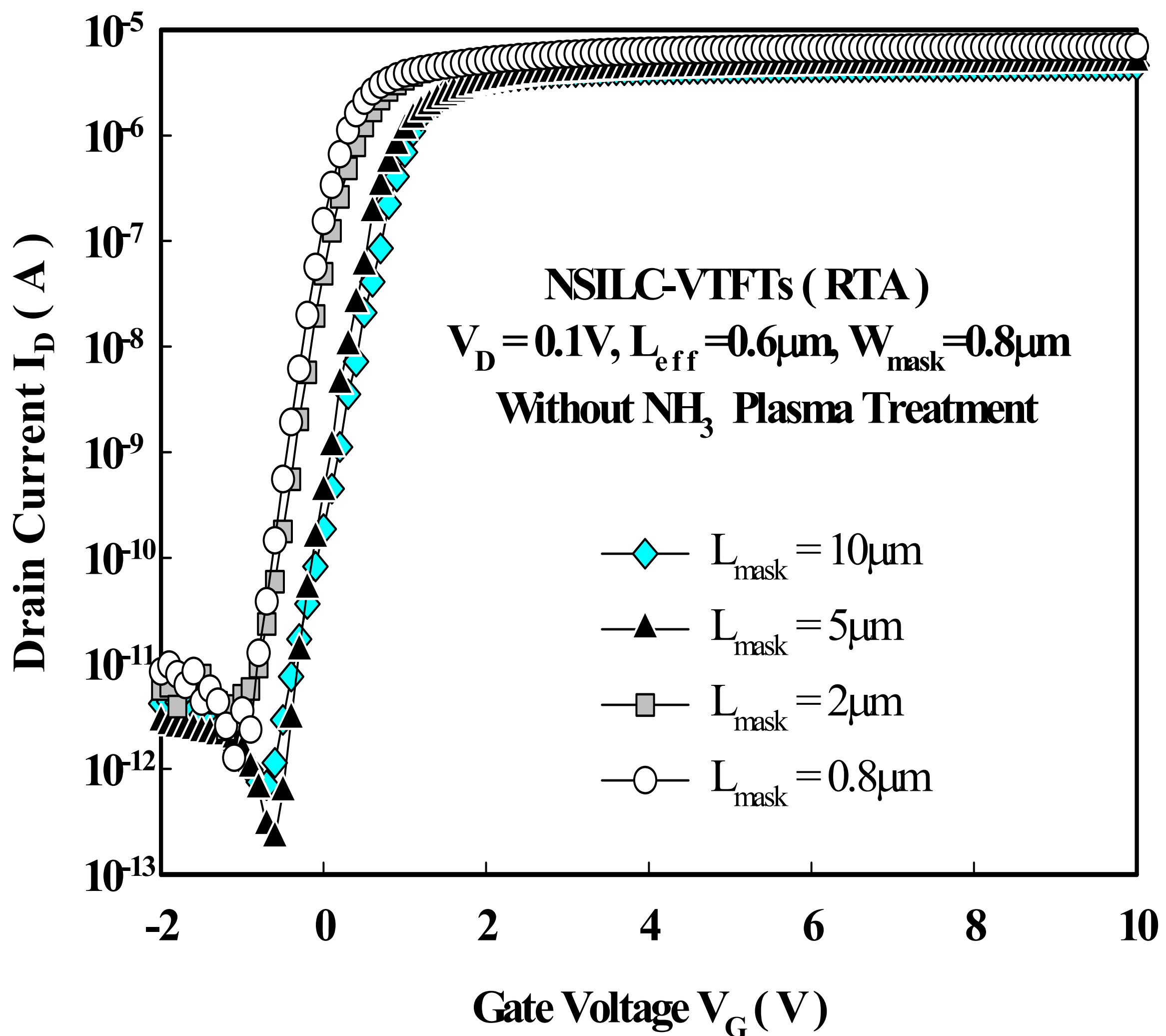


Fig.4.15 The transfer characteristics of the NSILC-VTFTs (RTA) with constant W_{mask} = 0.8μm and different L_{mask}. The NSILC-VTFTs (RTA) were crystallized by first step lateral crystallization (500°C for 12hr) and second step RTA (700°C for 60sec). The effective channel length of NSILC-VTFTs (RTA) is 0.6μm.

Table 4.5 The summary of measured devices parameters from NSILC-TFTs (RTA) with constant W_{mask} = 0.8μm and different L_{mask}. The effective channel length of NSILC-VTFTs (RTA) is 0.6μm. The NSILC-TFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 0.8μm have the highest field effect mobility. The NSILC-TFTs (RTA) with W_{mask} / L_{mask} = 0.8μm / 5μm have the largest Ion / Ioff current ratio.

NSILC-VTFTs (RTA) W_{mask} / L_{mask} (μm / μm) L_{eff}=0.6μm	Threshold VoltageV_{TH} (V)	Subthreshold Swing S.S. (mV/dec)	Field Effect Mobility μ (cm^2/V-s)	Ion/Ioff Ioff @ V_{DS}=0.1V Ion @ V_{GS}=10V
0.8/0.8	-0.272	180	553	$9x10^6$
0.8/2	-0.169	190	541	$8.2x10^6$
0.8/5	0.29	205	365	$2.2x10^7$
0.8/10	0.42	240	352	$8.6x10^6$

Chapter 5

Characteristics of Self-Aligned Si / Ge T-Gate Poly-Si Thin-Film Transistors with High ON/OFF Current Ratio

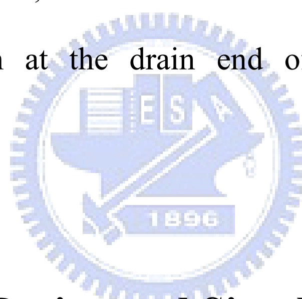
5.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many potential applications including high density flash memories, active matrix organic light emitting diode (AM-OLED), and active-matrix liquid crystal displays (AMLCDs) [5.1]-[5.4]. Poly-Si TFTs are considered to be promising devices for display system-on-panel applications [5.5].

However, the large OFF-state leakage current and device instability of poly-Si TFTs are hindrances to the high-performance and high reliability circuit applications. It is well known that the dominant mechanism of the OFF-state leakage current is the field emission via grain boundary traps due to a high electric field in the drain depletion region. The leakage current is increased with increasing gate and drain voltages which enhance the field emission via grain boundary traps in the depletion region near the drain [5.6], [5.7]. In order to increase the reliability and reduce the leakage current, poly-Si TFTs with offset gated, lightly doped drain (LDD), gate-overlapped LDD, floating gate spacer, air cavities, or field-induced drain (FID) structures have been suggested to reduce the electric field near the drain [5.8]-[5.14].

In this chapter, the novel self-aligned Si / Ge T-gate poly-Si TFTs were proposed

and demonstrated. The Si / Ge T-gate was formed by selective wet etching of Ge gate layer. The Ge regions etched at the gate edges were refilled by low-pressure chemical vapor deposition tetraethoxysilane (LPCVD TEOS) oxide in the passivation process. The thick gate oxide layer at the gate edges and the passivation oxide layer were deposited simultaneously in passivation process. The thick gate oxide at the gate edges effectively reduces the drain vertical and lateral electric fields without additional mask, LDD, spacer, and sub-gate bias. The lateral electric field within the channel can be lowered by using the lateral selective etching of Ge within the gate stack at the gate edges without extra fabrication cost in the Si / Ge T-gate TFTs. The Si / Ge T-gate TFTs have a reduced OFF-state leakage current at negative voltages, an improved ON / OFF current ratio, and a smaller drain conductance in saturation due to a reduced impact ionization at the drain end of the channel compared with conventional TFTs.



5.2 Device Structure Design and Simulation

5.2.1 Si / Ge T-gate Structure Design

Figure 5.1 shows the schematic cross-sectional device structures of (a) Si / Ge T-gate TFTs and (b) conventional TFTs. Both devices have the same photo-mask gate length and perform the same S / D implantation condition. The experimental split table of Si / Ge T-gate TFTs and conventional TFTs is defined in Table I. In Si / Ge T-gate TFTs, the thickness of thick gate oxide layer at the gate edges are controlled by the thickness of Ge gate layer (50-nm and 100-nm) and the Ge lateral undercut distances (400-nm and 800-nm) are controlled by the time of selective wet etching. For example, the Si / Ge_{50nm} T-gate TFTs (400nm) have a 150-nm / 50-nm stacked Si / Ge gate layer and a 400-nm Ge lateral undercut distance. The total thickness of

stacked Si / Ge gate layer is 200-nm for all devices.

The Si / Ge T-gate TFTs can reduce the vertical electric field near the drain due to the thick gate oxide layer at the gate edges [5.12]. The poly-Si region under thick gate oxide can be considered as an offset region and the gate edge over the thick gate oxide serve as a field plate connected with the gate, so that the proposed TFTs operate like field-induced drain TFTs (FID TFTs) except a sub-gate bias [5.13]. In the OFF-state, the lateral electric field near the drain can be reduced due to the thick gate oxide layer at the gate edges [5.12]. In the ON-state, a sufficient inversion layer can be induced by the thick gate edge oxide near the source [5.14].

5.2.2 Lateral Electric Field Simulation in Si / Ge T-gate TFTs

In order to demonstrate the reduction in drain lateral electric field in the Si / Ge T-gate TFTs. The electric fields in the TFTs were simulated by using a commercial two-dimensional (2-D) numerical simulator for semiconductor devices. Figures 5.2 show the simulated lateral electric field distribution along the channel / gate oxide interface for conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation at $V_G = 0$ V and $V_D = 15$ V. Figures 5.3 show the simulated lateral electric field distribution along the channel / gate oxide interface for conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation at $V_G = -10$ V and $V_D = 10$ V. The simulated result demonstrates that lateral electric field near the drain can be effectively reduced by the Si / Ge T-gate structure. The high κ gate dielectric SiN_X at the gate edges in Si / Ge T-gate TFTs with SiN_X passivation have larger the lateral drain electric field compared with Si / Ge T-gate TFTs with TEOS passivation. The Si / Ge T-gate TFTs with 100-nm Ge gate layer have the lowest lateral electric field near the drain due to the thickest gate oxide at the gate edges [5.12].

5.3 Experiment

Figure 5.4 shows the main fabrication process steps of Si / Ge T-gate TFTs. First, a 100-nm or 50-nm amorphous silicon (a-Si) layer was deposited by LPCVD at 550°C on oxidized silicon wafers and then was crystallized by solid phase crystallization (SPC) at 600°C for 24-hr. After the patterning of active region, a 50-nm TEOS gate oxide layer was deposited by LPCVD. Subsequently, a stacked a-Si / a-Ge gate layer was deposited by LPCVD at 550°C / 370°C. The thickness of thick gate oxide layer at the gate edges were controlled by the thickness of Ge gate layer (50-nm and 100-nm). A phosphorus gate implantation with dose 5×10^{15} cm^{-2} and energy 60keV was used to form the n^+ gate (Fig.5.4a). After defining gate electrode, the Si / Ge T-gate was formed by selective wet etching (H_2O: H_2O_2 solution) of Ge gate layer at 75°C. The Ge lateral undercut distances (400-nm and 800-nm) of Si / Ge T-gate were controlled by the time of wet etching. Then, the remaining oxide on the S / D region was removed by diluted HF. A self-aligned phosphorus implantation with dose 5×10^{15} cm^{-2} and energy 25keV was used to form the n^+ S / D (Fig.5.4b). The Ge undercut regions were refilled by LPCVD TEOS oxide or LPCVD SiN_X in the passivation process and dopants were activated by furnace at 600°C for 12-hr. After contact and metallization processes (Fig.5.4c), NH_3 plasma treatments were implemented after sintering at 400°C for 30-min. Conventional TFTs with self-aligned n^+ S / D and TEOS passivation were also fabricated to serve as control ones.

5.4 Results and Discussion

5.4.1 Cross-Sectional TEM microphotograph of Si / Ge T-gate TFTs

Figure 5.5 shows the cross-sectional transmission electron microscope (TEM)

microphotograph of Si / Ge T-gate TFTs with TEOS passivation. The Si / Ge T-gate was successfully obtained on the gate oxide and the interfacial oxide was not observed in the stacked Si / Ge interface. The Si gate layer and Ge gate layer were inter-alloyed between the stacked Si / Ge interface due to subsequent processes annealing. The undercut regions were fully refilled by LPCVD TEOS oxide in the passivation process and the thickness of thick gate oxide at the gate edges were controlled by the thickness of Ge gate layer. In the Fig.5.5, the thickness of Ge gate layer is about 100-nm and the Ge lateral undercut distance of Si / Ge T-gate is about 400-nm. The poly-Si at the gate edges was bent upward by subsequent processes-induced thermal stresses. The bending poly-Si at the gate edges brings about gradual variation in thickness of gate oxide at the gate edges and the thickest gate oxide is near the drain. The vertical and lateral electric fields at drain can be effectively reduced by a thick gate oxide at the gate edges. In addition, the bending poly-Si at the gate edges can promote the refilling ability of LPCVD TEOS. Figure 5.6 illustrates the composition of pure Ge gate layer extracted from the energy dispersive x-ray spectrometer analysis. The pure Ge gate layer of Si / Ge T-gate can be easily etched by the wet etching H_2O: H_2O_2 (100 : 1) solution at a low temperature of 75°C. The etching rate is about 2.5 nm/s.

5.4.2 Si / Ge T-gate TFTs with TEOS Passivation

Figures 5.7 exhibit the measured transfer characteristics of conventional TFTs and Si / Ge T-gate TFTs with (a) W / L = 10 μm / 10 μm and (b) W / L = 10 μm / 5 μm. The device channel thickness is 100-nm. The OFF-state leakage currents of Si / Ge T-gate TFTs are significantly lower than those of conventional TFTs. This is due to that the lateral electric field near the drain can be effectively reduced by the Si / Ge T-gate structure. Since the thick gate oxide at the gate edges greatly suppress the

lateral drain electric field, the anomalous OFF-state leakage currents of poly-Si TFTs can be controlled by the thickness of Ge gate layer and the Ge lateral undercut distances [5.14]. The Si / Ge_{100nm} T-gate (800 nm) TFTs have the lowest OFF-state leakage currents in the Si / Ge T-gate TFTs. The ON-state currents of Si / Ge T-gate TFTs are slightly lower than those of conventional TFTs. A sufficient inversion layer can be induced by the thick gate edge oxide near the source. For the Si / Ge T-gate TFTs, the ON-state currents are slightly reduced with increasing thickness of Ge gate layer and Ge lateral undercut distances. The Si / Ge_{50nm} T-gate (400 nm) TFTs have the highest ON-state currents among the all Si / Ge T-gate TFTs.

Figure 5.8 displays the measured OFF-state leakage currents of conventional TFTs and Si / Ge T-gate TFTs with W / L = 10 μm / 10 μm for different drain biases at V_G = -10 V. The device channel thickness is 100-nm. The OFF-state leakage currents of Si / Ge T-gate TFTs are significantly lower than those of conventional TFTs. The OFF-state leakage current is increased with increasing gate and drain voltages which enhance the field emission via grain boundary traps in the depletion region near the drain [5.6], [5.7]. In the Si / Ge T-gate TFTs, the lateral electric field near the drain can be greatly reduced due to the thick gate oxide layer at the gate edges and the OFF-state leakage currents are greatly decreased with increasing thickness of Ge gate layer and the Ge lateral undercut distances.

Figure 5.9 illustrates the measured ON / OFF current ratio of conventional TFTs and Si / Ge T-gate TFTs with W = 10 μm and different channel length. The device channel thickness is 100-nm. The ON / OFF current ratio is defined as the ratio of the ON-state current to the minimum OFF-state leakage current. The ON-state current is defined as drain current (I_D) at V_G = 20 V, V_{DS} = 10 V and the minimum OFF-state leakage current is defined as minimum drain current (I_{min}) at V_{DS} = 10 V. The Si / Ge T-gate TFTs not only reduce the OFF-state leakage current, but also maintain a high

ON-state current. The Si / Ge T-gate TFTs with 100-nm Ge gate layer have the highest ON / OFF current ratio than those with 50-nm Ge gate layer due to the lowest OFF-state leakage currents. On the other hand, the Si / Ge T-gate TFTs with 100-nm Ge gate layer can maintain a high ON-state current even though gate length is scaled down to 3 μm. Hence, to optimize the Si / Ge T-gate TFTs, the thickness of Ge gate layer should be considered first.

The Si / Ge T-gate TFTs are different from conventional FID TFTs. The conventional FID TFTs need an additional sub-gate electrode, a large sub-gate bias, and an additional sub-gate mask compared with Si / Ge T-gate TFTs. In addition, the conventional FID TFTs have the farther separation of n^+ S / D junction compared with conventional TFTs. In the conventional FID TFTs with a SiO_2 interlayer, a typical sub-gate bias of more than 60V is necessary to obtain a high ON / OFF current ratio [5.13]. The Si / Ge T-gate TFTs and conventional TFTs were fabricated with the same photo-mask gate length and the same S / D implantation condition. The Si / Ge T-gate TFTs and conventional TFTs have the identical position of S / D junction. The Si / Ge T-gate TFTs only need one gate electrode to obtain a high ON / OFF current ratio.

Figure 5.10 displays the output characteristics of conventional TFTs and Si / Ge T-gate TFTs with W / L = 10 μm / 10 μm. The device channel thickness is 100-nm. The Si / Ge T-gate TFTs have more saturated output characteristics compared with conventional TFTs. The kink current of Si / Ge T-gate TFTs is reduced considerably compared with that of conventional TFTs. The Si / Ge T-gate TFTs with 100-nm Ge gate layer have the most saturated output characteristics due to the lowest lateral electric field near the drain. The output characteristics exhibit an anomalous increase of current in the saturation regime, often called “kink” effect due to an analogy with silicon-on-insulator (SOI) devices [5.15]-[5.17]. This phenomenon can be attributed to the floating-body effect [5.18] and the avalanche multiplication enhanced by grain

boundary-traps [5.16], particularly in n-channel TFTs. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return [5.18], [5.19]. Since the Si / Ge T-gate TFTs can reduce the vertical and lateral electric fields near the drain due to the thick gate oxide layer at the gate edges and the poly-Si region under thick gate oxide can be considered as an offset region [5.12], the impact ionization can be effectively reduced and the avalanche multiplication enhanced by grain boundary-traps can be suppressed by the Si / Ge T-gate TFTs [5.9]-[5.11].

5.4.3 Si / Ge T-gate TFTs with TEOS Passivation or SIN_X Passivation

Figures 5.11 exhibit the measured transfer characteristics of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation. The device channel thickness is 50-nm. The ON-state current degrades with increasing thickness of Ge gate layer in Si / Ge T-gate TFTs with TEOS passivation but the ON-state current can be maintained with increasing thickness of Ge gate layer in Si / Ge T-gate TFTs with SiNx passivation. This is due to that the gate dielectric near the drain can be effectively refilled by the high κ gate dielectric SiN_X at the gate edges in Si / Ge T-gate TFTs with SiN_X passivation. The high κ gate dielectric SiN_X at the gate edges can increase the gate capacitance and maintain the ON-state current. The OFF-state leakage currents of Si / Ge T-gate TFTs with TEOS passivation are significantly lower than those of Si / Ge T-gate TFTs with SiN_X passivation. The larger OFF-state leakage currents of Si / Ge T-gate TFTs with SiN_X passivation is due to larger lateral drain electric field [5.8], [5.13]. In addition, the subthreshold swing (S.S.) can be improved with increasing undercut distance in Si / Ge T-gate TFTs with SiN_X passivation. The OFF-state leakage currents of Si / Ge T-gate TFTs with with

TEOS passivation or SiN_X passivation are almost identical in all experimental split conditions.

Figures 5.12 display the measured OFF-state leakage currents of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation for different drain biases at V_G = -10V. The device channel thickness is 50-nm.The OFF-state leakage currents of Si / Ge T-gate TFTs with TEOS passivation are significantly lower than those of Si / Ge T-gate TFTs with SiN_X passivation. The OFF-state leakage current is increased with increasing gate and drain voltages which enhance the field emission via grain boundary traps in the depletion region near the drain [5.6], [5.7]. In the Si / Ge T-gate TFTs with TEOS passivation, the lateral electric field near the drain can be greatly reduced due to the low κ gate dielectric TEOS oxide layer at the gate edges. The larger OFF-state leakage current of Si / Ge T-gate TFTs with SiNx passivation is due to the larger gate dielectric constant of SiNx at the gate edges and higher lateral electric field near the drain. The OFF-state leakage currents can be decreased with increasing thickness of Ge gate layer and the Ge lateral undercut distances in the Si / Ge T-gate TFTs with TEOS passivation but the OFF-state leakage currents are lightly decreased with only increasing thickness of Ge gate layer in the Si / Ge T-gate TFTs with SiNx passivation.

Figure 5.13 illustrates the measured ON / OFF current ratio of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation in different channel length and constant channel width = 10 μm. The device channel thickness is 50-nm. The ON / OFF current ratio is defined as the ratio of the ON-state current to the minimum OFF-state leakage current. The ON-state current is defined as drain current (I_D) at V_G = 20 V, V_D = 10 V and the minimum OFF-state leakage current is defined as minimum drain current (I_{min}) at V_D = 10 V. The ON-state current degrades with increasing thickness of Ge gate layer in Si / Ge T-gate TFTs

with TEOS passivation but the ON-state current can be maintained with increasing thickness of Ge gate layer in Si / Ge T-gate TFTs with SiNx passivation. It is due to larger the channel series resistance under the thick gate dielectric region at the gate edges in thinner channel thickness (50-nm) Si / Ge T-gate TFTs with TEOS passivation. The minimum OFF-state leakage currents of Si / Ge T-gate TFTs with TEOS passivation or SiN_X passivation are almost identical in all experimental split conditions. Therefore, the Si / Ge T-gate TFTs with 50-nm Ge gate layer have the highest ON / OFF current ratio than those with 100-nm Ge gate layer due to the highest ON-state currents in the Si / Ge T-gate TFTs with TEOS passivation. In the Si / Ge T-gate TFTs with SiN_X passivation, the Si / Ge T-gate TFTs have the identical ON / OFF current ratio in all experimental split conditions. Hence, to optimize the Si / Ge T-gate TFTs with TEOS passivation in two kinds of channel thicknesses (100-nm or 50-nm), the thickness of Ge gate layer should be considered different.

The output characteristics of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation are shown in Figure 5.14. The device channel thickness is 50nm. The Si / Ge T-gate TFTs with TEOS passivation have more saturated output characteristics compared with Si / Ge T-gate TFTs with SiN_X passivation due to lower drain lateral electric field. The kink current of Si / Ge T-gate TFTs with TEOS passivation is reduced considerably compared with that of Si / Ge T-gate TFTs with SiN_X passivation. The Si / Ge T-gate TFTs with 100-nm Ge gate layer have the most saturated output characteristics but the ON-state current degrades with increasing thickness of Ge gate layer in Si / Ge T-gate TFTs with TEOS passivation. The channel series resistances under the thick gate dielectric region at the gate edges raises with increasing thickness of Ge gate layer in thinner channel thickness (50-nm) Si / Ge T-gate TFTs with TEOS passivation.

The Si / Ge T-gate TFTs with SiNx passivation have high ON-state current due

to the high gate dielectric constant of SiNx and low channel series resistance under the thick gate dielectric region at the gate edges. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return [5.18], [5.19]. Since the Si / Ge T-gate TFTs with SiNx passivatiocan have larger lateral electric fields near the drain compared with Si / Ge T-gate TFTs with TEOS passivation, the impact ionization and avalanche multiplication can be enhanced with increasing drain voltage V_{DS} [5.8], [5.13].

5.5 Summary

In this work, a self-aligned Si / Ge T-gate poly-Si TFTs effectively reduce the OFF-state leakage current while still maintaining the ON-state current compared with conventional TFTs. The stacked Si / Ge gate layers were successfully deposited by LPCVD. The thick gate oxide layer at the gate edges and passivation oxide layer were deposited simultaneously in passivation process. The thick gate oxide at the gate edges effectively reduces the vertical and lateral electric fields near the drain without additional mask, LDD, spacer, or sub-gate bias. The Si / Ge T-gate poly-Si TFTs are proved to be a very promising structure with low OFF-state leakage current, improved ON / OFF current ratio, and saturated output characteristics for display system-on-panel applications.

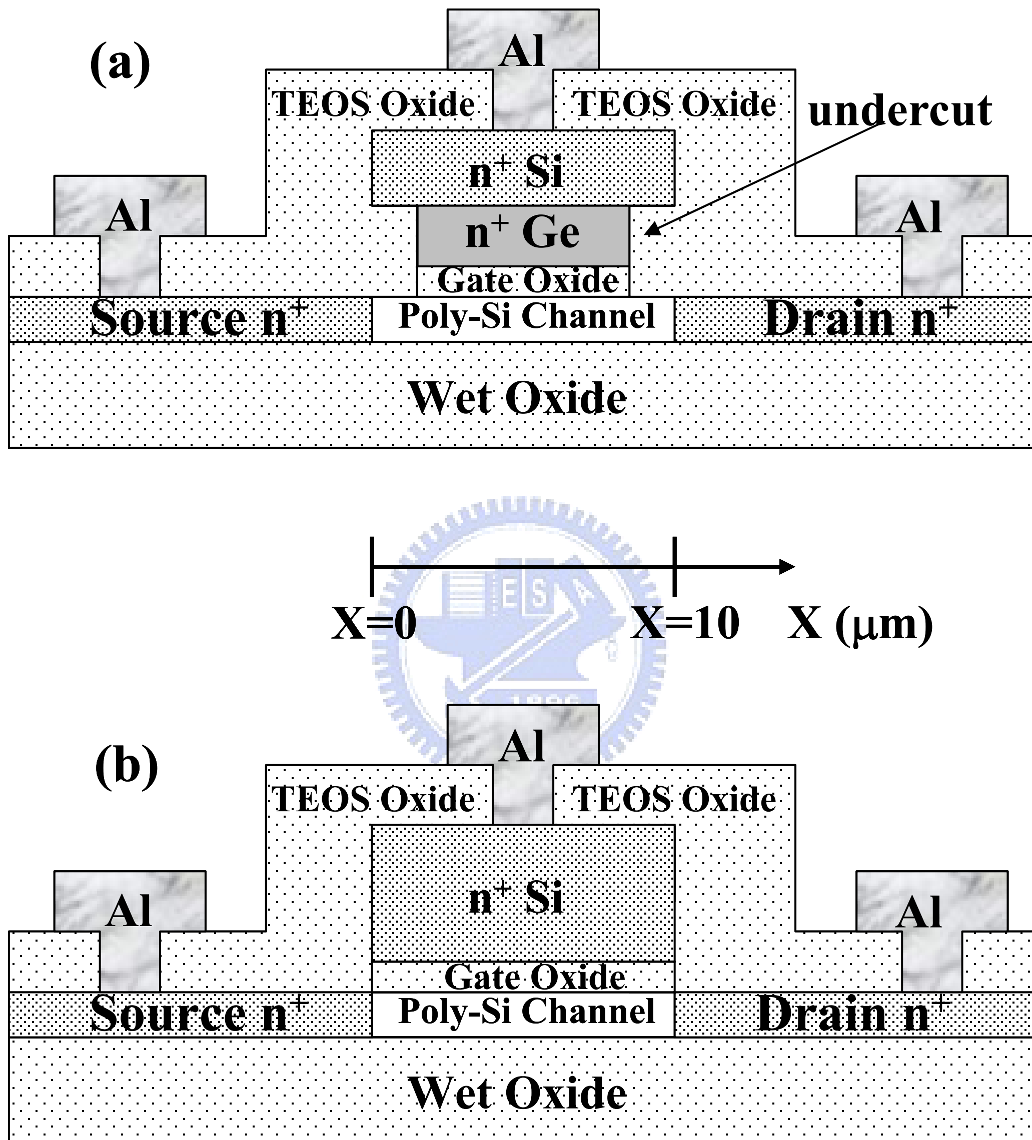
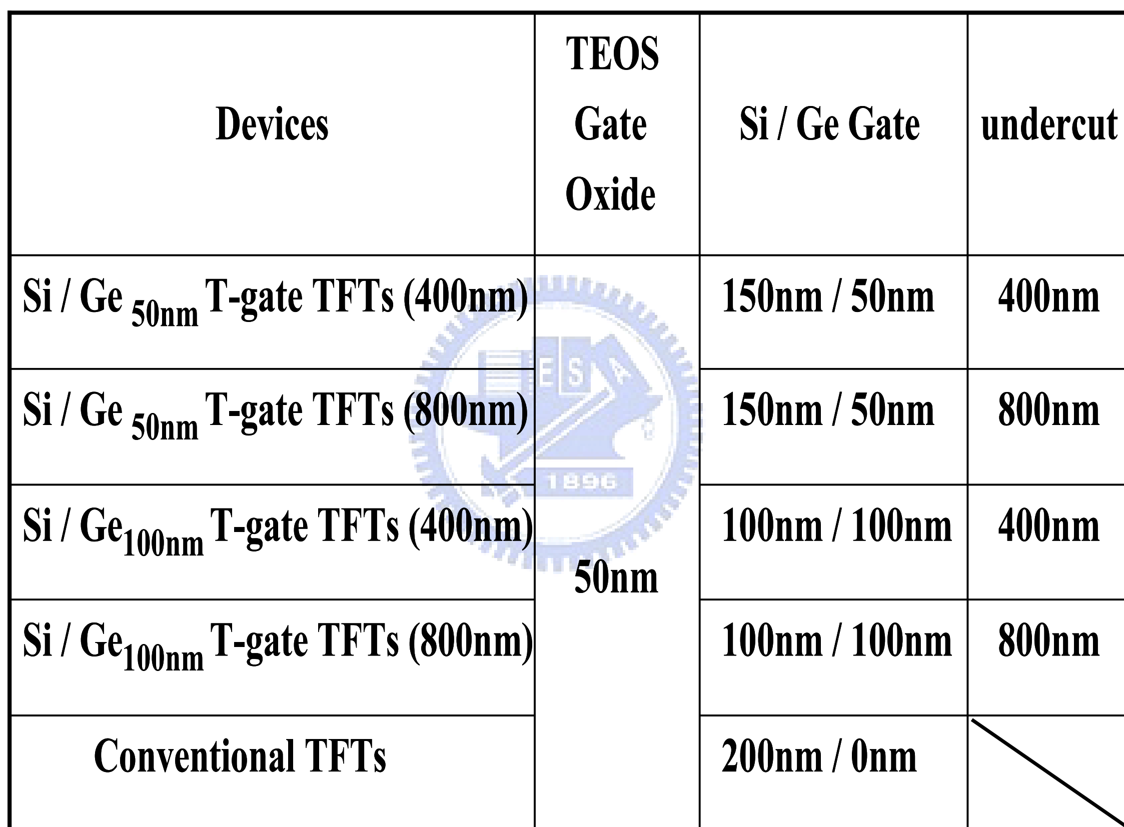
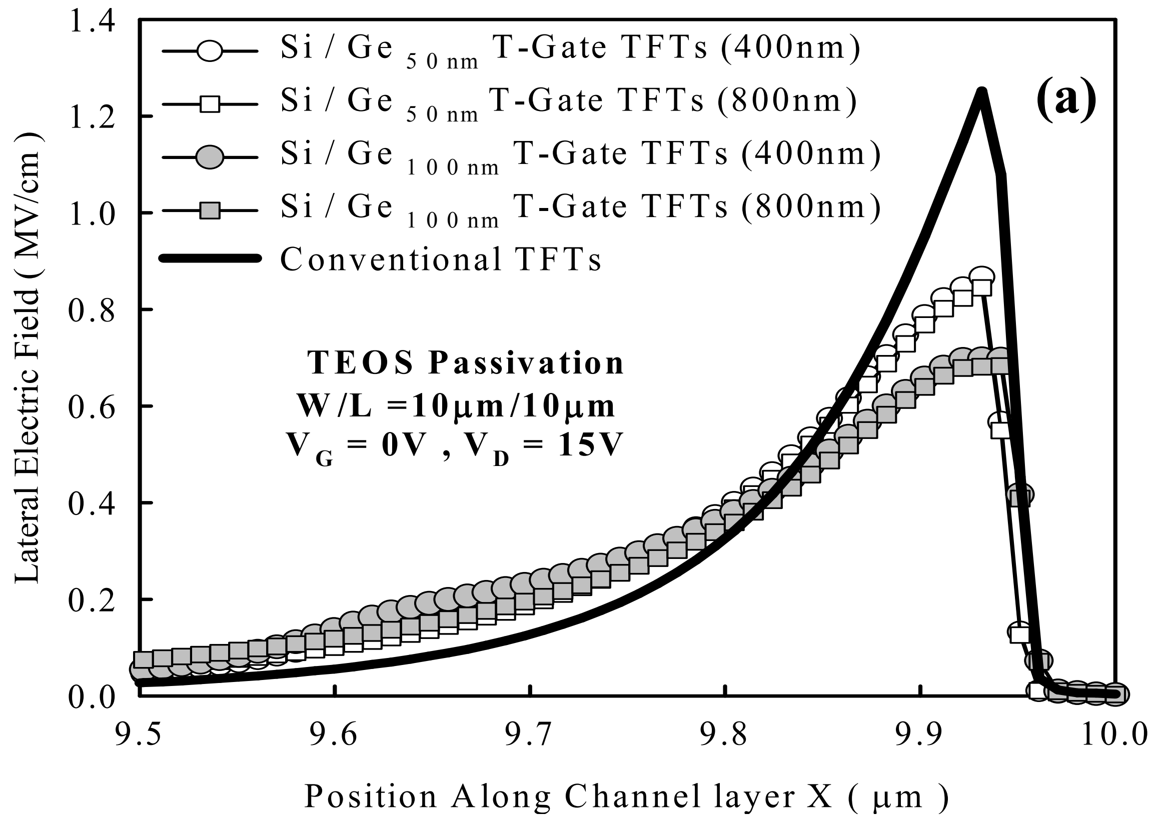


Fig.5.1 The schematic cross-sectional device structures of (a) Si / Ge T-gate TFTs and (b) conventional TFTs.

Table 5.1 The experimental split table of Si / Ge T-gate TFTs and conventional TFTs.



Devices	TEOS Gate Oxide	Si / Ge Gate	undercut
Si / Ge $_{50nm}$ T-gate TFTs (400nm)	50nm	150nm / 50nm	400nm
Si / Ge $_{50nm}$ T-gate TFTs (800nm)		150nm / 50nm	800nm
Si / Ge$_{100nm}$ T-gate TFTs (400nm)		100nm / 100nm	400nm
Si / Ge$_{100nm}$ T-gate TFTs (800nm)		100nm / 100nm	800nm
Conventional TFTs		200nm / 0nm	



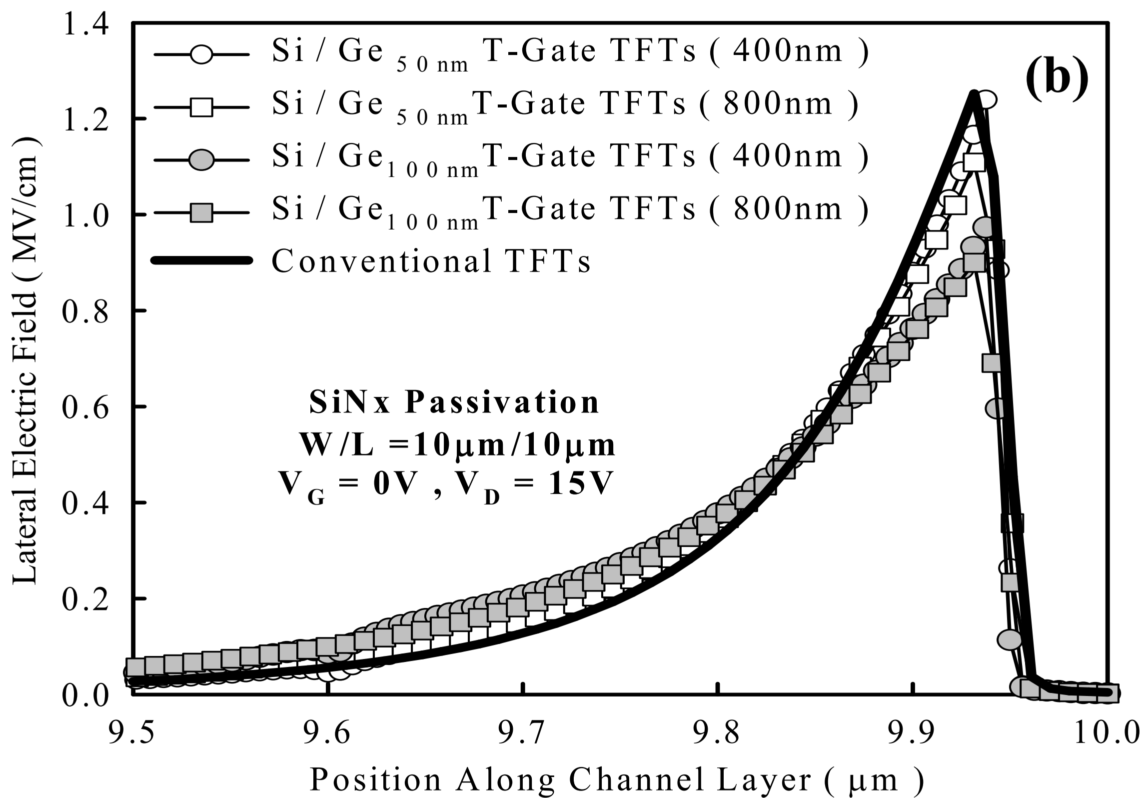
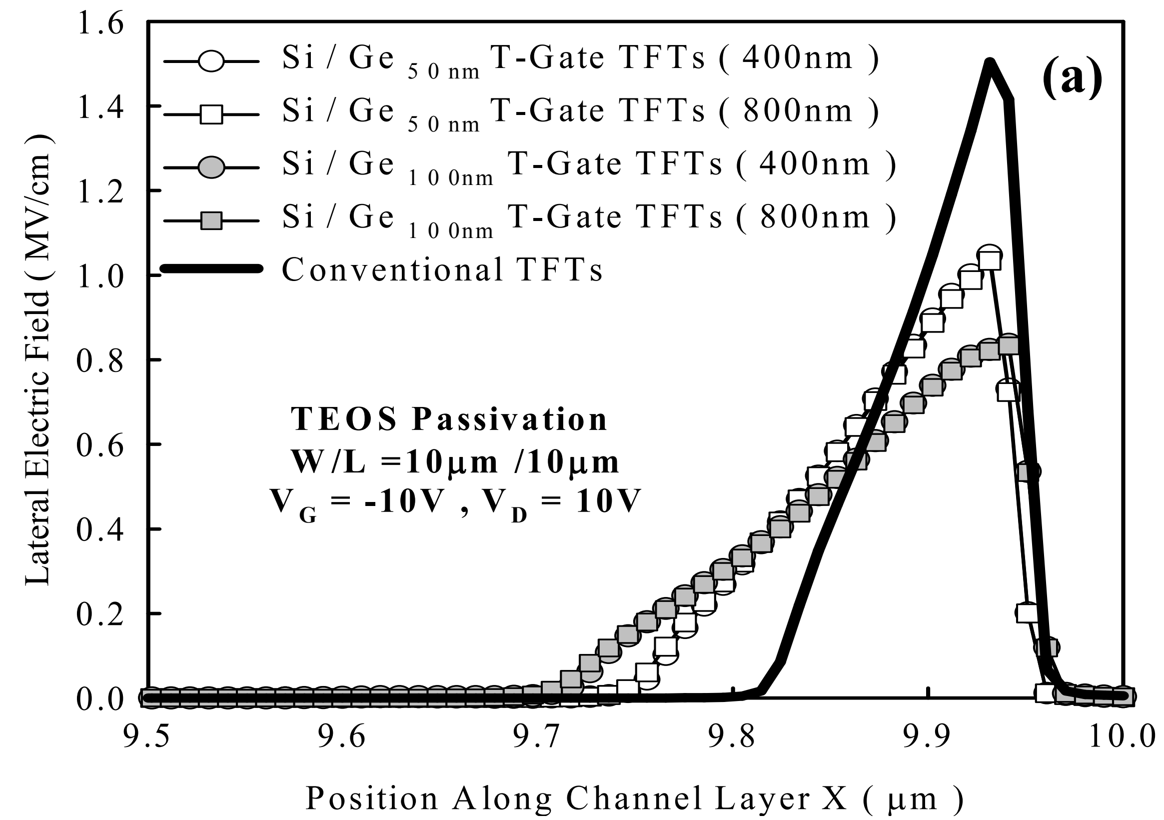


Fig.5.2 The simulated lateral electric field distribution along the channel / gate oxide interface for conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation at $V_G = 0$ V and $V_D = 15$ V.



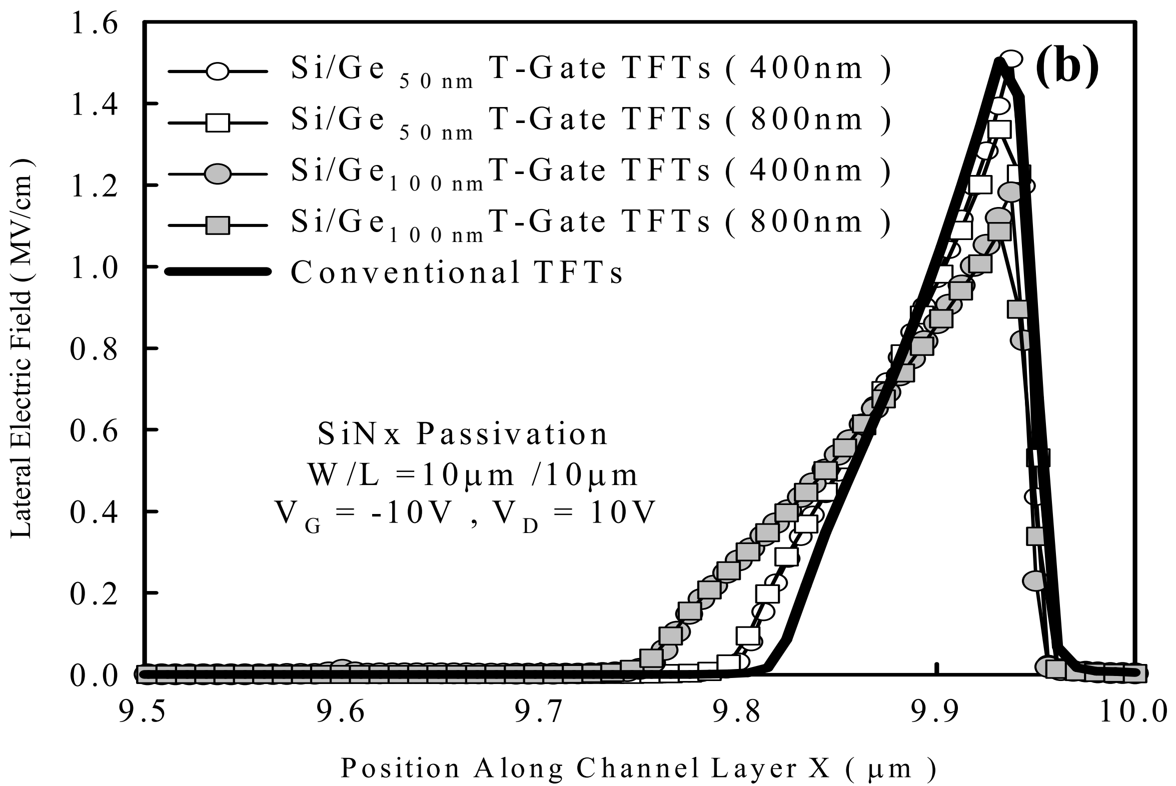


Fig.5.3 The simulated lateral electric field distribution along the channel / gate oxide interface for conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation at V_G = -10V and V_D = 10 V.

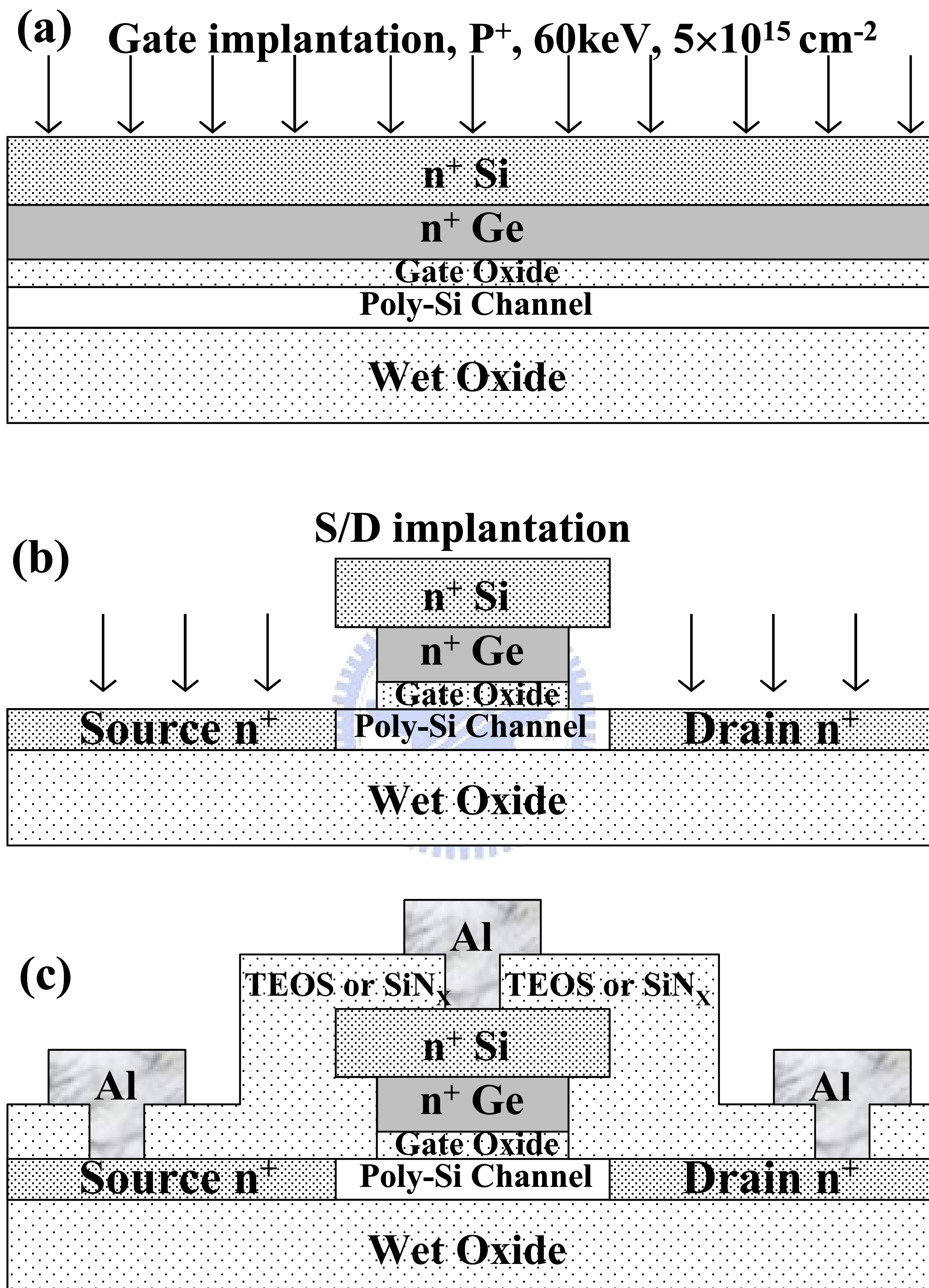


Fig.5.4 The main fabrication process steps of Si / Ge T-gate TFTs.

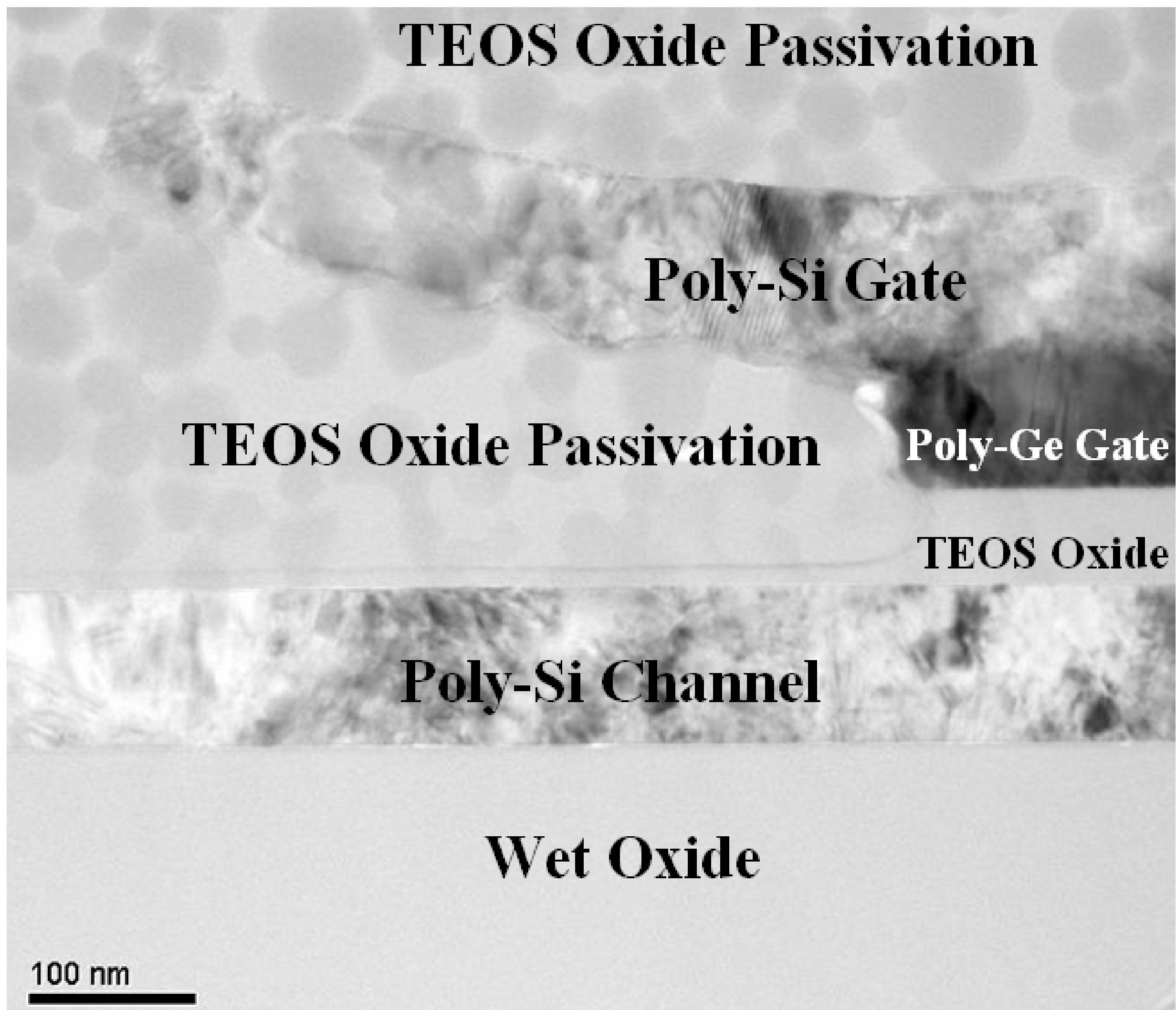
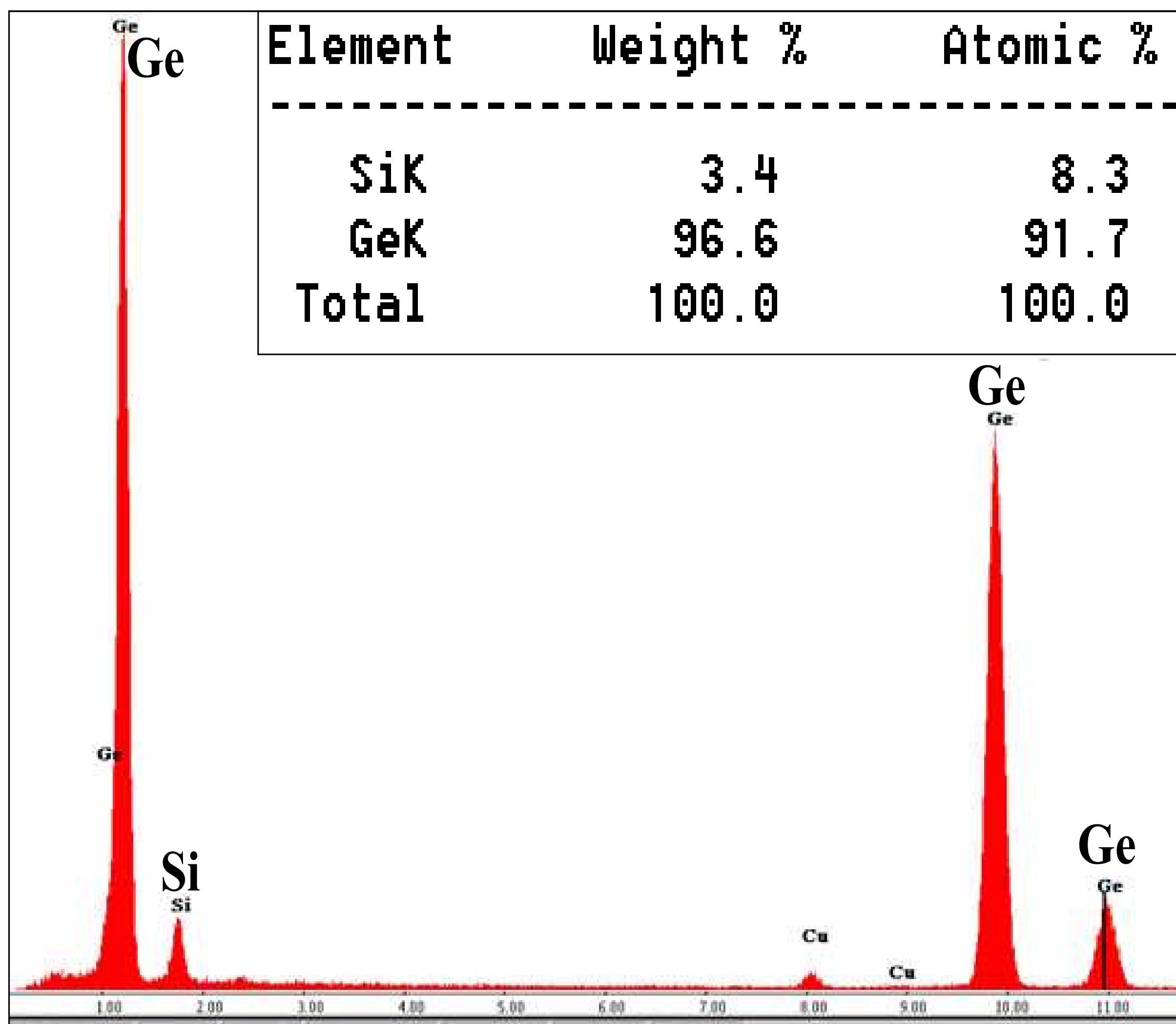
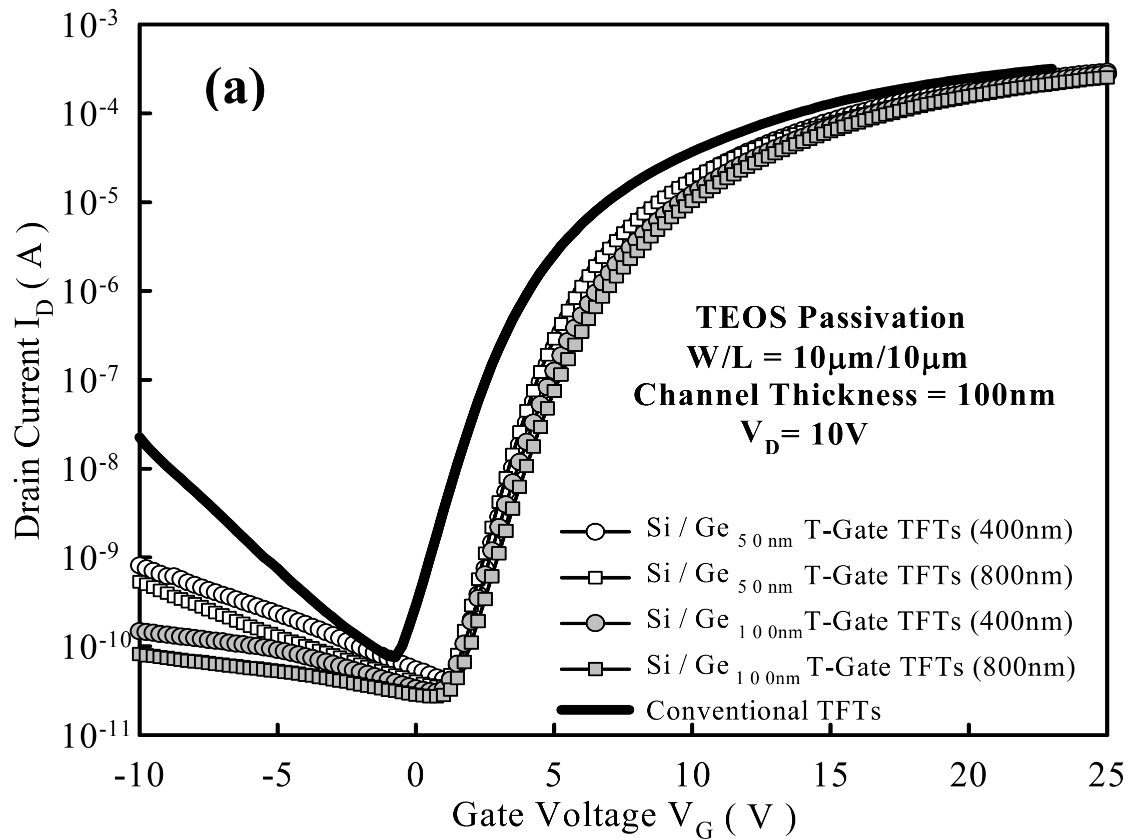


Fig.5.5 The cross-sectional transmission electron microscope (TEM) microphotograph of Si / Ge T-gate TFTs.



Element	Weight %	Atomic %
SiK	3.4	8.3
GeK	96.6	91.7
Total	100.0	100.0

Fig.5.6 The composition of pure Ge gate layer extracted from the energy dispersive x-ray spectrometer analysis.



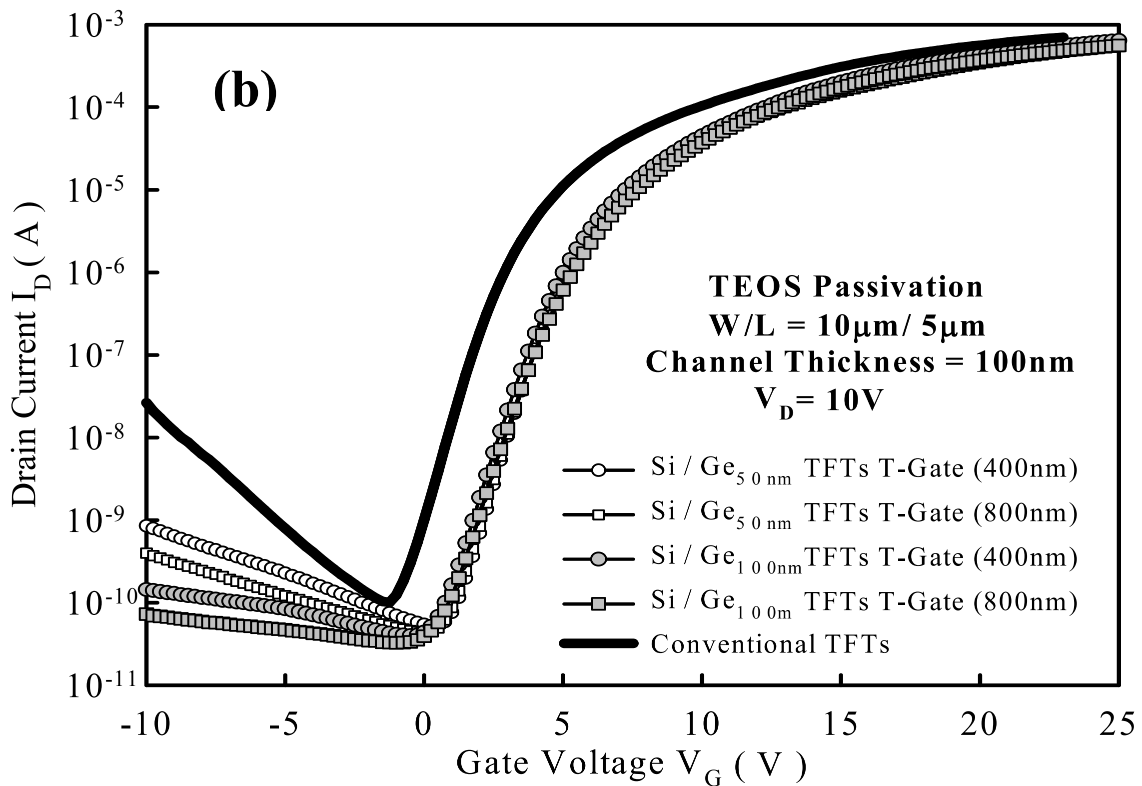


Fig.5.7 The measured transfer characteristics of conventional TFTs and Si / Ge T-gate TFTs with (a) W / L = 10 μm / 10 μm and (b) W / L = 10 μm / 5 μm. The device channel thickness = 100nm.

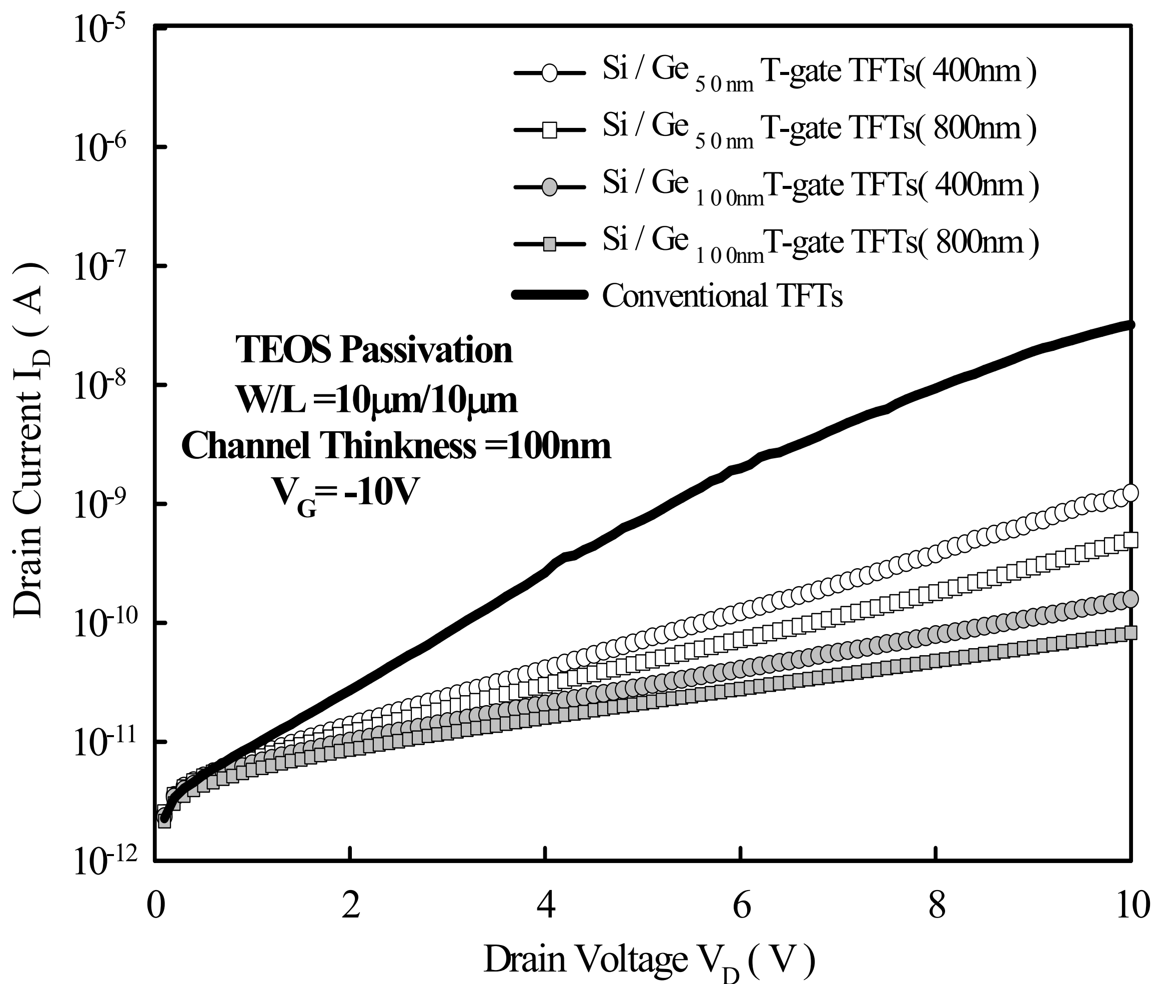


Fig.5.8 The measured OFF-state leakage currents of conventional TFTs and Si / Ge T-gate TFTs with W / L = 10 μm / 10 μm for different drain biases at V_G = -10V. The device channel thickness = 100nm

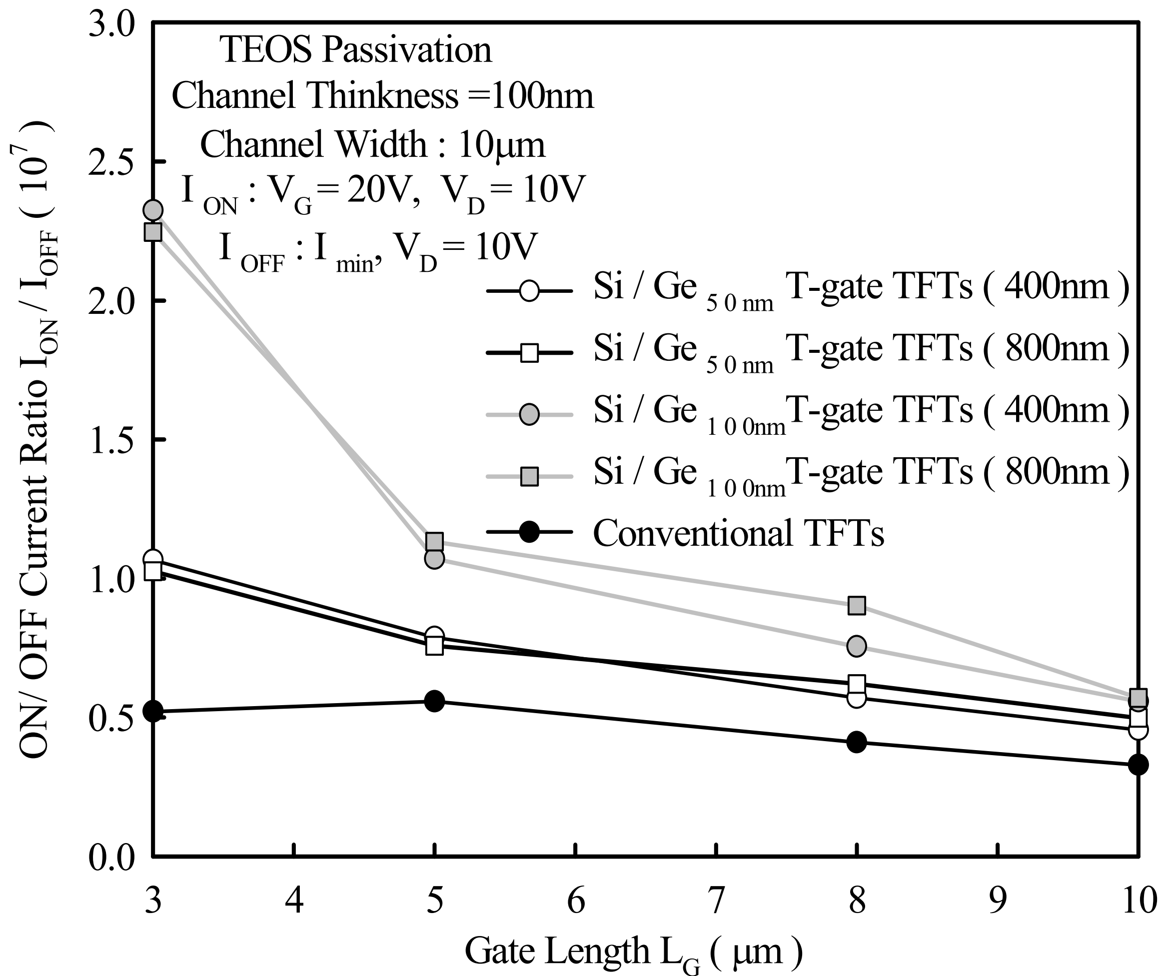


Fig.5.9 The measured ON / OFF currnet ratio of conventional TFTs and Si / Ge T-gate TFTs with W = 10 μm and different channel length. The device channel thickness = 100nm. The ON / OFF current ratio is defined as the ratio of the ON-state current to the minimum OFF-state leakage current. The ON-state current is defined as drain current (I_D) at V_G = 20 V, V_D = 10 V and the minimum OFF-state leakage current is defined as minimum drain current (I_{min}) at V_D = 10 V.

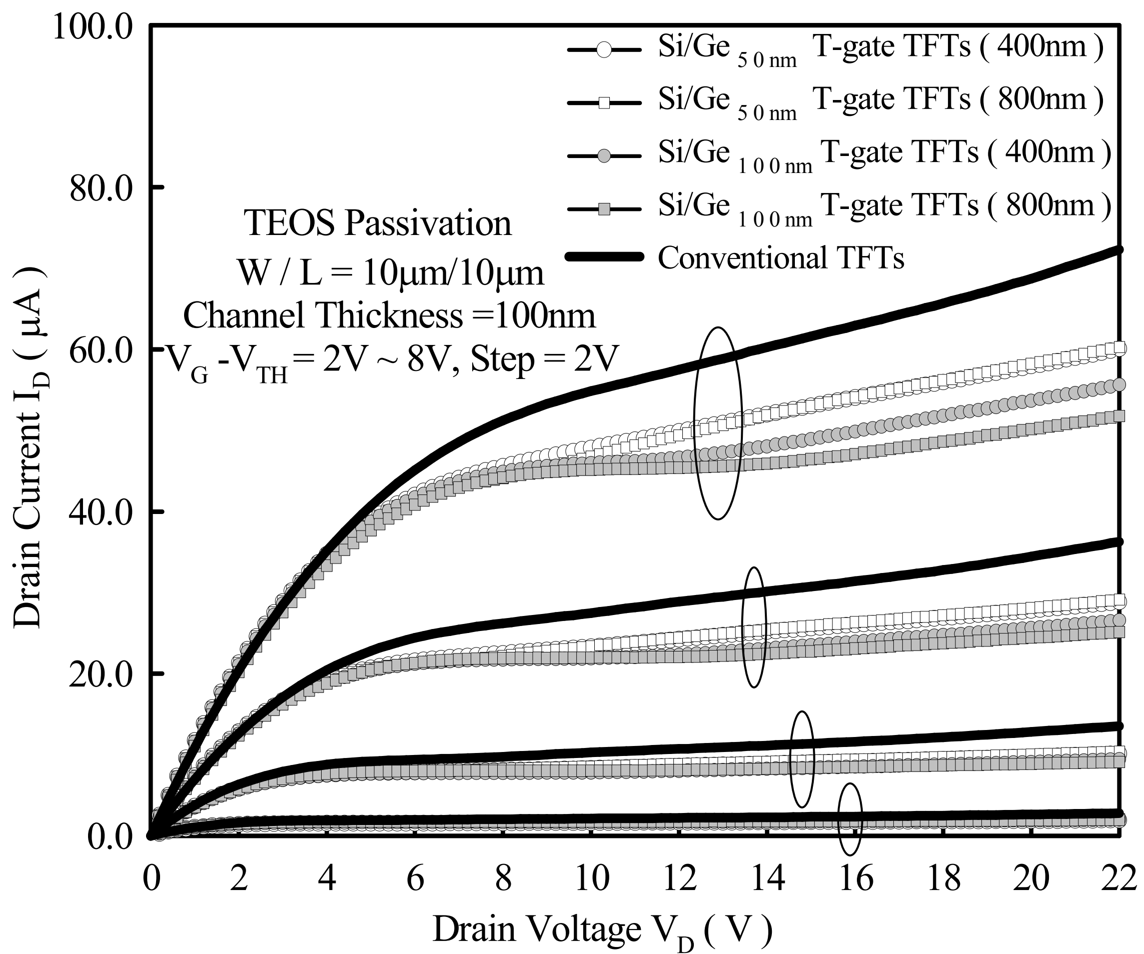
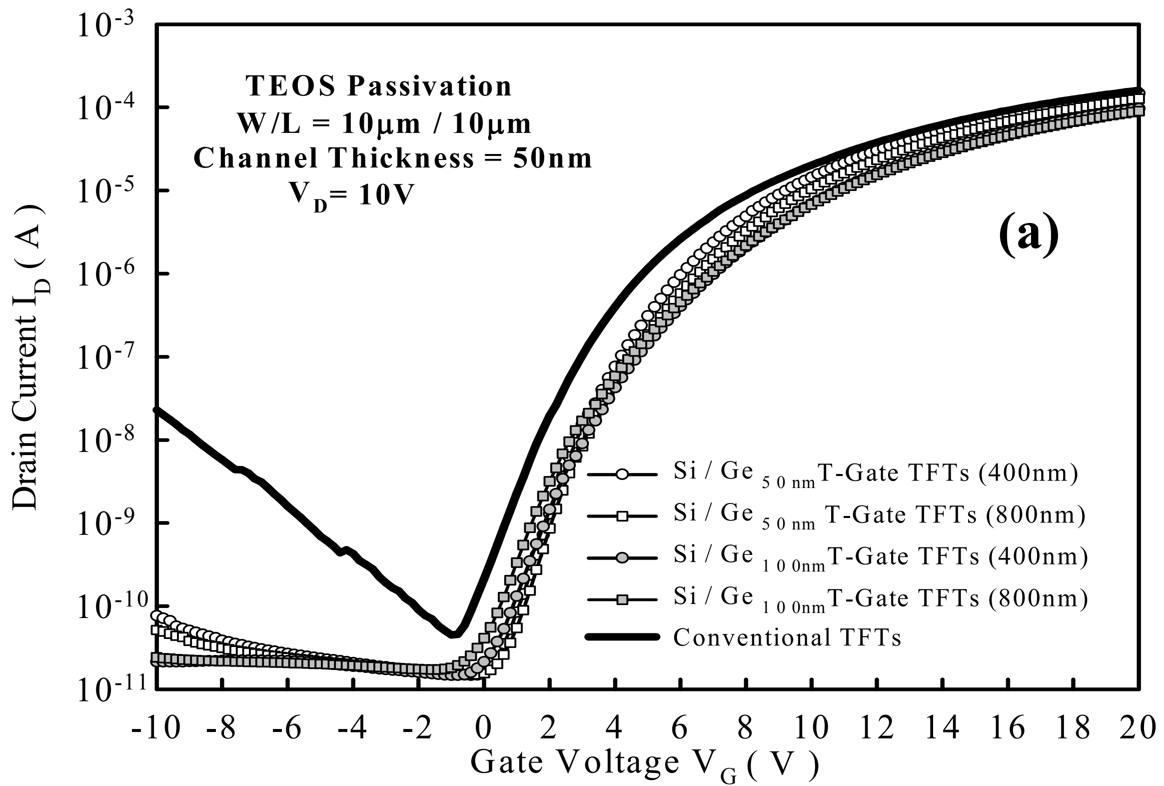


Fig.5.10 The output characteristics of conventional TFTs and Si / Ge T-gate TFTs with W / L = 10 μm / 10 μm. The device channel thickness = 100nm.



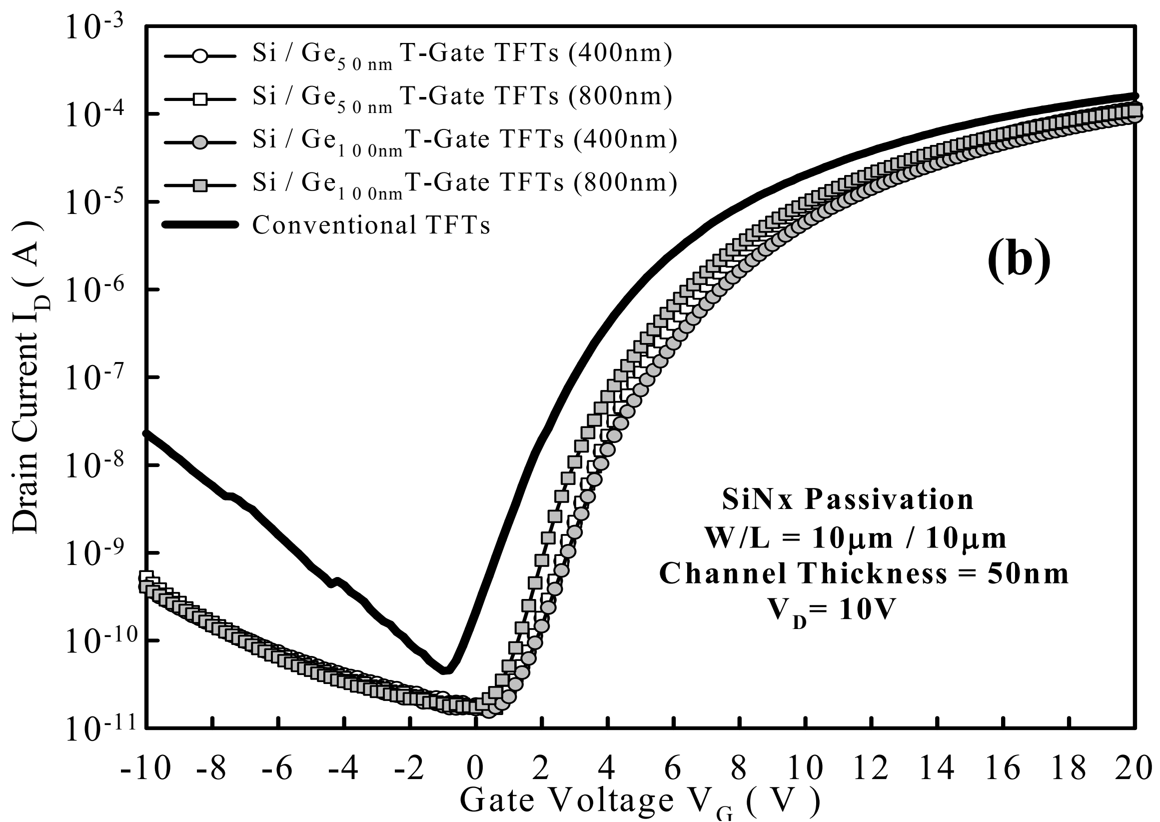
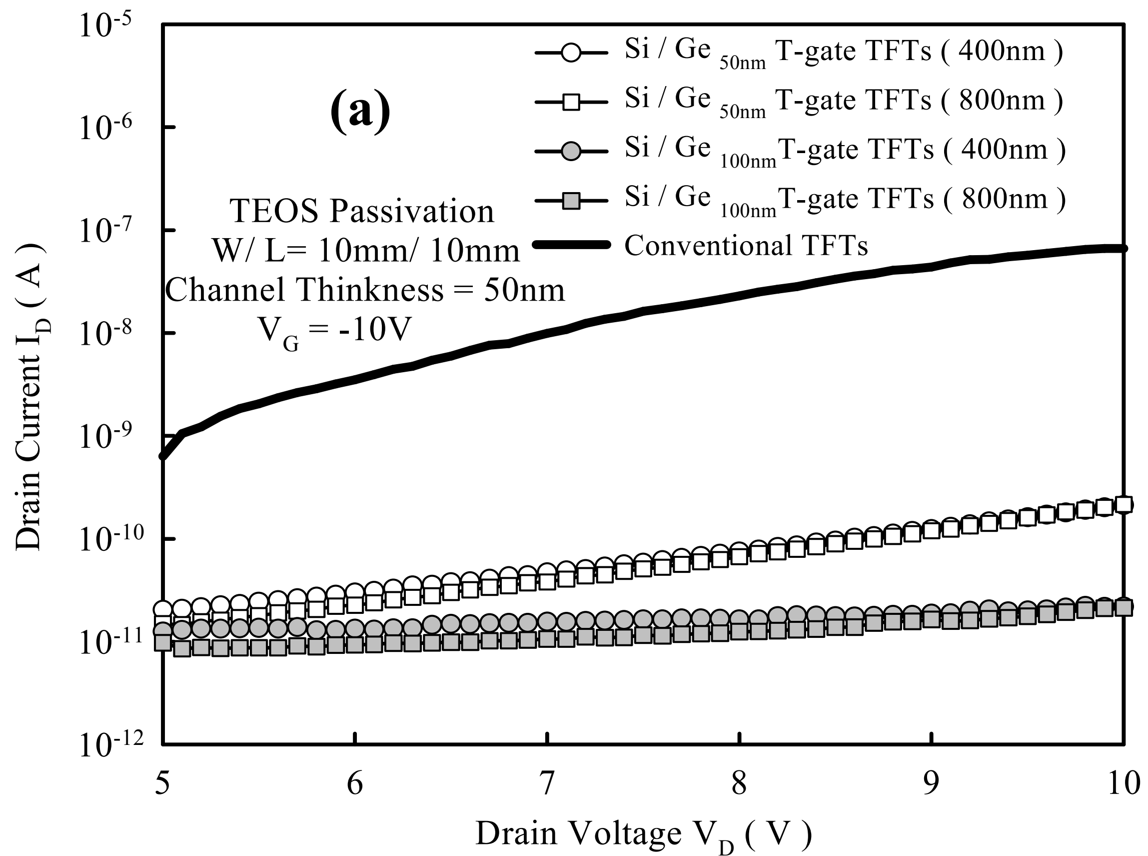


Fig.5.11 The measured transfer characteristics of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation. The device channel thickness = 50nm.



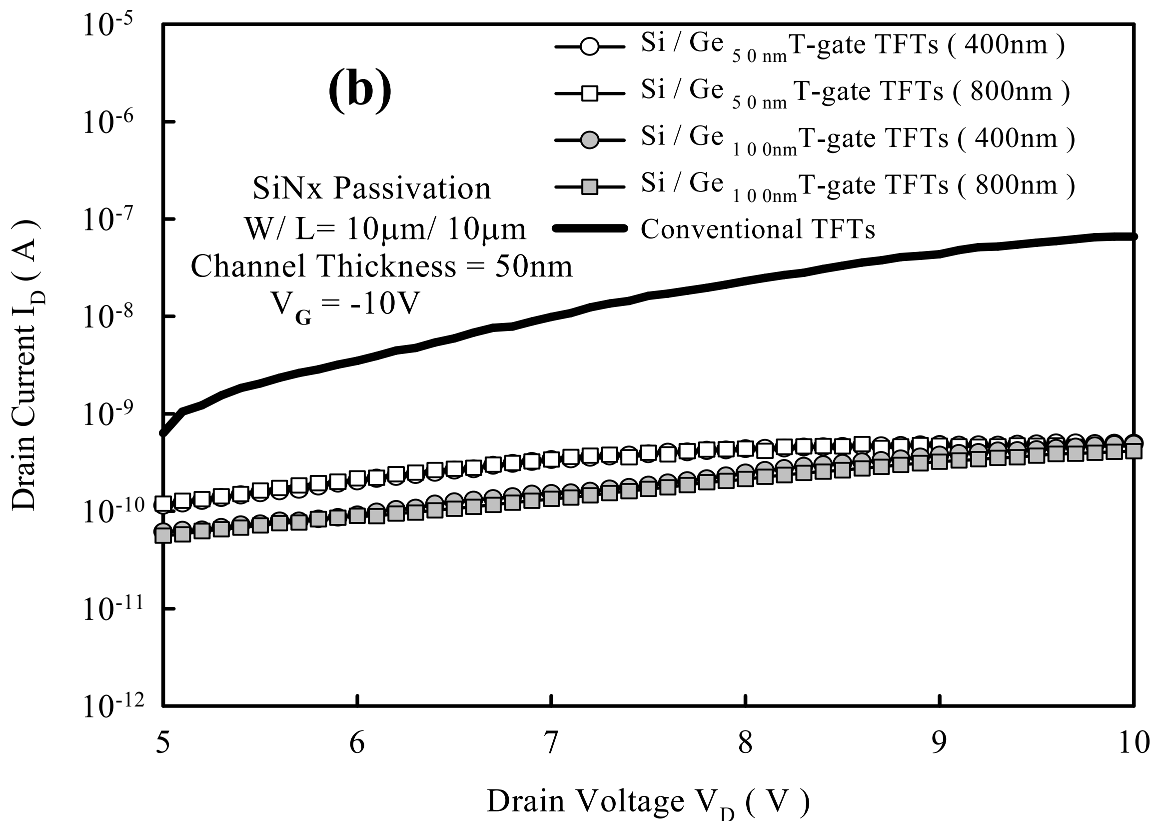


Fig.5.12 The measured OFF-state leakage currents of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation for different drain biases at V_G = -10V. W / L = 10 μm / 10 μm and device channel thickness = 50nm.

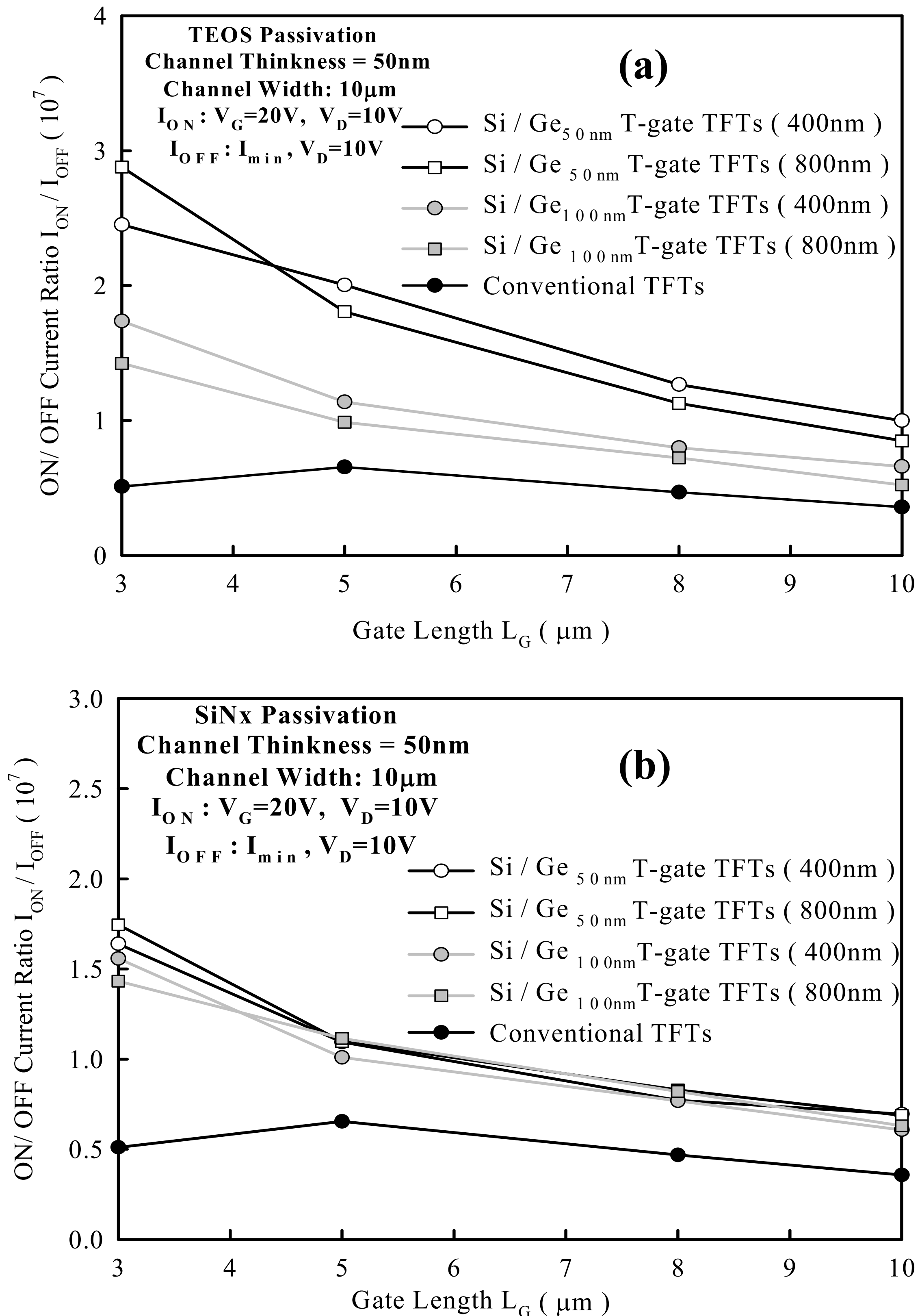
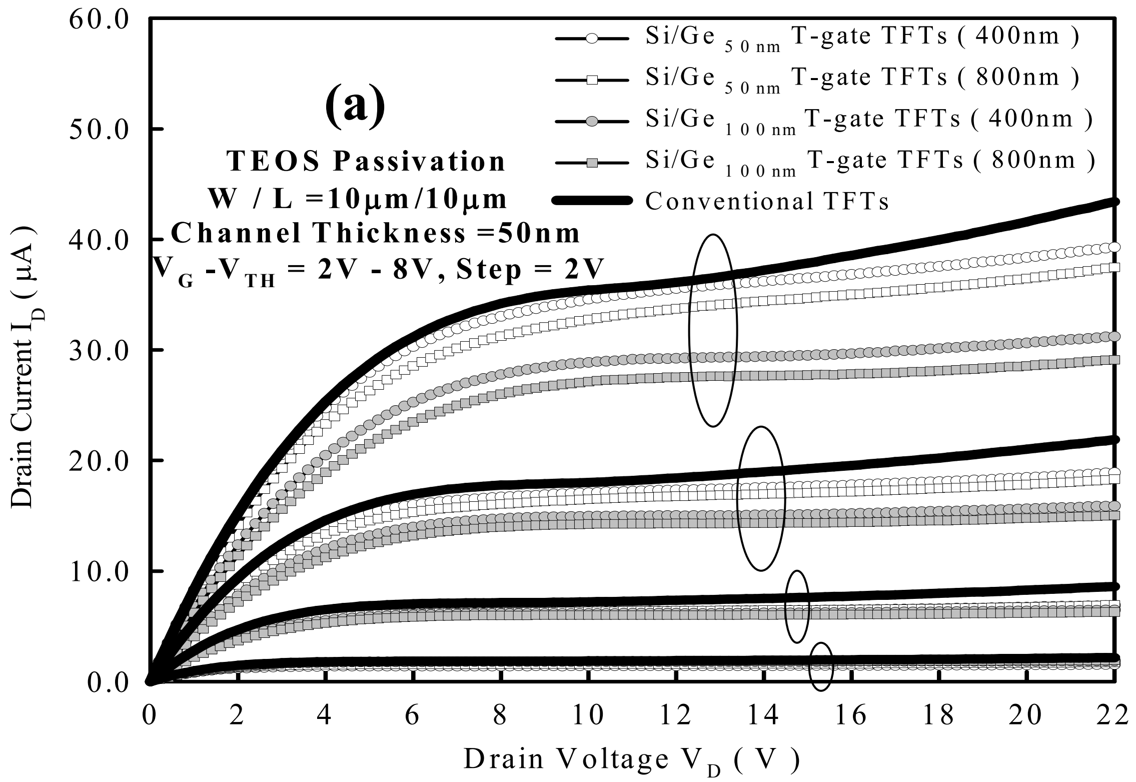


Fig.5.13 The measured ON / OFF current ratio of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation in different channel length and constant channel width = 10 μm. The device channel thickness = 50nm. The ON / OFF current ratio is defined as the ratio of the ON-state current to the minimum OFF-state leakage current. The ON-state current is defined as drain current (I_D) at V_G = 20 V, V_D = 10 V and the minimum OFF-state leakage current is defined as minimum drain current (I_{min}) at V_D = 10 V.



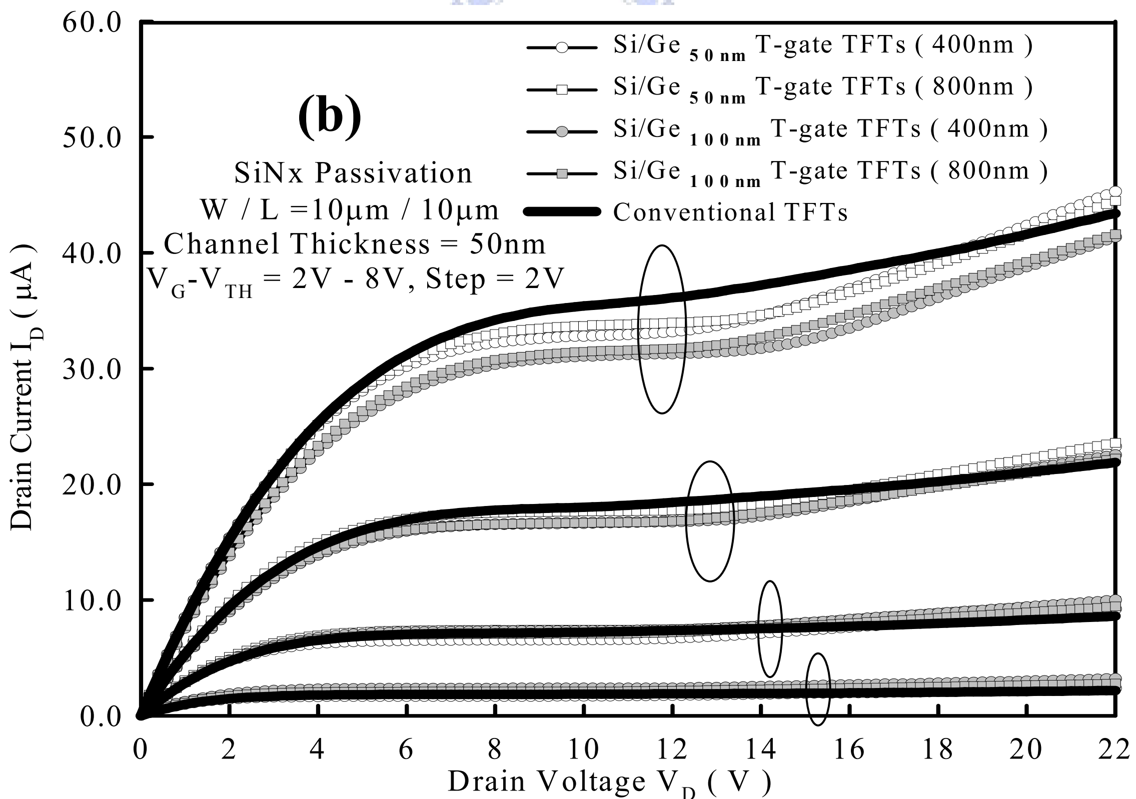


Fig.5.14 The output characteristics of conventional TFTs and Si / Ge T-gate TFTs with (a) TEOS passivation and (b) SiN_X passivation. W / L = 10 μm / 10 μm and device channel thickness = 50nm.

Chapter 6

Characteristics of Poly-Si Thin-Film Transistor Nonvolatile Ge Nanocrystals Memories with High Programming / Erasing Efficiency

6.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are very attractive for 3D integration of active devices and system on top of the panel (SOP) as devices performances improve further [6.1]. The degree of circuit integration will continue to increase as device performances improve further. The entire system will include memories, such as SRAM and nonvolatile FLSAH Memories, solar cells, and touch sensors as well as driver circuits for AMLCDs [6.2]-[6.4]. Poly-Si TFTs have been used as the driving devices for pixel, if they can have nonvolatile memories function, then they are very attractive for 3D integration of active devices and SOP application in the future.

Nanocrystal floating-gate memories offer a number of potential advantages over FLASH devices, including improved scalability, retention, and cyclability, as well as lower voltage operation. In these devices the floating gate is composed of discrete, electrically-isolated particles (rather than a continuous film as in conventional FLASH) [6.5]. Recently, nonvolatile memory devices using Ge or Si nanocrystals (Ge-NCs or Si-NCs) as floating gate (FG) have been widely studied because of its excellent memory performance and high scalability. Ge has smaller

bandgap and similar electron affinity compared with Si. Nonvolatile memory devices using Ge-NCs instead of Si-NCs have superior retention properties [6.6]-[6.11]. In addition, Ge/Si-NCs have been reported to possess superior charge retention capability than Ge or Si-NCs [6.7]. Most of the Ge-NCs fabrication methods, including the thermal annealing of Ge and dielectric mixture, the oxidation of SiGe, and Ge ion implantation all require annealing at high temperature [6.6], [6.9], [6.11].

In this chapter, the new poly-Si TFT nonvolatile Ge-NCs memories with low temperature annealing were proposed. The Ge-NCs embedded in oxide were formed by low-pressure chemical vapor deposition (LPCVD) at 370°C [6.10]. The size and density of Ge-NCs can be easily controlled by GeH_4 deposition time and flow rate. Furthermore, the programming / erasing (P/E) characteristics of thin film nonvolatile memory devices (SOI and TFTs) with floating body effect have been investigated [6.12]. We find that drain voltage is the key point to improve P/E efficiency in thin film nonvolatile memory devices. The mechanism is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the thin film devices. The drain voltage needs to adjust with different gate length and different channel thickness. We can reduce the applied drain voltage to achieve higher P/E efficiency by this floating body effect compared with bulk memory devices.

6.2 Experiment

Fig.6.1 shows the key process flows of poly-Si TFT nonvolatile Ge-NCs memories. First, a 50- or 100-nm amorphous silicon (a-Si) active region layer was deposited by LPCVD at 550°C on wet oxide and then was crystallized by solid phase crystallization (SPC) at 600°C for 24-hr. After the active region patterning, an 11-nm tetraethoxysilane (TEOS) tunneling oxide layer was deposited by LPCVD. Then a

stacked ultra thin a-Si capping layer / pure Ge-NCs / a-Si nuclei, a 44-nm TEOS blocking oxide layer, and a 200nm a-Si gate layer were deposited in sequence by LPCVD (Fig.6.1a). After deposition of a-Si nuclei, the pure Ge-NCs were directly deposited by using GeH_4 at 370°C. The ultra thin a-Si capping layer can prevent the pure Ge-NCs from oxidation in subsequent processes. This way, the pure Ge-NCs embedded in oxide were easy to control the real thickness of tunneling oxide. After gate implantation and defining gate electrode, a self-aligned implantation was used to form the n^+ S/D (Fig.6.1b). After passivation process, dopants were activated by furnace at 600°C for 12-hr. After contact and metallization processes (Fig.6.1c), NH_3 plasma treatments were implemented after sintering at 400°C for 30-min.

6.3 Results and Discussion

6.3.1 Formation of Ge-NCs Embedded in Oxide

Figure 6.2 shows schematics of the two-step growth process of Ge-NCs. First, the a-Si nuclei were deposited by using SiH_4 as a gaseous precursor at 550°C on tunneling SiO_2 surface. This way, we were able to adjust the a-Si nuclei density and, hence, the density of the Ge-NCs was between 10^9 cm^{-2} and slightly less than 10^{12} cm^{-2}. Second, once the a-Si nuclei were deposited, we stopped the SiH_4 gas flow. The sample was left under low pressure CVD chamber without oxidizing the a-Si nuclei. After cooling down CVD chamber temperature to 370°C, GeH_4 was introduced to selectively grow Ge-NCs on the a-Si nuclei. This way, the a-Si nuclei were not oxidized because they were never exposed to oxygen. Indeed, no Ge-NCs would grow on oxidized a-Si nuclei [6.10].

Figures 6.3 show the atomic force microscope (AFM) microphotographs of Ge-NCs for (a) 80sec and (b) 120sec GeH_4 deposition time at 370°C. The size of

Ge-NCs can be easily controlled by GeH_4 deposition time. As shown in Fig. 6.3, the size of Ge-NCs was enlarged with increasing GeH_4 deposition time. The low Ge-NCs deposition temperature is suitable for low temperature poly-Si TFTs applications.

Fig.6.4 displays the cross section Transmission Electron Microscope (TEM) microphotographs of poly-Si TFT nonvolatile Ge-NCs memories. A high resolution image of one typical Ge-NC is inserted for revealing the geometrical and crystal characteristics of the Ge-NC. Energy dispersive X-ray diffraction analysis shows that the dark dots between the two oxide layers are pure Ge. The blocking oxide and tunneling oxide thickness is about 44nm and 11nm respectively. The sizes of the Ge-NCs are about 9nm~12nm and the density of the Ge-NCs is about $2 \sim 4\times10^{11}cm^{-2}$. The pure Ge-NCs embedded in oxide are easy to control the real thickness of tunneling oxide. In NC nonvolatile memories, the size of NC is an important factor that affects electrical characteristics. The size of Ge-NC embedded in oxide should not be scaled below 5 nm, because the quantum confinement effect becomes very significant for such small Ge-NC [6.13], [6.14]. Large quantum confinement leads to the conduction band in the nanocrystal being much higher than that of the Si substrate resulting in enhanced leakage from NC and shorter retention time [6.6]. The TEM microphotographs of Ge-NCs suggest that the Ge-NCs embedded in oxide show good thermal stability after several thermal processing steps including source/drain anneal.

6.3.2 Channel Hot Electron Injection Programming Mechanism in Poly-Si TFTs

Figures 6.5 indicate the channel hot electron injection program mechanism in poly-Si TFTs with gate length = 1μm ~ 0.8μm. The floating body induced drain avalanche is biased at (a) $V_G = 0V$, $V_D = 8\sim12V$ and (b) $V_G = 10V$, $V_D = 8\sim12V$. The additional electron injection is due to the floating body induced drain avalanche with

parasitic n-p-n bipolar in the thin film devices. The drain avalanche can be enhanced by floating body in the thin film devices [6.12]. Figures 6.6 show the measured floating body induced drain avalanche currents of poly-Si TFTs with different channel thickness and (a) gate length = 1μm (b) ate length = 0.8μm. With increasing drain voltage, the added drain current enhances impact ionization and parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return [6.15], [6.16]. In the Fig.6.6, we can control the drain voltage before strong drain avalanche breakdown for different gate length and channel thickness in program region. These modified drain voltages are used to achieve high channel hot electron injection efficiency in the program region.

Table 6.1 is the split table of the applied drain biases with different gate length and channel thickness in the program region from measured results of Fig.6.6. The applied drain voltage can be reduced with short gate length and thick channel thickness.

6.3.3 Programming and Erasing Characteristics of Poly-Si TFT Nonvolatile Ge-NCs Memories

The measured transfer characteristics of poly-Si TFT nonvolatile Ge-NCs memories in the P/E states are shown in Fig.6.7. The memory windows of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm can be larger than 7~8V for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm. The threshold voltages V_{TH} is defined as $I_D = W / L \times 100nA$. The memory window is the threshold voltages shift between erase state and program state.

Next, we apply the drain voltage before strong drain avalanche breakdown for different gate length and channel thickness in program region. According to Table 6.1, the memories with channel thickness = 50-nm and W / L = 1μm / 1μm are biased at V_D = 11V, 12V in the program region. Figures 6.8 show the measured programming

characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 1μm / 1μm in the program region biased at (a) V_G = 10V, V_D = 11V, 12V and (b) V_G = 12V, V_D = 11V, 12V. In the Fig.6.8, the program speed of V_D = 12V is faster than that of V_D = 11V for (a) constant V_G=10V or (b) constant V_G =12V. According to Table 6.1, the memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm are biased at V_D = 10V, 11V in the program region. Figures 6.9 display the measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm in the program region biased at (a) V_G = 10V, V_D = 10V, 11V and (b) V_G = 12V, V_D = 10V, 11V. When gate length is scaled down to 0.8μm, the drain voltage is also scaled down to V_D = 10V, 11V. The program speed of V_D = 11V is faster than that of V_D = 10V for (a) constant V_G=10V or (b) constant V_G=12V.

According to Table 6.1, the memories with channel thickness = 100-nm and W / L = 1μm / 1μm are biased at V_D = 10V, 11V in the program region. Figures 6.10 show the measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 1μm / 1μm in the program region biased at (a) V_G = 10V, V_D = 10V, 11V and (b) V_G = 12V, V_D = 10V, 11V. In the Fig.6.10, the program speed of V_D = 11V is faster than that of V_D = 10V for (a) constant V_G=10V or (b) constant V_G=12V. According to Table 6.1, the memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm are biased at V_D = 9V, 10V in the program region. Figures 6.11 display the measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm in the program region biased at (a) V_G = 10V, V_D = 9V, 10V and (b) V_G = 12V, V_D = 9V, 10V. When gate length is scaled down to 0.8μm, the drain voltage is also scaled down to V_D = 9V, 10V. The program speed of V_D = 10V is faster than that of V_D = 9V for (a) constant V_G=10V or (b) constant V_G

=12V.

Table 6.2 is the program efficiency of poly-Si TFT nonvolatile Ge-NCs memories for different gate length and channel thickness in program region. The program efficiency can be significantly enhanced with increased V_D. In the Table 6.2, the program V_{TH} shifts are almost twice in program region for same gate length and channel thickness. For example, the program V_{TH} shift of V_D =12V is 4.01V and the program V_{TH} shift of V_D =11V is 2.11V in the memories with channel thickness = 50-nm and W / L = 1μm / 1μm. These results suggest that the modified drain voltages are used to achieve high channel hot electron injection efficiency for different gate length and channel thickness in the program region.

In order to investigate the erase efficiency of poly-Si TFT nonvolatile Ge-NCs memories for different gate length and channel thickness, we use the same drain voltage condition for erasing operation. We employed band-to-band hot hole injection mechanism for erasing. The measured erasing characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm in the erase region biased at (a) V_G = -10V, V_D = 10V, 11V and (b) V_G = -12V, V_D = 10V, 11V are shown in Fig.6.12. The erase speed of V_D = 11V is faster than that of V_D = 10V for (a) constant V_G =-10V or (b) constant V_G =-12V.

Figures 6.13 show the measured erasing characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm in the erase region biased at (a) V_G = -10V, V_D = 9V, 10V and (b) V_G = -12V, V_D = 9V, 10V. The erase speed of V_D = 10V is faster than that of V_D = 9V for (a) constant V_G = -10V or (b) constant V_G = -12V. The band-to-band hot hole injection erasing efficiency cab be enhanced by floating body effect induced drain avalanche.

In the thin film devices, we apply the drain voltages before strong drain avalanche breakdown for different gate length and channel thickness in program

region. These modified drain voltages are used to achieve high channel hot electron injection efficiency in the program region. The applied drain voltage can be reduced with short gate length and thick channel thickness.

6.3.4 Gate and Drain Disturbance Characteristics of Poly-Si TFT Nonvolatile Ge-NCs Memories

Figures 6.14 show the measured gate disturbance characteristics of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm in the erased state. Two different gate voltages (V_G = 10, 12 V, V_D = V_S = 0 V) were applied to the fresh devices. The poly-Si TFT nonvolatile Ge-NCs memories show good gate disturbance characteristics. In this work, the total thickness of tunneling oxide and blocking oxide is about 45-nm and the applied gate voltages are smaller than Fowler-Nordheim tunneling voltage.

Figures 6.15 display the measured drain disturbance characteristics of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm. Two different drain voltages (V_D = 10, 11 V, V_G = V_S = 0 V for channel thickness = 50-nm and V_D = 9, 10 V, V_G = V_S = 0 V for channel thickness = 100-nm) were applied to the fresh devices. The worst case is V_D = 11 V, V_G = V_S = 0 V for channel thickness = 50-nm. We observe that the V_{TH} shift value increased as the drain disturb time increased. This phenomenon is believed to be due to strong drain avalanche which makes the resultant V_{TH} shift toward positive rather than negative. When applied drain voltage is larger than critical drain voltage, the strong drain avalanche breakdown occurs. When the drain voltage is close to critical drain voltage, the device is under soft drain avalanche. The devices under critical drain voltage have poor drain disturbance characteristics. It implies that the

critical drain voltage is close to 11V for device with W / L = 0.8μm / 0.8μm and channel thickness = 50-nm. These critical drain voltages can be used to achieve high channel hot electron injection efficiency in the program region but resulting in poor drain disturbance characteristics. We have to choose the appropriate drain voltage to achieve high program / erase speed and less drain disturbance for different gate length and channel thickness.

6.3.5 Data Retention and Rewrite Endurance Properties of Poly-Si TFT Nonvolatile Ge-NCs Memories

Figures 6.16 indicate the measured retention characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm at (a) room temperature and (b) 85°C. Figures 6.17 displays the measured retention characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm at (a) room temperature and (b) 85°C. The poly-Si TFT nonvolatile Ge-NCs memories with two-level threshold voltage states have good retention characteristics at room temperature and 85 °C due to the sufficiently deep trapping level of Ge-NCs. Compared with Si, Ge has a narrower bandgap and a similar electron affinity. Nonvolatile memory devices using Ge-NCs instead of Si-NCs have superior retention properties. In addition, Ge/Si-NCs have been reported to possess superior charge retention capability than Ge or Si-NCs [6.6]-[6.11]. We believe that retention characteristics can be significantly improved by using high quality tunneling oxide and blocking oxide.

The measured endurance characteristics of 10^4 P/E cycled poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm are shown in Fig.6.18. The programming and erasing conditions are V_G =10V, V_D = 11V for 200 μs and V_G = -10

V, V_D = 11V for 10 μs for channel thickness = 50-nm. The programming and erasing conditions are V_G =10V, V_D = 10V for 300 μs and V_G = -10 V, V_D = 10V for 10 μs for channel thickness = 100-nm. We find that the memory window narrowing rate increases with increasing P/E cycles. The memory windows narrow to about 2V after 10^4 P/E cycles. It may be due to the stress induced electron traps generated in the tunnel oxide during cycling. We believe that endurance characteristics can be significantly improved by using high quality tunneling oxide. Thick tunnel oxide has more serious memory window closure. Thus, the tradeoff between retention and endurance characteristics shall be carefully conducted [6.17].

6.4 Summary

In this work, poly-Si TFT nonvolatile Ge-NCs memories have been reported and demonstrated. Ge-NCs were grown using a two-step process. In step 1, the Si nuclei are formed on the SiO_2 surface. Then, in step 2, the Ge-NCs grow selectively on the Si nuclei. The sizes of the Ge-NCs are about 9nm~12nm and the density of the Ge-NCs is about $2 \sim 4\times10^{11}cm^{-2}$. The pure Ge-NCs embedded in oxide were easy to control the real thickness of tunneling oxide. In addition, we find that drain voltage is the key point of P/E efficiency in thin film nonvolatile memory devices. The operating drain voltage changes with different gate length and different channel thickness. Experimental results show that the poly-Si TFT nonvolatile Ge-NCs memories have high P/E efficiency, long charge retention time, less gate and drain disturbance, and good endurance characteristics. Thus this device is very promising for future nonvolatile memory applications in 3D integration of active devices and SOP.

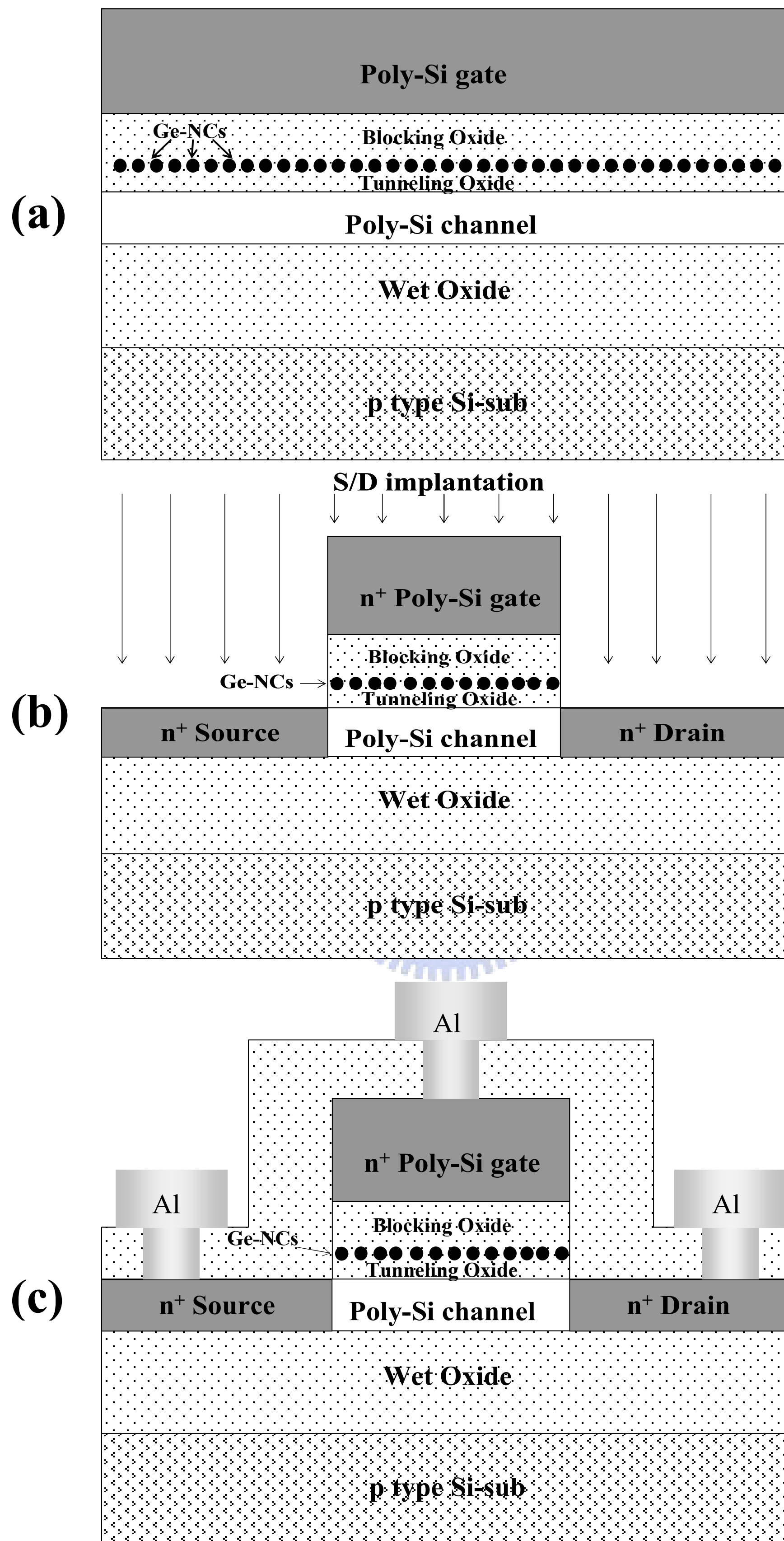


Fig.6.1 The key process flows of poly-Si TFT nonvolatile Ge-NCs memories.

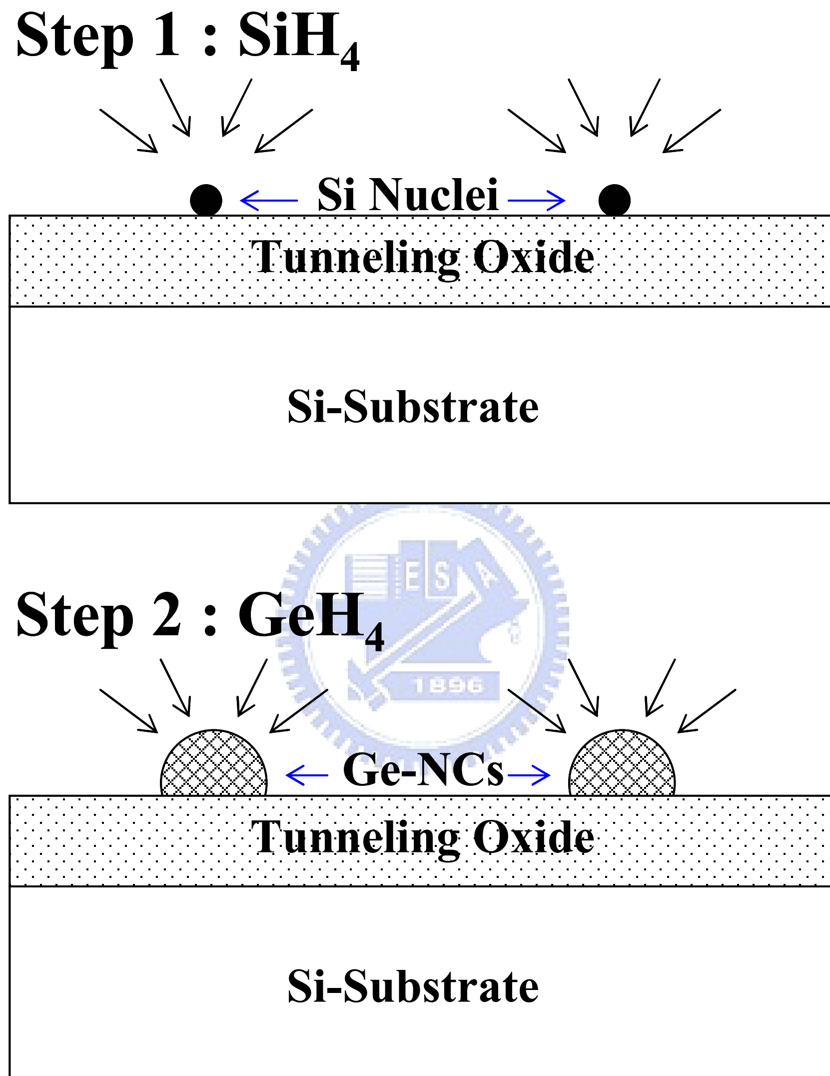


Fig.6.2 The schematics of the two-step growth process of Ge-NCs. In step 1, the Si nuclei are formed on the SiO_2 surface. Then, in step 2, the Ge-NCs grow selectively on the Si nuclei.

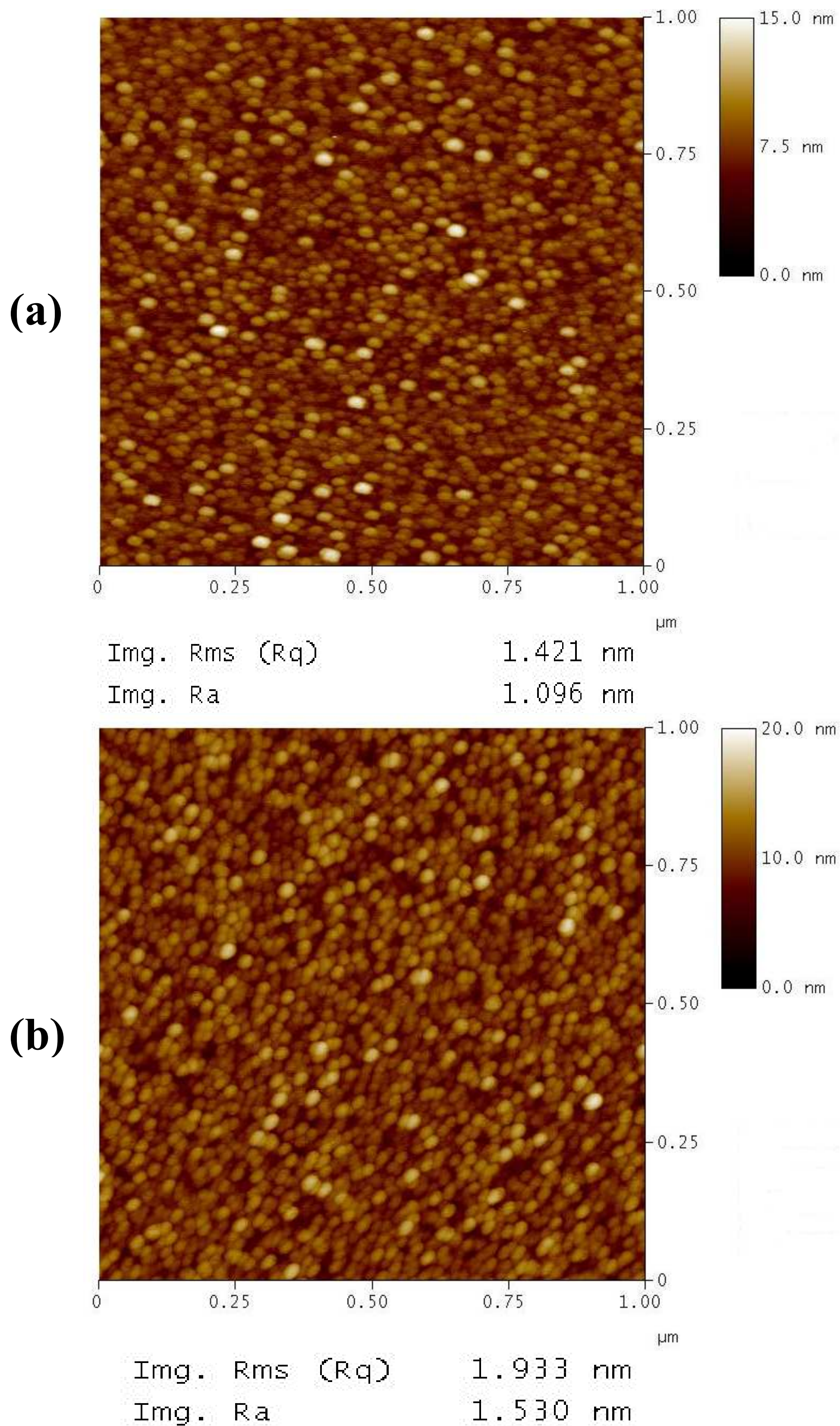


Fig.6.3 The atomic force microscope (AFM) microphotographs of Ge-NCs for (a) 80sec and (b) 120sec GeH_4 deposition time at 370°C.

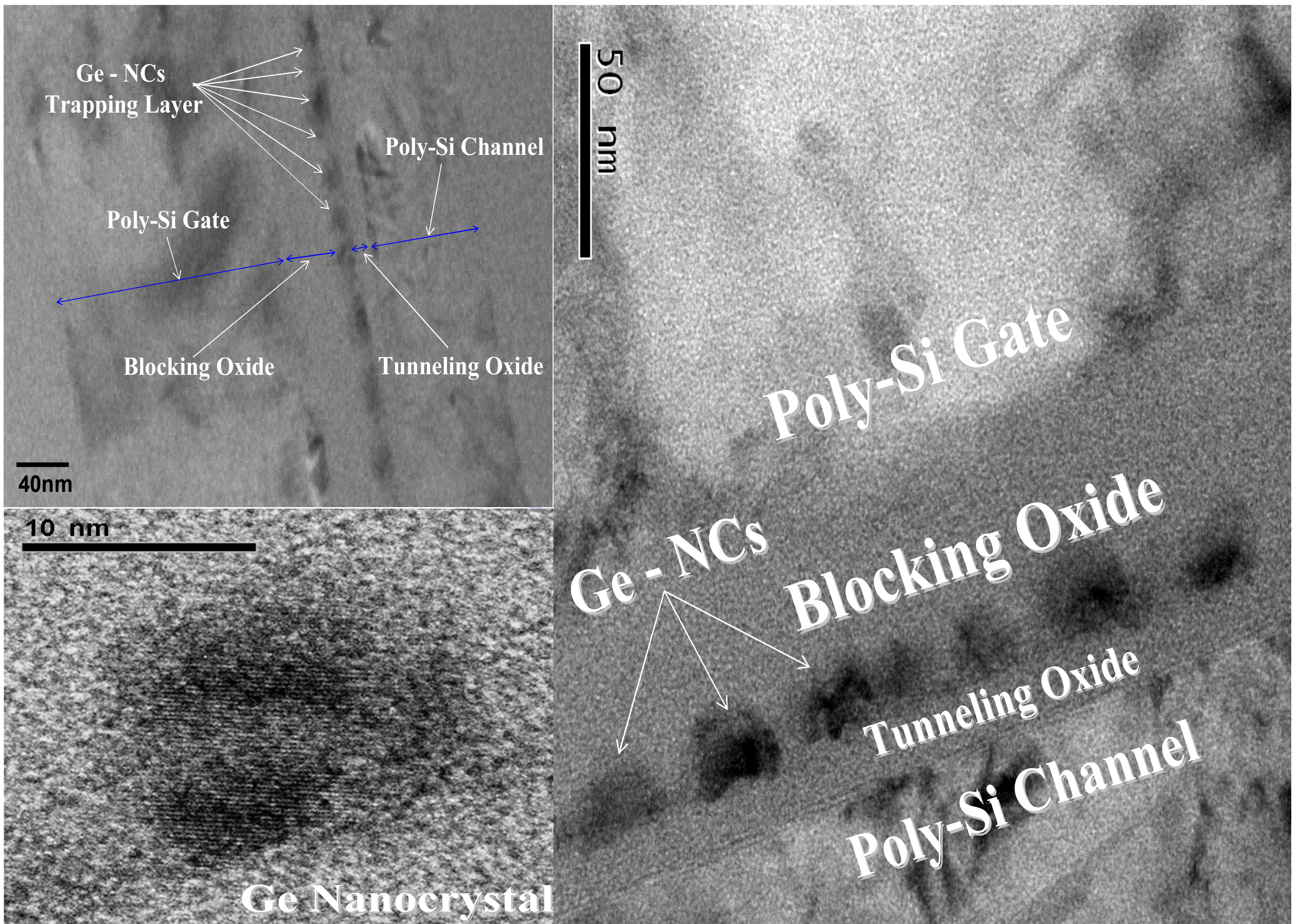


Fig.6.4 The cross section Transmission Electron Microscope (TEM) microphotographs of poly-Si TFT nonvolatile Ge-NCs memories. The blocking oxide and tunneling oxide thickness is about 44nm and 11nm respectively. The pure Ge-NCs embedded in oxide are easy to control the real thickness of tunneling oxide. The sizes of the Ge-NCs are about 9nm~12nm and the density of the Ge-NCs is about $2 \sim 4\times10^{11}cm^{-2}$.

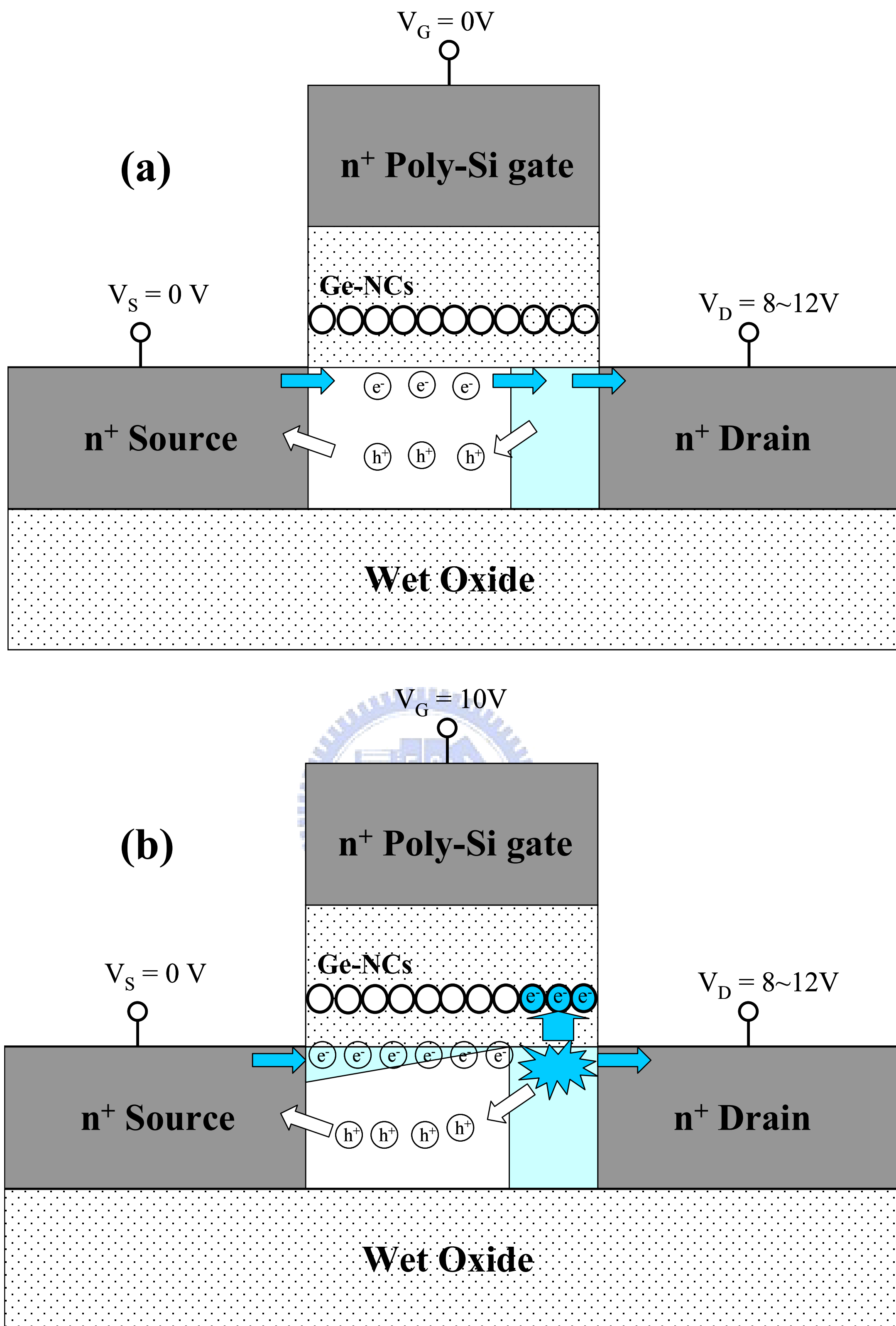


Fig.6.5 The channel hot electron injection program mechanism in poly-Si TFTs with gate length = 1μm ~ 0.8μm. The floating body induced drain avalanche is biased at (a) V_G = 0V, V_D = 8~12V and (b) V_G = 10V, V_D = 8~12V. The additional electron injection is due to the floating body induced drain avalanche with parasitic n-p-n bipolar in the thin film devices.

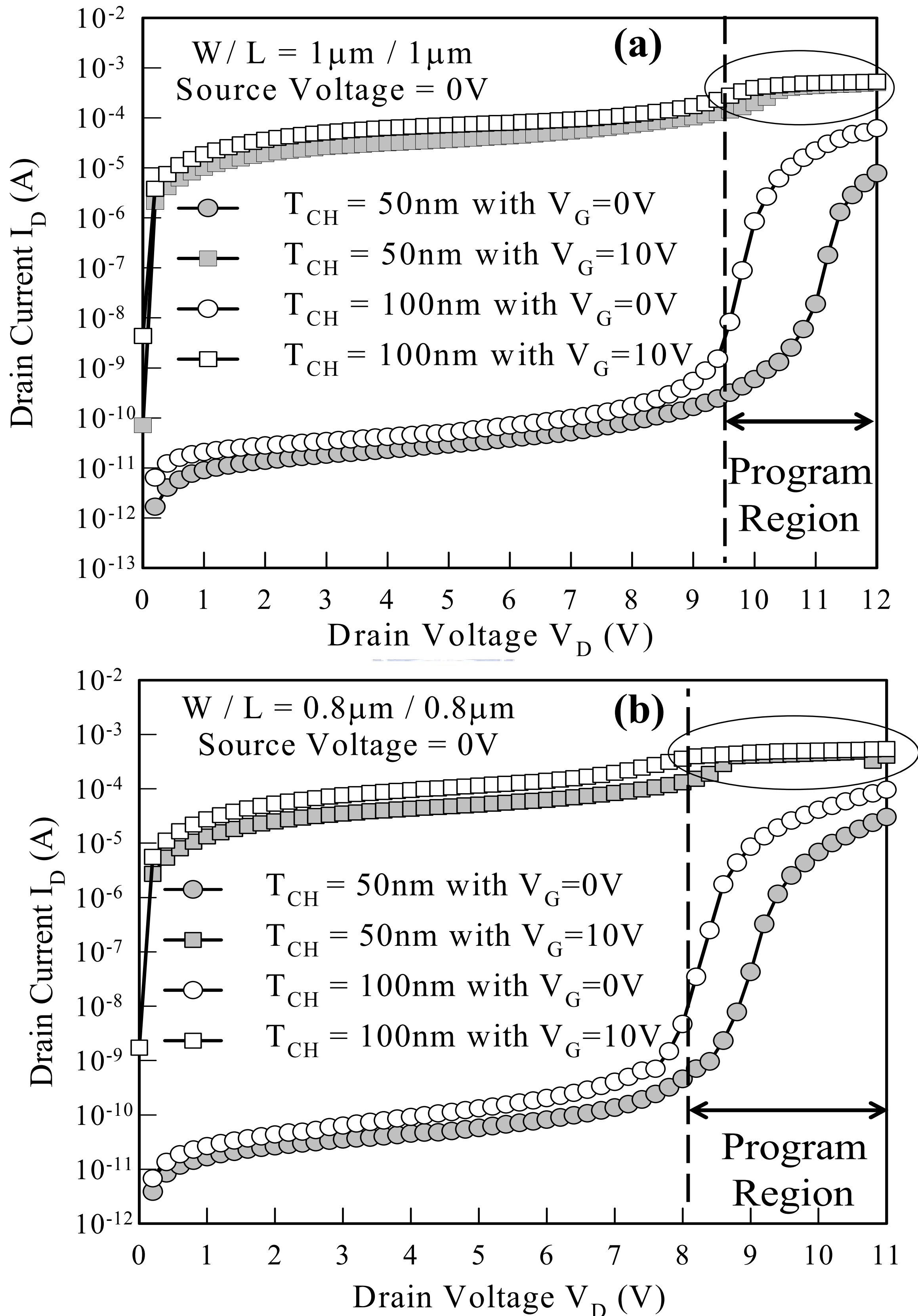
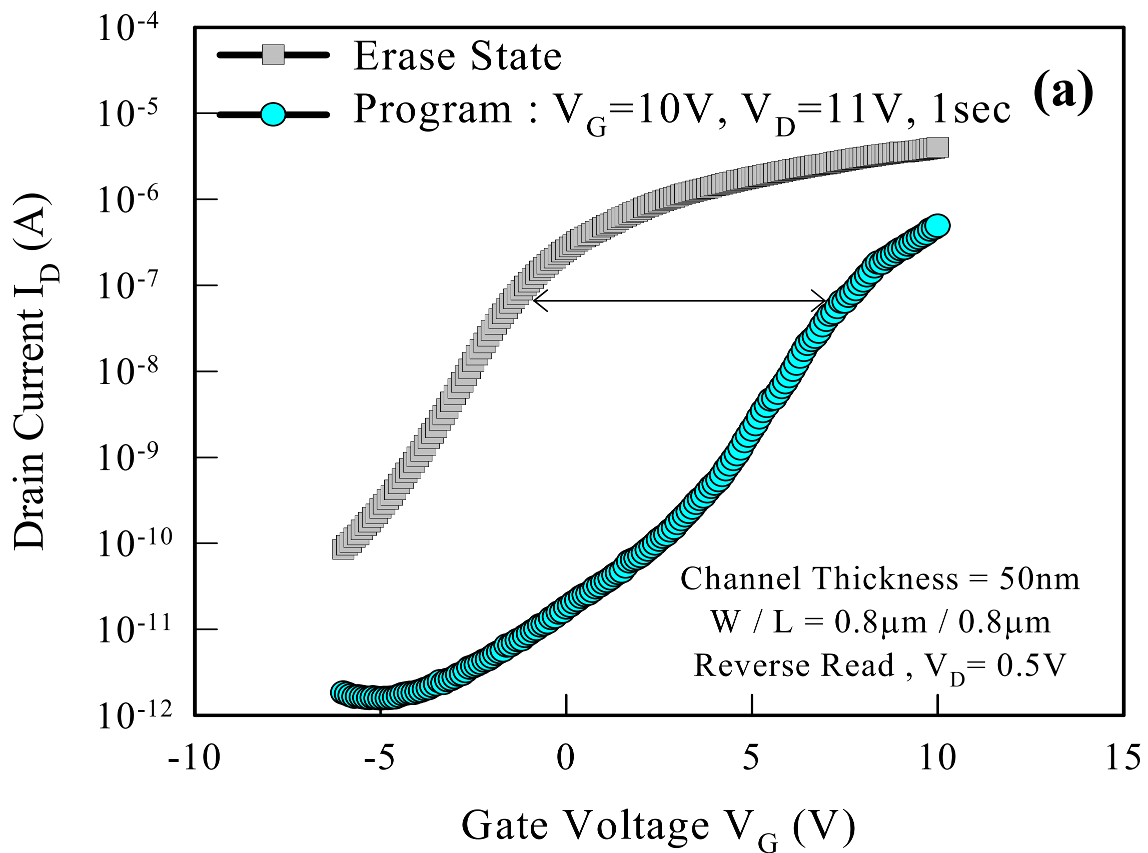


Fig.6.6 The measured floating body induced drain avalanche currents of poly-Si TFTs with different channel thickness and (a) gate length = 1μm (b) gate length = 0.8μm. The thin film devices have high channel hot electron injection efficiency in the program region. The applied drain voltage can be reduced with short gate length and thick channel thickness.

Table 6.1 The split table of the applied drain biases with different gate length and channel thickness in the program region. The applied drain voltage can be reduced with short gate length and thick channel thickness.

Channel Thickness	W / L	$V_D = 9$	$V_D = 10$	$V_D = 11$	$V_D = 12$
50nm	1 μm / 1 μm			★	★
	0.8 μm/0.8 μm		★	★	
100nm	1 μm / 1 μm		★	★	
	0.8 μm/0.8 μm	★	★		



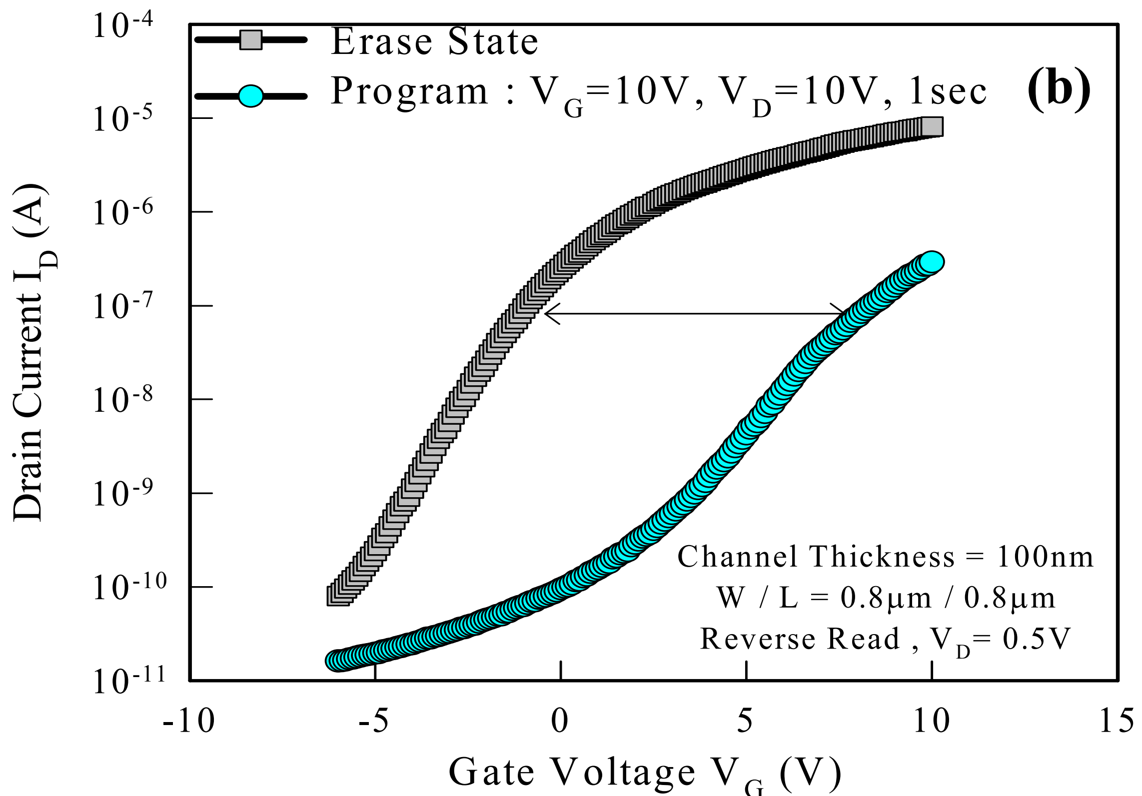
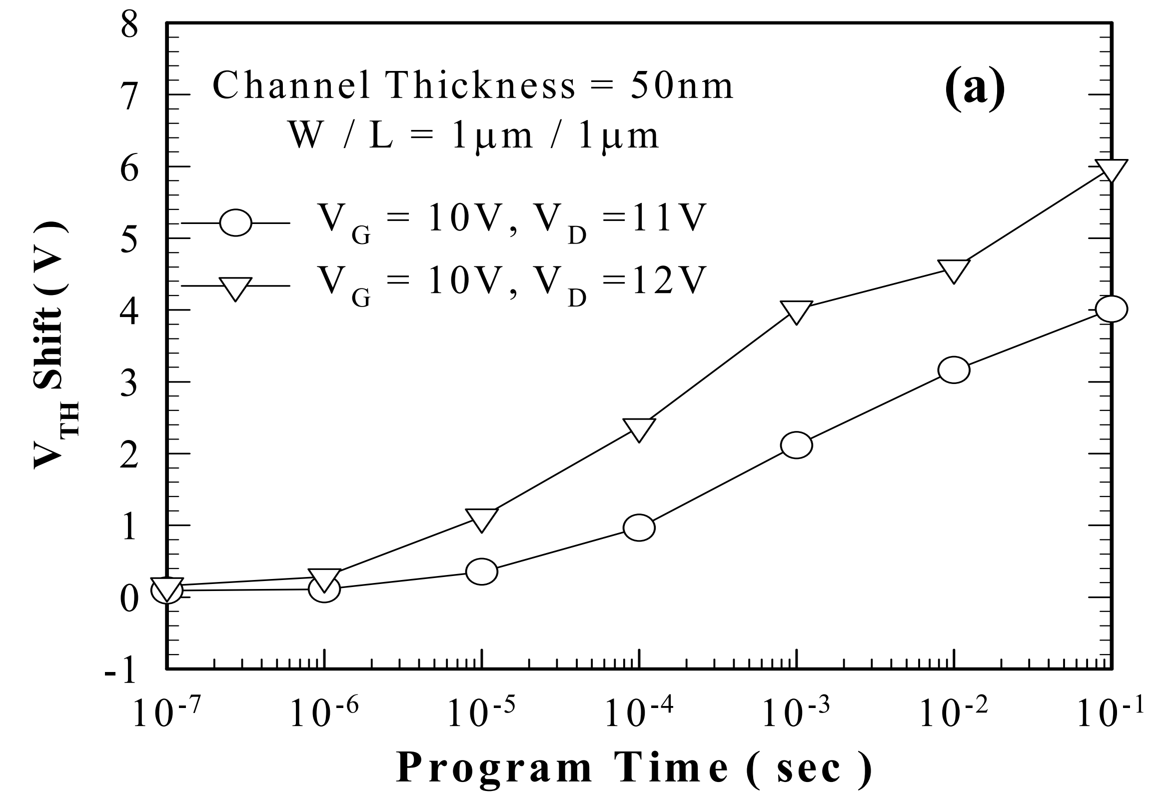


Fig.6.7 The measured transfer characteristics of poly-Si TFT nonvolatile Ge-NCs memories in the P/E states. The memory windows of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm can be larger than 7~8V for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm.



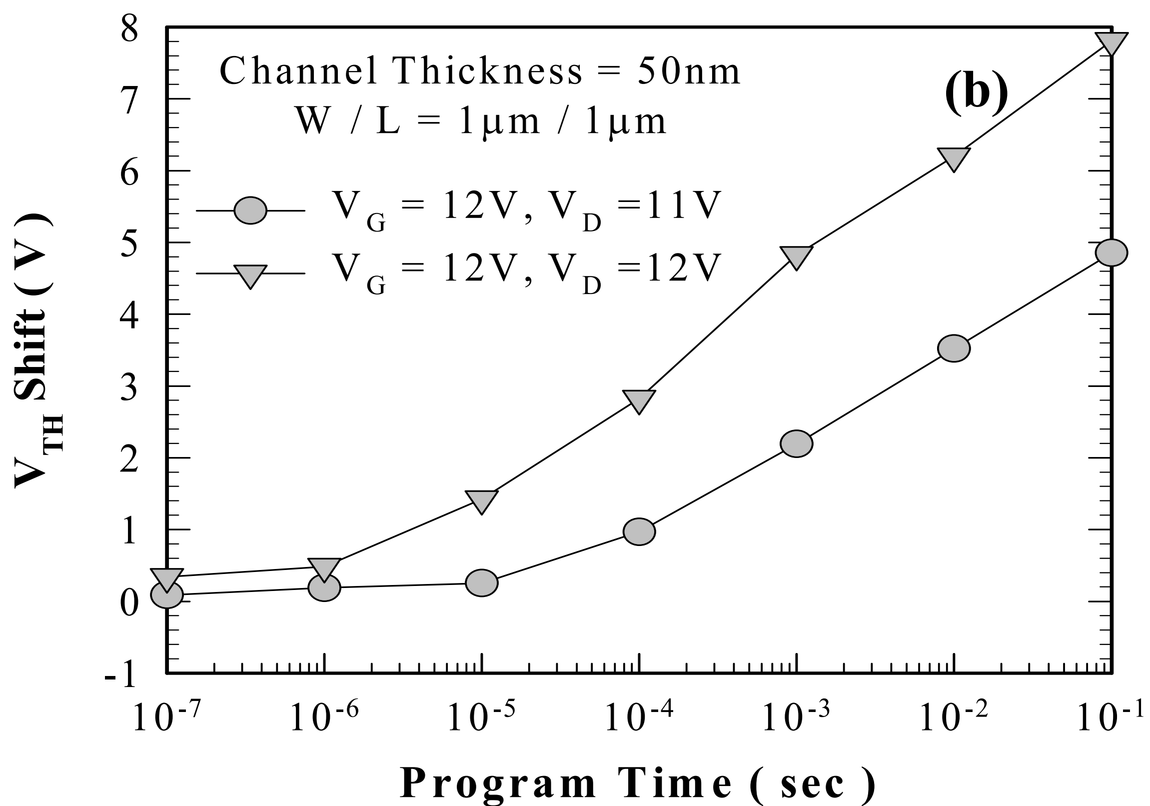
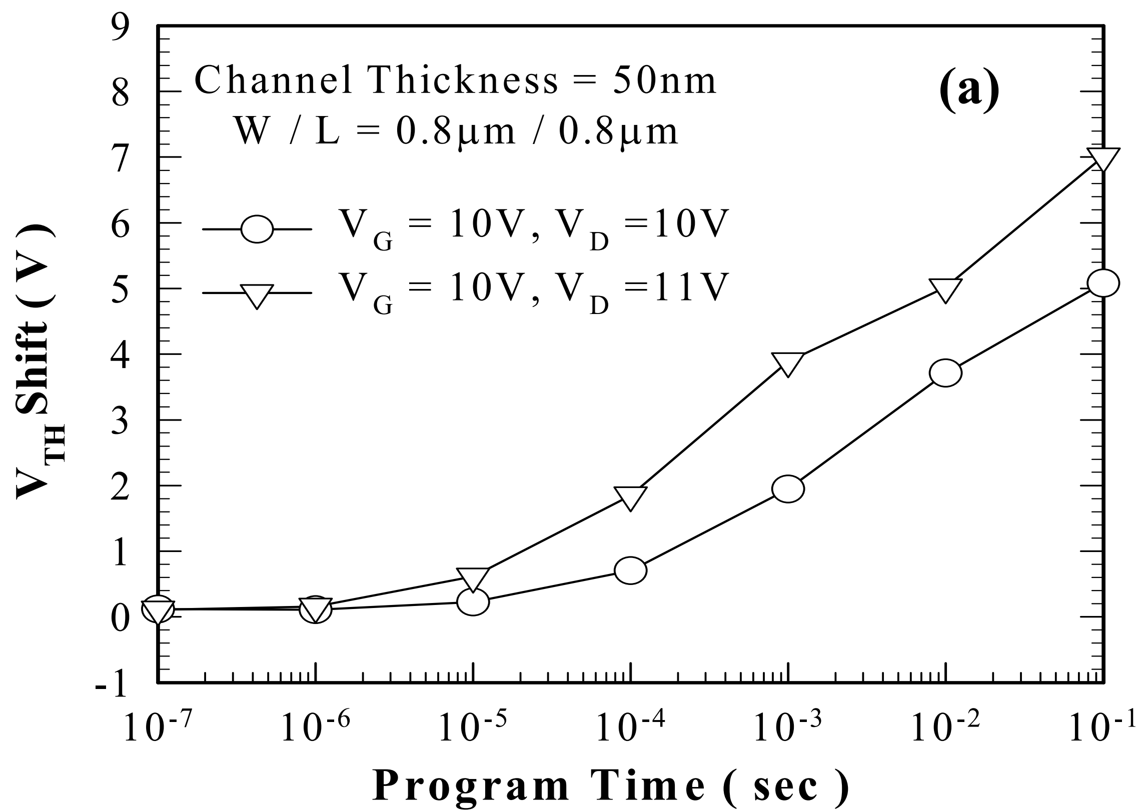


Fig.6.8 The measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 1μm / 1μm in the program region biased at (a)V_G = 10V, V_D = 11V, 12V and (b)V_G = 12V, V_D = 11V,12V.



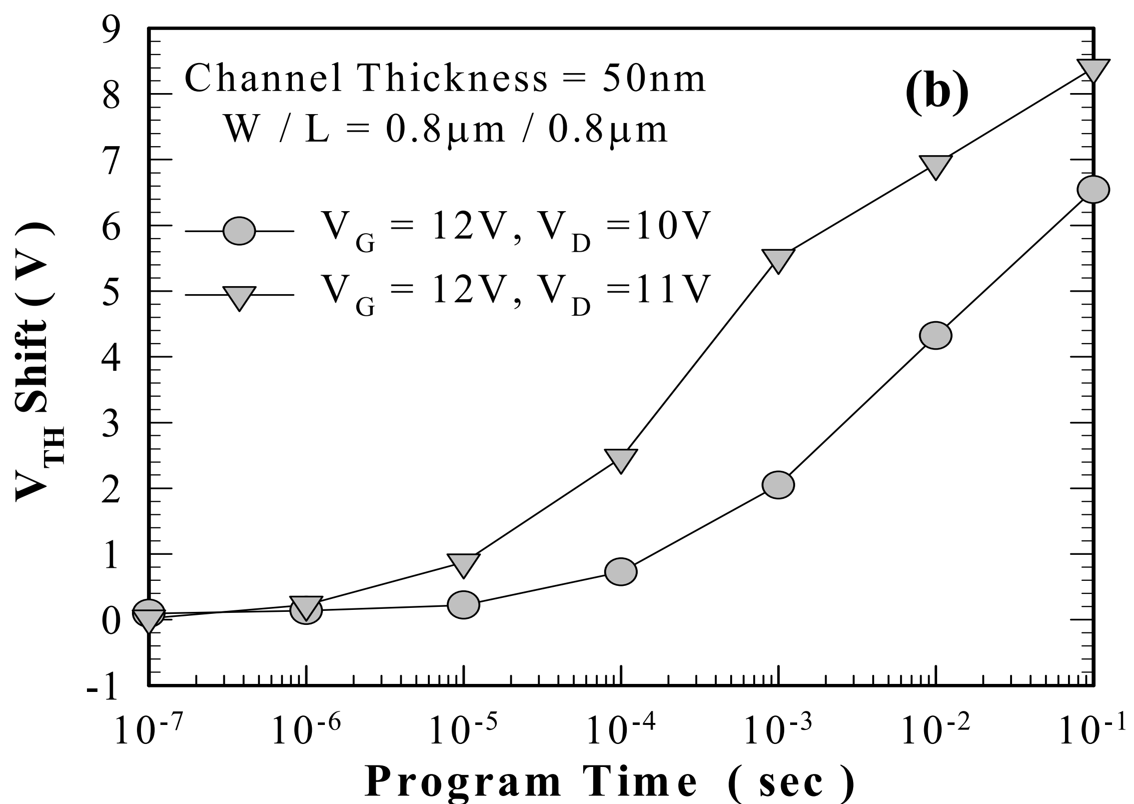
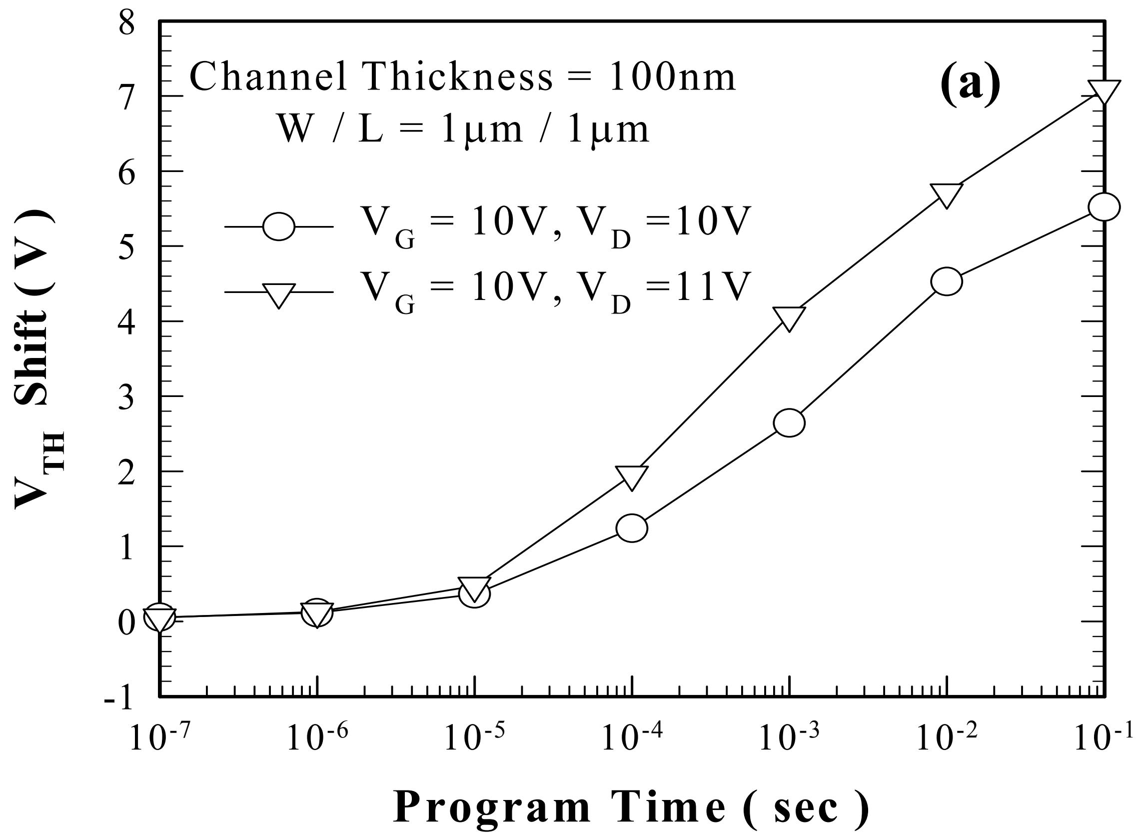


Fig.6.9 The measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm in the program region biased at (a)V_G = 10V, V_D = 10V, 11V and (b)V_G = 12V, V_D = 10V,11V.



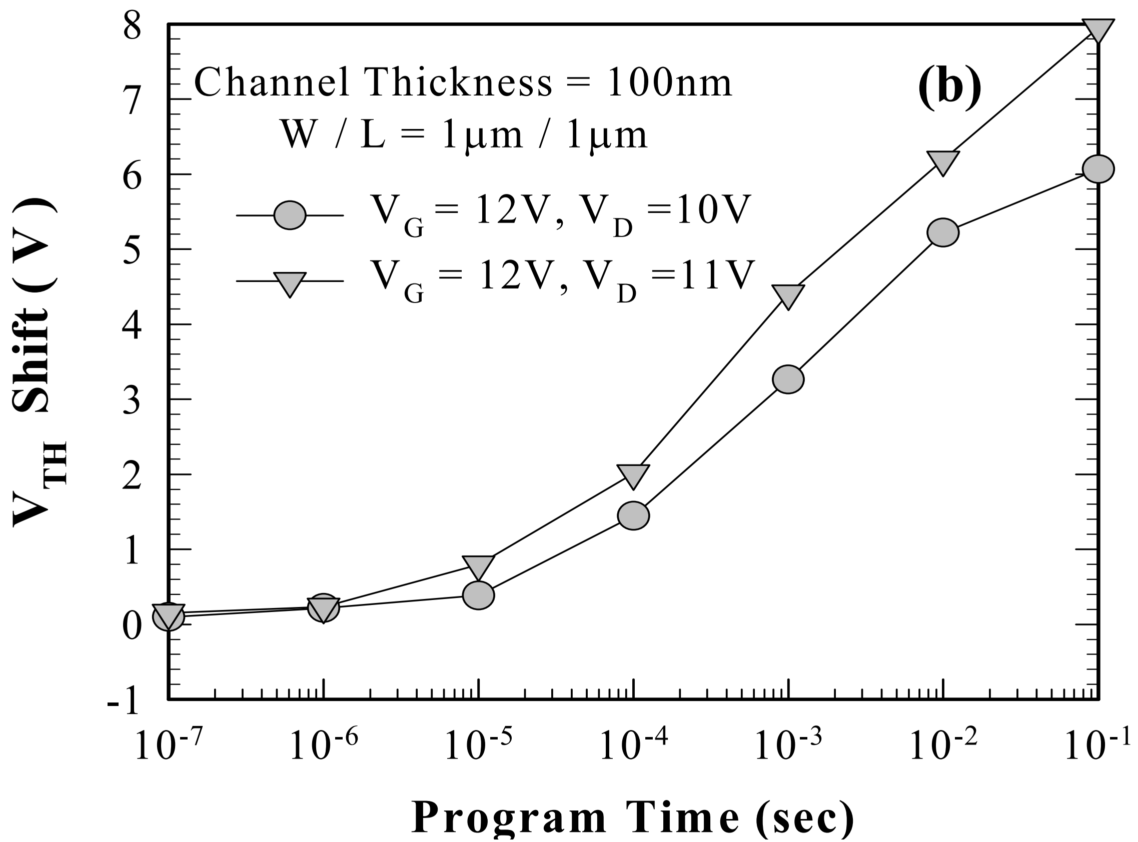
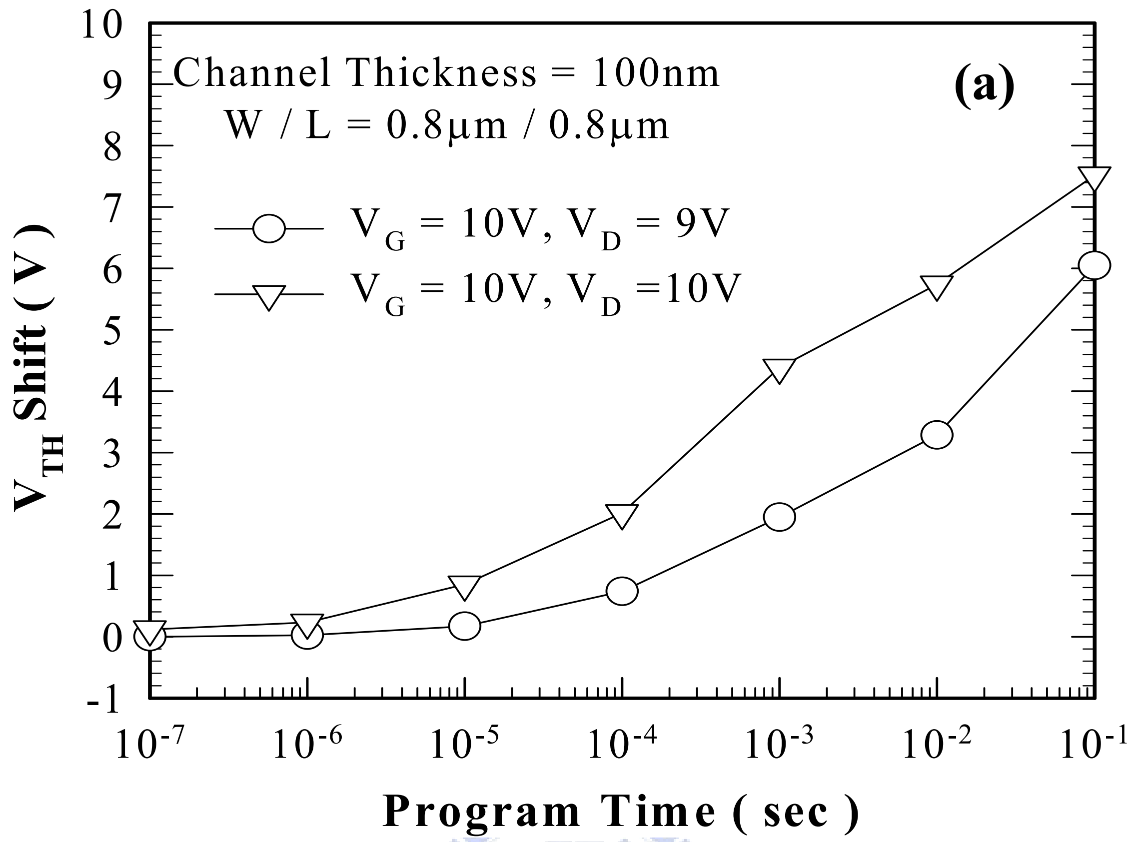


Fig.6.10 The measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 1μm / 1μm in the program region biased at (a)V_G = 10V, V_D = 10V, 11V and (b)V_G = 12V, V_D = 10V,11V.



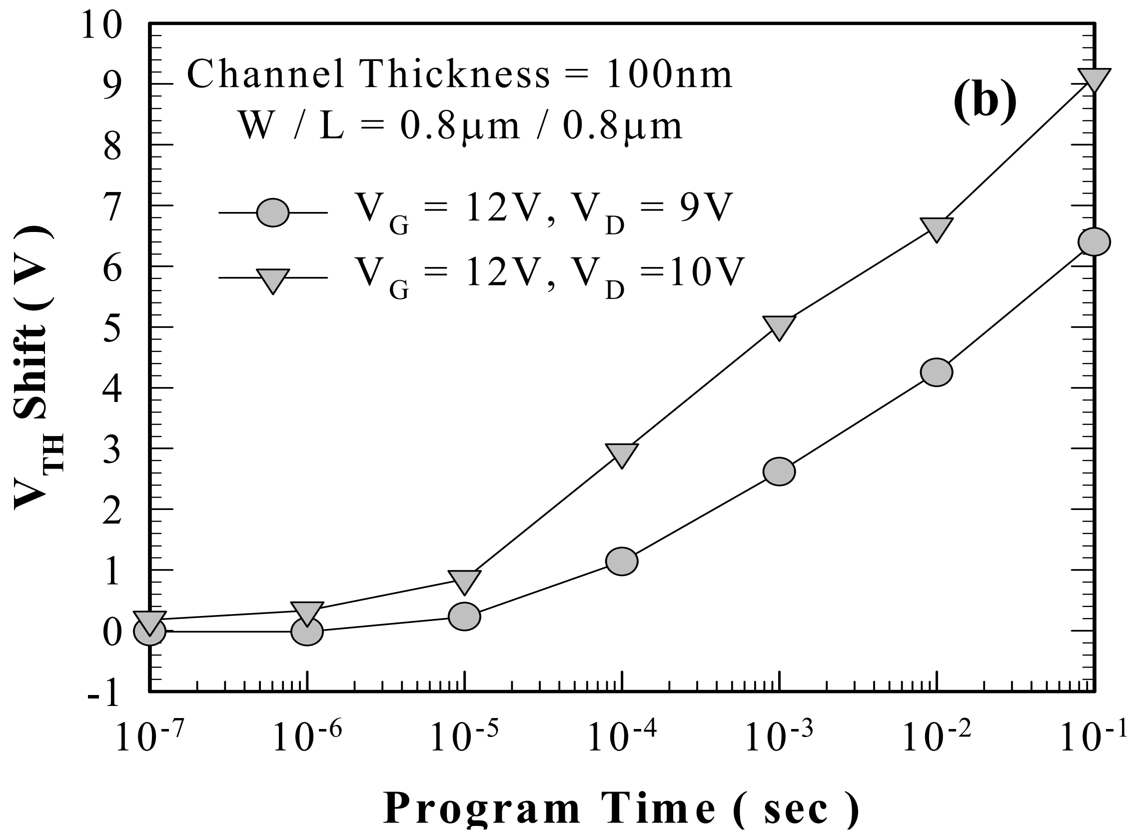
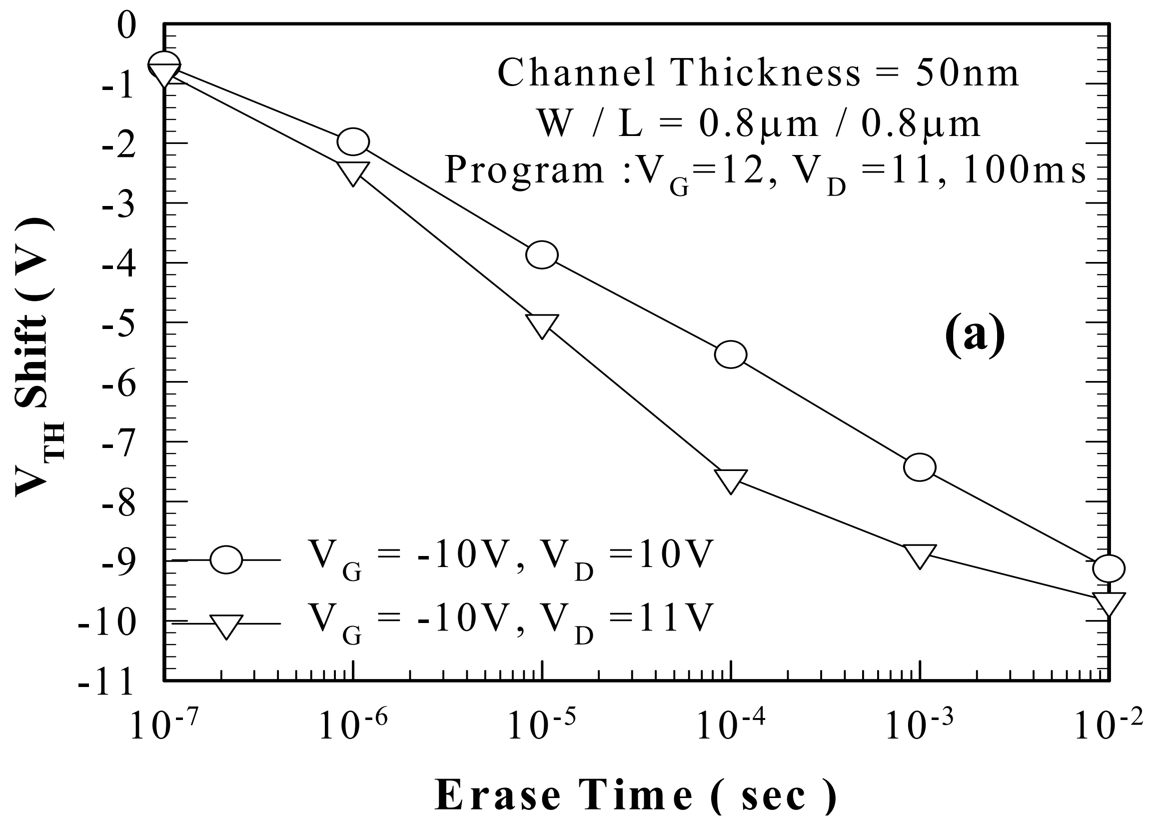


Fig.6.11 The measured programming characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm in the program region biased at (a)V_G = 10V, V_D = 9V, 10V and (b)V_G = 12V, V_D = 9V,10V.

Table 6.2 The program efficiency of poly-Si TFT nonvolatile Ge-NCs memories for different gate length and channel thickness in program region. The program efficiency can be significantly enhanced with increased V_D.

Program V_{TH} shift for 1ms					
Channel Thickness	W / L	$V_G = 10$			
		$V_D = 9$	$V_D = 10$	$V_D = 11$	$V_D = 12$
50nm	1 μm / 1 μm			2.11V	4.01V
	0. 8 μm / 0. 8 μm		1.94V	3.89V	
100nm	1 μm / 1 μm		2.63V	4.07V	
	0. 8 μm / 0. 8 μm	1.94V	4.38V		



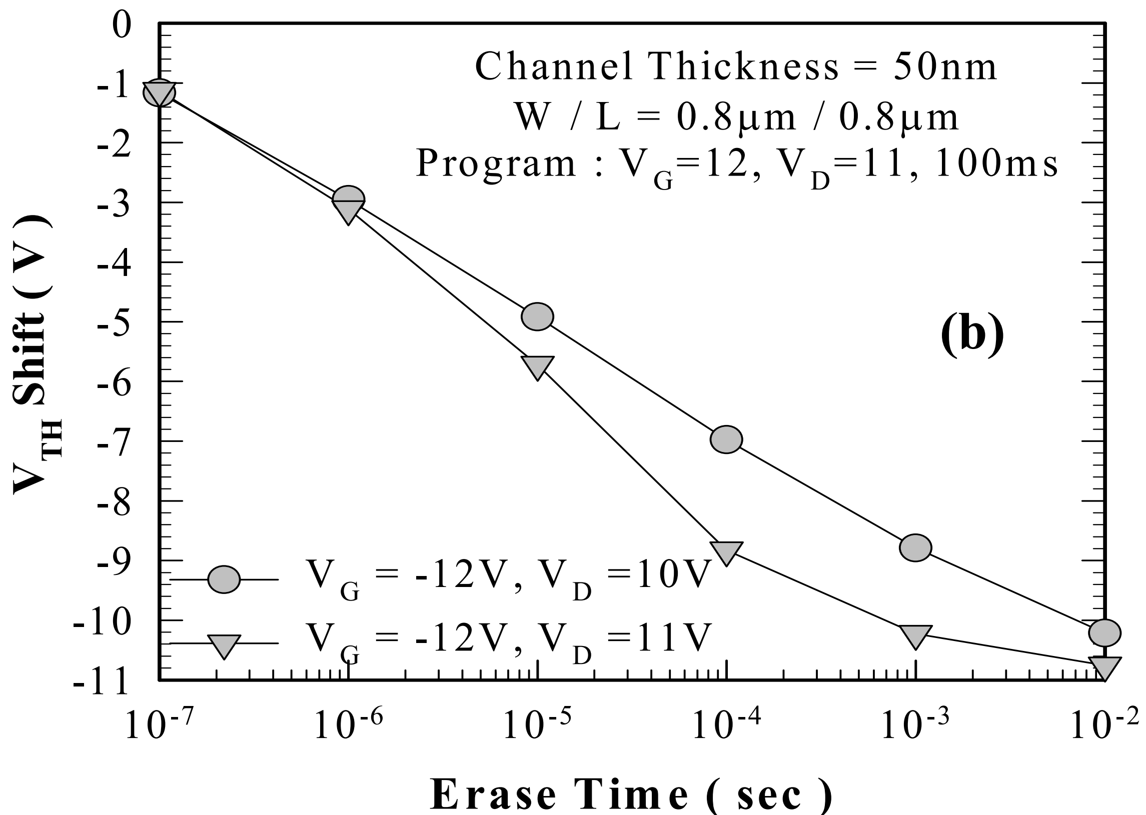
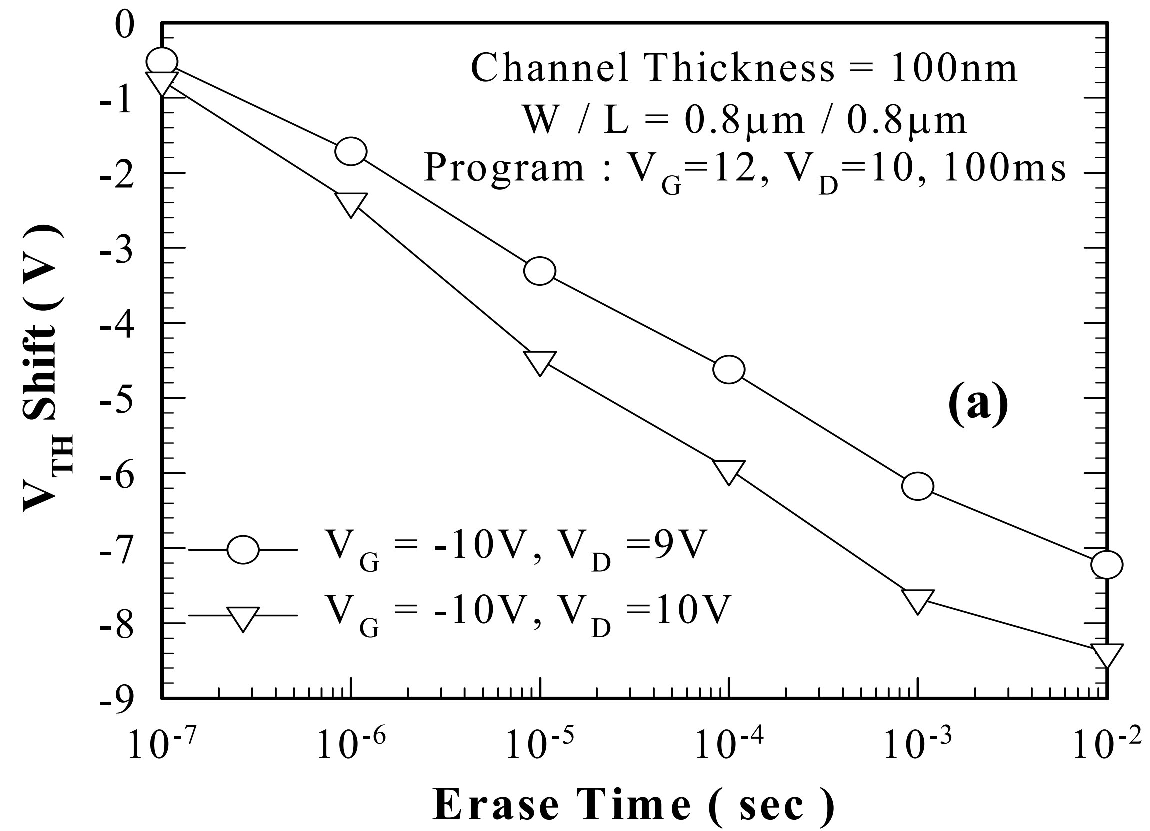


Fig.6.12 The measured erasing characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm in the erase region biased at (a)V_G = -10V, V_D = 10V, 11V and (b)V_G = -12V, V_D = 10V,11V. The high erasing efficiency is due to floating body effect induced drain avalanche.



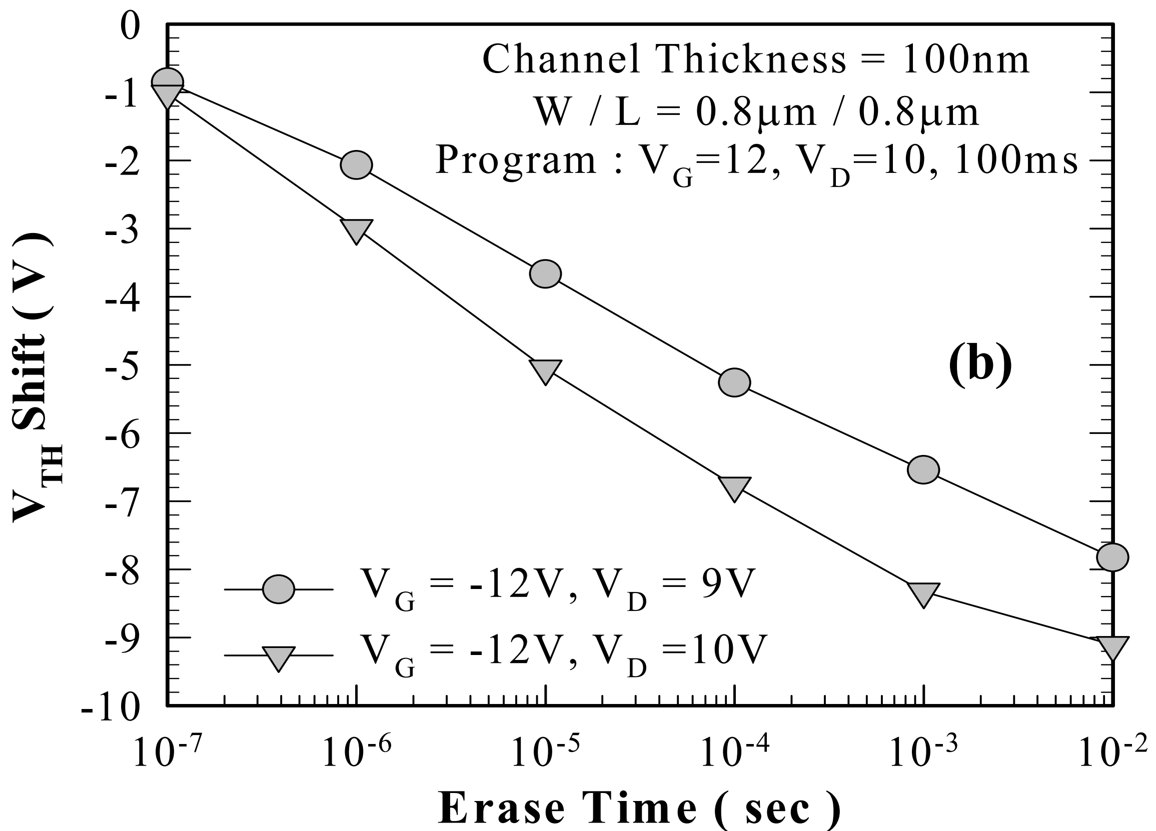
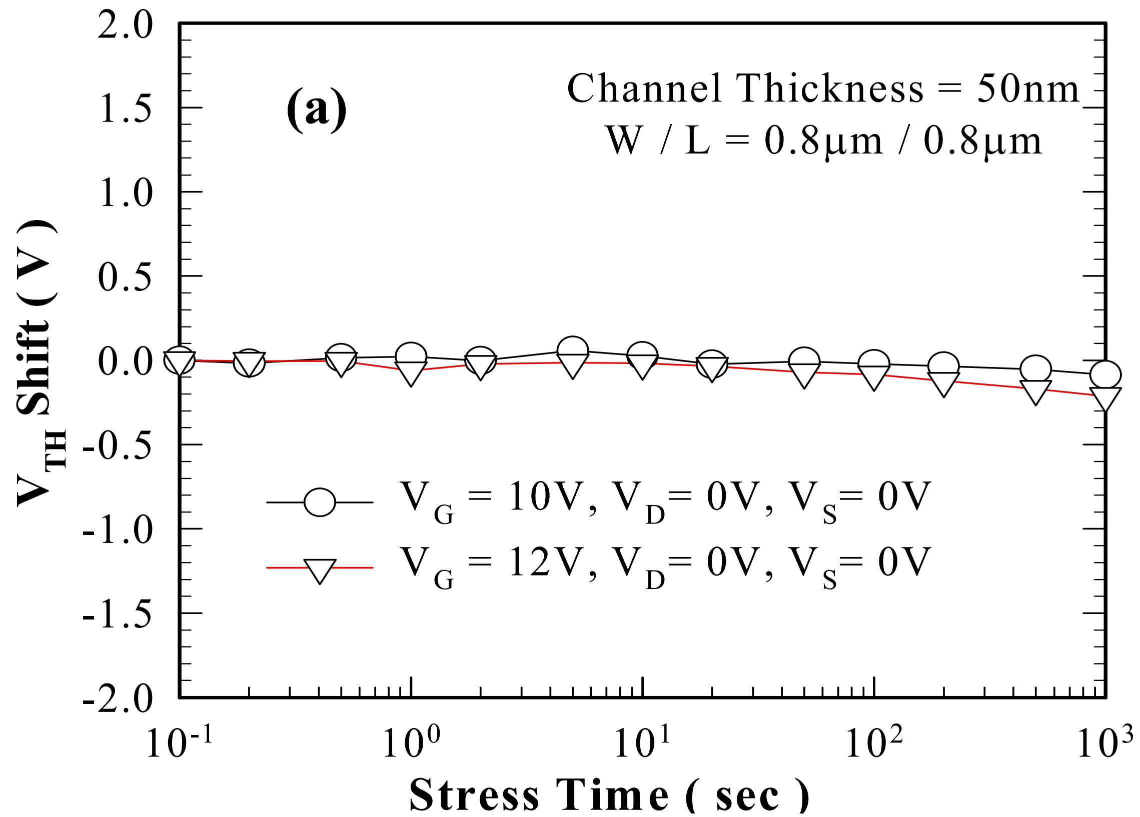


Fig.6.13 The measured erasing characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm in the erase region biased at (a)V_G = -10V, V_D = 9V, 10V and (b)V_G = -12V, V_D = 9V,10V. The high erasing efficiency is due to floating body effect induced drain avalanche.



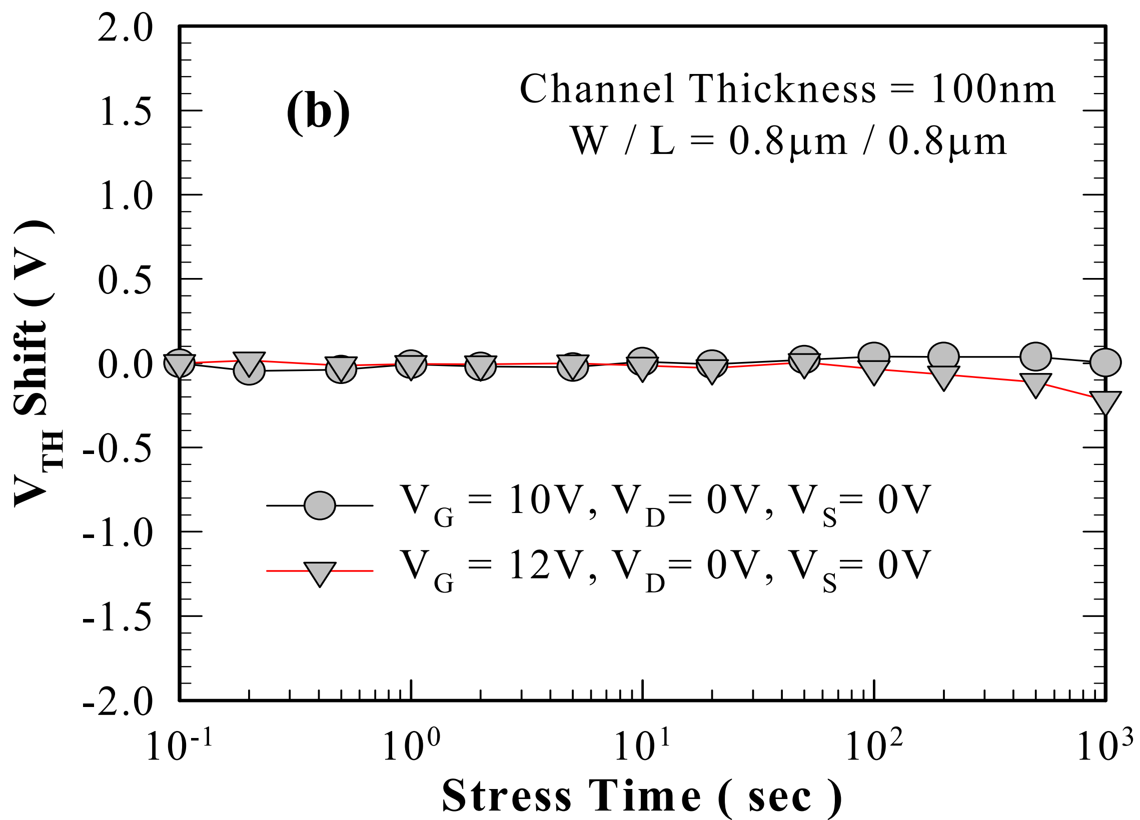
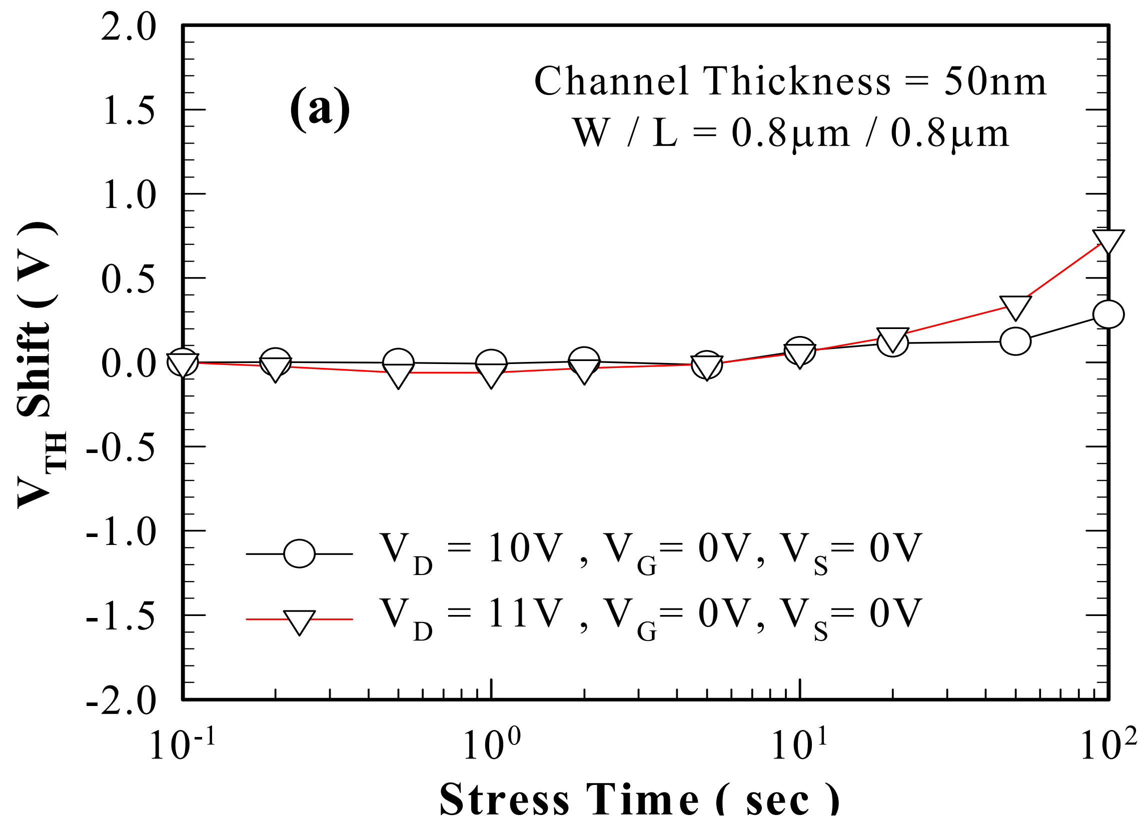


Fig.6.14 The measured gate disturbance characteristics of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm in the erased state.



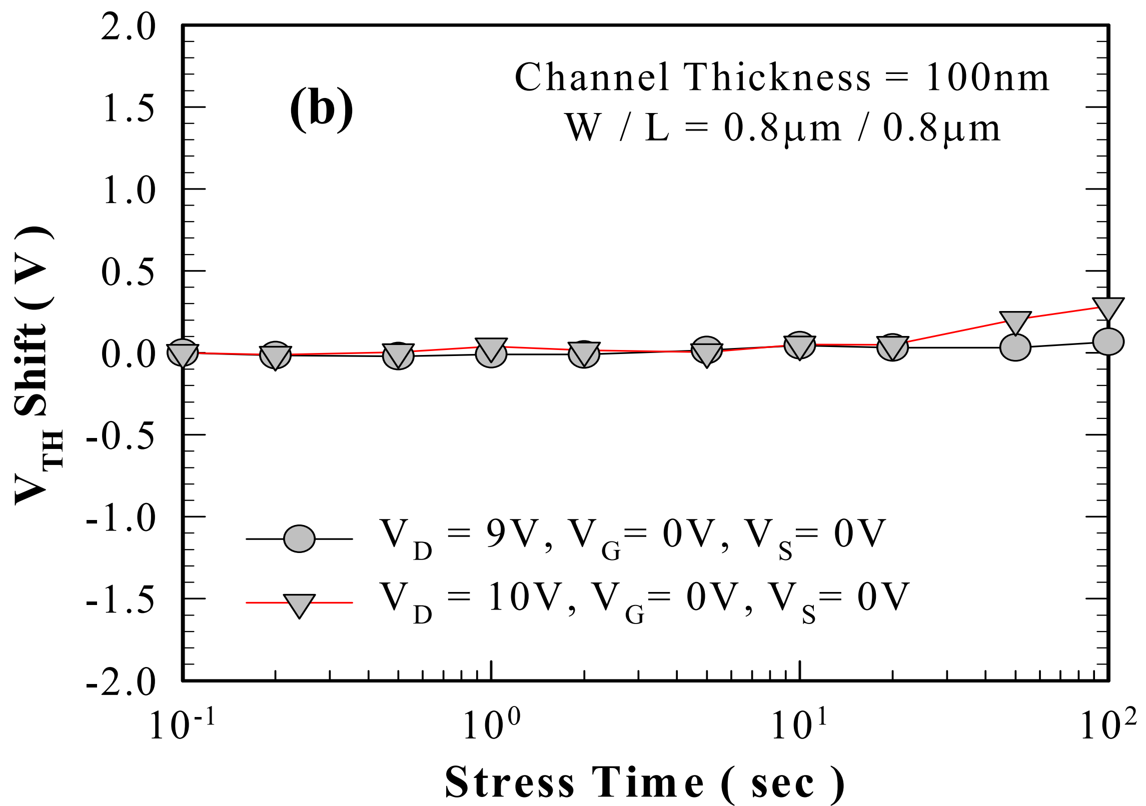
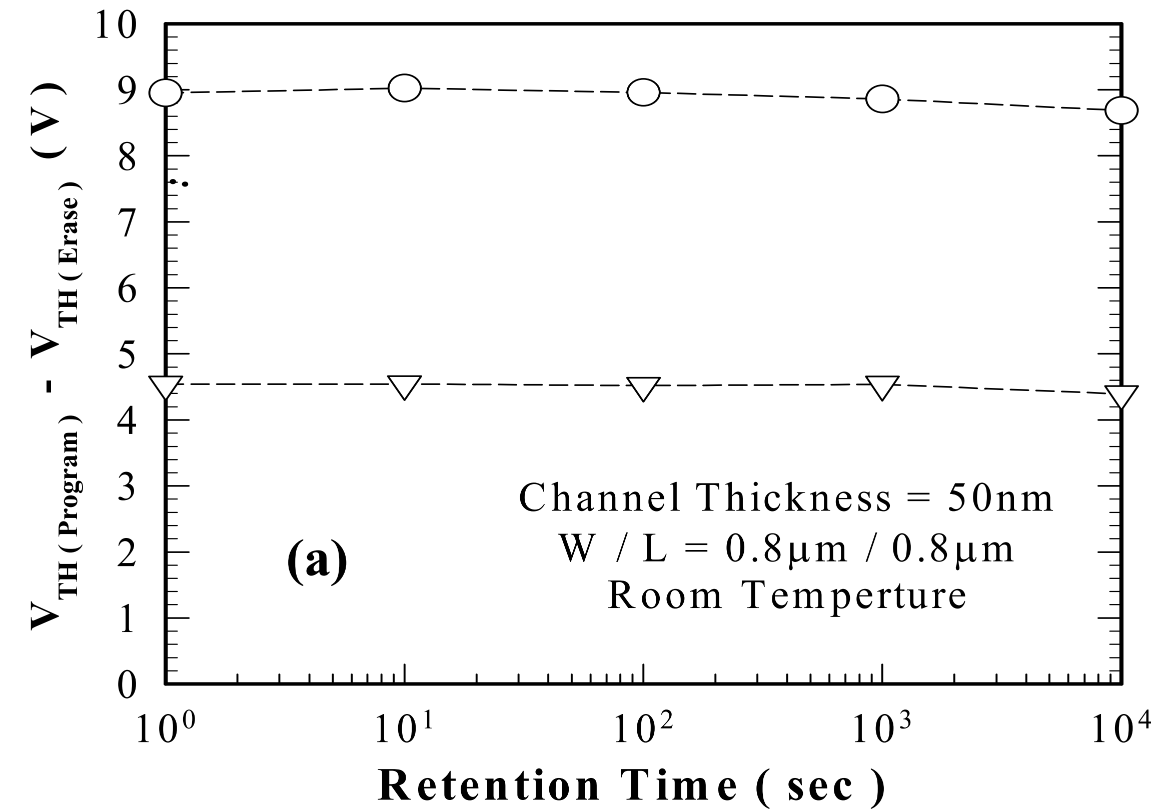


Fig.6.15 The measured drain disturbance characteristics of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm.



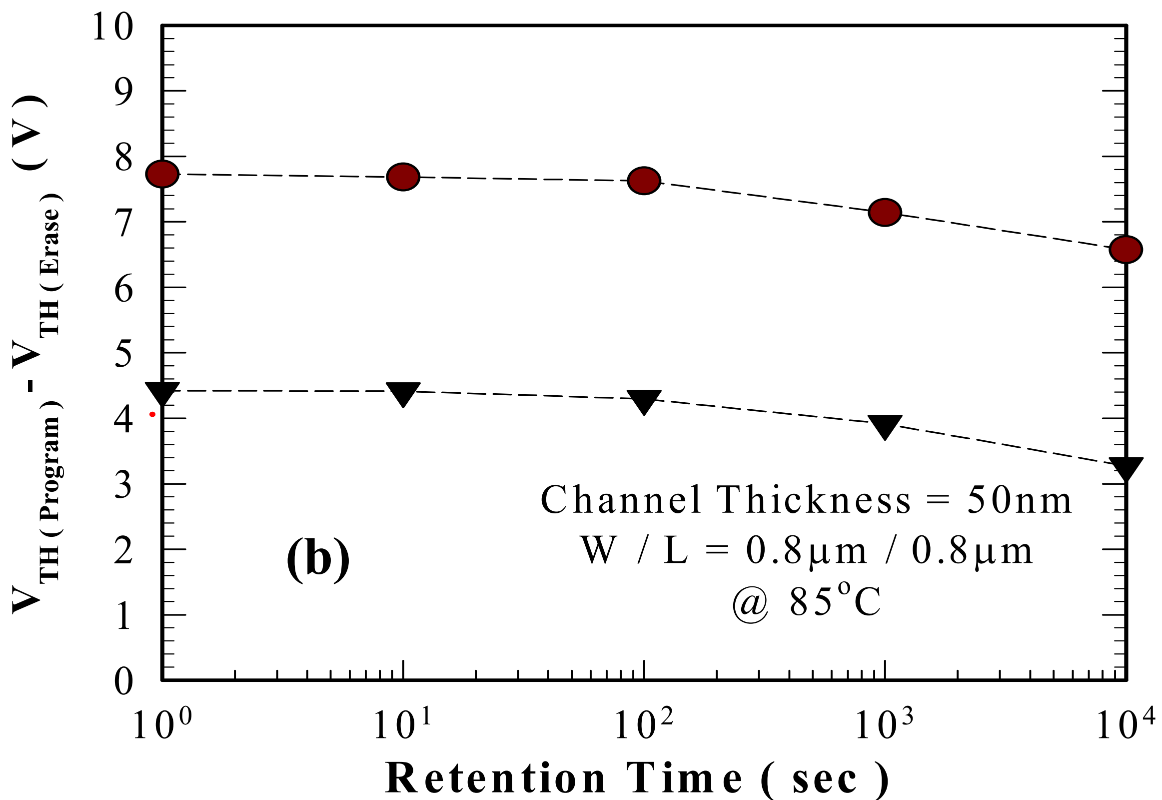
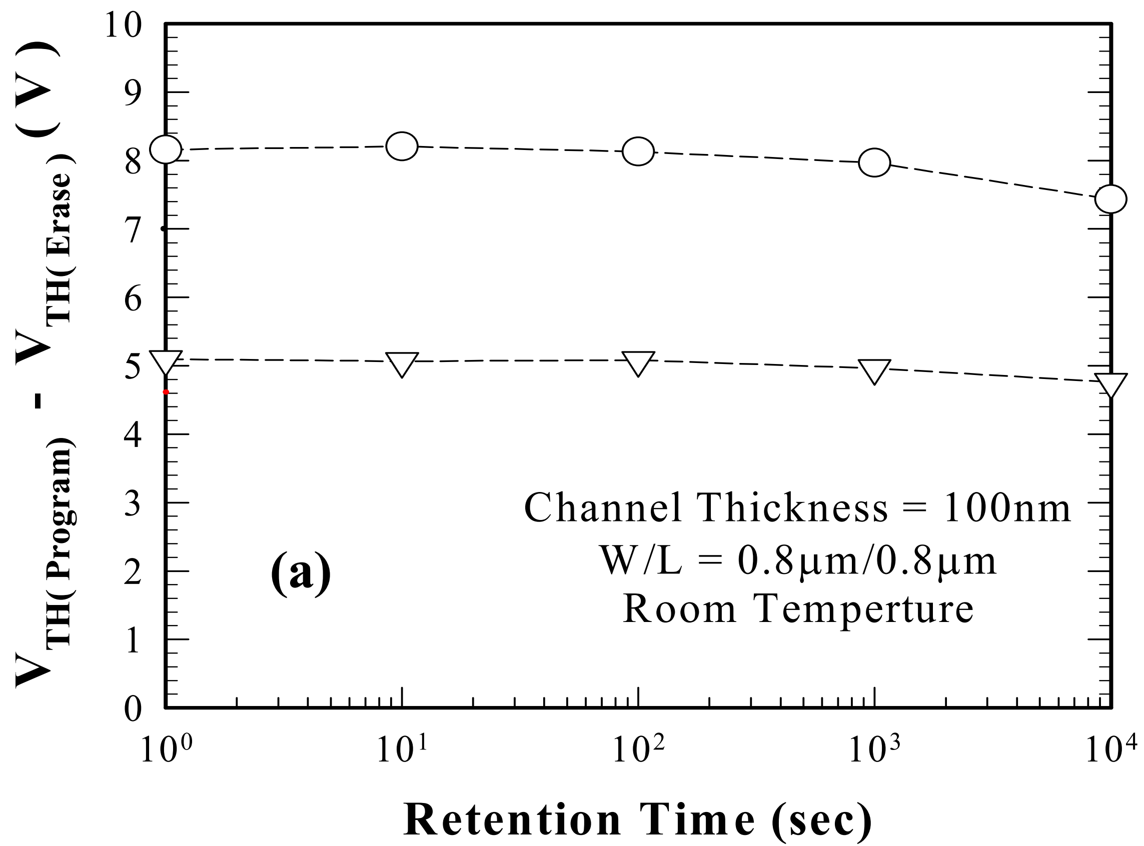


Fig.6.16 The measured retention characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 50-nm and W / L = 0.8μm / 0.8μm at (a) room temperature and (b) 85°C. The poly-Si TFT nonvolatile Ge-NCs memories with two-level threshold voltage states have good retention characteristics at 85 °C due to the deep trapping level of Ge-NCs.



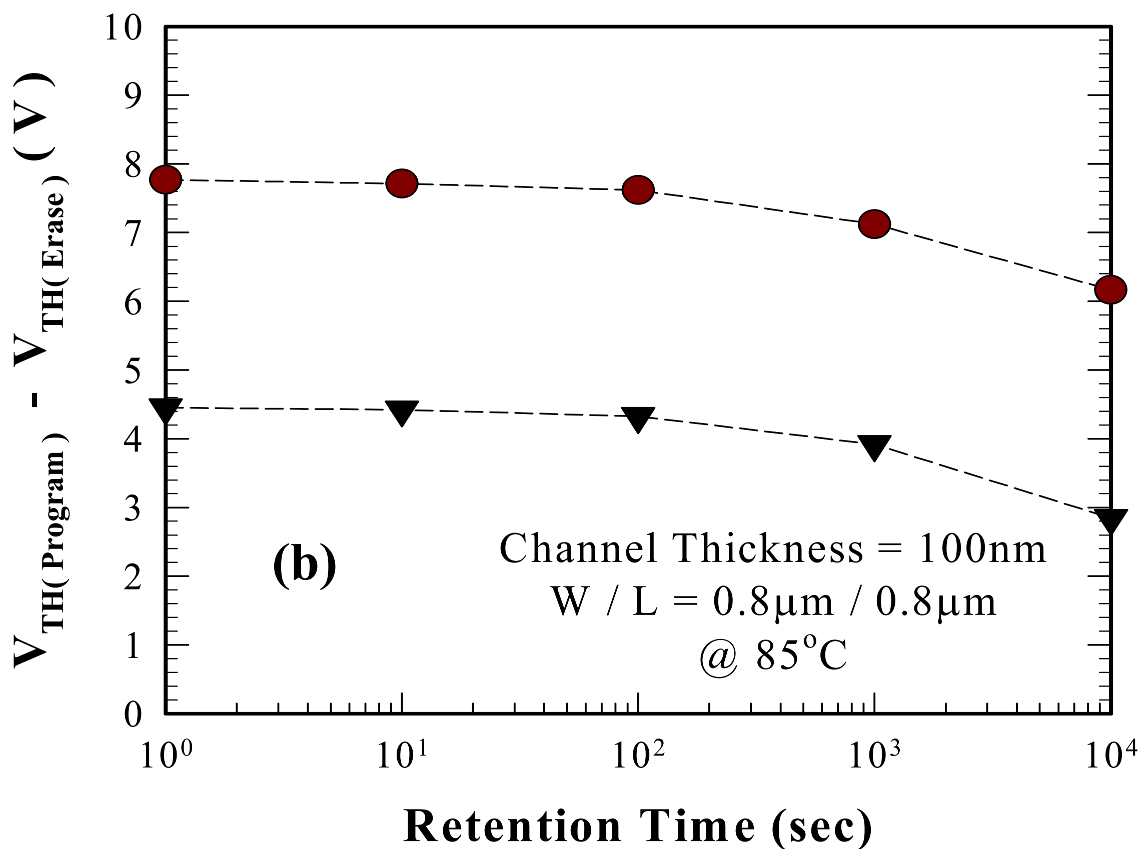
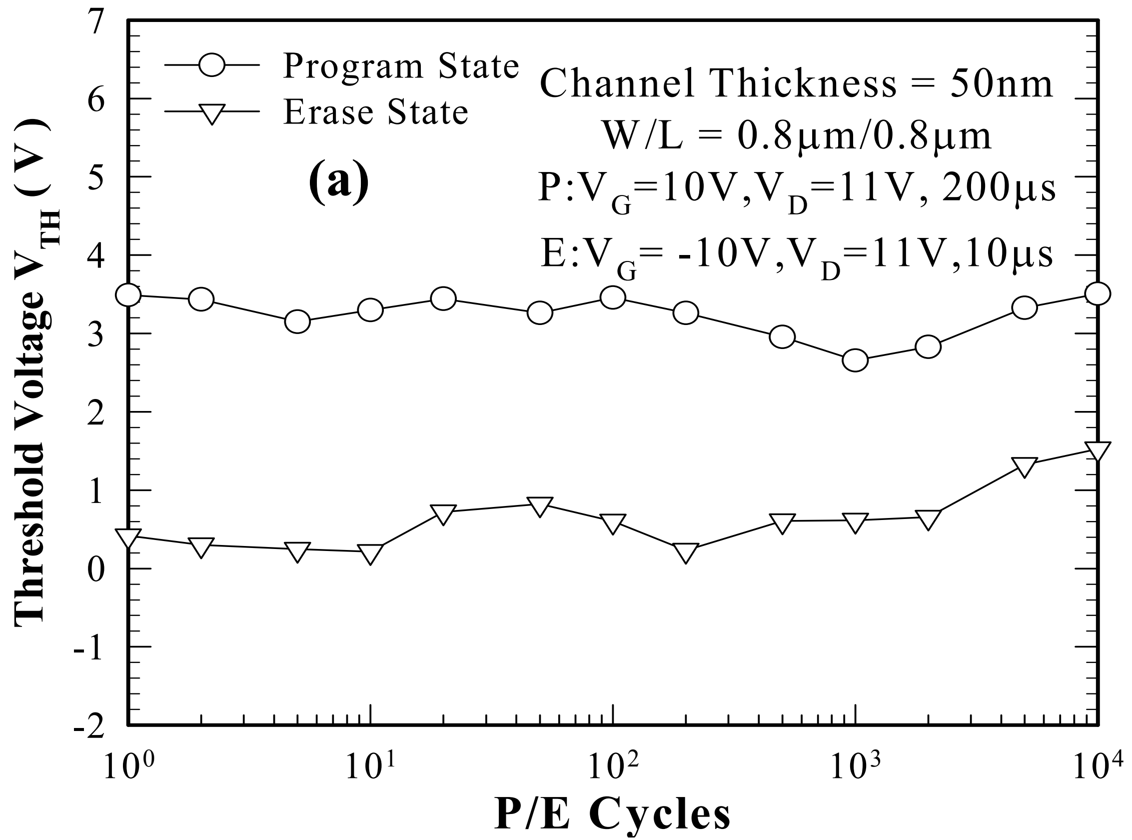


Fig.6.17 The measured retention characteristics of poly-Si TFT nonvolatile Ge-NCs memories with channel thickness = 100-nm and W / L = 0.8μm / 0.8μm at (a) room temperature and (b) 85°C. The poly-Si TFT nonvolatile Ge-NCs memories with two-level threshold voltage states have good retention characteristics at 85 °C due to the deep trapping level of Ge-NCs.



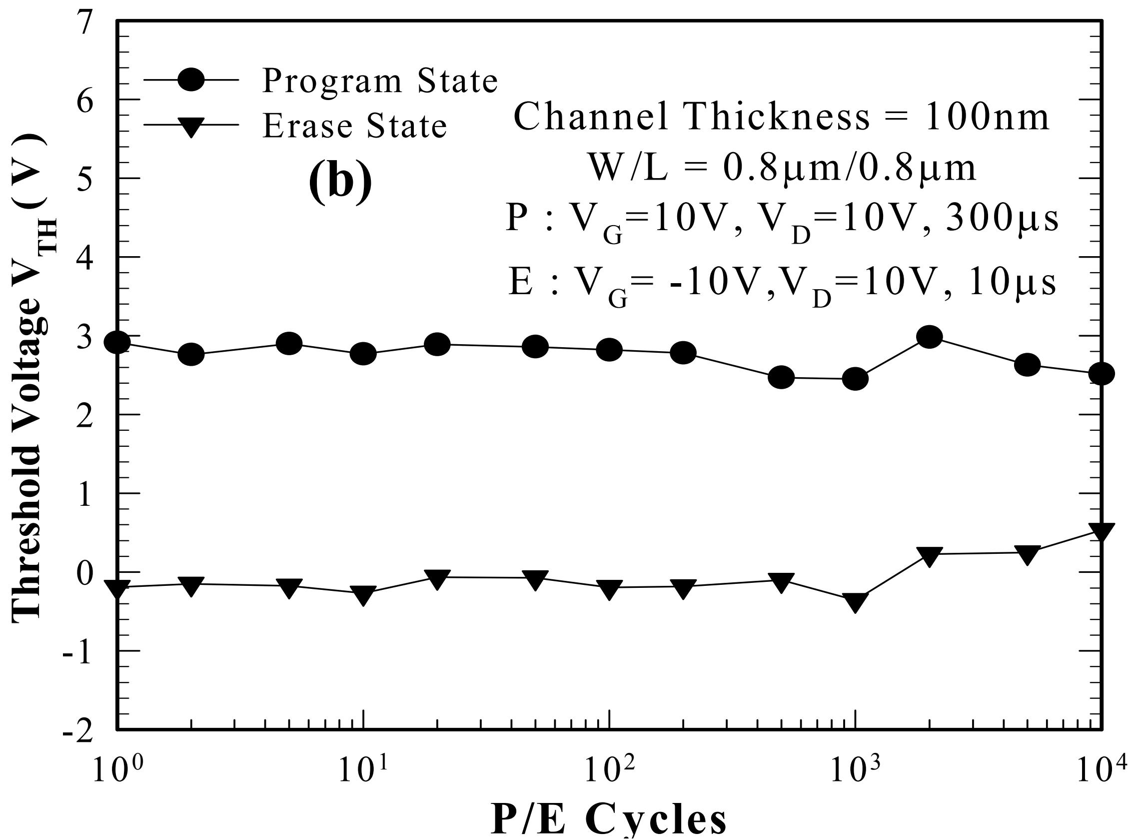


Fig.6.18 The measured endurance characteristics of poly-Si TFT nonvolatile Ge-NCs memories with W / L = 0.8μm / 0.8μm for (a) channel thickness = 50-nm and (b) channel thickness = 100-nm. The memory windows narrow to about 2V after 10^4 P/E cycles.

Chapter 7

Conclusions and Further Recommendations

7.1 Conclusions

In this thesis, various application of Ni-silicidation and Germanium techniques for fabricating high performance new structures of polycrystalline silicon thin-film transistors (poly-Si TFTs) have been demonstrated and investigated.

In Chapter 2, we have developed a self-aligned SSOB structure for poly-Si TFTs to provide an effective body contact and suppress the floating-body effect. The GIDL-like currents occurred in the Schottky drain TFTs are reduced by the SSOB-TFTs. This SSOB-TFTs show reduced kink effect and increased breakdown voltage and are suitable for driving circuit application for high voltage gain.

In Chapter 3, the n-channel FSA-TFTs show reduced kink effect, increased drain breakdown voltage, stable V_{TH} roll-off, improved S.S., low parasitic S/D resistance, high field-effect mobility and increased on /off current ratio. The p-channel FSA-TFTs were also fabricated with improved devices performance. The parasitic resistance of S/D and gate is greatly reduced and allows it possible to recover the intrinsic characteristics of thin-channel TFTs. The FSA-TFTs with low thermal budget fully Ni-salicidation processes are proved to be a very promising structure with low parasitic S/D resistance and high gate capacitance ability for 3D integration applications and high-performance driver circuits in the AMLCDs.

In Chapter 4, the NSILC-VTFTs have the symmetric S/D structure without additional MILC window mask. NSILC process can reduce metal contaminations and

improve poly-Si TFTs characteristics. One step NSILC (500 ^oC, 12hr) is controlled to study the effects of grain boundaries on the vertical channel and n^+ floating region. The NSILC-VTFTs with small W_{mask} and L_{mask} have improved device characteristics due to less poly-Si grain boundaries. Two step NSILC (1_{th} step: 500°C, 12hr and 2_{th} step: RTA 700°C, 60-sec.) has been introduced to enhance the grain size and improve the crystal integrity through secondary recrystallization. Significant improvements in TFT performance have been observed even for large devices with multiple grains in the channel. The novel NSILC-VTFTs without NH_3 plasma treatment have good S.S. characteristics, low off-state leakage current and high field-effective mobility.

In Chapter 5, the stacked Si / Ge gate layers were successfully deposited by LPCVD. The thick gate oxide layer at the gate edges and passivation oxide layer were deposited simultaneously in passivation process. The thick gate oxide at the gate edges effectively reduces the vertical and lateral electric fields near the drain without additional mask, LDD, spacer, or sub-gate bias. The Si / Ge T-gate poly-Si TFTs are proved to be a very promising structure with low OFF-state leakage current, improved ON / OFF current ratio, and saturated output characteristics for display system-on-panel applications.

In Chapter 6, Ge-NCs were grown using a two-step process. In step 1, the Si nuclei are formed on the SiO_2 surface. Then, in step 2, the Ge-NCs grow selectively on the Si nuclei. The sizes of the Ge-NCs are about 9nm~12nm and the density of the Ge-NCs is about $2 \sim 4\times10^{11}cm^{-2}$. The pure Ge-NCs embedded in oxide were easy to control the real thickness of tunneling oxide. In addition, we find that drain voltage is the key point of P/E efficiency in thin film nonvolatile memory devices. The operating drain voltage changes with different gate length and different channel thickness. Experimental results show that the poly-Si TFT nonvolatile Ge-NCs memories have high P/E efficiency, long charge retention time, less gate and drain

disturbance, and good endurance characteristics. Thus this device is very promising for future nonvolatile memory applications in 3D integration of active devices and SOP.

7.2 Further Recommendations

There are some interesting topics for further researches.

(1) In Chapter 2, we can study the effect of source side p^+ junction position in SSOB-TFTs. We divide experiment into two groups: the position of source side p^+ junction is under or offset away the poly-Si gate edge. The p-channel and n-channel characteristics can be combined together in SSOB-TFTs by using single side spacer if the position of source side p^+ junction is under the poly-Si gate edge.

(2) In Chapter 3, the channel film of FSA-TFTs can be crystallized by excimer-laser annealing or NILC technology, and then we can apply the high κ gate dielectric to fabricate high performance FSA-TFTs. Finally, the electrical characteristics can be further improved by fabricating nano-scale FAS-TFTs.

(3) In Chapter 4, first, we study the impact of NH_3 plasma treatment in NSILC-VTFTs. Second, the p-channel NSILC-VTFTs can be fabricated for CMOS application. Then, the electrical characteristics can be further improved by fabricating nano-scale NSILC-VTFTs. Finally, we can apply the high κ gate dielectric to fabricate high performance nano-scale NSILC-VTFTs.

(4) In Chapter 5, the Si / Ge T-gate thick gate oxide layer at the gate edges can be replaced by oxide/nitride/oxide (O/N/O) for nonvolatile memory applications.

(5) In Chapter 6, the tunneling and blocking oxide of poly-Si TFT nonvolatile Ge-NCs memories can be replaced by high quality low temperature oxide. We have discovered that the density of Ge-NCs can be improved by using stacked nitride/oxide

tunneling dielectric. We will develop the new oxide/nitride/Ge-NCs/nitride/oxide (O/N/Ge-NCs/N/O) hybrid memory structures to improve the memory characteristics.

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Chapter 1

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博士論文題目:

應用鎳矽化物與鍺於新穎結構複晶矽薄膜電晶體之研究

Applications of Ni-Silicidation and Germanium for Novel Structures of Polycrystalline Silicon Thin-film Transistors

Publication Lists

1. International Journal:

[1] **Po-Yi Kuo**, Tien-Sheng Chao, Pei-Shan Hsieh, and Tan-Fu Lei,“ Characteristics of self-aligned Si / Ge T-gate poly-Si thin-film transistors with high ON/OFF current ratio,” *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp.1171–1176, May 2007.

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[3] **Po-Yi Kuo**, Tien-Sheng Chao, Jyun-Siang Huang, and Tan-Fu Lei, “Characteristics of Poly-Si Thin-Film Transistor Nonvolatile Ge Nanocrystals Memories with High Programming / Erasing Efficiency,” *IEEE Trans. Electron Devices* in revision.

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2. International Letter:

[1] Hsiao-Wen Zan, Ting-Chang Chang, Po-Sheng Shih, Du-Zen Peng, **Po-Yi Kuo**, Tiao-Yuan Huang, Chun-Yen Chang, and Po-Tsun Liu,“ A study of parasitic resistance effects in thin-channel polycrystalline silicon TFTs with tungsten-clad source/drain,” *IEEE Electron Device Lett.*, vol. 24, no. 8, pp.509–511, Aug. 2003.

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3. International Conference:

[1] **Po-Yi Kuo**, Tien-Sheng Chao, and Tan-Fu Lei,“ Characteristics of poly-Si thin-film transistors with self-aligned Schottky barrier source and ohmic body contact structure,” *2004 International Electron Devices and Materials Symposium (IEDMS2004)*, pp. 301–304. **(Best student paper award)**

[2] **Po-Yi Kuo**, Tien-Sheng Chao, Yan-Syue Huang, and Tan-Fu Lei,“ Characteristics of poly-Si thin-film transistors with fully Ni-self-aligned silicided source/drain and gate structure,” *2006 International Electron Devices and Materials Symposium (IEDMS2006)*, symposium C, pp. 207–208.

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