國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

銅導線中電遷移效應所引發之故障特性探討

An Investigation into the Characteristics of Electromigration Failure Mechanisms in Copper Interconnects

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摘 要

隨著製程線寬快速縮小到奈米(sub-100nm)尺度時，後段連線系統中傳遞的時間延遲(簡稱為 RC 延遲)已逐漸變成限制元件效能的主要因素。因此，為了降低阻值和介電值，工業界已將金屬導線製程中所使用的材質，從鋁(銅)/氧化層變成較低阻值的銅和較低介電係數的低介電材料。然而，銅導線依舊需要解決電遷移所產生元件壽命失效機制的可靠度問題。快速地縮小銅導線的寬度，同時又要維持高的電流承受能力，和更嚴格的可靠度標準需求，電遷移效應將變成未來在銅製程中非常嚴峻的挑戰。

本篇論文將針對銅導線中電遷移效應所引發之故障機制的可靠性問題做一系列的探討。第一章簡介電遷移的物理機制，第二章詳述實驗技巧和樣本準備流程，第三章首先使用銅導線製程中不同的低介電值材料和不同的測試結構互相比較其電遷移效應。不同的測試結構設計可以用來作故障模式分析，進而找出連線系統中的弱連結，三層且兩端使用 via 作連結的金屬線發現到電遷移壽命和所加的電流方向有很大的關係，再者，不同製程策略流程會導致不同的電遷移結果及其故障模式。多重電遷移故障模式在銅雙鑲嵌式製程中已被完整地研究。利用重疊和弱連結模型的統計方法可以決定每一個故障模式的壽命，另外，根據阻值對時間變化關係圖，可以找出其對應的故障模式的壽命。兩種方法得到非常一致的結果。

接下來第四章，瞭解到連線系統中的弱連結，根據這資訊，一個很適合研究銅導線和蓋層之間接面特性的電遷移結構被設計出來。藉著修改蓋層沉積之前的清洗步驟和改變銅蓋層材料的方法，對電遷移壽命有相當顯著的改善。吾人提出一個可能的機制來解釋這個電遷移壽命提高原因，並發現到蓋層沉積前產生銅矽化合物(Cu-silicide)和銅/蓋層之間介面的黏著力對電遷移可靠度有非常重要的影響，且銅/蓋層之間介面的黏著力可以直接關聯到其壽命和活化能。

第五章接著研究電遷移在不同寬度從 0.12 到 10 微米和不同管洞/線(via/line)的排列變化。線寬縮小對電遷移壽命變化有兩方面不同的現象，第一是線寬小於 1 微米時，電遷移中位數故障時間(MTF)隨著線寬只有些微的變化，除了因為 via 限制的條件。第二是線寬大於 1 微米時，在這區域 MTF 和線寬有著強烈的關聯。吾人提出一個可能的理論來解釋這個電遷移壽命趨勢，對多晶結構的金屬線(寬度大於 1 微米)，最主要擴散路徑是晶粒邊界和表面擴散。對於線寬大於 1 微米時，主要的晶粒邊界擴散的活化能大約比起表面和晶粒邊界擴散的活化能高 0.2 eV。使用在電遷移下銅移動速度，亦可得到其相對的活化能，其結果與量測值相當一致。在銅連線系統中，控制電遷移壽命的機制已被完整地研究，進而可以藉著巧妙設計 via 連線而達到最常的壽命。

第六章，利用不同金屬線長度的結構，不同的電流密度和更接近真實情況的三層結構，吾人對電遷移中的短線長度效應作一系列完整的研究，銅製程已被良好的開發，確保缺陷不會造成影響。使用壽命量測和阻值劣化隨時間變化的關係來描述這現象。吾人提出一個簡單的模型理論來解釋不同長度和電流組合時的電遷移壽命趨勢，結果指出臨界長度值(jL)c 和溫度相關，在 250 和 300 度 C 區間隨著溫度下降而上升，藉著一系列電遷移實驗可以得到非常多深刻的理解，更可層別出銅鑲嵌技術其電遷移的特殊行為。

最後於第七章，總結本論文的結論，並對未來研究方向提供一些建議。此研究針對銅導線中電遷移效應所引發之故障機制的可靠性問題做一系列的探討。從設計測試電遷移結構，找出銅鑲嵌製程在連線中最弱的部分，接著，利用製程改變找出提高銅電遷壽命的方法，並提出模型解釋。最後，改變銅導線的幾何寬度、長度和不同 via/line 結構作一系列研究，實驗結果可由吾人的理論解釋，並提供給設計者對於電遷移可靠度設計的規範。藉著這一系列電遷移實驗可以得到非常多深刻的理解，更可層別出銅鑲嵌技術其電遷移的特殊行為。

關鍵字：電遷移，銅連線，多重失效模式，銅矽化合物，附著力，銅/蓋層介面，表面擴散，晶粒邊界擴散，短長度效應。

An Investigation into the Characteristics of Electromigration Failure Mechanisms in Copper Interconnects

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Abstract

The back-end-of-line (BEOL) RC delay has gradually become a major limiting factor in circuit performance as a result of the rapid shrinking of critical dimensions. With reduced resistivities and dielectric constants, the metallization system for the interconnect structures has shifted from Al(Cu)/oxide to copper/low-k dielectrics. However, Cu interconnects still pose a reliability concern due to electromigration-induced failure over time. The rapid decrease in Cu conductor dimensions while maintaining a high current capability and a high reliability has emerged as a serious challenge.

The objective of this dissertation is to investigate the characteristics and failure mechanism involved in Cu electromigration. Chapter 1 gives an introduction to the topic and discusses the background to study. Chapter 2 describes electromigration testing and analysis techniques in detail, and is intended to help familiarize the reader with the experimental aspects of this work in order to create a basis of understanding for the results sections that follow. In Chapter 3, first of all, Cu interconnect electromigration is examined using three low-k materials (k= 2.65 ~ 3.6) in a variety of structures. A number of test structures were designed to identify the EM failure modes and the weak links in the interconnect system. A strong dependence on current direction in the electromigration lifetime of three-level via-terminated metal lines was shown. Moreover, individual processing approaches lead to distinct EM behaviors and related failure modes. Multimodality in the electromigration behavior of Cu dual-damascene

interconnects was studied. Both superposition and weak-link models were used for the statistical determination of the lifetimes of each failure model (statistical method). Results correlated to the lifetimes of the respective failure models physically identified according to resistance time evolution behavior (physical method). A excellent agreement was achieved.

Based on the above understanding, the weak links of interconnect system were identified. Chapter 4 describes the correlation between the electromigration lifetime and the Cu surface cap-layer process. An especially suitable EM test structure was designed to evaluate the properties of the Cu cap-layer interface. A significant improvement in electromigration lifetime is achieved through modification of the pre-clean step before the deposition of the cap-layer and by changing the Cu cap/dielectric materials. A possible mechanism for the enhancement of EM lifetime was proposed. A Cu-silicide formation prior to cap-layer deposition and the adhesion of the Cu/cap interface were found to be the critical factors in controlling Cu electromigration reliability. The adhesion of the Cu/cap interface can be directly correlated to the electromigration MTF and the activation energy.

Chapter 5 outlines the effects of width scaling and layout variation on dual-damascene Cu interconnect electromigration. Electromigration versus line width in the 0.12—10 μm range and the configuration of the via/line contact has been investigated. There are two scenarios that cover the impact of width scaling on electromigration. One is the width <1 μm region, in which the MTF shows a weak width dependence, except under the via-limited conditions. The other is the width >1 μm region, in which the MTF shows a strong width dependence. A theory was proposed to explain the observed behavior. For polycrystalline lines (width >1 μm), the dominant diffusion paths are a mixture of grain boundary and surface diffusion. The activation energy for the dominant grain boundary transport (width >1 μm) is approximately 0.2 eV higher than that of the surface and grain-boundary transport (width ~ 1 μm). The derived activation energies for both grain-boundary and surface diffusion are obtained from the Cu drift velocity under EM stressing. The activation energy data obtained from both the measured and derived methods for both the surface and grain-boundary transport were found to be compatible. The mechanisms governing

the EM lifetime of interconnects leads to the identification of via interconnect design rules for maximizing electromigration lifetime.

In Chapter 6, the electromigration short-length effect is investigated through experiments on lines of various lengths (L), being stressed at a variety of current densities (j), and using a technologically realistic three-level structure. This investigation represents a complete study of the short-length effect following the development of an enhanced dual-damascene Cu process. Lifetime measurement and resistance degradation as a function of time were used to describe this phenomenon. A simplified equation is proposed to analyze the experimental data from various combinations of current density and line length at a certain temperature. The resulting threshold–length product $(jL)_C$ value appears to be temperature dependent, decreasing with an increase in temperature in a range of 250°C to 300°C.

Finally, Chapter 7 summarizes the results of the study and outlines some potential future directions for research into the interconnect electromigration reliability field. The multimodality distributions in various Cu/low-*k* processes are fitted using various bimodal methods to obtain precise lifetime values. Methods of optimizing the Cu electromigration performance have been investigated through Cap/dielectric interface re-engineering. Geometric variations of the test structure, including width scaling, length scaling, and vai/line configuration effects, were investigated to reveal the characteristics of Cu electromigration. A possible model is proposed to explain the electromigration behavior, and provides the means to ensure future design-in reliability. Much insight into electromigration failure modes and characteristics has been gained through experimentation using Cu dual-damascene technology to identify its distinctive behaviors.

Keyword: Electromigration, Cu interconnects, Multimodality failure, Cu-silicide, Cu/cap interface, Adhesion, Surface diffusion, Grain boundary diffusion, Blech effect.

Dedication

To my wife

瓊足

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FIGURE CAPTIONS

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LIST OF SYMBOLS

A	material constant based on the microstructure and geometric properties of the conductor
B	Effectice elastic modulus
C	Concentration of atoms (atoms/cm^3)
CDF	Cumulative density function
d	Grain size
D	Diffusion coefficient
D_0	Diffusion coefficient at the limit of an infinitely high temperature
D_{gb}	Diffusion coefficient along the grain boundary
D_I	Diffusion coefficient through the interface
D_l	Diffusion coefficient through the lattice
D_p	Diffusion coefficient through the pipe
D_s	Diffusion coefficient through the surface
D_{eff}	Effective Diffusion coefficient
e	The fundamental electron charge
E	Electric field
E_a	Activation energy
f_{gb}	The fraction of atoms diffusing along the grain boundary
f_l	The fraction of atoms diffusing through the lattice
j	Current density
J_a	The atomic flux
J_{gb}	The atomic flux along grain boundary
J_l	The atomic flux along lattice
$(jL)_C$	Threshold–length product
k	Boltzmann constant

l	The columnar grain length
L	Metal length
MTF	Median time to fail
n	Current density exponent
$P(A)$	Probability of one failure mode A
R	Resistance
T	Temperature (in K)
$T50$	the 50^{th} percentile fail time of a failure population
TTF	Time to fail
TCR	Temperature coefficient of resistance
V_{fail}	Failure volume
v_d	Drift velocity of Cu
w	Metal width
Z^e	Electrostatic charge
Z^w	Electron wind charge
Z^*	Effective charge
σ	Deviation in time to failure
σ_s	Stress in the metal line
δ	Grain boundary thickness
δ_{GB}	Width of grain boundary
δ_I	Width of metal/liner interface
δ_S	Width of surface
μ	Mobility
ρ	Electrical resistivity
Ω	Atomic volume

Chapter 1

Introduction

Beginning in 2000, Integrated Circuit (IC) technology has been driven towards the nanotechnology era in the pursuit of higher performance and integration. It has become increasingly desirable to integrate greater functionality in a single chip. However, interconnecting the devices using metal wires consequently occupies a larger percentage of the available space. In addition to achieving a higher density, smaller devices and a larger number of metal layers are required. ICs can have up to 11 metal layers, as used in 65nm designs, for programmable logic devices. Figure 1.1 shows the cross-section of hierarchical scaling in an integrated circuit. According to the International Technology Roadmap for Semiconductors (ITRS), 2005 edition [1.1], 1212 meters of interconnect length per centimeter squared of active area will be required to construct a high-performance chip in 2006. For a million-transistor microprocessor chip, an average interconnect length of ~ 100 μm is suggested, but actually a distribution of both shorter and longer lines is present. Critical interconnects such as clock, control, and data lines between processor and cache may run the entire length of a chip and be 1-2 cm long. Interconnect delay related to resistance (R) and capacitance (C) has become the more dominant concern rather than over gate delay issues that were the primary focus prior the ULSI era, as shown in Fig. 1.2. The parasitic effects introduced by the metal line display a scaling behavior that differs from the active components such as transistors, and they tend to gain in importance as device dimensions are reduced and circuit speed is increased. In fact, they start to dominate some of the relevant metrics of digital IC such as speed, energy consumption, and reliability. A careful and in-depth analysis of the role and behavior of the interconnect metal line in semiconductor technology is, therefore, not only desirable, but also essential.

1.1 Interconnect Reliability

The increasing complexity and performance of semiconductor products in combination with continuous feature size scaling imposes many new reliability challenges. For upcoming technology nodes, the introduction of new materials, processes, devices and packaging techniques will require the investigation of many additional advanced reliability engineering methods. IC reliability involves many disciplines, such as design, processing, assembly, and testing. Typically, manufacturers design an IC to have an operating lifetime of 10 years. Product reliability is assured if each of the elements contained in the product is reliable for that length of time. Product reliability consists of three major elements: design reliability, process reliability, and assembly reliability. If the reliability of each element matches the required lifetime, then product reliability is assured.

ICs are composed of a large number of discrete components, such as transistors, resistors, interconnects, dielectric thin film, and capacitors. These components are combined through process integration to produce ICs. One way to evaluate the reliability of the entire IC process is to measure the reliability of each of the major process modules. Some of the key modules from a reliability point of view are: (1) gate dielectric, (2) transistor, and (3) interconnects. In the nanotechnology era, the concept of *design for reliability* is extremely important. Reliability must be considered at all stages of IC development, including design, process development, and manufacturing. For example, the factor that limits IC Back-End-Of-Line (BEOL) reliability will change from total line length to the number of vias, via density and redundancy. Tools developed to cater for the concept can identify weak critical area and mitigate them automatically during the design process. From the interconnect design perspective, reliability is the quality by which the interconnects maintain signal integrity and produce the desired functionality over the lifetime of the chip. That is, the change of resistance in a metal interconnection, either as a series of vias or a

single metal line, must remain within the tolerance of the design rules as the current passes through it. It only takes the failure of one of these metal line segments or vias to cause the entire chip to fail. Consequently, interconnect reliability requirements have become more stringent, as shown in Fig. 1.3, and the issue will become a more critical challenge in the future. Electromigration has always been one of the primary interconnect reliability concerns, and investigation into the phenomenon has persisted to the present day, where it still remains a troublesome reliability issue, as reflected by the many publications and conference sessions devoted to the topic each year.

1.2 Basic Electromigration Physics

Assuming a thin Cu film line 0.1 μm wide and 0.2 μm thick carrying a current of 1 mA, the current density will be 5 x 10^6 A/cm^2. Such a high current density will cause mass transport in the line at a device operation temperature of 100°C. Mass transport resulting from the passage of a DC current has been identified as the cause of the majority of failures in the metal interconnect system of IC chips. This phenomenon, known as electromigration, demonstrates the atomic motion in a metal line under the influence of a supplied electric field, and is basically a diffusion phenomenon under a driving force. The electromigration phenomenon has been observed for more than a century [1.2]; however, it was first identified as a reliability problem in integrated circuit metallizations around 40 years ago [1.3]. Diffusion and atom movement in a solid, and a brief history and overview of electromigration theory will be given in this section.

1.2.1 Diffusion and Atom movement in a Solid

Diffusion is defined as the migration of atoms under the influence of a concentration-gradient driving force. Fick's law, the phenomenological equation that defines diffusion, is written as:

$$\mathbf{J_m = -D}\frac{dC}{dx} \tag{1.1}$$

Concentration gradients ($\frac{dC}{dx}$) in the positive x direction cause the transport of a mass flux of atoms (J_m) in the negative x direction. If more atoms leave a region than enter it, in time, this loss of matter ($\frac{dC}{dx} < 0$) leads to mass depletion, or even voids that can affect reliability. Such effects may occur at the interface between different phases, the grain boundary, or through structural defects. The diffusion coefficient D, a measure of the extent of mass transport, depends on a number of factors, including the nature of the diffusing atoms, the specific transport path (i.e., lattice, grain boundary, dislocation, surface, etc.), temperature, and the concentration of the diffusing species. The temperature dependence of the diffusion coefficient D, the most important factor, is given by the equation:

$$\mathbf{D = D_0 exp(-}\frac{Ea}{kT}\mathbf{)} \tag{1.2}$$

Where D_0 is the diffusion coefficient at the limit of an infinitely high temperature, Ea is the activation energy, which is a characteristic of the diffusion paths in the given metal. There are many paths an atom can take during diffusion in a metal line. Because most interconnect materials are polycrystalline, modeling the diffusion in polycrystalline materials is necessary and fundamental. The key to understanding diffusion in polycrystalline materials is the presence of grain boundaries and the fast diffusion paths that they provide. The diffusion coefficients for the grain boundary and the lattice are different. In addition, the atoms can move between the two regions depending on their local concentration and segregation coefficient. The flux equations for any species in each path are simply [1.4]:

$$\mathbf{J_{gb} = -D_{gb}}\left(\frac{\partial C}{\partial x}\right)_{gb} \tag{1.3}$$

$$\mathbf{J_l = -D_l}\left(\frac{\partial C}{\partial x}\right)_{l} \tag{1.4}$$

Where D_{gb} refers to the diffusivity along the grain boundary, and D_L is the diffusivity through the

lattice. The simplest model assumes that there is an effective diffusion coefficient for a species that describes the net diffusion through a polycrystalline material. This D_{eff} is just the sum of the diffusion coefficients in each of the two region types, grain boundary and lattice, each scaled using the relative cross-section area of each region. The larger the relative cross-sectional area of the region, the more atoms transport through that region, and the more weight is given to the diffusion coefficient of that region. The effective diffusion coefficient in this model is:

$$\mathbf{D_{eff}=D_l f_l+D_{gb} f_{gb}} \tag{1.5}$$

Where f_l and f_{gb} are the fraction of atoms diffusing through a given pathway. For example, consider diffusion through a structure with square columnar grains of length l, and grain boundary thickness δ, as shown in Fig. 1.4. The cross-sectional area of each grain is l^2 and the area of the grain boundary is $l\delta$. The fraction of the atoms diffusing through the grain boundary is thus:

$$\mathbf{f_{gb}=}\ \frac{gb\_area}{grain\_area}=\frac{l\delta}{l^2}=\frac{\delta}{l} \tag{1.6}$$

In the general form of the effective diffusion coefficient, a number of pathways, such as surface, interface, grain boundary, pipe, and lattice diffusion need to be considered. The various pathways can be expressed as [1.5]:

$$\mathbf{D_{eff}=D_l f_l+D_{gb} f_{gb}+ D_s f_s+ D_p f_p+ D_I f_I} \tag{1.7}$$

The subscripts identify the pathways of diffusion, where s≡surface, p≡pipe, and I≡interface. As electromigration can occur through these possible pathways, then the notion of pathways requires the identification of the fastest path that drives electromigration failure [1.6]. It is common to have more than one driving force acting on a solid. Electric fields, electric currents, mechanical stress, humidity gradients, and temperature gradients are examples of forces that serve to accelerate device failure.

1.2.2 Electromigration Phenomenon

Electromigration is a combination of thermal and electrical effects on mass motion. However, before describing the phenomenon, the origin of stress in metallization should be briefly introduced. The difference in thermal expansion between the metal and the dielectric material is rigidly bonded, and can cause mechanical stress in the lines. The stresses already exist as a result of the metal stack deposition and alloying processes. For Al, passivated by Si_3N_4 deposited at an elevated temperature, the metal contracts upon cooling more than the nitride. The tensile stress results when the actual lattice spacing is greater than the thermal equilibrium. The result, therefore, is tensile stress in the Al, and compression in the Si_3N_4. The driving force in conventional SiO_2 based materials is the tensile stress. The magnitude of stress in the confined Al line has been reported to be in a range of up to approximately 600 MPa [1.7]. With such a high level of stress, even small irregularities may have great effect as the Al tries to relieve itself of this large tensile stress. Since the Al is confined, it cannot relieve the stress by plastic deformation. It is believed the major relaxation of stress occurs by the diffusional creep of the atom, which causes void formation and growth. Thus, voids are created and grown. Even in the absence of a current, it has been observed that the resistance of the metal interconnect will degrade as a result of mechanical stress. This mechanism is called stressmigration (SM), and is one of the more unsettling reliability issues associated with metallization. The electromigration picture becomes even more complex if both a thermal and an electrical current are applied to the metal line.

1.2.3 Theory of Electromigration

At a fundamental level, electromigration involves the interaction between current carriers and migrating atoms. It is generally accepted that in an electrical conductor, electrons streaming towards the anode can impart sufficient momentum to the atomic ion core to propel them into neighboring vacant sites. Figures 1.5(a) and (b) illustrate this atomic movement along the lattice

[1.8] and grain boundaries, respectively. The lattice diffusion is shown in Fig. 1.5(a), where circles represent atoms, and a cross at B represents a vacancy, or a missing atom. An elementary step in electromigration will occur when the atom at A is forced into the vacancy at B under the influence of electrons move from left to right. The atom must squeeze through at O between the atoms at M and N. The theory of "electron wind" accounted for the induced mass transport, an idea that laid the foundation for the basic understanding of electromigration. The concept of the "electron wind" driving force was first formulated by Huntington and Grone [1.9], who employed a semiclassical "ballistic" approach to treat the collision of the moving atom by the charge carriers and yielded a driving force depending on the type of defects and the atomic configuration of the jumping path. This mass transport resulting from the passage of a DC current can be the cause of failure in the metal interconnects system on an IC chip.

When a high current passes through metals with high-atomic diffusivities, such as Al or Cu, the electrons can transfer some of their momentum to the metal atoms, causing them to move. Net atomic transport of metal ions arises under a supplied electric field as a result of two effects. The first of these effects is the interaction of the supplied electric field and the metal ions and is proportional to the product of the field strength E and the valence of the metal Z. The second effect is the momentum transferred to the ions from the electrons. This contribution is often referred to as the "electron wind" force. In Cu and Al, the "electron wind" force has been found to be about an order of magnitude greater than the electrostatic force [1.2]. The driving force is expressed usually in terms of an effective charge Z*, which includes the electrostatic (Z^e) and the electron wind (Z^w) contributions [1.2, 1.10]. The force on the atoms is found to be:

$$\text{Force}=(Z^e+Z^w)eE \equiv Z^*eE = -Z^*e\rho j \qquad (1.8)$$

where Z* is the effective ion valence or charge number [1.2,1.9], e is the fundamental electron charge, E is the electric field ($E=\rho j$), ρ is the electrical resistivity of the metal, and j is the current density. As current density opposes the electron flow direction, a negative sign for j

results in a positive sign in Force. The atomic flux induced by the current (in the direction of the electron flow) equals the force times the mobility times the concentration and is thus:

$$J_a=(\text{Force})x(\mu)x(C) = -Z^*e\,\rho\, j\,\mu C = -\frac{DC}{kT}Z^*e\,\rho\, j \quad \text{.....(1.9)}$$

where J_a denotes the flux of the atoms expressed in the number of atoms passing perpendicular to a reference surface of unit area in unit time (atoms per unit area per sec), μ is the mobility, C is the concentration of atoms (atoms/cm^3), D is the diffusion coefficient, *k* is Boltzmann's constant, T is temperature (in K), and the well-known Einstein equation is used. Equation 1.9 expresses the proportionality between atomic flux and electron flux. J_a is the atomic flux due to electromigration. Electromigration is thus characterized at a fundamental level by the material constants Z*, D, and ρ. Combining eq. 1.7 and 1.9, the various pathways for electromigration damage formation can be examined using Z^*D_{eff} term:

$$Z^*D_{eff} = Z_l^* \mathbf{D_l f_l} + Z_{gb}^* \mathbf{D_{gb} f_{gb}} + Z_s^* \mathbf{D_s f_s} + Z_p^* \mathbf{D_p f_p} + Z_I^* \mathbf{D_I f_I} \qquad (1.10)$$

Each pathway is anticipated to have a different Z* component because the "electron wind" force varies according to the local electronic environment surrounding a given atom.

1.2.4 Effect of Stress on Electromigration

The atomic flux in eq. 1.9 is an oversimplification. In reality, as atoms move from one end of an interconnect to another under electromigration, a mechanical stress gradient is created in the line. This additional effect is a back flux of atoms that opposes the forward flux. This back flux is due to a stress gradient that occurs as a result of the depletion and build-up of metal atoms at the flux divergence points. Figure 1.6 illustrates this phenomenon [1.4]. When the metal atoms diffuse due to the "electron wind" force, they become depleted at the start of a polygranular cluster region and accumulate at the end of the region. The "electron wind" force creates tensile stress near the cathode where the atoms deplete, and compressive stress near the anode where the

atoms accumulate [1.11]. The resulting stress gradient leads to mechanical driving force, referred to as the back-stress force, which opposes the "electron wind" force. The atomic flux can be described using the following equation [1.11].

$$J_a = -\frac{DC}{kT}\left(Z^*e\rho j - \Omega\frac{\partial\sigma_s}{\partial x}\right) \quad (1.11)$$

where Ω is the atomic volume, and $\partial\sigma_s/\partial x$ is the stress gradient along the line. The first observations of the effect suggested that there is a critical line length below which the electromigration atomic flux can be entirely balanced by the stress-directed counter flux of atoms [1.12]. This is a steady-state condition, and the steady-state stress of eq. 1.11 is the stress that would be present at that time. If the metal, in its environment, can withstand this stress then failure will not occur. But if it cannot, then failure is likely. The stress at which failure occurs is called the critical stress, σ_{crit}. Therefore, a criterion for the failure of an interconnect under elecromigration conditions could be if the steady-state stress is equal to or greater than a specific critical stress value.

1.3 Electromigration Lifetime Model

The reliability of a metal interconnect is most commonly determined by carrying out a lifetime experiment on a set of lines to obtain the median time to failure (MTF). The data for the actual time to failure for each line is plotted on a lognormal graph, and the value of T50 (the time at which 50% of the lines fail) is extracted, along with the lognormal shape parameter. In practice, the stress experiments are often based on tests conducted at accelerated conditions (i.e., high temperature and current densities), as shown in Fig. 1.7. If the failure mechanism is the same in both the accelerated and the standard operating conditions, the data is scaled back to design rule conditions (i.e., low temperature and current density). The lifetime extrapolation is commonly based on Black's equation [1.13,1.14], which expresses MTF, or T50 (the 50th percentile fail time

of a failure population), as:

$$\text{MTF}= A(\frac{1}{j})^n \exp\left(\frac{E_a}{kT}\right) \tag{1.12}$$

where A is a material constant based on the microstructure and geometric properties of the conductor, n is the current density exponent, j, Ea, and *k*T have previous definitions. In the electronics industry, the operating current density and temperature are the most important parameters in an interconnect system from a design perspective. The operating current density, j_{use} or j_{max}, represents the maximum current density that the interconnect system can maintain while still guaranteeing a certain failure rate over a certain period of operation time at a standard operating temperature. To determine this value, a ratio of Black's equation (eq. 1.12) between a standard operating and test conditions can be employed for extrapolation [1.15]:

$$TTF_{use} = MTF_{use}(\frac{j_{use}}{j_{test}})^{-n} \exp\left[\frac{E_a}{k}(\frac{1}{T_{use}} - \frac{1}{T_{test}})\right] \exp[-N\sigma] \tag{1.13}$$

where TTF_{use} is the time to failure under standard operating conditions, MTF_{test} is the median time to failure under accelerated test conditions, j_{test} is the test current density, T_{test} is the test temperature, T_{use} is the standard operating temperature, N is a constant that relates MTF to a time-to-failure at a different failure percentage, σ is the deviation in time to failure, and n, Ea and *k* have previous definitions. The expression term exp[-Nσ] in eq.1.13 relates the median time to failure to a different failure percent. An expression for j_{use} can be written as eq.1.14 by rearranging eq.1.13.

$$j_{use} = j_{test}\left[\frac{MTF_{test}}{TTF_{use}} \cdot \frac{1}{\exp\left[\frac{E_a}{k}(\frac{1}{T_{use}} - \frac{1}{T_{test}})\right]\exp[-N\sigma]}\right]^{1/n} \tag{1.14}$$

where TTF_{use} is a known operating lifetime of 10 years or 10^5 hours for a given specification.

1.4 Thesis Statement

The goal of this thesis is to investigate the characteristics and failure mechanisms involved in Cu electromigration. Cu interconnect test structures are characterized in terms of their design. The multimodality distributions in various Cu/low-*k* processes are fitted using various bimodal methods to obtain precise lifetime values. Methods of optimizing the Cu electromigration performance have been investigated through Cap/dielectric interface re-engineering. The dominant diffusion paths for polycrystalline lines (width >1 μm) are examined using activation energy extraction and a drift velocity model. The Blech effect on dual-damascene Cu interconnects is evaluated to reveal influence of the back-stress force on line length. Threshold–length product $(jL)_C$ values are determined using various methods. Much insight has been gained through electromigration experiments with Cu dual-damascene technology to identify its distinctive behaviors.

1.5 Organization of Thesis

This thesis consists of seven chapters. Chapter 1 gives an introduction to the topic and discusses the background to study. Chapter 2 describes electromigration testing and analysis techniques in detail, and is intended to help familiarize the reader with the experimental aspects of this work in order to create a basis of understanding for the results sections that follow.

In Chapter 3, following the successful integration of Cu/low-k BEOL processes, package level electromigration tests have been performed using various low-k materials in order to compare the performance and verify the stability of the Cu dual-damascene process. Various stress conditions for a number of structures were studied enable an understanding of the failure modes and to identify the weak links in an interconnect system. In addition to a well-understood failure mechanism, a precise lifetime prediction methodology is essential in order to describe

circuit degradation due to electromigration damage.

Chapter 4 describes the correlation between the electromigration lifetime and the Cu surface cap-layer process. An especially suitable EM test structure has been designed to evaluate the properties of Cu cap-layer interface. A three-level dual-damascene Cu interconnect line has been produced to allow a series of experiments to be carried out. This chapter illustrates the interface between the Cu line and the dielectric capping layer, pre-clean treatment prior to dielectric layer deposition.

Chapter 5 outlines the effects of width scaling and layout variation on dual-damascene Cu interconnect electromigration. Electromigration experiments have been conducted using both wide and narrow lines in order to emphasize the main diffusion path in a full Cu dual-damascene process, since the electromigration diffusion mechanism may be different for both narrow lines and wide lines. A theory is proposed to explain the results.

In Chapter 6, the Blech effect or the short-length effect on a dual-damascene Cu process and its temperature dependence is investigated by using a technologically realistic interconnect structure. The Blech effect is an important consideration from a reliability standpoint, since designers are able to create interconnect layouts that are mostly electromigration resistant by ensuring the majority of lines are below the critical length. In this work, an alternate means of determining the threshold–length product $(jL)_C$ value, and a model that relates it to the failure volume and atomic flux is proposed. A test was performed for a greatly extended time period to examine the extracted $(jL)_C$ values and verify the immortality of Cu/low-k interconnects.
Finally, Chapter 7 summarizes the results of the study and outlines some potential future directions for research into the interconnect electromigration reliability field.

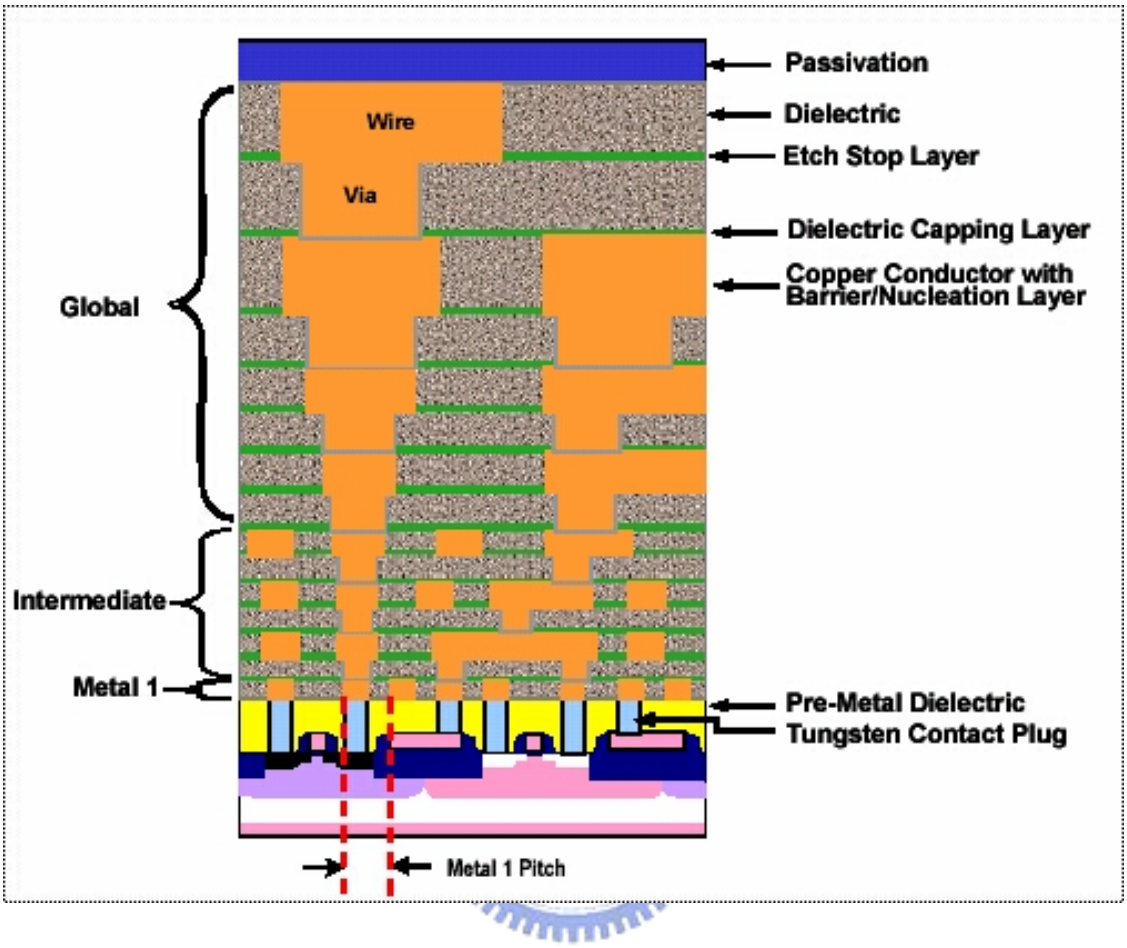


Fig.1.1 Cross-section of Hierarchical Scaling in an Integrated Circuit showing multi-layer interconnects on top of a device. Source: the ITRS 2005 edition [1.1]

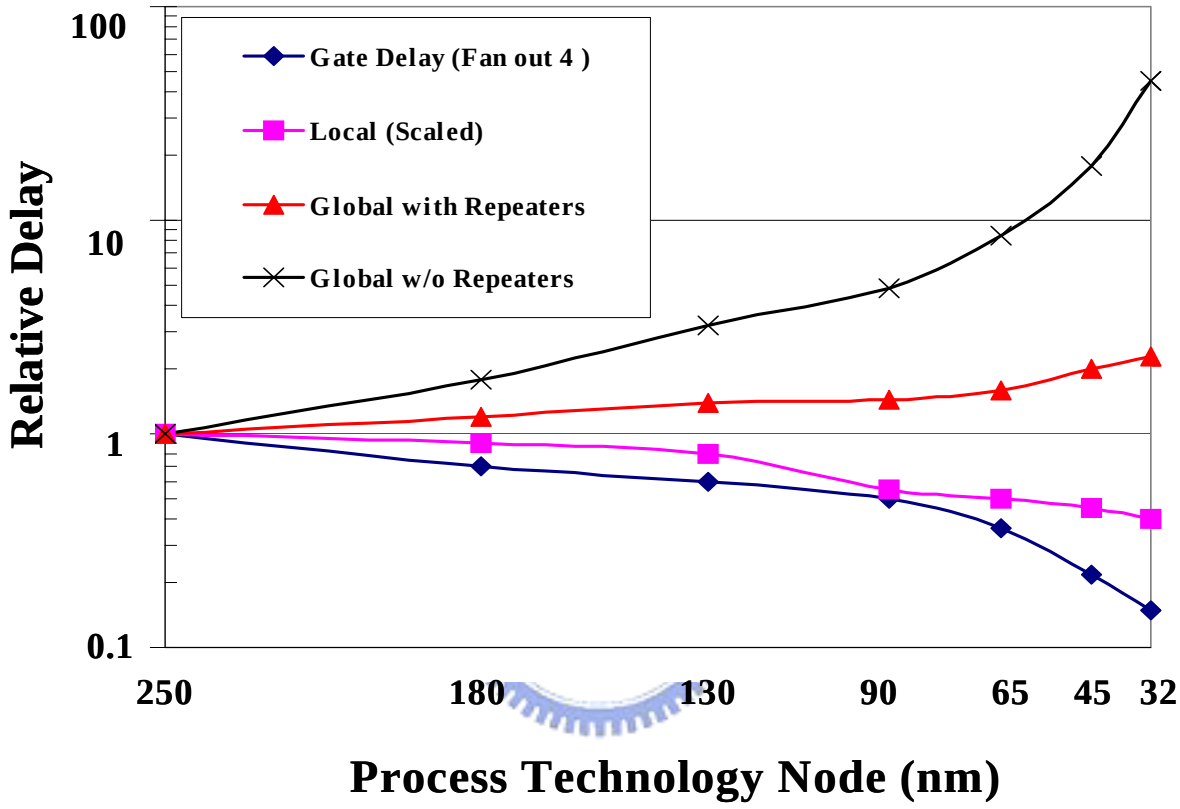


Fig.1.2 Demonstrates Delay for metal 1 and global wiring versus feature size. Source: the ITRS 2005 edition [1.1].

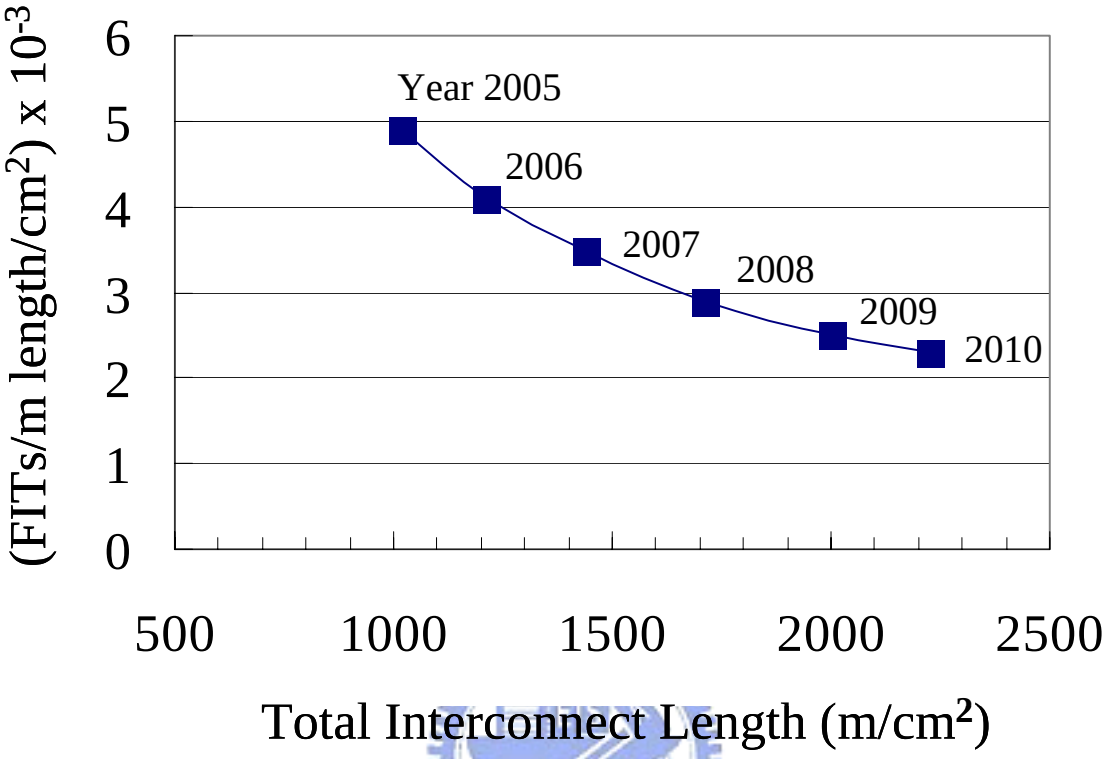


Fig.1.3 Interconnect reliability requirement versus total interconnect length in different years. FITs (1 failure in 10^9 hours of service =1 FIT), Source: the ITRS 2005 edition [1.1].

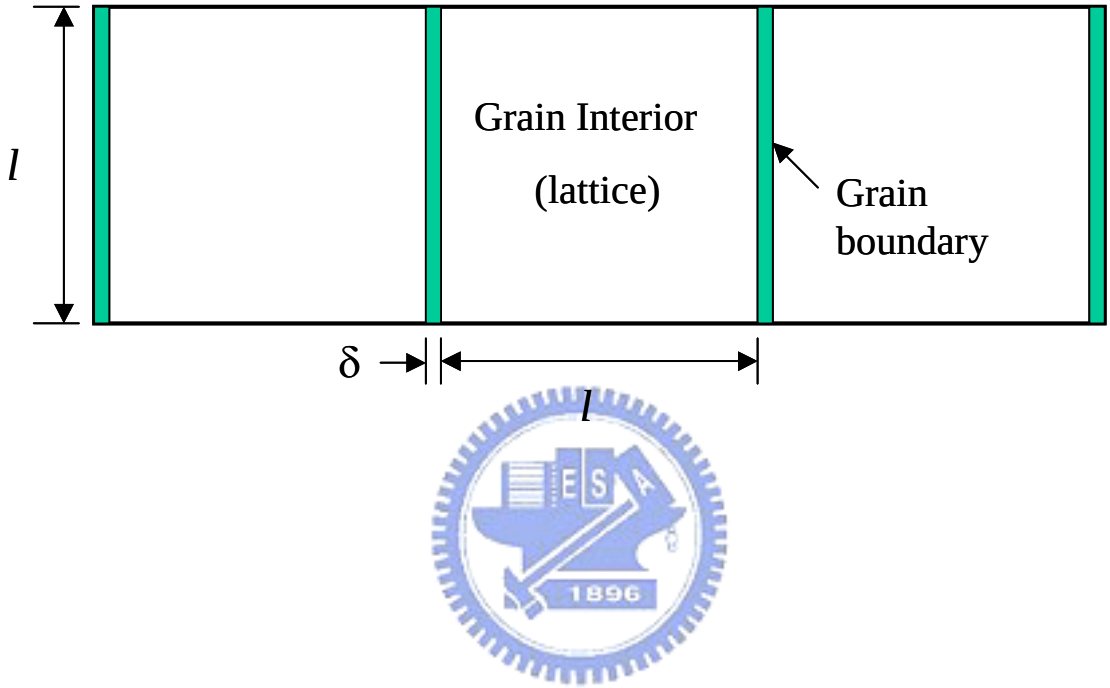


Fig.1.4 Simple representation of grains and grain boundary regions. This is a cross section of a columnar polycrystalline film with square grains. *l* is the grain width and length and d is the grain boundary width, *l*>>δ, Source [1.4].

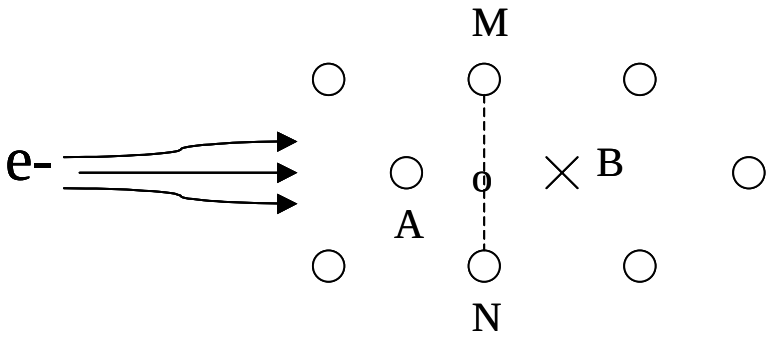


Fig.1.5(a) Schematic representation of the motion of an atom and a vacancy in lattice diffusion [1.5]. Circles represent the atomic cores.

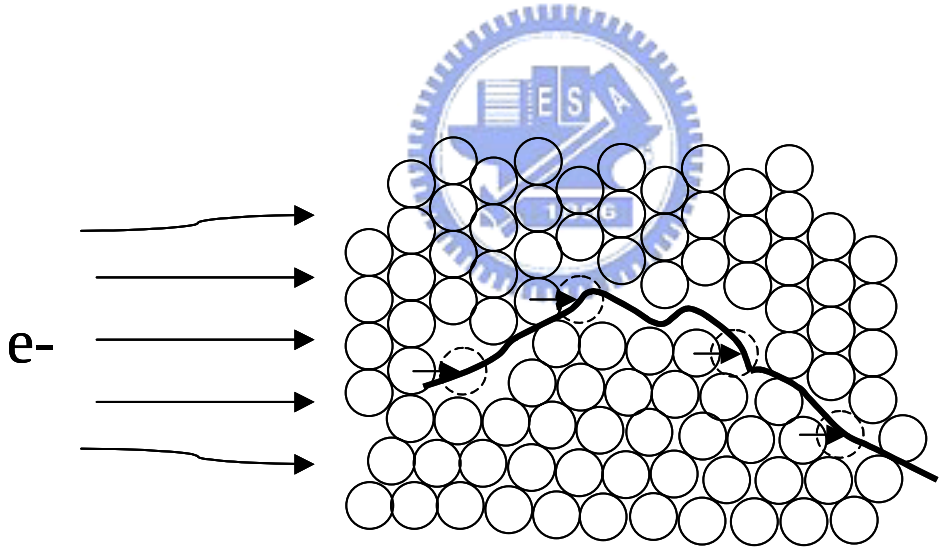


Fig.1.5(b) Schematic representation of the motion of an atom and a vacancy in grain boundary diffusion. Circles represent atom boundary, solid line is grain-boundary.

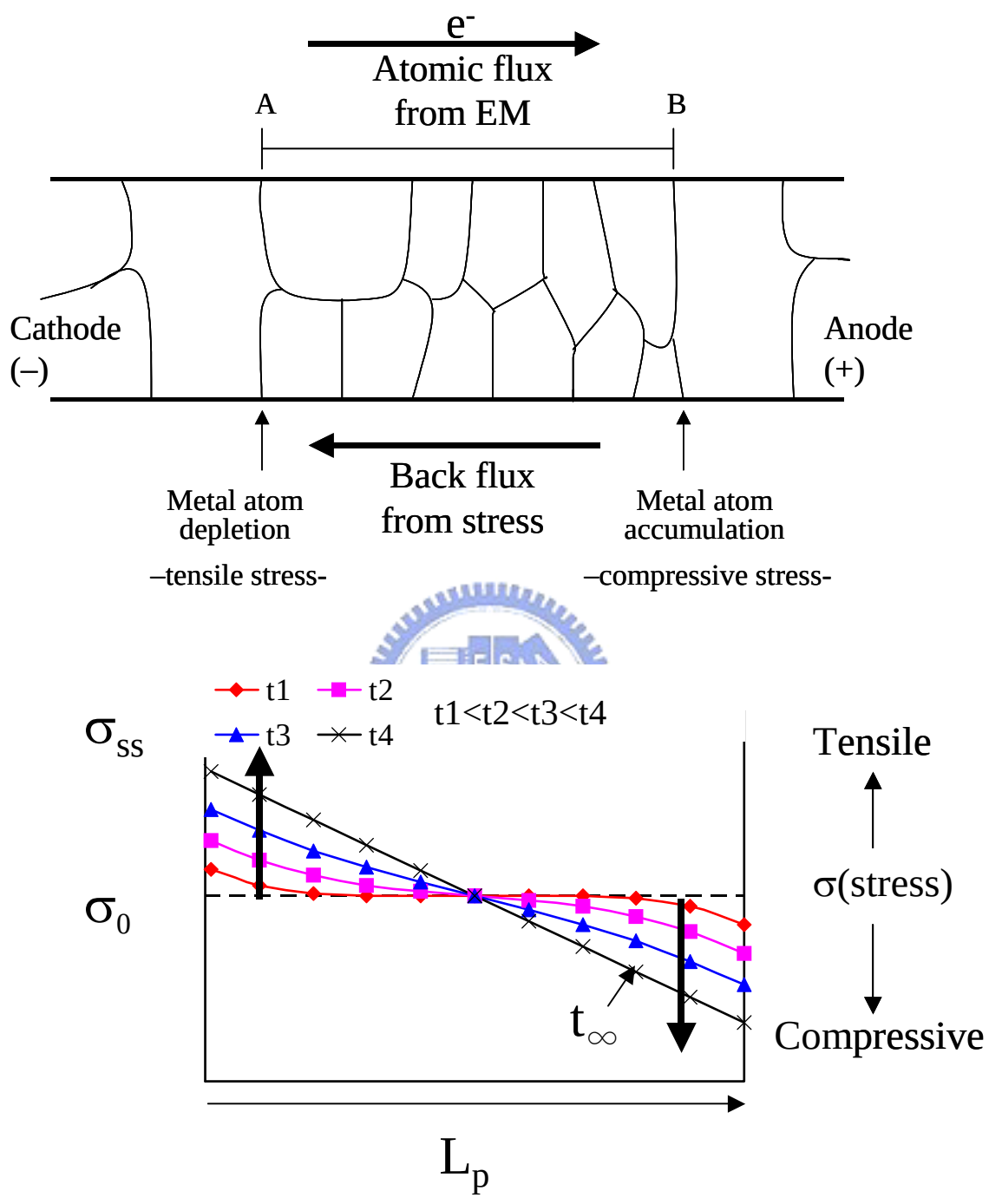


Fig.1.6 Schematic representation of stress buildup due to depletion and accumulation of the metal atoms at the ends of the region. This stress causes a back flux of the metal atoms, which opposes the flux due to EM [1.4].
In bottom graph, the stress evolution during electromigration in a straight-line interconnect terminating block boundary.

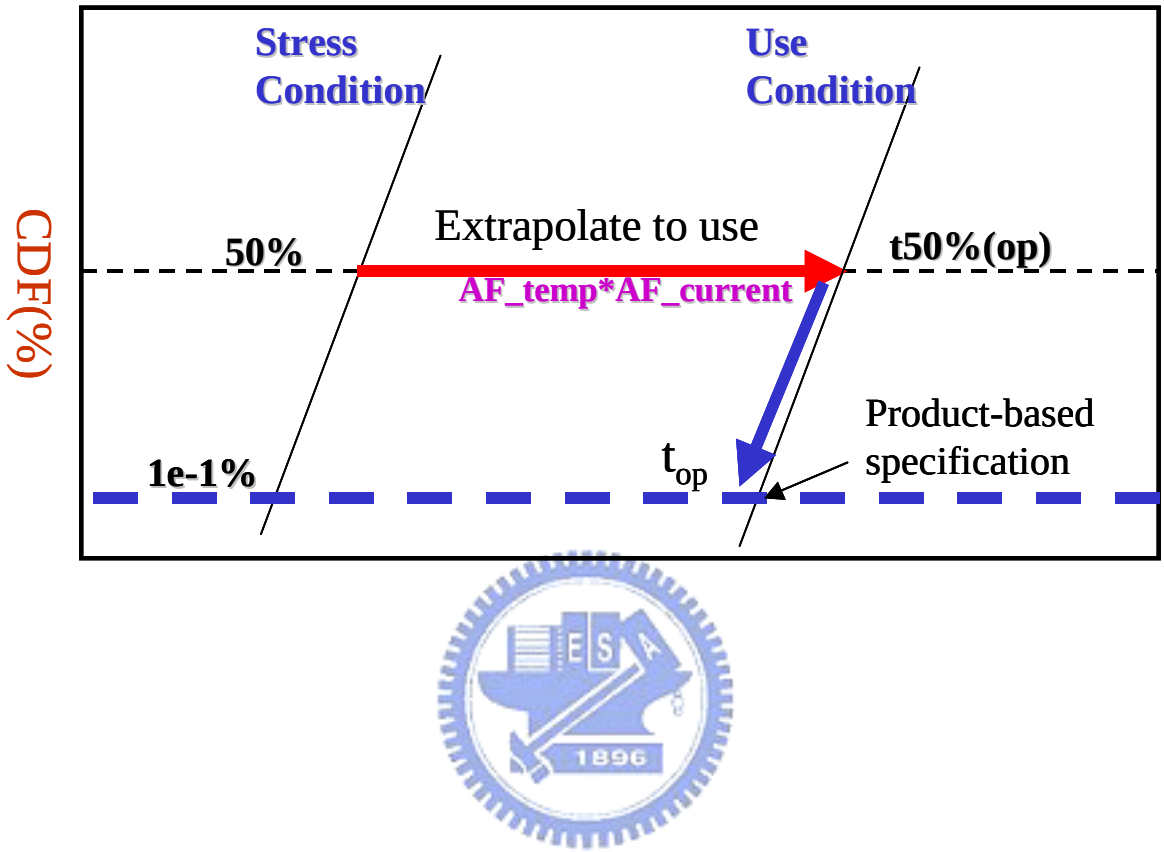


Fig.1.7 Lifetime calculation from accelerated test need to be extrapolated to use conditions, which are typically at lower temperatures and current densities.

Chapter 2

Experimental Techniques

In the following section, the experimental techniques used in this work will be described. This chapter is intended to help familiarize the reader with the experimental aspects of this work in order to create a basis of understanding for the following results sections.

2.1 Interconnect Processing

The fabrication of multi-level Cu interconnects is achieved using a dual-damascene process [2.1]. In a standard damascene process, the dielectric level is pattered first, then metal is deposited into the trenches, followed by chemical mechanical polishing (CMP) process to remove the excess surface layer and leave the material in the trenches. Figure 2.1 illustrates the process steps for Cu dual-damascene metallization. The first step is the deposition of a planar dielectric stack film, which is then patterned and etched using standard lithographic and dry-etch techniques to produce the desired via and wiring pattern. In order to protect the devices from damage by the diffusion of Cu, the vias and trenches formed in the dielectric layer must be coated with a diffusion barrier. This diffusion barrier material provides an efficient seal that prevent the Cu from migrating into the interlevel dielectric (ILD) and a surface on which the Cu seed can be deposited [2.2]. The barrier material used in this study was TaN/Ta, a bi-layer barrier in which a strong adhesion is formed between the TaN and the ILD, and is an excellent metal interface between the Ta and the Cu seed layer. The TaN/Ta liner and Cu seed layers were deposited sequentially using physical vapor deposition (PVD) [2.3]. In addition, resputtering results in excellent side wall coverage and void free vias. This seed layer provides a preferred surface to which Cu can be plated using an electrolysis method. The desired pattern is then filled with Cu

using this electroplating process [2.4]. Once the trench or via is filled, the excess Cu must be removed using a chemical mechanical polishing (CMP) technique. Finally, a cap-layer is deposited to seal the top surface of the Cu film. The process is then repeated for each interconnect level.

2.2 Sample package

All electromigration testing conducted in this study was performed using package level testing. The wafers are first diced using a diamond saw to provide the dies that contain the electromigration test structures. These dies are then bounded on a 16-Pin dual inline package (DIP), as shown in Figure 2.2(a). The package consists of two rows of 8 pins that correspond to bonding posts that surround the well of the package. The wirebonds are used to connect the bond posts of the package to the bond pads of the test structure, as shown in Figure 2.2(b). The wirebonded packages are then loaded into the socket boards, which are then inserted into an electromigration testing oven. The current is applied to the electromigration test pattern through the socket boards to the package, and then through the wirebonds to the test structure. The main advantage of this technique is that it allows for the simultaneous testing of great numbers of samples. The drawbacks of package level testing are the high cost and time consumption.

The wafer level technique is another electromigration testing method. In wafer level experiments, a wafer is placed on a hot-chuck, heated to the desired temperature, and then a probe card is lowered into contact with the test structure. An advantage of this method is that it does not require the expense of packaging the test structures. However, the technique is severely limited in that it can not effectively test a large number of samples simultaneously. Using the wafer level technique, it is difficult to maintain an adequate contact between the probe card and the test structure for testing period over hundred hours. In order to achieve a fast response (minutes to a few hours at most) from experimental testing, it is necessary to supply an extreme

high current on the test structure. A disadvantage of this rapid wafer level test is that large current densities that generate steep thermal gradients must be employed. Because of this, the measured lifetime may not physically extrapolate well to situations where a smaller current prevails. Consequently, the wafer level technique is not an industrial standard method for electromigration testing during the process qualification stage. On the contrary, the typical standard method for electromigration testing is at package level due to capability of measuring a large samples and using low stress current densities.

2.3 Electromigration testing

Electromigration testing is essentially the accelerated testing of interconnects using heat and electrical current as the accelerating factors. In this study, electromigration tests are conducted at temperatures in a range from 250^{o}C to 350^{o}C. The accuracy of the oven temperature can be guaranteed since the temperature setting is calibrated using standard thermocouple (K-type) procedure. The offset value between the set and the standard measured temperature, which is obtained from the thermocouple, is compensated by using a polynomial equation. Table 2.1 shows the minor deviations between the set and the standard measured temperature, and the offset equation can be written as: $0.00012344x^2 + 0.99744059x + 0.17101501$, where x is the standard measured temperature. The square of polynomial term is included to enable a higher accuracy. The temperatures at the four corners of the oven are measured to verify thermal uniformity. The specification of the oven is within a 3^{o}C deviation. As in any accelerated testing, it is important to conduct the tests in a range of temperatures that allow for the same failure mechanisms that one might see at standard operating conditions (80 ^{o}C to 125 ^{o}C).

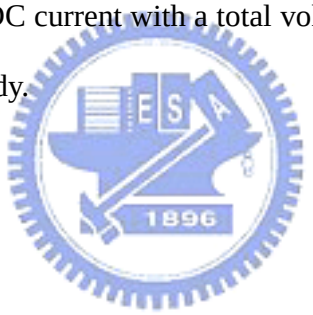
The supplied current can also be used as an accelerating factor during electromigration testing. The accuracy of the supplied current is verified by measuring the precision resistors. The test was started after the temperature within the oven was stable. The current were turned on and

the resistance was monitored. Figure 2.2(a) shows the error percentage of a 100 ohm precision resistor at a supplied current of 0.2mA for each device under test (DUTs), and the margin of error is less than 0.6%. The accuracy of the current meter is within a 1% deviation of the specification and current source resolution is 10 μA. Figure 2.2(b) shows the out resistance error percentage of 100 ohm precision resistor as the applied is 0.2mA for each DUTs, and the error is less than 0.8%. Reduced stress current densities in the range of 0.6 to $2.0x10^6$ A/cm^2 (defined with respect to the cross-section of the metal line) were used to limit any increase temperature due to Joule heating to a maximum of 3^oC, even for low-k materials known to possess small thermal conductivity [2.5]. Higher current densities will induce local Joule heating that can occur at the site of defects, or in thinned Cu sections, during electromigration testing. The impact of this local Joule heating is difficult to characterize. However, this issue does not seriously affect the work being discussed in this study.

Traditionally, Joule heating in electromigration testing has been quantified by measuring the metal line resistance at a relatively low current (i.e. the reference current), where the dissipated power and the related temperature increase were assumed to be negligible [2.6]. If the relationship is derived for the metal line resistance vs. temperature, the difference between the resistance measured at low current condition and the resistance measured under actual stress conditions (high current), respectively, can be easily translated into the actual metal line temperature under stress. Figure 2.4(a) illustrates the typical Joule heating calculation method. The Joule heating temperature can be obtained by subtracting the oven temperature from T_f. Unfortunately, the requirement of negligible Joule heating at low currents may result in significant resolution and noise related errors. In this work, the Qualitau^{TM} “two-current” method is used to extract the Joule heating value. The reference current can then be increased to a level where the corresponding accuracy is significantly improved. Measuring the resistance R(T) at several oven temperature values, using two selected current levels (one is stress current, the other

is reference current), enables the two related linear expressions to be established. If it is assumed that relationship between the R(T) and temperature is linear, a fitting line of the actual line temperature, in which the supplied current is extracted to zero, can be extrapolated. Figure 2.4(b) illustrates this “two-current” method, by which the actual temperature of metal line undergoing the electromigration test can be accurately determined.

Electromigration testing in this work was performed using the Qualitau^{TM} semiconductor reliability testing system. The Mainframe contains the circuitry that stresses the DUTs, and the associated data acquisition electronics. DUTs are plugged into Zero Insertion Force (ZIF) sockets on printed circuit boards (DUT boards), which, in turn, are connected to the EM modules via cable assemblies. The oven temperatures can range up to 350^{o}C with a N_2 ambient. The power supply module delivers a fixed DC current with a total voltage compliance of about 9 volts in the range of currents used in this study.



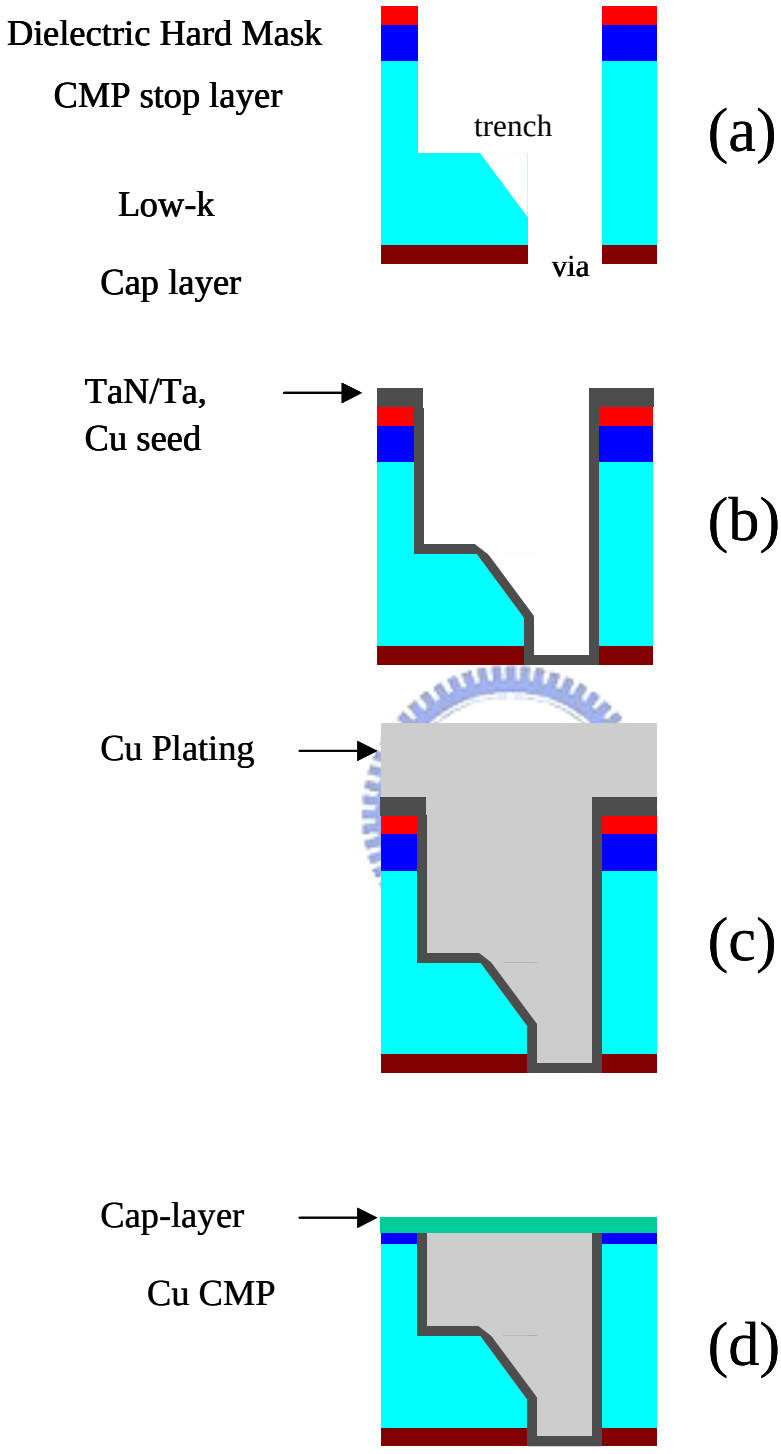
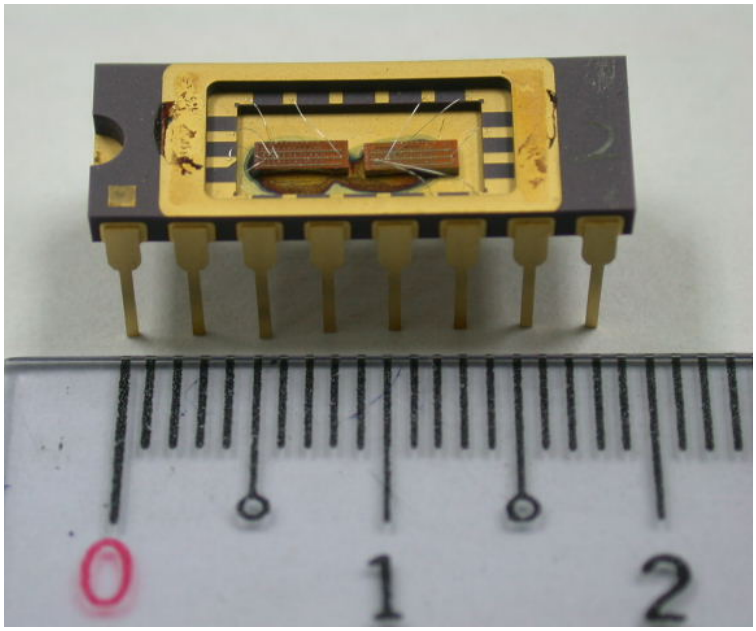
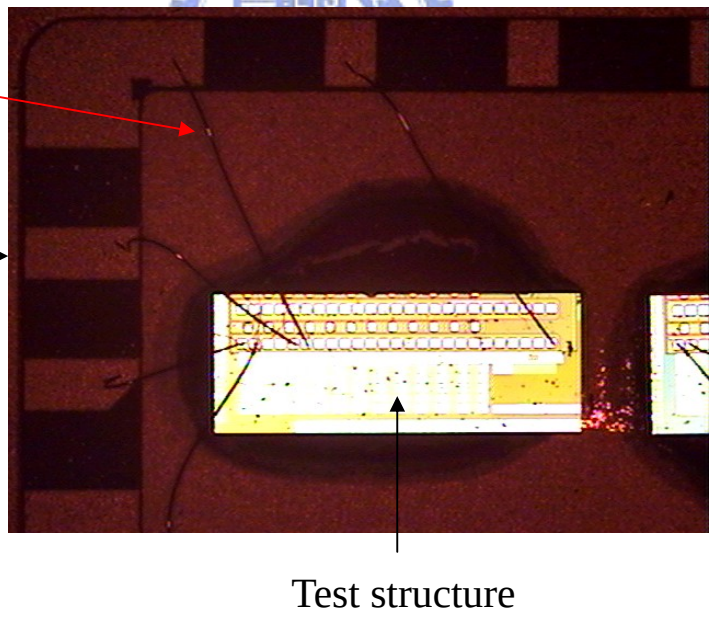


Fig.2.1 A schematic summarizes the major aspects of dual-damascene process. (a) The trench and via is patterned in ILD layer. (b) The barrier and Cu seed are deposited. (c) Cu is electroplated to fill the via and trench. (d) Recess Cu film is removed using CMP process and cap-layer is deposited.



(a)



(b)

Fig.2.2 (a) A top-down picture of 16-pin dual inline package. (b) Zoom-in the package, the wirebonds are used to connect to the bond posts of the package to the bond pads of the test structure.

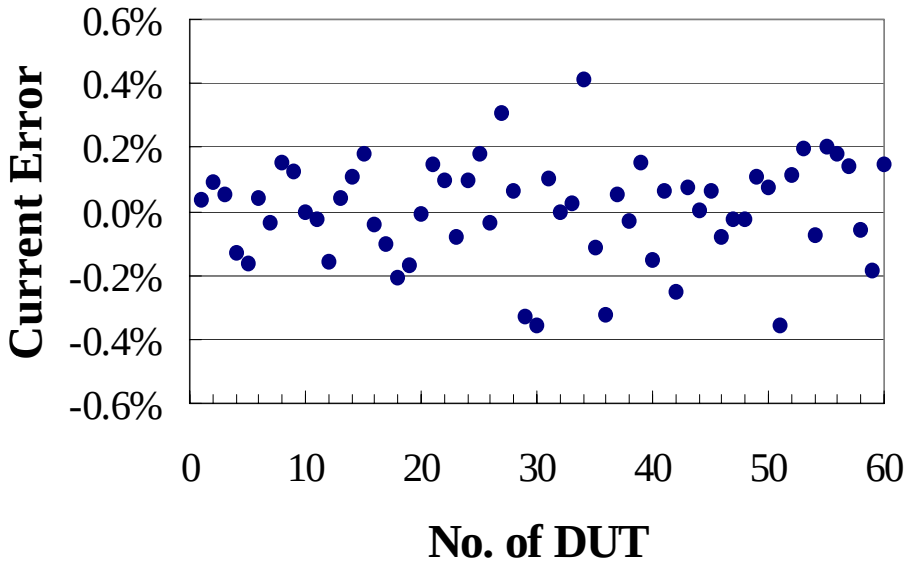


Fig.2.3(a) The error percentage of 100 ohm precision resistor as the applied is 0.2mA for total devices under test (DUTs), and the error is smaller than 0.6%.

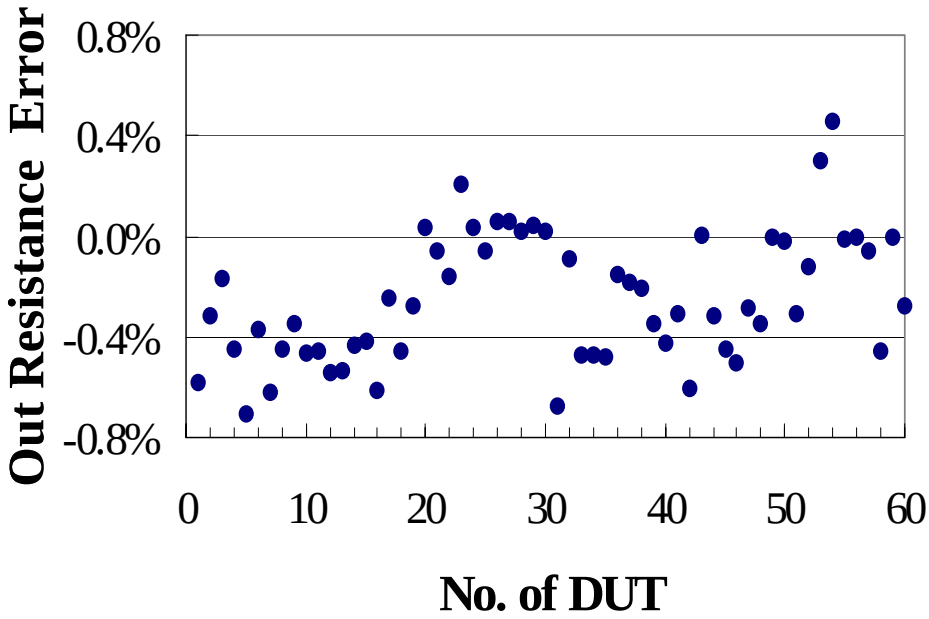


Fig.2.3(b) The out resistance error percentage of 100 ohm precision resistor as the applied is 0.2mA for total devices under test (DUTs), and the error is smaller than 0.8%.

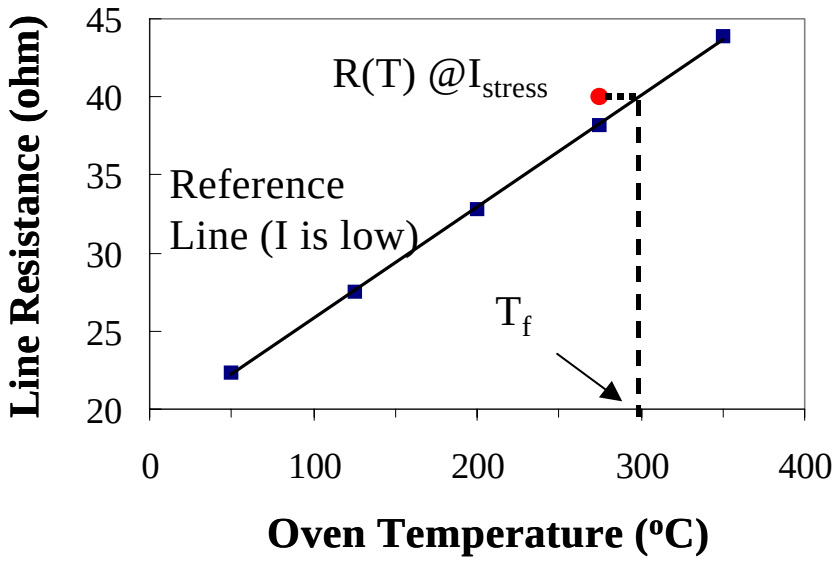


Fig.2.4(a) Illustration the typical Joule heating calculation method. Reference line is obtained, as the current is relatively low. R(T) point is the measured resistance as stress high current. Joule heating temperature can be obtained from T_f minus oven temperature.

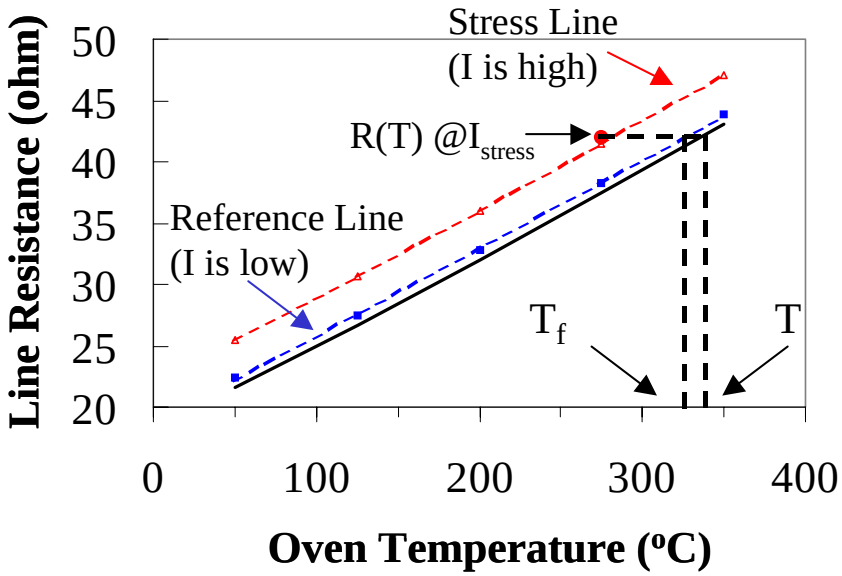


Fig.2.4(b) Illustration the “two-current” typical Joule heating calculation method. Black solid line is actual temperature of metal line with zero applied current. Joule heating temperature is T minus oven temperature.

Table.2.1 Illustrates EM oven temperature accuracy verification. Standard measured value is obtained from the calibrated thermocouple. The temperatures at four corner of the oven are measured to verify the thermal uniformity.

		100℃		**150℃**		**200℃**	
Oven Location	Thermal-couple Sensor No.	Standard measurement	Setting value	Standard measurement	Setting value	Standard measurement	Setting value
Right-up	B18436	100.8	100	150.4	150	200.6	200
Right-down	B18430	100.6	100	150.7	150	201.0	200
Left-up	B18438	100.3	100	149.9	150	200.1	200
Left-down	B18428	99.9	100	149.6	150	199.1	200
		250℃		**300℃**		**350℃**	
Oven Location	Thermal-couple Sensor No.	Standard measurement	Setting value	Standard measurement	Setting value	Standard measurement	Setting value
Right-up	B18436	251.6	250	301.6	300	351.5	350
Right-down	B18430	251.8	250	301.1	300	351.0	350
Left-up	B18438	250.7	250	300.4	300	350.2	350
Left-down	B18428	249.8	250	299.5	300	349.8	350

Fitting equation: $0.00012344x^2 + 0.99744059x + 0.17101501$, where x is the standard measurement temperature.

Chapter 3

Copper Interconnect Electromigration Behavior in Various Structures and Precise Bimodal Fitting

3.1 Preface

The EM reliability issue has been very important in interconnect technology since Al thin film wires were found to exhibit EM in 1966. Over the past 40 years, Al has been the interconnect conductor of choice in the microelectronic industry. The drive toward improved chip performance has resulted in a rapid push toward greater circuit density. Higher circuit density is a consequence of shrinking wire dimensions. This aggressive wire dimension scaling has resulted in an increase in current density. The probability of circuit failure induced by EM increases when current density increases. The back-end-of-line (BEOL) RC delay has gradually become a major limiting factor in circuit performance as a result of the rapid shrinking of critical dimensions. With reduced resistivities and dielectric constants, the metallization system for the interconnect structures has shifted from Al(Cu)/oxide to copper/low-k dielectrics. The reliability of Cu/low-k interconnects thus has become an important topic in 0.13 μm technology node and beyond [3.1]. Cu electromigration reliability is the key issue that limits the lifetime of advanced interconnect systems [3.2]. The rapid decrease in Cu conductor dimensions while maintaining a high current capability and a high reliability emerges as a serious challenge.

Many studies have been investigated to optimize Cu electromigration performance. Process improvements are necessary to increase EM performance, while some geometric features of the testkey design also play a significant role in EM. However, few studies have shown the effect of the various test structures on EM performance. In this work, we demonstrate systematical analyses to identify the weak link of copper interconnects, and then evaluate precise bimodal

fitting methods.

In chapter 3, following the successful integration of Cu/low-k BEOL processes, package level electromigration tests have been performed using various low-k materials in order to compare the performance and verify the stability of the Cu dual-damascene process. Various stress conditions for a number of structures were studied enable an understanding of the failure modes and to identify the weak links in an interconnect system. In addition to a well-understood failure mechanism [3.3-3.9], a precise lifetime prediction methodology is essential to describe the circuit degradation due to electromigration damage. The log-normal distribution is widely used to model the EM failure time distribution. Because of the multi-modality failure mechanism observed in dual-damascene Cu interconnects [3.10-3.14], a single log-normal distribution is no longer suitable to describe the time-to-failure distribution. The multimodality distributions were verified by failure analysis. The predicted lifetimes of each model determined by manually distinguishing different failure modes (physical method) were compared with lifetimes calculated using superposition and weak-link models. Various methods of data analyses for multimodal EM failure are presented.

3.2 Experimental Detail

Using 0.13 μm node BEOL technology and beyond, the electromigration behavior of dual-damascene Cu interconnects was compared among three different low-k inter metal dielectrics (IMDs): a spin-coated aromatic hydrocarbon thermosetting polymer (SOD, k=2.65), a chemical-vapor-deposited SiOC (k=2.7) and fluorosilicate glass (FSG, k=3.6). The TaN/Ta liner and Cu seed layers were deposited sequentially using physical vapor deposition (PVD). Test structures under evaluation included conventional NIST [3.15] metal lines, via terminated metal lines, and via chains of various geometry. The schematics are shown in Figs. 1(a)-(c), respectively. EM tests were carried out at the package level. The sample size per EM test was greater than 20.

Stress temperatures were in the range of 250 to 350^{o}C (typically 300^{o}C). Reduced stress current densities in the range of 0.6 to 2.0x10^{6} A/cm^{2} (defined with respect to the cross section of the metal line) were used to control the temperature rise due to Joule heating to less than 3^{o}C even for low-k materials known for possessing small thermal conductivity. Testing was conducted typically at 300^{o}C at a current density of 1.6x10^{6} A/cm^{2}. The relation between metal resistance and temperature is given by TCR(T) = [1/R(T)] ΔR/ΔT, where TCR is the temperature coefficient of resistance, R is the resistance, and T is the sample temperature. TCR was determined by resistance measurements in steps of 50^{o}C in the range from 50 to 300^{o}C. The correlation between R and T within the investigated temperature range was close to linear. For via-terminated metal lines, two applied stress current directions were investigated called “downstream”, defined for the electron flow from the upper wide metal line over the via into the under narrow metal line, and “upstream”, defined for the electron flow from the lower wide metal line over the via into the upper narrow metal line. The EM failure criterion is defined as 20% of the resistance increase or when the extrusion monitor current exceeds 1 μA. The failure site is identified by optical beam induced resistance change (IR-OBIRCH) technique. Abnormal resistance sites in test structures were detected. This technique was especially useful in finding failure spots in the case of via chains.

3.3 Results and Discussion

3.3.1 EM performance of various structures and weak link of interconnect system.

Various EM test structures were designed to evaluate the EM performance and the weak link of the interconnect system. It will be useful to classify this section into three types according to structure. We begin with a discussion of pure metal line EM performance and the width effect. Next, we discuss stress current direction and the failure mode in via-terminated structures. Finally, the weak link of the copper interconnect system is examined.

3.3.1.1 Pure metal line EM performance and width effect.

The pure metal line NIST structure is used to eliminate via-related processing issues. The structures are made at a single level and designed to have the test lead connected with a wide lead at each end. The EM behavior of Cu metal lines can be evaluated. However, due to the large Cu reservoir, the time to failure of the NIST line structures is orders of magnitude higher that those for via-associated metal lines. The Median time to fail (MTFs) of single-damascene metal 1 (M1) and dual-damascene metal 2 (M2) of various widths are shown in Fig. 2(a). MTF decreases as line width increases in the range below 1 μm, unlike that in the previous work [3.16], which reported that EM lifetime decreases as line width decreases. The line width dependence observed in this study is totally different. Before explaining this issue, one basic metal microstructure characteristic must be examined. The temperature coefficient of resistance (TCR) has been used as a parameter to qualitatively monitor the Al metal properties [3.17]. TCR values have been investigated with regard to median grain size and defects in the crystal lattice, respectively. High TCR values indicate large median grain sizes, whereas low TCR values correspond to a fine-grained microstructure. The correlations between TCR and both the microstructure and the stress-voiding behavior of copper interconnects were comprehensively investigated in a previous work. The TCR value was found to decrease with line width as in Fig. 2(b). Since the grain size in the narrow submicron region is finer grained microstructure than that in the wide metal line, the narrow line is expected to exhibit a higher grain boundary density. The probability of grain boundary diffusion in the narrow line is supposed to be higher than that in the wide line. The EM lifetime of a narrow line may be shorter than that of wide line; however, the anticipated EM performance conflicts with the experimental results. Two aspects suggest possible mechanisms for EM behavior of NIST line structure. One is that more samples with extrusion leakage failure were found in the wide line. The spacing between the metal line and the extrusion monitor line is

designed using the minimum allowable rule for various metal widths. As the metal width is larger than that suggested by the minimum spacing allowable rule, wide metal line will induce more Cu atoms to extrude than that of a metal width equal to the spacing, and the probability of extrusion failure on a wide line is higher than that on a minimum line. The other is the Cu reservoir effect on EM. Reservoirs are metal parts that act as a source to provide atoms to areas where the atoms migrate away due to electrical current. The use of such reservoirs can prolong EM lifetime; this is called the “reservoir effect”. The reservoir Cu volume for a width =0.16 μm is approximately 1.4 times that for a width=0.56 μm. The large reservoir volume increases the MTF of width =0.16 μm compared with that of width=0.56 μm. Consideration of the reservoir effect should play a role in designing the NIST structure.

To minimize the reservoir effect, single and repeated serial via chains of interconnects have been designed. Various via chain structures have been examined to identify the weak link of the interconnect system and assess the influence on failure distribution. For via-terminated metal line structures, two stress current directions can be applied: “downstream”, defined as electron flow from the upper wide metal line over the via into the under narrow metal line; and “upstream”, defined as electron flow from the lower wide metal line over the via into the upper narrow metal line. It is desirable to examine the stress current direction dependence of EM before evaluating the EM behavior of various via structures.

3.3.1.2 Stress current direction and failure mode in various via-terminated structures.

The current direction of the EM test had a marked effect on EM results in the via-terminated metal line structure and related failure mode. In addition, different dual-damascene process approaches and EM structures lead to different EM behavior. EM samples were fabricated using two process strategies. For the first process approach, a nearly vertical via profile was obtained [3.18]. Figure 3 shows the representative cumulative lifetime

plots stressed under both upstream and downstream electron flows. Comparable time-to-failure distributions were achieved after process optimization for each low-k material. Similar failure-time distributions for both stress directions were also shown. It is interesting to note that the distribution was no longer log-normal, especially in the case of upstream stress, as indicated by the poor fit, while the log-normal function still describes the typical downstream case. As shown in Fig. 4(a), two types of resistance change vs. stress time degradation behavior, namely instantaneous failure and long-lasting failure, were observed in the upstream case; however, in the downstream case, the resistance change vs. time curves look similar to long-lasting failure in upstream case plotted in Fig. 4(b). Extensive failure analysis was carried out to explain the root causes. Figure 5(a) shows the failure analysis results in the upstream case. Voiding inside the upstream stressed via was the major mechanism for instantaneous failure. On the other hand, voiding along metal lines is the predominant mechanism of long-lasting failure, though via depletion is occasionally found in conjunction with line voiding. The small amount of Cu depletion around the via/metal interface causes large resistance changes. In contrast, a very large amount of Cu depletion in metal lines was found at long time-to-fail (TTF) points. Two distinct failure modes were identified in the upstream stress cases. As a result, via depletion is the dominant factor in upstream cases due to short TTF points compared with the metal depletion mode. However, in the case of downstream stress, the failure mode involves voiding along the underlying metal lines, with the majority of voids initiated at the bottom of the via interface to the underlying metal, as shown in Fig. 5(b). Therefore, multimodality electromigration was found in the upstream case, while nearly single-mode EM was shown in the downstream case.

For the second process approach, a tapered via profile was obtained. The diameter of the via top was larger than that of the via bottom. The upstream stress showed a much better EM lifetime than the downstream case shown in Fig. 6. SEM images at different failure time points are shown in Figs. 7(a) and 7(b). The trench depletion failure mode was observed in the upstream

case, where a small amount of Cu depletion was observed for a short TTF point, while a large amount of Cu depletion correlated to a long TTF point. Two failure modes were found in the downstream case in the second process approach; in contrast, as we have seen, a bimodal distribution was shown in the upstream case in the first process approach. A possible mechanism has been proposed. Comparing this to the vertical via profile, it is easier to establish a uniform liner coverage on the via sidewall for a tapered via profile. A large volume of Cu compared with that required by the vertical via must be depleted to reach resistance failure criteria. In this case, a good liner coverage suppresses Cu diffusion, and via depletion is alleviated in the upstream case. However, for the downstream case in Fig.7(b), two failure modes corresponding to voiding in the via/metal interface and trench depletion were found. Via depletion was related to a short TTF that was actually much shorter than that in the upstream case. A small amount of Cu depletion around the via/metal interface can cause a large resistance change and requires a much shorter time to cause via depletion than trench depletion. For the trench depletion mode in the downstream case, the TTF and the volume of Cu depletion were very close to that in the upstream case. Both stress directions indicated the Cu diffusion velocity was almost the same for identical trench depletion conditions. Another failure mode of via depletion was observed in the case of downstream stress. In summary, EM failure mode correlates closely with process approach. We need stress two applied current directions, and then determine the applied direction causing worse case of EM. Using a via terminated structure with a single via, the downstream case is a good approach to study, to evaluate not only the worst case of the Cu cap-layer interface but also for the process integration of the via bottom interface. On the other hand, the upstream case is used to evaluate the gap filling of via. A poor filling process leads to void formation in via. This voids cause the early failures after stress upstream, and then degrade the EM lifetime.

3.3.1.3 Weak link of copper interconnect system.

We then attempted to expand the single via into a serial via chain structure. We evaluated the weak link of the copper interconnect system. The cumulative lifetimes of a minimum allowable rule 30-via chain and a single via terminated metal line in both stress directions are compared in Fig. 8(a). The MTFs of 30-via chain, an upstream single via, and a downstream single via structures are 90.6, 147.4, and 320.4 h, respectively. A bimodal distribution was clearly observed for the upstream single via-terminated case, where the probability of instantaneous failure is approximately 40%. For a 30-via chain in which 15 vias are stressed upstream, the probability of instantaneous failure is almost 100%, resulting in the lowest lifetime among all three structures. This also means that the upstream stressing is weaker than the downstream case. The TTF of the 30-via chains is very close to the TTF of the instantaneous failure mode in the upstream case. Figure 8(b) (left) shows such instantaneous failure in the resistance vs. stress time plot. The failure site localization on a 30-via chain structure was identified by the IR-OBIRCH technique. Abnormal resistance sites in test structure were detected. Figure 8(b) (right) showed IR-OBIRCH images. The high resistance sites marked by red spots are located only in the same stress current direction. The instantaneous failure mode in the 30-via chain was confirmed.

Thirty-via chains with different metal line widths were used to identify the weakest link of the interconnect system. It was found that a via connected to an underlying minimum width line was the worst case during downstream stress, followed by upstream stress to an overlying minimum width line. Figure 9(a) shows TTF plots of two kinds of via-chains. The widths of M1/M2 links in Chains A and B are 0.16 μm/3 μm and 3 μm/0.2 μm, respectively. Physical failure analysis indicates that the voiding always happened in an upstream via connected to an underlying line of minimum allowable width for Chain A (Fig. 9(b) left) and below a downstream via with an overlying the minimum allowable width line for Chain B (Fig. 9 (b) right). The

suppressed lifetime of chain A is attributed to the reduced depleted volume in the underlying minimum width links. Vias connected to minimum width lines (above/below) were found to be the weakest links of the dual-damascene interconnect system.

3.3.2 Practical method of bimodal fitting.

A precise methodology for reliable lifetime prediction is essential to describe circuit degradation due to electromigration damage. The reliability lifetime of an interconnet system is derived from EM stress data under the assumption of single failure mode. Since the multi modality failure mechanism extends the failure time distribution, relatively low projected lifetimes arise from the shallow slope of the curve of failure time distribution. Consequently, a reasonable fitting method is necessary for precise projected lifetimes. It is desirable to separate the different failure modes from EM stress data and then project lifetimes for each failure mode. Because of the multi modality failure mechanism observed in dual-damascene Cu interconnects, a single log-normal distribution is no longer suitable to describe the time-to-failure distribution. On the basis of this conclusion, two bimodal models, superposition and weak-link, were used to describe the failure behavior. The superposition model eq. 3.1 consists of five parameters expressed to describe the failure distribution. The weak-link model consists of four parameters as shown in eq. 3.2 and is used to describe the same failure distribution.

$$CDF(t)=P(A)xCDF_A(t)+(1-P(A))xCDF_B(t) \quad .(3.1)$$

$$CDF(t)=CDF_A(t)+CDF_B(t) - CDF_A(t)xCDF_B(t) \quad .(3.2)$$

Where CDF is the cumulative density function, and P(A) is the probability of one failure mode A. The Levenberg-Marquardt iteration is applied to the nonliner regression for both models. Table I summarizes the five parameters [P(A), MTF_A, σ_A, MTF_B, and σ_B] of the superposition model extracted by iteration fitting. A good agreement as shown in Fig. 10(a) was achieved as indicated by R^2=0.991(coefficient of determination). The same data was fitted by the weak-link model. The

fitting results are listed in Table I. Four parameters [MTF_A, σ_A, MTF_B, and σ_B] were extracted by iteration fitting (R^2=0.987) as in Fig. 10(b). Results from both methodologies, the superposition and the weak-link, were compared with the outcomes of the physical method. In this method, according to resistance change vs. time plot, the samples were manually grouped into two failure categories: instantaneous failure and long-lasting failure. Then a log-normal distribution was used to describe each group. As indicated in Fig. 11, each failure mode follows a log-normal distribution. The corresponding median-time-to-failure (MTF) and shape factor (sigma) were obtained. The fractions of instantaneous failure and long-lasting failure can be calculated by counting the number of failure modes. The fitting results of statistical methods with those data from the physical method are summarized in Table 3.1. As Table I indicates, MTF and sigma obtained from the superposition are close to those parameters from the physical method. These data suggest that the superposition method is better for simulating failure behavior in advanced Cu/low-k interconnect systems. The same methodology was carried out on samples produced from various Cu/low-k IMD materials. The different percentages of the two failure modes were calculated for in various Cu/low-k combinations. Table 3.2 lists key parameters of each IMD material obtained both by statistical and physical fitting methods. In spite of the large variation in the percentage of the two failure modes among the three IMD cells, good agreements were achieved between the physical and statistical fitting methods in terms of the failure percentage range. Accumulated Cu/FSG lots were examined to further confirm the bimodal EM behavior. When the sample size was increased, the uncertainties obtained for each parameter decreased. The large sample size of multiple lots is expected to improve the confidence interval. The results of each individual lot and all three lots were in good agreement from both the superposition fitting and the physical method, as shown in Table 3.3. The bimodal behavior is still clear in mixed data. A good agreement is shown in Fig. 12.

The kinetics of two failure modes was also studied. The medium time to failure (MTF) of

various stress temperatures and currents was determined separately for each mode by fitting the bimodal distribution. The activation energies of instantaneous and long-lasting failures were calculated to be 0.86 and 0.74 eV, respectively, as shown in Fig. 13. The discrepancy is attributed to the difference in the diffusion path. Because long-lasting failure resulted from line depletion, cap SiN/Cu interface with a relatively low Ea became the predominant diffusion path. The higher Ea of instantaneous failure was then attributed to the high Ea of the Cu/Ta interface leading to predominant via-depletion fail. The current exponents of instantaneous and long-lasting failures were calculated as 1.1 and 1.2, respectively, as shown in Fig. 14. These values are in good agreement with those resulting from the void growth mechanism of the Cu dual-damascene interconnect.

3.4 Summary

In conclusion, copper interconnect electromigration performance was demonstrated in various structures and three low-k materials (k= 2.65 ~ 3.6) using advanced BEOL technology. For pure line NIST structures, the MTF of single-damascene M1 and dual-damascene decreases M2 as line width increases in the range below 1 μm. For a via-terminated metal line structure, the current direction of the EM test was found to have a strong effect on the EM and related failure mode. In addition, different process approaches will lead to different EM behaviors. Voiding inside or under a stressed via was the major mechanism of instantaneous failure. On the other hand, voiding along metal lines is the predominated failure mechanism for long-lasting failure. The cumulative lifetimes of a minimum allowable rule 30-via chain and single via-terminated metal lines in both stress directions were also examined. For a 30-via chain in which 15 vias are stressed upstream, the probability of instantaneous failure is almost 100%, resulting in the lowest lifetime among all the three structures. The TTF of 30-via chain is very close to the TTF of the instantaneous failure mode in the upstream case. A via connected to a minimum width line

(above/below) was found to be the weakest links of the dual-damascene interconnect system. The lifetime prediction for samples with bimodal EM behavior was carried out by physical and statistical fitting methods. The TTF of each individual group was plotted as a log-normal distribution, then the corresponding MTF and shape factor were calculated. The same TTF data were also analyzed statistically using superposition bi-modality models. The activation energies of instantaneous and long-lasting failure were calculated to be 0.86 eV and 0.74 eV, respectively. The discrepancy is attributed to the difference in diffusion path. The current exponents of instantaneous and long lasting fails was calculated as 1.1 and 1.2, respectively. The good agreement between the two statistical approaches provides us with the possibility of precise lifetime prediction in a practical manner.

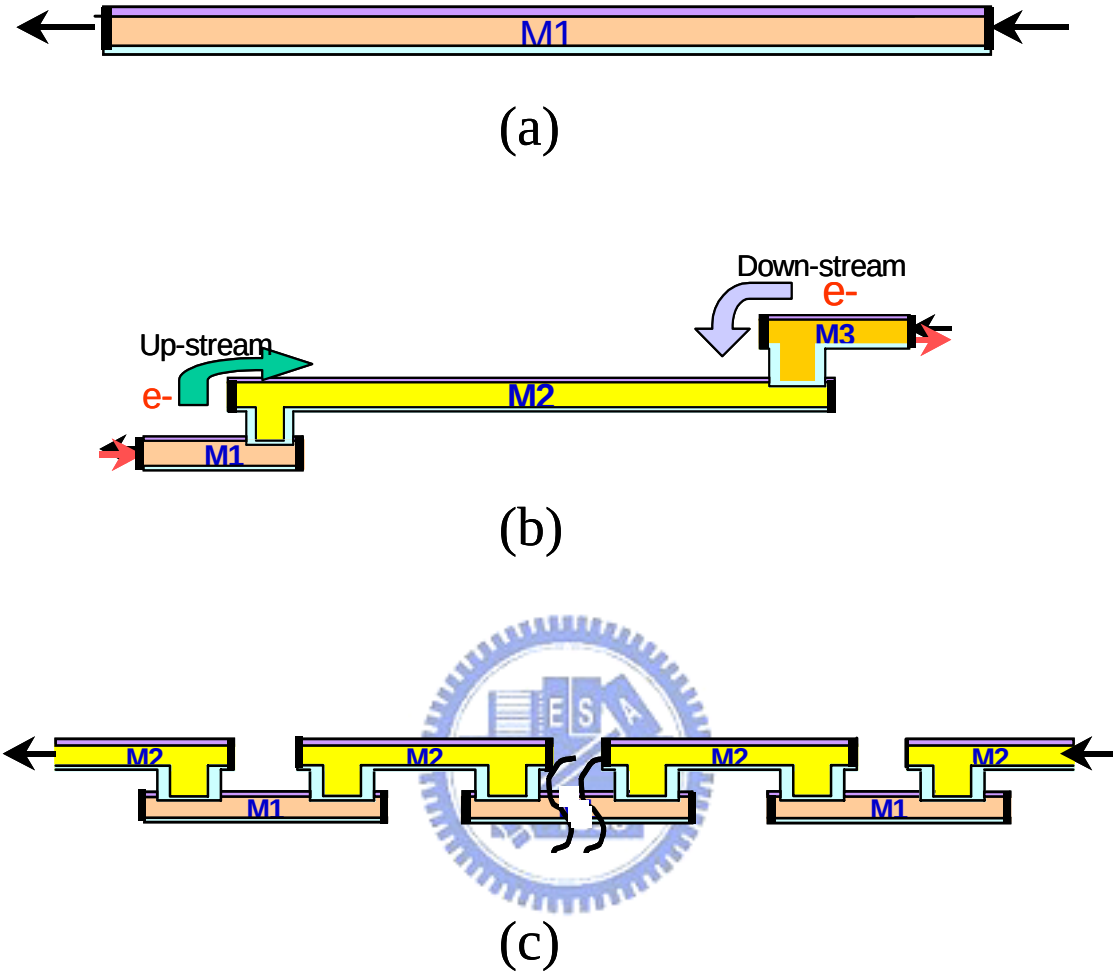


Fig.3.1 Schematics of EM test structures used: (a) NIST line. (b) via-terminated line, and (c) 30-via chain. The stress direction is defined by electron current flow direction.

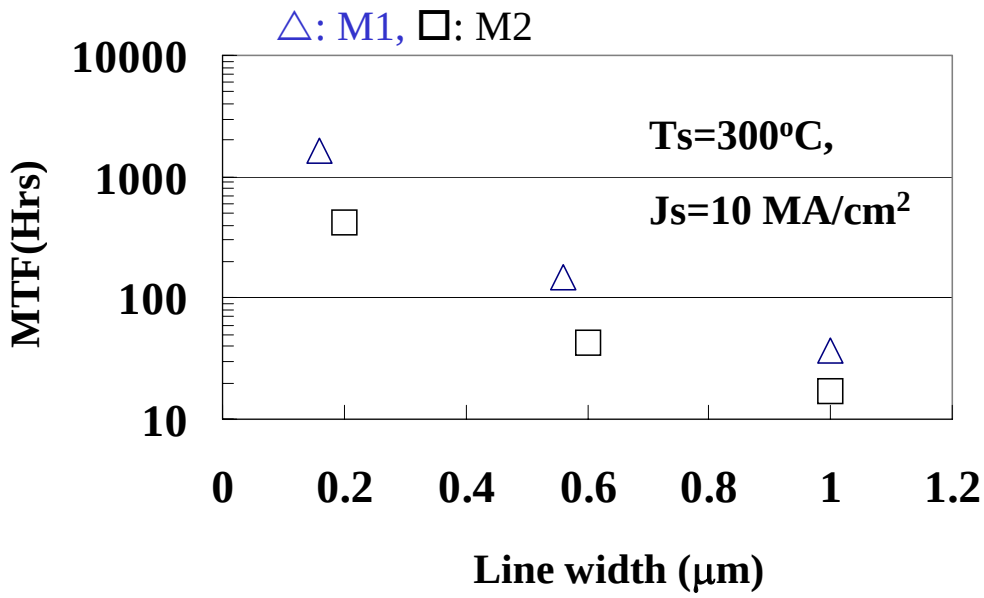


Fig.3.2(a) MTF as function of line width for Cu single- and dual-damascene lines with J=10x10^6 A/cm2 at 300^{o}C. Cu/SiOC low-k material is used.

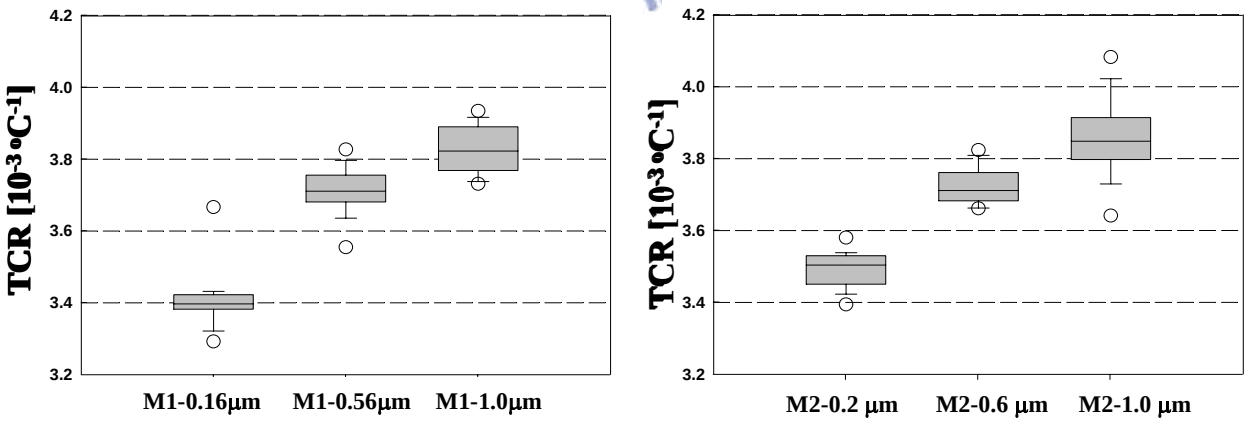


Fig.3.2(b) TCR value as function of line width. Left: M1, right: M2.

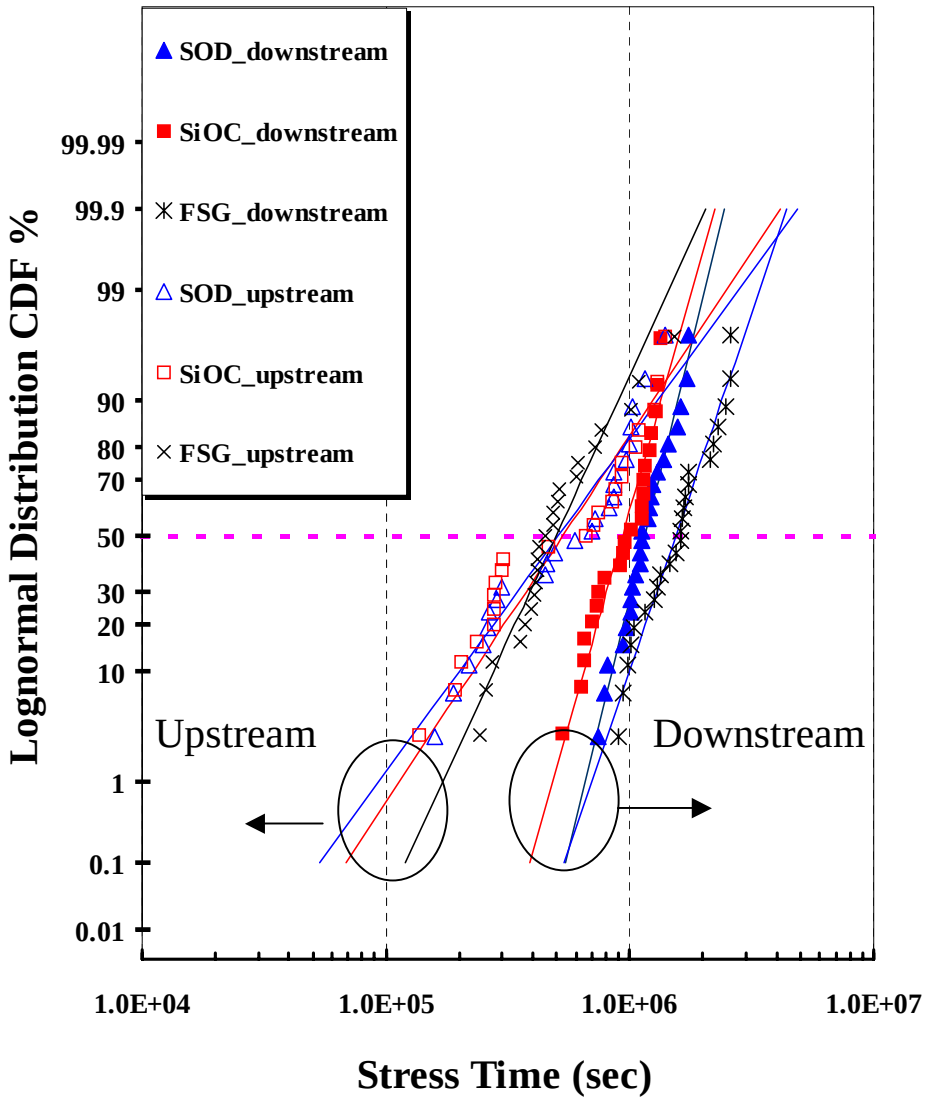
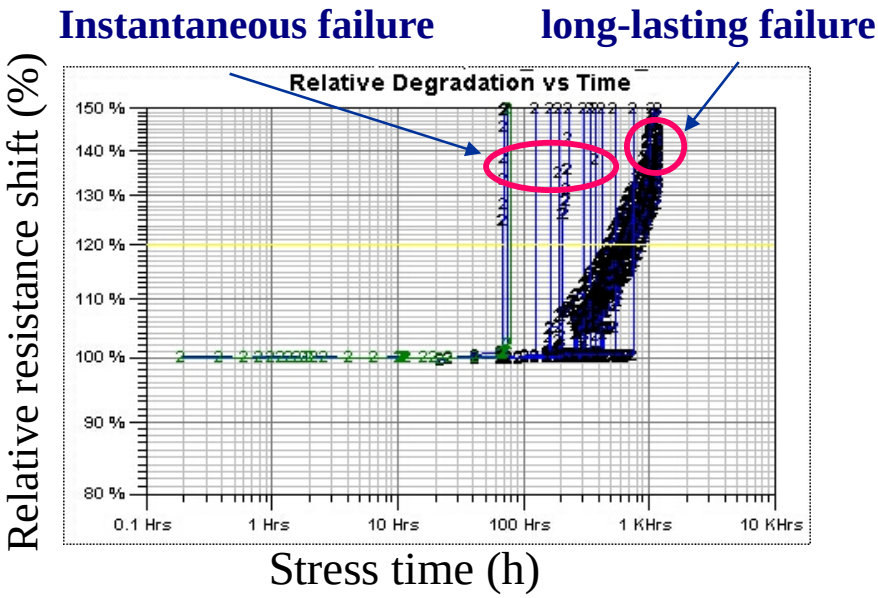
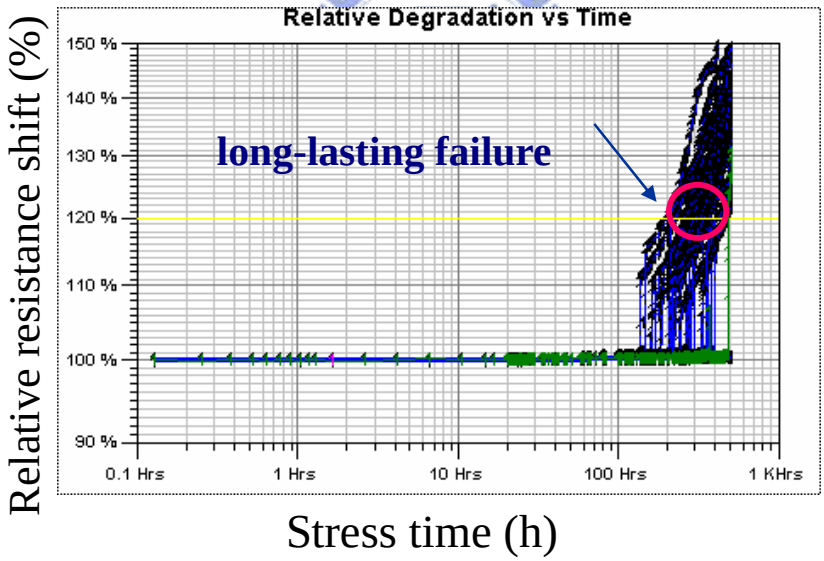


Fig.3.3 Typical time-to-failure distribution plots for upstream and downstream cases. The sample size is greater than 20 for upstream/downstream cases. Multimode was observed in the upstream, while a single log-normal function describes the typical downstream case. EM failure time were obtained at 300^{o}C under a current density of 1.6x10^{6} A/cm^{2}. The stress conditions are the same for all tests.

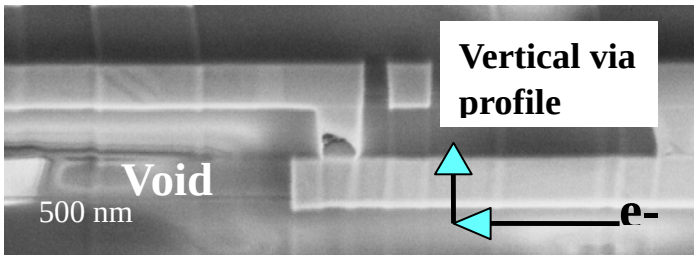


(a) dR/R vs. time plot for the up-stream case.

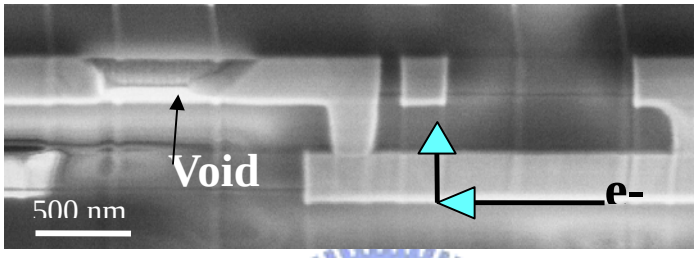


(b) dR/R vs.. time plot for the down-stream case.

Fig.3.4(a) Relative resistance vs. time degradation plots for (a) upstream case and (b) downstream case. Two different modes of degradation behavior are indicated in the upstream case, while only a long-lasting failure mode was found in the downstream case. Cu/FSG low-k material was used for this case.

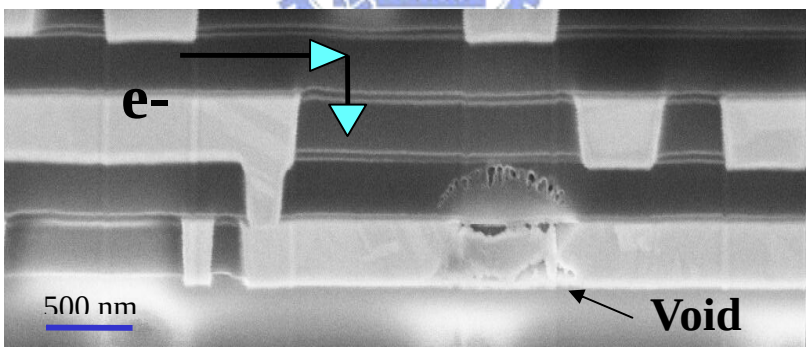


Instantaneous failure. (Up-stream case)



Long-lasting failure. (Up-stream case)

(a)



Long-lasting failure. (Down-stream case).

(b)

Fig.3.5 SEM image of representative upstream case (a) instantaneous failure (above); long-lasting failure (below). (b) SEM image of representative downstream failure site.

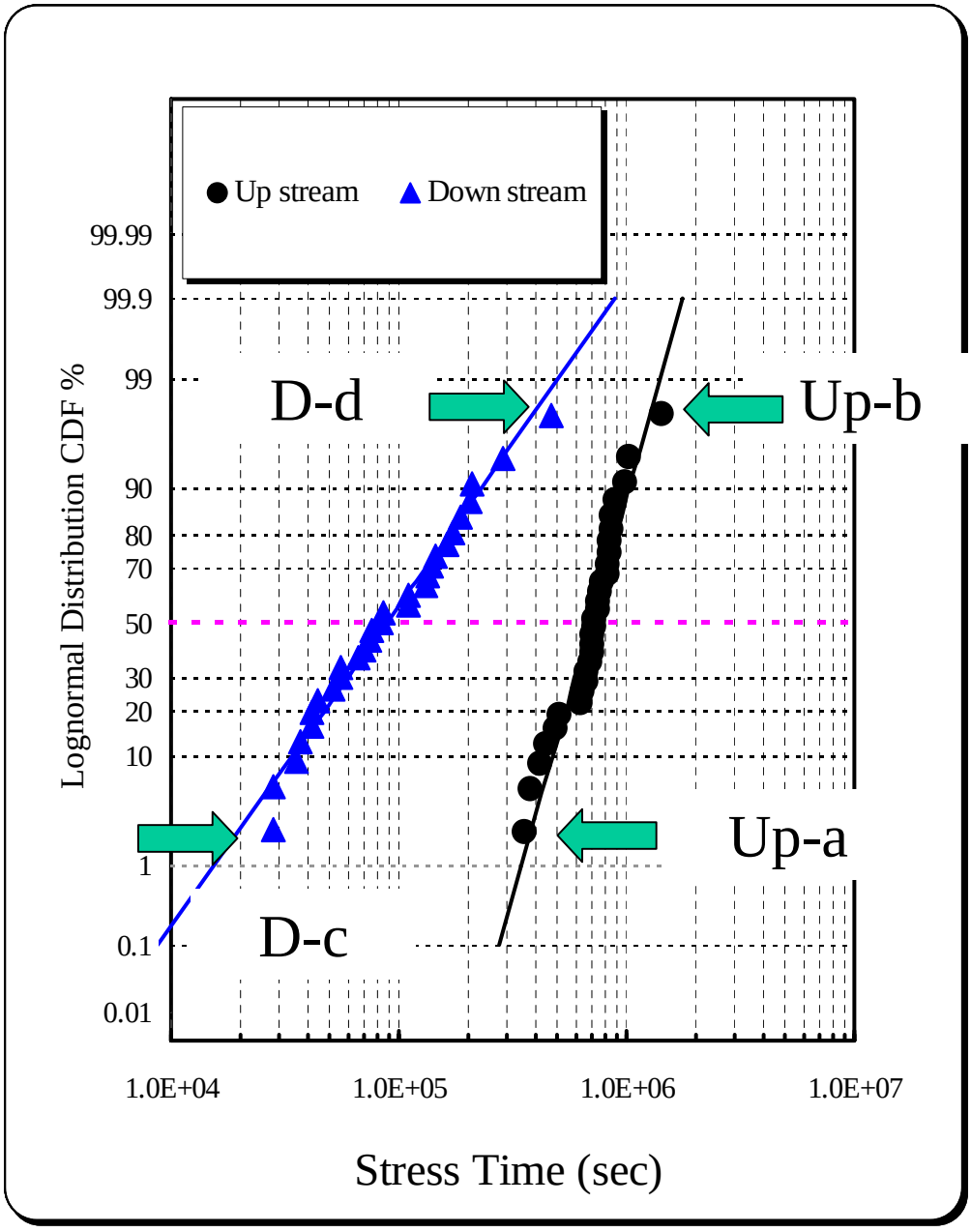
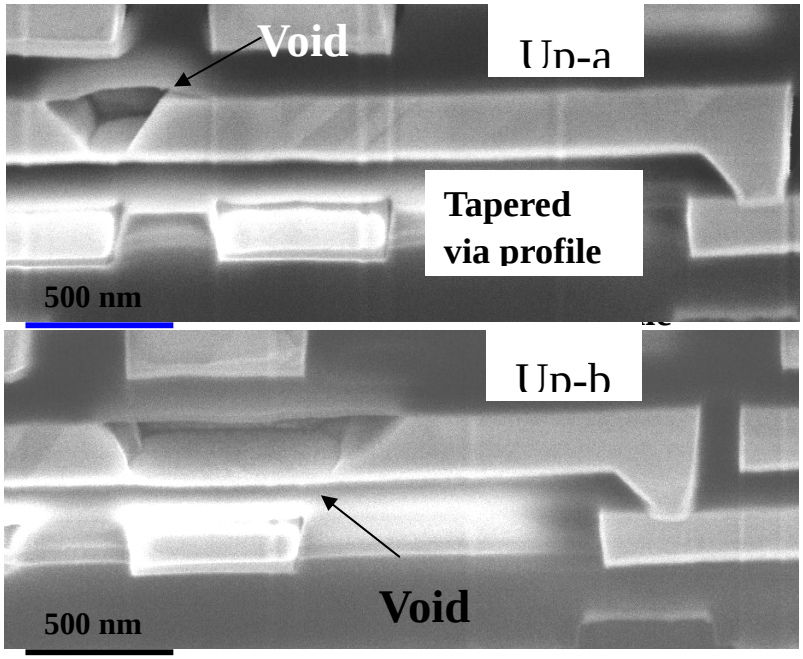
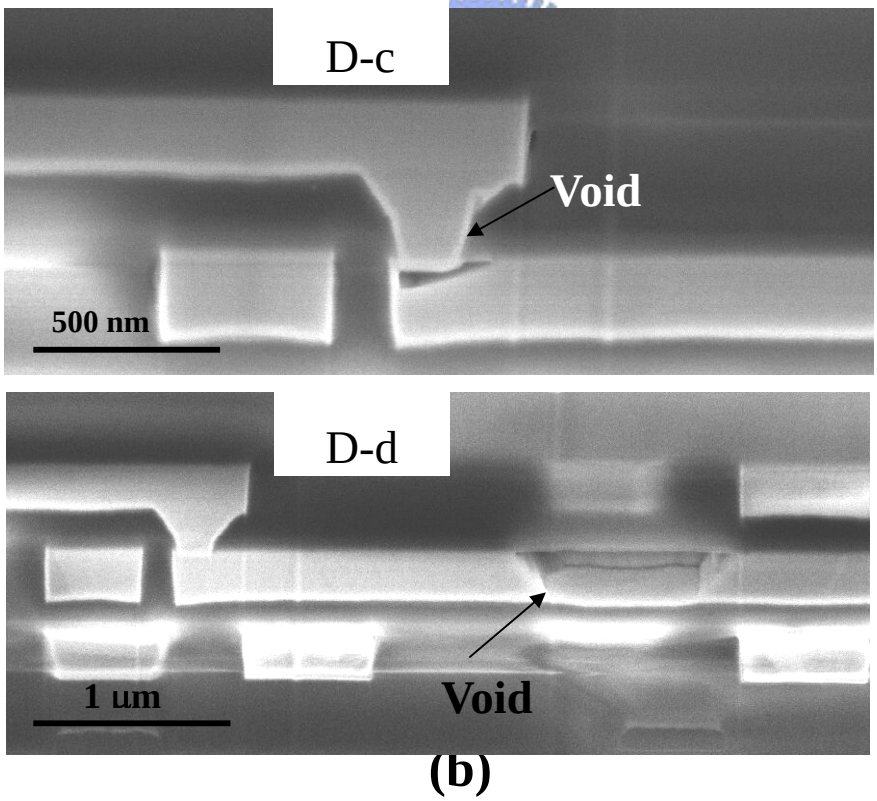


Fig.3.6 Log-normal time-to-failure distribution plots for upstream and downstream cases. EM failure time determined at 300^{o}C under current density of 1.6x10^{6} A/cm^{2} for two cases. The upstream case shows much better EM performance than the downstream case. The sample size is 30/29 for the upstream/downstream cases. MTF=193.8 h, σ = 0.3 for upstream; MTF=24.6 h, σ = 0.74 for downstream case. The samples chosen for physical failure analysis were indicated. Data shown here are for Cu/FSG low-k material.



(a)



(b)

Fig.3.7 (a) In the upstream stress case, SEM images show trench depletion. Up-a and Up-b show different TTFs indicated in Fig. 6. (b) In the downstream stress case, SEM images show voids in the via/metal interface and trench depletion. D-c and D-d show different TTFs indicated in Fig. 6..

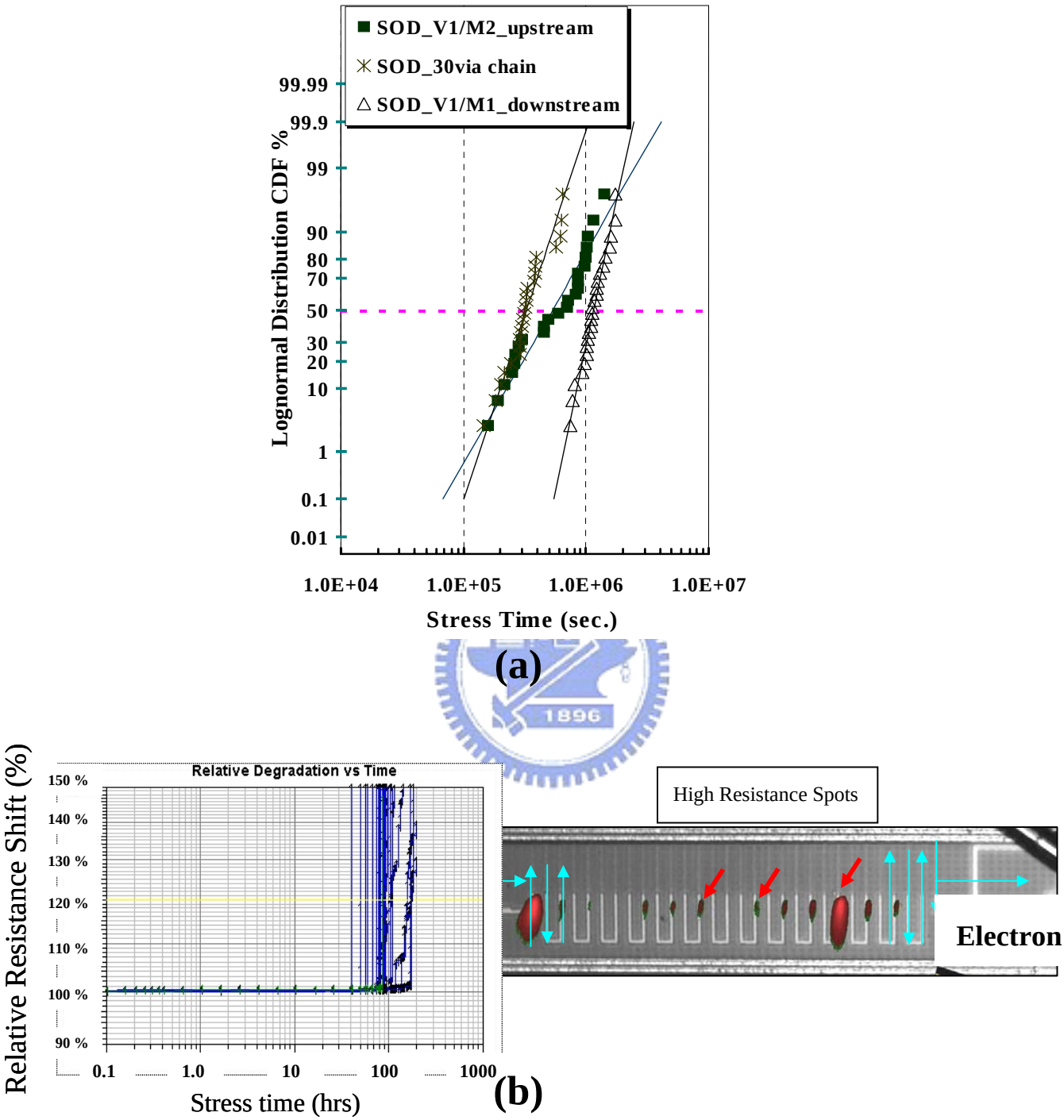


Fig.3.8 (a) Cumulative lifetime of minimum allowable rule 30-via chains and single-via terminated metal lines in both stress directions. Data shown here are for Cu/SOD interconnect. (b) Left: 30-via chain resistance change vs. stress time. Right: IR-OBIRCH image indicates that the high resistance spot is located in the same stress current direction.

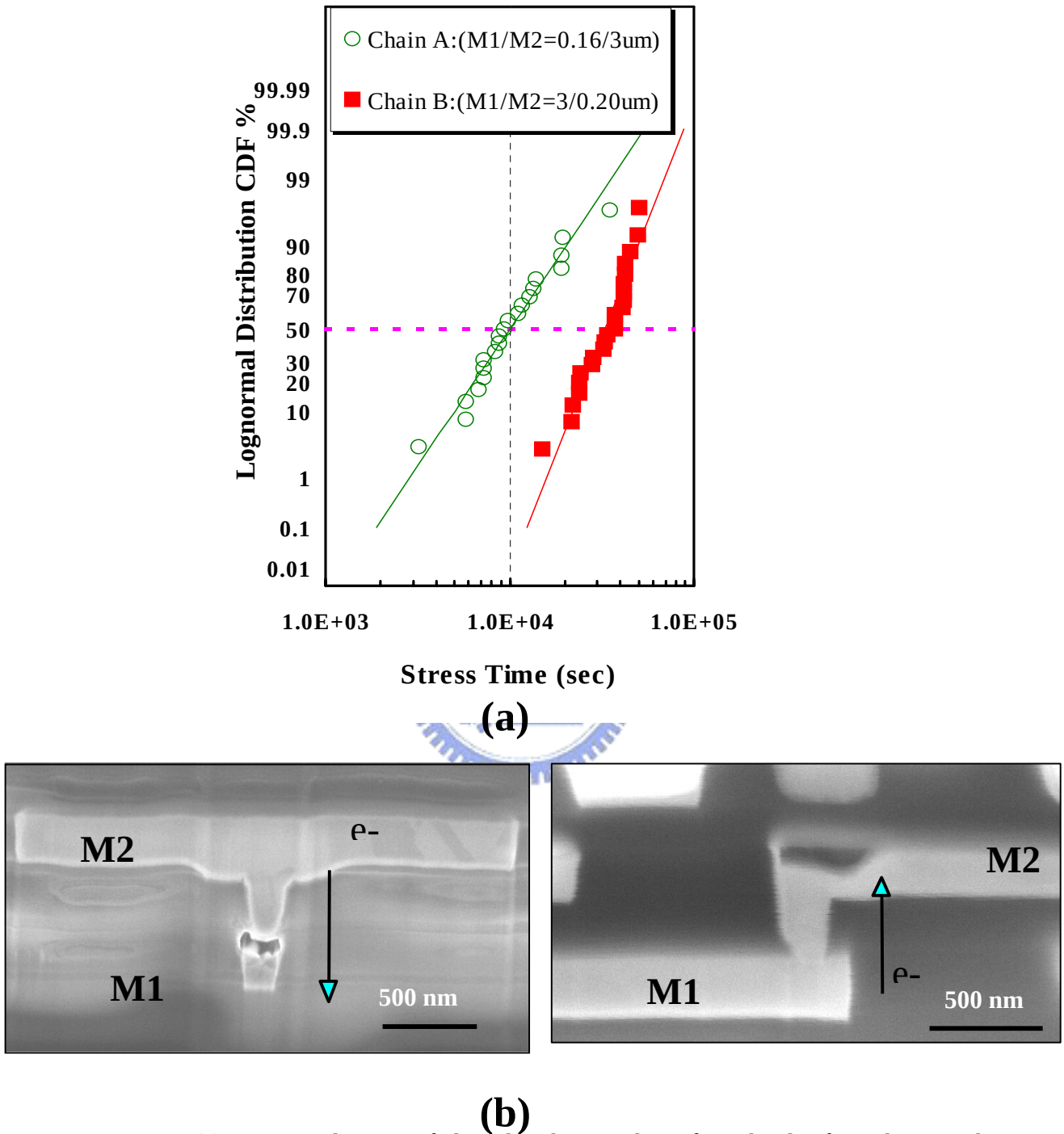
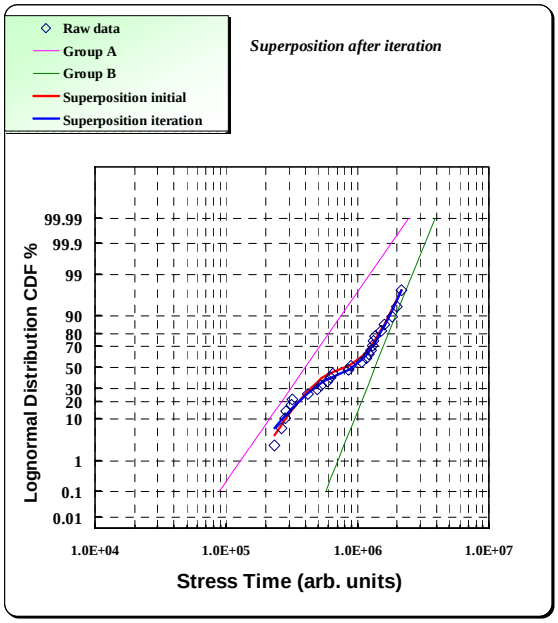
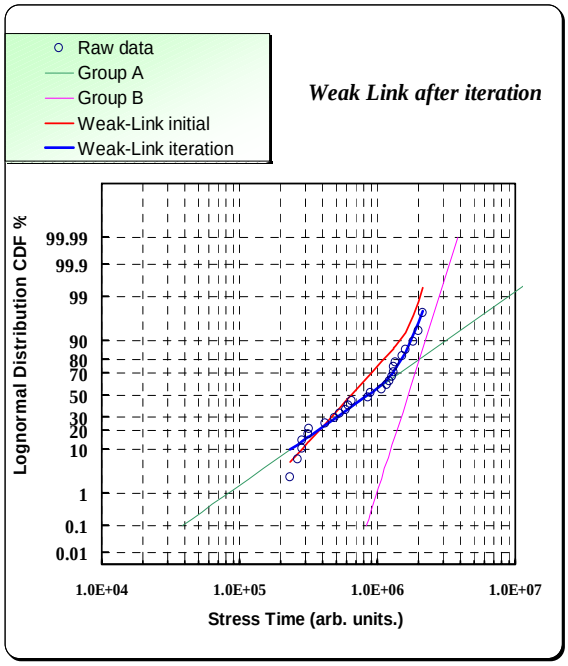


Fig.3.9 (a) Lognormal time-to-failure distribution plots of two kinds of via chains with different line width arrangements. The sample size is 21/23 for Chain A/ Chain B. MTF=2.80 h, σ = 0.54 for Chain A, MTF=9.17 h, σ = 0.32 for Chain B. Stress conditions are the same for both splits. (b) SEM image of left: Chain A is M1/M2 (0.16 μm/3 μm); right: Chain B is M1/M2 (3 μm/0.20 μm). Cu/SOD low-k material was used.



(a)



(b)

Fig.3.10 (a) Log-normal time-to-failure distribution plot using the superposition method (statistical method). A good fitting result was obtained after Levenberg-Marquardt iteration (R^2=0.991). A poor fit curve shows the initial guess result. (b) The same EM data was fitting by the weak-link method (statistical method). A good fit was obtained (R^2=0.987). A poor fit curve shows the initial guess result. The EM failure time was obtained at 295^{o}C under a current density of 1.28x10^{6} A/cm^{2} .

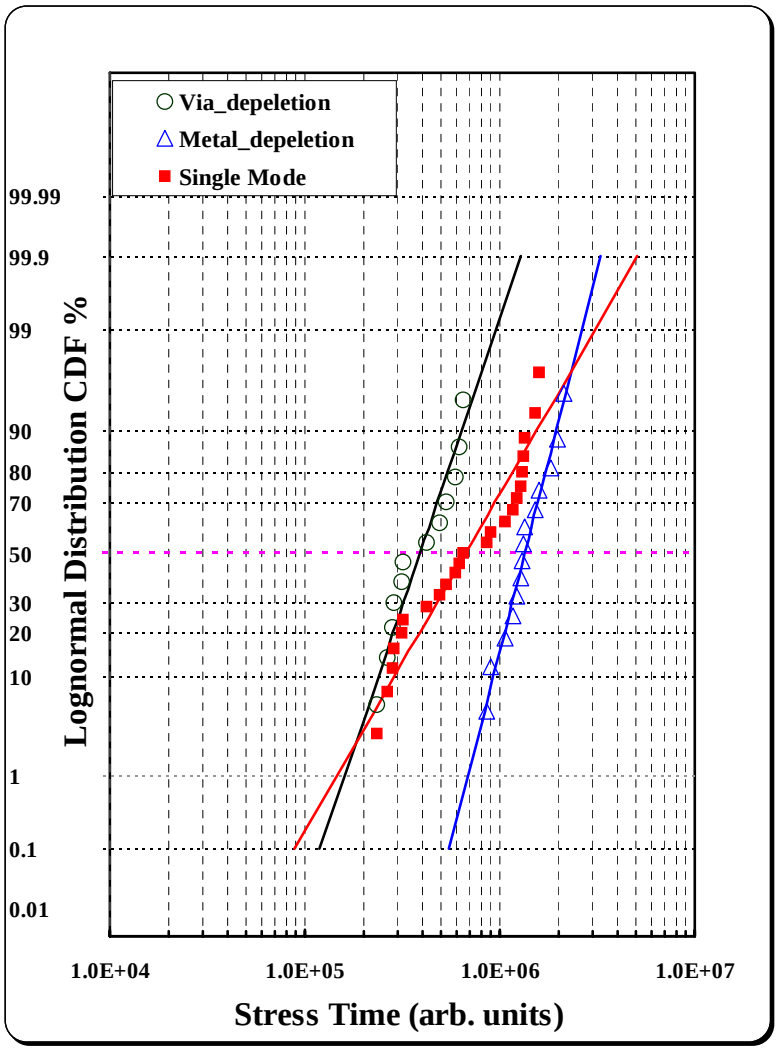


Fig.3.11 Bimodal fitting using the physical method. The physical method is defined according to relative resistance vs. time behaviors. Samples were manually grouped into two failure categories: instantaneous failure and long-lasting failure.

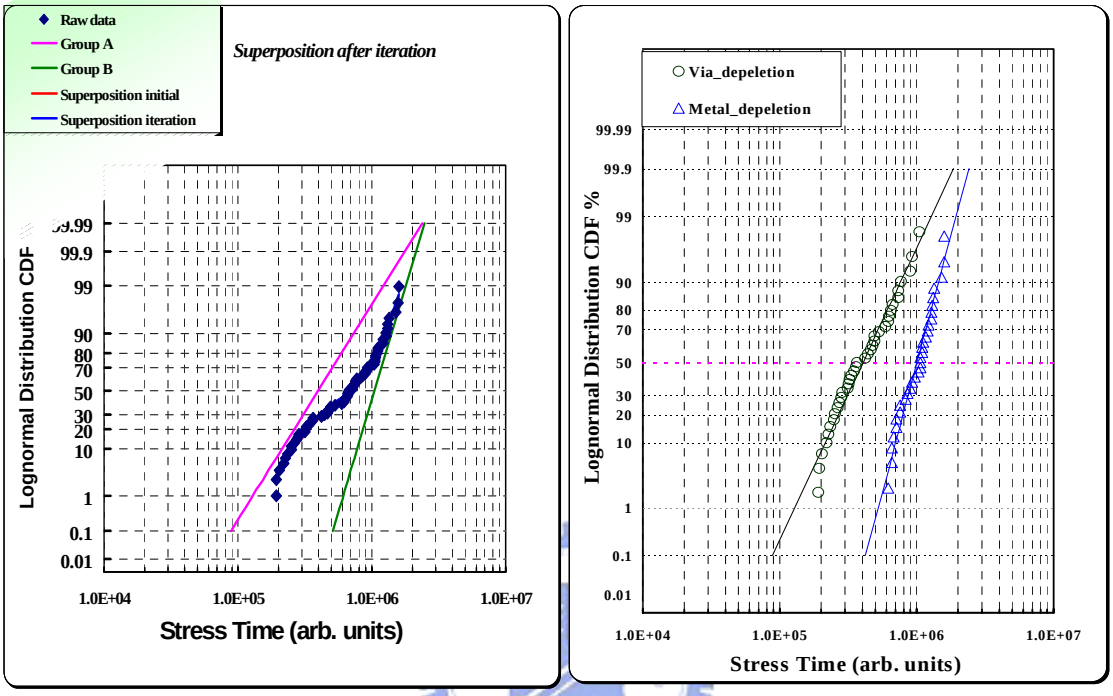


Fig.3.12 Many samples were analyzed by superposition (right) and physical (left) methods with bimodal fitting. The same stress conditions are used for all the samples.

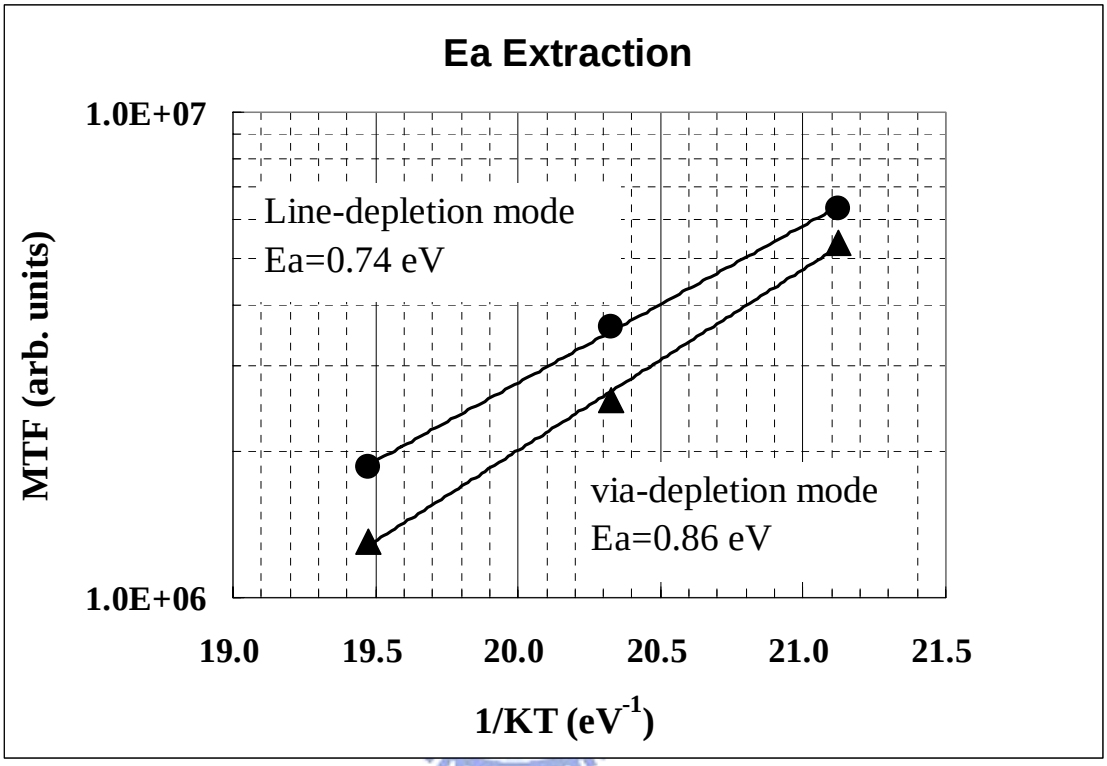


Fig.3.13 The activation energy Ea extracted from via and line depletion modes.

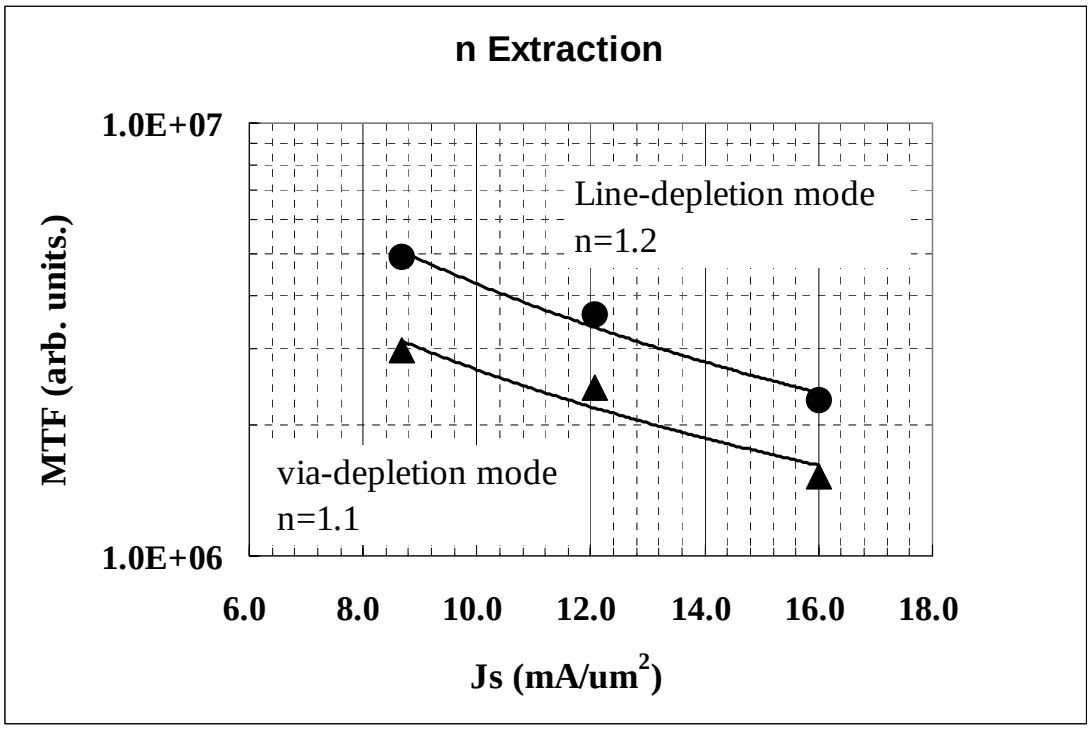


Fig.3.14 Current density exponent n extracted from via and line depletion modes.

TABLE 3.1 Summary of the five parameters [P(A), MTF_A, σ_A, MTF_B, σ_B] of superposition model extracted by iteration fitting (R^2=0.991), the four parameters [MTF_A, σ_A, MTF_B, σ_B] of the weak link model extracted by iteration fitting (R^2=0.987), and the fitting results of statistical methods with the data from the physical fitting method.

	Method	Failure Mode	MTF(h)	Sigma	P(A)	R^2
Statistic Method	Superposition	Via	110.6	0.48	48%	0.991
		Metal	278.0	0.28	52%	
	Weak link	Via	237.6	1.01	NA	0.987
		Metal	464.0	0.22	NA	
Physical Method	Physical Manual	Via	108.8	0.39	46%	0.928
		Metal	374.1	0.21	54%	0.977

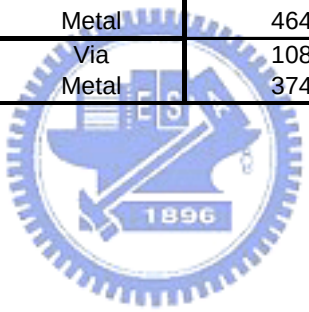


TABLE 3.2 Fitting results of statistical methods compared with those data from physical fitting method. The test structure consisted of a 0.2 μm wide, 400 μm long dual-damascene Cu M2 line. The low-k1, low-k2 and low-k3 are represented as SiOC, FSG and SOD, respectively. “Lot” means signifies a different batch of wafers using the same process flow.

Lot	Method	Failure Mode	MTF(h)	Sigma	P(A)
low-k1	Superposition	Via	483.3	0.26	15%
		Metal	839.3	0.20	75%
	Physical	Via	465.7	0.30	20%
		Metal	817.9	0.19	80%
low-k2	Superposition	Via	110.6	0.48	48%
		Metal	278.0	0.28	52%
	Physical	Via	108.8	0.39	46%
		Metal	374.1	0.21	54%
low-k3	Superposition	Via	72.9	0.74	91%
		Metal	278.2	0.10	9%
	Physical	Via	69.8	0.60	86%
		Metal	258.6	0.20	13%

TABLE 3.3 Key parameters of individual lot, combo lots using Cu/FSG materials obtained by both statistical and physical fitting methods. The test structure consists of a 0.2 μm wide, 400 μm long dual-damascene Cu M2 line.

Lot	Method	Failure Mode	MTF(h)	Sigma	P(A)
Lot1(low-k2)	Superposition	Via	110.6	0.48	48%
		Metal	278.0	0.28	52%
	Physical	Via	108.8	0.39	46%
		Metal	374.1	0.21	54%
Lot2(low-k2)	Superposition	Via	128.4	0.64	43%
		Metal	245.6	0.25	57%
	Physical	Via	112.0	0.55	40%
		Metal	255.0	0.21	60%
Lot3(low-k2)	Superposition	Via	106.1	0.51	65%
		Metal	269.9	0.22	35%
	Physical	Via	103.2	0.42	69%
		Metal	289.4	0.24	31%
3 lots Combo	Superposition	Via	109.9	0.48	55%
		Metal	290.3	0.23	45%
	Physical	Via	112.6	0.49	54%
		Metal	276.0	0.28	46%

Chapter 4

Copper Interconnect Electromigration Lifetime Improvement through Cap/dielectric Interface Re-engineering

4.1 Preface

For Cu interconnects, the electromigration atomic flux transports through all possible diffusion paths including bulk, grain boundaries, the Cu/metal-barrier interface, and the Cu/dielectric-barrier interface. The typical Cu conductor requires a liner to inhibit Cu atomic flux diffusion through the intralevel dielectric (ILD). The liner is usually metallic layer such as Ta or TaN/Ta, which generally provides a good adhesion to the Cu, so that the atomic flux transport along the liner is suppressed. Unfortunately, in dual-damascene process, the chemical mechanical polishing (CMP) is used to remove the excess Cu film on the top of trenches, and then fresh Cu is exposed. The top surface of the Cu damascene line is usually covered with a thin dielectric diffusion barrier layer. Many investigators have reported that the Cu/cap dielectric interface is the dominant diffusion path in Cu damascene interconnects [4.1-4.5]. Different surface treatments can significantly affect EM result. Various approaches including special process steps and cap layer materials have been used to increase the current capability of Cu lines. Lloyd et al [4.6-4.7] found that the adhesion between Cu and the upper surface cap material are directly correlated to electromigration lifetime. Hatano et al [4.8] reported electomigration lifetime improvement using a P-SiC cap layer as compared with P-SiN. Hu et al [4.9-4.11] reported improved electromigration lifetime of Cu interconnection with a selective electroless metal coating of CoWP, CoSnP, or Pd, on the top surface of Cu damascene lines. Fischer and Glasow [4.12, 4.13] discussed the influences of the pre-clean process after via-etch and SiN cap deposition for different pre-clean intensity. However, few studies have been done on the effect of cap-layer

pre-clean on MTF of EM. Therefore, the present study focuses on the correlation between electromigration lifetime and Cu surface cap-layer process.

In this chapter, an especially suitable EM test structure has been designed to evaluate the properties of Cu cap-layer interface. A three-level dual-damascene Cu interconnect line has been produced to allow a series of experiments to be carried out. This study illustrates the interface between the Cu line and the dielectric capping layer, and the pre-clean treatment prior to dielectric layer deposition. The results of this study indicate that the Cu cap-layer pre-clean treatment and the adhesion of the Cu/cap interface can be directly correlated to the electromigration lifetime of Cu interconnects.

4.2 Experimental Detail

Sample was fabricated using Cu dual damascene process with a TaN/Ta liner. The TaN/Ta liner and Cu seed layers were deposited sequentially by using PVD method. In addition, re-sputtering leads to the excellent side wall coverage, and void free in vias. The test structures film stack were fabricated using a dual damascene process in which both via and line were etched into the low-k dielectric followed by backfilling with liner, Cu seed, and electroplated Cu. The excess Cu and liner films were removed by chemical mechanical polishing process. The sample size per EM test was more than 20. The relationship between metal resistance and temperature is given by $TCR(T) = [1/R(T)]\ \Delta R/\Delta T$, where TCR is the temperature coefficient of resistance , R is the resistance, and T is the sample temperature. The TCR value was determined based on resistance measurements at a step of $50^{o}C$ in the range 50 to $300^{o}C$. The correlation between R and T within the investigated temperature was found to be close to linear. Reduced stress current density in the range of 0.6 to 2.0 MA/cm^2 (defined with respect to the cross-section of metal line) were used to control temperature raise due to Joule heating to less than $3^{o}C$ even for low-k

materials known for possessing small thermal conductivity. Testing was conducted typically at 300^{o}C with a current density of 1.6 MA/cm^{2}. The EM failure criterion was defined as 20% of resistance increase or when extrusion monitor current exceeds 1μA. The EM structure used in the tests described below is via terminated structure, as shown in Figure 4.1(a). The arrow indicates the Cu/cap dielectric interface layer of Cu damascene interconnects. Two stress current directions were investigated naming " down-stream " defined for the electron flow from upper wide metal line over via into the under narrow metal line and " up-stream " defined for the electron flow from lower wide metal line thru via into the upper narrow metal line. The wide trench line with single via was used to eliminate the liner redundancy effect and to characterize the mass transport at the Cu/Cap dielectric interface in Figure 4.1(b). It consists of a 0.42μm wide, 400 μm long dual damascene Cu M2 line connected with a single via diameter 0.14x0.14 μm^{2}. The test structure with a fully landed via was suitable for verifying the character of the Cu/cap interface. The EM test samples were processed with different cap layer pre-treatments and cap-layer materials. The process split studied is summarized in Table 4.1. The pre-clean A and pre-clean B represented different gas species (H_2 and NH_3, respectively) and the gas flow used. The cap-layer SiCN was a nitrided form of SiC. Quantitative adhesion data were obtained from modified Edge Liftoff Test (m-ELT) and four-point bending measurement [4.14]. The film stack of samples was Si/PEOX/Liner/Cu/PE-SiN or SiCN. Pre-clean B was employed for adhesion test samples. The reported adhesion results were averaged from ten samples.

4.3 Results and Discussion

4.3.1 The effect of geometrical layout on MTF.

Geometrical layout design is a simple way to increase EM resistance. The wide lines used in this study were designed as either single or dual vias, and the line end extension was optional. Wide lines with dual vias are expected to achieve a longer EM lifetime than that of a

single via. The plot of the relative resistance versus time shows an instantaneous change for a single via, but for dual via two modes were found (most samples are long-lasting and few undergo instantaneous change) [4.15], as shown in Figure 4.2(a). Failure analysis shows that via bottom depletion will induce instantaneous change. A dual via structure with a redundant via can support the current if the Cu under one of the via bottom becomes depleted, as shown in Figure 4.2(b), which causes the change in resistance to occur over an extended period of time. In comparison to a single via, the dual via structure not only extends the MTF by around three times, but also reduces the deviation in time-to-fail by about half, resulting in an EM lifetime enhancement of more than ten times. Furthermore, the major failure mechanism was found to have changed from instantaneous to long-lasting mode. The line-end extension will cause different trends in both narrow and wide lines [4.16]. When the line width is equal to the via diameter, the line-end extension may not change the redundancy effect, since the via liner is always connected to the wall liners on both sides of the line. The line-end extension will increase the EM lifetime, since the extra Cu in the line-end acts as a reservoir and means that it will take longer for the Cu to diffuse. But for wide lines with a single via, an EM structure without a line-end extension, the via liner will be connected to the trench liner, which serves as a current path when the void is in nucleation and there is void growth under the via bottom. It is expected that a zero line-end extension will achieve a better EM lifetime performance, however, no obvious improvement in EM lifetime was observed, as shown in Figure 4.3(a). This can be explained from two aspects. The first is that the interface diffusion is the dominant factor rather than liner connection; the second is that some early failure samples were found in structures that did not contain an extension as a result of the process variations, as shown in Figure 4.3(b). In this structure, the line-end between via and metal is zero. The via misaligning metal line may be due to process variations. The probability of misalign in no line-end extension is higher than that of the line-end extension. Consequently, the wide trench line using single via was used to

eliminate the liner redundancy effect and to characterize the mass transport at the Cu/Cap dielectric interface. A test structure that contained a fully landed via was found to be suitable for verifying the characteristics of the Cu/cap interface.

3.3.2 The effect of pre-treatment on MTF.

The Cu/cap dielectric interface is the dominant diffusion path in Cu damascene interconnects. The most critical process leading to this specific interface property is known to be the pre-clean treatment prior to cap dielectric film deposition together with the cap layer materials. In this work, two pre-clean recipes containing different H compounds were used. Pre-clean A and reference process pre-clean B used different recipes base on the gas species and gas flow. Figure 4.4(a) shows the time-to-fail distribution of the PE-SiN cap layer using both pre-clean A and pre-clean B. By using pre-clean A, a significant improvement in EM lifetime was obtained, with around three times increase in MTF. This result indicates that the Cu atom migration velocity at the interface after pre-treatment with H-rich pre-clean A is obviously slower than that of the N-based pre-clean B. In comparison to the relative resistance degradation shown in Figure 4.4(b), both cases display similar EM failure behavior. The distinct increase in MTF suggests that there should be an essential change taking place at the Cu/cap layer interface. The different initial resistances of the Cu-wire for both pre-treatment recipes are shown in Figure 4.5(a). The H-rich pre-clean A an initial resistance that is 8% larger than that of the N-based pre-clean B using various cap-layer materials. The temperature coefficient of resistance (TCR) has been used as a parameter to qualitatively monitor the Al metal properties [3.17]. The TCR values have been investigated with regard to both the median grain size and the defectiveness of the crystal lattice. High TCR values indicate large median grain sizes, whereas smaller TCR correspond to a fine-grained microstructure. The correlation between the TCR and both the microstructure and the stressvoiding behavior of Cu interconnects have been comprehensively

investigated in previous works [4.17]. The impact of the pre-clean treatment on the TCR values of Cu can be clearly seen in Figure 4.5(b). For the pre-clean A treatment, the TCR decreases strongly. One hypothesis is that the observed TCR decrease can possibly be explained by the increase in the residual resistivity. The net resistivity is given by $\rho(T)=\rho_L(T)+\rho_I$, where $\rho_L(T)$ is the resistivity caused by electron scattering by the thermal phonons, and ρ_I is the resistivity caused by electron scattering or static defects (e.g. surfaces, grain boundaries, defects) that disturb the periodicity of the lattice. Often $\rho_L(T)$ is independent of the number of defects where their concentration is small, and often ρ_I is independent of temperature. The resistance, R(T) = [L/A] $\rho(T)$, where L is the length of the metal, and A is the cross-sectional area of the metal, is proportional to the resistivity. TCR can be expressed by:

$$TCR(T) = [\frac{1}{(\rho_L(T)+\rho_L)}]\frac{\rho_L(T2)-\rho_L(T1)}{T2-T1}. \quad (4.1)$$

The TCR value will decrease with increasing residual resistivity ρ_I. The measured line resistance increases, as shown in Figure 4.5(a), with no change in the cross-section, which confirms the above-mentioned hypothesis. From this viewpoint, it may be said that the effect of the pre-clean on the Cu line is a residual resistivity change. Since all split samples were produced using the same process flow with the exception of the pre-clean and dielectric cap materials, the Cu grain boundary, defect and geometric dimensions should be the same for all split samples. It can be concluded that the majority of residual resistivity changes are dependent on the interface surface properties. High magnification TEM analysis was carried out to reveal the interface image, as shown in Figure 4.6. A very clear inter-layer between the Cu and the cap dielectric layer with a thickness of about 80A can be observed and is shown in a darker contrast. This demonstrates that the inter-layer is a high resistant compound formed on the Cu surface as a SiN deposition during the H-rich treatment. The physical and electrical evidence is consistent with previous studies [4.18], suggesting that the inter-layer should be Cu-silicide (Cu_xSi_y). Secondary

Ion Mass Spectrometry (SIMS) was used to analyze the top surface of the Cu following both pre-clean treatment methods. Unfortunately, the Cu_xSi_y layer was too thin to obtain a high Si concentration, and the cap-layer of the SiN film also caused the Si concentration to fluctuate. No significant Si concentration variation was shown in the top surface of the Cu after the H-rich pre-clean treatment. However, we have strong evidence to support the possibility of Cu silicide formation. The SiH_4 precursor concentration was increased before cap layer film deposition. After generating the plasma, more reactive Si species will be created in the CVD chamber, which react with the fresh Cu to form a Cu silicide layer prior to SiN cap layer deposition. As can be seen in Figure 4.7, the MTF of the EM increases as the Si species concentration increases. A possible explanation for the higher initial Cu wire resistance in Split5 is that the thickness of the Cu silicide increases. These findings lead us to believe that the Cu silicide formation mechanism is probable. The Cu-silicide acts as the metallic cap layer [4.9], which will reduce the mass transport at the Cu/cap interface. The inter-metallic compound capped on the top surface of the Cu wire provides a more cohesive interface between the Cu and the cap-layer and effectively reduces Cu migration. The reason is thought to be the changes in strength of the interface bond, and the reduction in mobility of the Cu atoms is caused by pinning. Therefore, a reasonable mechanism for enhancing the EM lifetime is proposed. After the Cu-oxide on the post-CMP surface is removed efficiently by the H-rich pre-clean A treatment, then a “fresh” Cu surface is exposed. Consequently, the SiH_4 precursor gas reacts with the fresh Cu surface and forms a thin Cu_xSi_y layer prior to the cap dielectric film deposition. A schematic flow for the formation of Cu-silicide is illustrated in Figure 4.8(a). A Cu-silicide layer provides a new interface with a lower Cu migration rate than a SiN/Cu interface and improves EM resistance of the Cu interconnect. Moreover, it has been proposed that N-based pre-clean B will form a very thin nitrided layer [4.18]. The Cu-nitridation reaction flow is shown in Figure 4.8(b). This nitridation layer will block the SiH_4 precursor gas from forming Cu-silicide and will suppress any increase

in resistance of the Cu wire, which is supported by the diagram in Figure 4.5(a). The diffusion velocity of the Cu atoms along the surface of the Cu wire during the pre-clean B treatment is speculated to be faster than that of pre-clean A due to the lack of a Cu-silicide layer. The MTF of pre-clean B is consequently shorter than that of pre-clean A.

3.3.3 The effect of cap-layer material on MTF.

Various cap-layer materials were used to examine the interface property. The EM lifetime performance of SiCN and PE-SiN with the same N-based pre-clean B were compared. The MTF for SiCN is two times longer than the PE-SiN cap dielectric layer, but the TTF distribution is broader than that of PE-SiN. Measurements of both the activation energy extraction and the adhesion of cap-layer were used to investigate the different interface properties. A higher activation energy (Ea~1.1 eV) of samples containing SiCN was obtained compared to PE-SIN (Ea~0.79 eV). The adhesion level between the cap-layer and the Cu was obtained through m-ELT and a four-point bending method. The activation energy data and the adhesion level data comparing SiCN and PE-SiN is listed in Table 4.2. Based on the result of both measurement methods, it is obvious that the adhesion strength of SiCN is stronger than PE-SiN. The enhancement in EM lifetime can be explained below. The adhesion of the Cu/cap interface can be directly correlated to the electromigration MTF and the activation energy [4.6]. The strength of the adhesion will affect the nucleation and growth rate of the void and is induced by the EM effect. Therefore, a better adhesion between the cap-layer and the Cu will suppress the mass transporting of Cu through the cap interface. A higher activation energy also indicates that the diffusion of Cu atoms along the interface between the Cu and the SiCN is slow. Thus, the EM degradation of SiCN is reduced as a result of better adhesion and higher activation energy when compared to PE-SiN. In conclusion, pre-clean A shows a longer MTF than pre-clean B under the same cap dielectric layer conditions. In addition, SiCN shows a better EM performance than

PE-SiN using the same pre-treatment. Finally, for the SiCN using the H-rich pre-clean A treatment, a ten times longer MTF and tight failure time distribution were attained. Figure 9 shows the discrepancy between the SiCN with H-rich pre-clean A and PE-SiN using the N-based pre-clean B. A significant improvement in EM performance has been achieved.

4.4 Summary

In conclusion, the dual via structure not only extends the EM lifetime but also changes the major failure mechanism from instantaneous to long-lasting mode. The effects of pre-clean and cap-layer material on MTF are significant. A SiCN+pre-clean A can improve the lifetime by 10x compared to a PESiN+pre-clean B process. The adhesion of the Cu/cap interface can be directly correlated to electromigration MTF and activation energy. A Cu-silicide formation mechanism prior to cap-layer deposition was proposed to explain the enhancement of EM lifetime. The critical process that leads to this specific interface property is known to be the pre-clean treatment before cap dielectric film deposition and cap layer materials.

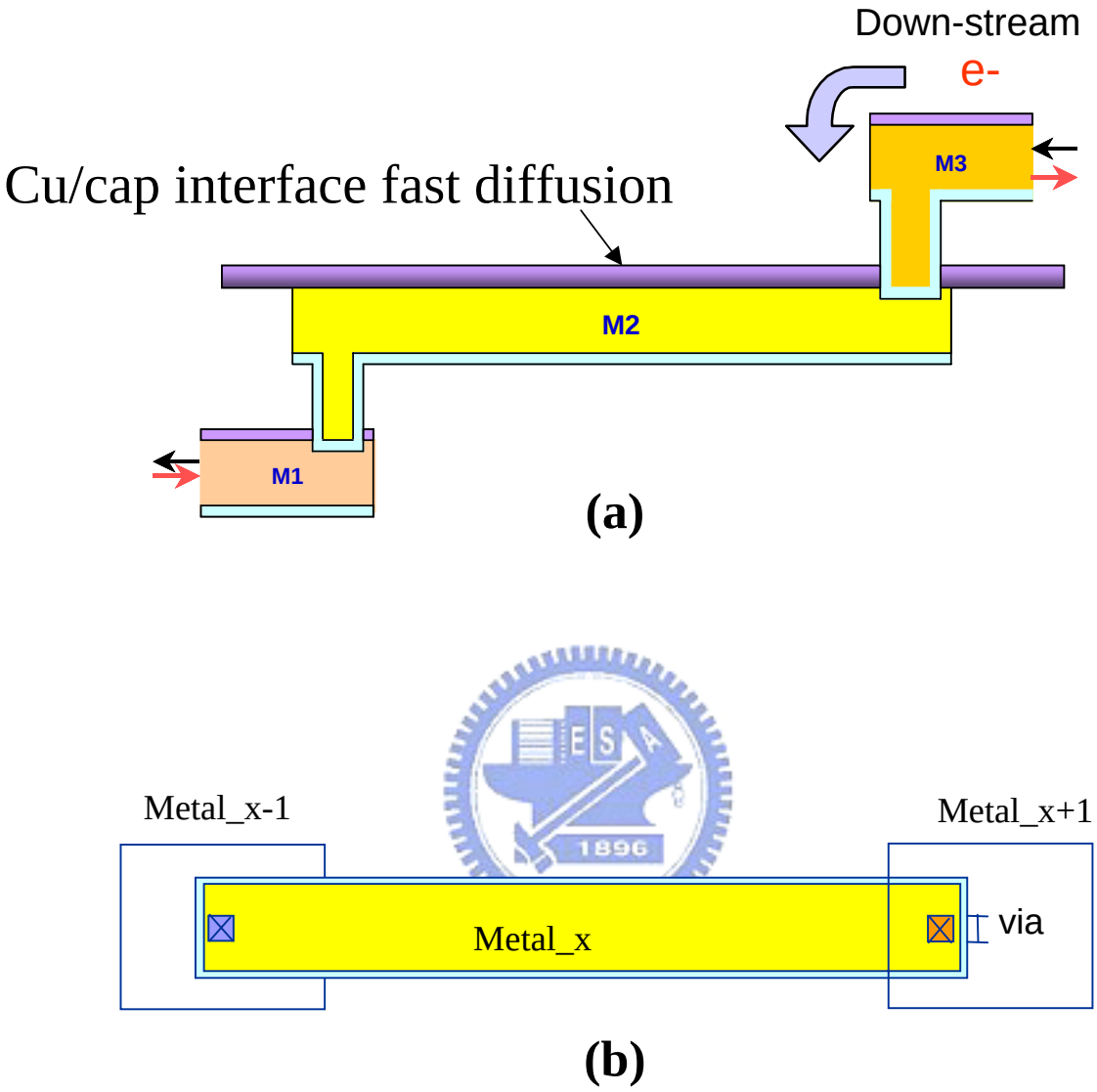
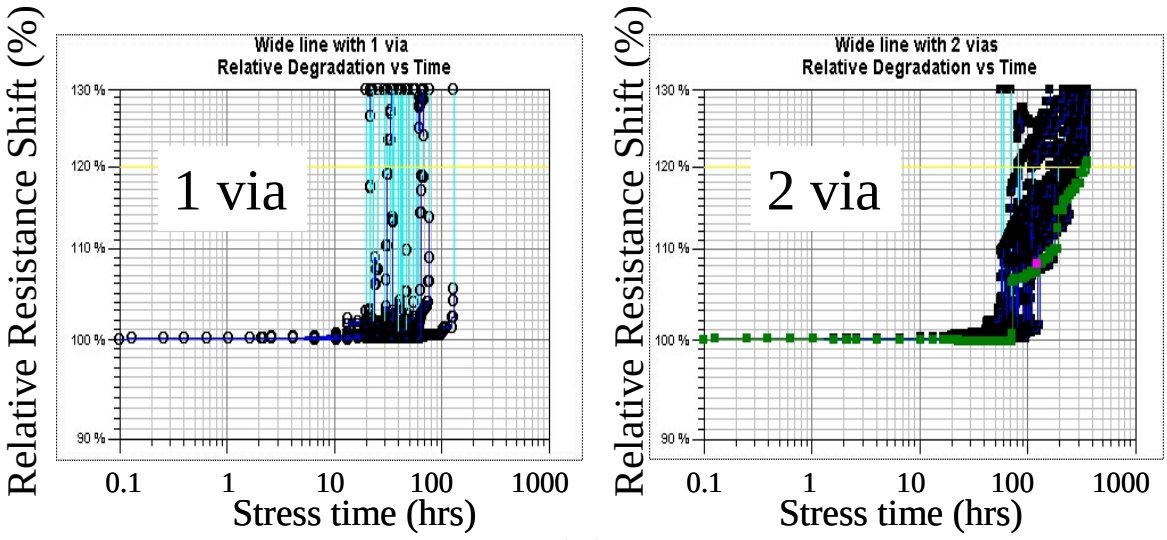
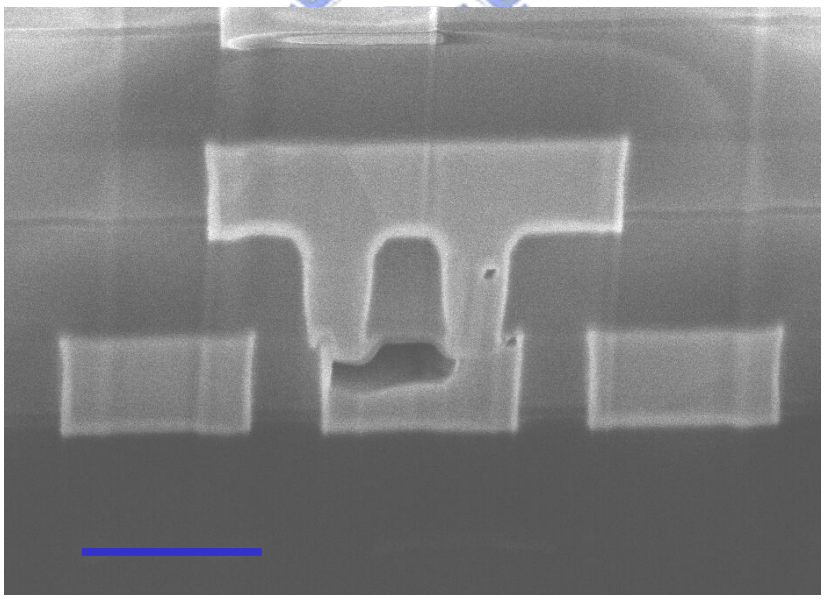


Fig.4.1 (a) Side view of via terminated line structure used in the present work. Stress direction is defined by electron current flow direction. (b) Top view of wide line with single via. The width of Metal =0.42 μm equals approximation 3x via diameter (0.14x0.14 μm^2).

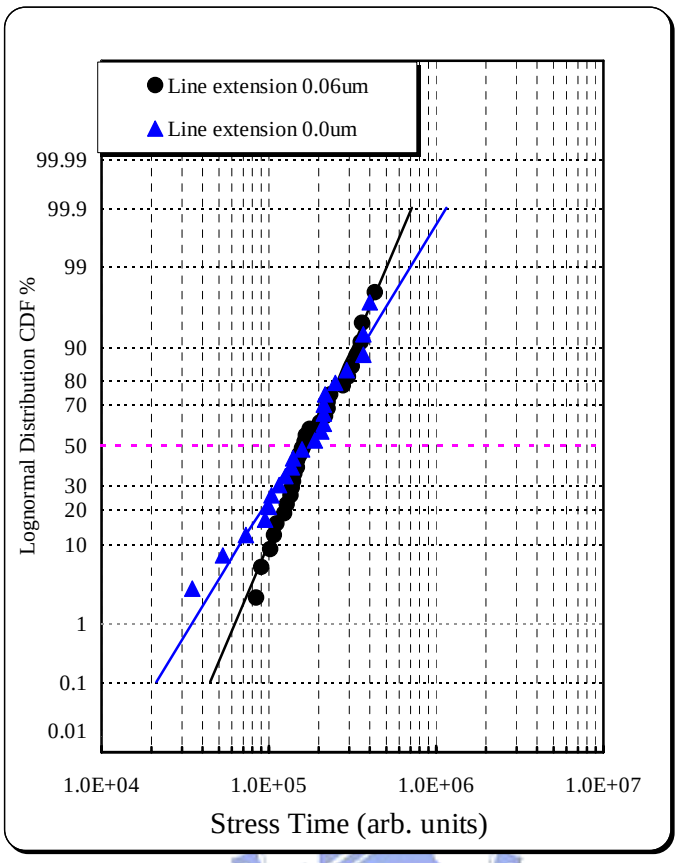


(a)

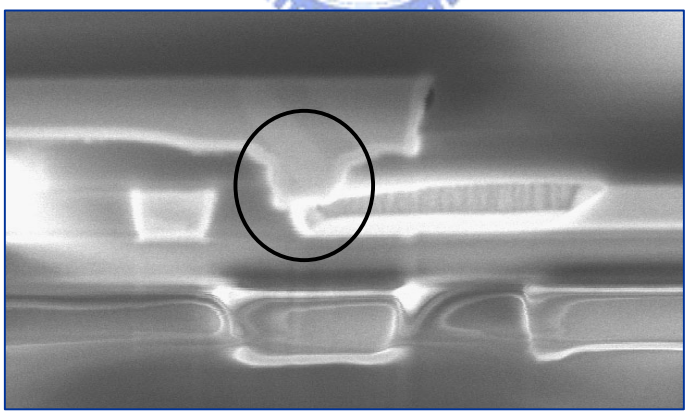


(b)

Fig.4.2 (a) Illustrates relative resistance degradation vs. time plot. Left: wide line with 1 via. Right: wide line with 2 vias.(b) SEM image for two vias wide line structure, void was found in one via bottom, the other serves a current path.

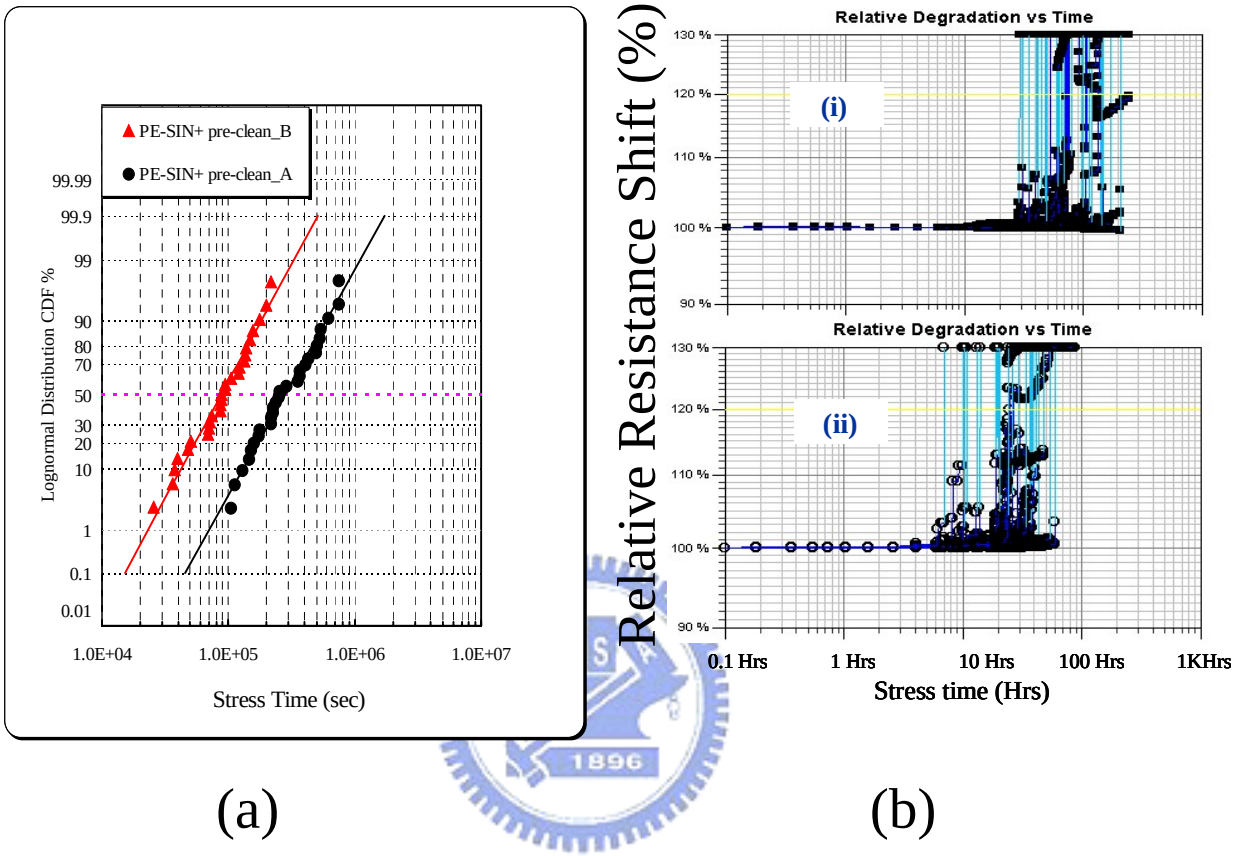


(a)



(b)

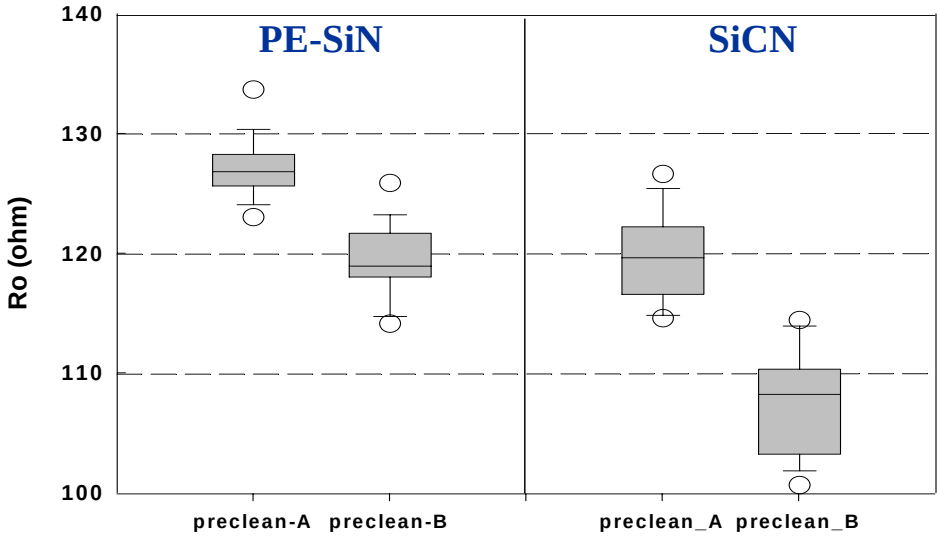
Fig.4.3 (a) Lognormal time-to-failure distribution plots for line end extensions of 0.06 vs. 0.0 μm. Cu/SiOC low-k material was used. (b) In this structure, the line-end between via and metal is zero. The via misaligning metal line may be due to process variation. The probability of misalign in no line-end extension is higher than that of the line-end extension.



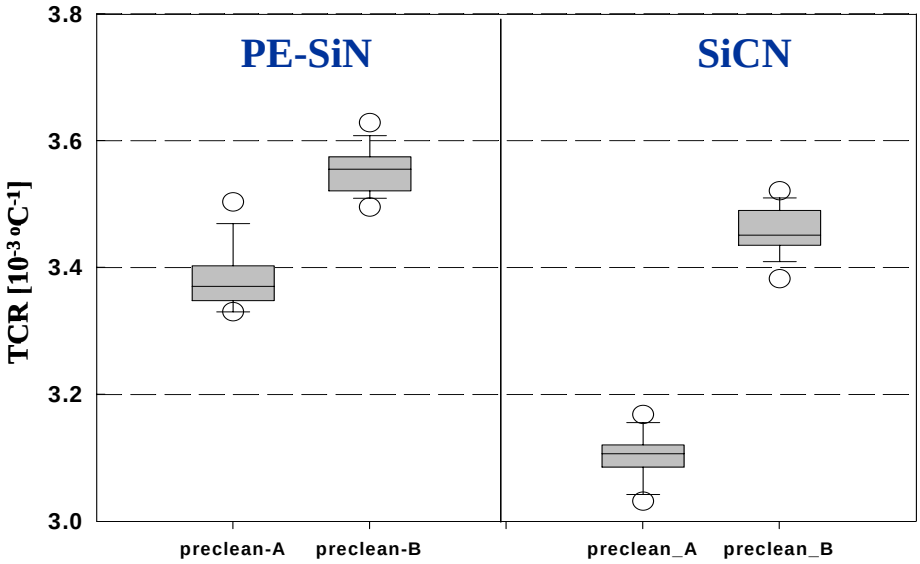
(a) (b)

Fig.4.4(a) Lognormal Time-To-Failure distribution plots for PE-SiN+pre-clean A and PE-SiN+pre-clean B. The sample size is 27/28 for PE-SIN+pre-cleanA/ PE-SIN+pre-clean B. MTF=77.8 hrs, σ = 0.58 for PE-SIN+pre-cleanA, MTF=24.4 hrs, σ = 0.56 for PE-SIN+pre-cleanB. Stress conditions are the same for both splits.

Fig.4.4(b) Relative resistance degradation vs. time plot for (i) PE-SiN+ pre-clean A.(ii) PE-SiN+ pre-clean B. The failure mode is almost same for both pre-clean recipes but the MTF is 3.2 times improvement for pre-clean A.



(a)



(b)

Fig.4.5 (a) Cu-wire initial resistance of PE-SiN and SiCN with pre-clean A or pre-clean B. The resistance of Cu wire with pre-clean A treatment is higher than that with pre-clean B for both cap-layer materials. The sample size is 30 for initial resistance extraction. The mean ± standard deviation of resistance(%) is 127.1 ± 2.1%, 119.4 ± 2.6%, 119.6 ± 3.1%, 107.5 ± 3.9% for PE-SiN+Pre-clean A, PE-SiN+Pre-clean B, SiCN+Pre-clean A, and SiCN+Pre-clean B, respectively.

Fig.4.5 (b) Effect of different pre-clean treatment on TCR value.

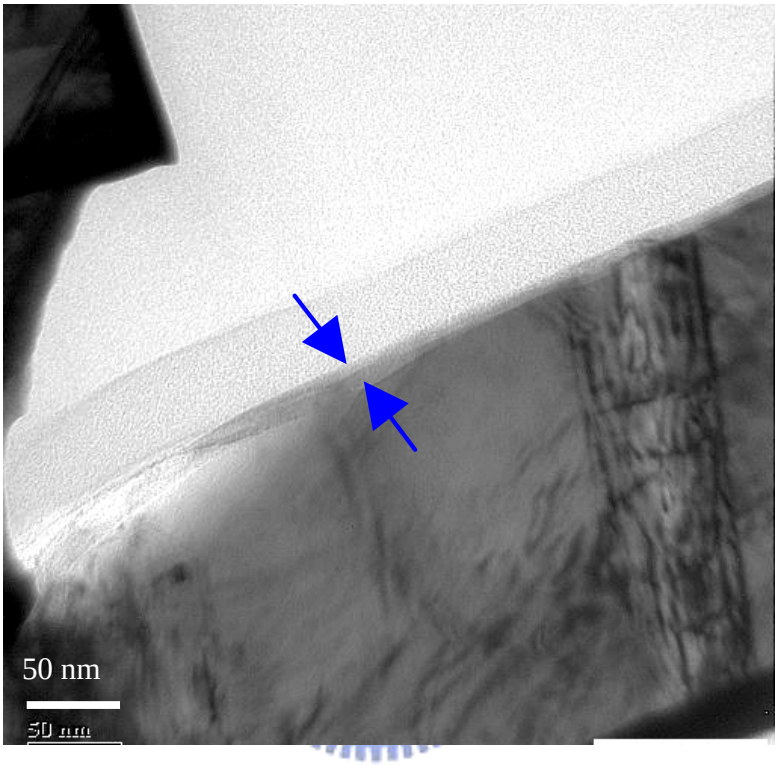


Fig.4.6 High magnification TEM image on Cu/Cap interface. A very clear inter-layer with darker contrast between Cu and cap dielectric layer is observed and its thickness is about 80A.

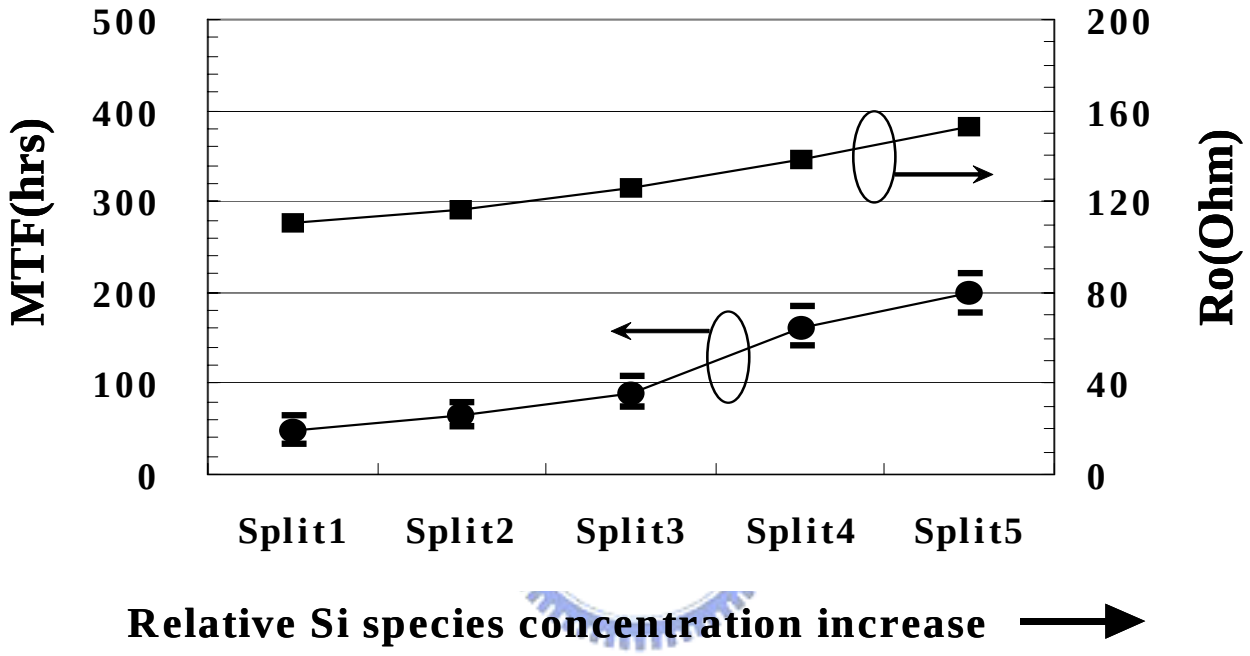
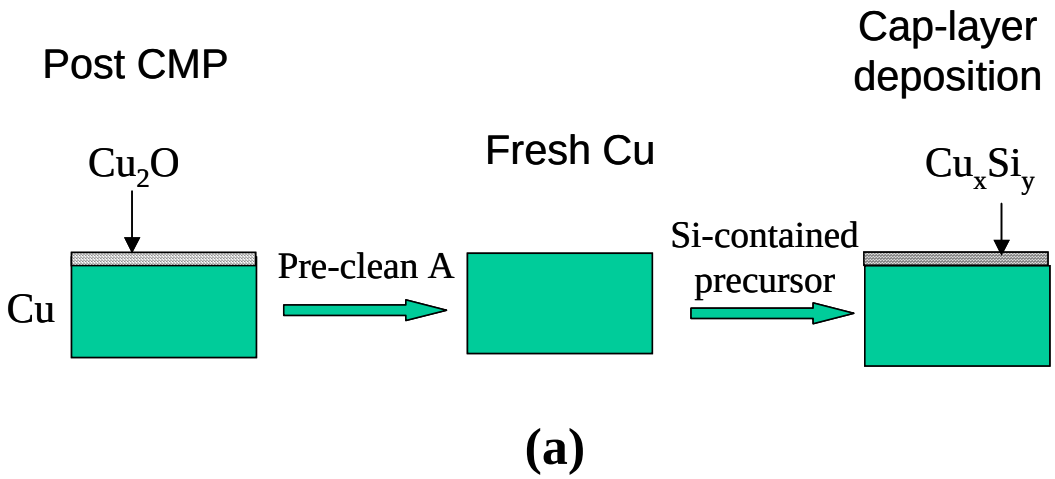
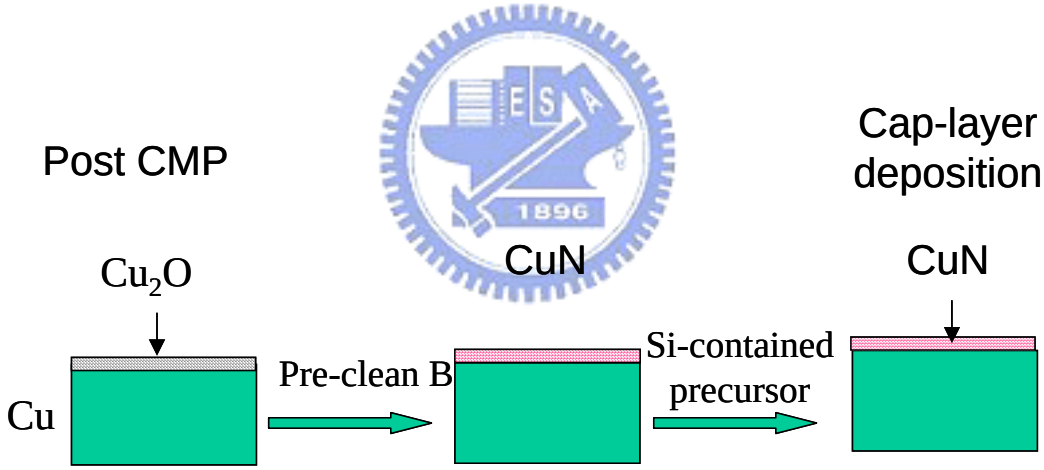


Fig.4.7 MTF (circles) and initial Cu wire resistance (squares) as a function of different split conditions. Error bars in MTF are the uncertainties to 90% CL. The split condition means that increase SiH_4 gas prior to cap layer deposition. Relative reactive Si species concentration is indicated by arrow direction.



(a)



(b)

Fig.4.8 (a) Schematic process flow of the Cu-silicide formation is shown

Fig.4.8 (b) Schematic process flow of the Cu-Nitridation reaction is proposed.

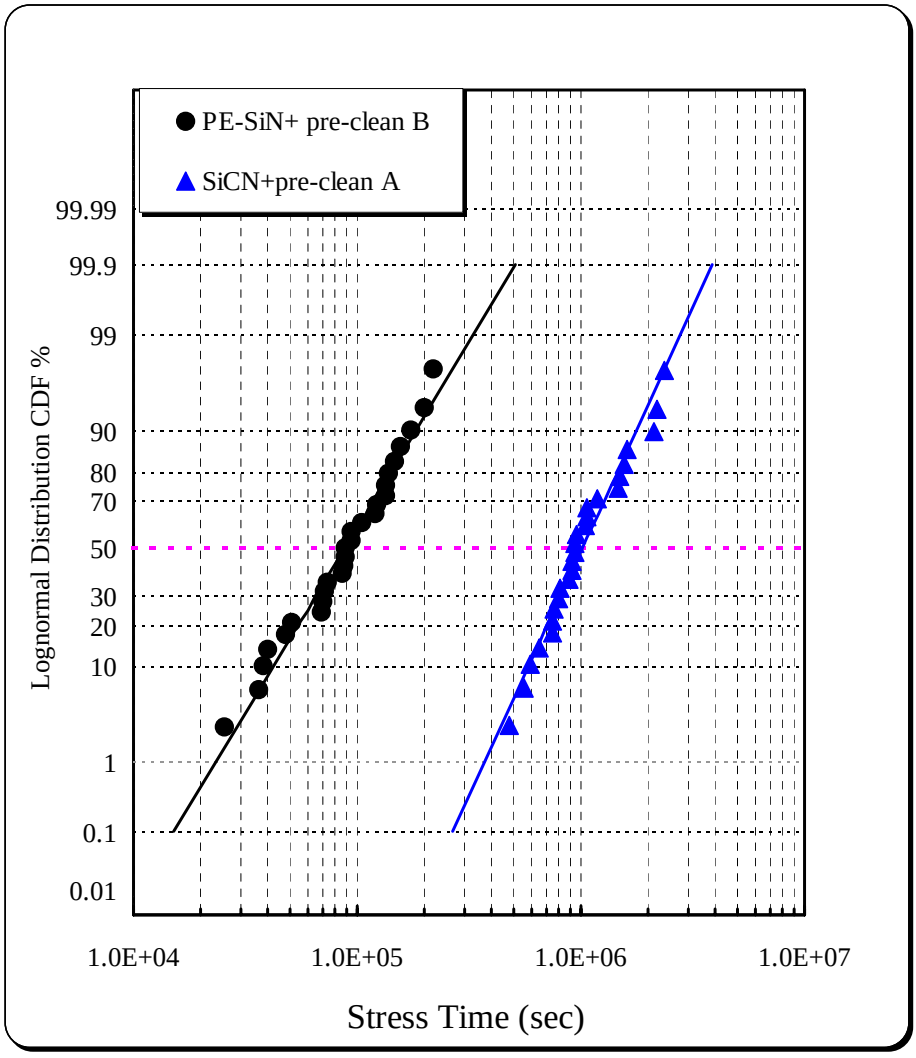


Fig.4.9 Lognormal Time-To-Failure distribution plots for PE-SiN+ pre-clean B and SiCN+pre-clean A, The sample size is 27/26 for PE-SIN+pre-cleanB/ SiCN+pre-clean A. MTF=24.4 hrs, σ = 0.56 for PE-SIN+pre-cleanB, MTF=281.6 hrs, σ = 0.47 for SICN+pre-cleanA. Stress conditions are the same for both splits. Significant improvement of EM lifetime performance is achieved.

TABLE 4.1 The process split studied is summarized. The pre-clean A and pre-clean B represented various gas species and the gas flow used. The cap-layer SiCN was a nitrided form of SiC.

	Pre-treatment parameter	Cap-layer Materials
1	Pre-clean-A	PE-SiN
2	Pre-clean-B	PE-SiN
3	Pre-clean-A	SiCN
4	Pre-clean-B	SiCN

TABLE 4.2 Comparison of adhesion and electromigration activation energy on different cap dielectric layer. SiCN shows better adhesion than PE-SiN for both measurement methods. Pre-clean B was employed for adhesion test samples. Sample size is 8 x 40mm^2 for 4PB, 10 x 10 mm^2 for m-ELT, respectively.

	PESiN	SiCN
m-ELT(MPa-m $^{1/2}$) *	0.35 ± 0.03	0.41 ± 0.05
4PB(J/m^2) *	37.6 ± 3.6	44.9 ± 5.2
Electromigration activation energy (eV)§	0.79 ±0.14	1.13 ± 0.2

* Standard deviation.

§ Uncertainties to 90% CL by Maximum Likelihood estimation method.

Chapter 5

Effects of Width Scaling and Layout Variation on Dual-Damascene Copper Interconnect Electromigration

5.1 Preface

Many studies have investigated methods of optimizing the Cu electromigration performance of narrow interconnects (<1 μm). The detail investigations into EM performance and reference improvement methods have been described in chapter 4. Process improvements are necessary to enable an increase in EM performance, while some geometric features of the testkey design also play a significant role in EM [5.1]. On one hand, the effect of via/line contact configuration was been examined in this work. On the other hand, the effect of width scaling on EM was investigated to identify the EM diffusion mechanism. EM involves atomic diffusion, typically along the dominant diffusion path. In contrast to Al-based interconnects, it has been shown that microstructure does not play a dominant role in the EM of Cu interconnects [4.4]. The fastest diffusion path is the Cu/cap interface [4.1,5.2], and the second fastest is the grain boundaries or Cu/liner interface [5.3], the slowest path should be grain bulk. Once the Cu diffusion along the top surface has been sufficiently slowed, the grain structure or interface boundary should affect reliability. The microstructure characteristics and the EM in Cu damascene line have been reported [5.4-5.6]. The grain size decreased as the line width decreased. Electroplated Cu has relatively larger grains, resulting in a longer EM lifetime than the CVD Cu. For wide lines, CVD Cu (3 μm) polycrystalline structure, and narrow lines (0.5 μm), quasi-bamboo structure, provide almost the same activation energy Ea~0.65 eV. Even with a polycrystalline orientation, PVD Cu samples showed a better activation energy value Ea~1.02 eV. However, a question remains as to why the PVD Cu process showed such a higher Ea value than that of the CVD Cu process. It may

be that surface diffusions have less effect, meaning that a higher Ea value was obtained from the experimental samples having a quasi bamboo grain microstructure using PVD Cu process. The interaction between the surface and the grain boundary diffusion provided the impetus for the investigation into electroplated Cu dual-damascene process. However, few studies have reported on the effect of line widths from w=0.14 μm to 10 μm on the MTF values. Therefore, the present study focuses on the effects of the wide linewidths region.

In this chapter, the effects of width scaling were evaluated after Cu/cap process optimization, that is to say the surface diffusion is sufficiently slow. Electromigration experiments were conducted in wide and narrow lines in order to emphasize the main diffusion path in a full Cu dual-damascene process. Especially, suitable EM test structures were designed to evaluate the properties of Cu. These test structures were more realistic than pure metal lines, and used a sufficient number of vias to eliminate any via-limited failures. The effect of width scaling on EM has been investigated to identify an EM diffusion mechanism that may be different for both narrow lines and wide lines. A theory was proposed to explain the results.

5.2 Experimental Detail

The EM tests were carried out at the package level. Samples were fabricated using a 90 nm Cu dual damascene process on 300 mm wafers. The film stacks in the test structures were fabricated using a dual-damascene process in which both the via and line were etched into the low-k dielectric followed by backfilling with a liner, a Cu seed, and electroplated Cu. The excess Cu and liner films were removed by chemical mechanical polishing process. The TaN/Ta liner and Cu seed layers were deposited sequentially by using physical vapor deposition (PVD). In addition, re-sputtering leads to excellent side wall coverage and void-free vias. Testing was typically conducted at 300^{o}C with a current density of 1.2~2.0x10^{6} A/cm^{2}. The EM failure

criterion was defined as a 10% increase in resistance, or when the extrusion monitor current exceeded 1 μA. Figures. 1(a)-(b) are schematic diagrams of the three-level interconnect structures discussed in this paper. The line length was designed to be 400 μm long to minimize the effect of EM induced back flow. The down-stream case is defined according to the electrons flowing from the upper wide metal line over the via into the narrow metal line below. While, the up-stream case is defined according to the electrons flowing from the lower wide metal line under the via into the narrow metal line above. The sample size per EM test was greater than 20. Stress temperatures were in the range of 250 to 350^{o}C (typically 300^{o}C).

5.3 Results and Discussion

5.3.1 The via/line configurations on EM performance.

EM test structure of various widths were designed to evaluate the effects of width scaling on EM performance. The direction of current used to apply the stress had a marked effect on EM results in the via-terminated three-level metal line structure and related failure modes. In order to examine the worst case EM performance, the structures were tested using currents applied in both directions. As can be seen in Fig. 5.2, the up-stream results for two different metal line widths showed a much better EM lifetime performance than in the down-stream case from. The following EM results in this work are stressing in down-stream current direction. The cumulative lifetime data for lines 0.14 μm to 0.42 μm in width, fitted using a lognormal distribution, is shown in Fig. 5.3, and the values of σ in the lognormal distributions, even in wider lines, are all quite similar. The median time to failure (MTF) was measured at different line widths, and the results are plotted in Fig. 5.4(a). The MTF decreases sharply as the line width increases in the range below 0.42 μm. Voids, which grow at the bottom of a via, cause the line to fail [5.7]. Due to large current crowding, and the lack of liner redundancy, design rules that allow maximum width with a single via show the worst MTF result. The maximum current allowed to pass

through the interconnects defined by the EM rule is proportional to the width of the line, while the maximum current allowed to pass through individual via is defined per via. As the line width increases to a point that allows current of line to be larger than allowed to pass through the via, the MTF will be restricted by the via current limitations. To remove the restriction on the current imposed by the via-limit on wide lines, dual vias are designed to relieve the via-related failure mode. For 0.42 μm wide lines, three different via arrangements were designed, i.e. a rectangular via, a dual via-row, and a dual via-column. The MTF increased by more than three times when compared to a single via structure. The variation of the MTF for different dual via designs is shown in Fig. 5.4(b). It is obvious that for wide lines with a dual via-row, which are parallel to the line length, the MTF is the longest due to the requirement for a large volume of Cu depletion. The MTF of the rectangular via decreases around 20% compared to that of a dual via-row. However, the width of the lines beneath the test structure can be decreased for the rectangular via, which is a trade-off between reliability and line routing design area. For a 0.14 μm narrow line, the MTF of the dual via-row is around 1.6 times that of a single via. In comparison with a 0.42 μm wide line, the MTF of a dual via-row increases to 4.6 times that of a 0.42 μm wide line with single via. It is interesting that for structures using a dual via design, the MTF of a 0.42 μm line is very close to that of a 0.14 μm line. The via-limit restriction on allowed current passing line, the case where a single via limits the EM performance in a 0.42 μm wide line, are eliminated. The via-related fails will not contribute to the current carrying capability for lines. The results indicate that the via/line configuration has remarkable impact on the current carrying capability in interconnects system. The via/line contact configuration needs to be evaluated for layout design.

5.3.2 The microstructure grain size of Cu.

The grain sizes were revealed by FIB in dual-damascene lines with the geometry of electromigration patterns. The microstructure of Cu in line trenches can be very different from

that of a blanket film since the grain growth is confined by the width of the trenches. The microstructure of Cu must be quantified as dual-damascene lines. Fig. 5.5(a) show top view FIB images of 0.14 μm, 0.42 μm and 1 μm wide EM patterns lines. A bamboo-like microstructure was found in the 0.14 μm lines, while a mixture of bamboo-like and polycrystalline structure was found in the 0.42 μm wide lines. The wide lines (1 μm) show a polycrystalline line structure where many grains coexist in the line width. The average grain size and dispersion were calculated for various line widths, and a lognormal distribution of grain size was assumed, using a mean lineal intercept, or Heyn's technique. The mean lineal intercept length is the average length of a line segment that crosses a sufficiently large number of grains. An example of a lognormal plot of the grain size for various widths of electroplated Cu lines is shown in Fig. 5.5(b). They are quite well lognormal distributed. Table 5.1 summarizes the medium grain size and standard deviation for each sample investigated. The median grain size decreases when the line width is smaller than the grain size. However, median grain size values can be larger than the width of the line, such as a value of 0.3 μm observed in the 0.14 μm Cu lines. A quasi-bamboo microstructure was also observed in narrow lines. Although different line widths show various grain sizes, the MTF shows a weak width dependence. These results further confirm that microstructure does not play a dominant role in Cu electromigration if the via-limited issue is eliminated. For line widths larger than 1 μm, the media grain size decreases slightly, and the value is very close to 1 μm.

5.3.3 The behavior of EM MTF on wide line regions.

The cumulative lifetime data for the 1 μm to 3.5 μm wide lines are shown in Fig. 5.6, and the values of σ, even in wider lines, are all about 0.3. The failure mode remains unchanged. SEM images illustrating failure samples for 1.68 μm are shown in Fig. 5.7. The images for various samples show almost the same void size. The void shape indicates that the void probably

started at the first via, and then continued to expand until it reached the second via. Here, the bottom of the vias is exposed, and an instantaneous fail is shown on the relative resistance plots, or line failed by open-circuit failure. No voids were found to have formed directly under the via bottom, such as a very thin slit void. It is reasonable to assume that EM lifetime does not degrade by via-limited issue. The TCR value was found to increase monotonically with linewidth, but reached a maximum where w ~ 1 μm and then slightly decreased to a constant value, as shown in Fig. 5.8. Since the thickness of the electroplated Cu film before CMP is 1μm, the grain size is limited by the deposited Cu thickness rather than by the metal width. The MTF as a function of linewidth is plotted in Fig. 5.9. The MTF slightly increases with linewidth w, but reaches a maximum where w ~ 1μm and then sharply decreases to a minimum where w ~3.5 μm. Where w > 3.5 μm, the MTF slightly increases to a constant value. The observed width dependency behavior can be explained by the equation below. For polycrystalline line structures, the Cu drift velocity can be written as Eq. 5.1 [5.8]:

$$V_d=[(\delta_{GB}/d)(1-d/w)D^0_{GB}e^{(-QGB/kT)}Z_{GB}^{*}+\underline{\delta_S(1/h)D^0_S e^{(-QS/kT)}Z_S^{*}} +\underline{\delta_I(2/w+1/h)D^0_I e^{(-QI/kT)}Z_I^{*}}]e\rho j/kT \quad (5.1)$$

where the subscript GB, S, and I refers to the grain boundary, surface, and metal/liner interface; respectively, δ_{GB}, δ_S, and δ_I denotes the width of the grain boundary, surface, and metal/liner interface; respectively, d is the grain size, and h is the thickness. The mass transport contribution along metal/liner interface is very smaller (10x~100x) than that of through the surface [5.9], so this term can be neglected. The surface diffusion velocities are almost the same for all large w regions. However, for w=1 μm in GB diffusion term, the grain size d ~ 1 μm, so the grain boundary diffusion term can be neglected. As a result, the MTF reaches a maximum where w ~ 1 μm. Since d is almost the same in the w > 1μm range, as w increases, the impact of grain boundary diffusion on EM will increase. The MTF sharply decreases to a minimum where w =3.5

μm. Thus we see once the Cu diffusion along the top surface is sufficiently slowed, the grain structure or interface boundary should affect reliability. The activation energy represents the energy barrier against the diffusive process resulting in electromigration. Different activation energies are associated with different diffusion paths in Cu interconnects. The plot illustrating activation energy (Ea) versus line width in Fig. 5.10 further supports the hypothesis. The activation energy where the dominant diffusion transport is the grain-boundary transport (width > 1 μm) is approximately 0.2 eV higher than that where surface mixed grain-boundary transport is dominant (width ~ 1 μm). Lower Ea value for w=1 μm, imply that the surface diffusion term has a significant contribution to mass transport induced by EM. When w > 5 μm, dielectric slots are automatically generated to prevent CMP dishing; EM induced atom diffusion will be scattered by the dielectric slot. As a result, the MTF will increase slightly for w=6 μm. However, EM behavior is completely different when w < 5 μm.

5.3.4 The theory of drift velocity on wide line region.

The relative resistance vs. time plots show that the line resistance slowly increases (delta resistance change <1%) for line widths larger than the 1 μm region, followed by an instantaneous rise. The instantaneous resistance increase occurred when the void grew and crossed the via bottom area, as shown in Fig. 7. As most sample failures are instantaneous mode, the void size is approximately equal to the spacing between the vias plus the width of each via. A long line dimension (length=400 μm) was used in the present study, thus the effect of the EM induced back flow on the drift velocity at the cathode end can be ignored. The drift velocity of Cu is directly related to the rate of displacement and can be obtained as $v_d=\Delta L/\Delta t$. The Cu drift velocity was estimated using $\langle\Delta L\rangle/\langle\tau\rangle$, assuming a constant drift velocity, where $\langle\Delta L\rangle$ and $\langle\tau\rangle$ are the mean void size and mean lifetime, respectively. We assume that $\langle\Delta L\rangle$ is approximately equal to the spacing between the vias plus the width of each via, and $\langle\tau\rangle$ is equal to the MTF.

Figure 5.11 shows the mean Cu drift velocity $<v_d>$ as a function of line width (w) and sample temperature (T). It is interesting that drift velocity increases as line width increases especially at high temperature while slightly increases to a constant value when the sample temperature decreases. According to the Ea measurement shown in Fig. 10, higher Ea value was obtained on wider line width. It is clear that larger Ea yields higher drift velocity especially at higher temperatures. Because the drift velocity is related to the product of mobility and driving force and uses Nernst-Einstein relation, $\mu = D/kT$, where μ is mobility, D is diffusivity, T is the test absolute temperature, and k is Boltzmann constant. It can be obtained as $v_d = \mu F = (D/kT)F$, where F is driving force, and diffusivity $D \sim \exp(-Ea/kT)$. The phenomenon probably is that gain-boundary density increase creates more flux divergence sites, which induce the void nucleation and formation quickly. The lines are the least-squares fits of the data to Eq. (1). The film thickness (h=0.25 μm), and the value of $e\rho j/kT$ are known. For line widths larger than the 1 μm region, the grain size d is very close to 1 μm since the thickness of the electroplated Cu file before CMP is 1 μm. Eq. (1) can be simplified to

$$V_d = [A\ (1-1/w) + B\ (4)]e\rho j/kT \tag{5.2}$$

where

$$A = \delta_{GB} D_{GB} Z_{GB}^* \tag{5.3}$$

and

$$B = \delta_S D_S Z_S^* \tag{5.4}$$

The solid lines shown in Fig. 5.11 are the least-squares fits and the best values of fitting parameters (A and B) are extracted. A careful inspection of Fig. 5.11 shows that error of least-square fitting for a low sample temperature is smaller than that of a high sample temperature. The ratio of B/A increases as the sample temperature decreases with a value range of 0.03 to 0.1. This implies that the surface diffusion contribution to mass transport induced by EM increases as

the sample temperature decreases. It should be noted that the interaction of grain boundary and surface diffusion is temperature dependence. In practice, electromigration assessments are based on tests conducted at accelerated conditions (i.e., high temperature and current density), which are then scaled back to use conditions. A model proposed here indicates that grain boundary diffusion dominates for wide lines at high temperature and surface diffusion contribution to mass transport increases as temperature decreases. It is difficult to predict precisely lifetime at operating conditions without clear relationship between grain boundary and surface diffusion. There is room for further investigation that the top surface diffusion will be the dominant mechanism at operating conditions. The extracted values of fitting parameters from the data in Fig. 11, $\delta_{GB}D_{GB}Z_{GB}*\rho j$ and $\delta_{S}D_{S}Z_{S}*\rho j$, as a function of e/kT are plotted in Fig. 5.12. The activation energies of surface and grain-boundary diffusion are estimated to be 0.92 eV and 1.45 eV, respectively. The derived value of activation energy for grain-boundary diffusion is in favorable agreement with the value of $w > 2$ μm in Fig. 5.10. This indicates that the major void growth is due to the grain-boundary diffusion for the polycrystalline wide line (w>2 μm). The derived value of activation energy is also very close to the reported value of 0.9 eV (Ref. 9) for the activation energy of surface diffusion. The derived activation energy of grain-boundary is found to be 0.5 eV higher than that of the surface diffusion. In comparison, the activation energy for the dominant grain boundary transport (width >1 μm) is approximately 0.2 eV higher than that of the surface and grain-boundary transport (width ~ 1 μm) from Ea measurement. This result further confirms that the grain-boundary term has significant contribution to mass transport induced by EM for the wide line (w>2 μm) region, while the grain-boundary transport contribution decreases at line widths of around 1 μm. It follows from what have been demonstrated that it is consistent with the data and proposed model.

5.4 Summary

In conclusion, the effect of line widths on electromigration in dual damascene Cu interconnects has been investigated. The via/line configuration has remarkable impact on the current carrying capability in interconnects system. The via/line contact configuration needs to be evaluated for critical layout designs. Width scaling was adjusted to improve reliability. There are two scenarios for width scaling. One is the w<1μm region, in which the MTF shows a weak width dependence, except for the via-limited condition. The other is the w>1μm region, in which the MTF shows a strong width dependence. The observed EM behavior was well explained by a proposed theory. The derived value of activation for grain-boundary diffusion is approximately 0.5 eV higher than that of surface diffusion. This study may lead to a better understanding of the effects of width scaling and may provide some contribution to the development of line routing for robust EM designs

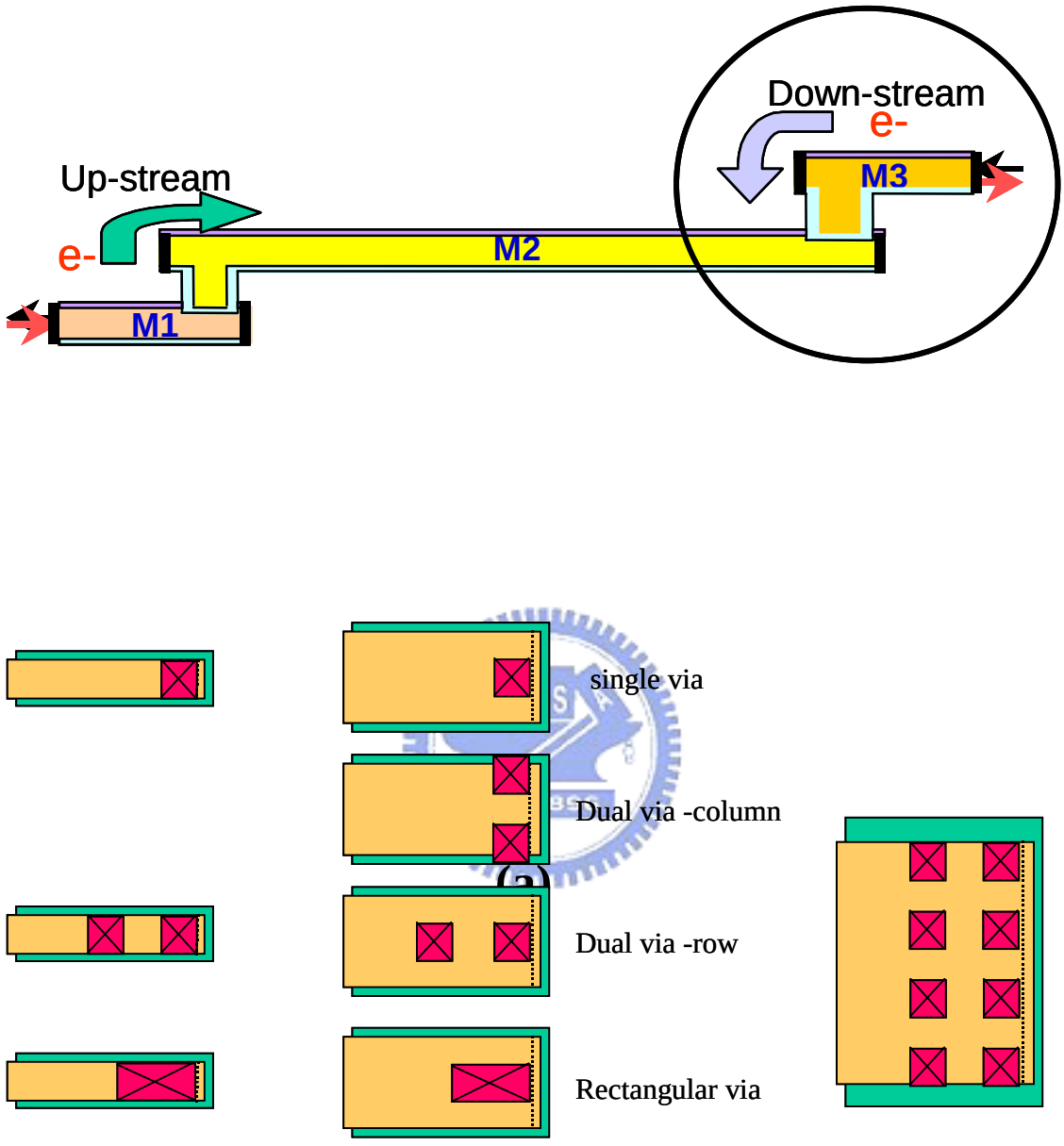


Fig.5.1 Schematics of EM test structures used (a). Via terminated line structure. Line length is equal to 400 μm. (b). Various EM structures for width dependence, left w=0.14 μm, middle w=0.42 μm, right w>0.42 μm. Stress direction is defined by electron current flow direction. Down-stream is evaluated.

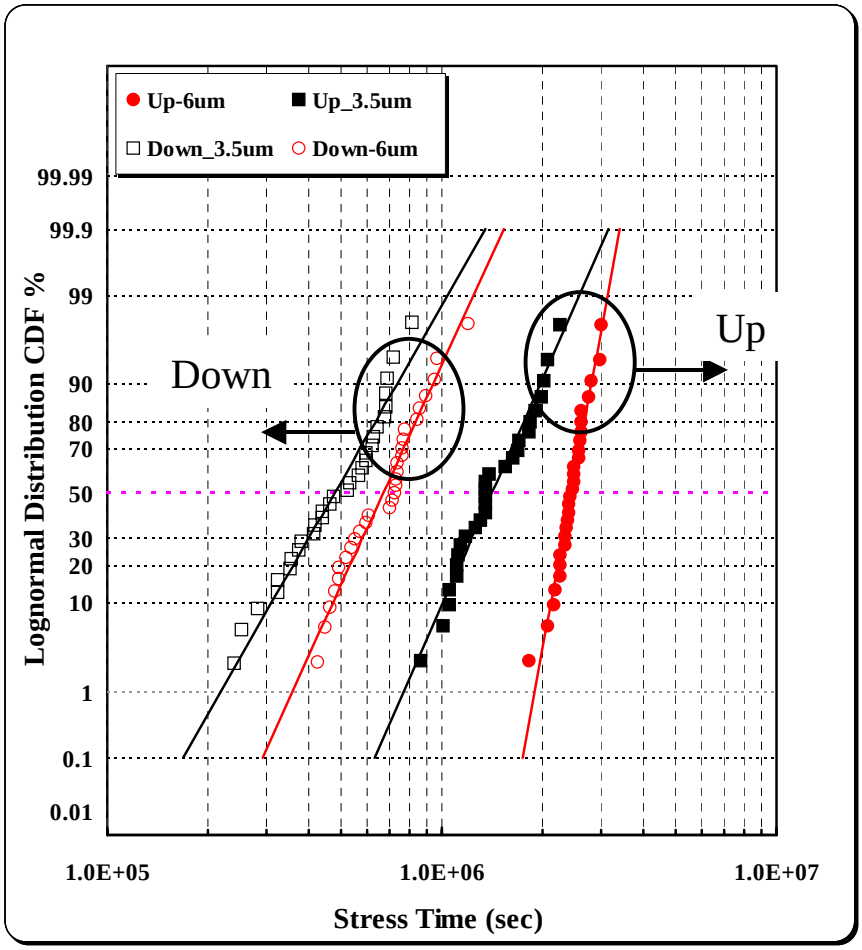


Fig.5.2 Typical Time-To-Failure distribution plots for Up-stream and Down-stream cases. The sample size is more than 24 for up-stream/down-stream case. EM fail time obtained at 300°C under current density of 1.6 $\times 10^6$ A/cm^2. The worse case is down-stream direction.

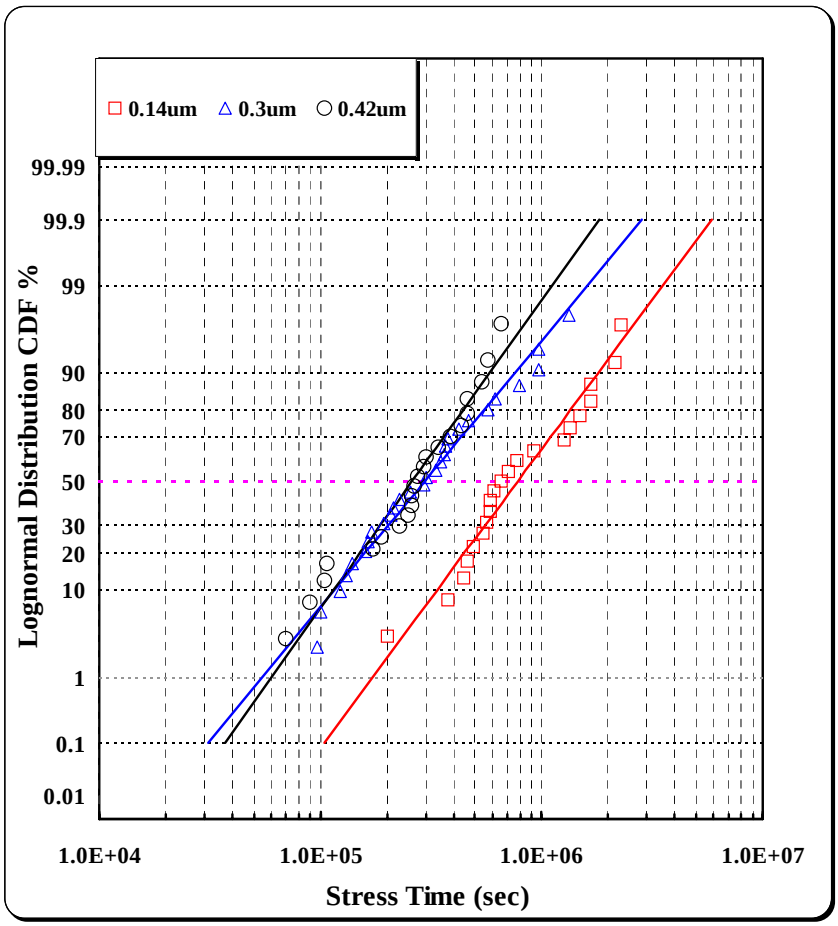


Fig.5.3 Lognormal time-to-failure distribution plots for w=0.14, 0.3, 0.42 μm for down-stream case. Similar distributions are shown. Stress conditions are the same for all tests

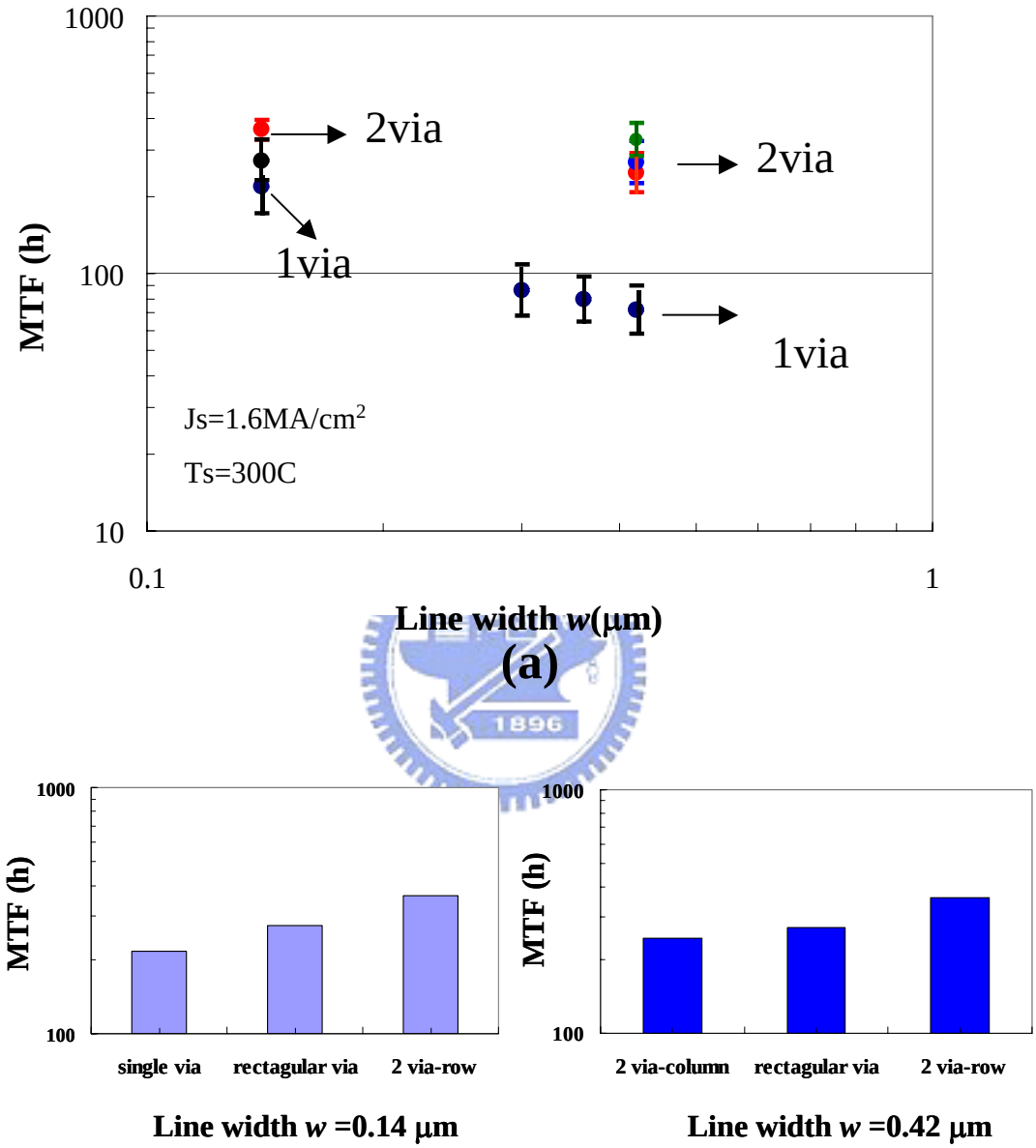


Fig.5.4(a) (a). Plot of the MTF as a function of linewidth (w< 0.42 μm), 90% confidence levels are lower and upper bound. (b). Plot of the MTF of different via/line configurations for 0.14 and 0.42 μm, stress conditions are the same for various structures.

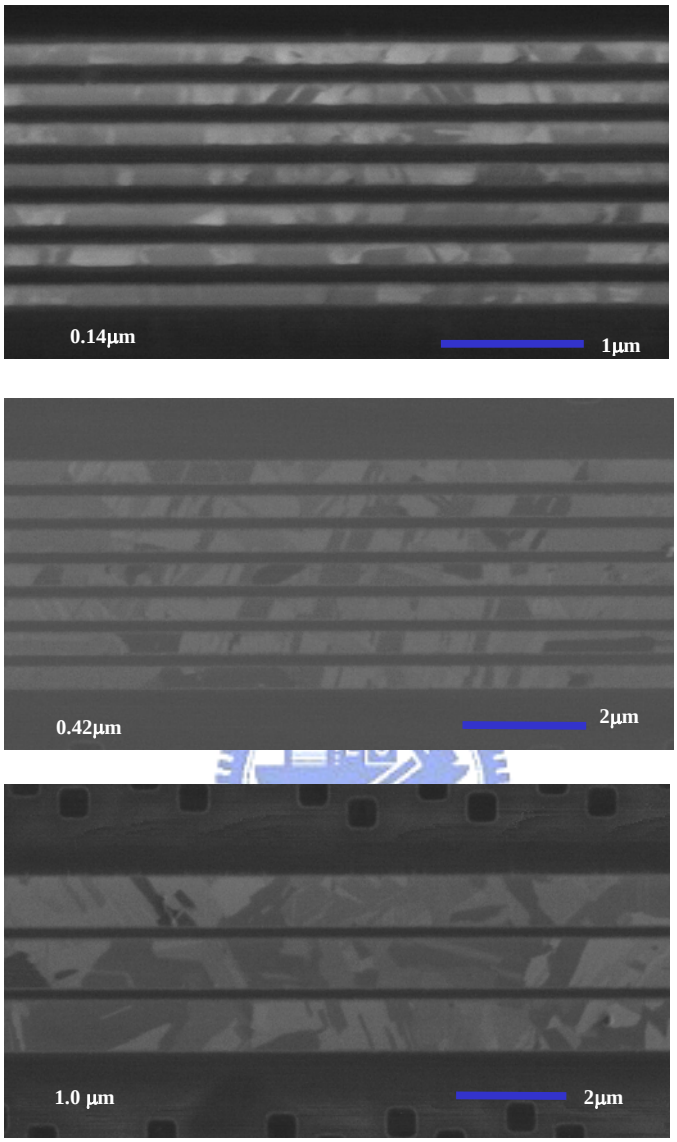


Fig.5.5(a) FIB images of 0.14 μm(top), 0.42 μm(middle) and 1.0 μm(bottom) EM structures, bamboo like and mixture microstructure are shown.

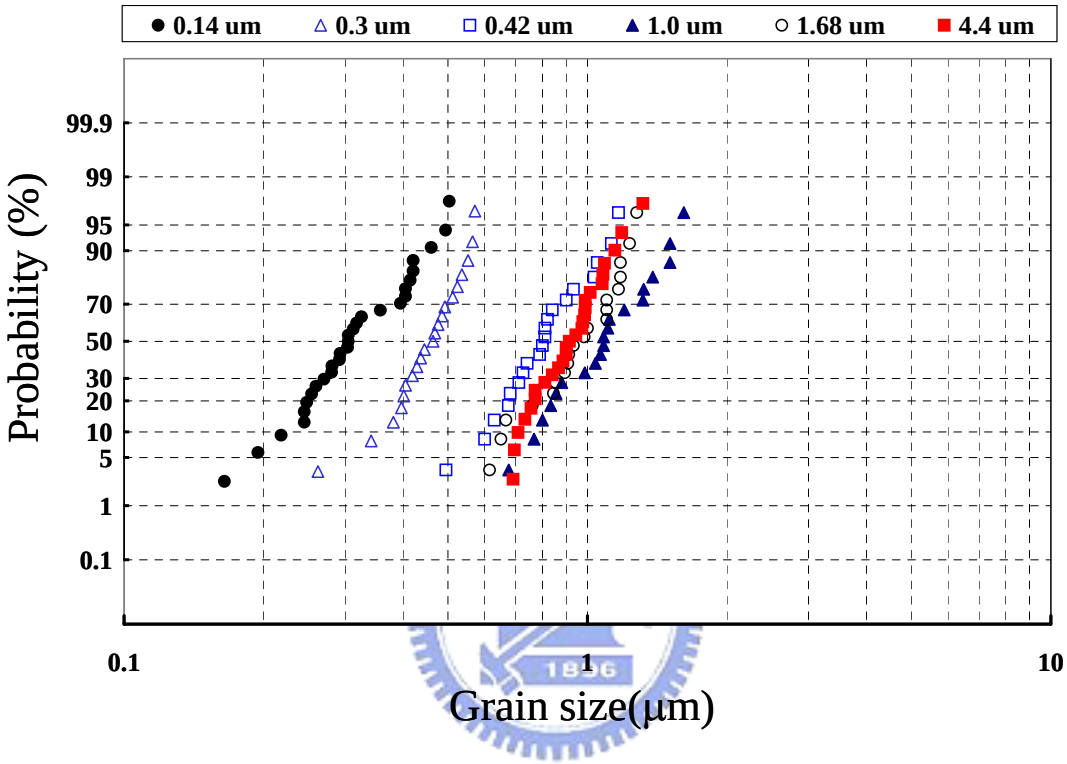


Fig.5.5(b) Grain size distribution versus line widths.

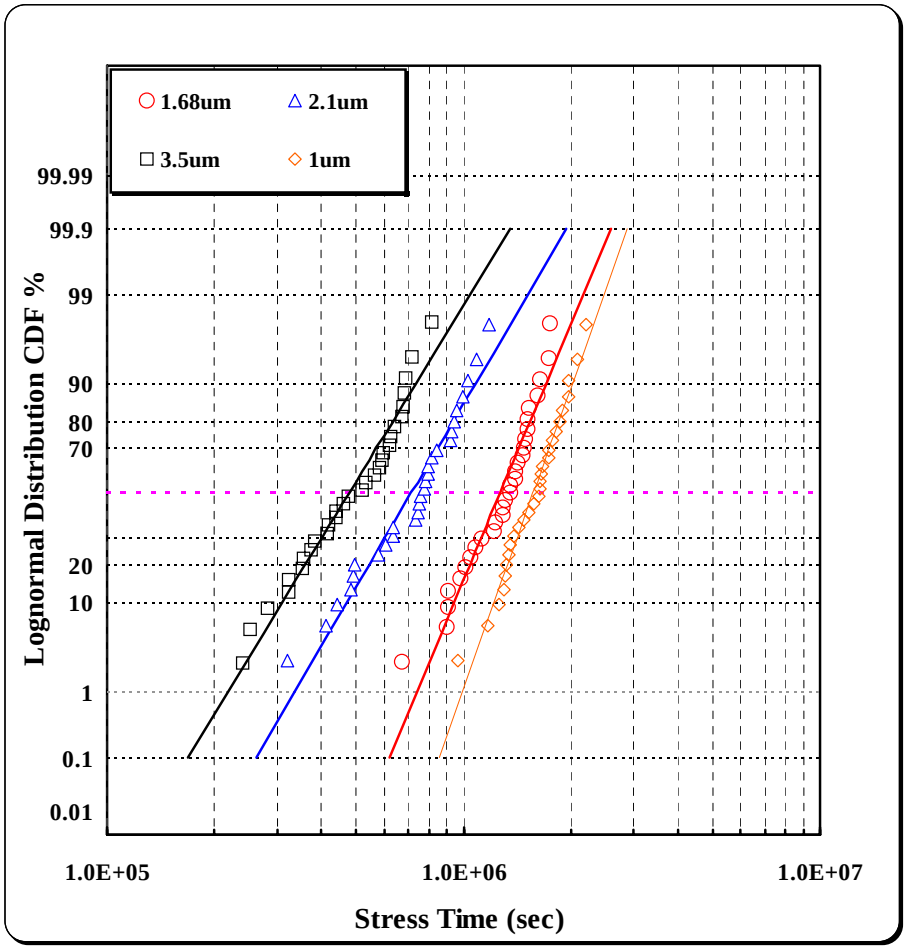


Fig.5.6 Lognormal time-to-failure distribution plots for w=1, 1.68, 2.1 and 3.5 μm for down-stream case. Similar distributions are shown. Stress conditions are the same.

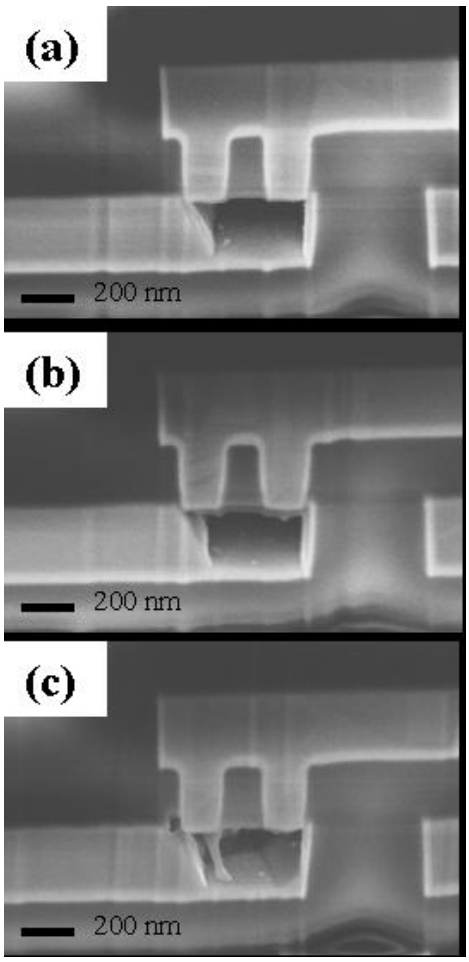


Fig.5.7 SEM images for w=1.68 μm wide line structure. Void was found in via bottom. Large trench void cross other via is depleted. The bottoms of the vias are exposed. (a)-(c) represent different failure samples.

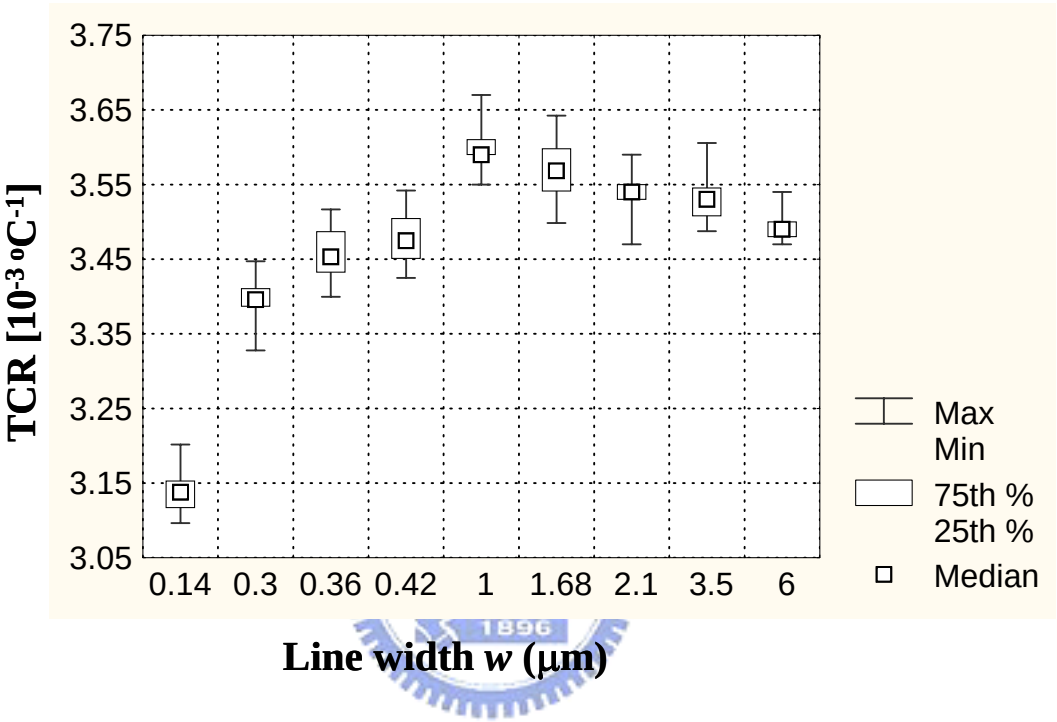


Fig.5.8 Plot of TCR as a function of line widths. It reaches a maximum at $w \sim 1$ μm and then slightly decreases to a constant value.

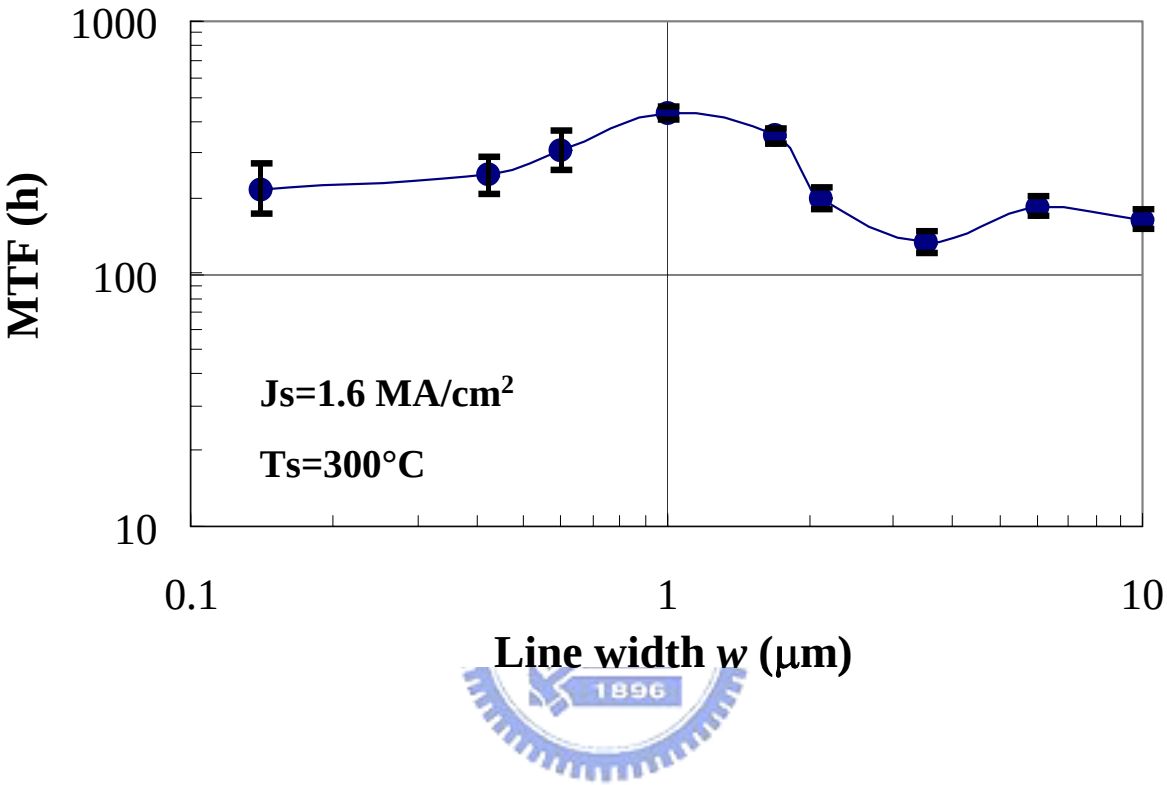


Fig.5.9 Plot of the MTF as a function of line widths. 90% confidence levels are lower and upper bounds. For w>0.42 μm, sufficient vias are designed to relieve the via-limited issue. Stress conditions are the same.

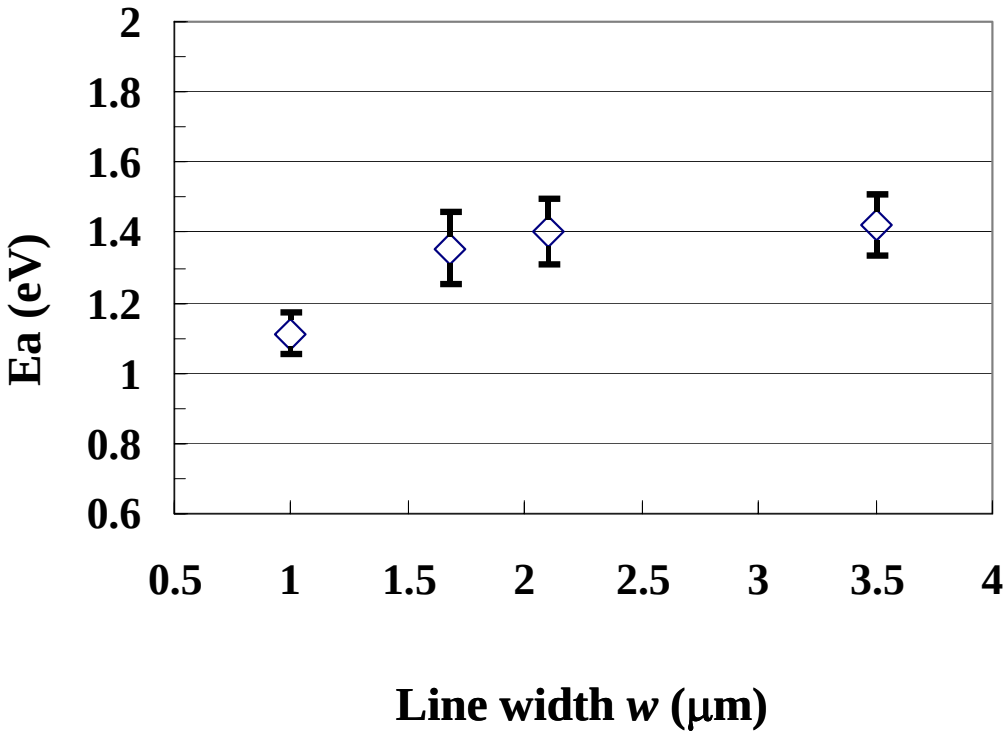


Fig.5.10 The activation energy Ea as a function of line widths..

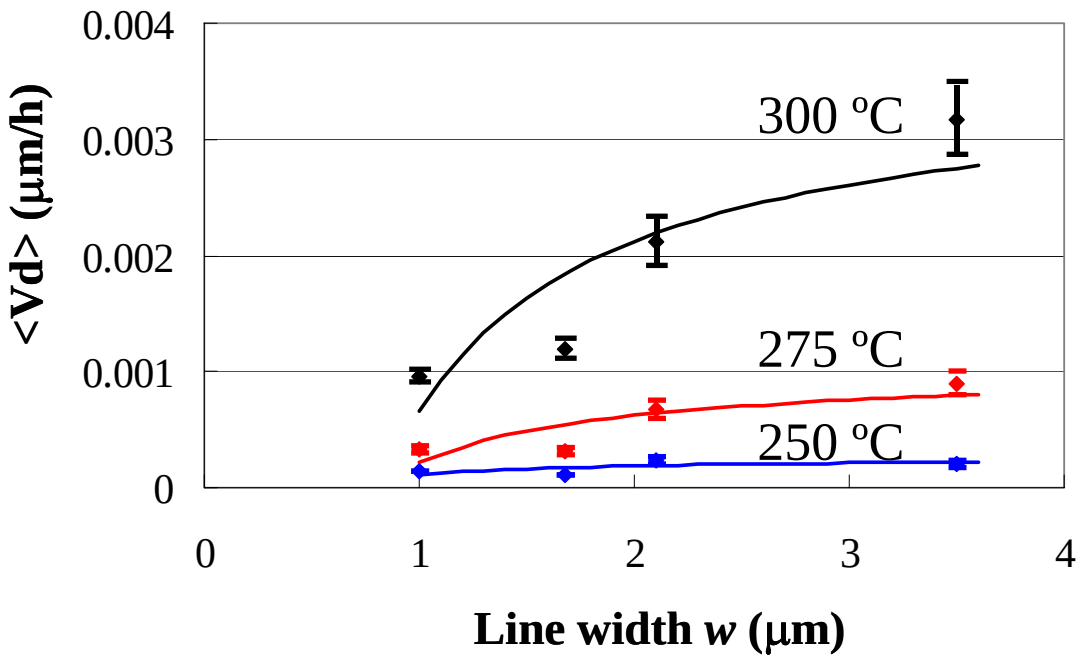


Fig.5.11 Plot of mean Cu drift velocity under EM stressing as function of line widths and sample temperatures. The solid lines are least-square fitting.

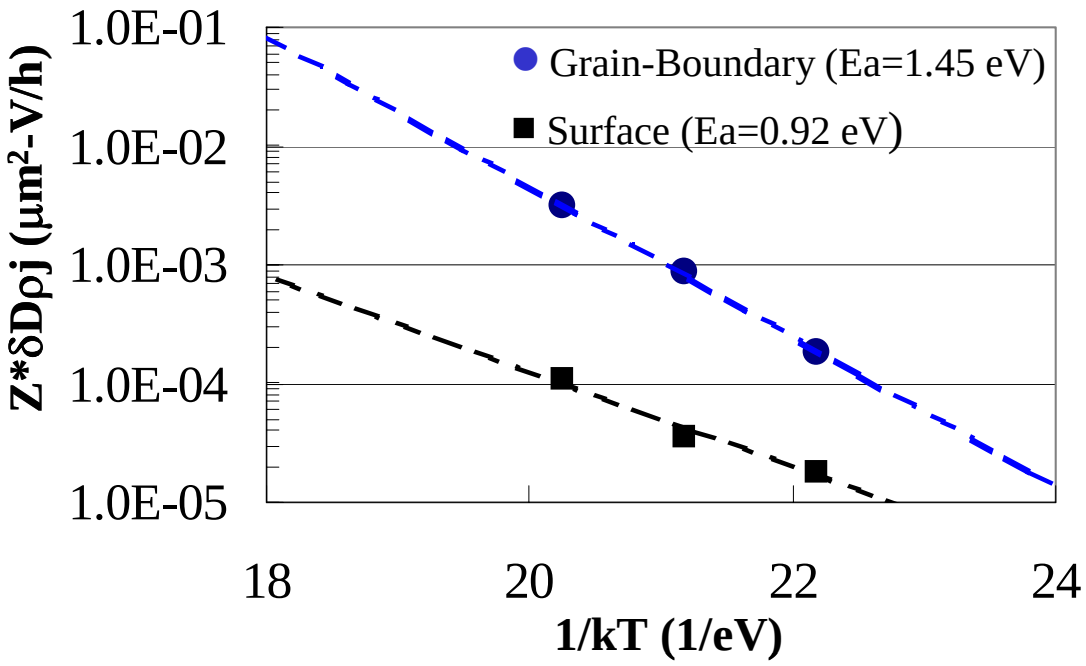


Fig.5.12 Plot of $Z_S*\delta_S D_S \rho j$ and $Z_{GB}*\delta_{GB} D_{GB} \rho j$ as function of $1/kT$. The solid lines are least-square fitting.

TABLE 5.1 Median grain size (probability=0.5) (D) and standard deviation (σ) versus metal line widths

Linewidth(μm)	D(μm)	σ
0.14	0.30	0.09
0.30	0.46	0.08
0.42	0.80	0.18
1.00	1.08	0.27
1.68	0.96	0.20
4.40	0.91	0.16

Chapter 6

Blech Effect on Dual-Damascene Copper Interconnect

6.1 Preface

In the past 30 years, it has been found that shorter Al wires are substantially less susceptible to EM damage than longer lines when stressed under the same conditions. This is called the short-length or Blech effect [6.1]. Blech reported that the electromigration flux transports atoms toward the anode, where the compressive stress, as well as the atom concentration, accumulates. This accumulation increases the chemical potential of Al to such a level that further transport of the atoms to the anode is impossible. In other words, the electrical driving force is balanced by a compressive stress gradient, which causes an equal but opposing driving force. The atomic flux (J) is the result of two opposing driving forces. The net atomic flux is expressed as follows:

$$J = C\frac{D}{kT}\left(Z^{*}ej\rho - \frac{\Omega\Delta\sigma}{L}\right) \tag{6.1}$$

where C is the concentration of atoms, D is the diffusivity, *k* is Boltzmann's constant, T is temperature, Z* is the effective charge number, *e* is the fundamental electric charge, ρ is the electric resistivity, j is the current density, Ω is the atomic volume, Δσ/L is the EM-induced average stress gradient between the anode and the cathode, and L is the metal line length. From Eq. 6.1, the first term is the electron wind force that moves the ions in the direction of the electron flow, and the second term is the back-stress that pushes the ions in the opposite direction. Once the back-stress gradient balances the EM-driven force, there is no net mass transport. The critical current density and line length product is given by:

$$(jL)_C = \left(\frac{\Omega\Delta\sigma}{Z^{*}\rho}\right) \tag{6.2}$$

Then, Eq. (1) can be further rearranged as

$$J = C\frac{D}{kT}Z^{*}e\rho\left[jL-(jL)_{C}\right]\frac{1}{L} \tag{6.3}$$

Blech also found that $(jL)_C$ is a constant for a given temperature and increases at decreasing temperatures in a range of 200-350^{o}C on Al films.

A question remains whether Cu dual-damascene interconnects exhibit a short-length effect. A reasonable argument was proposed to dispute the validity of this effect [6.2]. The dual-damascene Cu via is connected to the metal (M2) trench above and separated from the metal (M1) trench below by a thin diffusion barrier to form a flux divergence. A very small mass material depletion at the cathode via may cause an open circuit before a substantial back-stress develops at M2. In this case, the short-length effect would not occur, causing a serious interconnect design complication for dual-damascene Cu process microelectronics [6.3]. However, the Cu/cap dielectric interface is the dominant diffusion path in Cu damascene interconnects; mass transport in the trench along the interface can surpass via bottom depletion such that steady-state back-stress development will counteract EM-induced via or line failure. The short-length effect will then occur, but the criteria will require conditions that allow sufficient time for significant mass transport prior to steady-state back stress. An experimental complication exists because of potential EM damage in the dual-damascene Cu via/line interface where the weak point may require very little EM-driven material depletion at the cathode via prior to steady-state back stress development [6.4]. The elecromigration short-length effect depends critically on sample configurations and processing. The early failure rate at the via/line interface must be minimized in order to demonstrate this phenomenon. These concerns have provided the impetus for this investigation into the short-length effect on an electroplated Cu dual-damascene process.

In this chapter, the short-length effect on a dual-damascene Cu process and its temperature dependence was investigated by using a technologically realistic three-level interconnect

structure. The dual-damascene Cu process was optimized for mass production following high quality integration development. It will be shown that the median-time-to-fail (MTF) at relatively small current densities does not obey Black's empirical equation [6.5]:

$$MTF = Bj^{-n_1} \exp(\frac{Ea}{kT}) \tag{6.4}$$

where B is the material and geometry constant, and n_1 is the current density exponent. Rather, the MTF data appears to obey a modified Black's empirical equation [6.6].

$$MTF = C(j - jc)^{-n_2} \exp(\frac{Ea}{kT}) \tag{6.5}$$

where C and n_2 are analogous to B and n_1 in Eq. (4), and j_C is the critical current density. However, this modified Black's empirical equation cannot be used to extract j_C due to the dependence of the log-normal sigma or shape factor parameter on the current density. As an alternate means of determining the threshold–length product $(jL)_C$ value, a model that relates it to the failure volume and atomic flux is proposed. Moreover, this alternate method allows j_C to be estimated. A higher threshold-length value was obtained at 300°C compared to previous works. A test was performed for a greatly extended time period to examine the extracted $(jL)_C$ values and verify the immortality of Cu/low-k interconnects.

6.2 Experimental Detail

The EM tests were carried out at the package level. Samples were fabricated using a 90 nm Cu dual damascene process on 300 mm wafers. The process flow of testing sample is similar with the sample in chapter 5. The EM failure criterion was defined as a 10% increase in resistance, or when the extrusion monitor current exceeded 1 μA. Figure. 6.1 is a schematic diagram of the three-level interconnects structure discussed in this paper. Line lengths from 5 μm to 400 μm were used to examine the effect of EM induced back flow. The down-stream case was defined as

a condition where the electrons flow from the upper wide metal line over the via and into the narrow metal line below. More than 20 samples were used for each EM test. Stress temperatures were in the range of 250 to 350^{o}C (typically 300^{o}C).

6.3 Results and Discussion

6.3.1 The short length effect on TTF distribution.

It has been well-established that the back-stress force becomes stronger at lower current densities (j) and shorter line lengths (L) [6.7]. The maximum stress sustainable between the cathode and anode ends of a line is related to the mechanical strength of the interconnect material and the surrounding dielectric layer, which is related to the material properties, and is not dependent on the length of the metal lines. Therefore, the maximum stress gradient, and thus the back-stress force, is higher for shorter metal lines. As a result, the net EM flux and the rate of resistance increase are smaller for shorter metal lines. The EM critical length effect was evaluated using test structures of various lengths. The cumulative lifetime data for lines of 50 μm to 400 μm in length, fitted using a log-normal distribution, are shown in Fig. 6.2. The EM behavior of different line lengths was evaluated to reveal the influence of back-stress force on line length. The MTF and TTF distributions of the various line lengths are very similar. However, a careful inspection of the TTF distributions shows that the TTF of a 50 μm line is wider than that of other lines. The log-normal sigma parameter is a measurement of the variation in failure times. As failure times become more widely distributed, sigma must increase. The values of sigma in the log-normal distribution versus the jL^2 product are plotted in Fig. 6.3. The fitting curve is plotted using a statistical distribution of the critical void volume [6.8]. He *et al* reported that the void volume (V) is a function of time under EM stressing:

$$\frac{V}{V_{satu}} = 1 + \frac{32}{\pi^3}\sum_{n=1}^{\infty}\frac{(-1)^n}{(2n-1)^3}\exp\left[-\left(\frac{2n-1}{2}\pi\right)^2\frac{t}{\tau}\right] \qquad (6.6)$$

where $\tau = (L^2 kT)/(DB\Omega)$ and $V_{satu} = (AZ^*e\rho j L^2)/(2B\Omega)$, B is effective elastic modulus.

The fail data (t_i) is the time below which i percent of lines in a group fail lie, and the critical voids (Vi) is the volume below which i percent of the critical voids lie. The i percent of the critical voids (Vi) was obtained using Eq. 6.6. The constants $(kT)/(DB\Omega)$ and $(AZ^*e\rho)/(2B\Omega)$ in V_{satu} and τ were fitted using three sets of EM data (t_{50}, j, L) based on Eq. 6.6. These sets of t_{50s} were obtained from three structures where the line length (L) was equal to 50, 100, and 200 μm, and were conducted at 300°C with a current density of 1.6 x10^6 A/cm^2. The TTF data from the L=200 μm structure is used to calculate the Vi. He *et al* assume that Vi is independent of testing conditions and test structure lengths. Once the Vi was obtained, the t_i and sigma of $\ln(t_i)$ as a function of j and L can be predicted. The predicted and experimental sigma of $\ln(t_i)$ are plotted in Fig 6.3. The sigma for the experiment data shows an abrupt increase as jL^2 approaches zero, and remains constant as jL^2 increases. These results agree with the predicted model. A lower jL^2 product shows larger sigma values as a result of the back-stress-induced TTF dispersion. As the line length is increased to more than 200 μm, the sigma appears to decrease slightly. In order to avoid the Blech effect, the length of the EM test structure should be greater than 200 μm at a moderate stress current. A relative resistance versus time plot, shown in Fig. 6.4, further indicates that TTF dispersion is enhanced by back-stress force in line lengths below 50 μm. The relative resistance change becomes saturated at around 103% for L=25 μm, while an abrupt resistance change is shown for lengths greater than 100 μm. The change in behavior between the various lengths can only be the result of different rates of void growth. Since the results shown in Fig. 6.4 correspond to the same electromigration stress conditions, the first term of Eq. 6.1 can be assumed to be the same for the various lengths. Longer lines increase in resistance at a faster rate than shorter lines. This behavior implies that the net Cu drift velocity must increase as the line length increases, and can only occur if the second term of Eq. 6.1, the back-stress gradient, is smaller for longer lines in comparison to shorter lines. The results in the

present work show that the increase in resistance in long lines, i.e. the amount of EM-induced damage on resistance degradation, is higher than the increase in resistance in short lines. The results are consistent with the work of Korhonen *et al* [6.7], who theoretically showed that the EM-induced stress gradient in finite lines initially decreases from the region of accumulation. Only for longer times does the stress gradient approach a constant value. In addition, for a given time the stress gradient is smaller for long lines compared with short lines. Since it takes a longer time to reach a given back-stress gradient at the cathode end in longer lines, there will be more EM damage. When the opposing back-stress gradient approaches a constant value, the amount of EM damage begins to decrease. It can be noticed in Fig. 6.4 that the time of resistance onset (e.g. R increase of 1%) decreases as L decreases. A substantial back-stress force quickly develops in a short length line, which then suppresses increase in the resistance. The resistance saturation is a result of a reduction in the rate of EM damage because of the short-length effect. Two resistance evolution modes were observed. The percentage of abrupt open-circuit failures was found to decrease as the length decreases. As the length decreases to 25 μm, most samples show that the resistance gradually increases on time evolution. The length-dependent results seen in Fig. 6.4 are a direct result of the EM short-length effect, and is consistent with current knowledge of the EM short-length effect.

6.3.2 The Length scaling effect on n value.

The current exponent n value the Black's empirical equation Eq.(4) can be correlated to the failure mechanism on metal interconnects. It has been established through studies on Al interconnects that void-growth-limited failure is represented by a current exponent of 1 [6.9], while void-nucleation-limited failure is represented by a current exponent of 2 [6.10]. These concepts appear to be consistent in Cu interconnects where correlations were made between the n value and the failure analysis [6.11]. The n value increased significantly for shorter line lengths

[6.12,6.13]. Higher n values can be related to significant back-stress in shorter length lines. Figure. 6.5 shows a log-log plot of the MTF versus the current density-length product for 50 μm and 400 μm. The stress temperature is 300^{o}C. Fitting the MTF data for L=50 μm to Eq. (4), and assuming that the exponential term is constant, a linear regression yields a current exponent of $n_1 \approx 1.4$ for a high current density-length product, as indicated by the dashed line. This value is very close to the extracted value of 1.36 for L=400 μm. The observed n value (~1.4) indicates that certain lines in this population suffered failures that were void-growth-limited, while the failures in other lines were void-nucleation-limited. However, as the current density-length product is reduced, the data deviates from the fitting line, and Black's empirical equation is no longer valid (where B and n_1 are the two parameters). The MTF data for low current density-length products are better represented by a modified Black's empirical equation Eq. 6.5, which introduces a third parameter j_C. Equation 6.5 states that j_C is a critical current density. If the stress current density is below j_C, the samples will not suffer a failure. The solid line shown in Fig. 5 was obtained by fitting the MTF data for L= 50 μm to Eq. 6.5 with a least-squares nonlinear regression. The regression found that $(j_C L)$=6000 A/cm and n_2=1.2. The difference in the relationship between MTF and jL can be separated by a distinct boundary. One region (i) is the EM behavior following Black's empirical equation and has no significant back-stress. The other (ii) is EM behavior that can be better represented by a modified Black's empirical equation, and includes significant back-stress.

6.3.3 A model to determine the threshold-length

As an alternate means of determining the threshold–length product $(jL)_C$ value, a model that relates it to the failure volume and atomic flux is proposed. It is assumed that the electron flow is from the V2 via to the M2 line, the Ta/TaN liner at the V2/M2 interface stud acts as barriers against Cu diffusion, and the atomic flux divergence at the cathode end of the

interconnect is expected during EM. Once an electric current is applied to the line, the majority of its lifetime is taken up by expanding the void, while the time required to nucleate the void is neglected. When a period of time equal to the MTF, the depleted atoms occupy a volume equal to the failure volume, $V_{fail,}$, which is assumed to be independent of testing variables, such as electric current density [6.14], and is constant for the same line length. The MTF can be extrapolated using the following expression:

$$V_{fail} = JA\Omega * (MTF) \tag{6.6}$$

where J is the atomic flux as expressed in Eq. 6.1, A is the metal line cross-sectional area, and Ω is the atomic volume. Note that at a given temperature and metal line length, V_{fail}, A, and Ω are constants representing the material properties. In the assumptions made in this study, the MTF is inversely proportional to the atomic flux J. Therefore, Eq. (6) can be rearranged as:

$$1/(MTF) = A\Omega V_{fail} J \propto J = C\frac{D}{KT} Z^* e\rho[\, jL - (\, jL)_C\,]^{1}\!/_{L} \tag{6.7}$$

Similar relationships between the MTF with respect to the product of jL have been reported by others [6.15-6.17]. The threshold–length product $(jL)_C$ value can then be precisely determined. Figures 6.6(a)-(b) show the L/MTF versus the current density-length product. A linear relationship between (jL) and L/MTF is indicated by the linear extrapolation to zero. The intercepts with the *x* axis determined from the linear extrapolation are the $(jL)_C$ values that yield infinite MTF values. Therefore, these intercepts determine the threshold–length products, $(jL)_C$, below which there is no electromigration-induced resistance degradation at their corresponding temperatures. The threshold–length products, $(jL)_C$, determined from Fig. 6.6(a) are 10914 A/cm at 250°C, 10278 A/cm at 275°C, 6675 A/cm at 300°C for L=50 μm, and from Fig. 6.6(b) are 5806 A/cm at 250°C, 5530 A/cm at 275°C, 4314 A/cm at 300°C for L=25 μm. The value of $(jL)_C$=6675 A/cm at 300 °C for L=50 μm is consistent with the regression value (j_CL) =6000 A/cm from Eq. 6.5. In addition, to justify these $(jL)_C$ values, several experiments were conducted under stressing

conditions lower than the $(jL)_C$ values at their respective temperatures, e.g., 25 μm lines stressed at 1.6 $\times 10^6/cm^2$ and 300 °C. As expected, and shown in Fig. 6.7, for those stress cells below the threshold conditions, there is no major resistance degradation during an extended time period up to 5100 h, which shows that immortal behavior occurs when L=10 or 25 μm under these testing conditions. The resistance change is very small around 2 to 4%. For L=25 μm, the jL product at 300°C is 4000 A/cm, which further supports the proposed threshold–length extraction method and justifies the $(jL)_C$ values. Extensive failure analysis was carried out to reveal any potential failure mechanisms in the test structures. Figure 6.8(a) shows the FIB images of a metal line 10 μm in length after the passage of 1.6 $\times 10^6/cm^2$ for about 5100 h at 300 °C. No clear void was found at either the anode or cathode ends along the line. A high-resolution TEM was analyzed at the cathode end to reveal the detailed microstructure, as shown in Fig. 6.8(b), which shows that a very small void has formed at the cathode end, leading to only a minor increase in resistance. Figure 6.9 shows the FIB and TEM images of a metal line 5 μm in length after the passage of 1.6 $\times 10^6/cm^2$ for about 5100 h at 300 °C. The EM-induced void of the 5 μm line is much smaller than that of the 10 μm line. These results further support the hypothesis that mass transport in the trench along the interface is able to surpass via bottom depletion such that steady-state back-stress development will counteract EM-induced via or line failure. If (jL) exceeds the critical threshold–length product, void nucleation will occur, but is not necessarily fatal if the void does not completely separate the line from the via. Figure 6.10 is an example of a FIB cross-section at the cathode end of a 25 μm metal line. The void has partially exposed the bottom of the via, which likely represents a void-growth-limited failure, since a larger void size is required before the resistance increases to 10%.

6.3.4 Temperature dependence on Blech effect.

The temperature dependence of the threshold–length product is an important

consideration for determining critical current densities at standard operating conditions. The temperature dependence of the threshold–length product for 50 μm and 25 μm lines is shown in Fig. 6.11, and was found to be a function of the temperature. It is interesting that the jL value increases slowly at low temperatures for both lengths, which can be partly attributed to the temperature-dependent mechanical properties of the system [6.1,6.14] Note that the EM threshold-length product is critically dependent on sample configurations and processing, which in this study, was determined based only on the critical failure volume model. The activation energy was found to be 1.0 for the 50 μm line, which indicates no early failure mechanism affecting the result. It was also noticed that the $(jL)_C$ value needs to be obtained for the standard operating temperature that would be used in possible design implementations, typically around 100°C. A better understanding of the temperature dependence of the $(jL)_C$ is required. The discrepancy in the threshold–length product for 50 μm and 25 μm lines is not clear and will require further discussion. The dependence of the threshold-length product on the length is also shown in Al metallization, but the $(jL)_C$ value increases as the line length decreases [6.6]. The maximum stress difference in the interconnects for void nucleation was determined to be 400 MPa at 250°C. This value represents the tensile stress needed to nucleate a void in the metal. This value is larger than previously reported values, and may indicate differences in the quality of the Cu/cap interface. However, the value is much lower than the critical stress of 600 MPa observed for Al-based interconnect systems [6.18], which indicates that voids form much more readily in Cu- than in Al-based interconnects.

6.4 Summary

In conclusion, we have investigated the effect of line length scaling on electromigration in dual-damascene Cu interconnects by testing several three-level structures. Different line lengths were evaluated to reveal influence of the back-stress force on line length. The values of sigma in

the log-normal distribution versus the jL^2 product can be modeled using a statistical distribution of the critical void volume. A lower jL^2 product shows large sigma values as a result of back-stress-induced TTF dispersion. In order to avoid the Blech effect, the EM test structure length should be longer than 200 μm at moderate stress currents. A relative resistance versus time plot further indicates that TTF dispersion is enhanced by back-stress force at line lengths below 50 μm. Two resistance evolution modes were observed. The percentage of abrupt open-circuit failures was found to decrease as the line length decreases. As the line length decreases to 25 μm, most samples show that the resistance gradually increases over the time evolution. A direct result of the electromigration short-length effect was demonstrated.

The MTF at relatively low current densities does not obey Black's empirical equation. Instead, the MTF follows a modified Black's empirical equation in which MTF $\propto (j - jc)^{-n_2}$ at a constant temperature. The difference in the relationship between MTF and jL can be separated by a distinct boundary. One region (i) is the electromigration behavior following Black empirical equation and has no significant back-stress. The other (ii) is the electromigration behavior that can be better represented by a modified Black's empirical equation, and includes significant back-stress. As an alternate means of determining the threshold–length product $(jL)_C$ value, a model that relates it to the failure volume and atomic flux is proposed. The extracted values are consistent with the regression value from the modified Black's empirical equation, and these $(jL)_C$ value were verified during an extended stress test period. Extensive failure analysis shows that no clear void was found at the anode or cathode ends along the line if (jL) is below the critical threshold–length product, and was found to be a function of temperature. Since the $(jL)_C$ value needs to be obtained for the standard operating temperatures for possible design implementation, there is room for further investigation into the temperature dependence of the $(jL)_C$.

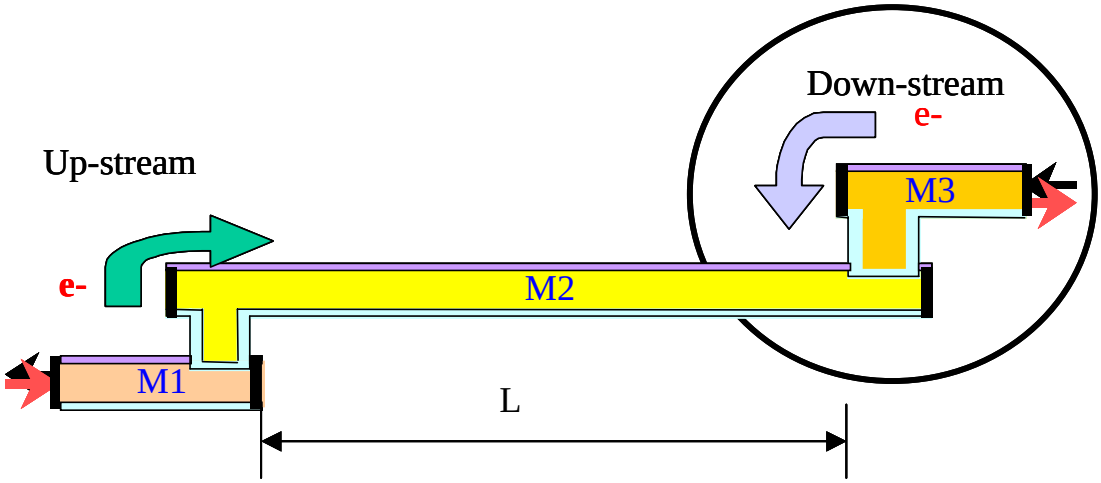


Fig.6.1 Schematic diagram of the 0.14 μm wide three-level via terminated line structure. The stripe length L is 5, 10, 25, 50, 100, 200, or 400 μm. Stress direction is defined by electron current flow direction. Down-stream is evaluated in this study

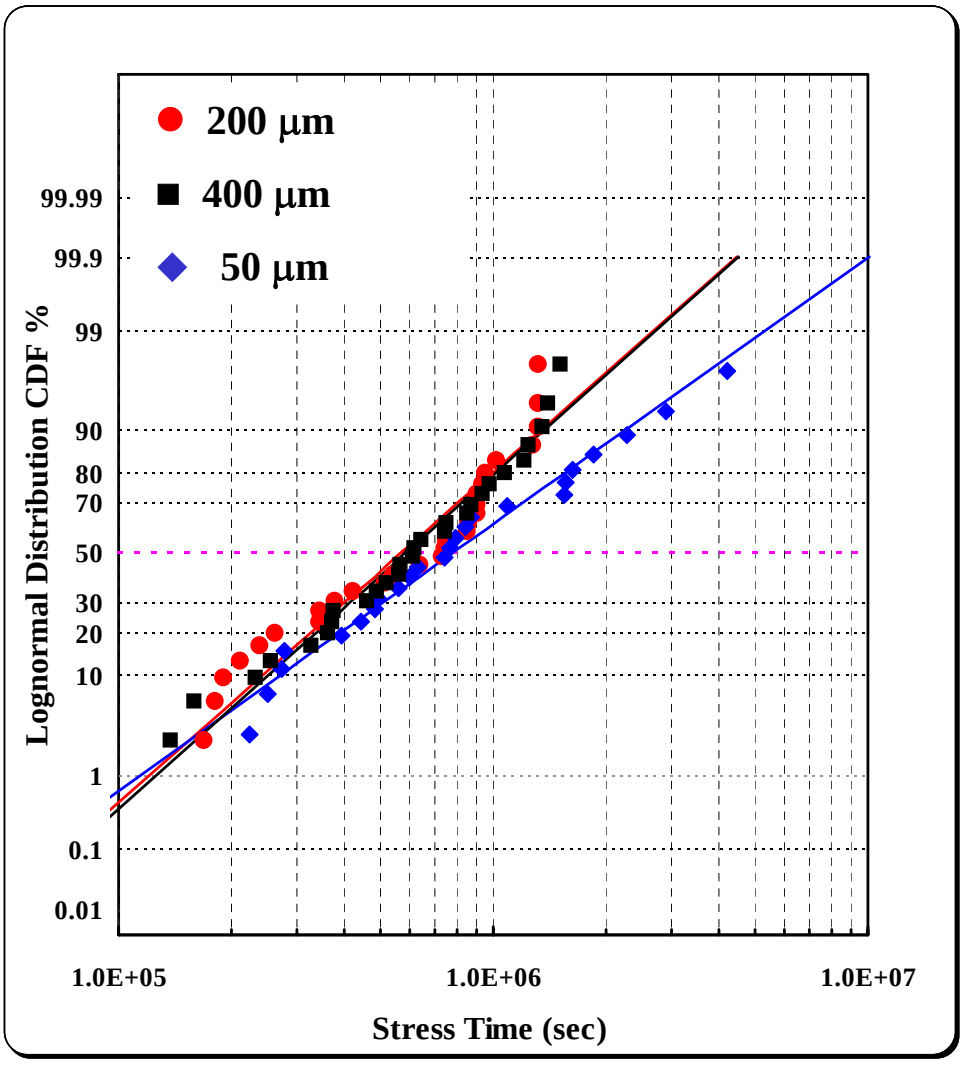


Fig.6.2 Log-normal time-to-failure distribution plots for L=50, 200, and 400 μm for down-stream case. Similar distributions are shown for 200 and 400 μm, but wider distribution was found for L=50 μm. EM fail time obtained at 300^{o}C under current density of 1.6 ×10^{6} A/cm^{2}.

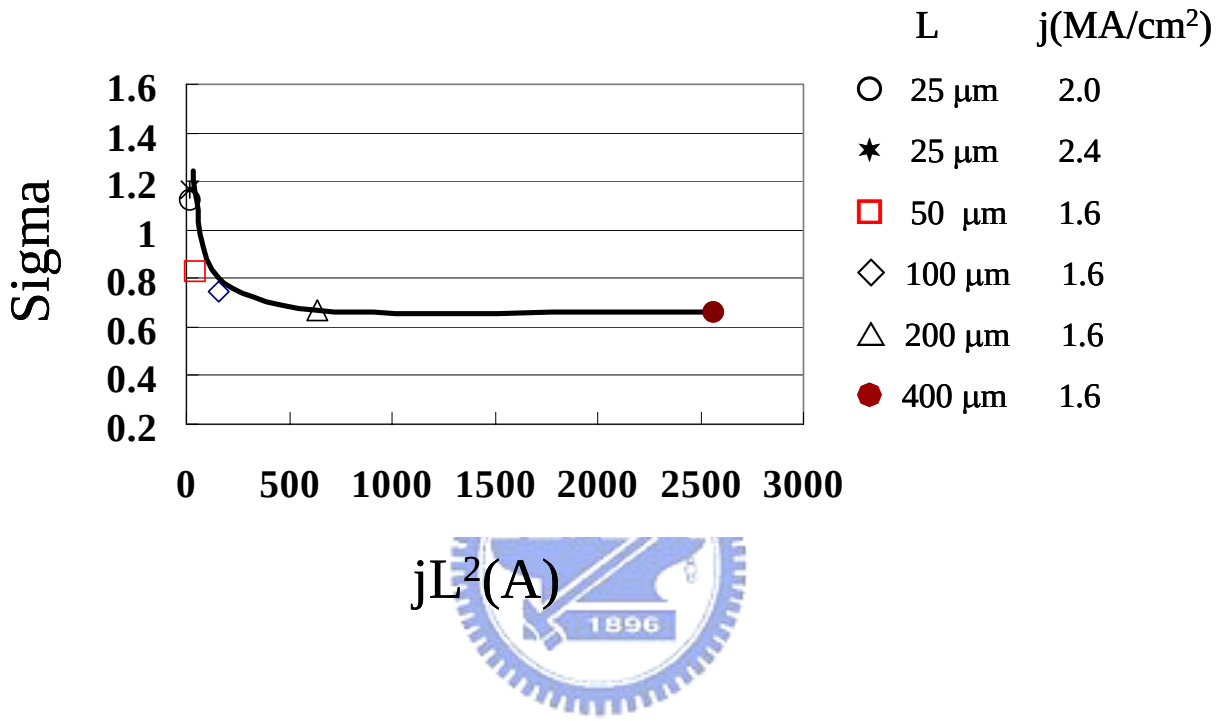


Fig.6.3 The sigma of log-normal distribution vs. jL^2. Smaller jL^2 values shows large TTF dispersion. The solid curve is plotted using the statistical distribution of the critical void volume.

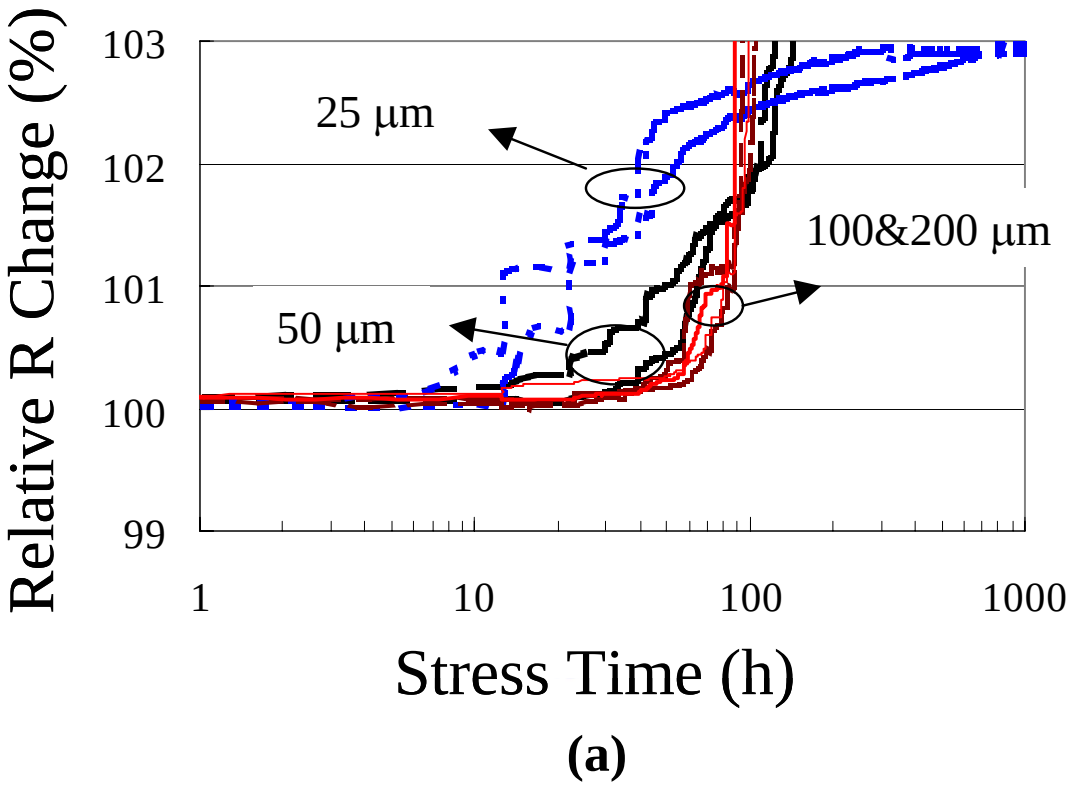


Fig.6.4 Relative R change vs. time plots for L=25, 50, 100 and 200 μm. Different resistance onset times are shown for various line lengths. Stress conditions are the same..

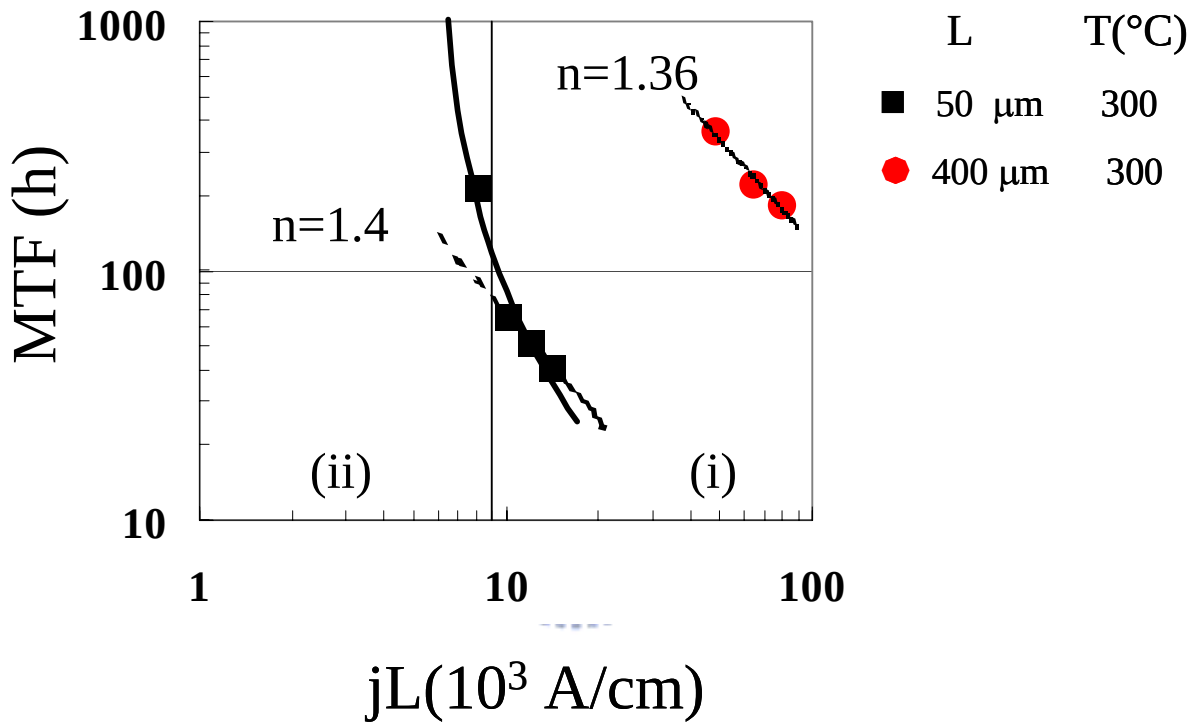
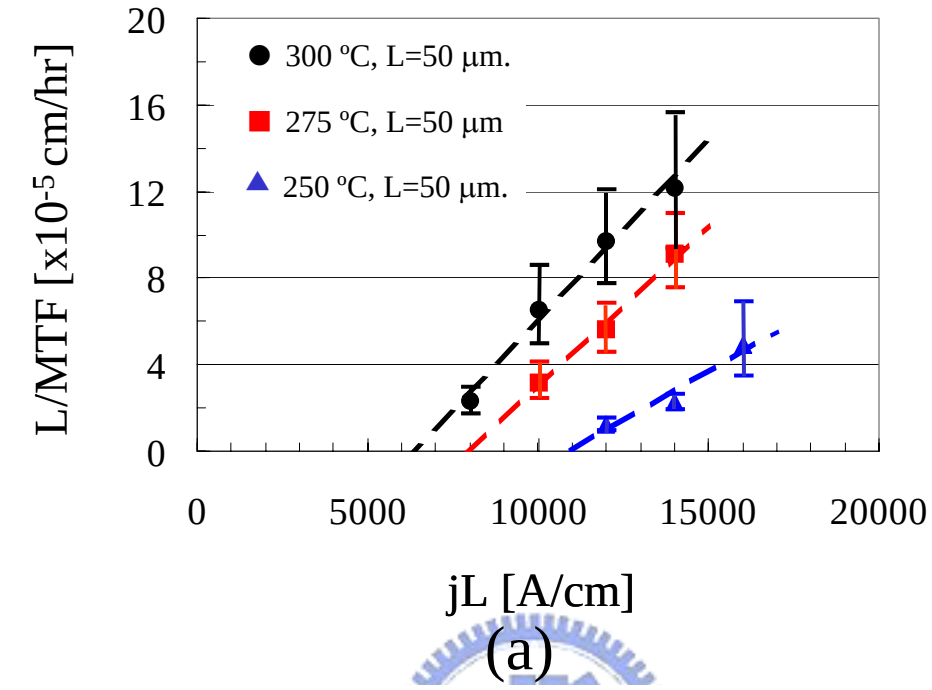


Fig.6.5 Log-log plot of MTF vs. current density-length product for L=50, 400 μm at 300 °C. The solid line was obtained by fitting the MTF data into Eq. 6.5, where the regression found (j_CL)=6000 A/cm and n_2=1.2. The dashed lines indicate n=1.4, 1.36 which fitting the MTF data of L=50, 400 μm to Eq. 6.4 and assuming that the exponential term is constant, a linear regression yields a current exponent of $n_1 \approx 1.4$, 1.36 respectively at high current density-length product



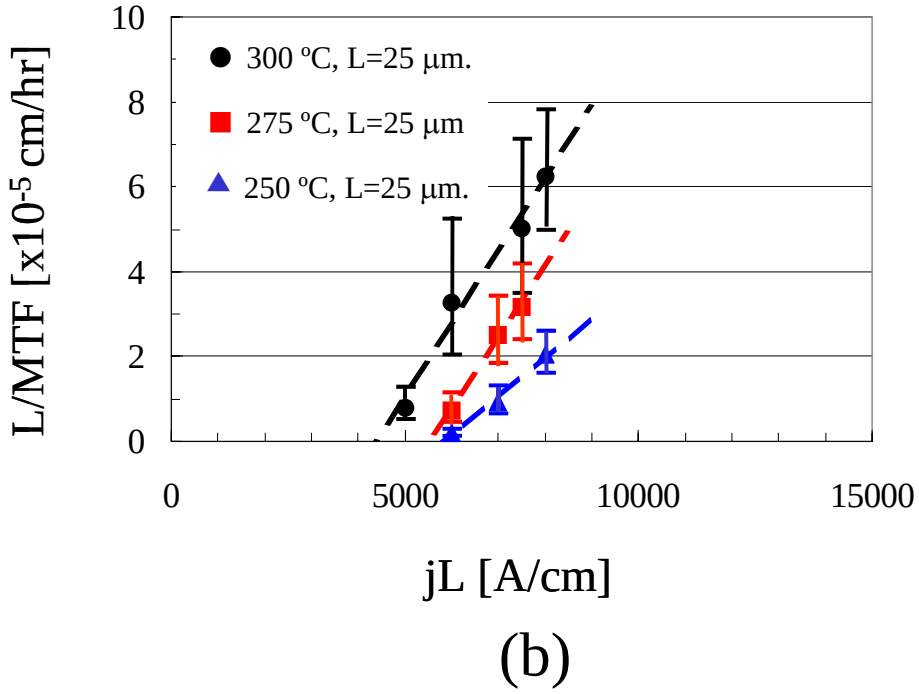
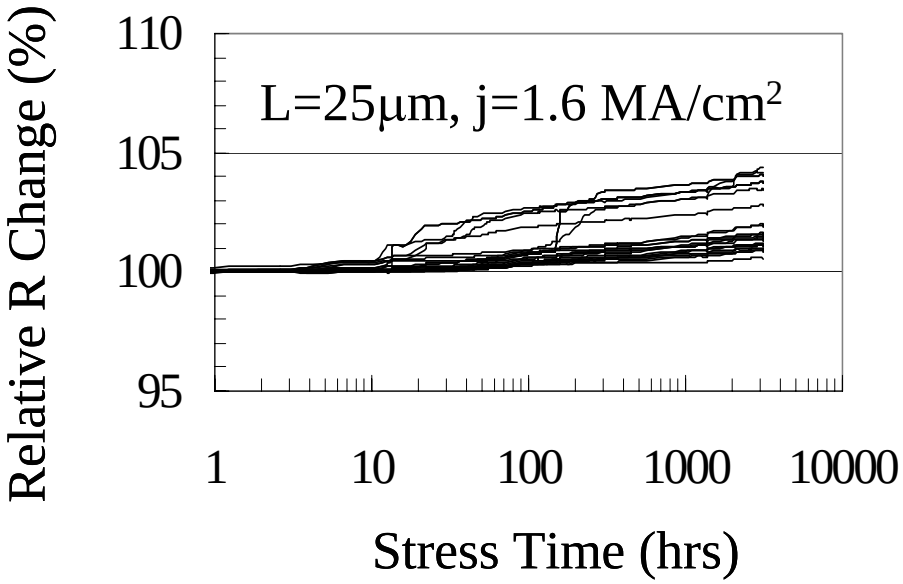
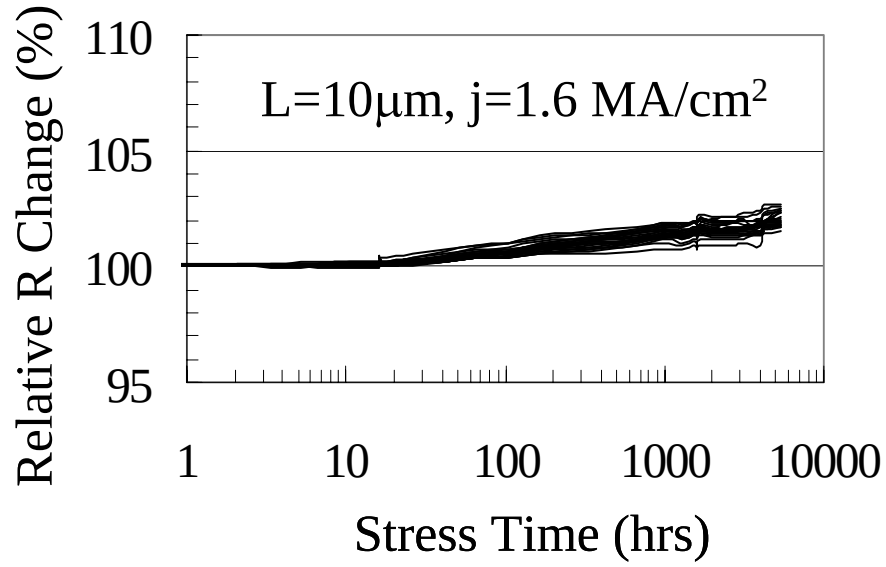


Fig.6.6 (a) L/MTF versus current density-length product for L=50 μm. The threshold–length products $(jL)_C$ was calculated to be 6319 A/cm for 300°C. (b) L/MTF versus current density-length product for L=25 μm. The threshold–length products $(jL)_C$ was calculated to be 4314 A/cm for 300 °C. Error bars represent 90% confidence intervals.

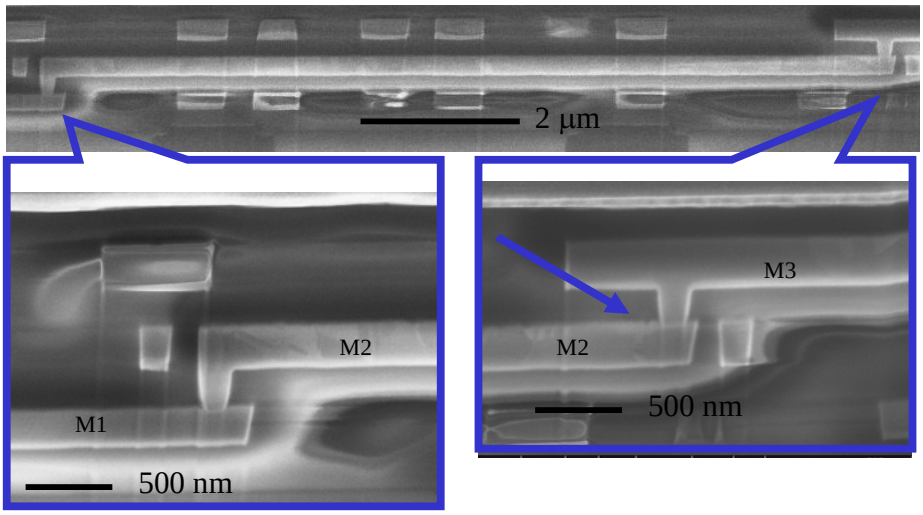


(a)

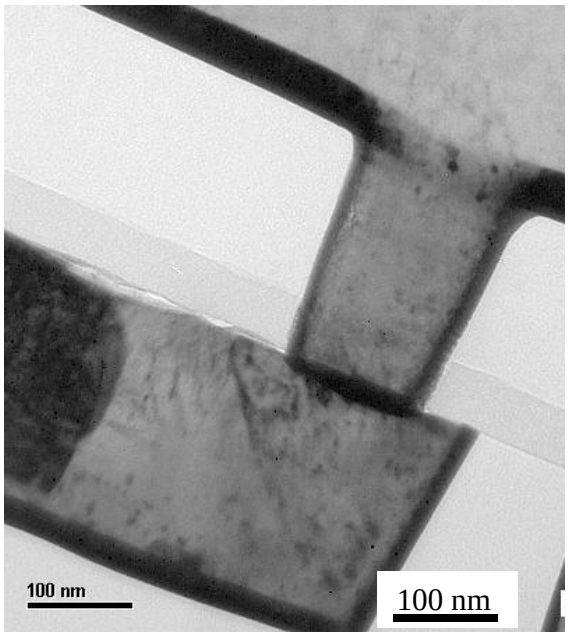


(b)

Fig.6.7 (a) Relative R change vs. time shows slight resistance increase up to 5100 hrs of testing for L=25 μm, j=1.6 $\times 10^6/cm^2$, T=300 ^oC, and sample size over 24. The resistance change is very small around 2 to 4%, show that the immortal behavior occurs, $(jL)_C$»4000 A/cm. (b) Relative R change vs. time shows slight resistance increase up to 5100 hrs of testing for L=10 μm, j=1.6 $\times 10^6/cm^2$, T=300 ^oC, and sample size over 24. $(jL)_C$ »1600 A/cm.



(a)



(b)

Fig.6.8 (a) SEM images for L=10 μm line structure after passage of 1.6 $\times 10^6/cm^2$ for about 5100 h at 300 ^oC. No clear void was found at the anode or cathode ends along the line. (b) A high-resolution TEM was analyzed at the cathode end to reveal the detail microstructure. Very small void has formed at cathode end, which lead to an only minor resistance increase.

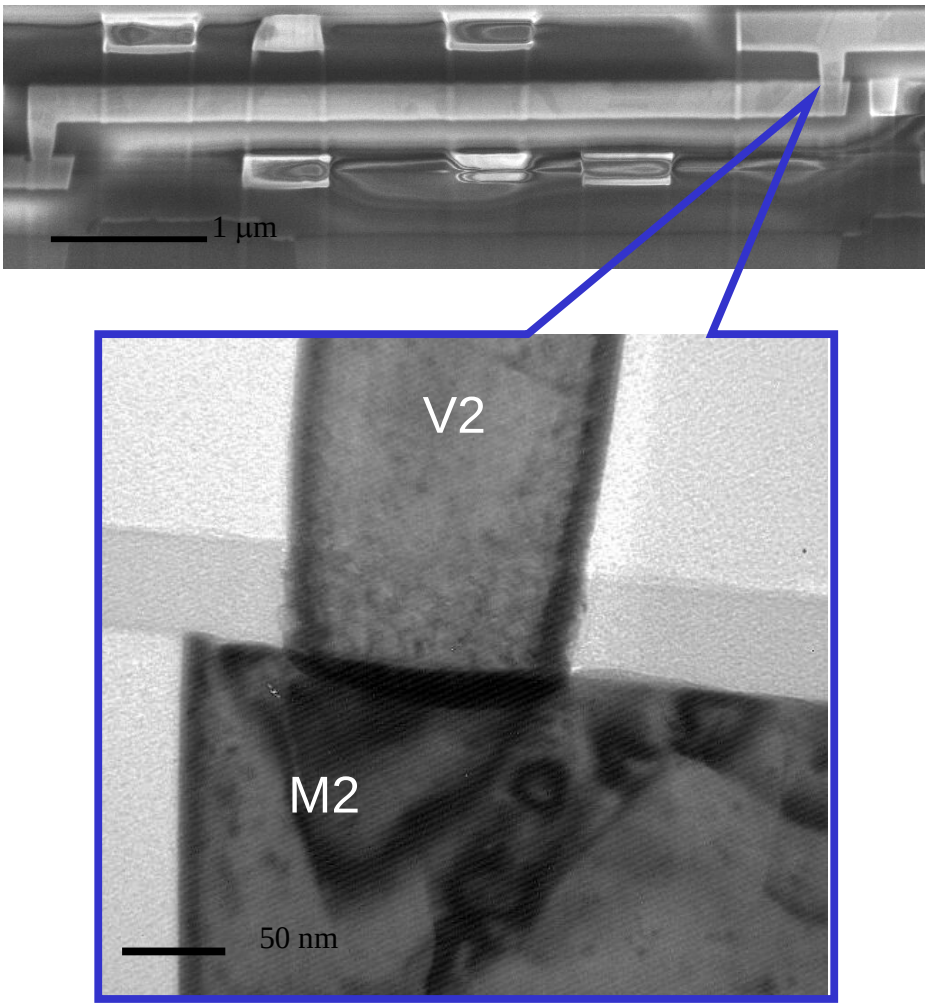


Fig.6.9 FIB and TEM images of a stripe 5 μm length after passage of 1.6 $\times 10^6/cm^2$ for about 5000 h at 300 °C. The EM-induced void of a stripe 5 μm length is much smaller than that of 10 μm length.

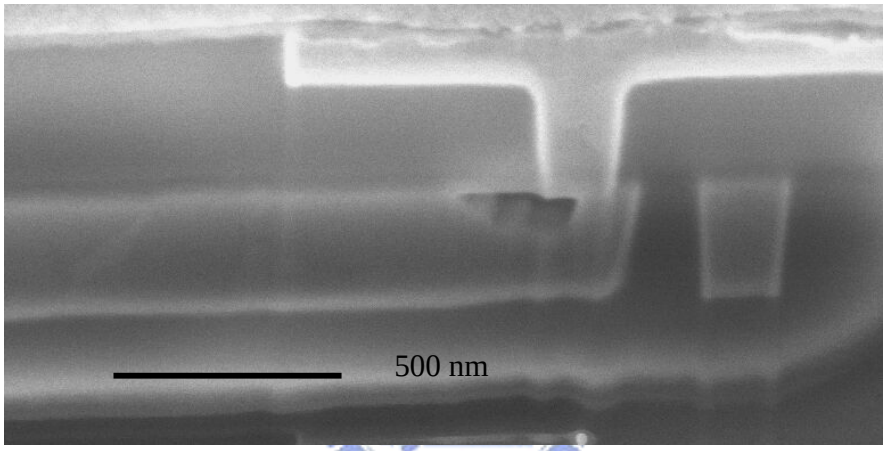


Fig.6.10 An example of FIB cross sections at the cathode end along the 25 μm length line after passage of 1.6 $\times 10^6/cm^2$ for about 5000 h at 300 ^oC. The void has partially exposed the bottom of the via.

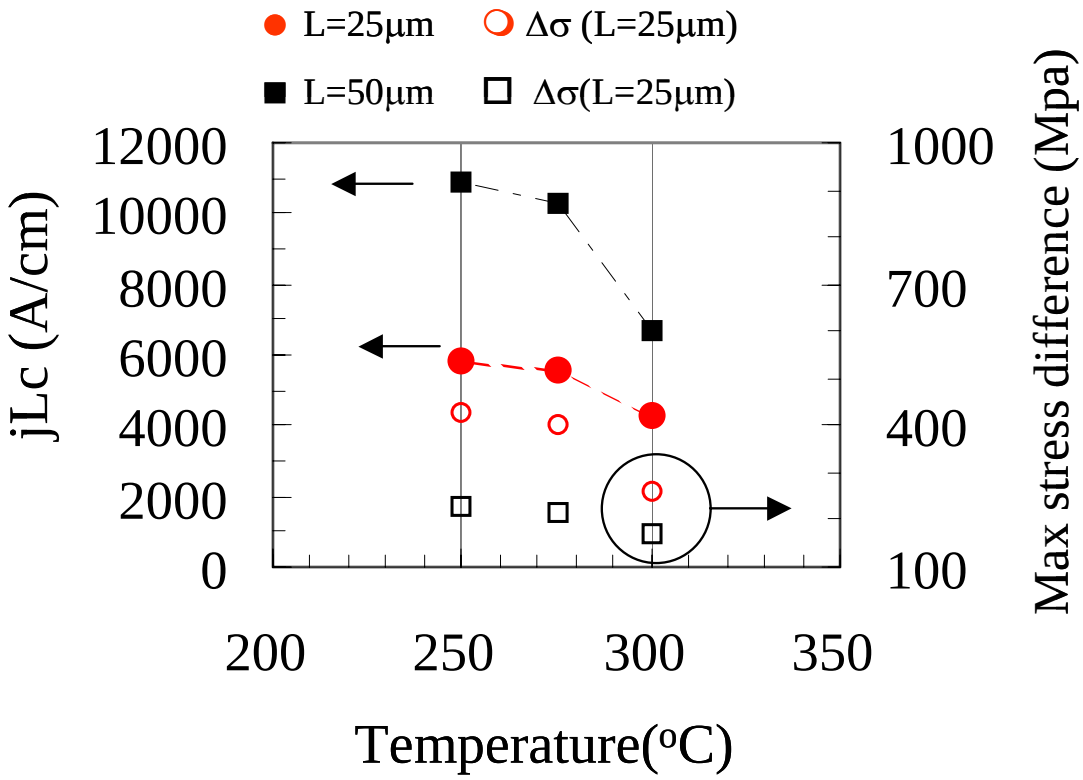


Fig.6.11 Temperature dependence of critical length effect and maximum stress difference in the interconnect for L=25, 50 μm. It is observed that jL value increase slowly at low temperature.

Chapter 7

Conclusions and Future Work

7.1 Summary and Conclusions

In this chapter, the key results of this study will be summarized and key contributions of this research will be reviewed. Potential directions for investigations are also suggested. The major contribution of each theme presented in this work can be summarized as follows.

First, the characteristics and failure mechanisms involved in Cu electromigration have been investigated. In chapter 3, following the successful integration of Cu/low-k BEOL processes, package level electromigration tests have been performed using various low-k materials in order to compare the performance and verify the stability of the Cu dual-damascene process. Various stress conditions for a number of structures were studied enable an understanding of the failure modes and to identify the weak links in an interconnect system. In addition to a well-understood failure mechanism, the multimodality distributions in various Cu/low-k processes are fitted using various bimodal methods to obtain precise lifetime.

Second, methods of optimizing Cu electromigration performance through Cap/dielectric interface re-engineering have been reported. Chapter 4 describes the correlation between electromigration lifetime and Cu surface cap-layer process. The dual via structure not only extends the EM lifetime but also changes the major failure mechanism from instantaneous to long-lasting mode. The effects of a pre-clean and the cap-layer material on the MTF are significant. A SiCN+pre-clean A can improve the lifetime by 10x compared to a PESiN+pre-clean B process. The adhesion of the Cu/cap interface can be directly correlated to the electromigration MTF and activation energy. A Cu-silicide formation mechanism before cap-layer deposition was proposed to explain the enhancement of electromigration lifetime. A significant improvement of

electromigration (EM) lifetime is achieved through modification of the pre-clean step prior to cap-layer deposition and by changing Cu cap/dielectric materials.

Next, Chapter 5 outlines the effects of width scaling and layout variation on dual-damascene copper interconnect electromigration. There are two scenarios that cover the impact of width scaling on electromigration. One is the width <1 μm region, in which the MTF shows a weak width dependence, except for the via-limited condition. The other is the width >1 μm region, in which the MTF shows a strong width dependence. A theory was proposed to explain the observed behavior. For polycrystalline lines (width >1 μm), the dominant diffusion paths are a mixture of grain boundary and surface diffusion. The activation energy for the dominant grain boundary transport (width >1 μm) is approximately 0.2 eV higher than that of the surface and grain-boundary transport (width ~ 1 μm). The derived activation energies for grain-boundary and surface diffusion are obtained from the Cu drift velocity under EM stressing.

Finally, in Chapter 6, the Blech effect or the short-length effect on a dual-damascene Cu process and its temperature dependence is investigated by using a technologically realistic interconnect structure. A lower jL^2 product shows large sigma values as a result of back-stress-induced TTF dispersion. In order to avoid the Blech effect, the EM test structure length should be longer than 200 μm at moderate stress currents. The difference in the relationship between MTF and jL can be seen to be separated by a distinct boundary. One region (i) is the electromigration behavior which follows Black's empirical equation and has no significant back-stress. The other (ii) is the electromigration behavior that can be better represented by a modified Black's empirical equation, and includes significant back-stress. As an alternate means of determining the threshold–length product $(jL)_C$ value, a model that relates it to the failure volume and atomic flux was proposed. The extracted values are consistent with the regression value from the modified Black's empirical equation, and these $(jL)_C$ value were verified during an extended stress test period. The resulting threshold–length product $(jL)_C$ value

appears to be temperature dependent, decreasing with an increase in temperature in a range of 250°C to 300°C. Much insight has been gained through electromigration experiments with Cu dual-damascene technology to identify its distinctive behaviors.

7.2 Future Work

Almost all electromigration lifetime measurements have been carried out under a steady current (DC). However, in most applications, the current signals in the device are often applied under pulsed conditions, as shown in Fig.7.1. So the electromigration characteristics under pulsed conditions are of practical interest. This can be examined using a square current to study the effect on the lifetime of the on/off time. In practice, the actual waveform of the pulse current contains a transient part due to the charging and discharging of the circuit, so nearly square waveform is obtained at high frequencies, as shown in Fig. 7.2.

A number of investigations have reported the effect of frequency and duty cycle on the Al electromigration lifetime under pulsed current conditions [7.1-7.7]. Several models have been proposed to correlate the electromigration lifetime under pulse conditions to that of DC conditions. One assumes that the damage accumulates only when the current is on, and the current–off periods have no effect. The MTF under pulsed DC conditions is inversely proportional to the duty cycle and can be expressed in terms of a steady DC condition as:

$$\text{MTF(pulse DC)} = \frac{1}{r}\text{MTF(steady DC)} \qquad (7.1)$$

where r is the duty cycle defined as the percentage of time while the current is on. A second model assumes that the migrating ions experience an average current density (rj) rather than the individual pulse. Then, the MTF under pulse conditions can be expressed as:

$$\text{MTF(pulse DC)} = \text{A}\,(rj)^{-n}\exp(\frac{Ea}{kT}) = \frac{1}{r^n}\text{MTF(steady DC)} \qquad (7.2)$$

However, few studies have reported details of Cu electromigration under time-varying

current stress. A question remains whether Cu dual-damascene interconnects exhibit a similar behavior. The dual-damascene Cu via is connected to the metal (M2) trench above and separated from the metal (M1) trench below by a thin diffusion barrier to form a flux divergence. A very small mass material depletion at the cathode via may cause an open circuit. A complication arises in the experiment exists because of potential electromigration damage in the dual-damascene Cu via/line interface. In addition, the relaxation time for Cu (0.2 μs) has been reported to be about 100 times smaller that that for Al-2%Si (20 μs) [7.6]. The characteristics of Cu electromigration under a pulsed DC current are expected to be different from Al, which gives room for further investigation.

Many of the problems that result in Cu/low-k interconnect reliability issues will become more severe as feature sizes scale down, as current density rises, and as new materials are introduced. Continuing research is needed to fully understand the multi-variable nature of Cu/low-k interconnect reliability and provide more accurate models to ensure design-in reliability. In the past 30 years, it has been found that shorter Al wires are substantially less susceptible

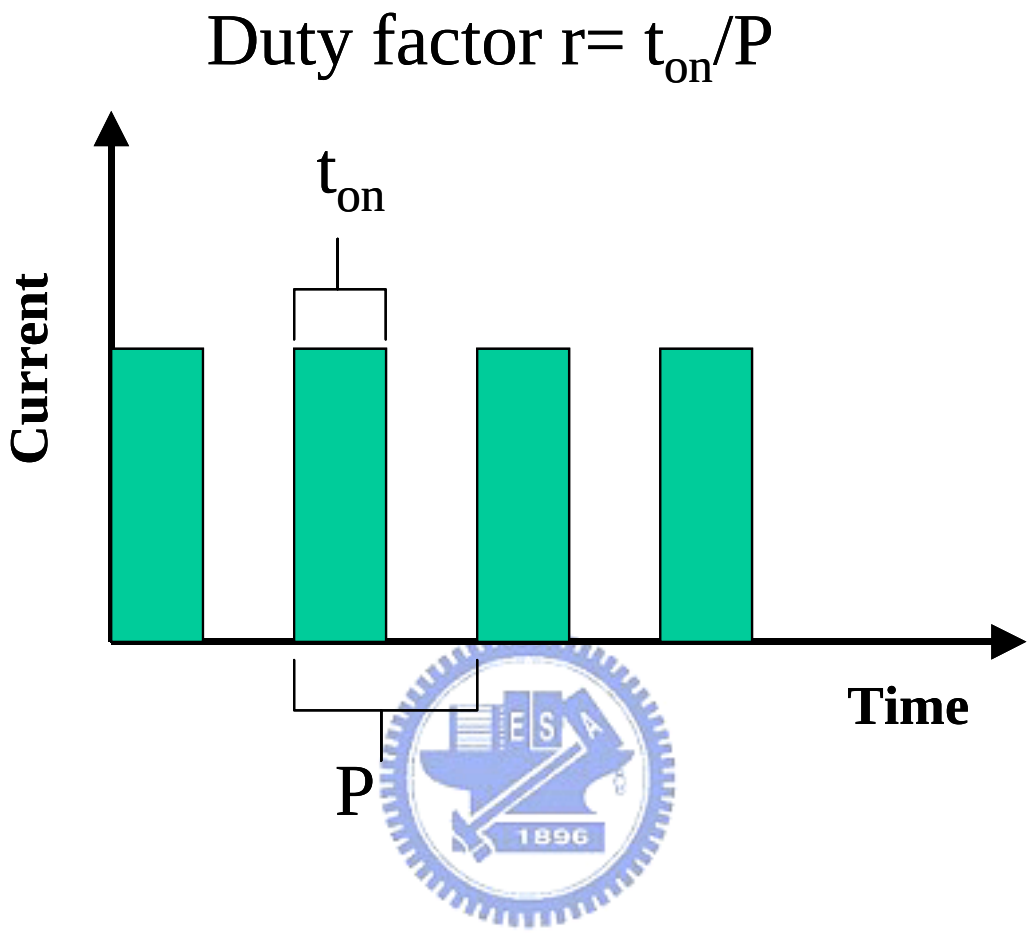


Fig.7.1 A schematic AC pulse current, the current is applied every P period and remains on for a time ton, so that the duty cycle r = t_{on}/P.

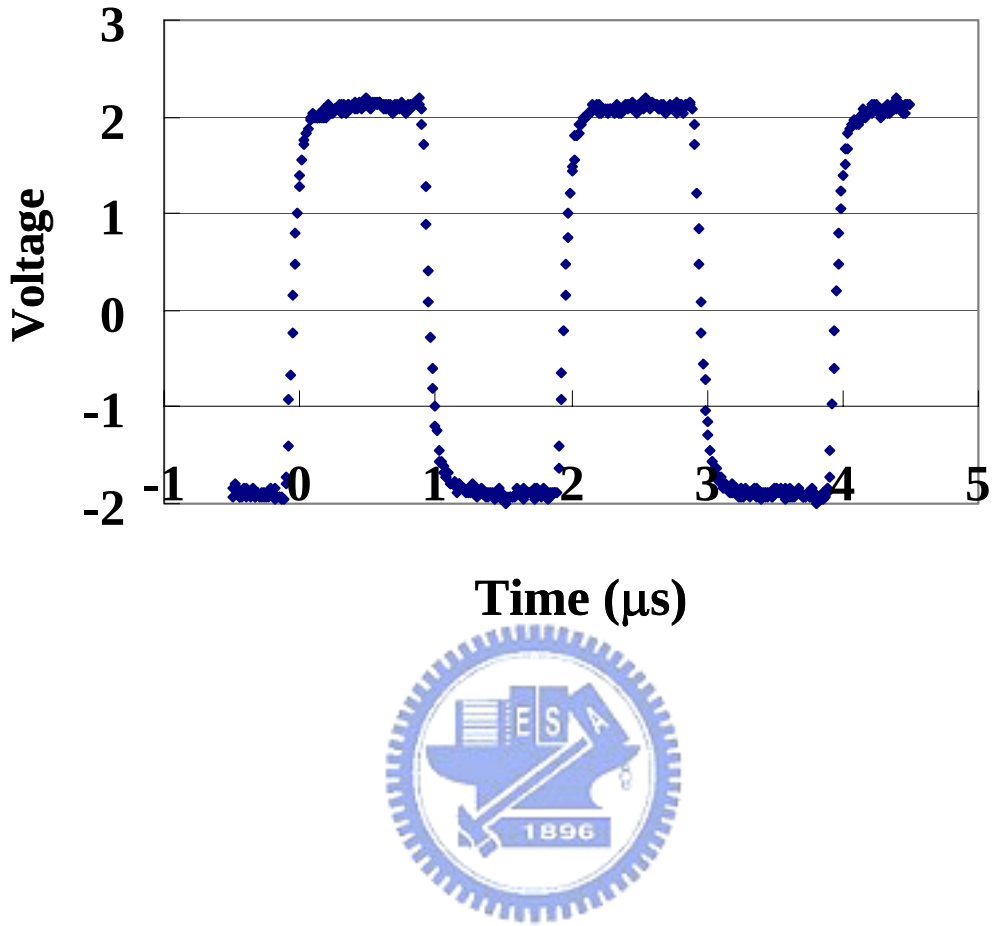


Fig.7.2 Pulse DC waveform as ton =1ms, which is extracted from the scope.

References

Chapter 1

[1.1] International Technology Roadmap for Semiconductors. http://public.itrs.net. interconnects.

[1.2] T. Kwok and P. S. Ho, “Electromigration in Metallic Thin films” Diffusion Phenomena in Thin Film and Microelectronic Materials, 1988.

[1.3] I. A. Blech and H. Sello, “A study of failure mechanisms in Silicon planar epitaxial transistors” in Physics of Failure in Electronics, vol. **5**, pp.496 – 505, 1966.

[1.4] J. D. Plummer, M. D. Deal, and P. B. Griffin, Silicon VLSI Technology, Chap. 11 Prentice Hall, 2000.

[1.5] E. T. Ogawa, K. D. Lee, V. A. Blaschke, and P. S. Ho, “Electromigration Reliability Issue in Dual-Damascene Cu Interconnections,” *IEEE Tran. Reliability*, vol. **51**, pp. 403-419, 2000.

[1.6] J. R. Lioyd, and J. J. Clement, “Electromigration in Copper Conductors,” *Thin Soild Films*, vol. **262**, pp. 135-141, 1995.

[1.7] A. Tezaki, T. Mineta, and H. Egawa, “Measurement of Three Dimensional Stress and Modeling of Stress Induced Migration Failure in Aluminum Interconnects” *in Proc. Int. Reliab. Phys. Symp.*, pp. 221-229, 1990.

[1.8] F. M. D’Heurle, “Electromigration and Failure in Electronics: An Introduction,” *in Proc. IEEE*. vol. 59, pp.1409 – 1971, 1971.

[1.9] H. B. Huntington, and A. R. Grone, “Current-induced Marker Motion in Gold Wires,” *J. Phys.Chem. Solids*, vol. **20**, pp. 76-87, 1961.

[1.10] K. N. Tu, “Electromigration in Stress Thin Film” *Phys.Rev. B.*, vol. 45, p.1409-1413, 1992.

[1.11] I. A. Blech and C. Herring, “Stress generation by electromigration” *Appl. Phys. Lett*, vol.

29, p.131-133, 1976.

[1.12] I. A. Blech, “Electromigration in thin aluminum films on titanium nitride”, J. Appl. Phys. **47**, p.1203-1208, 1967.

[1.13] J. R. Black, “Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons” *in Proc. Int. Reliab. Phys. Symp.*, pp. 148-159, 1967.

[1.14] J. R. Black, “Electromigration—A Brief Survey and Some Recent Results,” *IEEE Tran. Electron Devices*, vol. **16**, pp. 338-347, 1969.

[1.15] C. S. Hau-Riege, “Current Challenges in Cu Electromigration Reliability” *in Proc. Int. Reliab. Phys. Symp. Tutorial Note.*, p. 232, 2003.

Chapter 2

[2.1] C. –K. Hu, and J. M. E. Harper, “Copper Interconnects and reliability,” J. Materials Chem. and Phys., vol. **52**, p.5-16, 1998.

[2.2] D. Edelstein et al, “A high Performance Liner for Copper Damascene Interconnects,” in *IEEE Int’l. Interconnect Tech. Conf.* pp.9-11, 2001.

[2.3] C. C. Yang et al, “Extendibility of PVD Barrier/Seed for BEOL Cu Metallization,” in *IEEE Int’l. Interconnect Tech. Conf.* pp.135-137, 2005.

[2.4] D. Chung, J. Korejwa, and E. Walton, “Introduction of Copper Electroplating Into a Manufacturing Fabrication,” in *IEEE/SEMI adv..Semiconductor Manufacturing Conf.* pp.282-289, 1999.

[2.5] F. Chen, J. Gill, D. Harmon, T. Sullivan, B. Li, A. Strong, H. Rathore, D. Edelstein, C. –C. Yang, A. Cowley, and L. Clevenger, “Measurements of effective thermal conductivity for advanced interconnect structures with various composite low-k dielectrics,” *in Proc. Int. Reliab. Phys. Symp.*, pp. 25-29, 2004.

[2.6] JEDEC Solid State Technology Association, “Standard Method for measuring and using

the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line**,**" in JESD33b.

Chapter 3

[3.1] C.-K. Hu and J. M. E. Harper “Copper Interconnect: Fabrication And Reliability” *in Proc. Tech. Pap. VLSI Technology, Systems, and Applications*, pp.18-22, 1997.

[3.2] C.-K. Hu, R. Rosenberg, H. S. Rathore, D. B. Nguyen and B. Agarwala, “Scaling Effect on Electromigration in on-chip Cu Wiring,” *in IEEE Int’l. Interconnect Tech. Conf.*, pp. 247-269, 1999.

[3.3] A. H. Fisher, A. von Glasow, S. Penka and F. Ungar, “Electromigration failure mechanism studies on copper interconnects,” *in IEEE Int’l. Interconnect Tech. Conf.*, pp. 139-141, 2002.

[3.4] C.-K. Hu, R. Rosenberg, W. Klaasen and A. K. Stamper, “Electromigration Reliability Study of Submicron Cu”: in *Proc. Adv. Metallization. Conf.*, p. 1-7, 1999.

[3.5] C.-K. Hu, L. Gignac, S. G. Malhotra and R. Rosenberg, “Mechanisms for very long Electromigration Lifetime in Dual-Damascene Cu Interconnects“ *Appl. Phys. Lett.* vol. **78**, pp.904-906, 2001.

[3.6] S. Yokogawa, N. Okada, Y. Kakuhara and H. Takizawa, “Electromigration Performance of Multi-level Damascene Copper Interconnects,” Microelectronics Reliability, vol. **41**, pp. 1409-1419, 2001.

[3.7] C.-K. Hu, L. Gignac, E. Liniger, B. Herbst, D. L. Rath, S. T. Chen, S. Kaldor, A. Simon and W. -T. Wang: “Comparison of Cu Electromigration Lifetime in Cu Interconnects Coats with Various Caps “ *Appl. Phys. Lett.* vol. **83**, pp.869-871 ,2003.

[3.8] E. Liniger, L. Gignac, C.-K. Hu, and S. Kaldor, “In situ Study of Void Growth Kinetics in Electroplated Cu lines,” *J. Appl. Phys.*, vol. **92**, pp. 1803-1809, 2003.

[3.9] A. V. Vairagar, S. G. Mhaisalkar, M. A. Meyer, E. Zschech, A. Krishnamoorthy, K. N. Tu, and A. M. Gusak, "Direct Evidence of Electromigration Failure Mechanism in in Dual-Damascene Cu Interconnect tree Structures," *Appl. Phys. Lett.* vol. **87**, p.0081909, 2005.

[3.10] M. Lepper, A. H. Fisher, and A. E. Zitzelsberger, "On the Bimodal Lognormal Distribution of Electromigration Lifetime" *IEEE Integrated Reliability Workshop,* pp. 146-147, 1999.

[3.11] A. H. Fisher, A. Abel, M. Lepper, A. E. Zitzelsberger and A.von Glasow, "Esperimental Data and Statistical Models for Bimodel EM Failure" *in Proc. Int. Reliab. Phys. Symp.,* pp. 359-363, 2000.

[3.12] J. B. Lai, J. L. Wang, S. H. Chang, R. L. Hwang, Y. S. Huang, and C. S. Hou, "A Study of Bimodal Distributions of Time-to-Failure of Copper Via Electromigration," *in Symp. VLSI Tech.*, pp. 271-274, 2001.

[3.13] C.-K. Hu, L. Gignac, E. Liniger and R. Rosenberg, "Bimodal electromigration mechanisms in dual-damascene Cu line/via on W" *in IEEE Int'l. Interconnect Tech. Conf.*, pp. 133-135, 2002.

[3.14] E. T. Ogawa, K.-D. Lee, H. Matsuhashi, K.-S. Ko, P.R. Justison, A. N. Ramamurthi, A. J. Bierwag, P. S. Ho, V.A. Blaschke and R.H. Havemann, "Statistics of Electromigration Early Failures in Cu/Oxide Dual-Damascene Interconnects," *in Proc. Int. Reliab. Phys. Symp.*, pp. 341-349, 2001.

[3.15] H. A. Schafft, "Reliability test chips: NIST 33 and NIST 34 for JEDEC inter-laboratory experiments and more" *in IEEE Integrated Reliability Workshop*, pp. 144-147, 1997.

[3.16] H. Sato and S. Ogawa , "Mechanism of Dependency of EM Properties on Linewidth in Dula Damascene Copper Interconnects," *in IEEE Int'l. Interconnect Tech. Conf.*, pp. 186-189, 2001.

[3.17] H. A. Schafft et al., “The Measurement, Use and Interpretation of the Temperature Coefficient of Resistance of Metallizations.” Solid-State Electronics **35**(3), pp. 403-410,1992

[3.18] M. H. Lin, G.. S. Yang, Y. L. Lin, M. T. Lin, C. C. Lin, M.-S. Yeh, K. P. Chang, K. C. Su, J. K. Chen, Y. J. Chang and T. Wang ”A Practical Methodology for Multi-modality Electromigration Lifetime Prediction,” *in IEEE Integrated Reliability Workshop*, pp. 50-54, 2002.

[3.19] B.-Z. Li, D. T. Sullivan and T. C. Lee, “Line Depletion Electromigration Characteristic of Cu Interconnects” *in Proc. Int. Reliab. Phys. Symp.*, pp. 140-145, 2003.

Chapter 4

[4.1] C.-K. Hu, R. Rosenberg, and K. Y. Lee, “Electromigration path in Cu thin-film lines“ *Appl. Phys. Lett.*, vol. **74**, pp. 2945-2947, 1999.

[4.2] P. Besser, A. Marathe, L. Zhao, M. Herrick; C. Capasso, and H. Kawasaki, “Optimizing the electromigration performance of copper interconnects,” in *IEDM Tech. Dig.*, pp. 199-122 , 2000.

[4.3] J. Proost, T. Hirato, T. Furuhara, K. Maex, and J.-P. Celis, “Microtexture and Electromigration-induce Drift in Electroplated Damascene Cu,” *Appl. Phys. Lett.*, vol. **74**, pp. 2945-2947, 2001.

[4.4] C. S. Hau-Riege, and C. V. Thompson, “Electromigration in Cu Interconnects with Very Different Grain Structures,” *J. Appl. Phys.*, vol. **78**, pp. 3451-3453, 2001.

[4.5] C. D. Hartfiled, E. T. Ogawa, Y. J. Park, and T. C. Chiu, “Interface reliability assessments for copper/low-k products,” *IEEE Trans. Device and Materials Reliability*. vol. **4**, pp. 129-141, 2004.

[4.6] M. W. Lane, E. G. Liniger, and J. R. Lloyd, “Relationship between Interface Adhesion and

Electromigration in Cu Metallization," *J. Appl. Phys.*, vol. **93**, pp. 1417-1421, 2003.

[4.7] J. R. Lloyd, M. W. Lane, E. G. Liniger, C.-K. Hu, and R. Rosenberg, "Electromigration and Adhesion," *IEEE Trans. Device and Materials Reliability*. vol. **5**, pp. 113-118, 2005.

[4.8] M. Hatano, T. Usui, Y. Shimooka, and H. Kaneko, "EM Lifetime improvement of Cu damascene interconnect by P-SiC cap layer" *IEEE Int'l. Interconnect Tech. Conf.* pp.212-214, 2002.

[4.9] C.-K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. Domenicucci, X. Chen, and A. K. Stamper, "Reduced Electromigration of Cu wires by Surface Coating" *Appl. Phys. Lett.*, vol. **81**, pp. 1782-1784, 2002.

[4.10] C.-K. Hu, L. M. Gignac, R. Rosenberg, B. Herbst, S. Smith, J. Rubino, D. Canaperi, S. T. Chen, S. C. Seo, and D. Restaino, "Atom Motion of Cu and Co in Cu Damacsene lines with CoWP cap" *Appl. Phys. Lett.*, vol. **84**, pp. 4986-4988, 2004.

[4.11] C.-K. Hu, D. Canaperi, S. T. Chen, L. M. Gignac, B. Herbst, S. Kaldor, M. Krishnan, E. Liniger, D. L. Rath, D. Restaino, R. Rosenberg, J. Rubino, S. Smith, and W.-T. Tseng, "Effects of Overlayers on Electromigration Reliability Improvement for Cu/low-k Interconnect" *in Proc. Int. Reliab. Phys. Symp.*, pp. 222-228, 2004.

[4.12] A. H. Fischer, A. von Glasow, S. Penka, and F. Ungar, "Process optimization-the key to obtain highly reliable Cu interconnects" *IEEE Int'l. Interconnect Tech. Conf.* pp.253-255, 2003.

[4.13] A.von Glasow, A. H. Fischer, D. Bunel, G. Friese, A. Hausmann, O. Heitzsch, M. Hommel, J. Kriz, S. Penka, P. Raffin, C. Robin, H.-P. Sperlich, F. Unger, and A. E. Zitzelsberger, "The Influence of the SiN cap process on the Electromigration and stressvoiding performance of dual damascene Cu Interconnects" in *Proc. Int. Reliab. Phys. Symp.*, pp. 146-150, 2003.

[4.14] Q. Ma "A Four-Point Bending Technique for Studying Subcritical Crack Growth in Thin

Film and Interfaces," *J. Materials Research*, vol. **12**, p.840-845, 1997.

[4.15] M. H. Lin, G. S Yang, Y. L. Lin, M. T. Lin, C. C. Lin, M. S. Yeh, K. P. Chang, K. C. Su, J. K. Chen, Y. J. Chang, and Tahui Wang, "A Practical Methodology for Multi-modality Cu Electromigration Lifetime Prediction" *in Proc. Int. Integrated Reliability Workshop*, Lake Tahoe, CA, pp. 50-54, 2002.

[4.16] B.-Z. Li, T. D. Sullivan, and T. C. Lee, "Line Depletion Electromigration Characteristic of Cu Interconnects", in *Proc. Int. Reliab. Phys. Symp.*, pp. 140-145, 2003.

[4.17] A.von Glasow, A. H. Fisher, and A. E. Zitzelsberger, "Using the Temperature Coefficient of the Resistance (TCR) as Early Reliability Indicator for Stressvoiding Risks in Cu Interconnects", in *Proc. Int. Reliab. Phys. Symp.*, pp126-131, 2003.

[4.18] J. Noguchi, N. Ohashi, T. Jimbo, H. Yamaguchi, K, Takeda, and K. Hinode, "Effect of NH3-Plasma Treatment and CMP Modification on TDDB Improvement Cu Metallization", *IEEE Trans. Electron. Devices*, vol. **48**, pp1340-1345, 2001.

Chapter 5

[5.1] B.-Z. Li, J. Gill, C. J. Christiansen, T. D. Sullivan and P. S. McLaughlin. "Impact of via-line contact on Cu interconnect electromigration performance" in *Proc. Int. Reliab. Phys. Symp.*, pp24-30, 2005.

[5.2] T. Usui, H. Nasu, T. Watanabe, H. Shibata, T. Oki, and M. Hatano. "Electromigration diffusion mechanism of electroplated copper and cold/hot two-step sputter-deposited aluminum-0.5-wt% copper damascene interconnects" *J. Appl. Phys.*, vol. **98**, 063509, 2005.

[5.3] H. Sato and S. Ogawa: "Mechanism of Dependency of EM Properties on Linewidth in Dual Damascene Copper Interconnects", *IEEE Int'l. Interconnect Tech. Conf.* pp.186-188, 2001.

[5.4] C. Ryu, K. W. Kwon, A L. S. Loke, H. Lee, T. Nogami, V. M. Dubin, R. A. Kavari, G. W. Ray, and S. S. Wong, "Microstructure and Reliability of Copper Interconnects" *IEEE Trans Electron Devices*, vol. **46**, pp.1113-1120, 1999.

[5.5] L. Arnaud, G.. Tartavel, T. Berger, D. Mariolle; Y. Gobil, and I. Touet, "Microstructure and electromigration in copper damascene lines" in *Proc. Int. Reliab. Phys. Symp.*, pp263-269, 1999.

[5.6] L. Arnaud, G.. Tartavel, T. Berger, D. Mariolle; Y. Gobil, and I. Touet, "Microstructure and electromigration in copper damascene lines" Microelectron Reliab., vol. **40**, pp.77-86, 2000.

[5.7] M. H. Lin, Y. L. Lin, J. M. Chen, C. C. Tsai, M.-S Yeh, C. C. Liu, S. Hsu, C. H. Wang, Y. C. Sheng, K. P. Chang, K. C. Su, Y. J. Chang, and Tahui Wang, "The Improvement of Copper Interconnect Electromigration Resistance by Cap/Dielectric Interface Treatment and Geometrical Design"in *Proc. Int. Reliab. Phys. Symp.* pp.229-233, 2004.

[5.8] C.-K. Hu, R. Rosenberg, and K. Y. Lee, "Electromigration path in Cu thin-film lines" *Appl. Phys. Lett.*, vol. **74**, pp. 2945-2947, 1999.

[5.9] C.-K. Hu, (private communication).

Chapter 6

[6.1] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride", *J. Appl. Phys.* vol. **47**, pp. 1203-1208, 1976.

[6.2] E. T. Ogawa, A. J. Bierwag, K. D. Lee, H. Matsuhashi, P. R. Justison, A. N. Ramamurthi, P. S. Ho, V. A. Blaschke, D. Griffiths, A. Nelsen, M. Breen, and R. H. Havemann, "Direct Observation of a Critical Length Effect in Dual-Damascene Cu/oxide Interconnects," *Appl. Phys. Lett.* vol. **78**, pp. 2652-2654, 2001.

[6.3] C. V. Thompson, C. L. Gan, S. M. Alam, and D. E. Troxel, "Experiments and models for

circuit-level assessment of the reliability of Cu metallization“, *IEEE Int'l. Interconnect Tech. Conf.* pp.69-71, 2004.

[6.4] S. P. Hau-Riege, “Probabilistic immortality of Cu damascene interconnects ” J. Appl. Phys. vol. **91**, pp.2014-222, 2002.

[6.5] J. R. Black, “Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons ” in *Proc. Int. Reliab. Phys. Symp.*, pp 1-6, 2005.

[6.6] R. G. Filippi, G. A. Biery, and R. A. Wachnik “The electromigration short-length effect in Ti-AlCu-Ti metallization with tungsten studs ” *J. Appl. Phys.* vol. **78**, pp. 3756-3768, 1993.

[6.7] M. A. Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li, “Stress Evolution due to Electromigration in Confined Metal Lines ” *J. Appl. Phys.* vol. **73**, pp. 3790-3799, 1993.

[6.8] J. He, Z. Suo, T. N. Marieb, and J. A. Maiz, “Electromigration Lifetime and Critical Void Volume“ *Appl. Phys. Lett.*, vol. **85**, pp. 4639-4641, 2004.

[6.9] R. Kircheim, and U. J. Kaeber, “Atomistic and Computer Modeling of Metallization Failure of Intergrated Circuits by Electromigration“ *J. Appl. Phys*. vol. **70**, pp. 172-181, 1991.

[6.10] J. R. Lloyd, “ Electromigration Failure” *J. Appl. Phys.* vol. **69**, pp. 7601-7604, 1991.

[6.11] C. S. Hau-Riege, “ An Introduction to Cu Electromigration” Microelectron Reliab., vol. **44**, pp195-205, 2004.

[6.12] C. S. Hau-Riege, A. P. Marathe and V. Pham, “The Effect of low-k ILD on the Electromigration reliability of Cu Interconnects with Different Line lengths,” *in Proc. Int. Reliab. Phys. Symp.*, pp. 173-177, 3003.

[6.13] C. S. Hau-Riege, S. P. Hau-Riege, and A. P. Marathe, “The Effect of Interlevel Dielectric on the Critical Tensile Stress to void Nucleation for the reliability of Cu Interconnects,” *J. Appl. Phys*. vol. **96**, pp. 5792-5796, 2004.

[6.14] P.-C. Wang, and R. G. Filippi, “Electromigration Threshold in Cu Interconnects,” *Appl. Phys. Lett.*, vol. **78**, pp. 3598-3600, 2004.

[6.15] S. Thrasher, C. Capasso, L. Zhao, R. Hernandez, P. Mulski, S. Rose, T. Nguyen, and H. Kawasaki, “Blech Effect in Single-Inlaid Cu Interconnects”. *IEEE Int’l. Interconnect Tech. Conf*. pp.177-179, 2001.

[6.16] D. Ney, X. Federspiel, V. Girault, O. Thomas, and P. Gerqaud, “Electromigration Threshold in Copper Interconnects and Consequences on Lifetime Extrapolations”. *IEEE Int’l. Interconnect Tech. Conf*. pp.105-107, 2005.

[6.17] D. Ney, X. Federspiel, V. Girault, O. Thomas, and P. Gerqaud, “Blech Effect in Dual-Damascene Copper-low k Interconnects”. *in Proc. Int. Integrated Reliability Workshop*, Lake Tahoe, CA, pp. 27-30, 2005.

[6.18] C. S. Hau-Riege, and C. V. Thompson, “The effects of microstructural transitions at width transitions on interconnect reliability,” *J. Appl. Phys.* vol. **87**, pp. 8467-8472, 2000.

Chapter 7

[7.1] J. A. Maiz, “Characterization of Electromigration under Bidirectional (BC) and Pulsed Unidirectional (PDC) Currents”, in *Proc. Int. Reliab. Phys. Symp.*, pp. 220-228 1989..

[7.2] T. Noguchi, K. Hatanaka, and K, Maeguchi, “A Threshold Pulse Width for Electromigration Under Pulsed Stress Conditions,” *IEEE VLSI Multilevel Interconnect. Conf*. pp.183-189, 1989.

[7.3] B. K. Liew, N. W. Cheung, and C, Hu, “Projecting Interconnect Electromigration Lifetime for Arbitrary Current Waveforms,” *IEEE Tran. Electron Devices*, vol. **37**, pp. 1343-1351, 1990.

[7.4] J. Tao, K. K. Young, N. W. Cheung, and C, Hu, “Electromigration Reliability of Tungsten and Aluminum Vias and Improvements under AC Current Stress,” *IEEE Tran. Electron Devices*, vol. **40,** pp. 1398-1405, 1993.

[7.5] L. M. Ting, J. S. May, W. R. Hunter, and J. W. McPherson, “AC Electromigration Characterization and Modeling of Multilayered Interconnects”, in *Proc. Int. Reliab. Phys. Symp.*, pp. 311-316 1993.

[7.6] J. Tao, B. K. Liew, J. F. Chen, N. W. Cheung, and C, Hu, “Electromigration under Time-varying Current Stress,” Microelectronics Reliability, vol. **38,** pp. 295-308, 1998.

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經　歷：

一．02/2001 – present

現於任職聯華電子 Q&RA/RE/後段(BEOL)可靠度工程。主要負責全聯電銅/低介電(Cu/low-*k*)製程的 qualification，從 0.13 um 到最新的 0.65 um 製程，全程參與銅製程的電遷移(electromigration) qualification 和問題解決，建立 low-*k* dielectric TDDB 測試。藉由 testkey design 到最後 electromigration 測試和分析，task force 解決問題，完成銅製程 electromigration qualification，累積可靠度實務經驗。

二．09/2002 – present

交大電子博士班，課程的修習及論文的訓練，開展自己在可靠度及半導體元件與 IC 製程的知識領域。

三．02/2000 – 02/2001

任職聯華電子 Q&RA/RA，負責新製程品質保證可靠度管理，及與客戶協調可靠度測試項目，建立 FAB Wafer Leveling Reliability，以期能即時反映製程品質。

四．06/1997 – 02/2000

進入華邦電子，參與四廠建廠, 負責氧化擴散爐管製程及高電流，高能量離子植入(GSD)製程機台，C-V, Quantax 量測機台和石英材料評估並負責報告擴散部門 SPC 數據。藉由 0.35, 0.25, and 0.2 um 64Mb DRAM 製程調機和量產，累積豐富製程經驗。指派參加 0.25 um 東芝擴散研討會，學習東芝工程師經驗和工作方式。

五．07/1995 – 05/1997

於海軍陸戰隊步兵團退伍，兵役期間訓練我體魄及吃苦能力。

六．09/1993 – 06/1995

世界首次發現並測量 $DyNi_2B_2C$ 超導溫度(3.8K)及磁性溫度(10.2K)其結果很快被國際超導期刊(Physica C 1995)刊出。研究所期間發表國際期刊七篇。

七．09/1989 – 06/1993

大學在社團方面成功登頂台灣百岳三十餘座，累積多次冬攀經驗並擔任清大登山社高山嚮導及多項活動領隊，學業方面則以優異成績

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博士論文題目:

銅導線中電遷移效應所引發之故障特性探討

An Investigation into the Characteristics of Electromigration failure mechanisms in Copper Interconnects

Publication Lists

(a) Journal Papers

2. B 類國際性期刊

(1) M. H. Lin, Y. L. Lin, K. P. Chang, K. C. Su and Tahui Wang, “Copper Interconnect Electromigration Behaviors in Various Structures and Lifetime Improvement by Cap /dielectic Interface treatment”, **(Invited paper)**, *Microelectronics Reliability*, vol. 45, pp. 1061–1078, 2005.

3. A 類國際性期刊

(2) M. H. Lin, Y. L. Lin, J. M. Chen, M.-S. Yeh, K. P. Chang, K. C. Su and Tahui Wang, “Electromigration Lifetime Improvement of Copper Interconnect by Cap /dielectric Interface Treatment and Geometrical Design”, *IEEE Trans. Electron. Devices*, vol. ED-52, pp. 2602-2608, 2005.

2. B 類國際性期刊

3) M. H. Lin, Y. L. Lin, K. P. Chang, K. C. Su and Tahui Wang, “Copper Interconnect Electromigration Behavior in Various Structures and Precise Bimodal Fitting”, Jap. J. Appl. Phys, vol. 45, No.4B, 2006.

(b) Conference Papers

(4) M. H. Lin, M. T. Lin, K. P. Chang, K. C. Su and Tahui Wang, “Effects of Width Scaling, Length Scaling, and Layout Variation on Electromigration in Dual Damascene Copper Interconnects ”, in *Proc. Int. Reliability Physics Symp.(IRPS)*, San Jose, CA, pp. 671-673, 2006.

(5) M. H. Lin, K. P. Chang, K. C. Su and Tahui Wang, “Width Scaling and Layout Variation Effects on Dual Damascene Copper Interconnects Electromigration”, in. *Int. Conf. Solid State Devices and Materials (SSDM)*, Kobe, Japan, pp. 296-297, 2005.

(6) M. H. Lin, Y. L. Lin, G. S Yang, M.-S. Yeh, K. P. Chang, K. C. Su and Tahui Wang, “Comparison of Copper Interconnect Electromigration Behaviors in Various Structures for Advanced BEOL Technology ”, in *Proc. Int. Symp. on the Physical and Failure Analysis (IPFA)*, Hsinchu, Taiwan, pp. 177-180, 2004.

1. B類國際會議論文

(7) M. H. Lin, M. H. Lin, Y. L. Lin, J. M. Chen, C. C. Tsai, M.-S. Yeh, C. C. Liu, S. Hsu, C. H. Wang, Y. C. Sheng, K. P. Chang, K. C. Su, Y. J. Chang, and Tahui Wang, “The Improvement of Copper Interconnect Electrimigration Resistance

by CAP /Dielectric Interface Treatment and Geometrical Design", *in Proc. Int. Reliability Physics Symp.(IRPS)*, Phoenix, AR, pp. 229-233, 2004.

(8) M. H. Lin, G. S Yang, Y. L. Lin, M. T. Lin, C. C. Lin, M. S. Yeh, K. P. Chang, K. C. Su, J. K. Chen, Y. J. Chang, and Tahui Wang, "A Practical Methodology for Multi-modality Cu Electromigration Lifetime Prediction ", in *Proc. Int. Integrated Reliability Workshop(IIRW)*, Lake Tahoe, CA, pp. 50-54, 2002.

(9) M. H. Lin, G. S Yang, Y. L. Lin, C. Y. Wu, C. C. Yeh, M. S. Lin, J. K. Chen, Alan Liang, Y. J. Chang, and Tahui Wang, "Comparison of Copper Interconnect Electromigration Behaviors in Various Low-k Materials for 0.13um Technology", *in Advanced Metallization Conf.(AMC)*, p. 203, 2002.

五、著作總點數： 8 (依新法記點)