國立交通大學

電子工程學系電子研究所

博士論文

系統層級靜電放電測試下之積體電路暫態觸發閂鎖效應

TRANSIENT-INDUCED LATCHUP IN CMOS INTEGRATED CIRCUITS UNDER SYSTEM-LEVEL ESD TEST

研 究 生：許勝福(Sheng-Fu Hsu)

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**A Dissertation
Submitted to
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
For the Degree of Doctor of Philosophy
in
Electronic Engineering**

**June 2006
Hsinchu, Taiwan, Republic of China**

中華民國九十五年六月

推薦函

中華民國 九十五年六月

事由：推薦電子研究所博士班研究生**許勝福**提出論文並參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生**許勝福**已完成電子研究所規定之學科及論文研究訓練。

有關學科部份，許君已修畢31學分（請查閱學籍資料），通過資格考試；有關論文研究部份，許君已完成『系統層級靜電放電測試下之積體電路暫態觸發閂鎖效應』論文初稿，並已有數篇相關之論文發表或送審，茲列舉如下：

(A) Referred Journal Papers:

[1]. M.-D. Ker and **S.-F. Hsu**, “Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test,” *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821–1831, Aug. 2005.

[2]. M.-D. Ker and **S.-F. Hsu**, “Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test,” *IEEE Trans. Electromagnetic Compatibility*, vol. 48, no. 1, pp. 161–171, Feb. 2006.

[3]. M.-D. Ker and **S.-F. Hsu**, “Component-level measurement for transient-induced latchup in CMOS ICs under system-level ESD considerations,” *IEEE Trans. Device and Materials Reliability*, *in press*, 2006.

[4]. **S.-F. Hsu** and M.-D. Ker, “Transient-induced latchup dependency on power-pin damping frequency and damping factor in CMOS integrated circuits,” revised by *IEEE Trans. Electron Devices*.

[5]. **S.-F. Hsu** and M.-D. Ker, “Dependence of device structures on latchup immunity in high-voltage 40-V CMOS process with drain-extended MOSFETs,” submitted to *IEEE Trans. Electron Devices*.

(B) International Conference Papers:

[1]. M.-D. Ker and **S.-F. Hsu**, “Transient-induced latchup in CMOS technology: physical mechanism and device simulation,” in ***IEDM** Tech. Dig.*, 2004, pp. 937–940.

[2]. M.-D. Ker and **S.-F. Hsu**, “Evaluation on efficient measurement setup for transient-induced latchup with bi-polar trigger,” in *Proc. IEEE International Reliability Physics Symp.*, 2005, pp. 121–128.

[3]. **S.-F. Hsu** and M.-D. Ker, “Dependences of damping frequency and damping factor of bi-polar trigger waveforms on transient-induced latchup,” in *Proc. EOS/ESD Symp.*, 2005, pp. 118–125.

[4]. M.-D. Ker and **S.-F. Hsu**, “Evaluations on board-level noise filter networks to suppress transient-induced latchup under system-level ESD test,” in *Proc. EOS/ESD Symp*., 2005, pp. 262–269.

[5]. **S.-F. Hsu** and M.-D. Ker, “Study of board-level noise filters to prevent transient-induced latchup in CMOS integrated circuits during EMC/ESD test,” in *Proc. International Zurich Symp. on Electromagnetic Compatibility*, Singapore, 2006, pp. 533–536.

[6]. **S.-F. Hsu**, M.-D. Ker, G.-L. Lin, and Y.-N. Jou, “Experimental evaluation and device simulation of device structure influences on latchup immunity in high-voltage 40-V CMOS process,” in *Proc. IEEE International Reliability Physics Symp.*, 2006, pp. 140–144.

總言之，許君已具備國立交通大學電子研究所應有的訓練水準。因此推薦許君參加國立交通大學電子研究所博士論文口試。

國立交通大學電子研究所教授　　柯明道　博士

系統層級靜電放電測試下之積體電路
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摘要

隨著半導體製程的持續進步，閂鎖效應(Latchup)的可靠度問題更顯的日趨重要。由於在互補式金氧半場效電晶體製程中無法避免的寄生矽控整流器(Silicon Controlled Rectifier, SCR)，閂鎖效應可藉由正迴授(Positive Feedback)機制所觸發。一但閂鎖效應被觸發，巨大的電流便會在積體電路中產生，造成積體電路產品的電路誤動作，甚至可能因過大的電功率(Power)造成積體電路產品的永久損毀。因此一直以來，積體電路產業便一直致力於發展各種防止閂鎖效應發生的製程技術，如磊晶矽晶圓(Epitaxial Wafer)，退化式井區(Retrograde Well)，溝槽隔絕(Trench Isolation)，以及矽在絕緣層上成長(Silicon on Insulator, SOI)等技術。

暫態觸發閂鎖效應(Transient-Induced Latchup)是指一種由快速暫態觸發源所引起的閂鎖效應。目前為止已有數種暫態觸發源被證實會導致暫態觸發閂鎖效應的發生，包括電源開啟暫態(Power-On Transition)，傳輸線反射(Transmission Line Reflection)，電源供應電壓(Power Supply Voltage)的暫態過電壓突波(Overshoot)及欠電壓突波(Undershoot)，以及電纜放電效應(Cable Discharge Event, CDE)等。這些暫態觸發源已經有各種相對應的實驗

方法來加以驗證積體電路產品對暫態觸發閂鎖效應的防護能力。除了上述幾種暫態觸發源外，一種新的暫態觸發源—系統層級靜電放電效應(System-Level Electrostatic Discharge)，也將在本論文被分析證實為另一種可導致暫態觸發閂鎖效應發生的暫態觸發源。

電子產品為了符合電磁共容(Electromagnetic Compatibility, EMC)法規之要求規範，系統層級靜電放電測試通常被用來評估電子產品對系統層級靜電放電效應的耐受能力(Immunity)。然而在進行系統層級靜電放電測試時，本論文發現系統層級靜電放電所引發的暫態電流將會導致暫態觸發閂鎖效應發生，造成待測電子產品的功能誤動作或者是永久損毀。然而目前為止並沒有任何研究文獻探討造成此一暫態觸發閂鎖效應現象的物理形成機制。因此相關研究對系統或電路設計者而言非常地迫切需要，以期能提供系統層級靜電放電所引發暫態觸發閂鎖效應的相關知識及解決方法。

有鑒於此，本論文將針對由系統層級靜電放電測試所引發的暫態觸發閂鎖效應進行研究分析。主要的研究方向包括：(1)了解造成此暫態觸發閂鎖效應的物理機制，(2)發展相關的元件層級(Component-Level)實驗設置，(3)評估各種面板層級(Board-Level)雜訊濾波器對抑制暫態觸發閂鎖效應的效用，以及(4)暫態觸發閂鎖效應相對於積體電路電源腳位上雜訊電壓之阻尼頻率(Damping Frequency)及阻尼因子(Damping Factor)的關係。除了上述有關暫態觸發閂鎖效應的研究主題外，由於高電壓(High Voltage, HV)互補式金氧半場效電晶體製程中的閂鎖效應一直以來受到工業界所重視。因此本論文也將針對高電壓互補式金氧半場效電晶體製程，研究各種不同的高壓元件結構對閂鎖效應敏感度的影響。

本論文第二章首先針對造成此暫態觸發閂鎖效應的物理機制加以探討分析。經由相關的半導體元件模擬(Device Simulation)分析以及實驗量測驗証，本論文發現系統層級靜電放電將導致一種電壓振幅會隨時間遞減的欠

阻尼弦式電壓(Underdamped Sinusoidal Voltage)產生於積體電路的電源腳位上。此欠阻尼弦式電壓亦稱為雙極性觸發電壓(Bipolar Trigger Voltage)。本論文證實此種欠阻尼弦式電壓乃造成積體電路產生暫態觸發閂鎖效應的主要暫態觸發源。此種欠阻尼弦式電壓會使儲存於積體電路內的少數載子(Minority Carrier)快速移動，進一步形成“掃回電流(Sweep-Back Current)”而引發暫態觸發閂鎖效應。本論文所提出的實驗驗證及元件模擬技巧能提供實用的研究分析工具，以期能進一步發展出能有效防止暫態觸發閂鎖效應的電路設計技巧、佈局(Layout)準則、以及半導體製程技術。

由於目前為止沒有相關的元件層級實驗設置用於評估積體電路對系統層級靜電放電測試所引發暫態觸發閂鎖效應之防護能力，本論文第三章提出一種能有效評估積體電路對暫態觸發閂鎖效應防護能力的元件層級實驗設置。此元件層級實驗設置能產生欠阻尼弦式電壓於待測積體電路的電源供應電壓上，以用來模擬待測積體電路在實際系統層級靜電放電測試下所遭受到的靜電放電干擾情形。本論文所提出的元件層級實驗設置不但能精確評估積體電路對暫態觸發閂鎖效應的防護能力，更能進一步避免積體電路在暫態觸發閂鎖效應發生時所帶來電性過應力(Electric Over Stress, EOS)損害。

為了能更進一步地提升積體電路對暫態觸發閂鎖效應的防護能力，本論文第四章評估了不同面板層級雜訊濾波器對抑制暫態觸發閂鎖效應的實際效用。這些雜訊濾波元件包括電容濾波器、電容−電感濾波器(LC-Like)、π形濾波器、亞鐵鹽珠(Ferrite Bead)、暫態突波抑制器(Transient Voltage Suppressor, TVS)、及混合式濾波器等。藉由這些雜訊濾波元件反耦合(Decouple)或吸收因系統層級靜電放電測試在積體電路電源(地)端造成的瞬間雜訊，則積體電路對抑制暫態觸發閂鎖效應的防護能力將可有效提升。所得到的實驗結果可提供印刷電路板(Printed Circuit Board, PCB)設計者

一個有用的參考準則，以期能利用適當的雜訊濾波器來有效提升積體電路對暫態觸發閂鎖效應的防護能力。

由於在系統層級靜電放電測試下，雙極性觸發電壓已被證實是造成暫態觸發閂鎖效應的主要雜訊電壓觸發源，因此決定雙極性觸發電壓的二個重要參數—阻尼頻率及阻尼因子，決定了暫態觸發閂鎖效應對雙極性觸發電壓的敏感度。本論文第五章利用元件模擬探討暫態觸發閂鎖效應相對於雙極性觸發電壓之阻尼頻率及阻尼因子的關係。此相關研究成果可應用在高效能晶片濾波器(On-Chip Filter)設計，以抑制暫態觸發閂鎖效應。也可應用於發展高效能元件層級暫態觸發閂鎖效應量測裝置，以準確評估待測積體電路對抑制暫態觸發閂鎖效應的防護能力。

閂鎖效應在高壓互補式金氧半場效電晶體製程中扮演著一個非常重要的角色。和一般標準積體電路製程不同的是，利用高壓積體電路製程所製造出來的積體電路，其額定電源供應電壓一般皆高於十伏特(Volt)。在此高壓積體電路中所寄生的矽控整流器，其維持電壓(holding voltage)一般皆遠低於其額定電源供應電壓。這意味著閂鎖效應在高壓積體電路中大多是無法避免的，導致閂鎖效應在高壓積體電路中扮演著一個極關鍵的角色。有鑒於此，本論文第六章將針對 0.25 微米高壓 40 伏特積體電路製程中的汲極擴散(Drain-Extended)金氧半場效電晶體，研究各種不同的元件結構及佈局幾合參數對於閂鎖效應敏感度的相互關係。所得到的相關實際晶片量測結果可藉由半導體元件模擬進一步地加以分析驗証。利用本論文所提出的各種實驗測試結構及元件模擬技巧，可進一步評估萃取(Extract)出能適用在高壓積體電路中的閂鎖效應防護佈局準則。

以上針對由系統層級靜電放電測試所引發的暫態觸發閂鎖效應，以及高壓積體電路製程中的閂鎖效應特性，本論文所進行的相關研究皆有實際晶片量測及元件模擬驗証，並有相對應的國際會議及期刊論文發表。

TRANSIENT-INDUCED LATCHUP IN CMOS INTEGRATED CIRCUITS UNDER SYSTEM-LEVEL ESD TEST

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Abstract

With the continual scaling of CMOS technologies, latchup is an increasingly significant reliability issue in semiconductor technologies. Because of the parasitic silicon controlled rectifier (SCR) in CMOS technologies, latchup can be initiated via a positive regeneration feedback if there is large enough substrate or well current. Once latchup occurs in a powered system, huge current can conduct through a low-impedance path from the power supply to ground nodes. If the resulting high current is not limited, irreversible damages can occur to the CMOS ICs due to the latchup-generated high power. Even though the latchup current is limited to prevent the permanent damage, it is possible that the CMOS ICs will malfunction. For a long time, IC industry has been devoted to develop process solutions for latchup prevention, such as epitaxial layer, retrograde well, trench isolation, and silicon on insulator (SOI).

Transient-induced latchup (TLU) means a latchup event initiated by a fast “transient” triggering mode. Continual scaling of device feature size leads to an increasing susceptibility to TLU of the CMOS ICs. Thus, the TLU reliability issue has attracted more attentions recently than before in CMOS technologies. Several different transient triggering modes have been proven to be able to initiate TLU, such as power-on transition, transmission line reflections, supply voltage overshoots or undershoots, and cable discharge event (CDE). For these transient triggering modes, several corresponding measurement setups have been also

developed to evaluate the TLU immunity of CMOS ICs. In addition to these transient triggering modes, the system-level electrostatic discharge (ESD) event has been proven a new TLU-triggering mode in this dissertation.

For electronic products to satisfy the electromagnetic compatibility (EMC) regulations, system-level ESD test is necessary to evaluate the system-level ESD robustness of electronic products. During the system-level ESD test, the ESD-generated transient current can induce TLU in CMOS ICs within the electronic products, leading to temporary shutdown or permanent damage of the equipment under test (EUT). So far there is no literature to clarify the physical mechanism of TLU under the system-level ESD test. Thus, a clear understanding of TLU physical mechanism is necessary to help system or IC designers to solve TLU issues under the system-level ESD test.

This dissertation focuses on the analysis and characterization of TLU under the system-level ESD test. Several major topics including: (1) clarification of TLU physical mechanism, (2) development of component-level TLU measurement setup, (3) evaluations of board-level noise filters to suppress TLU, (4) and TLU dependency on power-pin damping frequency and damping factor, are discussed in this dissertation. In addition to the TLU topic, latchup is also a very significant reliability issue in a high-voltage (HV) CMOS process. This dissertation also investigates the dependences of the device structure on latchup immunity in a HV 40-V CMOS process with drain-extended MOSFETs (DEMOS).

In chapter 2, the physical mechanism of TLU in CMOS ICs under the system-level ESD test is clearly characterized by device simulation and experimental verification in time domain. For TLU characterization, an underdamped sinusoidal (bipolar) voltage stimulus has been clarified as the realistic TLU-triggering stimulus under the system-level ESD test. The specific “sweep-back” current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. Through both the understanding of physical mechanism and the proposed simulation/verification methodology on TLU, the safe design/layout rules or circuit techniques in CMOS ICs can be developed against TLU events.

Because no component-level measurement setup has been developed to evaluate the TLU immunity of CMOS ICs under the system-level ESD test, an efficient component-level TLU measurement setup with bipolar trigger is developed in chapter 3. From the experimental and simulation results, TLU measurement setup without a current-blocking diode but with a small current-limiting resistance is suggested to accurately evaluate the TLU immunity of CMOS ICs without over estimation or electric over stress (EOS) damage to DUT.

The proposed component-level TLU measurement setup can be widely utilized to evaluate the TLU immunity of CMOS ICs in practical field applications.

To further suppress the susceptibility to TLU under the system-level ESD test, different board-level noise filter networks are evaluated in chapter 4 to find their effectiveness for TLU prevention under the system-level ESD test. By using the proposed component-level TLU measurement setup in this dissertation, it can be proved that the TLU immunity of CMOS ICs can be greatly improved with proper noise filter networks. All the experimental evaluations have been verified with the SCR test structures and the ring oscillator circuit fabricated in a 0.25-µm CMOS technology.

TLU dependency on two dominant parameters of the TLU-triggering bipolar voltage—damping frequency and damping factor, is also investigated by device simulation and experimental measurement in chapter 5. Damping frequency and damping factor are two dominant parameters of bipolar transient noises, and they are strongly dependent on the system shielding, board-level noise filter, chip-/board- level layout, etc. The simulated TLU characteristics are useful for optimizing a bipolar trigger to evaluate the TLU immunity of CMOS ICs without overestimation. Furthermore, the board-/chip- level noise filters can be properly designed to efficiently eliminate the ESD-coupled noises for TLU prevention.

In order to characterize the latchup characteristics in HV CMOS process, chapter 6 investigates the dependence of device structures on latchup immunity in a 0.25-µm HV 40-V CMOS process with DEMOS transistors. Layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. All the experimental results can be qualitatively and quantitatively verified with 2-D device simulation. Both the proposed latchup test structures and simulation methodologies can be further applied to extract safe and compact design rule for latchup prevention in HV CMOS ICs.


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誌　謝

在此首先要感謝柯明道教授這四年來的細心指導與鼓勵，使我得以順利完成博士學位。在柯教授的指導教誨下，除了在課業研究上所獲得的指導外，柯教授認真的研究態度與嚴謹的處事原則更讓我獲益良多，也讓我了解到如何面對並克服困難的重要性。

在這段求學過程中，我要特別感謝『工研院系統晶片技術發展中心』的『產品與靜電防護技術部』、『奇景光電股份有限公司』、『世界先進積體電路股份有限公司』、『閎康科技股份有限公司』等給予我在研究方面的支持與協助。在此我要特別感謝曾任職於『工研院系統晶片技術發展中心』的林昆賢博士、莊哲豪先生、陳子平先生，任職於『奇景光電股份有限公司』的蔡志忠副總、陳東暘博士、羅文裕先生，任職於『世界先進積體電路股份有限公司』的林耿立經理、周業甯先生，以及任職於『閎康科技股份有限公司』的謝詠芬博士等人所給予我在研究方面的支持與協助。

我也要感謝『奈米電子與晶片系統實驗室』的陳世倫、陳榮昇、徐新智、鄧志剛、張瑋仁、顏承正、蕭淵文、陳世宏以及實驗室其他學長、同學、及學弟妹們，在我博士班學業生涯中所給予我的支持與協助。在此也要感謝實驗室助理卓慧貞小姐在實驗室行政事務上的許多協助。

最後，我要在此由衷感謝我的父親許永賜先生、母親王玉秋女士、祖父許圳生先生、哥哥許真祿先生、姐姐許雯卿女士、女友陳婉如小姐，沒有你們這多年來的付出、鼓勵、扶持與照顧，就沒有我今日的成就，在此再一次表達我最衷心的感謝。另外，要祝福所有在這幾年來與我相處過的師長、朋友、學弟妹們，有緣與你們同在這一階段成長，是我一生的榮幸，願大家平安和樂，事事順心！

許勝福
謹誌於竹塹交大
九十五年　六月

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Fig. 5.8 Simulated V_{DD} and I_{DD} transient responses for bipolar trigger voltage with D_{Factor}, D_{Freq}, and V_P of $1.5\times10^6 s^{-1}$, 0.1MHz, and -200V, respectively. TLU doesn't occur because t_P is too long (~3μs) to generate sufficient I_{Sb} [28], [29].

Fig. 5.9 Simulated V_{DD} and I_{DD} transient responses for bipolar trigger voltage with the same parameters as those in Fig. 5.8 but with V_P of +150V. TLU can be triggered on by I_{Ds} while V_{DD} initially increases from the normal operating voltage (+2.5V) to $+V_{Peak}$.

Fig. 5.10 Simulated V_{DD} and I_{DD} transient responses for bipolar trigger voltage with D_{Factor}, D_{Freq}, and V_P of $1.5\times10^6 s^{-1}$, 2GHz, and -60V, respectively. I_{DD} cannot follow the V_{DD} variation in time for such a high-D_{Freq} (>1GHz) bipolar trigger, because $+I_{Peak}$ doesn't simultaneously appear with $+V_{Peak}$ but at the end of the first duration (~50.5ns).

Fig. 5.11 Relations between (a) D_{Factor} and $D_{Freq(min)}$, and (b) D_{Factor} and $D_{Freq(max)}$. $D_{Freq(min)}$ ($D_{Freq(max)}$) is defined as the minimum (maximum) D_{Freq} to initiate TLU under a fixed V_P of +15V or -15V.

Fig. 5.12 Measured V_{DD} and I_{DD} transient responses of the SCR with V_{Charge} of (a) +10V, and (b) +14V.

Fig. 5.13 With a discharge resistor with resistance of 1.5kΩ between the relay and the V_{DD} node in TLU measurement setup (Fig. 2.7), the measured V_{DD} and I_{DD} transient responses with V_{Charge} of (a) +120V, and (b) +200V. In Figs. 5.12(b) and 5.13(b), the minimum $-V_{Peak}$ to initiate TLU is fixed (-2.5V) for the same SCR structure (D=6.7μm, S=1.2μm, and W=22.5μm).

Fig. 5.14 Relations between the decoupling capacitance and the TLU level of SCR.

Chapter 6

Fig. 6.1 Device cross-sectional views of the (a) isolated, and (b) non-isolated, n-DEMOS.

Fig. 6.2 Device cross-sectional view of the isolated p-DEMOS.

Fig. 6.3 Device cross-sectional view of the non-isolated symmetric n-DEMOS.

Fig. 6.4 Device cross-sectional view of the inverter logic circuit consisting of a non-isolated asymmetric n-DEMOS and an isolated asymmetric p-DEMOS.

Fig. 6.5 (a) Device cross-sectional view, and (b) layout top view, of the test structure A. Test structure A is used to simulate the parasitic SCR resulting from the non-isolated asymmetric n-DEMOS and isolated asymmetric p-DEMOS.

Fig. 6.6 (a) Device cross-sectional view, and (b) layout top view, of the test structure B. Test structure B is used to simulate the parasitic SCR resulting from the non-isolated symmetric n-DEMOS and isolated symmetric p-DEMOS.

Fig. 6.7 (a) Device cross-sectional view, and (b) layout top view, of the test structure C. Test structure C is used to simulate the parasitic SCR resulting from the isolated asymmetric n-DEMOS and p-DEMOS.

Fig. 6.8 Relationships between TLP-measured latchup trigger (holding) voltage and anode-to-cathode spacing for test structures A, B, and C.

Fig. 6.9 TLP-measured latchup I-V characteristics of test structure C with anode-to-cathode spacing of 27.5µm.

Fig. 6.10 TLP-measured latchup I-V characteristics of test structure A with anode-to-cathode spacing of 31.6µm.

Fig. 6.11 TLP-measured latchup I-V characteristics of test structure B with anode-to-cathode spacing of 31.6µm.

Fig. 6.12 Relationships between TLP-measured latchup trigger (holding) voltage and guard ring width for test structures A, B, and C with anode-to-cathode spacing (parameter “X”) of 19.6µm, 25.6µm, and 27.5µm, respectively.

Fig. 6.13 Device structures used in the 2-D device simulation for (a) test structure A, (b) test structure B, and (c) test structure C. These device structures have the same layout parameters as the silicon test chips.

Fig. 6.14 Simulated latchup I-V characteristics for the test structures A and B with anode-to-cathode spacing of 31.6µm, and for the test structure C with anode-to-cathode spacing of 27.5µm. All these test structures have the same guard ring width of 0.8µm.

Fig. 6.15 Simulated 2-D current flow lines under latchup condition for (a) test structure A, (b) test structure B, and (c) test structure C.

Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the background of transient-induced latchup (TLU) is introduced. Secondly, the categories of TLU-triggering modes in field applications are discussed. Finally, the organization of this dissertation is well described.

1.1. Background of Transient-Induced Latchup (TLU)

It has been a long time since latchup was a significant reliability issue in semiconductor technologies [1]-[15]. Latchup originates from the parasitic silicon controlled rectifier (SCR), which is composed of two cross-coupled parasitic bipolar junction transistors (BJTs) in CMOS technologies. The device cross-sectional view of an inverter circuit is shown in Fig. 1.1. These two parasitic BJTs are a vertical PNP (Qpnp) and a lateral NPN (Qnpn) BJT. The equivalent circuit of the parasitic SCR is illustrated in Fig. 1.2. Once there is large enough substrate (well) current flowing through the parasitic substrate (well) resistance of R_{Sub} (R_{Well}), the Qnpn (Qpnp) will be turned on because of its forward-biased emitter-base junction. Thus, the other Qpnp (Qnpn) will be also turned on via the mechanism of the positive regeneration feedback. If the product of the beta gains of these two BJTs is larger than one, this positive feedback mechanism can lead to a large current conducting through a low-impedance path from V_{DD} (source of PMOS) to GND (source of NMOS). This phenomenon is the so called latchup. As a result, CMOS ICs will malfunction or even be burned out due to the latchup-generated high power.

TLU means a latchup event initiated by a fast “transient” triggering mode. Once some transient triggering mode happens to generate large enough substrate or well current in CMOS ICs, TLU can be triggered on via a positive-feedback mechanism. With the continual scaling of CMOS technologies [16], the smaller device feature size enables a larger packing density of transistors in CMOS chips. However, CMOS ICs are more susceptible to TLU because the spacing from N+ to P+ junction has been also continuously decreasing. Thus, the reliability issue of TLU has attracted more attentions recently than before in CMOS technologies [17]-[25]. For the quasi-static latchup, the formal test standard [26] has been announced and widely used for evaluations of latchup immunity. For TLU, however, there is no related formal test standard, but only “standard practice” [27] to evaluate the TLU immunity of CMOS ICs. Thus, it’s necessary to clarify the TLU physical mechanism, to develop an efficient TLU measurement setup, and to develop a useful TLU-protection design for high-robustness CMOS ICs.

1.2. Categories of TLU-Triggering Modes

Several different transient triggering modes have been proven to be able to initiate TLU [3]-[6], [20], [21], [27]. These transient triggering modes include power-on transition [3], [4], transmission line reflections [5], [6], supply voltage overshoots [20] or undershoots [27], and cable discharge event (CDE) [21]. In most of these transient triggering modes, their corresponding measurement setups have been also developed to evaluate the TLU immunity of CMOS ICs. In addition to these transient triggering modes, a new TLU-triggering mode called system-level electrostatic discharge (ESD) event [28], [29] has been analyzed in this dissertation. These TLU-triggering modes are introduced below.

1.2.1. Power-On Transition [3], [4]

When power-supply voltage ramps up from 0V to its normal circuit operating voltage during the power-on transition, the displacement current will be formed due to the rapid-increasing power-supply voltage. The time-dependent power-supply voltage during the power-on transition is shown in Fig. 1.3. The ramp rate (RA) of the power-supply voltage during the power-on transition can be expressed as

$$RA \equiv \frac{V_{DD}}{T_r}. \tag{1.1}$$

V_{DD} is the normal circuit operating voltage, and T_r is the rise time of power-supply voltage. Once RA is above some critical value, TLU will be triggered on by the large enough displacement current that flows through the well/substrate junction capacitance ($C_{Well\text{-}Sub}$) of CMOS ICs, as shown in Fig. 1.4. By applying different ramp rates of the power-supply voltage, the threshold ramp rate to initiate TLU can be evaluated. The susceptibility of this TLU is strongly dependent on the ramp rate of the power-supply voltage, because TLU can occur even if the normal circuit operating voltage is far below the required latchup trigger voltage in DC latchup I-V characteristic.

1.2.2. Transmission Line Reflections [5], [6]

When the transmission line reflections take place due to impedance mismatch during signal propagation, transient voltage overshoots or undershoots can occur on the I/O pins of CMOS ICs, as shown in Fig. 1.5. Because the I/O pins are directly connected to P+ (N+) diffusions in N-well (P-substrate), such transient voltage overshoots (undershoots) can make the emitter-base junction of the parasitic PNP (NPN) BJT momentarily forward-biased. Once the forward-biased emitter-base junction of one parasitic BJT provides enough diffusion current to turn on the other parasitic BJT, the positive-feedback regeneration mechanism can induce TLU. The techniques to simulate transient voltage overshoots and undershoots on the I/O pins of CMOS ICs are shown in Fig. 1.6(a) and 1.6(b), respectively. The transient voltage overshoots (undershoots) can be simulated by applying a rectangular voltage pulse on the emitter-base junction of parasitic PNP (NPN) BJT in CMOS ICs. Thus, the threshold voltage amplitude and pulse width to initiate TLU can be determined. In general, when the pulse width decreases, the threshold voltage amplitude required to induce TLU will increase. However, when the pulse width is long enough, a quasi-static situation could be reached. As a result, the threshold voltage amplitude required to induce TLU is approximate to the DC bias (~0.7V) required to turn on the emitter-base junction of the parasitic BJT in CMOS ICs.

1.2.3. Supply Voltage Overshoots/Undershoots [20], [27]

The transient overshoots or undershoots on power-supply voltage can take place due to the noise coupling under system or environment disturbance, as shown in Fig. 1.7. Such transient overshoots or undershoots on power-supply voltage can induce the junction diffusion or displacement current within the CMOS ICs. If the diffusion or displacement current is large enough to activate the parasitic PNP or NPN BJT, TLU can be triggered on and sustained via the regeneration feedback. The techniques to simulate the transient overshoots and undershoots on power-supply voltage are shown in Fig. 1.8(a) and 1.8(b), respectively. The power-supply voltage overshoots (undershoots) can be simulated by applying a positive (negative) rectangular pulse voltage which is superposed on the normal circuit operating voltage (V_{DD}). The positive rectangular pulse voltage can simulate a rapid-increasing power supply voltage, leading to the excitation of transient displacement current. The negative rectangular pulse voltage can simulate a power-supply voltage undershoot with a negative peak voltage, leading to the excitation of P-substrate/N-well junction diffusion current. Related experimental results show that the threshold voltage amplitude required to initiate TLU will decrease with the pulse width, regardless of positive or negative voltage pulse.

1.2.4. Cable Discharge Event [21]

Large number of charges can accumulate in cables when the un-terminated cables are dragged on the floor (known as triboelectricity). CDE is the phenomenon in which the accumulated charges in cables are discharged into another object in proximity. An example of the CDE event occurring on the Ethernet interface of computer systems is shown in Fig. 1.9. Once the accumulated static charges in cables are discharged into the I/O pins of the CMOS ICs, TLU can be easily initiated within the CMOS ICs due to the injection of the transient positive or negative current.

CDE-induced TLU is a typical off-chip signal latchup-triggering event, the injection of the CDE-induced current can induce TLU on I/O or internal circuits of CMOS ICs. For the general off-chip signal latchup-triggering events, most CMOS IC products use the EIA/JESD78 latchup test [26] to evaluate the product robustness. Compared with the other off-chip signal latchup-triggering events, however, CDE-induced latchup is a more severe latchup condition because the injection of CDE-induced current can possess peak current of several amperes. Thus, the EIA/JESD78 latchup test standard is unsuitable for evaluations of the CDE-induced latchup robustness, and so far there is no established component-level test standard for CDE-induced latchup. In the state-of-the-art CMOS technologies where the TLU issues are more severe, design methodologies to suppress CDE-induced TLU are necessarily developed.

1.2.5. System-Level ESD Event [28], [29]

ESD is a phenomenon due to the electrostatic charges transferring from one object to another with different electric potentials [30], [31]. Usually, huge transient current or electromagnetic interferences (EMI) accompany ESD phenomenon. In real world, electronic products or systems could malfunction or be damaged when subject to ESD events. Thus, system-level ESD event is an important interference source to evaluate the electromagnetic sustainability (EMS) of electronic products. Thus, for electronic products to satisfy the electromagnetic compatibility (EMC) regulations, system-level ESD test [32] is necessary to evaluate the system-level ESD robustness of electronic products.

An example of the system-level ESD test with direct contact discharge test mode on an electronic product is shown in Fig. 1.10. Compared with the component-level ESD tests [33], [34] where the objects under test are ICs, the system-level ESD test aims to evaluate the robustness of electronic products. The equivalent circuit of ESD gun used in the system-level ESD test is shown in Fig. 1.11. The ESD gun has the charging (energy-storage) capacitor of 150pF and discharge resistor of 330Ω. The equivalent circuit of human body model (HBM) in the component-level ESD test is shown in Fig. 1.12. In the HBM component-level ESD test, however, the charging capacitor (discharge resistor) is a smaller (larger) value of 100pF (1.5kΩ). Thus, compared with the ESD current in component-level ESD test, ESD current in system-level ESD test has much larger peak current and shorter rise time, leading to more severe damages for electronic products or their interior ICs. Additionally, ESD protection designs for system- and component- level ESD tests are quite different. It has been proven [35] that a robust CMOS IC product with high component-level ESD levels could be very susceptible to the system-level ESD test. Thus, efficient ESD protection methodologies against system-level ESD events are very significant for electronic products.

During the system-level ESD test, the ESD-generated transient current can induce TLU in CMOS ICs within the electronic products, leading to temporary shutdown or permanent damage of the equipment under test (EUT). However, so far there is no literature to clarify the physical mechanism of TLU under the system-level ESD test. Additionally, no component-level measurement setup has been developed to evaluate the TLU immunity of CMOS ICs under the system-level ESD test. Thus, a clear understanding of TLU physical mechanism is necessary to help system or IC designers to solve TLU issues under the system-level ESD test.

1.3. Organization of This Dissertation

This dissertation is composed of seven chapters. This dissertation (chapter 2 ~ chapter 5) focuses on the analysis and characterization of TLU under the system-level ESD test. Several major topics including: (1) clarification of TLU physical mechanism (chapter 2), (2) development of component-level TLU measurement setup (chapter 3), (3) evaluations of board-level noise filters to suppress TLU (chapter 4), (4) and TLU dependency on power-pin damping frequency and damping factor (chapter 5), are discussed in this dissertation. In addition to the TLU topic, latchup is a very significant reliability issue in a high-voltage (HV) CMOS process [36], [37]. Thus, this dissertation (chapter 6) also investigates the dependences of the device structures on latchup immunity in a HV 40-V CMOS process with drain-extended MOSFETs (DEMOS). Chapter 7 gives the conclusions and future works of this dissertation. The outlines of each chapter are summarized below.

In chapter 2, the physical mechanism of TLU in CMOS ICs under the system-level ESD test is clearly characterized by device simulation and experimental verification in time domain. For TLU characterization, an underdamped sinusoidal (bipolar) voltage stimulus has been clarified as the realistic TLU-triggering stimulus under the system-level ESD test. The specific “sweep-back” current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. All the simulation results on TLU have been practically verified in silicon with test chips fabricated in a 0.25-μm CMOS process.

Chapter 3 optimizes an efficient component-level TLU measurement setup with bipolar (underdamped sinusoidal) trigger. The developed measurement setup can accurately evaluate the immunity of CMOS ICs against TLU under the system-level ESD test. Current-blocking diode and current-limiting resistance, which are generally suggested to be used in TLU measurement setup with bipolar trigger, are investigated for their impacts to both bipolar trigger waveforms and TLU immunity of device under test (DUT). All the experimental results have been successfully verified with device simulation. From the experimental and simulation results, TLU measurement setup without a current-blocking diode but with a small current-limiting resistance is suggested, which can accurately evaluate the TLU immunity of CMOS ICs without over estimation or EOS damage to DUT. The suggested measurement setup has been verified with the SCR test structures and the real circuitry (ring oscillator) fabricated in a 0.25-μm CMOS technology.

In chapter 4, different types of board-level noise filter networks are evaluated to find their effectiveness for improving the immunity of CMOS ICs against TLU under the system-level ESD test. By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs can be greatly improved. All the experimental evaluations have been verified with the SCR test structures and the ring oscillator circuit fabricated in a 0.25-μm CMOS technology. Some of such board-level solutions can be further integrated into the chip design to effectively improve the TLU immunity of CMOS IC products.

In chapter 5, TLU dependency on power-pin damping frequency and damping factor is characterized by device simulation and verified by experimental measurement. Damping frequency and damping factor are two dominant parameters of bipolar transient noises, and they are strongly dependent on the system shielding, board-level noise filter, chip-/board-level layout, etc. From the simulation results, bipolar trigger waveform with damping frequency of several tens of megahertz can trigger on TLU most easily. However, TLU is less sensitive to bipolar trigger waveform with an excessively large damping factor, an excessively high damping frequency, or an excessively low damping frequency. The simulation results have been experimentally verified with the SCR test structures fabricated in a 0.25-μm CMOS technology.

In chapter 6, the dependence of device structures on latchup immunity in a 0.25-μm HV 40-V CMOS process with DEMOS transistors has been verified with silicon test chips and investigated with device simulation. Layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. It was demonstrated that the drain-extended NMOS (n-DEMOS) with a specific isolated device structure can greatly enhance the latchup immunity. The proposed test structures and simulation methodologies can be applied to extract safe and compact design rule for latchup prevention of DEMOS transistors in HV CMOS process.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

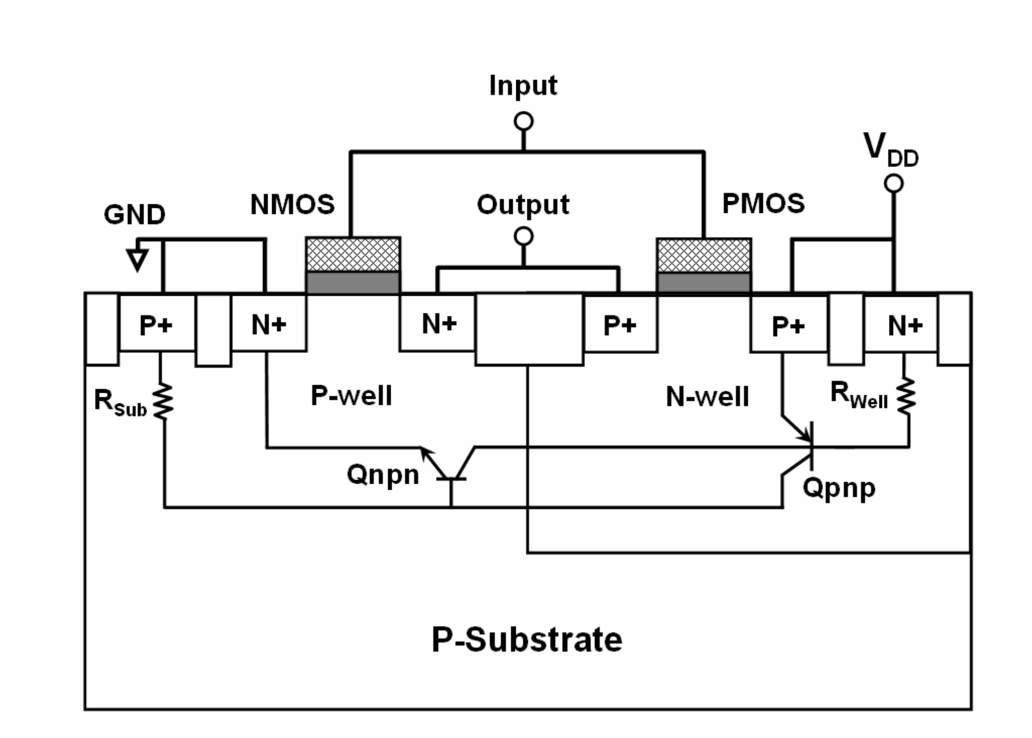


Fig. 1.1 Device cross-sectional view of an inverter circuit in CMOS technologies. Two parasitic BJTs are a vertical PNP (Qpnp) and a lateral NPN (Qnpn) BJT.

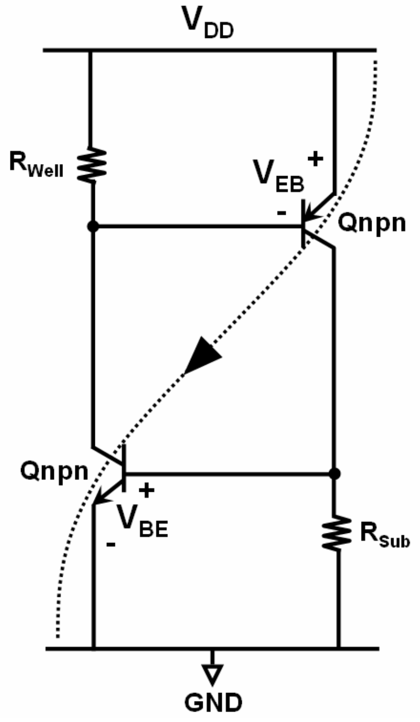


Fig. 1.2 Equivalent circuit of the parasitic SCR in CMOS technologies.

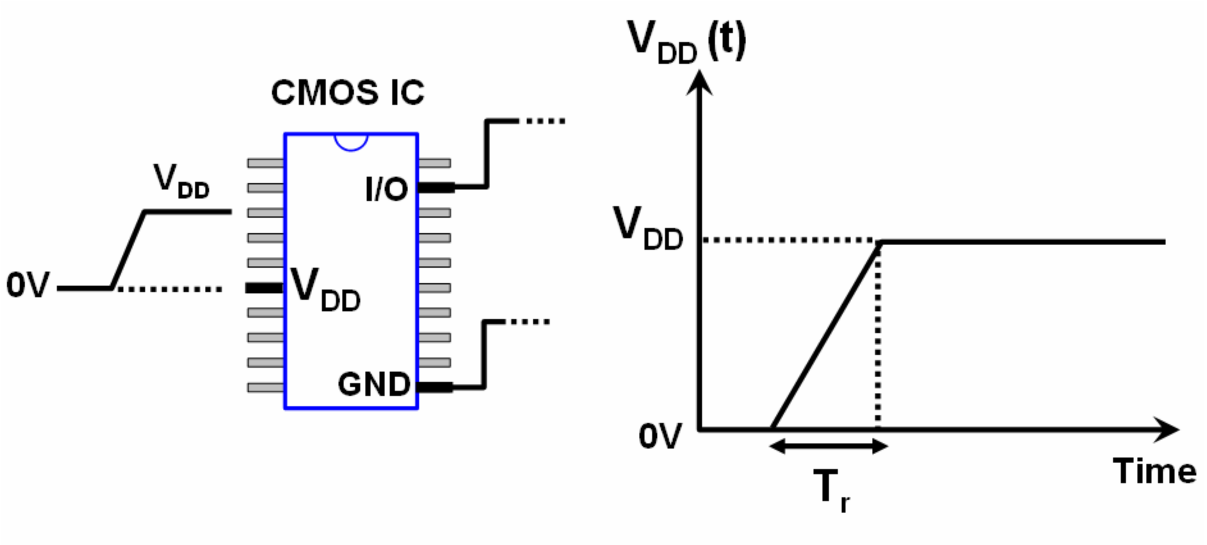


Fig. 1.3 Time-dependent power-supply voltage during the power-on transition.

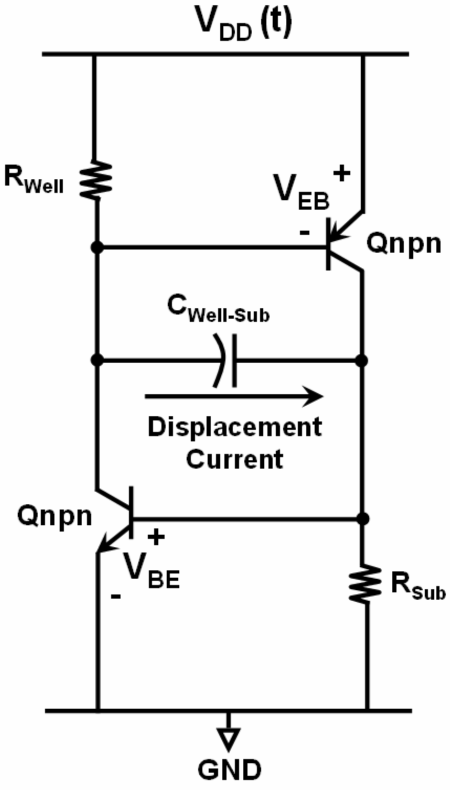


Fig. 1.4 Displacement current generated by the rapid-increasing power-supply voltage on the well/substrate junction capacitance ($C_{Well\text{-}Sub}$).

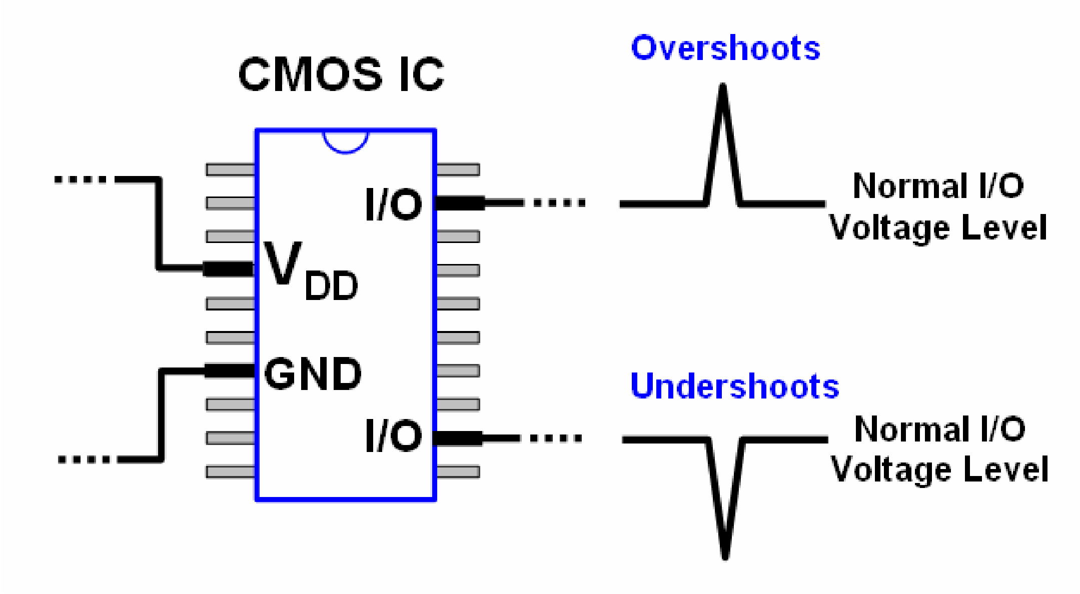
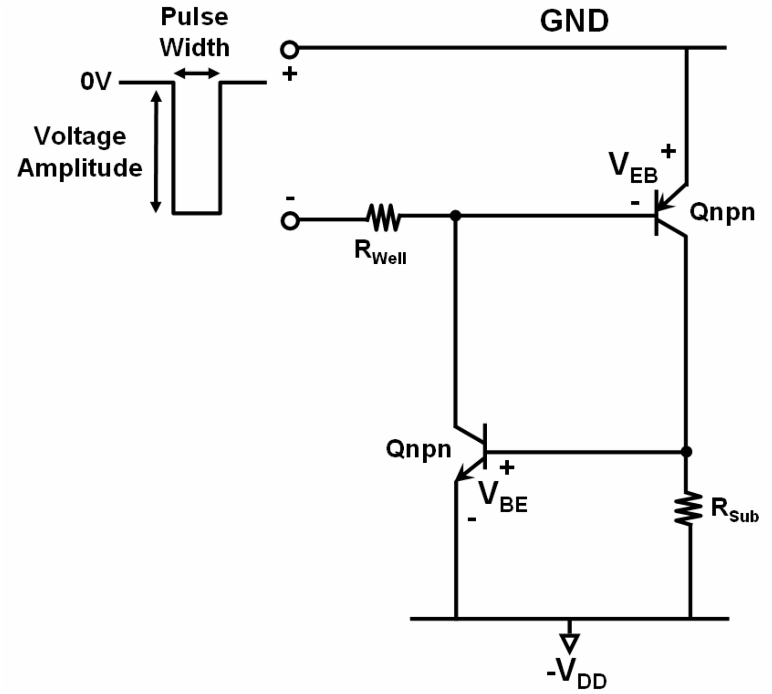
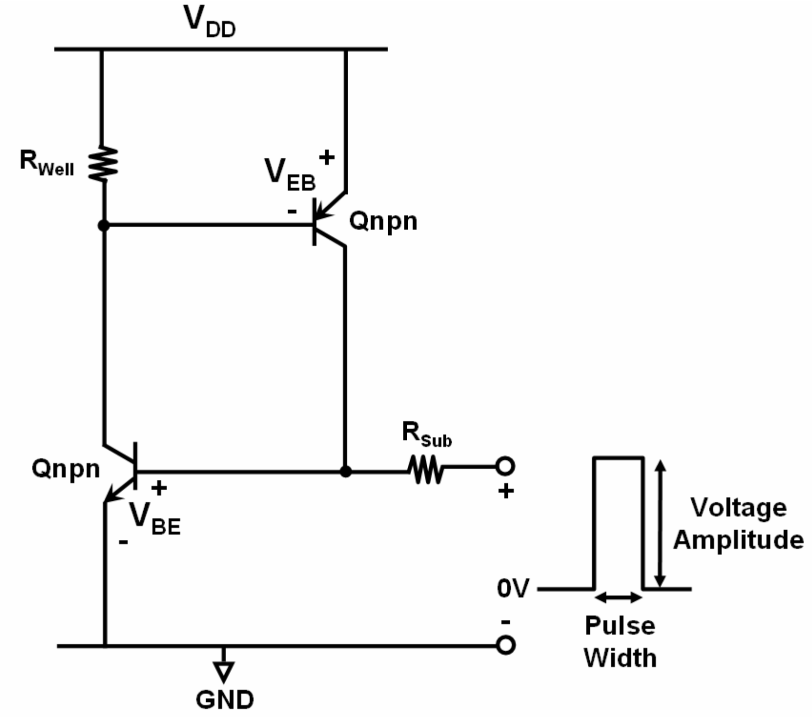


Fig. 1.5 Transient voltage overshoots or undershoots on the I/O pins of CMOS ICs due to the transmission line reflections.



(a)



(b)

Fig. 1.6 Techniques to simulate the transient (a) overshoots, and (b) undershoots, on the I/O pins of CMOS ICs.

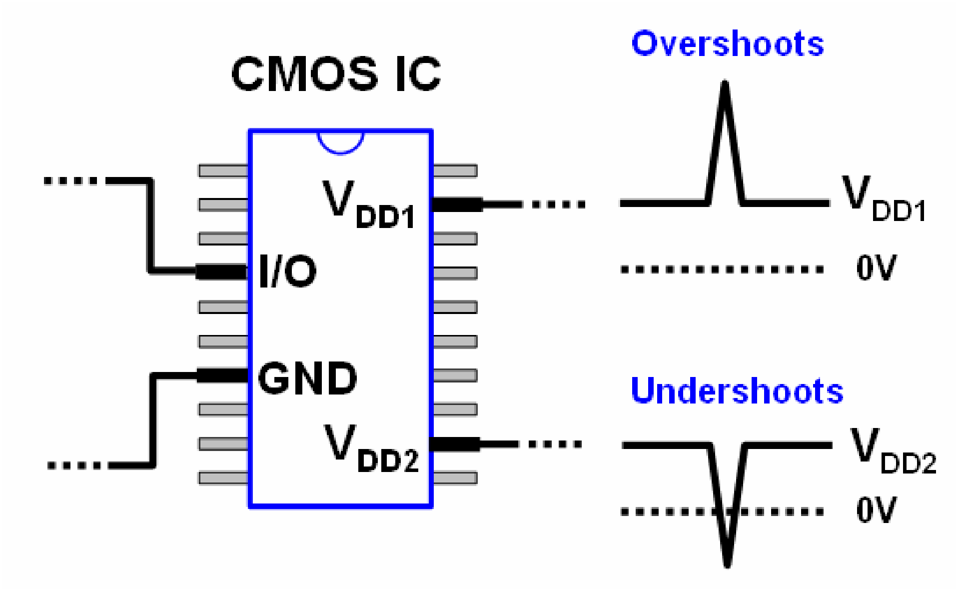
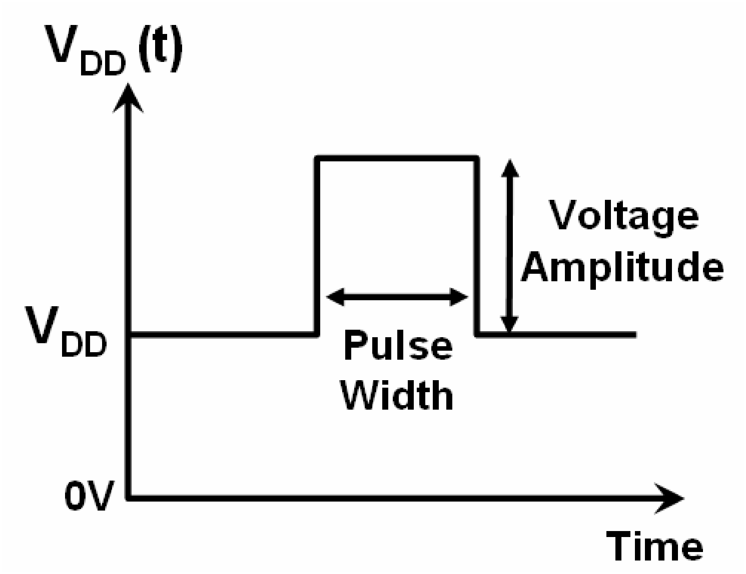
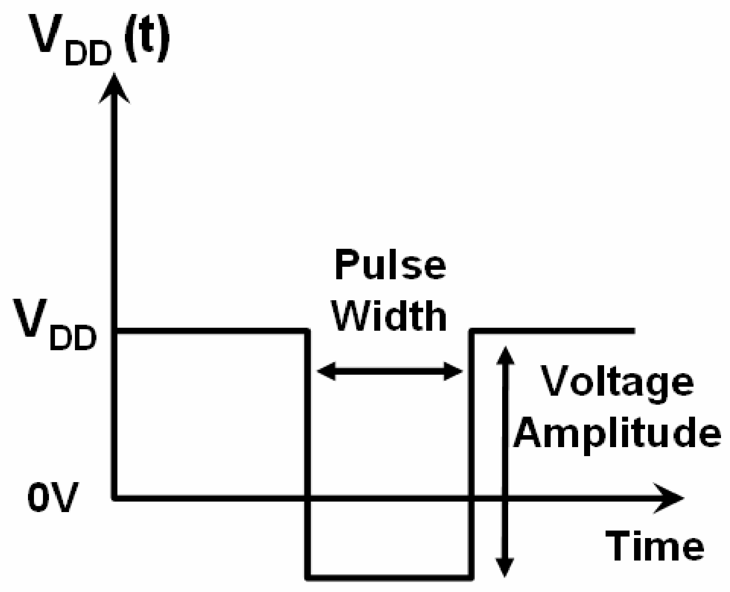


Fig. 1.7 Transient overshoots or undershoots on the power-supply voltage due to the noise coupling under system or environment disturbance.



(a)



(b)

Fig. 1.8 Techniques to simulate the transient (a) overshoots, and (b) undershoots on power-supply voltage of CMOS ICs. V_{DD} is the normal circuit operating voltage.

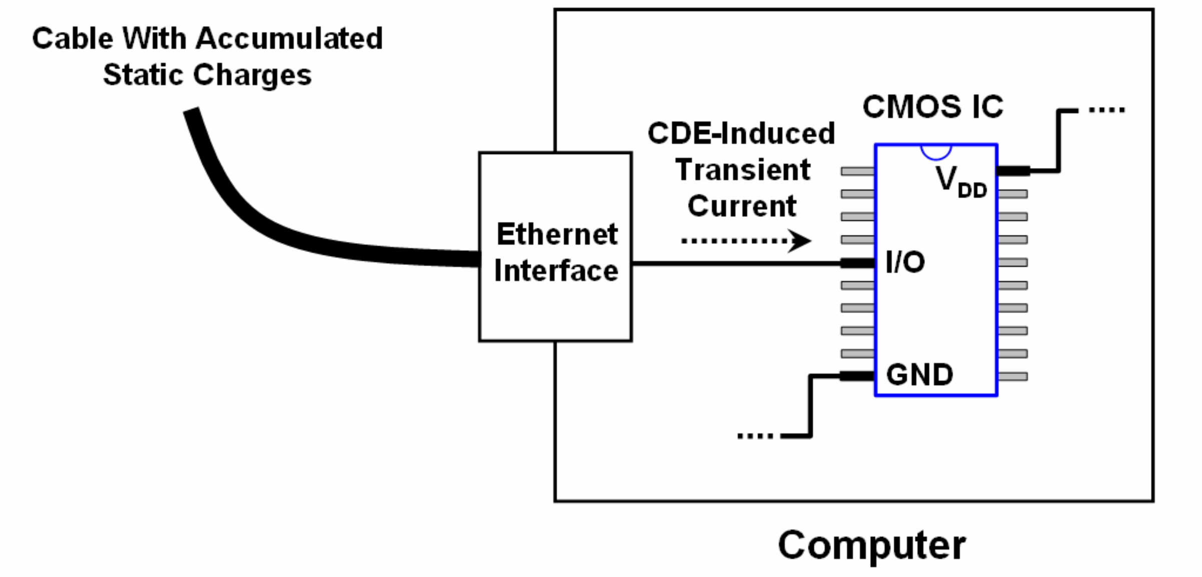


Fig. 1.9 Example of the CDE event occurring on the Ethernet interface of computer systems.

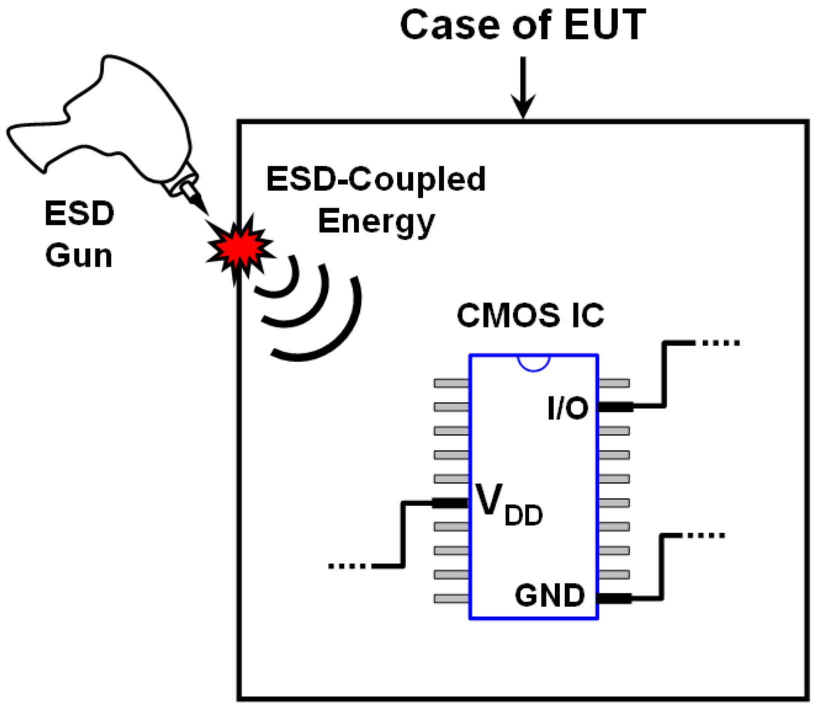


Fig. 1.10 Example of the system-level ESD test with direct contact discharge test mode on an electronic product.

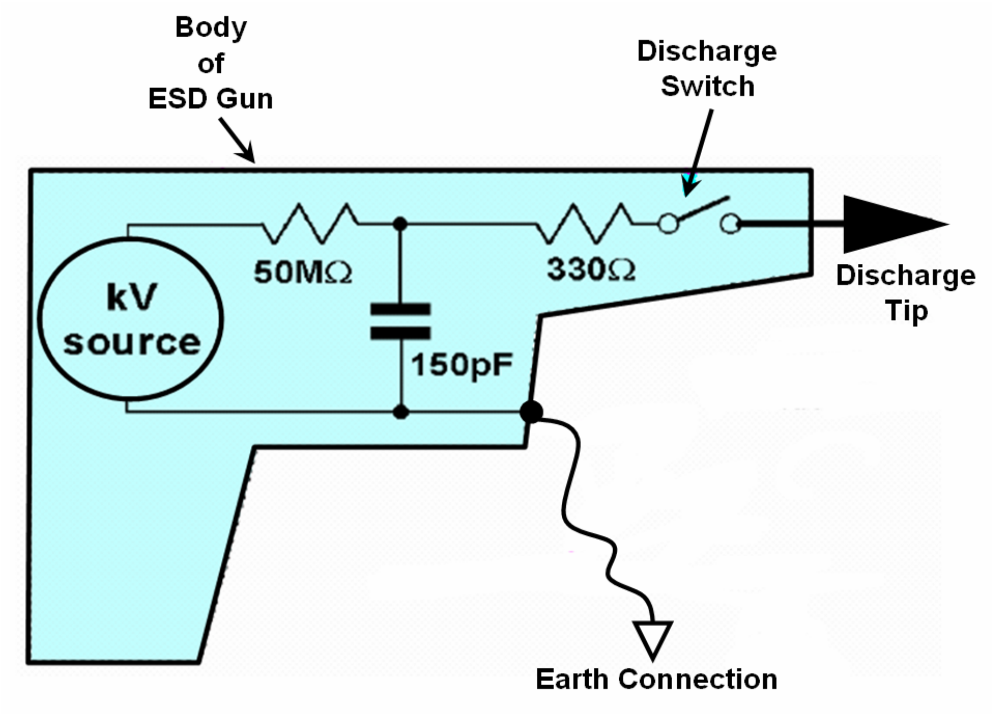


Fig. 1.11 Equivalent circuit of ESD gun used in the system-level ESD test. The ESD gun has the charging (energy-storage) capacitor of 150pF and discharge resistor of 330Ω.

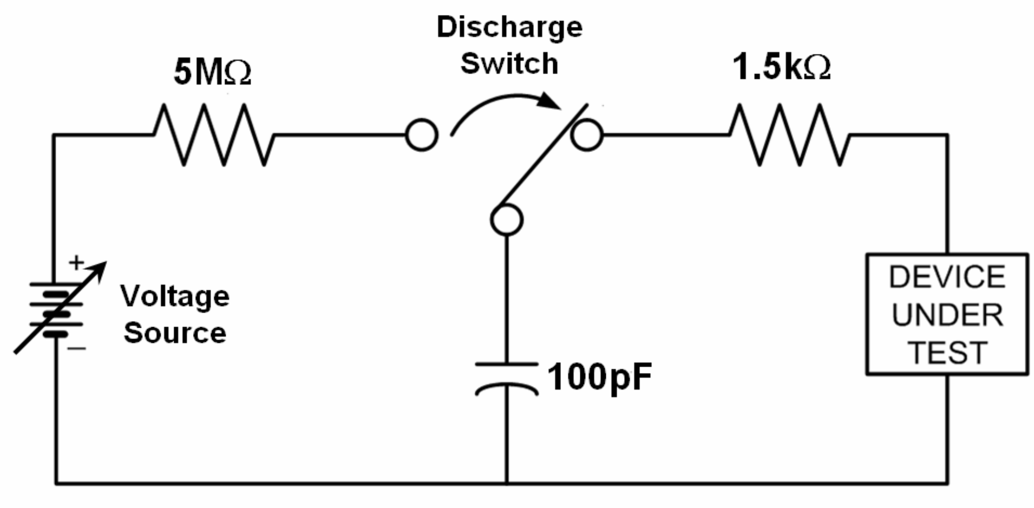


Fig. 1.12 Equivalent circuit of human body model (HBM) in the component-level ESD test. The charging capacitor (discharge resistor) is a smaller (larger) value of 100pF (1.5kΩ).

Chapter 2

Physical Mechanism and Device Simulation on Transient-Induced Latchup in CMOS ICs Under System-Level ESD Test

The physical mechanism of transient-induced latchup (TLU) in CMOS ICs under the system-level electrostatic discharge (ESD) test is clearly characterized by device simulation and experimental verification in time domain. For TLU characterization, an underdamped sinusoidal voltage stimulus has been clarified as the realistic TLU-triggering stimulus under the system-level ESD test. The specific “sweep-back” current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. All the simulation results on TLU have been practically verified in silicon with test chips fabricated by 0.25-μm CMOS technology.

2.1. Background

Transient-induced latchup (TLU) will increasingly be a primary reliability issue in CMOS IC products [17]-[25]. Recently, the test standard to verify the immunity of TLU on CMOS ICs has been announced [27]. This TLU tendency is caused by several reasons. First, there are much more complicated implementations of integrated circuits, such as mix-signal, multiple power supplies, RF, SOC, etc. The environment where these CMOS devices locate will suffer from considerable noises coming from both interior and exterior of CMOS ICs. Thus, such transient stimuli, those unpredictably exist on power, ground, or I/O pins of ICs, certainly induce TLU much more easily than before. Second, more and more ICs, unfortunately, are rather susceptible to TLU under a strict-demanded system-level ESD test [32]. Third, aggressive scaling of both device feature size, as well as the clearance between PMOS and NMOS devices, leads the inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs to exhibit a rather worse latchup immunity. The occurrence of latchup could still happen, even though the power supply voltage is reduced with the scaling rule of CMOS ICs. The latchup triggering current doesn’t prominently increase with the scaling rule of CMOS ICs while the power supply voltage keeps decreasing [9].

To investigate the physical mechanism of TLU under the system-level ESD test, the most significant part is to clarify the TLU-triggering stimulus at first. So far, several TLU-triggering stimuli have been found to probably trigger on TLU [3]-[6], [20], [21], [27]. The first developed TLU-triggering stimulus is to consider the power-on situation when power supply voltage ramps up from 0V to its normal operating voltage during the power-on transition [3], [4]. Once the rise time (ramp rate) of the power supply voltage during the power-on transition is short (fast) enough, latchup will probably be triggered on by the transient displacement current that flows through the parasitic well/substrate resistance of CMOS ICs. However, this situation only interpreted the occurrence of TLU during the initial power-on transition, but cannot reflect most TLU during the normal circuit operation. The second developed TLU-triggering stimulus is to utilize a single-positive (single-negative) voltage pulse applying on the PMOS (NMOS) drain terminal of CMOS ICs [5], [6]. Such single-positive (single-negative) voltage pulse is used to generate the transient overshooting (undershooting) noise on the output nodes of CMOS logic gates to simulate the dynamically switching operations. Thus, TLU could be triggered on due to the instantaneous forward-biased emitter/base junction current of the parasitic PNP (or NPN) bipolar junction transistor (BJT). However, TLU issue still exists even if CMOS ICs are operated in a DC steady state without dynamically switching under the system-level ESD test. Recently, a single-positive current pulse [20] applying to the power pins of CMOS ICs is also used for TLU characterization. This TLU-triggering stimulus, however, doesn't reflect the real one under the system-level ESD test.

To clarify this issue, an underdamped sinusoidal voltage stimulus, which can be observed on all ICs within the equipment under test (EUT) under the system-level ESD test [35], [38], [39], is adopted in this chapter as the TLU-triggering stimulus for both TLU measurement and device simulation [28], [29]. With the clearly-defined TLU-triggering stimulus, the physical mechanism of TLU under the system-level ESD test can be well explained in time domain by device simulation. Finally, all the simulation results on TLU have been practically verified in silicon with test chips fabricated by 0.25-μm CMOS technology.

2.2. TLU under System-Level ESD Test

To evaluate the performance of electrical/electronic equipments when subjected to ESD events, performing the system-level ESD test for the electrical/electronic equipments is necessary. For example, a notebook under the system-level ESD test with direct contact-discharge test mode is shown in Fig. 2.1. An electrical/electronic product with CMOS ICs must sustain the ESD level of ±8kV (±15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of “level 4” in the system-level ESD test [32]. During such a system-level ESD test, electromagnetic interference (EMI) coming from the ESD will be coupled into the driver ICs of the liquid crystal display (LCD) panel. The inset figure in Fig. 2.1 depicts the typically measured ESD-generated voltage waveforms on the power pins of CMOS ICs, which locate within the equipment under test (EUT), under the system-level ESD test [35], [38], [39]. This ESD-generated transient voltage is quite large (with amplitude of several tens to hundreds volts) and fast (with period of several tens nanoseconds), which can randomly exist on power, ground, or I/O pins of the driver ICs to cause TLU failures.

To clarify this issue, the system-level ESD test with indirect contact-discharge test mode is shown in Fig. 2.2 [32]. When the ESD gun zaps to the horizontal coupling plane (HCP), EMI coming from the ESD will be coupled into all CMOS ICs inside the EUT. With ESD voltage of +1000V, the measured V_{DD} transient waveforms on one of the CMOS ICs (CMOS IC#A) inside the EUT are shown in Fig. 2.3. The transient peak voltage on V_{DD} is as large as ±70V in Fig. 2.4. Clearly, the V_{DD} with initial DC voltage of +2.5V will become an underdamped sine-wave-like voltage due to the disturbance of the ESD energy. Once the ESD voltage keeps increasing, TLU can be initiated and results in malfunction or damage of the CMOS IC inside the EUT. For example, with ESD voltage of +2000V, the measured V_{DD}, I_{DD}, and V_{OUT} transient waveforms on CMOS IC#A are shown in Fig. 2.4. The transient peak voltage on V_{DD} is greater than ±100V, during such system-level ESD test. TLU occurs with instantaneously increasing I_{DD}, so that V_{OUT} (100MHz voltage clock) will fail to function correctly (pulled down to 0V). Thus, it can be clarified that the underdamped sinusoidal voltage existing on power (ground) line of the CMOS ICs is the major cause to initiate TLU during the system-level ESD test.

2.3. Test Structure

The SCR structure is used as the test structure for TLU measurements because the occurrence of latchup is due to the inherent SCR of two cross-coupled BJTs, parasitic vertical PNP and lateral NPN BJTs, in bulk CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 2.5(a) and 2.5(b), respectively. The geometrical parameters such as D, S, and W represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. In CMOS ICs, the P^+ anode (source of PMOS) and the N^+ well contact are connected to V_{DD}, whereas the N^+ cathode (source of NMOS) and the P^+ substrate contact are connected to ground. Once latchup occurs inside the SCR structure, huge current will be generated through a mechanism of positive-feedback regeneration [15], [40]. As a result, the huge current will conduct through a low-impedance path from V_{DD} to ground, and further probably burn out the chip due to excess heat.

Different values of geometrical parameters such as D, S, and W in Figs. 2.5(a) and 2.5(b) will certainly result in different TLU immunities of the SCR structures due to different latchup triggering (holding) voltages or currents. However, TLU physical mechanism should be the same and not related to the variations of geometrical parameters. As a result, to qualitatively analyze the physical mechanism of TLU through TLU measurements, a specified SCR structure with layout parameters of D=6.7µm, S=1.2µm, and W=22.5µm fabricated in 0.25-µm CMOS technology is used for all TLU measurements in this chapter. Because the parasitic SCR existing in the core circuitry of CMOS ICs is most sensitive to TLU due to compact integration, the minimum anode-to-cathode spacing (S=1.2µm) according to foundry's design rule is used to consider the worst-case situation (most sensitive to TLU) encountered in the core circuitry of CMOS ICs.

To verify the relationship between the TLU measurement and device simulation, the specified SCR structure with the same geometrical parameters of D=6.7µm and S=1.2µm is used for all TLU device simulations in this chapter by the two-dimensional device simulation tool (MEDICI), as shown in Fig. 2.6. With the specified two-dimensional SCR structure, the boundary condition can be well defined to perform the numerical analysis of electrical characteristics such as electric potential, electric field, carrier concentration, 2-D current flow line, etc.

2.4. Measurement Setup

For the system-level ESD test, it can only judge whether the EUT passes the required criterion through its abnormal function (e.g. EUT shuts down). Nevertheless, it is hard to directly evaluate the TLU immunity of single IC inside the EUT. To solve this problem, a component-level TLU measurement setup with the following two advantages is used. First, it can easily evaluate the TLU immunity of single IC by the related measured voltage/current waveforms through oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise under the system-level ESD test. Fig. 2.7 depicts such a component-level TLU measurement setup [41], [42]. The SCR structure shown in Fig. 2.5 is used as the device under test (DUT) where the P^+ anode and the N^+ well contact are connected together to V_{DD}, but the N^+ cathode and the P^+ substrate contact are connected to ground. An electrostatic-discharge simulator is used as the TLU-triggering source, V_{Charge}, to produce an underdamped sinusoidal voltage stimulus. Through applying a positive (negative) V_{Charge}, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated just as that under the system-level ESD test for ESD gun with positive (negative) voltage [35]. For example, with V_{Charge} of +10V (-2V), Fig. 2.8(a) (2.8(b)) shows the measured V_{DD} waveform across the SCR structure. Clearly, the intended underdamped sinusoidal voltage can be produced to simulate the transient voltage on power pins of CMOS ICs under the system-level ESD test, no matter which polarity (positive or negative) the ESD voltage is. Because a large discharge resistance will result in a large damping factor of the intended underdamped sinusoidal voltage [41], there is no discharge resistance (0Ω) between the relay and the V_{DD} node, as shown in Fig. 2.7. As a result, the intended underdamped sinusoidal voltage can be produced, but not the unwanted overdamped voltage waveform due to a large discharge resistance [41]. In addition, a charged capacitance of 200pF is used to store charges offered by the TLU-triggering source, V_{Charge}, and then these stored charges are discharged to DUT through the relay. Because the charged capacitance will affect the damping frequency of the underdamped sinusoidal voltage, it should be properly selected to achieve the reasonable damping frequency as that under the system-level ESD test. For example, the damping frequency (~10MHz) observed in Figs. 2.8(a) and 2.8(b) is slightly smaller than that under the system-level ESD test (~20MHz) [35], therefore indicating that this measurement setup is reasonable for TLU characterization. Moreover, a small current-limiting resistance (5Ω) is recommended to protect the DUT from electrical-over-stress (EOS) damage during a high-current (low-impedance) latchup state.

2.5. Device Simulation for TLU

A two-dimensional device simulation tool (MEDICI) is used to investigate the physical mechanism of TLU in time domain under the system-level ESD test. In this two-dimensional device simulation tool, a specific time-dependent voltage source given by

$$V_{DD}(t)=V_0+V_P\cdot\exp\left(-(t-t_d)D_{Factor}\right)\cdot\sin\left(2\pi D_{Freq}(t-t_d)\right). \qquad (1)$$

is used to apply an underdamped sinusoidal voltage on V_{DD} of the already defined SCR structure in Fig. 2.6. With the proper parameters such as initial voltage V_0, applied voltage amplitude V_P, damping factor D_{Factor}, damping frequency D_{Freq}, and time delay t_d, the intended underdamped sinusoidal voltage can be constructed. In the following TLU simulation with positive or negative V_{Charge}, the same parameters such as V_0=2.5V, $D_{Factor}=2\times10^7 s^{-1}$, D_{Freq}=20MHz, and t_d=50ns are used in both positive and negative V_{Charge}, whereas the only difference is V_P=+14.6V for positive V_{Charge}, but -14.6V for negative V_{Charge}. In addition, the specified SCR structure with geometrical parameters of D=6.7μm and S=1.2μm is used for all TLU device simulations in this chapter.

2.5.1. Simulated Latchup DC I-V Characteristics

The simulated latchup DC *I-V* characteristic of the specified SCR structure is shown in Fig. 2.9. Once latchup occurs in the SCR structure, a low-impedance path will exist from V_{DD} to ground, resulting in huge current conducting through this low-impedance path. The inset figure in Fig. 2.9 shows that the DC latchup triggering voltage (current), V_{Trig} (I_{Trig}), is about 15.5V (0.24mA), while the DC latchup holding voltage (current), V_{Hold} (I_{Hold}), is about 1.25V (0.5mA). Clearly, under a latchup state, when the power supply voltage, V_{DD}, keeps at its normal circuit operating voltage (+2.5V), the total power supply current, I_{DD}, flowing into both anode and well contact is about 150mA. This will offer a vital evidence to verify whether TLU certainly occurs in time domain through device simulation.

2.5.2. TLU Simulation with Negative V_{Charge}

With a negative V_{Charge}, the simulated V_{DD} and I_{DD} transient responses on the SCR structure are shown in Fig. 2.10. This can be divided into several parts for detailed discussions in time domain. First, during the period of 0ns≤t<50ns, the SCR operates in the blocking condition and V_{DD} is fixed at its normal operating voltage, +2.5V. Within this duration, the N-well/P-substrate junction is at a normal reverse-biased state, and I_{DD} only comes from the negligible leakage current in the reverse junction. Second, during the period of 50ns≤t≤62.5ns, V_{DD} begins to decrease rapidly from +2.5V at t=50ns, and will eventually reach the negative peak voltage, -V_{peak} (-8V), at t=62.5ns. Within this duration, the

N-well/P-substrate junction gradually becomes slightly reverse biased when V_{DD} decreases from +2.5V to 0V, and even becomes forward biased when V_{DD} drops below 0V. Thus, at t=62.5ns, the largest forward-biased N-well/P-substrate junction can generate the forward peak current, $-I_{peak}$ (~20mA). Third, during the period of $62.5\text{ns}<t\leq 75\text{ns}$, when V_{DD} increases from $-V_{peak}$ to its normal operating voltage, +2.5V, the N-well/P-substrate junction will rapidly change from the forward-biased state to its original reverse-biased state. Meanwhile, inside the N-well (P-substrate) region, large number of stored minority holes (electrons) offered by the forward peak current at t=62.5ns, will be instantaneously "swept-back" to the P-substrate (N-well) region where they originally come from. Thus, such "sweep-back" current, I_{Sb}, will produce a localized voltage drop while flowing through the parasitic P-substrate or N-well resistance. Once this localized voltage drop approaches to some critical value, the emitter-base junction of either vertical PNP or lateral NPN BJT in the SCR structure will be forward biased to further trigger on latchup. This can be further illustrated by the simulated transient responses of both anode and well contact current, as shown in Fig. 2.11. It clearly proves where these stored minority carriers, Q_{Stored}, come from and when they will be "swept-back" to cause TLU. For example, the gradually-enhanced forward-biased N-well/P-substrate junction will lead the gradually-increasing well contact current during the period of $50\text{ns}\leq t\leq 62.5\text{ns}$. Meanwhile, anode current is the negligible junction-leakage current due to an almost zero bias across the P^+-anode/N-well junction. Afterwards, during the period of $62.5\text{ns}<t\leq 75\text{ns}$, the forward well contact current will gradually decrease when V_{DD} increases from $-V_{peak}$ to +2.5V, indicating that the stored minority electrons (holes) are swept-back to the N-well (P-substrate) region where they originally come from. As a result, once the V_{DD} returns to, and even above, +2.5V ($75\text{ns}<t\leq 87.5\text{ns}$), latctup will be triggered on and huge anode current will conduct through the pnpn latchup path of the SCR structure. Meanwhile, the well contact current, however, is much smaller than the anode current because the well contact current is only the small base current of the parasitic vertical PNP BJT in the SCR structure.

In real CMOS ICs, when a low-impedance latchup state appears, V_{DD} may be pulled down to about the DC latchup holding voltage. This phenomenon is caused by two reasons. One is a finite current-supply ability of the system power supply, and the other is the inevitable parasitic series resistance existing between the V_{DD} node and the system power supply. In device simulation, however, when TLU occurs during the period of $75\text{ns}<t\leq 100\text{ns}$ shown in Figs. 2.10 and 2.11, V_{DD} was not immediately pulled down to the DC latchup

holding voltage. Instead, V_{DD} keeps at the given underdamped sinusoidal voltage. This fact results from the native limitation of device simulation tool for transient analysis in time domain. However, TLU is sure to occur because huge I_{DD} (150mA, refer to Figs. 2.10, and 2.11) can be found when V_{DD} finally returns to its normal operating voltage, +2.5V. More importantly, it is consistent with the simulated latchup DC I-V characteristics that I_{DD} is 150mA when V_{DD} keeps at its normal operating voltage, +2.5V, under a latchup state in Fig. 2.9.

To further judge whether TLU indeed occurs, Fig. 2.12 shows the corresponding simulated two-dimensional current flow lines with respect to various transient timing points with a negative V_{Charge}. Clearly, large forward well (substrate) contact current appears when N-well/P-substrate junction is forward-biased (timing points A, B, and F). Once the N-well/P-substrate junction quickly changes from the forward-biased state to its original reverse-biased state, TLU will be triggered on due to large enough I_{Sb} (timing points C-E, G, and H).

2.5.3. TLU Simulation with Positive V_{Charge}

With a positive V_{Charge}, Fig. 2.13 shows the simulated V_{DD} and I_{DD} transient responses on the SCR structure. During the period of $50\text{ns} \leq t \leq 62.5\text{ns}$, unlike the V_{DD} waveform with a negative V_{Charge} shown in Fig. 2.10 where V_{DD} begins decreasing rapidly at t=50ns, V_{DD} starts to increase at t=50ns and eventually reaches a positive peak voltage at t=62.5ns. Within this duration, the N-well/P-substrate junction is always reverse biased, and thus only transient displacement current caused by N-well/P-substrate junction can be found within the SCR. Such displacement current will not cause TLU unless the frequency (amplitude) of V_{DD} is large enough to induce large enough displacement current [3], [4]. Afterwards, V_{DD} decreases from its positive peak voltage, at t=62.5ns, to its negative peak voltage, at t=87.5ns. Within this duration, N-well/P-substrate junction gradually changes from the reverse-biased state to the forward-biased state, while more and more minority electrons (holes) are injected into the P-substrate (N-well) region. Once these Q_{Stored} are subsequently ($87.5\text{ns} \leq t \leq 100\text{ns}$) swept back to N-well (P-substrate) regions where they originally come from, TLU will be triggered on. As a result, I_{DD} will considerably increase during the period of $100\text{ns} \leq t \leq 112.5\text{ns}$. Obviously, TLU is sure to occur because the huge I_{DD} (150mA, refer to Figs. 2.9 and 2.13) can be found when V_{DD} eventually returns to its normal operating voltage of +2.5V.

Fig. 2.14 shows the simulated two-dimensional current flow lines with respect to various transient timing points with a positive V_{Charge}. The N-well/P-substrate junction displacement current will not cause TLU (timing points A and B). However, large forward well (substrate) contact current will appear when N-well/P-substrate junction is forward-biased (timing points C and D), and then TLU will certainly be triggered on if I_{Sb} is large enough (timing points E-H).

2.5.4. More Realistic Case

In real situation under the system-level ESD test, the oscillatory resonance voltage can randomly occur at both V_{DD} and GND nodes [35], [38], [39], but not only at the V_{DD} node. With considerations of such a realistic situation, Fig. 2.15 shows the simulated V_{DD}, GND, and I_{DD} transient responses on the SCR structure. Obviously, once V_{DD}-to-GND voltage is negative enough ($87.5\text{ns} \leq t \leq 100\text{ns}$) to produce large enough I_{Sb} within the N-well/P-substrate junction, TLU can be easily triggered on afterwards when V_{DD}-to-GND voltage returns to a positive voltage ($100\text{ns} \leq t \leq 112.5\text{ns}$). Because the power and ground lines are widely distributed over the whole circuitry in a chip, such oscillatory resonance voltage can appear on some core circuitry. This fact implies that TLU can occur within the core circuitry, but not only in I/O circuitry. Thus, unlike the quasi-static latchup issue [26] which primarily concerns about latchup immunity on I/O circuitry, the latchup prevention skills such as layout optimization with additional guard rings [43], other specific advanced process technologies, or even latchup self-stop circuit [44] may be necessary for the core circuitry to prevent TLU in CMOS ICs.

2.6. Experimental Results for TLU

The component-level TLU measurement setup in Fig. 2.7 is used to perform the TLU test. With both positive and negative V_{Charge}, the measured V_{DD} (I_{DD}) transient response will be recorded through the voltage (current) probe to display on the oscilloscope. This will clearly indicate whether the TLU occurs (I_{DD} significantly increases) when the absolute value of positive or negative V_{Charge} gradually increases from 0V during the TLU test. More importantly, this will provide useful information for the comparisons between the TLU measurement and the device simulation. In addition, the specified SCR structure with layout parameters of D=6.7μm, S=1.2μm, and W=22.5μm fabricated in 0.25-μm CMOS technology is used for all the TLU measurements in this chapter.

2.6.1. Measured Latchup DC I-V Characteristics

The measured latchup DC *I-V* characteristic for the fabricated SCR structure is shown in Fig. 2.16. The inset figure in Fig. 2.16 indicates the DC latchup trigger voltage (current), V_{Trig} (I_{Trig}), is about 19.5V (2mA), while the DC latchup holding voltage (holding current), V_{Hold} (I_{Hold}), is about 1V (9.5mA). Through comparing these measured DC latchup parameters with the simulated ones in Fig. 2.9, there is no large difference between the measured and the simulated DC latchup parameters. Thus, this non-calibrated device simulation tool is capable of performing the reasonable qualitative analysis to TLU.

2.6.2. TLU Measurement with Negative V_{Charge}

With a negative V_{Charge} of -5V, the measured V_{DD} and I_{DD} transient waveforms on the SCR structure are shown in Fig. 2.17. Obviously, forward I_{DD} current appears due to the forward-biased N-well/P-substrate junction when V_{DD} initially decreases below 0V. Afterwards, I_{DD} will greatly increase while V_{DD} returns to above 0V, and therefore TLU does occur. As a result, both V_{DD} and I_{DD} waveforms are slightly oscillatory under a low-impedance (high-current) latchup state. Finally, V_{DD} will eventually be pulled down to about the DC latchup holding voltage (~1V) with the huge I_{DD} (~80mA) after this transition.

Through the comparisons between the experimental and the device simulation results in Figs. 2.10 and 2.17, the experimental results are consistent with the device simulation results in time domain. For example, TLU will be triggered on due to large enough I_{Sb} while V_{DD} increases from -V_{Peak} to its normal operating voltage of +2.5V. This can once again verify that the large number of Q_{Stored} can trigger on TLU while they are quickly swept back to the regions where they originally come from.

2.6.3. TLU Measurement with Positive V_{Charge}

With a positive V_{Charge} of +20V, the measured V_{DD} and I_{DD} transient waveforms on the SCR structure are shown in Fig. 2.18. V_{DD} begins to increase rapidly from the normal operating voltage (+2.5V) to a positive peak voltage of +17V. Meanwhile, the N-well/P-substrate junction is reversed biased, and thus only transient displacement current caused by the N-well/P-substrate junction can be founded within the SCR. Such junction displacement current is too small to initiate TLU because I_{DD} doesn't significantly increase when V_{DD} increases from the normal operating voltage (+2.5V) to the positive peak voltage of +17V. Afterwards, once large enough I_{Sb} is produced when V_{DD} increases from its negative peak voltage back to the normal operating voltage (+2.5V), TLU will be initiated with large-increasing I_{DD}. Moreover, both V_{DD} and I_{DD} waveforms are slightly oscillatory under a low-impedance (high-current) latchup state. Finally, V_{DD} will eventually be pulled down to about the DC latchup holding voltage (~1V) with the huge I_{DD} (~80mA) after this transition.

The physical mechanism of TLU under the system-level ESD test can be well proved once again by comparing the experimental results with the device simulation. As shown in Figs. 2.13 and 2.18, large enough I_{Sb} caused by the instantaneously forward-biased N-well/P-substrate junction can trigger on TLU more easily than the reverse junction displacement current does.

2.7. Discussion

It has been clarified that the sweep-back current, I_{Sb}, caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs is the major cause of TLU under the system-level ESD test. Based on a simple 1-D analytical model of I_{Sb} [28], [29], the dominant parameter to initiate TLU can be identified. In addition, the minimum magnitude of the applied voltage to initiate TLU under different damping frequencies can be determined by the device simulations. By combining these 2-D device simulation results and the 1-D model of I_{Sb}, the minimum I_{Sb} or the minimum number of the total stored minority carriers (Q_{Stored}) to initiate TLU can be also estimated. To further provide the evidence that I_{Sb} is the major cause of TLU, the transient responses on the minority carriers stored within SCR are calculated.

2.7.1. Dominant Parameter to Induce TLU

As shown in the inset figure of Fig. 2.19, with the assumption that the N-well/P-substrate junction is treated as an ideal 1-D diode with step junction profile, a simple 1-D analytical model of the averaged I_{Sb} ($\equiv I_{Ave}$) [28], [29] can be expressed as

$$I_{Ave} \equiv \frac{Q_{Stored}}{t_B - t_A}. \tag{2}$$

t_A (t_B) is the initial (final) timing point of a specific duration when I_{Sb} exists, as shown in Fig. 2.19. Q_{Stored} represents the total stored minority carriers (holes) causing I_{Sb} ($t_A \le t \le t_B$) inside the N-well region, which is given by

$$Q_{Stored} = q\frac{n_i^2}{N_D}L_P(1-e^{-\frac{X_{n'}-X_n}{L_P}})\left(e^{\frac{qV(t_A)}{kT}} - e^{\frac{qV(t_B)}{kT}}\right). \tag{3}$$

From (2) and (3), I_{Ave} can be further simplified as

$$I_{Ave} \equiv \frac{Q_{Stored}}{t_B - t_A} = \frac{Q_{Stored}}{\left(1/D_{Freq}\right)/4} = 4D_{Freq}q\frac{n_i^2}{N_D}L_P(1-e^{-\frac{X_{n'}-X_n}{L_P}})\left(e^{\frac{qV(t_A)}{kT}} - e^{\frac{qV(t_B)}{kT}}\right)$$

$$= Z \cdot D_{Freq} \cdot e^{\frac{qV(t_A)}{kT}}, (\because e^{\frac{qV(t_B)}{kT}} = e^{\frac{V(t_B)}{kT/q}} = e^{\frac{-2.5}{0.0259}} \cong 0) \qquad (4)$$

where

$$Z = 4q\frac{n_i^2}{N_D}L_P(1-e^{-\frac{X_{n'}-X_n}{L_P}}) \qquad (5)$$

is a constant and independent on damping frequency (D_{Freq}), applied voltage amplitude (V_P), and damping factor (D_{Factor}). By substituting $t_A=t_d+(1/D_{Freq})/4$ into (1), $V(t_A)$ can be expressed as

$$V\left(t_A\right) = V_0 + V_P \cdot \exp\left(-\left(t_A - t_d\right)D_{Factor}\right) \cdot \sin\left(2\pi D_{Freq}\left(t_A - t_d\right)\right)$$

$$= V_0 + V_P \cdot \exp\left(-\frac{D_{Factor}}{4D_{Freq}}\right). \qquad (6)$$

From (4) and (6), it can be obviously identified that D_{Freq} is dominant to I_{Ave} (i.e. dominant to induce TLU), because there is not only a proportional exponential relationship between D_{Freq} and $V(t_A)$ in (6), but also a multiplication factor "D_{Freq}" on I_{Ave} in (4).

2.7.2. Minimum Applied Voltage Amplitude to Initiate TLU

The minimum V_P to initiate TLU can be determined by the device simulation results. For the underdamped sinusoidal voltage with D_{Factor} of $1.5\text{x}10^6\text{s}^{-1}$, the simulated V_{P-} dependences on D_{Freq} are shown in Fig. 2.20. V_{P-} is defined as the minimum magnitude of the negative applied voltage to initiate TLU. Clearly, V_{P-} decreases with D_{Freq}. This can be demonstrated by (2) where the higher D_{Freq} (i.e. smaller t_B-t_A) can initiate TLU by a smaller V_{P-} (i.e. smaller Q_{Stored}), if the critical I_{Ave} to initiate TLU is fixed. Thus, the critical value of D_{Factor}, V_P, or D_{Freq} to initiate TLU isn't fixed but correlated with each other, because D_{Factor}, V_P, and D_{Freq} are all correlated with I_{Ave} (I_{Sb}) to determine the occurrence of TLU [45].

2.7.3. Minimum Q_{Stored} or I_{Sb} to Initiate TLU

By combining the 2-D device simulation results and the 1-D analytical model of I_{Ave}, the minimum I_{Ave} or Q_{Stored} to initiate TLU can be estimated. As shown in Fig. 2.20, for the underdamped sinusoidal voltage with D_{Factor} of 1.5x10^6s^{-1} and D_{Freq} of 10MHz, the minimum magnitude of the negative applied voltage (V_{P-}) to initiate TLU is 6V. With this trigger condition, it can be calculated from (1) that $V(t=t_A=t_d+(1/D_{Freq})/4=t_d+25ns)$=3.26V. However, it's improper to directly apply such a high $V(t_A)$ of 3.26V into (3) to obtain Q_{Stored}, because the forward-biased P-substrate/N-well junction current is dominated by the parasitic series resistance effect at a high current state ($t=t_A$). As a result, the $V(t_A)$ considering the parasitic series resistance effect of the P-substrate/N-well diode can be defined as $V(t_A)'$ and extracted from

$$I(t_A) = J_0 \times W_{Diode} \times e^{\frac{qV(t_A)'}{kT}}. \qquad (7)$$

W_{Diode} is the distance perpendicular to X direction of the ideal 1-D P-substrate/N-well diode, as shown in the inset figure of Fig. 2.19. With J_0 of about 10^{-19}A/μm^2 at T=300K, W_{Diode} of about 5μm (approximated from the 2-D SCR structure in Fig. 2.6), and $I(t_A)$ of 2.676x10^{-3}A/μm from the simulation result, $V(t_A)'$ of 0.95V can be calculated from (7). Thus, with N_D=10^{17}cm^{-3}, $L_p=(D_p\tau_p)^{0.5}\cong 30$μm at T=300K, $V(t=t_B)$=2.5V, and the assumption that the distance between the depletion region edge and the contacts of 1-D P-substrate/N-well diode is much larger than the minority carrier diffusion length (i.e. $X_{n'}-X_n>>L_p$), the minimum Q_{Stored} to initiate TLU of 2.57x10^{-11}C/μm^2 can be calculated from (3). With the known Q_{Stored} and $t_B-t_A=(1/D_{Freq})/4$=25ns, the minimum I_{Ave} to initiate TLU of 1.03x10^{-3}A/μm^2 can be calculated from (2).

2.7.4. Transient Responses on the Minority Carriers Stored within SCR

To further provide the evidence that I_{Sb} is the major cause of TLU, the transient responses on the minority carriers stored within SCR, $Q_{Stored}(t)$, can be estimated from (3) by using t to substitute for t_A. For the underdamped sinusoidal voltage with the same parameters (D_{Factor}, D_{Freq}, and V_P of 2×10^7s^{-1}, 20MHz, -14.6V, respectively) as those in the case with negative V_{Charge} of Figs. 2.10 and 2.11, the calculated transient responses of Q_{Stored} (hole) in the N-well region are shown in Fig. 2.21. Compared with the simulated TLU transient responses in Figs. 2.10 and 2.11, the minority carriers (holes) stored in the N-well region significantly increase with forward well contact current (50ns≤t≤62.5ns) when V_{DD} decreases from 2.5V to -V_{peak}. Afterwards, Q_{Stored} decreases because these minority holes are swept back to their original P-substrate region (62.5ns≤t≤75ns). As a result, TLU will be triggered on by these swept-back Q_{Stored}, so the anode current will significantly increase (75ns≤t≤87.5ns).

From Figs. 2.10, 2.11, and 2.21, the swept-back current I_{Sb} can be confirmed as the major cause of TLU during system-level ESD stress.

2.8. Conclusion

The underdamped sinusoidal voltage stimulus has been clarified as the realistic TLU-triggering stimulus under the system-level ESD test. With the aid of device simulation, the specific “sweep-back” current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. Through comparisons between device simulations and experimental measurements, TLU reliability issue may still exist in a qualified CMOS IC product through quasi-static latchup test. Thus, an efficient TLU measurement setup is needed to evaluate the TLU reliability of CMOS IC products. Because TLU reliability issue potentially exists within the whole circuitry of CMOS ICs, latchup prevention skills such as layout optimization, the specific advanced process technologies, or circuit technique may be necessary to improve TLU immunity for core circuitry. Through both the understanding of physical mechanism and the proposed simulation/verification methodology on TLU, the safe design/layout rules or circuit techniques in CMOS ICs can be developed against TLU events.

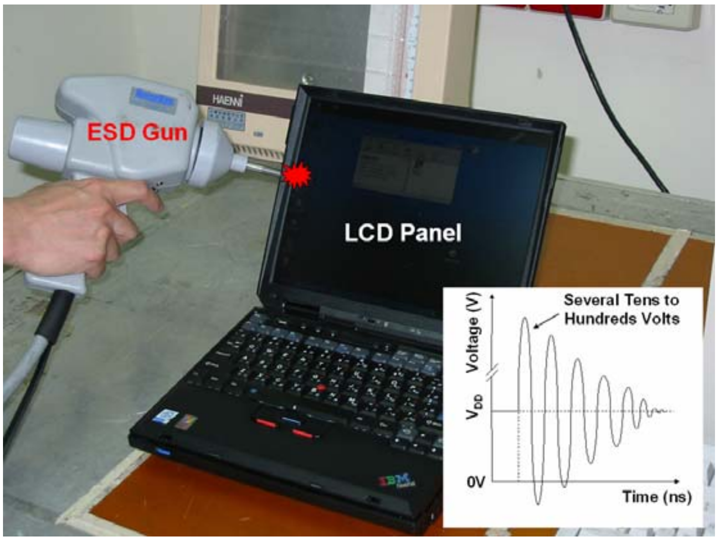


Fig. 2.1 System-level ESD test on a notebook with direct contact-discharge mode according to IEC 61000-4-2 international standard [32]. The inset figure depicts the typically measured waveforms of transient noise voltage on the power pins of CMOS ICs, which locate within the EUT, under the system-level ESD test [35], [38], [39].

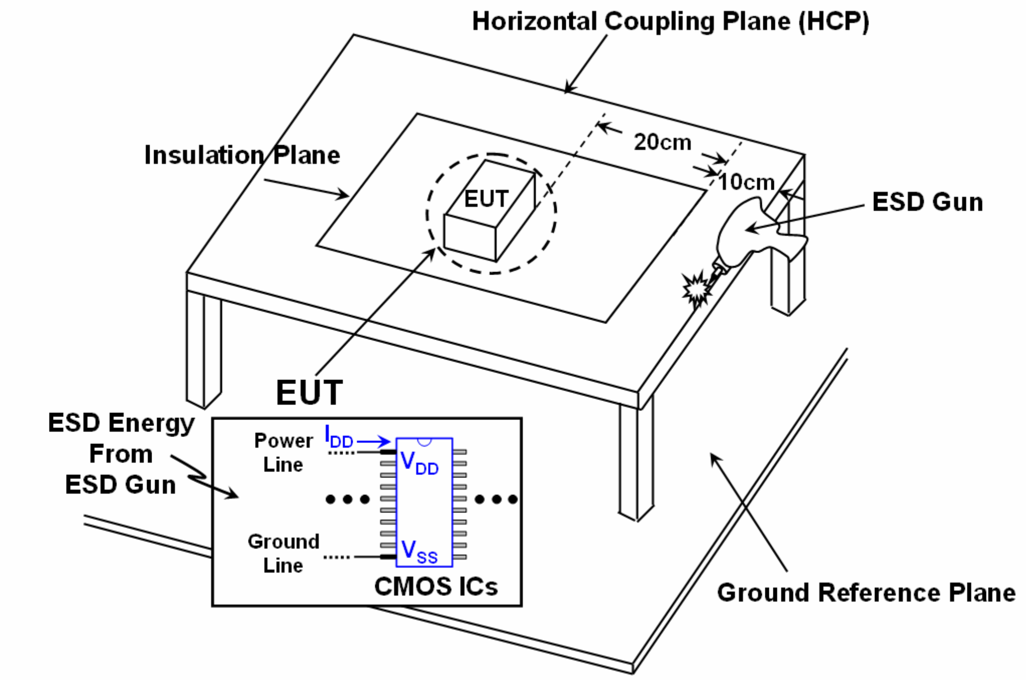


Fig. 2.2 Measurement setup of the system-level ESD test with indirect contact-discharge test mode [32]. The ESD gun zapping on the horizontal coupling plane (HCP) could cause TLU events on all the CMOS ICs inside the EUT.

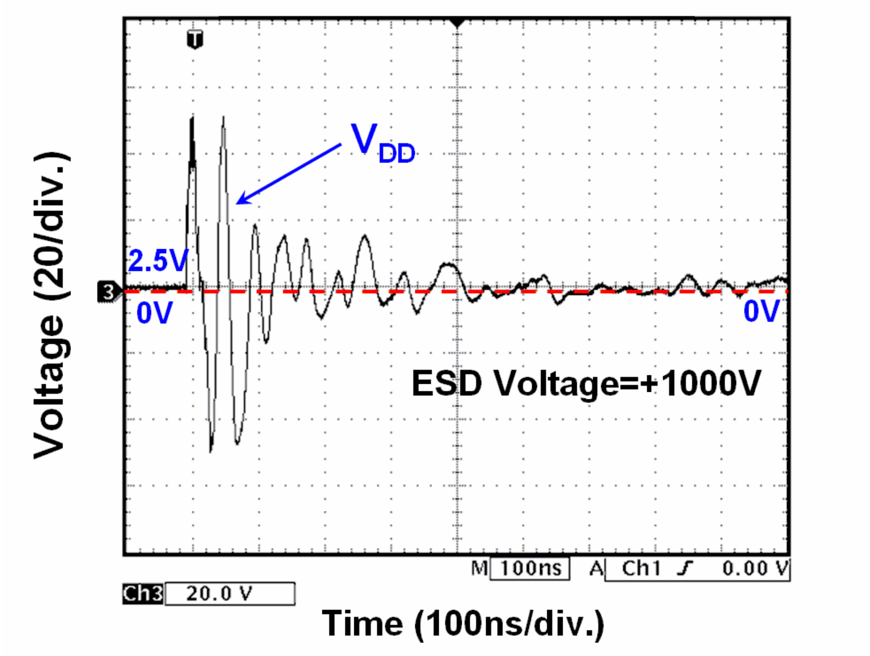


Fig. 2.3 For ESD gun with ESD voltage of +1000V zapping on the HCP, the measured V_{DD} transient waveform on one of the CMOS ICs (CMOS IC#A) inside the EUT.

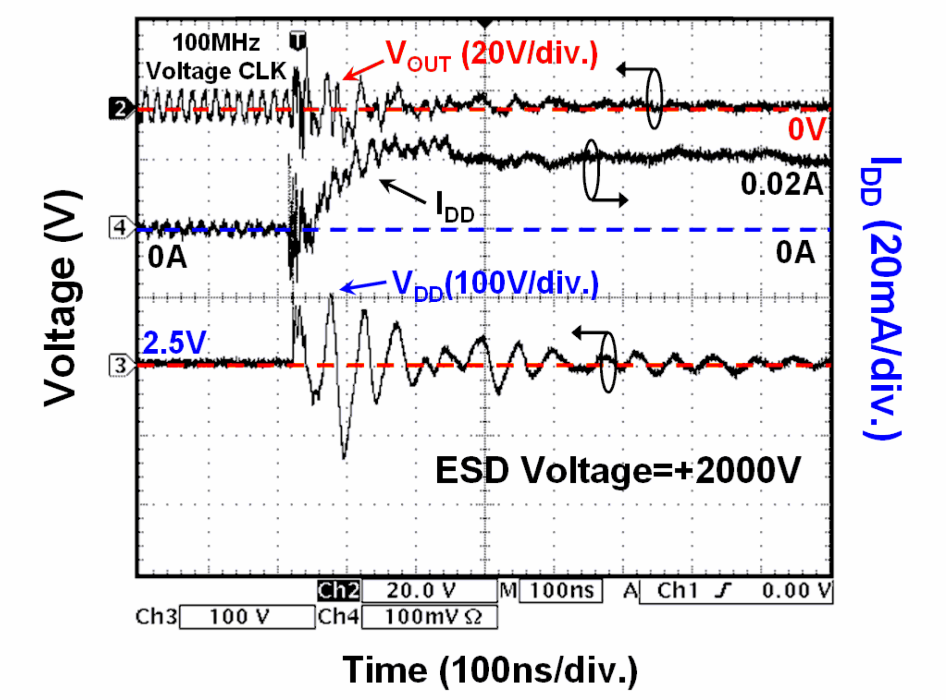


Fig. 2.4 For ESD gun with ESD voltage of +2000V zapping on the HCP, the measured V_{DD}, I_{DD}, and V_{OUT} transient waveforms on CMOS IC#A inside the EUT. TLU occurs during the system-level ESD test.

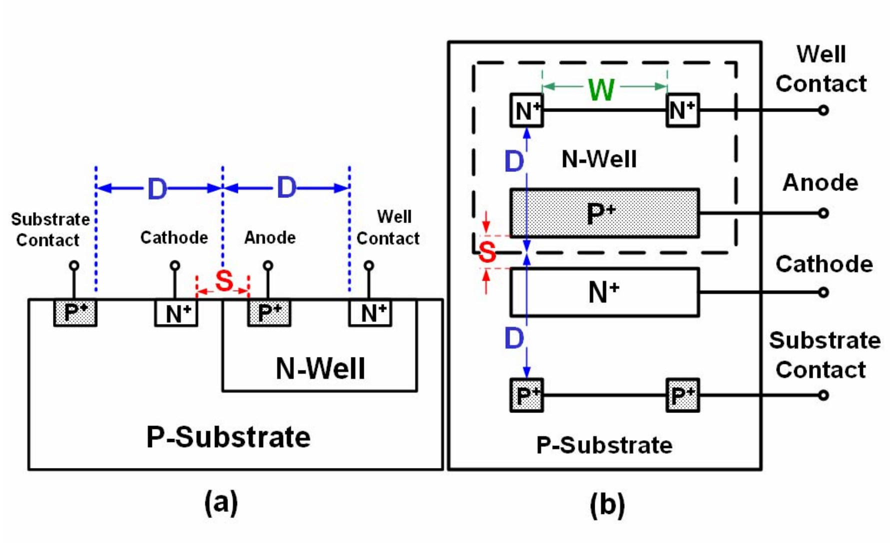


Fig. 2.5 (a) Device cross-sectional view, and (b) layout top view, of the SCR structure for TLU measurements. Geometrical parameters such as *D*, *S*, and *W* represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively.

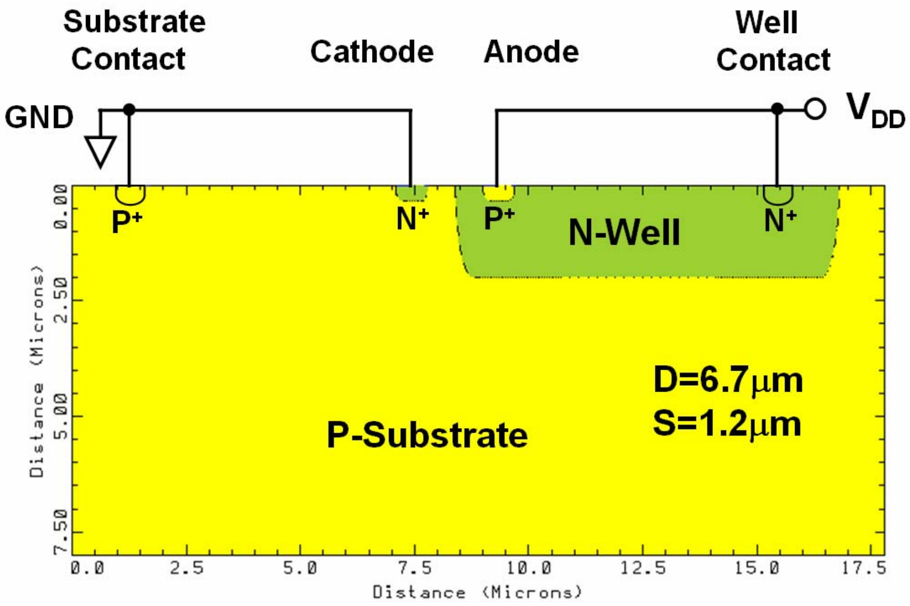


Fig. 2.6 The SCR structure used in a two-dimensional device simulation tool (MEDICI). The specified SCR structure with the geometrical parameters of *D*=6.7μm and *S*=1.2μm is used for all the TLU device simulations in this chapter.

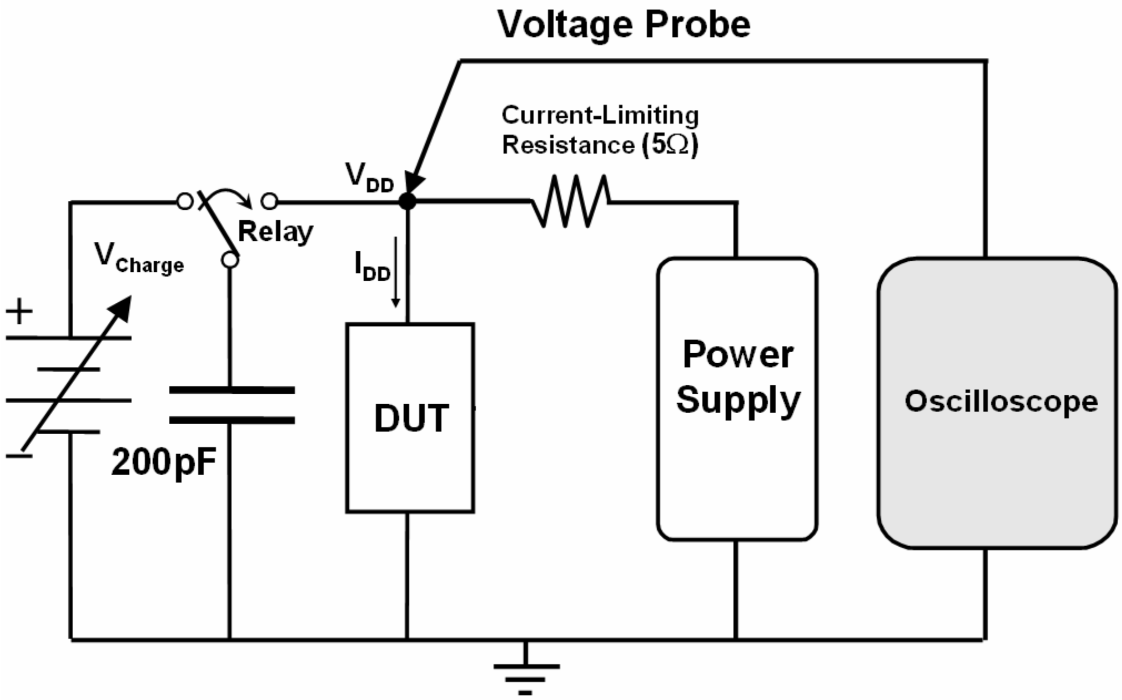
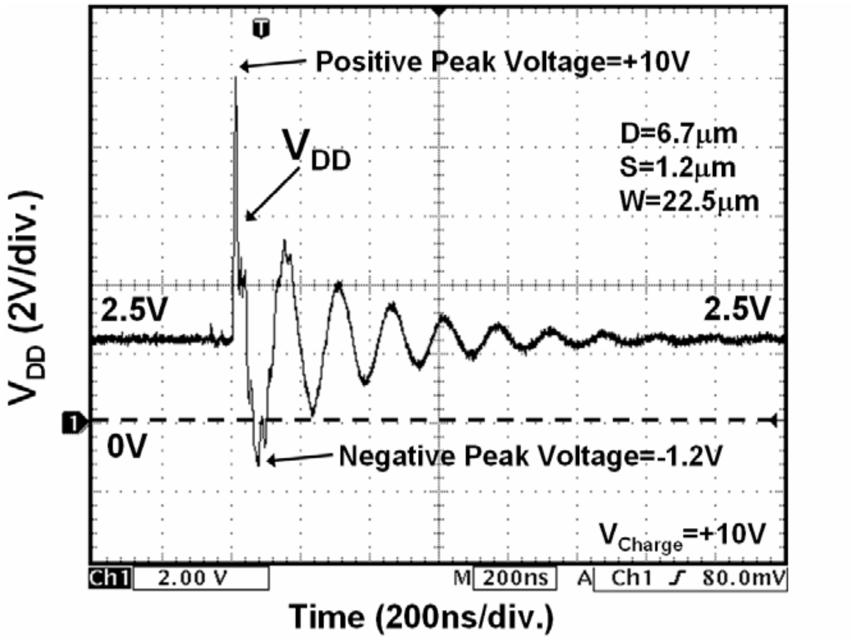
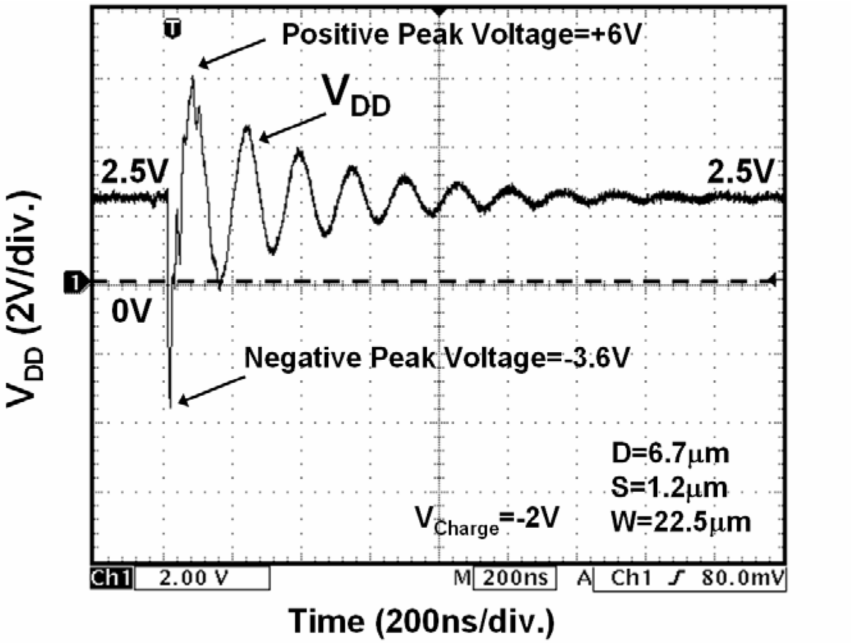


Fig. 2.7 A component-level TLU measurement setup [41], [42]. It can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise under the system-level ESD test.



(a)



(b)

Fig. 2.8 Measured V_{DD} waveform for the SCR structure with V_{Charge} of (a) +10V, and (b) -2V. Clearly, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated just as that under the system-level ESD test for ESD gun with positive (negative) voltage [35].

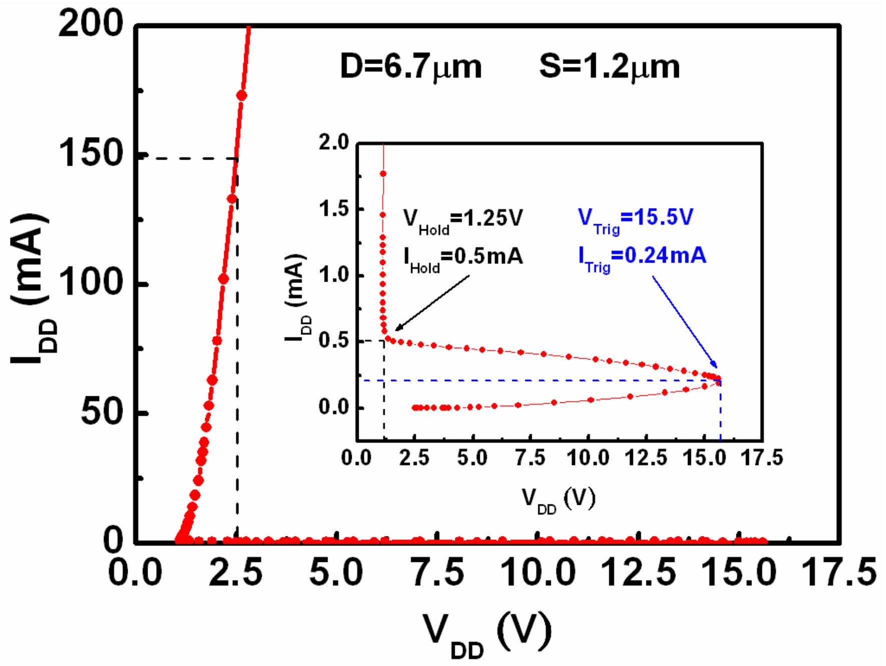


Fig. 2.9 Simulated latchup DC *I-V* characteristic for the SCR structure. Under a latchup state, the fact that I_{DD} is about 150mA when V_{DD} keeps at its normal operating voltage (+2.5V) will offer a vital evidence to prove whether TLU certainly occurs in time domain through device simulation.

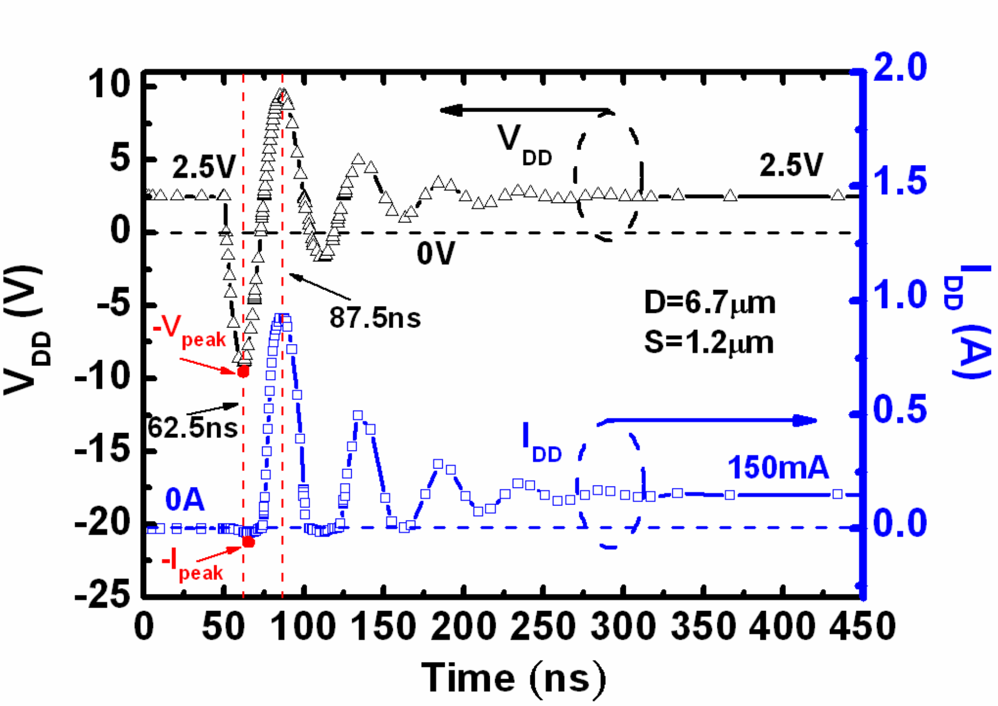


Fig. 2.10 Simulated V_{DD} and I_{DD} transient responses for TLU with a negative V_{Charge}. During the period of 62.5ns≤t≤87.5ns, the "sweep-back" current, I_{Sb}, will be produced to initiate TLU (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage of +2.5V.

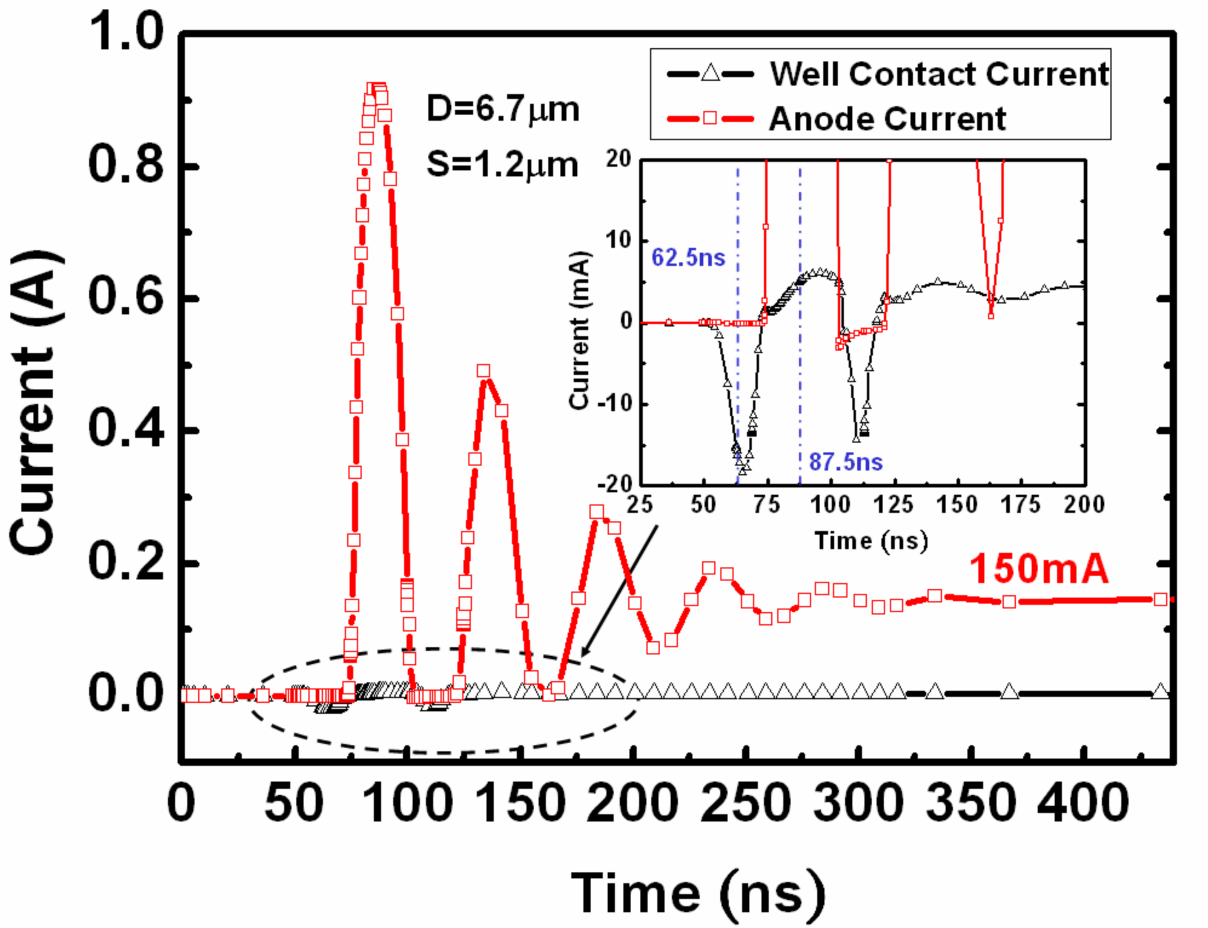


Fig. 2.11 Simulated transient responses of both anode current and well contact current for TLU with a negative V_{Charge}. During the period of 62.5ns≤t≤87.5ns, latctup will be triggered on by I_{Sb}. Meanwhile, huge anode current will conduct through the pnpn latchup path of the SCR structure.

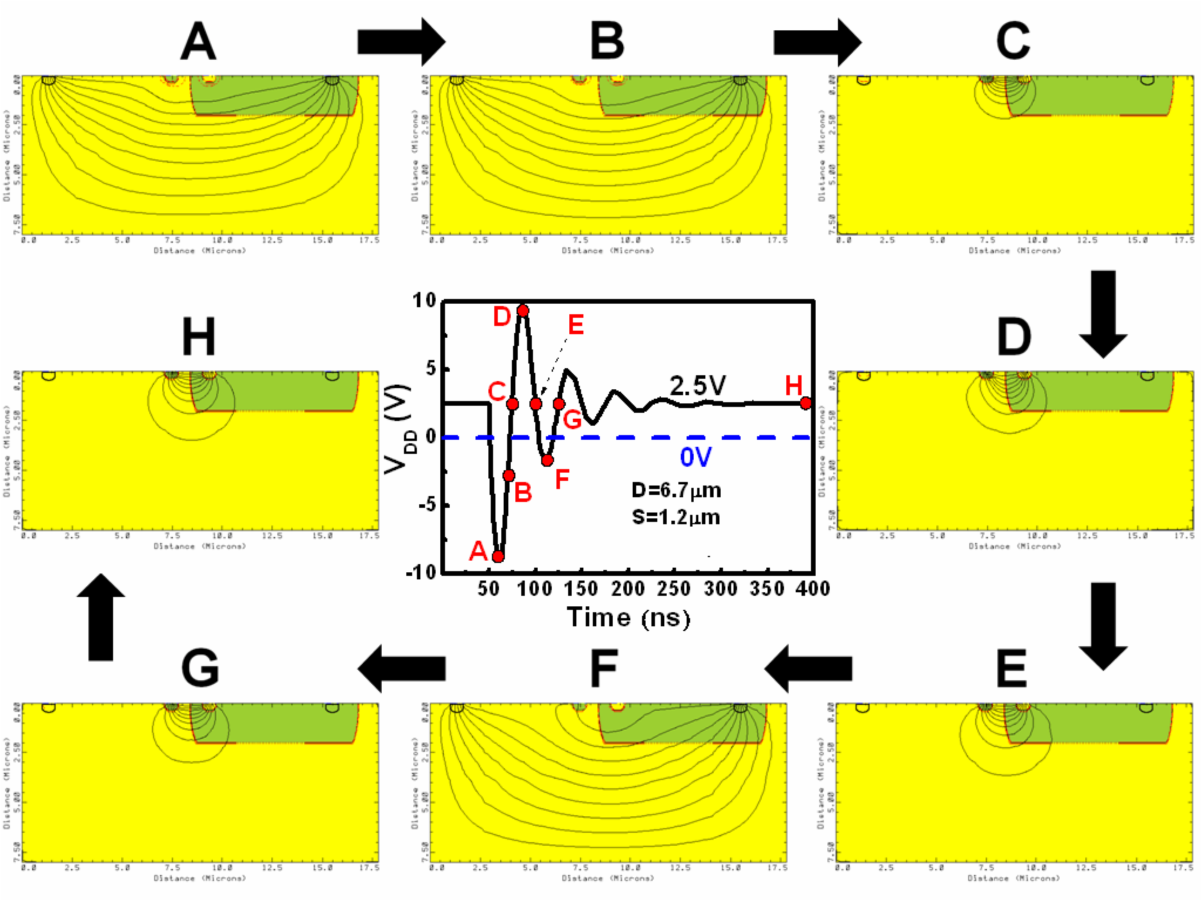


Fig. 2.12 Simulated 2-D current flow lines with respect to various transient timing points for TLU with a negative V_{Charge}. Forward well (substrate) contact current appears when N-well/P-substrate junction is forward-biased (timing points A, B, and F), and TLU will be triggered on due to large enough I_{Sb} (timing points C-E, G, and H).

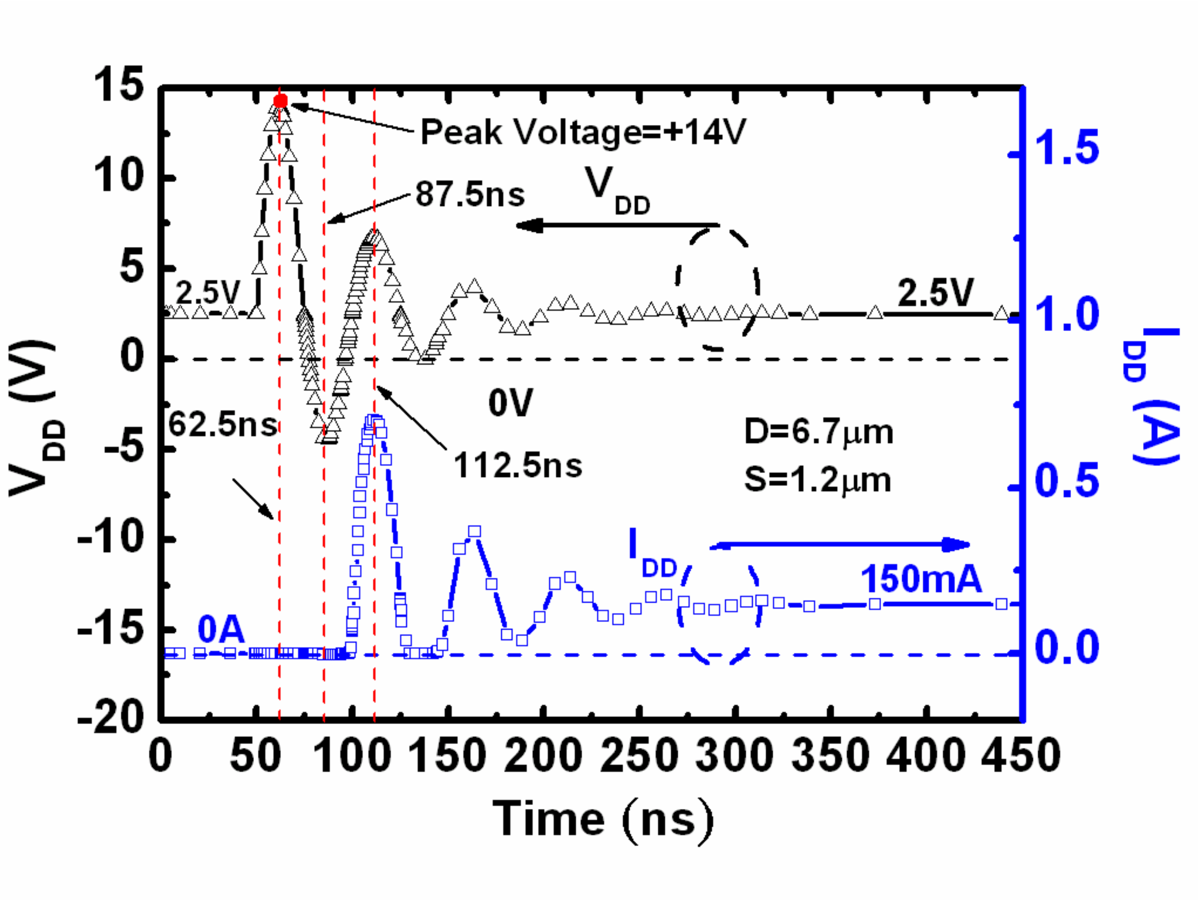


Fig. 2.13 Simulated V_{DD} and I_{DD} transient responses for TLU with a positive V_{Charge}. During the period of 50ns≤t≤75ns, TLU will not be triggered on by the N-well/P-substrate junction displacement current. Afterwards, during the period of 87.5ns≤t≤112.5ns, I_{Sb} will be produced to initiate TLU (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage, +2.5V.

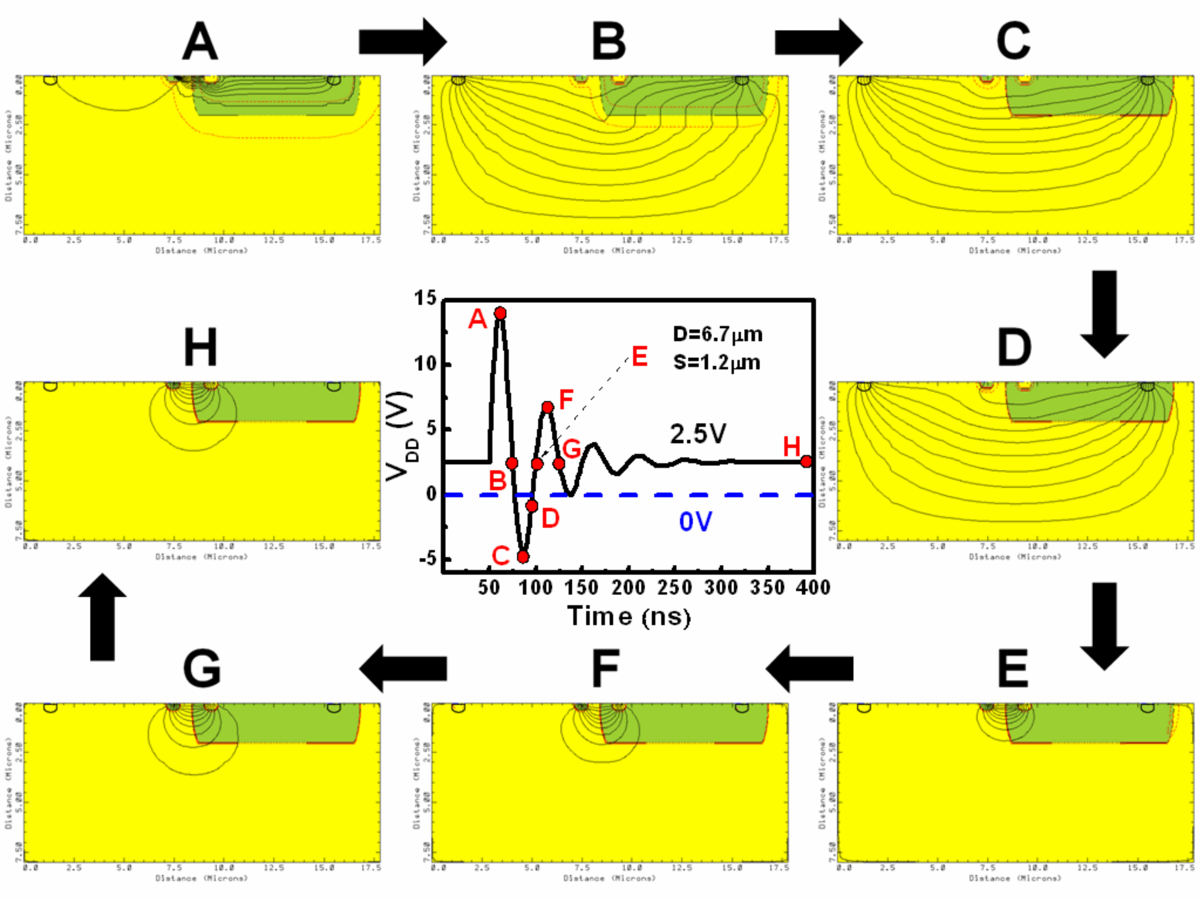


Fig. 2.14 Simulated 2-D current flow lines with respect to various transient timing points for TLU with a positive V_{Charge}. The N-well/P-substrate junction displacement current will not cause TLU (timing points A and B) until large enough I_{Sb} is produced (timing points E-H).

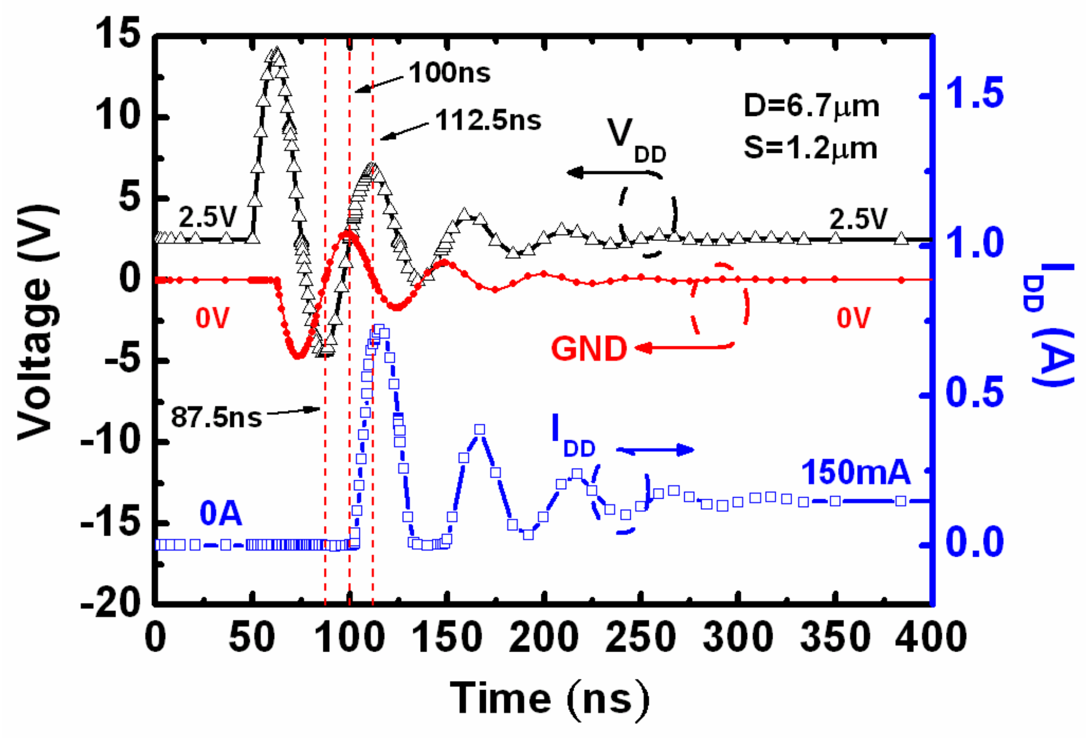


Fig. 2.15 Simulated V_{DD}, GND, and I_{DD} transient responses for TLU under a more realistic situation. V_{DD} and GND can be disturbed simultaneously by EMI under a system-level ESD test [35], [38], [39]. Once V_{DD}-to-GND voltage is negative enough ($87.5\text{ns} \le t \le 100\text{ns}$) to produce large enough I_{Sb}, afterwards TLU could be easily triggered on when V_{DD}-to-GND voltage returns to a positive voltage ($100\text{ns} \le t \le 112.5\text{ns}$).

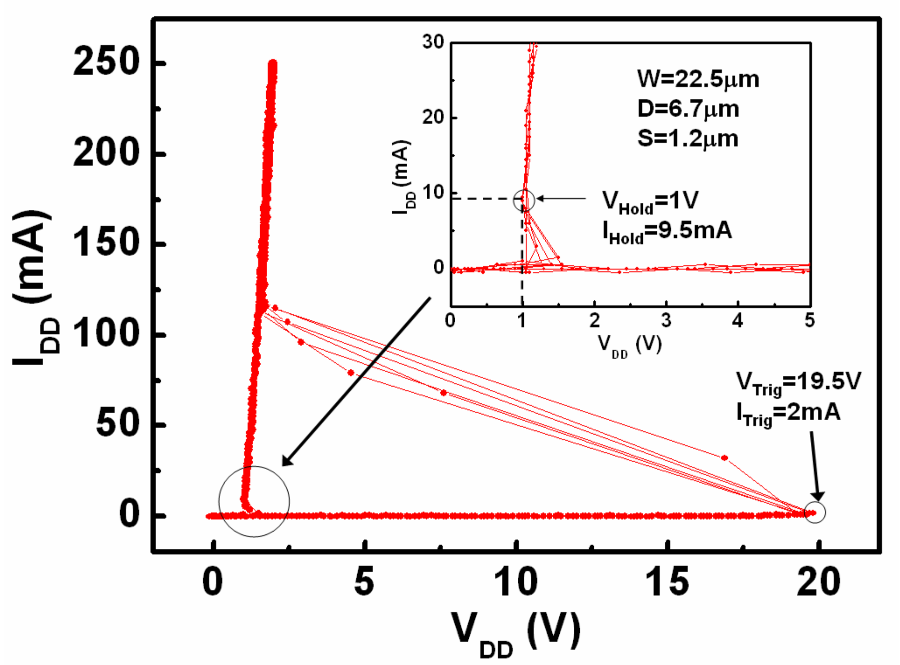


Fig. 2.16 Measured latchup DC *I*-*V* characteristic for the SCR structure.

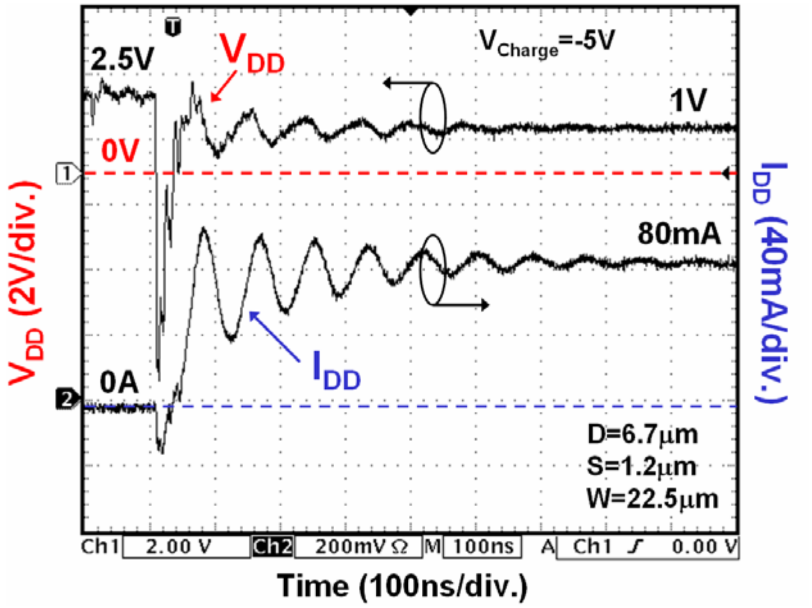


Fig. 2.17 Measured V_{DD} and I_{DD} transient waveforms from the TLU test with a negative V_{Charge} of -5V. It is consistent with the device simulation results in Fig. 2.10 that TLU will be triggered on (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage, +2.5V.

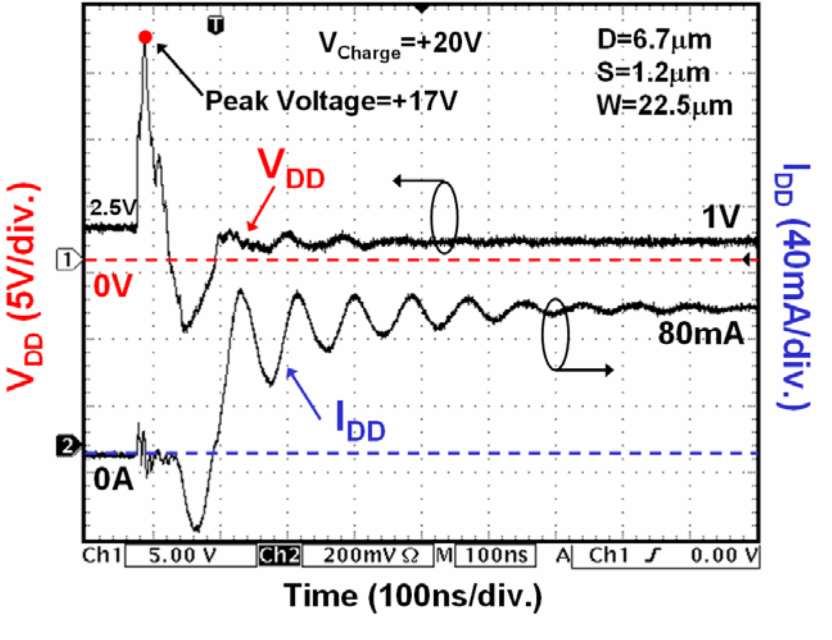


Fig. 2.18 Measured V_{DD} and I_{DD} transient waveforms from the TLU test with a positive V_{Charge} of +20V. It is consistent with the device simulation results in Fig. 2.13 that TLU will not be initially (V_{DD}>0V) triggered on by the N-well/P-substrate junction displacement current until large enough I_{Sb} is produced when V_{DD} increases from its negative peak voltage to the normal operating voltage, +2.5V.

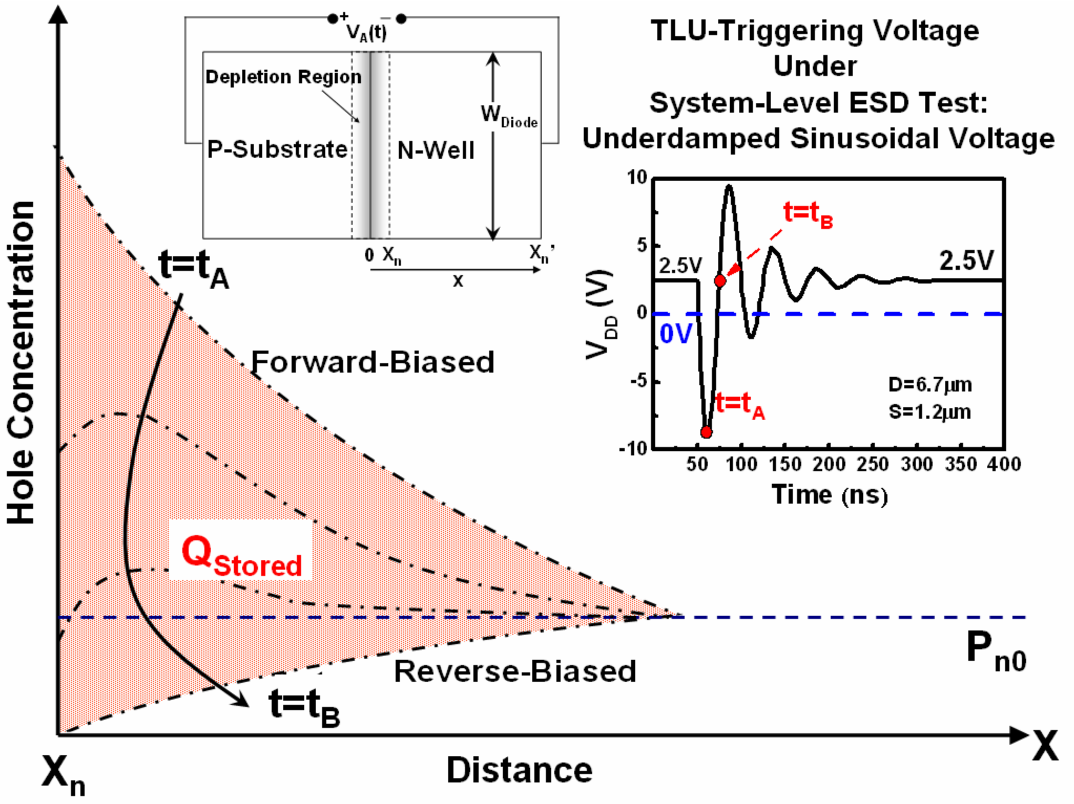


Fig. 2.19 Total stored minority carriers, Q_{Stored}, causing I_{Sb} ($t_A \le t \le t_B$) inside the N-well region. The inset figure is an ideal 1-D diode used for deriving the 1-D analytical model of the averaged I_{Sb} ($\equiv I_{Ave}$) [28], [29].

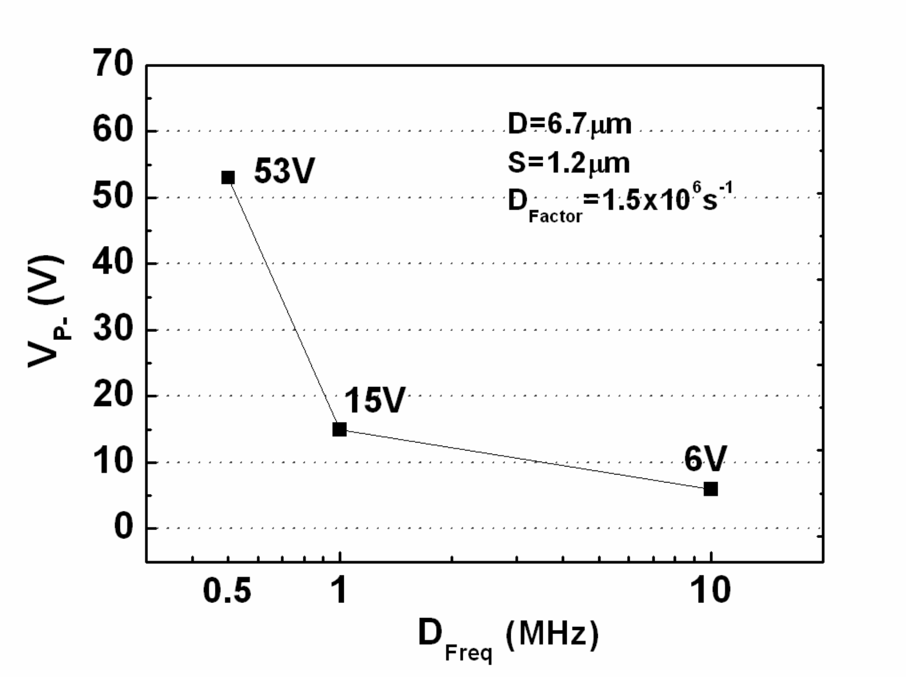


Fig. 2.20 Simulated V_{P-} dependences on damping frequency (D_{Freq}). V_{P-} is defined as the minimum magnitude of the negative applied voltage to initiate TLU.

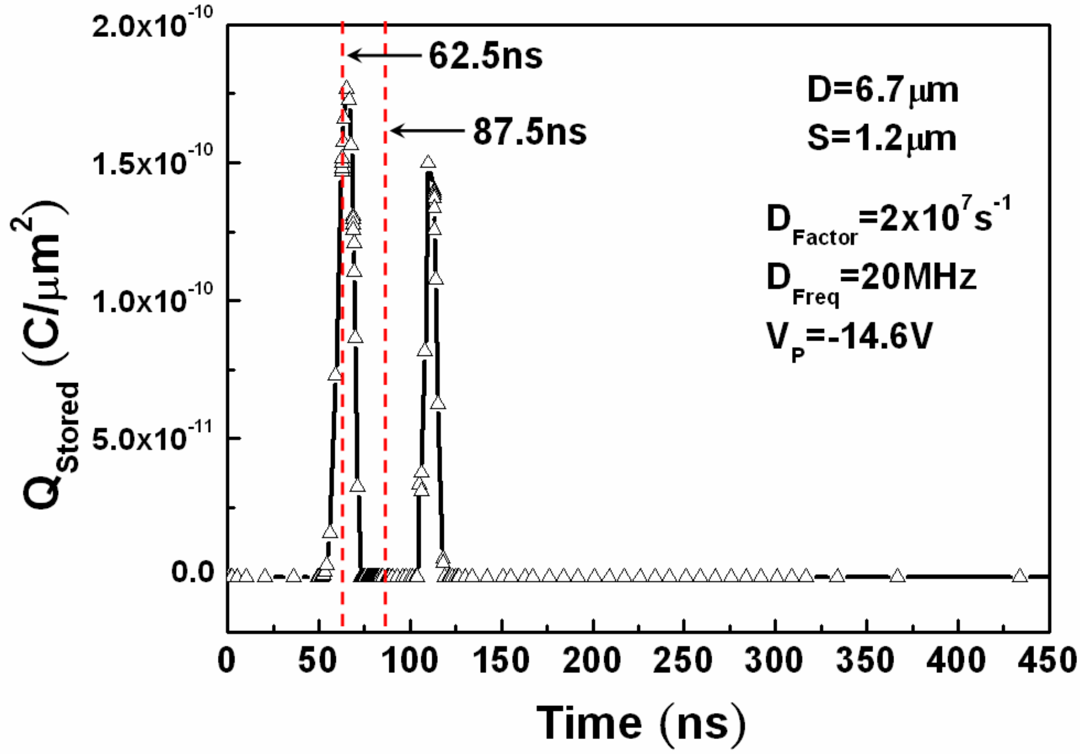


Fig. 2.21 Calculated transient responses of Q_{Stored} (hole) in the N-well region. The underdamped sinusoidal voltage has the same parameters as those used in the negative V_{Charge} case of Figs. 2.10 and 2.11 (D_{Factor}, D_{Freq}, and V_P of $2\times10^7 s^{-1}$, 20MHz, and -14.6V, respectively).

Chapter 3

Component-Level Measurement for Transient-Induced Latchup in CMOS ICs under System-Level ESD Considerations

To accurately evaluate the immunity of CMOS ICs against transient-induced latchup (TLU) under the system-level electrostatic discharge (ESD) test for electromagnetic compatibility (EMC) regulation, an efficient component-level TLU measurement setup with bipolar (underdamped sinusoidal) trigger is developed in this chapter. Current-blocking diode and current-limiting resistance, which are generally suggested to be used in TLU measurement setup with bipolar trigger, are investigated for their impacts to both bipolar trigger waveforms and TLU immunity of device under test (DUT). All the experimental results have been successfully verified with device simulation. Finally, a TLU measurement setup without a current-blocking diode but with a small current-limiting resistance is suggested, which can accurately evaluate the TLU immunity of CMOS ICs with neither over estimation nor EOS damage to DUT during TLU test. The suggested measurement setup has been verified with the silicon controlled rectifier (SCR) test structures and the real circuitry (ring oscillator) fabricated in a 0.25-μm CMOS technology.

3.1. Background

During the system-level ESD test, the high-energy ESD-induced noises often cause TLU on CMOS ICs inside the electrical/electronic products, leading to shutdown or malfunction of the EUT. However, during the realistic system-level ESD test, it could be rather complicated or difficult to directly evaluate the TLU immunity of “single” CMOS IC inside the EUT. To solve such problem, a component-level TLU measurement setup with bipolar trigger waveform [41], [42], [46] is utilized. This measurement setup has the advantage of easily evaluating the TLU immunity of single IC by monitoring the voltage/current waveforms through oscilloscope. More importantly, with the ability of generating a bipolar trigger voltage, it can accurately simulate how a CMOS IC will be disturbed by the ESD-generated noises under the system-level ESD test.

The purpose of this chapter is to evaluate an efficient TLU measurement setup with bipolar trigger, which can accurately evaluate the TLU immunity of CMOS ICs under the system-level ESD test. Current-blocking diode and current-limiting resistance, which are generally suggested to be used in TLU measurement setup with bipolar trigger, are investigated to find their impacts to both bipolar trigger waveforms and TLU immunity of the device under test (DUT). All the experimental results can be successfully verified with 2-D device simulation (MEDICI). Finally, a TLU measurement setup without a current-blocking diode but with a small current-limiting resistance is suggested. This suggested measurement setup can accurately evaluate the TLU immunity of CMOS ICs without over estimation. All the experimental results have been verified in silicon with the silicon controlled rectifier (SCR) test structures and the real circuitry (ring oscillator) fabricated in a 0.25-μm CMOS technology.

3.2. Component-Level TLU Measurement Setup

The SCR structure is used as the test structure for TLU measurement because the occurrence of latchup results from the parasitic SCR in CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 2.5(a) and 2.5(b), respectively. The geometrical parameters such as D, S, and W represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent contacts, respectively. In order to consider the layout dependences, the SCR structures with two sets of layout parameters (D=16.6μm, S=1.2μm, and W=22.5μm, as well as, D=16.6μm, S=20μm, and W=22.5μm) are used in this chapter. All the SCR structures have been fabricated in a 0.25-μm salicided CMOS technology.

Several component-level measurement setups to evaluate TLU immunity of CMOS ICs have been developed [20], [27], [41], [42], [46]. In order to accurately simulate the ESD-induced noises on power lines of CMOS ICs under the system-level ESD test, a component-level TLU measurement setup with bipolar trigger voltage [41], [42], [46] is utilized in this chapter. The typical TLU measurement setup with bipolar trigger is sketched in Fig. 3.1. The charging voltage, V_{Charge}, has two different polarities: positive ($V_{Charge}>0$) and negative ($V_{Charge}<0$). The positive (negative) V_{Charge} can generate the positive-going (negative-going) bipolar trigger noises on power pins of the DUT. A capacitor with capacitance of 200pF used in the machine model (MM) [34] ESD test is employed as the charging capacitor. The SCR device shown in Fig. 2.5 is used as the DUT where the P^+ anode

(N^+ cathode) and the N^+ well (P^+ substrate) contact are connected together to V_{DD} (ground). I_{DD} is the total current flowing into the P^+ anode and the N^+ well contact of SCR. The I_{DD} current magnitude and waveform are measured by a separated current probe. The current-blocking diode, which is used to prevent the capacitor-discharged current from flowing into the power supply (*Agilent E3631A*), is used to avoid the possible over estimation for the TLU immunity of DUT [41], [42]. The current-limiting resistance is used to avoid the EOS damage to DUT under a high-current latchup state [46].

For TLU measurement setup with a current-limiting resistance of 5Ω but without the current-blocking diode, the measured V_{DD} and I_{DD} transient responses with V_{Charge} of -3V, -6V, and +13V are shown in Figs. 3.2(a), 3.2(b), and 3.2(c), respectively. The DUT under initial V_{DD} bias of 2.5V is the SCR with specified layout parameters of D=16.6μm, S=1.2μm, and W=22.5μm. With a smaller V_{Charge} of -3V, V_{DD} acts as the intended bipolar trigger just similar to that measured in Fig. 2.3 under the system-level ESD test. Meanwhile, TLU doesn't occur due to a rather small V_{Charge} (only -3V), because I_{DD} doesn't increase after applying the bipolar trigger voltage on V_{DD}. However, with a larger negative (positive) V_{Charge} of -6V (+13V), TLU can be initiated, as shown in Fig. 3.2(b) (3.2(c)). Thus, I_{DD} significantly increases up to 120mA, and V_{DD} is pulled down to the latchup holding voltage of 1.6V. By using this TLU measurement setup with bipolar trigger voltage, the measured V_{DD} and I_{DD} waveforms in Fig. 3.2 can simulate the ESD-disturbed V_{DD} and I_{DD} waveforms in Figs. 2.3 (no TLU) and 2.4 (TLU occurs) under the system-level ESD test.

3.3. Experimental Results

Although TLU measurement setup with bipolar trigger can accurately simulate the practical system-level ESD event, both bipolar trigger waveforms and TLU immunity of CMOS ICs are strongly dependent on the current-blocking diode and current-limiting resistance. To clarify this issue, TLU measurement setups combing two kinds of current-blocking diodes, fast recovery diode (PR1507) and general purpose diode (1N4007), with various current-limiting resistances (0Ω, 5Ω, 10Ω, 20Ω, and 30Ω) are investigated to find their impacts to both bipolar trigger waveforms and TLU immunity of DUT. Both the PR1507 and 1N4007 diodes have a very high reverse breakdown voltage of 1000V. Thus, for $V_{Charge}<1000V$, the PR1507 or 1N4007 diode can certainly prevent the discharge current from flowing into the power supply without junction breakdown.

3.3.1. Dependences of Current-Blocking Diode and Current-Limiting Resistance on Bipolar Trigger Waveforms

The SCR structure in Fig. 2.5 drawn with layout parameters of D=16.6μm, S=1.2μm, and W=22.5μm is used to investigate the influences of current-blocking diode and current-limiting resistance on the bipolar trigger waveform. Furthermore, the charging voltage source (V_{Charge}) is set as small as +8V for positive V_{Charge} and -3V for negative V_{Charge} to prevent the occurrence of TLU, so the bipolar trigger waveform on V_{DD} can be clearly observed.

3.3.1.1. Positive V_{Charge}: With a positive V_{Charge} of +8V, when there is neither current-blocking diode nor current-limiting resistance in the TLU measurement setup, the measured V_{DD} and I_{DD} transient waveforms are shown in Fig. 3.3(a). The V_{DD} waveform reveals the intended positive-going bipolar trigger with a damping frequency of ~10 MHz. Afterwards, when a current-limiting resistance of 20Ω is added to the TLU measurement setup but still without the current-blocking diode, the damping factor of V_{DD} waveform obviously increases, as shown in Fig. 3.3(b). In Fig. 3.3(a), the initial positive peak voltage of V_{DD} takes about 2.5μsec to be fully attenuated, but only 0.8μsec in Fig. 3.3(b). Furthermore, if a current-blocking diode (PR1507) is added to the measurement setup but without the current-limiting resistance, the V_{DD} waveform no longer reveals an underdamped bipolar waveform, but an overdamped unipolar waveform instead, as shown in Fig. 3.3(c). When the initially-stored positive charges in the charging capacitor (200pF) are discharged through the relay into the DUT and power supply, these positive charges are blocked by the current-blocking diode from flowing into the power supply, so the current-blocking diode acts as a large equivalent resistance (open circuit) to these positive charges. As shown in Fig. 3.3(b), a current-limiting resistance of 20Ω increases the damping factor of the V_{DD} waveform, so the equivalent large resistance of the current-blocking diode tremendously increases the damping factor to result in an overdamped unipolar V_{DD} waveform in Fig. 3.3(c).

3.3.1.2. Negative V_{Charge}: With a negative V_{Charge} of -3V, the measured V_{DD} transient waveforms are similar to the positive V_{Charge} case. For example, the measured V_{DD} waveform is a negative-going bipolar trigger when there is neither current-blocking diode nor current-limiting resistance in the measurement setup, as shown in Fig. 3.4(a). Additionally, the damping factor of this measured V_{DD} waveform will increase if an additional current-limiting resistance of 20Ω is added to the measurement setup, as shown in Fig. 3.4(b). However, unlike the positive V_{Charge} case in Fig. 3.3(c) where the V_{DD} waveform is an overdamped unipolar waveform, the V_{DD} waveform in Fig. 3.4(c) is an underdamped bipolar waveform if there is a current-blocking diode (PR1507) but without the current-limiting resistance. When the initially-stored negative charges in the charging capacitor (200pF) are discharged into the power supply, the current-blocking diode is seen as a forward-biased diode by these negative charges, so the current-blocking diode acts as a small equivalent resistance (short circuit) to these negative charges. Thus, similar to the current-limiting resistance of 20Ω in Fig. 3.4(b), the small equivalent resistance of the current-blocking diode also leads to a larger damping factor of the V_{DD} waveform in Fig. 3.4(c).

3.3.2. Dependences of Current-Blocking Diode and Current-Limiting Resistance on TLU Level

The TLU level is defined as the minimum V_{Charge} which can trigger on TLU. Thus, higher TLU level is desired for DUT, because it means that DUT is less sensitive to TLU. Furthermore, layout dependences on TLU level are also investigated by using two SCR structures with the same D (16.6μm) and W (22.5μm) but different S of 1.2μm and 20μm in a 0.25-μm salicided CMOS process.

3.3.2.1. Latchup DC I-V Characteristics of SCR Structures: The experimentally measured latchup DC I-V characteristics of two SCR structures with the same D (16.6μm) and W (22.5μm) but different S of 1.2μm and 20μm are shown in Fig. 3.5. These latchup DC I-V curves are measured by the continuous-type curve tracer. The SCR structure with S=1.2μm (S=20μm) has the trigger voltage (V_{Trig}) and the trigger current (I_{Trig}) of 19.5V (21V) and 2mA (4mA), respectively. Once latchup occurs, a low-impedance path will exist between V_{DD} and ground to conduct a huge current.

For the same SCR, the latchup holding voltage should be the same for both quasi-static latchup and TLU, because the holding voltage only depends on the DUT layout styles and the process parameters. However, the pull-down V_{DD} (~1.6V) of the measured TLU voltage waveforms in Figs. 3.2(b) and 3.2(c) is somewhat higher than the holding voltage (~1V) in the measured latchup DC I-V curves in Fig. 3.5. For the measured TLU voltage waveforms, the pull-down V_{DD} is equal to the $V_{Power\text{-}supply}-(\Delta V_{Resistor}+\Delta V_{Diode})$. Here, $V_{Power\text{-}supply}$ is the applied DC voltage of power supply, and $\Delta V_{Resistor}$ (ΔV_{Diode}) is the voltage drop across the 5Ω current-limiting resistance (current-blocking diode). This pull-down V_{DD} must be higher than the holding voltage of the DUT to sustain the latchup state. For the measured latchup DC I-V curves, however, there is neither additional current-limiting resistance nor current-blocking diode, and the latchup holding voltage is the minimum voltage that the DUT can pull down in the latchup state. Thus, the pull-down V_{DD} (~1.6V) of the measured TLU voltage waveforms is slightly higher than the holding voltage (~1V) in the measured latchup DC I-V curves.

3.3.2.2. Positive TLU Level: For the SCR structure with layout parameters of D=16.6μm, S=1.2μm, and W=22.5μm, the relations between positive TLU level and current-limiting resistances under different current-blocking diodes are shown in Fig. 3.6(a). For measurement setup without current-blocking diode, the TLU level is overall smaller than that equipped with current-blocking diode, no matter with general purpose (1N4007) or fast recovery (PR1507) diode. For measurement setup with current-blocking diode, the TLU-triggering voltage is the unipolar trigger shown in Fig. 3.3(c). Such unipolar trigger can generate I_{Ds} to initiate TLU while V_{DD} rapidly increases from +2.5V to its positive peak voltage (i.e. large dV_{DD}/dt). However, for measurement setup without current-blocking diode, the TLU-triggering voltage is the bipolar trigger shown in Fig. 3.3(a). Such bipolar trigger can generate I_{Sb} instead of I_{Ds} to initiate TLU while V_{DD} switches the forward-biased state ($V_{DD}<0$) to the normal reversed-biased blocking state ($V_{DD}>0$). Because I_{Sb} can initiate TLU more easily than I_{Ds} [45], [46], the measurement setup without a current-blocking diode (induced I_{Sb}) can evaluate a much lower TLU level than that equipped with a current-blocking diode (induced I_{Ds}).

The influences of current-limiting resistance on positive TLU level are also shown in Fig. 3.6(a). For measurement setup without current-blocking diode, the TLU level linearly increases with the current-limiting resistance, because a larger current-limiting resistance can cause a larger damping factor of bipolar voltage on V_{DD}, as shown in Fig. 3.3(b). A larger damping factor will lead to a smaller I_{Sb} due to a smaller voltage magnitude of $-V_{Peak}$ [45]. Therefore, although current-limiting resistance can avoid EOS damage to DUT, it over estimates the TLU level under a bipolar trigger voltage. However, for measurement setup equipped with a current-blocking diode, TLU level is almost independent to current-limiting resistance, because the current-limiting resistance does not obviously affect the I_{Ds} (i.e. dV_{DD}/dt in Fig. 3.3(c)). The equivalent large resistance of current-blocking diode in series with a small current-limiting resistance (<30Ω) makes the effect of current-limiting resistance negligible.

In Fig. 3.6(a), the TLU levels are different from the latchup trigger voltage (+19.5V) of the quasi-static latchup measurements shown in Fig. 3.5. For the quasi-static latchup measurements, the main latchp-triggering current is the reverse junction breakdown current [15]. For the TLU measurements, if the unipolar trigger is the TLU-triggering voltage, it can generate the additional I_{Ds} (due to large dV_{DD}/dt) to initiate TLU in addition to the junction breakdown current. Thus, if there is a current-blocking diode (inducing unipolar trigger) but without the current-limiting resistance in the TLU measurement setup, the TLU level (~+16V) is slightly lower than the latchup trigger voltage (+19.5V) of the quasi-static latchup measurements. However, if the bipolar trigger voltage is the TLU-triggering voltage, the major TLU-triggering current is I_{Sb} (due to V_{DD} switching from negative voltage level to positive voltage level), but not I_{Ds}. It has been clarified that the bipolar trigger can initiate TLU more easily than the unipolar trigger [45], [46]. Thus, there will be a much lower TLU level (~+12V) if there is neither current-blocking diode (induced bipolar trigger) nor current-limiting resistance in the TLU measurement setup.

For the SCR structure with layout parameters of D=16.6μm, S=20μm, and W=22.5μm, the relations between positive TLU level and current-limiting resistances under different current-blocking diodes are shown in Fig. 3.6(b). For measurement setup equipped with a current-blocking diode, the TLU level greatly increases to exceed +100V when the current-limiting resistance is larger than 20Ω. In fact, TLU does not occur in these cases due to one of the following two reasons. First, larger current-limiting resistance leads I_{DD} lower than the latchup holding current. Second, larger voltage drop across larger current-limiting resistance makes V_{DD} lower than the latchup holding voltage. No matter which one happens, TLU does not occur. For example, with a positive V_{Charge} of +35V, the measured V_{DD} and I_{DD} transient waveforms under measurement setup with a current-blocking diode (PR1507) and a current-limiting resistance of 20Ω are shown in Fig. 3.7. TLU initially occurs but finally fails to be maintained, because V_{DD} is pulled down to about 1V, which is lower than its latchup holding voltage (~1.5V). Thus, an additional voltage drop across the current-blocking diode or larger current-limiting resistance can prohibit the occurrence of TLU when the SCR has a larger latchup holding voltage or current (D=16.6μm, S=20μm, and W=22.5μm).

3.3.2.3. Negative TLU Level: For SCR structure with layout parameters of D=16.6μm, W=22.5μm, and S=1.2μm (20μm), the relations between negative TLU level and current-limiting resistances under different current-blocking diodes are shown in Fig. 3.8(a) (Fig. 3.8(b)). Compared with the positive TLU level tests in Fig. 3.6(a) (Fig. 3.6(b)), the magnitudes of negative TLU level are overall lower than those of positive TLU level. For example, the magnitudes of negative TLU level are all lower than 6V in Fig. 3.8(a), but those of positive TLU level are all higher than 10V in Fig. 3.6(a). Compared with the negative-going ($V_{Charge}<0$) bipolar trigger, the positive-going ($V_{Charge}>0$) bipolar trigger needs to take an additional half duration for decaying before V_{DD} reaches to $-V_{Peak}$. Thus, under the same voltage magnitude of both positive and negative V_{Charge}, negative V_{Charge} can provide a larger voltage magnitude of $-V_{Peak}$ (i.e. larger I_{Sb}) than positive V_{Charge} [45]. As a result, SCR structures are more sensitive to TLU with a negative V_{Charge}, leading to a very low negative TLU level in comparison with positive TLU level.

3.4. TLU Simulation

A two-dimensional device simulation tool (MEDICI) is used to verify the dependences of both current-blocking diode and current-limiting resistance on TLU level of the SCR structure. A specified SCR structure with the same geometrical parameters (D=16.6μm and S=1.2μm) in the silicon is used for all TLU device simulations, as shown in Fig. 3.9. With the device simulation, the 2-D boundary conditions of this specified SCR can be well defined to analyze TLU electrical characteristics such as transient I-V characteristics, 2-D current flow lines, electric field, carrier concentration, etc.

3.4.1. Dependences of Current-Blocking Diode on TLU Level

From the measured TLU level dependences in Figs. 3.6 and 3.8, TLU measurement setup equipped with the current-blocking diode (positive-going unipolar trigger) will lead to a higher TLU level (over estimation) of DUT than without the current-blocking diode (bipolar trigger). To demonstrate this phenomenon by device simulation, the simulated V_{DD} and I_{DD} transient responses under unipolar trigger and bipolar trigger are shown in Figs. 3.10 and 3.11, respectively. The related parameters of unipolar trigger (bipolar trigger) such as rise time and falling rate (damping frequency and damping factor) are extracted from the corresponding measured waveforms in Fig. 3.3(c) (Fig. 3.3(a)).

Under the unipolar trigger in Fig. 3.10, TLU will not be initiated due to insufficient I_{Ds}, because the increasing rate ($\equiv +V_{Peak}$-2.5V/rise time) of V_{DD} isn't large enough, even though the $+V_{Peak}$ is as high as +20V. Thus, I_{DD} only comes from the small I_{Ds} or leakage current whose positive peak current (I_{Peak}) is only 0.18mA/μm, and then I_{DD} decreases to 0A when V_{DD} finally returns to its normal operating voltage (+2.5V). The simulated 2-D current flow line after applying the unipolar trigger voltage on V_{DD} (at 18ms) is also shown in the inset figure of Fig. 3.10. Clearly, TLU doesn't occur because no current flow lines conduct through the low-impedance latchup path.

Under the bipolar trigger in Fig. 3.11, TLU can be initiated (I_{DD} significantly increases) by large enough I_{Sb} while V_{DD} returns from $-V_{Peak}$ (-5V) to the normal operating voltage of +2.5V, even though its $+V_{Peak}$ is only +13V, which is much smaller than +20V in Fig. 3.10

(unipolar trigger). Thus, I_{DD} will be kept at a high current latchup state (150mA/μm) after V_{DD} finally returns to its normal operating voltage (+2.5V). The simulated 2-D current flow line after applying the bipolar trigger voltage on V_{DD} (at 1200ns) is also shown in the inset figure of Fig. 3.11. Clearly, TLU occurs because all current flow lines conduct through the low-impedance latchup path. The simulation results in Fig. 3.11 are consistent with the measured TLU waveforms in Fig. 3.2(c) that I_{DD} simultaneously increases with V_{DD} while V_{DD} increases from $-V_{Peak}$ to +2.5V (induced I_{Sb}), but not initially from +2.5V to $+V_{Peak}$ (induced I_{Ds}). Thus, I_{Sb} is the major TLU-triggering current rather than I_{Ds}.

TLU can be also initiated by unipolar trigger with a large enough I_{Ds}. For the unipolar trigger with a higher $+V_{Peak}$ of +25V, the simulated V_{DD} and I_{DD} transient responses for TLU are shown in Fig. 3.12. Due to a larger increasing rate of V_{DD}, TLU can be initiated by large enough I_{Ds} while V_{DD} rapidly increases from the normal operating voltage (+2.5V) to $+V_{Peak}$ (+25V). Thus, I_{DD} will be kept at a high current latchup state (150mA/μm) after V_{DD} finally returns to its normal operating voltage.

The comprehensive simulation results in Figs. 3.10, 3.11 and 3.12 are all consistent with the experimental results to point out that TLU measurement setup equipped with the current-blocking diode will lead to a higher TLU level (over estimation) of DUT than that without the current-blocking diode.

3.4.2. *Dependences of Current-Limiting Resistance on TLU Level*

From the measured TLU level dependences shown in Figs. 3.6 and 3.8, the TLU level of CMOS IC (SCR) increases with current-limiting resistance. To demonstrate this phenomenon by device simulation, two different bipolar triggers are used. As shown in Figs. 3.11 and 3.13, these two different bipolar triggers have the same damping frequency of ~10MHz but different damping factors. Compared to Fig. 3.11, the bipolar trigger with a larger damping factor in Fig. 3.13 is used to simulate the TLU measurement setup equipped with a current-limiting resistance, because the measured V_{DD} waveforms in Figs. 3.3(a) and 3.3(b) show that current-limiting resistance will lead to a larger damping factor. Clearly, because the magnitude of $-V_{Peak}$ decreases from 5V (Fig. 3.11) to 2.5V (Fig. 3.13) due to a larger damping factor, I_{Sb} isn't large enough to initiate TLU while V_{DD} returns from $-V_{Peak}$ to its normal operating voltage. Thus, I_{DD} doesn't significantly increase (I_{Peak} is only of 75μA/μm) with V_{DD}, and then I_{DD} decreases to 0A when V_{DD} finally returns to its normal operating voltage. Thus, the simulation results in Figs. 3.11 and 3.13 are all consistent with the experimental results to verify that TLU level is increased by the current-limiting resistance, as shown in Figs. 3.6 and 3.8.

3.5. Suggested Component-Level TLU Measurement Setup

From the comprehensive measured and simulated TLU level dependency on current-limiting resistance and current-blocking diode in the component-level TLU measurement setup, the TLU measurement setup without a current-blocking diode but with a small current-limiting resistance (5Ω) is suggested. This suggested measurement setup not only can accurately evaluate the TLU immunity of CMOS ICs without over estimation, but also can avoid the EOS damage to DUT during the TLU test.

The current-blocking diode should be eliminated from the TLU measurement setup to accurately evaluate the TLU immunity of CMOS ICs without over estimation. The bipolar transient noises on the power pins of DUT are indeed representative of the practical system-level ESD events, as shown in Figs. 2.3 and 2.4. However, because the current-blocking diode inherently alters the power supply network impedance, the use of current-blocking diode certainly prohibits such bipolar trigger voltage on the power pins of DUT. Instead, an unipolar overdamped trigger voltage will be formed if the diode was added in the TLU measurement setup. Thus, to accurately simulate the practical system-level ESD event, the current-blocking diode should be eliminated from the TLU measurement setup. Additionally, unipolar and bipolar transient V_{DD} noises can generate two different TLU-triggering currents—I_{Ds} for unipolar trigger, and I_{Sb} for bipolar trigger. It has been clarified that the bipolar trigger (I_{Sb}) can initiate TLU more easily than the unipolar trigger (I_{Ds}). Thus, to accurately represent the actual TLU immunity of DUT under the system-level ESD test, the component-level TLU test should be performed without the current-blocking diode.

Similar to current-blocking diode, current-limiting resistance is also unsuitable for being equipped in the component-level TLU measurement setup. Although using current-limiting resistance will not lead to an unipolar trigger, it certainly attenuates the voltage magnitude of bipolar trigger (i.e. larger damping factor), as shown in Figs. 3.3(b) and 3.4(b). A larger damping factor will lead to a smaller TLU-triggering current (I_{Sb}) due to a smaller voltage magnitude of $-V_{Peak}$ [45]. Thus, the TLU level of DUT will increase with the current-limiting resistance, leading to an over estimation of the TLU immunity. Even worse, a too large current-limiting resistance ($>20\Omega$) has been proved to lead TLU not occurring in the SCR structure with a higher holding voltage (1.5V), i.e. SCR with a larger S of $20\mu m$ shown in Figs. 3.6(b) and 3.8(b). As a result, to accurately represent the actual TLU immunity of DUT under the system-level ESD test, a small current-limiting resistance (5Ω) is suggested to be used. This small current-limiting resistance has the advantage of not leading to a serious over estimation of TLU level, as shown in Figs. 3.6 and 3.8. In addition, it can prevent the DUT from the EOS damage during the high-current latchup state.

3.6. TLU Verification on Real Circuits

A 100-MHz ring oscillator consists of 101-stage inverter chain and 7-stage taper buffer fabricated in a 0.25-μm CMOS technology is used as a real circuit for TLU verification. The schematic diagram and layout top view of the ring oscillator are shown in Figs. 3.14(a) and 3.14(b), respectively. The geometrical parameters such as X, Y, and Z represent the distances between well-edge and well (substrate) contact, source (drain) regions of PMOS and NMOS, and the adjacent well (substrate) contacts, respectively. The ring oscillator is treated as the DUT, where the N^+ well contact and the P^+ source of PMOS are connected together to V_{DD1}, whereas the P^+ substrate contact and the N^+ source of NMOS are connected to ground. To evaluate the TLU level of the inverter chain but not the taper buffer, the power line of the taper buffer (V_{DD2}) is separated from the power line of the inverter chain (V_{DD1}). Once TLU is triggered on by a positive or negative V_{Charge} within the ring oscillator, rapid-increasing current will conduct through a low-impedance path between V_{DD1} and ground to probably burn out the chip. To verify TLU issue on ring oscillator, TLU measurement setup equipped with a current-limiting resistance of 5Ω but without the current-blocking diode is used. For the ring oscillator with layout parameters of X=16.6μm, Y=1.2μm, and Z=22.5μm, the measured V_{DD1}, I_{DD1}, and V_{OUT} transient responses for TLU with a V_{Charge} of +7V and -5V are shown in Figs. 3.15(a) and 3.15(b), respectively. In both cases, TLU is triggered on due to large enough I_{Sb} while V_{DD1} increases from its negative peak voltage to the normal operating voltage (+2.5V). Meanwhile, rapid-increasing I_{DD1} accompanies the pull-down V_{DD1} due to a low-impedance path between V_{DD1} and ground. Thus, the ring oscillator fails to function correctly, causing the output voltage of the ring oscillator, V_{Ring}, to be pulled down to ground. Thus, V_{OUT} is kept at +2.5V after the 7-stage taper buffer.

Four measurement setups with two different types of current-blocking diodes (PR1507 and 1N4007) and current-limiting resistances (5Ω and 20Ω) are used to verify whether the suggested measurement setup has the lowest TLU level (without over estimation). Moreover, ring oscillators with two sets of layout parameters (X=16.6μm, Y=1.2μm, and Z=22.5μm, as well as, X=16.6µm, Y=10µm, and Z=0.3µm) are also used to investigate the layout dependences on TLU level. Table 3.1 lists the TLU levels of the ring oscillators with two sets of layout parameters under four different TLU measurement setups.

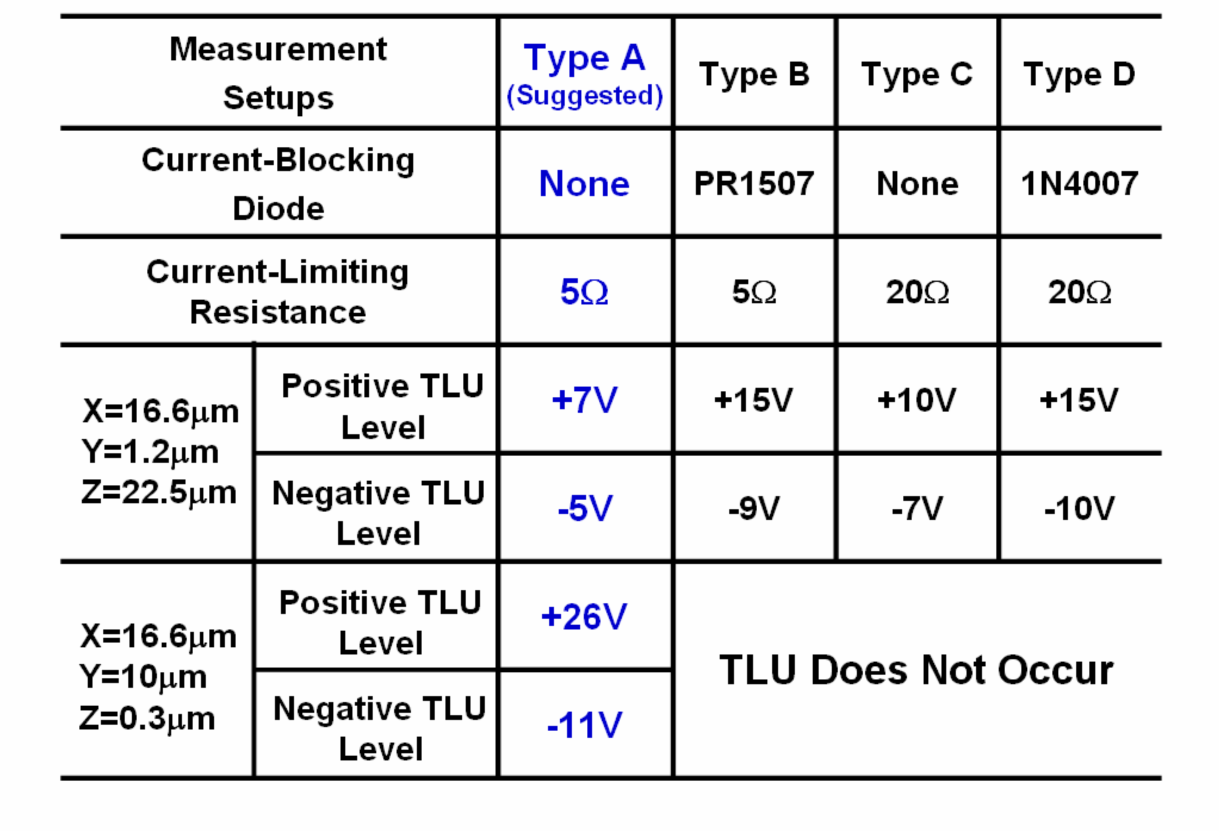
For the ring oscillator with layout parameters of X=16.6µm, Y=1.2µm, and Z=22.5µm, both positive and negative TLU levels measured by the suggested TLU measurement setup (Type A) are lower than those measured by the other three measurement setups (type B, C, and D) where a current-blocking diode or a large current-limiting resistance of 20Ω is used. For the ring oscillator with layout parameters of X=16.6µm, Y=10µm, and Z=0.3µm, TLU occurs only for the suggested measurement setup (type A). In type B, C, and D measurement setups, the additional voltage drop across the current-blocking diode or large current-limiting resistance leads the V_{DD} (I_{DD}) lower than the holding voltage (holding current) of the parasitic SCR in the ring oscillator. Thus, it has been proved once again that the suggested measurement setup (no current-blocking diode but a small current-limiting resistance) can efficiently evaluate TLU level of CMOS ICs without over estimation.

3.7. Conclusion

An efficient component-level TLU measurement setup with bipolar trigger, which can accurately evaluate (without over estimation) the TLU immunity of CMOS ICs under the system-level ESD test for EMC regulation, has been proposed and successfully verified with silicon test chips and device simulation. Through investigating the influences of both current-blocking diode and current-limiting resistance on TLU-triggering voltage waveform and TLU level, it has been demonstrated that TLU measurement setup equipped with either current-blocking diode or current-limiting resistance will over estimate the TLU level of CMOS ICs. However, a small current-limiting resistance has no significant impact to the TLU level, therefore the TLU measurement setup without a current-blocking diode but with a small current-limiting resistance of 5Ω is suggested. This suggested TLU measurement setup not only can accurately evaluate the TLU immunity of CMOS ICs without over estimation, but also can avoid the EOS damage to DUT during TLU test. Such TLU measurement setup can be widely utilized to evaluate the TLU immunity of CMOS ICs in practical field applications.

Table 3.1

TLU levels of the ring oscillators with two sets of layout parameters under four different TLU measurement setups



Measurement Setups		Type A (Suggested)	Type B	Type C	Type D
Current-Blocking Diode		None	PR1507	None	1N4007
Current-Limiting Resistance		5Ω	5Ω	20Ω	20Ω
X=16.6μm Y=1.2μm Z=22.5μm	Positive TLU Level	+7V	+15V	+10V	+15V
	Negative TLU Level	-5V	-9V	-7V	-10V
X=16.6μm Y=10μm Z=0.3μm	Positive TLU Level	+26V	TLU Does Not Occur		
	Negative TLU Level	-11V			

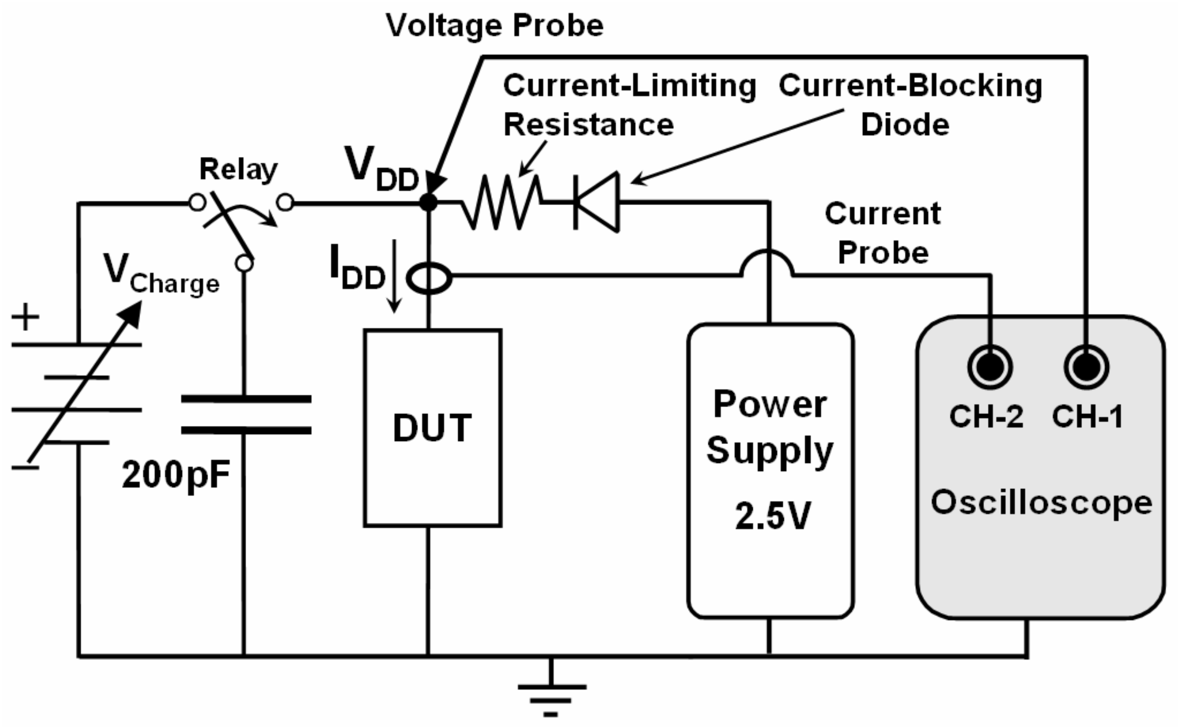
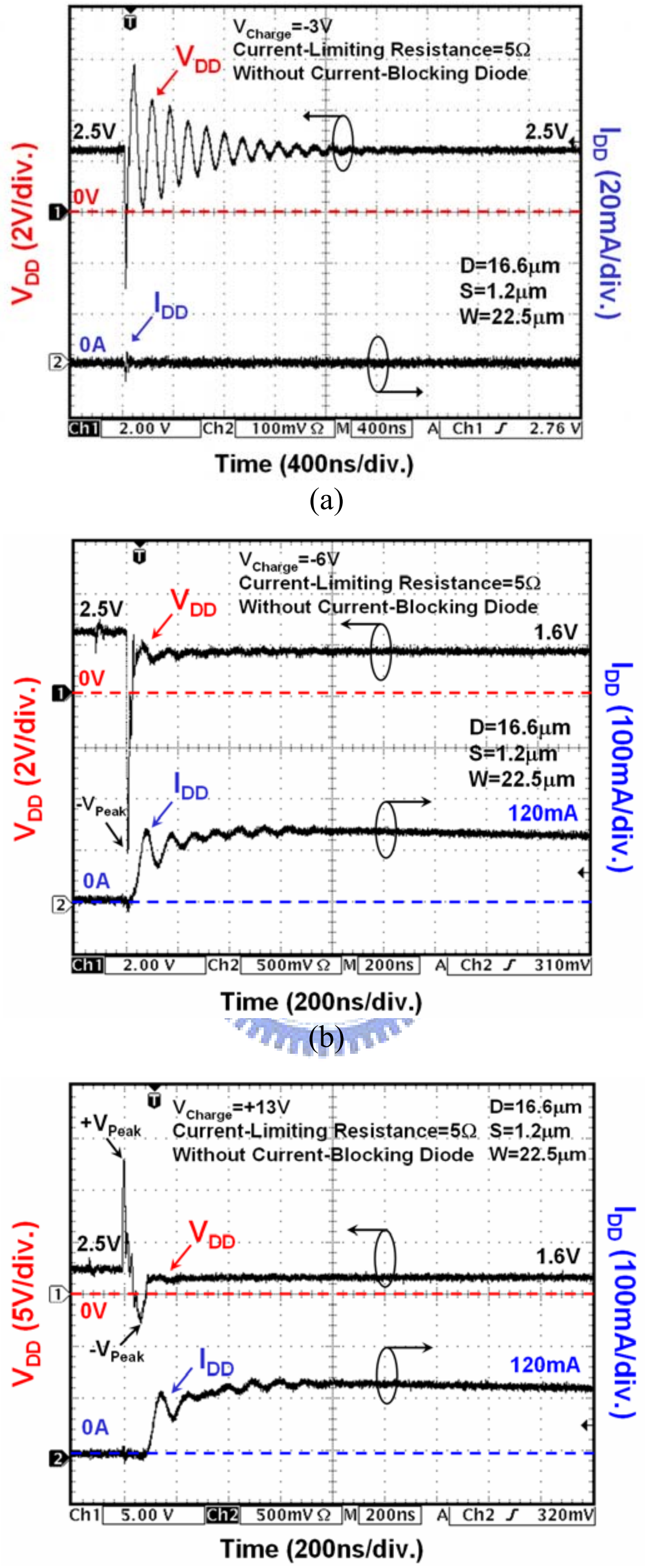


Fig. 3.1 Component-level TLU measurement setup with bipolar trigger [41], [42], [46]. It can accurately simulate how a CMOS IC will be disturbed by the ESD-generated noises under system-level ESD test.

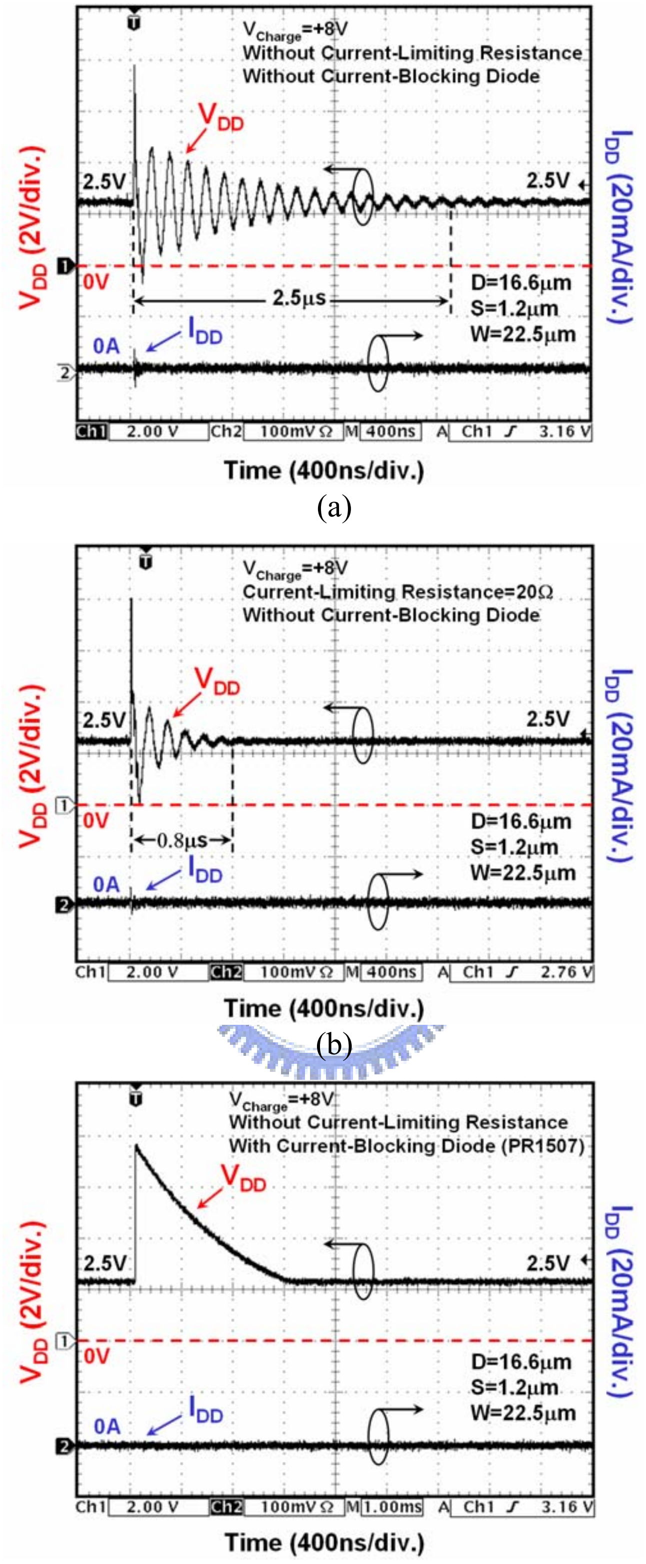


(a)

(b)

(c)

Fig. 3.2 For TLU measurement setup with a current-limiting resistance of 5Ω but without the current-blocking diode, the measured V_{DD} and I_{DD} transient responses with V_{Charge} of (a) -3V, (b) -6V, and (c) +13V.



(a)

(b)

(c)

Fig. 3.3 Measured V_{DD} and I_{DD} transient waveforms with a positive V_{Charge} of +8V. (a) Neither current-blocking diode nor current-limiting resistance, (b) a current-limiting resistance of 20Ω but without a current-blocking diode, and (c) a current-blocking diode (PR1507) but without a current-limiting resistance, is used in the TLU measurement setup.

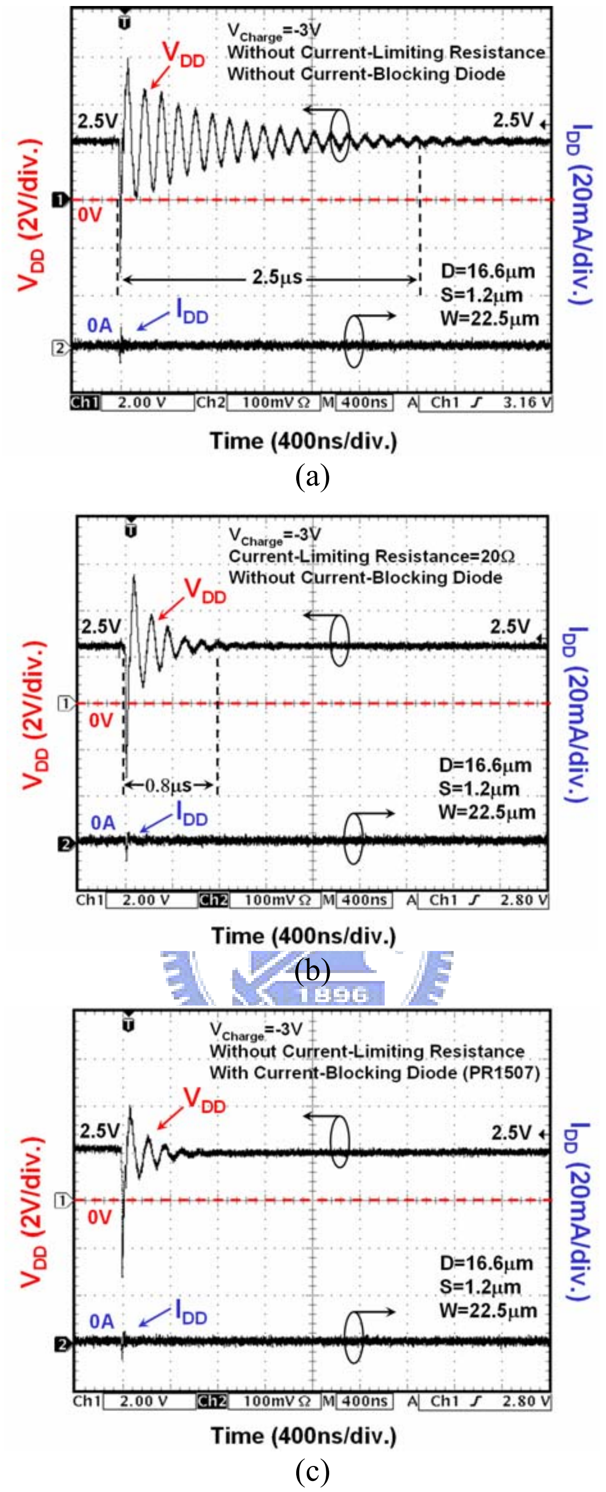


Fig. 3.4 Measured V_{DD} and I_{DD} transient waveforms with a negative V_{Charge} of -3V. (a) Neither current-blocking diode nor current-limiting resistance, (b) a current-limiting resistance of 20Ω but without a current-blocking diode, and (c) a current-blocking diode (PR1507) but without a current-limiting resistance, is used in the TLU measurement setup.

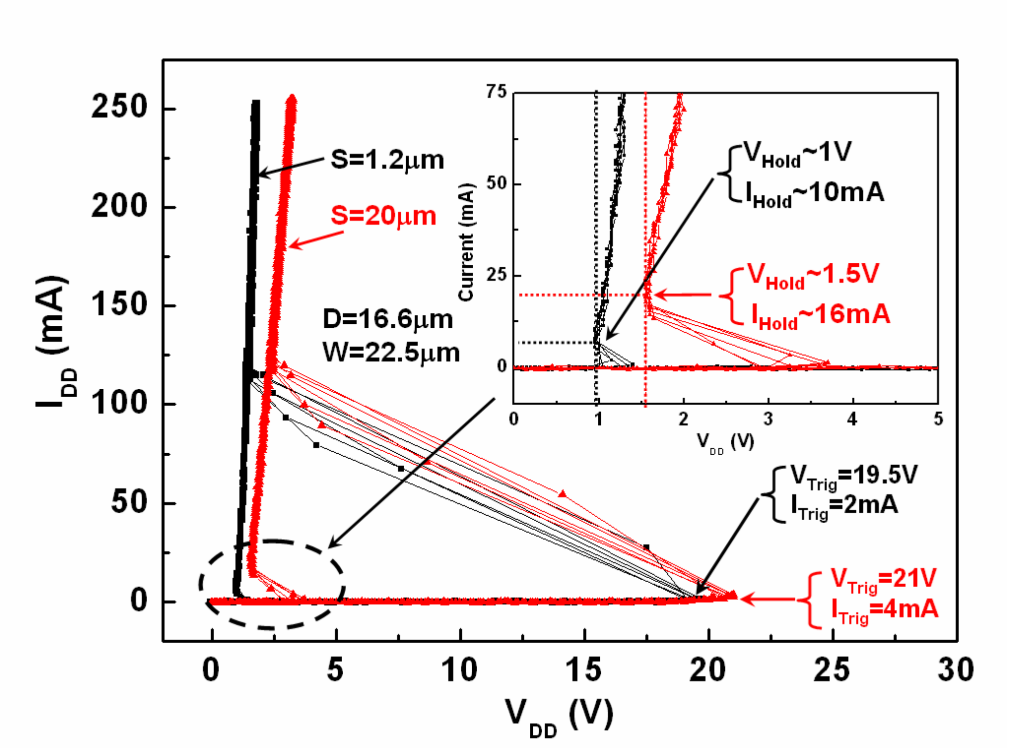
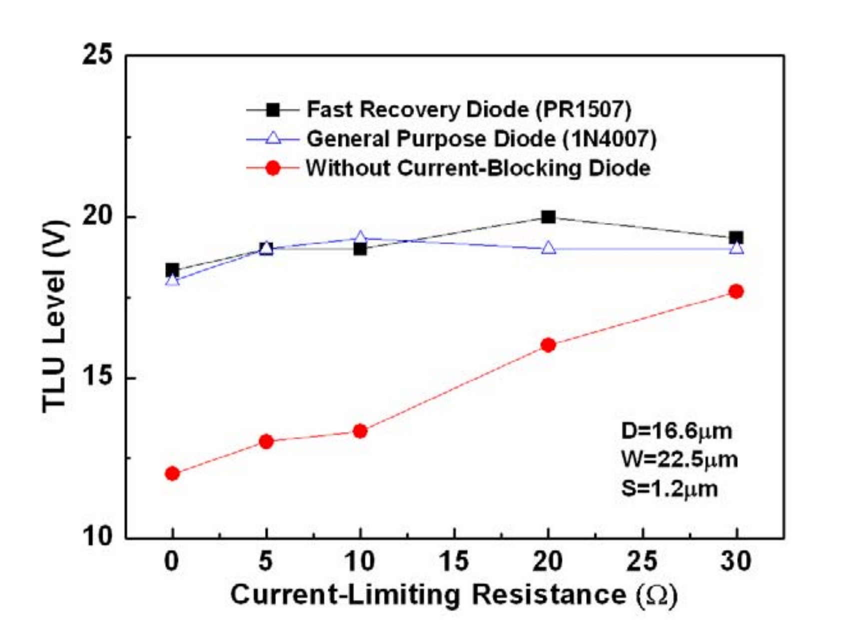
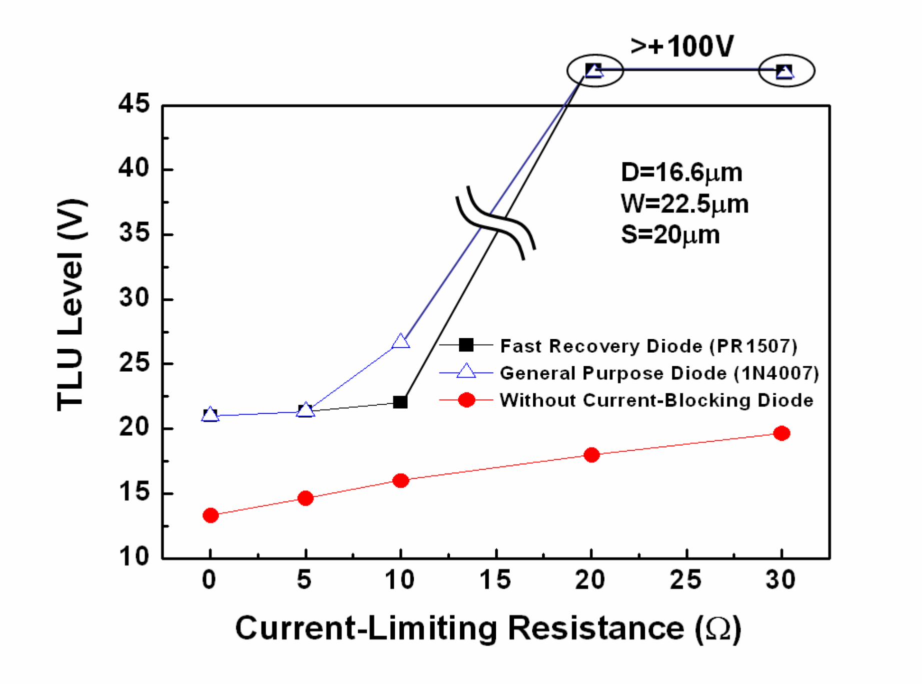


Fig. 3.5 Measured latchup DC I-V characteristics of two SCR structures with the same D (16.6μm) and W (22.5μm) but different S of 1.2μm and 20μm.



(a)



(b)

Fig. 3.6 Relations between positive TLU level and current-limiting resistances under different current-blocking diodes. The SCR structure has the layout parameters of (a) D=16.6μm, S=1.2μm, and W=22.5μm, and (b) D=16.6μm, S=20μm, and W=22.5μm.

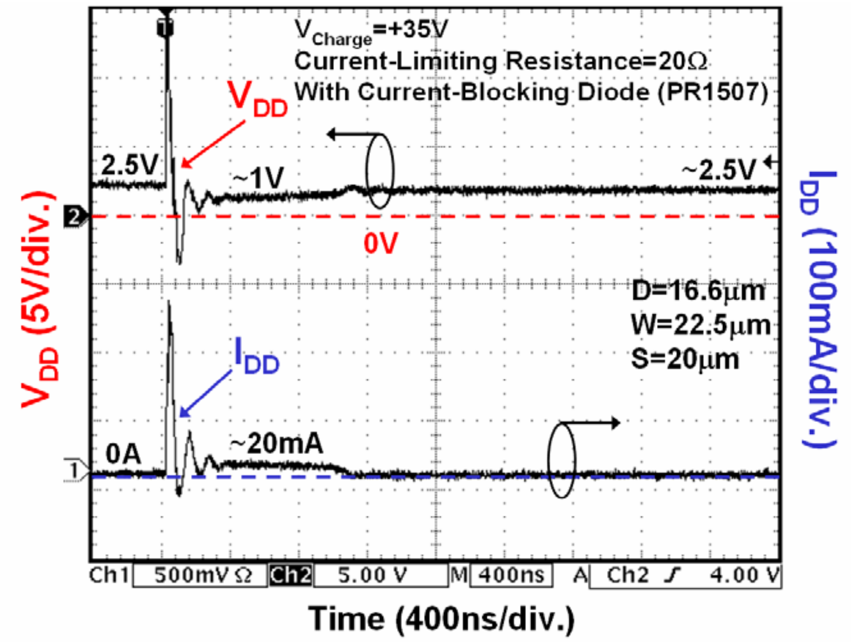
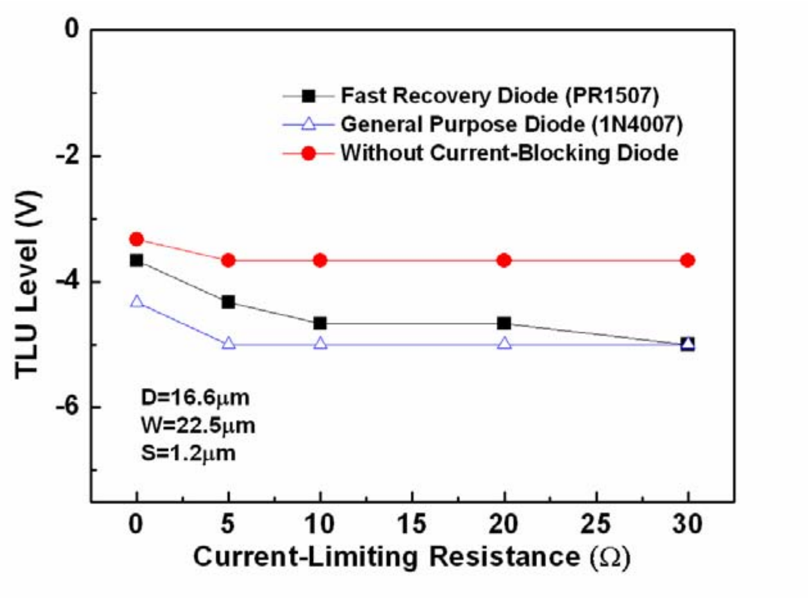
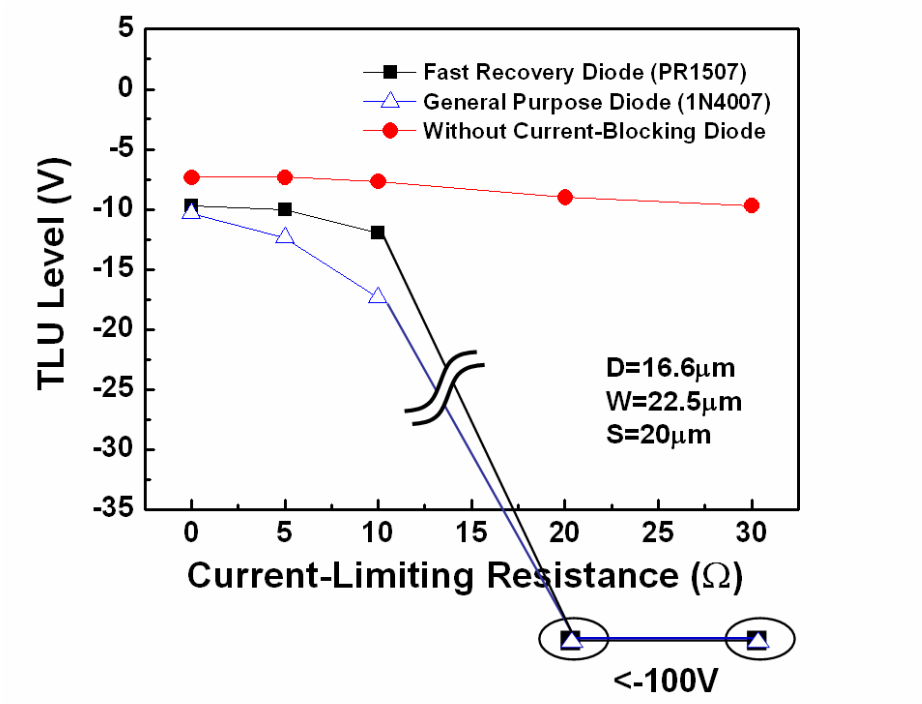


Fig. 3.7 Measured V_{DD} and I_{DD} transient waveforms with a positive V_{Charge} of +35V. A current-blocking diode (PR1507) and a current-limiting resistance of 20Ω are used in the TLU measurement setup.



(a)



(b)

Fig. 3.8 Relations between negative TLU level and current-limiting resistances under different current-blocking diodes. The SCR structure has the layout parameters of (a) D=16.6μm, S=1.2μm, and W=22.5μm, and (b) D=16.6μm, S=20μm, and W=22.5μm.

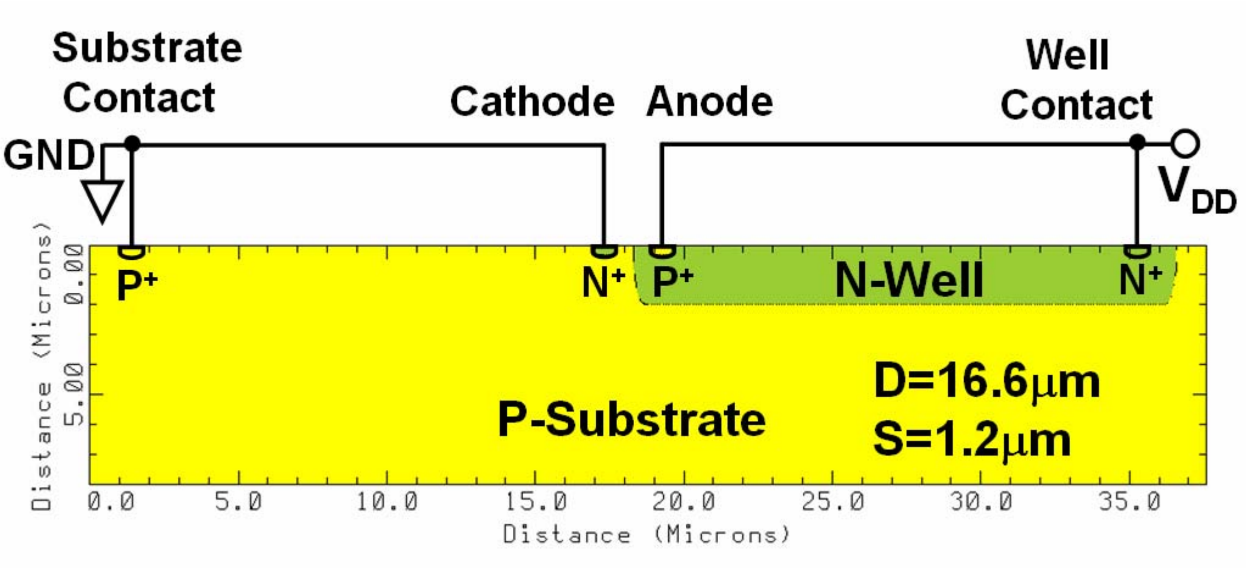


Fig. 3.9 SCR structure used in a two-dimensional device simulation tool (MEDICI). This specified SCR structure has the same geometrical parameters (D=16.6µm and S=1.2µm) of SCR silicon test chips.

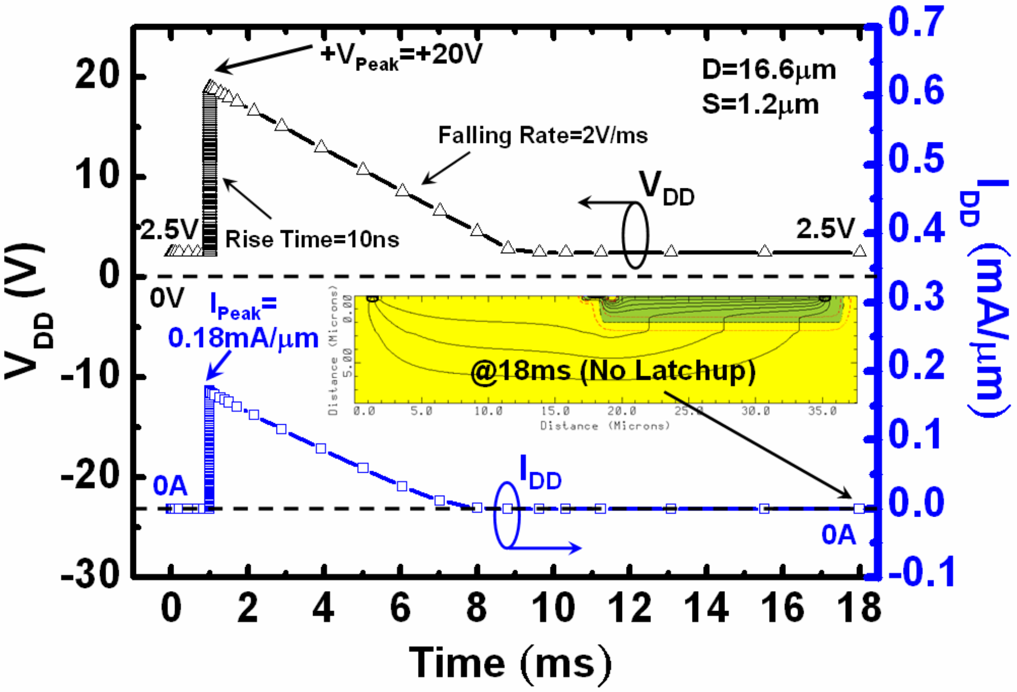


Fig. 3.10 Simulated V_{DD} and I_{DD} transient responses for TLU with unipolar trigger. It can simulate the V_{DD} voltage disturbance in Fig. 3.3(c) for TLU measurement setup equipped with the current-blocking diode. TLU cannot be initiated even though V_{Peak} is as high as +20V.

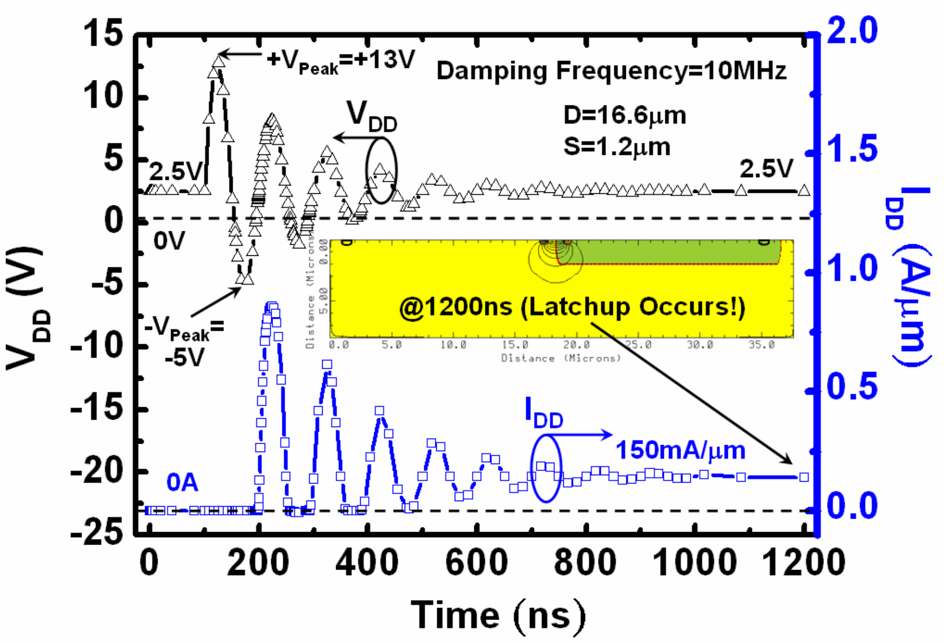


Fig. 3.11 Simulated V_{DD} and I_{DD} transient responses for TLU with bipolar trigger. It can simulate the V_{DD} voltage disturbance in Fig. 3.3(a) for TLU measurement setup without the current-blocking diode. TLU can be initiated even though V_{Peak} is as low as +13V.

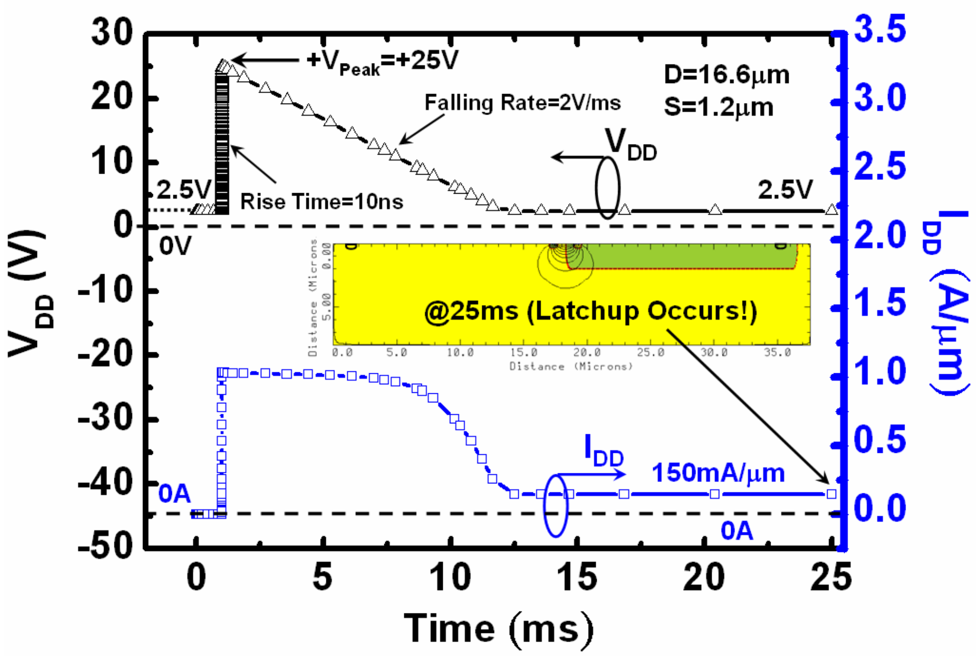


Fig. 3.12 Simulated V_{DD} and I_{DD} transient responses for TLU with unipolar trigger. V_{DD} has a V_{Peak} of +25V, which is larger than +20V in Fig. 3.10, so the increasing rate (≡+V_{Peak}-2.5V/rise time) of V_{DD} is large enough to produce large I_{Ds} to initiate TLU.

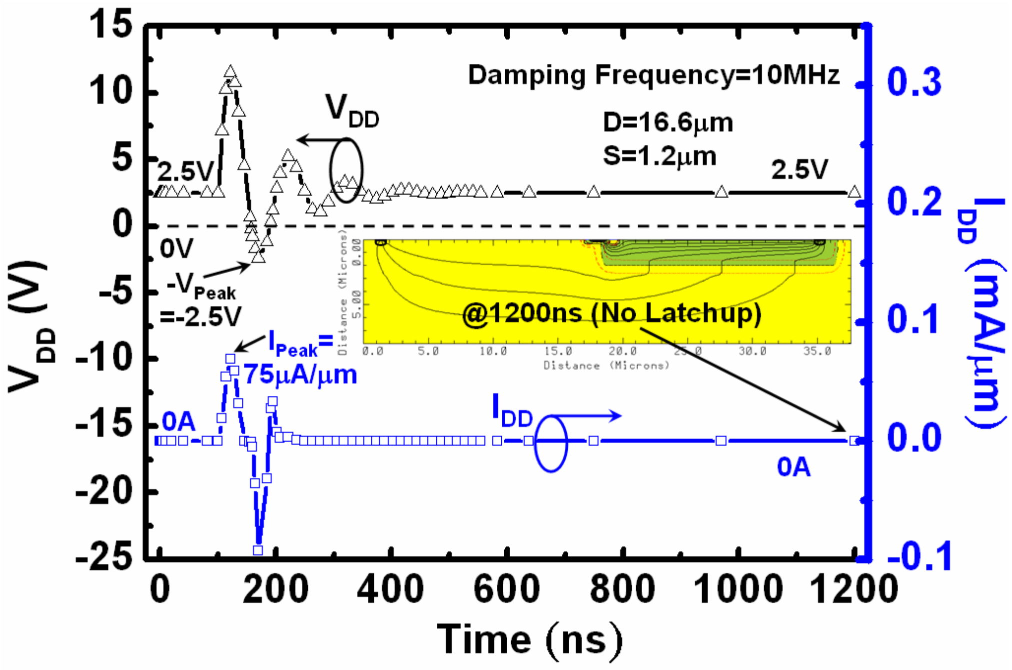


Fig. 3.13 Simulated V_{DD} and I_{DD} transient responses for TLU with bipolar trigger. Compared to Fig. 3.11, it can simulate the bipolar trigger with a larger damping factor in Fig. 3.3(b) for TLU measurement setup equipped with a current-limiting resistance. TLU cannot be initiated due to insufficient I_{Sb}.

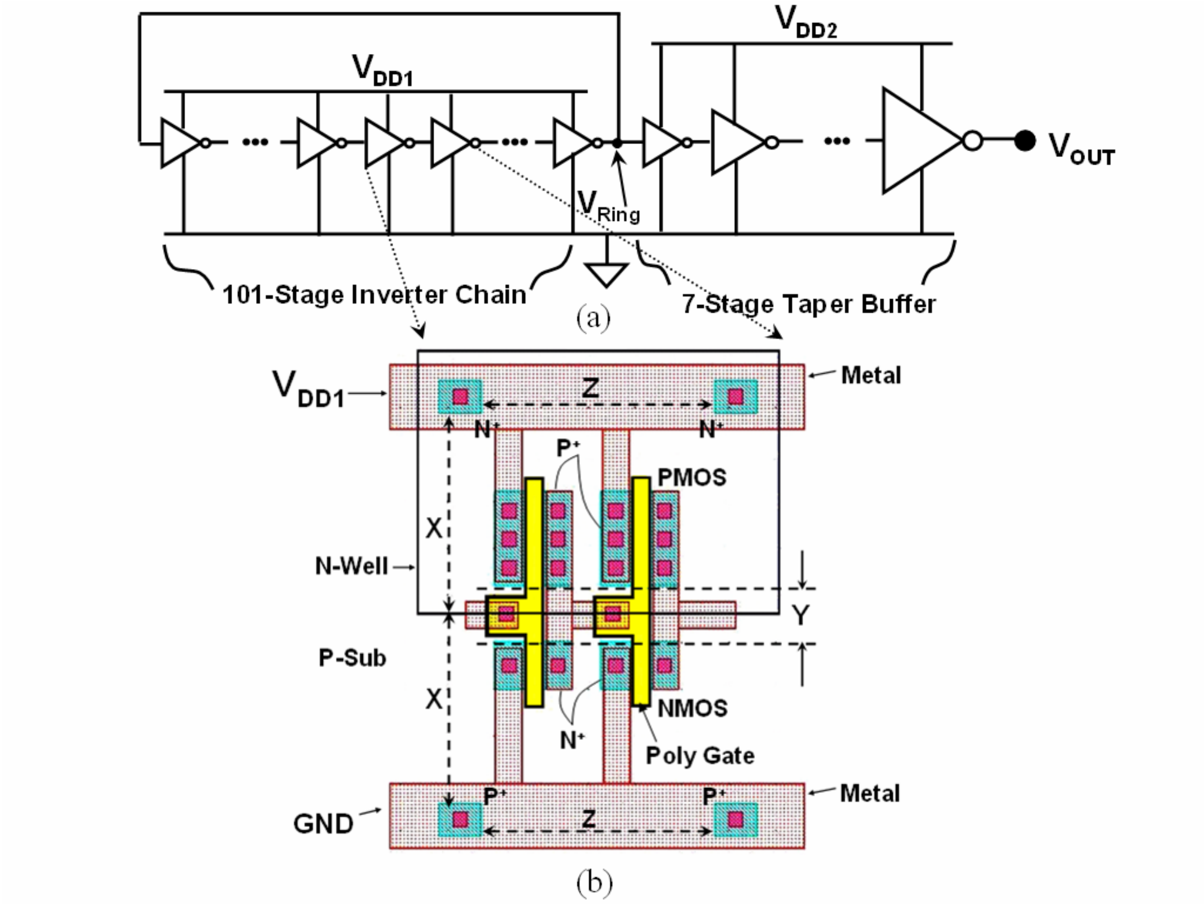
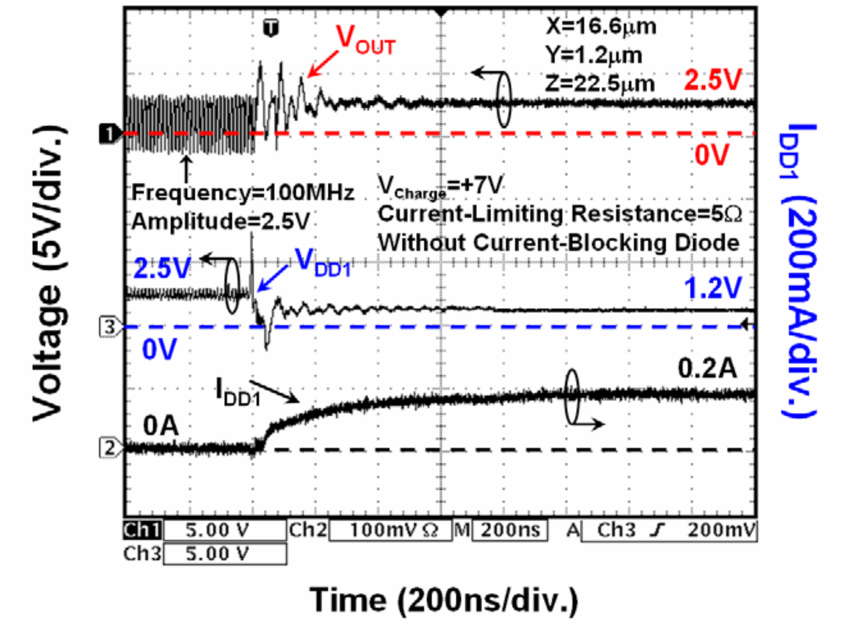
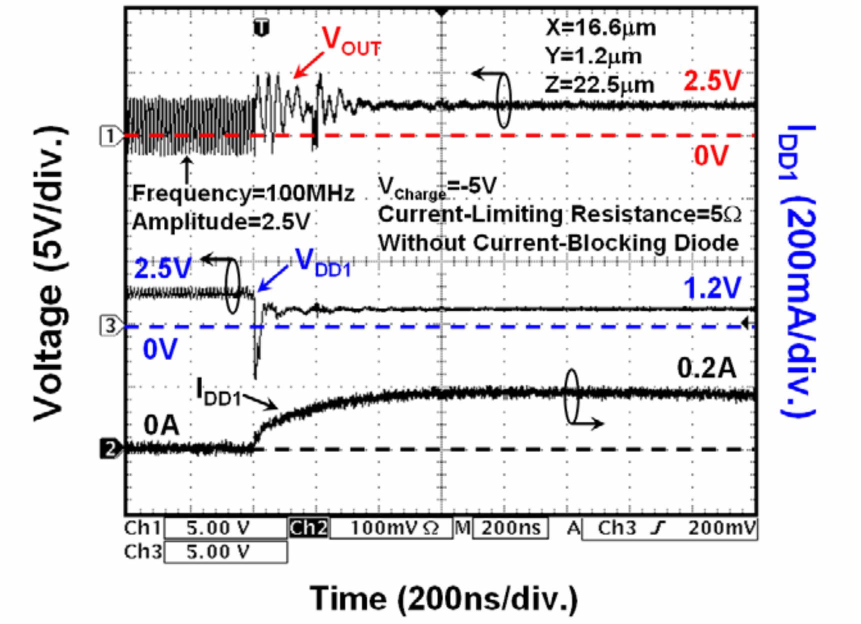


Fig. 3.14 (a) Schematic diagram, and (b) layout top view, of the ring oscillator. The geometrical parameters such as X, Y, and Z represent the distances between well-edge and well (substrate) contact, source (drain) regions of PMOS and NMOS, and the adjacent well (substrate) contacts, respectively.



(a)



(b)

Fig. 3.15 Measured V_{DD1}, I_{DD1}, and V_{OUT} transient waveforms of the ring oscillator with a V_{Charge} of (a) +7V, and (b) -5V. A current-limiting resistance of 5Ω but without a current-blocking diode is used in the TLU measurement setup.

Chapter 4

Evaluation on Board-Level Noise Filter Networks to Suppress Transient-Induced Latchup in CMOS ICs under System-Level ESD Test

Different types of board-level noise filter networks are evaluated to find their effectiveness for improving the immunity of CMOS ICs against transient-induced latchup (TLU) under system-level electrostatic discharge (ESD) test. By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs can be greatly improved. All the experimental evaluations have been verified with the silicon controlled rectifier (SCR) test structures and the ring oscillator circuit fabricated in a 0.25-μm CMOS technology. Some of such board-level solutions can be further integrated into the chip design to effectively improve TLU immunity of CMOS IC products.

4.1. Background

In chapter 2, it has been clarified that the “sweep-back current” [28], [29] caused by the bi-polar trigger voltage on power (ground) pins of CMOS ICs is the major cause of TLU under the system-level ESD test. TLU can be initiated by sweep-back current when bi-polar trigger voltage on V_{DD} increases from its negative peak voltage to a positive voltage [28], [29]. Such sweep-back current is strongly dependent on the related dominant parameters of the bi-polar trigger voltage waveform such as transient peak voltage, damping frequency, and damping factor [45]. In real situations, however, all these parameters depend on the charged voltage of ESD gun, the adopted TLU test mode, metal traces of board-level (chip-level) layout, board-level noise filter network where the device under test (DUT) located, etc. Among these factors to possibly determine the occurrence of TLU, board-level noise filter could be a dominant solution to enhance the TLU immunity of CMOS ICs, because the usage of board-level noise filter network between the noise sources and CMOS ICs can decouple, bypass, or absorb noise voltage (energy) [47], [48] which may initiate TLU. Thus, the TLU immunity of CMOS ICs will strongly depend on the board-level noise filter network. However, so far, it was not investigated yet how the board-level noise filter network can enhance the TLU immunity of CMOS ICs under the system-level ESD test.

The purpose of this chapter is to develop a high efficiency board-level noise filter network for TLU prevention under the system-level ESD test. Different types of noise filter networks are evaluated to find their improvements on TLU immunity, including capacitor filter, ferrite bead, transient voltage suppressor (TVS), and several high-order noise filters such as LC-like (2nd-order) and π-section (3rd-order) filters. All the experimental results have been verified with the SCR test structures and the ring oscillator circuit fabricated in a 0.25-μm CMOS technology.

4.2. Dependencies of Board-Level Noise Filters on Bi-Polar Trigger Waveform under System-Level ESD Test

During the system-level ESD test, boar-level noise filter can enhance TLU immunity of CMOS ICs by decoupling, bypassing, or absorbing ESD-induced noise voltage (energy) which may initiate TLU. That is, boar-level noise filter has strong impacts to the related dominant parameters of the TLU-triggering voltage (bi-polar trigger voltage) such as transient peak voltage, damping frequency, and damping factor. To better clarify how the boar-level noise filter will affect these parameters to further enhance TLU immunity of CMOS ICs, several examples about the dependencies of board-level noise filters on bi-polar trigger waveform under system-level ESD test are given below.

The measurement setup of the system-level ESD test with indirect contact-discharge test mode [32] is shown in Fig. 2.2. Without board-level noise filters to help suppress ESD-induced transient noises, the measured V_{DD} transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT with ESD voltage of -1000V zapping on the HCP is shown in Fig. 4.1. Severe ESD-induced voltage disturbance on V_{DD} can be clearly observed. With a decoupling capacitance of 1nF and 0.1μF between V_{DD} and V_{SS} (ground) of the CMOS IC#1 under the system-level ESD test, the measured V_{DD} transient waveforms with ESD voltage of -1000V zapping on the HCP are shown in Figs. 4.2(a) and 4.2(b), respectively. The decoupling capacitor can suppress transient peak voltage of the original V_{DD} waveform in Fig. 4.1. Thus, the sweep-back current to induce TLU can be greatly reduced, resulting in a better TLU immunity of CMOS IC#1 [28], [29]. Moreover, compared with the original V_{DD} transient waveform in Fig. 4.1, both damping frequency and damping factor are quite different in Fig. 4.2, which cause the impacts to TLU immunity of CMOS IC#1 [45]. For such a simple first-order noise filter, the ability to reduce ESD-induced noise is determined by its dominant pole, i.e., the capacitance of the decoupling capacitor. As a result, larger decoupling capacitance (0.1μF) will perform better ability for noise reduction, as show in Fig. 4.2(b). Thus, for CMOS ICs with different TLU immunity under system-level ESD test, the decoupling capacitance can be optimized upon the intrinsic TLU immunity of DUT.

With bidirectional-type TVS (part number: P6KE series; breakdown voltages (V_{BR}): ±6.8V) between V_{DD} and V_{SS} (ground) of the CMOS IC#1 under system-level ESD test, the measured V_{DD} transient waveform with ESD voltage of -1000V zapping on the HCP is shown in Fig. 4.3. With the equivalent circuit of two Zener diodes in series but opposite in polarity, TVS can protect CMOS ICs from high-voltage transient surges by shunting transient current to have a low clamping voltage across its two terminals. Thus, compared with the original V_{DD} transient waveform in Fig. 4.1, the ESD-induced voltage on V_{DD} can be greatly reduced when it exceeds the V_{BR} of TVS. In addition, both damping frequency and damping factor are also different in Fig. 4.3 due to the parasitic capacitance and inductance in the TVS.

With a resistor-type ferrite bead (minimum impedance of 80Ω at 25MHz) in series with the V_{DD} pin of the CMOS IC#1, the measured V_{DD} transient waveform with ESD voltage of -1000V zapping on the HCP is shown in Fig. 4.4. With the equivalent circuit of an inductor and a small series resistor, ferrite bead can protect CMOS ICs from RF field by absorbing RF energy while the ESD-induced transient current flows through it. Thus, compared with the original V_{DD} transient waveform in Fig. 4.1, there is a smaller transient peak voltage (larger damping factor) of V_{DD} transient waveform in Fig. 4.4, which has the impacts to TLU immunity of CMOS IC#1. From the above several comprehensive measurements, it has been found out that the related dominant parameters of the bi-polar trigger voltage to induce TLU such as transient peak voltage, damping factor, and damping frequency are strongly dependent on the board-level noise filters.

To clarify such TLU issue, with ESD voltage of -3000V zapping on the HCP, the measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 are shown in Fig. 4.5. With a large transient peak voltage of ±60V, TLU is triggered on with large transient current of I_{DD}. Thus, I_{DD} is kept at a high current of 80mA, and V_{DD} is pulled down to the latchup holding voltage of 1.8V, after the ESD-induced disturbance on V_{DD}. If an additional decoupling capacitance of 0.1μF is added between V_{DD} and V_{SS} (ground) of such a TLU-sensitive CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with the same (-3000V) ESD voltage zapping on the HCP are shown in Fig. 4.6. Compared with the measured waveforms in Fig. 4.5 where there is no decoupling capacitance for suppressing ESD-induced noise, the transient peak voltage (damping factor) of the bi-polar trigger waveform is greatly reduced (increased) in Fig. 4.6. As a result, TLU does not occur, and I_{DD} doesn't increase after the ESD-induced disturbance on V_{DD}. Thus, the occurrence of TLU strongly depends on the board-level noise filters, and they should be further investigated to find their improvements on TLU immunity of CMOS ICs.

4.3. Measurement Setup

The proposed component-level TLU measurement setup in chapter 3 is used for TLU measurements, as shown in Fig. 4.7. Through an optimal design for placing a small current-limiting resistance (5Ω) but removing the current-blocking diode between V_{DD} node and the power supply, this measurement setup not only can avoid the possible electrical over-stress (EOS) damage under a high-current latchup state, but also can accurately evaluate the TLU immunity of DUT without over estimation [46]. Noise filter network located between TLU-triggering source and the DUT is used to decouple, bypass, or absorb noise voltage (energy) produced by TLU-triggering source. The DUT in this chapter is the SCR structure. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 2.5(a) and 2.5(b), respectively.

With this component-level TLU measurement setup, the measured V_{DD} and I_{DD} transient responses with V_{Charge} of -2V and -7V are shown in Figs. 4.8(a) and 4.8(b), respectively. The DUT with initial V_{DD} bias of 2.5V is the SCR with specified layout parameters of D=16.6μm, S=20μm, and W=22.5μm. No board-level noise filter is added to the DUT during the TLU measurements in Figs. 4.8(a) and 4.8(b). With a smaller V_{Charge} of -2V, V_{DD} acts as the intended bi-polar trigger voltage just similar to that under the system-level ESD test [35]. In addition, TLU doesn't occur because I_{DD} doesn't increase after applying the bi-polar trigger voltage on V_{DD}, as shown in Fig. 4.8(a). TLU still doesn't occur until V_{Charge} increases up to -7V. Once TLU is initiated, I_{DD} significantly increases up to 60mA, and V_{DD} is pulled down to the latchup holding voltage of 1.8V, as shown in Fig. 4.8(b). With an additional decoupling capacitance of 0.1μF between V_{DD} and V_{SS} (ground) of SCR, the measured V_{DD} and I_{DD} transient responses with a higher V_{Charge} of -15V are shown in Fig. 4.9. With the help of the decoupling capacitor for suppressing transient negative peak voltage of V_{DD} down to -0.8V, TLU will not be initiated, even though V_{Charge} is as high as -15V. As a result, I_{DD} doesn't increase, and V_{DD} is still kept at its normal operating voltage of +2.5V after applying the bi-polar trigger voltage on V_{DD}. From the above TLU measurements in Figs. 4.8 and 4.9, this component-level TLU measurement setup can be used to evaluate the effectiveness of different types of board-level noise filter networks to improve the TLU immunity of CMOS ICs under system-level ESD test.

4.4. Experimental Evaluation

Different types of noise filter networks are investigated for their effectiveness to improve the TLU immunity of SCR structure, including: (1) capacitor filter, (2) LC-like filter, (3) π-section filter, (4) ferrite bead, (5) TVS, and (6) hybrid type filters based on the combinations with TVS and ferrite bead. In this measurement, the SCR structure for all test cases has the same specified layout parameters of D=16.6μm, S=20μm, and W=22.5μm.

4.4.1. TLU Level of the SCR Structure without Noise Filter Network

Without any noise filter networks, the component-level TLU measurement setup in Fig. 4.7 can be used to evaluate the intrinsic (without noise filter network) TLU level of the SCR with various geometrical parameters. The TLU level is defined as the minimum positive (negative) V_{Charge} which can trigger on TLU. Obviously, higher TLU level is better for DUT, because it means that the DUT is less sensitive to TLU under the system-level ESD test. The relations between TLU level and the SCR structures with various geometrical parameters are shown in Figs. 4.10(a) and 4.10(b). The specified SCR structure (with D=16.6μm, S=20μm, and W=22.5μm) used in this chapter has a very low TLU level (positive (negative) level of +15V (-7V)), as shown in Fig. 4.10(b). Actually, it was found out that the SCR structures are rather susceptible to TLU for all different geometrical parameters (the magnitudes of both positive and negative TLU levels are all smaller than 18V) unless the SCR is latchup-free (i.e. latchup holding voltage is larger than the normal operating voltage of +2.5V). Thus, due to such weak immunity to TLU, the board-level noise filter network is indeed necessary to improve the TLU immunity of DUT through bypassing, decoupling, or absorbing noise voltage (energy) between the TLU-triggering source and DUT.

4.4.2. TLU Level of the SCR Structure with Noise Filter Networks

4.4.2.1. Capacitor Filter, LC-Like Filter, and π-Section Filter: Three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter are depicted in Figs. 4.11(a), 4.11(b), and 4.11(c), respectively. Fig. 4.12 shows their improvements on both positive and negative TLU levels of the SCR structure.

The ceramic disc capacitor with advantages such as high rated working voltage (1kV), good thermal stability, and low loss at wide range of frequency is employed as the decoupling capacitor in the noise filter of Fig. 4.11(a). Decoupling capacitances widely ranging from 100pF to 0.1μF are used to investigate their improvements on TLU level of the SCR structure. With the aid of the capacitor filter to reduce the noise voltage on V_{DD}, the positive TLU level can be significantly enhanced from +15V (without decoupling capacitor) to +200V (with decoupling capacitance of 0.1μF), as shown in Fig. 4.12. Similarly, the negative TLU level can be also greatly enhanced from -7V (without decoupling capacitor) to -160V (with decoupling capacitance of 0.1μF). Thus, by choosing a decoupling capacitor with proper capacitance value, a simple 1st-order decoupling capacitor placed between V_{DD} and V_{SS} (ground) of CMOS ICs can be used to appropriately improve the TLU immunity of DUT under the system-level ESD test, no matter for the positive or the negative TLU level.

The ferrite bead, which is commonly used for absorbing RF energy, substitutes for inductor as a 2nd-order LC-like filter component, as shown in Fig. 4.11(b). Here, a resistor-type ferrite bead (part number: RH 3.5x9x0.8 with minimum impedance of 80Ω (120Ω) at 25MHz (100MHz)) is employed. Due to a higher insertion loss (2nd-order filter), such LC-like filter has better TLU level enhancements than capacitor filter (1st-order filter) in Fig. 4.11(a). For example, the positive TLU level can be significantly enhanced from +15V (without decoupling capacitor) up to +310V (with decoupling capacitance of 0.1μF), as shown in Fig. 4.12. Similarly, the negative TLU level can be also greatly enhanced from -7V (without decoupling capacitor) to -280V (with decoupling capacitance of 0.1μF). Thus, in order to achieve higher TLU level, the LC-like filter can be used to avoid an excessively or unreasonably large decoupling capacitance in a simple 1st-order capacitor filter.

A 3rd-order π-section filter is used to further enhance the TLU level of the SCR, as shown in Fig. 4.11(c). This π-section filter consists of a ferrite bead (the same one in Fig. 4.11(b)) and two decoupling capacitors with equal decoupling capacitance. With the highest insertion loss among the noise filter networks in Figs. 4.11(a), 4.11(b), and 4.11(c), the TLU level of SCR can be most greatly improved. For example, the positive TLU level can be significantly enhanced up to +410V (with decoupling capacitance of 0.1μF), as shown in Fig. 4.12. Similarly, the negative TLU level can be also significantly enhanced up to -370V (with decoupling capacitance of 0.1μF). From the comprehensive measured results in Fig. 4.12, the decoupling capacitance can be optimized according to how large the intended TLU level will be and what kind of board-level noise filter one is chosen.

4.4.2.2. Ferrite Bead, TVS, and Hybrid Type Filters: Four other types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II are depicted in Figs. 4.13(a), 4.13(b), 4.13(c), and 4.13(d), respectively. Fig. 4.14 shows their improvements on both positive and negative TLU levels of the SCR structure.

The ferrite bead can absorb RF energy while the noise-induced transient current flows through it. The resistor-type ferrite beads with three different minimum impedances at 25MHz are employed in this chapter: 35Ω, 50Ω, and 80Ω. However, a noise filter network with only ferrite bead alone doesn't perform well enhancement on TLU level due to a worse energy-absorbing ability at frequency lower than 10MHz [48]. As a result, TLU level of the SCR structure will not be efficiently improved (the magnitudes of both positive and negative TLU levels are all lower than 25V), even though the minimum impedance of the ferrite bead at 25MHz is as high as 80Ω, as shown in Fig. 4.14.

TVS, which is commonly used to bypass/decouple the high-frequency transient noises, is also considered for its enhancement on TLU immunity of the SCR. The bidirectional-type TVS (part number: P6KE series) with three different breakdown voltages, V_{BR}, (±6.8V, ±16V, and ±27V) are employed. As shown in Fig. 4.14, the TVS with breakdown voltage of ±16V or ±27V fail to efficiently improve the TLU level of the SCR (the magnitudes of both positive and negative TLU levels are all lower than 25V), because TLU occurs prior to the breakdown of such high-V_{BR} TVS. That is, the intrinsic TLU level of SCR (positive and negative TLU level of +15V and -7V) is smaller than the V_{BR} of such high-V_{BR} TVS (±16V and ±27V). Only the TVS with V_{BR} lower than the intrinsic TLU level of DUT can effectively enhance the TLU level. For example, the positive (negative) TLU level can be enhanced up to +240V (-50V) for low-V_{BR} (±6.8V) TVS. Thus, to optimize the efficiency of TVS for TLU prevention, it should be clarified in advance for the correlations between V_{BR} of TVS and the intrinsic TLU level of DUT.

Hybrid type filters consisting of both ferrite bead (minimum impedance of 80Ω at 25MHz) and TVS (with different V_{BR}) are also evaluated for their improvements on TLU level of the SCR, as shown in Figs. 4.13(c) and 4.13(d). Hybrid types I and II are the counterparts of the LC-like and π-section filters where the TVS substitutes for the decoupling capacitor as a low-pass filter component. Because the magnitude of intrinsic TLU level is larger than 7V, only the hybrid type filters with a low-V_{BR} (±6.8V) TVS can efficiently improve the TLU level, as shown in Fig. 4.14. For example, hybrid type I with low-V_{BR} (±6.8V) TVS can greatly enhance the positive (negative) TLU level up to +480V (-65V), which is much larger than +25V (-15V) for that with high-V_{BR} (±16V and ±27V) TVS. In addition, because such higher-order hybrid type filters provide the higher insertion loss, they can enhance the TLU level of SCR more greatly than ferrite bead or TVS alone. For example, for hybrid type filters with a low-V_{BR} (±6.8V) TVS, hybrid type I (II) can greatly enhance the positive TLU level up to +480V (+620V), and enhance the negative TLU levels up to -65V (-410V).

Through investigating different types of noise filter networks to find their improvements on TLU levels in Figs. 4.12 and 4.14, it can be found out TVS (hybrid type I) doesn't improve the negative TLU level as greatly as the 1st-order capacitor filter (LC-like filter). For example, the negative TLU level can be greatly enhanced up to -160V (-280V) for 1st-order capacitor filter (LC-like filter) with decoupling capacitance of 0.1μF, but only up to -50V (-65V) for TVS (hybrid type I) with a low V_{BR} of ±6.8V. Thus, the decoupling capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance negative TLU level more efficiently, but also is compatible to CMOS technology for integrating the noise filter into the CMOS chips.

4.5. Verification on Real Circuits

A 100-MHz ring oscillator circuit with 101-stage inverter chain and 7-stage taper buffer fabricated in a 0.25-μm CMOS technology is used as a real circuit to investigate different types of noise filter networks for their enhancements on TLU levels. The schematic diagram and layout top view of the ring oscillator are shown in Figs. 3.14(a) and 3.14(b), respectively. The ring oscillator is treated as the DUT in Fig. 4.7, where the N^+ well contact and the P^+ source of PMOS are connected together to V_{DD1}, but the P^+ substrate contact and the N^+ source of NMOS are connected to V_{SS} (ground). The component-level TLU measurement setup in Fig. 4.7 can be used to simulate system-level ESD test by applying the bi-polar trigger voltage on V_{DD1}, and to further evaluate the effectiveness of different types of board-level noise filter networks to improve TLU immunity of the ring oscillator circuit under system-level ESD test.

To consider the worst case of evaluating TLU level, the ring oscillator circuit with layout parameters of X=16.6μm, Y=1.2μm, and Z=10.5μm is used. The anode to cathode spacing (Y) of 1.2μm is the minimum allowed distance according to the foundry's design rule. In addition, a large X (Z) of 16.6μm (10.5μm) makes sure there is a large parasitic well or substrate resistance of the parasitic SCR within ring oscillator, so that this ring oscillator circuit has a small latchup triggering current or holding voltage (i.e. most sensitive to latchup).

4.5.1. TLU Transient Waveforms of the Ring Oscillator

Figs. 4.15(a) and 4.15(b) show the measured V_{DD1}, I_{DD1}, and V_{OUT} transient responses for the ring oscillator without and with the board-level noise filter network, respectively. For the ring oscillator without the board-level noise filter network, TLU can be triggered on even if the V_{Charge} is as low as -5V, as shown in Fig. 4.15(a). Once TLU is initiated, I_{DD1} will significantly increase (0.14A) with the pull-down V_{DD1} (1.2V) due to a low-impedance latching path between V_{DD1} and ground. Thus, the ring oscillator fails to function correctly, causing the output voltage of the ring oscillator, V_{Ring}, to be pulled down to ground. So, V_{OUT} is kept at +2.5V after the 7-stage taper buffer.

For the ring oscillator with the board-level noise filter network (capacitor filter with decoupling capacitance of 0.1μF), TLU doesn't occur even though the V_{Charge} is as high as -30V, as shown in Fig. 4.15(b). Clearly, with the aid of the decoupling capacitor to decouple TLU-triggering noises on V_{DD1}, the ring oscillator still maintains its normal function (V_{OUT} with 100-MHz voltage clock) after the TLU-triggering disturbance on V_{DD1}.

4.5.2. TLU Level of the Ring Oscillator with Noise Filter Networks

Fig. 4.16 shows the relations between the decoupling capacitance and the TLU level of the ring oscillator under three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter. With the aid of the 1st-order capacitor filter (0.1μF), the positive (negative) TLU level can be enhanced from +8V (-5V) to +70V (-60V). In addition, higher-order noise filter networks such as LC-like filter and π-section filter can be used to achieve higher TLU level. For example, with decoupling capacitance of 0.1μF, the positive (negative) TLU level can be enhanced up to +90V (-85V) for LC-like filter, and up to +210V (-155V) for π-section filter.

Fig. 4.17 shows the relations among the TLU level of the ring oscillator circuit, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II. Due to a worse energy-absorbing ability of ferrite bead at frequency lower than 10MHz [48], the TLU level will not be efficiently improved by only ferrite bead alone (the magnitudes of both positive and negative TLU levels are all lower than 25V), even though the minimum impedance of the ferrite bead at 25MHz is as high as 80Ω. With the low-V_{BR} (±6.8V) TVS alone, the positive (negative) TLU level can be enhanced up to +30V (-33V). Such low-V_{BR} TVS can be used in hybrid type filters to further enhance the TLU level. As shown in Fig. 4.17, the positive (negative) TLU level is only +30V (-33V) for TVS alone, but it can be enhanced up to +40V (-42V) for hybrid type I, and up to +100V (-125V) for hybrid type II.

Among the comprehensive measured results in Figs. 4.12, 4.14, 4.16, and 4.17, through investigating the TLU level enhancements by different types of noise filter networks for stand-alone SCR and the ring oscillator circuit, the TLU levels of the ring oscillator are overall smaller than those of the SCR. The reason is that the ring oscillator has smaller DC latchup trigger current (voltage) due to both the layout geometrical parameters and the larger total p-n junction area. That is, the ring oscillator circuit is more sensitive to latchup than the SCR. Thus, the effectiveness of noise filter networks to enhance TLU immunity strongly depends on DUT. As a result, the DC latchup characteristics of DUT should be identified in advance when the board-level noise filter networks are designed to improve the TLU immunity of DUT under the system-level ESD test.

4.6. Conclusion

By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs under the system-level ESD test can be greatly improved. From the experimental results, the decoupling capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance negative TLU level more efficiently, but also is compatible to CMOS technology for integrating the noise filter into chips. In addition, the TLU level enhancements by different types of noise filter networks strongly depend on the DUT. Thus, the DC latchup characteristics of DUT should be identified in advance when the board-level noise filter networks are designed to improve the TLU immunity of DUT under the system-level ESD test. The optimal design for enhancements of TLU immunity can be achieved through well characterization between the intrinsic latchup characteristics of DUT as well as the efficiency of TLU prevention from different kinds of board-level noise filters. To further improve TLU immunity of electronic products, chip-level solutions should be adopted along with board-level solutions to meet the applications with high system-level ESD specification.

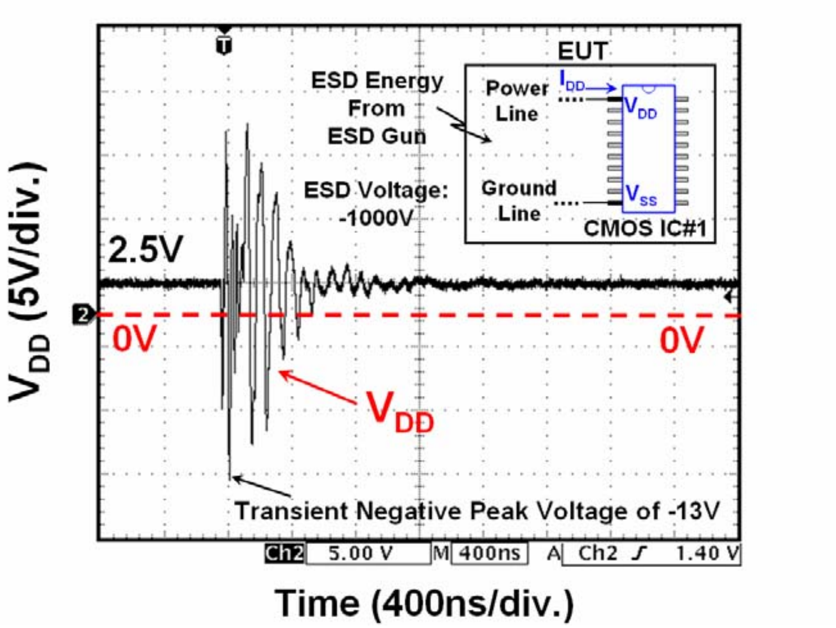
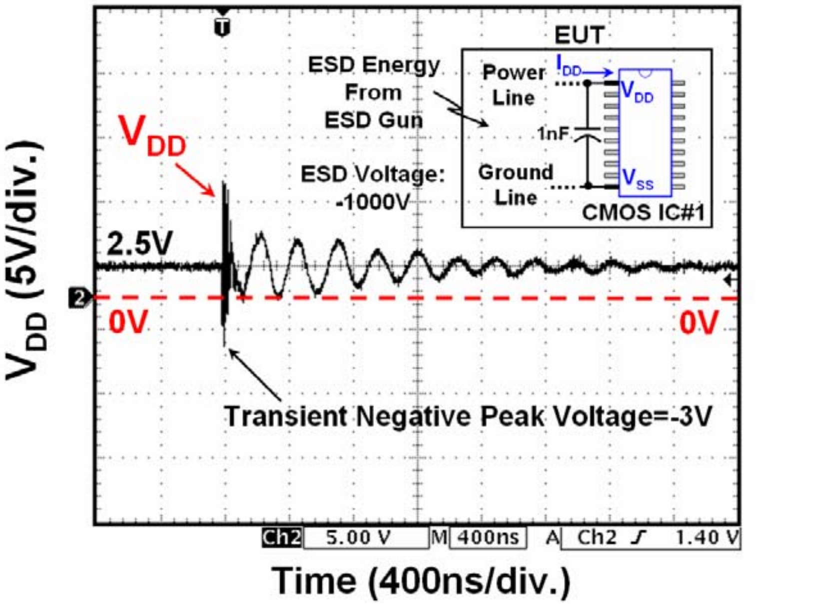
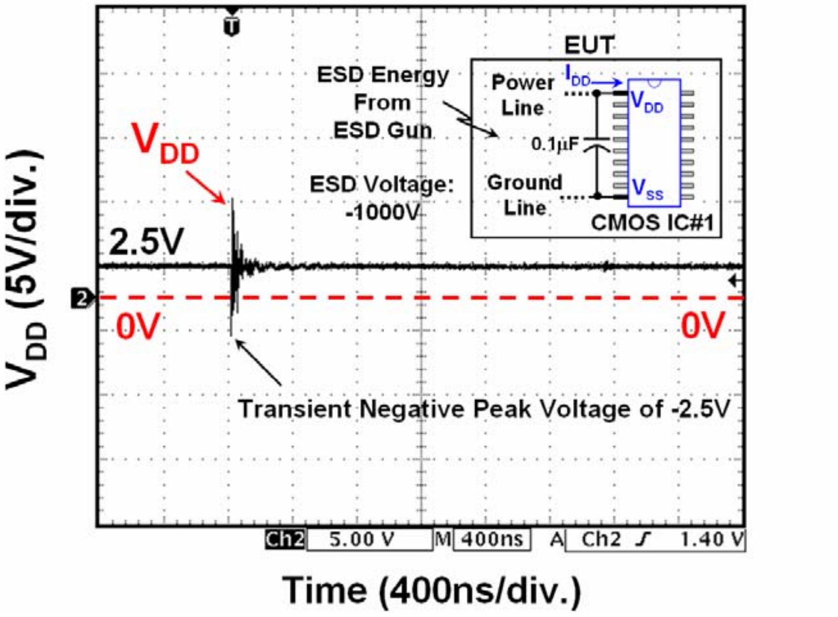


Fig. 4.1 Measured V_{DD} transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT with ESD voltage of -1000V zapping on the HCP. V_{DD} waveform acts as a bi-polar voltage due to the disturbance of the high ESD-coupled energy.



(a)



(b)

Fig. 4.2 With an additional decoupling capacitance of (a) 1nF, and (b) 0.1μF, between V_{DD} and V_{SS} (ground) of the CMOS IC#1 under system-level ESD test, the measured V_{DD} transient waveform with ESD voltage of -1000V zapping on the HCP. Compared with the original V_{DD} transient waveform in Fig. 4.1, transient peak voltage of V_{DD} waveform can be suppressed to enhance the TLU immunity of CMOS IC#1.

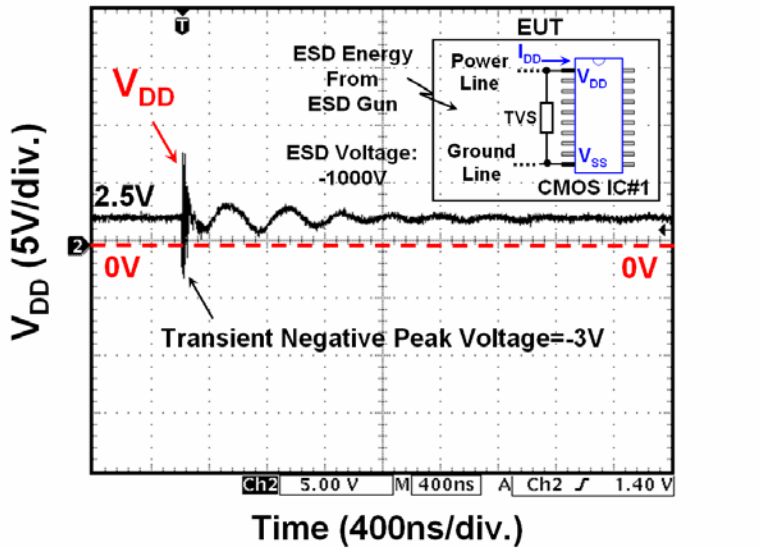


Fig. 4.3 With a bidirectional-type TVS (part number: P6KE series; breakdown voltages: ±6.8V) between V_{DD} and V_{SS} (ground) of the CMOS IC#1 under system-level ESD test, the measured V_{DD} transient waveform with ESD voltage of -1000V zapping on the HCP. Transient peak voltage on V_{DD} of CMOS IC#1 can be greatly reduced when it exceeds the V_{BR} of TVS.

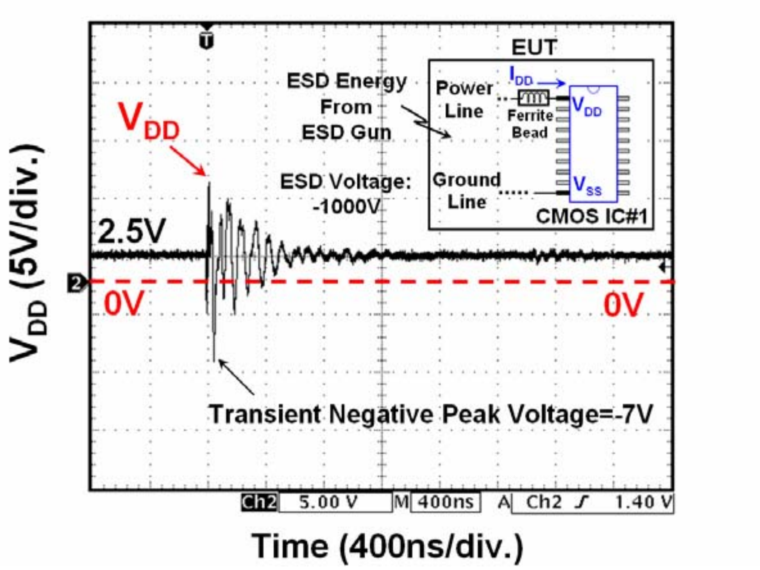


Fig. 4.4 With a resistor-type ferrite bead (minimum impedance of 80Ω at 25MHz) in series with the V_{DD} pin of the CMOS IC#1 under system-level ESD test, the measured V_{DD} transient waveform with ESD voltage of -1000V zapping on the HCP. The transient peak voltage (damping factor) of V_{DD} waveform is smaller (larger) than that of the original V_{DD} transient waveform in Fig. 4.1.

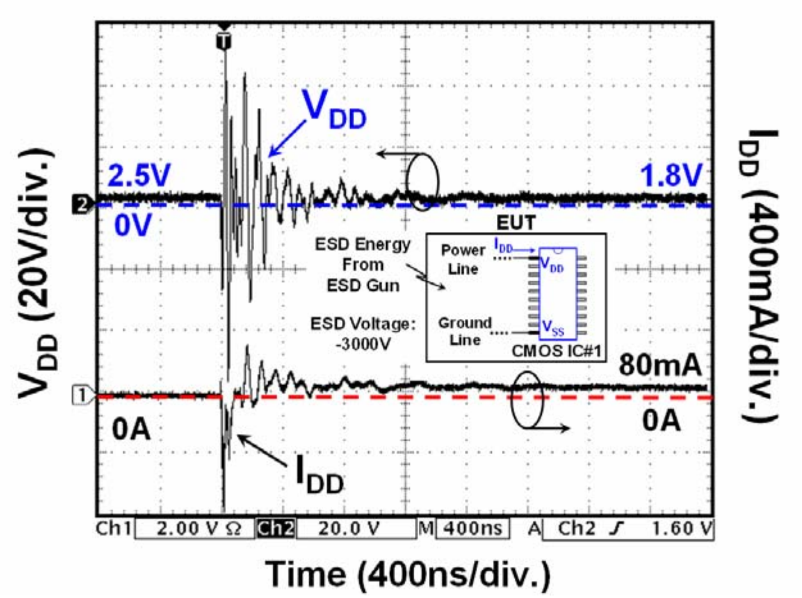


Fig. 4.5 Measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 with ESD voltage of -3000V zapping on the HCP. With a large transient peak voltage of ±60V, TLU is triggered on (I_{DD} is kept at a high current of 80mA) after the ESD-induced disturbance on V_{DD}.

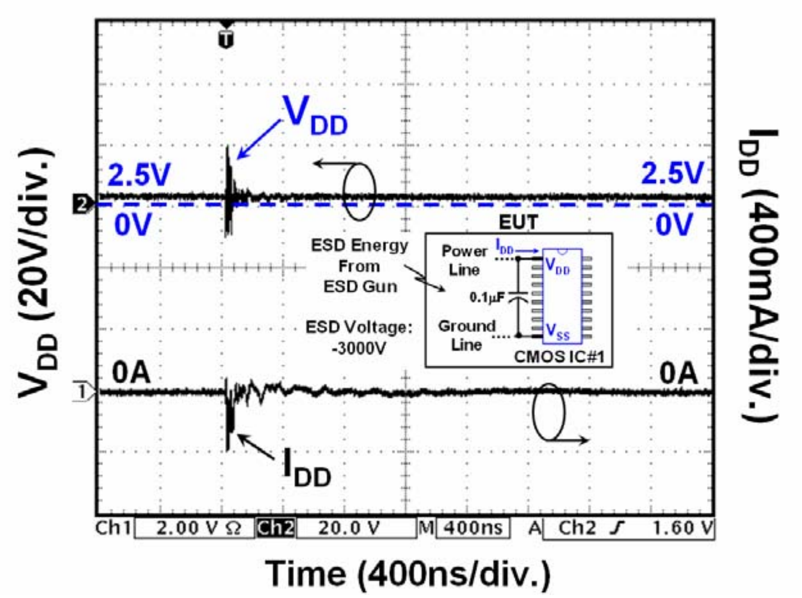


Fig. 4.6 With the decoupling capacitance of 0.1μF between V_{DD} and V_{SS} of the CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with the same (-3000V) ESD voltage zapping on the HCP. Compared with the measured waveforms in Fig. 4.5, TLU does not occur, because ESD-induced disturbance on V_{DD} is greatly reduced.

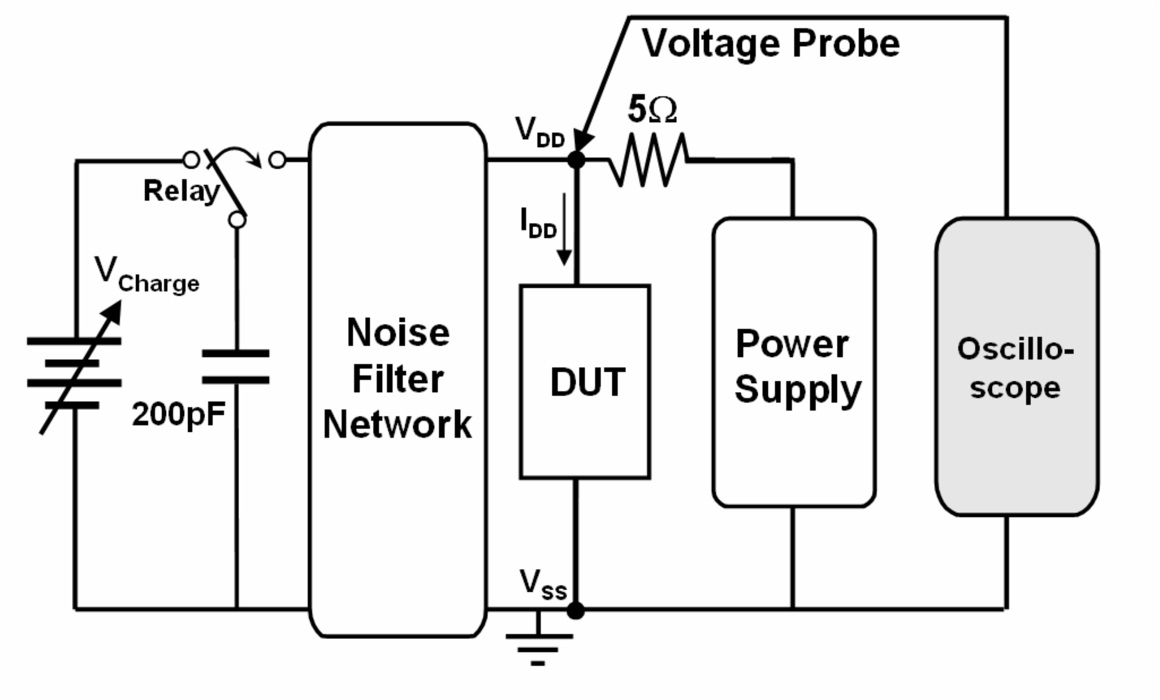
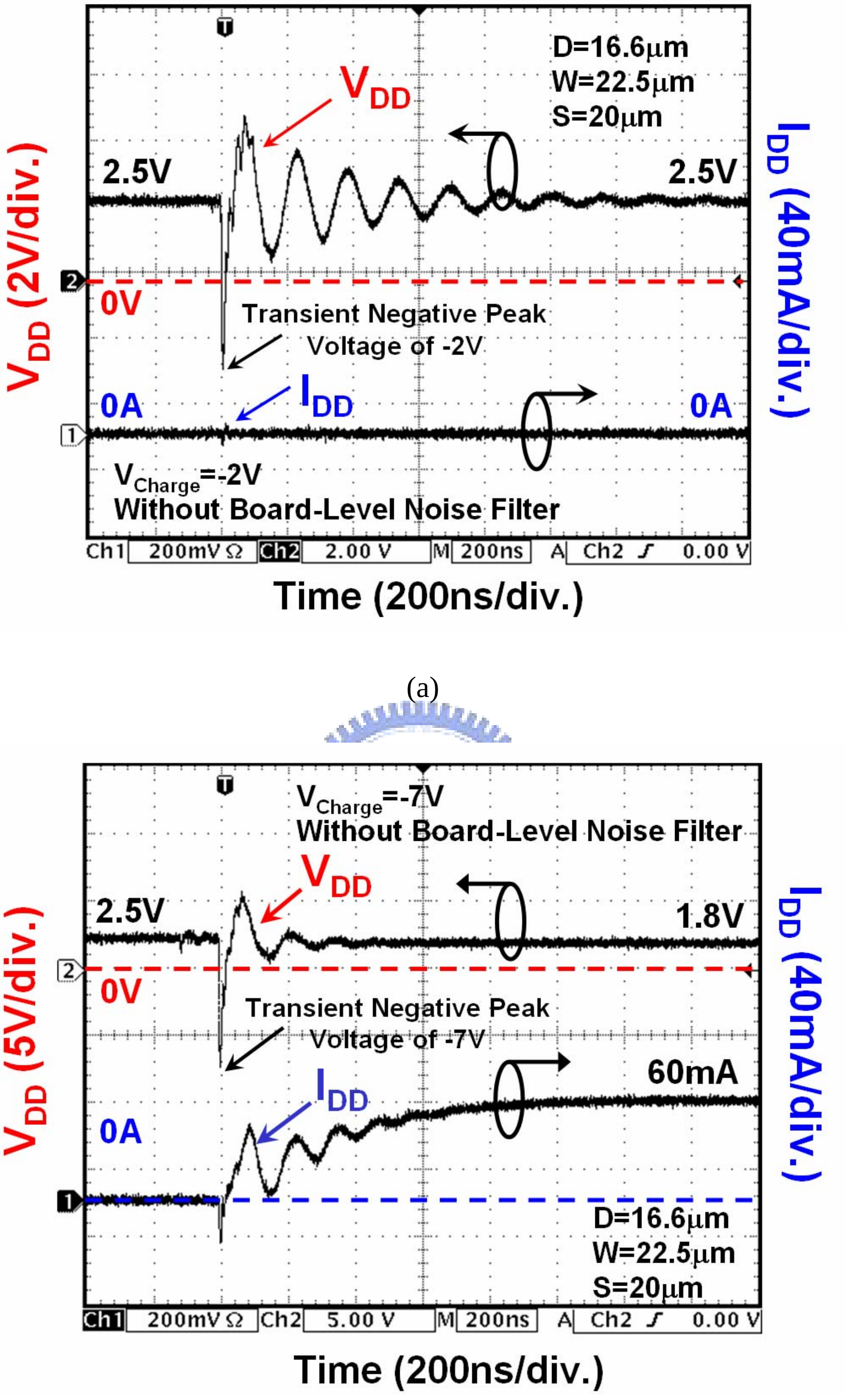


Fig. 4.7 A modified component-level TLU measurement setup with bi-polar trigger [41], [42]. It can accurately simulate how a CMOS IC inside the EUT will be disturbed by the ESD-generated noises under system-level ESD test.



(a)

(b)

Fig. 4.8 Without any board-level noise filters, the measured V_{DD} and I_{DD} transient responses of the SCR with V_{Charge} of (a) -2V, and (b) -7V.

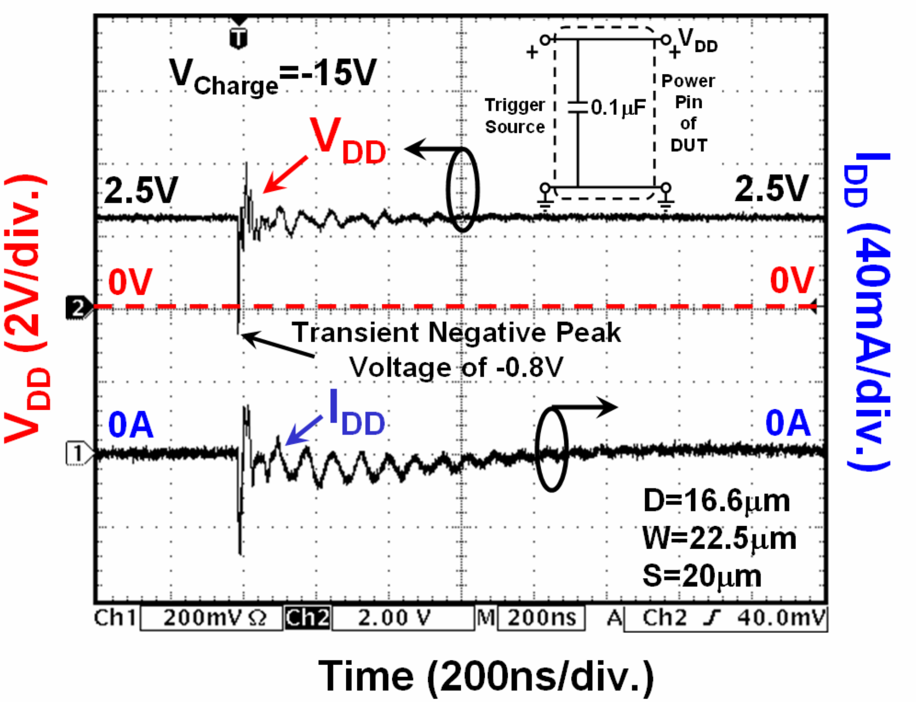
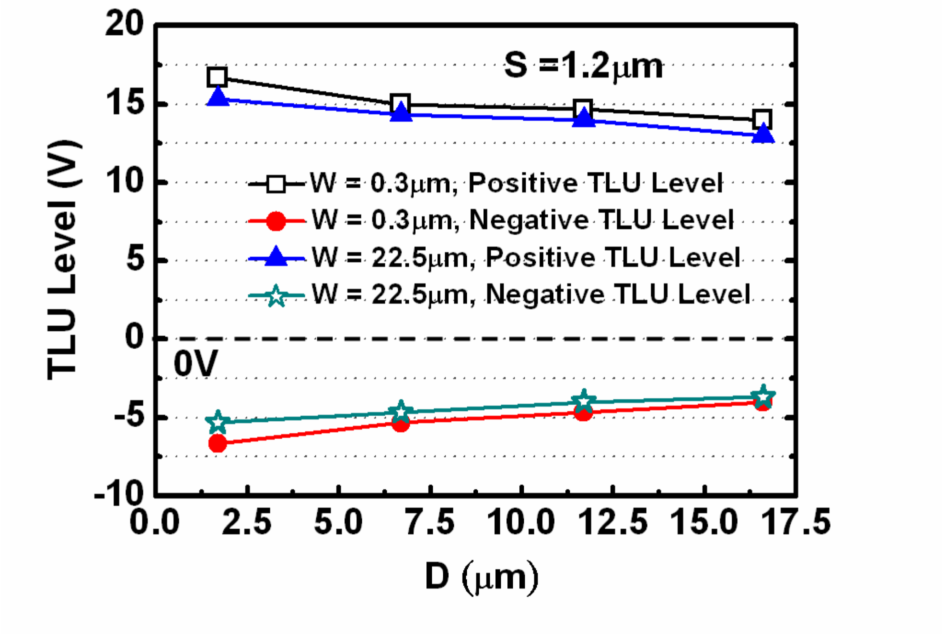
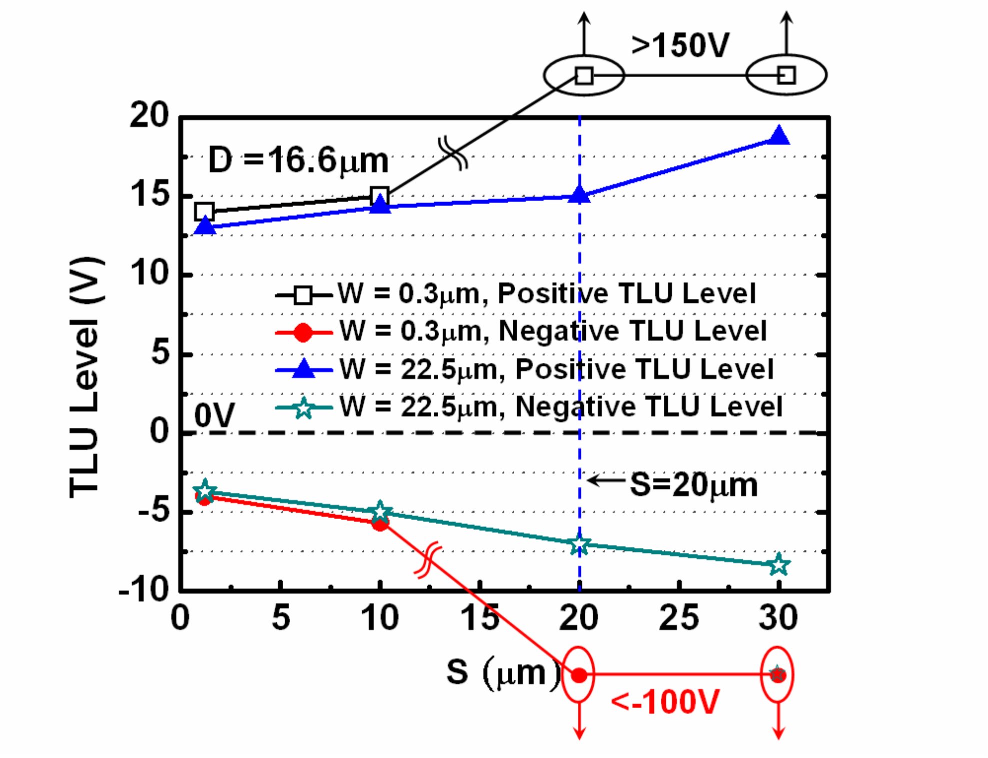


Fig. 4.9 With an additional decoupling capacitance of 0.1μF between V_{DD} and V_{SS} (ground) of the SCR, the measured V_{DD} and I_{DD} transient responses with V_{Charge} of -15V. With the help of the decoupling capacitor for suppressing the transient negative peak voltage of V_{DD} down to -0.8V, TLU will not be initiated.



(a)



(b)

Fig. 4.10 Measured TLU level of the SCR structures with (a) various D and W but a fixed S of 1.2μm, and (b) various S and W but a fixed D of 16.6μm. The SCR structures are rather susceptible to TLU for all different geometrical parameters (the magnitudes of both positive and negative TLU levels are all smaller than 18V) unless the SCR is latchup-free.

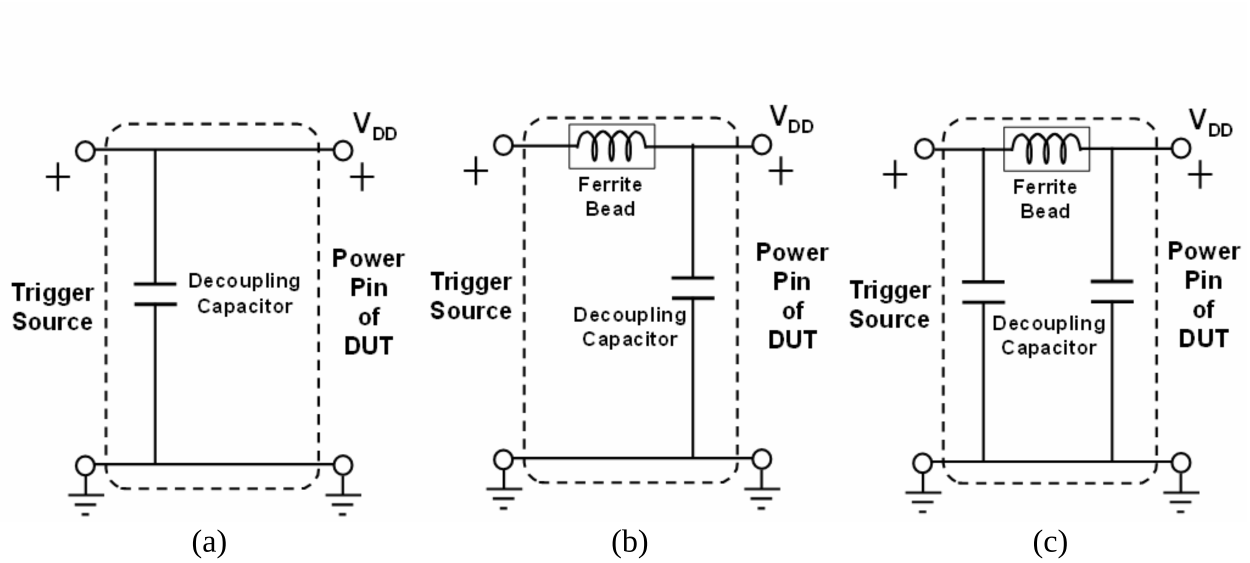


Fig. 4.11 Three types of noise filter networks investigated for their improvements on TLU level of SCR: (a) capacitor filter, (b) LC-like filter, and (c) π-section filter.

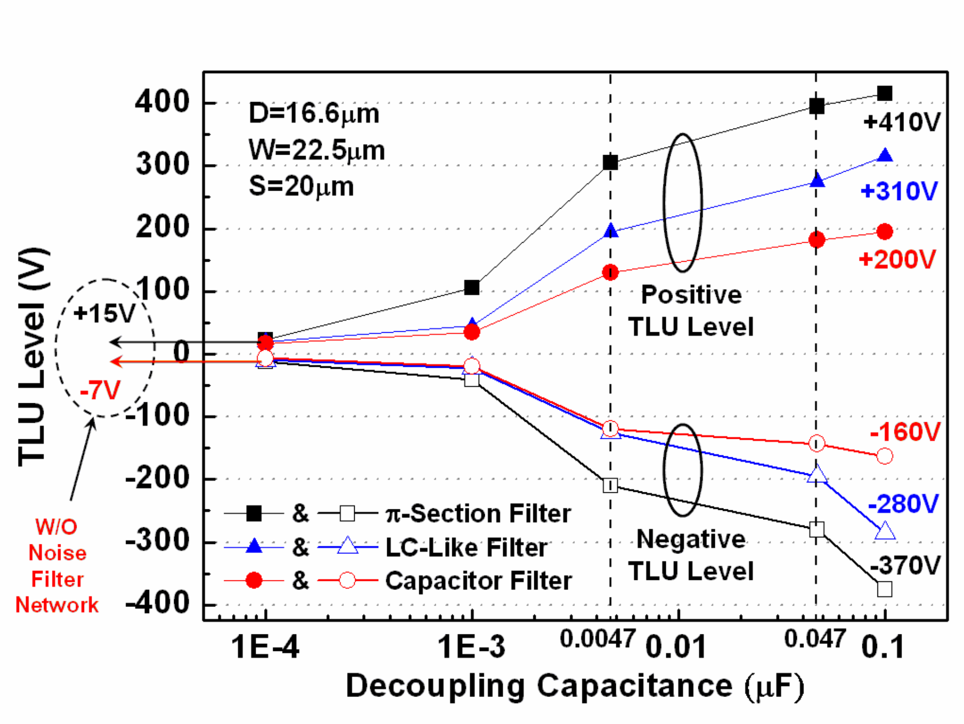


Fig. 4.12 Relations between the decoupling capacitance and the TLU level of the SCR under three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter.

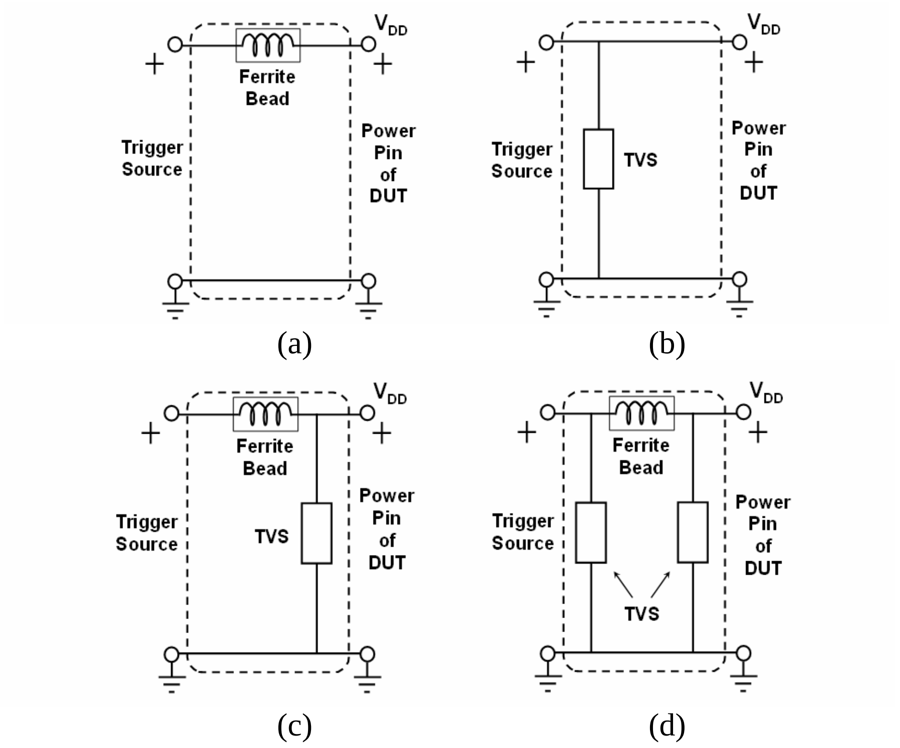


Fig. 4.13 Four other types of noise filter networks investigated for their improvements on TLU level of SCR: (a) ferrite bead, (b) TVS, (c) hybrid type I, and (d) hybrid type II.

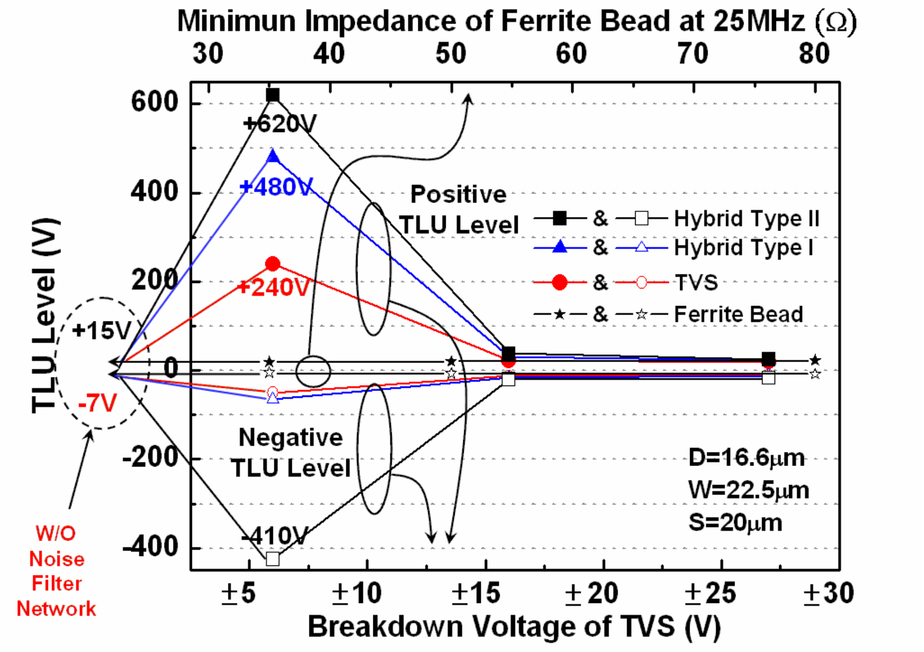
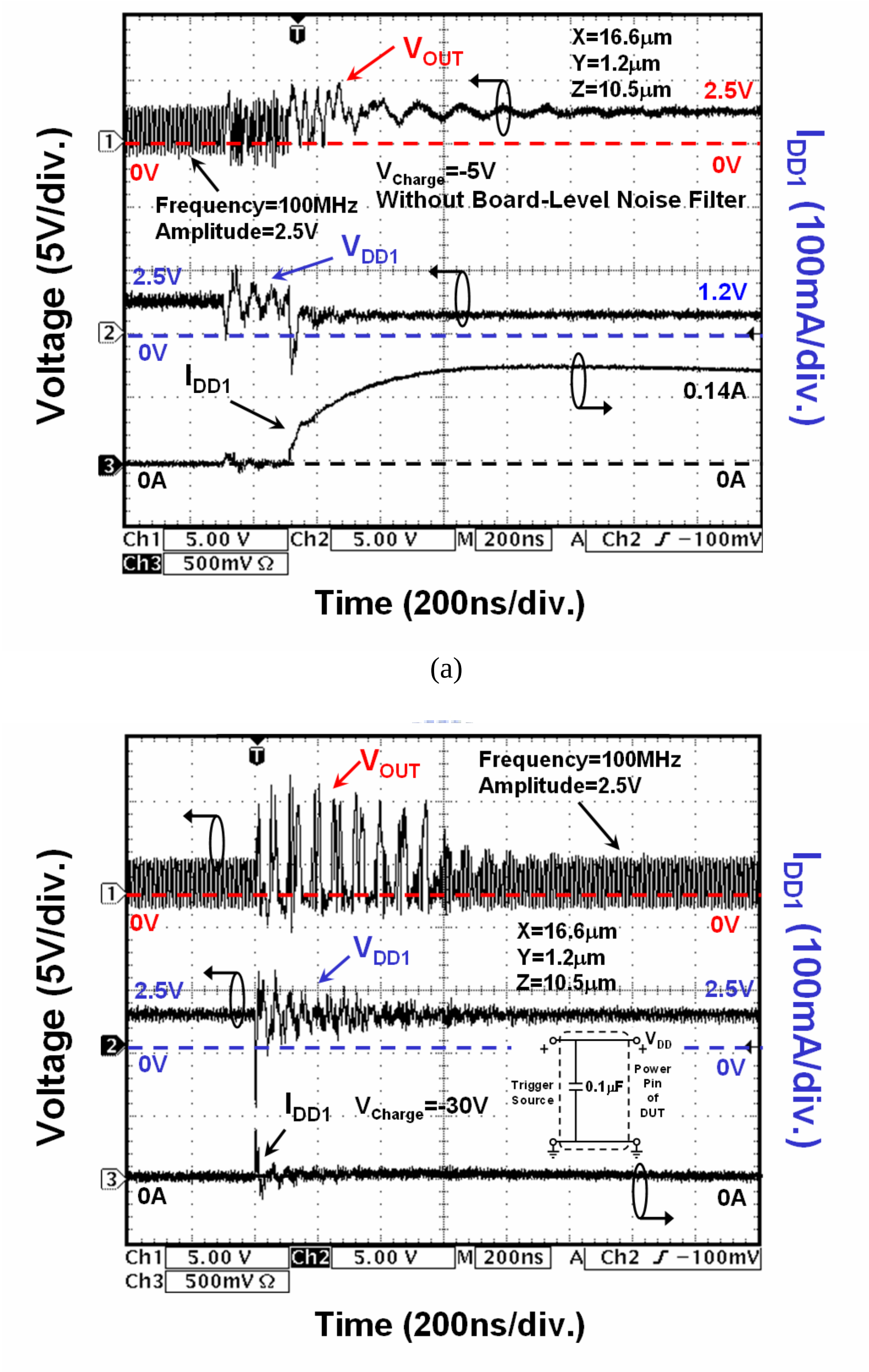


Fig. 4.14 Relations among the TLU level of SCR, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.



(a)

(b)

Fig. 4.15 Measured V_{DD1}, I_{DD1}, and V_{OUT} transient responses for the ring oscillator (a) without, and (b) with, the board-level noise filter network.

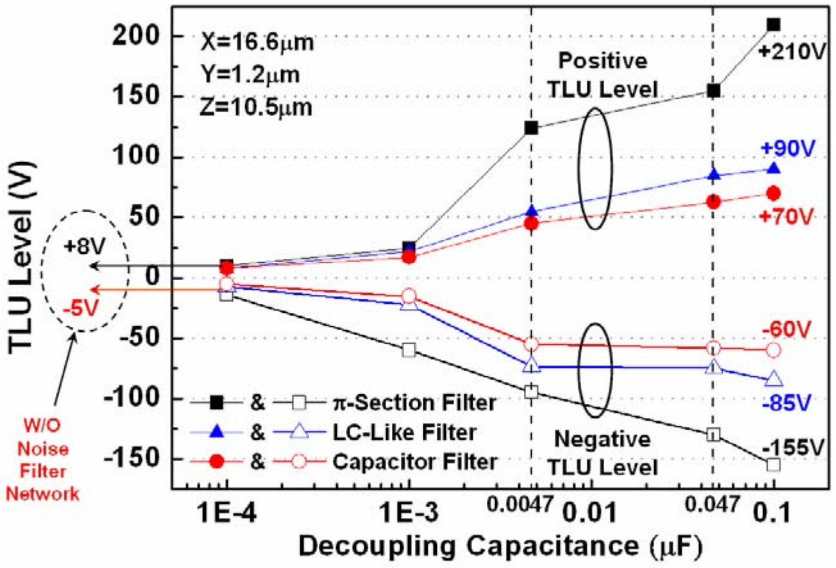


Fig. 4.16 Relations between the decoupling capacitance and the TLU level of the ring oscillator under three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter.

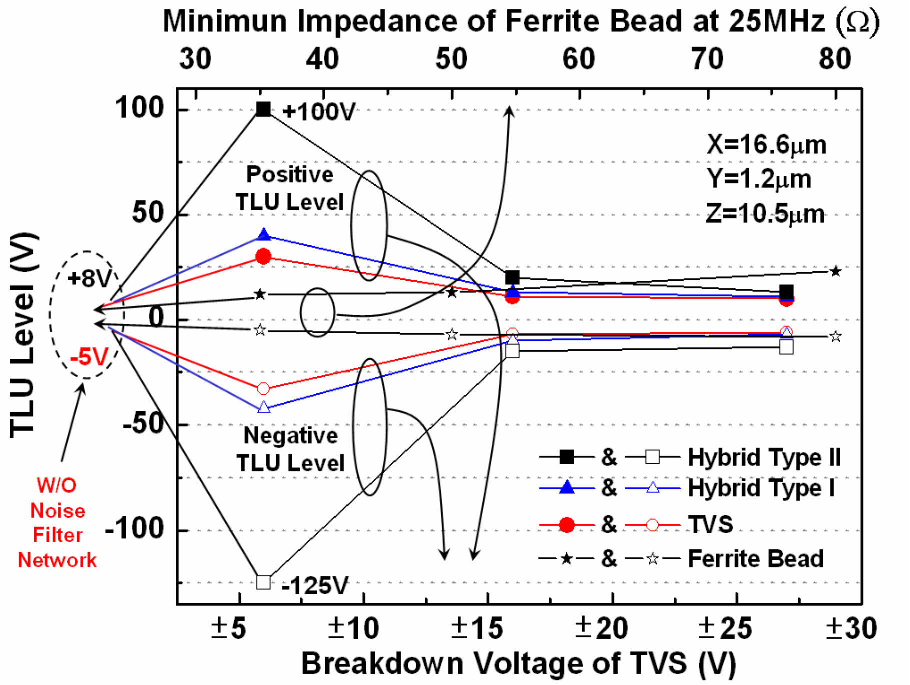


Fig. 4.17 Relations among the TLU level of the ring oscillator, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.

Chapter 5

Transient-Induced Latchup Dependency on Power-Pin Damping Frequency and Damping Factor in CMOS Integrated Circuits

The bipolar (underdamped sinusoidal) transient noises on power pins of CMOS integrated circuits (ICs) can trigger on the latchup events in CMOS ICs under system-level electrostatic discharge (ESD) test. Two dominant parameters of bipolar transient noises—damping frequency and damping factor, strongly depend on system shielding, board-level noise filter, chip-/board- level layout, etc. The transient-induced latchup (TLU) dependency on power-pin damping frequency and damping factor were characterized by device simulation and verified by experimental measurement. From the simulation results, bipolar trigger waveform with damping frequency of several tens of megahertz can trigger on TLU most easily. However, TLU is less sensitive to bipolar trigger waveform with an excessively large damping factor, an excessively high damping frequency, or an excessively low damping frequency. The simulation results have been experimentally verified with the silicon controlled rectifier (SCR) test structures fabricated in a 0.25-μm CMOS technology.

Nomenclature

D_{Freq}	Damping frequency of bipolar trigger voltage on power pins of CMOS ICs.
D_{Factor}	Damping factor of bipolar trigger voltage on power pins of CMOS ICs.
$+V_{Peak}$	Transient positive peak voltage of bipolar trigger voltage on power pins of CMOS ICs.
$+I_{Peak}$	Transient positive peak current of bipolar trigger voltage on power pins of CMOS ICs.
$-V_{Peak}$	Transient negative peak voltage of bipolar trigger voltage on power pins of CMOS ICs.
$-I_{Peak}$	Transient negative peak current of bipolar trigger voltage on power pins of CMOS ICs.
I_{Sb}	Sweep-back current caused by the bipolar trigger voltage on power pins of CMOS

	ICs.
D	Distance between well-edge and well (substrate) contact in the p-n-p-n latchup path.
S	Distance between anode and cathode in the p-n-p-n latchup path.
W	Distance between the two adjacent well (substrate) contacts in the p-n-p-n latchup path.
$V_{DD}(t)$	Time-dependent voltage function used in device simulation to simulate the bipolar trigger voltage on power pins of CMOS ICs. $V_{DD}(t)=V_0+V_P\cdot\exp\left(-(t-t_d)D_{Factor}\right)\cdot\sin\left(2\pi D_{Freq}(t-t_d)\right)$. V_0 is the initial voltage, t_d is time delay, and V_P is the applied voltage amplitude.
I_{Ds}	Transient displacement current of P/N junction.
V_{P+}	Magnitude of minimum positive V_P to initiate TLU.
V_{P-}	Magnitude of minimum negative V_P to initiate TLU.
t_P	Time period needed for V_{DD} increasing from $-V_{Peak}$ to the normal circuit operating voltage.
$D_{Freq(min)}$	Minimum D_{Freq} to initiate TLU.
$D_{Freq(max)}$	Maximum D_{Freq} to initiate TLU.
V_{Charge}	Applied voltage on charged capacitor (200pF) in component-level TLU measurement setup.
f_{SR}	Self-resonant frequency.

5.1. Background

In chapter 2, the sweep-back current, I_{Sb} [28], [29], has been proven the major cause of TLU under the system-level ESD test. Three dominant parameters to determine I_{Sb} are D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) [28], [29]. Thus, it's important to investigate the TLU dependency on D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$). In real situations, these three parameters depend on the charged voltage of ESD gun, the adopted TLU test mode, and the board-level noise-decoupling filters, etc. Furthermore, the board-level transient voltage coupled into chips also strongly depends on the parasitic capacitance, inductance, and resistance of metal traces in board-/chip- level layout. Thus, the occurrence of TLU strongly depends on these three parameters. It is straightforward that a larger voltage amplitude of $+V_{Peak}$ ($-V_{Peak}$) (i.e. larger transient noises) will initiate TLU more easily. However, so far it hasn't been investigated yet how D_{Freq} and D_{Factor} will affect the TLU immunity of the CMOS ICs under the system-level ESD test.

In this chapter, TLU dependency on both D_{Freq} and D_{Factor} will be well explained in time domain by device simulation. Based on the comprehensive simulation results, the board-level noise filters can be properly developed to efficiently eliminate the ESD-coupled noises for TLU prevention. The simulation results on TLU have been experimentally verified with silicon test chips fabricated in a 0.25-μm CMOS process.

5.2. Examples of Different D_{Freq} and D_{Factor} under System-Level ESD Test

The measurement setup of the system-level ESD test with indirect contact-discharge test mode [32] is shown in Fig. 2.2. Without board-level noise filters to help suppress ESD-induced transient noises, the measured V_{DD} transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT with ESD voltage of +1000V zapping on the HCP is shown in Fig. 5.1. During the system-level ESD test, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) depend on many factors. Specifically, the board-level noise-decoupling filter is a dominant factor to determine these parameters. To clarify this issue, a decoupling capacitance of 1nF is added between V_{DD} and V_{SS} (ground) of the CMOS IC#1. With ESD voltage of +1000V zapping on the HCP, the measured V_{DD} transient waveform is shown in Fig. 5.2. Compared with the original V_{DD} transient waveform in Fig. 5.1, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) are all different in Fig. 5.2. Furthermore, with a resistor-type ferrite bead (minimum impedance of 80Ω at 25MHz) in series with the V_{DD} pin of the CMOS IC#1, the measured V_{DD} transient waveform with ESD voltage of +1000V zapping on the HCP is shown in Fig. 5.3. Clearly, D_{Factor} is larger than that of the original V_{DD} waveform in Fig. 5.1, because the ferrite bead can absorb RF energy while the ESD-induced transient current flows through it. Without any board-level noise-decoupling filter on CMOS IC#1, the measured V_{DD} transient waveform with a higher ESD voltage of +2000V zapping on the HCP is shown in Fig. 5.4. The $+V_{Peak}$ of +30V doubles that (+15V) in Fig. 5.1 (ESD zapping voltage of +1000V), so the V_{DD} peak voltage is proportional to the ESD zapping voltage. As a result, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) could be different in each case, thus strongly dominating the occurrence of TLU under the system-level ESD test.

To clarify this issue, with ESD voltage of +3000V zapping on the HCP, the measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 are shown in Fig. 5.5. With a large transient peak voltage of ±50V, TLU is triggered on with instantaneously increasing I_{DD}.

After the ESD-induced disturbance on V_{DD}, I_{DD} is kept at a high current of 80mA, while V_{DD} is pulled down to the latchup holding voltage of 1.8V. If an additional decoupling capacitance of 0.1μF is added between V_{DD} and V_{SS} (ground) of this TLU-sensitive CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with ESD voltage of +3000V zapping on the HCP are shown in Fig. 5.6. Compared with the V_{DD} waveforms in Fig. 5.5 where no decoupling capacitance is used for suppressing the ESD-induced noise, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) are all different in Fig. 5.6. As a result, TLU does not occur, and I_{DD} doesn't increase after the ESD-induced disturbance on V_{DD}. Thus, the occurrence of TLU strongly depends on D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) of bipolar trigger waveforms on power pins of CMOS ICs. The board-level noise filters dominate these parameters, which have strong impacts to TLU.

5.3. TLU Simulation

A two-dimensional device simulation tool (MEDICI) is used to characterize the TLU dependency on both D_{Freq} and D_{Factor}. The SCR structure with the specified layout parameters of D=6.7μm and S=1.2μm is used for all the TLU device simulations in this chapter, as shown in Fig. 2.6.

5.3.1. Relations between D_{Factor} and Minimum Positive (Negative) V_P to Initiate TLU

With a fixed D_{Freq} of 8MHz, the relations between D_{Factor} and V_{P+} (V_{P-}) are shown in Fig. 5.7(a). V_{P+} (V_{P-}) is defined as the magnitude of minimum positive (negative) V_P to initiate TLU. TLU cannot be initiated if the magnitude of the applied positive (negative) V_P is smaller than V_{P+} (V_{P-}), because a too small V_P cannot provide a large enough $-V_{Peak}$ (i.e. large enough I_{Sb}) to initiate TLU. In addition, because D_{Factor} determines how fast the bipolar trigger voltage will be attenuated in time domain, so the magnitude of $-V_{Peak}$ strongly depends on D_{Factor}. For example, larger D_{Factor} causes larger voltage attenuation within the first cycle of the bipolar trigger waveform (i.e. smaller $-V_{Peak}$ or I_{Sb}). Thus, the relations between D_{Factor} and V_{P+} (V_{P-}) are very important for TLU characterization.

For $D_{Factor}<10^4 s^{-1}$, both V_{P+} and V_{P-} are independent to D_{Factor} and equal to 6V. From (1), for the given D_{Freq} of 8MHz, such small D_{Factor} will not result in an obvious voltage attenuation within the first cycle of the bipolar trigger waveform (i.e. $-V_{Peak}$ isn't obviously attenuated). Thus, for such a small D_{Factor}, if a known minimum $-V_{Peak}$ to initiate TLU is fixed, both V_{P+} and V_{P-} are the same and independent to D_{Factor}.

For $D_{Factor}>10^4s^{-1}$, both V_{P+} and V_{P-} increase with D_{Factor}. A larger D_{Factor} will result in a larger voltage attenuation (i.e. smaller $-V_{Peak}$) within the first cycle of the bipolar trigger waveform, so a larger V_{P+} (V_{P-}) is necessary for a larger D_{Factor} to provide a known fixed $-V_{Peak}$ (i.e. fixed I_{Sb}) which can initiate TLU. Compared with the negative-going ($V_P<0$) bipolar voltage, the positive-going ($V_P>0$) bipolar voltage needs to take an additional half duration for decaying before reaching to $-V_{Peak}$. As a result, V_{P+} larger than V_{P-} is necessary to compensate this additional voltage attenuation within the half duration.

5.3.2. Relations between D_{Freq} and Minimum Positive (Negative) V_P to Initiate TLU

With a fixed D_{Factor} of $1.5\times10^6s^{-1}$, the relations between D_{Freq} and V_{P+} (V_{P-}) are shown in Fig. 5.7(b). D_{Freq} is inversely proportional to the duration of bipolar trigger waveform. Thus, D_{Freq} determines how fast the bipolar trigger waveform will be attenuated within its first duration (cycle). For example, for a fixed V_P and D_{Factor}, higher D_{Freq} (shorter duration) means that bipolar trigger voltage takes less time for decaying before reaching to $-V_{Peak}$ (i.e. larger $-V_{Peak}$). Thus, $-V_{Peak}$ (I_{Sb}) strongly depends on D_{Freq}, and the relations between D_{Freq} and V_{P+} (V_{P-}) are significant for TLU characterization.

For 0.8MHz<D_{Freq}<100MHz, V_{P+} is larger than V_{P-} because the positive-going bipolar voltage must take an additional half duration for decaying before reaching to $-V_{Peak}$. Thus, if the minimum $-V_{Peak}$ to initiate TLU is fixed, V_{P+} larger than V_{P-} is needed to compensate the additional voltage attenuation within the half duration.

For D_{Freq}<0.8MHz, however, V_{P+} is smaller than V_{P-}. For V_{P-} case, Fig. 5.8 shows the simulated V_{DD} and I_{DD} transient responses for bipolar trigger with D_{Factor}, D_{Freq}, and V_P of $1.5\times10^6s^{-1}$, 0.1MHz, and -200V, respectively. Clearly, the given D_{Factor} of $1.5\times10^6s^{-1}$ is too large for such a low-frequency bipolar trigger to perform a negative-going bipolar voltage, but a negative-going unipolar overdamped voltage instead. TLU doesn't occur because t_P is too long (~3μs) to generate sufficient I_{Sb} [28], [29], even though the magnitude of $-V_{Peak}$ is as high as 28V. For V_{P+} case, Fig. 5.9 shows the simulated V_{DD} and I_{DD} transient responses for bipolar trigger with the same parameters as those in Fig. 5.8 but with V_P of +150V. Similarly, a positive-going unipolar overdamped voltage is formed due to the given large D_{Factor}. However, TLU could be initiated by the I_{Ds} while V_{DD} initially increases from the normal operating voltage (+2.5V) to $+V_{Peak}$, even though the magnitudes of both V_P and $+V_{Peak}$

(150V and 25V) are smaller than those (200V and 28V) in Fig. 5.8. Two different TLU-triggering currents have been mentioned: I_{Ds} [3], [4] and I_{Sb} [28], [29]. I_{Ds} results from a rapid increase of V_{DD} with time (e.g. power-on transition or V_{DD} overshooting), and it's proportional to the junction capacitance. I_{Sb} results from V_{DD} switching from negative voltage level to positive voltage level (e.g. bipolar transient noises on V_{DD}), and it correlates closely with D_{Freq}, D_{Factor}, and $-V_{Peak}$. It has been clarified that I_{Sb} can initiate TLU more easily than I_{Ds} [46]. From the simulation results in Figs. 5.8 and 5.9, however, I_{Ds} (Fig. 5.9) can initiate TLU more easily than I_{Sb} (Fig. 5.8) due to a very low D_{Freq}. A too low D_{Freq} will significantly reduce I_{Sb} because of a too long t_P (e.g. 3μs in Fig. 5.8) [28], [29].

For D_{Freq}>1000MHz, both V_{P+} and V_{P-} significantly increase, as shown in Fig. 5.7(b). Fig. 5.10 shows the simulated V_{DD} and I_{DD} transient responses for bipolar trigger with D_{Factor}, D_{Freq}, and V_P of $1.5\times10^6 s^{-1}$, 2GHz, and -60V, respectively. Clearly, $+I_{Peak}$ doesn't simultaneously appear with $+V_{Peak}$ but at the end of the first duration (~50.5ns), because I_{DD} cannot follow the V_{DD} variation in time for such a high-D_{Freq} (>1GHz) bipolar trigger. Thus, $+I_{Peak}$ of 0.3A is smaller than that (0.75A) under low-D_{Freq} (20MHz) case in Fig. 2.13, even though $+V_{Peak}$ of +60V is much larger than that (+7.5V) in Fig. 2.13. This means that larger V_{P+} or V_{P-} is necessary for such a high-D_{Freq} (>1GHz) bipolar trigger to provide a fixed I_{Sb} which can initiate TLU. If D_{Freq} further increases to above 3GHz, TLU doesn't occur (both V_{P+} and V_{P-} larger than 1000V), because the duration of bipolar trigger isn't long enough to sustain a positive-feedback latchup event [15].

5.3.3. Relations between D_{Factor} and Minimum (Maximum) D_{Freq} to Initiate TLU

With a fixed V_P of both +15V and -15V, the relations between D_{Factor} and $D_{Freq(min)}$ ($D_{Freq(max)}$) are shown in Fig. 5.11(a) (Fig. 5.11(b)). $D_{Freq(min)}$ ($D_{Freq(max)}$) is defined as the minimum (maximum) D_{Freq} to initiate TLU under a fixed V_P of +15V or -15V. Bipolar trigger with $D_{Freq}<D_{Freq(min)}$ ($D_{Freq}>D_{Freq(max)}$) cannot trigger on TLU due to insufficient I_{Sb}. For D_{Freq} lower than $D_{Freq(min)}$, there is a too serious voltage attenuation on $-V_{Peak}$ (or a too long t_P) to produce sufficient I_{Sb} for initiating TLU. For D_{Freq} higher than $D_{Freq(max)}$, I_{DD} cannot follow the V_{DD} variation in time to generate enough I_{Sb} for initiating TLU.

For $D_{Factor}<2\times10^3 s^{-1}$ ($1\times10^5 s^{-1}$), $D_{Freq(min)}$ ($D_{Freq(max)}$) is independent to D_{Factor} and equal to 500kHz (1.45GHz). For such a small D_{Factor}, there is only little voltage attenuation within the first cycle of the bipolar trigger (i.e. almost no voltage attenuation on $-V_{Peak}$). Thus, if a known minimum -V_{Peak} to initiate TLU under a low- or high-D_{Freq} situation is fixed, both V_{P+} and V_{P-} are the same and independent to D_{Factor}.

For D_{Factor}>2×10^{3}s^{-1} (1×10^{5}s^{-1}), however, $D_{Freq(min)}$ ($D_{Freq(max)}$) increases with D_{Factor}. A larger D_{Factor} will result in a larger voltage attenuation (i.e. smaller -V_{Peak}) within the first cycle of the bipolar trigger. Thus, to provide a known fixed -V_{Peak} to initiate TLU, a higher $D_{Freq(min)}$ or $D_{Freq(max)}$ (i.e. shorter duration) is necessary for a larger-D_{Factor} bipolar trigger to compensate a larger voltage attenuation. In addition, there are higher $D_{Freq(min)}$ and $D_{Freq(max)}$ under V_P of +15V. Compared with the negative-going bipolar trigger (V_P of -15V), the positive-going bipolar trigger (V_P of +15V) has a smaller -V_{Peak} (smaller I_{Sb}) because it must take an additional half duration for decaying before reaching to -V_{Peak}. Thus, a higher $D_{Freq(min)}$ or $D_{Freq(max)}$ is necessary for positive-going bipolar voltage to initiate TLU.

From the above comprehensive simulation results, bipolar trigger with D_{Freq} of several tens of megahertz can initiate TLU most easily due to the smallest V_{P+} (V_{P-}) under 10MHz<D_{Freq}<100MHz, as shown in Fig. 5.7(b). Otherwise, TLU is less sensitive to bipolar trigger with an excessively large D_{Factor} (Fig. 5.7(a)), an excessively high D_{Freq} (Fig. 5.7(b)), or an excessively low D_{Freq} (Fig. 5.7(b)).

5.4. Experimental Verification on TLU

The proposed component-level TLU measurement setup shown in Fig. 2.7 is used for TLU measurements. As the measurement results in chapter 3, this proposed TLU measurement setup has a small current-limiting resistance (5Ω) but no current-blocking diode between V_{DD} node and the power supply. It can avoid the possible EOS damage under a high-current latchup state, and can accurately evaluate the TLU immunity of DUT without overestimation. The SCR structure is used as the test structure for TLU measurements. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 2.5(a) and 2.5(b), respectively. The measured V_{DD} and I_{DD} transient responses with V_{Charge} of +10V and +14V are shown in Figs. 5.12(a) and 5.12(b), respectively. With the initial V_{DD} bias of 2.5V, the DUT (SCR) has layout parameters of D=6.7μm, S=1.2μm, and W=22.5μm. With a smaller V_{Charge} of +10V, V_{DD} is the intended bipolar trigger just similar to that under the system-level ESD test [35]. In addition, TLU doesn't occur because I_{DD} doesn't increase after applying the bipolar trigger on V_{DD}, as shown in Fig. 5.12(a). TLU still doesn't occur until V_{Charge} increases up to +14V. Once TLU is initiated, I_{DD} significantly increases up to 120mA, and V_{DD} is pulled down to the latchup holding voltage of 1.5V, as shown in Fig. 5.12(b). The measured waveforms in Fig. 5.12 can simulate the occurrence of TLU (or the voltage disturbance on V_{DD}) in Figs. 5.5 and 5.1 under the system-level ESD test. Thus, this measurement setup can be used to evaluate the TLU dependency on D_{Factor} and D_{Freq} under the system-level ESD test.

The simulation results in this chapter can be experimentally verified with the proposed TLU measurement setup. The TLU levels of the fabricated SCR devices with various geometrical parameters are shown in Fig. 4.10. The TLU level is defined as the minimum positive (negative) V_{Charge} which can initiate TLU. The magnitudes of the negative TLU level (<9V) of all the SCR structures are smaller than those of the positive TLU level (>13V), unless the SCR is initially latchup-free (i.e. latchup holdinging voltage>+2.5V). With the measured bipolar trigger waveform in Fig. 5.12(a), it can be extracted from (1) that D_{Freq} is about 8MHz (duration is about 125ns), and D_{Factor} is about $1.5\times10^{6}s^{-1}$. From the simulation results in Figs. 5.7(a) and 5.7(b), V_{P-} is smaller than V_{P+} for bipolar trigger with D_{Freq} of 8MHz and D_{Factor} of $1.5\times10^{6}s^{-1}$. Thus, the experimental verifications in Fig. 4.10 are consistent with the device simulation results in Fig. 5.7.

The simulated TLU characteristics in Figs. 5.7 and 5.11 are explained with the assumption that the minimum $-V_{Peak}$ to initiate TLU is fixed for the same SCR structure. To experimentally verify this, a discharge resistor with resistance of 1.5kΩ is placed between the relay and the V_{DD} node in the TLU measurement setup. Thus, another bipolar trigger with a higher D_{Freq} and a larger D_{Factor} can be generated. Fig. 5.13(a) shows the measured V_{DD} and I_{DD} transient responses with V_{Charge} of +120V. Compared with the measured V_{DD} waveform in Fig. 5.12(a), higher D_{Freq} of 12.5MHz (larger D_{Factor} of $1.5\times10^{7}s^{-1}$) can be extracted from (1). In addition, TLU doesn’t occur due to a larger D_{Factor}, even though V_{Charge} is as high as +120V. If V_{Charge} further increases, TLU still doesn’t occur until V_{Charge} increases up to +200V. Fig. 5.13(b) shows the measured V_{DD} and I_{DD} transient responses with V_{Charge} of +200V. In Figs. 5.12(b) and 5.13(b), the minimum $-V_{Peak}$ to initiate TLU is fixed (-2.5V) for the same SCR structure (D=6.7μm, S=1.2μm, and W=22.5μm), even though there are different D_{Freq} and D_{Factor}. Based on this result, the simulated TLU characteristics in this chapter are indeed explained well with a reasonable assumption.

The simulated TLU characteristics in Fig. 5.7(a) that V_{P+} increases with D_{Factor}, can be also experimentally verified by Figs. 5.12(b) and 5.13(b). For the bipolar trigger with a larger D_{Factor} in Fig. 5.13(b), in order to compensate larger voltage attenuation within the first cycle, a larger V_{Charge} (+200V) is necessary to produce the same minimum $-V_{Peak}$ (-2.5V) to initiate

TLU. As a result, the positive TLU level of +200V in Fig. 5.13(b) is much larger than that of +14V in Fig. 5.19(b), which is consistent with the simulation result in Fig. 5.7(a).

The typical TLU-sensitive D_{Freq} and D_{Factor} under the real system-level ESD-induced bipolar noise are 25MHz and $3.2\times10^6 s^{-1}$, respectively, as shown in Fig. 5.1. To further verify the relations between TLU immunity and D_{Freq}/D_{Factor}, more TLU cases considering wide ranges of D_{Freq}/D_{Factor} should be investigated in detail under the system-level ESD test.

5.5. Suggested Guidelines for TLU Prevention

To prevent the occurrence of TLU in CMOS ICs under the system-level ESD test, the most intuitional solution is to eliminate the ESD-coupled noises on the power lines of CMOS ICs. Usually, board-level noise filter is a common and efficient solution to decouple or bypass ESD-induced noises. Based on the comprehensive simulation results in this chapter, the board-level noise filters can be properly developed to efficiently eliminate the ESD-coupled noises for TLU prevention.

Fig. 5.7(a) shows that increasing the D_{Factor} can enhance the TLU immunity of CMOS ICs. To achieve a larger D_{Factor}, board-level noise filter with higher insertion loss is necessary. Without any board-level noise filter (with a decoupling capacitance of 0.1μF between V_{DD} and ground lines) on SCR under the layout parameters of D=16.6μm, S=20μm, and W=22.5μm, the measured V_{DD} and I_{DD} transient responses with V_{Charge} of -7V (-15V) are shown in Fig. 4.8(b) (Fig. 4.9). Without any board-level noise filter, TLU occurs even if the V_{Charge} is as small as -7V. With a decoupling capacitance, TLU doesn't occur due to a larger D_{Factor}, even though the V_{Charge} is as high as -15V. However, an actual decoupling capacitor remains capacitive only up to its self-resonant frequency (f_{SR}) [48]. Above f_{SR}, the impedance of decoupling capacitance will increase with frequency (i.e. inductive impedance characteristic). Thus, continually increasing the decoupling capacitance cannot efficiently enhance the TLU level of CMOS ICs, because f_{SR} is inversely proportional to decoupling capacitance [48]. From Fig. 5.7(b), CMOS ICs are most sensitive to TLU under frequency range of $10MHz<D_{Freq}<100MHz$. Thus, a trade-off between a high insertion loss (decoupling capacitance is as large as possible) and a self-resonant frequency>100MHz (decoupling capacitance is as small as possible) is necessary to achieve the optimal decoupling capacitance for TLU prevention. For example, the relations between the decoupling capacitance and the TLU level of SCR are shown in Fig. 5.14 [49], [50]. When the decoupling capacitance increases from 100pF (f_{SR} of ~150MHz [48]) to 4.7nF (f_{SR} of

~32MHz [48]), TLU level will significantly increase with decoupling capacitance (insertion loss dominant). However, if decoupling capacitance further increases from 4.7nF (f_{SR} of ~32MHz [48]) to 0.1μF (f_{SR} of ~5MHz [48]), TLU level doesn't increase as significantly as that equipped with decoupling capacitance<4.7nF (f_{SR} dominant). A too large decoupling capacitance cannot efficiently eliminate the TLU-sensitive harmonics (10MHz<D_{Freq}<100MHz) due to a very low f_{SR}. Although the largest decoupling capacitance (0.1μF) provides the highest TLU level (+200V, -160V), the optimal decoupling capacitance to enhance TLU level is a smaller value of ~4.7nF. Thus, instead of continuously increasing the decoupling capacitance of 1st-order capacitor filter, it's suggested to use higher-order noise filters (e.g. 3rd-order π-section filter [49], [50]) based on the optimal decoupling capacitance (~4.7nF) to further enhance TLU level (>+200V).

From the simulated TLU dependency on D_{Freq} and D_{Factor}, an optimal on-chip decoupling capacitance can be estimated to efficiently enhance the TLU immunity of CMOS ICs. Based on the optimal decoupling capacitance, chip-level noise filters could be well designed for TLU prevention. Additionally, by combing the board-level noise filters with system-level solutions (e.g. shielding) and chip-level noise filters (e.g. on-chip decoupling capacitor), the ESD-coupled noises can be further eliminated to enhance the TLU immunity of CMOS ICs.

5.6. Conclusion

To clarify the correlations between TLU and the bipolar trigger noises, two dominant parameters of bipolar trigger—D_{Freq} and D_{Factor}, have been characterized to find their impacts to TLU. With the simulated TLU dependency on D_{Freq} and D_{Factor}, the bipolar trigger waveform with D_{Freq} of several tens of megahertz can initiate TLU most easily. However, TLU is less sensitive to bipolar trigger waveforms with an excessively large D_{Factor}, an excessively high D_{Freq}, or an excessively low D_{Freq}. The simulated TLU characteristics are useful for optimizing a bipolar trigger to evaluate the TLU immunity of CMOS ICs without overestimation. Furthermore, the board-/chip- level noise filters can be properly designed to efficiently eliminate the ESD-coupled noises for TLU prevention. The simulation results in this chapter have been practically verified with the SCR structures fabricated in a 0.25-μm CMOS technology.

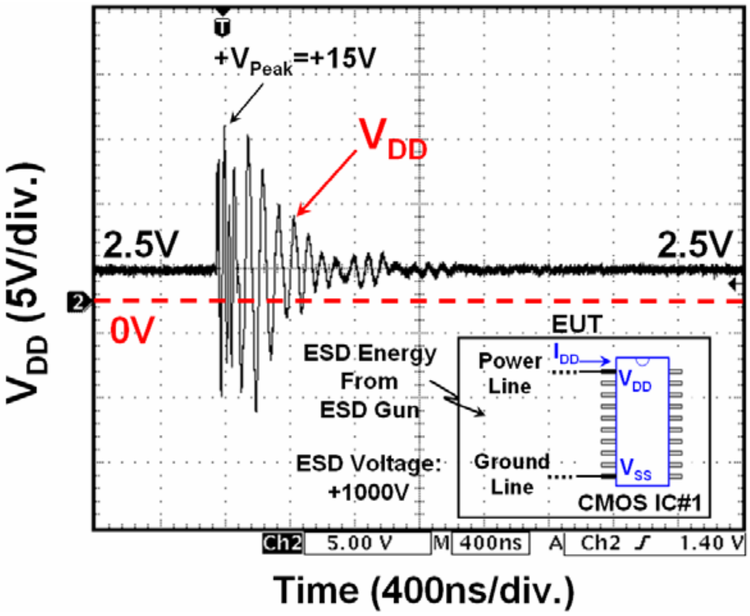


Fig. 5.1 With ESD voltage of +1000V zapping on the HCP, the measured V_{DD} transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT. V_{DD} waveform is a bipolar voltage due to the disturbance of high ESD-coupled energy.

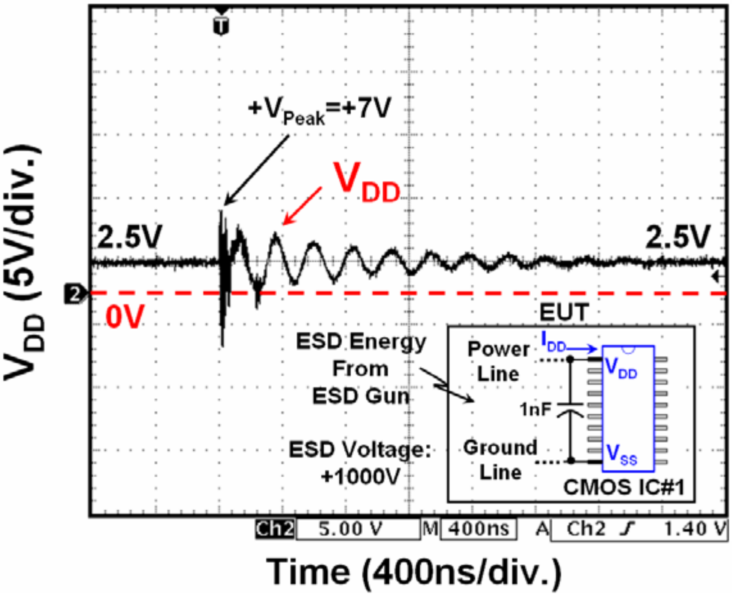


Fig. 5.2 With an additional decoupling capacitance of 1nF between V_{DD} and V_{SS} (ground) of the CMOS IC#1, the measured V_{DD} transient waveform with ESD voltage of +1000V zapping on the HCP. Compared with the original V_{DD} transient waveform in Fig. 5.1, D_{Freq}, D_{Factor}, and $+V_{Peak}$ are all different.

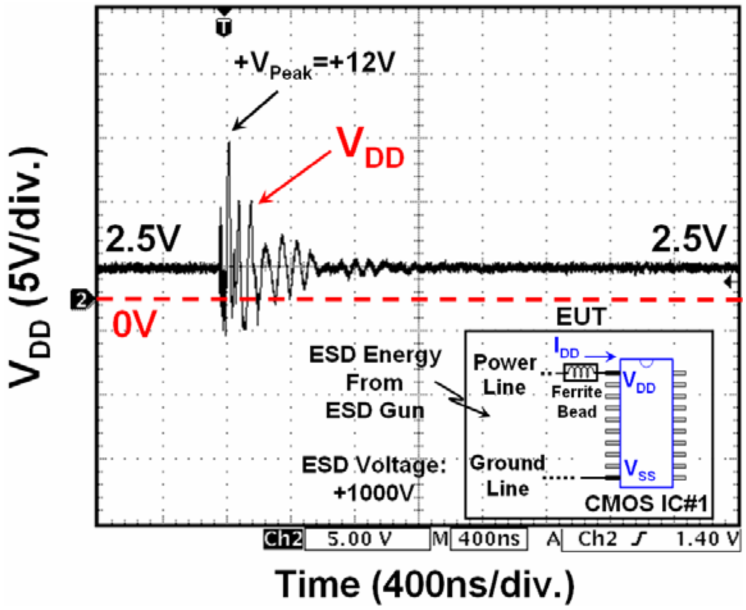


Fig. 5.3 With a resistor-type ferrite bead (minimum impedance of 80Ω at 25MHz) in series with the V_{DD} pin of the CMOS IC#1, the measured V_{DD} transient waveform with ESD voltage of +1000V zapping on the HCP. D_{Factor} is larger than that of the original V_{DD} waveform in Fig. 5.1.

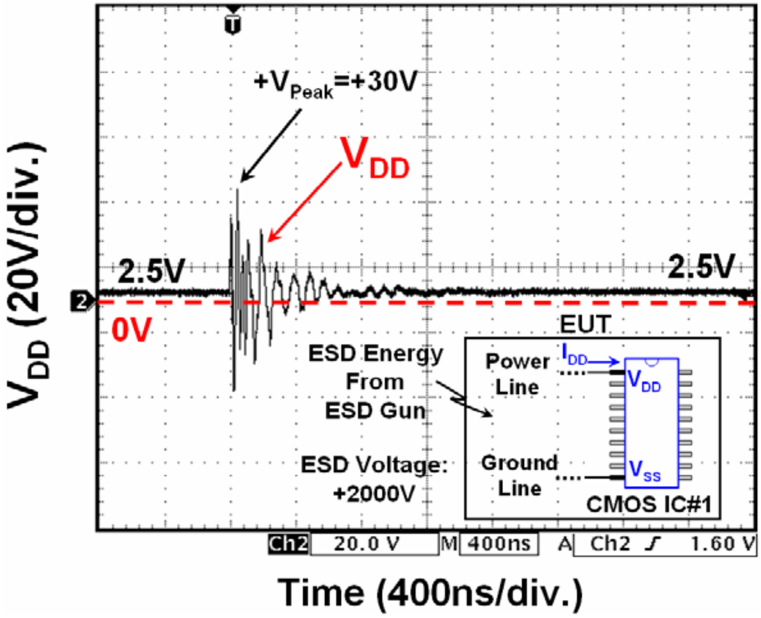


Fig. 5.4 Without any board-level noise-decoupling filter on CMOS IC#1, the measured V_{DD} transient waveform with a higher ESD voltage of +2000V zapping on the HCP. The $+V_{Peak}$ of +30V doubles that (+15V) in Fig. 5.1 with a smaller ESD voltage of +1000V.

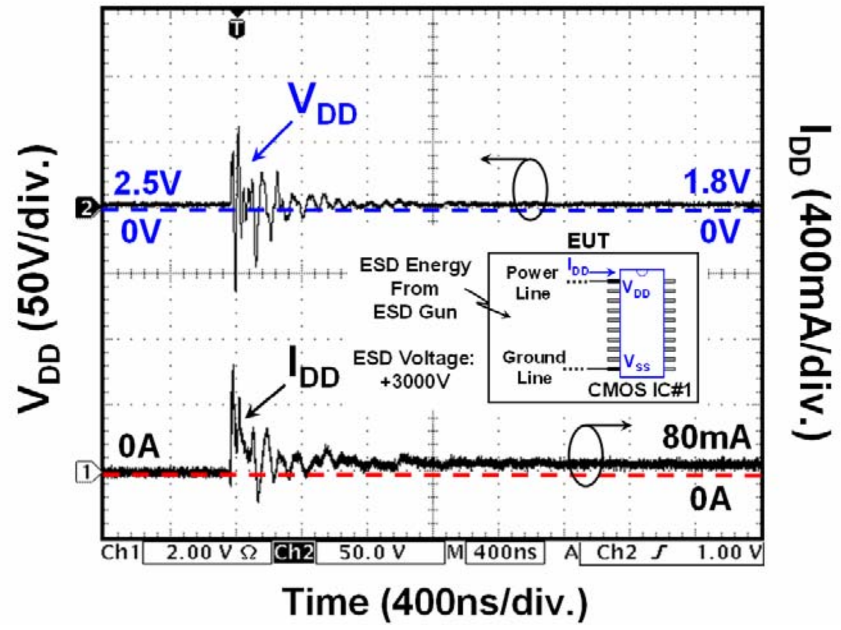


Fig. 5.5 Measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 with ESD voltage of +3000V zapping on the HCP. With a large transient peak voltage of ±50V, TLU is triggered on (I_{DD} is kept at a high current of 80mA) after the ESD-induced disturbance on V_{DD}.

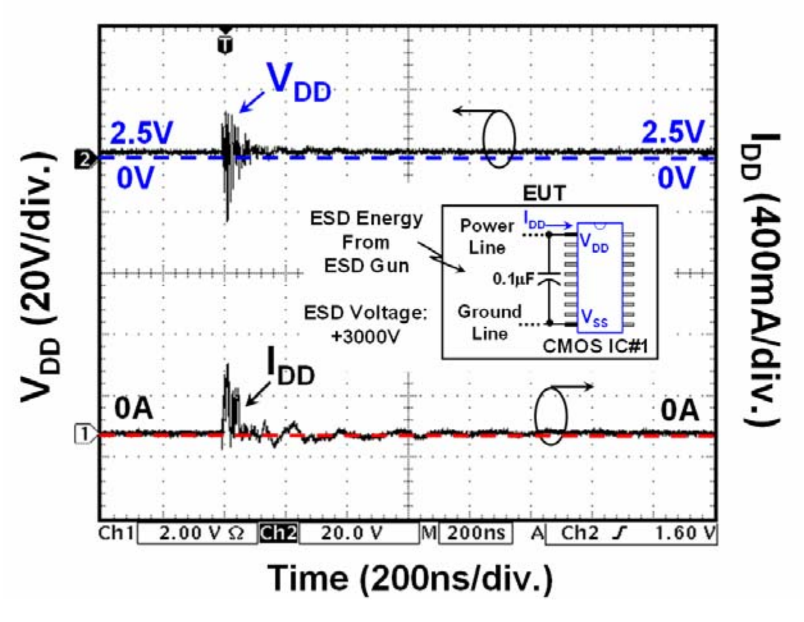
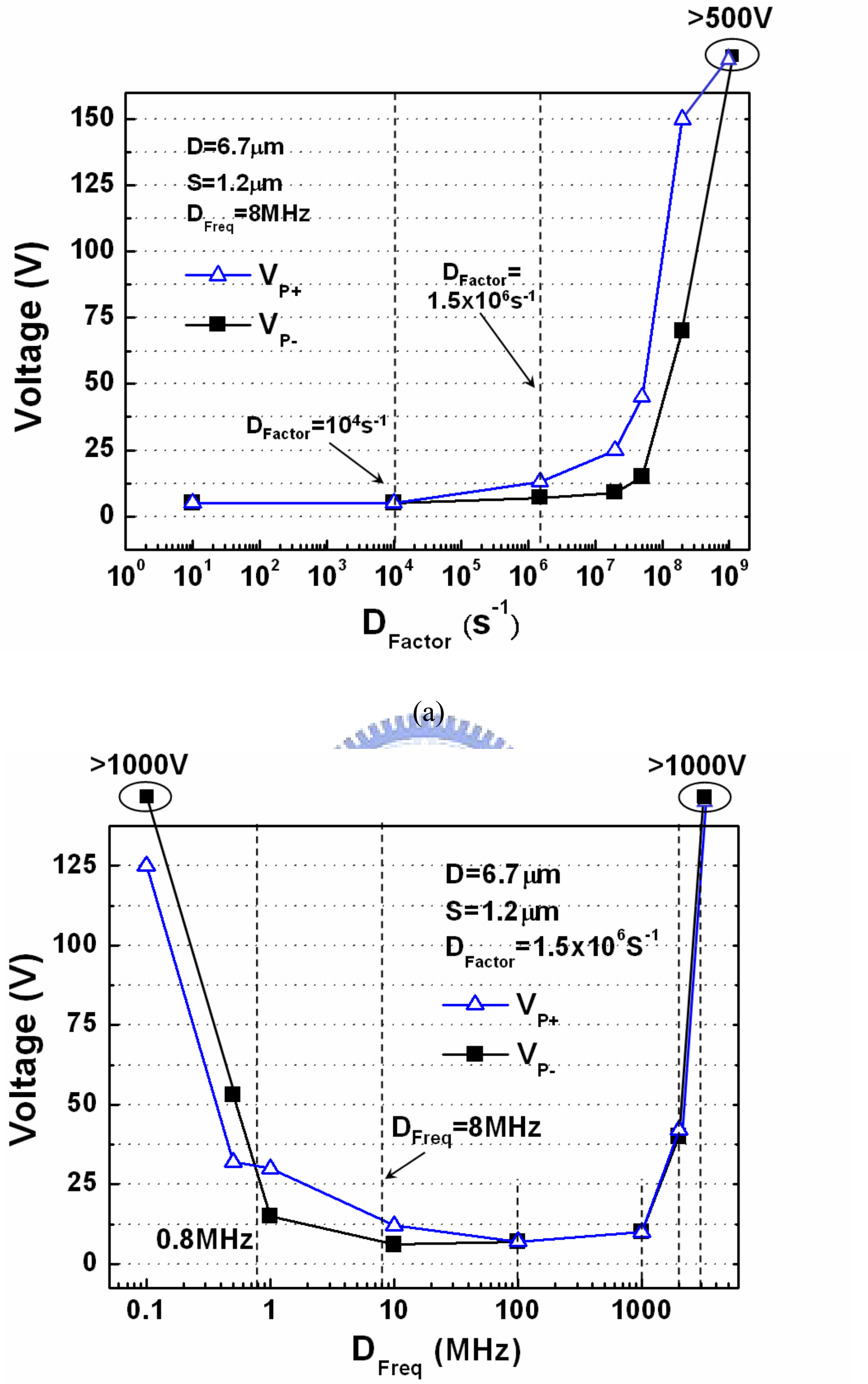


Fig. 5.6 With the decoupling capacitance of 0.1μF between V_{DD} and V_{SS} of the CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with ESD voltage of +3000V zapping on the HCP. TLU does not occur due to different D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$).



(a)

(b)

Fig. 5.7 Relations between (a) D_{Factor} and V_{P+} (V_{P-}), and (b) D_{Freq} and V_{P+} (V_{P-}). V_{P+} (V_{P-}) is defined as the magnitude of minimum positive (negative) V_P to initiate TLU.

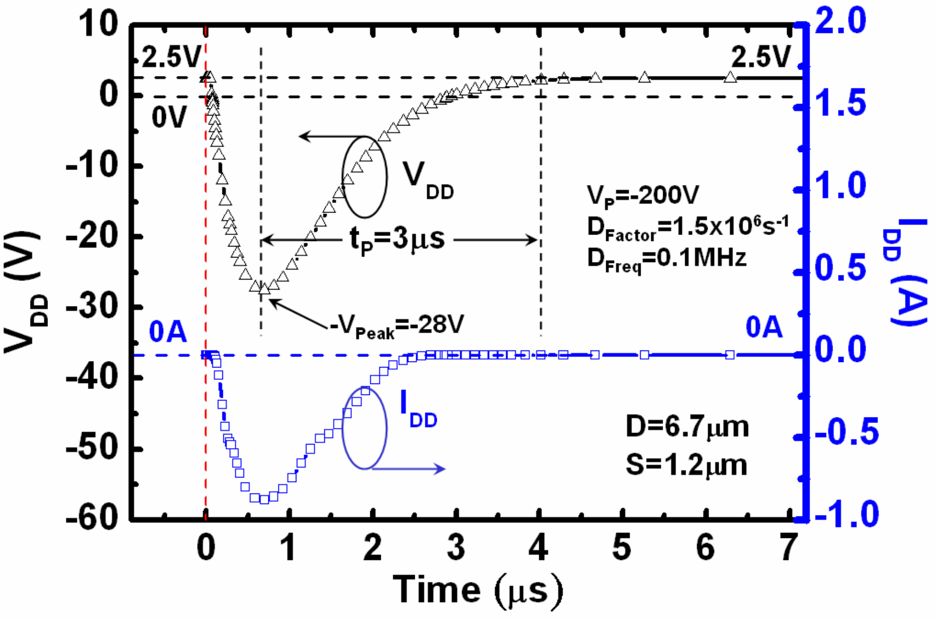


Fig. 5.8 Simulated V_{DD} and I_{DD} transient responses for bipolar trigger voltage with D_{Factor}, D_{Freq}, and V_P of $1.5\times10^6 s^{-1}$, 0.1MHz, and -200V, respectively. TLU doesn't occur because t_P is too long (~3μs) to generate sufficient I_{Sb} [28], [29].

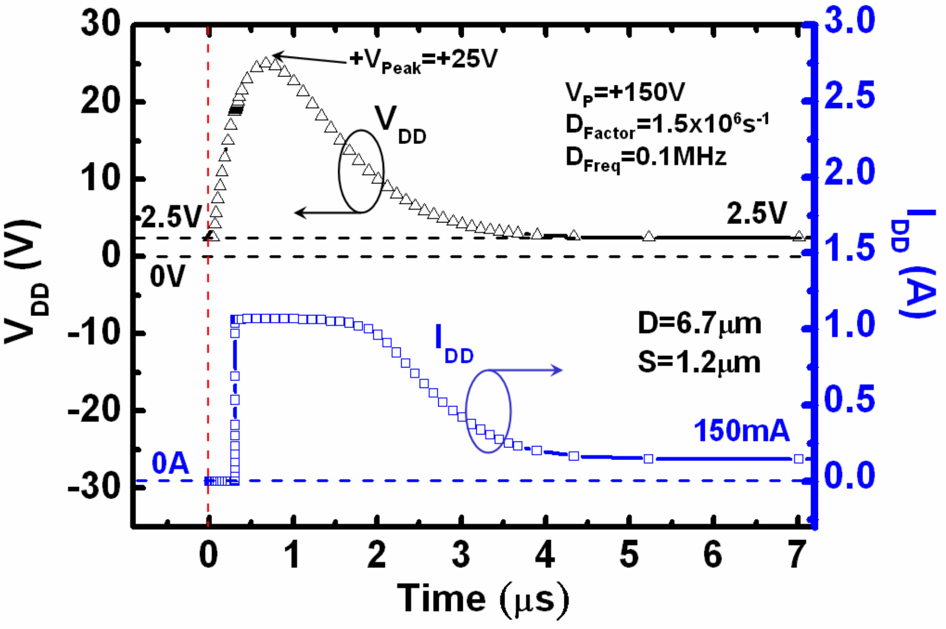


Fig. 5.9 Simulated V_{DD} and I_{DD} transient responses for bipolar trigger voltage with the same parameters as those in Fig. 5.8 but with V_P of +150V. TLU can be triggered on by I_{Ds} while V_{DD} initially increases from the normal operating voltage (+2.5V) to $+V_{Peak}$.

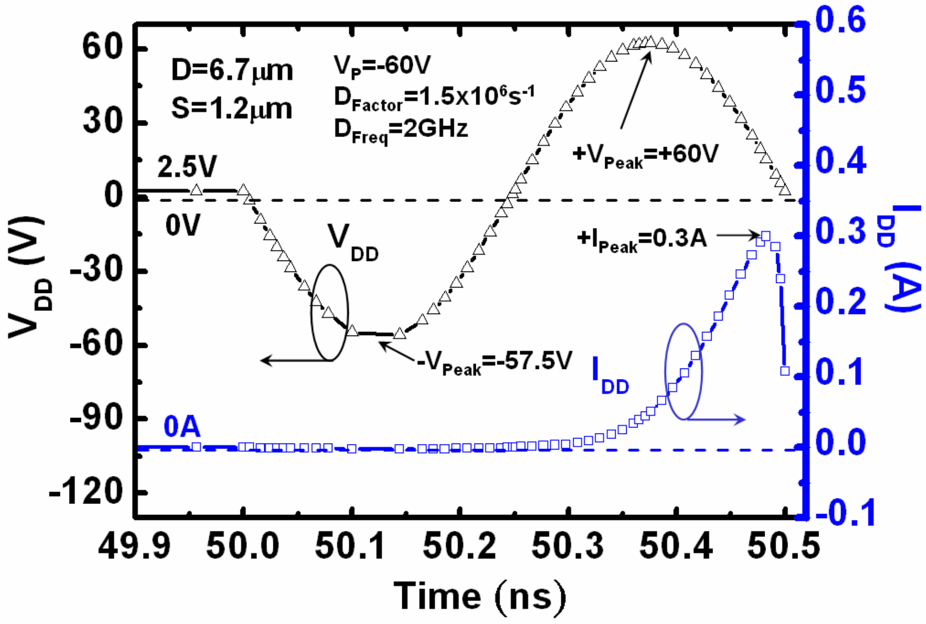
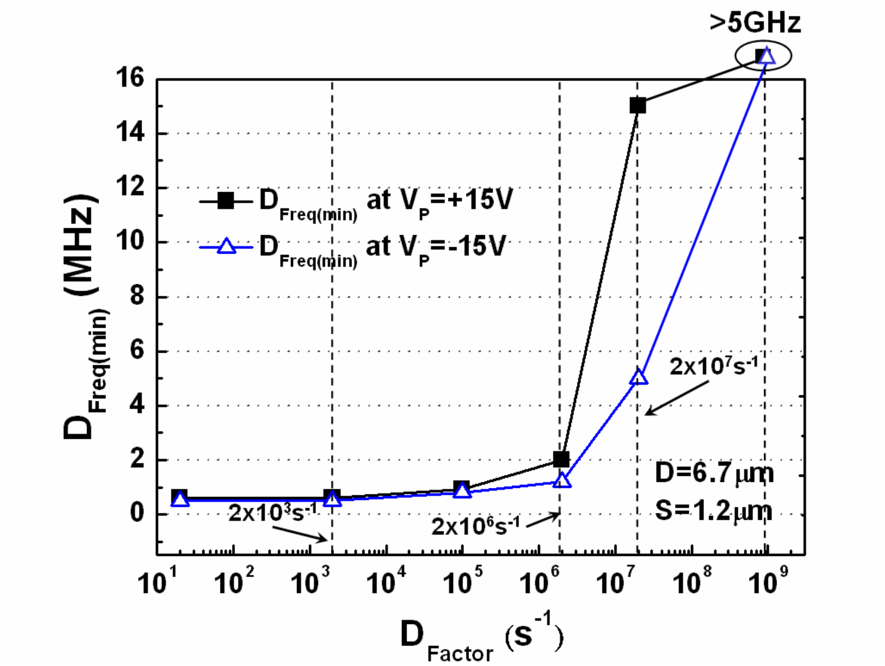
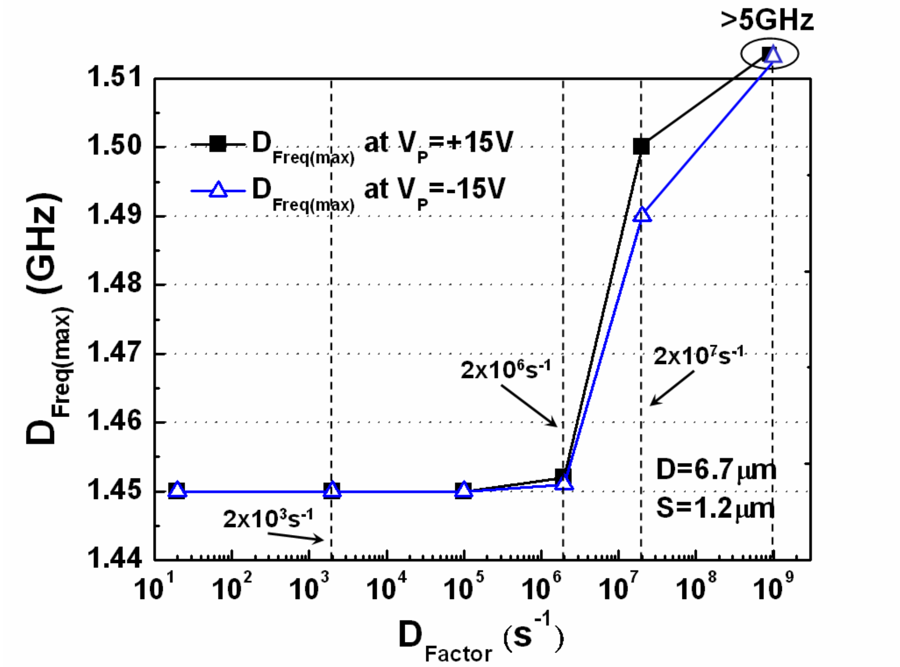


Fig. 5.10 Simulated V_{DD} and I_{DD} transient responses for bipolar trigger voltage with D_{Factor}, D_{Freq}, and V_P of $1.5\times10^6 s^{-1}$, 2GHz, and -60V, respectively. I_{DD} cannot follow the V_{DD} variation in time for such a high-D_{Freq} (>1GHz) bipolar trigger, because $+I_{Peak}$ doesn't simultaneously appear with $+V_{Peak}$ but at the end of the first duration (~50.5ns).

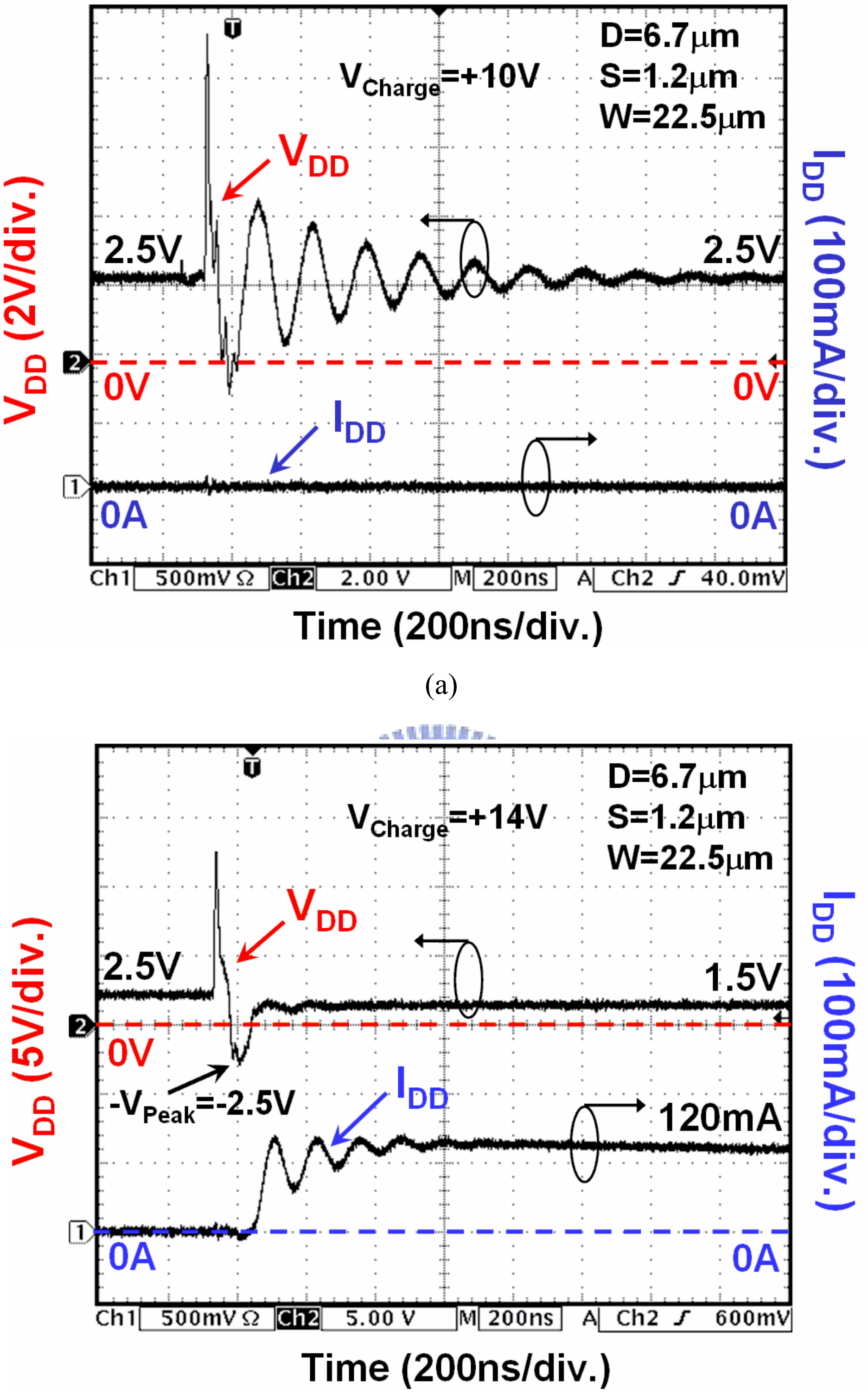


(a)



(b)

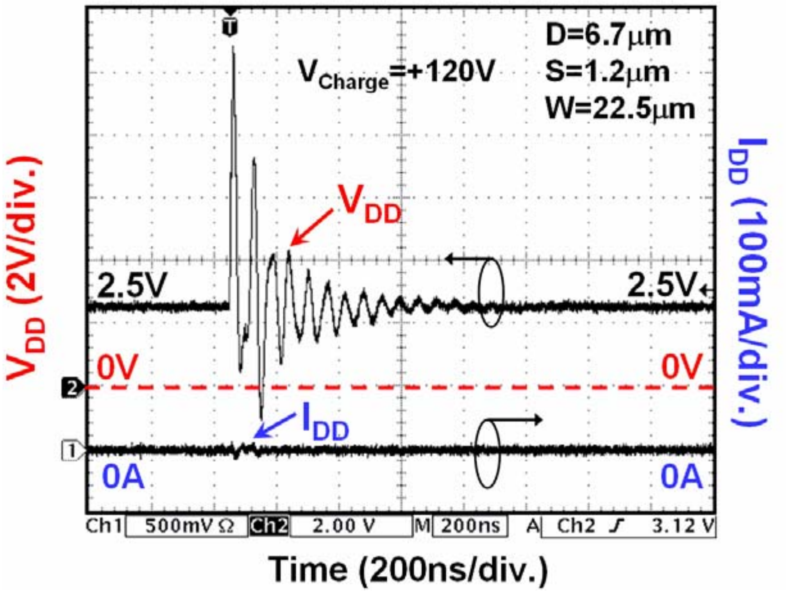
Fig. 5.11 Relations between (a) D_{Factor} and $D_{Freq(min)}$, and (b) D_{Factor} and $D_{Freq(max)}$. $D_{Freq(min)}$ ($D_{Freq(max)}$) is defined as the minimum (maximum) D_{Freq} to initiate TLU under a fixed V_P of +15V or -15V.



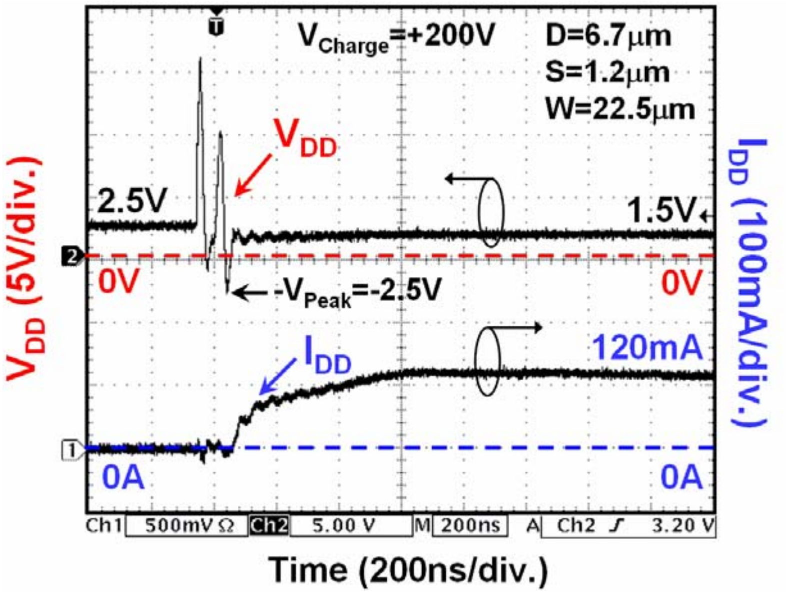
(a)

(b)

Fig. 5.12 Measured V_{DD} and I_{DD} transient responses of the SCR with V_{Charge} of (a) +10V, and (b) +14V.



(a)



(b)

Fig. 5.13 With a discharge resistor with resistance of 1.5kΩ between the relay and the V_{DD} node in TLU measurement setup (Fig. 2.7), the measured V_{DD} and I_{DD} transient responses with V_{Charge} of (a) +120V, and (b) +200V. In Figs. 5.12(b) and 5.13(b), the minimum $-V_{Peak}$ to initiate TLU is fixed (-2.5V) for the same SCR structure (D=6.7μm, S=1.2μm, and W=22.5μm).

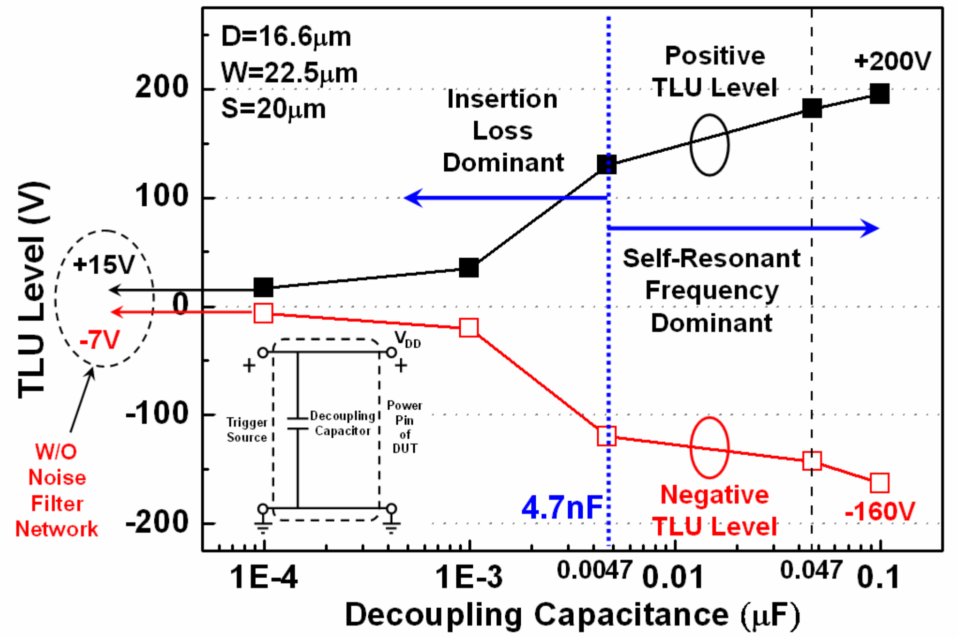


Fig. 5.14 Relations between the decoupling capacitance and the TLU level of SCR.

Chapter 6

Dependence of Device Structures on Latchup Immunity in High-Voltage 40-V CMOS Process with Drain-Extended MOSFETs

The dependence of device structures on latchup immunity in a 0.25-μm high-voltage (HV) 40-V CMOS process with drain-extended MOS (DEMOS) transistors has been verified with silicon test chips and investigated with device simulation. Layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. It was demonstrated that the drain-extended NMOS (n-DEMOS) with a specific isolated device structure can greatly enhance the latchup immunity. The proposed test structures and simulation methodologies can be applied to extract safe and compact design rule for latchup prevention of DEMOS transistors in HV CMOS process.

6.1. Background

High-voltage (HV) drain-extended MOS (DEMOS) transistors are increasingly important in modern integrated circuits (ICs) design, because DEMOS can provide a cost-effective solution to integrate both low-voltage (LV) and HV devices into a single silicon chip [36], [37], [51]-[55]. DEMOS transistors have been widely used in HV ICs or power ICs such as driver circuits, telecommunication, power management switches, motor control systems, automotive electronics, medical applications, etc. Compared with the vertical HV MOSFET structures such as diffused MOSFET (DMOS) [36], [37] or vertical MOSFET (VMOS) [36], [37] which cannot be integrated with LV devices, DEMOS transistors have the primary advantage of easily being implemented in a standard LV CMOS process. Additionally, DEMOS transistors can provide advantages such as high driving current and high junction breakdown voltage. As a result, DEMOS transistors can offer IC (system) designers a better design flexibility as well as cost-effective solution, hence leading DEMOS transistors to become a significant topic in system-on-chip (SOC) design.

When DEMOS transistors are used for products which require high reliability demand such as liquid crystal display (LCD) driver, automotive electronics, and medical applications, the detailed understanding of their reliability issues is necessary. In addition to the earlier researches of DEMOS transistors under hot-carrier [53], [54] and electrostatic discharge (ESD) [55] stresses, latchup characteristic in DEMOS transistors is also very critical and should be investigated. When DEMOS transistors are used in HV ICs design, one tough challenge on their reliability issues is to eliminate the possible occurrence of latchup [56]-[60]. However, due to an ultra-high circuit operating voltage in HV CMOS ICs, it's rather difficult to achieve the latchup-free purpose by raising the latchup holding voltage to exceed a high circuit operating voltage. In addition, latchup in HV CMOS ICs usually consumes much power in comparison with that in LV CMOS ICs [37]. Once latchup occurs, HV CMOS ICs are always inevitable to be damaged by latchup-generated high power. Thus, how to improve the latchup immunity in HV ICs is indeed a crucial reliability issue. Particular cares, such as DEMOS device structures and their layout styles, must be taken for latchup prevention. However, compared with the standard LV CMOS technology where many detailed process [1], [10], [11], [15], layout [7], [43], and circuit [44] solutions have been proposed for latchup prevention, so far there are no related researches to investigate the dependence of DEMOS device structures and their layout styles on latchup immunity in HV CMOS technology.

In this chapter, the dependence of DEMOS device structures on latchup immunity has been investigated under three different HV latchup test structures [61]. These three latchup test structures can simulate each possible case of the parasitic silicon controlled rectifier (SCR) with different DEMOS device structures, including isolated, non-isolated, symmetric, and asymmetric device structures. Additionally, layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. In order to avoid the HV latchup test structures being damaged so easily under the long-period (μs~ms) latchup overstress of the continuous-type curve tracer, the transmission line pulsing (TLP) [62] generator with pulse width of 100ns and limited energy is used instead in this chapter for latchup I-V measurements. All the TLP-measured latchup I-V characteristics on different HV latchup test structures can be qualitatively and quantitatively verified by the 2-D device simulation. All the silicon test chips are fabricated in a 0.25-μm 40-V CMOS technology.

6.2. Device Structures of DEMOS Transistors

The devices studied in this chapter are the 0.25-μm 40-V DEMOS transistors implemented in a standard 0.25-μm 2.5-/5-V CMOS technology. Both HV and LV MOSFETs are built on a high-resistance P-epitaxial (P-epi.) layer above the P-substrate. The device structures of DEMOS transistors can be classified into two major parts: (1) isolated or non-isolated, and (2) symmetric or asymmetric, device structures.

6.2.1. Isolated and Non-Isolated Device Structures

The device cross-sectional views of the isolated and non-isolated drain-extended NMOS (n-DEMOS) are depicted in Figs. 6.1(a) and 6.1(b), respectively. An N-well region enclosing the N+ drain with some overlap of poly gate is used as the drain drift region. This drain drift region (N-well) can sustain high voltage (+40V) on drain terminal by increasing the drain junction breakdown voltage. In addition, it can lower the high electric field in channel region to suppress the short channel effect [52]. The shallow trench isolation (STI) between the gate oxide and N+ drain is used to lower the electric field in gate oxide far below the critical value of oxide breakdown (10^6V/cm). Thus, the gate-oxide breakdown near the drain side can be efficiently eliminated.

The term “isolated” means that there is an additional N+ buried layer (NBL) beneath the N-well (P-well) region in device active region. Thus, the NBL can combine its peripheral N-well regions to “isolate” the whole device active region from other devices, as shown in Fig. 6.1(a). In contrast with the isolated n-DEMOS, there is no NBL in the non-isolated n-DEMOS. Instead, whole device is fabricated on a thin P-epitaxial (P-epi.) layer above the P-substrate, as shown in Fig. 6.1(b).

The device cross-sectional view of the isolated drain-extended PMOS (p-DEMOS) is depicted in Fig. 6.2. The isolation region consists of the NBL and its peripheral N-well regions. For p-DEMOS, such isolated device structure is necessary, because it can prevent the possible leakage current path from the P+ source (+40V) of p-DEMOS to the P+ pickups (0V) outside the isolation region. Similar to n-DEMOS, a P-well region enclosing the P+ drain is used as the drain drift region to sustain high voltage on drain terminal. The STI between the gate oxide and P+ drain is used to eliminate the gate-oxide breakdown near the drain side.

6.2.2. Symmetric and Asymmetric Device Structures

The device cross-sectional views of the non-isolated symmetric and non-isolated asymmetric n-DEMOS are depicted in Figs. 6.3 and 6.1(b), respectively. The term “symmetric” means that both drain and source N+ diffusions are enclosed with the N-well regions, which are used as the drain and source drift regions to sustain high operating voltage, as shown in Fig. 6.3. For asymmetric n-DEMOS, however, such N-well region to sustain high voltage is only implemented on the drain side, as shown in Fig. 6.1(b). With a better design flexibility for IC designers, symmetric device has the advantage of high-voltage sustainability on both drain and source sides. However, it must suffer larger turn-on resistance and larger layout area than the asymmetric device.

6.3. HV Latchup Test Structures

In HV CMOS ICs, latchup can be triggered on due to the inherent existence of the parasitic SCR between n-DEMOS and p-DEMOS. The device cross-sectional view of the inverter logic circuit, which consists of a non-isolated asymmetric n-DEMOS and an isolated asymmetric p-DEMOS, is shown in Fig. 6.4. The parasitic SCR composed of two cross-coupled bipolar junction transistors (BJTs) is also depicted in Fig. 6.4. Such an inverter circuit is the basic logic component in CMOS ICs. It is well known that the parasitic SCR within it, however, is the origin of latchup [15]. Once latchup is triggered on by large enough substrate or well current, a positive feedback mechanism will lead to a large current conducting through a low-impedance path from V_{DD} (source of p-DEMOS) to GND (source of n-DEMOS). As a result, HV CMOS ICs will malfunction or even be burned out due to the latchup-generated high power.

In this chapter, three different HV SCR test structures (test structures A, B, and C) are used to investigate the dependence of DEMOS device structures on latchup immunity. These three latchup test structures can simulate each possible case of the parasitic SCR in HV CMOS ICs with different DEMOS device structures, including asymmetric, symmetric, non-isolated, and isolated device structures. Table 6.1 summarizes the device structures of DEMOS transistors in test structures A, B, and C. Additionally, layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. All the latchup test structures are fabricated in a 0.25-µm 40-V CMOS process.

The device cross-sectional views and their layout top views of test structures A, B, and C are depicted in Figs. 6.5, 6.6, and 6.7, respectively. The P+ anode (N+ cathode) is used to simulate the P+ source of p-DEMOS (N+ source of n-DEMOS). Once latchup occurs, huge current will conduct from the P+ anode to the N+ cathode. To gain a better latchup immunity, both anode and cathode in test structures A, B, and C are surrounded by their base guard rings for complying with foundry’s design rules, as shown in Figs. 6.5(b), 6.6(b), and 6.7(b). In addition, the spacing from anode (cathode) to its surrounding guard ring in each test structure is kept at its minimum allowable distance according to foundry’s design rules.

Test structure A is used to simulate the parasitic SCR resulting from the non-isolated asymmetric n-DEMOS and isolated asymmetric p-DEMOS. Due to the “asymmetric” device structures in both p- and n-DEMOS, there is no P-well (N-well) region enclosing the P+ anode (N+ cathode) for source-extended region. In addition, due to the “isolated” device structure in the p-DEMOS, the P+ anode and N+ guard rings are fabricated on the NBL above the P-substrate. However, because of the “non-isolated” device structure in the n-DEMOS, the N+ cathode and P+ guard rings are fabricated on the P-epi. layer instead of NBL. Test structure B is used to simulate the parasitic SCR resulting from the non-isolated symmetric n-DEMOS and isolated symmetric p-DEMOS. Due to the “symmetric” device structures in both p- and n-DEMOS, the P+ anode and N+ cathode are enclosed with the P-well and N-well region, respectively, for the source-extended regions. Test structure C is used to simulate the parasitic SCR resulting from the isolated asymmetric p-DEMOS and n-DEMOS. Compared with test structures A and B where the n-DEMOS has the “non-isolated” device structure, the n-DEMOS in test structure C has the “isolated” device structure. Thus, the N+ cathode in test structure C is enclosed (i.e. isolated) by the NBL and its peripheral N-well regions, but not only fabricated on the P-epi. layer as in test structures A and B.

6.4. Experimental Results

To investigate the latchup characteristics of DEMOS transistors in HV CMOS ICs, the latchup I-V curves are measured in three different latchup test structures A, B, and C, with various layout parameters. In these test structures, P+ anode and N+ guard rings are connected to V_{DD}, whereas N+ cathode and P+ guard rings are connected to GND. By extracting two dominant parameters of the latchup robustness, latchup trigger voltage and holding voltage, from the measured latchup I-V curves, the dependence of DEMOS device structures and their layout styles on latchup immunity can be well evaluated. Latchup trigger voltage represents the minimum applied voltage that can “trigger” the device under test (DUT) into a latchup state. Latchup holding voltage represents the minimum applied voltage needed for the DUT to “hold” a latchup state. Thus, a higher latchup trigger or holding voltage means a better latchup robustness for the DUT. All the latchup measurements are performed at the room temperature of 25^{o}C.

Compared with the LV devices, HV devices usually require a much larger minimum-allowable spacing between the adjacent n-DEMOS and p-DEMOS (i.e. much larger anode-to-cathode spacing) because of the ultra-high circuit operating voltage. According to foundry's design rule, guard ring structures are also forced for each DEMOS transistor to enhance its latchup robustness. As a result, latchup I-V curves in HV CMOS ICs usually have a much higher holding voltage and holding current (i.e. much higher latchup holding power) than those in LV CMOS ICs. Due to such high latchup power in HV ICs, when the continuous-type curve tracer (e.g. *Tektronix 370A*) is used to measure the latchup I-V curves in HV ICs, HV devices are usually damaged before the latchup I-V curves are certainly observed or extracted. In order to avoid the HV devices being damaged so easily under the long-period (μs~ms) latchup overstress of continuous-type curve tracer, the TLP generator [62] with a pulse width (rise time) of 100ns (~10ns) is used instead in this chapter to measure latchup I-V curves of HV latchup test structures. Such 100ns-TLP generator is commonly used for ESD characterization. Compared with the general continuous-type curve tracer whose stress time approximates to μs~ms range, the TLP generator has much shorter stress time of 100ns and limited energy. Thus, by using the TLP generator for latchup I-V characterizations, the HV devices will not be damaged so easily under a latchup state, so the latchup trigger and holding voltage can be certainly extracted.

6.4.1. Relationships between Latchup Trigger (Holding) Voltage and Anode-to-Cathode Spacing

The relationships between TLP-measured latchup trigger (holding) voltage and anode-to-cathode spacing for test structures A, B, and C are shown in Fig. 6.8. Obviously, test structure C (considering the parasitic SCR resulting from isolated asymmetric n-DEMOS and p-DEMOS) has the best latchup immunity due to its highest latchup trigger and holding voltage. For example, latchup trigger voltage (holding voltage) can be as high as 97V (48V) for test structure C, even though the anode-to-cathode spacing is only as short as 27.5μm, as its TLP-measured latchup I-V curve shown in Fig. 6.9. Because of a high latchup holding voltage of 48V, which is higher than 40V of the normal circuit operating voltage, the test structure C can be latchup-free. However, latchup trigger voltage (holding voltage) can be only enhanced up to 71V (36V) for test structure A, and 70V (37V) for test structure B, even though the anode-to-cathode spacing is as long as 31.6μm, as their TLP-measured latchup I-V curves shown in Figs. 6.10 and 6.11. For test structures A, B, and C, increasing anode-to-cathode spacing can improve the latchup immunity. However, it cannot help the test structures A and B to gain a good latchup immunity as in test structure C.

Compared with the test structures A and B which have the traditional four-layer p-n-p-n latchup path, the test structure C has a six-layer p-n-p-n-p-n latchup path due to the isolation region in isolated n-DEMOS. This six-layer latchup path consists of P+ anode, N-well, P-well, NBL, P-well, and N+ cathode in sequence. Due to the isolation region in isolated n-DEMOS, both holes and electrons need to overcome an additional NBL/P-well junction barrier to initiate a positive feedback latchup event. Such unique characteristics will lead to a prominent latchup immunity, i.e. high latchup trigger and holding voltage, in test structure C. In addition, compared with the test structure A, test structure B has a shorter base width in its parasitic vertical pnp and lateral npn BJTs because of the additional source-drift region (i.e. longer emitter width). A shorter base width will lead to a higher current gain of the parasitic BJTs, hence degrading the latchup robustness [15] (i.e. lower latchup trigger and holding voltage) in test structure B. In test structures A and B, however, such difference of the base width is not obvious under a larger anode-to-cathode spacing. As a result, test structure A has a better latchup immunity (i.e. higher latchup trigger and holding voltage) than test structure B under a shorter anode-to-cathode spacing of <25.6μm, as shown in Fig. 6.8. For a larger anode-to-cathode spacing of >25.6μm, however, both test structures A and B have almost the same latchup trigger and holding voltage.

6.4.2. Relationships between Latchup Trigger (Holding) Voltage and Guard Ring Width

Fig. 6.12 shows the relationships between TLP-measured latchup trigger (holding) voltage and guard ring width for test structures A, B, and C with anode-to-cathode spacing (parameter “X”) of 19.6μm, 25.6μm, and 27.5μm, respectively. For test structures A and B, increasing guard ring width can moderately improve the latchup immunity. For example, when guard ring width increases from 0.8μm to 3μm, latchup trigger voltage (holding voltage) can be enhanced from 73V (26V) to 83V (34V) in test structure A, and from 67V (32V) to 74V (35V) in test structure B. For test structure C, however, increasing guard ring width only has little improvement on latchup immunity. Thus, in test structure C, the dominant factor to gain a good latchup immunity is the isolation region of isolated n-DEMOS, but not the guard ring structure.

From the comprehensive experimental results in Figs. 6.8 and 6.12, Table 6.2

summarizes the dependence of DEMOS device structures on latchup robustness. HV ICs with isolated n-DEMOS (test structure C) have much better latchup immunity than those with non-isolated n-DEMOS (test structures A and B). Thus, the isolated n-DEMOS in test structure C is the dominant factor to enhance the latchup robustness in HV ICs. However, symmetric or asymmetric DEMOS in test structures A and B has no great impact to improve the latchup immunity, even though asymmetric DEMOS has better latchup immunity than symmetric DEMOS under a shorter (<25.6μm) anode-to-cathode spacing, as shown in Fig. 6.8. Additionally, increasing both anode-to-cathode spacing and guard ring width can enhance the latchup immunity. However, continuously increasing anode-to-cathode spacing or guard ring width will lead to a larger layout area and higher cost. More importantly, using the isolated n-DEMOS in HV ICs can gain much better latchup robustness than only increasing anode-to-cathode spacing or guard ring width in layout schemes. Thus, using the isolated n-DEMOS in HV ICs can not only gain a good latchup immunity, but can save the total chip layout area.

6.5. Device Simulation

The experimental measured latchup characteristics of different HV latchup test structures can be verified with 2-D device simulation. The device structures used in 2-D device simulation for test structures A, B, and C are shown in Figs. 6.13(a), 6.13(b), and 6.13(c), respectively. To accurately verify the experimental results, these device structures in device simulation have the same layout parameters as the silicon test chips. For example, the anode-to-cathode spacing in device simulation of the test structures A, B, and C are 31.6μm, 31.6μm, and 27.5μm, respectively, which are the same as silicon test chips in Figs. 6.10, 6.11, and 6.9. Guard ring width in test structures A, B, and C is a fixed value of 0.8μm in device simulation. With the aid of 2-D device simulation, latchup I-V curves and their 2-D current flow lines can be clearly observed to determine which device structure will be dominant to enhance the latchup robustness in HV ICs.

The simulated latchup I-V curves of test structures A, B, and C are shown in Fig. 6.14. These simulated I-V curves are performed by connecting P+ anode and N+ guard rings to V_{DD}, whereas connecting N+ cathode and P+ guard rings to GND. The simulation results in Fig. 6.14 are consistent with the measured results in Fig. 6.8 where test structure C has the best latchup immunity because of its highest latchup trigger and holding voltage. For example, latchup trigger (holding) voltage can be as high as 94V (41V) for test structure C, even though the anode-to-cathode spacing is only as short as 27.5μm. However, latchup trigger (holding) voltage can be only enhanced up to 72V (27V) for test structure A, and 62 (26V) for test structure B, even though they have a larger anode-to-cathode spacing of 31.6μm. The simulated holding voltage of 41V (>40V) in test structure C is consistent with the experimental result in Fig. 6.9 that test structure C can be latchup-free. Additionally, the simulation results are also consistent with the experimental result in Figs. 6.10 and 6.11 that both test structures A and B have almost the same latchup holding voltage (~27V). The only difference between the experimental and simulated results is that both test structures A and B have almost the same latchup trigger voltage (~71V) in experimental result, but test structures A has a larger one (72V) than test structures B (62V) in device simulation.

The simulated 2-D current flow lines under latchup condition for test structures A, B, and C are shown in Figs. 6.15(a), 6.15(b), and 6.15(c), respectively. Clearly, concentrated current flow lines will conduct from P+ anode (V_{DD}) to N+ cathode (GND) under latchup condition. Compared with the test structures A and B which have the traditional four-layer p-n-p-n latchup path, the test structure C has a unique six-layer p-n-p-n-p-n latchup path because of the isolated region in n-DEMOS, as shown in Fig. 6.15(c). Thus, it will lead test structure C to have much better latchup robustness than test structures A or B.

6.6. Conclusion

The dependence of DEMOS device structures on latchup immunity has been investigated under three different latchup test structures in a 0.25-μm 40-V CMOS process. Layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. In order to avoid the HV latchup test structures being damaged so easily under the long-period (μs~ms) latchup overstress of continuous-type curve tracer, the TLP generator with pulse width of 100ns and limited energy is used in this chapter for latchup I-V measurements. With the TLP-measured latchup I-V curves of different latchup test structures, it was demonstrated that HV ICs with isolated n-DEMOS (test structure C) can gain much better latchup immunity than those with non-isolated n-DEMOS (test structures A and B). However, symmetric or asymmetric DEMOS has no great impact to improve the latchup robustness in HV ICs. All the TLP-measured latchup I-V characteristics on different HV latchup test structures can be qualitatively and quantitatively verified with 2-D device simulation. Both the proposed latchup test structures and simulation methodologies can be further applied to extract safe and compact design rule for latchup prevention in HV CMOS ICs.

Table 6.1

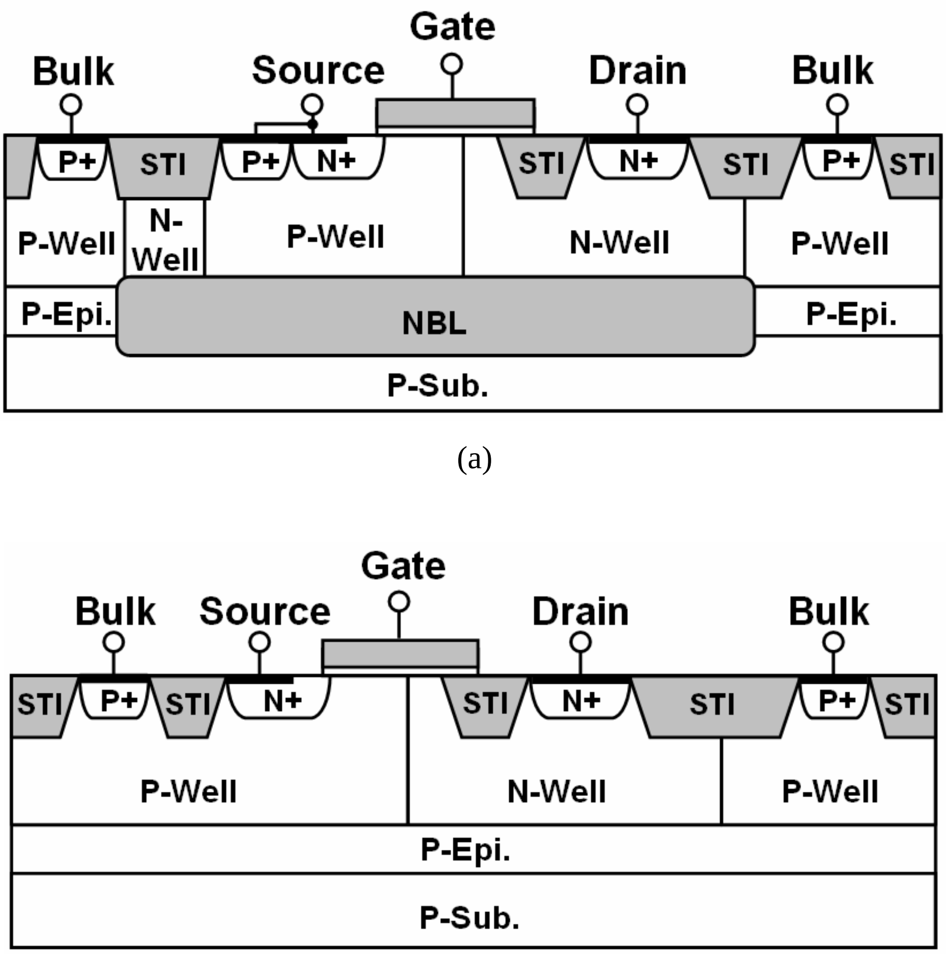
Summary of the device structures of DEMOS transistors
in latchup test structures A, B, and C

	n-DEMOS Type	p-DEMOS Type
Latchup Test Structure A (Fig. 5)	Non-Isolated Asymmetric	Isolated Asymmetric
Latchup Test Structure B (Fig. 6)	Non-Isolated Symmetric	Isolated Symmetric
Latchup Test Structure C (Fig. 7)	Isolated Asymmetric	Isolated Asymmetric

Table 6.2

Summary of the dependence of DEMOS device structures
on latchup robustness

	n-DEMOS Type	p-DEMOS Type	Latchup Robustness
Latchup Test Structure A (Fig. 5)	Non-Isolated Asymmetric	Isolated Asymmetric	Poor
Latchup Test Structure B (Fig. 6)	Non-Isolated Symmetric	Isolated Symmetric	Poor
Latchup Test Structure C (Fig. 7)	Isolated Asymmetric	Isolated Asymmetric	Good



(a)

(b)

Fig. 6.1 Device cross-sectional views of the (a) isolated, and (b) non-isolated, n-DEMOS.

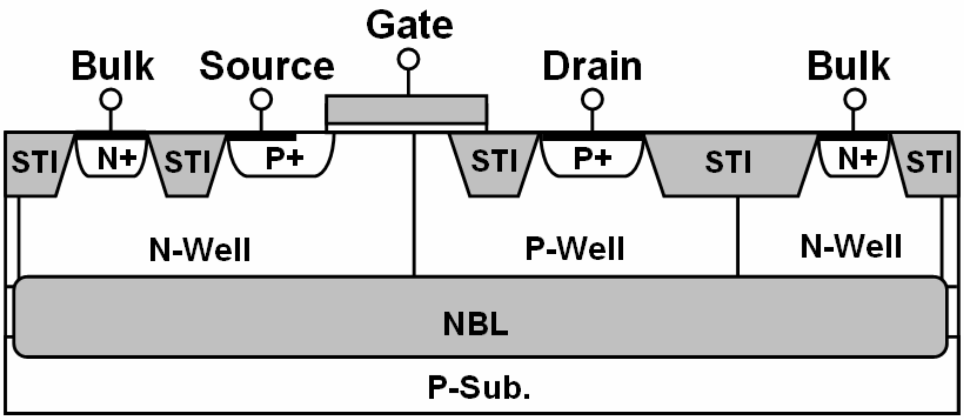


Fig. 6.2 Device cross-sectional view of the isolated p-DEMOS.

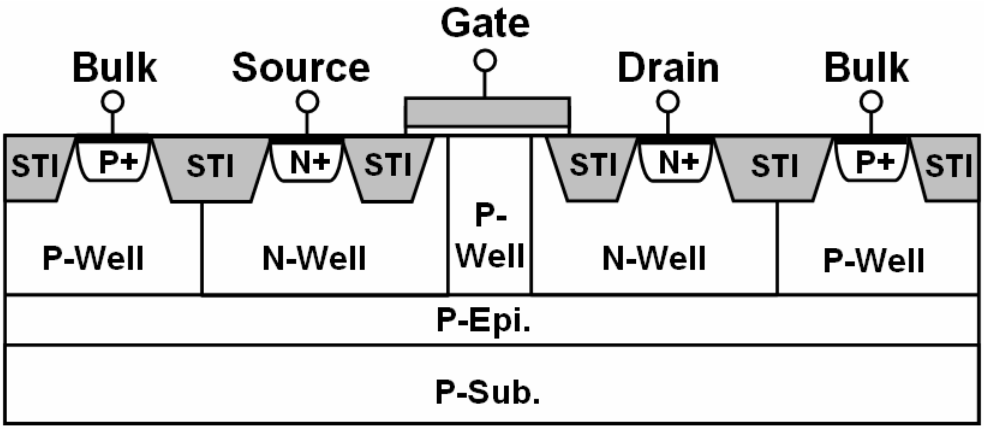


Fig. 6.3 Device cross-sectional view of the non-isolated symmetric n-DEMOS.

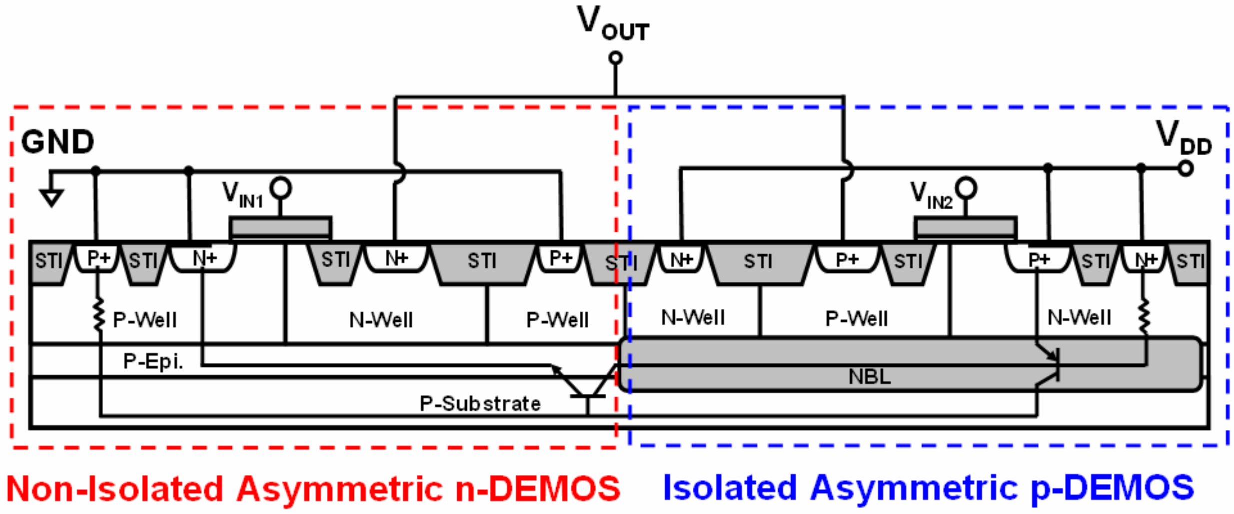
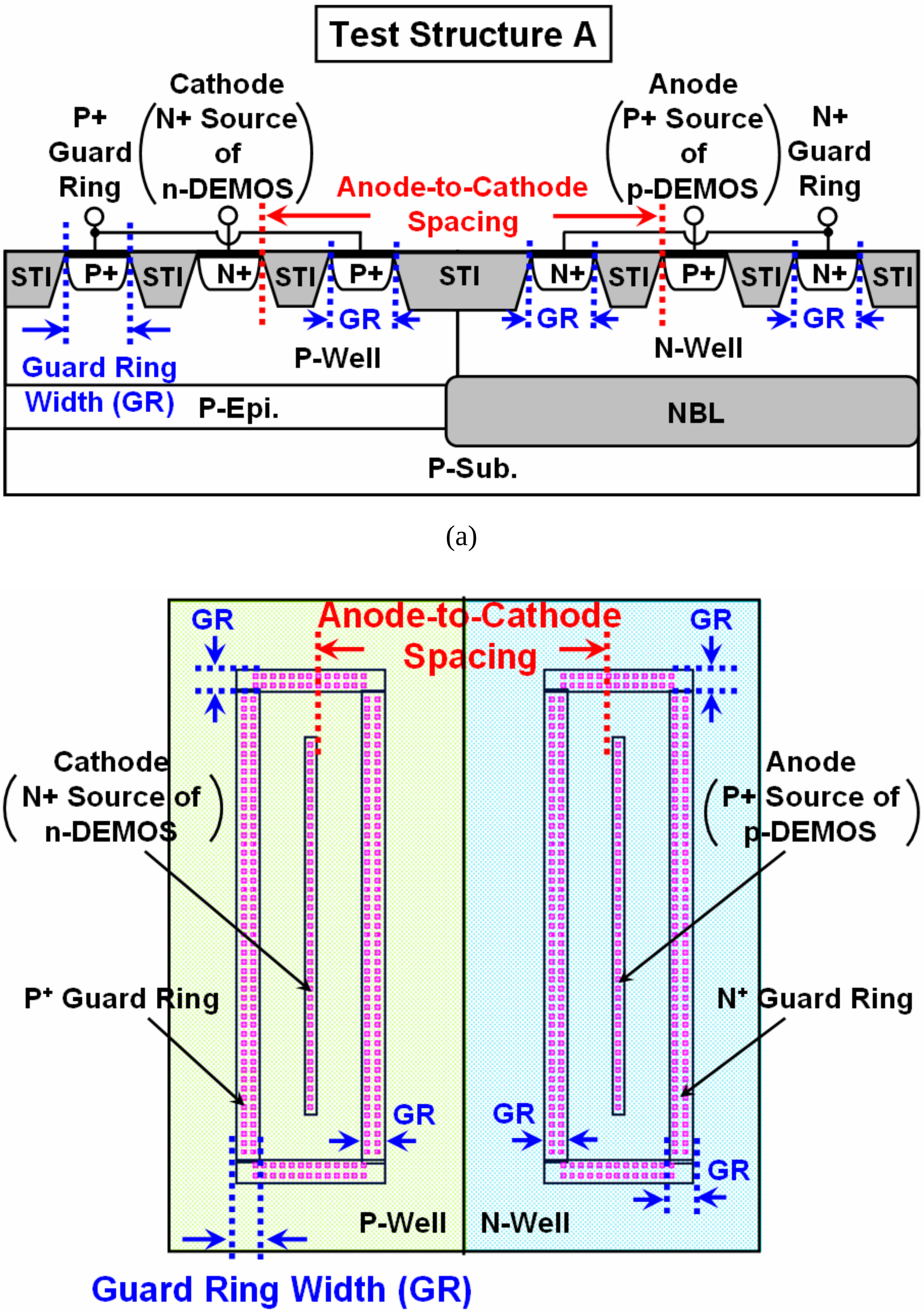


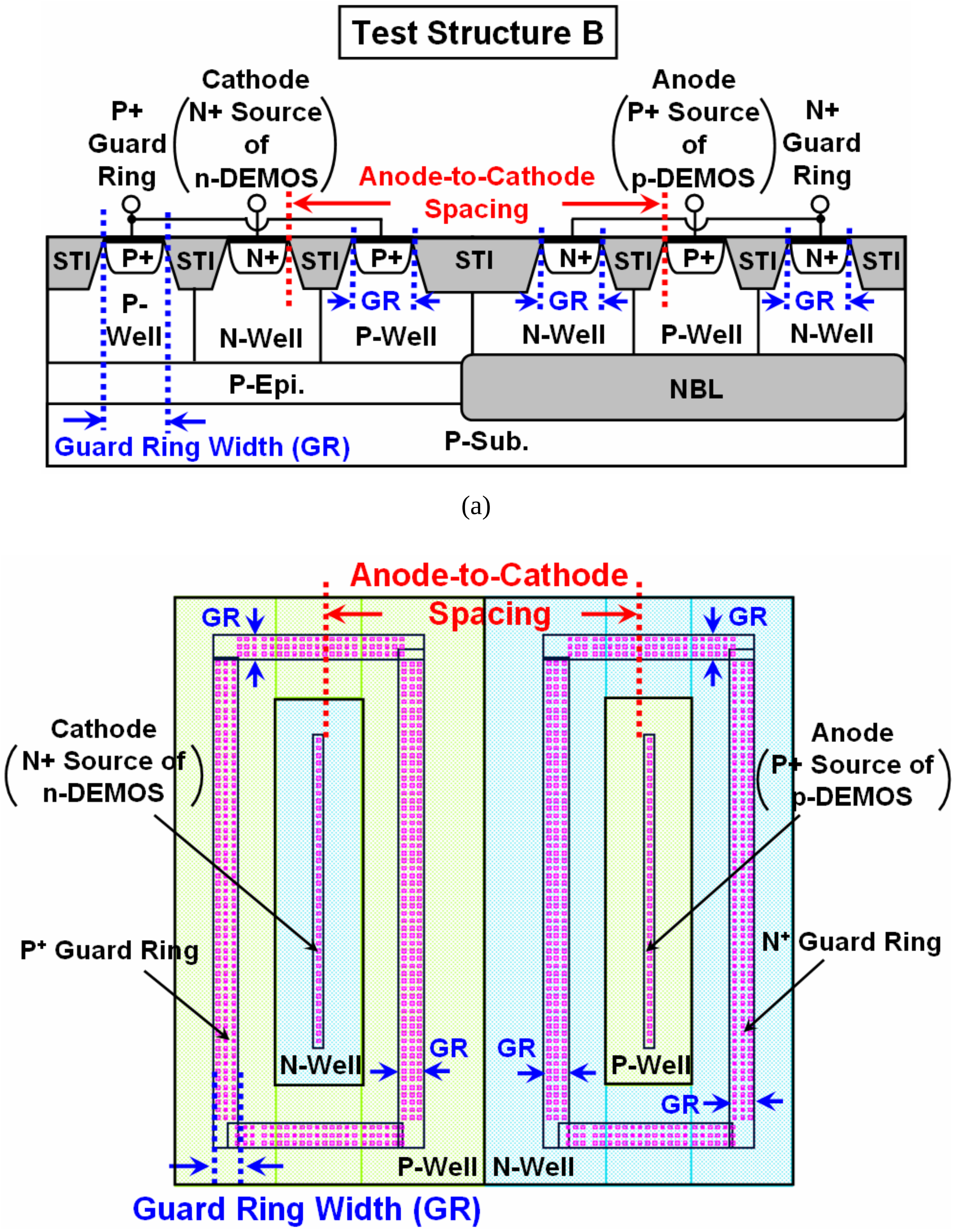
Fig.6.4 Device cross-sectional view of the inverter logic circuit consisting of a non-isolated asymmetric n-DEMOS and an isolated asymmetric p-DEMOS.



(a)

(b)

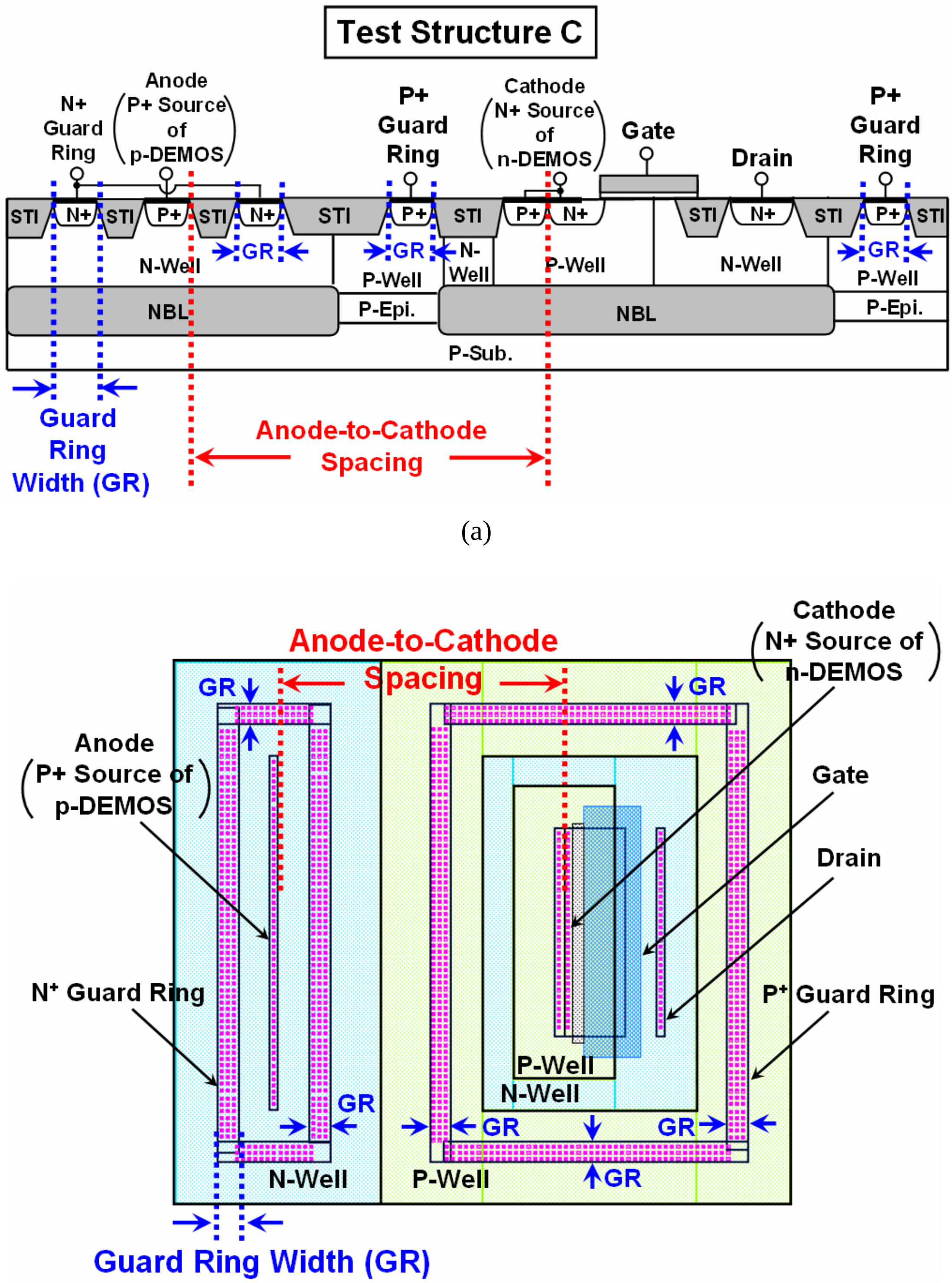
Fig. 6.5 (a) Device cross-sectional view, and (b) layout top view, of the test structure A. Test structure A is used to simulate the parasitic SCR resulting from the non-isolated asymmetric n-DEMOS and isolated asymmetric p-DEMOS.



(a)

(b)

Fig. 6.6 (a) Device cross-sectional view, and (b) layout top view, of the test structure B. Test structure B is used to simulate the parasitic SCR resulting from the non-isolated symmetric n-DEMOS and isolated symmetric p-DEMOS.



(a)

(b)

Fig. 6.7 (a) Device cross-sectional view, and (b) layout top view, of the test structure C. Test structure C is used to simulate the parasitic SCR resulting from the isolated asymmetric n-DEMOS and p-DEMOS.

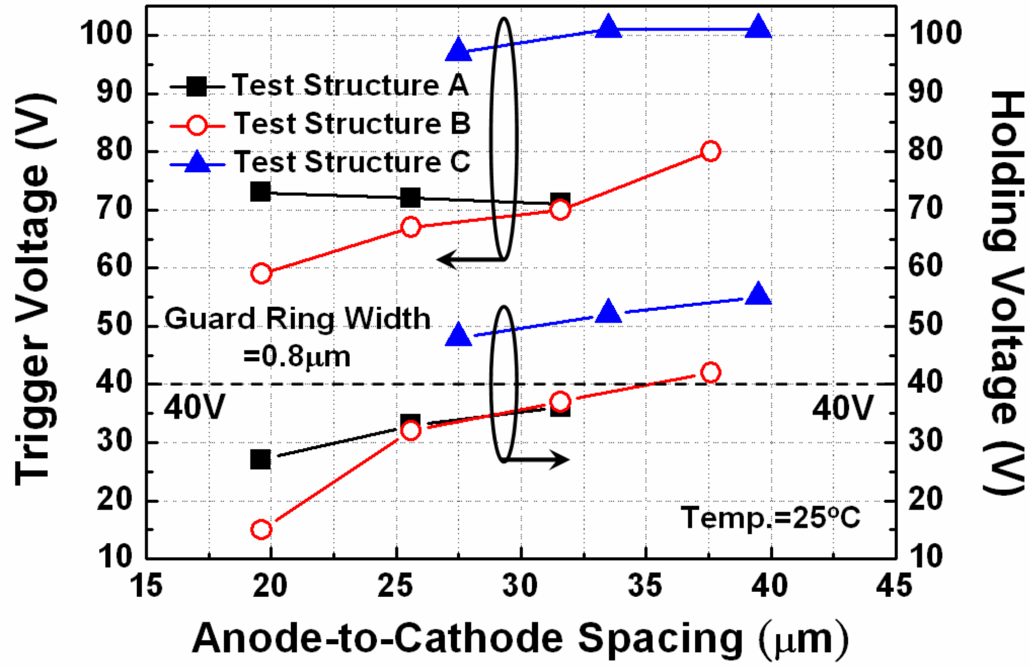


Fig. 6.8 Relationships between TLP-measured latchup trigger (holding) voltage and anode-to-cathode spacing for test structures A, B, and C.

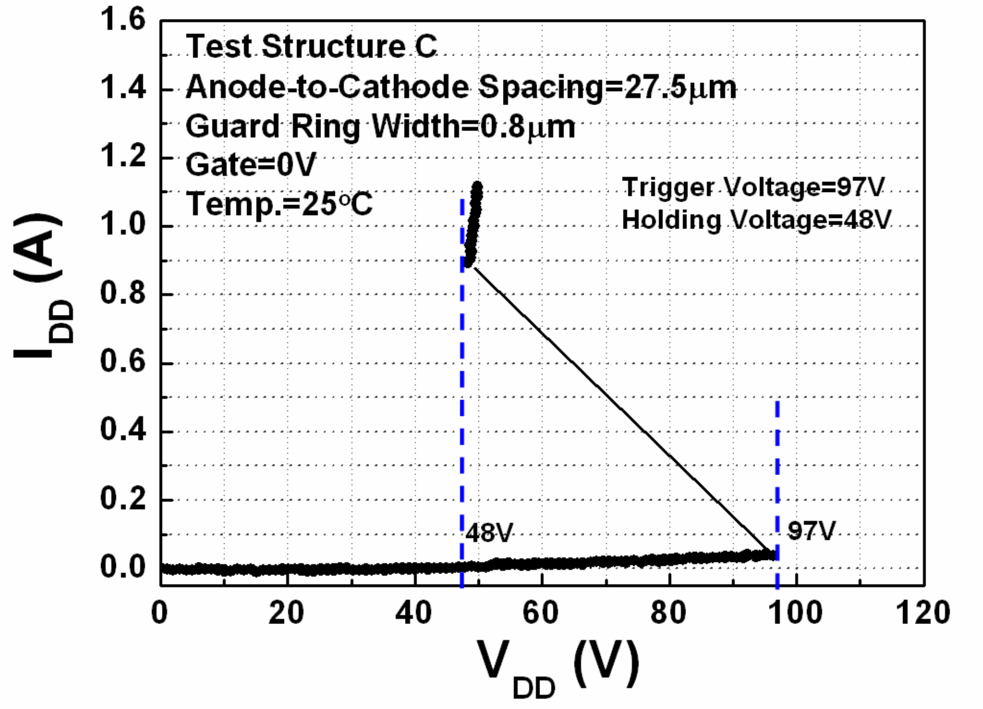


Fig. 6.9 TLP-measured latchup I-V characteristics of test structure C with anode-to-cathode spacing of 27.5μm.

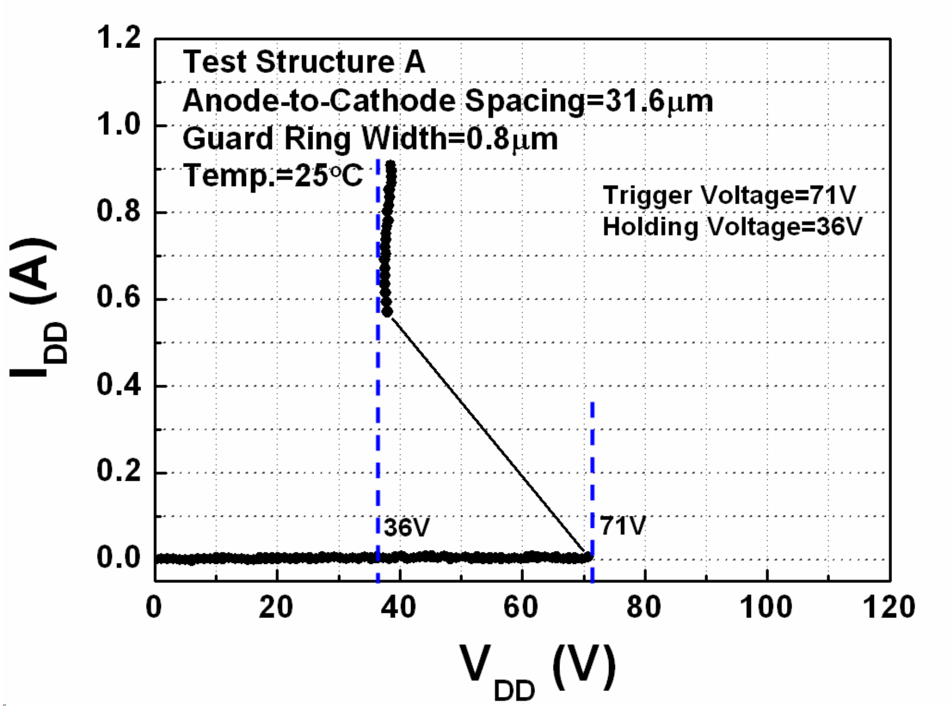


Fig. 6.10 TLP-measured latchup I-V characteristics of test structure A with anode-to-cathode spacing of 31.6μm.

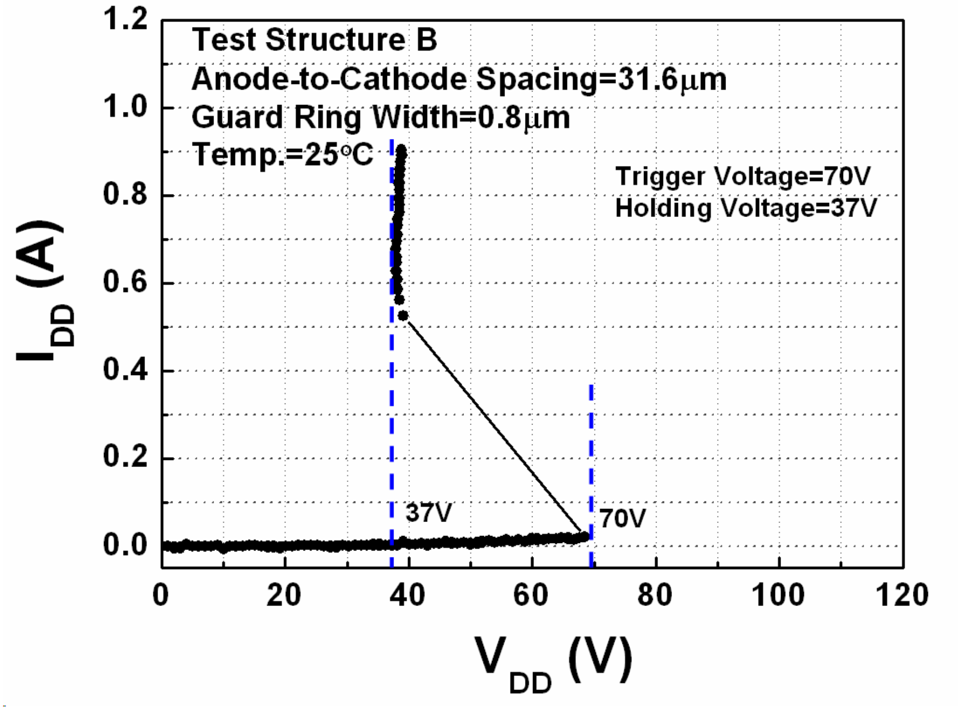


Fig. 6.11 TLP-measured latchup I-V characteristics of test structure B with anode-to-cathode spacing of 31.6μm.

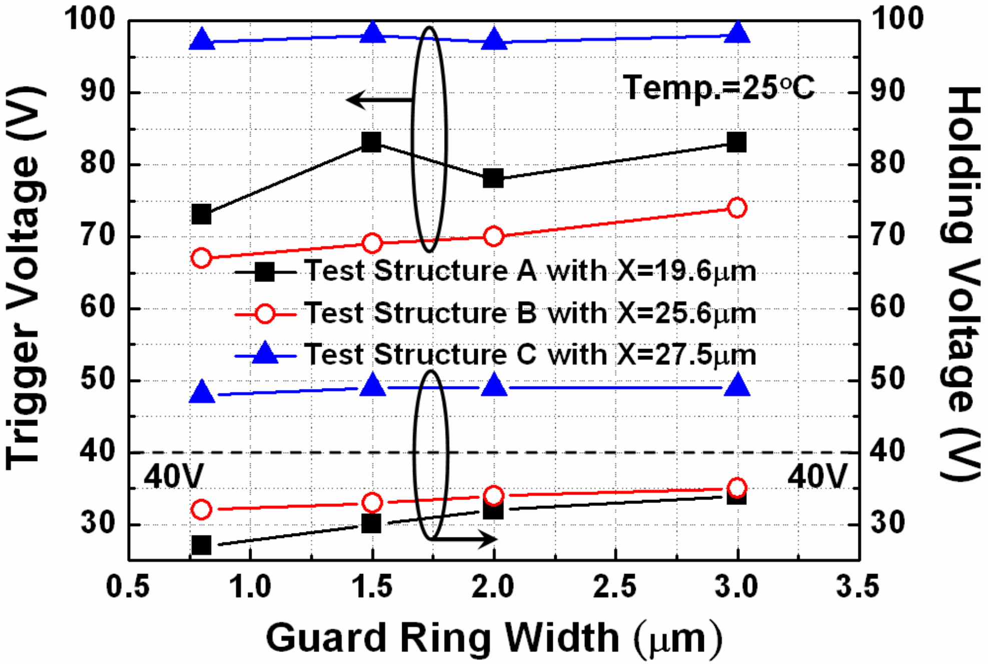
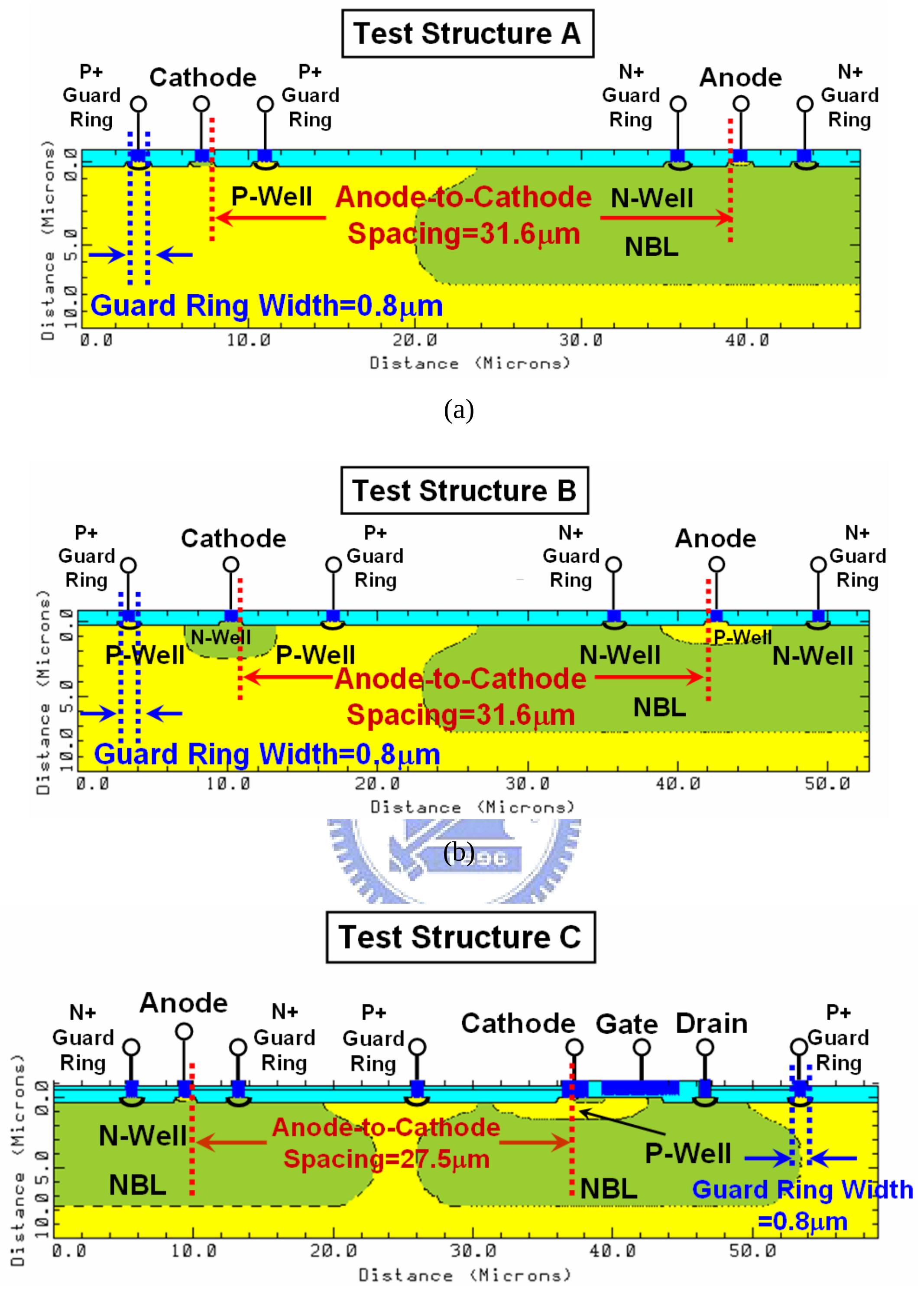


Fig. 6.12 Relationships between TLP-measured latchup trigger (holding) voltage and guard ring width for test structures A, B, and C with anode-to-cathode spacing (parameter "X") of 19.6μm, 25.6μm, and 27.5μm, respectively.



(a)

(b)

(c)

Fig. 6.13 Device structures used in the 2-D device simulation for (a) test structure A, (b) test structure B, and (c) test structure C. These device structures have the same layout parameters as the silicon test chips.

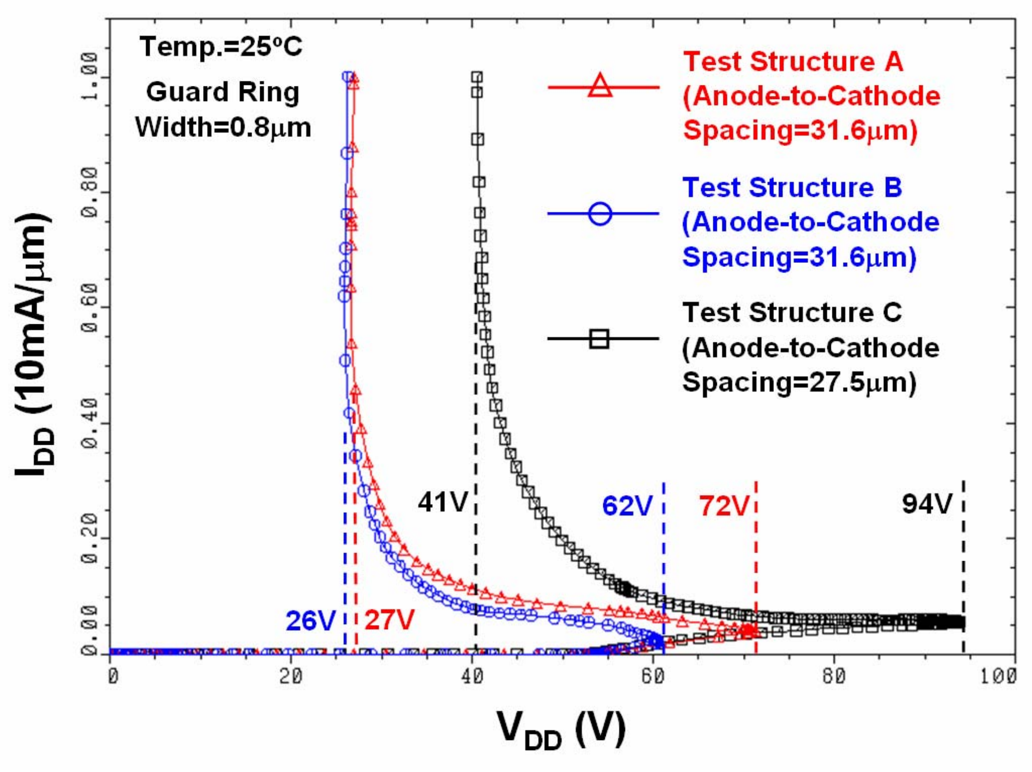
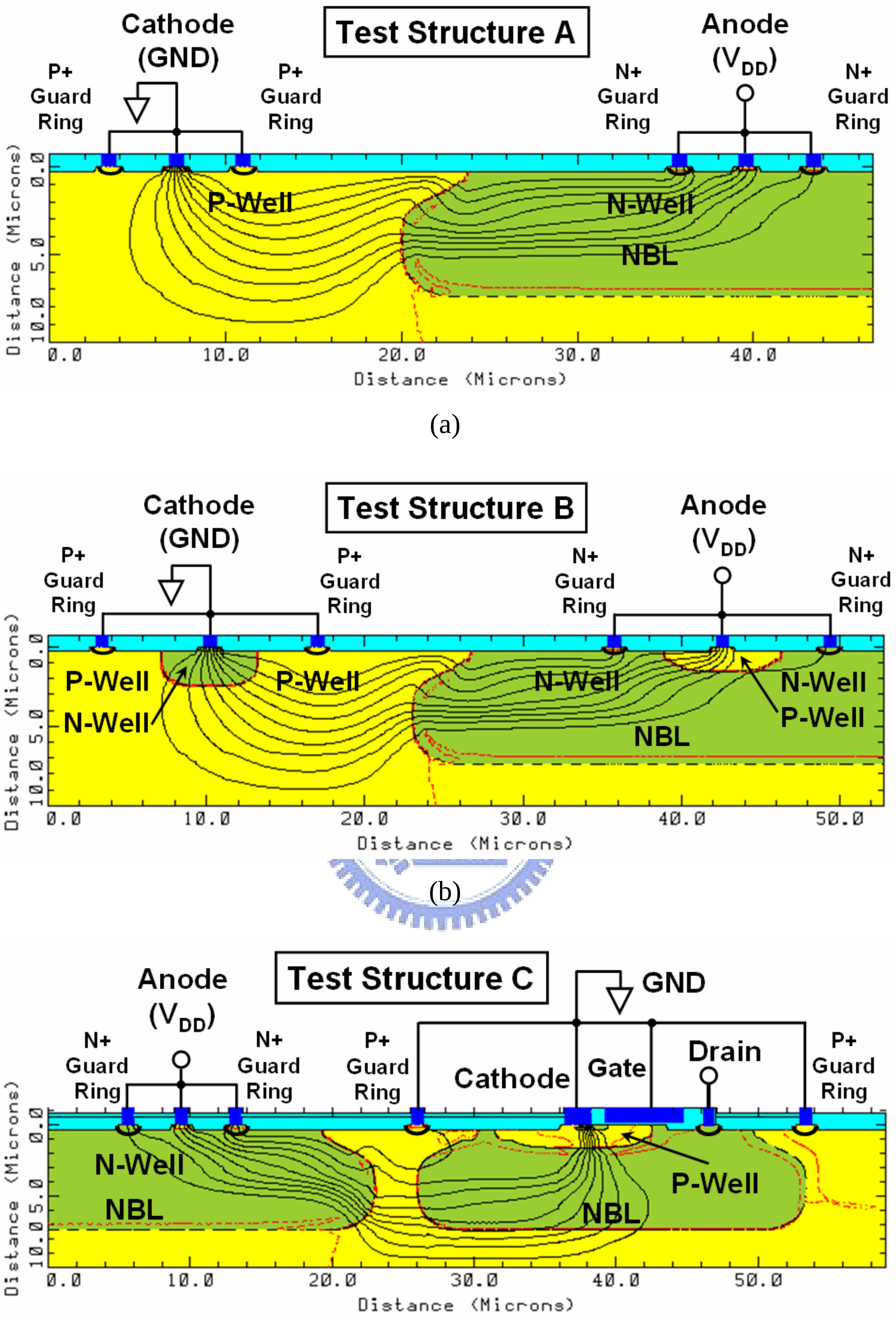


Fig. 6.14 Simulated latchup I-V characteristics for the test structures A and B with anode-to-cathode spacing of 31.6μm, and for the test structure C with anode-to-cathode spacing of 27.5μm. All these test structures have the same guard ring width of 0.8μm.



(a)

(b)

(c)

Fig. 6.15 Simulated 2-D current flow lines under latchup condition for (a) test structure A, (b) test structure B, and (c) test structure C.

Chapter 7

Conclusions and Future Works

This chapter summarizes the specific new results of this dissertation. Future works for TLU and HV latchup topics are also addressed in this chapter.

7.1. Specific New Results of This Dissertation

The specific new results of this dissertation are summarized below:

(1) This dissertation clarifies the TLU physical mechanism by device simulation and experimental verification in time domain. The proposed simulation methodology can help system or IC designers to develop safe design/layout rules or circuit techniques against TLU events.

(2) This dissertation optimizes an efficient component-level TLU measurement setup with bipolar trigger. The proposed component-level measurement setup can provide the IC industry a reliable and accurate method for evaluating the TLU immunity of CMOS ICs.

(3) This dissertation evaluates different board-level noise filter networks to find their effectiveness for TLU prevention under the system-level ESD test. The related technical know-how can provide the printed circuit board (PCB) designers useful references to optimize PCB designs for TLU prevention.

(4) This dissertation investigates TLU dependency on power-pin damping frequency and damping factor. It's useful for optimizing a bipolar trigger to evaluate the TLU immunity of CMOS ICs without overestimation. Furthermore, it's also useful to help properly design board-/chip- level noise filters to efficiently eliminate the ESD-coupled noises for TLU prevention.

(5) This dissertation investigates the dependence of device structures on latchup immunity in a 0.25-µm HV 40-V CMOS process with DEMOS transistors. Both the proposed latchup test structures and simulation methodologies can be further applied to extract safe and compact design rule for latchup prevention in HV

CMOS ICs.

The systematic investigations in this dissertation, such as theoretical analyses and practical verifications, can inspire system or IC designers to develop novel techniques for TLU prevention.

7.2. Future Works

This dissertation proves that the ESD-induced underdamped sinusoidal (bipolar) voltage on power or ground pin of CMOS ICs is the major cause of TLU under the system-level ESD test. Because the power and ground lines are widely distributed over the whole circuitry in a chip, such bipolar TLU-triggering voltage can easily trigger on TLU in the core circuitry. For quasi-static latchup, the general solution to improve the latchup immunity of core circuitry is to enlarge the distance from I/O to core circuitry. Such solution, however, is not suitable for TLU prevention, because the ESD-coupled coupled noises can be generated via the induction of electromagnetic filed. This new result reminds us that ICs will be much more susceptible to TLU than to quasi-staic latchup in advanced CMOS technologies. Thus, novel system, circuit, and process techniques to efficiently suppress the TLU susceptibility of CMOS ICs are necessary.

In addition to using the board-level noise filters proposed in this dissertation, some other techniques could be the useful candidates to further improve the TLU immunity of the CMOS ICs under the system-level ESD test. These future works are listed below.

(1) On-Chip Noise Filter
(2) ESD-Induced Noise Detection Circuit
(3) Latchup Auto-Detection, Self-Stop, and Auto-Reset Circuit
(3) Hardware and Firmware Co-Design with System-Auto-Reset Function
(4) Layout Optimization
(5) Other Specific Advanced Process Technologies

With the developments of future TLU-preventing techniques, it is anticipated that TLU can be efficiently suppressed in the continual-scaling CMOS technologies.

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論文名稱：系統層級靜電放電測試下之積體電路暫態觸發閂鎖效應
Transient-Induced Latchup in CMOS Integrated Circuits under System-Level ESD Test

Publication List

(A) Referred Journal Papers:

[1]. M.-D. Ker and **S.-F. Hsu**, “Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test,” *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821–1831, Aug. 2005.

[2]. M.-D. Ker and **S.-F. Hsu**, “Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test,” *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 161–171, Feb. 2006.

[3]. M.-D. Ker and **S.-F. Hsu**, “Component-level measurement for transient-induced latchup in CMOS ICs under system-level ESD considerations,” *IEEE Trans. Device Mater. Reliab., in press*, 2006.

[4]. **S.-F. Hsu** and M.-D. Ker, “Transient-induced latchup dependency on power-pin damping frequency and damping factor in CMOS integrated circuits,” revised by *IEEE Trans. Electron Devices*.

[5]. **S.-F. Hsu** and M.-D. Ker, “Dependence of device structures on latchup immunity in high-voltage 40-V CMOS process with drain-extended MOSFETs,” submitted to *IEEE Trans. Electron Devices*.

(B) International Conference Papers:

[1]. M.-D. Ker and **S.-F. Hsu**, “Transient-induced latchup in CMOS technology: physical mechanism and device simulation,” in *IEDM Tech. Dig.*, 2004, pp. 937–940.

[2]. M.-D. Ker and **S.-F. Hsu**, “Evaluation on efficient measurement setup for transient-induced latchup with bi-polar trigger,” in *Proc. IRPS*, 2005, pp. 121–128.

[3]. **S.-F. Hsu** and M.-D. Ker, “Dependences of damping frequency and damping factor of bi-polar trigger waveforms on transient-induced latchup,” in *Proc. EOS/ESD Symp.*, 2005, pp. 118–125.

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(C) Local Conference Papers:

[1]. **S.-F. Hsu** and M.-D. Ker, “Evaluation on measurement setup for transient-induced latchup in time-domain observation,” in *Proc. Taiwan ESD Conference*, 2004, pp. 20–24.

[2]. **S.-F. Hsu**, M.-D. Ker, G.-L. Lin, and Y.-N. Jou, “Dependencies of device structures and layout parameters on latchup immunity in high-voltage CMOS process,” in *Proc. Taiwan ESD Conference*, 2005, pp. 29–31.