國立交通大學

電子工程學系 電子研究所

博 士 論 文

# 矽化鎳之熱穩定性與超淺接面應用的研究

# A Study on the Thermal Stability and Shallow Junction Applications of Nickel Silicide

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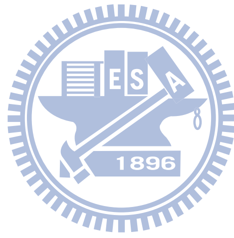
指導教授：崔秉鉞　教授

中 華 民 國 九 十 八 年 十 月



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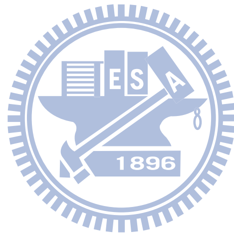
博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

October 2009
Hsinchu, Taiwan, Republic of China

中華民國九十八年十月



# 矽化鎳之熱穩定性與超淺接面應用的研究

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## 摘要

在現今微縮驅使下，矽化鎳是最常用在先進製程中的金屬矽化物。在矽化鎳熱穩定性及接面特性之研究方面，本論文提出利用高劑量鍺離子佈值來改善其熱穩定性。我們發現在矽基板上，鍺摻雜可提升結塊及二矽化鎳相轉變溫度各攝氏 50~100 度。而將其利用在高摻雜之 n 型或 p 型矽基板上時，因受其它高摻雜離子影響，改善程度只有攝氏 50 度左右，但是對於 n 型或 p 型多晶矽閘極，卻仍保有攝氏 100 度的改善能力。此外還發現高劑量鍺離子佈值可以改善矽化鎳與矽的介面平坦度。在熱穩定性研究的基礎下，進一步研究 n 型或 p 型二極體特性的改善。我們發現對於漏電流而言，雖然有鎳沿著鍺離子佈植產生的缺陷往下擴散之影響，仍可以看出對週邊漏電流降低以及整體漏電流耐溫增加的改善。

為了減少寄生電容及改善短通道效應，電晶體結構趨向多閘極結構，並可能進一步製作在絕緣層上矽(SOI)的晶片上面。由於先將離子植入矽化鎳，再經過退火後，會使得佈值離子被離析到矽中，可形成超淺接面，本論文遂利用此技術在 SOI 上製做並研究超淺接面之特性。在現今常用的二氟化硼($BF_2^+$)、磷($P^+$)、砷($As^+$)離子佈值入

矽化鎳後再經由攝氏 500~750 度的再退火製程，可以發現其具有良好的熱穩定性及可得到遠低於矽化鎳蕭基特接面的漏電流。在此也針對其週邊二氧化矽介面造成漏電流的捕獲能態密度進行探討，藉由閘極二極體(gated-diode)及電荷捕捉(charge pumping)兩種方法量測捕獲能態密度的大小，分析漏電流機制。

針對上述兩種在不同基板上製作的超淺接面，我們製作不同的結構來量測此兩種接面的矽化鎳/矽的接觸阻抗。在矽基板上，經過鍺離子佈值後，矽化鎳對高摻雜 p 型基板的接觸阻抗可以低到 $10^{-8}$ $\Omega$-cm$^2$ 的數量級，而在 SOI 上可量到 $BF_2^+$佈值的接面有 $2\times10^{-8}$ $\Omega$-cm$^2$ 的低接觸電阻率，而 $P^+$佈值的接面則有偏高的 $3\times10^{-7}$ 的接觸電阻率。

最後我們希望利用掃描探針顯微術之一的 Kelvin-Probe Force Microscopy (KPFM) 來量測半導體表面電位差，透過常用的的幾種不同一維載子濃度分布測定方法為基準，來推算表面二維載子濃度分布。雖可成功利用在較深的 p-n 接面剖面濃度的分析，但是空間解析度不理想，尚待改善。

整體而言，本論文研究了利用鍺離子佈植改善矽化鎳的熱穩定性和利用離子植入矽化鎳再經退火之方法改善蕭基特二極體接面的電特性，以及研究了它們的接觸阻抗大小並期待利用 KPFM 來量測超淺接面深度。

# A Study on the Thermal Stability and Shallow Junction Applications of Nickel Silicide

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## Abstract

In the ULSI IC industry, as the gate length is being scaled down to the nanometer level, metal silicides are being used as contact materials to reduce parasitic resistance. Among the different silicide materials, nickel silicide is the most popular. In a study on the thermal stability and junction properties of nickel monosilicide (NiSi), I proposed high-dosage germanium ion implantation (Ge I/I > $5 \times 10^{15}$ $cm^{-3}$) before silicide formation to improve the thermal stability. The experimental results showed that Ge implantation resulted in an improvement in both the phase transformation and agglomeration temperatures of NiSi by 50~100 °C. We applied this technique to NiSi contacted $n^+$-p and $p^+$-n shallow junctions. The improvement was reduced to 50 °C due to the high concentration of dopants in the bulk-Si substrate. However, the application to a highly doped poly-Si gate yielded in improvements by 100 °C. Additionally, for samples implanted with Ge I/I before NiSi formation, we found a very smooth NiSi/Si interface at 750 °C. Although fast Ni diffusion via the defects induced by the Ge I/I was present, we still observed smaller peripheral leakage currents and better thermal stability by electrical characterization.

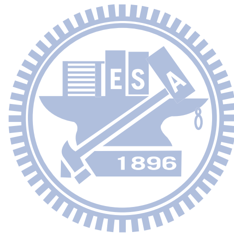
Multi-gate transistors fabricated on silicon-on-insulator (SOI) wafers were developed against the short channel effect and demonstrated lower parasitic capacitance. When using the implant-to-silicide (ITS) technique, the implanted atoms diffused out of the silicide and piled up at the silicide/silicon interface during the post-annealing process. The segregated atoms formed an ultra-shallow junction. In my study, the ITS technique was utilized to fabricate lateral modified Schottky barrier (MSB) junctions on SOI wafers. $BF_2^+$, $As^+$, and $P^+$ dopants were used and the electrical characteristics of the diodes after annealing from 500 °C to 750 °C were compared. It was found that the MSB junction maintained a good thermal stability and had much lower leakage currents than the NiSi contacted SB junction. We also measured the interface trap density between the Si and $SiO_2$ of MSB $p^+$-n and $n^+$-p diodes. Charge pumping and gated diode methods were used to measure the interface trap density and analyze the leakage current mechanism for MSB diodes.

We designed contacts and structures with different dimensions to measure the contact resistance of the NiSi/Si interface for a $p^+$-n junction with Ge I/I on bulk-Si and MSB junctions on SOI. The specific contact resistivity for the $p^+$-n junction with Ge I/I was around $10^{-8}$ $\Omega$-cm$^2$, $2 \times 10^{-8}$ $\Omega$-cm$^2$ for the $p^+$ MSB contact, and $3 \times 10^{-7}$ $\Omega$-cm$^2$ for the $n^+$ MSB contact.

Finally, we demonstrated a two-dimensional (2-D) carrier/dopant profiling technique that uses Kelvin-probe force microscopy (KPFM) to measure the surface potential of a p-n junction. The correlations between the surface potential difference measured by KPFM and the results of secondary ion mass spectroscopy (SIMS), the surface carrier concentration obtained by spreading resistance profiling, and the capacitance-voltage method were established. These results indicate that 2-D carrier depth profiling of a p-n junction was successfully achieved.

To summarize, the thermal stability and junction properties of NiSi were improved by Ge I/I and ITS techniques, respectively. The contact resistances were measured, and a 2-D

carrier depth profiling technique was proposed, which is expected to be very useful for NiSi contacted ultra-shallow junction applications in the future.



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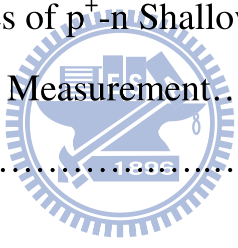

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# 誌 謝

能夠順利完成論文，我想感謝我的指導教授 崔秉鉞老師。感謝老師在我這七年來博士生涯中實驗、研究、與論文上的指導跟教誨，並感謝老師在我遇到困難跟發生意外時給予的關懷，謝謝老師的體諒跟這麼多年來的照顧。

其次我要感謝在實驗上提供幫助的國家奈米元件實驗室、交通大學奈米中心、清大果老師實驗室跟漢民科技公司提供優良的機台設備以及管理完善的實驗環境使得實驗可以順利進行，並感謝在奈米中心跟 NDL 廠內服務的技術人員們，謝謝你們提供的服務與實驗上寶貴經驗和建議。

感謝我的實驗室伙伴們，謝謝已畢業學長及同學們: 國龍、家彬、誌鋒、琪聰、修維、偉豪、明賢們在實驗上幫忙跟規劃，也謝謝畢業或在學的學弟妹們能在漫漫長夜的無塵室內一起打拼，也特別感謝俊凱跟振銘學弟在我車禍時生活上的幫忙，真的很謝謝大家。其次我想感謝這麼多年來一起打球的龍捲風隊員跟東方球隊的大叔們，能跟你們打球真的很快樂，也謝謝你們在為人處世上提供的寶貴經驗。

最後我想感謝我的家人母親、大哥跟大嫂、妹妹跟舅舅、姑姑們，謝謝你們的支持跟這麼多年來的栽培與體諒，也希望在天上的父親跟阿嬤可以替我高興。

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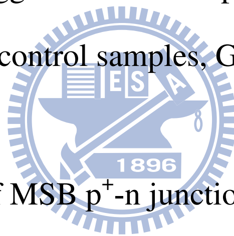

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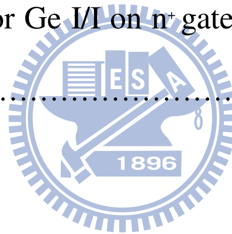

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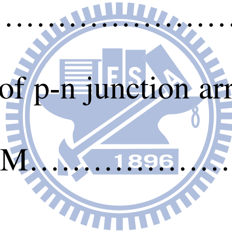

# Chapter 1

# Introduction

## 1-1 Scaling down of CMOS

In 1960, the first successful metal-oxide-semiconductor field-effect transistor (MOSFET) was demonstrated by D. Khang and M. M. Atalla [1]. Later, the first CMOS circuit was invented by Frank Wanlass in 1963 [2]. The CMOS circuit gradually went on to become the building block of integrated circuits. In order to obtain high-performance, high-density MOSFET devices, it became necessary to scale down the dimensions of these devices; it was found that this scaling down followed Moore's Law, proposed in 1965 [3]. The paper, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," published in 1974, is regarded as providing the earliest guiding principle for MOSFET, circuit, and chip design [4]. Table 1-1 shows the variation in circuit performance obtained by constant-field scaling or constant-voltage scaling [5]. The basic aim of these methods is to scale down the size of a MOSFET by a factor "k" to produce a smaller MOSFET with similar electrical behavior. In constant-field scaling, for example, all voltages and dimensions are reduced by a scaling factor, and the doping and charge densities are increased by the same factor. However, the parameters of a MOSFET were tuned to eliminate the disadvantages of constant-field scaling, as illustrated in Fig.1-1 [5]. No matter which type of scaling method is used, as the device is scaled down, the resistance effects become more and more pronounced. Since 1992, the Semiconductor Industry Association has annually published The International Technology Roadmap

for Semiconductors (ITRS). This roadmap provides future technology targets for the semiconductor industry.

As mentioned above, devices are scaled down for achieving better performance, higher device density, lower operation voltage, and also lower cost. However, there are some disadvantages that arise as a result of devices being scaled down: The parasitic resistance increases when the dimensions of a device are reduced, the gate leakage current increases as the gate oxide thickness shrinks, and the short channel effect (SCE) becomes increasingly pronounced as the gate control capability weakens. ITRS reports have suggested some new materials and structures that might provide solutions to these problems [6]. The parasitic resistance can be reduced by using a metal gate, increasing S/D, and using a silicide contact. High-dielectric constant dielectrics can be used to reduce the effective oxide thickness and gate leakage currents, while maintaining better performance than before [7,8]. Several methods have been proposed to suppress the SCE, such as raising the substrate doping concentration, utilizing ultra-shallow source/drain (S/D) junctions, and increasing gate controllability [9]. Some structures have been invented to enhance the gate control capability and suppress the SCE, such as ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs [10,11], multigate (MG) FETs [12-14], and gate-all-around (GAA) FETs [15]. Most of these structures have been fabricated on an SOI substrate. An additional advantage of an SOI wafer is that the bottom oxide layer (BOX) can also reduce the parasitic capacitance [16].

## 1-2 Scaling down of a Junction

We now focus on the effects of junction scaling: the scaling down of the junction depth and series resistances of a MOSFET. Table 1-2 lists some important parameters

stipulated by the 2008 ITRS roadmap [6], such as the junction depth, junction leakage current, silicide sheet resistance, silicide thickness, and contact resistivity. Junction depth scaling includes reducing the diffusion depth of the dopant and shrinking the thickness of the contact silicide. The series resistances are dominated by silicide materials, which affect the Schottky barrier height between the silicide and junction, and the activated dopant concentration of the junction.

## 1-2-1 Contact Silicide Issues for a Junction

Metal silicides have been used in the Si microelectronics industry for more than thirty years. Since the first paper on the application of metal silicide to doped poly-silicon for low-resistivity interconnections was published in 1979 [17], many noble and refractory metals have been found to have potential to form stable silicide with silicon. In the integrated circuit industry, metal silicides are usually used as contact materials at source, drain, and gate regions. Their low sheet resistances are an important virtue in device applications for reducing the parasitic resistance and signal propagation delay time [18]. Table 1-3 shows the characteristics of some commonly used metal silicides [19].

Titanium disilicide ($TiSi_2$) was the first metal silicide successfully used in the IC industry [18]. However, its phase transformation from the high-resistivity phase (C49-$TiSi_2$: 60~80 μΩ-cm) to the low-resistivity phase (C54-$TiSi_2$: 10~16 μΩ-cm) becomes more and more difficult as the line width shrinks to less than 0.2 μm [20-23]. Unlike $TiSi_2$, $CoSi_2$ solves the narrow line width impact on sheet resistance and also the bridging effect. Therefore, at the 0.18 μm technology node, $TiSi_2$ was replaced by cobalt disilicide ($CoSi_2$: 14~20 μΩ-cm) [22,24]. However, the high Si volume consumption during $CoSi_2$ formation is no longer acceptable after the 90-nm node because it would drastically increase the leakage current of an ultra-shallow S/D

junction.

Recently, nickel monosilicide (NiSi: 14~20 μΩ-cm) has become a popular contact material due to its low sheet resistance. Moreover, NiSi has less Si consumption (0.82 nm Si for 1 nm NiSi), low film stress, and low formation temperature (~350 °C) [19,25-27]. The main problem with NiSi is its poor thermal stability, and some improvements should be made to integrate NiSi into nanometer-scale device fabrication.

## 1-2-2 Series Resistance Issues for a MOSFET

As a MOSFET device is scaled down, channel resistance decreases with decreasing gate length. Therefore, the portion of parasitic resistance becomes increasingly significant and even becomes a hindrance for device performance. In 1986, K. K. Ng and W. T. Lynch calculated the relationship between the device structure and parasitic resistance, including the contact resistance, S/D sheet resistance, spreading resistance, and accumulation resistance [28]. In 2002, S. D. Kim reported an analysis of the series resistance when CMOS was scaled to the nanometer regime [29] and suggested that the overlap and contact resistances would dominate the total resistance as a device was scaled to the nanometer level. Moreover, the contribution of contact resistance would rapidly increase due to the shrinking of the contact area and therefore contact resistance would be the major part of the total series resistance. Based on the ITRS roadmap, they calculated the series resistance of NMOS and PMOS transistors, and found that the silicide-diffusion contact resistance always accounts for a large proportion of the total series resistance: 49% in an NMOSFET and 34.5% in a PMOSFET, as shown in Fig.1-2 [29]. MGFETs and GAAFETs are two structures that use sidewalls to increase the effective channel

width and improve the gate-controllability. However, the problem of a smaller contact area, which causes a higher contact resistance, is still unsolved. If the contact resistance is larger than the channel resistance, the scaling down of the device would be meaningless. Therefore, a method to effectively reduce the parasitic resistance is an important issue.

## 1-3 Motivation

The possible applications of nickel silicide in the microelectronic industry have been studied since the early 1980s. The main issue with NiSi is its poor thermal stability, including thin film agglomeration and high-resistivity phase ($NiSi_2$: 40~50 μΩ-cm) transformation [19]. Since the line width and thickness of NiSi are continuously being scaled down, a new technique to improve its thermal stability is required. Several methods have been proposed to improve the thermal stability of a NiSi film on a Si substrate. For example, fluorine ion implantation [30,31], nitrogen ion implantation [32,33], capping layers [34,35], palladium (Pd) incorporation [36], and platinum (Pt) incorporation [37-38] have all been tried. Among these methods, Pt incorporated Ni silicide showed the most promising results. A drawback of Pt-incorporation is the higher resistivity due to Pt doping.

In the 1980s, Ge ion implantation was reported as a substrate amorphization technique to eliminate the dopant channeling effect [39-41]. Several investigations on the effects of the Ge pre-amorphization implantation (PAI) process on metal-silicide formation have been reported [42-45]. Most of these papers have focused on Ti-silicides and Co-silicides. High-dose Ge PAI can improve the thermal stability of $TiSi_2$, while low dose ($\leq 1 \times 10^{15}$ $cm^{-2}$) Ge PAI does not play any role [44]. On the

other hand, the incorporation of Ge causes an increase in the nucleation temperature of $CoSi_2$ from about 600 °C to about 800 °C [45]. The effects of Ge incorporation on Ni-silicides were reported recently [46-50]. Kittl et al. found that Ge PAI can increase the growth rate of $Ni_2Si$ at 250 °C [46]. Surdeanu et al. reported that a shallow junction and better short channel effect in MOSFETs can be obtained with Ge PAI [47]. Yun et al. observed that Ge PAI to a dose of $1\times10^{14}$ $cm^{-2}$ could cause a smooth NiSi/Si interface and suppressed the oxidation on arsenic doped $n^+$ Si [48]. However, medium dose Ge PAI did not affect the thermal stability of NiSi. The retardation of the phase transformation from NiSi to $NiSi_2$ was found on a $Si_xGe_{1-x}$ substrate, but the NiSi agglomeration and Ge out-diffusion on a $Si_xGe_{1-x}$ substrate were worse than those on a Si substrate [49,50]. Kim et al. reported that a thin Si capping layer on a $Si_{0.81}Ge_{0.19}$ substrate could improve the NiSi(Ge) agglomeration temperature due to the strain effect [51].

According to the above reports, a suitable concentration of Ge-incorporation may benefit the thermal stability of NiSi films, but the effect of Ge-incorporation on the NiSi-contacted shallow junction has not been investigated. This thesis discusses a thorough study of the thermal stability improvement of NiSi/Si (S/D contacts) and NiSi/poly-Si (gate contacts) structures by Ge ion implantation. The effects of Ge ion implantation on the electrical characteristics of shallow $n^+$-p and $p^+$-n junctions were also examined.

For non-classical MOSFET structures, which were generally fabricated on an SOI substrate for SCE improvement, NiSi was reported to have good thermal stability even when the formation temperature was over 900 °C. Because the junction depth is limited by the thickness of the top Si layer, the junction improvement of UTBFETs, MGFETs, and GAAFETs focused on the reduction of the S/D resistance and S/D lateral diffusion length. Schottky-barrier (SB) MOSFETs have some advantages such

as a superior scaling ability due to the abrupt S/D junctions, low extrinsic parasitic resistance, and process compatibility with CMOS technology [52,53]. Because of the inherent physical scalability, the abrupt junction formed at the silicide/Si interface was beneficial to the scaling-down of the gate length to the sub-10-nm region. The Schottky barrier at the source side can also improve the drain induced barrier lowering (DIBL) and SCE [54]. However, SB MOSFETs were often fabricated with mid-gap-metal silicides, such as NiSi. These provide extremely poor saturation driving-currents and high subthreshold leakage currents due to a high gate induced drain leakage (GIDL) and junction leakage [53]. In 2004, Kinoshita et al. demonstrated a 50-nm high-performance Schottky-like NMOSFET device by using a dopant-segregation (DS) technique to form an approximately 10-nm-thick interfacial dopant layer at the source and drain [55,56]. Then in 2005, B. Y. Tsui and C. P. Lin reported a Modified-Schottky-Barrier (MSB) FinFET on SOI, which had an S/D extension-like interfacial layer placed between the silicide S/D and channel region, provided by an implant-to-silicide (ITS) technology [57]. This interfacial dopant layer was thought to be created by a dopant segregation effect. The main advantage of Schottky-like devices is the ability to reduce the effective barrier height for n and p-type Si due to different implanted dopants. Thus, they can also keep the driving current high enough and eliminate the subthreshold leakage current.

Using the reported ITS method, we fabricated some MSB $n^+$-p and $p^+$-n junctions. The purpose of this thesis is to make a differential comparison of an MSB junction's characteristics on SOI substrate, including $P^+$, $As^+$, and $BF_2^+$ doping. Different thermal budgets were tested to examine their segregation efficiency. In addition, we measured the electrical characteristic of MSB junctions.

The importance of contact resistance was stated in section 1-3. The contact resistances of Ge I/I and MSB junctions are also an interesting topic for device scaling;

both of them are still unknown. Some studies have reported that Ge ions can assist Boron doping activation [58]. The segregated dopant concentration dominates the barrier height and contact resistance of an MSB junction. Thus, based on measurements using the cross bridge Kelvin resistor (CBKR) method [59,60], we designed some structures to obtain their contact resistances.

For non-classical MOSFETs, there is another disadvantage with regard to electrical characteristic analysis. In order to simulate and model device performance precisely with technology computer aided design (TCAD) tools, the measurement of the two-dimensional (2-D) carrier/dopant distribution is becoming increasingly important. However, traditional methods like SRP and SIMS cannot be applied to these non-classical MOSFET structures. Scanning probe microscopy might be a possible solution to measure the 2-D carrier concentration of a device's cross section. Thus, Kelvin-probe force microscopy (KPFM) [61-62] was used to measure the 2-D carrier concentration of a p-n junction in our report.

## 1-4 Thesis Organization

There are seven chapters in this dissertation. In chapter 1, a brief review of the scaling down issues of metal silicide and S/D junctions is given. The motivation for the thesis is also described.

In chapter 2, the thermal stability of NiSi with Ge ion implantation (Ge I/I) is investigated. The energies and dosages of Ge I/I before and after silicide formation are examined to test the efficiency improvement. Applications on differential substrates for poly-Si and bulk-Si are also carried out. The sheet resistance, SEM, TEM, AFM, SIMS, and XRD are employed to examine the thermal stability of NiSi.

In chapter 3, we show how the best Ge I/I condition in chapter 2 is applied to

junction fabrication. The electrical characteristics of $p^+$-n and $n^+$-p junctions with Ge I/I are investigated in detail. We also discuss the temperature and time effects for the junction leakage. The contact resistance between the NiSi and $p^+$ Ge I/I layer is measured by the CBKR structure.

In chapter 4, the ITS technology is utilized in the fabrication of MSB $p^+$-n and $n^+$-p lateral junctions on SOI. The electrical characteristics of MSB $p^+$-n and $n^+$-p junctions are discussed. Different temperatures and durations are used to examine the dopant segregation efficiency. The interface trap density between the Si and $SiO_2$ of the MSB $p^+$-n and $n^+$-p junctions is also measured. Charge pumping and gated-diode methods are used to measure the interface trap density. Here, we also report the fabrication of MSB $p^+$ and $n^+$ contacts on SOI and measure their contact resistivity with different contact areas.

In chapter 5, the 2-D carrier/dopant profiling technique using the Kelvin-probe force microscopy (KPFM) method is first explained. To measure the surface potential, a feedback control circuit is fabricated to improve the signal response speed. The effect of the surface treatment on the surface potential image is also studied. Then the correlations between the surface potential difference measured by KPFM and the surface carrier/dopant concentration obtained by spreading resistance profiling technique, capacitance-voltage method, and secondary ion mass spectroscopy analysis are established.

Finally, in chapter 6, we summarize the important conclusions obtained in this dissertation. Some worthwhile works are suggested for the future.

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Table 1-1 Variations of circuit performances by constant-field and constant voltage scaling method. [5]

| Parameter | Constant-Field Scaling | Constant-Voltage Scaling |
|---|---|---|
| Dimensions | 1/k | 1/k |
| $V_{DD}$ | 1/k | 1 |
| Field | 1 | k |
| Vt | 1/k | 1 |
| Current | 1/k | 1 |
| Capacitance | 1/k | 1/k |
| Delay Time | 1/k | $1/k^2$ |
| Power/Circuit | $1/k^2$ | k |
| Power/Area | 1 | $1/k^3$ |
| Line Resistance | k | k |
| RC | 1 | 1 |
| $IR/V_{DD}$ | k | $k^2$ |

Table 1-2 ITRS roadmap 2008 Edition. [6]

| Year of production | 2009 | 2010 | 2011 | 2012 | 2013 |
|---|---|---|---|---|---|
| DRAM 1/2 pitch (nm) | 52 | 45 | 40 | 36 | 32 |
| Drain extension $X_j$ for bulk MPU/ASIC (nm) | 11 | 11 | 11 | 10 | 9 |
| Max. parasitic series resistance for bulk NMOS (Ω/□) | 200 | 200 | 200 | 200 | 180 |
| Max. drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/□) | 660 | 680 | 750 | 810 | 900 |
| Contact $X_j$ (nm) for bulk MPU/ASIC | 29 | 26.7 | 24.7 | 22 | 19.8 |
| Allowable junction leakage for bulk MPU/ASIC (μA/μm) | 0.25 | 0.48 | 0.71 | 0.7 | 0.64 |
| Sidewall spacer thickness for bulk MPU/ASIC (nm) | 29 | 26.7 | 24.8 | 22 | 19.8 |
| Max. silicon consumption for bulk MPU/ASIC (nm) | 14.5 | 13.4 | 12.4 | 11 | 9.9 |
| Silicide thickness for bulk MPU/ASIC (nm) | 17.9 | 16.2 | 14.7 | 13 | 12 |
| Contact silicide sheet resistance for bulk MPU/ASIC (Ω/□) | 9.1 | 9.9 | 10.8 | 12.1 | 13.5 |
| Contact Max. resistivity for bulk MPU/ASIC (Ω-cm$^2$) | $1.25 \times 10^{-7}$ | $1.12 \times 10^{-7}$ | $9.87 \times 10^{-8}$ | $9.20 \times 10^{-8}$ | $7.00 \times 10^{-8}$ |

Table 1-3 Basic characteristics of common used metal silicides. [19]

| Silicide | Resistivity (μΩ-cm) | Stable on Si up to (℃) | nm of Si consumed per nm of metal | nm of resulting silicide per nm of metal | Barrier height to n-Si(eV) | Film stress (dyne/cm) |
|---|---|---|---|---|---|---|
| PtSi | 28-35 | ~750 | 1.12 | 1.97 | 0.84 | $1\times10^{10}$ |
| $TiSi_2$(C54) | 13-16 | ~900 | 2.27 | 2.51 | 0.58 | $1.5\times10^{10}$ |
| $TiSi_2$(C49) | 60-70 | x | 2.27 | 2.51 | x | x |
| $Co_2Si$ | ~70 | x | 0.91 | 1.47 | x | x |
| CoSi | 100-150 | x | 1.82 | 2.02 | x | x |
| $CoSi_2$ | 14-20 | ~950 | 3.64 | 3.52 | 0.65 | $1.2\times10^{10}$ |
| NiSi | 14-20 | ~650 | 1.83 | 2.34 | 0.67 | $6\times10^{9}$ |
| $NiSi_2$ | 40-50 | x | 3.65 | 3.63 | 0.66 | x |
| $WSi_2$ | 30-70 | ~1000 | 2.53 | 2.58 | 0.67 | x |
| $MoSi_2$ | 40-100 | ~1000 | 2.56 | 2.59 | 0.64 | x |
| $TaSi_2$ | 35-55 | ~1000 | 2.21 | 2.41 | 0.59 | x |

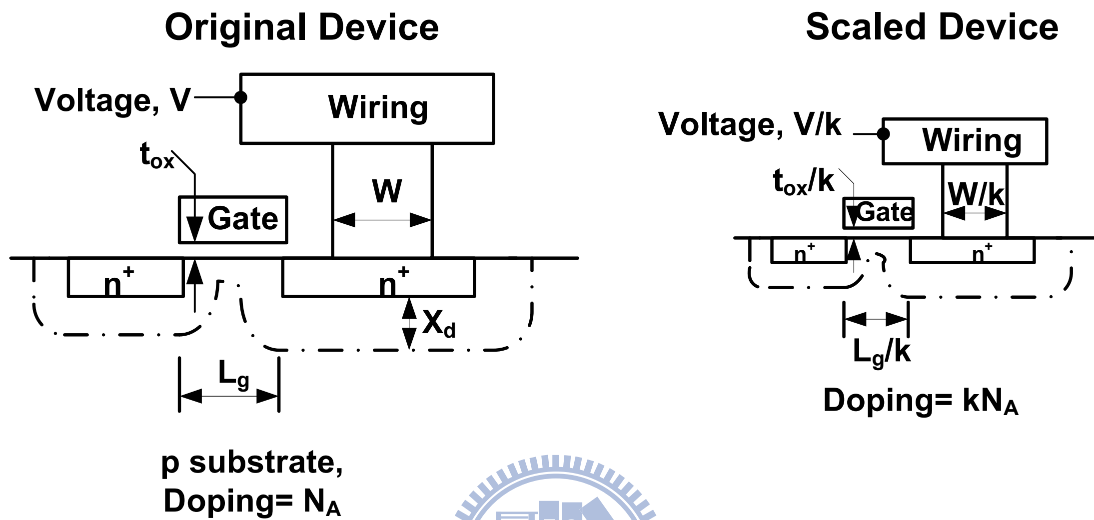
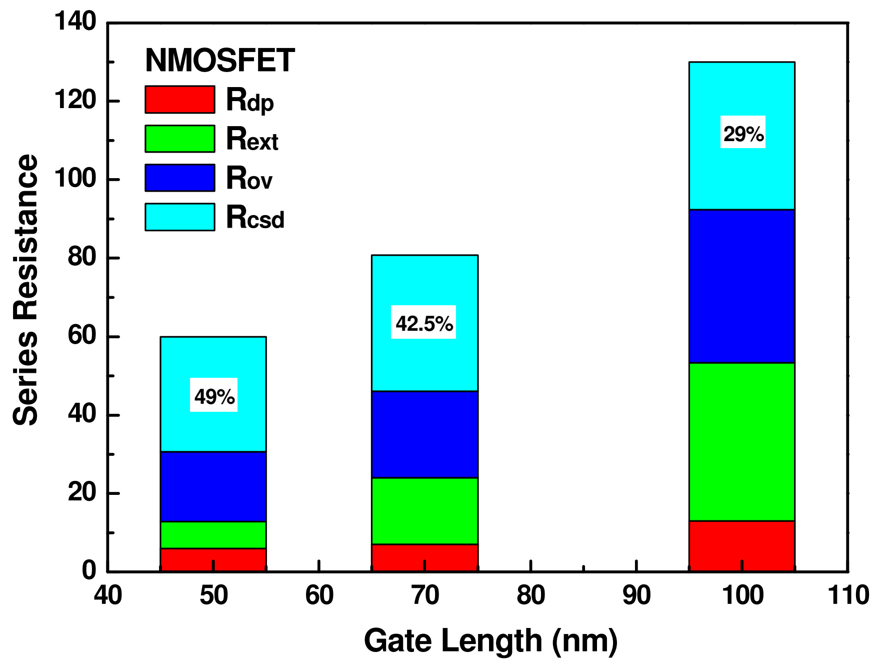
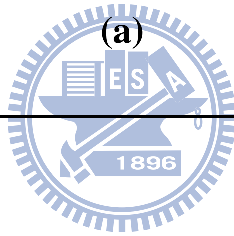
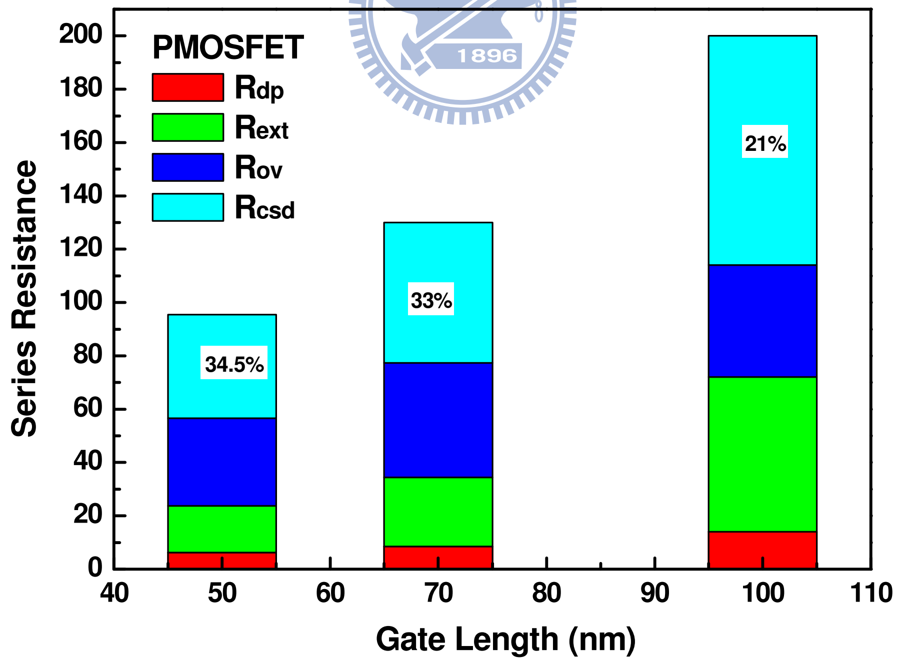


Fig.1-1 Constant-field scaling down of MOSFET. [5]




(a)






(b)

Fig.1-2 Series resistance of (a) NMOS and (b) PMOS transistors with different gate lengths. [29]

# Chapter 2

# Improvement of Nickel Silicide Characteristics with Germanium Ion Implantation

## 2-1 Introduction

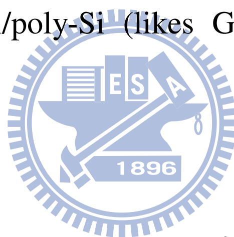
The reactions of Ni and Si for possible use in microelectronic manufacturing have been studied starting in the early 1980s [1,2]. The electrical and mechanical properties of Ni-silicdes depend on the thickness of silicide film and the incorporation of various impurities. The main disadvantage of the nickel monosilicide (NiSi) is its poor thermal stability including thin film agglomeration and high-resistivity phase ($NiSi_2$) transformation. Agglomeration starts with grain grooving in the silicide, followed by grain separation and then forms silicide islands. Some models based on surface/interface energies, grain boundary grooving, and silicide grain size have been proposed to predict the onset of agglomeration on single crystal Si [3-6]. These models involve the following process: dissolution and transport of Si atoms in silicide, precipitation and epitaxial re-growth of Si, and deformation of silicide. Because the NiSi phase is not in equilibrium with Si at high temperature, the expected reaction of NiSi + Si $\rightarrow$ $NiSi_2$ will occur. Similar to the thin film agglomeration, the phase transformation is a nucleation-controlled reaction and depends on silicide thickness, dopant impurities, and annealing ramp rate because of changing activation energies for nucleation. Several methods have been proposed to improve the thermal stability of NiSi film on Si substrate; for example, fluorine ion implantation [7-8], nitrogen ion implantation [9-10], capping layers [11-12], palladium (Pd) incorporation [13], and

platinum (Pt) incorporation [14-17]. Among these methods, Pt incorporated Ni silicide produces the most promising results in terms of NiSi agglomeration and $NiSi_2$ phase transformation. One of the drawbacks of the Pt-incorporation method is the higher resistivity due to Pt doping. Recently, carbon incorporation has been reported to improve the thermal stability of NiSi [18-20], however, the solid-state solubility of C in Si is very low and improper thermal budget after carbon incorporation would produce a large amount of interstitial carbon and result in junction leakage. Since the line width and thickness of NiSi scale down continuously, new technique to improve its thermal stability is required.

In the 1980s, Ge ion implantation was reported as a substrate amorphization technique in order to eliminate dopant channeling effect for shallow junction formation [21-23]. Several investigations regarding to the effects of Ge pre-amorphization implantation (PAI) process on metal-silicide formation have been reported [24-27]. Most of these papers focused on the Ti-silicides and Co-silicides. The formation energy of Ti-silicides is substantially reduced by Ge PAI on Si substrate. Low-resistivity C54-$TiSi_2$ film can be achieved with a lower thermal budget and at 250nm narrows line width [28]. High dose Ge PAI can improve the thermal stability of $TiSi_2$ while low dose ($\leq 1 \times 10^{15}$ $cm^{-2}$) Ge PAI does not play any role [26]. On the other hand, the incorporation of Ge results in an increase in the nucleation temperature of $CoSi_2$ from about 600 °C to about 800 °C which is too high for the manufacturing of advanced devices [27]. The studies of the effects of Ge incorporation on Ni-silcides were reported recently [29-34]. Kittle et al. [29] found that the Ge PAI can increase the $Ni_2Si$ growth rate at 250 °C, and Yun et al. [31] observed that Ge PAI to a dose of $1 \times 10^{14}$ $cm^{-2}$ results in a smooth NiSi/Si interface and suppresses oxidation on arsenic doped $n^+$ Si. However, medium dose Ge PAI did not affect the thermal stability of NiSi. The retardation of phase transformation from

NiSi to $NiSi_2$ was found on the $Si_xGe_{1-x}$ structure [32]. Although $NiSi_2$ phase transformation can be suppressed, the NiSi agglomeration and Ge out-diffusion on $Si_xGe_{1-x}$ substrate during Ni silicide formation are worse than those on Si substrate at low temperature [33]. Kim et al. reported that a thin Si capping layer on $Si_{0.81}Ge_{0.19}$ substrate can improve the NiSi(Ge) agglomeration temperature due to the strain effect [34].

According to the above reports, Ge incorporation to a suitable concentration may benefit the thermal stability of NiSi films but the effect of Ge incorporation on the NiSi-contacted shallow junction has not been investigated. Moreover, Ge incorporation by high dose ion implantation has not been employed. In this chapter, a thorough study on the thermal stability improvement of the NiSi/Si (likes Source/Drain regions) and NiSi/poly-Si (likes Gate region) structure by Ge ion implantation has been carried out.




## 2-2 Samples Preparation and Experimental Procedures

### 2-2-1 Ni-Silicides on Bulk-Si Substrate

The starting materials were boron-doped 6-inch (100) Si wafers with resistivity of 15~25 Ω-cm. Wafers are divided into two categories: GIBS and GIAS.

1. GIBS (Ge Implantation Before Silicidation) sample preparation: After initial clean, a 20 nm thick screen oxide was thermally grown on blanket wafers. Some of the blanket samples were implanted by Ge ions at 20 keV or 50 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$ or $1 \times 10^{16}$ $cm^{-2}$. The projected ranges ($R_p$) of Ge implantation at 20 keV and 50 keV are about 5 nm and 25 nm below the Si surface as simulated by the Monte Carlo method, respectively. For the 20 keV samples, the Ge implanted layer would be

fully consumed during silicide formation. After removing the oxide screen layer, the Ni/TiN (25 nm/5 nm) films were deposited on all of the blanket samples by a high vacuum physical vapor deposition system (HV-PVD). A two-step silicidation process was employed to form the NiSi film [35]. The silicidation step was including annealed at 300 °C for 60 min in vacuum, and the capping layer TiN and un-reacted Ni were selectively removed by immersing in sulfuric peroxide solution ($H_2SO_4$:$H_2O_2$ = 3:1) for 10 min. Then GIBS samples were received 2nd rapid thermal annealing (RTA) in $N_2$ ambient at different temperatures for different times.

2. GIAS (Ge Implantation After Silicidation) sample preparation: After initial clean, 25 nm thick Ni film was deposited on blanket wafers. Then we did 1st annealing process at 300 °C for 60 min in vacuum and the 2nd RTA at 600 °C for 30 s in $N_2$ ambient was done for these samples. Following, they were implanted by Ge ions at 40 keV to a dose of $5 \times 10^{15}$ and $1 \times 10^{16}$ $cm^{-2}$. The $R_p$ was about 17 nm below the NiSi surface and all of the Ge ions were located in the NiSi layer. The GIAS samples were then received RTA in $N_2$ ambient at different temperatures for different times.

Table 2-1 lists the process conditions of the GIAS and GIBS samples. We also fabricated "Control sample" followed the above process except Ge ion implantation.

### 2-2-2 Ni-Silicides on Heavily Doped Si Substrate

After considering the results of 2-2-1, only GIBS method was used to fabricate the following samples because this method results in better thermal stability than the GIAS method. And the implantation energy was decreased to instead screen oxide for preventing oxygen atoms knock-in during Ge ion implantation. So the implantation energy was reduced to 30 keV to obtain an $R_p$ of about 26 nm below the Si surface and dosage was set to $1 \times 10^{16}$ $cm^{-2}$. Here, two kinds of categories: 1. Junction and 2. Gate samples were fabricated. In all of them Ge ion implantation was done before $n^+$

or $p^+$ heavily doping.

1. Junction sample preparation: In order to form $n^+$-p and $p^+$-n junctions, $As^+$ and $BF_2^+$ ions were implanted on opposite type (100) Si wafers at 35 keV and 20 keV, respectively, to a dose of $5 \times 10^{15}$ $cm^{-2}$. A spike annealing at 1050 ºC was performed to activate the dopants and annihilate the ion implantation induced defects. After HF-dipping, the Ni/TiN (25 nm/5 nm) films were deposited on gate samples by HV-PVD. Then junction samples were followed 1st silicidation process and then received 2nd RTA in $N_2$ ambient at different temperatures for different times.

2. Gate sample preparation: After RCA cleaning process, a 100 nm thermal oxide was grown on p type (100) Si wafers. An un-doped 200 nm a-Si gate layer was stacked on thermal oxide in a low pressure chemical vapor deposition (LPCVD) system at 550 $^oC$. Then samples were prepared to be implanted by Ge and different type heavily doping. We implanted $As^+$ ions at 35 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$ preparing $n^+$ doping gates, and implanted $BF_2^+$ ions at 30 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$ preparing $p^+$ gates. All the samples were annealed at 950 $^oC$ for 30 sec for dopant activation and crystallization of the poly-Si gate. After HF-dipping, the Ni/TiN (25nm/5 nm) films were deposited on gate samples by HV-PVD. But we let all gate samples were just annealed at different temperatures for 30 s by RTA in $N_2$ ambient and stripped un-reacted metal.

Table 2-2 lists the process conditions of the junction samples. Table 2-3 lists the process conditions of the gate samples. We also fabricated “Control sample” followed the above process except Ge ion implantation.

### 2-2-3 Material Analysis

Surface morphology was inspected by a scanning electron microscope (SEM). Cross-sectional micro-structure was inspected by a transmission electron microscope

(TEM). Interface roughness was analyzed by an atomic force microscope (AFM). Phases of Ni-silicide were identified by X-ray diffraction (XRD). Depth profiles of species were analyzed by a Secondary Ion Mass Spectroscope (SIMS). The sheet resistance ($R_s$) of silicide was measured by a four-point probe system.

## 2-3 Results and Discussion

### 2-3-1 Ni-silicides on Bulk-Si Substrate

Fig.2-1 shows the normalized sheet resistance values of the GIBS samples after annealing at different temperatures for 10 s. The sheet resistance values were normalized with those of the 500 °C annealed samples. The samples with annealing temperature lower than 700 °C have similar sheet resistance values of around 4~6 Ω/□. Either higher energy or higher dose of Ge ion implantation (Ge I/I) results in better thermal stability. The sheet resistance value of the sample with Ge I/I at 20 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$ increases apparently after annealing at 750 °C. By increasing the Ge dose to $1 \times 10^{16}$ $cm^{-2}$, the sustainable temperature can be increased to 750 °C. The samples with Ge I/I at 50 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$ exhibit a similar thermal stability of 750 °C in terms of the sheet resistance value. When increasing the dose to $1 \times 10^{16}$ $cm^{-2}$, the sheet resistance value does not degrade even after annealing at 850 ºC for 10 s. The GIAS samples exhibit the same trend, i.e., a higher Ge I/I dose results in better thermal stability. As shown in Fig.2-2, when the dose increases from $5 \times 10^{15}$ $cm^{-2}$ to $1 \times 10^{16}$ $cm^{-2}$, the sustainable temperature increases from 750 °C to 800 °C. It should be noted that the GIBS samples have better thermal stability than the GIAS samples. These observations imply that Ge I/I can improve the thermal stability of the NiSi/Si structure, and that the reason should be related to the Ge concentration at the

NiSi/Si interface.

As the annealing time is increased to 30 s, the GIBS samples still show better thermal stability than the GIAS samples, as shown in Fig.2-3. It is also observed that the sustainable temperature degrades upon increasing the annealing time. For example, the sustainable temperature of the GIBS sample with Ge I/I at 50 keV to a dose of $1 \times 10^{16}$ $cm^{-2}$ decreases from 850 ºC to 800 ºC upon increasing the annealing time from 10 s to 30 s. A similar 50 ºC reduction in the sustainable temperature is observed for the GIAS samples.

Two mechanisms are expected to increase the sheet resistance value of the Ni-silicide film. When the agglomeration of the silicide film occurs, the silicide film first breaks and then becomes discontinuous. In this case, the sheet resistance value increases apparently. On the other hand, the silicide phase may transform from NiSi to $NiSi_2$ at high temperature. Although the resistivity of $NiSi_2$ is higher than that of NiSi, the thickness is also increased, so that the increase in the sheet resistance value is moderate. Therefore, the actual mechanisms for the sheet resistance behavior observed in Fig.2-3 were clarified by SEM inspection and XRD analysis.

Fig.2-4 shows the surface morphologies of the control sample, GIBS, and GIAS under the same conditions as Fig.2-3. The control sample agglomerates at 700 ºC. However, the 750 ºC-annealed GIBS sample still exhibits a very smooth surface. The agglomeration phenomenon is observed on the 800 ºC-annealed GIBS sample. The GIAS also starts agglomerating at 750 ºC, and becomes a rough NiSi island at 800 ºC. It is clear that Ge-ion implantation can effectively suppress agglomeration. Fig.2-5~Fig.2-7 show the XRD spectra of the control sample, GIBS, and GIAS, respectively. In the Ge I/I samples, the NiSi phase remains stable up to 800 ºC even if agglomeration has occurred at this temperature. Furthermore, the $NiSi_2$ transformation is observed in the GIBS and GIAS at 850 ºC, which is higher than in the control

sample. This result indicates that the Ge I/I can retard the phase transformation from NiSi to $NiSi_2$, and that the phase transformation occurs behind the agglomeration on samples with high-dose Ge-ion implantation.

Another advantage of Ge I/I on a NiSi/Si structure is the smooth NiSi/Si interface. Fig.2-8 shows a cross-sectional TEM micrograph of the GIBS sample with Ge I/I at 50 keV to a dose of $1 \times 10^{16}$ $cm^{-2}$ after annealing at 750 ºC for 30 s. The NiSi/Si interface is still quite smooth, which is consistent with the high agglomeration temperature in Fig.2-3. The thickness of the NiSi film is 45 nm, which translates to a resistivity of 21 μΩ-cm. This value is slightly higher than the bulk value, but is much lower than the resistivities of $NiSi_xGe_{1-x}$ and Ni(Pt)Si. Fig.2-9 shows the SIMS depth profile of the Ge in the GIBS samples with Ge I/I at 50 keV to a dose of $1 \times 10^{16}$ $cm^{-2}$ after annealing at 600 °C for 30 s. The $R_p$ of Ge implantation exists at 25 nm below the Si surface, and the NiSi grew over the depth of $R_p$. A large number of Ge atoms were pushed into the Si with the NiSi growth and piled up at the NiSi/Si interface. It is suspected that the improved thermal stability and smooth interface are correlated to the high concentration of Ge atoms at the interface.

Table 2-3 summarizes the agglomeration and phase transformation temperatures of the control samples, GIBS sample, and GIAS sample. The mechanisms for improving the agglomeration temperature are discussed next. It has been reported that ion implantation before the silicidation process has two main effects on silicide formation: pre-amorphization of the substrate, like $Ar^+$ and $N_2^+$ implantation, and a change in the surface/interface energy, likes $F^+$ and $N_2^+$ implantation. The Ge I/I produces a uniform amorphous layer because ion implantation is a uniform process. The low-temperature first step annealing process causes the Ni to uniformly react with the amorphous Si layer. The NiSi growth rate on the amorphous Si region is higher than that on the crystalline Si region. Once the NiSi front edge reaches the

amorphous/crystalline interface, the growth rate is retarded. Therefore, a smooth NiSi/Si interface is obtained even at 750 °C. In addition to the efficiency of pre-amorphization, the high concentration of Ge also retards the Ni-silicide growth rate [36]. As the Ni-silicide grows, Ge atoms are repelled out of the silicide layer and pile up at the silicide/Si interface. The Ge concentration can auto-adjust the Ni-silicide growth rate to produce a smooth interface. The high-dosage Ge implantation results in a small and uniform grain size, which is kinetically more stable. Therefore, the agglomeration temperature can be improved. The GIBS samples have better thermal stability than the GIAS samples because the GIAS process incorporates less Ge in the NiSi/Si interface, as seen in Fig.2-10, compared to Fig.2-9. The implanted Ge diffused out the NiSi during post-annealing of GIAS sample, so that only a few Ge atoms were finally segregated to the NiSi/Si interface. The piled-up Ge atoms change the NiSi/Si interface energy so that the NiSi agglomeration at high temperature is suppressed. Similar results can be observed for various silicide/Si structures by $F^+$ or $N_2^+$ implantation [10-13]. Higher ion implantation energy and dose result in a higher Ge concentration at the NiSi/Si interface, which implies that the sustainable temperature will be higher. This was confirmed by our results.

From the classical nucleation theory, the improvement in thermal stability can be explained by the change in mixing entropy, which raises the activation energy barrier for nucleation. The formation energy of $Ni_2Si$ (-142.7 kJ/mol) is more negative than that of $Ni_2Ge$ (-37 kJ/mol), and the Ge atoms were segregated to the NiSi/Si interface during silicide formation [37]. The piled-up and segregated Ge atoms act as a barrier to suppress Ni diffusion toward the Si substrate. This implies less driving force for silicide island grooving, which in turn prevents agglomeration. The high resistance to agglomeration is also attributed to the retardation of the $NiSi_2$ grain growth. The $NiSi_2$ formation was assumed to be a nucleation controlled reaction, with $\Delta G$ as the Gibbs

free energy of the reaction: NiSi + Si → $NiSi_2$. Since the piled-up and segregated Ge atoms can retard the reaction, the absolute value of the new ΔG* will decrease and raise the activation free energy for nucleation. Hence, as the agglomeration is suppressed, the phase transformation from NiSi to $NiSi_2$ is also suppressed. Similar results have been reported for Pt-incorporated NiSi film [15,17].

## 2-3-2 Ni-Silicides on Heavily Doped Bulk-Si Substrate

For junction samples, Fig.2-11(a) and Fig.2-12(a) show the normalized sheet resistance value as a function of the annealing temperatures of the NiSi-contacted $n^+$-p and $p^+$-n junctions, respectively. The improvement in thermal stability by Ge I/I presented in the previous sub-section is almost eliminated in the $n^+$-p junction samples. From Fig.2-11(b) and Fig.2-12(b), the agglomeration phenomenon occurs after annealing at temperatures higher than 700 °C for $n^+$-p and 750 °C for $p^+$-n junction samples. We postulate that the cluster defects due to the high-dose $As^+$ ion implantation change the interface energy so that agglomeration occurs earlier than in the control sample. The segregated Ge atoms at the NiSi grain boundaries still suppress the phase transformation from NiSi to $NiSi_2$, while the XRD analysis in Fig.2-13 indicates that the phase transformation from NiSi to $NiSi_2$ does not occur even at 850 °C for Ge I/I junctions. In the $p^+$-n junction samples, the agglomeration may be improved by either F- or Ge-incorporation [10,11,38]. The phase transformation of the sample without Ge I/I occurs at 750 ºC (XRD data not shown), which is consistent with the published data. These results indicate that Ge-incorporation is better than F-incorporation in terms of raising the phase transformation temperature. Fig.2-14 shows cross-sectional TEM micrographs of the $n^+$-p and $p^+$-n samples with Ge I/I after annealing at 600 °C for 30 s. The NiSi thickness of the $p^+$-n and $n^+$-p junctions with Ge I/I after annealing at 600 °C for 30 s

is about 20 nm and 36 nm, respectively. The different thickness of NiSi was influenced by the non-uniformity of HV-PVD or RTA equipments. The thinner NiSi thickness of the NiSi on the $p^+$-n sample explains the poorer thermal stability compared to the Ge I/I only sample, as shown in Fig.2-12. The resistivity of the 500 °C annealed $n^+$-p junction with Ge I/I is 19.8 μΩ-cm. In Fig.2-14, we see that the smooth NiSi/Si interface is still improved, as in the previous result. To quantify the interface roughness, the NiSi film was removed and the Si surface was scanned by AFM. With Ge I/I, the roughness decreases from 1.50 nm to 0.85 nm and from 2.23 nm to 1.61 nm on $n^+$ and $p^+$ Si, respectively.

### 2-3-3 Ni-Silicides on Heavily Doped Poly-Si Gate

For gate samples, Fig.2-15 shows the sheet resistance of NiSi films on $n^+$ and $p^+$ poly gates for samples with Ge I/I and without Ge I/I as a function of the temperature for RTA for 30 s. The sheet resistance of all the samples after the 550 °C 30s RTA process is 5~6 Ω/□. In the gate samples without Ge I/I, the measured sheet resistance values of the NiSi after annealing at 650 °C for the $n^+$ gate sample and 700 °C for the $p^+$ gate sample are double the values for 550 °C. Thus, the NiSi on the $p^+$ gate sample has a higher thermal stability temperature than on the $n^+$ gate sample. This is often explained due to the $F^+$ from the $BF_2^+$ implant, because $F^+$ can slightly suppress the NiSi agglomeration. In the Ge I/I gate samples, the sheet resistance of the NiSi increased after annealing above 750 °C for the $n^+$ sample and 800 °C for the $p^+$ sample. The sheet resistance values of the NiSi at 750 °C on the $n^+$ and $p^+$ Ge I/I gate samples are just 6.2 Ω/□ and 8.4 Ω/□, respectively. This shows that the thermal stability is clearly improved in the Ge I/I gate samples. The maximum temperature with no increase in sheet resistance is increased by about 100 °C.

The situation for a Ni-silicide film on poly-Si is much more complex than for the

bulk-Si. Silicide grain boundary grooving, island formation, silicide inversion, and deformation due to poly-Si grain growth can occur nearly simultaneously. The agglomeration of NiSi on the poly-Si occurs because both the poly-Si and silicide grows vertically through the whole structure, and a nearly continuous silicide layer is reestablished under the poly-Si layer, called "inversion" [39]. The increase in sheet resistance at 750 °C for the $p^+$ gate samples without Ge I/I is due to a discontinuous agglomeration silicide layer during inversion. The sheet resistance is reduced when a continuous silicide layer is re-established and extends vertically through the whole structure. The reestablished silicide layer includes the transformation to $NiSi_2$ [36]. From the XRD analysis results, as shown in Fig.2-16(a), we can see that the NiSi started to transform into the $NiSi_2$ phase at 700 °C in the $p^+$ gate samples without Ge I/I. Although the resistivity of $NiSi_2$ is higher than that of NiSi, the thickness of the $NiSi_2$ is greater than that of the NiSi. Thus, we can see a decrease in the sheet resistance on the $p^+$ gate sample without Ge I/I between 750 and 800 °C. In Fig.2-16(b), the $NiSi_2$ transformation occurs at 800 °C for the $p^+$ Ge I/I gate samples. The temperature of the $NiSi_2$ transformation is also increased by the Ge I/I by 100 °C.

The plan-view SEM images of NiSi films after the $n^+$ gate samples were annealed for 30 s at various RTA temperatures are shown in Fig.2-17; $p^+$ gate samples are shown in Fig.2-18. As shown in Fig.2-17, we can see that the NiSi in the $n^+$ gate samples without Ge I/I is already agglomerated and becomes a rough discontinuous surface at 700 °C. However, the NiSi in $n^+$ gate samples with Ge I/I just begins to agglomerate at 750 °C. A similar trend is observed in the $p^+$ gate samples, as shown in Fig.2-18. The NiSi on $p^+$ gate samples without Ge I/I formed small nucleated pits at 700 °C and then agglomerated at 750 °C. The NiSi on $p^+$ Ge I/I gate samples just began to agglomerate at 850 °C. The agglomerated and discontinuous NiSi has a higher resistivity, as seen in Fig.2-15, which was consistent with the SEM images.

The cross-sectional view SEM images of NiSi for $n^+$ and $p^+$ on Ge I/I gate samples after 30 s of annealing at various RTA temperatures are shown in Fig.2-19. In Fig.2-20, the NiSi in the $n^+$ Ge I/I gate samples annealed at 750 °C is beginning to grow along the poly-Si grain boundaries and the NiSi/poly-Si interface becomes rough. Finally, the silicide becomes laterally discontinuous islands. This condition is often called “mixing.” It commonly occurs on silicides at high temperature, causing an increase in $R_s$ [6]. Thus, when the NiSi on the $n^+$ Ge I/I gate samples shows a serious discontinuous silicide layer at 800 °C, the measured sheet resistance is increased to 296 Ω/□. The behavior of the NiSi in the $p^+$ Ge I/I gate samples is similar to that for $n^+$; the NiSi begin to grow thicker and the NiSi/poly-Si interface becomes rough at 800 °C. Because the agglomeration of NiSi is retarded by Ge I/I, the transformation from NiSi to $NiSi_2$ and the silicide thickness increase dominate the sheet resistance at high temperatures in the $p^+$ Ge I/I gate samples.

We have shown the advantages of Ge I/I in suppressing agglomeration and $NiSi_2$ transformation. From the measured sheet resistance results, SEM inspections, and XRD results, the allowable temperature of NiSi for $n^+$ poly gates is improved from 650 °C to 750 °C, with an improvement from 700 °C to 800 °C for $p^+$ poly gates. Fig.2-20 shows the SIMS analysis results for Ge I/I on an $n^+$ gate after silicide formation at 650 °C RTA for 30 s. The implanted and segregated Ge atoms around $R_p$ become a barrier suppressing Ni diffusion along the poly-Si grain boundaries. We think that the thermal stability improving mechanism and results on poly-Si are much the same as those on bulk-Si.

## 2-4 Conclusions

The sustainable process temperature of a GIBS sample, considering the thin film agglomeration and phase transformation, can be improved by 50~100 ºC with high-dosage Ge ion implantation at a suitable energy. The GIBS results also show a very smooth NiSi/Si interface. The GIAS process exhibits a similar effect but the performance is not as good as the GIBS process. These observations are explained by the change in surface energy due to the pile-up of Ge atoms at the NiSi/Si interface. Since only a few Ge atoms remain in the NiSi layer, the resistivity of the NiSi film is close to the bulk value. When applying the GIBS method to $n^+$-p and $p^+$-n junctions, the agglomeration temperature of the NiSi on the $n^+$-p junction did not improve due to the cluster defects induced by a high concentration of As atoms. We still see a smooth NiSi/Si interface and a 100 °C increase in the phase transformation temperature with Ge ion implantation.

In a poly-Si gate structure, Ge ion implantation also improves the thermal stability of the NiSi. With high-dosage Ge implantation at a suitable energy, the agglomerated temperature of the NiSi on $n^+$ and $p^+$ poly-Si gates can be increased from 650 °C to 750 °C and from 700 °C to 800 °C, respectively. The phase transformation from NiSi to $NiSi_2$ is also retarded to 800 ºC.

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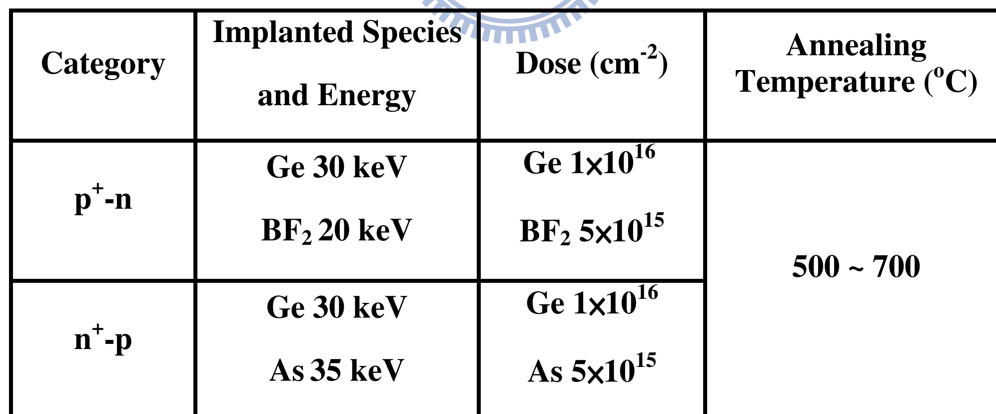
Table 2-1 Process split conditions of the blanket samples.

| Category | Energy(keV) | Dose ($cm^{-2}$) | Annealing Temperature ($^oC$) | Annealing Time (sec) |
|---|---|---|---|---|
| GIBS | 50 , 20 | $5\times10^{15}$<br>$1\times10^{16}$ | 500 ~ 850 | 10, 30, 60 |
| GIAS | 40 | | | |

Table 2-2 Process split conditions of the p-n junction samples.



| Category | Implanted Species and Energy | Dose ($cm^{-2}$) | Annealing Temperature ($^oC$) |
|---|---|---|---|
| $p^+$-n | Ge 30 keV<br>$BF_2$ 20 keV | Ge $1\times10^{16}$<br>$BF_2$ $5\times10^{15}$ | 500 ~ 700 |
| $n^+$-p | Ge 30 keV<br>As 35 keV | Ge $1\times10^{16}$<br>As $5\times10^{15}$ | |

Table 2-3 Process split conditions of the gate samples.

| Category | Implanted Species and Energy | Dose ($cm^{-2}$) | Annealing Temperature ($^{o}C$) |
|---|---|---|---|
| $p^+$-gate | Ge 30 keV<br>$BF_2$ 30 keV | Ge $1\times10^{16}$<br>$BF_2$ $5\times10^{15}$ | 550 ~ 850 |
| $n^+$-gate | Ge 30 keV<br>As 35 keV | Ge $1\times10^{16}$<br>As $5\times10^{15}$ | |

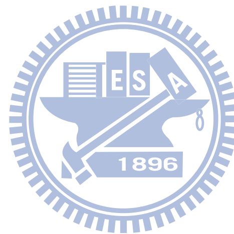



Table 2-4 Summary of the thin film agglomeration temperatures and phase-transformation temperatures of the blanket control samples, GIBS samples and GIAS samples.

| Sample Type | Control Sample | GIAS | | GIBS | |
|---|---|---|---|---|---|
| Ge I/I Energy (keV) | -------- | 40 | | 50 | |
| Ge I/I Dose ($cm^{-2}$) | -------- | $5\times10^{15}$ | $1\times10^{16}$ | $5\times10^{15}$ | $1\times10^{16}$ |
| Agglomeration Temperature | 700 $^{o}C$ | 700 $^{o}C$ | | 800 $^{o}C$ | |
| Phase Transformation Temperature | 750 $^{o}C$ | 850 $^{o}C$ | | 850 $^{o}C$ | |

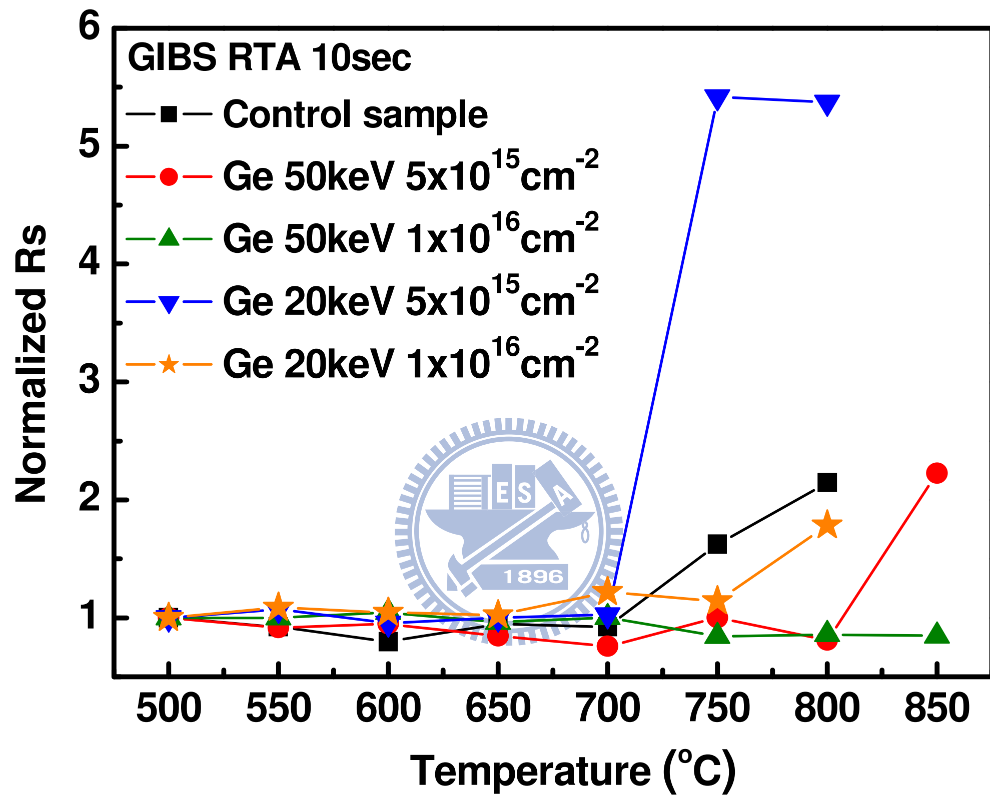



Fig.2-1 Normalized sheet resistance values ($R_s$) of the GIBS samples after annealing at different temperatures for 10 sec. The sheet resistance values are normalized to those of the 500 °C annealed samples.

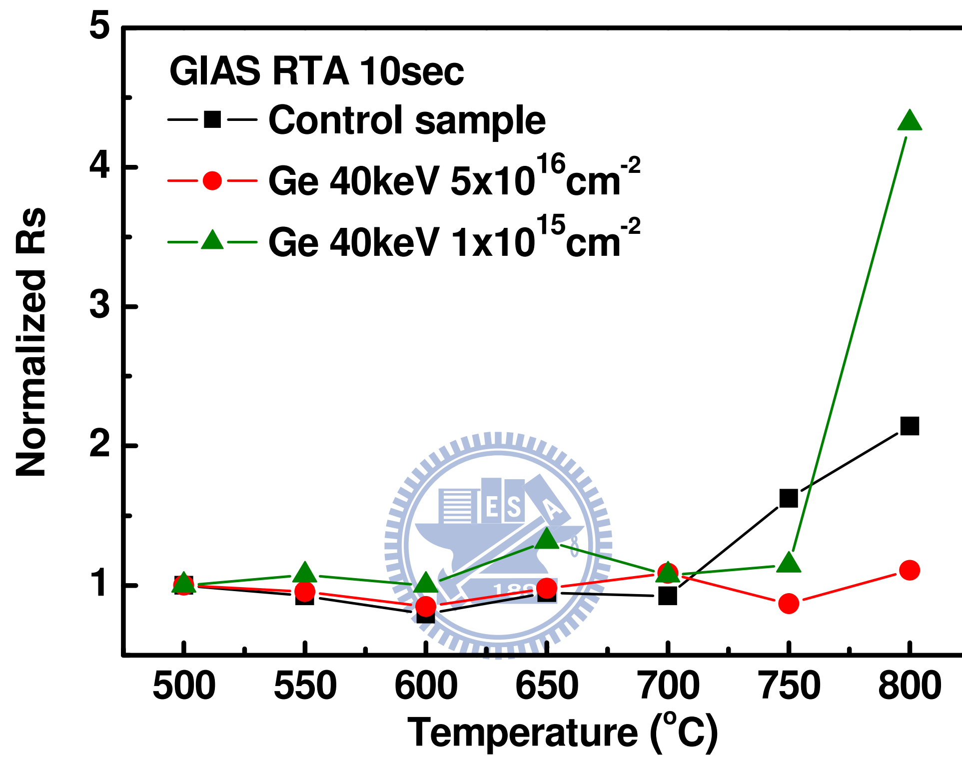



Fig.2-2 Normalized sheet resistance values ($R_s$) of the GIAS samples after annealing at different temperatures for 10 sec. The sheet resistance values are normalized to those of the 500 °C annealed samples.

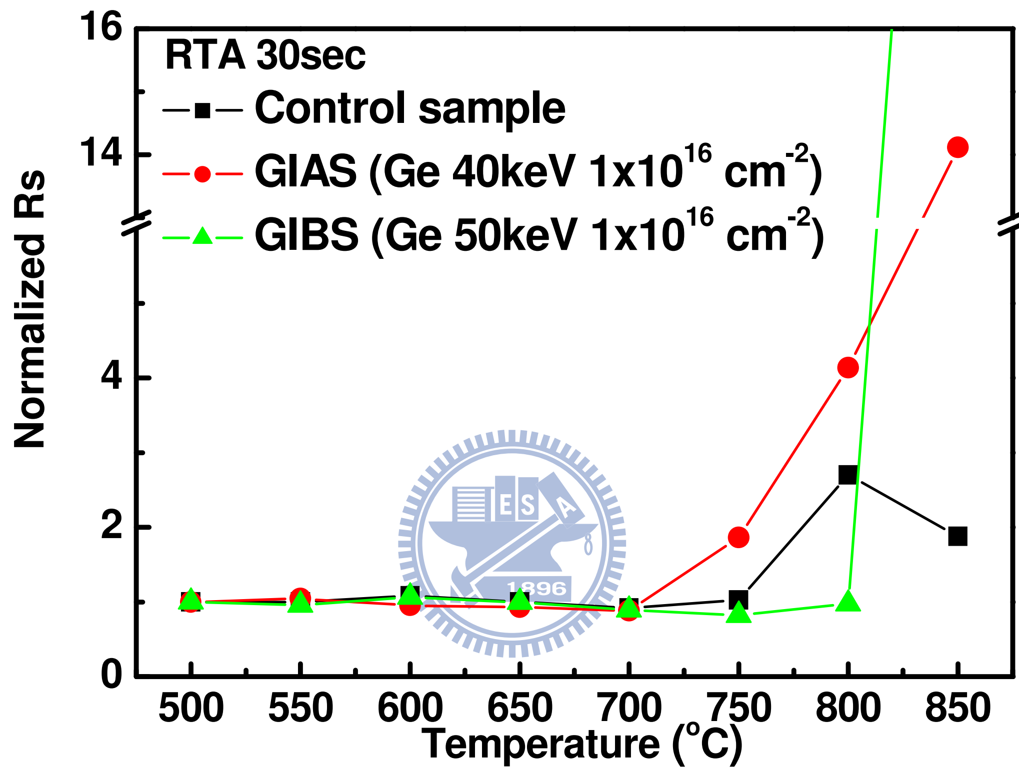



Fig.2-3 Normalized sheet resistance values ($R_s$) of the GIBS and GIAS samples with Ge ion implantation at 40 and 50 keV, respectively to a dose of $1 \times 10^{16}$ $cm^{-2}$. The annealing time is 30 sec. The sheet resistance values are normalized to those of the 500 °C annealed samples.

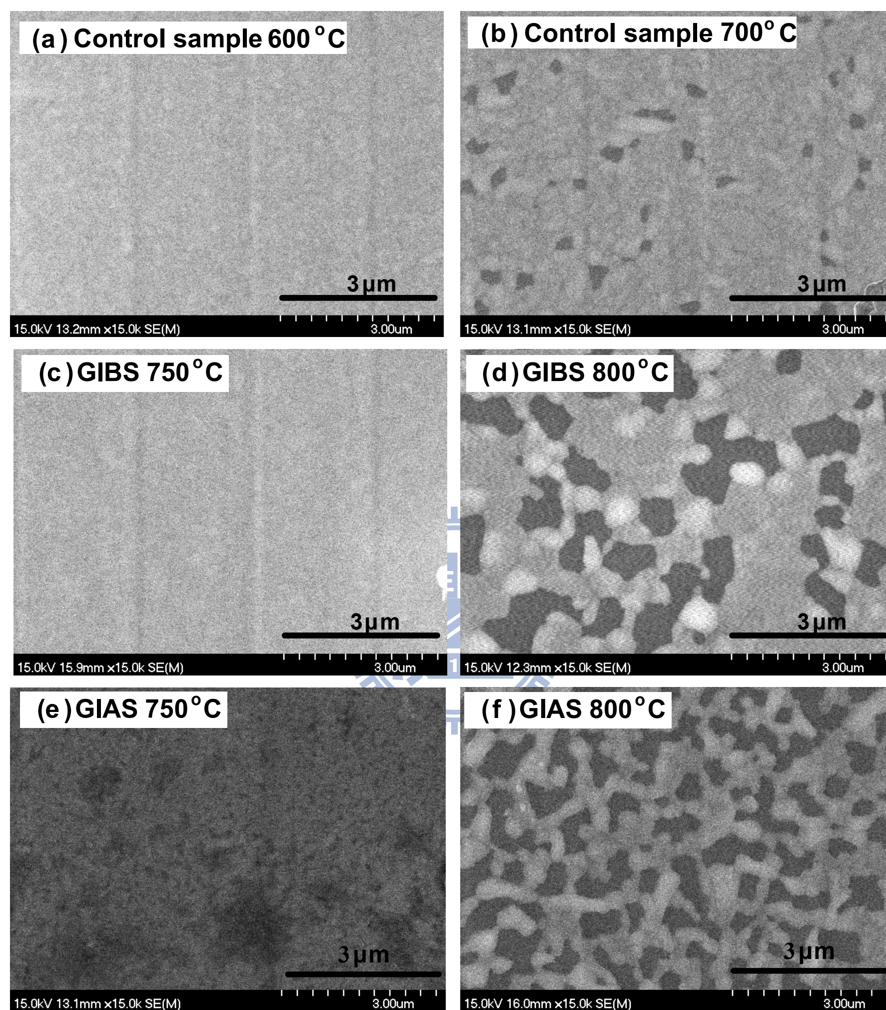



Fig.2-4 Surface morphology inspected by SEM of the control sample, GIBS and GIAS samples after annealing at different temperatures for 30 sec.

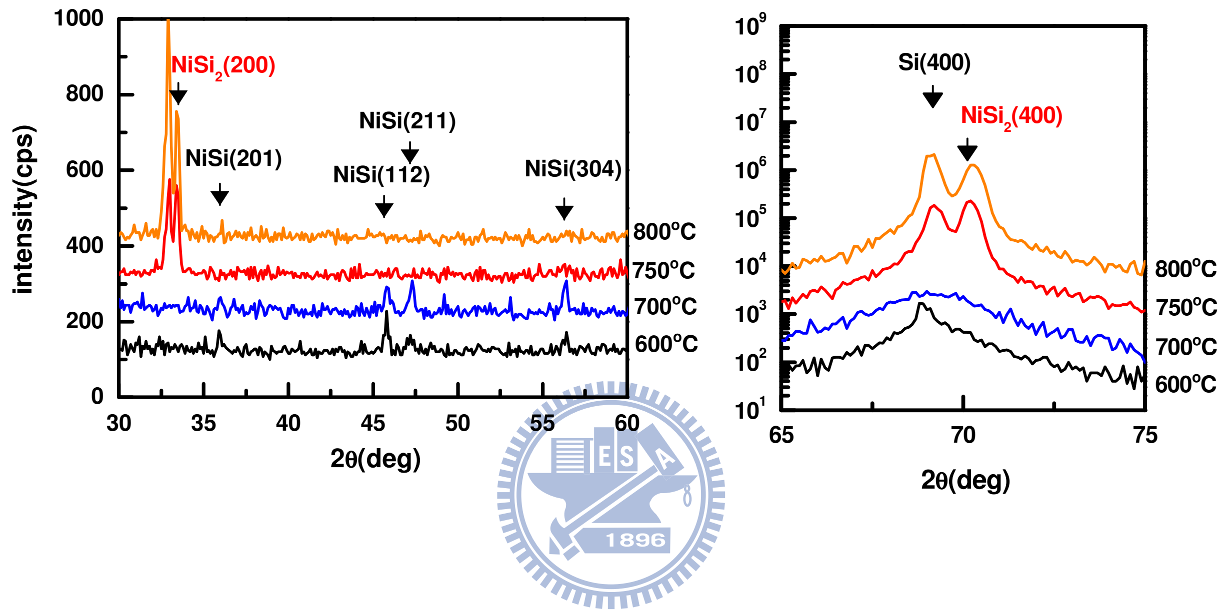



Fig.2-5 XRD spectra of the control sample after annealing at different temperatures for 30 sec.

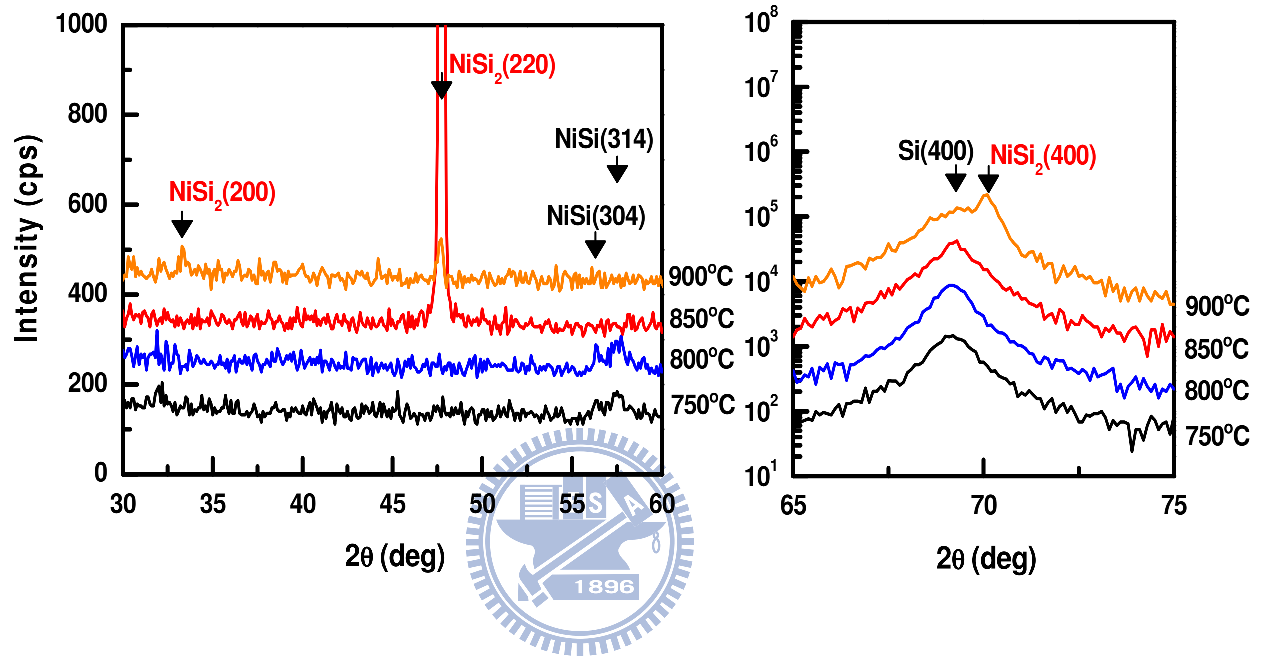



Fig.2-6 XRD spectra of the GIBS samples with Ge ion implantation at 50 keV to a dose of $1\times10^{16}$ $cm^{-2}$ after annealing at different temperatures for 30 sec.

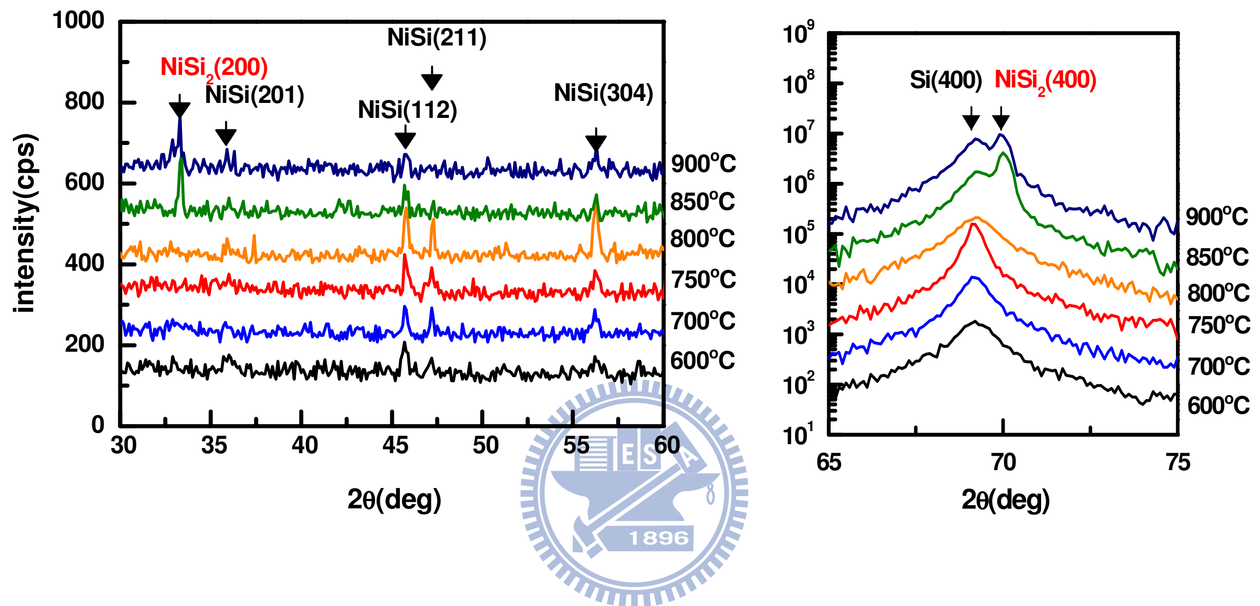



Fig.2-7 XRD spectra of the GIAS samples with Ge ion implantation at 40 keV to a dose of $1\times10^{16}$ cm$^{-2}$ after annealing at different temperatures for 30 sec.

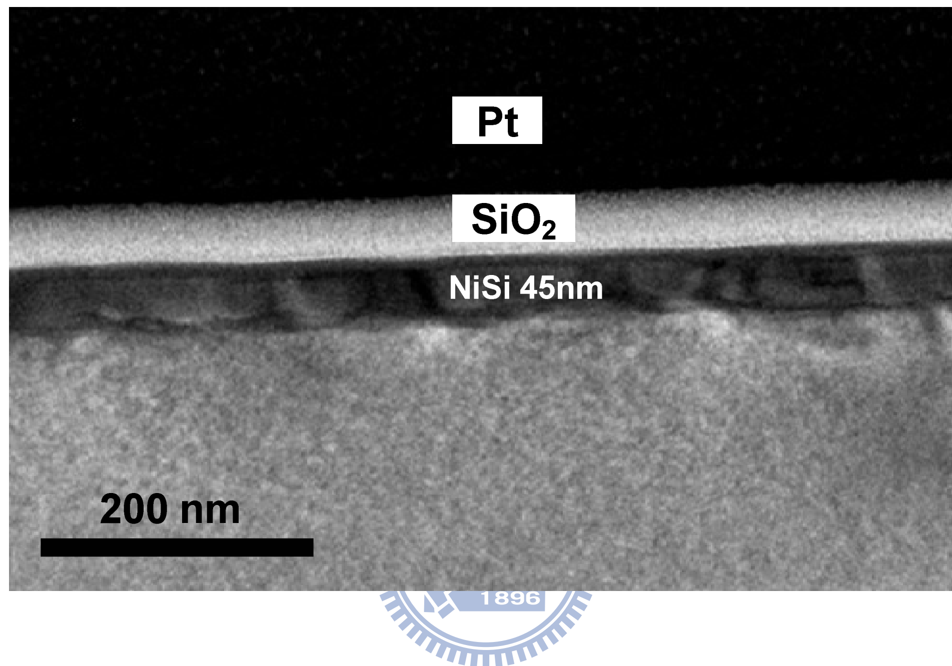



Fig.2-8 Cross-sectional TEM micrograph of the GIBS sample with Ge ion implantation at 50 keV to a dose of $1 \times 10^{16}$ $cm^{-2}$ after annealing at 750 ºC for 30 sec.

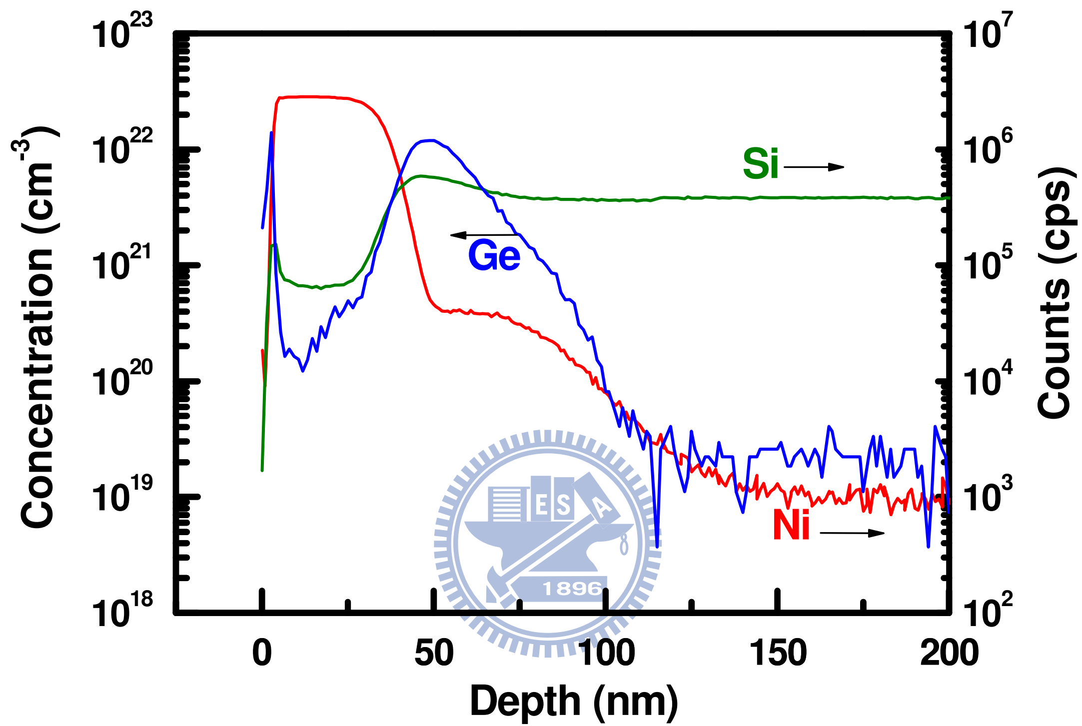



Fig.2-9 SIMS depth profile of Ge atoms of the GIBS samples with Ge I/I at 50 keV to a dose of 1 × $10^{16}$ cm$^{-2}$ after annealing at 600 °C for 30 sec. The depth is measured from the top surface of the NiSi film.

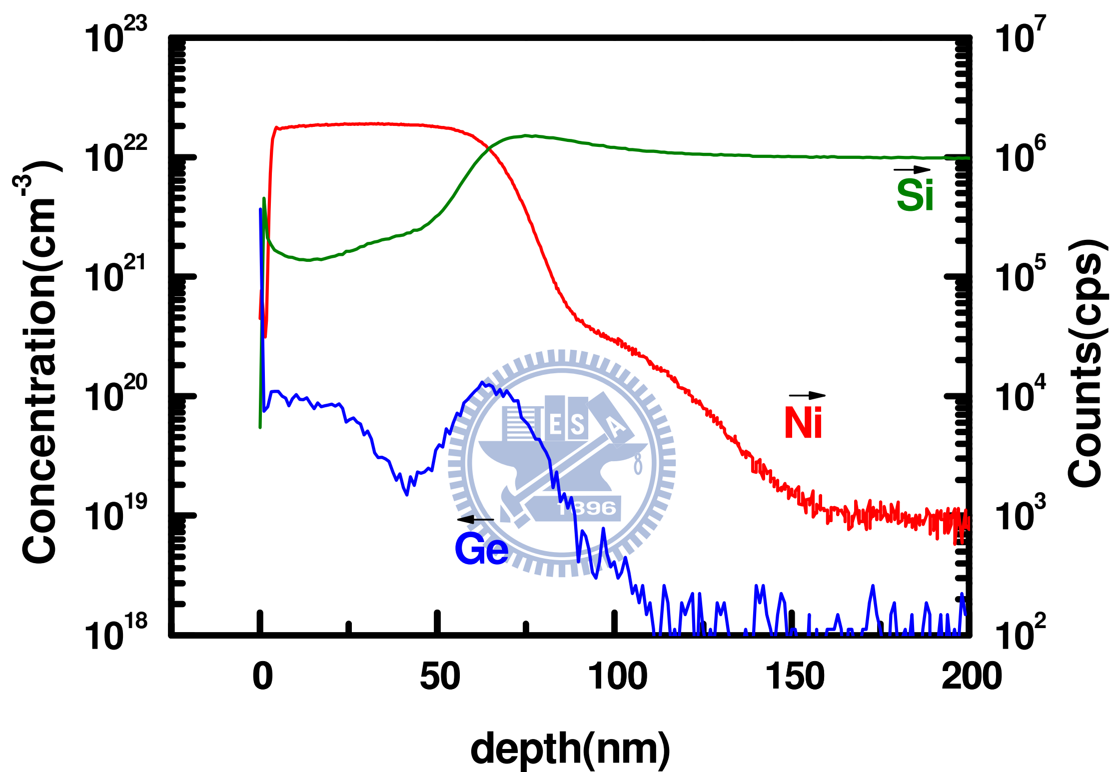
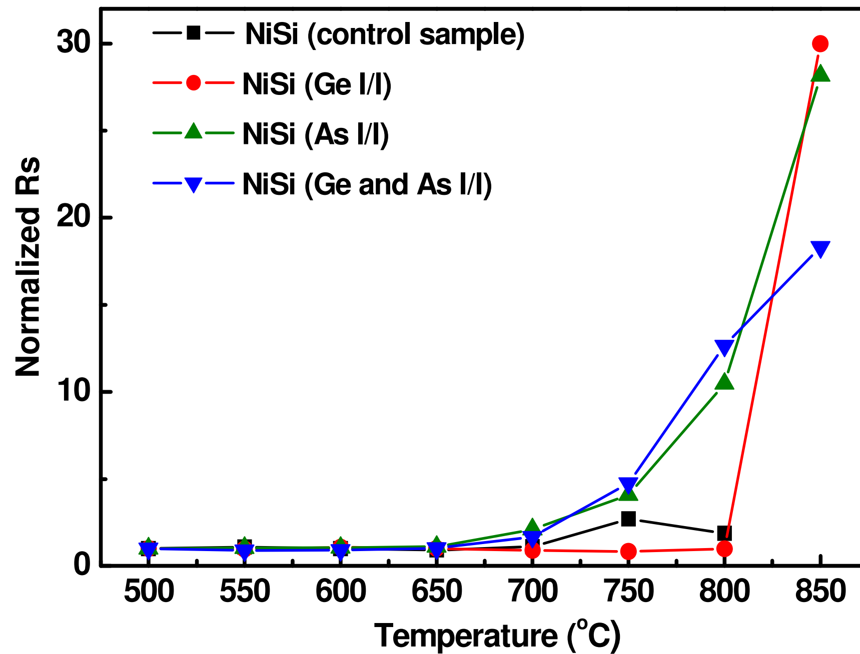
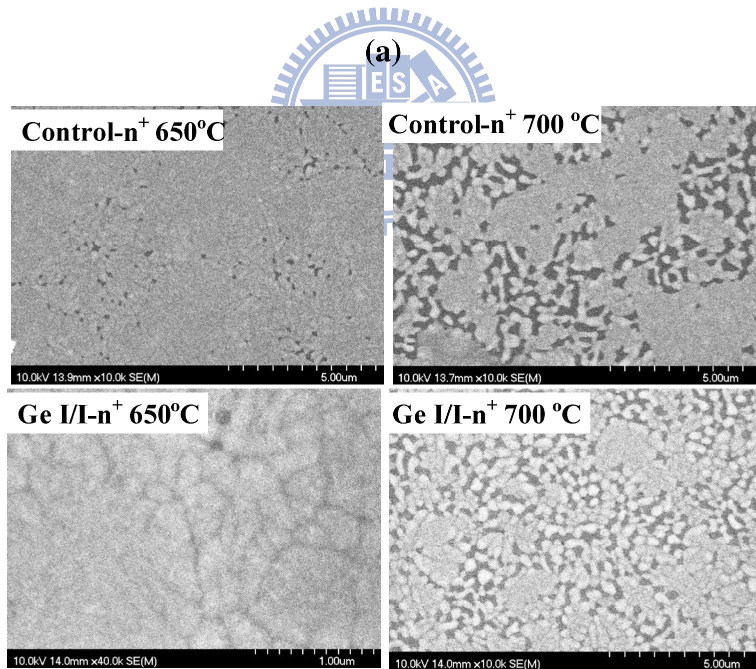



Fig.2-10 SIMS depth profile of Ge atoms of the GIAS samples with Ge I/I at 40 keV to a dose of $1 \times 10^{16}$ cm$^{-2}$ after annealing at 600 °C for 30 sec. The depth is measured from the top surface of the NiSi film.

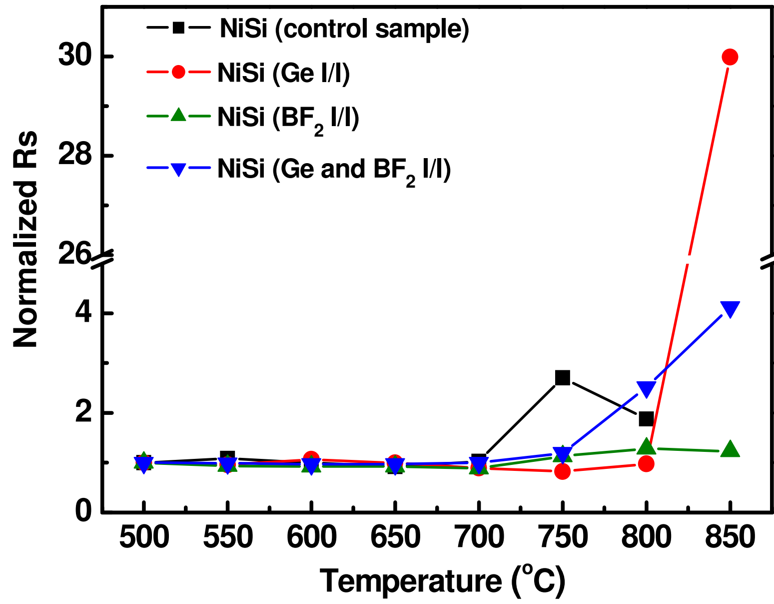



(a)

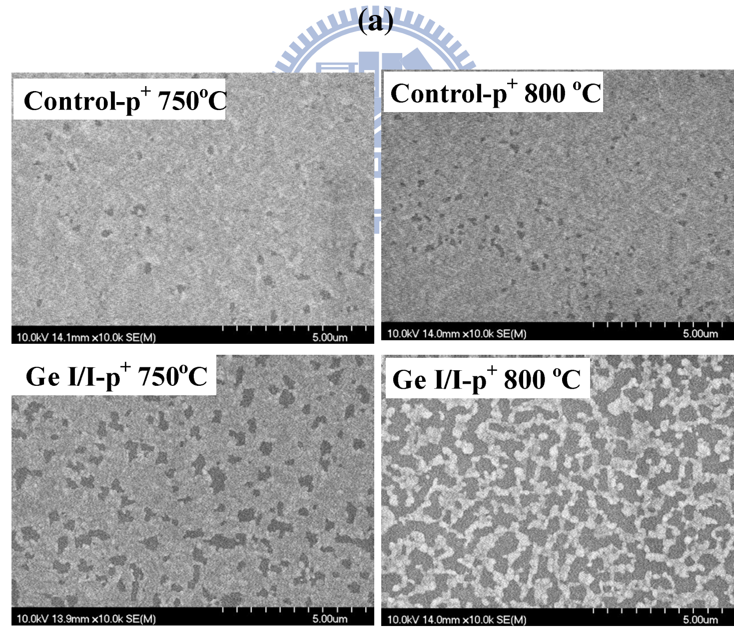



(b)

Fig.2-11 (a) Normalized sheet resistance values and (b) Plan-view SEM images of the NiSi films on $n^+$-Si layer after annealing at different temperatures for 30 sec. The sheet resistance values are normalized to those of the 500 °C annealed samples.

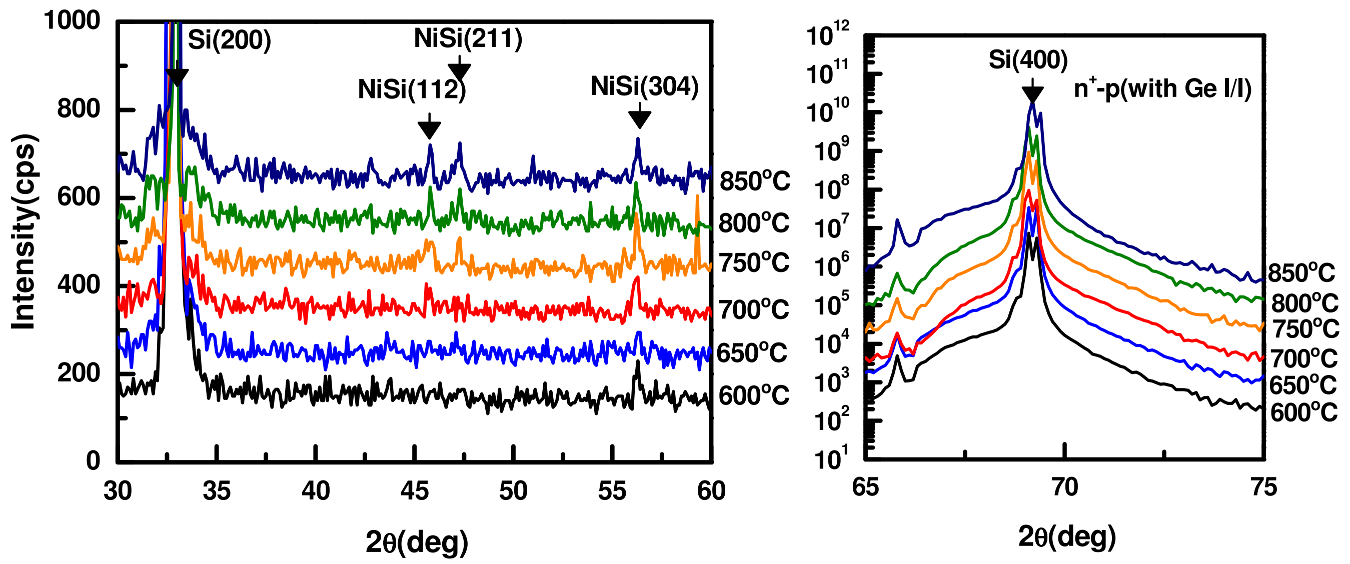



(a)

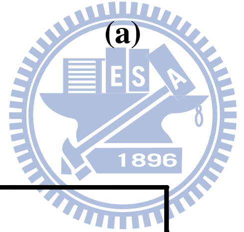


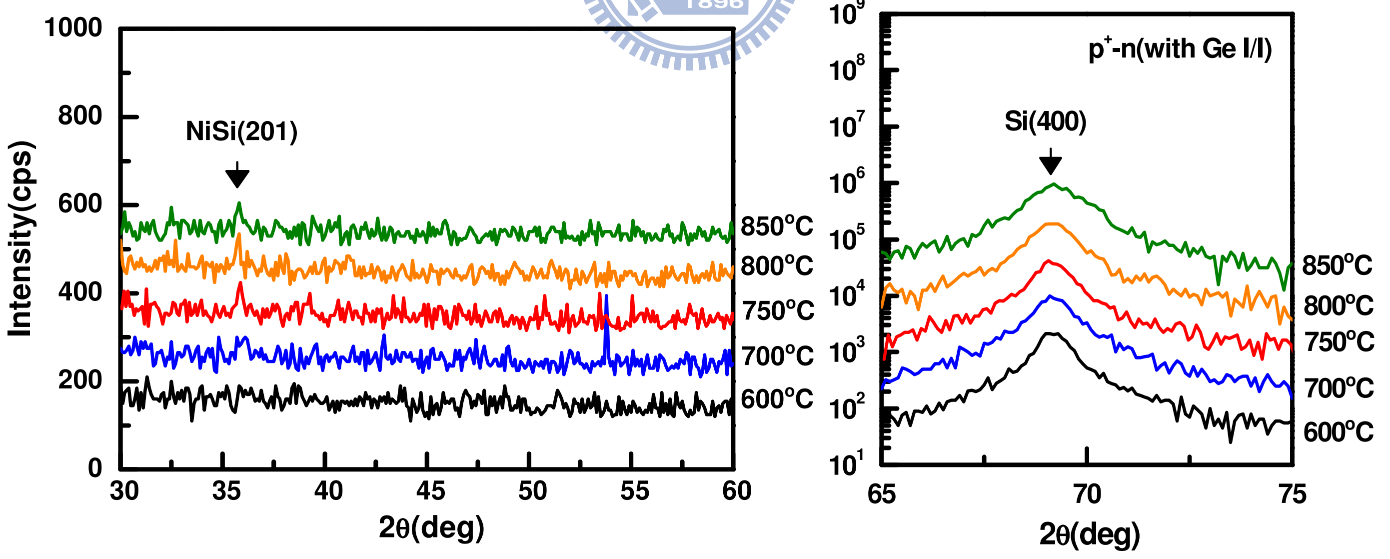

(b)

Fig.2-12 (a) Normalized sheet resistance values and (b) Plan-view SEM images of the NiSi films on $p^+$-Si layer after annealing at different temperatures for 30 sec. The sheet resistance values are normalized to those of the 500 °C annealed samples.




(a)




(b)

Fig.2-13 XRD analysis results for (a) $n^+$-p GeI/I and (b) $p^+$-n junction samples at different RTA annealing temperatures for 30 sec.

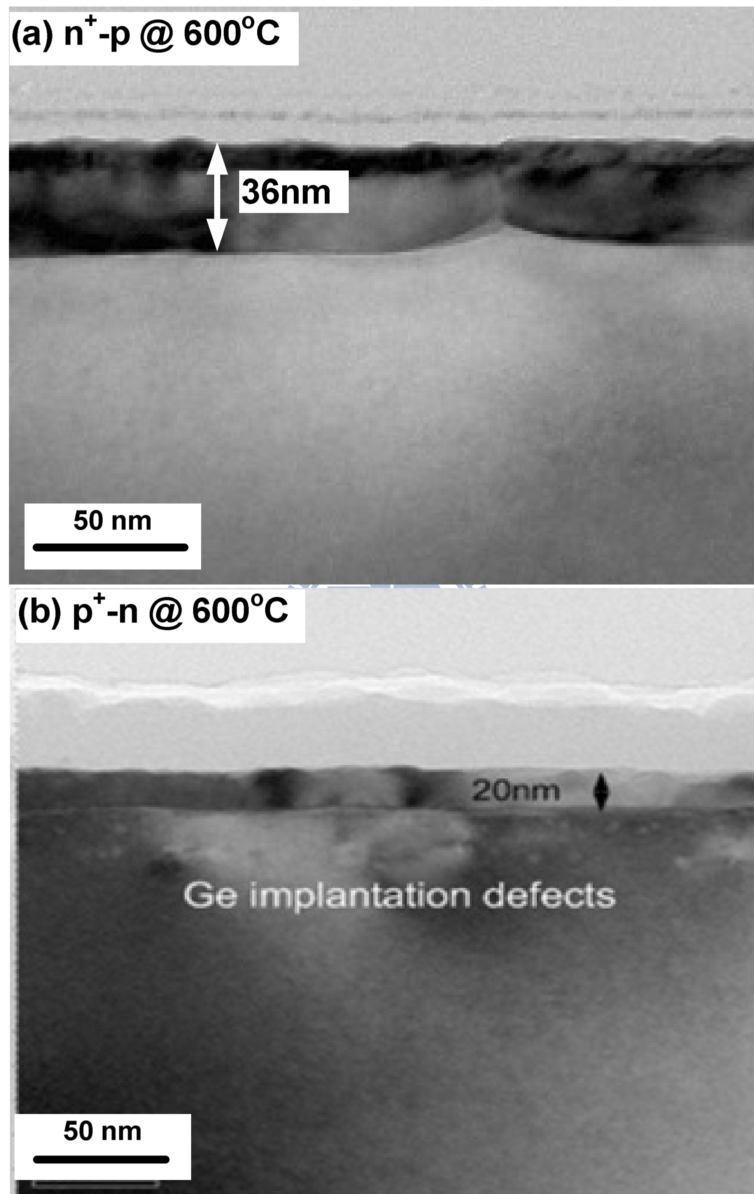



Fig.2-14 Cross-sectional TEM micrographs of the (a) $n^+$-p and (b) $p^+$-n samples with Ge I/I after annealing at 600 °C for 30 sec.

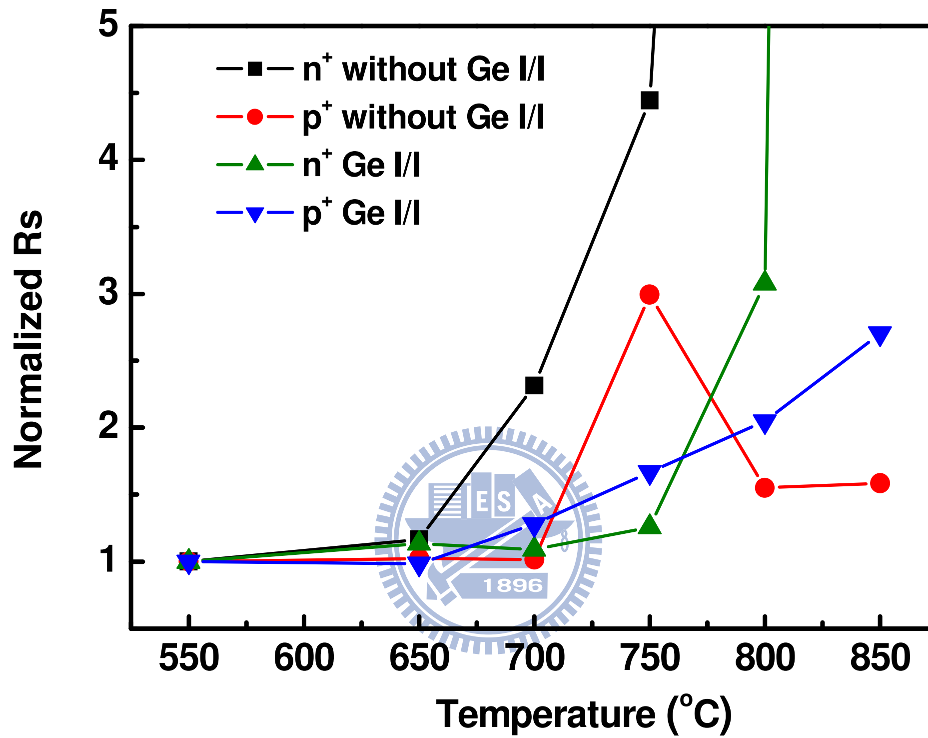
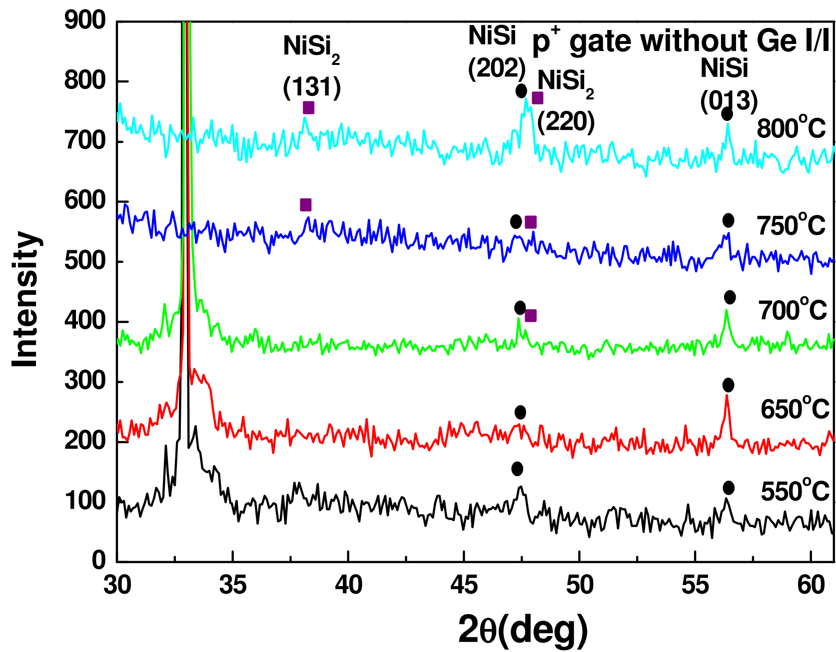
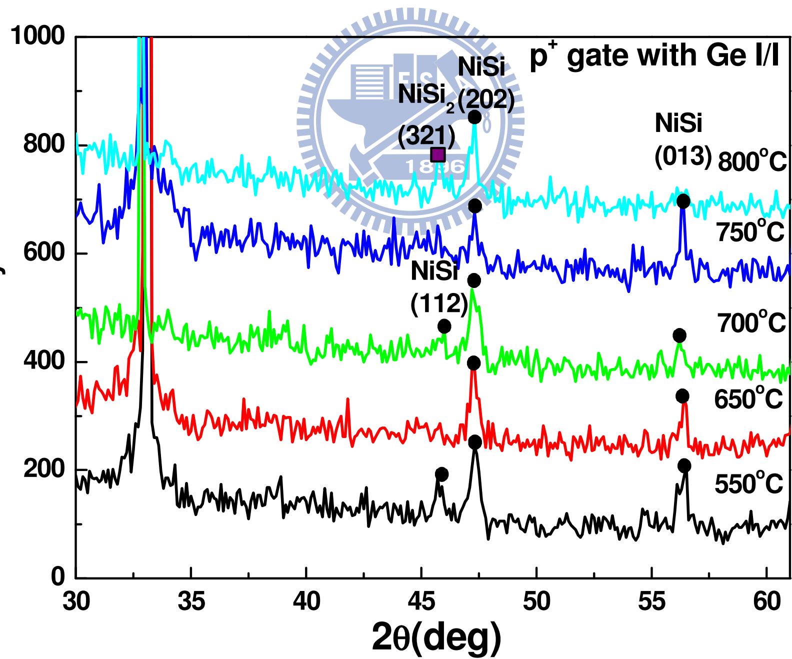



Fig.2-15 Normalized sheet resistance values of Ni silicide on $n^+$ and $p^+$ poly-Si gate for GeI/I and without GeI/I samples as a function of RTA annealing temperature. The sheet resistance values are normalized to those of the 500 °C annealed samples.




**(a)**




**(b)**

Fig.2-16 XRD analysis results for (a) without GeI/I and (b) with GeI/I on $p^+$ gate at different RTA annealing temperatures.

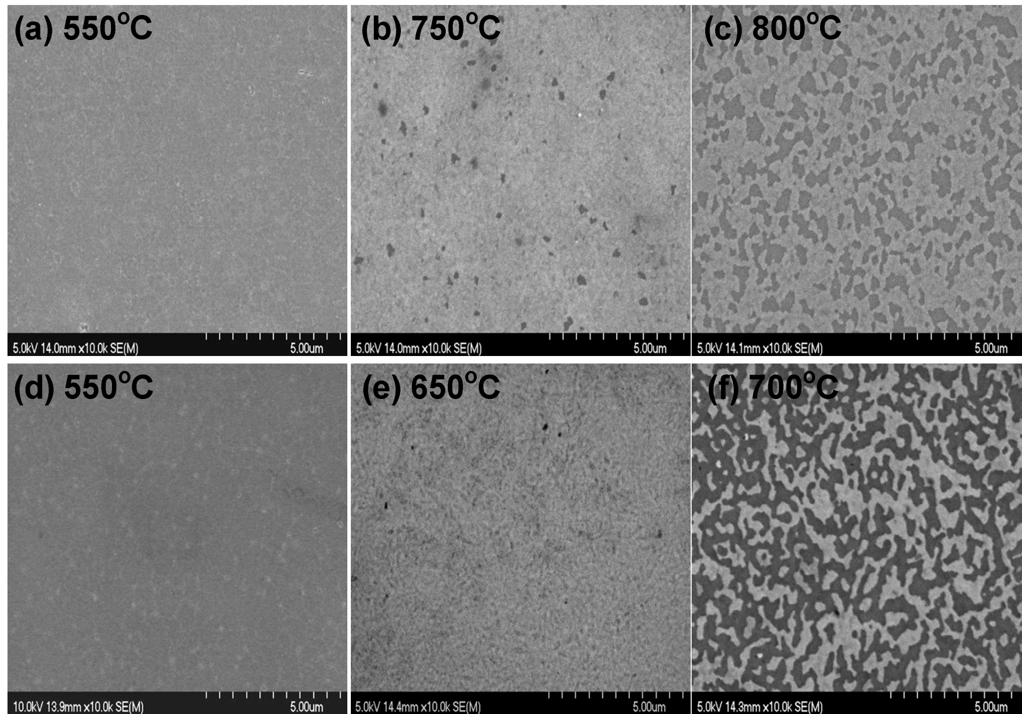



Fig.2-17 Plan-view SEM images of NiSi for (a)~(c) with GeI/I and (d)~(f) without GeI/I samples after various RTA annealing temperatures for 30 s on $n^+$ gate.

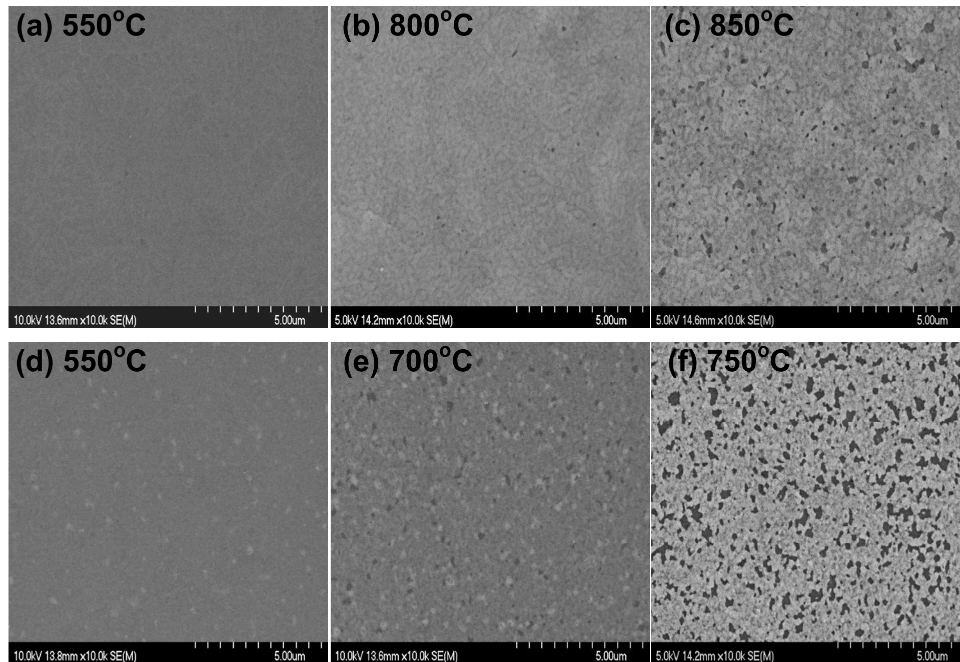



Fig.2-18 Plan-view SEM images of NiSi for (a)~(c) with GeI/I and (d)~(f) without GeI/I samples after various RTA annealing temperatures for 30 s on $p^+$ gate.

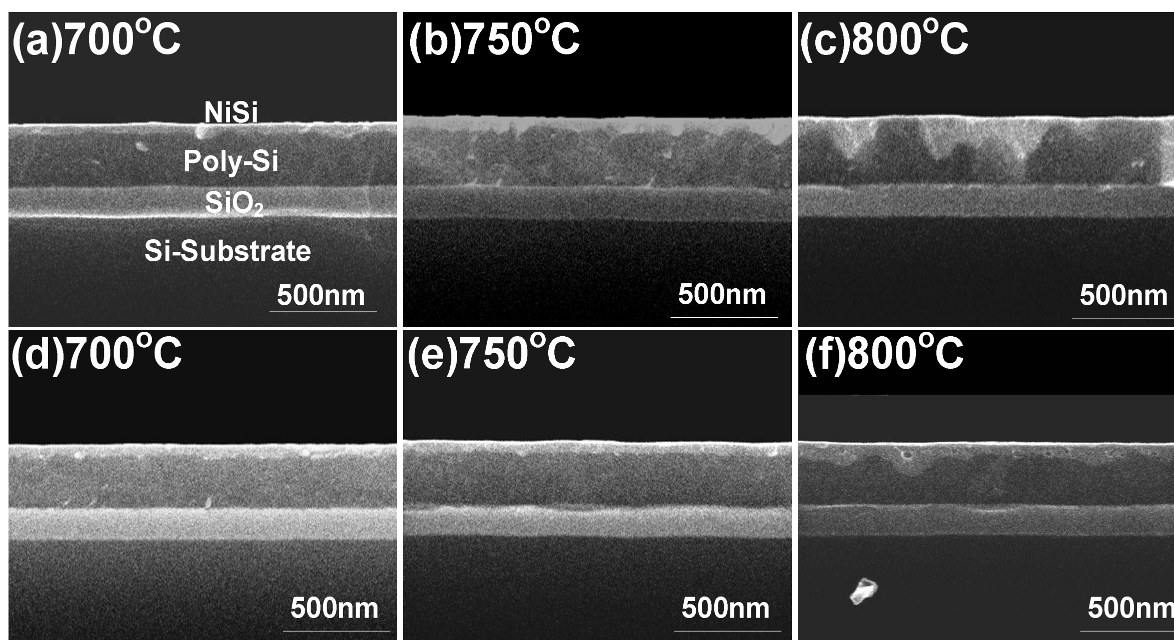



Fig.2-19 Cross-sectional view SEM images of NiSi (a)~(c) for $n^+$ and (d)~(f) for $p^+$ on GeI/I gate samples after various RTA temperature for 30 s.

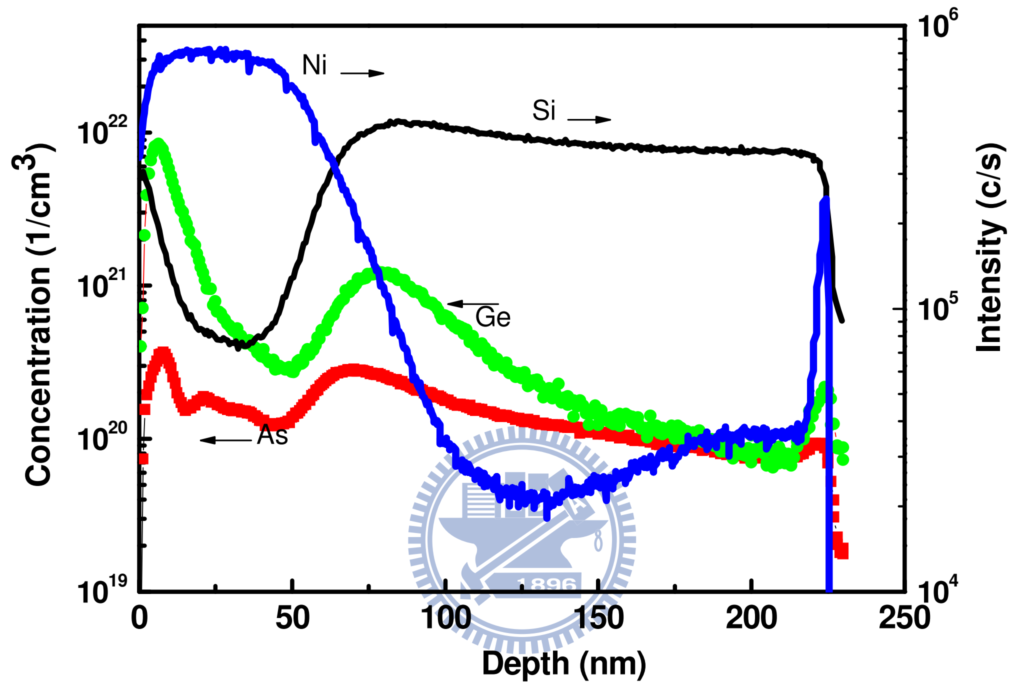



Fig.2-20 SIMS analysis results for Ge I/I on n$^+$ gate after silicide formation at 650 $^o$C RTA annealing for 30 s.

# Chapter 3
# Electrical Characteristic of NiSi Shallow Junction with Ge Ion Implantation

## 3-1 Introduction

The self-aligned silicide process for the source/drain and gate regions of a MOSFET is one of the most important applications in the semiconductor industry [1-7]. As device geometries are scaled down to the deep submicrometer region and below, the source and drain junction depth becomes shallower to mitigate the punch-through and other short channel effects [8]. Many new technologies and materials have been studied to solve these problems. Silicide is used to increase the drain current and suppress degradation by reducing the parasitic resistance of the source/drain and gate regions [9]. Nickel monosilicide (NiSi) is now the most desirable contact material because of its low sheet resistance, lower Si consumption, and low formation temperature. However, silicidation on shallow junctions could cause a drastic increase in the leakage current or abnormal soft breakdowns [10-13]. Many methods have been developed to prevent that, such as a raised source/drain [14-15], new incorporations of silicide [16], and implant-through-silicide [17].

In ULSI technology, the new silicidation process is considered to suppress short channel effects when forming ultra-shallow source/drain junctions. Metal silicide with a perfect interface property above an ultra-shallow junction is considered to be a critical issue. In chapter 2, we showed that Ge ion implantation produces good thermal stability and a smooth interface in a heavily doped bulk-Si substrate. Here, we continue the discussion on the fabrication of NiSi contacted shallow $n^+$-p and $p^+$-n junctions with Ge ion implantation (Ge I/I). The current–voltage (I–V) characteristic of these shallow junctions was investigated in the reverse bias region.

In addition to measuring the junction characteristic, we also fabricated a test structure to measure the contact resistance on a Si substrate. Three contact resistance ($R_c$) measurement methods have been reported; these involve transfer length structures, transmission lines [18], and cross bridge Kelvin resistor (CBKR) test structures [19-22]. The disadvantages of the transfer length structure and transmission line methods are that they are indirect measurements and have specific contact resistivity ($\rho_c$) value limitations. In contrast, the CBKR test structure, as shown in Fig.3-1 [23], is considered to be the best method for $\rho_c$ measurement at the $10^{-7}$~$10^{-8}$ ($\Omega$-$cm^2$) level. However, some difficult parasitic resistance error corrections are required when using the CBKR structure. The measurement of $R_c$ is influenced by many parameters, e.g. junction depth, the distribution of substrate concentration, and the mask shift of contact hole [24-26].These corrections affect the accuracy of the $\rho_c$ determination. By varying the size of the contact hole in CBKR structures, a proposed simplified method can reduced that influences. Thus, based on the best condition obtained in chapter 2, we fabricated a CBKR test structure with a good thermally stable NiSi contacted junction. The $R_c$ of the NiSi/$p^+$ interface with GeI/I was measured and $\rho_c$ was also calculated.

## 3-2 Experimental Procedures

### 3-2-1 Junction Sample Preparation

Typical local-oxidation-of-Si (LOCOS) isolation was employed to fabricate the p-n junction samples. Only the GIBS method was used to fabricate the p-n junction samples because this method results in better thermal stability than the GIAS method. The Ge dose was $1 \times 10^{16}$ $cm^{-2}$. There was no screen oxide before Ge I/I, so the implantation energy was reduced to 30 keV to obtain an $R_p$ of about 25 nm below the Si surface. This $R_p$ value is similar to that of Ge implantation at 50 keV through a 20-nm thick screen oxide. To form $n^+$-p and $p^+$-n junctions, $As^+$ and $BF_2^+$ ions were implanted at 35 keV and 20 keV, respectively, to a

dose of $5 \times 10^{15}$ $cm^{-2}$. After RCA cleaning, spike annealing at 1050 ℃ was performed to activate the dopants and annihilate the ion implantation induced defects. Following an HF-dipping, Ni/TiN (25 nm/5 nm) films were deposited on the samples by physical vapor deposition (PVD) at $10^{-7}$ Torr. The 1st Ni-silicide formation step was annealed at 300 ℃ for an hour in vacuum. After the 1st silicidation process, the capping layer TiN and un-reacted Ni were selectively removed by immersion in a sulfuric peroxide solution ($H_2SO_4$:$H_2O_2$ = 3:1) for 10 min. Then the samples received a 2nd RTA in $N_2$ ambient at different temperatures and for different times. Table 2-2 in chapter 2 lists the 2nd silicide process conditions for the p-n junction samples. Finally, front and back side aluminum metal patterns were fabricated for measurements.

### 3-2-2 Cross Bridge Kelvin Resistor Structure Fabrication

Typical LOCal-Oxidation-of-Si (LOCOS) isolation was employed to fabricate the $p^+$-n CBKR structure samples. Ge were implanted at 30 keV to a dose of $1 \times 10^{16}$ $cm^{-2}$ and $BF_2$ were implanted at 20 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$. After HF-dipping, a spike annealing at 1025 ℃ was performed for dopant activation and to annihilate defects induced by ion implantation. After a RCA cleaning, an 80-nm thick passivation oxide was growth by low pressure chemical vapor deposition (LPCVD). The contact holes were patterned by lithography and dry etching. Then, Ni/TiN (25 nm/5 nm) films were deposited by physical vapor deposition (PVD) at $10^{-7}$ Torr. The first Ni-silicide formation step was a 300 ℃ annealing for 60 min in vacuum. After that, the capping TiN and un-reacted Ni were selectively removed by immersing in a sulfuric peroxide solution ($H_2SO_4$:$H_2O_2$=3:1) for 10 min. Then the 2nd RTA was taken at 600°C in $N_2$ ambient. Then a 500-nm thick aluminum layer was deposited by thermal coater and patterned to become contact metal of upper and lower arm of CBKR structure. Finally, a sintering process was carried out at 450 °C in $N_2$ ambient.

### 3-2-3 Analysis Method

The cross-sectional microstructure was inspected using a transmission electron microscope (TEM). The depth profiles of the species were analyzed by a secondary ion mass spectroscope (SIMS). The current-voltage (I-V) characteristics of the junctions were measured by a semiconductor parameter analyzer (Agilent 4156C).

### 3-2-4 Characterization Techniques

The forward ideality factor, n, of a junction diode can be extracted from the basic I-V relation: $I = I_S\left[\exp\left(\frac{qV}{nkT}\right)-1\right]$ ......(3.1)

where $I_S$ is the reverse saturation current, q is the electronic charge, k is the Boltzmann constant, and T is the temperature at measurement.

When qV >> kT in equation (3.1), the ideality factor, n, can be determined from the slope of the ln(I)-V plot as equation (3.2). An ideality factor of unity indicates that the diffusion current predominates, while a factor of 2 indicates that the depletion recombination current is dominant.

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln I)} \qquad ......(3.2)$$

The reverse bias leakage current ($I_R$) of a $p^+$-n or $n^+$-p junction consists of the reverse area leakage current ($I_{RA}$) and the reverse peripheral leakage current ($I_{RP}$):

$$I_R = I_{RA} + I_{RP} = A\times J_{RA} + P\times J_{RP} \qquad ......(3.3)$$

where A is the junction area, P is the length of the junction perimeter, $J_{RA}$ is the junction area leakage current density, and $J_{RP}$ is the junction peripheral leakage current density. A simple arrangement gives:

$$J_R = J_{RA} + J_{RP}\left(P/A\right) \qquad ......(3.4)$$

where $J_R = I_R/A$. By measuring the $I_R$ values of junctions with different P/A ratios, the slope

of the $J_R$ versus P/A plot gives the $J_{RP}$ and the Y-axis intersection gives the $J_{RA}$.

The reverse current is also constructed from the generation current ($I_{gen}$) and diffusion current ($I_{diff}$). The reverse current equations of these two components are as follows:

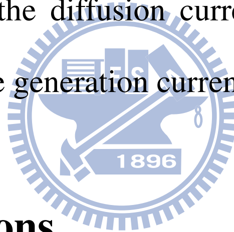
$$I_{diff} = I_{diff,n} + I_{diff,p} = qA\left(\frac{D_n}{L_n N_a} + \frac{D_p}{L_p N_d}\right) n_i^2 \propto T^3 e^{-E_g/kT} \quad \ldots\ldots(3.5)$$

$$I_{gen} = \frac{1}{2} q \frac{n_i}{\tau_0} WA \propto T^{\frac{3}{2}} e^{-E_g/2kT} \quad \ldots\ldots(3.6)$$

Then, the temperature dependence of reverse current $I_R$ is given by:

$$I_{\mathbf{R}} \propto T^3 e^{-E_a/kT} \quad \ldots\ldots(3.7)$$

where $E_a$ is the activation energy of the junction, k is the Boltzmann constant, and T is the temperature at measurement. The value of $E_a$ is close to the bandgap of silicon ($E_g$) when the reverse current is dominated by the diffusion current and will be close to $E_g/2$ when the reverse current is dominated by the generation current.




## 3-3 Results and Discussions

### 3-3-1 Electrical Properties of $n^+$-p Shallow Junctions

Fig.3-2 shows the basic I-V characteristics of an $n^+$-p shallow junction (a) without and (b) with Ge ion implantation (Ge I/I). The ideality factor (n) was extracted from equation (3.2). The forward biased current has n values of around 1.1 on the $n^+$-p junctions below an annealing temperature of 600 °C, as shown in Fig.3-3. This low value implies that most of the ion implantation induced defects near the metallurgic junction have been annihilated. The increase in the n values above 650 °C implies that the recombination current increases at the low voltage region. There may be many causes for the increase in the recombination current, such as implantation defects, Ni-silicide agglomeration, and the diffusion of Ni ions from the silicide to the substrate. From the changes in the sheet resistance seen in Fig.2-12(a), the

Ni-silicide started agglomerating at 650 °C and was completely agglomerated at 700 °C. In fact, the electrical I-V characteristic might more sensitive to Ni-silicide agglomeration, even if the sheet resistance or surface morphology remains unchanged. Therefore, we stripped the Ni-silicide from a $n^+$-p shallow junction and measured the surface roughness of the NiSi/Si interface by AFM. Fig.3-4 shows the roughness 2 × 2 μm areas of $n^+$-p shallow junction samples with Ge I/I and without Ge I/I annealed at 600 °C. In the sample with Ge I/I, the surface roughness decreases from 1.50 nm to 0.85 nm. The Ni-silicide agglomeration could cause increases in the recombination current and n value.

The reverse currents of $n^+$-p shallow junctions were measured at +3 volts. Fig.3-5 shows the reverse biased junction leakage current statistics for $n^+$-p shallow junctions after annealing at different temperatures for (a) 30 and (b) 60 s. With 30 s of RTA, we found that Ni-silicide agglomeration caused the leakage current to rapidly increase 2 orders of magnitude from 600 °C to 750 °C in the sample without Ge I/I. This situation was more significant in the sample with 60 s of RTA. The leakage current and agglomeration temperature were degraded with a larger thermal budget. The increase in the leakage current with Ge I/I $n^+$-p shallow junctions was moderate. We consider that the Ge I/I helped to prevent agglomeration, as shown in the results in chapter 2. The reverse biased leakage currents of Ge I/I $n^+$-p shallow junctions annealed below 600 °C were slightly higher than the samples without Ge I/I. As the annealing temperature increased higher than 650 ºC, the junctions with Ge I/I exhibited lower leakage currents in comparison with the junctions without Ge I/I. Fig.3-6(a) and (b) show the SIMS depth profiles of the 600 °C annealed junctions with and without Ge I/I, respectively. The metallurgic $n^+$-p junction depth is 90 nm beneath the NiSi/Si interface. The depth profile of the Ni shows a tail toward the metallurgical junction with the Si owing to the Ni dissolution and diffusion, along with the defects induced by ion implantation during silicide formation. The tail in the Ge implanted sample is more apparent than that in the sample without Ge I/I, due to the extra defects generated by the Ge I/I process. Fig.3-7(a) and (b) are the $J_R$ versus

P/A plots, from equation (3.4), for $n^+$-p shallow junctions with and without Ge I/I and annealed at different temperatures. According to equation (3.4), the slope of the $J_R$ versus P/A plot gives the $J_{RP}$, and the Y-axis intersection gives the $J_{RA}$; the extracted $J_{RA}$ and $J_{RP}$ values were respectively plotted, as shown Fig.3-7(c) and (d). We suggest that the higher $J_{RP}$ values might come from the oxide trap density of the LOCOS's $SiO_2$/Si interface or that the junction peripheral lateral diffusion depth was too shallow because of the spike RTA dopant activation process. Below 600 °C, the Ge I/I samples still have better $J_{RP}$ characteristics, which might be attributed to the smooth silicide peripheral edges. The $J_{RA}$ values of the Ge I/I shallow junctions were a little higher than samples without Ge I/I. This condition was also influenced by Ni ion diffusion or Ge I/I defects. However, the advantage of the Ge I/I on shallow junction can also be found beyond 650 °C.

The activation energy of the 600 °C annealed $n^+$-p junctions was also measured from equation (3.7). In Fig.3-8(a) and (b), the extracted $E_a$ is close to $E_g/2$ below 80 °C and close to $E_g$ above 100 °C. In the 600 °C annealed sample, the Ge I/I $n^+$-p shallow junction shows a higher $E_a$ below 80 °C than the sample without Ge I/I.

### 3-3-2 Electrical Properties of $p^+$-n Shallow Junctions

The basic I-V characteristics of $p^+$-n shallow junctions (a) without and (b) with Ge I/I were measured, as shown in Fig.3-9. Then, the ideality factors (n) of the $p^+$-n junctions with or without Ge I/I and annealed for 30 s at different temperatures are outlined in Fig.3-10. The n values of $p^+$-n junctions without Ge I/I are all higher than those of $n^+$-p junctions without Ge I/I below 600 °C. Therefore, we think that the slightly higher values of the $p^+$-n junctions compared with the $n^+$-p junctions might be attributed to the quality of the original Si substrates. The $p^+$-n junctions with Ge I/I have higher values of n than samples without Ge I/I at any annealing temperature. This might be the influence of junction implantation defects in the depletion region, as seen Fig.2-15(b). Moreover, our NiSi film on the $p^+$-n junction is

thinner than on the $n^+$-p junction with Ge I/I. Fig.3-11 shows the reverse biased junction leakage current statistics of the $p^+$-n junctions after annealing for 30 s at different temperatures. The leakage current of junctions with and without Ge I/I slightly increases as the annealing temperature increases from 500 °C to 750 °C. The SIMS analysis, shown in Fig.3-12, reveals that the metallurgical junction depth is 120 nm beneath the NiSi/Si interface. The deeper junction and better thermal stability of the NiSi on a $p^+$-n junction in comparison with those on an $n^+$-p junction explain the better integrity of the leakage current. According to the sheet resistance data in Fig.3-9(b), the NiSi on the $p^+$-n junction starts agglomerating at 750 °C. Therefore, the thermal stability effects of the junction leakage current without Ge I/I are similar to those with Ge I/I from 500 °C to 750 °C. The phase transformation from NiSi to $NiSi_2$ after the 750 °C annealing of the Ge I/I junctions is retarded, so the agglomeration after 750 °C becomes pronounced. Therefore, the Ge I/I $p^+$-n junction leakage current increases apparently at 800 °C. Although the leakage current of a $p^+$-n junction without Ge I/I shows no obvious increase, the measured NiSi/Si interface roughness at 600 °C shows values of 1.612 nm and 2.227 nm for $p^+$-n junctions with and without Ge I/I, respectively. As the temperature increases, the {111} facets of the $NiSi_2$/Si interface are formed at 800 °C in samples without Ge I/I, as shown in Fig.3-13. Since the $p^+$-n junction depth is not very shallow; the phase transformation does not significantly degrade the leakage current performance.

Figs.3-14(a) and (b) are the $J_R$ versus P/A plots, from equation (3.4), for $p^+$-n shallow junctions with and without Ge I/I, respectively, and annealed at different temperatures. The extracted $J_{RA}$ and $J_{RP}$ values are plotted in Figs.3-14(c) and (d), respectively. The $J_{RA}$ values of $p^+$-n shallow junctions with and without Ge I/I are similar to those of the $n^+$-p shallow junctions. The $J_{RA}$ values of the Ge I/I samples are all about $10^{-8}$ A/cm$^2$, and higher than the samples without Ge I/I because of the Ge-ion implantation induced defects. The $J_{RP}$ values of the $p^+$-n junctions without Ge I/I exceed those of the Ge I/I $p^+$-n junctions after 700 °C, at which temperature the NiSi starts transforming into the $NiSi_2$ phase. The $J_{RP}$ values of the Ge

I/I $p^+$-n junctions are slightly increased due to the Ni diffusion to the substrate. The activation energy of the 600 °C annealed $p^+$-n junctions was also measured from equation (3.7), as seen in Fig. 14. In Figs.3-15(a) and (b), the extracted Ea values are close to $E_g/2$ below 100 °C and close to $E_g$ above 100 °C. The Ge I/I $p^+$-n junction's $E_a$, 0.942 eV, is much lower than $E_g/2$. We think that the Ge implantation defects or the strains induced by the high concentration of Ge ions cause the $E_a$ to decrease.

### 3-3-3 Contact Resistance Measurement

Loh *et al.* showed that, because of the lateral current spreading, the measured contact resistance ($R_c^{'}$) could be much larger than the actual $R_c$ in an L-type CBKR structure when the arm width is larger than the size of the contact hole. As shown in Fig.3-16, the L-type current paths were narrower than those of the D-type. Hence, the D-type was substituted for the L-type CBKR structure to measure the contact resistance. Equation (3.8) is used to calculate the measured $R_k$ of the CBKR structure [21].

$$R_K = \frac{\rho_C}{l\,l} + \frac{4R_S\delta^2}{3W\,W}\left[1 + \frac{\delta}{2(W-\delta)}\right] \quad \text{..... (3.8)}$$

The sheet resistances of the $p^+$ Si and NiSi in our experiment were measured with a four-point probe system. For the $p^+$ Si layer, the sheet resistance was 165 Ω/□, and for the NiSi it was 7 Ω/□.

Our designed D-type CBKR structure with Ge I/I on bulk Si is shown in Fig.3-17. In addition, Fig.3-18 shows the measured contact resistance. The calculated specific contact resistivity is around $1.2 \times 10^{-8}$ Ω-cm$^2$ and $2.04 \times 10^{-8}$ Ω/-cm$^2$ for the 0.8 μm and 1.0 μm hole sizes, respectively. Structures with hole sizes smaller than 0.8 μm were also measured, but the yield was poor because $Ni_xO_y$ existed at the NiSi/Al interface. Thus, the measured I-V relation of a CBKR structure with a 0.5 μm hole size was quite nonlinear, as shown Fig.3-19. As a previous paper reported, a high Ge concentration can improve the activation of B ions [27].

The contact resistances were lower in our study compared to conventional NiSi/$p^+$ contact structures.

## 3-4 Conclusions

When applying the GIBS method to $n^+$-p and $p^+$-n junctions, although the phase transformation temperature was increased, the agglomeration temperature of the NiSi on the $n^+$-p junction did not improve due to a high concentration of As doping atoms. Electrical measurements indicated that the Ge ion implanted junction exhibited a slightly higher but acceptable leakage current after medium temperature annealing. This observation is explained by the Ni diffusion and dissolution enhancement due to the extra defects induced by the Ge ion implantation. If these defects can be annihilated by suitable thermal annealing techniques such as laser annealing, the smooth NiSi/Si interface would provide a greater benefit to ultra-shallow junctions. All of these observations suggest the promising nature of the Ge ion implantation technique. The highest sustainable process temperature of the thinner NiSi may be lower than that observed in this work. However, the mechanisms identified in this work for thermal stability improvement could be applied.

Using a D-type CBKR structure, we performed some experimental measurements on a NiSi contacted interface. A Ge ion implanted $p^+$ contact also had a low specific contact resistivity due to the enhanced activation of B ions by the Ge at the interface.

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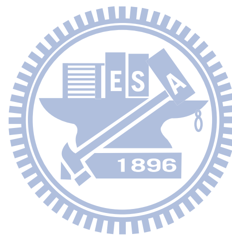


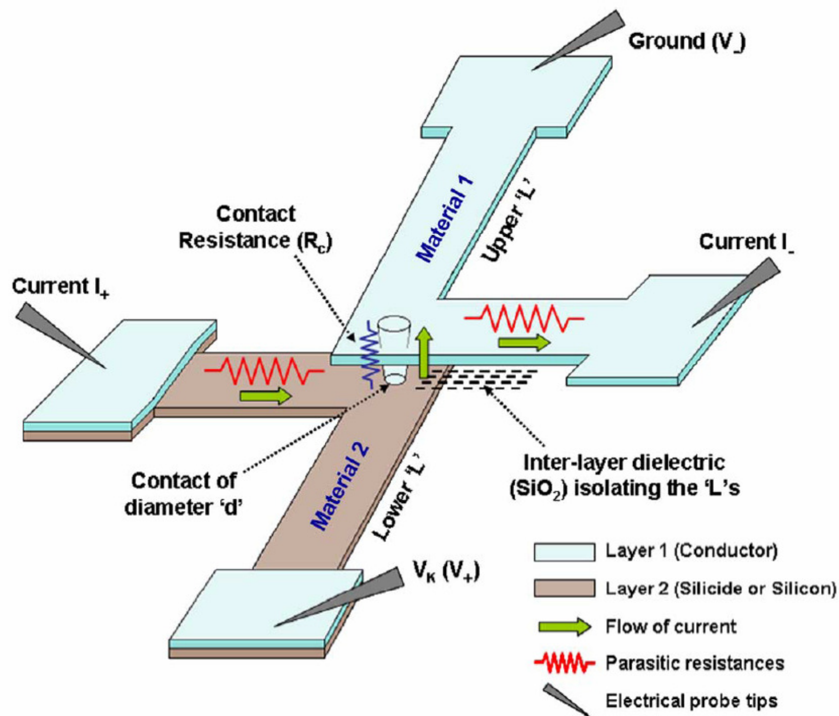
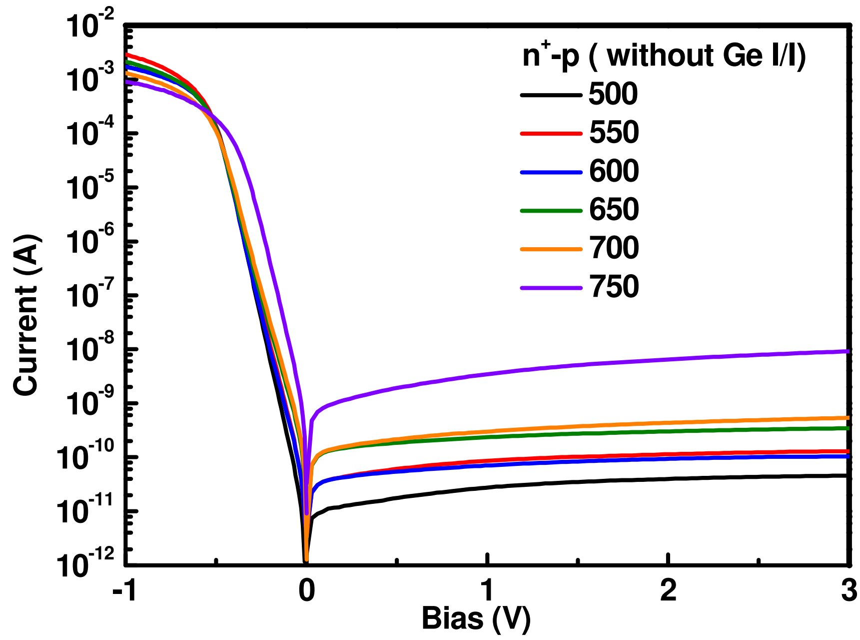
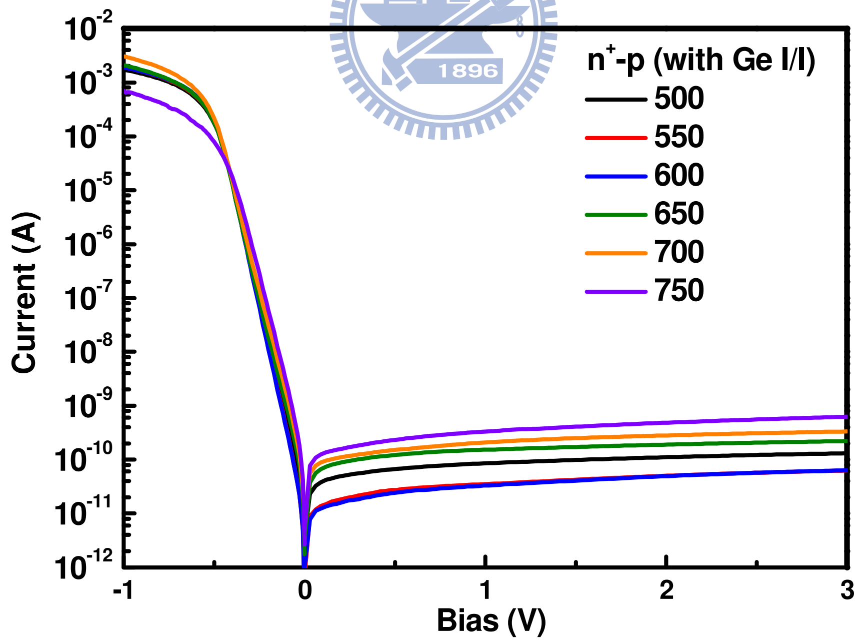



Fig.3-1 A cross bridge Kelvin resistor (CBKR) structure. [23]




(a)




(b)

Fig.3-2 Basic I-V characteristic of $n^+$-p shallow junction (a) without and (b) with Ge ion implantation (Ge I/I).

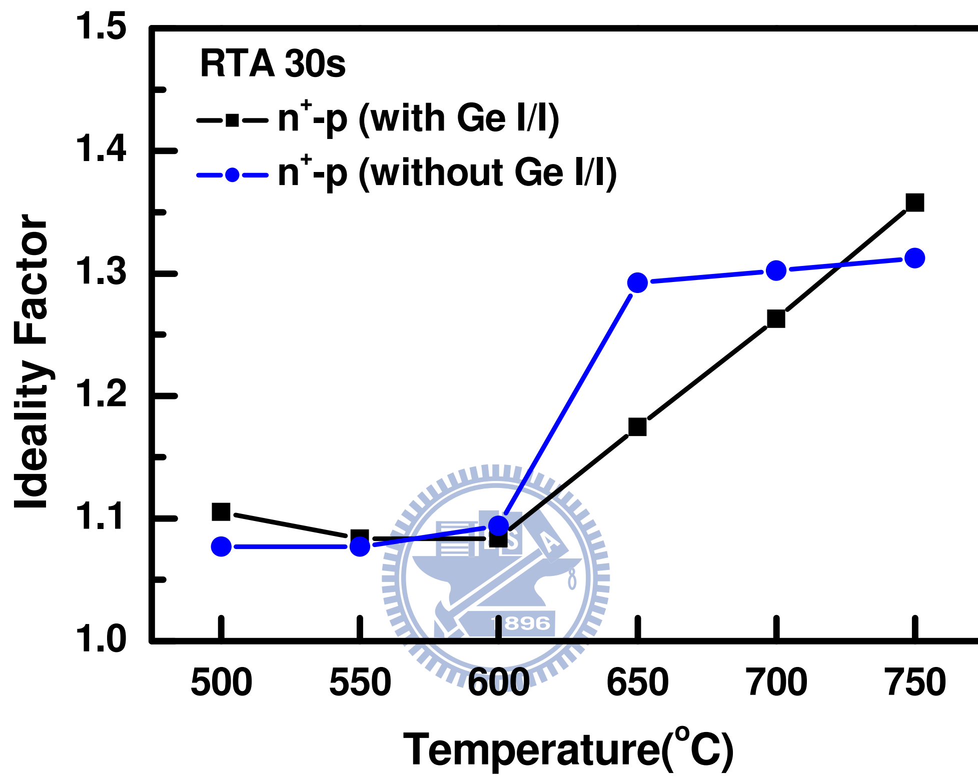
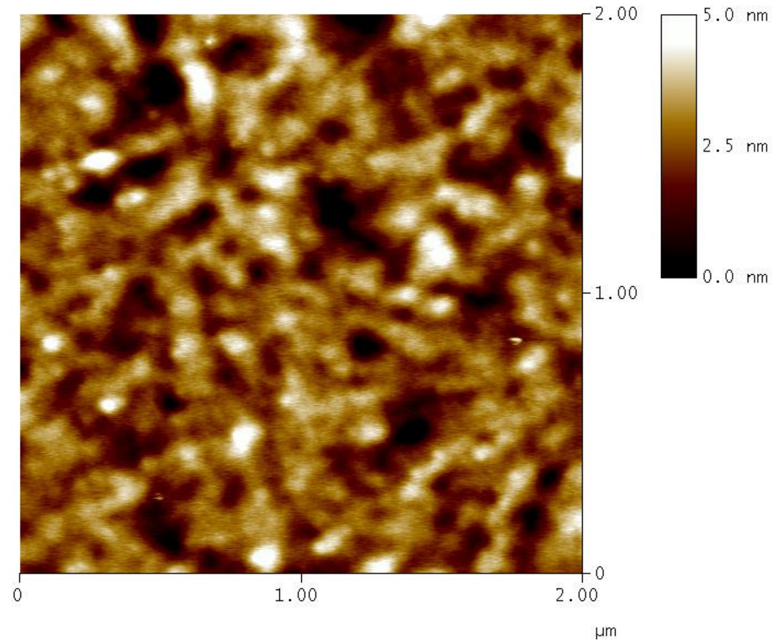
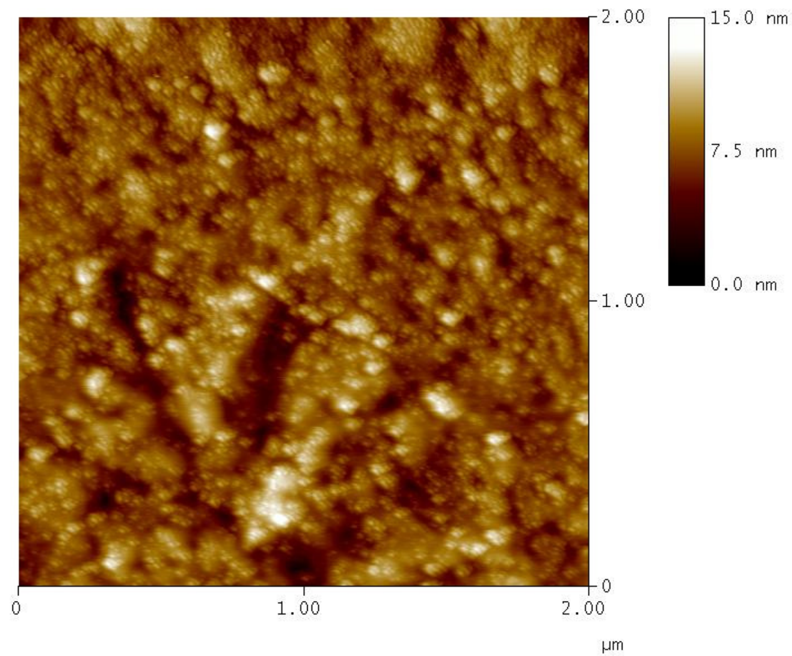



Fig.3-3 n values of the $n^+$-p junctions

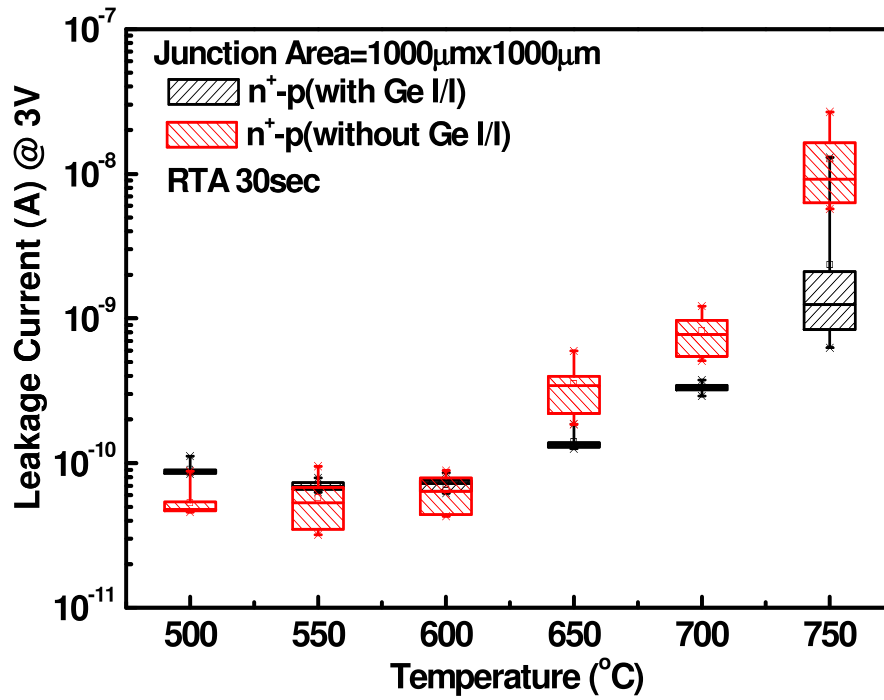



**(a) Roughness(rms):0.846nm**

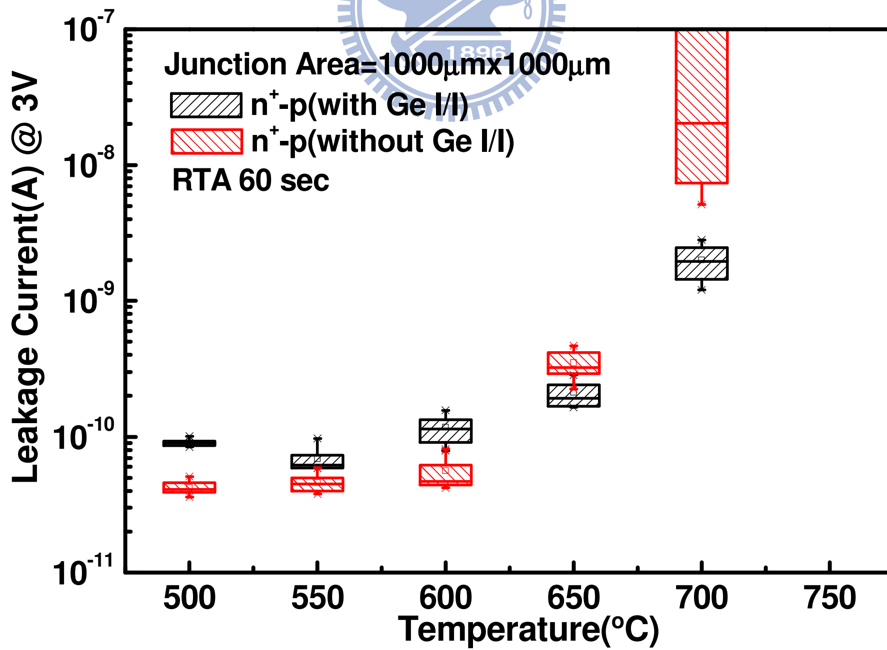



**(b) Roughness(rms): 1.499nm**

Fig.3-4 Surface roughness of NiSi/Si interface on $n^+$-p shallow junction by AFM (a) Ge I/I and (b) without Ge I/I.

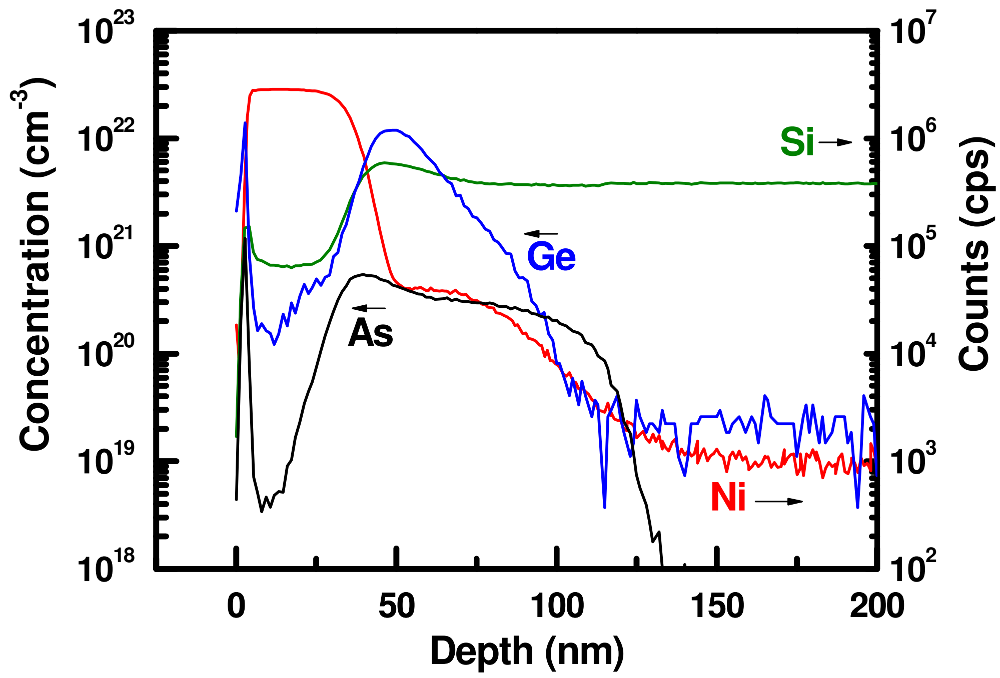



(a)

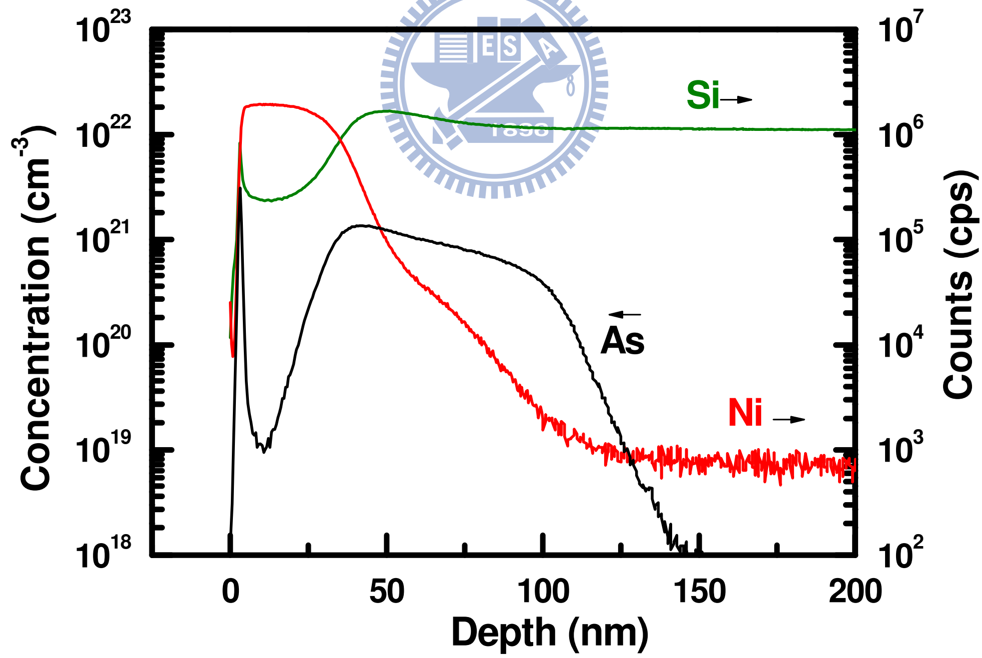



(b)

Fig.3-5 Reverse biased junction leakage current statistics of the $n^+$-p shallow junctions after annealing at different temperatures for (a) 30 and (b) 60sec.




(a)




(b)

Fig.3-6 SIMS depth profiles of the 600°C annealed $n^+$-p junctions (a) with and (b) without Ge I/I.

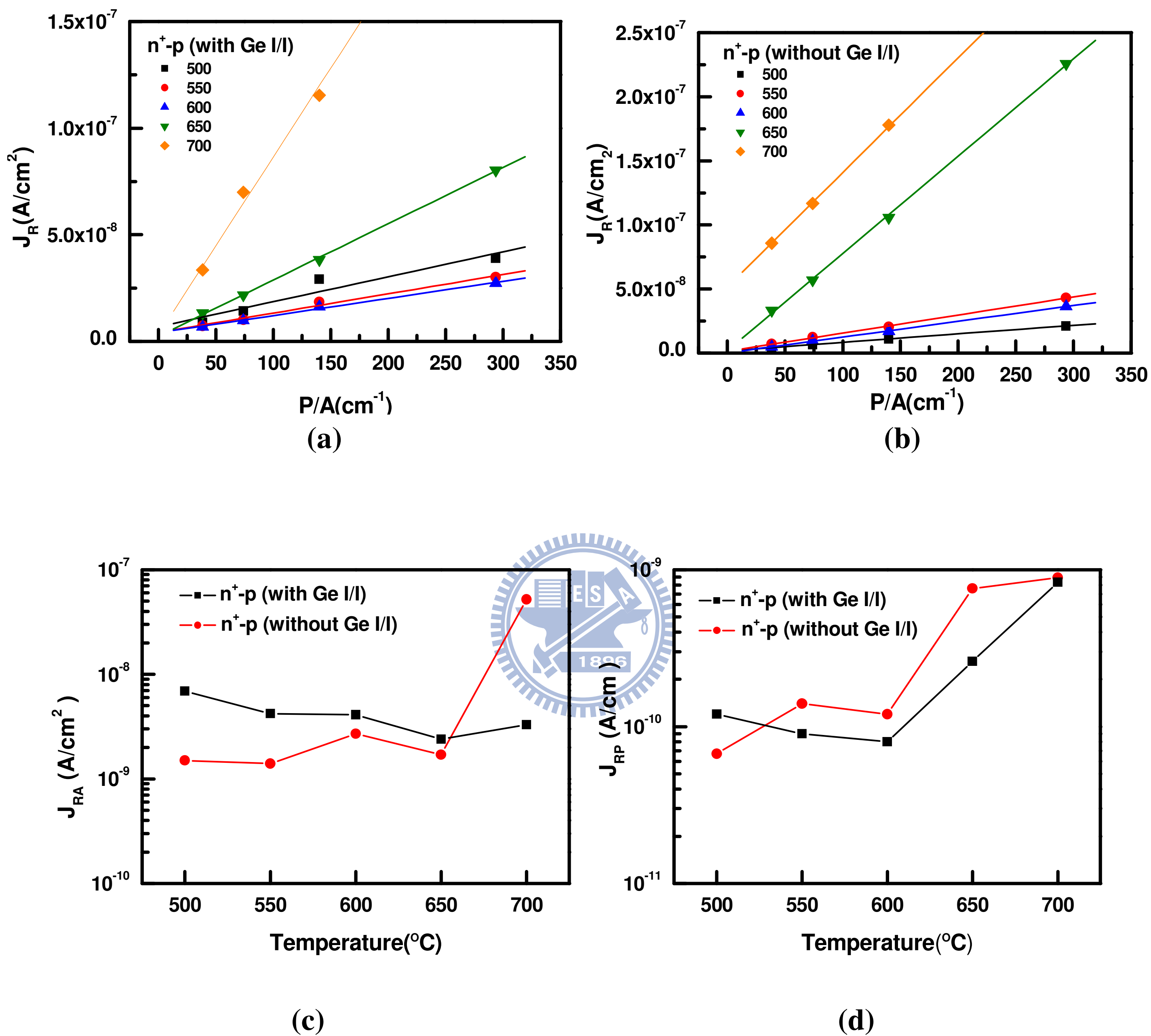
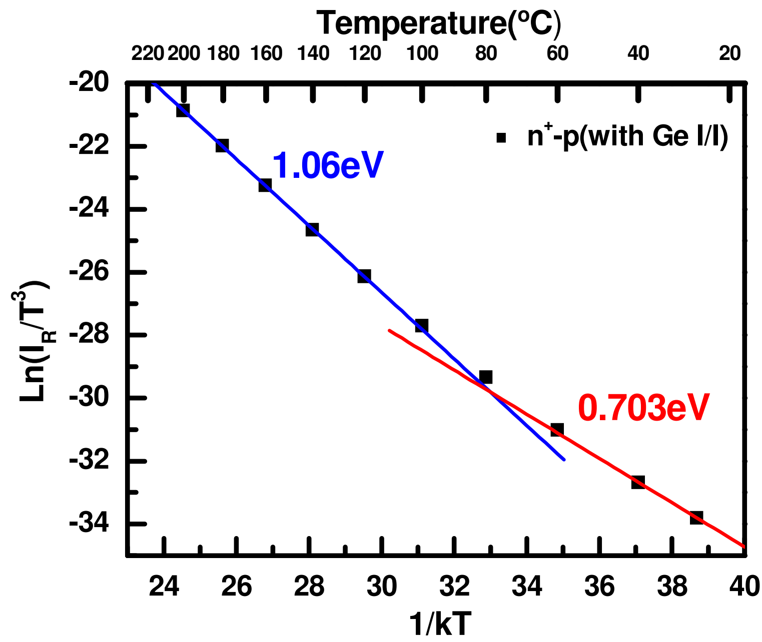
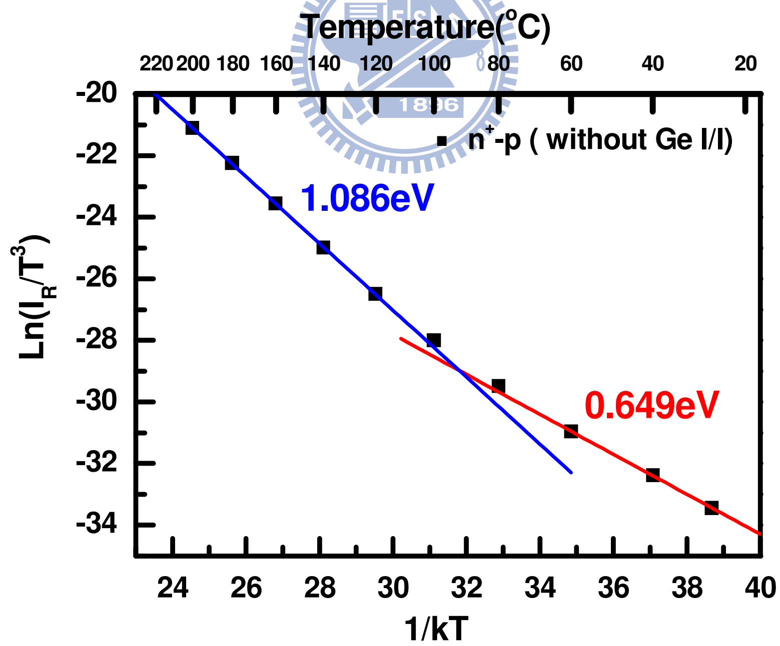



Fig.3-7 $J_R$ versus P/A plot of (a) with and (b) without Ge I/I $n^+$-p shallow junctions annealed at different temperature. The extracted $J_{RA}$ and $J_{RP}$ values were respectively plotted as (c) and (d).

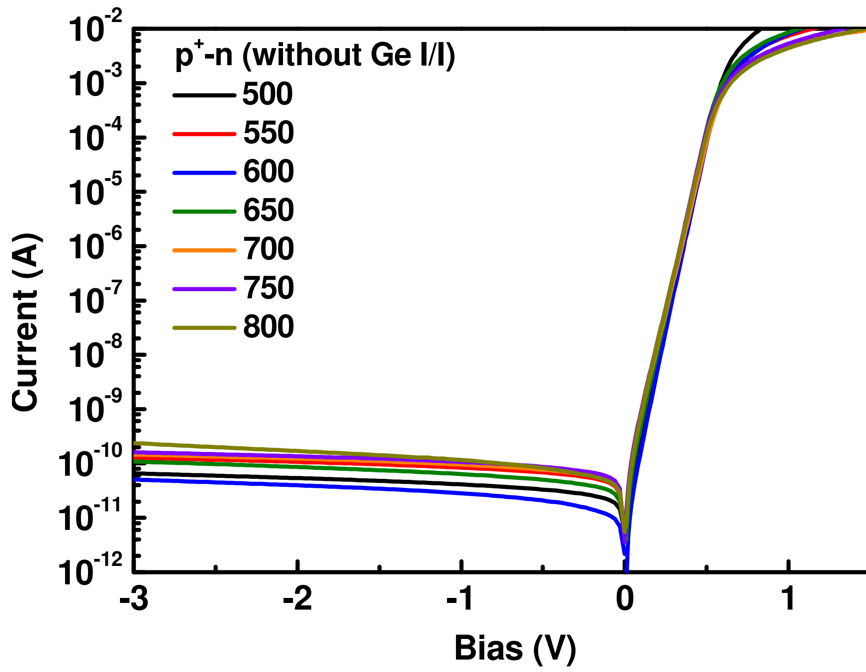



(a)

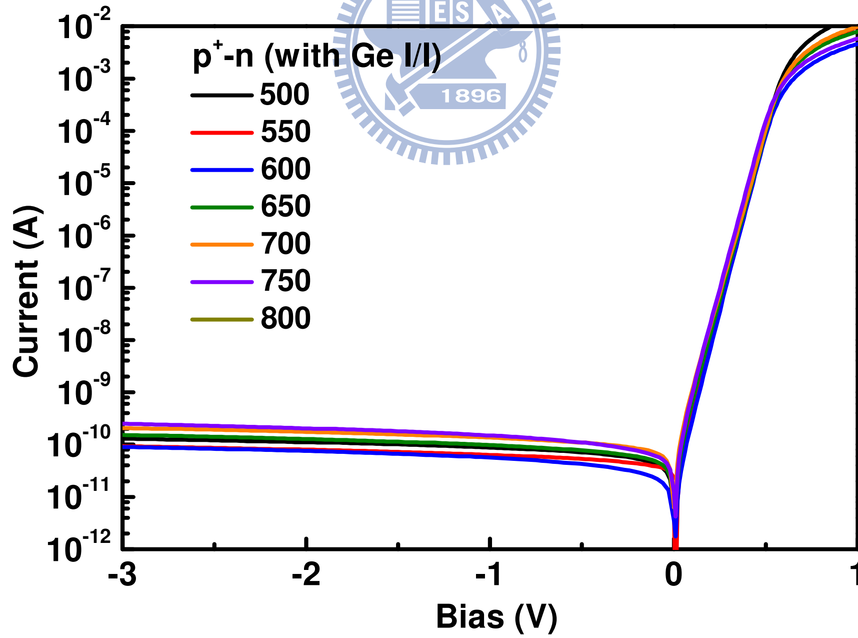



(b)

Fig.3-8 Activation energy of the (a) with and (b) without Ge I/I $n^+$-p shallow junctions annealed at 600 °C.




(a)




(b)

Fig.3-9 Basic I-V characteristic of $p^+$-n shallow junction (a) without and (b) with Ge ion implantation (Ge I/I).

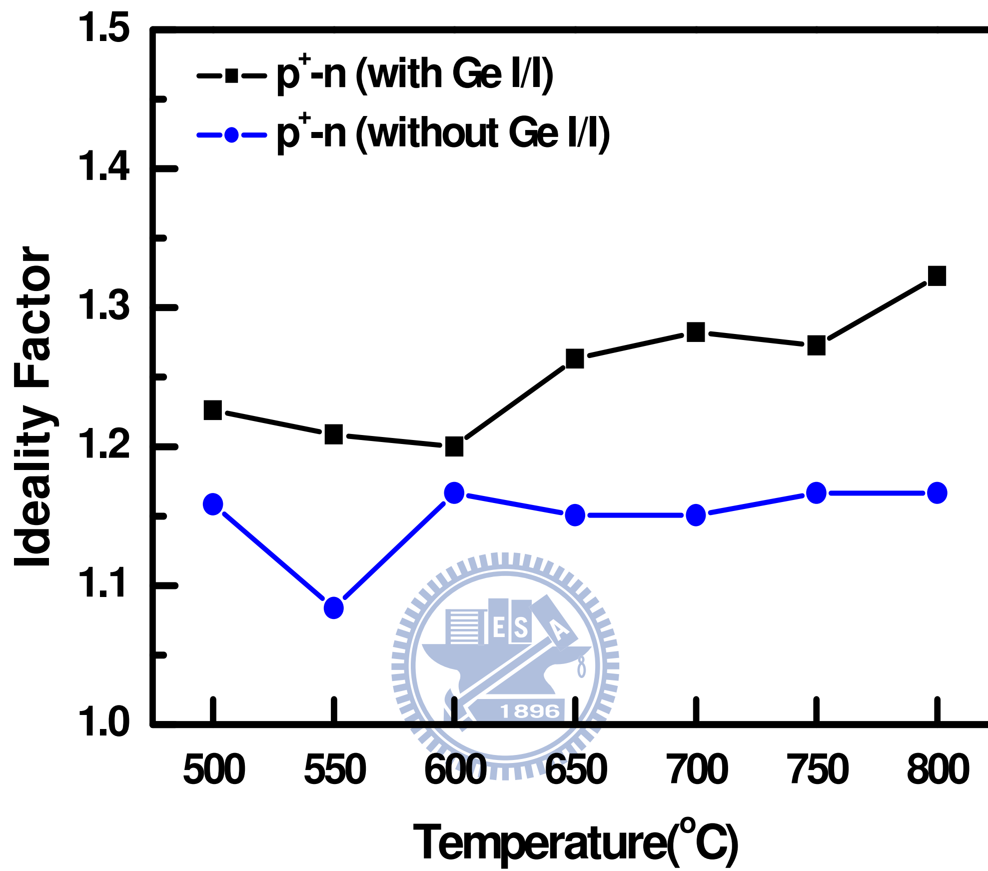



Fig.3-10 n values of the $p^+$-n junctions.

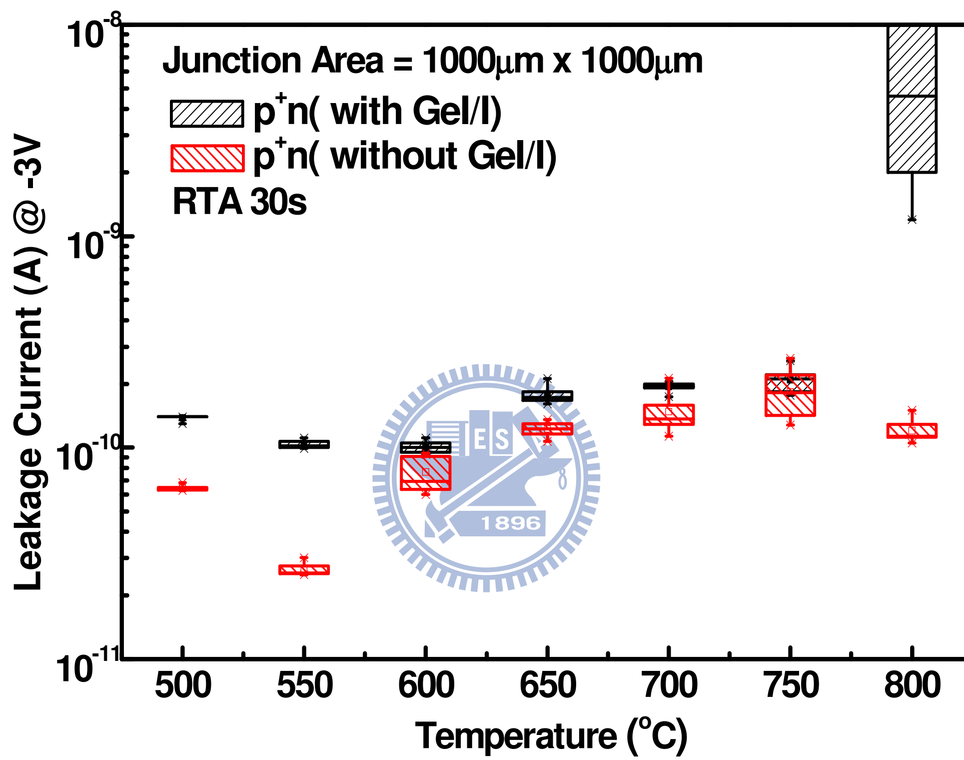



Fig.3-11 Reverse biased junction leakage current statistics of the $p^+$-n junctions after annealing at different temperatures for 30 sec.

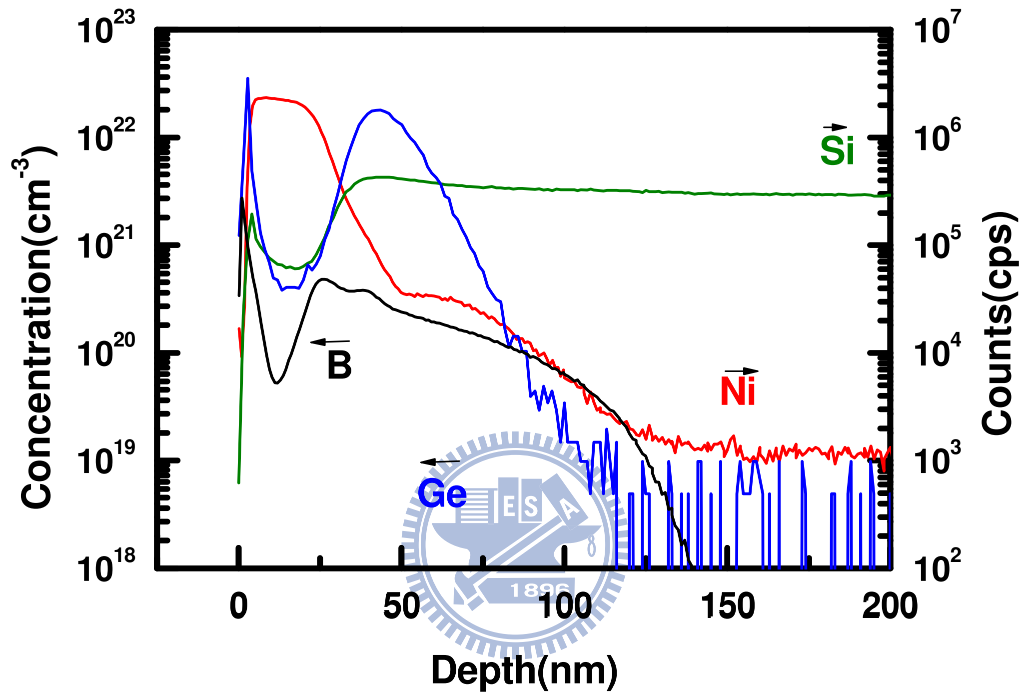



Fig.3-12 SIMS depth profiles of the 600 °C annealed $p^+$-n junction with Ge I/I.

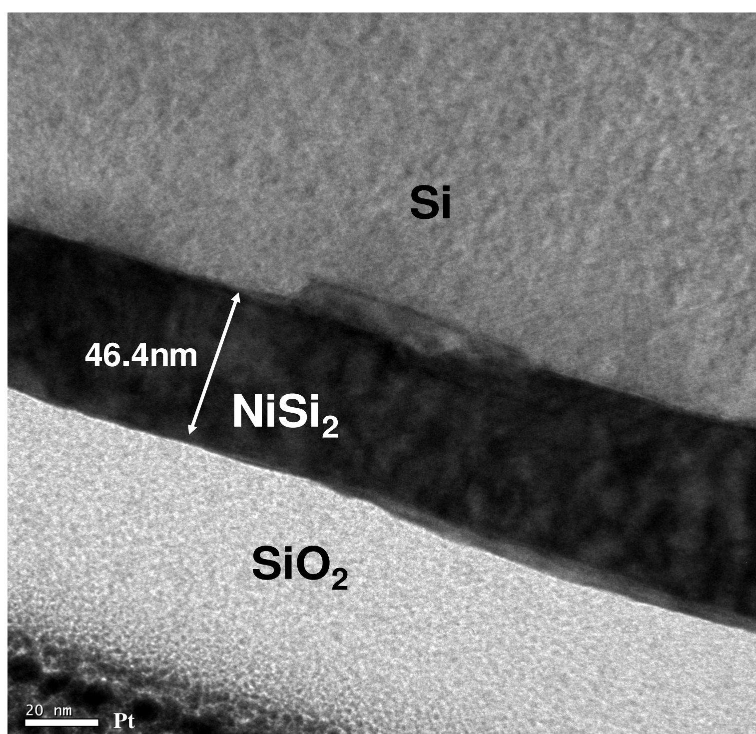
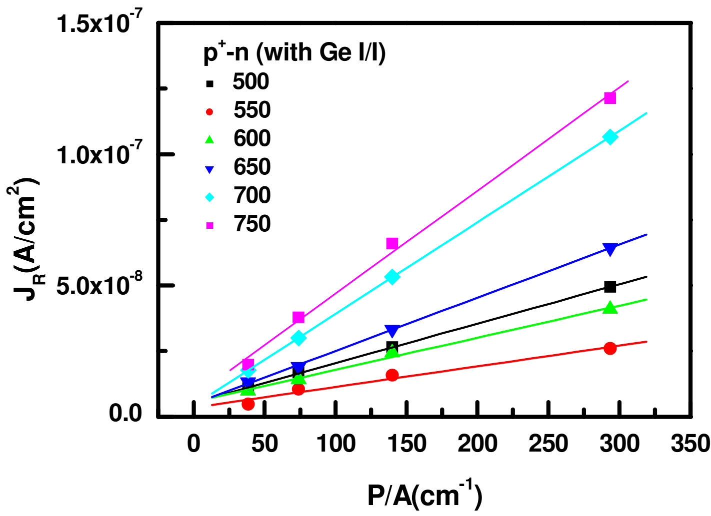
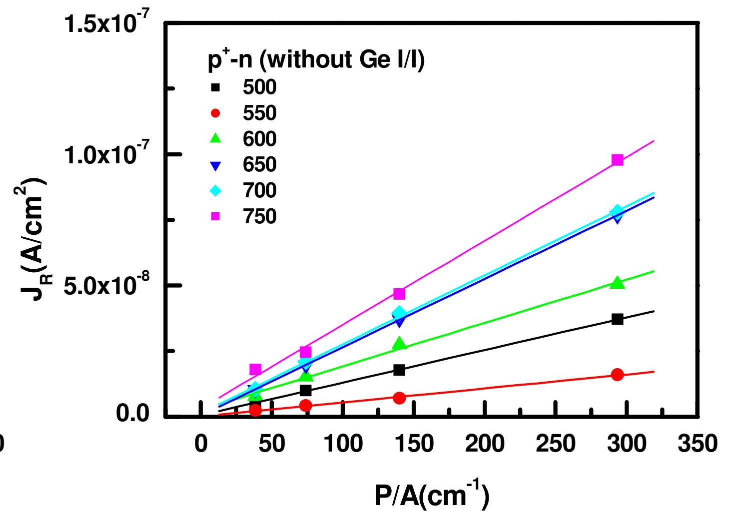



Fig.3-13 TEM image of the 800 °C annealed $p^+$-n junction without Ge I/I.




(a)

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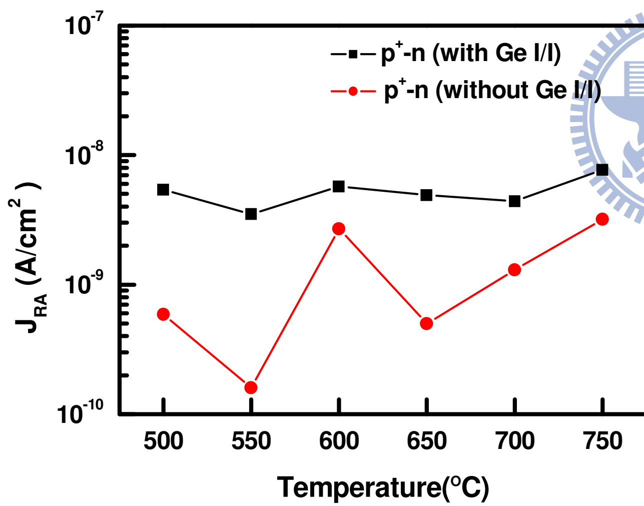
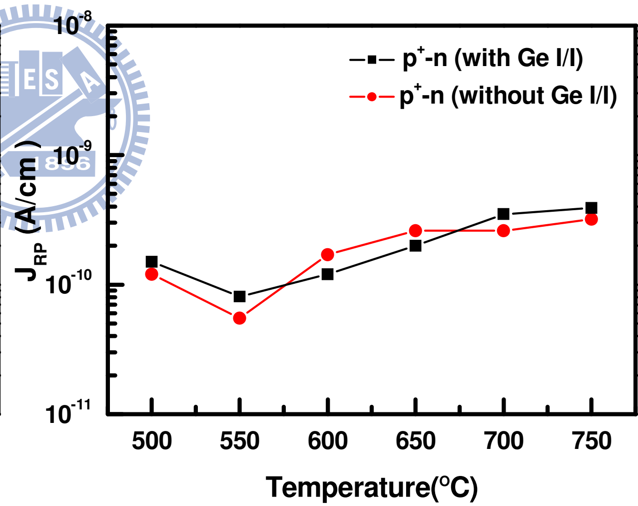
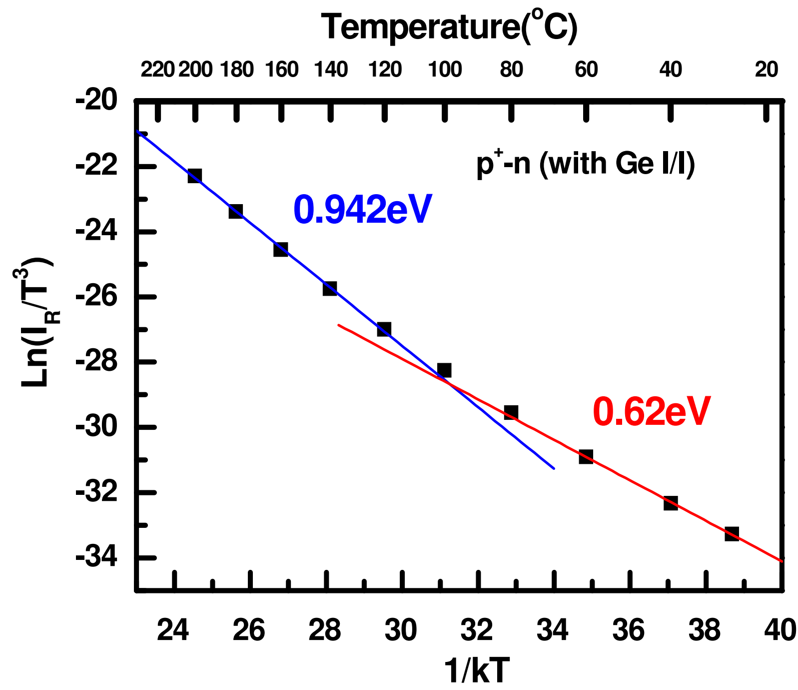



(c)

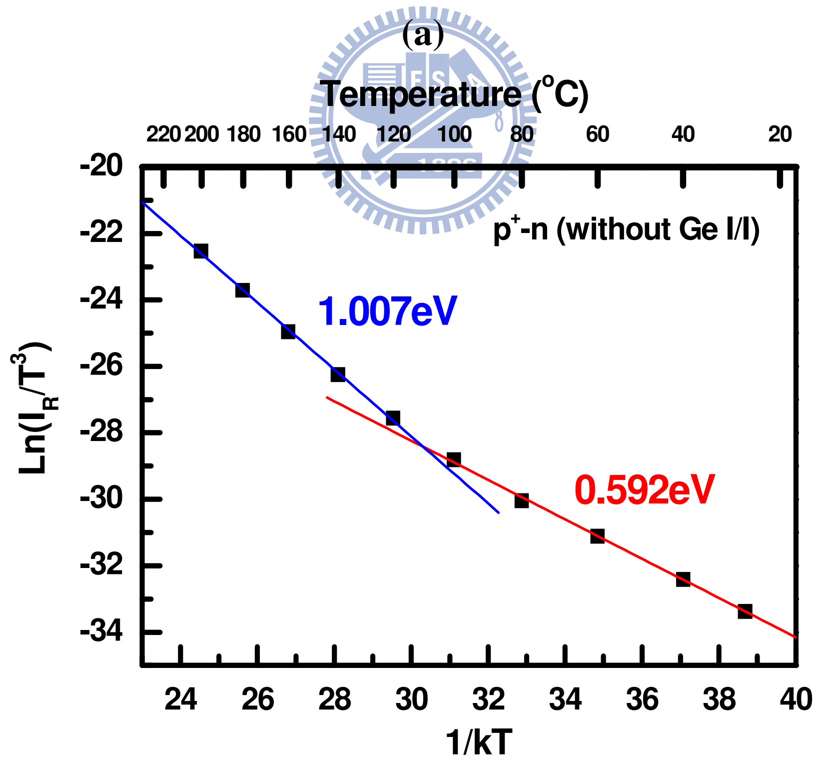



(d)

Fig.3-14 $J_R$ versus P/A plot of (a) with and (b) without Ge I/I $p^+$-n shallow junctions annealed at different temperature. The extracted $J_{RA}$ and $J_{RP}$ values were respectively plotted as (c) and (d).

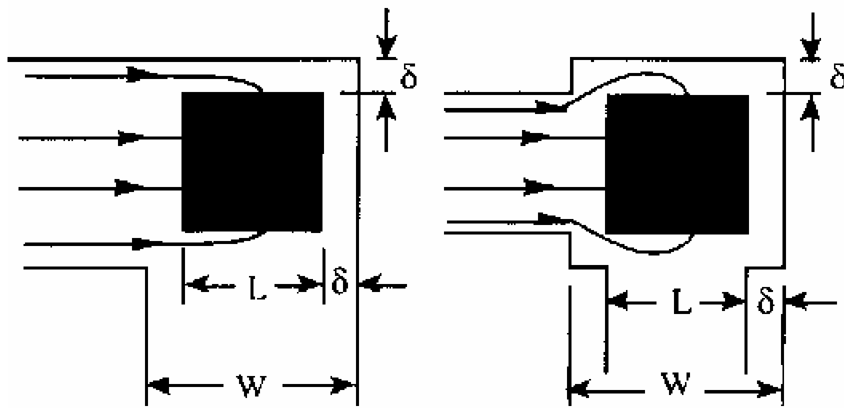



(a)



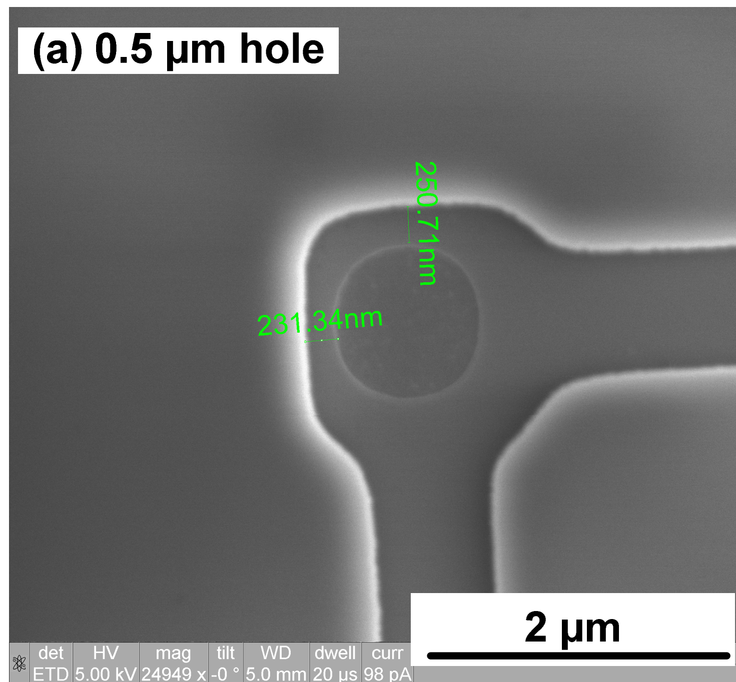

(b)

Fig.3-15 Activation energy of the (a) with and (b) without Ge I/I $n^+$-p shallow junctions annealed at 600 °C.




$$R_K = \frac{\rho_C}{l_y l_x} + \frac{4R_S\delta^2}{3W_xW_y}\left[1 + \frac{\delta}{2(W_x - \delta)}\right]$$

Fig.3-16 Current paths and calculation formula of L-type and D-type. [22]



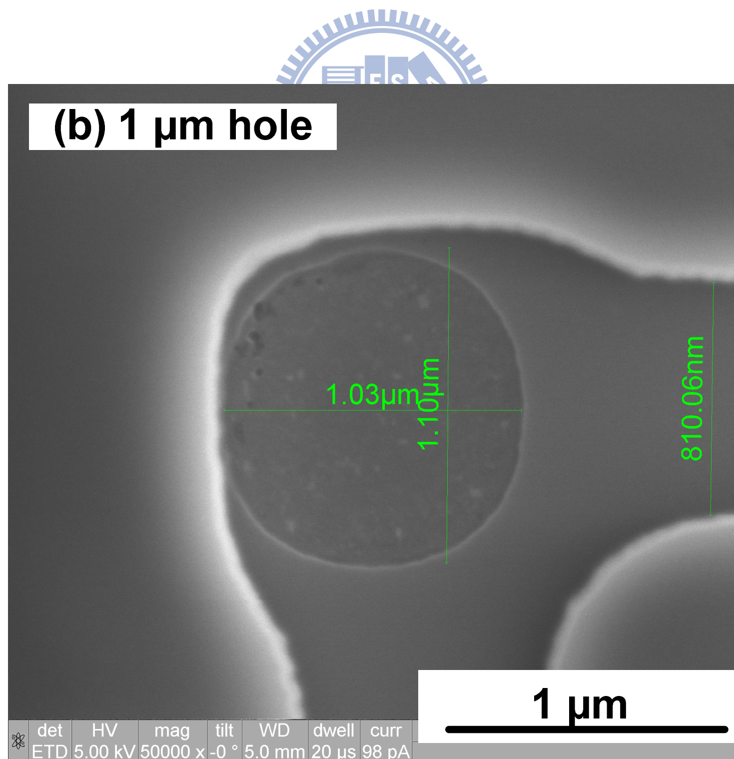




Fig.3-17 Fabricated D-typ CBKR structure with Ge I/I on $p^+$-Si.

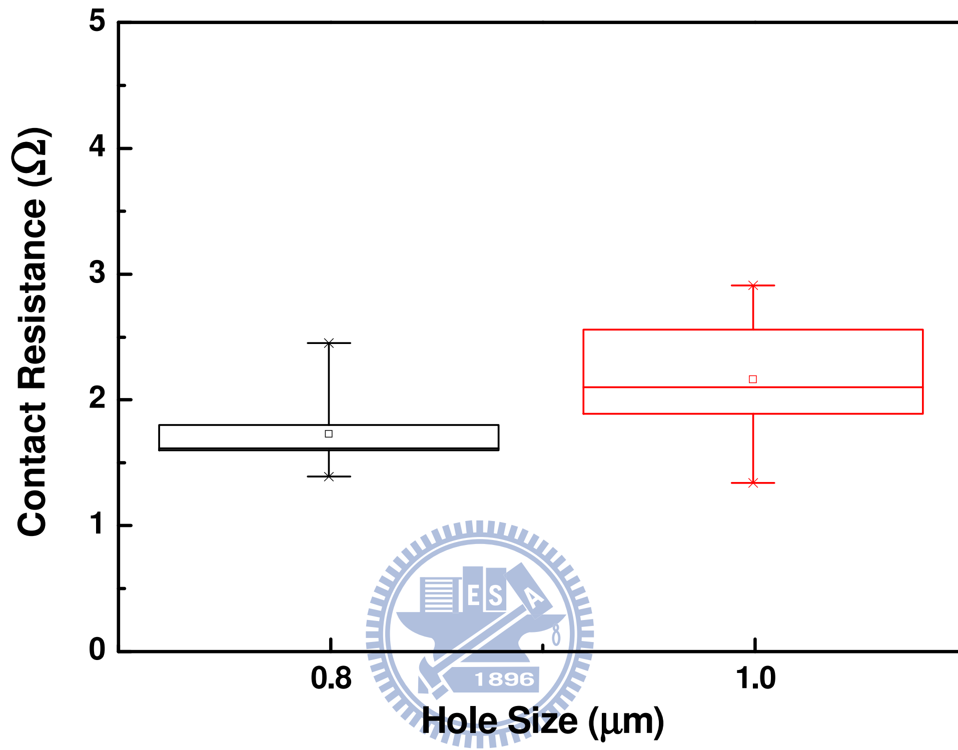



Fig.3-18 Measured contact resistance of D-type structure.

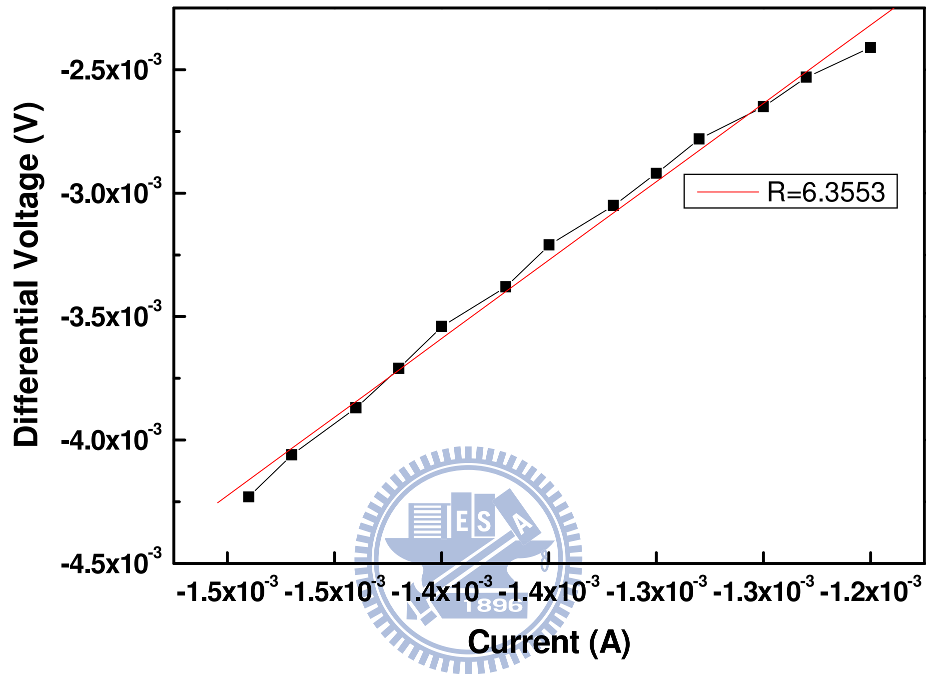



Fig.3-19 Measured contact resistance of D-type structure with 0.5μm hole size.

# Chapter 4

# Electrical Characteristics of NiSi Modified Schottky Barrier Lateral Junctions on SOI Substrate

## 4-1 Introduction

Many techniques have been invented to prevent large increases in leakage current or short channel effects, such as raised source/drain, new incorporations of Ni-silicide, and implant-through-silicide [1-4]. A Schottky-barrier (SB) MOSFET has abrupt junctions formed at the silicide/Si interface that enable the scaling of the device to the nanoscale region. SB MOSFETs have low source/drain (S/D) external resistance and low process temperature requirements. However, a large Schottky barrier height ($\Phi_b$) at the source junction might lower the on-state driving current. In previous studies, a complementary silicide contact S/D (PtSi for PMOS [5-6] and ErSi or YbSi for NMOS [7-8]) has been proposed to reduce $\Phi_b$ and improve the driving current. However, researchers are still searching for a single silicide that meets the low SB barrier height requirement for both conduction polarities, because the process for complementary silicides is rather complex. In recent years, implant into silicide (ITS) and dopant segregation techniques have been suggested as two major S/D junction modification processes [9-11]. Both methods employ implanted dopants segregated at the silicide/Si interface after a low-temperature process. The implanted Boron, Arsenic, and Phosphorous are usually used to lower $\Phi_b$ for $n^+$-p and $p^+$-n junctions.

In 2005, B. Y. Tsui and C. P. Lin reported a successful modified-Schottky-barrier (MSB) FinFET on SOI, which utilized an ITS technique, to place an interfacial layer between the silicide S/D and channel region [11]. Using a 4-nm-thick gate oxide, a current ratio ($I_{on}/I_{off}$) greater than $10^9$ and 60.4 mV/dec subthreshold swings for 49-nm MSB FinFETs were

achieved with small short channel effects at room temperature. The leakage current at the drain junction in the off-state is dominated by the surface generation current caused by the surface states at the gate oxide/Si and buried oxide/Si interfaces. Thin silicon on insulator (SOI) is very attractive for fully-depleted FinFET fabrication; the quality of SOI greatly affects device performance [12-17].

As the thermal stability of NiSi on SOI has been reported to be excellent, even above 850 °C, this thesis first investigated the thermal stability of NiSi films after $As^+$, $P^+$, or $BF_2^+$ implantation on an SOI wafer. Then, we fabricated $p^+$-n and $n^+$-p junctions on SOI wafers with the ITS technique. $As^+$ or $P^+$ was implanted to MSB $n^+$-p junctions and $BF_2^+$ was implanted to MSB $p^+$-n junctions. In addition, different durations of post implantation annealing were applied for the dopant drive-in. During annealing, implanted atoms were expected to diffuse out of the silicide films and pile up at the silicide/silicon interface. The accumulation of the dopant at the interface would lead to the desired SB height modification. The current–voltage (I–V) characteristics of these MSB junctions (both $p^+$-n and $n^+$-p) were investigated in the reverse bias region. We also examined the influences of interface traps at the front and back oxide/silicon interfaces for MSB junctions on SOI. The interface traps of junctions on SOI dominate the generation and recombination currents at the low-bias region. Both charge pumping and gated-diode techniques were used for interface quality characterization. Other studies have used these techniques on FD-MOSFETs or p-i-n diodes on SOI [15-17]. Here, we successfully evaluated the quantity of interface traps in our MSB junctions using these methods. Finally, based on our designed CBKR test structure (fabricated using the ITS method on SOI wafers), the contact resistance ($R_c$) of the MSB junction between the NiSi and $n^+$ or $p^+$ Si was also measured.

## 4-2 Experimental Procedures

### 4-2-1 MSB Junction Device Preparation

Initially, 6-inch silicon-on-insulator (SOI) wafers with a $1 \times 10^{15}$ $cm^{-3}$ boron-doped top Si layer were used. The top Si and buried oxide layers were 50 nm and 150 nm, respectively. Some of these were implanted with $As^+$ at 30 keV to a dose of $1 \times 10^{12}$ $cm^{-2}$ for MSB $p^+$-n junction preparation. The others were prepared for MSB $n^+$-p junctions. After that, the active regions were defined by electron-beam lithography and reactive ion etching on all of the wafers. Two contacts were defined in a junction device: a substrate contact and MSB contact. The substrate contact were first implanted using $As^+$ at 30 keV and $BF_2^+$ at 35 keV to a dose of $2 \times 10^{15}$ $cm^{-2}$ for MSB $p^+$-n and $n^+$-p junctions, respectively. After RCA cleaning, 3 nm of $SiO_2$ was grown using rapid thermal annealing at 1000 ºC for 20 s in $O_2$ ambient to remove the sidewall etching defects and activate the dopants. Then, a 150-nm passivation oxide was deposited by low-pressure chemical vapor deposition (LPCVD).

After that, the contact regions were defined and etched. A $SiO_2$ (15 nm)/$Si_3N_4$ (30 nm) composite spacer was formed at the silicide region's sidewall to prevent dopants from penetrating into the substrate in the following processes. Then, a Ni (25 nm)/TiN (5 nm) layer was deposited by physical vapor deposition (PVD) and a two-step silicidation process was performed to form nickel (Ni) silicide. The first step was 300 °C annealing in vacuum for 45 min and the second step was rapid thermal annealing (RTA) at 500 °C in $N_2$ ambient. After the silicide formation, the substrate contacts were protected by photo-resist and the following implantation was performed only on the MSB contact area.

The MSB contacts were implanted after the silicide formation. For $n^+$-p junctions, $As^+$ and $P^+$ were implanted at 30 keV and 25 keV, respectively, to a dose of $5 \times 10^{15}$ $cm^{-2}$. On the other hand, for $p^+$-n junctions, $BF_2^+$ was implanted at 35 keV to a dose of $5 \times 10^{15}$ $cm^{-2}$. All of

the wafers were then cut into smaller pieces and RTA was performed in $N_2$ ambient at different temperatures and annealing times.

After the MSB contact implantation, an aluminum pad was deposited using a thermal coater. The back side oxide and nitride were stripped, and aluminum evaporation was performed for the back contact. Finally, a sintering process was performed at 450 ºC in $N_2$ ambient for 30 min.

Fig.4-1 shows the process flow diagram of our MSB $n^+$-p junction's cross-section, and Fig.4-2 is a TEM image at the edge of the MSB $n^+$ region in Fig.4-1. In order to obtain sufficient junction leakage currents (>1 pA), the area of the lateral junction was increased. Fig. 2 shows two types of active regions for our junction. Fig.4-3(a) is an "island" type, marked with an "I," and Fig.4-3(b) is a "line" type, marked with an "L". Large numbers of junctions were connected to make junctions with different widths.

Conventional $n^+$-p and $p^+$-n junctions were also fabricated with the same process, but without Ni-silicide formation at the contact region.

### 4-2-2 Device Preparation for CBKR structure on SOI

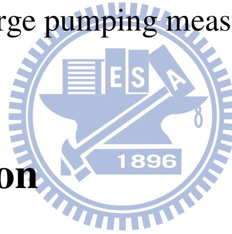
Initially 6-inch SOI wafers with 50 nm top silicon and 150 nm buried oxide were used. Some of them were implanted by $As^+$ at 30 keV to a dose of 5 × $10^{13}$ $cm^{-2}$ for $p^+$ MSB NiSi contacted CBKR structure. The others were implanted by $BF_2^+$ at 30 keV to a dose of 5 × $10^{13}$ $cm^{-2}$ for $n^+$ MSB NiSi contacted CBKR structure. The dopant activation was performed by 1000$^o$C rapid thermal annealing in $N_2$ ambient for 20 s. Then, active regions were defined by electron-beam lithography and reactive ion etching. The $SiO_2$ (15 nm)/$Si_3N_4$ (50 nm) composite passivation layer were deposited by LPCVD. After that, silicide regions were defined and passivation layer were etched by dry etching. Next, a Ni (25 nm) / TiN (5 nm) film was deposited by PVD. Two-step silicidation process was used for Ni silicide formation.

The first step was 300 °C annealing in vacuum for 45 min and the second step was rapid thermal annealing at 500 °C in $N_2$ ambient.

After silicide formation of MSB contacted region, $As^+$ and $BF_2^+$ were implanted to a dose of $5 \times 10^{15}$ $cm^{-2}$ at 30 keV and 35 keV, respectively, for $n^+$ and $p^+$ MSB NiSi contacted CBKR structure. All the samples were finally cut into small pieces and received RTA in $N_2$ ambient at different temperatures with different annealing times.

### 4-2-3 Analysis Method

The cross-sectional structure was inspected using a transmission electron microscope (TEM). The current–voltage (I–V) characteristics of the junctions were measured by a semiconductor parameter analyzer (Agilent 4156C). The Agilent 4156C and an HP 8110A were used for gated-diode and charge pumping measurements.




## 4-3 Results and Discussion

### 4-3-1 Thermal Stability of NiSi on SOI

The thermal stability of NiSi on SOI has been reported to be excellent even above 850 °C. Hence, before measuring the contact resistance, we measured the sheet resistance of ITS samples after annealing at different temperatures for 30 s, as illustrated in Fig.4-4. Three dopant sources ($As^+$, $P^+$, and $BF_2^+$) were employed in the experiments. The initial sheet resistance of the NiSi on SOI was 2.6 Ω/□ and after implantation all of the sheet resistance values increased to over 6 Ω/□. The ITS implantation would damage the NiSi grains and allow the sheet resistance to increase. The NiSi grains may re-organize after post annealing, causing the sheet resistance to decrease. From the XRD analysis of the $P^+$ implanted NiSi films in Fig.4-5, it can be seen that the NiSi peaks still vary obviously, even at 800 °C, and

that a non-$NiSi_2$ phase exists here. The phase transformation of NiSi into $NiSi_2$ should be because of the Si source at the NiSi bottom, but no Si exists on the full-silicide layer of SOI. The same results could be seen in the $As^+$ and $BF_2^+$ implanted NiSi films on SOI, are shown in Fig.4-6 and Fig.4-7. There also has strong intensity around 33~35 degree, which implies the $NiSi_2$ phase exist, but we have not seen another $NiSi_2$ phase in XRD result. This unreasonable phenomenon may be checked in the future works.

The plan-view SEM images of the NiSi films on $P^+$ implanted samples after 30 s of annealing at various RTA temperatures are shown in Fig.4-8, while those of the $BF_2^+$ implanted samples are shown in Fig.4-9. Both the $P^+$ and $BF_2^+$ implanted samples have small surface pits at 550 °C, and then re-organize to form a large grain area at 600 °C. Finally, they all divided into medium grains and had rougher silicide surfaces. From the XRD and sheet resistance analysis, the NiSi just experienced local grain grooving because obvious NiSi peaks still exist at 800 °C and it maintains a low resistivity. Fig.4-10 shows plan-view SEM images of NiSi films on $As^+$ implanted samples after annealing for 30 s at various RTA temperatures. The re-organizing temperature of the As implanted sample seems to have been 100 °C higher than those of the $P^+$ and $BF_2^+$ implanted samples. This result is quite different from the NiSi on bulk-Si. The changes in the surface roughness of the ITS NiSi films was considered to be due to the NiSi grain grooving. Because no Si remains for a full silicide film on BOX layer, the agglomeration of NiSi and phase transformation of $NiSi_2$ were eliminated.

### 4-3-2 Electrical Characteristics of Conventional Junctions

Fig.4-11 shows the basic I–V characteristics of our conventional $n^+$-p and $p^+$-n junctions. Their widths were 500 or 1000 μm for both L and I type junctions. The n values of the forward current were around 1.4 for $n^+$-p junctions and 1.35 for $p^+$-n junctions, both with a non-annealed TEOS passivation oxide. The higher n values were caused by traps at the Si/buried oxide (BOX) and Si/passivation oxide interfaces. These traps induced excess

recombination currents.

These n factors were too high for device fabrication and annealing had to be performed. After annealing at 950 °C for 30 min in $N_2$, the oxide traps and interface traps were largely eliminated and the n factor was obviously decreased in the $p^+$-n junction, as shown in Fig.4-12. However, in the $n^+$-p junction, there was less of an improvement. Fig.4-13 shows the statistics for the reverse biased (3 V) junction leakage current of the (a) $n^+$-p and (b) $p^+$-n junctions after annealing at 950 °C for 30 min in $N_2$. The junction leakage currents were also decreased by this annealing. The leakage current of the L type junction was higher than the I type junction, because of its larger sidewall area, which caused more interface charges.

Based on this result, we performed an annealing step on our MSB junctions after passivation. The interface trap densities were measured and are discussed later.

### 4-3-3 Electrical Characteristics of MSB Junctions

The MSB $p^+$-n junction was implanted with $BF_2^+$ and annealed at different temperatures for 30 s. Fig.4-14 shows the junction leakage current statistics of the MSB $p^+$-n junction after annealing. The original Schottky junction has the highest leakage current, at around $10^{-5}$ A. After being implanted with $BF_2^+$ and annealed, the leakage currents of the $p^+$-n junctions were decreased to $10^{-9}$ A. This was attributed to the segregation of the dopant from the Ni-silicide and diffusion to the $n^-$ Si substrate.

Band diagrams for both the Schottky and MSB $p^+$-n junctions at reverse bias are schematically illustrated in Figs.4-15(a) and (b), respectively. The MSB contact has a wider and higher barrier than the Schottky contact. Thus, electron tunneling at reverse bias was efficiently blocked in the MSB case. The minimum average leakage current was measured on samples with different annealing temperatures. Below 600 °C, defects caused by implantation might exist at the spacer. In addition, the thermal budgets were insufficient for boron to segregate from the Ni-silicide. As the annealing temperature increased, the leakage current

slightly increased. This was because of the re-diffusion of Ni ions along the sidewall corners during annealing. The average leakage current of the MSB $p^+$-n junction annealed at 600 °C is given in Table 4-1. Using equation (3.5), $J_R = J_{RA} + J_{RP}$ (P/A), we can determine the current density of the junction base area or peripheral. In our junctions, the leakage currents were almost always attributed to the peripheral because of the large P/A values (~ $4.4 \times 10^5$) and small $J_{RA}$ ($J_R >> J_{RA}$). Hence, the leakage current was obviously increased in the 500L type junctions due to their large number of sidewalls and corners.

The junction leakage current was also measured for the $As^+$ and $P^+$ implanted MSB $n^+$-p junctions, as shown in Figs.4-16 and Fig.4-17, respectively. The as-implanted junctions had leakage currents of $6 \times 10^{-6}$ A. As the post-annealing temperature increased, the leakage current decreased to around $8 \times 10^{-10}$ in the $As^+$ implanted junction and to $3 \times 10^{-9}$ in the $P^+$ implanted junction. The different values of leakage current implied that the segregation of As ions from the Ni-silicide was more effective than that of P ions. From our results, the thermal budgets required for dopant aggregation were smaller for As and P ions than for B ions. However, the higher concentration of the $n^-$ substrate compared to the $p^-$ substrate might also affect the results. The thermal budgets required for dopant segregation were similar to those found in studies on bulk Si.

The activation energy ($E_a$) of the MSB $p^+$-n junction annealed at 600 °C was extracted from equation (3.6), as shown in Fig.4-18(a). The $E_a$ values measured at the reverse biases of 3 V and 1 V were 0.524 and 0.582, respectively. As the reverse bias increases, the depletion width, and hence the generation current, also increases. Thus, the $E_a$ extracted at a -3 V bias was closer to $E_g/2$ than that at a -1 V bias. Usually, the diffusion current would increase and dominate the leakage current. However, in our device, the generation current still dominated because a large number of traps existed at the Si/BOX and Si/passivation oxide interfaces. The same results were also found for the MSB $n^+$-p junctions annealed at 600 °C and implanted with $As^+$ and $P^+$, as shown in Figs.4-19(a) and (b), respectively. Post-annealing

with different durations and temperatures was performed on the MSB $p^+$-n junctions and the $E_a$ values were also determined. Fig. 4-17(b) shows that the L type junctions have smaller $E_a$ values than the I type junctions, and that the $E_a$ was pinned at around $E_g/2$. This is because the L type junction has more sidewall areas than the I type, which contributes more defects.

### 4-3-4 Interface Trap density Measurement of MSB Junctions

The schematic diagrams of the gated-diode method are illustrated in Fig.4-20. Fig. 4-20(a) shows a measurement setup diagram and Fig. 4-19(b) is the measured I–V characteristic. The total currents in Fig.4-20(b) are attributed to the generation current of the metallurgical junction ($I_1$), the generation current of the field induced junction ($I_2$), and the surface generation current ($I_3$). The interface trap density per area ($D_{it}$) could be calculated from equation (4.1).

$$I_3 = \frac{1}{2} q n_i s_o A_s, \qquad s_o = \sigma v_{th} \left(\pi kT D_{it}\right) \quad \text{.....(4.1)}$$

The gated-diode characteristics of MSB (a) $p^+$-n and (b) $n^+$-p 1000I type 600 °C annealed junctions are shown in Fig.4-21. The applied voltage, $V_d$, provided a lateral electrical field. Thus, the conducting current increased as $V_d$ increased in the accumulation region. As $V_g$ was applied at the depletion region, the Si/BOX interface traps could be measured. From depletion to inversion, the thin SOI layer causes an abrupt current variation. The threshold voltage shift increases as $V_d$ increases because the junction depletion width is increased. The $D_{it}$ ($cm^{-2} \cdot eV^{-1}$) values calculated at a 1 V reverse bias are $2.02 \times 10^{11}$ for the MSB $p^+$-n junction and $5.03 \times 10^{11}$ for the MSB $n^+$-p junction. A $D_{it}$ value greater than $1 \times 10^{11}$ is too high to use in high-performance MOSFET devices. It would decay the $I_{on}/I_{off}$ ratio.

The charge pumping method was also applied to the 1000I type MSB $p^+$-n junction that was annealed at 600 °C. The measurement schematic diagram and band diagram vs. I–V characteristics are shown in Figs.4-22(a) and (b), respectively. The $I_{cp}$ vs. $V_{base}$ results are

shown in Fig.4-23. The $D_{it}$ is 1.17 × $10^{11}$ ($cm^{-2}$ · $eV^{-1}$) at $V_{amp}$ = 6 V and $\Delta\psi_s$ = 0.56, according to equation (4.2). By applying a triangular wave with $V_{amp}$ = 6 V at different frequencies, the interface trap density could be extracted from equation (4.3). Fig.4-24 shows $Q_{ss}$ vs. ln(*f*). The slope = $2qD_{it}A_GkT$ and gives an interface trap density of 1.6 × $10^{11}$ ($cm^{-2}$ · $eV^{-1}$).

$$I_{CP} = qfA_G \int_{E_{em,h}}^{E_{em,e}} D_{it}(E)dE \approx qfA_G \overline{D_{it}}\left(E_{em,e} - E_{em,h}\right) \approx qfA_G \overline{D_{it}} \Delta\psi_s \qquad .....(4.2)$$

$$Q_{SS} = \frac{I_{CP}}{f} = 2q\overline{D_{it}}A_G kT\left[\ln\left(v_{th}n_i\sqrt{\sigma_n\sigma_p}\right) + \ln\left(\frac{|V_{FB} - V_t|}{\Delta V_G}\frac{\sqrt{\alpha(1-\alpha)}}{f}\right)\right] \qquad .....(4.3)$$

### 4-3-5 Contact Resistance Measurement

The $p^+$ and $n^+$ MSB contacts were fabricated on an SOI wafer, as shown in Fig.4-25. The sheet resistance of the NiSi and low-doping Si substrate are 7.6 Ω/□ and 285 Ω/□, respectively. The total resistance of the lateral CBKR structure consists of the substrate resistance and contact resistance of the NiSi/MSB interface. The $n^+$ MSB contact was implanted with As and annealed at 600 °C. The total resistance of the $n^+$ MSB contact was measured with line width variations, and the calculated specific contact resistivity was illustrated in Fig.4-26. The efficiency of the dopant diffusion to the interface is related to the line width, with a smaller line width causing fewer dopants to be required for a high-concentration interface. The same result was also considered in the $p^+$ MSB contact, as shown in Fig.4-27. The specific contact resistivity of the $p^+$ MSB contact is around 2 × $10^{-8}$, which is much lower than that of the $n^+$ MSB contact (~3 × $10^{-7}$).

## 4-4 Conclusions

The ITS technique was used for SOI lateral junctions. The thermal stability of the $As^+$, $P^+$, and $BF_2^+$ ITS samples was examined. The ITS NiSi maintained the same good thermal stability as non-implanted NiSi on SOI. Although the SEM showed local roughness in a small area, the sheet resistance was still low after post annealing. MSB $p^+$-n junctions with implanted $BF_2^+$ and MSB $n^+$-p junctions with implanted $As^+$ and $P^+$ were fabricated. The MSB $p^+$-n junction annealed at 600 °C had the smallest leakage current compared to the other annealing temperatures. The decrease in junction leakage current could be attributed to B ions segregated from the Ni-silicide after the post-annealing. The MSB $n^+$-p junctions with implanted $As^+$ and $P^+$ had the same results after the RTA. A 500 °C post annealing process could largely decrease the junction leakage current. The influences of the thermal budget and type of junction were discussed. The large n values of conventional $n^+$-p junctions implies more interface traps than $p^+$-n junctions. The interface traps were found to come from sidewalls. The Si/BOX interface and Si/passivation oxide interface were also discussed. The measured $E_a$ values of our MSB junctions were all pinned at around $E_g/2$. Gated-diode and charge pumping methods were utilized. The $D_{it}$ values calculated from these methods were about $2 \times 10^{11}$ ($cm^{-2} \cdot eV^{-1}$) for the MSB $p^+$-n junction and $5 \times 10^{11}$ ($cm^{-2} \cdot eV^{-1}$) for the MSB $n^+$-p junction. The $n^+$ and $p^+$ MSB contacts fabricated on SOI were also successfully measured. The $p^+$ MSB contact showed lower resistivity, which might come from the low barrier height of the NiSi.

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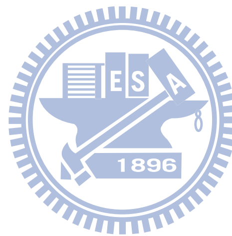


Table 4-1 Average leakage currents of MSB $p^+$-n junction annealed at 600 $^oC$.

| | W | D | A | P | P/A | I | J | $J_{RP}$ |
|---|---|---|---|---|---|---|---|---|
| 500I | $5.00 \times 10^{-2}$ | $4.50 \times 10^{-6}$ | $4.50 \times 10^{-5}$ | 20.00 | $4.44 \times 10^{5}$ | $2.59 \times 10^{-10}$ | $5.76 \times 10^{-6}$ | $1.29 \times 10^{-11}$ |
| 1000I | $1.00 \times 10^{-1}$ | $4.50 \times 10^{-6}$ | $4.50 \times 10^{-5}$ | 20.00 | $4.44 \times 10^{5}$ | $3.28 \times 10^{-10}$ | $7.29 \times 10^{-6}$ | $1.64 \times 10^{-11}$ |
| 500L | $1.50 \times 10^{-3}$ | $4.50 \times 10^{-6}$ | $4.59 \times 10^{-5}$ | 20.05 | $4.46 \times 10^{5}$ | $5.59 \times 10^{-10}$ | $1.22 \times 10^{-5}$ | $2.73 \times 10^{-11}$ |
| 1000L | $1.50 \times 10^{-3}$ | $4.50 \times 10^{-6}$ | $4.52 \times 10^{-5}$ | 20.02 | $4.46 \times 10^{5}$ | $3.63 \times 10^{-10}$ | $8.02 \times 10^{-6}$ | $1.80 \times 10^{-11}$ |

W: width of junction (cm)

D: depth of junction (cm)

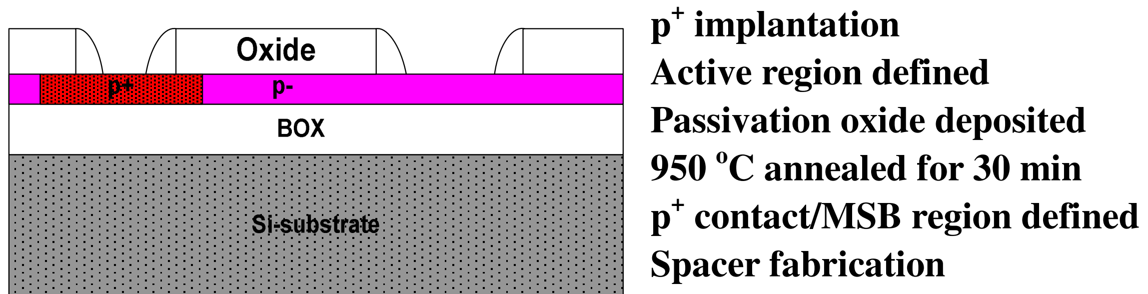
A: total area of junction ($cm^2$)

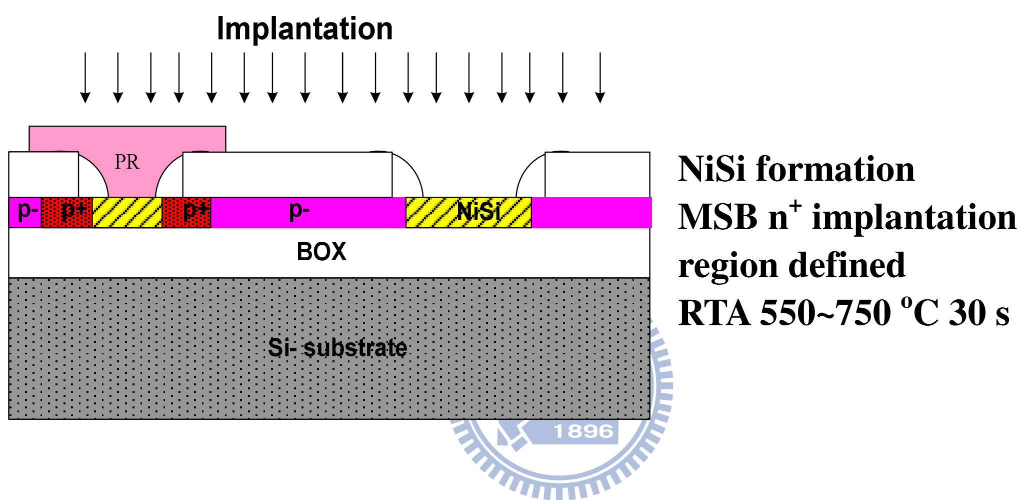
P: total peripheral of junction (cm)

I: leakage current of junction (A)

J: current density of junction ($A/cm^2$)

$J_{RP}$: peripheral current density of junction (A/cm)



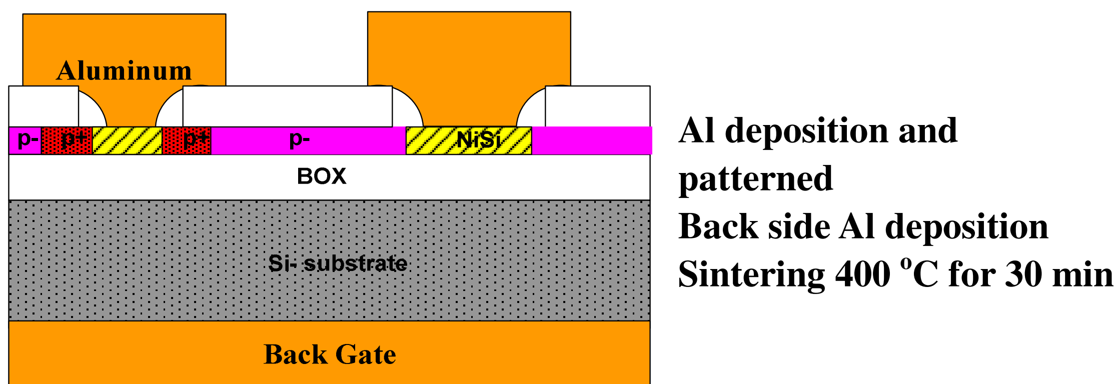




Fig.4-1 Process flow for MSB $n^+$-p junction.

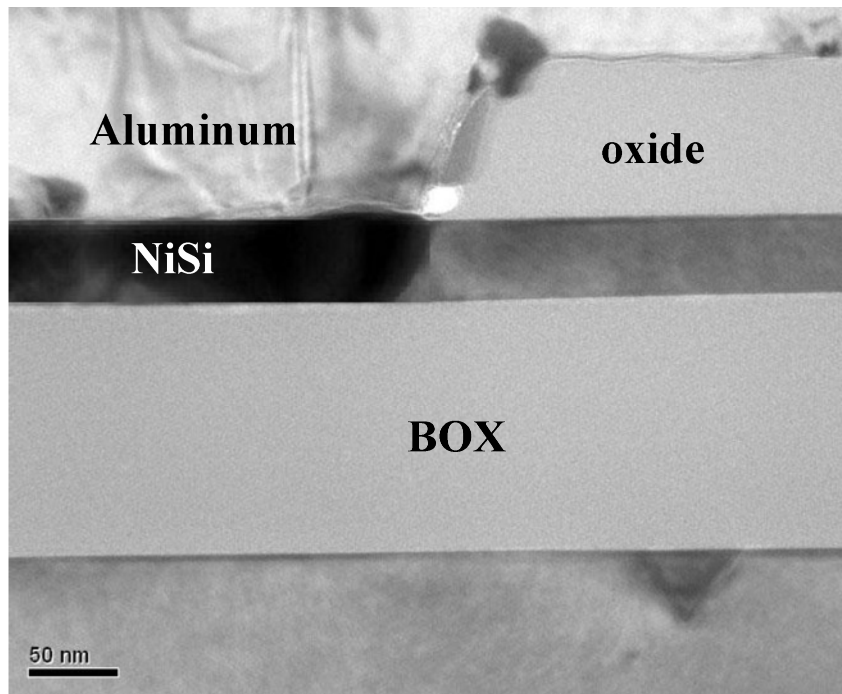
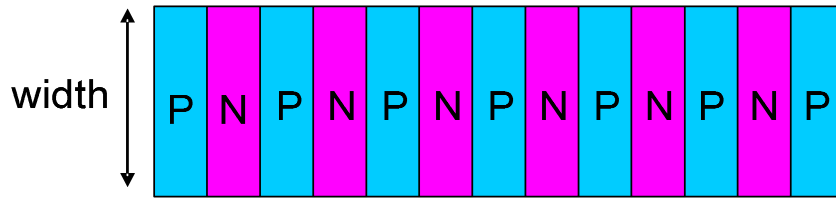
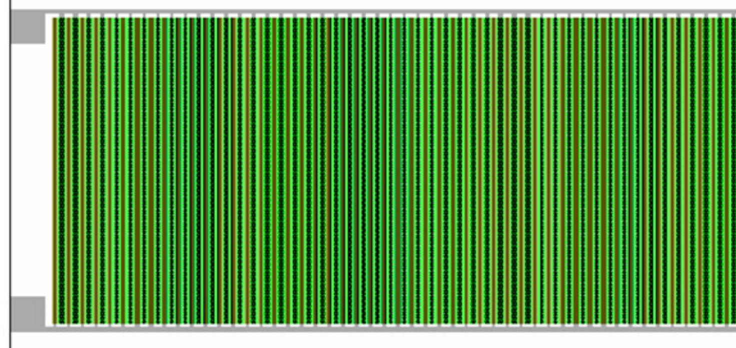
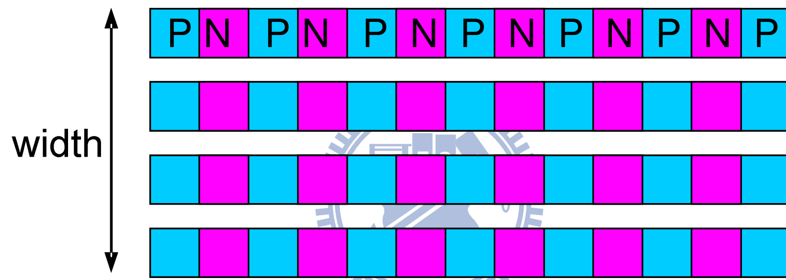


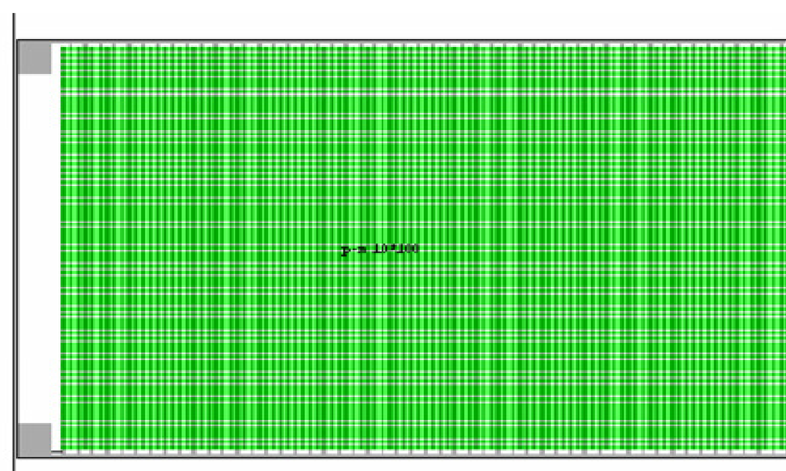

Fig.4-2 TEM cross section view of MSB $n^+$ region edge.



**(a)**



**(b)**

Fig.4-3 Two categories of MSB junction's active region. (a) is Island type marked as "I", and (b) is Line type marked as "L".

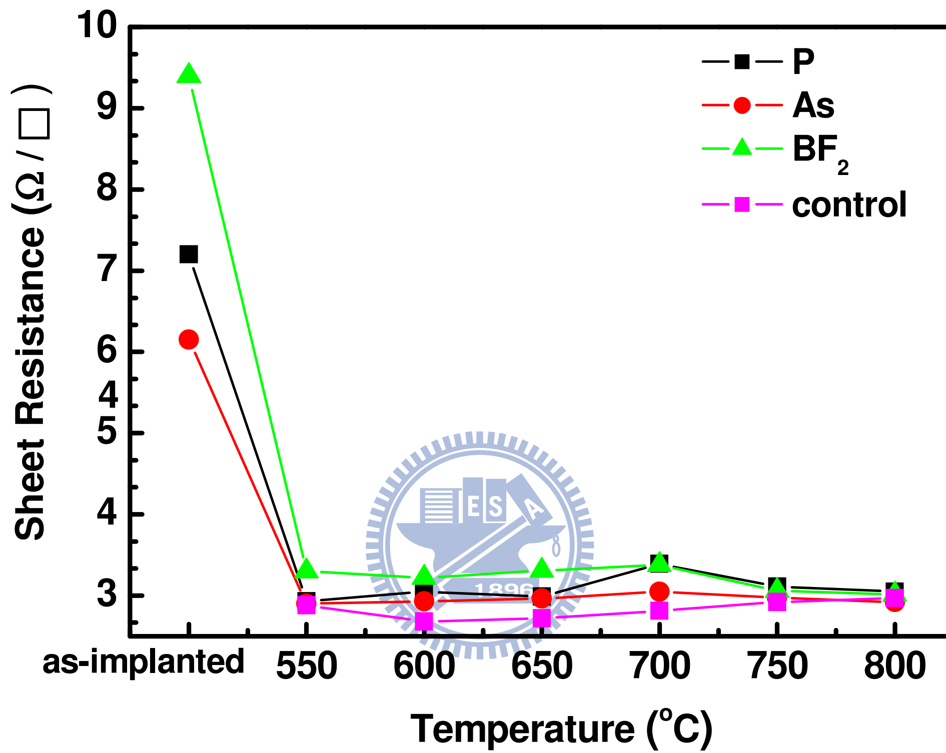



Fig.4-4 Sheet resistance values of the ITS samples after annealing at different temperatures for 30 sec.

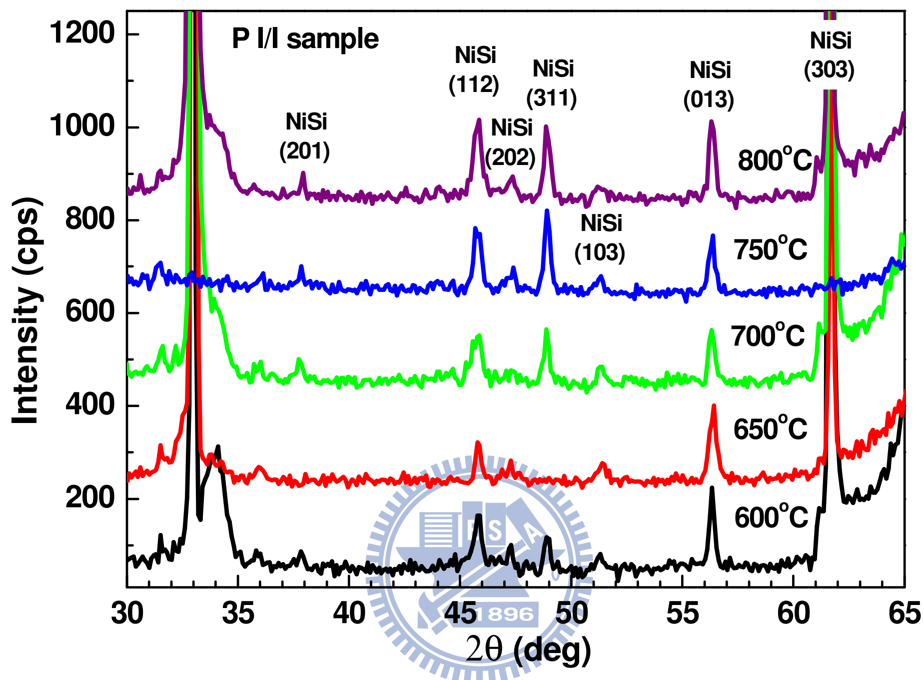



Fig.4-5 XRD spectra of the P implanted ITS samples after annealing at different temperatures for 30 sec.

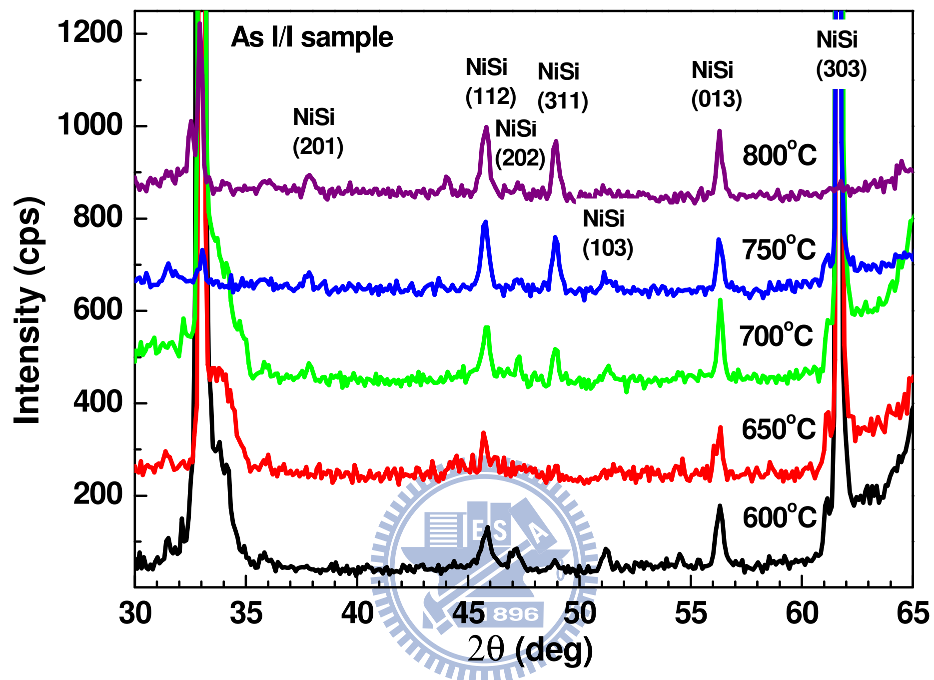



Fig.4-6 XRD spectra of the As implanted ITS samples after annealing at different temperatures for 30 sec.

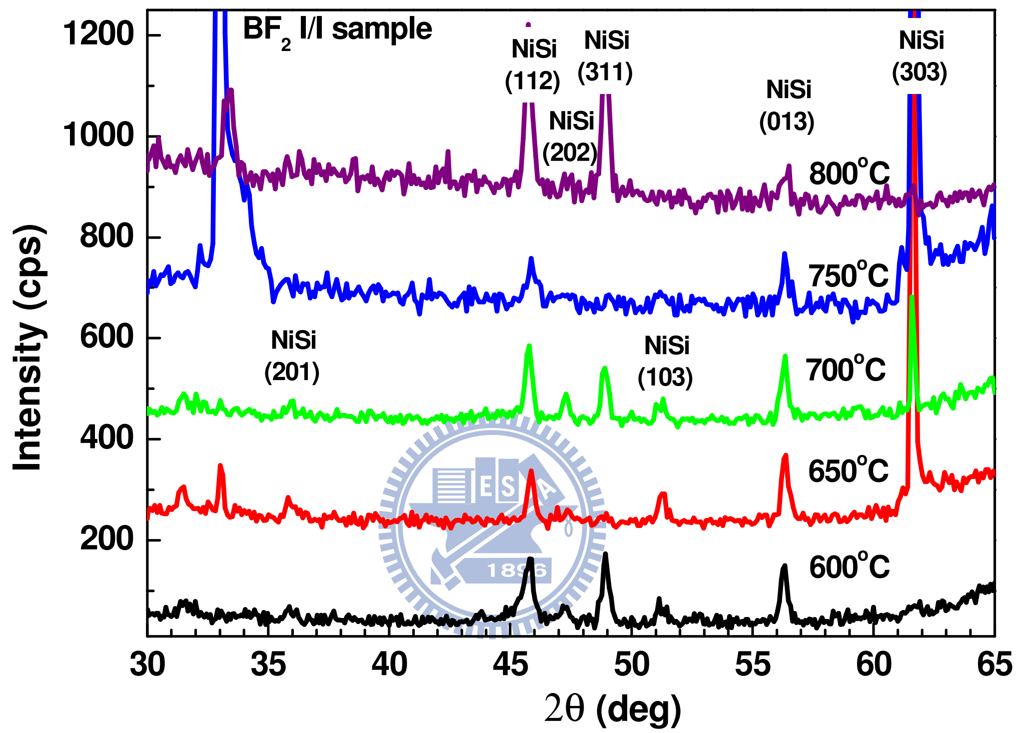



Fig.4-7 XRD spectra of the $BF_2$ implanted ITS samples after annealing at different temperatures for 30 sec.

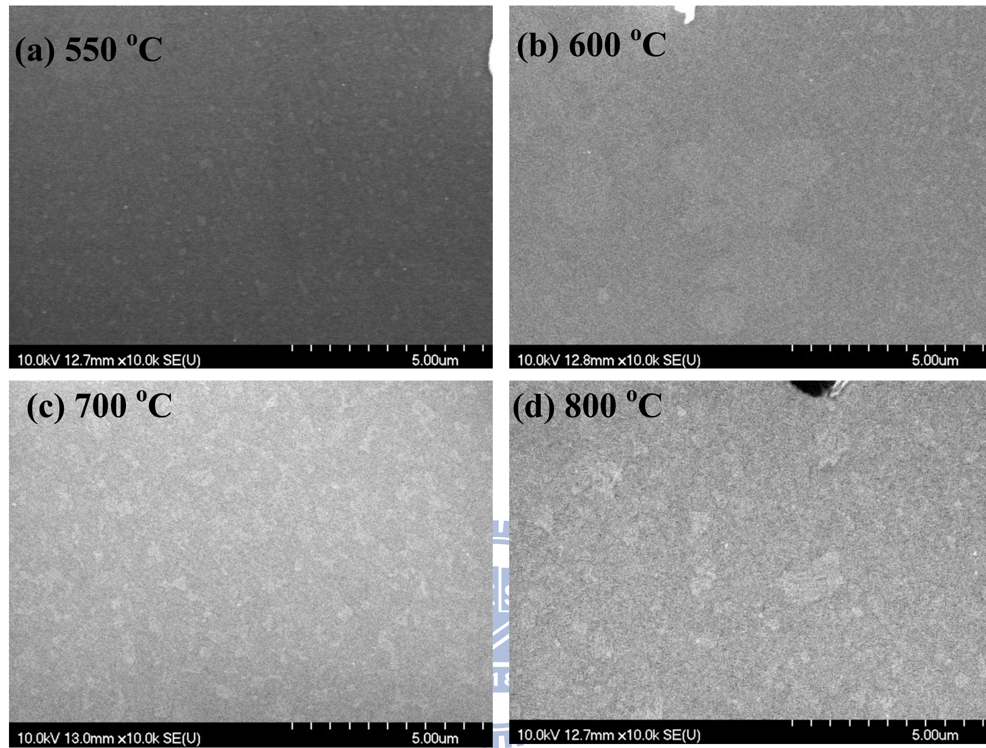



Fig.4-8 Plan-view SEM images of NiSi with P implanted ITS samples after various RTA annealing temperatures for 30 s on SOI.

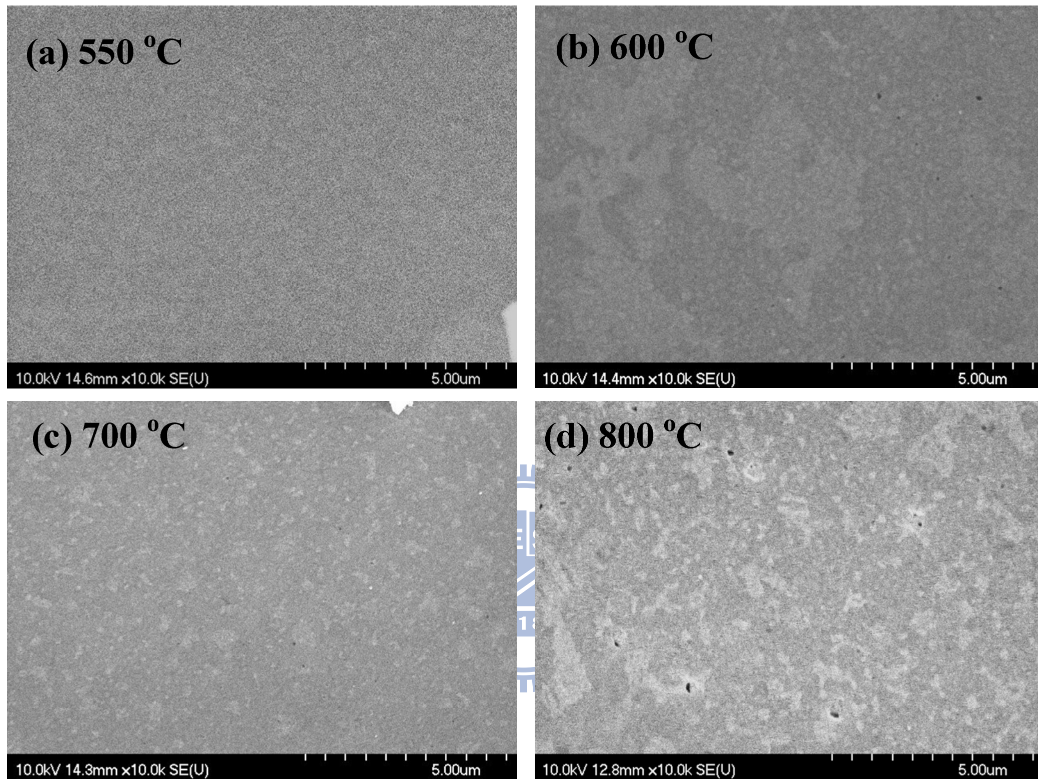



Fig.4-9 Plan-view SEM images of NiSi with $BF_2$ implanted ITS samples after various RTA annealing temperatures for 30 s on SOI.

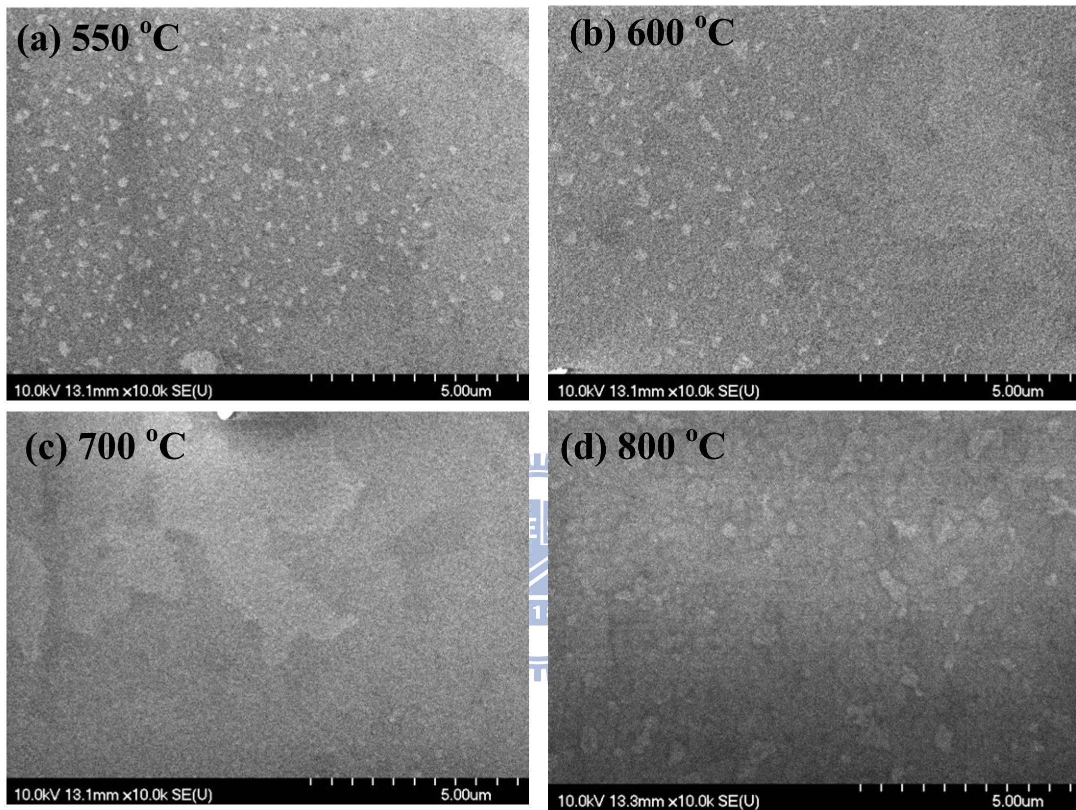
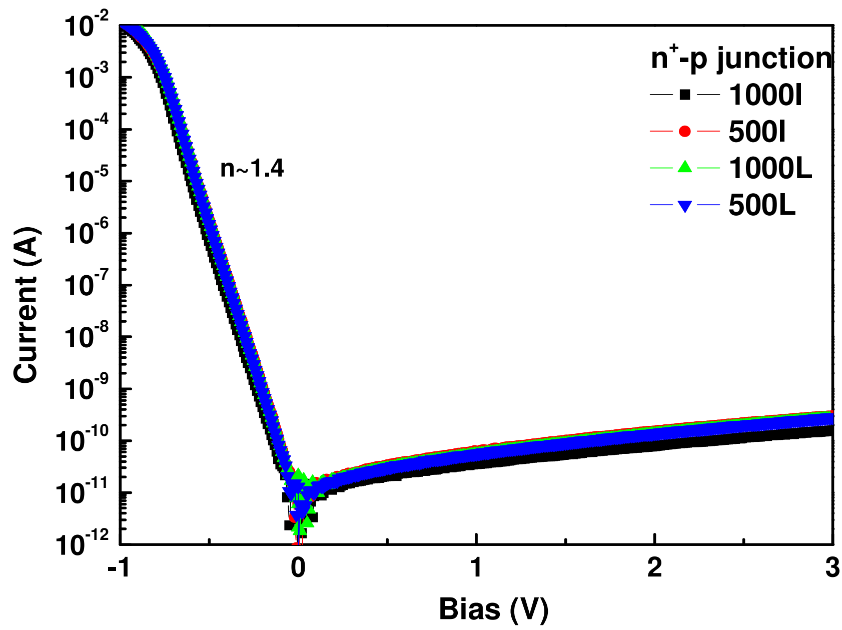
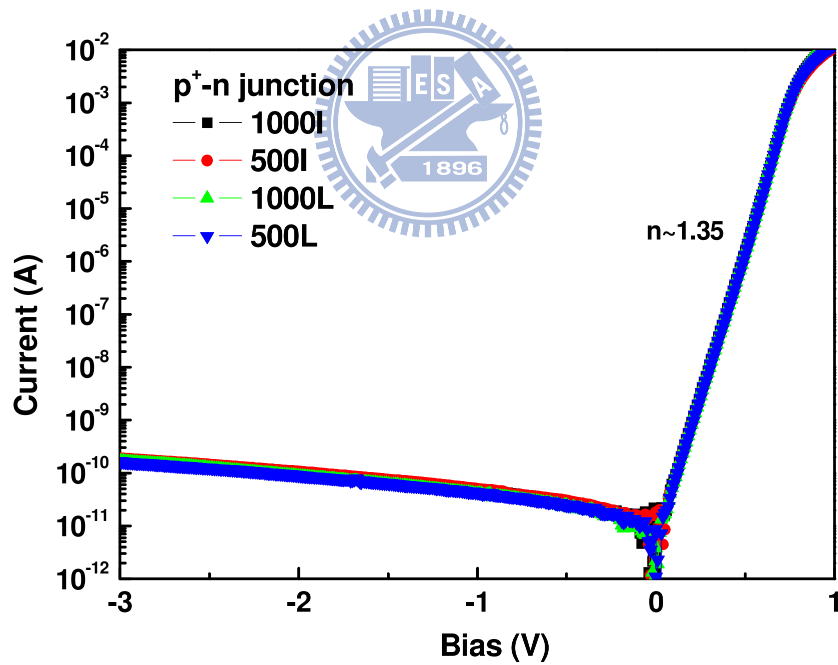



Fig.4-10 Plan-view SEM images of NiSi with As implanted ITS samples after various RTA annealing temperatures for 30 s on SOI.

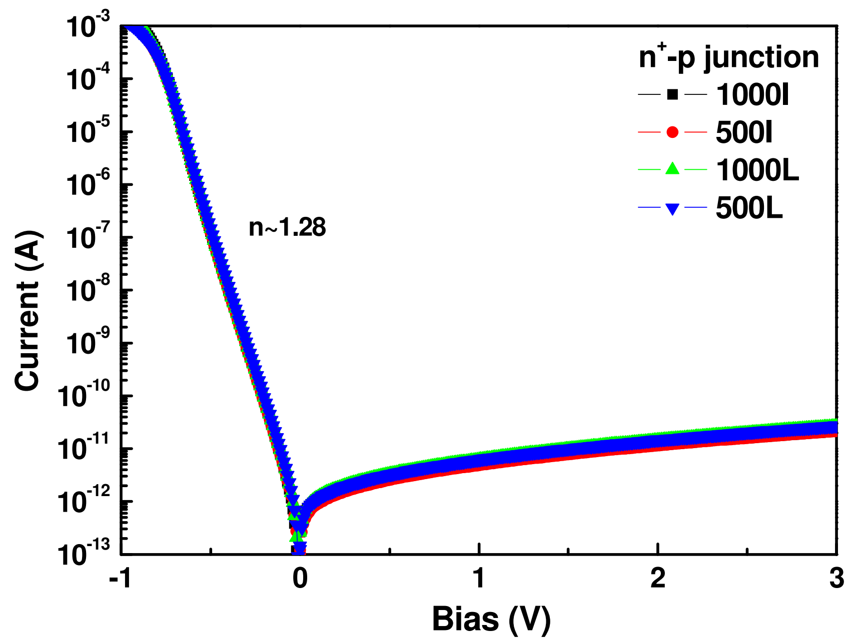



(a)

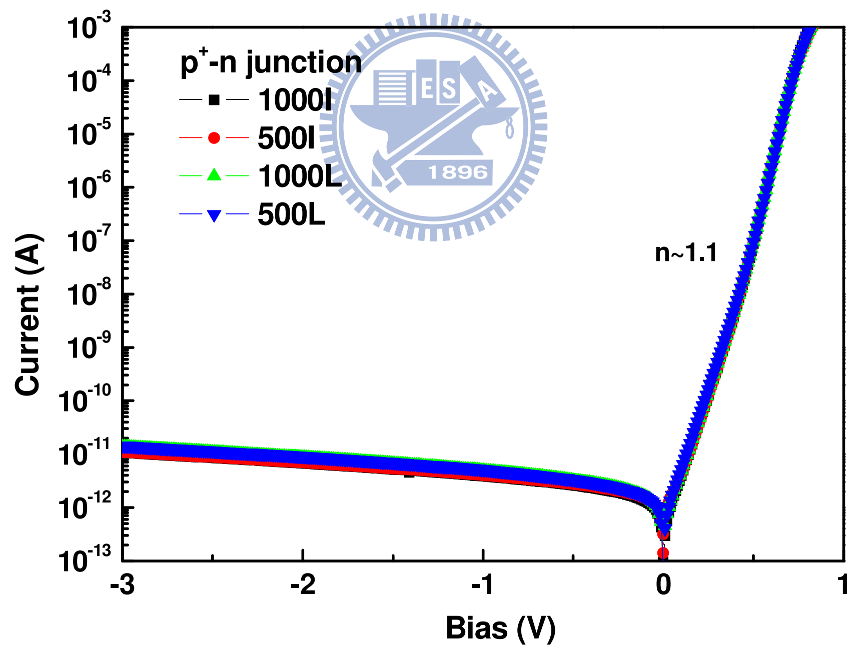



(b)

Fig.4-11 Basic I-V characteristic of conventional $n^+$-p and $p^+$-n junctions, the width of them were designed as 500 or 1000 $\mu$m for L and I type junctions.

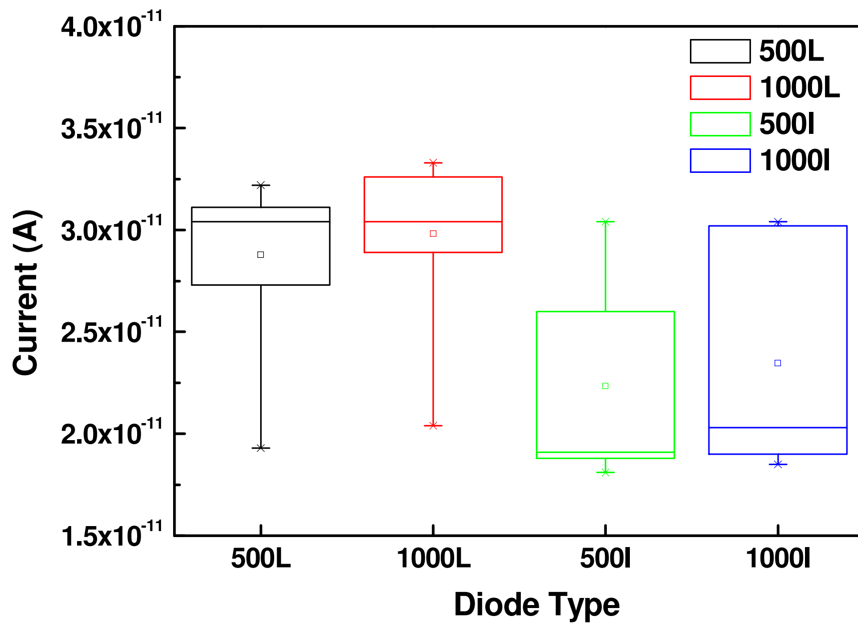



(a)

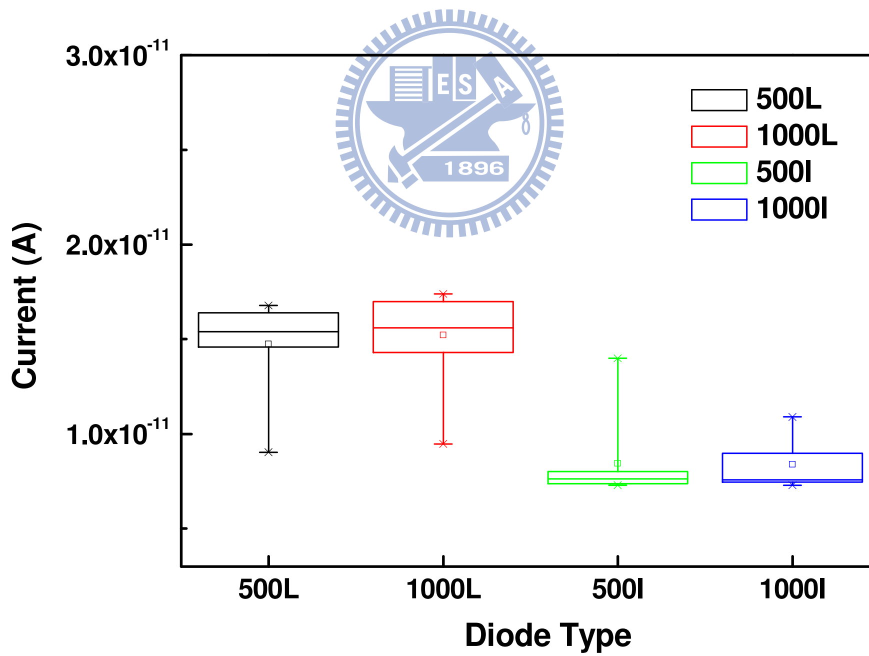



(b)

Fig.4-12 Basic I-V characteristic of conventional $n^+$-p and $p^+$-n junctions after passivation oxide annealed at 950 $^oC$ for 30 min in $N_2$.

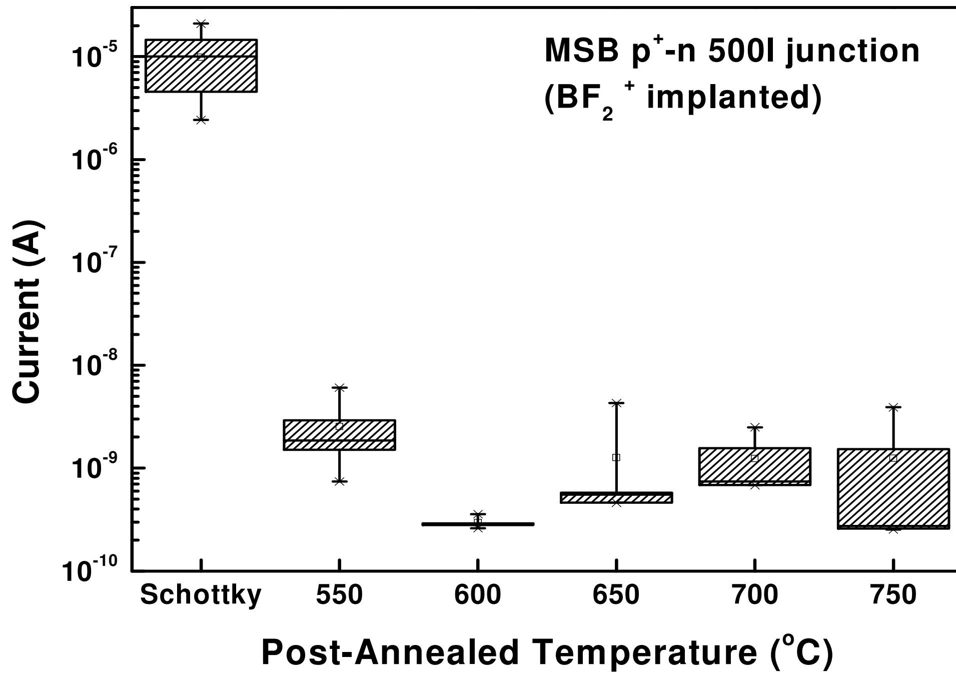



(a)

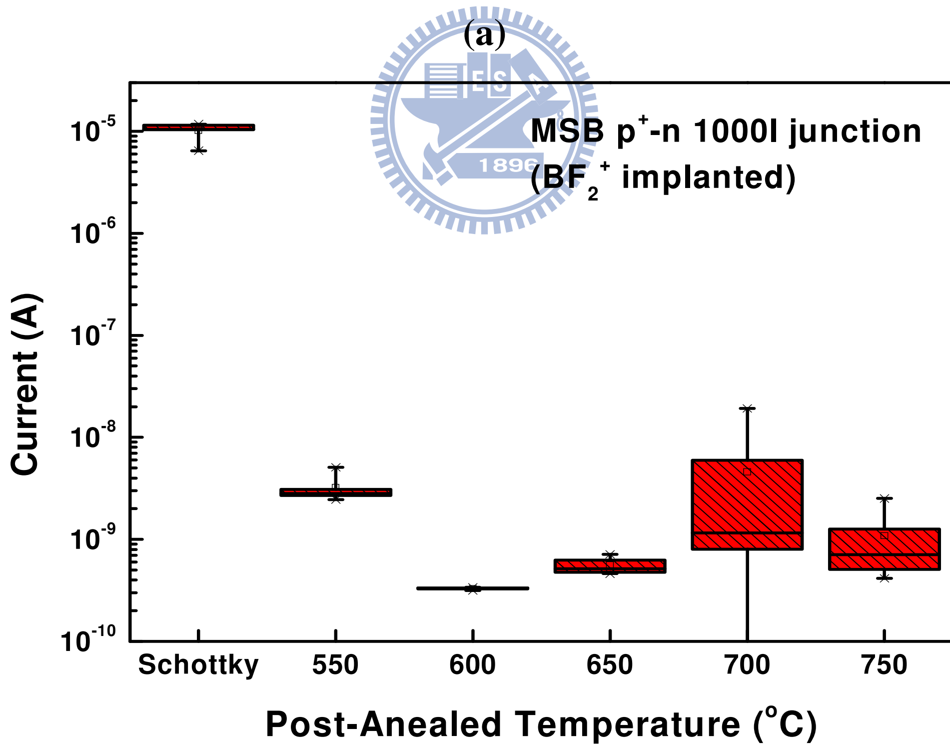



(b)

Fig.4-13 Reverse biased (3V) junction leakage current statistics of the (a) $n^+$-p and (b) $p^+$-n junction after passivation oxide annealed at 950 °C for 30 min in $N_2$.

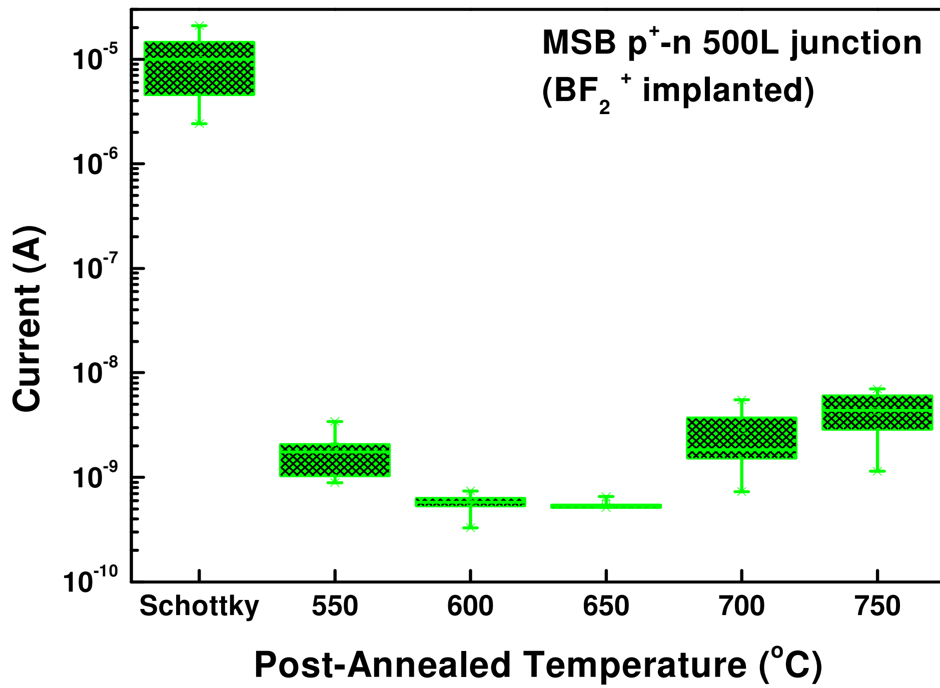



(a)

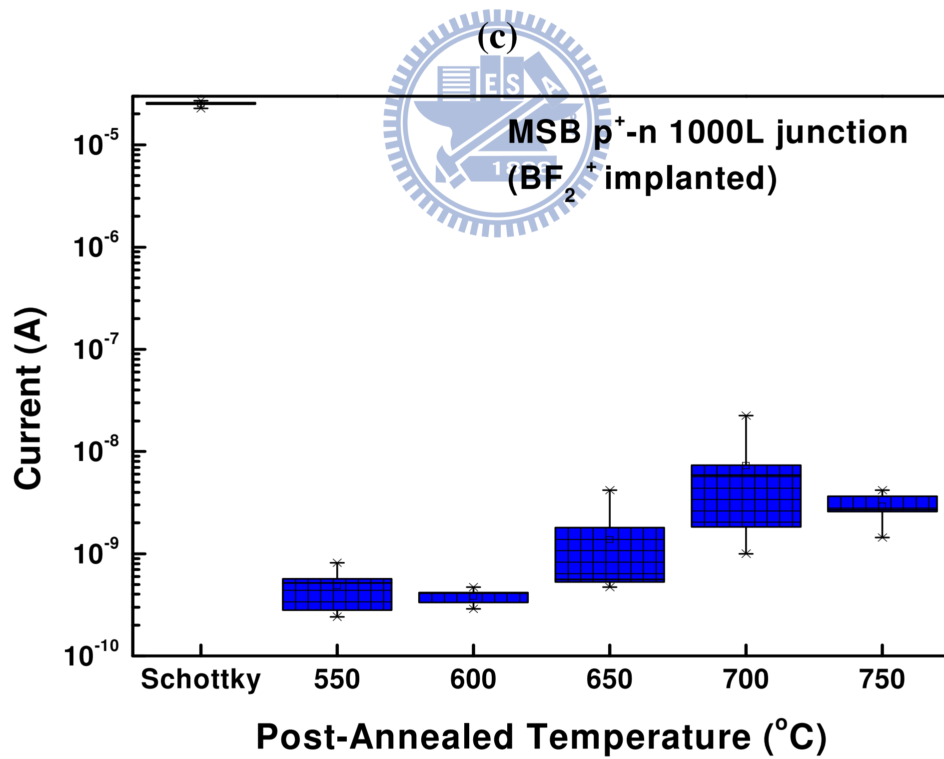



(b)

Fig.4-14 Reverse biased (3V) junction leakage current statistics of the (a) 500I and (b) 1000I type MSB $p^+$-n junctions.




(c)




(d)

Fig.4-14 Reverse biased (3V) junction leakage current statistics of the (c) 500L and (d) 1000L type MSB $p^+$-n junctions.

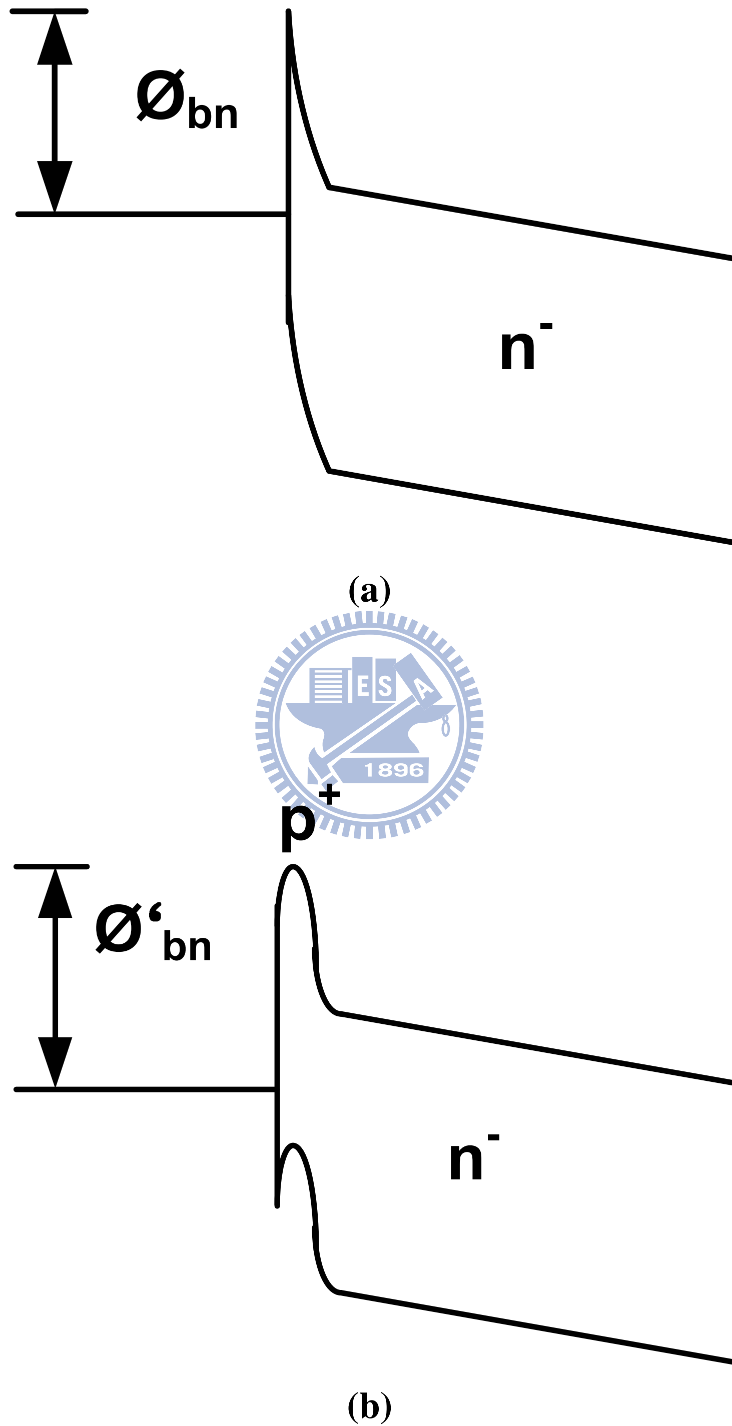
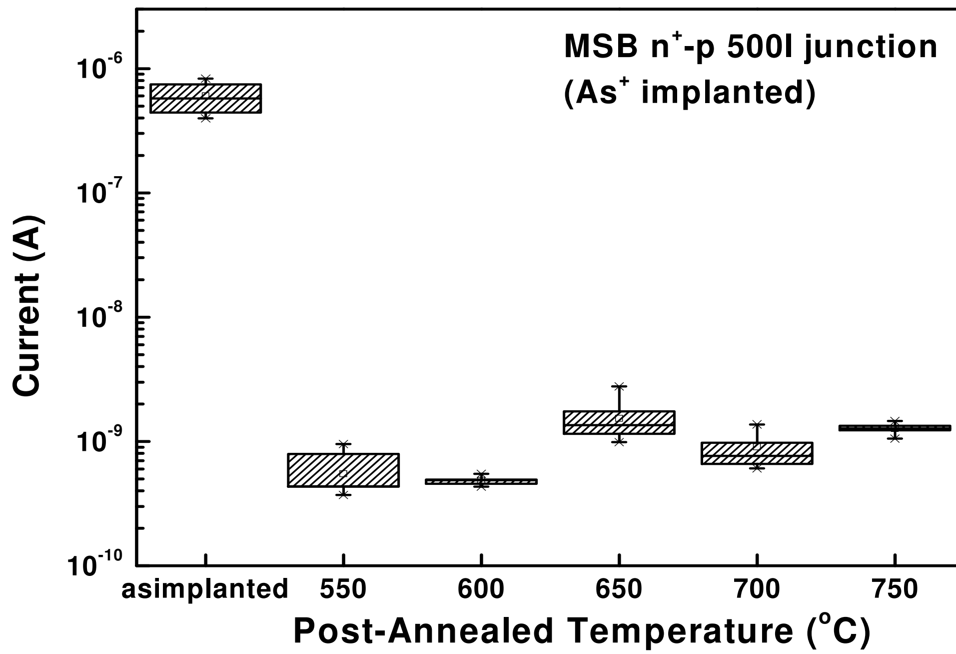
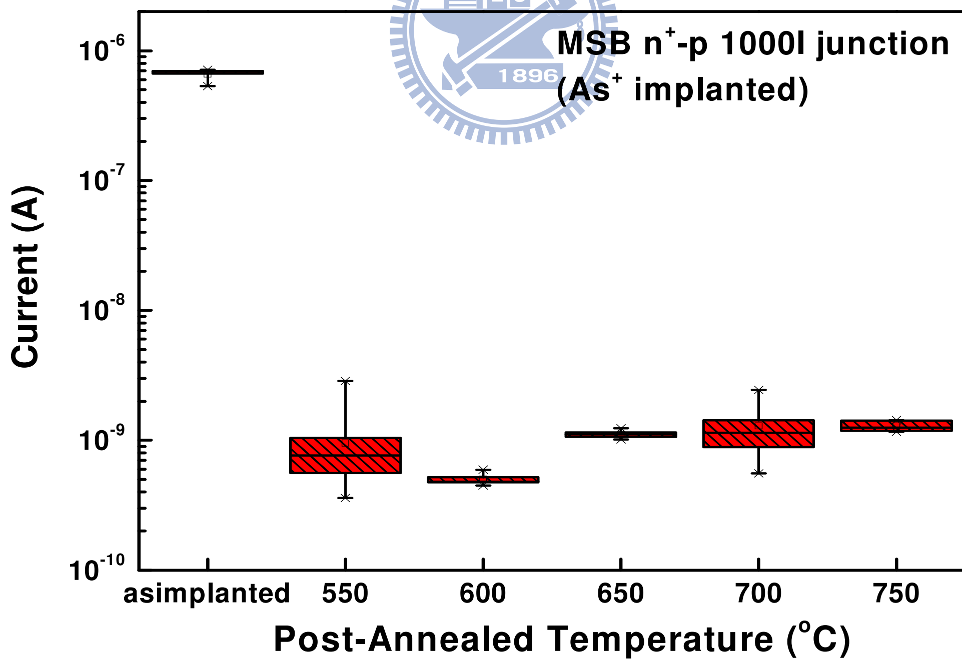



Fig.4-15 Band diagram of (a) Schottky and (b) MSB $p^+$-n junction at reverse biased.

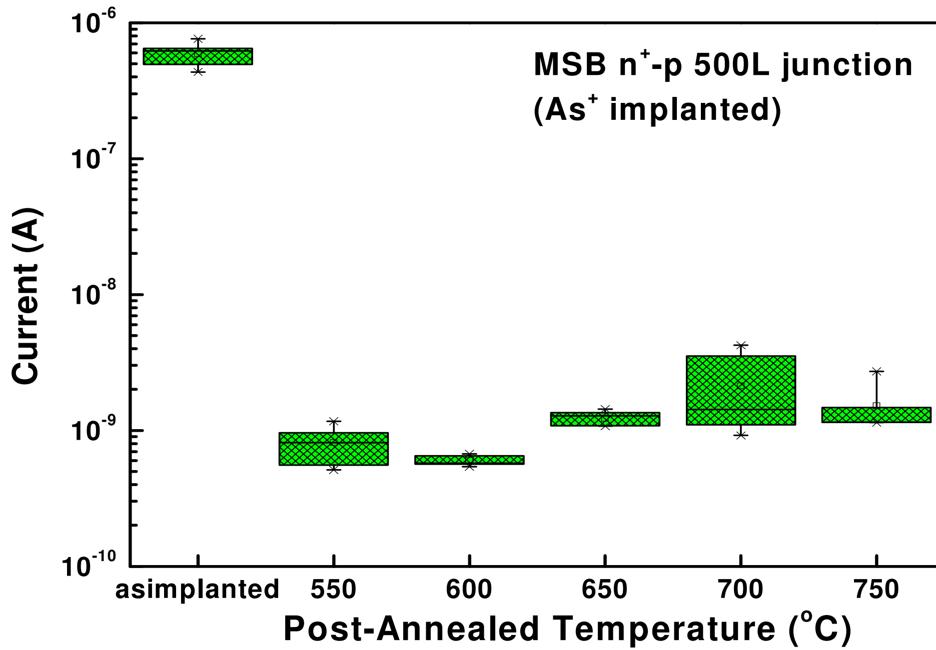



(a)

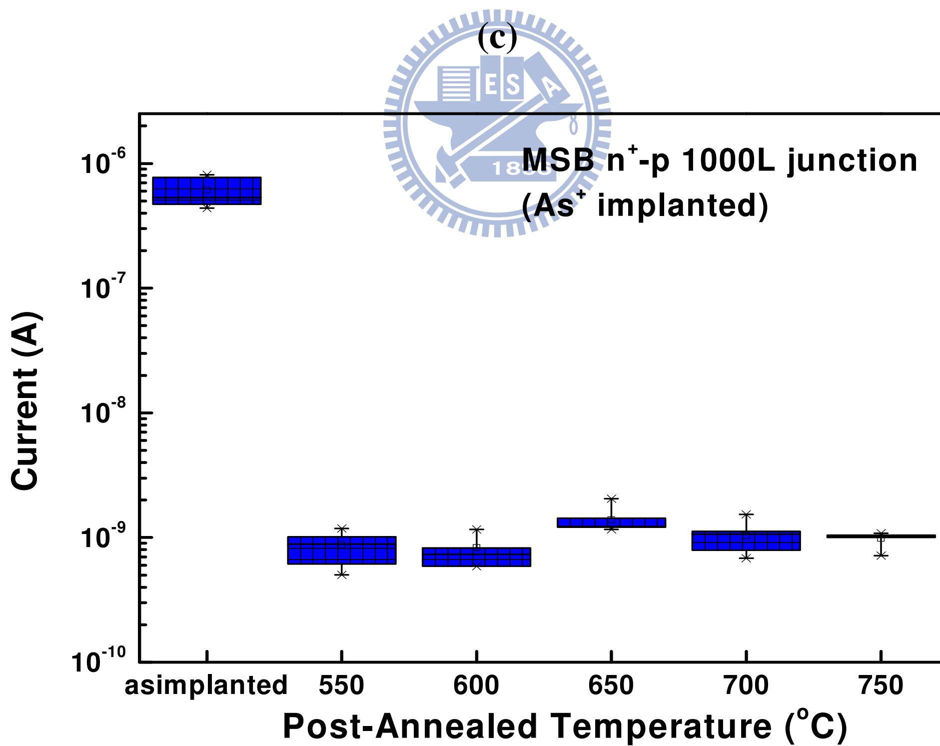



(b)

Fig.4-16 Reverse biased (3V) junction leakage current statistics of the (a) 500I and (b) 1000I type MSB $n^+$-p junctions with $As^+$ implantation.

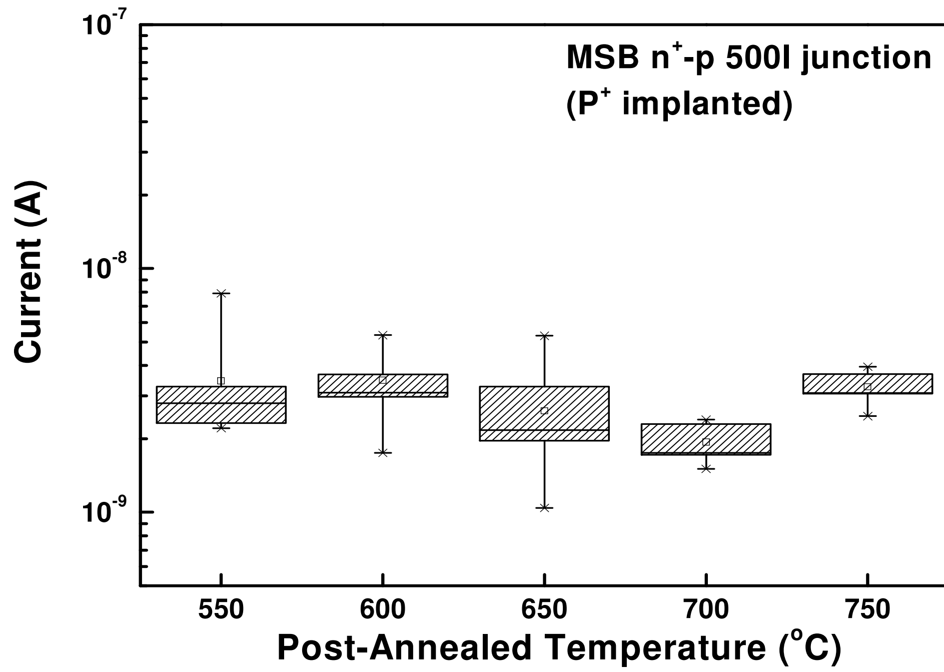



(c)

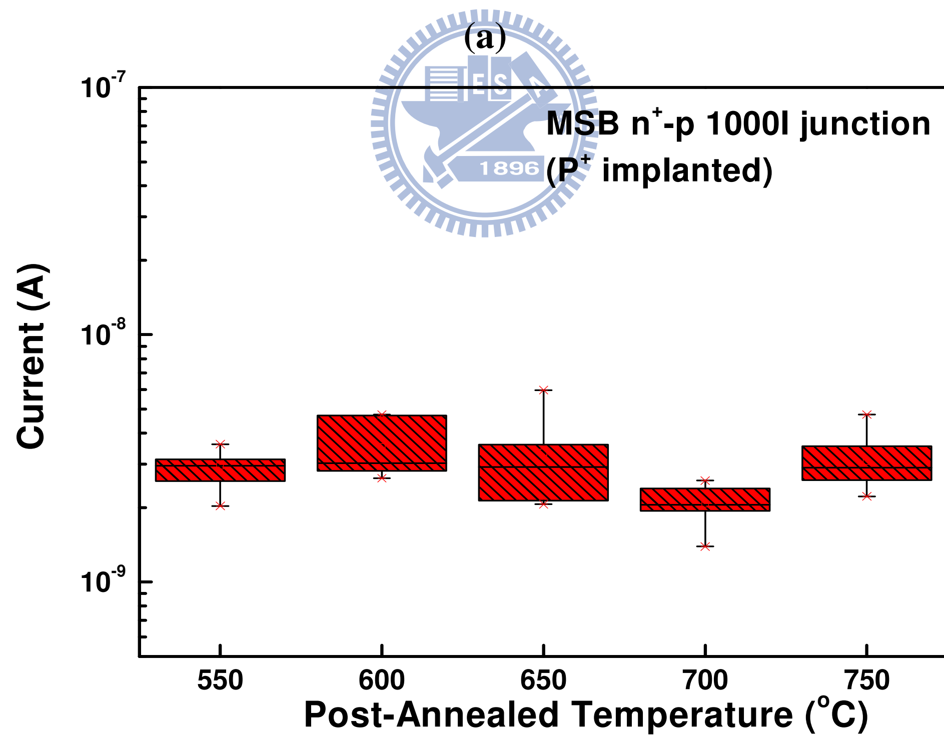



(d)

Fig.4-16 Reverse biased (3V) junction leakage current statistics of the (c) 500L and (d) 1000L type MSB $n^+$-p junctions with $As^+$ implantation.

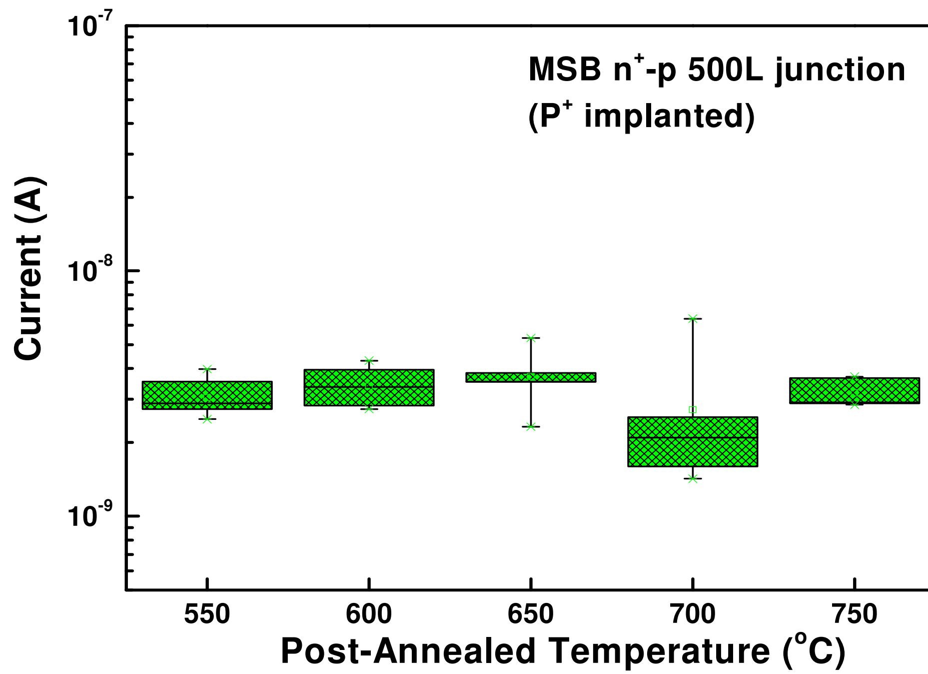



(a)




(b)

Fig.4-17 Reverse biased (3V) junction leakage current statistics of the (a) 500I and (b) 1000I type MSB $n^+$-p junctions with $P^+$ implantation.

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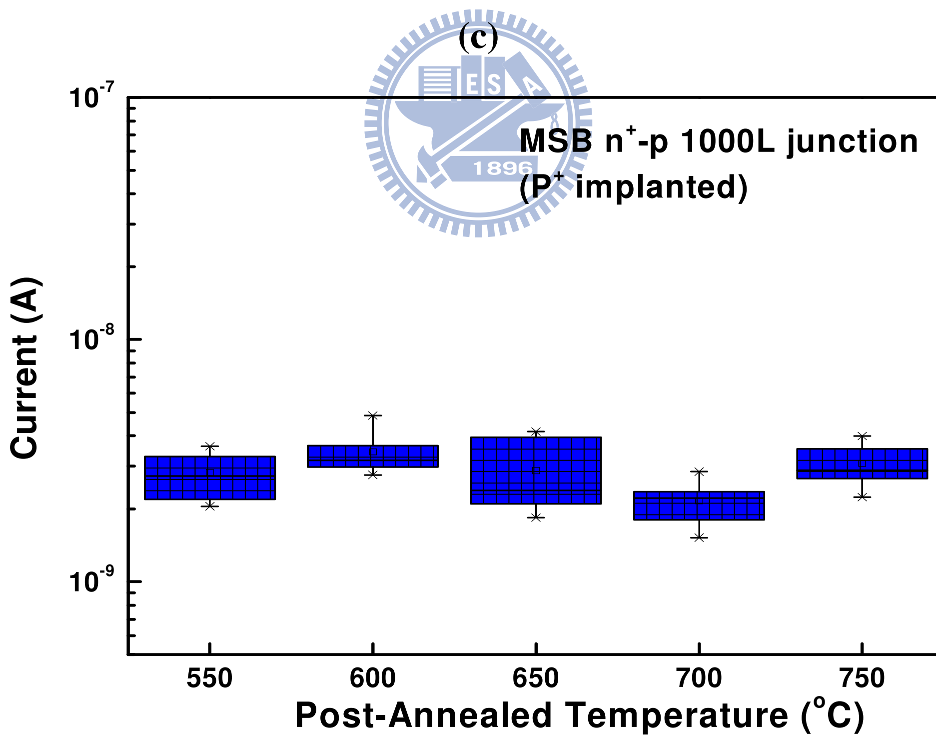
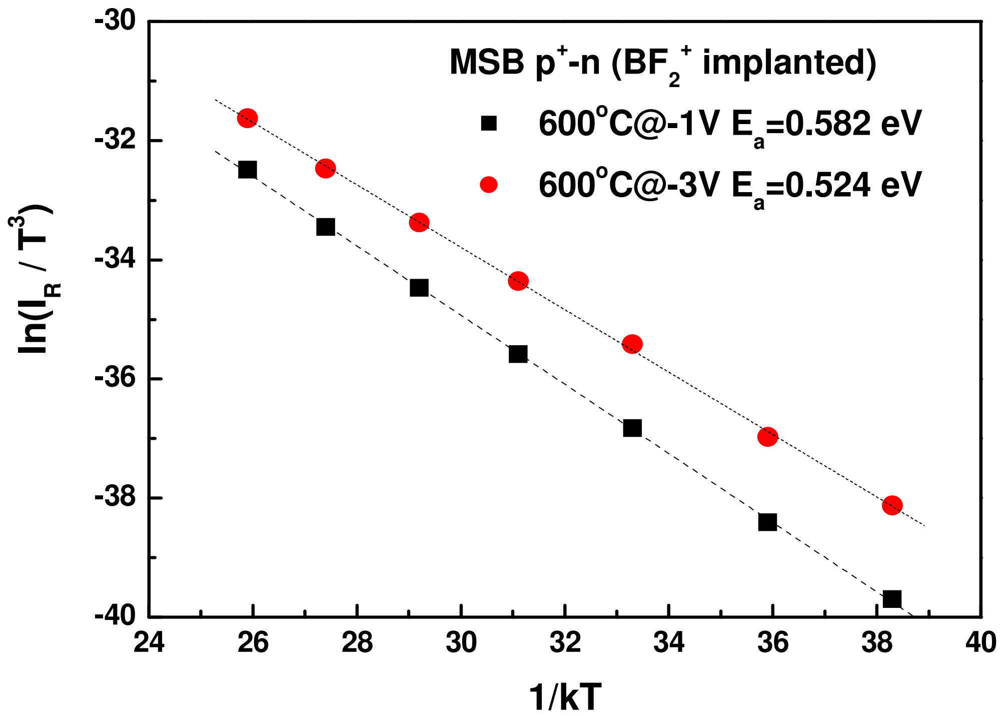
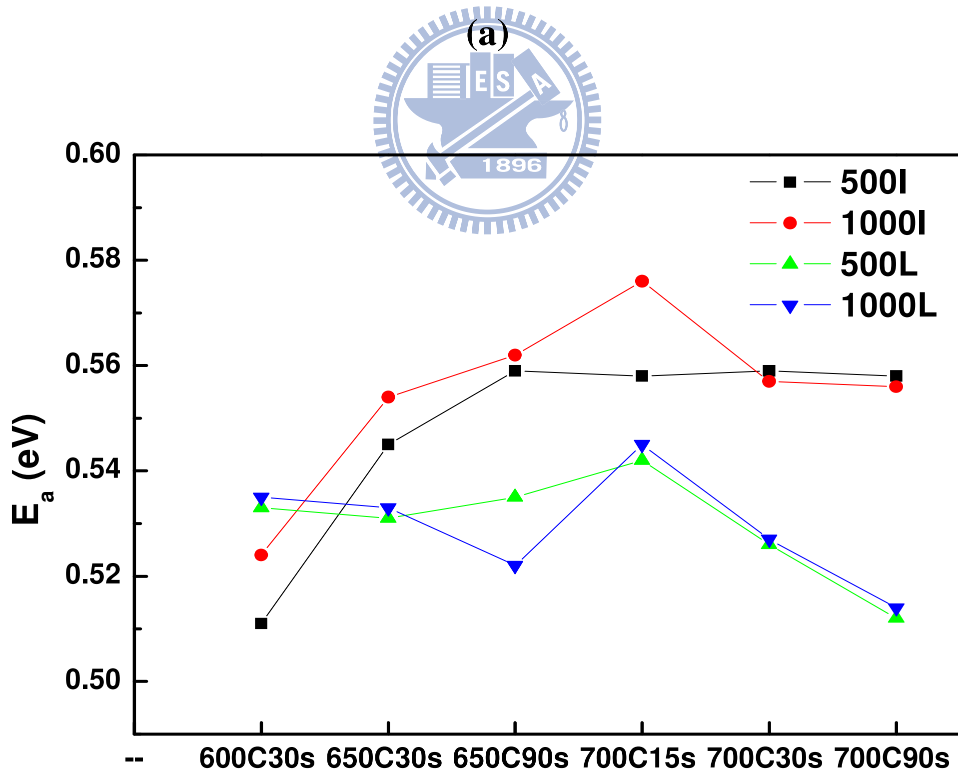



(d)

Fig.4-17 Reverse biased (3V) junction leakage current statistics of the (c) 500L and (d) 1000L type MSB $n^+$-p junctions with $P^+$ implantation.

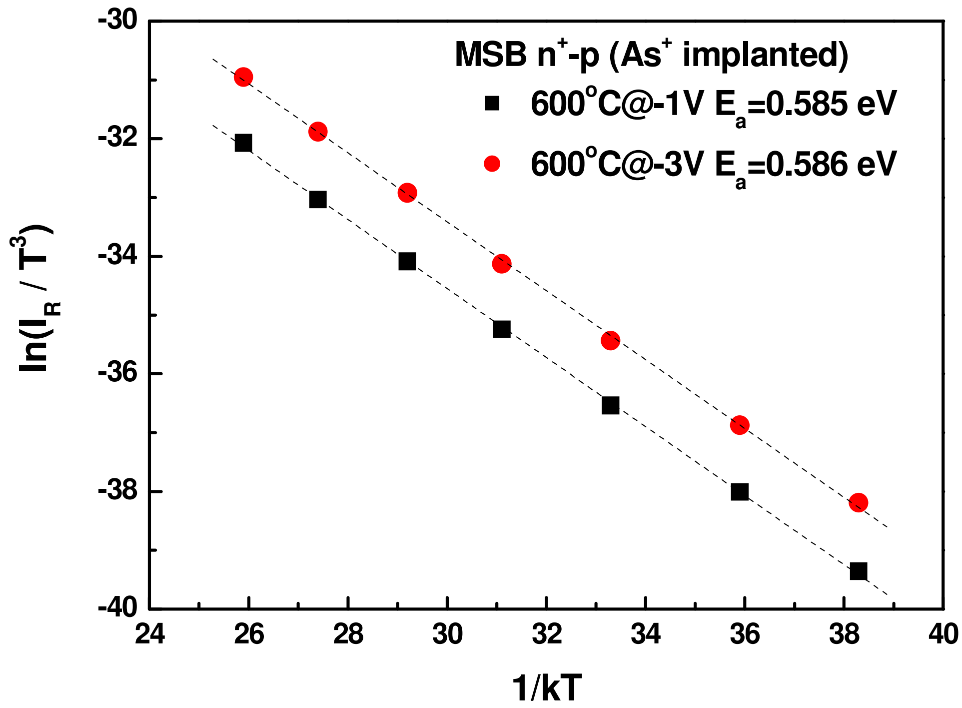



(a)

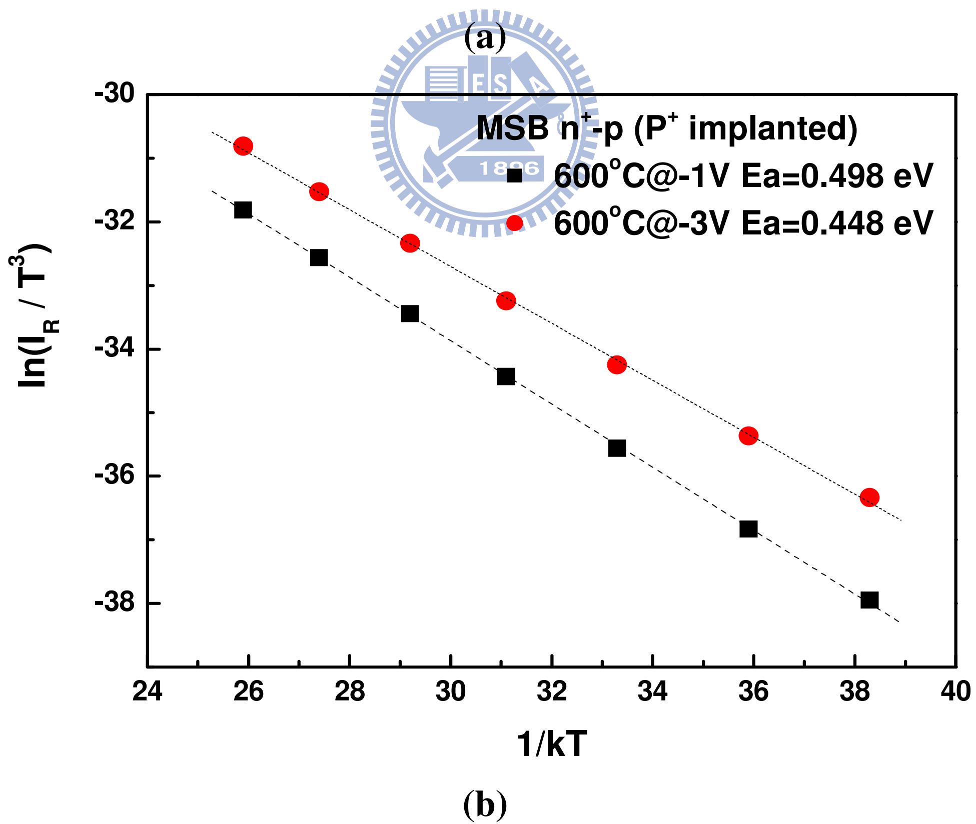



(b)

Fig.4-18 (a) Activation energy of 600 °C annealed 1000I type junction, and (b) Summary of $E_a$ in different post-annealed conditions of MSB $p^+$-n junctions.




(a)




(b)

Fig.4-19 Activation energy of 600 °C annealed MSB $n^+$-p 1000I junction (a) with $P^+$ implantation and (b) with $As^+$ implantation.

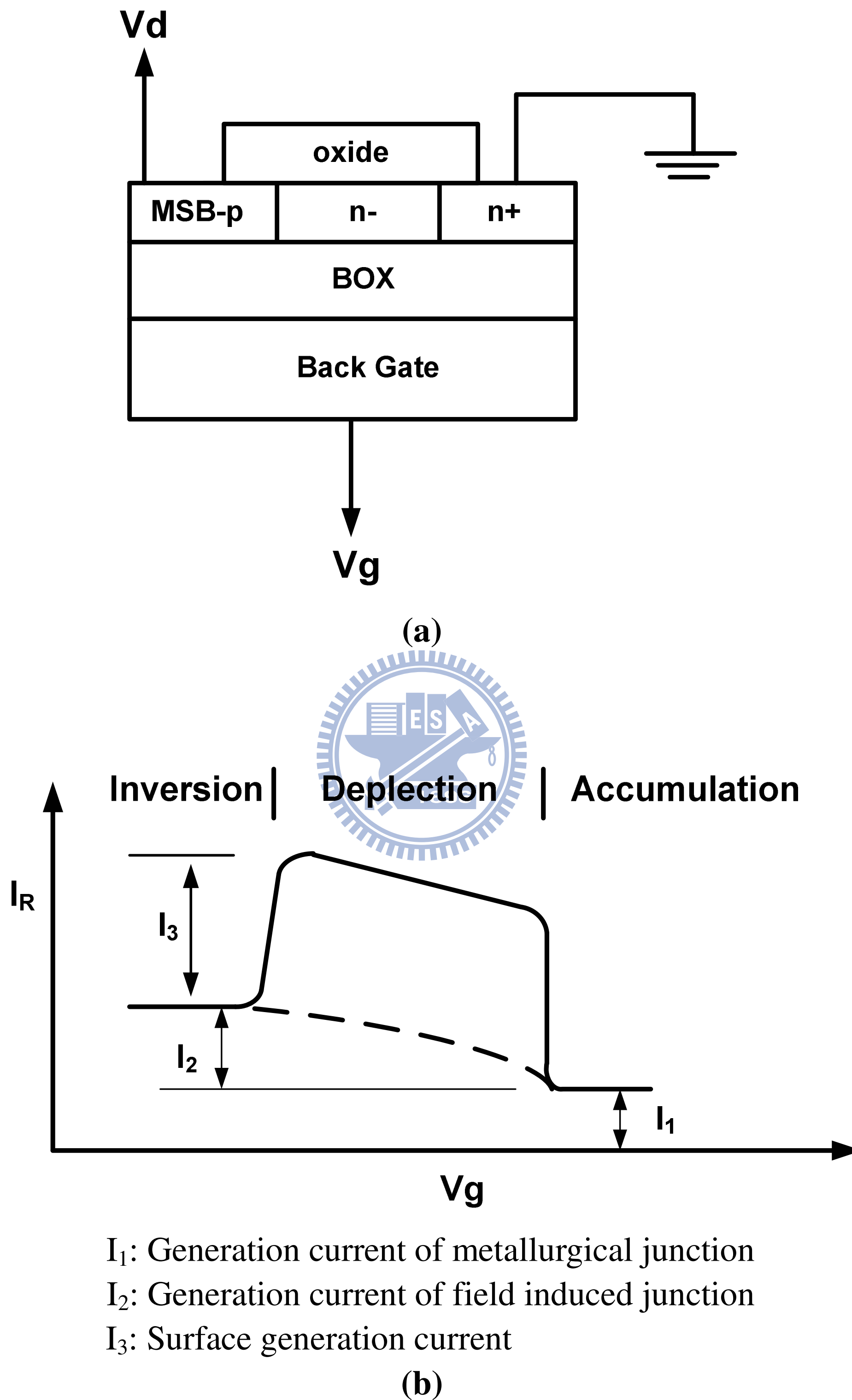
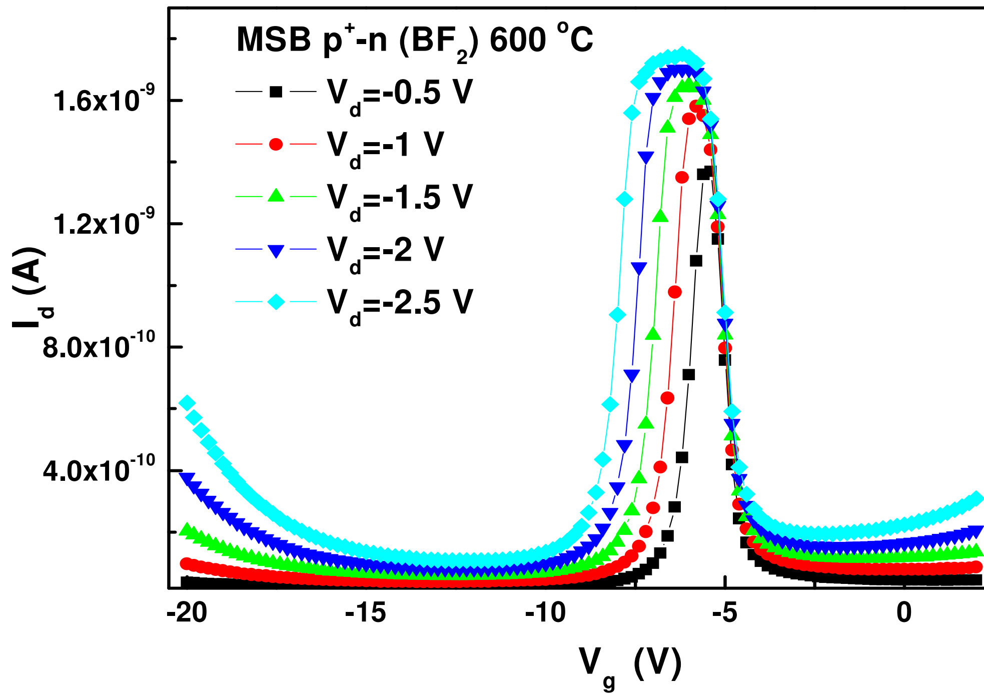
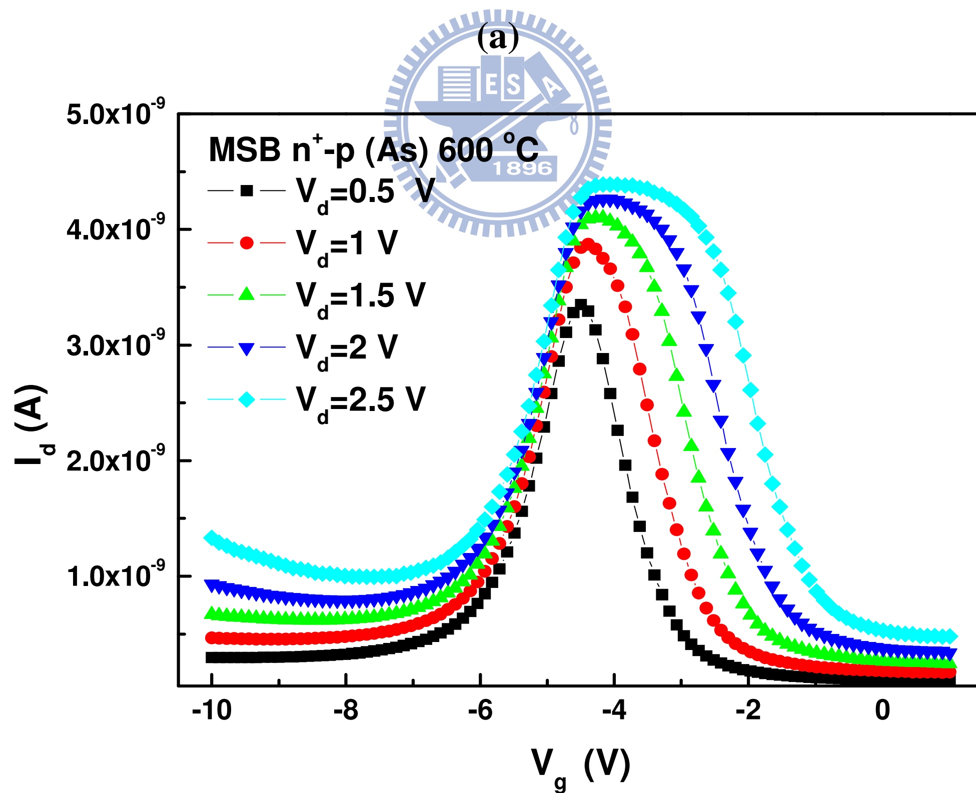



Fig.4-20 Schematic diagrams of gated-diode method (a) was the measurement setup diagram and (b) was the measured I-V characteristic.




(a)




(b)

Fig.4-21 Gated-diode I-V characteristics of MSB (a) $p^+$-n and (b) $n^+$-p for 1000I type 600 $^o$C annealed junction.

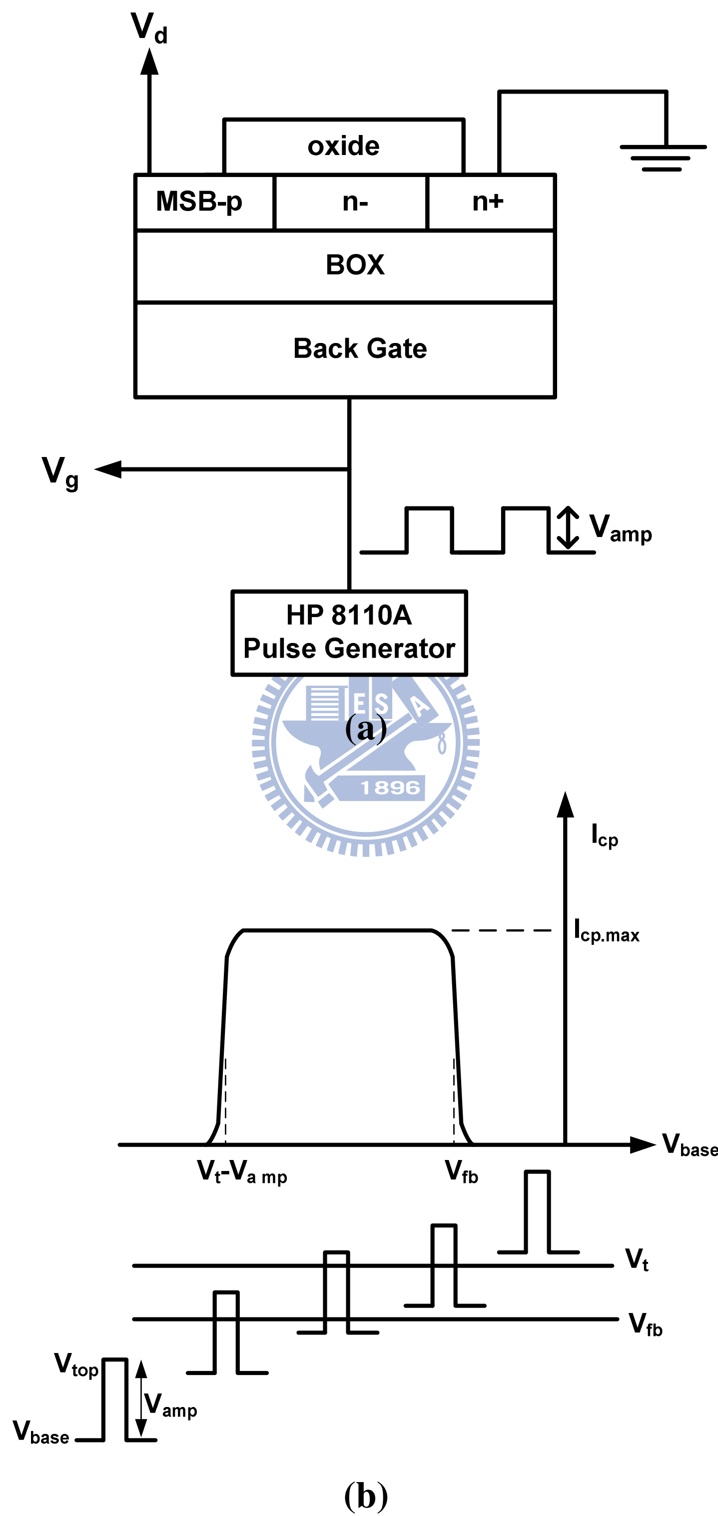



Fig.4-22 (a) measurement schematic diagram and (b) band diagram vs I-V characteristics of charge pumping method.

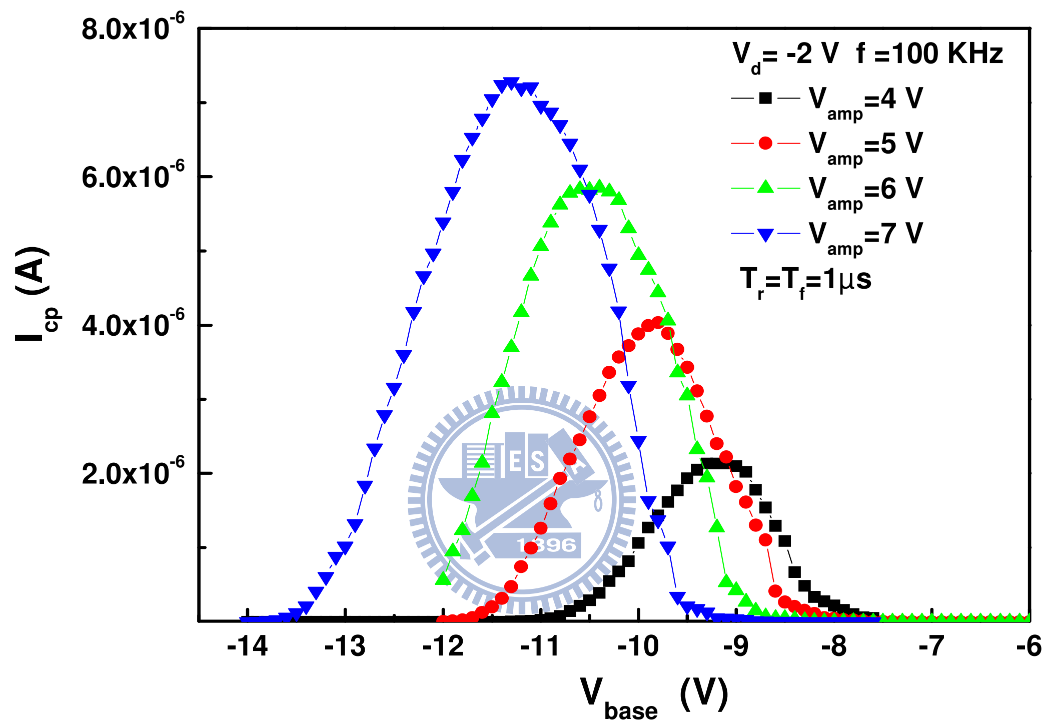
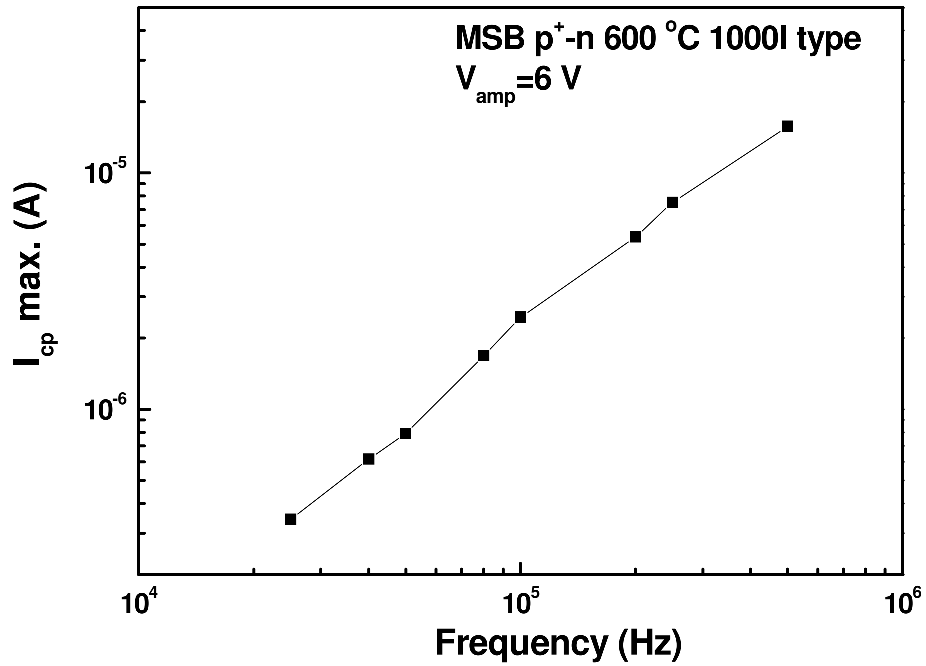
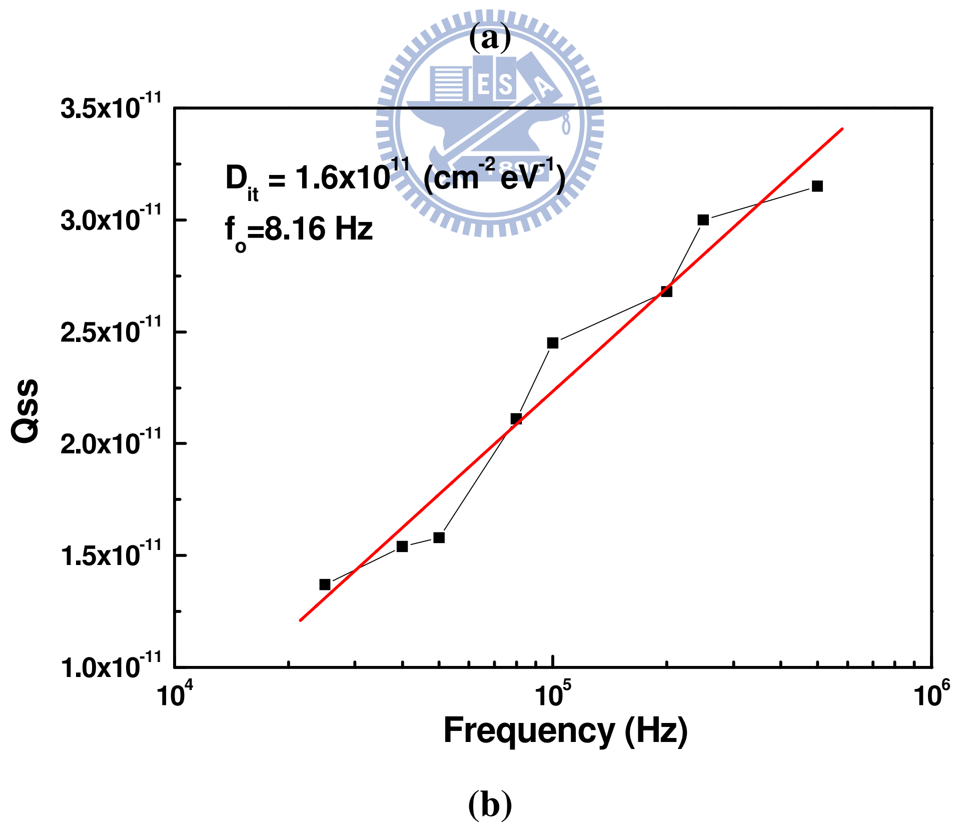



Fig.4-23 Charge pumping method measured $I_{cp}$ versus $V_{base}$ result.




(a)




(b)

Fig.4-24 (a) $I_{cp}$max. versus Frequency Plot and (b) $Q_{ss}$ versus ln(*f*) Plot.

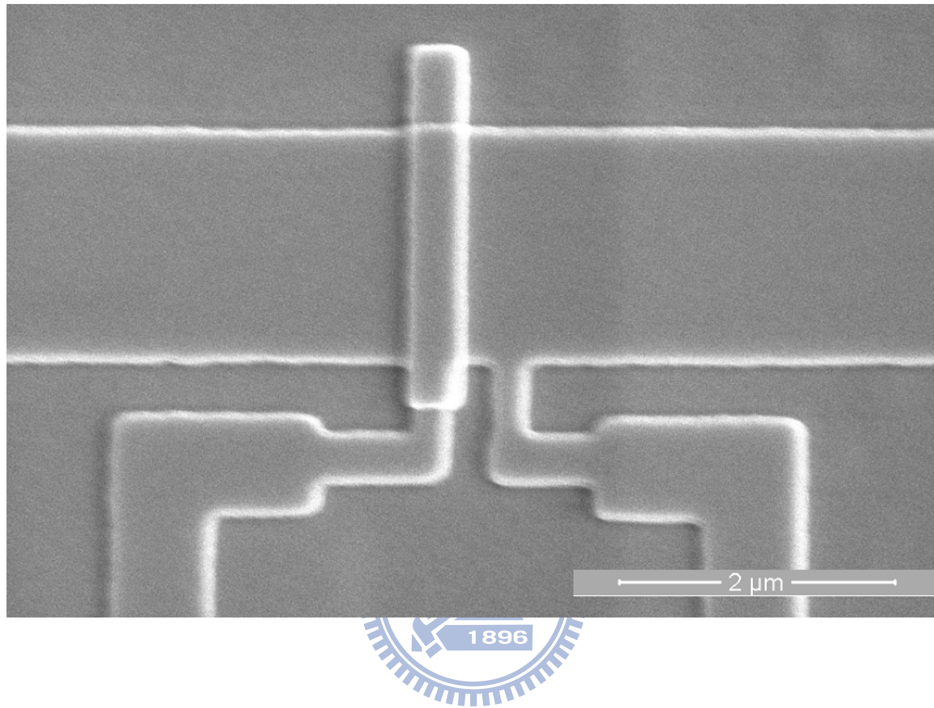



Fig.4-25 Fabricated lateral CBKR structure on SOI.

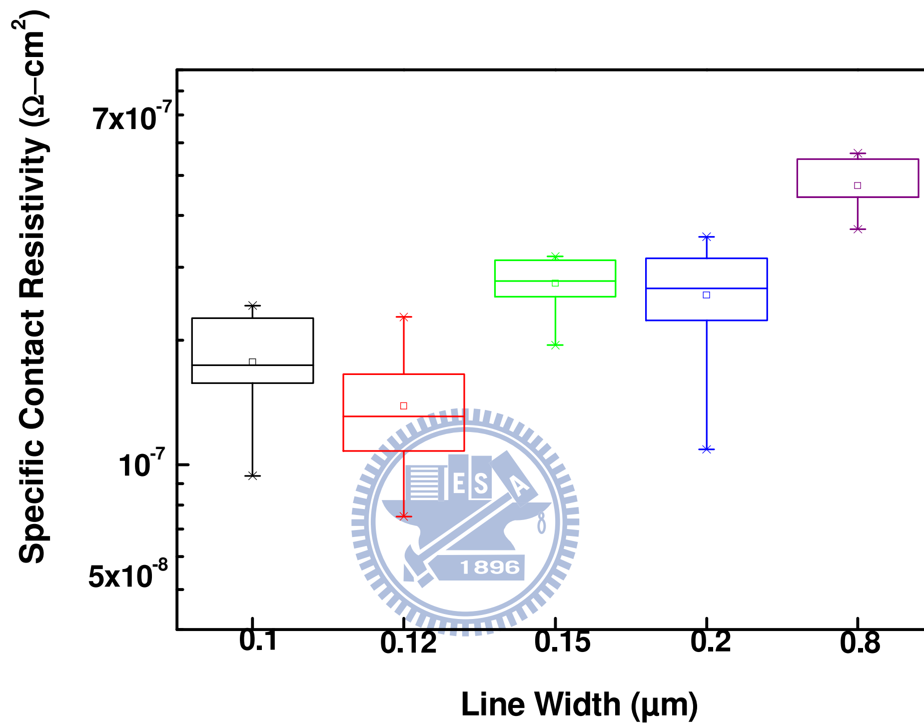



Fig.4-26 Measured specific contact resistivity values of $n^+$ MSB contact.

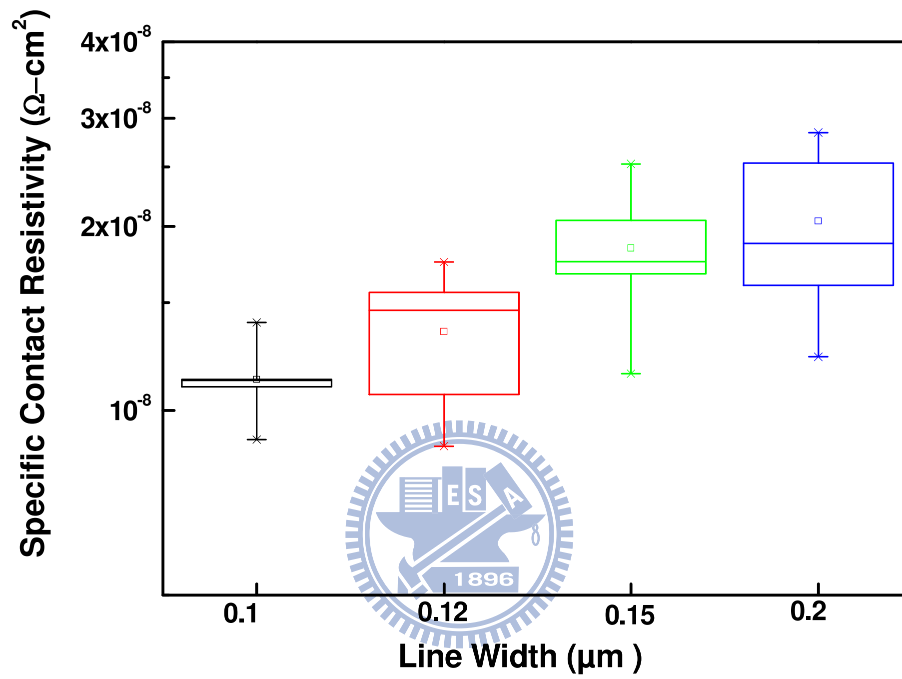



Fig.4-27 Measured specific contact resistivity values of $p^+$ MSB contact.

# Chapter 5
# Carrier Concentration Profiling of P-N Junction by Kelvin-Probe Force Microscopy

## 5-1 Introduction

As the CMOS devices scale down to the nano-regime, the measurement of two-dimensional (2-D) carrier/dopant distribution becomes more and more important in order to simulate and model device performance precisely. However, the typical spreading resistance profiling (SRP) technique and secondary ion mass spectroscopy (SIMS) measure one-dimensional (1-D) junction depth profiles. Although some special SIMS techniques have been proposed to measure 2-D depth profiles, the spatial resolution is destructive and not sufficient [1,2]. Therefore, 2-D carrier/dopant distribution for traditional device modeling is estimated first from a 1-D depth profile done by SIMS analysis, and then technology computer aided design (TCAD) tools have been used to simulate device characteristics while adjusting the 2-D dopant distribution until the measured device characteristics are well fitted. Since the adjusted 2-D dopant distribution may be not the actual distribution, the error between the actual and the adjusted dopant distributions makes device modeling more and more difficult as devices scale down into the nano-regime.The scanning probe microscopy was invented in 1982; G. Binnig and H. Rohrer etc. invented the scanning tunneling microscopy (STM) which can directly detect the atomic surface images first. The atomic force microscopy (AFM) technique was improved to measure the van der Waals force between tip and non-conductive sample's surface by G. Binnig, and C. F. Quate, *et al.* [3,4]. Scanning capacitance microscopy (SCM) [5-11], scanning spreading resistance microscopy (SSRM) [12-14] and Kelvin-probe force microscopy (KPFM) [15-17] are the major reported modes of

for 2-D carrier/dopant distribution measurements. They are non-destructive techniques with high spatial resolution. For SCM, the accuracy often depends on many undetermined parameters and complex calculations. A uniform and high quality dielectric on the sample surface is required for SCM; however, the derivative of dC/dV also generates noise during data manipulation. The SSRM cannot rapidly follow the steep spatial changes of majority carrier distribution at p-n junction interface, and the tips wear fast in β-tin operation region.

The KPFM is a surface potential measurement technique for conductive samples, and the theoretical principle behind it has been well derived [15,17]. However, the sample's surface potential is very sensitive to surface charges and to adsorb the molecules. The most common method in KPFM is to use a high vacuum chamber, smaller conductive tips, and in-situ heating to reduce any external influence on surface potential [19-21]. The spatial resolution of KPFM is influenced by the tip diameter as well as the signal response speed. The tip diameter could be reduced greatly by attaching a carbon nanotube (CNT) to the end of a conventional tip. The signal response time could be improved by adding an external feedback control circuit. In this chapter, the basic theory of KPFM is briefly introduced. The system setup and the effect of a feedback control circuit on the signal response speed are described. Several surface treatment methods were studied to obtain stable and high contrast surface potential images. The correlation between surface potential difference of a p-n junction ($\Delta\phi_{pn}$) and carrier/dopant concentration has been established for the first time. Finally, the cross-sectional depth profiling of a p-n junction and the detection of p-n junction array have been successfully demonstrated.

## 5-2 Operating Principle and System Setup

KPFM is known as a surface potential microscopy based on non-contacting mode AFM. The purpose of KPFM is to measure the potential offset between a probe tip and sample

surface. Fig.5-1 shows a block diagram of the high vacuum KPFM system (Seiko Instruments SPA300HV) used in this work. The vacuum in this system can be better than $1 \times 10^{-6}$ Torr. The cantilever we used is a PtIr coated silicon tip with a typical tip radius of ~20 nm. The force constant and resonant frequency of tip are about 1.5 N/m and 60 kHz, respectively. By using a dual-modulation scheme (with both mechanical and electrical modulations) at two non-interfering modulation frequencies, AFM topographic and KPFM surface potential images can be obtained simultaneously. The vibration frequency of the tip ($\omega_1$) was chosen to be slightly lower than the resonant frequency of the tip (60 kHz) and the typical vibration amplitude was about 100 mV. We use the tapping mode for measurement, which reduces damage to the tips. The appropriate ac modulation voltage ($V_{ac}$) and frequency ($\omega_2$=20~80 kHz) were chosen based on the response between the sample and the tip. Therefore, an additional feedback control circuit was inserted to improve the response speed.

Equation (5.1) expresses the total force experienced by the tip in a KPFM system.

$$\begin{aligned} F_t &= F_a + F_c + F_e \\ &= F_a + \frac{1}{2}\frac{\partial C}{\partial z}V^2 - \frac{q_{tip}q_e}{4\pi\varepsilon z^2} \\ &= F_a + \frac{1}{2}\frac{\partial C}{\partial z}(V_{dc}-V_s)^2 + \frac{\partial C}{\partial z}\frac{V_{ac}^{\ 2}}{4} + \frac{q_e^{\ 2}}{4\pi\varepsilon z^2} + \frac{q_e C(V_{dc}-V_s)}{4\pi\varepsilon z^2} \\ &\quad + \left[\frac{\partial C}{\partial z}(V_{dc}-V_s) + \frac{q_e C}{4\pi\varepsilon z^2}\right]\cdot V_{ac}\sin\omega_2 t - \frac{\partial C}{\partial z}\frac{V_{ac}^{\ 2}}{4}\cos(2\omega_2 t) \end{aligned} \quad ....(5.1)$$

The total force ($F_t$) is composed of the van der Waals force ($F_a$), capacitance force ($F_c$), and coulomb electrostatic force ($F_e$) [9,15,16,20]. where C is the tip-sample capacitance, which is a function of their separation distance z, $q_{tip}$ is the total charge on the tip, $q_e$ is the charge on sample surface, ε is the effective permittivity between the tip charge and surface charge, $V_{dc}$ is the dc potential difference between tip and sample, $V_{ac}$ is the amplitude of the ac modulation signal with frequency $\omega_2$, and $2\omega_2$ is the second harmonic frequency. A lock-in amplifier is used to lock the signal $\omega_2$ and determine its amplitude. If the surface charge ($q_e$) is zero, we

can calculate $V_{dc}$-$V_s$. Finally, we can determine $V_{dc}=V_s$=surface potential using the crossing feedback control circuit.

A map of the dc potential versus the lateral position coordinate produces an image of the work function of the surface. The work function relates to many surface phenomena, including catalytic activity, reconstruction of surfaces, doping and band-bending of semiconductors, charge trapping in dielectrics, and corrosion. The map of the work function produced by KPFM gives information about the composition and electronic state of the local structures on the surface of a solid. Fig5-2 illustrates a p-n junction that is measured by KPFM. Theoretically, the measured results of p-type and n-type regions by KPFM should be the work function difference between the tip and the Si surface. As shown in Fig.5-2(b), we can obtain the surface potential ($\phi_m$-$\phi_n$) on n-type region and ($\phi_m$-$\phi_p$) on a p-type region, where $\phi_m$ is the work function of tip, $\phi$n is the work function of the n-type region, and $\phi_p$ is the work function of the p-type region. Their potential difference, $\phi_p$-$\phi_n$, is the same as the built-in voltage $\phi_b$ if there is no surface charge on the sample [10].The feedback control circuit dominates the spatial resolution of the potential image because the response of the feedback circuit must be faster than the speed of data sampling. In order to have more data points, i.e. better resolution, over the same scanning area, the feedback circuit must respond faster. Using a built-in circuit, a scanning tail is clearly observed, and the shape of the junction is different when scanned in different directions, as shown in Fig.5-3. Due to the signal delay, a large horizontal shift between the two surface potential profiles scanned in different directions is observed. To solve this problem, a new feedback control circuit was implemented to replace the built-in circuit, as shown in Fig.5-4. Fig.5-5 shows the surface potential of a planar p-n junction detected by KPFM with a built-in feedback control circuit. As we see, the potential image and scanning response are improved.

## 5-3 Experimental Procedures

The starting material was a (100) oriented 4-inch Si wafer. The n-type wafers were phosphorous-doped and the p-type wafers were boron-doped. The doping concentration determined by the SRP technique is $5 \times 10^{14}$ $cm^{-3}$ for a p-type wafer and $2 \times 10^{15}$ $cm^{-3}$ for an n-type wafer.

Two sets of samples were prepared. In the first sample set, periodic $n^+$-p and $p^+$-n junctions with different doping concentrations were fabricated in order to establish a correlation between surface potential difference and carrier/dopant concentration difference. After the typical RCA cleaning, the $n^+$ and $p^+$ regions were defined by lithography. $As^+$ ions and $BF_2^+$ ions were implanted to form $n^+$ and $p^+$ junctions, respectively, at a dose level of $1 \times 10^{13}$, $5 \times 10^{13}$, $1 \times 10^{14}$, $2 \times 10^{14}$, $1 \times 10^{15}$, $2 \times 10^{15}$, and $5 \times 10^{15}$ $cm^{-2}$. The implantation energies for $As^+$ and $BF_2^+$ were both 20KeV. After ion implantation, a 200-nm thick $SiO_2$ film was deposited on the wafer surface in a plasma enhanced chemical vapor deposition (PECVD) system to prevent the dopant from diffusing out during the thermal activation at 950 ºC for 30 min. The capping $SiO_2$ layer was removed by dilute HF (DHF) solution, and different surface treatments were performed on the samples with $As^+$ ion implantation at a dose of $5 \times 10^{15}$ $cm^{-2}$ before KPFM measurement to determine the most suitable surface preparation method. Table 5-1 summarizes the sample ID and the surface treatment methods.

The second sample set has the $n^+$-n and $p^+$-p high-low junction structure. These samples were used to determine the surface concentration by conventional methods. The $n^+$ and $p^+$ doping conditions are identical to those used for the first sample set. The surface concentrations of samples with lower implantation doses were determined by the

capacitance-voltage (C-V) method [23-25] and SIMS [26] while the surface concentrations of samples with higher implantation doses were determined by SRP [27-28].

For C-V measurement, a 48-nm thick $SiO_2$ layer was deposited on the sample surface in a PECVD system at 350 ℃. An Al gate electrode was deposited in a thermal evaporation system and patterned by lithography and wet etching. The process temperatures were low enough so that dopant redistribution can be ignored. Because of the limitation of the Debye length ($L_D$), the concentration at the first $3L_D$ is not valid [24]. For highly concentrated samples, the $L_D$ should be replaced by the Thomas-Fermi length ($L_{TF}$) due to quantum effects, and then the resultant concentration becomes more plausible [24]. The SRP measurements were performed at two different laboratories: the Nano Facility Center of the National Chiao-Tung University and Episil Technology. Both sites used the SSM 150 spreading resistance system. The systems were calibrated with standard Si calibration kits before measurement. The SIMS analyses were performed at three different sites: Cameca IMS-4F in NTHU, Cameca IMS-5F in NDL, and Cameca IMS-6F in MA-tek. The primary ions were $Cs^+$ for As depth profiling and $O_2^+$ for B depth profiling. The SIMS counts over the first 10 nm are unstable so that the concentrations 20 nm deep were treated as the surface concentration. Furthermore, SIMS detects dopants but not carriers so that the measured dopant concentration is higher than the actual carrier concentration.

Since it is the carrier concentration which determines the surface potential, we adopt the C-V and the SIMS data for the three lower-implantation-dose samples and the SRP data for

the three higher-implantation-dose samples. Therefore, we use 'carrier' instead of 'dopant' in the following sections.

## 5-4 Results and Discussion

### 5-4-1 Effects of surface treatment

Figs.5-6(a) ~ (d) shows the measured surface potential images of samples A to D, respectively. The KPFM measurement parameters are: $\omega_2$= 34~38 kHz, $V_{ac}$= 1.1~1.5 V, and scanning speed ~ 0.05 Hz. It is clear that sample A shows the best potential image contrast and sample B shows the worst contrast. An X-ray photoelectron spectrometer (XPS) was used to analyze the surface condition of samples after different surface treatments. Fig.5-7 shows the F 1s binding energy of samples A and B. The peaks at 686 and 689.9 eV observed for sample B are the binding energy of Si-F and H-F, respectively. No F 1s signal was observed for sample A. Fig.5-8 shows the O 1s binding energies of samples A and B. The strong O-H peak in sample A suggests that Si-OH bonds substitute for the Si-F bonds after rinsing with deionized water (DI) water [29-30]. The reaction can be expressed as Si-F+$H_2O$ -> Si-OH + HF. Sample B also exhibits an O-H bond, but the intensity is much weaker than that of sample A. Only Si-O bonds were detected on samples C and D, so that the data is not shown.

According to XPS analyses, it is clear that as the sample surface becomes covered by Si-O or Si-F bonds, the contrast in the surface potential image is degraded [29,31], because the Si-F bond increases the surface charge ($q_e$) and has a larger dipole moment. The Si-O bond isolates the Si surface and increases the capacitance (C) between surface and tip. As shown in eq.(5.1), $q_e$ and C are included in the amplitude of the $\omega_2$ signal. With non-zero $q_e$ and large C value, the term $V_{dc}$-$V_s$ cannot be determined directly from the amplitude of $\omega_2$.

Therefore, the surface treatment procedure before KPFM measurement is determined to be dipping in DHF followed by rinsing with DI water. To remove possible organic contamination, a 10-min ultrasonic oscillation in acetone may be performed before DHF dipping.

### 5-4-2 Correlation between surface potential difference and surface carrier/dopant concentration

Fig.5-9 shows the measured surface potential image in 10x10μm$^2$ region, and the samples were implanted with $As^+$ or $BF_2^+$ at a dose of $5 \times 10^{15}$ or $2 \times 10^{14}$ cm$^{-2}$. The measured surface potential image in Fig.5-9(a) and Fig.5-9(c) shows the inverse profile because of opposite dopant type for Si. Theoretically, the measured surface potential difference between the p-region and n-region of a p-n junction should be equal to the build-in voltage ($\phi_b$), which is the Fermi-energy difference between n- and p-type Si. However, even if sample A shows the strongest image contrast, the measured surface potential difference ($\Delta\phi_{pn}$) between the n$^+$ region and the p-substrate is only 0.103 V, as shown in Fig.5-10, which is much lower than the theoretical build-in voltage of about 0.8 V. This discrepancy arises from the states existing on the sample surface. Equation (5.2) defines the situation:

$$\Delta\phi_{pn} = (\phi_p - \Delta\phi_p) - (\phi_n - \Delta\phi_n) = (\phi_p - \phi_n) - (\Delta\phi_p - \Delta\phi_n) < (\phi_p - \phi_n) = \phi_b \qquad ....(5.2)$$

where $\phi_p$ is the Fermi-level of the p-type Si region, $\phi_n$ is the Fermi-level of the n-type Si region, $\Delta\phi_p$ is the shift in the Fermi-level due to the surface states on the p-type Si region, and $\Delta\phi_n$ is the shift in the Fermi-level due to the surface states on n-type Si. The surface states should trap surface charge to maintain charge neutrality. Usually, the trapped charge is

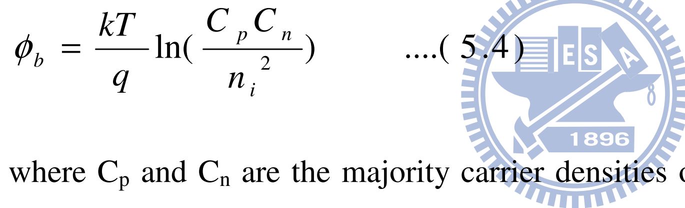
positive on a p-type silicon surface and therefore reduces the surface charge concentration and the Fermi level. The $\Delta\phi_p$ may be derived as equation (5.3) [28]:

$$C_p = N_V \exp\left(\frac{E_i - q\phi_p}{kT}\right) \propto \exp\left(-\frac{q\phi_p}{kT}\right)$$

$$=> \frac{dC_p}{d\phi_p} \propto -\exp\left(-\frac{q\phi_p}{kT}\right)$$

$$=> \Delta\phi_p \propto -\Delta C_p \cdot \exp\left(\frac{q\phi_p}{kT}\right) \qquad \ldots.(5.3)$$

where $C_p$ is the hole concentration in the p-type Si, $N_v$ is the energy state density of the valence band, and $E_i$ is the intrinsic Fermi energy. As the n-type Si concentration ($C_n$) is fixed, $\Delta\phi_{pn}$ should be a function of $e^{\phi_b}$; that is, $\phi_b$ is a function of $\ln(\Delta\phi_{pn})$. On the other hand the eqs. (4):



$$\phi_b = \frac{kT}{q}\ln\left(\frac{C_p C_n}{n_i^2}\right) \qquad \ldots.(5.4)$$

where $C_p$ and $C_n$ are the majority carrier densities of the p-type and n-type Si, respectively, and $n_i$ is the intrinsic carrier density. In the case of fixed $C_n$, $\phi_b$ would be proportional to $\ln C_p$. Therefore, we conclude that $\ln(\Delta\phi_{pn})$ should be correlated with $\ln C_p$.

Several methods including the C-V method, SRP, and SIMS were employed to determine the surface carrier concentration in order to setup an experimental correlation between $\Delta\phi_{pn}$ and $C_s$. Fig.5-11 and Fig.5-12 show the correlation between $C_s$ and $\Delta\phi_{pn}$. A very good linear relationship is observed in the full-log plot. It is postulated that the carrier concentration is an exponential function of the Fermi energy, while the Fermi energy of a free Si surface depends on the surface charge. The shift of Fermi energy due to surface charge is an exponential function of the carrier concentration so that the measured surface potential

difference is proportional to the surface concentration in the full-log plot. This result confirms the theoretical prediction. From Fig.5-11 and Fig.5-12, the empirical correlation between $C_s$ and $\Delta\phi_{pn}$ can be established by

$$\log(C_n) = 15.938 + 2.073\log(\Delta\phi_{pn}) \qquad \text{for } n^+\text{-p junction} \qquad \ldots(5.5)$$

$$\log(C_p) = 16.778 + 1.459\log(\Delta\phi_{pn}) \qquad \text{for } p^+\text{-n junction} \qquad \ldots(5.6)$$

### 5-4-3 Depth profiling of p-n junction and detection of junction array

On the basis of eq. (5.5) and (5.6), we can determine the depth profile of a p-n junction by measuring the surface potential. Figs.5-13(a) and 5-13(b) shows the surface potential image and the surface potential profile in the A-B direction of an Al-contacted $p^+$-n junction in the vertical direction after cleaving and polishing. The 500-nm-thick Aluminum layer was deposited to help to determine the position of the $p^+$ surface. Point A is the interface between the Aluminum and $p^+$ layer and was defined as the starting point of the junction surface.

Fig.5-14 shows the depth profiles measured by KPFM and SIMS. The peak concentration and junction depth measured by KPFM are consistent with those measured by SIMS. At the $p^+$ surface, the carrier concentration determined by KPFM is much lower than the dopant concentration measured by SIMS. We postulate that it was affected by either the Aluminum reference capping layer or the polishing defects at the Aluminum/Si interface; the defect charges make the KPFM measurement unstable in near surface region. The additional work is required to solve this in the future.

Fig.5-15 shows the surface image of $n^+$-p junction array with a pitch of 0.8 or 0.4 μm and an equal pattern/space. Clear contrast with the $\Delta\phi_{pn}$ image can be obtained by KPFM.

Fig.5-15(b) gets worse contrast image than Fig.5-15(a) is because of $As^+$ dopants were lateral diffused. So we also can prove that the resolution is enough to measure the profile in Fig.5-14 and surface is interfered with Aluminum.

## 5-5 Conclusions

A feedback controller circuit was fabricated to achieve higher response frequency and to improve the spatial resolution. The effect of surface treatment on the contrast of surface potential images was evaluated first. A simple surface treatment method, DHF dipping followed by DI water rinsing, was observed to provide a KPFM image with the highest contrast. The XPS analysis indicates that Si-OH bonds replace Si-F bonds after rinsing with DI water so that surface charge is minimized and a high-contrast KPFM image can be obtained.

A correlation between surface potential difference and carrier concentration was established. Several methods were employed to determine the surface carrier concentration of a series of samples with different dopant concentrations. They include C-V method, SRP, and SIMS. Experimental results confirm a linear correlation between surface carrier concentration and surface potential difference in a log-log plot. According to these correlations, carrier depth profiling by KPFM is has been achieved. Peak concentration and 0.5 µm junction depth are consistent with the dopant profile determined by SIMS analysis. A high resolution 2-D surface image of a p-n junction array with a pitch as small as 0.4 µm was also demonstrated.

These results indicate that KPFM is a very promising technique with which to obtain high resolution 2D carrier profiles of semiconductor devices.

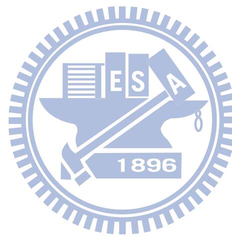


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Table 5-1 Surface treatment methods and samples IDs used in this work.

| | Sample ID | | | |
|---|---|---|---|---|
| Surface treatment | A | B | C | D |
| Rapid thermal oxidation 900°C, 1 min | | | V | |
| $H_2SO_4$ ： $H_2O_2$ =3:1, 100°C, 10 min | | | | V |
| ACE immersion 3~5 min | V | V | V | V |
| DHF (100:1) dipped~20 s | V | V | | |
| DI water rinse & $N_2$ purge | V | | V | V |

Fig.5-1 Block diagram of the KPFM with an external feedback control module used in this work.

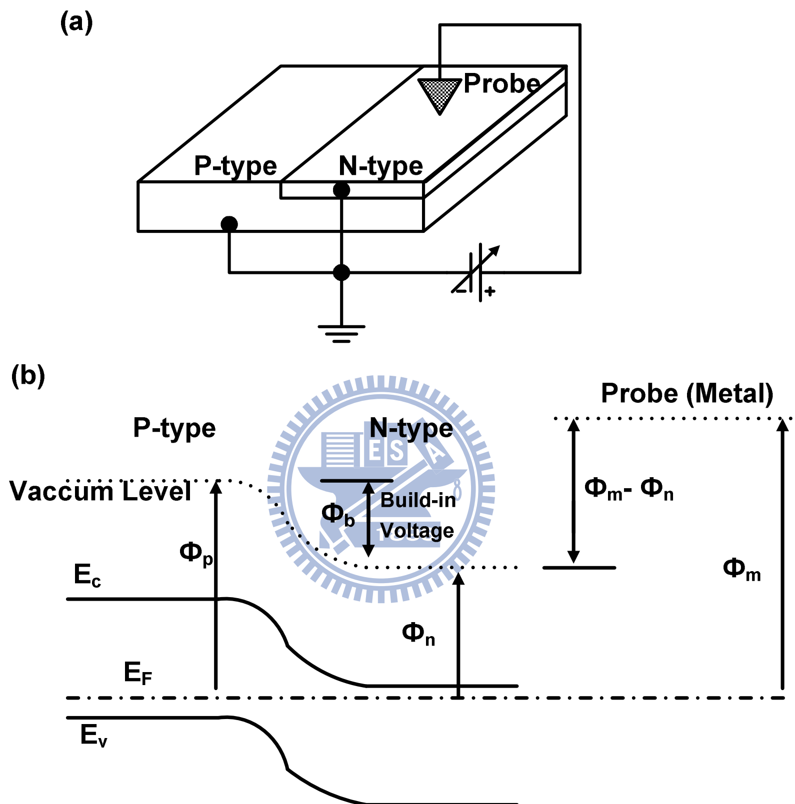



Fig.5-2 (a) Circuit and (b) Band diagram schematic drawing of a p-n junction measured by a KPFM system.

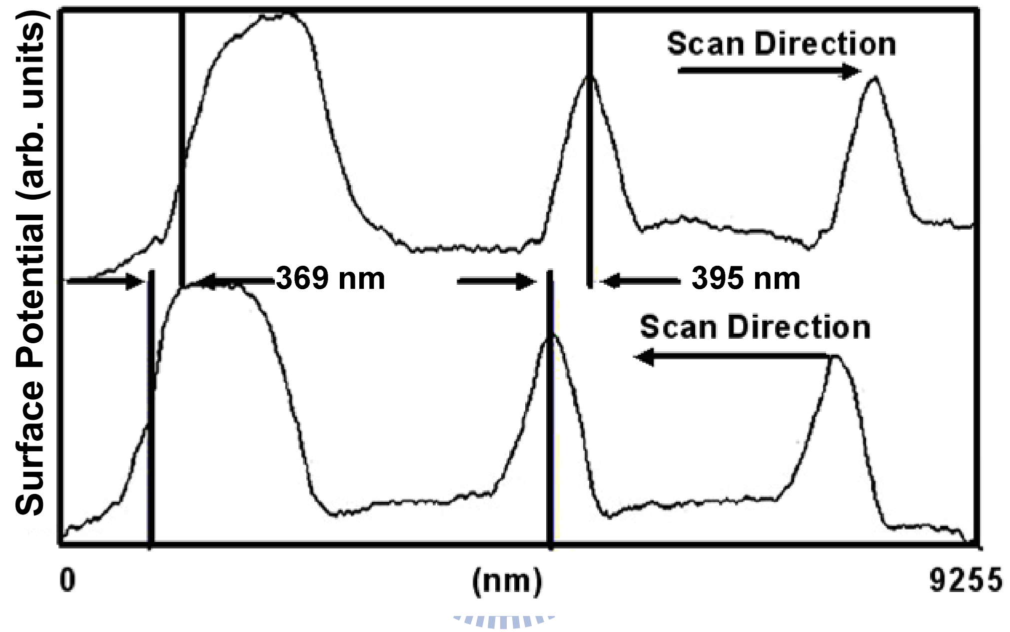



Fig.5-3 Surface potential image of a p-n junction measured by KPFM with a built-in feedback control circuit.

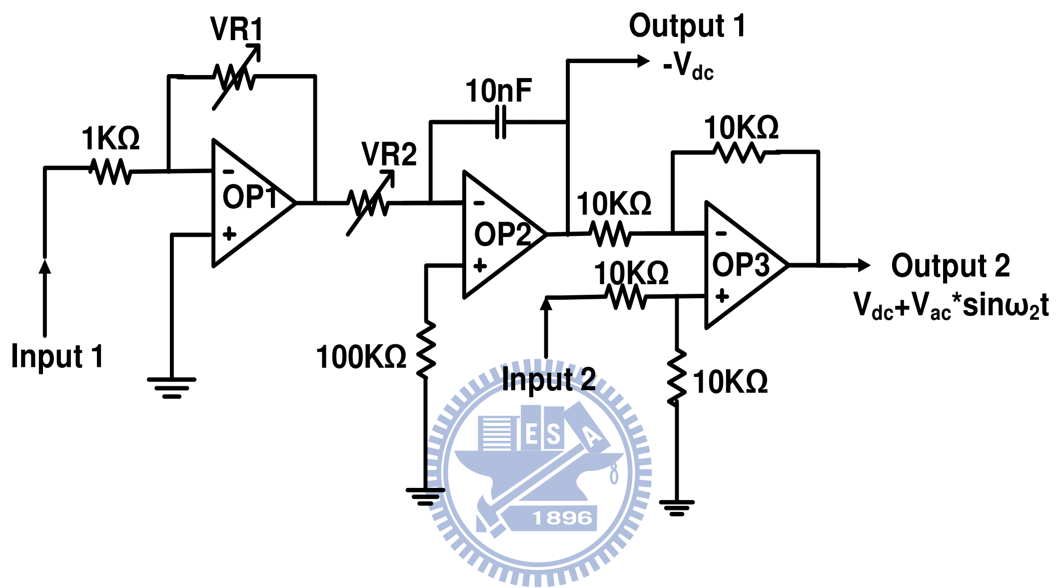



Fig.5-4 Block diagram of the external feedback control circuit.

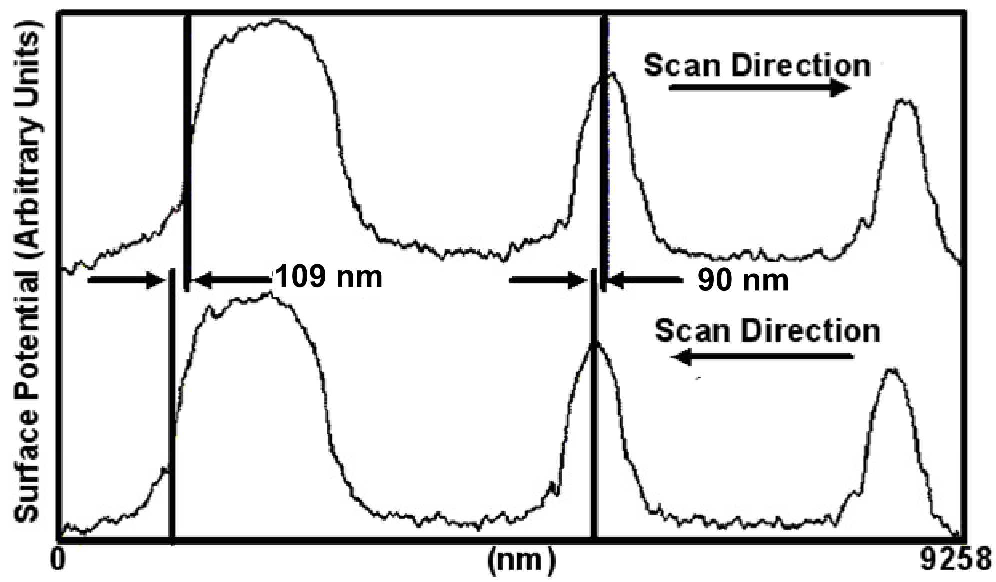



Fig.5-5 Surface potential image of a p-n junction measured by KPFM with an external feedback control circuit.

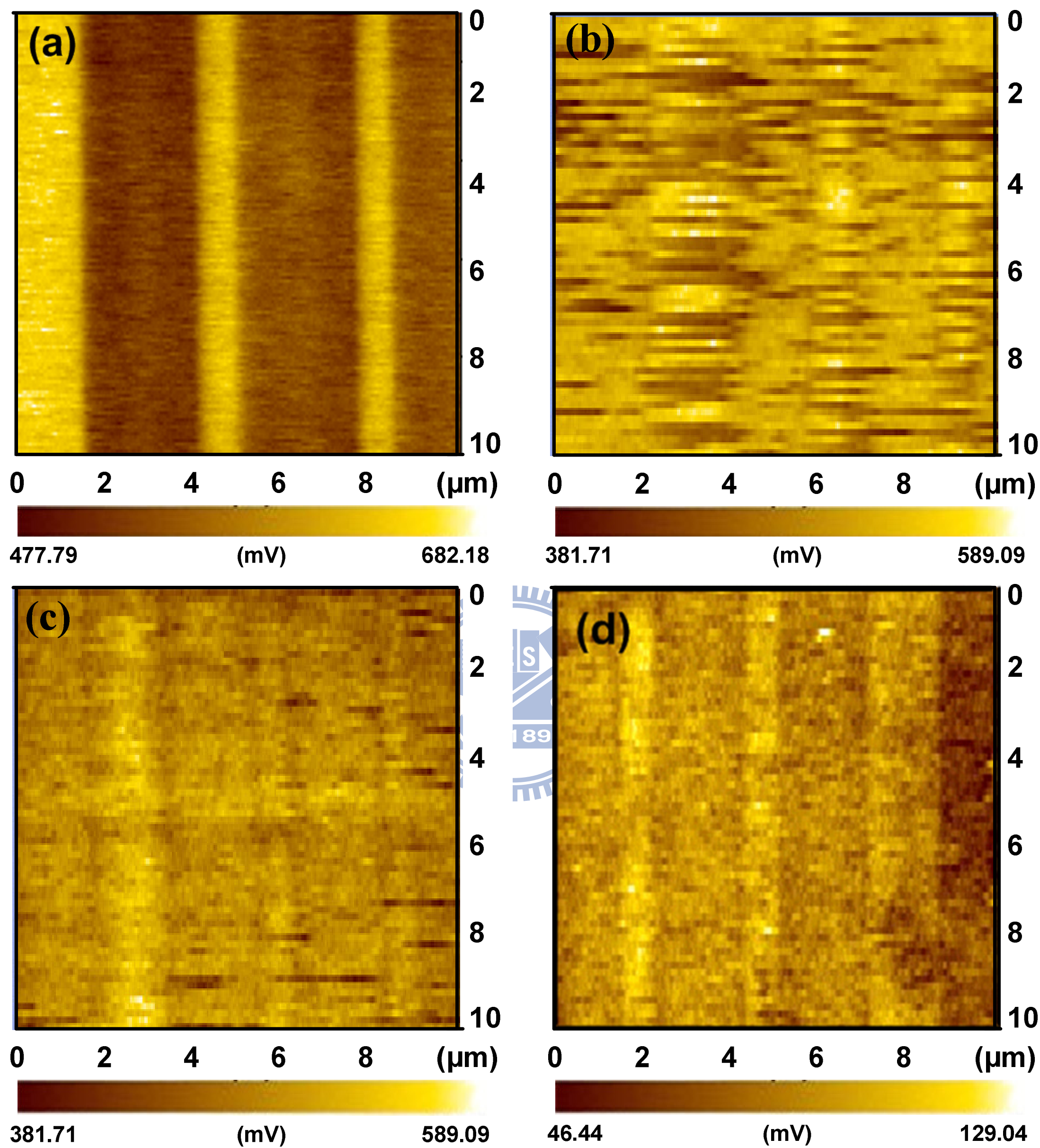



Fig.5-6 Surface potential images of samples A, B, C, and D measured by KPFM. The surface treatment methods for the four samples are listed in Table I.

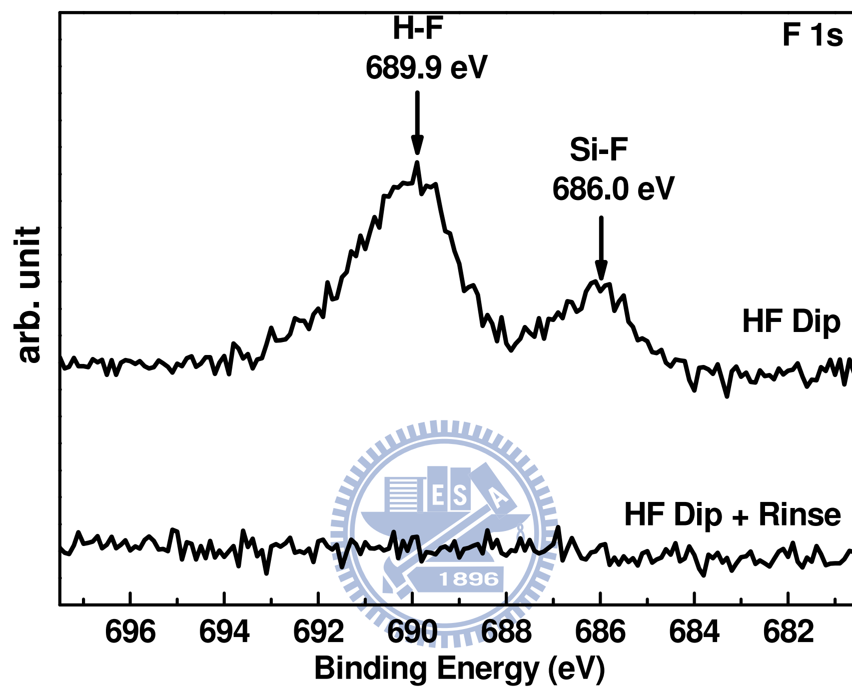



Fig.5-7 The F 1s binding energies of samples A and B measured by XPS.

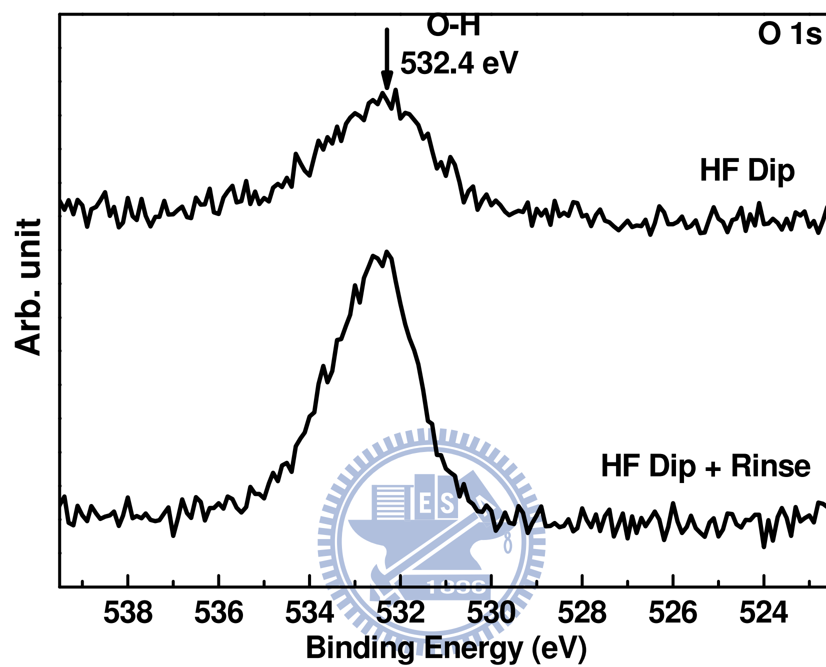



Fig.5-8 The O 1s binding energies of samples A and B measured by XPS.

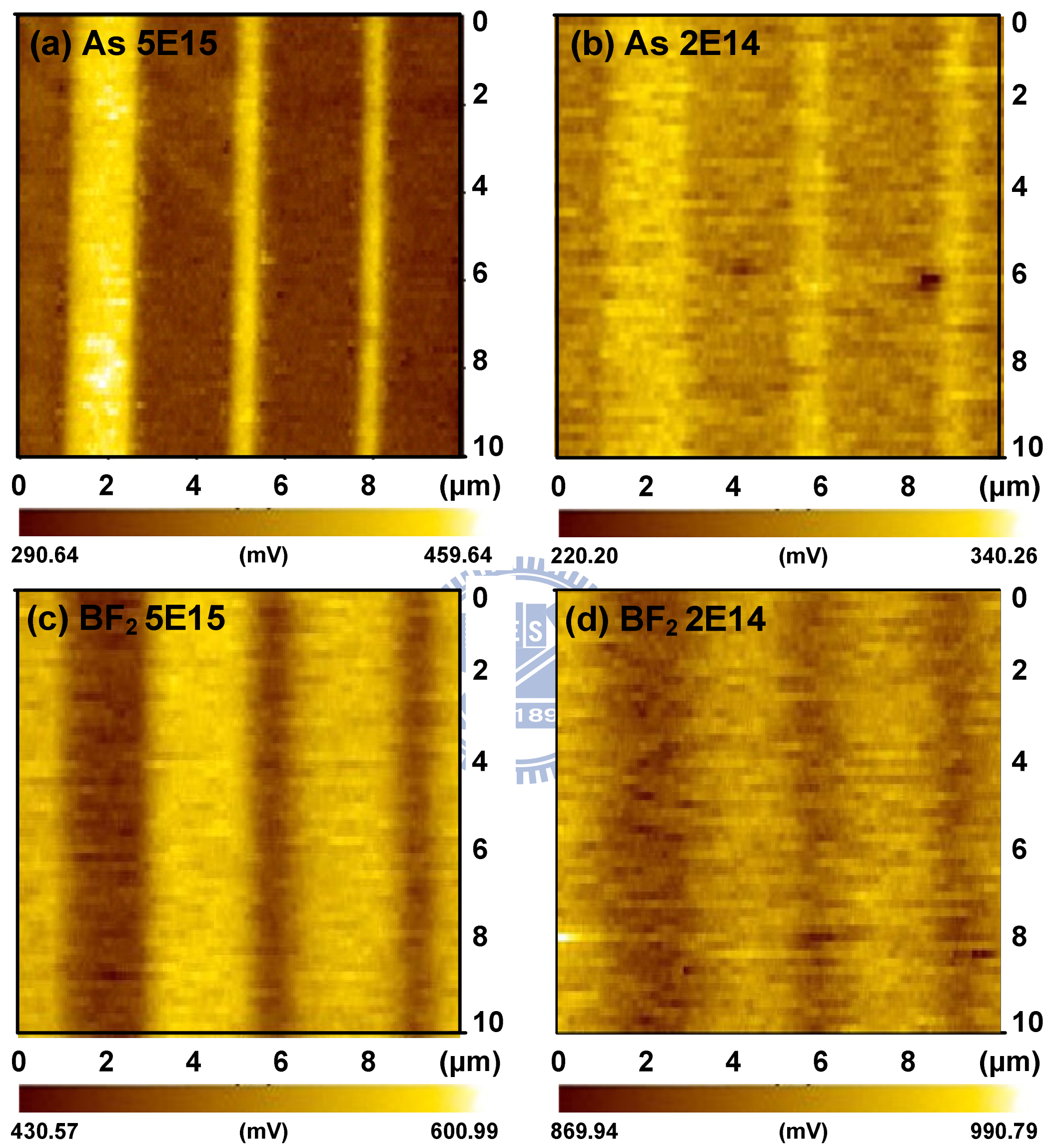



Fig.5-9 Surface potential images of samples with different ion implantation conditions: (a) $As^+$ 5 × $10^{15}$, (b) $As^+$ 2 × $10^{14}$, (c) $BF_2^+$ 5 × $10^{15}$ and (d) $BF_2^+$ 2 × $10^{14}$ $cm^{-2}$.

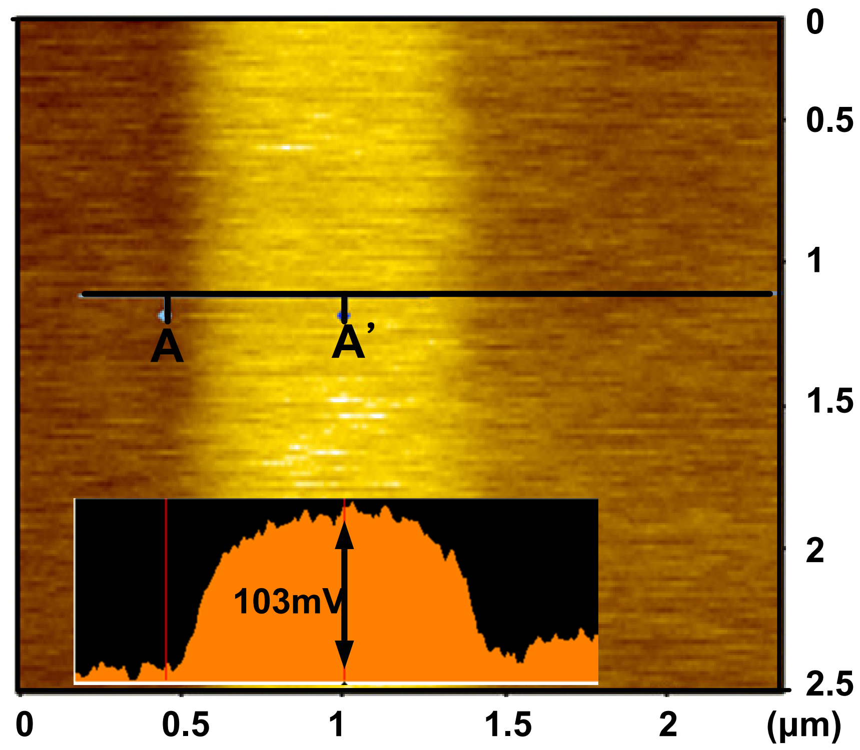



Fig.5-10 Surface potential images with $BF_2^+$ implantation at a dose of $5 \times 10^{15}$ $cm^{-2}$.

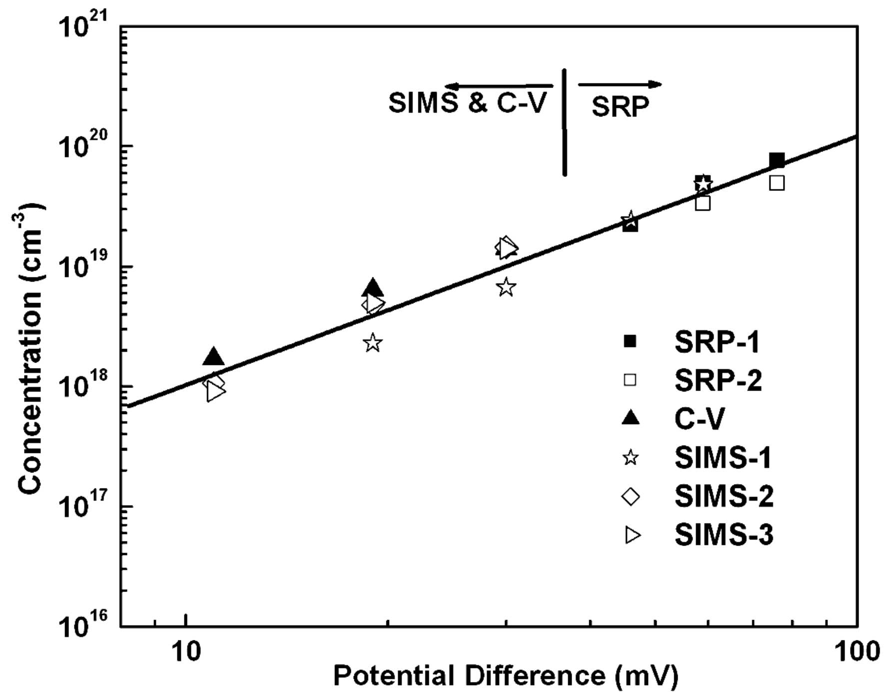



Fig.5-11 Correlation between surface potential difference and surface carrier concentration of the $n^+$-p junctions with different $As^+$ ion implantation doses.

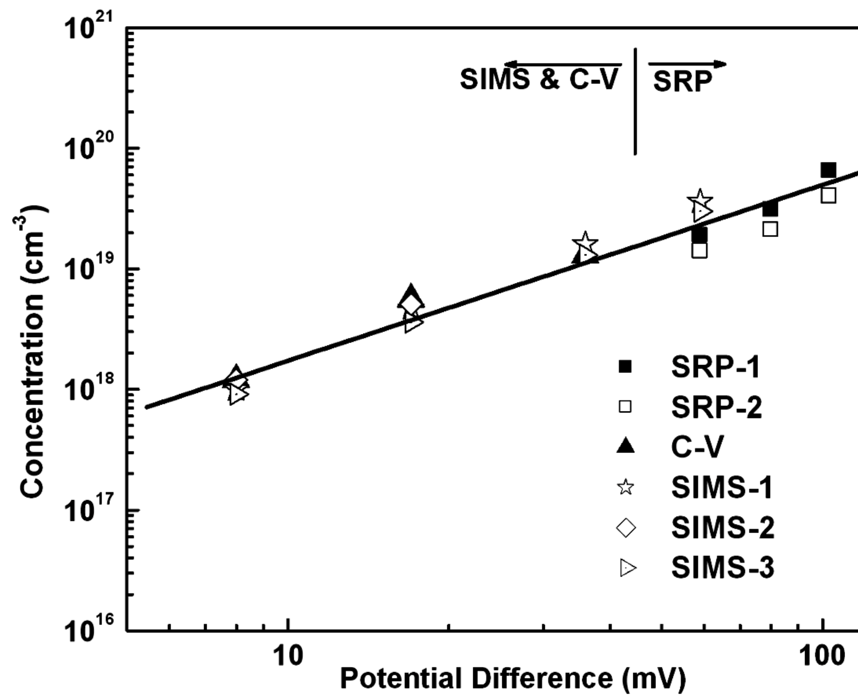



Fig.5-12 Correlation between surface potential difference and surface carrier concentration of the $p^+$-n junctions with different $BF_2^+$ ion implantation doses.

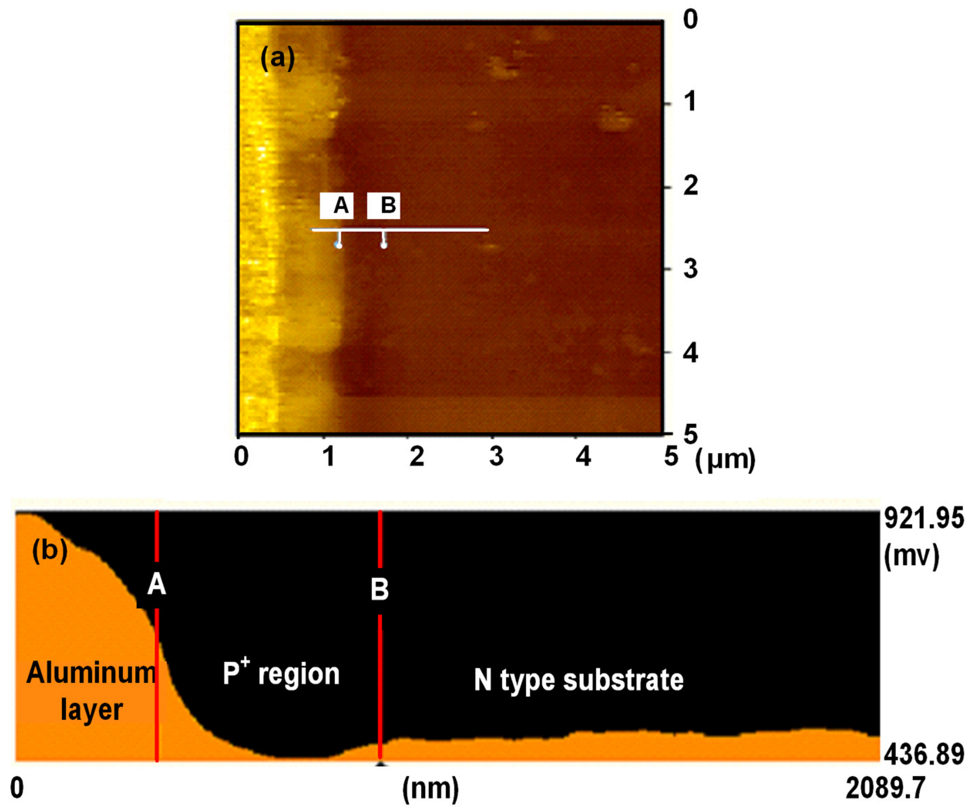



Fig.5-13 Surface image and the potential profile of a $p^+$-n junction in vertical direction after cleaving and polishing.

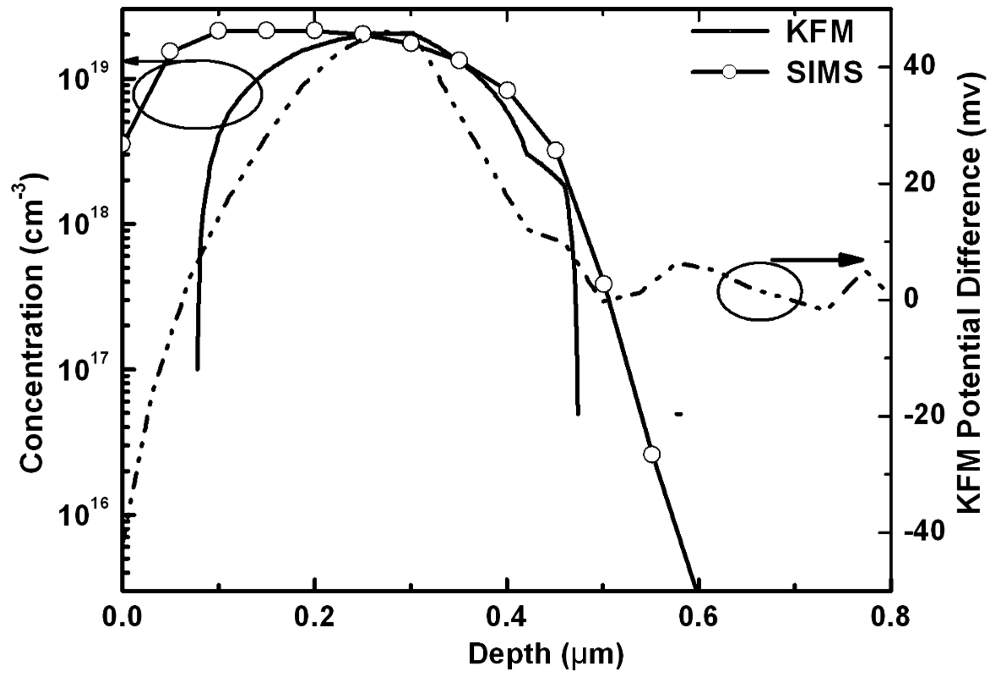



Fig.5-14 Carrier depth profiles of the $p^+$-n junction shown in Fig.13 measured by KPFM and SIMS.

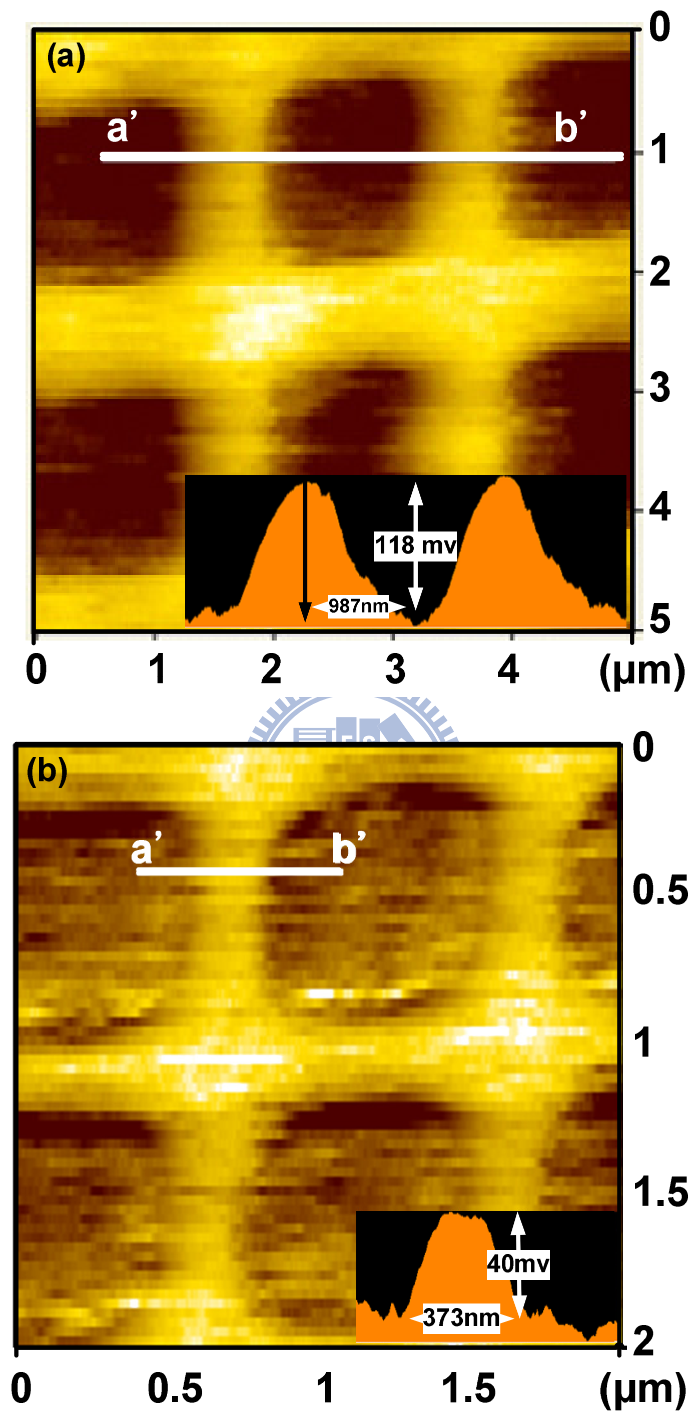



Fig.5-15 Surface potential image of p-n junction array (a) 0.8 × 0.8 μm$^2$ and (b) 0.4 × 0.4 μm$^2$ measured by KPFM.

# Chapter 6

# Summary and Future Recommendations

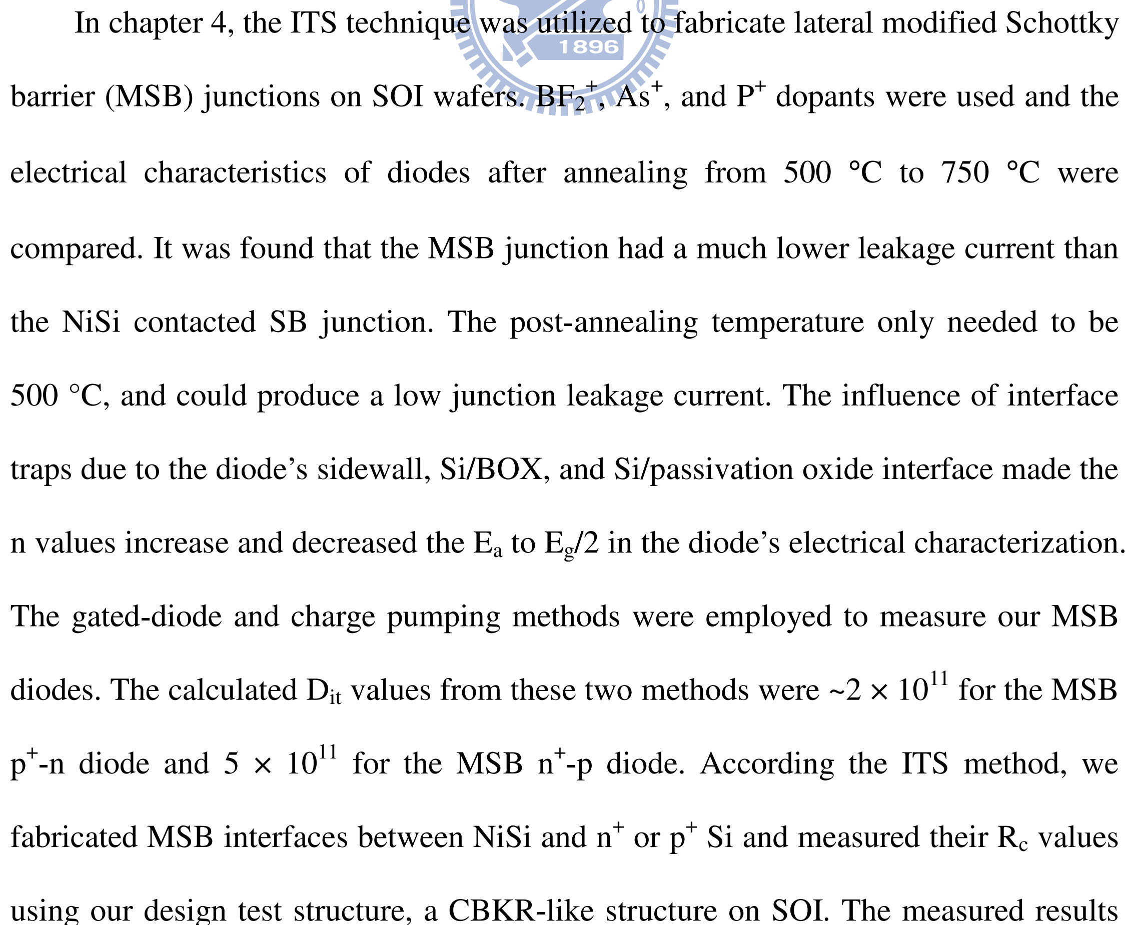
## 6-1 Summary

This dissertation included several nickel silicide (NiSi) analyses and the application of NiSi contacted junctions. The major contributions of each subject in this work are summarized as follows.

First, several material characteristics of NiSi films with Ge ion implantation (Ge I/I) were studied in chapter 2. We investigated the thermal stability of NiSi with Ge I/I, and compared it with the conventional NiSi process. An obvious improvement of NiSi's thermal stability can be obtained without degrading the sheet resistance even after a $2^{nd}$ formation step as high to 850 °C. The sustainable process temperature of the GIBS sample, considering thin film agglomeration and phase transformation, could be improved by 50~100 ºC for highly doped $n^+$ and $p^+$ bulk Si substrates. In our experiments, we also applied GIBS to $n^+$ and $p^+$ poly-gates, which was compatible with the self-aligned CMOS process. From the measured sheet resistance results, SEM inspections, and XRD results, the allowable temperature of NiSi on $n^+$ poly gates was improved from 650 °C to 750 °C and from 700 °C to 800 °C for $p^+$ poly gates. A smooth NiSi/Si or NiSi/poly-Si interface could also be obtained, even at high temperatures, as seen in SEM and TEM images. The total experimental results of thermal stability were summarized in Table 6-1.

Then, in chapter 3, NiSi contacted $n^+$-p and $p^+$-n junctions combined with the Ge

I/I technique of chapter 2 were demonstrated. As expected, the Ge I/I junction had better thermal stability and could improve the junction leakage current at high temperatures in $p^+$-n junctions. We observed smaller peripheral leakage currents and better thermal stability by electrical characterizations, including n factor, I–V, $E_a$, etc. Yet, the Ge I/I junction had a reliability issue involving Ni diffusion and dissolution enhancement due to the extra defects induced by the Ge I/I. However, the mechanisms were identified in this work, and the advantage of a smooth NiSi/Si interface with Ge I/I was shown to be more beneficial for application to ultra-shallow junctions. Here, the contact resistsnce of a Ge I/I contacted interface was also studied. The lateral CBKR structure was fabricated on a $p^+$-Si layer with Ge I/I. A low contact resistivity was measured, with a value around $10^{-8}$ Ω-cm$^2$, which may be due to the fact that Ge ions can assist the activation of Boron ions.



In chapter 4, the ITS technique was utilized to fabricate lateral modified Schottky barrier (MSB) junctions on SOI wafers. $BF_2^+$, $As^+$, and $P^+$ dopants were used and the electrical characteristics of diodes after annealing from 500 °C to 750 °C were compared. It was found that the MSB junction had a much lower leakage current than the NiSi contacted SB junction. The post-annealing temperature only needed to be 500 °C, and could produce a low junction leakage current. The influence of interface traps due to the diode’s sidewall, Si/BOX, and Si/passivation oxide interface made the n values increase and decreased the $E_a$ to $E_g/2$ in the diode’s electrical characterization. The gated-diode and charge pumping methods were employed to measure our MSB diodes. The calculated $D_{it}$ values from these two methods were ~$2 \times 10^{11}$ for the MSB $p^+$-n diode and $5 \times 10^{11}$ for the MSB $n^+$-p diode. According the ITS method, we fabricated MSB interfaces between NiSi and $n^+$ or $p^+$ Si and measured their $R_c$ values using our design test structure, a CBKR-like structure on SOI. The measured results

were $2 \times 10^{-8}$ Ω-cm$^2$ for the $p^+$ MSB contact and $3 \times 10^{-7}$ Ω-cm$^2$ for the $n^+$ MSB contact.

In chapter 5, we demonstrated the two-dimensional carrier profiling technique by Kelvin-probe force microscopy (KPFM). First, the surface treatment effects and a feedback control circuit were used to improve the contrast and resolution in scanning surface potential images. Then, the correlations between the surface potential difference measured by KPFM and the results of secondary ion mass spectroscopy (SIMS), the surface carrier concentration obtained by spreading resistance profiling, and the capacitance-voltage method results were established. On the basis of these results, the carrier depth profiling of a 0.5 μm depth junction and $0.4 \times 0.4$ μm$^2$ junction array were successfully demonstrated.

## 6-2 Future Works

The following points are suggestions and requirements that are worthy of further research.

1. The Ge I/I defects could be eliminated by laser annealing or another low-temperature method. The repaired Si substrate may have strain due to Ge doping; this will contribute to the mobility or contact resistivity enhancement. We could integrate this method into the MOSFET fabrication and investigate the device performance and reliability.
2. It has been reported that Ge I/I can reduce the grain size of NiSi and help to incorporate the low barrier height segregated metal. Perhaps, it is possible to combine the advantage of stable thermal stability because the post-annealing

process usually requires an additional thermal budget. Moreover, a new incorporated metal for a low barrier height to n-type Si is needed.

3. The KPFM can be improved by nanotube tips, and a fast responding feedback system. A very smooth polishing method and a non-influence capping layer are needed to scan the carrier distribution of a MOSFET's cross section.
4. A cleaning method for a NiSi surface is needed for contact holes before the metal layer is deposited. This will help us to measure the lower contact resistivity.

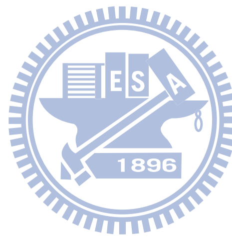


Table 6-1 Summary of thermal stability results for all samples.

| | **Blanket sample** | | | **Junction sample** | | | |
|---|---|---|---|---|---|---|---|
| **Sample type** | **NiSi (control)** | **GIBS** | **GIAS** | **$n^+p$ (control)** | **$n^+p$ (Ge I/I)** | **$p^+n$ (control)** | **$p^+n$ (Ge I/I)** |
| **Agglomeration Temperature** | 700 °C | 800 °C | 700 °C | 650 °C | 650 °C | 750 °C | 750 °C |
| **Phase transfer temperature** | 750 °C | 850 °C | 850 °C | 700 °C | >850 °C | 750 °C | >850 °C |
| | **Gate sample** | | | | **ITS sample** | | |
| **Sample type** | **$n^+p$ (control)** | **$n^+p$ (Ge I/I)** | **$p^+n$ (control)** | **$p^+n$ (Ge I/I)** | **$P^+$ I/I** | **$As^+$ I/I** | **$BF_2^+$ I/I** |
| **Agglomeration Temperature** | 700 °C | 750 °C | 700 °C | 800 °C | >800 °C | >800 °C | >800 °C |
| **Phase transfer temperature** | 700 °C | 800 °C | 700 °C | 800 °C | >800 °C | >800 °C | >800 °C |

# Publication List

A. International Paper

1. B. Y. Tsui, **C. M. Hsieh**, P. C. Su, S. D. Tzeng, S. Gwo, "Two-Dimensional Carrier Profiling by Kelvin-Probe Force Microscopy", *Japanese Journal of Applied Physics*, Vol. 47, pp. 4448-4453, 2008

2. **C. M. Hsieh**, B. Y. Tsui, Y. R. Hung, Y. Yang, R. Shen, "Thermal Stability Improvement of NiSi on Gate by High Dosage Germanium Implantation", *Electrochemical and Solid-State Letters*, Volume 12, pp. H226-H228, 2009

3. Bing-Yue Tsui, **Chih-Ming Hsieh**, Yu-Ren Hung, York Yang, Ryan Shen, Sam Cheng, and Tony Lin, "Improvement of the Thermal Stability of NiSi by Germanium Ion Implantation," *Journal Electrochemical Society,* vol.157*,* pp. H137-H143, 2010

B. International Conference

1.**C. M. Hsieh**, B. Y. Tsui, P. C. Su, S. D. Tzeng, and S. Gwo, Two-Dimensional Carrier/Dopant Profiling by Kelvin-Probe Force Microscopy" in *IEEE Si Nanoelectronics Workshop,* 2006

2.Chia-Pin Lin, Bing-Yue Tsui, **Chin-Ming Hsieh**, Chin-Feng Huang "Low Threshold Voltage CMOSFETs with NiSi Fully Silicided Gate and Modified Schottky Barrier Source/Drain Junction" in *International Symposium on VLSI Technology, Systems and Applications,* 2007

3. **Chih-Ming Hsieh**, Yu-Ren Hung, Bing-Yue Tsui, York Yang, Ryan Shen, Sam Cheng, and Tony Lin, "Improving Thermal Stability of Nickle Silicide by Germanium Ion Implantation", in *International Electron Devices and Materials Symposia*, 2007

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89 年 9 月-91 年 6 月

國立交通大學電子研究所博士班

91 年 9 月-98 年 9 月

博士論文題目：

矽化鎳之熱穩定性與超淺接面應用的研究

A Study on the Thermal Stability and Shallow Junction Applications of Nickel Silicide