國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

利用矽控整流器當做記憶單元之系統層級靜電放電暫態偵測電路

On-Chip Transient Detection Circuit with SCR as Memory Unit for System-Level ESD Protection

研 究 生：林宛彥　　(Wan-Yen Lin)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一百年八月

利用矽控整流器當做記憶單元之系統層級靜電放電暫態偵測電路

On-Chip Transient Detection Circuit with SCR as Memory Unit for System-Level ESD Protection

研 究 生：林宛彥　　Student: Wan-Yen Lin

指導教授：柯明道教授　　Advisor: Prof. Ming-Dou Ker

國立交通大學

電子工程學系　電子研究所

碩士論文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering
August 2011
Hsin-Chu, Taiwan, Republic of China

中華民國一百年八月

利用矽控整流器當做記憶單元之系統層級靜電放電暫態偵測電路

學生：林宛彥　　指導教授：柯明道教授

國立交通大學　電子工程學系電子研究所碩士班

ABSTRACT (CHINESE)

靜電放電 (Electrostatic Discharge, ESD) 是造成電子產品遭受過度電性應力 (Electrical Overstress, EOS) 最主要的原因。近年來，隨著積體電路 (Integrated Circuits, ICs) 技術進步至深次微米製程，同時為了減少電子產品成本，越來越多的積體電路整合在單一晶片系統上。在先進製程中，較薄的氧化物層和較窄的通道，都會使得積體電路的產品更容易受到靜電放電的破壞，因此，靜電放電的防護設計在積體電路技術中是一項很重要可靠度議題。

系統層級靜電放電在近年中的可靠度問題逐漸受到重視。許多電子產品即使已經通過元件層級靜電放電(Component-Level ESD)規範的測試，仍然無法達到系統層級靜電放電(System-Level ESD)防護的要求。在系統層級靜電放電防護的測試條件下，快速暫態雜訊會使得系統進入未知的當機、故障，或是不正常的工作狀態。傳統的解決方法是在微電子產品之中，加入許多種不同的濾波或是抗雜訊用的分離元件，但卻大幅地增加了微電子產品的生產成本。因此，對於系統層級靜電放電防護而言，應用於金氧半導體製程的積體電路設計防護方法可以整合於晶片系統中，減少產品成本，更具有其重要性。

本論文首先利用矽控整流器(Silicon Controlled Rectifier, SCR)元件會被暫態突波觸發的特性，提出了一種應用於系統層級靜電放電防護的暫態偵測電路設計。電路主要的原理是利用矽控整流器當作記憶元件。由實驗的結果證實，當有系統層級靜電放電事件發生時，提出的電路可以成功的偵測並且記憶快速暫態電波在積體電路電源線上產生的

干擾現象。

其次，提出一個結合積體電路雜訊濾波器以及暫態偵測電路的四位元暫態對數位轉換器。利用電流鏡電路，可以放大在電源線之間的等效電容值，在雜訊濾波器上的電容值可以有效的減小並節省晶片面積，以及避免漏電問題。此轉換器可以成功的將系統層級靜電放電之電壓轉換為四位元數位碼輸出，因此能夠確切知道積體電路在系統層級靜電放電測試之下所遭受影響之程度。

這份論文總共分成五個章節。第一章是有關於系統層級靜電放電防護國際法規的內容和條例；第二章介紹了傳統用來解決系統層級靜電放電防護的方法；第三章為以矽控整流器做為記憶單元的暫態偵測電路之介紹及實驗結果；第四章提出四位元暫態對數位轉換器，包括模擬和量測結果；第五章為此份論文的結論和未來展望。

On-Chip Transient Detection Circuit with SCR as Memory Unit for System-Level ESD Protection

Student: Wan-Yen Lin **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering and Institute of Electronics
National Chiao-Tung University

ABSTRACT (ENGLISH)

Electrostatic discharge (ESD) is the main reason that causes electrical overstress (EOS) on microelectronic products. Recently, as technology scaling down to the deep sub-micron, more integrated circuits are integrated into single chip to decrease the cost of microelectronic products. Due to thinner oxide and shallower junction depth in advance technology, microelectronic products equipped with CMOS ICs are more susceptible to ESD damage. Therefore, ESD protection has become an important reliability issue in CMOS ICs.

System-level ESD tests is an increasingly important reliability issue for CMOS ICs. It has been reported that reliability issues still exist in CMOS ICs under system-level ESD tests, even though they have passed component-level ESD specifications. The transient noise generated by system-level ESD events can cause microelectronic system into locked state, frozen state, or even hardware damage such as transient-induced latch-up. For traditional solutions, extra discrete components are often added on printed circuit board (PCB) to suppress system-level ESD events in microelectronic products. However, those discrete components are substantially increasing the cost of microelectronic products. As a result, chip-level solutions with silicon integration and to meet high system-level ESD specification for microelectronic products are strongly requested by IC industry.

In this thesis, first, with silicon controlled rectifier (SCR) device as memory unit, on-chip SCR-based transient detection circuit has been proposed and fabricated in 0.18-μm CMOS

process. It has been investigated that, under system-level ESD tests, the SCR device can be triggered on and the cross voltage can be dropped into holding voltage. Experimental results has confirmed that, when system-level ESD events happens, the detection circuit can successfully detect and memorize the occurrence of positive and negative fast electrical transients coupled on the power line and ground line of CMOS ICs. Furthermore, with hardware/firmware system co-design, display panel can automatically recover from the frozen state into normal operation after the system-level ESD zapping.

Second, a new on-chip transient-to-digital converter composed of four CR-based transient detection circuits and four different noise filters has been successfully designed and verified in a 0.13-μm CMOS process with 1.8-V devices. By using the current amplification techniques, capacitor used in the noise filter could be reduced to save silicon area and avoid leakage in deep submicron process. The output digital codes of the proposed on-chip transient-to-digital converter correspond to different level of positive/negative ESD voltages under system-level ESD tests. And these digital codes can be used as the firmware index to execute partial/total auto-recovery procedures in microelectronic systems.

This thesis is divided into five parts. In the first chapter, international standards about system-level ESD are generally guided. In chapter two, some traditional solutions to overcome system-level ESD events are collected and introduced. In chapter three, on-chip SCR-based transient detection circuit is proposed. In chapter four, on-chip transient-to-digital converter has been simulated in detail and circuit performance has been verified under system-level ESD tests. The last chapter includes conclusions and future works.

ACKNOWLEDGEMENT

兩年半的碩士生涯，默默的即將到了尾聲。在這些日子中，很感謝柯明道老師的指導，每一次與老師討論的過程中，都能從中得到不同的知識和啟發！也謝謝老師支持我出國交換學生的機會，除了學得更深，也看得更廣！

感謝實驗室眾多學長姐們的照顧和教導，林群佑學長、小王學長、小胖學長、陳穩義學長、惠雯學姐和竹立煒學長，謝謝你們在我遇到研究上的問題時，總是熱心的幫忙和鼓勵我！林佑達、陳思翰、張堂龍和陳韋霖和其他研究群的學長姐們，謝謝你們在我剛進實驗室人生地不熟時對我的照顧和幫忙！帶給大家歡樂的小州哥，謝謝你這兩年多來大小事的幫忙和鼓勵！最重要的，是要感謝帶我的正哥，在研究上總是不遺餘力的幫助我很多很多，細心和耐心的一步一步教導我，能 cover 我所有的問題和疑惑，從學長身上真的學到很多，也更深知自己還有很多不足的地方！

還有跟我同屆的夥伴們，黃筱晴和李易儒，能跟你們當同學真好，一起討論，一起擔心 Meeting 沒有人要報告，謝謝你們在口試的時候的幫忙和鼓勵！艷婷、簡仲、Adely，每次和你們聊天都會覺得很開心，帶給我很多的歡樂！安仔和建宏，能在研究所再待同一間實驗室真的很有緣，謝謝你們當初 DIC 的 cover！

謝謝奇景光電蔡志忠技術長、陳東暘博士、蔡青霖博士以及陳世範學長，不論是研究計畫的支持與實際面板應用上的協助，有你們的幫忙這份論文才能得以順利完成。

謝謝與我一同去魯汶的夥伴們，阿凱、吃吃、博堯、水哥、恕平、小客和燿嘉，一年的日子多虧有你們的照顧和幫忙，還有在魯汶的眾多學長姐們，Crystal 和韋智，能夠認識你們真的很幸運！謝謝 EP98 的朋友們，到了研究所仍然能與大家互相討論和分享生活的感覺很棒！謝謝一路陪我走過研究所生涯的 G 軒，你的鼓勵和你帶給我的歡笑，都是我繼續往前走的動力之一。

最後謝謝我的父母和姊姊，謝謝你們的支持和鼓勵！我愛你們！

林宛彥 2011.08.15 @新竹交通大學

CONTENTS

Table Captions

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Introduction

1.1. Motivation

Electrostatic discharge (ESD) is a serious reliability event that causes electrical overstress (EOS) on microelectronic products. This kind of phenomenon is a permanent destruction that would affect the function of integrated circuits (ICs). Recently, as technology scaling down to the deep sub-micron, more ICs are integrated into single chip to decrease the cost of microelectronic products. Due to thinner oxide and shallower junction depth in advanced technology, microelectronic products equipped with CMOS ICs are more susceptible to ESD stresses. Therefore, ESD protection has become an important reliability design in CMOS IC [23]-[27]. In order to verify the robustness of the ESD protections against the ESD-induced energy, many international standards have been established. Generally, component-level ESD and system-level ESD are two kinds of specifications to verify the ESD robustness of the CMOS ICs. The major difference between them is whether the equipment under test (EUT) is evaluated with or without power supply. Component-level ESD tests are used to simulate the well-controlled environment, such as factory environment. To characterize component-level ESD susceptibility of CMOS ICs, the test method should follow three ESD test standards: human-body-model (HBM), machine-model (MM), and charge-device-model (CDM) [1]-[3], [28]-[36].

On the other side, system-level ESD is now an increasingly important issue on microelectronic products due to transient-induced damage effect among the CMOS devices. [4], [5]. Under system-level ESD test, the ESD-generated transient electrical disturbance with

quite large amplitude and fast period can randomly exist on power line (V_{DD}), ground line (V_{SS}), and input/output (I/O) pins. This energy may cause malfunction or hardware destruction, such as logic data losing or the chip burning out. In order to ensure the yield of the microelectronic products, several electromagnetic compatibility (EMC) regulations are defined. The microelectronic products are required to evaluate system performances under test standard of system-level ESD test. For examples, in the system-level ESD test standard of IEC 61000-4-2 [6], the microelectronic products are required to sustain the ESD-generated voltage of ±8 kV (±15 kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4". Unfortunately, it has been reported that even though some CMOS IC products have passed component-level ESD specifications, they are still susceptible to system-level ESD stresses. The experimental results have confirmed the power and ground lines of microelectronic products no longer maintain the normal operating voltage under system-level ESD tests, but underdamped sinusoidal waveforms with an amplitude of several tens to hundreds of volts and period of several tens of nanoseconds instead [4]. From previous studies, it has been reported the super twisted nematic (STN) liquid crystal display (LCD) panel keeps in locked state and shows error display after system-level ESD tests [7]. Traditionally, extra discrete components are added to suppress system-level ESD events in microelectronic products [8]. Those discrete components including, ferrite bead, magnetic core, and transient voltage suppressor (TVS), are used to decouple, absorb or bypass the electrical transients generating from system-level ESD zapping. In traditional solutions, the total cost of microelectronic products will increase substantially. Additionally, the requirement of ESD level is often depended on customer-defined specifications and ESD protection designs need to be different for various product applications. It is more challenging to achieve high ESD level compared with previous products. Therefore, system-level ESD protection design plays an important role in many kinds of CMOS IC products. As a result, the chip-level solutions with silicon integration design and to meet high system-level ESD

specification for microelectronic products are strongly requested by IC industry.

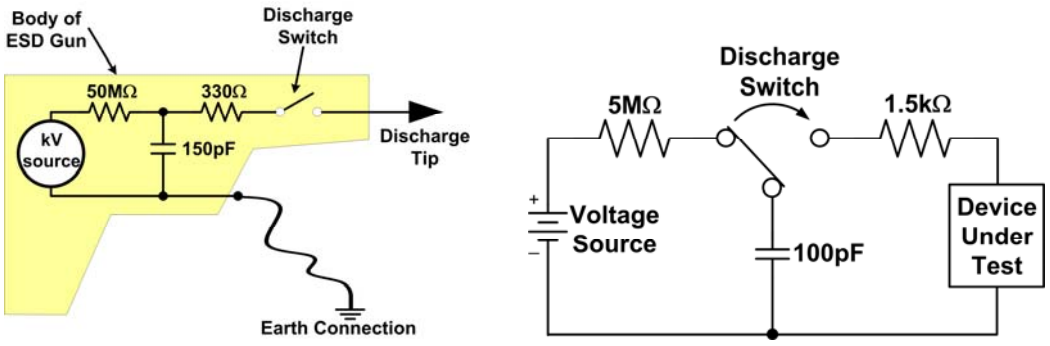
1.2. Introduction of International Standard

ESD is an important reliability issue on CMOS IC products, especially in the advanced technology. Many international associations, such as ESDA (Electrostatic Discharge Association), AEC (Automotive Electronics Council), EIA (Electronic Industries Alliance), JEDEC (Joint Electron Device Engineering Council), and MIL-STD (US Military Standard), etc, have drawn up the different ESD standards for all kinds of ESD conditions. All of the international standards described above are component-level ESD standards. The component-level ESD standards defined the test environment, test methods, and the corresponding ESD test level. In order to verify the robustness of CMOS ICs under system-level ESD events, many international companies adopt other specifications, such as IEC 61000-4-2 (system-level ESD events) and IEC 61000-4-4 (EFT events). IEC 61000-4 is a part of the IEC 61000 series, and the main contents of part 4 are about testing and measurement techniques. In this section, the international standards are described below.

1.2.1. IEC 61000-4-2 Specification

The objective of the standard, IEC 61000-4-2, is to establish a common and reproducible basis for evaluating the performance of CMOS ICs inside the electrical/electronic microelectronic products. This standard specifies typical waveform of the discharge current, test levels, test equipment, test set-up, and test procedure. In order to verify the disturbance of CMOS ICs under system-level ESD tests, the ESD gun is used to zap the ESD-induced energy into the EUT. Fig. 1.1 (a) shows the equivalent circuit of ESD gun. Moreover, the equivalent circuit of the human body model is shown in Fig. 1.1 (b). The energy storage capacitor, the discharge resistor, and the discharge switch shall be placed as close as possible to the discharge electrode. Comparing with the two equivalent circuits, the storage capacitor

in system-level ESD test is 150pF, while in component-level ESD test, it is 100pF. That means, the ESD-induced energy stored in the system-level ESD condition is larger than that in the component-level ESD condition. The discharge resistors used in the Fig. 1.1 (a) and (b) are 330Ω and 1.5kΩ, respectively. Therefore, the ESD-induced energy generating from ESD gun in system-level ESD tests has faster rise time than that in component-level ESD tests. Fig. 1.2 shows the typical waveforms of the discharge current under system-level ESD test (IEC 61000-4-2) and component-level ESD test (MIL-STD 883). Under 8-kV ESD zapping condition, the peak current in system-level ESD test is about five times larger than that in component-level ESD test. In order to compare the test results obtained from different ESD generators, the characteristics of the waveform of discharge current are listed in Table I. Table II shows the test level (test voltage) of component-level ESD test, such as HBM, MM, and CDM. The system-level ESD tests are divided into contact discharge and air discharge test modes, as shown in Table III. The discharge electrodes of two test modes are shown in Fig. 1.3. Contact discharge is the preferred test method, and air discharge shall be used when contact discharge cannot be applied. There is no obvious relationship to imply that the test severity is related between contact discharge and air discharge test modes.



(a) (b)

Fig. 1.1 The equivalent circuit of (a) ESD gun which is used to zap the ESD-induced energy under system-level ESD test and of (b) human body model under component-level ESD test.

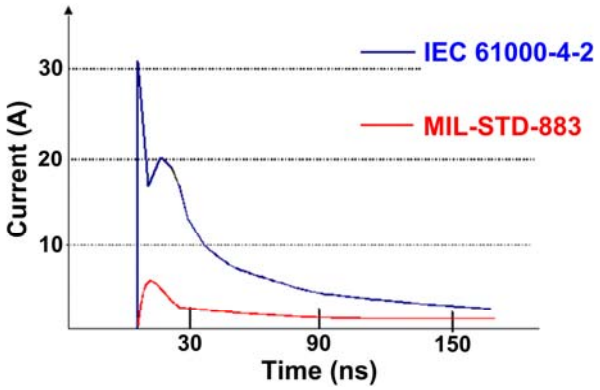


Fig. 1.2 Under 8-kV ESD zapping, the peak current in system-level ESD test is about five times larger than that in component-level ESD test.

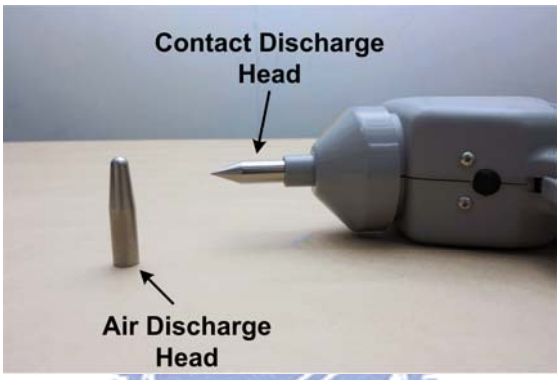


Fig. 1.3 Discharge electrodes of ESD gun which is used under system-level ESD test with (a) contact discharge mode and (b) air discharge mode.

TABLE I Waveform parameters of discharge current.

Level	Indicated Voltage (kV)	First Peak Current ±10% (A)	Rise Time (ns)	Current (±30%) at 30ns (A)	Current (±30%) at 60ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

TABLE II Component-level ESD specifications.

Model Name	Test Voltage
Human Body Model	＞2000V
Machine Model	＞200V
Charge Device Model	＞1000V

TABLE III System-level EMC/ESD specifications - test levels.

Contact Discharge		Air Discharge	
Level	Test Voltage (kV)	Level	Test Voltage (kV)
1	± 2	1	± 2
2	± 4	2	± 4
3	± 6	3	± 8
4	± 8	4	± 15
X	Specified by Customer	X	Specified by Customer

Comparing Table III with Table II, the test voltage of system-level ESD is larger than component-level ESD, whether under contact discharge or air discharge test modes. According to these phenomena, system-level ESD tests affect the system operation of the microelectronic products more seriously than component-level ESD tests. Table IV shows the evaluation of system-level ESD test results. The test results shall be classified in terms of hardware damage, loss function, or degradation of performance of the EUT. From the evaluation table, the microelectronic product should reset itself automatically after system-level ESD test to pass the “class B” specification.

TABLE IV Recommended classifications of system-level ESD test results.

Criterion	Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. **(Automatic Recovery)**
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. **(Manual Recovery)**
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

The EUT shall be operated within the specified climatic conditions to avoid unnecessary influence from electromagnetic environment of the laboratory. The measurement setup of system-level ESD test is shown in Fig. 1.4 and the elaboration of this setup will be followed in chapter 3.

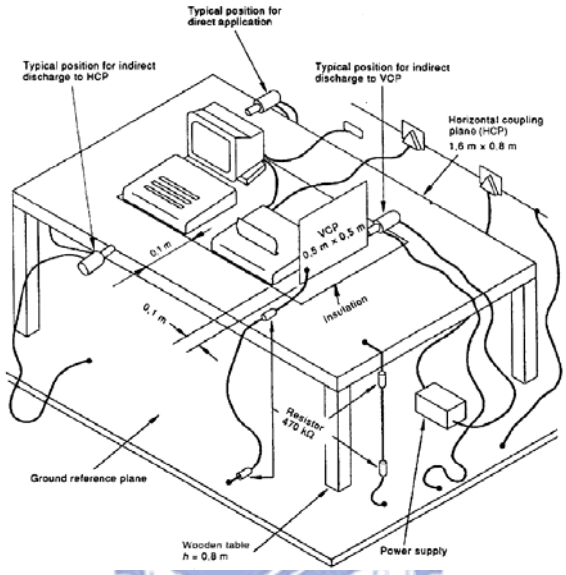


Fig. 1.4 Measurement instruments of system-level ESD test.

1.2.2. IEC 61000-4-4 Specification

IEC 61000-4-4 is an international standard which gives immunity requirements and test procedures related to electrical fast transients (EFT) [9]. EFT disturbances commonly exist in industrial environment where electromechanical switches are used. The EFT test intends to demonstrate the immunity of electronic equipments against transient disturbances originating from switching transients, such as interruption of inductive loads, relay constant bounce, etc.

The equivalent circuit diagram of the EFT generator is shown in Fig. 1.5 and the major elements of the EFT test generator are listed in Table V. In particular, the impedance matching resistor R_m (50Ω) and the DC blocking capacitor C_d (10nF) are defined in the standard. The charging capacitor C_c is used to store the charging energy and R_c is the charging resistor. The R_s shapes the pulse duration. The effective output impedance of the generator is 50Ω.

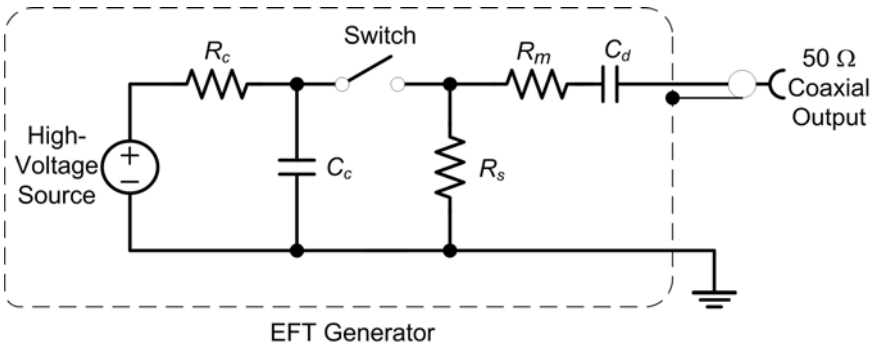


Fig. 1.5 The equivalent circuit of EFT generator.

TABLE V Characteristics of the EFT generator.

Parameter	Definition
R_c	Charge Resistor
C_c	Energy Storage Capacitor
R_s	Duration Shaping Resistor
R_m	Impedance Matching Resistor
C_d	DC Blocking Capacitor

During EFT tests, the power lines of the CMOS ICs inside the microelectronic products no longer maintain their initial voltage levels. A number of fast transients would randomly couple into power, ground, and I/O pins, causing the ICs inside the EUT to be upset or frozen after EFT zapping. The characteristics of such a high-voltage-level EFT-induced disturbance are listed in Table VI and shown in Fig. 1.6. The test voltage waveforms of these fast transients are defined in the standard with the repetition frequency of 5kHz and 100kHz. A burst consists of 75 pulses with repetition period of 0.2ms (repetition rate of 5kHz) under EFT tests. Therefore, the burst duration time is 15ms, and the period between two adjacent bursts is 300ms. Similarly, for the EFT pulse with the repetition frequency of 100kHz, there are seventy-five pulses in each burst and the burst duration time is 0.75ms. The rise time and duration of a single pulse voltage waveform must accord with the characteristics which are listed in Table VII and shown in Fig. 1.7. A voltage pulse waveform with rise time of 5ns±30% and duration of 50ns±30% occurs on the test pins of EUT under EFT tests. The EFT

test levels for testing power supply ports and for testing I/O, data, and control ports of the EUT are listed in Table VIII. The voltage peak for I/O, data, and control ports is half of the voltage peak for testing power supply ports. Level "X" is an open level, and is specified in the dedicated equipment specification.

TABLE VI Characteristics of the fast transient/burst.

Repetition Rate (kHz)	Repetition Period (ms)	Pulse Number	Burst Duration (ms)	Burst Period (ms)
5	0.2	75	15	300
100	0.01	75	0.75	400

TABLE VII Characteristics of a single pulse in each burst.

Parameter	Value
Frequency	5 kHz or 100 kHz
Rise Time	5ns ± 30%
Duration	50ns ± 30%

TABLE VIII EFT specifications - test levels.

Level	On Power and PE (Protective Earth) Ports		On I/O (Input/Output) Signal, Data, and Control Ports	
	Voltage Peak (kV)	Repetition Rate (kHz)	Voltage Peak (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	Specified by Customer	Specified by Customer	Specified by Customer	Specified by Customer

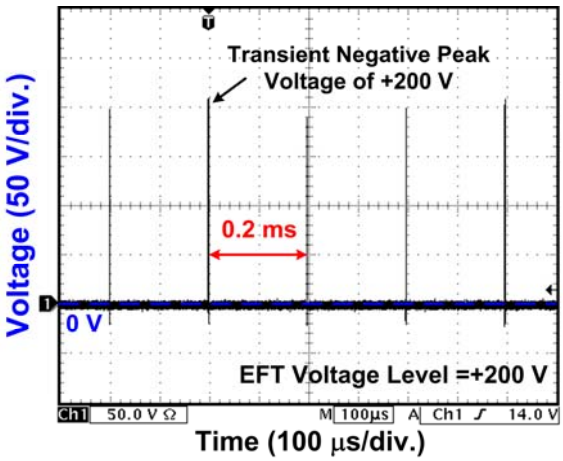


Fig. 1.6 General graph of fast transient/burst.

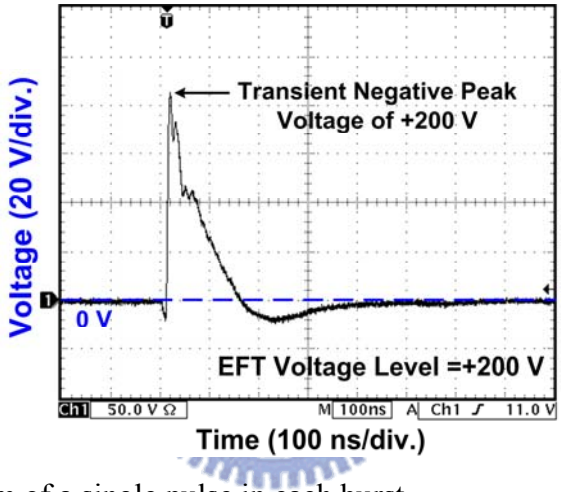


Fig. 1.7 Voltage waveform of a single pulse in each burst.

1.3. Thesis Overview

Based the previous introduction, how to solve the system-level ESD events has become an important issue for the IO industry. The goal of this thesis is to find some chip-level solutions towards system-level ESD problems. This thesis would divide into five chapters.

In chapter 2, an overview of some traditional techniques on solving system-level ESD events is introduced. In chapter 3, by using the device of silicon controlled rectifier (SCR) as memory unit, the on-chip SCR-based transient detection circuit is proposed. In chapter 4, the topic focuses on the 4-bit transient-to-digital converter. Finally, in chapter 5, the conclusions and the future works of this thesis are given.

Chapter 2

Solutions to Overcome System-Level Electrical Transient Disturbance

2.1. Background

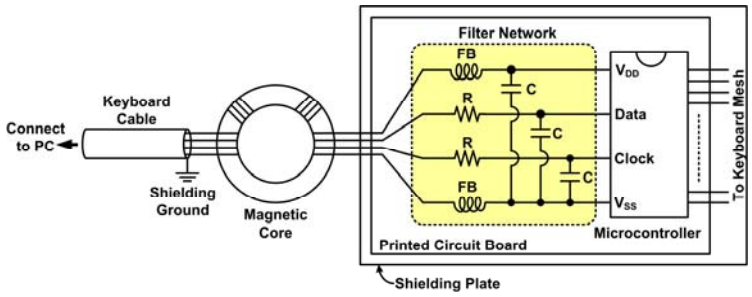
The phenomenon of electrostatic discharge commonly exists in the real world. For component-level ESD protection, grounded-gate NMOS (GGNMOS) and diode are the simple way to protect CMOS ICs from ESD events. Moreover, to provide strong protection against transient disturbance, other protection methods and new structure device have been studied and proposed to enhance immunity against large impulse current. However, system-level ESD test is defined when the power line of the microelectronic products connects to the normal operating voltage, which is different from test conditions of component-level ESD tests. Furthermore, as shown in Fig. 1.2, the peak current in system-level ESD test is about five times larger than that in component-level ESD test. The system-level ESD stresses can cause more serious damage compared with component-level ESD events. Therefore, the methods to prevent damages against component-level ESD event may not be available in system-level ESD protection considerations.

Recently, IC designers gradually pay more attentions to the system-level ESD events. More and more test methods have been published to investigate the system-level ESD events. It would provide an appropriate way for IC designers to obtain more analysis ways on the transient disturbance protection. Generally in laboratory tests, the ESD robustness of discrete devices is tested by applying a current pulse with a waveform compliant to the IEC 61000-4-2 standard. The ESD failure threshold is typically determined by monitoring the leakage current.

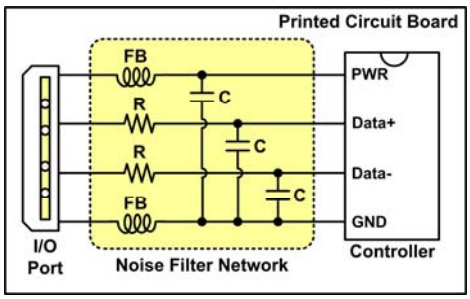
When the leakage current is larger than the defined value, ESD damage is considered to happen [10]. Based on this knowledge, several software, including finding the hot spot on the IC chip, are now popular in the IC industry. A new test standard, which called human metal model (HMM), also comes up to connect the relationship between the component-level ESD and the system-level ESD tests [11]. Although there are lots of ways to do the system-level ESD test, the on-chip solution towards it is still not too much. For traditional solution for microelectronic products against system-level ESD tests, the basic concept is to use off filters to bypass or absorb the large transient disturbance. Since for the advanced technology, system-on-a-chip (SOC) has become a trend to provide multi-function integration and save cost, how to avoid system-level ESD stresses causing SOC system locked in frozen state would become an important design topic

2.2. Traditional System Design Solutions

In order to improve the immunity of microelectronic products to achieve the strict ESD specifications, system designers can take many approaches to prevent ESD damage. One of the system design solution against system-level ESD events is to add some discrete noise-decoupling components or board–level noise filters on the printed circuit board (PCB), as shown in Fig. 2.1. For example, Fig. 2.1(a) shows the system solution to overcome the system-level ESD issue in keyboard, and Fig. 2.1(b) is used for universal series bus (USB) input/output (I/O) port.



(a)



(b)

Fig. 2.1 The system solution to overcome the system-level ESD issue by adding extra discrete components to absorb or bypass the electrical fast transients (a) in keyboard and (b) in USB I/O port.

These discrete components are used to decouple, bypass, or absorb the transient noise generated from system-level ESD events. Therefore, the discrete components can reduce the transient energy of transient disturbance coupled on power lines of CMOS ICs inside microelectronic products. Some noise-decoupling components can even clamp the transient voltage at low level to avoid ESD damage on internal circuits of CMOS ICs. Some discrete noise-bypassing components for system-level ESD protection, such as transient voltage suppressor (TVS), or low-pass noise filters, have been reported and would discuss in the following sections [12].

2.2.1. Transient Voltage Suppressor (TVS)

Transient voltage suppressor (TVS) is commonly used to improve the system-level ESD immunity of microelectronic products. It can provide ESD energy discharge path under system-level ESD tests. TVS is located between I/O ports and connected pins of CMOS ICs

to provide system-level ESD protection function in the PCB of microelectronic products. The main function of TVS is to absorb high peak power under ESD tests. It is acted as a surge protector. The peak pulse power of TVS can be estimated by

$$P_{peak} = I_{pp} \times V_{clamp} \quad (1)$$

where I_{pp} is the maximum lightning current that TVS can bypass, and V_{clamp} is the voltage when I_{pp} is applied across the device. Devices with lower clamping voltage during ESD stress conditions can sustain higher ESD level. Although TVS could be ESD protector, its immunity performance is not well enough compared to other discrete components. Moreover, TVS has high capacitive loading, which can cause distortion on high data rate signals. As a result, TVS is not suitable for high speed applications.

For ESD protections, there are many types of TVS components, such as varistor, metal oxide varistors (MOVs), and zener diode, etcs. Varistors are made of ceramic materials. MOVs contain a ceramic mass of zinc oxide grains. Compare with other TVS components, MOVs have lower capacitance. However, for high speed interface applications, the capacitance of MOVs is still too high to prevent signal distortion. Moreover, MOVs has high impedance with low clamping voltage. When the voltage across this device is high, the resistance value would drop to a low level. This voltage drop across the varistor will dramatically increase as the current increase. As a result, if the ESD clamping voltage is too high, varistor is hard to protect electronic products.

2.2.2. Low-Pass Noise Filter

To meet the strict system-level ESD specification, different types of board-level noise filters have been investigated to improve the immunity of CMOS ICs inside the

microelectronic products under system-level ESD tests [13]. Adding board-level noise filter between noise trigger source and CMOS ICs can absorb, bypass, or decouple ESD-generated energy to avoid ESD damage on EUT. Several types of board-level noise filters, such as capacitor filter, LC-like filter (2^{nd}-order), and π-section filter (3^{rd}-order), as shown in Fig. 2.2, have been confirmed the enhancement of system-level ESD immunity. For evaluating the transient-induced latchup (TLU) level of DUT, these three different kinds of filters are investigated. Among different noise filter network, the higher-order noise filters have better performance to enhance TLU-triggered level of DUT, and thus have better immunity against system-level ESD events. Experimental data is shown in Fig. 2.3 [13].

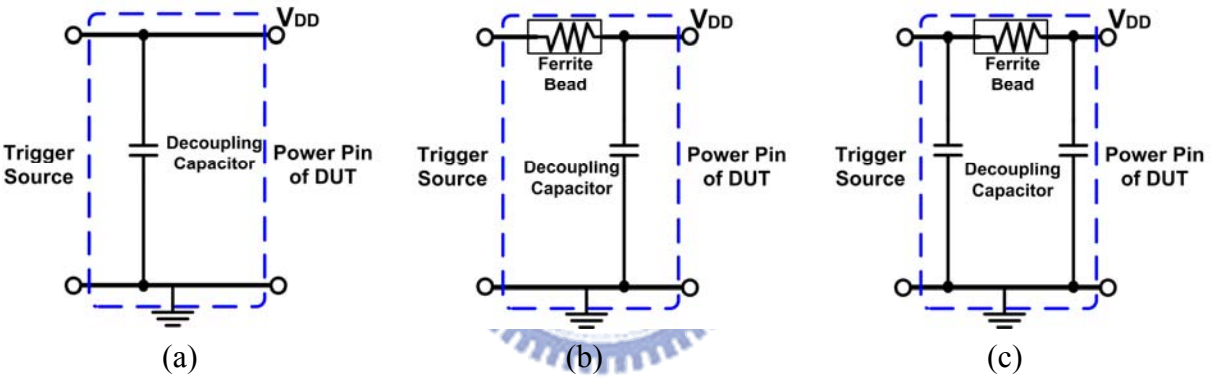


Fig. 2.2 Board-level noise filter of (a) capacitor filter, (b) LC-like filter, and (c) π-section filter.

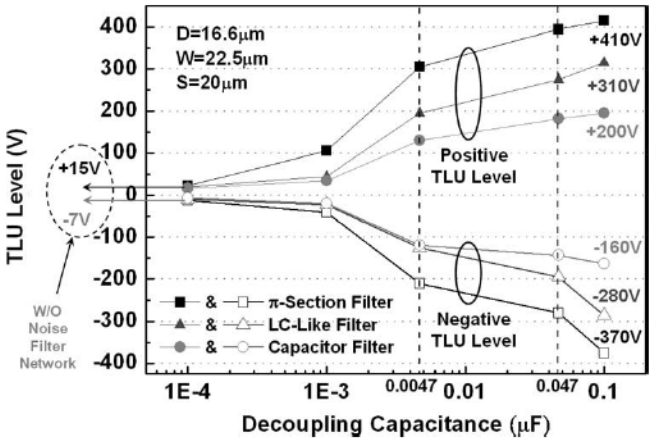


Fig. 2.3 Relations between the decoupling capacitance and the TLU level of the DUT under three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter [13].

2.2.3. Design Concept of Printed Circuit Board (PCB)

While discrete ESD components are used to suppress the effect of system-level ESD events, PCB design is another important topic on ESD protection design. A simple diagram was shown in Fig. 2.1. To design the printed circuit board against system-level ESD events, few concepts needs to be taken into account. First, the induced magnetic current into circuit loop will be proportional to the size of the loop [12]. Therefore, minimizing the loop size on the PCB is a critical design for ESD reliability enhancement. Second, place the circuit devices on the PCB as close as possible to minimize the lengths of signal and power lines. It can avoid receiving too much energy generating from system-level ESD events.

2.2.4. External Hardware Timer

Another method which is totally different from the previous solutions is to regularly check the system abnormal conditions by using an external hardware timer, such as watch dog timer. This additional hardware timer is often designed with registers or flip flops as a reference clock for system operation if the main program was locked or frozen due to some fault conditions. However, during system-level ESD or EFT tests, the logic states stored in the registers or flip flops of hardware timer would sometimes also be destroyed, still causing malfunction or frozen condition in the system operation. Therefore, this kind of timer is not a stable way to protect microelectronic products against system-level ESD events.

2.3. Hardware/Firmware Co-Design

The above solutions try to solve system-level ESD events by off-chip designs, which would occupy additional chip area. It has been reported that the ESD protection device required more IC area to achieve 2 kV HBM ESD protection when the gate oxide thickness shrinks, as shown in Fig. 2.4 [14].

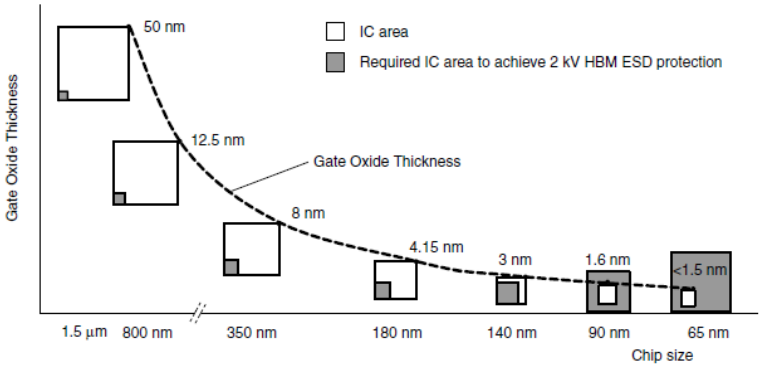


Fig. 2.4 Required IC area for ESD protection as a function of chip size [14].

In recent years, it had been reported that the hardware/firmware co-design can effectively improve the system-level ESD susceptibility of the CMOS IC products [8]. As the hardware/firmware co-design case shown in Fig. 2.5, the detection results (V_{OUT}) from the on-chip transient detection circuit can be temporarily stored as a system recovery index for firmware check. The transient detection circuit is designed to detect and memorize the occurrence of system-level ESD events. For example, the output (V_{OUT}) state in the on-chip transient detection circuit and the firmware index are initially set to logic "1". When the fast electrical transient happens, the on-chip transient detection circuit can detect the fast electrical transient and then change the output state (V_{OUT}) from logic "1" to logic "0". The system recovery index is therefore flagged at logic "0", which will be checked by the firmware to automatically recover all system functions to a stable state as soon as possible. After the recovery procedure, the output state of the on-chip transient detection circuit and the firmware index are re-set to logic "1" again for detecting the next electrical transient disturbance events.

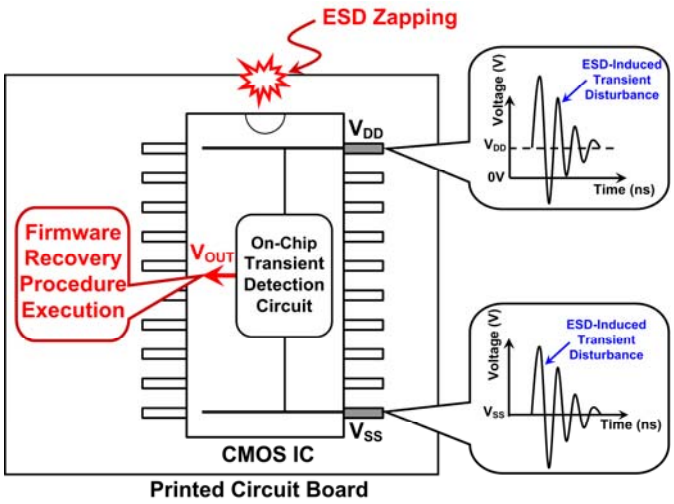


Fig. 2.5 Hardware/firmware co-design for system recovery by using the detection results of the on-chip transient detection circuit.

Moreover, it had been proven that the hardware/firmware co-design can effectively improve the robustness of the industrial products against electrical transient disturbance [8]. For display system protection design with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power systems are needed for electrical display functions, as shown in Fig. 2.6. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and digital power line (VDDD) is used for shifter register to store display signals. The transient detection circuit, designed for detecting and memorizing the occurrence of ESD-induced transient disturbance, can connect with VDDD power line to implement the hardware/firmware protection design in display system. The detection results from the detection circuit can be temporarily stored as a system recovery index for firmware check, as shown in Fig. 2.6. In the beginning, the output (V_{OUT}) state of the detection circuit is initially reset to logic "1." When the electrical transients happen, the detection circuit can detect the occurrence of system-level ESD-induced transient disturbance and transit the output state (V_{OUT}) to logic "0." At this moment, the firmware index is also changed to logic "0" to initiate automatic recovery operation to restore the microelectronic display system to a desired stable state as soon as possible. After the automatic recovery

operation, the output of the detection circuit and the system recovery index are re-set to logic "1" again for detecting the next ESD-induced electrical transient disturbance events.

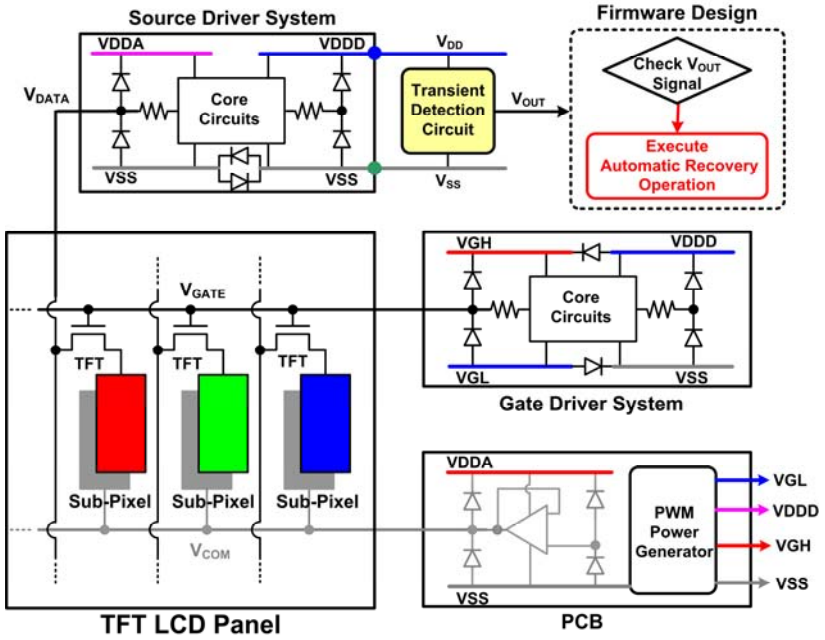


Fig. 2.6 Hardware/firmware system co-design with transient detection circuit in display panel product.

2.4. Summary

System-level ESD protection has now become more and more important for IC industry. Several methods have been discussed and analyzed in this chapter. Transient voltage suppressor can provide ESD energy discharge path under system-level ESD tests, but its nonlinear resistance characteristic is its drawback. Board-level noise filter on PCB is another choice to enhance system-level immunity, but the occupied area should be taken into account as well. Above all, traditional solutions toward system-level ESD immunity have some limitation, either in the aspect of occupied area or cost. Hardware/firmware co-design has been proved to have capability enhancing the system-level ESD robustness of microelectronic products. Moreover, on-chip detection circuit can be used to save PCB area and provide detection results for firmware to execute the automatic system recovery procedures. Based on

this request, the on-chip solutions will be developed in advance and to be the trend for future solution for system-level ESD events.

Chapter 3

Design of On-Chip SCR-Based Transient Detection Circuit

3.1. Background

It has been investigated that during the system-level ESD events, the power line and ground line of the microelectronic products would be disturbed by the fast and large transient electrical disturbance. As technology continues to scale down, designers should put more emphasis on the electrical disturbance generated from system-level ESD stresses, which would cause malfunction of CMOS ICs. Traditional board-level solutions have limitation in silicon integration and product cost. According to the IEC61000-4-2 standard, IC product is recommended to pass “class B” at least. That means, system should have the capability to automatically recover from upset states after the ESD zapping, not stay in the frozen or any unknown state. In recent years, on-chip transient detection has proposed to co-operate with hardware/firmware system to execute the system auto recovery procedures. With the published experimental results, it has been confirmed that chip-level co-design can successfully improve system-level ESD immunity and save ESD protection device area.

3.2. Prior Art

Previously, four transient detection circuits for system-level ESD protections have been proposed [8], [15]-[17]. The circuit diagram of the first on-chip transient detection circuit is shown in Fig. 3.1 (a). Two latch logic gates are used as the ESD sensor unit to detect the system-level ESD events on the power and ground lines. Coupling capacitors can be added

between the input/output nodes of latch and V_{DD}/V_{SS} lines in order to enhance the sensitivity of the ESD sensor to fast transients on the V_{DD}/V_{SS} line. It has been analyzed that the NMOS in the inverter of sensor_1 in Fig. 3.1 (a) is designed with a larger W/L ratio than that of the PMOS to make the latch locking at logic "0" easily. The PMOS in the inverter of sensor_2 is designed with a larger W/L ratio than that of the NMOS to make the latch easily locking at logic "1" [8].

The second transient detection circuit is designed with latch logic gates and capacitors shown in Fig. 3.1 (b). In this transient detection circuit, a latch circuit composed of two inverters is used to memorize the logic state after the system-level ESD tests. The capacitors C_{p1} (C_{p2}) are used to detect the positive (negative) fast electronic transients. It has been confirmed that the W/L ratio of inverters in the latch and the coupling capacitance will strongly influence the sensitivity of this detection circuit. The NMOS (M_{nr}) can provide a reset function to set the V_{OUT} to be logic "0". When the voltage of V_{DD} is below the voltage of V_{SS}, the parasitic diodes of PMOS would be turned on. Therefore, this circuit can detect the positive system-level ESD events. Similarly, the parasitic diodes of NMOS of inverters would be turned on under the negative system-level ESD stress.

The third one is designed with RC-based circuit structure to realize the transient detection circuit, as shown in Fig. 3.1(c). The two inverter latch is used to memorize the logic state before and after the system-level ESD events. The NMOS (M_{nr}) provides the reset function to set the output (V_{OUT}) logic state to be initially high. Under system-level ESD stress, due to RC time constant delay, the PMOS device of INV_1 and NMOS (M_{n1}) would be turned on by the overshooting ESD voltage. M_{n1} can pull down the output voltage level and thus change the output logic state from logic "1" to logic "0". Therefore, the third proposed transient detection can successfully detect and memorize the occurrence of system-level ESD events.

The last one uses RC-based circuit structure without latch circuit to implement the

detection function, as shown in Fig. 3.1(d). The PMOS device (M_{p1}) helps to memorize the logic state before and after the system-level ESD stress. The NMOS device (M_{nr}) provides the reset function to set the initial output voltage (V_{OUT}) to be 0 V. When there is fast electrical transient disturbance, RC-time constant delay would urge PMOS device (M_{p1}) to turn on by the overshooting ESD voltage. Therefore, output logic state would transfer from logic "0" to logic "1". Those previous transient detection can detect and memorize the occurrence of system-level ESD events.

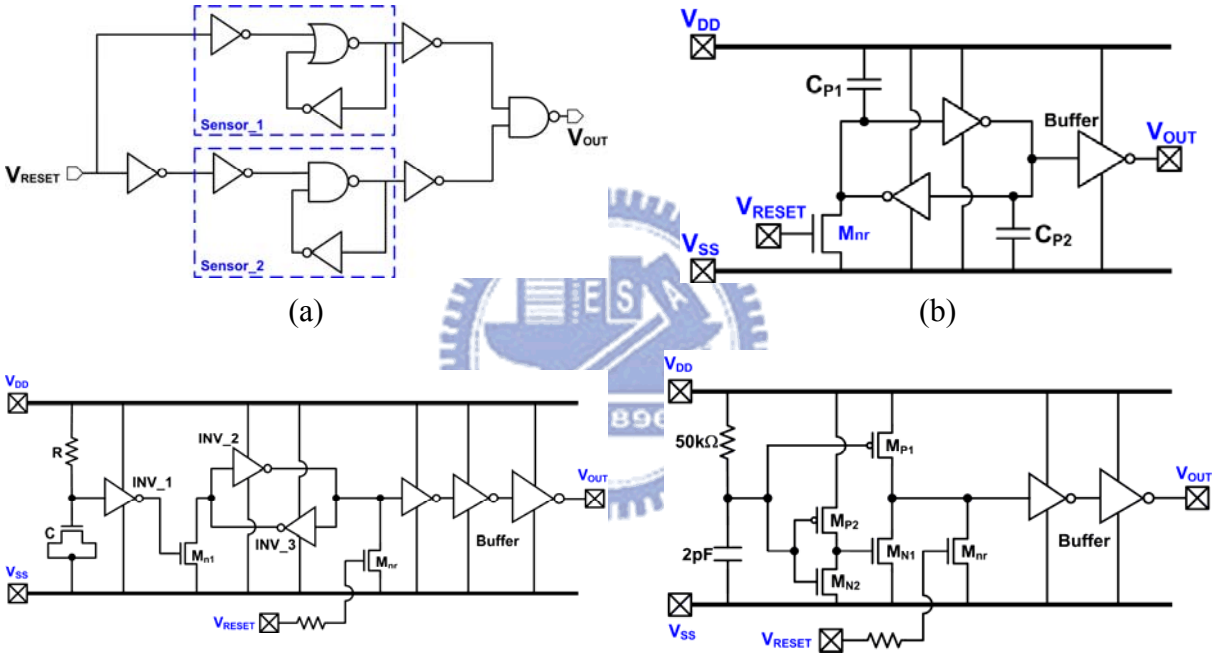


Fig. 3.1 Previous transient detection circuits composed of (a) a sensor circuit, (b) a latch circuit with additional capacitors (C_{P1} and C_{P2}), (c) RC-based detection cell, and (d) RC circuit without latch cell.

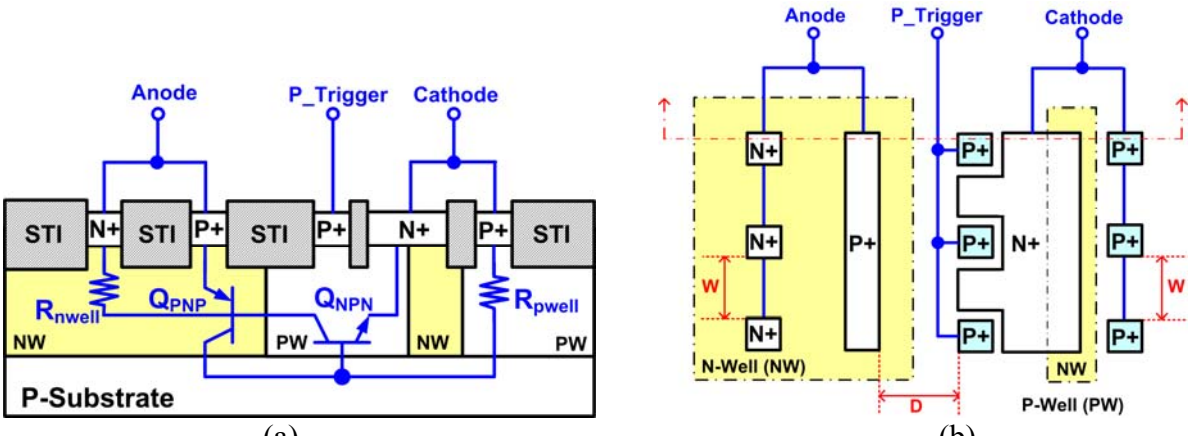
3.3. New On-Chip SCR-Based Transient Detection Circuit

The new on-chip SCR-based transient detection circuit is designed to detect the positive or negative fast electrical transients during the system-level ESD or EFT tests. Under the normal circuit operation condition (V_{DD}=3.3 V), the output state of the new proposed on-chip

SCR-based transient detection circuit is kept at 3.3 V as logic “1”. After the transient disturbance, the output state will transit from 3.3 V to 0 V. Therefore, the new proposed on-chip SCR-based transient detection circuit can detect and memorize the occurrence of system-level electrical transient disturbance events.

3.3.1. Silicon Controlled Rectifier (SCR)

The silicon controlled rectifier (SCR) was often used as the on-chip ESD protection device due to its high ESD robustness within small layout area [18]. The anode of SCR is connected to the P+ and N+ diffusions in N-well (NW), whereas the cathode of SCR is connected to the N+ and P+ diffusions in P-well (PW). The equivalent circuit of the SCR structure composes of a lateral NPN and a vertical PNP bipolar transistor to form the 2-terminal/4-layer PNPN (P+/NW/PW/N+) structure. The original switching voltage of the SCR device is decided by the avalanche breakdown voltage of the N-well/P-well junction. It has been reported that the turn-on mechanism of SCR device is essentially a current triggering event [19]. While a current is applied to the base or substrate of SCR device, it can be quickly triggered into its latching state. The device cross-sectional view and the layout top view of the p-type substrate-triggered SCR (P_STSCR) are shown in Fig. 3.2(a) and Fig. 3.2(b), respectively.



(a) (b)

Fig. 3.2 (a) Device cross-sectional view and (b) layout top view, of the p-type substrate-triggered SCR (P_STSCR).

An extra P+ diffusion is inserted into the P-well of the P_STSCR device and connected out as the p-trigger node. The geometrical parameters such as D and W represent the distance between the anode and cathode, and the distance between the adjacent well contacts, respectively. In this work, the P_STSCR structure with the layout parameters of D=0.86 μm and W=3.8 μm in a 0.18-μm CMOS process with 3.3-V devices is used as the memory unit to memorize the occurrence of electrical transient disturbance. The SCR in this work is not used as on-chip ESD protection device, but as the memory unit in the transient detection circuit.

The setup to measure the DC current–voltage (I-V) curves of the fabricated P_STSCR device under substrate-triggered current (I_{bias}) is shown in Fig. 3.3. The measured DC I-V curves of the P_STSCR under different substrate-triggered currents are shown in Fig. 3.4. When the substrate-triggered current applied to the p-trigger node increases from 1 mA to 4 mA, the switching voltage of P_STSCR is reduced from 8.6 V to 1.5 V. With the substrate-triggered current, the P_STSCR structure can be triggered into the latching state without involving the avalanche junction breakdown.

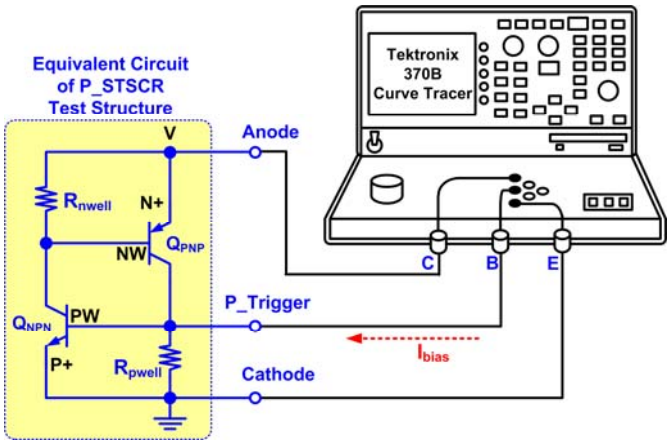


Fig. 3.3 Measurement setup of P_STSCR device under different trigger currents.

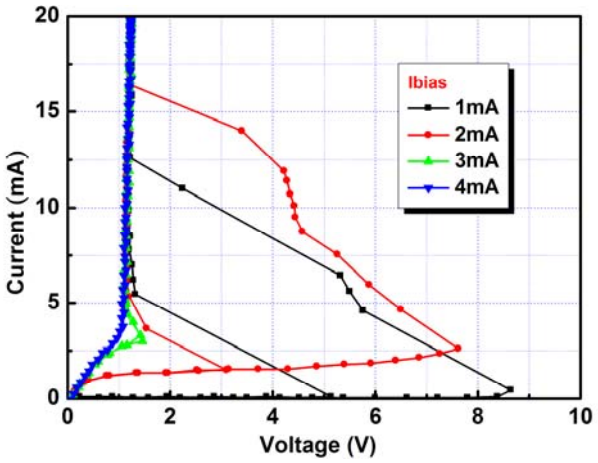


Fig. 3.4 The measured I-V characteristics of P_STSCR device under different trigger currents.

3.3.2. SCR-Based Transient Detection Circuit

The new proposed on-chip SCR-based transient detection circuit of this work is shown in Fig. 3.5. The P_STSCR device shown in Fig. 3.2 is used as the memory unit to memorize of the occurrence of system-level electrical transient disturbance. The anode of P_STSCR is connected to the drain of PMOS (M_{pr}) device. The gate of PMOS (M_{pr}) is connected to V_{SS} by the initial reset signal (V_{RESET}) to set the initial output voltage (V_{OUT2}) at 3.3 V. The RC-delay circuit and the inverter are designed to provide the SCR triggering current. Under the system-level ESD or EFT events, the transient voltage has a fast rise time in the order of nanosecond (ns). Because the RC-delay circuit is designed with a time constant in the order of microsecond (μs), the voltage level of V_X has much slower voltage response than the transient voltage coupling to V_{DD}. Due to the longer delay of the voltage increase at the node V_X, the PMOS device (M_{p1}) can be turned on by the overshooting voltage at V_{DD} and conduct trigger current to the p-trigger node. The SCR device is therefore turned on to pull down the output voltage (V_{OUT1}) level to the SCR holding voltage of ~1.2 V. In the two-inverter buffer stage, the logic threshold voltage of inverter1 (INV_1) is designed at ~2.4 V and that of inverter2 (INV_2) is ~1.7 V. Therefore, after electrical transient disturbance, the final output voltage (V_{OUT2}) of the proposed detection circuit will change from 3.3 V to 0 V to detect and

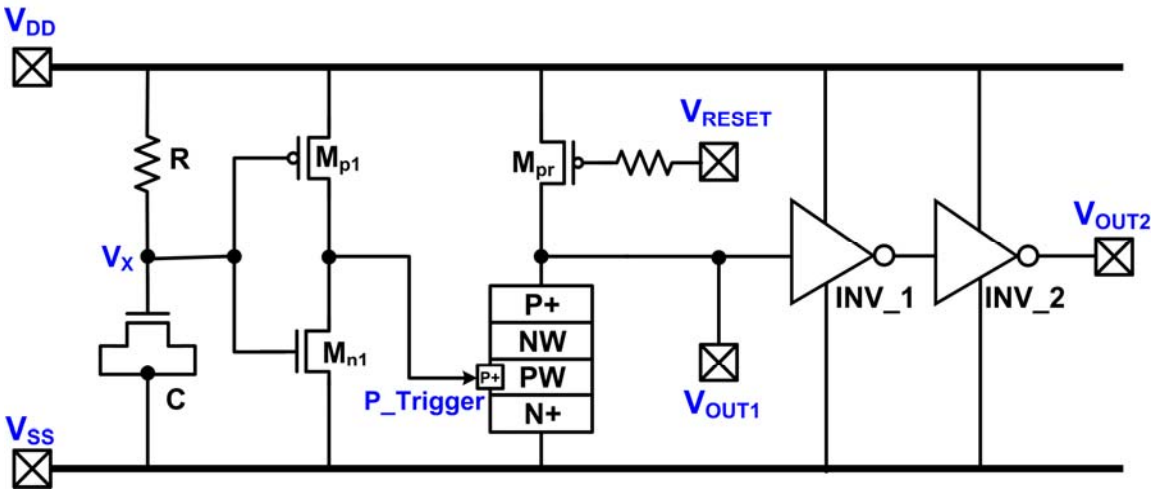


Fig. 3.5 The new proposed on-chip SCR-based transient detection circuit. The P_STSCR is used as memory cell to memorize the occurrence of electrical transient disturbance.

memorize the occurrence of system-level ESD/EFT-induced transient disturbance. The reset function (V_{RESET}) is then used to release the turn-on state of SCR device by turning off M_{pr}_device, and reset the output voltage (V_{OUT2}) back to 3.3 V again for detecting the next system-level transient disturbance.

3.4. Experimental Results

The proposed detection circuit has been designed and fabricated in a 0.18-μm CMOS process with 3.3-V devices. The fabricated test chip with the silicon area of 542 μm x 240 μm is shown in Fig. 3.6.

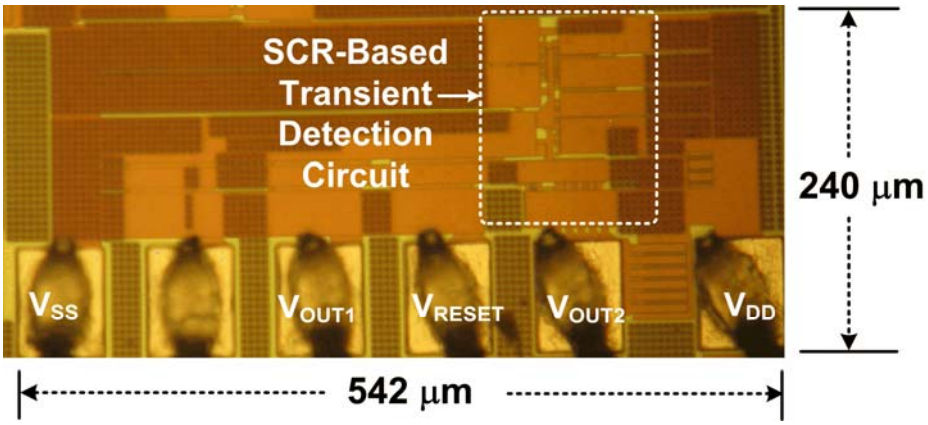


Fig. 3.6 Chip photo of the new proposed on-chip SCR-based transient detection circuit fabricated in a 0.18-μm CMOS process with 3.3-V devices.

3.4.1. Transient-Induced Latchup (TLU) Test

To evaluate the system-level ESD immunity of a single IC inside the equipment under test (EUT), a component-level transient-induced latchup (TLU) measurement setup was reported with the following two advantages [20]. First, the TLU immunity of a single IC can be evaluated by the measured voltage and current waveforms through the oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how an IC inside the EUT is disturbed by the ESD-generated transient disturbance during the system-level ESD test. Fig. 3.7 illustrates such a component-level TLU measurement setup. A charging capacitance of 200pF is used to store the charges as the TLU-triggering source, V_{Charge}, and then the stored charges are discharged to the device under test (DUT) through the relay. The underdamped sinusoidal voltage generated by TLU measurement is similar to the transient voltage on the power pins of CMOS ICs under the system-level ESD tests, whether polarity (positive or negative) of the ESD voltage is. Moreover, a small current-limiting resistance of 5 Ω is recommended to protect the DUT from electrical-over-stress (EOS) damage during the high-current (low-impedance) latching state. The supply voltage of 3.3 V is used as V_{DD} and the trigger source is directly connected to DUT through the relay in the TLU measurement setup.

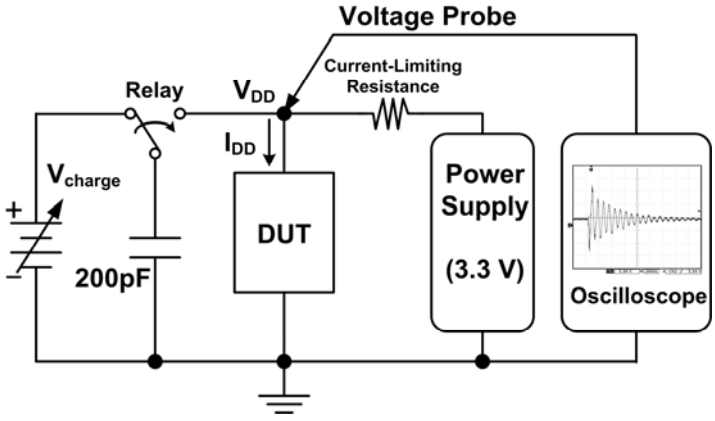
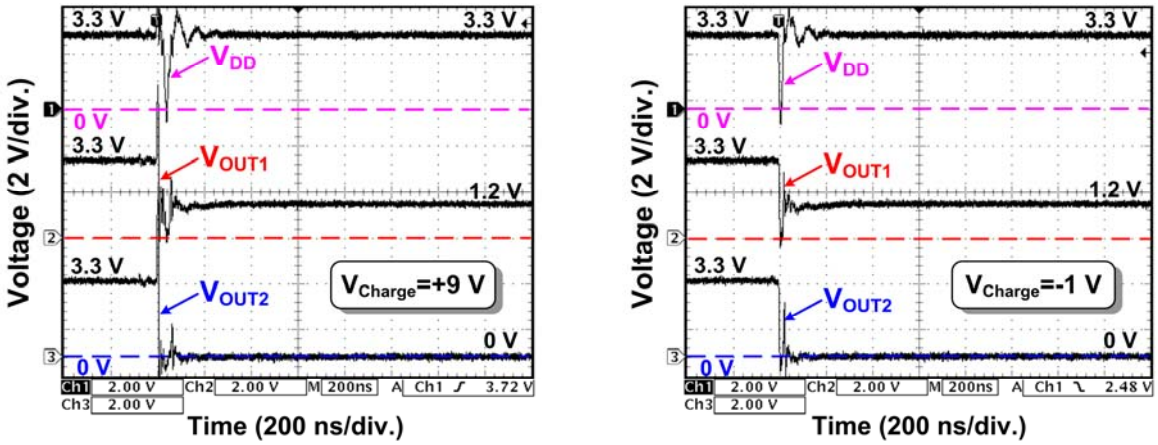


Fig. 3.7 Measurement setup for transient-induced latchup (TLU) [20].

Figs. 3.8(a) and 3.8(b) show the measured V_{DD}, V_{OUT1}, and V_{OUT2} transient voltage waveforms of the on-chip SCR-based transient detection circuit under the TLU tests with V_{Charge} of +9 V and -1 V, respectively. As shown in Fig. 3.8(a), under the TLU test with V_{Charge} of +9 V, V_{DD} begins to increase rapidly from 3.3 V with positive-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT1} and V_{OUT2} are influenced simultaneously by the positive-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of +9 V, the output voltage V_{OUT1} of the proposed transient detection circuit is changed from 3.3 V to 1.2 V, which is equal to the SCR holding voltage. Through two-inverter buffer stage, V_{OUT2} of the proposed detection circuit is pulled down to 0 V. In Fig. 3.8(b), under the TLU test with V_{Charge} of -1 V, V_{DD} begins to decrease rapidly from 3.3 V with negative-going underdamped sinusoidal voltage waveform. During this TLU test, V_{OUT1} and V_{OUT2} are influenced simultaneously by the negative-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of -1 V, the V_{OUT2} of the proposed transient detection circuit also transits from 3.3 V to 0 V.

From the TLU test results, the proposed on-chip SCR-based transient detection circuit can successfully memorize the occurrence of electrical transients. With positive or negative underdamped sinusoidal voltages coupled to V_{DD} power line, the output voltage (V_{OUT2}) of the proposed on-chip SCR-based transient detection circuit can be changed from logic “1” to logic “0” after TLU tests.



(a) (b)

Fig. 3.8 Measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms on the on-chip SCR-based transient detection circuit under TLU tests with the V_{Charge} of (a) +9 V and (b) -1 V.

3.4.2. System-Level ESD Test

In IEC 61000-4-2, two test modes have been specified, which are the air-discharge and contact-discharge test mode. In the case of contact discharge test mode, the sharp discharge tip is used to simulate the mechanical ESD damage on the EUT. The contact discharge is applied to the conductive surfaces of the EUT (direct application) or to the coupling planes (indirect application). Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to the horizontal or vertical coupling planes. Fig. 3.9 shows the measurement setup of the system-level ESD test standard with indirect contact-discharge test mode. The measurement setup of system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series [6]. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from ESD gun will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

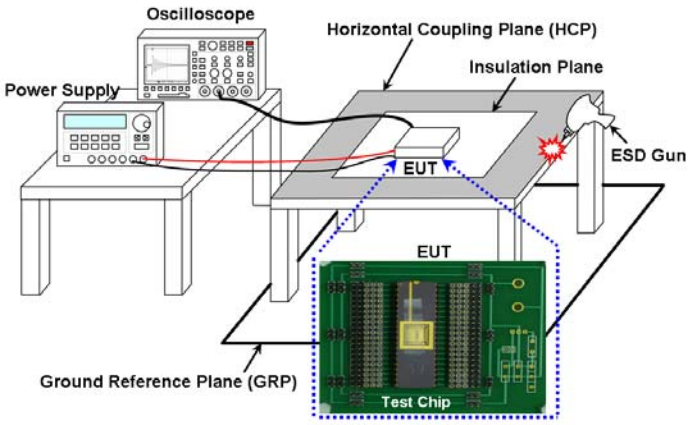


Fig. 3.9 Measurement setup for system-level ESD test with indirect contact-discharge test mode [6] to evaluate the detection function of the on-chip SCR-based transient detection circuit.

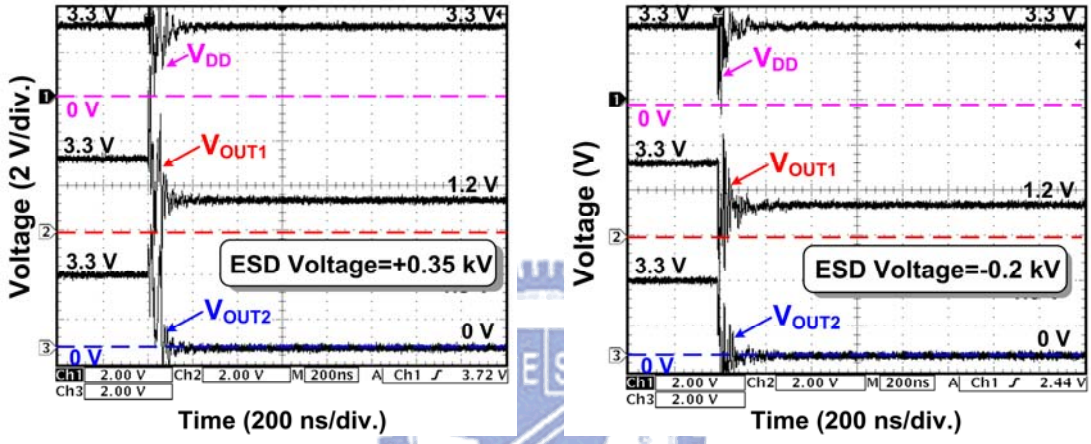
With such measurement setup, the circuit function of the proposed detection circuit after system-level ESD tests can be evaluated. By monitoring the oscilloscope, the transient responses on power lines of CMOS ICs can be recorded and analyzed. Before each system-level ESD test, the initial output voltages (V_{OUT1} and V_{OUT2}) of the proposed detection circuit are all reset to 3.3 V. After each system-level ESD test, the output voltages (V_{OUT1} and V_{OUT2}) are monitored to check their final voltage levels. Thus, the function of the proposed detection circuit can be evaluated under system-level ESD tests.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of +0.35 kV zapping on the HCP are shown in Fig. 3.10(a). V_{DD} begins to rapidly increase from the normal voltage level of 3.3 V. Meanwhile, V_{OUT1} and V_{OUT2} begin to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD}, V_{OUT1}, and V_{OUT2} are influenced simultaneously. Finally, V_{OUT1} is pulled down to 1.2 V. Through buffer stages, V_{OUT2} of the proposed detection circuit transits from 3.3 V to 0 V.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of -0.2 kV zapping on the HCP are shown in Fig.

3.10(b). During the ESD-induced transient disturbance, V_{DD} begins to decrease rapidly from the original voltage level of 3.3 V. Finally, the output voltage (V_{OUT2}) of the proposed transient detection circuit is changed from 3.3 V to 0 V.

Therefore, the new proposed on-chip SCR-based transient detection circuit can successfully detect the electrical transients under system-level ESD tests with positive or negative ESD voltages.



(a) (b)

Fig. 3.10 Measured V_{DD}, V_{OUT1}, and V_{OUT2} transient voltage waveforms of the on-chip SCR-based transient detection circuit under system-level ESD tests with ESD voltage of (a) +0.35 kV and (b) -0.2 kV.

3.4.3. Electrical Fast Transient (EFT) Test

The measurement setup for EFT test combined with attenuation network is shown in Fig. 3.11. EFT generator is connected to the DUT with V_{DD} of 3.3 V through the attenuation network. In order to simulate the degraded EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with -40 dB degradation is used in this work. The amplitude of EFT-induced transients can be adjusted by the attenuation network.

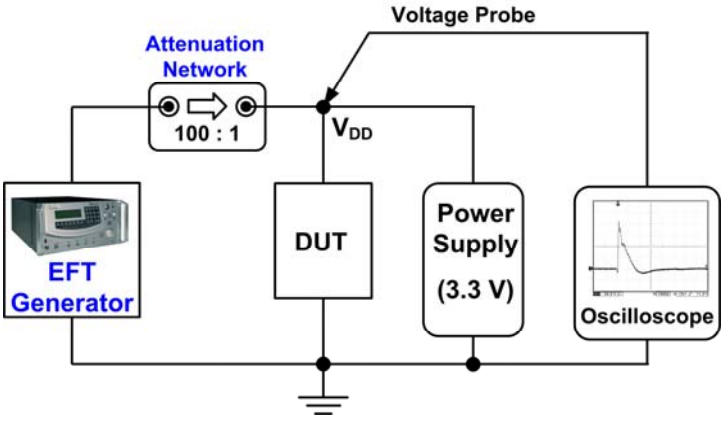
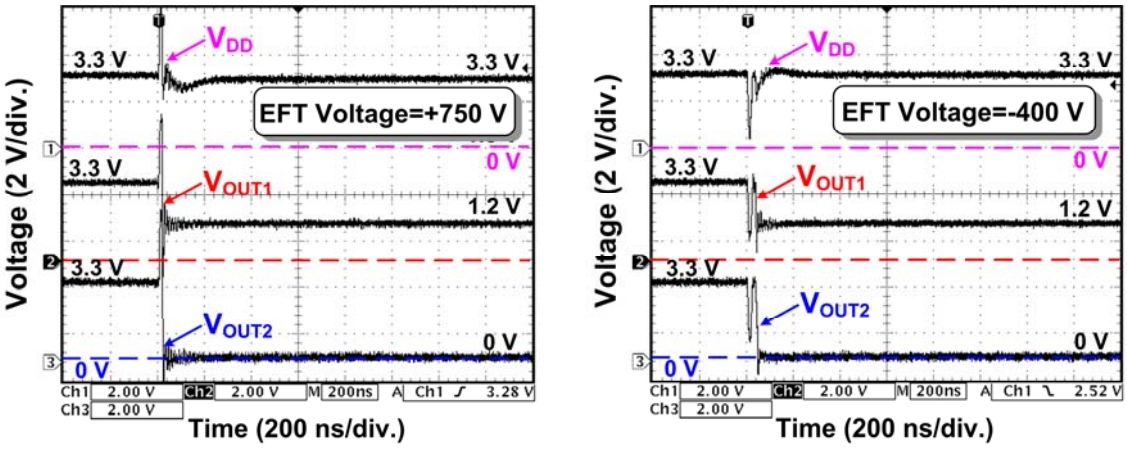


Fig. 3.11 Measurement setup for EFT test combined with attenuation network [9].

Figs. 3.12(a) and 3.12(b) show the measured V_{DD}, V_{OUT1}, and V_{OUT2} transient responses of the proposed detection circuit under the EFT tests with input EFT voltages of +750 V and -400 V, respectively. As shown in Fig. 3.12(a), under the EFT test with positive voltage of +750 V, V_{DD} begins to increase rapidly from 3.3 V with positive exponential voltage pulse. During the EFT test, V_{OUT1} and V_{OUT2} are influenced simultaneously by the positive exponential voltage pulse coupled to V_{DD} power line. After the +750-V EFT test, the output voltage V_{OUT1} (V_{OUT2}) of the proposed detection circuit transits from 3.3 V to 1.2 V (0 V). In Fig. 3.12(b), under the EFT test with negative voltage of -400 V, V_{DD} begins to decrease rapidly from 3.3 V with negative exponential voltage pulse. After the EFT test, the output voltage V_{OUT2} of the proposed detection circuit transits from logic "1" to logic "0".

From the EFT test results shown in Figs. 3.12(a) and 3.12(b), either positive or negative EFT voltages coupled to V_{DD} power line, the output voltage (V_{OUT2}) of the proposed detection circuit can be changed from 3.3 V to 0 V. Therefore, the new proposed on-chip SCR-based transient detection circuit can successfully memorize the occurrence of EFT-induced exponential pulse transient disturbance.



(a) (b)

Fig. 3.12 Measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms on the on-chip SCR-based transient detection circuit under EFT tests with (a) +750-V and (b) -400-V EFT voltages combined with attenuation network.

3.5. Summary

A new on-chip SCR-based transient detection circuit to detect system-level electrical transient disturbance has been implemented in a 0.18-μm CMOS process with 3.3-V devices. By using P_STSCR device and RC-delay circuit, the proposed detection circuit is designed to detect fast electrical transients during the system-level ESD or EFT tests. Experimental results in silicon chip have successfully verified that the proposed detection circuit can successfully memorize the occurrence of electrical transients under system-level ESD or EFT tests. From the previous research, it is reasonable that with hardware/firmware co-design method, the output state of the proposed on-chip SCR-based transient detection circuit can be used as the firmware index to provide an effective solution against the system malfunction caused by system-level electrical transient disturbance.

Chapter 4

Design of On-Chip Transient-to-Digital Converter

4.1. Background

In the previous work [21], on-chip transient-to-digital converter with on-chip noise filters and RC-based transient detection circuit has been designed and fabricated. It has been investigated that the noise filter networks can enhance susceptibility of CMOS ICs to system-level ESD-induced transient disturbance by decoupling, bypassing, or absorbing ESD-induced voltage and energy. With different types of noise filter, the higher order noise filter located between the power and ground lines can provide better bypassing ability to reduce the ESD-induced energy coupled on power lines of CMOS ICs. As shown in Fig. 4.1, the previous on-chip noise filter (1) composed of two resistors and one 10-pF capacitor is used in previous transient-to-digital converter. However, as the technology and the CMOS process scaling down, the large 10-pF capacitor used in the noise filter not only occupies large area but also induces gate leakage current leakage which is not tolerable in deep sub-micron CMOS circuit design. Therefore, to solve these kinds of problems, in this chapter, a new transient-to-digital converter designed with novel type of noise filter and the CR-based transient detection circuit has been proposed and investigated under TLU, EFT, and system-level ESD tests. Under system-level ESD tests, the detection circuit with high-order noise filter would need more ESD coupling energy to change the output logic state; on the other side, the detection circuit with low-order noise filter would be more sensible to ESD disturbance and easily change the output logic state from logic “1” to logic “0”.

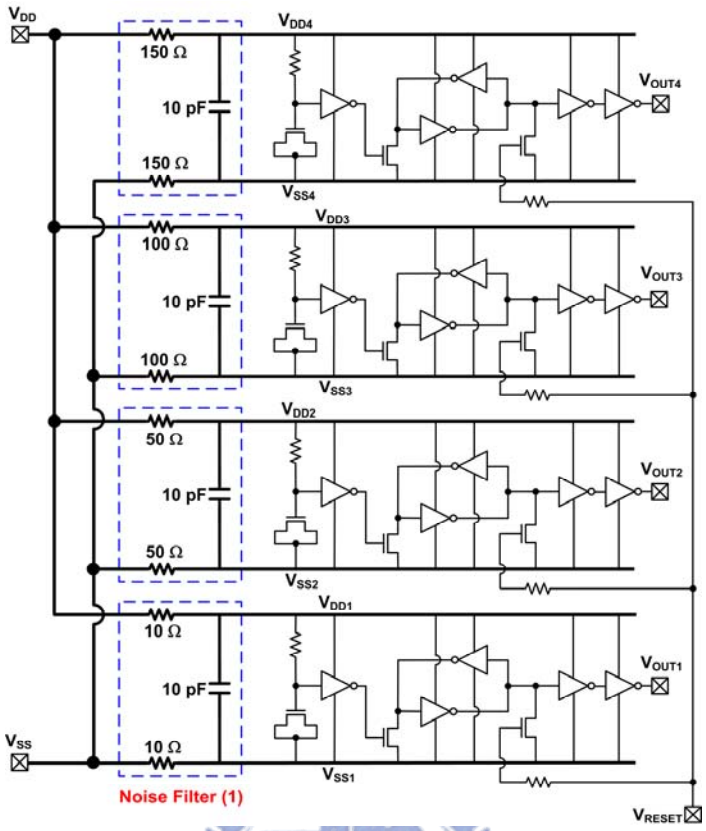


Fig. 4.1 The previous transient-to-digital converter [21].

With these design concepts of transient-to-digital converter, the positive and the negative fast electrical transient voltages under system-level tests can be converted to digital codes by different on-chip noise filter designs. By using the proposed on-chip transient-to-digital converter, the ESD voltage zapped into the CMOS ICs inside the microelectronics product can be quantified as digital codes under system-level ESD tests. Moreover, the output digital codes can be further co-designed with the firmware system to execute total or partial system recovery procedures.

4.2. New On-Chip CR-Based Transient Detection Circuit

4.2.1. Circuit Implementation

Fig. 4.2 shows the new proposed on-chip CR-based ESD detection circuit. The CR-based

circuit structure is designed to realize the transient detection function. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial voltages at node V_{OUT} and node V_A as 1.8 V with the V_{DD} of 1.8 V in a 0.13-μm CMOS process. In Fig. 4.2, the node V_G is biased at V_{SS} during the normal operating condition. Under the system-level ESD stress with an overshooting ESD voltage, the node V_G will be coupled with positive voltage. Then, the NMOS device (M_{n1}) can be turned on by the overshooting ESD voltage to pull down the voltage level at the node V_A. Therefore, the logic level stored at the node V_A can be changed from logic "1" to logic "0" to memorize the ESD-induced transient disturbance. With the buffer inverters, the output voltage is finally changed from 1.8 V to 0 V to detect the occurrence of system-level ESD events. Furthermore, by different combination design of R_1 and R_2, the ESD energy coupled to node V_G can be adjusted. Therefore, the minimum ESD voltage to cause transition at the output (V_{OUT}) of the proposed detection circuit can be designed by this resistive voltage divider technique.

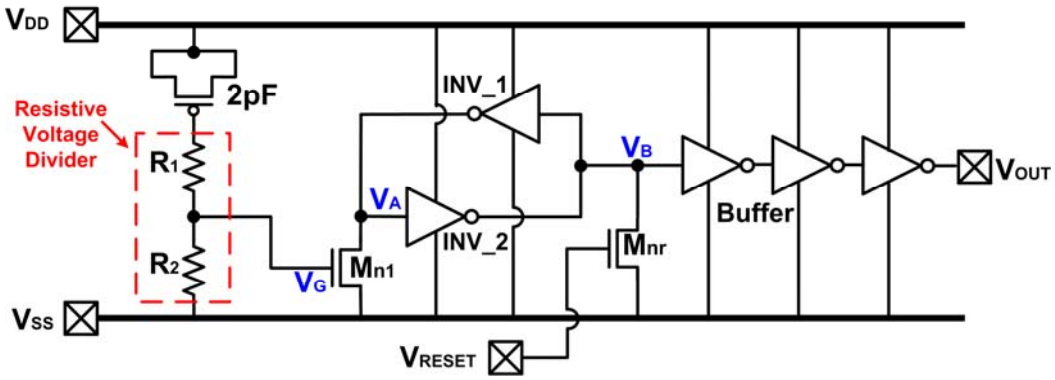


Fig. 4.2 The new proposed on-chip CR-based transient detection circuit.

4.2.2. HSPICE Simulation

It has been investigated that the underdamped sinusoidal voltage waveform has been observed on power line of CMOS IC during the system-level ESD stress. Therefore, a sinusoidal time-dependent voltage source given by

$$V(t) = V_0 + V_a \cdot \sin(2\pi f(t - t_d)) \cdot \exp(-(t - t_d)D_a), \quad (2)$$

is used to simulate ESD-induced transient disturbance coupled on the power lines of the proposed detection circuit. With the proper parameters (including the applied voltage amplitude V_a, initial dc voltage V_0, damping factor D_a = 2x10^7 s^{-1}, frequency f = 50 MHz, and time delay t_d = 300 ns), the underdamped sinusoidal voltage can be used to simulate the electrical transient waveforms under system-level ESD tests.

The simulated V_{DD} and V_{OUT} waveforms of the proposed detection circuit with a positive-going (negative-going) underdamped sinusoidal voltage on V_{DD} line are shown in Fig. 4.3(a) (Fig. 4.3(b)). The positive-going underdamped sinusoidal voltage with amplitude of +3 V (-3 V) is used to simulate the coupling ESD transient noise under the system-level ESD test. From the simulated waveforms, V_{DD} begins to increase (decrease) rapidly from 1.8 V. V_{OUT} also acts with a positive-going (negative-going) underdamped sinusoidal voltage waveform during the simulated system-level ESD events on V_{DD} line. After this disturbance duration, V_{DD} returns to its normal voltage level of 1.8 V and the output state (V_{OUT}) of the detection circuit is changed from 1.8 V to 0 V, as shown in Fig. 4.3(a) (Fig. 4.3(b)). As a result, the detection circuit can detect the occurrence of simulated ESD-induced electrical transients.

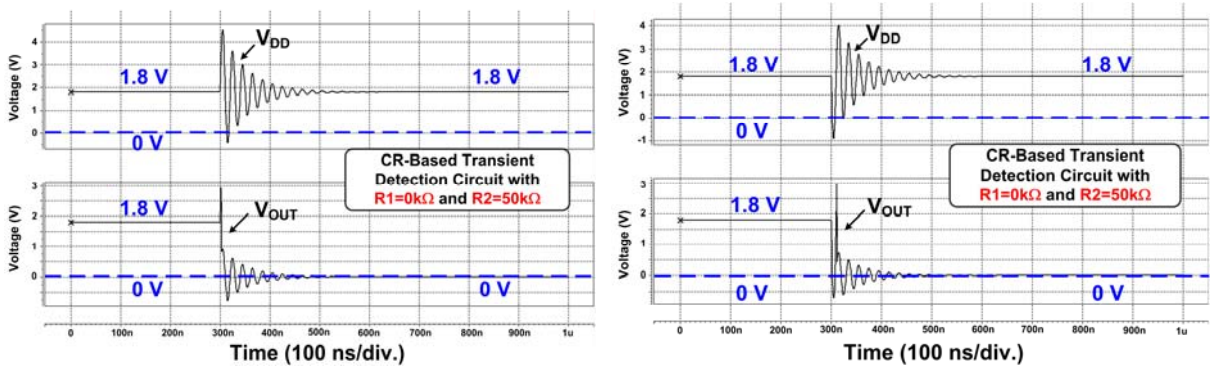


Fig. 4.3 Simulated V_{DD} and V_{OUT} waveforms of the new proposed on-chip CR-based transient detection circuit under system-level ESD test with (a) positive-going, and (b) negative-going, underdamped sinusoidal voltages.

To confirm the minimum V_a voltage, an exponential time-dependent voltage source with rise/fall time constant parameters is used to simulate the EFT-induced transient disturbance on the power lines of CMOS ICs. The rising edge of the exponential voltage pulse is expressed as

$$V_{P1} = V_1 + (V_2 - V_1) \times [1 - \exp(-\frac{Time - t_{d1}}{\tau_1})] \quad \text{, when } t_{d1} \le t \le t_{d2}. \quad (3)$$

The falling edge of the exponential voltage pulse is expressed as

$$V_{P2} = V_1 + (V_2 - V_1) \times [1 - \exp(-\frac{t_{d2} - t_{d1}}{\tau_1})] \times \exp(-\frac{Time - t_{d2}}{\tau_2}) \quad \text{, when } t \ge t_{d2}. \quad (4)$$

With the proper parameters such as rise (fall) time constant τ_1 (τ_2), rise (fall) delay time t_{d1} (t_{d2}), initial DC voltage value V_1, and exponential pulse voltage V_2, the exponential voltage source can be constructed to simulate the EFT-induced disturbance under EFT tests as shown in Fig. 4.4.

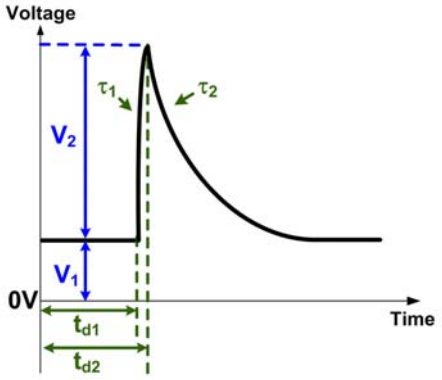
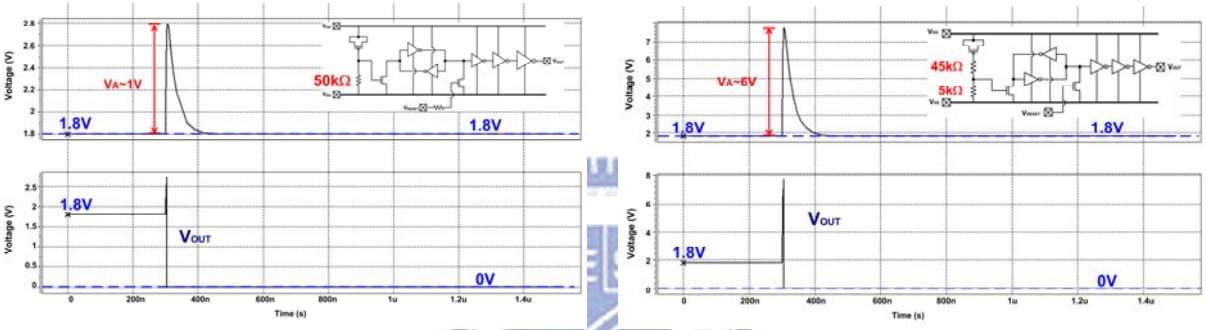


Fig. 4.4 The specific time-dependent exponential pulse waveform applied on the power lines to simulate the disturbance under EFT zapping.

Furthermore, with increasing resistor ratio of R_1/R_2, the ESD energy coupled to node V_G will be decreased and the minimum ESD amplitude ($\equiv V_{a(min)}$) to cause transition of proposed

detection circuit will be increased. Simulation results show that, when R_1 equals to 0 kΩ and R_2 equals to 50 kΩ, minimum V_a voltage to stimulate the detection circuit to transit output from logic high to logic low equals to +3 V, as shown in Fig. 4.5(a). When R_1 increases its value to 45 kΩ and R_2 decreases to 5 kΩ, minimum V_a voltage for circuit transition would increase to +9 V, as shown in Fig. 4.5(b). As a result, the minimum amplitude of simulated EFT pulse to cause circuit transition would be different with different combination in resistive voltage divider techniques, as shown in TABLE XI.



(a) (b)

Fig. 4.5 CR-based transient detection circuit (a) without and (b) with resistor divider.

TABLE IX Simulation results of the minimum EFT amplitude corresponding to different resistor combinations used in resistive voltage divider.

R_1	R_2	The minimum amplitude of EFT pulse to cause transition of detection circuit
0 kΩ	50 kΩ	+3 V
15 kΩ	35 kΩ	+4 V
25 kΩ	25 kΩ	+5 V
35 kΩ	15 kΩ	+6 V
45 kΩ	5 kΩ	+9 V

4.3. Experimental Results

The proposed detection circuit has been designed and fabricated in a 0.13-μm CMOS process. The fabricated chip for transient disturbance tests is shown in Fig. 4.6. The silicon area of the proposed on-chip CR-based detection circuit is 245 μm x 155 μm.

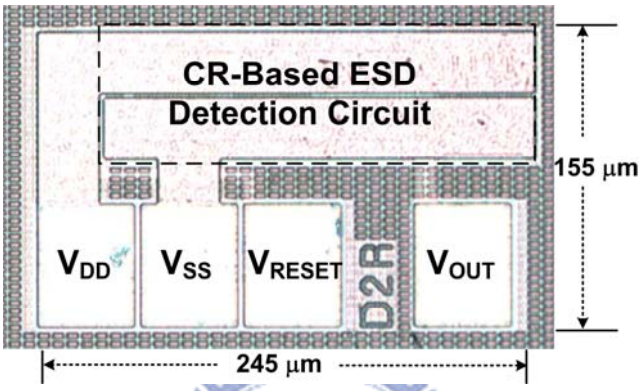


Fig. 4.6 Chip photo of the new proposed on-chip CR-based transient detection circuits fabricated in a 0.13-μm CMOS process.

4.3.1.. Transient-Induced Latchup (TLU) Test

Fig. 4.7 depicts such a component-level transient-induced latchup (TLU) measurement setup on display system. Figs. 4.8(a) and 4.8(b) show the measured V_{DD} and V_{OUT} transient responses of the proposed detection circuit under the TLU test with V_{Charge} of +200 V and -200 V, respectively. As shown in Fig. 4.8(a), under the TLU test with V_{Charge} of +200 V, V_{DD} begins to increase rapidly from 1.8 V with positive-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT} is influenced simultaneously with positive-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of +200 V, the output voltage (V_{OUT}) of the proposed detection circuit can transit from 1.8 V to 0 V. In Fig. 4.8(b), under the TLU test with V_{Charge} of -200 V, V_{DD} begins to decrease rapidly from 1.8 V with negative-going underdamped sinusoidal voltage waveform. During

the TLU test, V_{OUT} is influenced simultaneously with negative-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of -200 V, the output voltage (V_{OUT}) of the proposed detection circuit can transit from 1.8 V to 0 V.

From the TLU test results, the proposed detection circuit can successfully memorize the occurrence of electrical transients coupled on power line of display system. With positive or negative underdamped sinusoidal voltages coupled to 1.8-V power line, the output voltages (V_{OUT}) of the proposed detection circuit can both change from logic“1” to logic“0” after TLU tests.

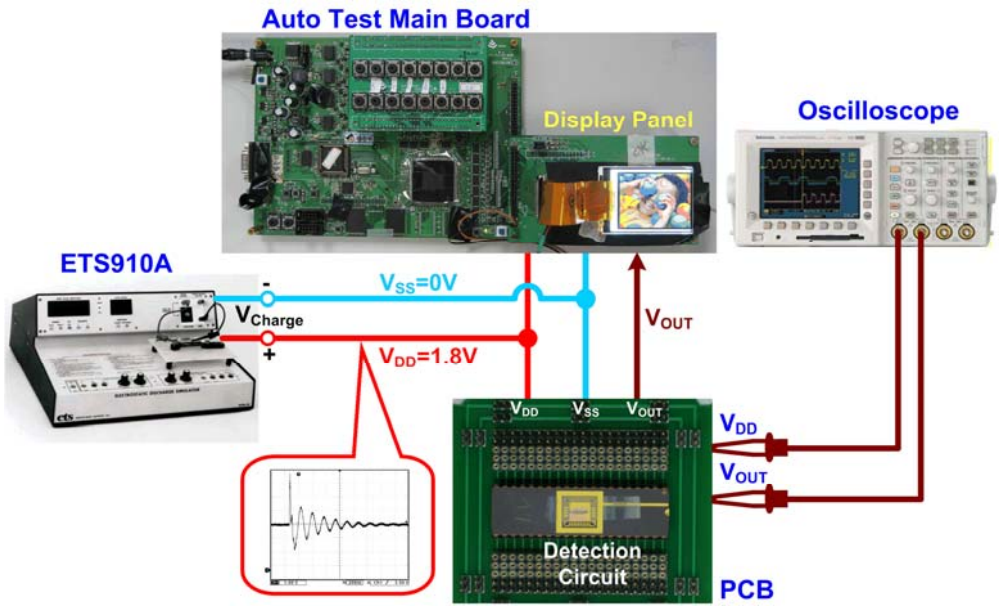
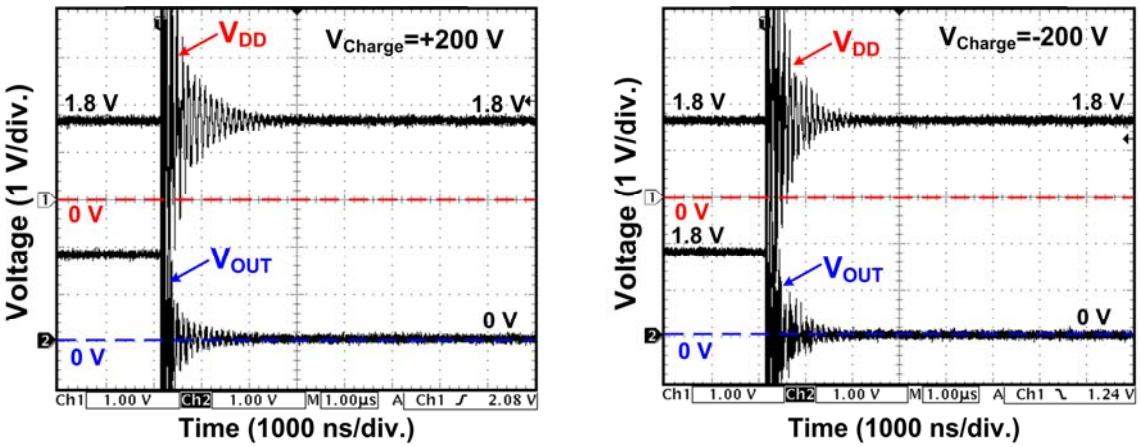


Fig. 4.7 Measurement setup for transient-induced latchup (TLU) test on display panel.



(a) (b)

Fig. 4.8 Measured V_{DD} and V_{OUT} waveforms on the new proposed CR-based transient detection circuit under TLU tests with V_{Charge} of (a) +200 V, and (b) -200 V.

4.3.2. System-Level ESD Test

Fig. 4.9 shows the measurement setup of the system-level ESD test standard with air-discharge test mode in a display system. When the ESD gun is approaching the EUT, the electromagnetic interference (EMI) coming from ESD gun will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

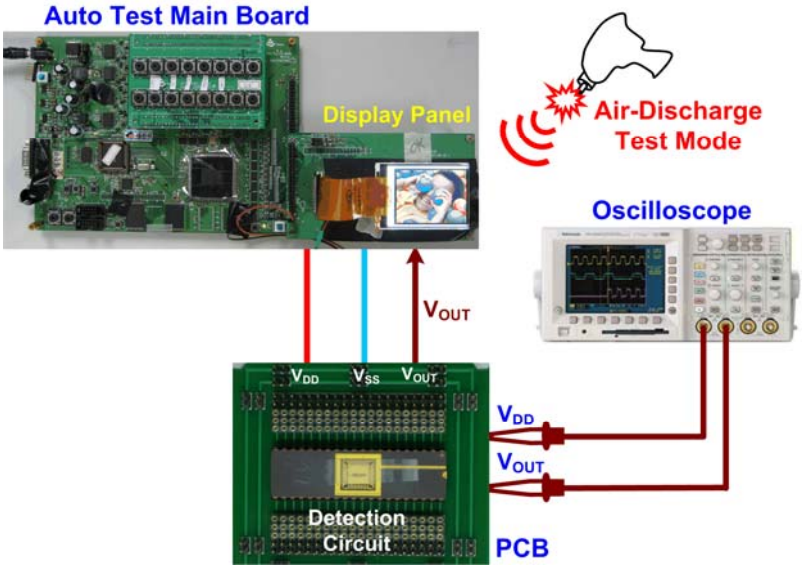


Fig. 4.9 Measurement setup for system-level ESD test with air discharge test mode. [6]

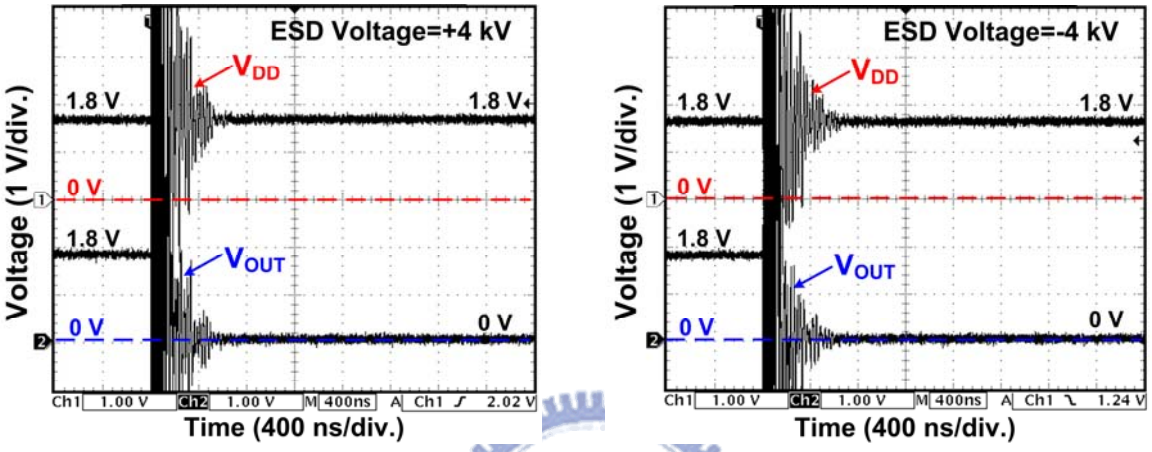
With such a measurement setup shown in Fig. 4.9, the circuit function of the proposed detection circuit after system-level ESD tests can be evaluated. Before each system-level ESD test, the initial output voltage (V_{OUT}) of the proposed detection circuit is reset to 1.8 V. After each system-level ESD test, the output voltage (V_{OUT}) level is monitored to check the final voltage level and to verify the detection function.

The measured V_{DD} and V_{OUT} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of +4 kV are shown in Fig. 4.10(a). V_{DD} begins to increase rapidly from the normal voltage of +1.8 V. Meanwhile, V_{OUT} is disturbed under such a high-energy ESD stress. During the period with positive-going ESD-induced electrical transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, the output voltage (V_{OUT}) of the proposed detection circuit transits from 1.8 V to 0 V. Therefore, the proposed detection circuit can sense the positive-going electrical transient on the power line and memorize the occurrence of positive system-level ESD event.

The measured V_{DD} and V_{OUT} transient voltage waveforms of proposed detection circuit with the ESD voltage of -4 kV under system-level ESD test are shown in Fig. 4.10(b). During the negative-going ESD-induced electrical transient disturbance on V_{DD} power line, V_{OUT} is disturbed simultaneously. After the system-level ESD test with the ESD voltage of -4 kV, V_{DD} returns to the operation voltage level of 1.8 V and V_{OUT} transits from logic“1” to logic“0.” The detection function of the proposed on-chip detection circuit after the system-level ESD tests has been verified by both the experimental results in silicon chip and HSPICE simulation.

Experimental results show that when the ESD gun zaps with air-discharge test mode, all the CMOS ICs inside the equipment under test (EUT) would be disturbed due to ESD-coupled energy. Under the normal operation, the display panel can continuously show the correct information composed of red, green, and blue display signals, as shown in Fig. 4.11(a).

With coupling electrical transient disturbance under system-level ESD test, the display panel is locked in a frozen state, as shown in Fig. 4.11(b). For advanced system-level ESD verification on industrial display products, 9 zapping locations are defined on display panels with air-discharge test mode, as shown in Fig. 4.12.



(a) (b)

Fig. 4.10 Measured V_{DD} and V_{OUT} transient voltage waveforms of the new proposed detection circuit under system-level ESD tests with ESD voltage of (a) +4 kV, and (b) -4 kV.

(a) (b)

Fig. 4.11 Measurement results of display system under (a) normal operation, and (b) system-level ESD test.

Fig. 4.12 Test points definition on display panel under system-level ESD tests with air-discharge test mode.

TABLE X

Measured Results of Display Panel Without And With System Hardware/Firmware Co-Design

Zapping Location	ESD Zapping Voltage = +4 kV		ESD Zapping Voltage = -4 kV	
	W/o System Hardware/Firmware Co-Design	With System Hardware/Firmware Co-Design	W/o System Hardware/Firmware Co-Design	With System Hardware/Firmware Co-Design
#1	Class C	Class B	Class C	Class B
#2	Class C	Class B	Class B	Class B
#3	Class C	Class B	Class C	Class B
#4	Class C	Class B	Class C	Class B
#5	Class A	Class A	Class B	Class B
#6	Class C	Class B	Class C	Class B
#7	Class C	Class B	Class C	Class B
#8	Class C	Class B	Class C	Class B
#9	Class C	Class B	Class C	Class B

In the IEC 61000-4-2 standard, for microelectronic products after system-level ESD zapping, class A, class B, and class C denote normal performance, automatic recovery, and manual recovery, respectively. By using the output digital codes as the firmware index, the display panel can automatically recover all electrical functions to successfully release the locked or frozen states caused by system-level ESD transient disturbance. TABLE X shows the comparison among measured results between display panel without and with system hardware/firmware co-design via the proposed detection circuit. The display system criterion

can be improved from “class C” to “class B” to meet the typical specifications of commercial microelectronic products.

4.4. Transient-to-Digital Converter

4.4.1. Circuit Implementation

The new proposed on-chip transient-to-digital converters composed of two circuit blocks, the on-chip noise filter and the CR-based transient detection circuit blocks. In order to reduce capacitor size used in noise filter (1), as shown in Fig.4.1, the current amplification technique in proposed active clamp has been investigated [22]. The active clamp circuit is shown in Fig. 4.13. A current mirror with current-gain device width ratio of N is used to multiply the capacitance (C_1). The current through the node V_x is multiplied N+1 times, thus allowing the capacitor C_1 to increase by a factor of N+1 to achieve desired RC_1 time constant. Numerical computation shows the same result as following:

$$I_i = I_c + NI_c = I_c(N+1)$$

The impedance (Z) from node V_x to ground is

$$Z = \frac{V_x}{I_i} = \frac{I_c \cdot \frac{1}{SC_1}}{I_c \cdot (1+N)} = \frac{1}{SC_1(1+N)} = \frac{1}{SC_{eq}}$$

$$\Rightarrow C_{eq} = C_1(1+N) \tag{4}$$

By using current amplification concept in Fig. 4.13, the 3-pF capacitor designed with current mirror circuit can be used to replace 10-pF capacitor in noise filter (1). Therefore, with different device width ratio of M_{N2} over M_{N1} (≡N), different equivalent capacitance used in noise filters were implemented to bypass or absorb the electrical transient disturbance energy.

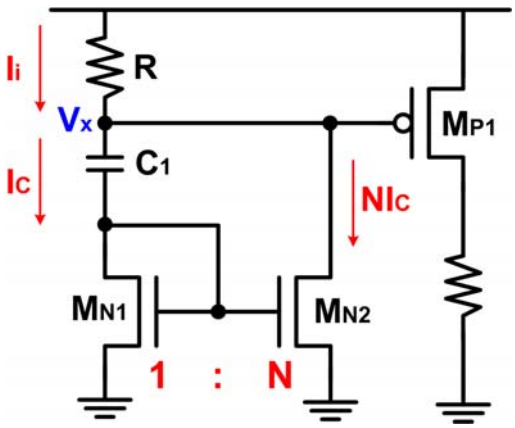
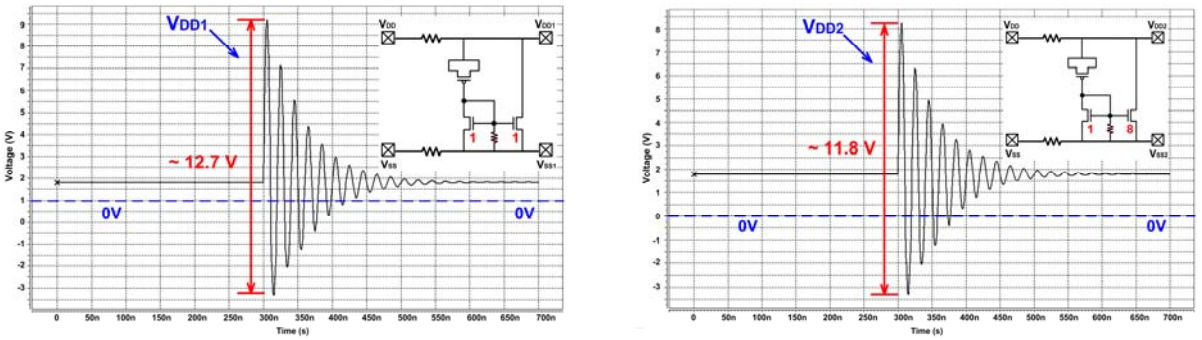


Fig. 4.13 Schematics of the active clamp [22].

Using HSPICE tool and the parameters mentioned in equation (2), when V_{DD} was disturbed by underdamped sinusoidal voltages, the ESD-induced energy coupled on power lines can be different with different current-gain device width ratios. Simulation results are shown in Fig. 4.14. The device width ratio in Fig. 4.14(a) equals to 1 (=1:1), whereas that in Fig. 4.14(b) is 8 (=1:8). When the amplitude of zapping underdamped sinusoidal voltages is 9 V, the peak-to-peak amplitude of transient waveform coupled on Fig. 4.14 (a) (Fig. 4.14 (b)) can be decreased to 12.7 V (11.8 V). Simulation results show that when the current-gain device width ratios increase, the effective capacitance between power lines can be increased due to current magnification. Above all, the transient-to-digital converter consists of four different noise filters and four CR-based transient detection circuits with resistive voltage divider. Therefore, for 4-bit transient-to-digital converter design, the energy coupled into power line of each detection circuit can be different by combining four different current-gain device width ratios.



(a) (b)

Fig. 4.14 Simulation results of the noise filters with different M_{N2} over M_{N1} device ratios of (a) 1:1 and (b) 1:8.

The schematic of the proposed 4-bit transient-to-digital converter is shown in Fig. 4.15. Four different noise filters (2) with 3-pF on-chip capacitor and four different current amplifier designs are used to provide noise filter function under TLU, EFT, and system-level ESD tests. For four current amplifiers, the current-gain device width ratios are ranging from 1:1 to 1:8. The CR-based detection circuit with four different resistive voltage divider designs can adjust ESD level to cause output signal transition in advance. Therefore, with resistive voltage divider and capacitance multiplier techniques, the detection circuit combined novel noise filter design can decrease the suppressed ESD-induced energy coupled on power lines of CMOS ICs and adjust the minimum amplitude to trigger transition of CR-based detection circuit. When the ESD disturbance happened, the outputs of four CR-based transient detection circuits would be influenced simultaneously, but the transient disturbance affected on the power lines of each detection circuit is different owing to the different current-gain device width ratios and R_1/R_2 resistor ratios. By suppressing transient disturbance coupled on internal power lines into different levels, the four detection circuit would have different output voltage responses. Therefore, the system-level ESD-induced energy can be further converted into digital codes and correspond to different quantities of ESD stresses coupling into the CMOS ICs under system-level ESD tests.

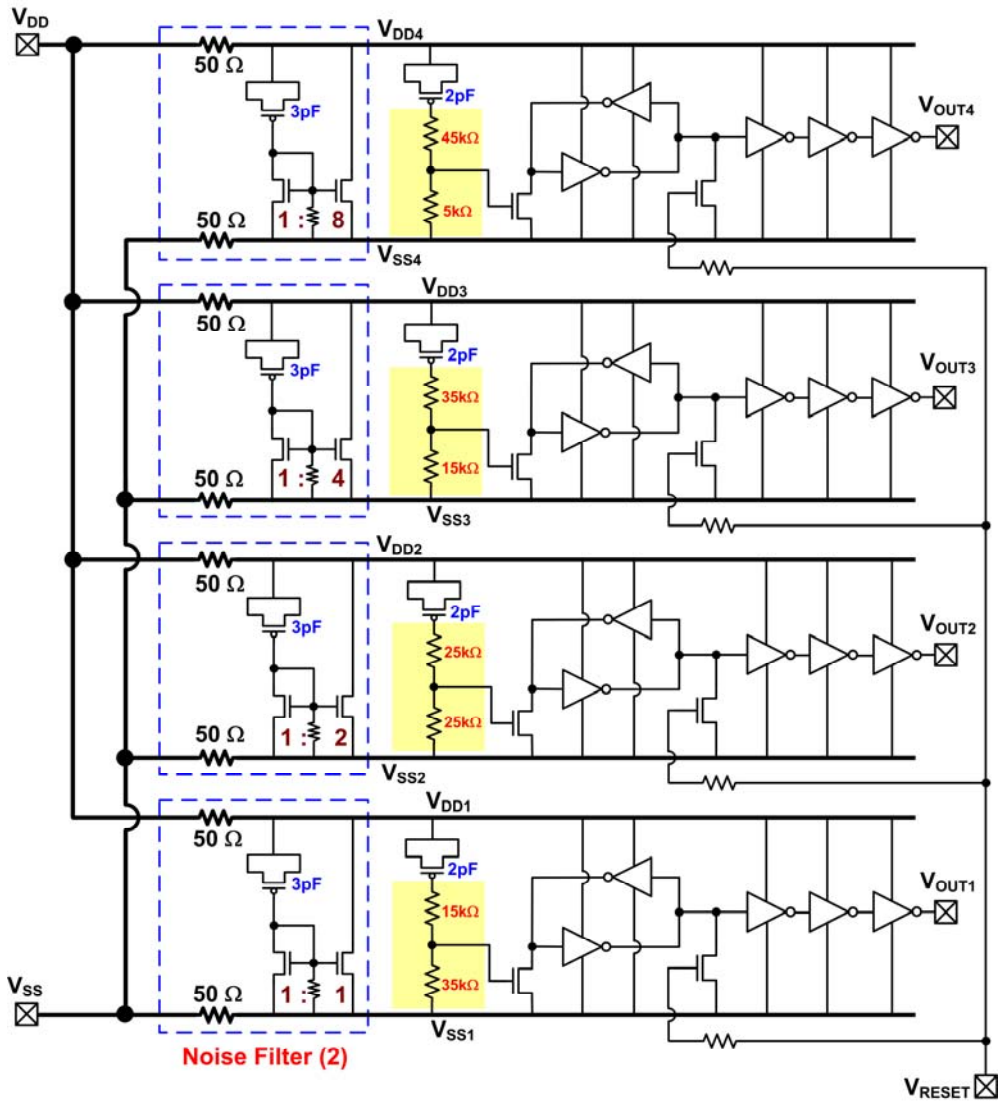


Fig. 4.15 Schematic of the proposed 4-bit transient-to-digital converters.

4.4.2. Experimental Results

The layout of proposed on-chip 4-bit transient-to-digital converter is consisted of four unit cells of CR-based detection circuit and different on-chip noise filter networks. The silicon area is 600 μm x 600 μm, as shown in Fig. 4.16.

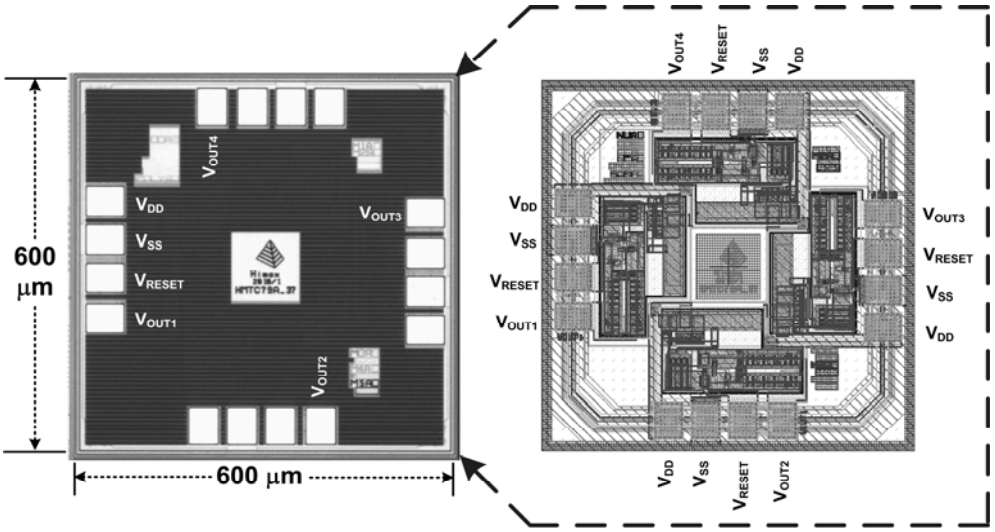


Fig. 4.16 Chip photo and layout of the proposed 4-bit transient-to-digital converter realized in a 0.13-μm CMOS process. (This project is supported by Himax Technologies Inc.)

System-level ESD gun, TLU, and EFT tests were used to verify the circuit performance of the proposed on-chip 4-bit transient-to-digital converter. The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD with positive ESD voltage of +0.7 kV are shown in Fig. 4.17 (a). When the power and ground lines of transient-to-digital converter are affected by ESD stress under system-level ESD test, V_{OUT1}, V_{OUT2}, V_{OUT3} and V_{OUT4} are influenced simultaneously. Due to the different noise suppression by on-chip noise filters and the required noise amplitude enhancement by resistive voltage divider, V_{OUT1} is changed from 1.8 V to 0 V, and V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at 1.8 V. Therefore, for the proposed converter, +0.7-kV system-level ESD zapping can be successfully converted into digital code "1110."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD with positive ESD voltage of +0.8 kV are shown in Fig. 4.17 (b). When the power and ground lines of transient-to-digital converter are affected by ESD stress under system-level ESD test, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced at the same time. V_{OUT1} and V_{OUT2} are changed from 1.8 V to 0 V, and V_{OUT3} and V_{OUT4} are still kept their initial voltage of 1.8 V. Therefore, +0.8-kV system-level ESD zapping can be

successfully converted into digital code “1100.”

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD with positive ESD voltage of +1.0 kV are shown in Fig. 4.17 (c). When the power and ground lines of transient-to-digital converter are affected by ESD stress under system-level ESD test, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. V_{OUT1}, V_{OUT2}, and V_{OUT3} are changed from 1.8 V to 0 V and V_{OUT4} are still kept at initial voltage of 1.8 V. Therefore, +1.0-kV system-level ESD zapping can be successfully converted into digital code “1000.”

Furthermore, the measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD with positive ESD voltage of +1.3 kV are shown in Fig. 4.17 (d). When the power and ground lines of transient-to-digital converter are affected by ESD stress under system-level ESD test, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are all changed from 1.8 V to 0 V. Therefore, the +1.3-kV system-level ESD zapping can be successfully converted into digital code “0000.”

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} voltage waveforms of the proposed transient-to-digital converter under system-level ESD test with ESD voltage of -0.2 kV are shown in Fig. 4.18(a). During the fast transient of ESD stress, all transient detection circuits are affected by ESD-induced transient disturbance coupled on V_{DD} line. Finally, V_{OUT1} transits from logic “1” to logic “0” while V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at logic “1” states. Therefore, the -0.2-kV system-level ESD zapping can be successfully converted into digital code “1110.”

Similarly, under system-level ESD tests with ESD voltages of -0.3 kV, -0.6 kV, and -1.1 kV, the transferred digital codes generated by proposed 4-bit transient-to-digital converter are “1100,” “1000,” and “0000”, as shown in Figs. 4.18(b)-(d). Similarly, the same trends of the digital code transformation have been observed under TLU tests and EFT tests. When the

transient disturbed energy goes larger, the output of the transient-to-digital can transfer into the codes of “1110,” “1100,” “1000,” to “0000” in order. Measurement results of TLU (EFT) tests with positive and negative voltage levels are shown in Fig. 4.19 and Fig. 4.20 (Fig. 4.21 and Fig. 4.22), respectively. The completed measured results of transient-to-digital converter under system-level ESD test, TLU test, and EFT test are listed in TABLE XI. From the measurement results, the detection and response time of the proposed converter is about 300 ns.

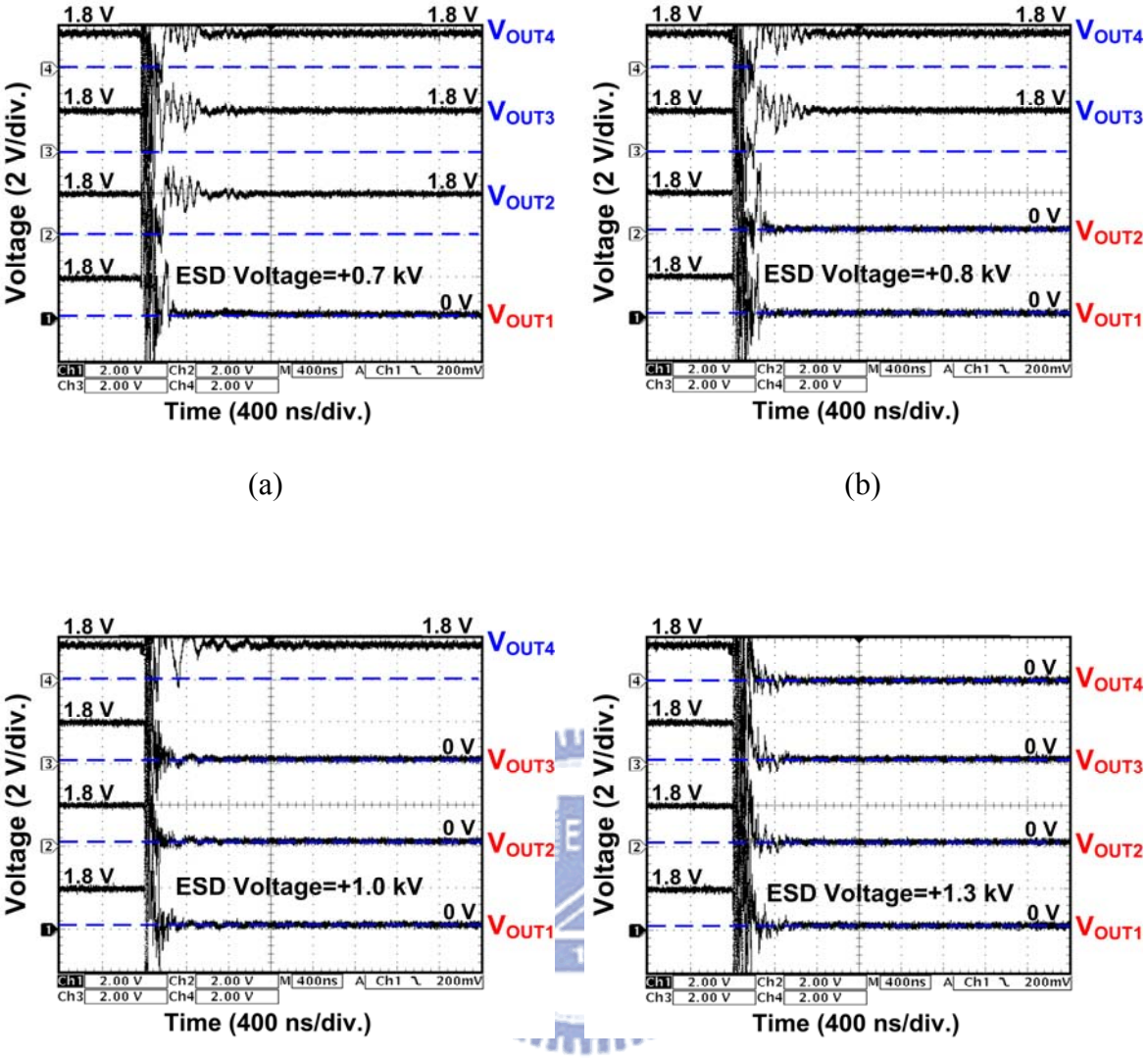


Fig. 4.17 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under positive system-level ESD tests with ESD voltage of (a) +0.7 kV, (b) +0.8 kV, (c) +1.0 kV, and (d) +1.3 kV.

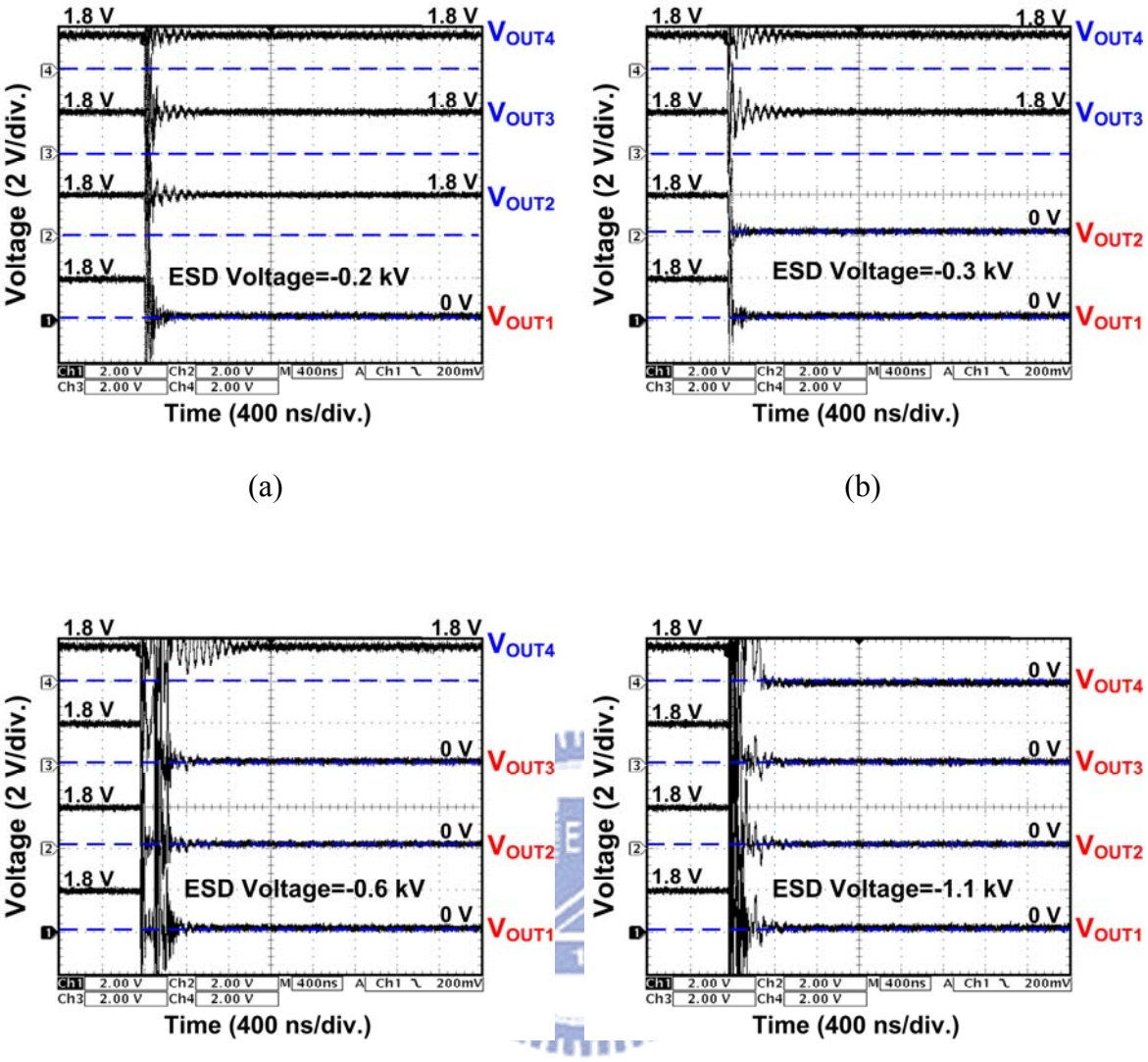


Fig. 4.18 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under negative system-level ESD tests with ESD voltage of (a) -0.2 kV, (b) -0.3 kV, (c) -0.6 kV, and (d) -1.1 kV.

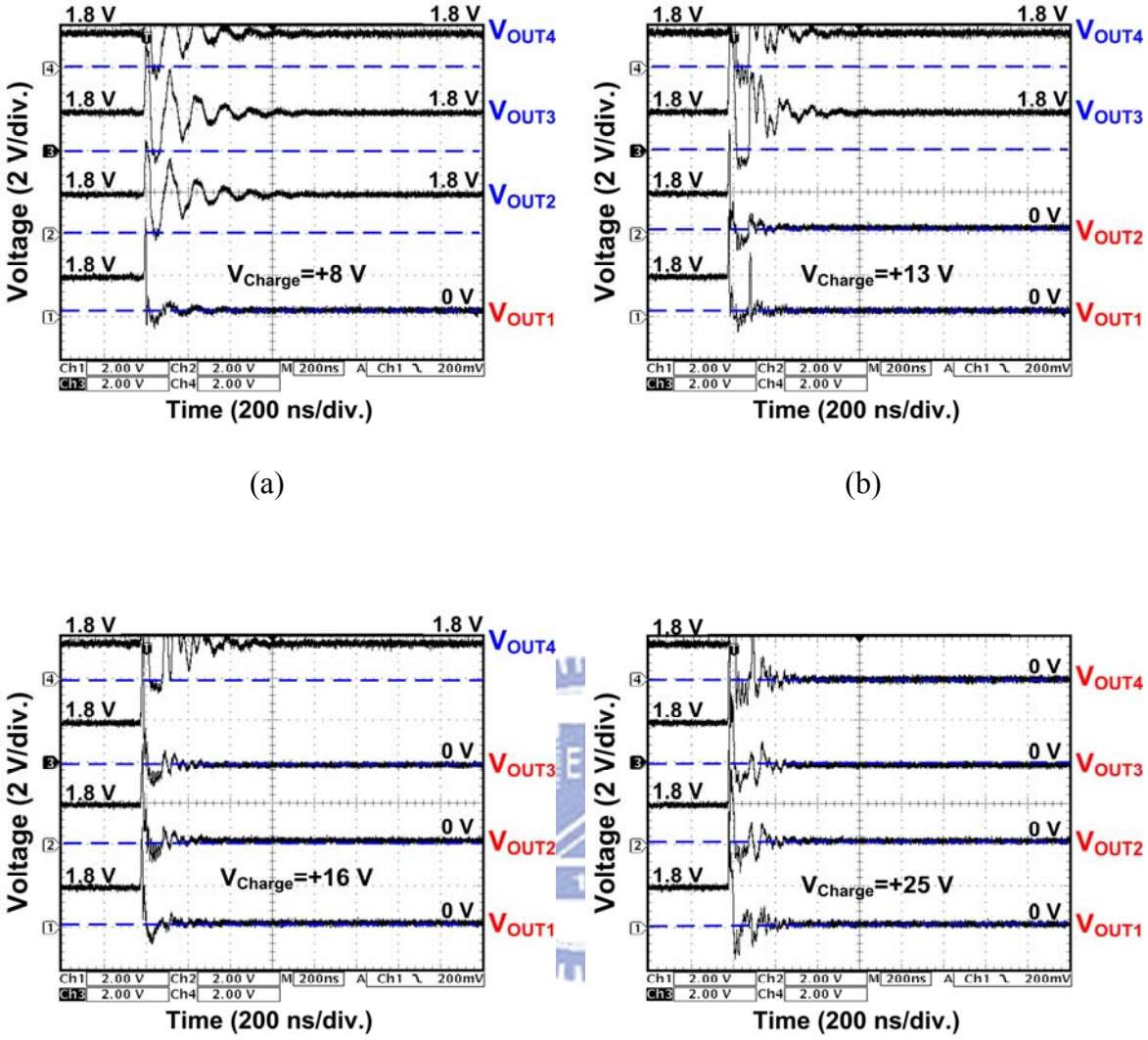


Fig. 4.19 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under positive TLU tests with V_{Charge} of (a) +8 V, (b) +13 V, (c) +16 V, and (d) +25 V.

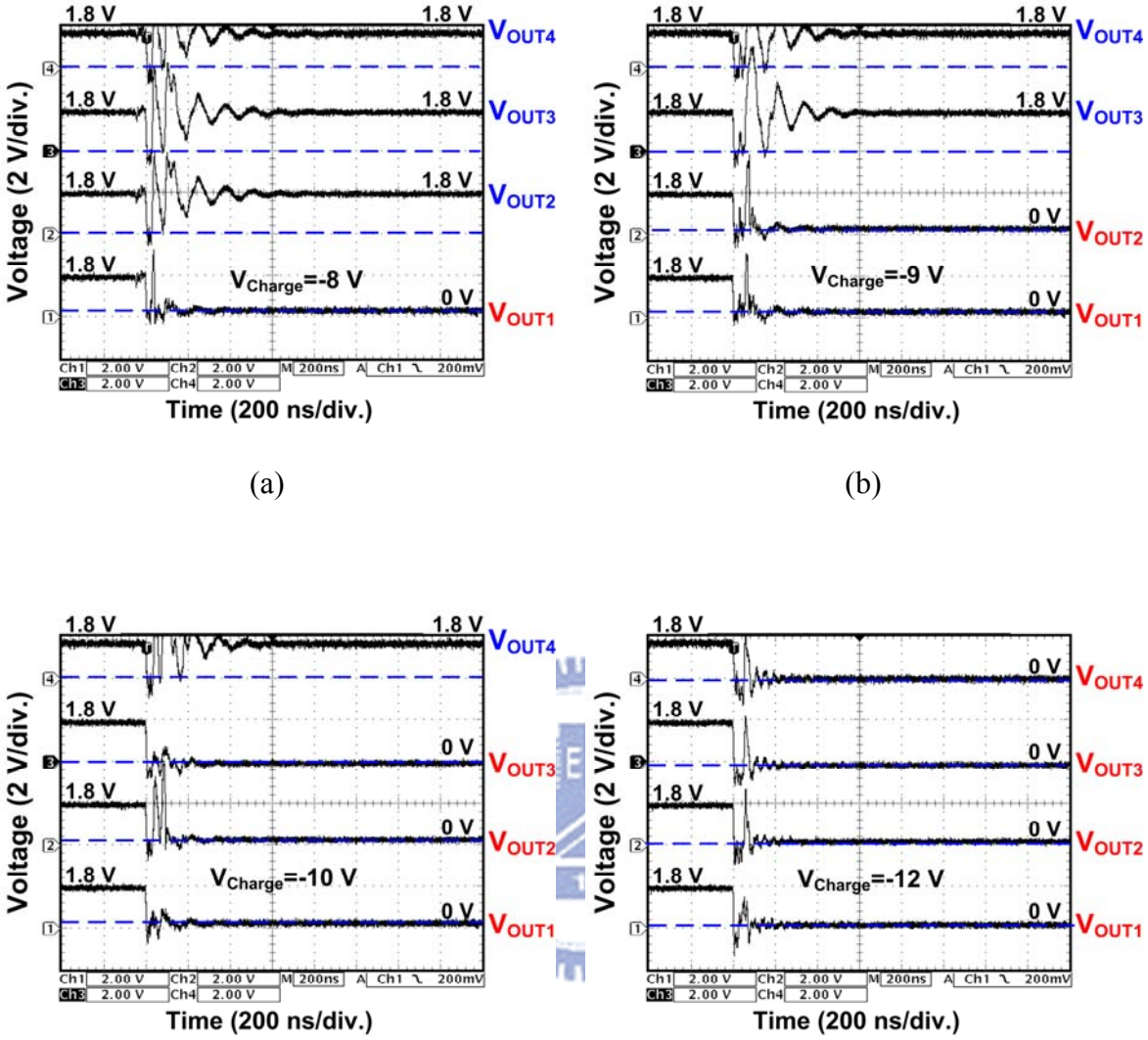


Fig. 4.20 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under negative TLU tests with V_{Charge} of (a) -8 V, (b) -9 V, (c) -10 V, and (d) -12 V.

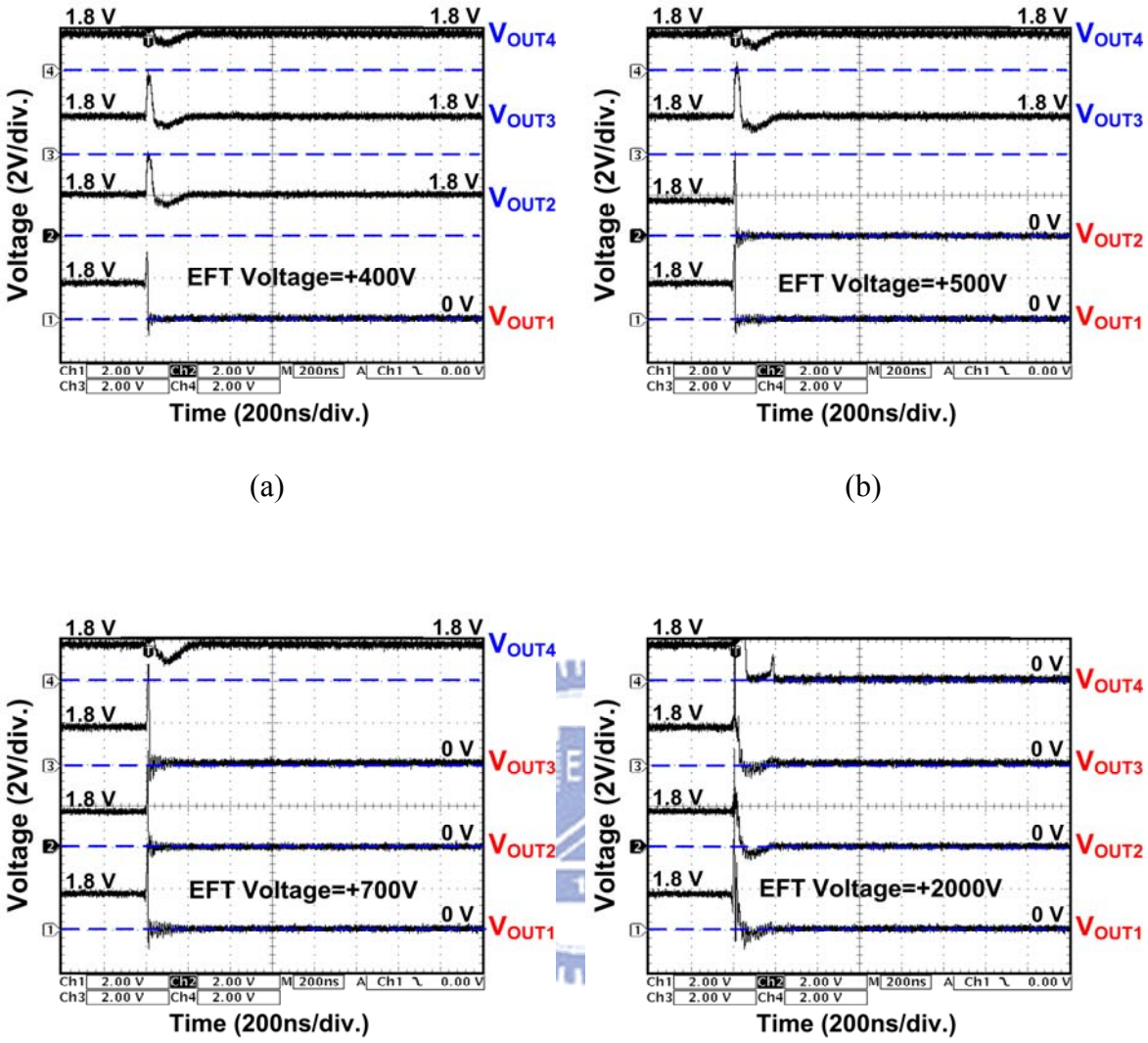


Fig. 4.21 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under positive EFT tests with EFT voltage of (a) +400 V, (b) +500 V, (c) +700 V, and (d) +2000 V.

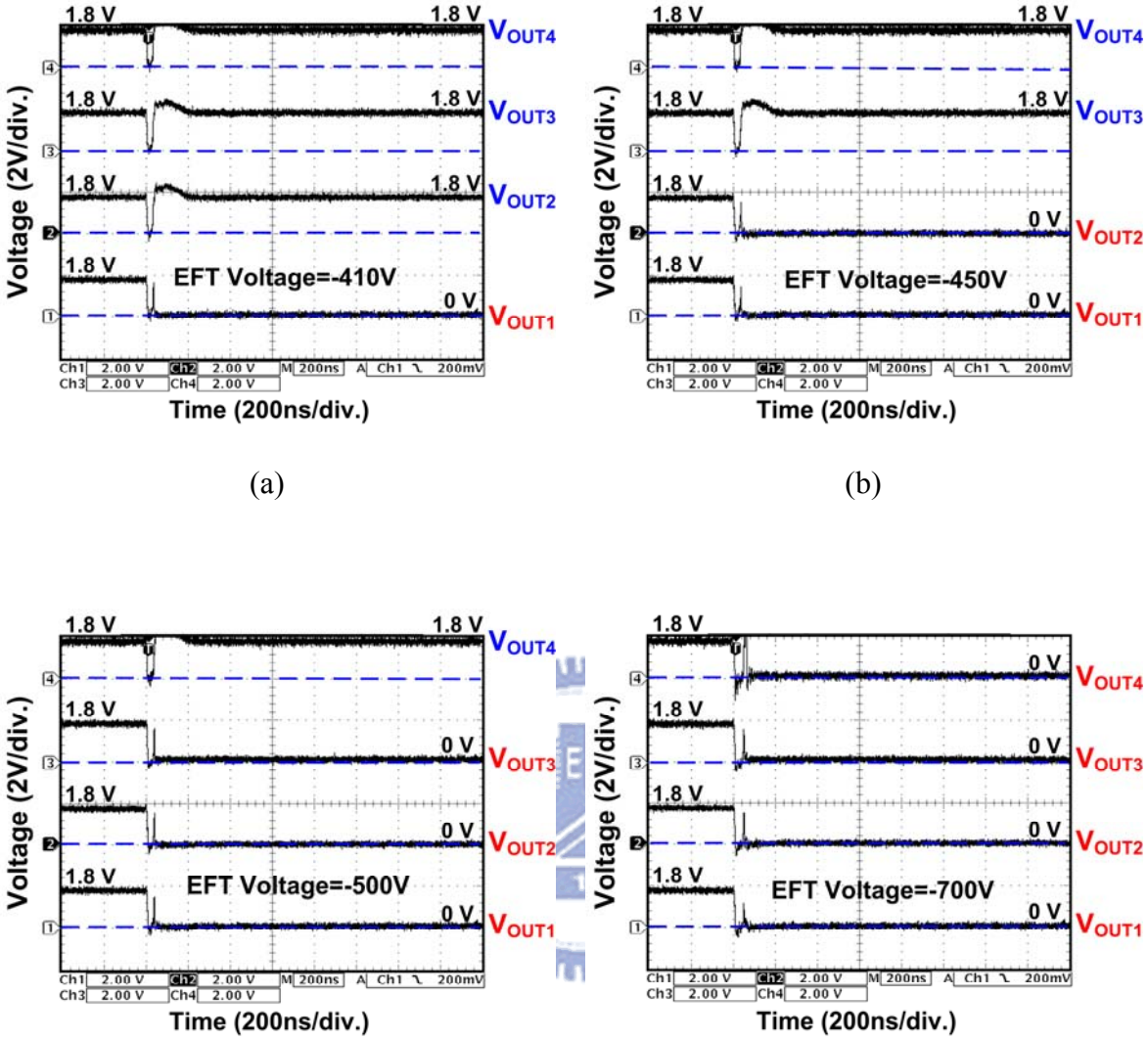


Fig. 4.22 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under negative EFT tests with EFT voltage of (a) -410 V, (b) -450 V, (c) -500 V, and (d) -700 V.

TABLE XI
Measurement results of digital codes corresponding to transient voltages under system-level ESD, TLU, and EFT tests.

Digital Code	ESD Gun		TLU		EFT	
	Positive ESD Voltage (kV)	Negative ESD Voltage (kV)	Positive V_{Charge} (V)	Negative V_{Charge} (V)	Positive EFT Voltage (kV)	Negative EFT Voltage (kV)
1111	< 0.7	> -0.2	< +8	> -8	< 0.4	> -0.41
1110	0.7 ~ 0.8	-0.2 ~ -0.3	+8 ~ +13	-8 ~ -9	0.4 ~ 0.5	-0.41~-0.45
1100	0.8 ~ 1.0	-0.3 ~ -0.6	+13 ~ +16	-9 ~ -10	0.5 ~ 0.7	-0.45 ~ -0.5
1000	1.0 ~ 1.3	-0.6 ~ -1.1	+16 ~ +25	-10 ~ -12	0.7 ~ 2.0	-0.5 ~ -0.7
0000	> 1.3	< -1.1	> +25	< -12	> 2.0	< -1.1

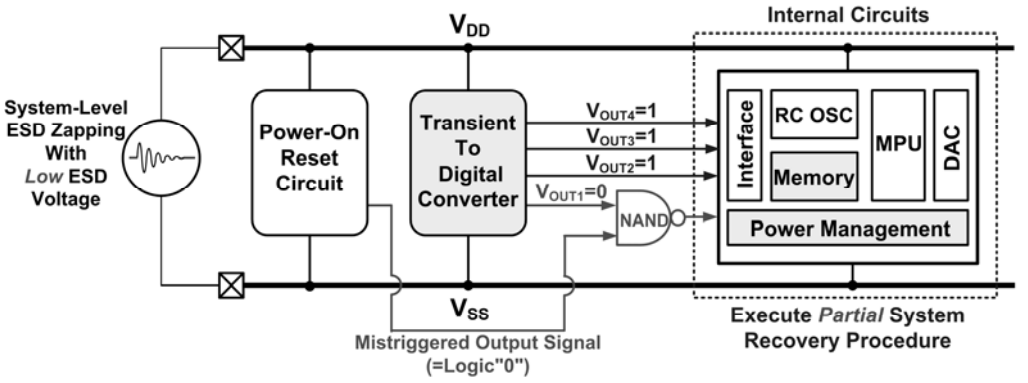
4.4.3. Hardware/Firmware Co-Design

To perform the hardware/firmware co-design, the digital codes from transient-to-digital converter can be temporarily stored as system recovery index for firmware check. The display system can be programmed to execute different recovery procedures according to different digital codes with the consideration of system recovery time and energy saving.

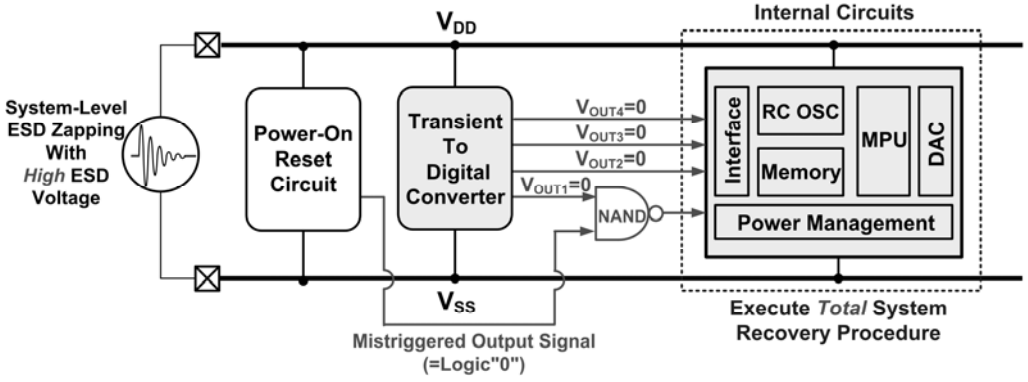
At the beginning, the output digital code is set as “1111.” When the electrical transients happen, the transient-to-digital converter can detect the occurrence of system-level electrical transient disturbance and transfer the ESD voltage levels into digital codes. At this moment, the firmware index is also changed to initiate system recovery procedure to restore system to a known stable state as soon as possible. According to different digital codes, the firmware can program corresponded system recovery procedures. For example, under system-level ESD test with low ESD voltage zapping, the transferred digital code is “1110” and the firmware can execute partial system recovery procedure in display panel, as shown in Fig. 4.23(a). With high ESD zapping, the transferred digital code is “0000” and the firmware can execute total

system recovery procedure, as shown in Fig. 4.23(b).

For system initial state setting, the power-on reset circuit can further design into hardware/firmware co-design to set the initial digital code into "1111." However, there are some mis-triggered conditions for power-on reset circuit. For example, a sudden surge can result in a very short interval between the power-down and power-up transitions. Such short interval of power-off creates difficult situations for some power-on reset circuits to work properly. Therefore, the NAND logic gate circuit can be further added into the hardware/firmware co-design flow. The V_{OUT1} signal of transient-to-digital converter and the output signal of power-on reset circuit are connected as the input signals of NAND logic gate. When electrical transient disturbance happens, the system recovery procedure can be still initiated to protect microelectronic display products against the electrical transitions caused by system-level ESD events.



(a)



(b)

Fig. 4.23 Hardware/firmware operation in display panel system during (a) low, and (b) high system-level ESD zapping conditions.

4.5 Summary

The new proposed on-chip 4-bit transient-to-digital converter composed of noise filter networks and CR-based transient detection circuits has been designed and fabricated in a 0.13-μm process with 1.8-V devices. By using on-chip noise filter to reduce the transient disturbance voltage on the power and ground lines of CMOS ICs, the minimum system-level ESD voltage to cause transition at outputs of four transient detection circuits can be adjusted. From the measurement results, the proposed on-chip transient-to-digital converter can successfully detect and transfer electrical transient energy into digital codes under TLU, EFT, and system-level ESD tests. Furthermore, these output digital codes can be used as the firmware index to execute different auto-recovery procedures of industrial products. Compared to the previous work shown in Fig. 4.1, the new proposed transient-to-digital converter can reduce the silicon area and still provide the output digital codes corresponding to different ESD-induced/ EFT-induced transient disturbance.

Chapter 5

Conclusions and Future Works

5.1. Conclusions

In this thesis, new on-chip SCR-based transient detection circuit has been proposed in chapter 3. The transient detection circuit has been fabricated in a 0.18-μm CMOS process with 3.3-V devices. The circuit performances have been investigated under TLU, EFT, and system-level ESD tests. The output voltage level of on-chip transient detection circuit can transit from logic "1" to logic "0" when fast electrical transient disturbance coupled on power lines of CMOS ICs.

The output digital code can be further co-designed with the hardware/firmware to execute the system automatically recovery procedure. This co-design technique has also been confirmed with the display system. Without the transient detection circuit, display panel would be locked at frozen state when system-level ESD events happened. In this study, with the transient detection circuit, the display system could auto-recover from upset state to the normal operation when fast electrical transient voltage disturbed the power lines. Equivalently, display system can achieve the criterion of "class B" level in the IEC 61000-4-2 standard when co-working with the transient detection circuit.

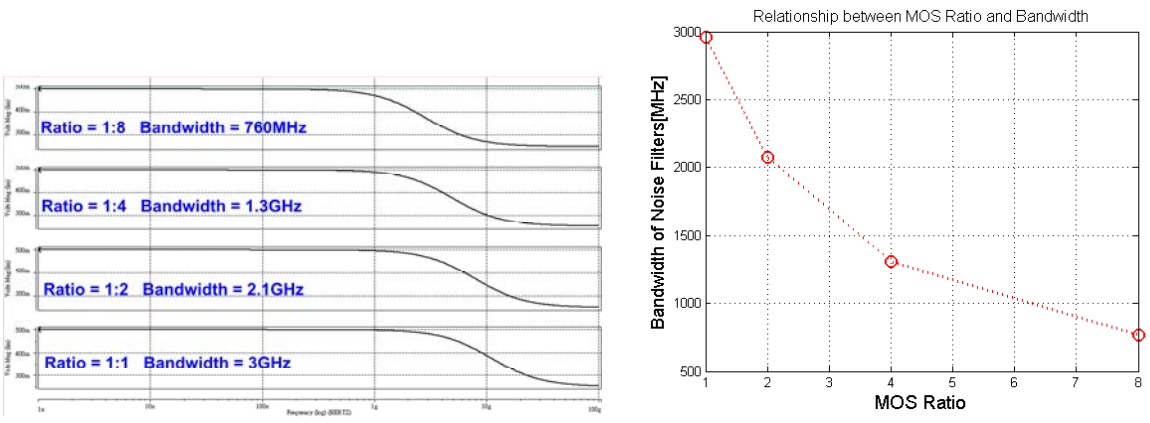
In chapter 4, a novel proposed on-chip transient-to-digital converter composed of four different filters and four CR-based transient detection circuits has been designed and fabricated in a 0.13-μm CMOS process with 1.8-V devices. By using the current mirror amplification techniques, the value of capacitor used in on-chip noise filter can be reduced. Furthermore, with the resistive voltage divider used in the CR-based transient detection circuit, the output detection range of each detection circuits can be further adjusted. From the

measurement results, the proposed on-chip transient-to-digital converter can successfully detect and transfer different ESD voltages into digital codes under TLU, EFT, and system-level ESD tests.

5.2. Future Works

It has been investigated that, for the SCR devices, different triggering methods and layout parameters would have different triggered voltage. Based on this characteristic, for the SCR-based transient detection circuit, it is possible to realize the transient-to-digital converter by using the different types of SCR device and without the noise filter networks. This would save more chip area and avoid the leakage problem for MOS capacitors in deep-submicron technology.

For the transient-to-digital converter, the voltage interval between two adjacent digital codes should be increased to further distinguish the different ESD voltages. For example, the detection level could be enhanced to meet the test level specified in the IEC 61000-4-2 standard. Furthermore, simulations of frequency response with different noise filter are shown in Fig. 5.1.



(a) (b)

Fig. 5.1 Frequency simulation results of noise filters (a) noise filters and (b) linear plot.

And compared with the measurement results, Fig. 5.2 shows relationship between the bandwidth of the noise filters and test voltages.

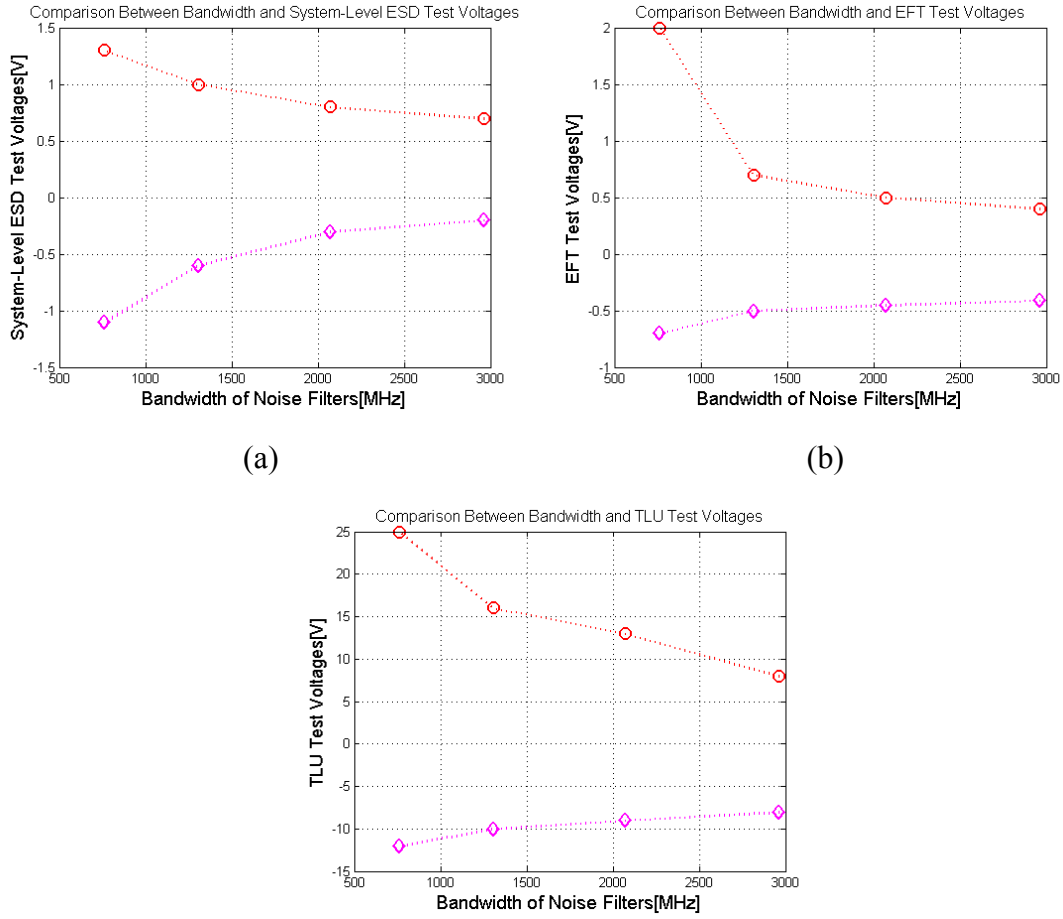


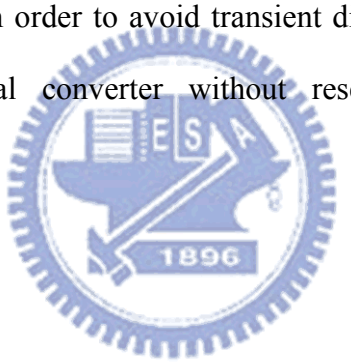
Fig. 5.2 Relationship between the bandwidth of the noise filters and test voltages (a) system-level ESD, (b) EFT, and (c)TLU.

On the other side, the frequency of the system-level ESD voltages should be further analyzed. The linear relation between ESD zapping voltages and digital codes should be improved by optimizing the noise filter networks.

Due to the transient disturbance under system-level ESD tests, the proposed on-chip transient-to-digital converter can detect the ESD-induced voltage variation on the power and ground lines. Nevertheless, the quantity of ESD-induced voltage variation is strongly

dependent on the impedance of the EUT. The detection range of on-chip transient-to-digital converter would be influenced by this condition. For advanced applications, the on-chip transient-to-digital converter should be designed to detect ESD-induced current variation of power and ground lines under system-level ESD zapping condition.

In system application, the on-chip transient-to-digital converter can be cooperated with power-on reset circuits and operating firmware to provide a hardware/firmware co-design solution for system-level ESD protection. After firmware receives different digital codes as ESD index, different recover procedures can be executed and finally reset the output voltage levels of on-chip transient-to-digital converter as initial state for detecting next system-level ESD events. Therefore, the IC products can achieve the “class B” system-level ESD specification at least. Besides, in order to avoid transient disturbance coupling on reset pad, the modified transient-to-digital converter without reset function should be further investigated.



Reference

[1] *EOS/ESD Standard for ESD Sensitivity Testing – Human Body Model – Component Level*, STM 5.1, EOS/ESD Association, NY., 2011.

[2] *EOS/ESD Standard for ESD Sensitivity Testing – Machine Model – Component Level*, STM 5.2, EOS/ESD Association, NY., 2009.

[3] *EOS/ESD Standard for ESD Sensitivity Testing – Charge Device Model – Component Level*, STM 5.3.1, EOS/ESD Association, NY., 2009.

[4] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821-1831, Aug. 2005.

[5] D. Smith and A. Wallash, "Electromagnetic interference (EMI) inside a hard disk driver due to external ESD," in *Proc. EOS/ESD Symp.*, 2002, pp. 32-36.

[6] IEC 61000-4-2 Standard, "*EMC – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*," IEC, 2008.

[7] T.-H. Wang, W.-H. Ho, and L.-C. Chen, "On-chip system ESD protection design for STN LCD drivers" in *Proc. EOS/ESD Symp.*, 2002, pp. 316-322.

[8] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in a 8-bits microcontroller to solve the system-level ESD issue on keyboard" in *Proc. EOS/ESD Symp.*, 1999, pp. 352-360.

[9] IEC 61000-4-4 Standard, "*EMC – Part 4-4: Testing and Measurement Techniques –Electrical Fast Transient/Burst Immunity Test*," IEC, 2004.

[10] Z. Pan, S. Holland, D. Schroeder, and W. Krautschneider, "Understanding the mechanisms of degradation and failure observed in ESD protection devices under

system-level tests," *IEEE Trans. Device Mater. Reliab.*, vol. 10, no. 2, pp. 187-191, June 2010.

[11] M. Scholz, D. Linten, S. Thijs, M. Sawada, T. Nakaei, T. Hasebe, D. Lafonteese, V. Vashchenko, G. Vandersteen, P. Hopper, and G. Groeseneken, "On-wafer human metal model measurements for system-level ESD analysis," in *Proc. EOS/ESD Symp.*, 2009, pp. 1-9.

[12] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, 2000.

[13] M.-D. Ker and S.-F. Hsu, "Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electromagn. Compat.* vol. 48, no. 1, pp. 161-171, Feb. 2006.

[14] *ESD Protection for USB 2.0 Interfaces (AN10753)*, NXP semiconductor, 2010.

[15] M.-D. Ker, C.-C. Yen, and P.-C. Shin, "On-chip transient detection circuit for system-level ESD protection in CMOS integrated circuits to meet electromagnetic compatibility regulation," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 1, pp. 13-21, Feb. 2008.

[16] C.-C. Yen, C.-S. Liao, and M.-D. Ker, "New transient detection circuit for system-level ESD protection," in *Proc. VLSI-DAT Symp.*, 2008, pp. 180-183.

[17] M.-D. Ker, C.-S. Liao, and C.-C. Yen, "Transient detection circuit for system-level ESD protection and its on-board behavior with EMI/EMC filters," in *Proc. IEEE Int. Sym. Electromagn. Compat. (EMC)*, 2008, pp. 1-4.

[18] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device Mater. Reliab.*, vol. 52, no. 7, pp. 235-249, Jun. 2005.

[19] M.-D. Ker and K.-C. Hsu, "Substrate-triggered SCR device for on-chip ESD protection in fully silicided sub-0.25-μm CMOS process," *IEEE Trans. Electron Devices*, vol. 50,

no. 2, pp. 397-405, Feb. 2003.

[20] M.-D. Ker and S.-F. Hsu, "Component-level measurement for transient-induced latchup in CMOS ICs under system-level ESD considerations," *IEEE Trans. Device Mater. Reliab.*, vol. 6, no. 3, pp. 461-472, Sep. 2006.

[21] M.-D. Ker and C.-C. Yen, "Transient-to-digital converter for system-level electrostatic discharge protection in CMOS ICs," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 3, pp. 620-630, Aug. 2009.

[22] O. Quittard, Z. Mrcarica, F. Blanc, G. Notermans, T. Smedes, and H. Zwol, "ESD protection for high-voltage CMOS technologies," in *Proc. EOS/ESD Symp.*, 2006, pp. 77-86.

[23] A. Ristow, M. Begovic, A. Pregelj, and A. Rohatgi, "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Trans. Ind. Electron.,* vol. 55, no. 7, pp. 2581-2592, Jul. 2008.

[24] C. Rodriguez and G. Amaratunga, "Long-lifetime power inverter for photovoltaic AC modules," *IEEE Trans. Ind. Electron.,* vol. 55, no. 7, pp. 2593-2601, Jul. 2008.

[25] H. Hansson, T. Nolte, C. Norstrom, and S. Punnekkat, "Integrating reliability and timing analysis of CAN-based systems," *IEEE Trans. Ind. Electron.,* vol. 49, no. 6, pp. 1240-1250, Dec. 2002.

[26] P. Hammond, "Enhancing the reliability of modular medium-voltage drives," *IEEE Trans. Ind. Electron.,* vol. 49, no. 5, pp. 948-954, Oct. 2002.

[27] S. Petrovic, A. Ramirez, T. Maudie, D. Stanerson, J. Wertz, G. Bitko, J. Matkin, and D. Monk, "Reliability test methods for media-compatible pressure sensors," *IEEE Trans. Ind. Electron.,* vol. 45, no. 6, pp. 877-885, Dec. 1998.

[28] S. Voldman, *ESD: Circuits and Devices*, John Wiley & Sons, 2006.

[29] K. Muhonen, P. Erie, Nate Peachey, and A. Testin, "Human metal model (HMM) testing, challenges to using ESD guns," in *Proc. EOS/ESD Symp.*, 2009, pp. 387-395.

[30] D. Liu, D. Pommerenke, S. Kwon, and K. Martwick, "Full wave model for simulating a noiseken ESD generator parameters," in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, 2009, pp. 334-339.

[31] G. Muchaidze, J. Koo, Q. Cai, T. Li, L. Han, A. Martwick, K. Wang, J. Min, J. Drewniak, and D. Pommerenke, "Susceptibility scanning as a failure analysis tool for system-level electrostatic discharge (ESD) problems," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 2, pp. 268-276, May 2008.

[32] N. Lacrampe, F. Caignet, M. Bafleur, N. Nolhier, and N. Mauran, "Characterization and modeling methodology for IC's ESD susceptibility at system level using VF-TLP tester," in *Proc. EOS/ESD Symp.*, 2007, pp. 304-310.

[33] M. Honda, "EMI power measurements of ESD radiated fields," in *Proc. EOS/ESD Symp.*, 2006, pp. 160-165.

[34] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821-1831, Aug. 2005.

[35] W. Stadler, S. Bargstadt-Franke, T. Brodbeck, R. Gaertner, M. Goroll, H. Goβner, N. Jensen, and C. Muller, "From the ESD robustness of products to the system-level ESD robustness," in *Proc. EOS/ESD Symp.*, 2004, pp. 67-74.

[36] N. Shimoyama, M. Tanno, S. Shigematsu, H. Morimura, Y. Okazaki, and K. Machida, "Evaluation of ESD hardness for fingerprint sensor LSIs," in *Proc. EOS/ESD Symp.*, 2004, pp. 75-81.

Publication List

(A) Referred Journal Papers:

[1]. M.-D. Ker, **W.-Y. Lin**, and C.-C. Yen, "SCR-based transient detection circuit for on-chip protection design against system-level electrical transient disturbance," submitted to *IEEE Trans. Electromagn. Compat.*, 2011. **(SCI, EI, Impact Factor : 1.294)**

(B) International Conference Papers:

[1]. M.-D. Ker, **W.-Y. Lin**, C.-C. Yen, C.-M. Yang, T.-Y. Chen, and S.-F. Chen, "Protection design against system-level ESD transient disturbance on display panels," in *Proc. Asian-Pacific Int. Symp. Electromagn. Compat. (APEMC)*, 2010, pp. 445-448.

[2]. M.-D. Ker, **W.-Y. Lin**, C.-C. Yen, C.-M. Yang, T.-Y. Chen, and S.-F. Chen, "New transient detection circuit for electrical fast transient (EFT) protection design in display panels," in *Proc. IEEE Int. Conf. Integr. Circuit Design and Technology (ICICDT)*, 2010, pp. 51-54.

[3]. M.-D. Ker, **W.-Y. Lin**, C.-C. Yen, C.-M. Yang, T.-Y. Chen, and S.-F. Chen, "On-chip ESD detection circuit for system-level ESD protection design," in *Proc. IEEE Int. Conf. Solid-State and Integrated Circuit Technology (ICSICT)*, 2010, pp. 1584-1587.

[4]. **W.-Y. Lin** and C.-C. Yen, "New transient detection circuit to detect system-level ESD disturbance for automatic recovery operation in display panels," in *2010 AMD Technical Forum*, 2010.

[5]. C.-C. Yen, **W.-Y. Lin**, M.-D. Ker, C.-M. Yang, S.-F. Chen, and T.-Y. Chen, "New transient detection circuit to detect ESD-induced disturbance for automatic recovery design in display panels," in *6th Int. Conf. Design and Technology of Integrated Systems (DTIS)*, 2011, *in press*.

[6]. C.-C. Yen, M.-D. Ker, **W.-Y. Lin**, C.-M. Yang, and T.-Y. Chen, "On-chip detection circuit for protection design in display panel against electrical fast transient (EFT) disturbance," in *13th Int. Conf. Electrostatics*, 2011.

[7]. C.-C. Yen, **W.-Y. Lin**, and M.-D. Ker, "Transient-to-digital converter to detect electrical fast transient (EFT) disturbance for system protection design," in *Proc. IEEE Int. Conf. Integr. Circuit Design and Technology (ICICDT)*, 2011.

(C) Local Conference Papers:

[1]. **W.-Y. Lin**, C.-C. Yen, M.-D. Ker, C.-M. Yang, T.-Y. Chen, and S.-F. Chen, "New ESD transient detection circuit against system-level transient disturbance in TFT LCD panels," in *Electronic Technology Symposium*, 2010.

[2]. **林宛彥**、顏承正、柯明道、蔡青霖、楊哲明、陳東暘、陳世範, "應用於系統層級靜電放電防護設計之新式暫態偵測電路," in *Proc. Taiwan ESD Conference*, 2010, pp. 42-45.

[3]. M.-D. Ker, **W.-Y. Lin**, C.-C. Yen, C.-L. Tsai, S.-F. Chen, and T.-Y. Chen, "Transient-to-digital converter to detect system-level ESD-induced disturbance in display panel," accepted by *VLSI Design/CAD Symposium*, 2011.

簡歷 (Vita)

姓　　名：林宛彥

學　　歷：

私立聖功女子高級中學　　(91 年 9 月~94 年 6 月)

國立交通大學電子物理系　　(94 年 9 月~98 年 2 月)

國立交通大學電子研究所碩士班　　(98 年 2 月~100 年 9 月)

比利時天主教魯汶大學電機碩士班　　(99 年 9 月~100 年 6 月)

研究所修習課程：

類比積體電路	吳介琮教授
數位積體電路	黃　威教授
積體電路之靜電放電防護設計特論	柯明道教授
計算機結構	劉志尉教授
類比濾波器設計	蔡嘉明教授
功率積體電路設計	陳科宏教授
奈米電子元件	荊鳳德教授
半導體物理及元件(一)	陳衛國教授

永久地址: 高雄市岡山區明得街 105 號

Email： m9711689@alab.ee.nctu.edu.tw