國立交通大學

電子工程學系 電子研究所

博 士 論 文

新穎多閘極多晶矽奈米線薄膜電晶體之研製與其應用

Fabrication and Analysis of Novel Multiple-Gated Poly-Si Nanowire Thin-Film Transistors and Their Applications

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摘要

在本篇論文中，我們利用數種簡易的奈米線製備技術，製作並研究各式具有多閘極結構的多晶矽奈米線薄膜電晶體。所提出的多閘極奈米線電晶體製備方式包括"側壁邊襯蝕刻法(side-wall spacer etching)”與”空腔形成填充法(cavity formation and filling)”，使用此兩種製備方式均可免除昂貴的微影設備與製作技術，自我對準形成各式高效能的多晶矽奈米線通道電晶體。

首先，我們針對使用側壁邊襯蝕刻技術所製作的雙獨立閘極多晶矽奈米線電晶體，探討在不同操作模式下(雙閘或單閘)之元件特性。由於奈米線通道厚度僅有約 10 奈米，強烈的閘極耦合效應(gate-to-gate coupling)會對元件電性造成深切的影響。在雙閘操作模式下，此元件可達到小於 100mV/dec 之次臨限擺幅(subthreshold swing)；而在單閘模式下，利用閘極耦合效應來調整輔助閘偏壓的方式可獲得不同的臨限電壓。實驗中我們也發現，在雙閘模式下由於不受背閘極效應(back-gate effect)的影響，在輸出特性上會有比單閘操作高之飽和汲極電壓，因此可獲得較大之飽和輸出電流(output saturation current)；此外，在雙閘

操作下對於通道中晶粒邊界與缺陷所造成之位能障(grain-boundary potential barrier)具有較佳的調控能力，因而可獲得較單閘操作下為佳之元件特性。此發現對於分析多晶矽通道元件之傳導機制具有重要的影響。我們也探討了雙獨立閘極多晶矽奈米線電晶體的基本電性擾動分析。從實驗數據顯示，利用電漿處理修補多晶矽通道裡的缺陷，可使元件之間的臨限電壓差異性降低，由此推測出複晶矽奈米線通道中的缺陷密度與電性擾動有一密切的關聯性。另外，在不同的操作模式下(雙閘或單閘)，以雙閘極操作模式，可得到最小的臨限電壓標準差。由於元件間通道厚度的差異所造成的臨限電壓擾動，會隨著橫跨在通道薄膜之電場大小而不同；實驗中也證實，當在單閘操作模式下，控制閘極的固定偏壓存在著一最佳值，能有效地降低臨限電壓的變異度。

除了使用側壁邊襯蝕刻法製作奈米線元件，我們也提出並發展了另一種新穎的奈米線製備技術，稱作空腔形成填充法。利用此技術製作出的三閘極(tri-gate)多晶矽奈米線電晶體展現了相當陡峭的次臨限擺幅(~100mV/dec)，和大於 10^8 的開關電流比值(ON/OFF current ratio)。此結果驗證了多閘極可以有效增進元件的效能。另外，一種基於空腔形成填充法，可以同時製作出具有不同閘極結構但奈米線通道形狀相同之電晶體的製程技術也被提出。利用此簡單有趣的製程，能有效分析與評估多重閘(Multi-gate)的實際效應，且有助於探討多重閘對於奈米線元件的基本特性和及電性擾動的影響。實驗結果亦顯示越佳的閘極控制能力對於奈米線元件之變異度也能越有效的控制。

在非揮發記憶體應用方面，我們利用空腔形成填充法成功地製作了多種閘極型態的 SONOS 記憶體元件，包含單側閘極(side-gated, SG)、Ω 型閘(Ω-gated)和全環繞閘極(gate-all-around, GAA)。其中全環繞閘極奈米線記憶體元件除了展現出最佳的基本電性，記憶體特性方面包含寫入/抹除速度、電荷保持能力(retention)和忍耐力(endurance)也具有很顯著的增進。這些實驗結果都歸因於全環繞閘極奈米線電晶體擁有接近理想的圓形奈米線通道截面，和最有效的閘極

控制能力。

在論文的最後部份，我們提出並製作一種具有延伸式感測閘(SENSE-gate)與讀取閘(READ-gate)的新穎雙獨立閘極奈米線感測元件，並對於各種感測應用的可行性進行初步的探討。此感測架構結合奈米線電晶體結構與延伸式閘極離子感測場效電晶體(EGFET)的概念，可有效將元件操作區與充滿酸/鹼性化學物質或生物分子溶液的感測區與隔離。因此所製作出之感測元件，同時具有延伸式閘極感測元件之可靠度與系統整合能力，還有奈米線感測元件之優良的轉導特性。此研究也呈現並討論各種實際感測的初步實驗結果，包括酸鹼感測(pH sensing)、生物分子偵測(bio-molecules detection)和氣體感測(gas sensing)。另外，相較於把多晶矽奈米線直接曝露在環境中作感測的感測元件，此雙獨立閘感測元件由於使用了延伸式閘極結構，在中性水溶液環境中的施壓測試(stressing testing)中明顯展現更穩定與可靠的電性結果。

關鍵字：奈米線, 多閘極, 多晶矽, 薄膜電晶體, 背閘極效應, 變異度, 非揮發記憶體, SONOS, 感測器。

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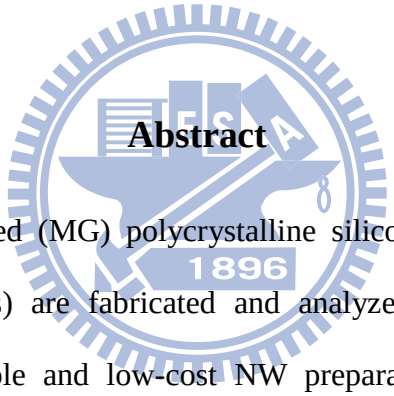

Abstract

Various multiple-gated (MG) polycrystalline silicon nanowire (poly-Si NW) thin-film transistors (TFTs) are fabricated and analyzed. The proposed NWTFT schemes utilize very simple and low-cost NW preparation techniques, including “side-wall spacer etching” and “cavity formation and filling”, to fabricate poly-Si NWs in a self-aligned manner. Detailed characteristics of the MG NWTFT devices and their potential applications involving non-volatile memory (NVM) and chemical sensors are also studied and demonstrated.

For NW devices fabricated by the side-wall spacer etching technique, the characteristics of the poly-Si NWTFT featuring an independent double-gated (DG) configuration are analyzed and compared. It is found that the device under DG mode exhibits significantly better performance with respect to the two single-gated (SG) modes in terms of a higher current drive over the combined sum of the two SG modes

and a smaller subthreshold swing (SS) of less than 100 mV/dec. Origins of such improvement are identified to be due to the elimination of the back-gate effect as well as an enhancement in the effective mobility with DG operation. The mobility improvement in DG mode is ascribed to more efficient gate control in lowering the grain-boundary potential barrier. Moreover, the V_{TH} fluctuation behavior of poly-Si NWTFTs is also investigated and studied. The defects existing in the NW channels are identified as one of the major sources for the V_{TH} fluctuation. The passivation of these defects by plasma treatment is shown to be effective in reducing the V_{TH} fluctuation. It is also found that the fluctuation is closely related to the operation modes. When only one of the gates is employed as the driving gate to control the device's switching behavior, an optimum bias for the other gate could be found for minimizing the V_{TH} fluctuation.

On the development of new NW preparation method, the cavity formation and filling technique is proposed, which enables the fabrication of poly-Si NW without resorting to advanced lithographic tools. The tri-gated poly-Si NWTFTs built on this novel technique show steep SS of around 100 mV/dec and ON/OFF current ratio higher than 10^8, signifying the effectiveness of MG scheme in improving the device performance. Furthermore, a clever scheme based on cavity formation and filling technique allowing fabricating test structures with identical NW channel but different gate configurations is also proposed, and the impact of MG configurations on the variation of NWTFTs characteristics is also investigated. The results show the variation is reduced by increasing the portion of NW channel surface that is modulated by the gate.

As regards NVM applications, we demonstrate the poly-Si NW-SONOS devices using the cavity formation and filling technique. Three types of devices

having various gate configurations, namely, side-gated (SG), Ω-shaped gated (ΩG) and gate-all-around (GAA), are successfully fabricated and characterized. The experimental results show that much improved transfer characteristics are achieved with the GAA devices as compared with the other types of devices. Moreover, GAA devices also exhibit the best memory characteristics among all splits, including the fastest P/E efficiency, largest memory window and best endurance/retention characteristics.

Finally, the feasibility of the novel independent DG NW sensing device scheme featuring an extended sensing gate (SENSE-gate) and a READ-gate for various sensing applications is explored. This scheme takes advantages of extended-gate ion-sensitive FET's (EGFET) effective isolation of device from chemical and biological environment, and NWFET's good switching properties. The preliminary study using this novel sensing device for pH sensing, gas sensing and bio-molecules detection is presented and described. In addition, owing to the use of extended-gate structure, this novel sensing scheme exhibits more stable and reliable electrical characteristics during the stressing test in aqueous solution as compared with those of NW sensor devices having poly-Si NWs exposed to the ambient.

Keywords: Nanowire (NW), Multiple-Gate (MG), Polycrystalline Silicon (Poly-Si), Thin-Film Transistor (TFT), Back-Gate Effect, Variability, Non-Volatile Memory (NVM), Silicon-Oxide-Nitride-Oxide-Silicon (SONOS), Sensor.

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徐　行　徽

誌於風城交大

2011 年 10 月

Contents

Table Captions

Chapter 2

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Introduction

1-1 Overview of Nanowire Technology

In the past two decades, the field of nanotechnology has been vastly explored and investigated. The study of nanotechnology involves diverse topics, including material science, biological science, atomic- and molecular-scale physics, electronics engineering, *etc*. In terms of the usefulness and potential applications of nanotechnology, some novel nanostructures, such as nanowire (NW), have received particular attention and regarded as a promising choice for future electronics due to their desirable features as well as progressively improved fabrication techniques for pragmatic development and production purposes.

An NW is defined as a stripe-shaped material with a diameter or feature size smaller than 100 nm. For this kind of structure, the ratio of the surface area to volume increases as its cross-sectional dimensions shrink. Accordingly, NW can achieve a very large surface-to-volume ratio from its tiny volume, giving rise to a significant impact of the surface condition on material properties and carrier transport. Owning to this inherent property, semiconductor NWs are attractive to a variety of electronic applications, such as nano CMOS [1.1], NW TFTs [1.2], memory devices [1.3], and sensors [1.4]. For a field-effect transistor (FET), using NWs as the channel enables excellent controllability over the carrier transport and therefore suppresses the off-

state leakage current to realize high performance and fast switching property. For memory applications, memory devices built on NW structure possess high programming/erasing (P/E) efficiency and low-voltage operation [1.5]. For sensor applications, NW's high surface-to-volume ratio is conducive to high sensitivity to the target under detection [1.6].

In general, the preparation methods of NWs can be classified into two groups, one is "top-down" and the other one is "bottom-up". In top-down methods, advanced lithography tools, like deep-UV [1.1], e-beam [1.7] and nano-imprint [1.8], are usually essential to generate NW patterns. With its capability of precise positioning and good reproducibility, this approach is suitable for mass production. Currently nano-scale lines down to or even narrower than 30 nm are routinely generated in production lines to fabricate advanced circuitries with high yield. However, the mature processing techniques still face certain issues. For example, the fabrication cost is extremely high as costly exposure apparatus or expensive materials like silicon-on-insulator (SOI) are used. Moreover, the process usually requires cutting-edge technology. Therefore, it is hard to be employed popularly in academia such as university for research purpose. Besides, the selection of NW materials is quite inflexible because of the limitation set by the substrate material. Some alternative top-down approaches using relatively cheap conventional photolithography tools (*e.g.*, G-line and I-line steppers) with unique process techniques, such as thermal flow [1.9], chemical shrink [1.10] and spacer patterning [1.11], have also demonstrated their ability of fabricating NW devices. Nevertheless, these methods are not able to generate NW patterns directly, and hence require more complex processing procedures.

For bottom-up approach, one of the advantages pertaining to this approach is

the capability of synthesizing NW with various kinds of materials [1.12]. Methods categorized under bottom-up approach include metal-catalyzed vapor-liquid-solid (VLS) [1.13], solid-liquid-solid (SLS) [1.14], solid-phase-diffusion [1.15], molecular beam epitaxy (MBE) [1.16], oxide-assisted growth [1.17], and so forth. Among these diverse techniques, the most successful and prevalent one is the VLS method because of its flexible and simple preparation procedure. VLS method offers a more economical and affordable option to fabricate NWs, greatly facilitating the related researches in academia. Although bottom-up methods are remarkably cheaper than top-down methods and more flexible for experimental purpose, they have their own shortcomings. First, length, diameter and orientation of NWs are not easy to be controlled precisely. The prepared NWs are difficult to be aligned and positioned accurately, especially for the purpose of device fabrication. For metal-catalyzed growth, metal contamination is also a potential concern. Furthermore, the formation of reliable contacts for electrodes reveals another challenging issue.

1-2 Multiple-Gated Transistors

In the challenges of shrinking devices to nanometer scale, one critical obstacle is how to increase the gate controllability over the channel in order to suppress the short-channel effects (SCEs), which stem from the lateral electric field penetrating from the drain into the channel region and thus weakens the gate control [1.18]. Reduction of gate oxide thickness could provide some help, but may also dramatically increase the tunneling current from gate electrode and then aggravate the power consumption of circuits. To cope with these issues, two methods for enhancing gate

controllability are feasible; one is applying high-κ materials as gate insulator in place of conventional SiO_2, and the other is adopting a multiple-gated (MG) configuration.

A number of MG device schemes have been proposed so far [1.19-1.24]. In comparison with single-gated device, MG structure can provide much better electrostatic control over the channel region to mitigate SCEs, as shown in Fig. 1 [1.25]. Among the innovations of MG devices, quasi planar FinFET has already drawn a lot of attention in the past decade [1.20, 1-21]. The FinFET structure is able not only to perform double-gated or tri-gated control, but also to have good ability to shrink the channel dimension into nano-meter scale. Moreover, owing to its quasi-planar structure, FinFET is versatile to be incorporated into modern fabrication processes. Several types of FinFET structures have been proposed and evolved (as shown in Fig. 2 [1.26]), including double-gate (DG) (UC Berkeley) [1.21], tri-gate (Intel) [1.22], Ω-gate (TSMC) [1.23], *etc*. The most ideal and ultimate MG configuration is gate-all-around (GAA) NW structure [1.24], which exhibits the best gate controllability over the channel potential. In addition, with moderate size of NW, the quantum mechanical effects existing in quasi-1D NW channel could benefit carrier transport properties in terms of lower scattering rate and higher ballistic efficiency [1.27]. In mid-2011, Intel has announced that the tri-gated body-tied Si-fin structure (on the right of Fig. 3) will be used as the building block on the company's next 22 nm-generation chips [1.28].

1-3 Variability of MOSFETs Characteristics

In principle, the miniaturization of MOSFETs generally necessitates reducing

operation voltage to retain acceptable reliability and power dissipation [1.29]. Nevertheless, the functionality of circuits and individual electrical properties of advanced CMOS devices become more sensitive to the device structural parameters as well as process variations during the fabrication [1.30]. Threshold voltage (V_{TH}) fluctuation in MOSFETs has been regarded as one of the most difficult challenges for further down-scaling [1.31]. This fluctuation is originated from a plethora of variation sources, including patterning proximity effects [1.32], line-edge roughness due to lithographic and etching [1.33], thin-film variation (thickness variation [1.34], defects and fix charges [1.35]), the granularity of gate material [1.36, 1.37], strain process variation [1.38], and random dopant fluctuation (RDF) [1.39, 1.40].

It has been shown that RDF plays an increasingly pronounced role in V_{TH} fluctuation in extremely scaled MOSFETs [1.41]. RDF means the fluctuation caused by randomly scattered spatial distribution of impurity atoms in the channel of devices. Since the ion implantation and diffusion processes for doping are unable to control the exact number of dopants and precisely locate them individually, RDF is an inevitable phenomenon in conventional MOSFET scheme. In a 50 cubic nanometer volume with doping concentration of 10^{18} cm^{-3}, there are only 125 dopants in this space. Therefore, the variation of dopant number in the depletion region would result in a considerable difference in V_{TH}. Consequently, it is imperative to find out a suitable solution or strategy to circumvent this intrinsic problem while device dimensions keep shrinking. Fully depleted SOI (FD-SOI) and MG schemes might be possible solutions to deal with this problem [1.42]. Owing to their enhanced gate controllability and immunity to SCEs, the channel doping formerly used to prevent SCEs in conventional MOSFETs can be relieved and remain undoped to eliminate the part of V_{TH} fluctuation related to RDF effects.

1-4 Overview of Nonvolatile Memory

Driven by the unceasing reduction of cost and increase of memory density, the market of nonvolatile memory (NVM) has been growing rapidly over the last two decades. “Non-volatile” indicates that a memory device can retain stored data even if the power is switched off. This feature enables more convenient data access and therefore ideally suitable for portable electronic products. One of the most important inventions in NVMs is flash memory [1.43], which possesses a number of advantages such as byte-selectable write operation combined with sector “flash” erase, non-volatility, good durability and low power. Therefore it becomes the most ideal choice for data storage in numerous electronic systems.

At present, the most prevailing cell device structure for flash memory is the floating-gate device. However, as the memory cell keeps shrinking, the floating-gate device is confronted by several scaling limits. Since the storage layer is made of poly-silicon, the narrow spacing between two adjacent memory cells would lead to coupling interference, resulting in undesirable threshold voltage shift and data disturbance [1.44]. Another issue is associated with the scaling of tunnel oxide thickness which is essential for low P/E operation voltages. For a thin dielectric, the stress-induced leakage current (SILC) may cause all charges stored in the conductive floating gate to leak out, thus degrading the reliability of memory devices [1.45]. This limits the thickness of tunneling oxide at around only 7 nm. Although the multi-level cell (MLC) technique has been applied in real products to increase memory capacity per cell [1.46], the number of charges needed for differentiating storage levels is down to tens of electrons in a sub 30 nm node flash, giving rise to a large variation in memory window and aggravated interference between cells [1.47]. Consequently, SCE and decreased number of stored charges will raise obstacles to further scaling of

planar NAND flash technology at around the 10 nm node [1.48]. In addition, below the 20 nm technology node, 3-D NAND flash will be a likely solution to increase the memory density without aggressively reducing the feature size of memory devices [1.48].

1-4.1 Charge-Trapping Flash Memory

To address the aforementioned problems met in conventional floating-gate flash technology, the most likely candidate is the charge-trapping flash (CTF) memory [1.49]. Silicon-oxide-nitride-oxide-Silicon (SONOS) multi-layer scheme has been widely studied and reported in CTF device technology [1.50]. For a SONOS device, each layer of the ONO dielectric stack, namely, oxide tunneling layer, nitride trapping layer and oxide blocking layer, represents distinct function for memory operation. Unlike conventional floating-gate flash device, CTF-type device normally uses an insulator (*e.g.*, Si_3N_4) or discrete nano-crystals (e.g. metal nano-dots [1.51]) in place of the floating gate as the charge storage layer, so that the charges can be discretely stored and isolated by deep-energy-level trapping centers in the trapping layer. Therefore, CTF memory devices not only effectively minimize cell to cell coupling interference, but also exhibit much stronger immunity against charge leaking through a single defect formed in the tunneling oxide, hence improving the data retention.

Recently, some advanced multi-layer structures have been conducted to replace SONOS for further improving the performance of CTF devices, such as TANOS (TaN/Al_2O_3/Nitride/SiO_2/Si) structure proposed by Samsung [1.52] and band-gap engineered SONOS (BE-SONOS) proposed by Macronix [1.53]. In the TANOS structure, a high-κ Al_2O_3 dielectric which has an energy barrier comparable to that of SiO_2 is applied to replace traditional blocking layer to obtain higher gate voltage

coupling ratio, thus enhancing the electric field in tunneling oxide under P/E operation while maintaining adequate retention characteristics with thick enough blocking and tunneling layers. Besides, the high-work-function TaN gate material can effectively suppress gate-injection current during erase operation due to the higher energy barrier seen by the electrons in the gate, leading to a better erasing efficiency. In BE-SONOS, the conventional SiO_2 tunneling layer is replaced by an ultra-thin ONO multi-layer. With proper band-gap engineering, this tunneling layer structure can provide thick energy barrier to restrain direct tunneling at low electric field during retention. While during erase operation, the tunneling barrier becomes ultrathin due to a suitable band offset at high electric field, allowing efficient hole direct tunneling for fast erasing.

1-4.2 Nanowire Nonvolatile Memory

Silicon NW (SiNW) has a great potential to shrink memory cells to nano-meter scale without suffering from short-channel effects (SCEs). Furthermore, due to the inherently large surface-to-volume ratio, electric potential in NW channel is very sensitive to the surface condition. By utilizing this property to nonvolatile memory, a smaller amount of charge storage could cause a larger threshold voltage shift of memory device to obtain sufficient memory window. In addition, for a SONOS device with a cylindrical NW channel and gate-all-around (GAA) configuration (as shown in Fig. 4 [1.54]), the electric field at the channel-to-gate dielectric interface can be enlarged compared to that of planar devices, hence P/E time or voltage could be dramatically reduced [1.54]. At present, the proposed concepts and techniques for NW NVM include SONOS [1.55], FRAM [1.56], nano-dot [1.57], molecule-gate [1.58], *etc*. The working principles of the above-mentioned techniques are basically identical

to those of the flash memory nowadays. SONOS and FRAM can be built on the development experience of planar devices, relatively feasible for NW NVM applications in the near future.

1-4.3 Three-Dimensional Stackable Nonvolatile Memory

With respect to high-density memory applications such as NAND flash, currently many studies have been devoted to exploring alternative approaches to deal with the forthcoming physical scaling limit of memory devices. The most apparent way is to increase memory cell density in vertical dimension, i.e. 3-D memory. Samsung has reported a 3-D stacked NAND flash array with double single-crystalline Si (c-Si) layer [1.59]. However, in this approach it is difficult to further stack more c-Si layers on their inter-layer-dielectric (ILD) because of more and more rigorous thermal budget and thin-film quality control. At the expense of transistor performance, using poly-Si thin-film-transistor (TFT) as SONOS device would be much easier to stack memory arrays vertically for 3-D configuration due to the relatively low process temperature (Fig. 5) [1.60, 1.61]. An even more sophisticated 3-D NVM array architecture called Bit-Cost Scalable (BiCS) flash has been proposed by Toshiba (Fig. 6) [1.62, 1.63]. The NAND strings in BiCS scheme consist of vertical poly-Si TFT-SONOS pillars and multi-layer electrodes. This novel 3-D NVM scheme allows much more increased device density without aggressively reducing device size, and also provides more flexibility in circuit architecture design.

1-5 Overview of Solid-State Sensors

Solid-state sensor is a sensor device made of solid-state material (*e.g.*, silicon), which is able to detect and respond to physical or chemical stimuli, and then convert the input signal into a suitable output (*e.g.*, electrical response) to be transferred to an actuator for actuating, or a monitor for observing. Based on the properties of the object to be sensed, sensor devices can be classified into three types. The first one is physical sensor for measuring physical characteristics such as mass, distance, temperature, *etc* [1.64]. The second one is chemical sensor for detecting chemical substances according to their chemical or physical responses [1.65]. The last one is biosensor for identifying particular biological substances by using a modified sensor device with biological sensing interface [1.66].

Since the first ion sensitive field effect transistor (ISFET) introduced by P. Bergveld in 1970 [1.67], solid-state sensors based on semiconductor devices have attracted a substantial attention. Owing to their capability of miniaturization and compatibility with modern VLSI processes, numerous advantages could be obtained in terms of low cost, standardization, mass production, and applicability for simple testing equipment. Moreover, by integrating miniature sensors with microelectronic circuit, the performance of the so-called integrated sensors can be further improved. These features make semiconductor-based sensors a favorable choice for medical applications.

Two of the most prominent innovations for chemical and biological sensor technologies using semiconductor FETs are introduced in the following subsections.

1-5.1 Ion-sensitive Field-Effect Transistor

In brief, Ion-sensitive field-effect transistor (ISFET) is a sensor device combined with electrochemistry and microelectronics, featuring an ion-selective electrode together with the traits of FET. The configuration and working principle of ISFETs are quite similar to those of conventional MOSFETs, except the gate electrode is generally replaced by an electrolytic solution with a reference electrode inserted, as shown in Fig. 7 [1.68]. Therefore, the gate dielectric or the sensing membrane on top of the channel of the ISFET is directly exposed to the solution to serve as a receptor with its surface dangling bonds (binding sites), enabling the binding reaction with target ions (*e.g.*, H^+) in electrolyte to determine the electric potential of the chemical gate [1.68]. Consequently, alterations in electrolyte such as the species of ions or ion concentration can vary the potential of the chemical gate, so that the sensing operation can be achieved by detecting either the threshold voltage shift or the drain current change of the ISFET modulated by the field-effect mechanism.

Compared to the traditional glass ion-selective electrode, ISFET possesses several distinctive merits, including compactness, compatibility with standard CMOS process, high input and low output impedances, high durability, measurability with small volume of sample, faster response, *etc.* In addition to ion selective sensing, ISFET modified with an immobilized enzyme as sensing membrane can be functionalized to serve as an enzyme selective sensor, called enzyme-modified FET (ENFET) [1.69]. Various applications of ISFET and its derivatives, as well as the detectable analytes are shown in Fig. 8 [1.70]. While dealing with the invasive chemical solution or biological environment, another commonly-used ISFET-type sensor is extended gate field-effect transistor (EGFET) [1.71]. In this configuration, the chemically or biologically sensitive membrane is deposited on the end of an

extended conduction wire connected to the gate electrode of FET (as shown in Fig. 9), so that the active region of FET can be isolated from the invasive environment during operation. Moreover, the EGFET structure is insensitive to noises caused by light and temperature, and provides good flexibility for selecting suitable membranes for different targets as well as the shape of extended gate, thus simpler passivation and encapsulation for packaging can be achieved.

1-5.2 Nanowire Sensors

In recent years, one dimensional (1-D) nanostructures such as NWs for sensor applications have attracted considerable research interests, especially for bio-molecular sensing because of the stringent requirements for ultra-sensitive detection with low-level molecular concentration [1.66, 1.72]. For a conventional ISFET-based biosensor, the exposed sensing area of device channel is exceedingly larger than molecular dimensions, necessitating a great amount of molecules to be bound to the sensing membrane in order to create a sufficient potential change of the chemical gate, and therefore the sensitivity and response time for low-level detection are greatly impeded.

NW biosensors have shown desirable potential for overcoming many obstacles encountered by current ISFET biosensor technologies [1.4, 1.73]. Since NW features high surface-to-volume ratio and its critical dimensions are comparable to the size of biological molecules, such as proteins and nucleic acids (as shown in Fig. 10 [1.74]), any interaction between NW's surface and charged molecules in the testing environment may provoke significant changes in electrical properties of the NW device, enabling ultra-sensitive, real-time and direct (*i.e.*, label-free) sensing capability for bio-molecule detection. The ability of directly sensing low

concentrations of proteins [1.75], DNA [1.76] and single virus [1.77] has been demonstrated by using silicon NW. Fig. 11 illustrates a reversible nanoscale biosensing process with an NW sensor [1.78].

However, using measurement approaches which directly immerse NW sensor in a test solution during testing could drastically affect the reliability of the sensor device and precision of the measurement results. Besides, it is difficult to preserve the NW devices for a long time without solid passivation, hence hindering the realization of practical production.

1-6 Motivation

Since Si NWs are attractive to various applications and have potential to be an ideal building block for future electronics, pursuing a more reliable and high-performance NW device as well as developing more feasible fabrication processes are imperative and worthy of studying. To address the issues encountered in typical top-down and bottom-up approaches for NW device fabrication as introduced in Sec. 1-1, our laboratory (ADT Lab) has proposed and developed a novel poly-Si NW field-effect transistor scheme which cleverly employs the sidewall spacer etching technique to define poly-Si NWs channels and features a single side-gate structure [1.79, 1.80]. This scheme offers the following advantages: (1) Simple and low-cost fabrication process, (2) controllable NW's size, (3) accurate positioning and self-aligned source/drain and NW formation, (4) more reliable formation of contact, and (5) easy to integrated with CMOS processes.

The fabricated NW devices have been shown to be beneficial for enhancing the

device performance compared to the planar counterparts in our previous works, including reduced short channel effects (SCEs) and steeper subthreshold swing (SS). Nonetheless, the ON current and gate controllability of this NW device are limited by the small conducting width inherent with the single side-gated structure. Another major concern associated with this scheme is the use of poly-Si NWs as the channel material. Defects contained in the granular poly-Si channel are known to hinder carrier transport and provoke undesirable leakage current, leading to deteriorated ON-state current drive as well as switching properties of the devices.

Several ways are possible to alleviate these concerns. One is to improve the film crystallinity by implementing available process schemes such as metal-induced lateral crystallization (MILC) [1-81]. An alternative strategy is the adoption of MG configuration, which is expected to further improve the performance of poly-Si NWTFT devices through an increase in the effective channel width and enhanced gate controllability over the channel. In addition, the MG configuration can be designed to consist of several separate gates, and each gate can be biased independently, enabling more freedoms for device operation.

For NVM application, some challenging issues existing in conventional TFT memory devices, such as poor SS and large leakage current, which would require high voltages for P/E operations and raise the power dissipation. By adopting poly-Si NW channel with a MG configuration, these problems could be mitigated.

For sensor application, to cope with the obstacles met in conventional ISFET and NW sensor technologies, applying a suitable MG NWTFT scheme is believed to promote the reliability and durability of NW sensors while retaining its good transfer characteristics by adopting an extended sensing gate to separate the device region from the chemical and biological environment.

1-7 Thesis Organization

In this dissertation, several types of poly-Si NWTFT with MG configurations, including independent double-gate (DG), tri-gate (TG) and gate-all-around (GAA) were fabricated and characterized. In addition, various applications involving NVM and biosensors by using MG NWTFT are also demonstrated.

This dissertation comprises six chapters. Chapter 1 introduces the background and motivation of this study. Chapter 2 is basically an extension of our previous work [1-82], and more comprehensive investigation and understanding of physical phenomena in independent DG poly-Si NWTFT devices are discussed. Chapter 3 proposes a simple but novel method to fabricate MG NW devices. Chapter 4 shows and compares the impacts of MG configuration on the characteristics of poly-Si NW TFT-SONOS memory. Chapter 5 proposes and discusses a new sensor scheme using poly-Si NWTFT with extended-gate structure for various sensing applications. And Chapter 6 is the conclusions and suggested future work. The detailed content of each chapter is described as follows.

In Chapter 1, an overview of NWs and related potential applications are briefly introduced, including MG transistors, variability issues, NVM devices, and solid-state sensors. The motivation part describes the incentive of utilizing several modified schemes of poly-Si NWTFTs to deal with the problems existing in previous structures, and also to explore their capability for possible applications.

In Chapter 2, the characteristics of a poly-Si NWTFT device with an independent DG configuration under different operation modes are investigated and compared. In the device, the tiny NW channels are surrounded by an inverse-T-shaped gate and a top gate. It is found that the device under DG mode exhibits significantly

better performance in comparison with the two single-gate (SG) modes in terms of a higher current drive over the combined sum of the two SG modes and a smaller subthreshold swing (SS) of less than 100 mV/dec. Origins of such improvement are identified to be due to the elimination of the back-gate effect as well as an enhancement in the effective mobility with DG operation.

Moreover, the V_{TH} fluctuation of poly-Si NWTFT devices is also studied in this chapter. The defects existing in the NW channels are identified as one of the major sources for the V_{TH} fluctuation. The passivation of these defects by plasma treatment is shown to be effective for reducing the V_{TH} fluctuation. It is also found that the fluctuation is closely related to the operation modes. When only one of the gates is employed as the driving gate to control the device's switching behavior, an optimum bias for the other gate can be found for minimizing the V_{TH} fluctuation.

In Chapter 3, several types of poly-Si NWTFTs with various MG configurations are demonstrated and characterized. These devices were fabricated with simple methods without resorting to costly lithographic tools and processes. The fabricated tri-gated devices show a low subthreshold swing (SS) of around 100 mV/dec and on/off current ratio higher than 10^8. These results indicate the effectiveness of MG scheme in enhancing the device performance. Furthermore, the impact of MG on the variation of NWTFT characteristics is investigated with a clever method that allows the fabrication of test structures with identical NW channel but different gate configurations. The results show that the variation could be reduced by increasing the portion of NW channel surface that is modulated by the gate.

In Chapter 4, we propose a simple and novel way to fabricate poly-Si NW-SONOS devices with various gate configurations. Three types of devices having various gate configurations, namely, side-gated (SG), Ω-shaped gated (ΩG) and gate-

all-around (GAA), are successfully fabricated and characterized. The experimental results show that, owing to the superior gate controllability over NW channels, much improved transfer characteristics are achieved with the GAA devices as compared with the other types of devices. Moreover, GAA devices also exhibit the best memory characteristics among all splits, including the fastest P/E efficiency, largest memory window and best endurance/retention characteristics, highlighting the potential of such scheme for future SONOS applications.

In Chapter 5, results of the preliminary study using a novel NWFET sensing scheme featuring an extended sensing gate for various sensing purposes including pH sensing, gas sensing and bio-molecules detection are presented and described. In one of the embodiments of the proposed scheme, the NW channel is gated with two gates, namely, the SENSE-gate and the READ-gate. An antenna-like extended-gate structure acting as a sensing area is connected to the SENSE-gate of the NW device. During measurement the SENSE-gate is used for detecting the targets entities in the test solution. A change in the amount of sensing charges would promptly affect the characteristics of the NW devices which can be effectively monitored with the READ-gate. This scheme takes advantages of EGFET's effective isolation of device from chemical and biological environment, and NWFET's good switching properties. The high manufacturability, low fabrication cost and improved reliability make this scheme extremely useful and potential for practical biosensor applications.

Finally, we summarize the conclusions and our major achievements, and also the suggested future work in Chapter 6.

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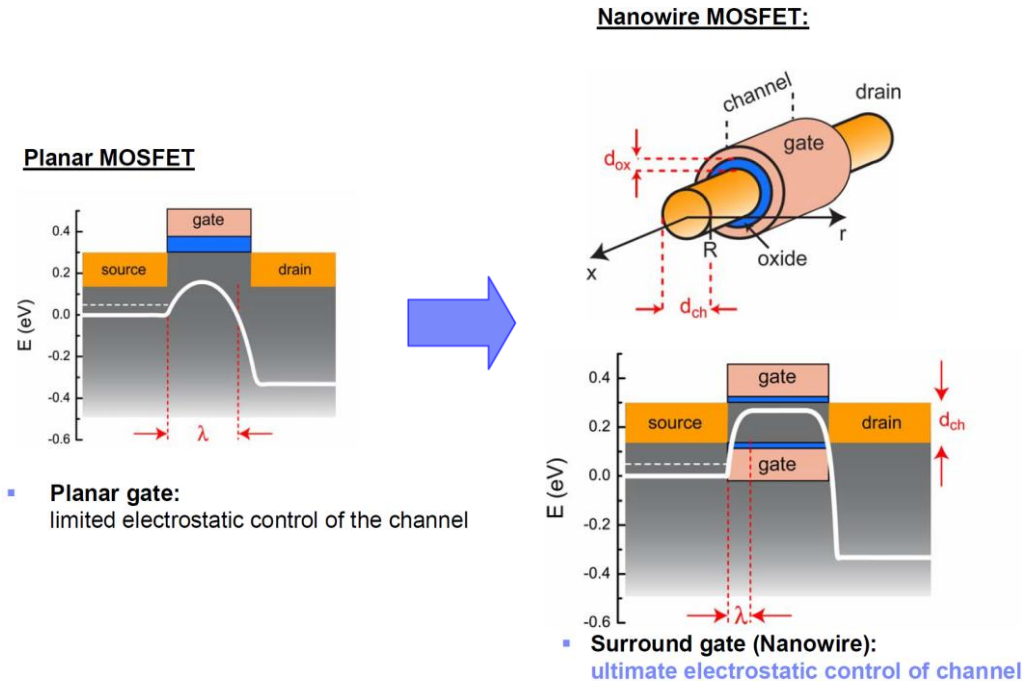


Fig. 1-1 Schematic structures and energy band diagrams of planar single-gated MOSFET (left) and gate-all-around (GAA) NW MOSFET (right). Apparently the GAA NW structure can provide much better electrostatic control to prevent the lateral electric field penetrating from the drain into the channel region [1.25].

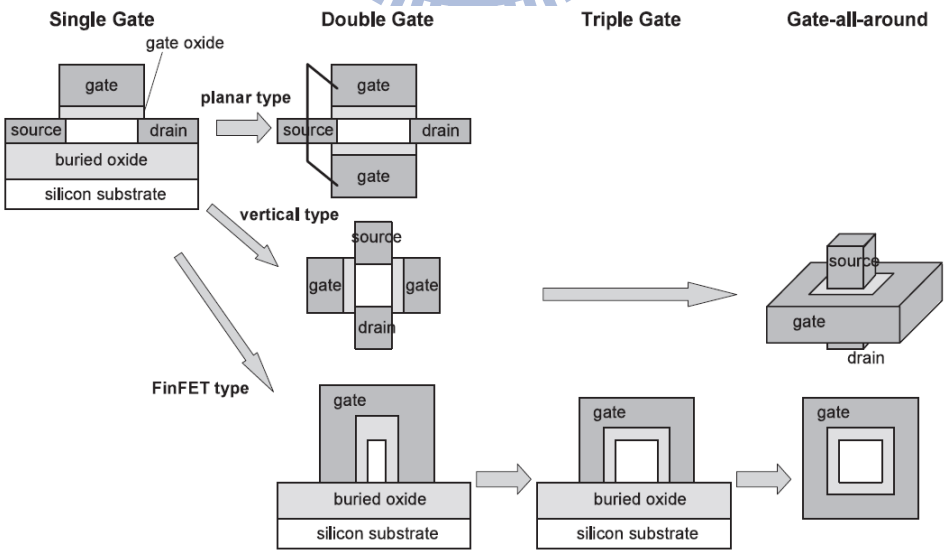


Fig. 1-2 Evolution of the new transistor structure to improve the electrostatics of a MOSFET [1.26].

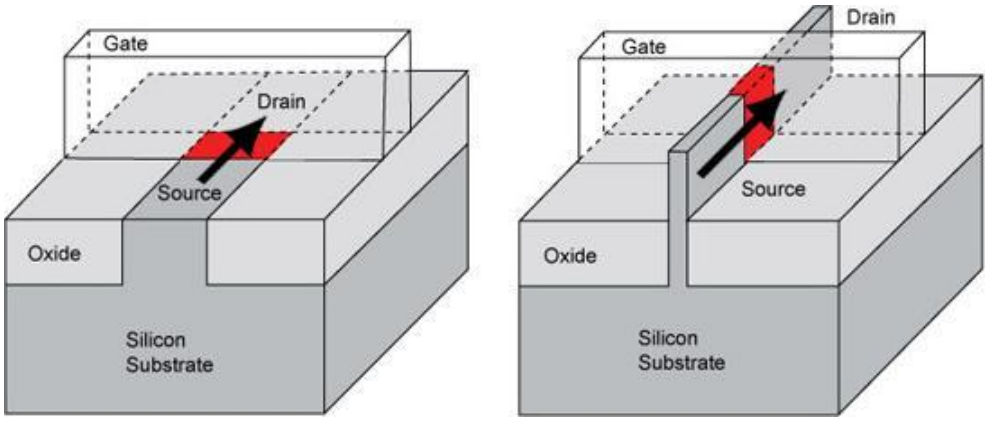


Fig. 1-3 Schematics of conventional transistor with a top-mounted gate (left) and Intel's tri-gate transistors with body-tied Si-fin structure (right) [1.28].

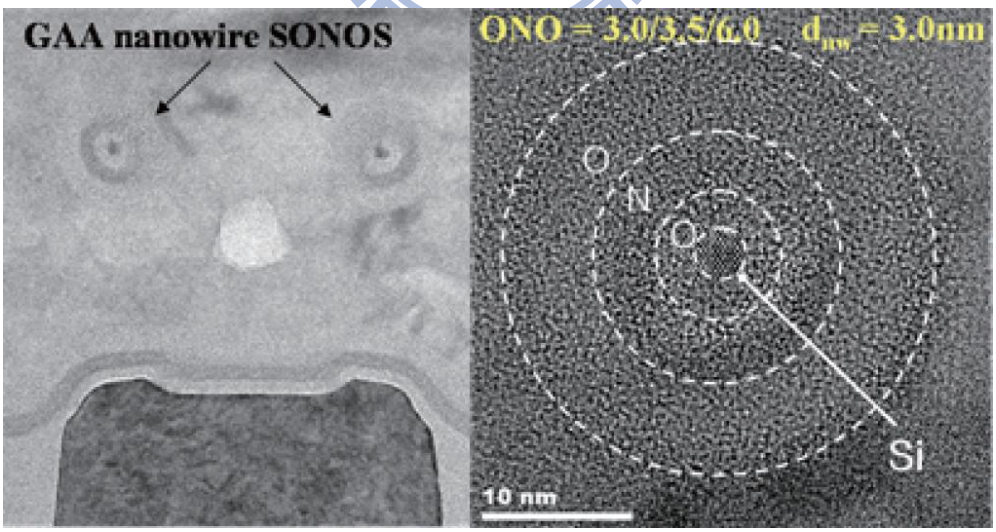


Fig. 1-4 Cross-sectional TEM images of gate-all-around twin silicon nanowire SONOS memory [1.54].

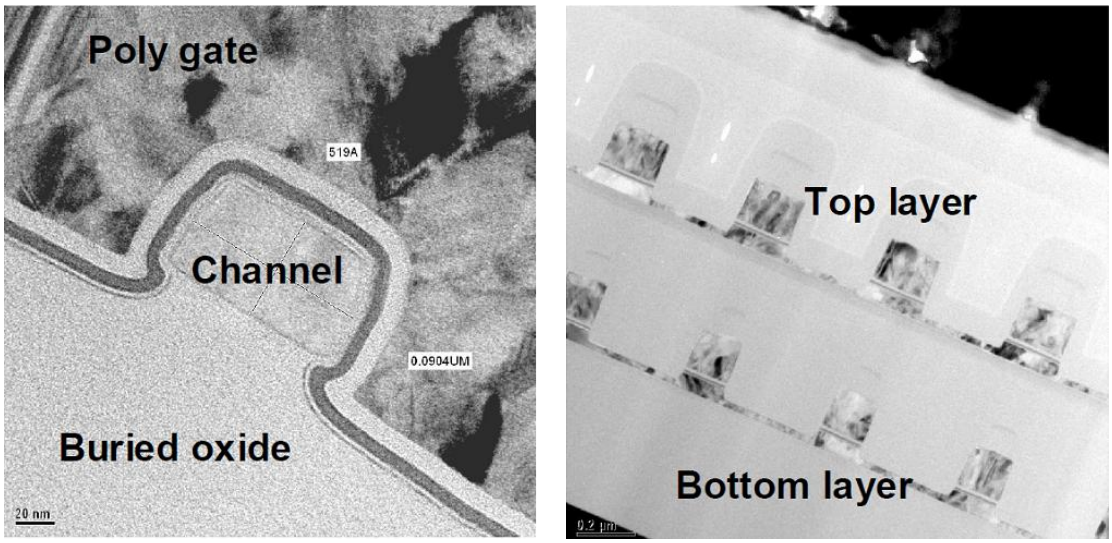


Fig. 1-5 Cross-sectional TEM images of (a) Tri-gate structure of the TFT device, (b) Channel-length direction of double-layer TFT NAND devices [1.60].

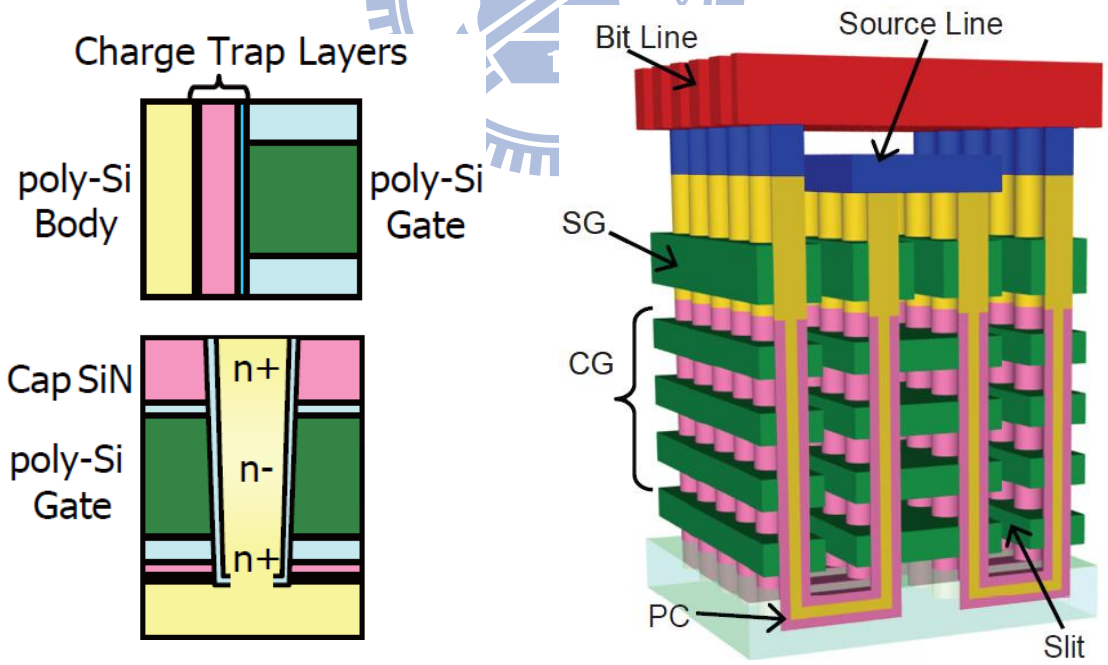


Fig. 1-6 Schematic cross-section of Toshiba's BiCS flash memory (right) and its vertical SONOS cell (left) [1.62, 1.63].

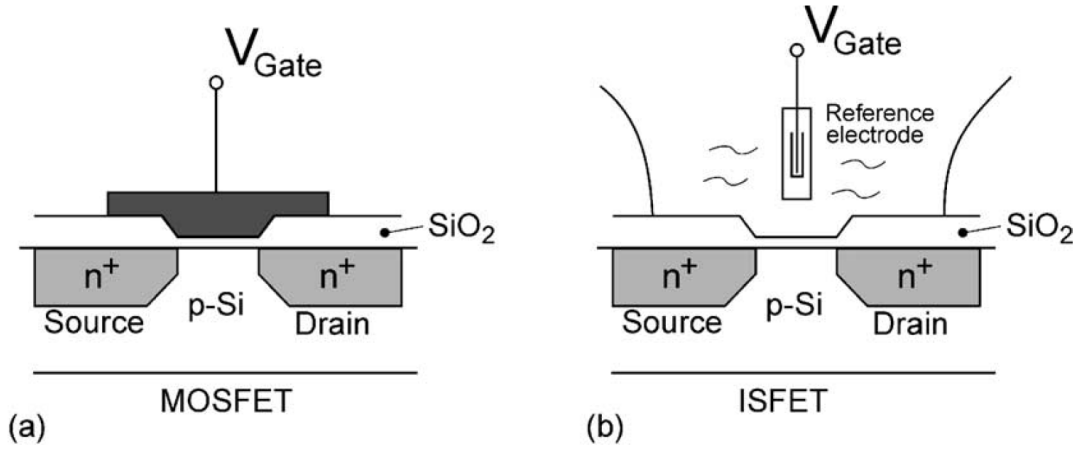


Fig. 1-7 Schematic representation of (a) MOSFET and (b) ISFET [1.68].

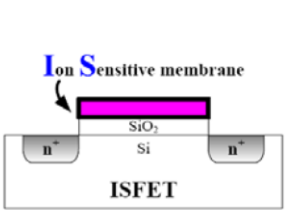
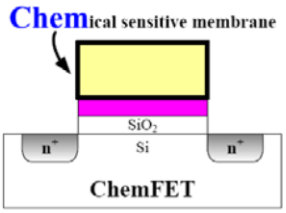
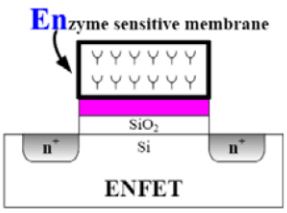
	ISFET	ChemFET	EnFET
Inventor	P. Bergveld[4]	S. D. Moss, C. C. Johnson and J. Janata[16]	S. Caras and J. Janata[23]
Year	1970	1978	1980
Structure			
Ion/Analyte	H^+, OH^-	K^+, Na^+. Li^+, $NH4^+$, Ca^{2+}, Mg^{2+}, NO_3^-, SO_4^{2-}, Cl^-	Glucose, Urea, Penicillin
Sensitive membrane	Si_3N_4, Al_2O_3, Ta_2O_5, SnO_2	Polymeric membranes with ionophores	Glucose oxidase, Urease, Penicillinase

Fig. 1-8 Table of ISFET, ChemFET and EnFET structures, detectable analytes, and sensitive membranes with bio-receptors [1.70].

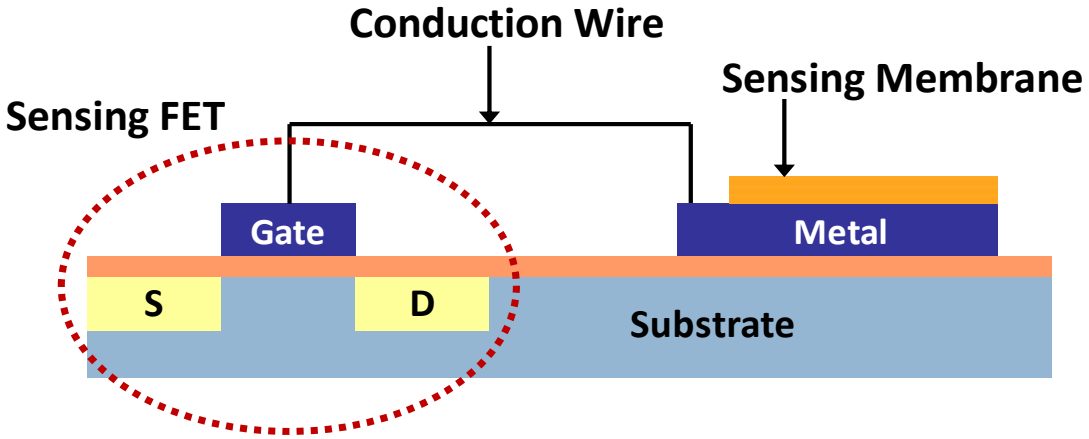


Fig. 1-9 An illustrative representation of a sensor scheme built on extended gate field-effect transistor (EGFET).

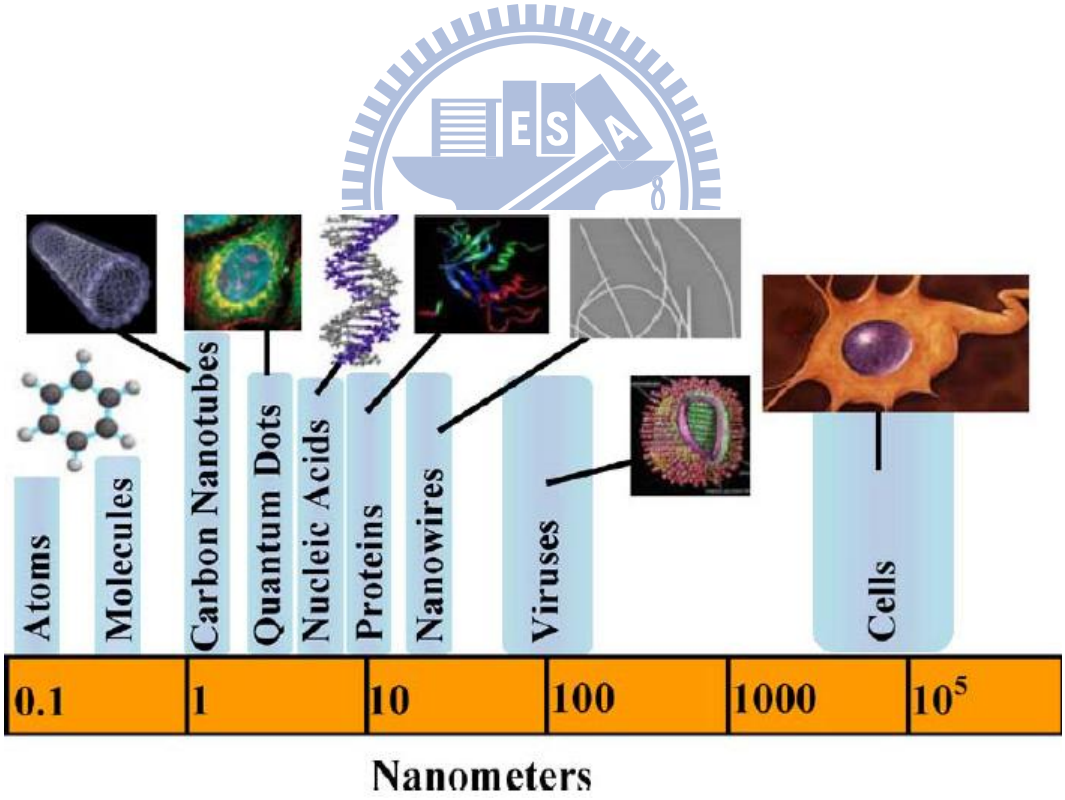


Fig. 1-10 Size of several nano-materials as compared to the size of some biological entities, such as nucleic acids, proteins, virus, and cells [1.74].

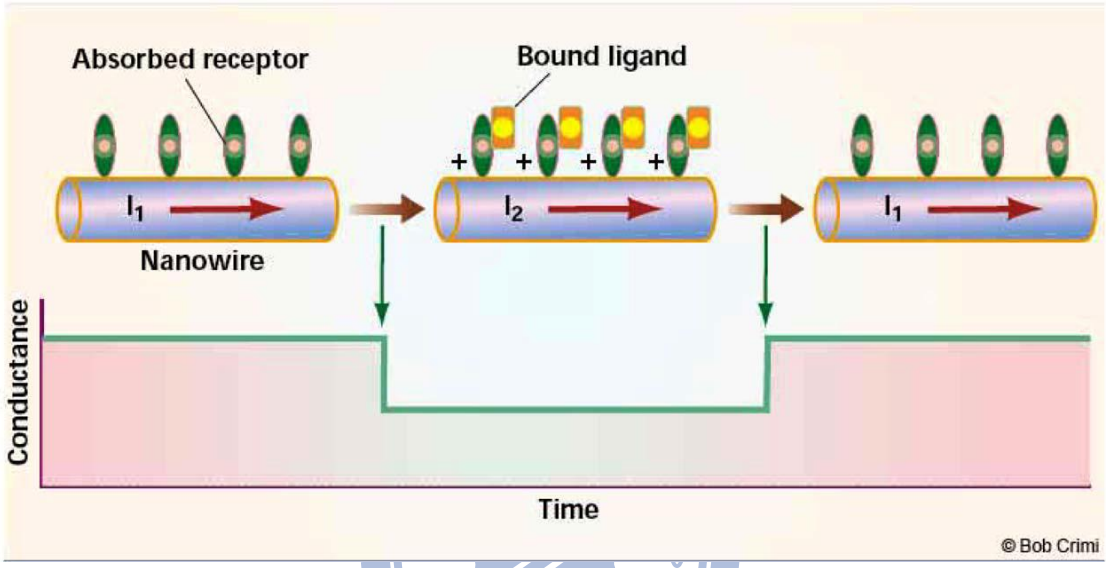


Fig. 1-11 Illustration of a reversible nanoscale biosensing process with NW sensor. (Left) A p-type silicon NW is functionalized with a receptor. (Center) Introduction of the appropriate ligand causes a change in NW conductance. (Right) NW conductance will return to its original value upon removal of the bound ligand, achieved by washing with buffer [1.78].

Chapter 2

Multiple-Gated Poly-Si Nanowire Thin-Film Transistors Fabricated by Sidewall-Spacer Etching Technique

2-1 Introduction

Si nanowire (NW)-based device technology has recently received considerable attention and is widely exploited for various applications in nano-electronics. The NW structure features a high surface-to-volume ratio, making it extremely sensitive to the variation of surface conditions, and suitable for a number of device applications, including NW field-effect transistors (FETs) [2.1], nonvolatile memories [2.2], and sensors [2.3]. Preparations of NW structures can be categorized into bottom-up [2.4, 2.5] and top-down [2.6, 2.7] approaches. The former approach is flexible in preparing the NW composition and structure, but lacks the controllability over precise positioning and alignment of NW patterns, and is therefore not suitable for mass manufacturing. On the other hand, top-down methods typically employ advanced but costly lithography tools like e-beam or deep ultraviolet (DUV) steppers to generate the NW patterns. To address these issues, we've recently proposed and developed a simple NW TFT fabrication method by cleverly taking advantage of sidewall spacer etching technique to form poly-Si NWs serving as the device channel (as shown in Fig. 2-1), and demonstrated that most advantages pertaining to the NW structure

could be retained with the new scheme [2.8, 2.9]. One major concern associated with the proposed devices is the use of poly-Si NWs as the channels. Defects contained in the poly-Si material are known to hinder carrier transport and lead to degradation in device's current drive. This concern may be relaxed with multiple-gated (MG) configuration, which can increase the gate controllability over the channel and potentially improve the device performance [2.10].

In this chapter, we investigate the characteristics of independent double-gated (DG) NW TFTs with ultra-thin body that were developed recently by our group [2.11]. Fig. 2-2 depicts the schematic layout view and perspective view of an independent DG NWTFT. In this scheme the tiny NW channels are surrounded by an inverse-T gate and a top gate. Since the two gates can be biased independently, more freedoms are allowed for device operation. For example, a specified voltage can be applied to one of the gates for modulation of the threshold voltage (V_{TH}) of the transfer curve driven by the other gate [2.11-2.13]. Due to the strong coupling between the two separate gates, V_{TH} of the device can be widely modulated with independent gate control scheme. This phenomenon is called "back-gate effect" in independent DG silicon-on-insulator (SOI) MOS transistors [2.12, 2.13]. Impacts of such effect on the NW device performance with various operation modes are examined in this study. Beside, for practical applications, it is important to understand the properties associated with poly-Si NW devices, especially the fluctuation of device characteristics. However, few works were devoted to this topic [2.14]. In this chapter we intend to address this issue and study the impacts of process treatment, channel length, and operation mode on the characteristics of the novel poly-Si NW TFTs.

2-2 Experimental

2-2.1 Device Structure and Fabrication

Figs. 2-3 (a) to (f) brief the fabrication processes by depicting the structures of the NWTFT formed at different steps. In short, the fabrication started on 6-inch silicon wafers capped with a 100 nm silicon dioxide layer. After depositing a 150-nm-thick *in situ* doped n^+ poly-Si, the inverse-T-shaped gate (denoted as G1) was formed by applying twice standard G-line lithography/dry etching steps (Figs. 2-3 (a) and (b)). This was followed by the deposition of a low-pressure chemical vapor deposition (LPCVD) oxide layer serving as the dielectric of G1. A 100-nm-thick amorphous-Si layer was then deposited by LPCVD system. Next, an annealing step was performed at 600 ℃ in N_2 ambient for 24-hour to transform the amorphous-Si into poly-Si (Fig. 2-3 (c)). Subsequently, a source/drain (S/D) implant was executed by P_{31}^+ ion implantation at 15 keV and a dose of 10^{15} cm^{-2} (Fig. 2-3 (d)). It should be noted that the implant energy was kept low so that the implanted dopants were temporarily distributed near the top surface of the poly-Si layer. After forming the S/D photo-resist patterns, an anisotropic reactive-plasma etching step was employed to form the NW channels simultaneously with S/D definition (Fig. 2-3 (e)). Note that the height of the upper step of G1 was designed to be twice higher (100 nm) than the lower one (50 nm). In this way, by controlling the duration of etching process the two NW channels were able to be precisely positioned on the upper stud of G1 in a self-aligned manner, and the channel size (*i.e.*, width and thickness) could also be determined by tuning the over-etching time. The NW channels were further capped with another LPCVD TEOS oxide, and then a 100-nm-thick *in situ* doped n^+ poly-Si was deposited and patterned to serve as the top gate (denoted as G2) (Fig. 2-3 (f)). All devices were then covered

with a 200-nm-thick TEOS oxide passivation layer. Since the depositions of TEOS oxide were performed at a temperature of 700 ℃ and the process duration was long enough for dopant activation purposes, it is worth noting that the S/D dopant activation process was accomplished simultaneously with the LPCVD TEOS oxide deposition steps after the formation of NW channels, preventing deeper diffusion of dopants into the NW channel region. The fabrication was completed after the formation of contact holes and test pads using standard metallization steps. All fabricated devices received an NH_3 plasma treatment at 300 ℃ for 3-hour before characterization. For comparison purpose, planar DG thin-film transistors (TFTs) with symmetrical gate oxide of 20 nm and poly-Si channel thickness of 50 nm were also fabricated and characterized in this study (as shown in Fig. 2-3 (g)).

The cross-sectional transmission electron microscopic (TEM) images of a fabricated device are given in Fig. 2-4. From the picture, gate oxides of G1 and G2 are both 18.5 nm, and peripheral lengths of the NW channel cross-section abutting against G1 and G2 are 45 nm and 40 nm, respectively. The NW channel is almost completely surrounded by G1 and G2, ensuring excellent gate coupling during operation. In the figure of the enlarged view of the NW, three corners denoted as A, B, and C, are specified. Corner A is the one that directly faces the re-entrant of G1. Owing to the nature of poly-Si etching the corner is rounded and has an angle larger than 90^o. This would help relax the corner effect [2.15] and improve gate oxide reliability. Although the other two corners (B and C) are sharp, they are unlikely to cause noticeable negative effects as they are sandwiched between the two gates. Note that the largest thickness of NW channel is apparently smaller than 20 nm.

2-2.2 Electrical Characterization Methods and Measurement Setup

Electrical characteristics of fabricated devices in this dissertation are mainly characterized by an automated measurement setup comprising an HP4156 semiconductor parameter analyzer and the Interactive Characterization Software (ICS) control program. The temperature was controlled at a stable value by the temperature-regulated hot-chuck. From the I_D-V_G curve at V_D = 0.1 V, performance parameters of the NW devices including subthreshold swing (SS), threshold voltage (V_{TH}) and field-effect mobility (μ_{FE}) can be extracted according to their definitions. SS can be calculated from the subthreshold current in the weak inversion region by

$$SS = \frac{\partial V_G}{\partial (\log I_D)}, \tag{2-1}$$

The V_{TH} here, calculated by constant current method, is defined as the gate voltage (V_G) to achieve a drain current (I_D) of (W/L) × 10nA, *i.e.*,

$$V_{TH} = V_G @ I_D = \frac{W}{L} \times 10nA, \tag{2-2}$$

where W and L are the channel width and length, respectively.

Finally, the field-effect mobility (μ_{FE}) is determined by

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_D}, \tag{2-3}$$

where C_{ox} is the gate capacitance per unit area, and g_m represents the transconductance which is extracted by the differentiation of I_D to V_G, as expressed below,

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const}. \tag{2-4}$$

2-3 Basic Electrical Characteristics

2-3.1 Device Characteristics with Different Operation Modes

Typical transfer characteristics of the NWTFT having L = 0.8 μm under single-gate (SG) and double-gate (DG) modes are shown and compared in Fig. 2-5. SG modes refer to the two modes when the sweeping voltage is applied to one of the two gates (the driving gate), while the other gate is grounded during the measurement. Table 2-1 lists the bias conditions for the three operation modes studied in this section. In Table 2-1, G1 and G2 serves as the driving gate for SG1 and SG2 modes, respectively; for DG mode, the sweeping voltage is applied simultaneously to G1 and G2. As can be seen in Fig. 2-5, drain-induced-barrier-lowering (DIBL) in all operation modes are essentially eliminated due to the use of ultra-thin NW channels. The SS of device under each operation mode is 175 mV/dec in SG1 mode, 230 mV/dec in SG2 mode, and 95 mV/dec in DG mode. It is evident that DG mode exhibits conspicuously better performance with respect to the two SG modes in terms of a higher drive current per unit gated width and a smaller SS. The differences in SS and drive current between the two SG modes reflect that G1 has better controllability over the NW channel than G2 does due to its larger gated width (see Fig. 2-4).

Note that such SS performance in DG mode is comparable to that of modern CMOS devices, despite the use of polycrystalline channels for the devices characterized in this study. This improvement is attributed to the reduction in the effective defect density per unit gated area [2.11]. The SS is expected to reduce further as a thinner gate dielectric is used, while the on-current can be further improved by scaling the channel length. These trends were actually observed in a recent report [2.9]. It is also interesting to see that the drain current under DG mode is

much larger than the results of SG modes. Reasons for such phenomenon are addressed in the subsequent section (Section 2-4).

The abnormally high leakage current behavior in OFF-state shown in Fig. 2-5 stems from the gate-induced drain leakage (GIDL) mechanism, which is caused by the unique structure with large gate-to-S/D overlap area (Fig. 2-2) and vertically non-uniform S/D doping profile above/under the overlap region. The GIDL effect in such structure has been identified in our previous study [2.9] by observing the dependence on the extent of gate-to-drain overlap region under high electric field in the OFF operation regime. It is also worth noting that SG2 mode depicts smaller GIDL current as compared to SG1 and DG modes. This could be ascribed to the aforementioned vertically non-uniform doping profile in the S/D region. To further verify this proposition, a simple simulation analysis of a poly-Si DG-TFT with its cross-sectional structure similar to the NW devices used in this study (Fig. 2-6 (a)) was performed by using the ISE-TCAD tool [2-16]. Fig. 2-6 (b) depicts the designed S/D doping profile with a gradually decreased concentration from the top ($N_D \sim 5\times10^{19}$ cm^{-3}) to the bottom ($N_D \sim 10^{18}$ cm^{-3}) of S/D regions. Since the low energy ion implantation was deliberately executed in the device fabrication to avoid NW channel being doped, such doping profile could be formed after the dopant activation process. Based on this S/D doping profile, the simulated I-V characteristic shown in Fig. 2-7 (a) clearly exhibits a severe GIDL current at high V_D. Furthermore, from the simulated trap-assisted band-to-band tunneling (BTBT) generation rate with device operating in the OFF-state (Fig. 2-7 (b)), it is found that BTBT generation occurs more profoundly in the drain region with lower doping concentration, which is qualitatively in accord with the measured OFF-state characteristic showing that SG1 mode has larger GIDL current (Fig. 2-5). This is because with low (or insufficient) S/D doping concentration,

it is relatively easy to achieve sufficiently large band bending and depletion width for depletion region near the gate/drain interface to induce considerable trap-assisted BTBT under high gate-to-drain bias, leading to a drastic GIDL current in the OFF-state [2.9]. Since the simulated structure and doping condition are in line with those of the fabricated device, the experimental result of OFF-state leakage is generally well described by the simulation analysis.

2-3.2 Modulation of V_{TH} with Back-Gate Bias

Fig. 2-8 (a) shows the ability of the NW device in modulating the V_{TH} of operation. In this case, the sweeping voltage is applied to G1 (V_{G1}) while G2, dubbed the V_{TH}-control gate, is fixed at a bias (V_{G2}) ranging from -3 V to 3 V. It can be seen that the transfer curves are effectively shifted by varying V_{G2}. This is owing to the use of the tiny NW channels, so the potential level of the entire channel layer is sensitive to either gate, allowing a strong back-gate effect and hence V_{TH} can be easily modulated by V_{G2}. To further highlight this point, we also characterize planar device with similar operation conditions and typical results are shown in Fig. 2-8 (b). The planar device contains a 50-nm-thick poly-Si channel film sandwiched between a top-gate and a bottom-gate, and the gate oxides are both 20-nm-thick. In Fig. 2-8 (b) we can see that the V_{TH} is only slightly affected by the bottom-gate bias. This indicates that the potential of the top channel interface is only weakly dependent on the bottom gate voltage for the planar device. Such a trend is reasonable when considering the large amount of defects contained in the poly-Si layer which tend to trap charges and screen the electric field originating from the bottom gate. A totally different picture emerges with the implementation of tiny NW channels because of the dramatic reduction in the amount of defects. With the tunable V_{TH} capability, the NW devices

could be applied for low standby power circuits [2.13]. An example is depicted in Fig. 2-9. In standby circuit operation, a lower subthreshold leakage can be attained by raising the V_{TH} of the transistors. While in active mode, V_{TH} can be adjusted to a moderate value to provide sufficient driving current.

The extracted V_{TH} and SS from Fig. 2-8 (a) as a function of V_{G2} are depicted in Fig. 2-10. The plot is divided into two regions by V_{THDG} (= 0.4 V) which is the V_{TH} measured under DG mode (see Fig. 2-5). It can be seen that the V_{TH} of the transfer curves driven by G1 ($V_{TH\,(G1)}$) is almost linearly modulated by V_{G2}. But a closer look reveals that the exact V_{TH}-shift rate ($dV_{TH(G1)}/dV_{G2}$) is -0.7 V/V for $V_{G2} < V_{THDG}$, slightly smaller than the rate of -0.8 V/V in the region of $V_{G2} > V_{THDG}$. Moreover, the SS values in the region of $V_{G2} > V_{THDG}$ are much larger than those as $V_{G2} < V_{THDG}$. When V_{G2} is smaller than V_{THDG}, the portion of channel surface gated by G2 is essentially depleted, and the inversion electron layer is mainly induced in the channel near G1 side as the device is turned on. In this situation, the V_{TH} modulation ability by V_{G2} is relatively weak owing to the longer distance between G2 and the inversion layer. On the other hand, when V_{G2} is larger than V_{THDG}, an inversion layer would form near the surface of the NW channel close to G2 side unless a sufficiently negative G1 bias is applied to deplete the channel. In this circumstance, the effective gate dielectric consists of the gate oxide adjacent to G1 and the fully depleted NW body, and thus is thicker than the nominal gate oxide. Accordingly, the SS becomes worse. Furthermore, switching of the device is mainly determined by the conduction path in the channel near G2 side, therefore V_{TH} is more sensitive to V_{G2}.

The characteristics about V_{TH} modulation in independent DG device with an ultra-thin body have been explored by Masahara *et al*. [2.13] who proposed a linear potential distribution model to describe the back-gate effect. From this theoretical

model, the phenomena can be further clarified by using simple potential distribution diagrams throughout gate-to-channel direction, as illustrated in Fig. 2-11 and Fig. 2-12. In Fig. 2-11, G2 is defined as the V_{TH}-control gate, and G1 is the driving gate. The silicon channel region is assumed to be fully depleted due to the subthreshold condition, so that it can be considered as a dielectric material. According to the dielectric constant ratio of Si to SiO_2 (11.9/3.9), the thickness of oxide layer for both sides (T_{OX1} and T_{OX2}) are multiplied by 3 in the diagrams. Consequently, both Si and SiO_2 can be treated as an identical dielectric, and hence the potential distributions can be illustrated as straight lines. With these potential distribution lines, the V_{TH}-shift rate, or the so-called back-gate-effect factor γ, can be easily obtained by using the similarity of the two triangles, ΔABC and ΔDEC, in Fig. 2-11 and then is expressed in the equation form associated with equivalent channel thickness (T_{Si}) and gate oxide thickness (T_{OX1} and T_{OX2}). As a result, when V_{G2} is lower than V_{THDG} (corresponding to Fig. 2-11 (a)), the V_{TH}-shift rate is given by $|dV_{THG1}/dV_{G2}| = 3T_{OX1}/(3T_{OX2} + T_{Si})$. When V_{G2} is higher than V_{THDG} (Fig. 2-11 (b)), the V_{TH}-shift rate is expressed in another similar form, $|dV_{THG1}/dV_{G2}| = (3T_{OX1} + T_{Si})/3T_{OX2}$. According to the equations, it can be perceived that the shifting rate becomes smaller as V_{G2} is lower than V_{THDG}, and larger as V_{G2} is higher than V_{THDG}. Moreover, the relation between SS and G2 bias can also be described through simple diagrams, as shown in Figs. 2-12 (a) and (b). First, it is well known that the SS is proportional to $dV_G/d\varphi_S$, where φ_S is the surface potential, and it can be obtained by using the similarity of ΔABC and ΔADE in Fig. 2-12. Similar to V_{TH}-shift rate, the SS is smaller when V_{G2} is lower than V_{THDG}. This simple model is suitable for any device structure with ultra thin body and independent DG. And the trends of the device characteristics shown in Fig 2-10 are basically consistent with this model.

To give more comprehensive study about the coupling effect between the two gates, the functions of G1 and G2 performed in Fig. 2-8 (a) can be exchanged to further investigate the transfer characteristics of the device. The results are shown in Fig. 2-13. Fig. 2-14 exhibits and compares the capability of V_{TH}-control gate voltage in modulating the device's V_{TH} based on the results shown in Fig. 2-8 (a) and Fig. 2-13. Owing to the aforementioned better controllability of G1 over the NW channel than G2 in this asymmetrical DG configuration, it is apparent that the V_{TH}-shift rates are different in the two cases and the rate is larger as G1 is employed as the V_{TH}-control gate. Table 2-2 summarizes equations of V_{TH}-shift rate (or back-gate-effect factor γ [2.13]) corresponding to the four operation regions specified as (i) ~ (iv) in Fig. 2-14. The extracted γ values from the experimental data in different regions shown in Fig. 2-14 are also given in Table 2-2. From the equations, the γ value in region (i) is equal to the reciprocal of that in region (iv). Similarly, the V_{TH}-shift rate in region (ii) is equal to the reciprocal of that in region (iii). Such relations are experimentally confirmed by the extracted γ values, since 0.7 is nearly equal to $(1.4)^{-1}$ and 0.8 is equal to $(1.25)^{-1}$.

2-4 On the Origins of Performance Enhancement in Independent Double-Gated Poly-Si NWTFTs

2-4.1 Impacts of Back-Gate Effect on Device Performance

Comparisons of output characteristics normalized to the effective channel width (W) between SG and DG modes are shown in Fig. 2-15 (a). The long-channel device

(L = 5 μm) is chosen here in order to eliminate the effect of series resistance on the drain current. It can be noticed that the drain current under DG mode is substantially larger than that of either SG mode. To more carefully illustrate this observation, Fig. 2-15 (b) shows the ratio of drain current of DG mode to the sum of the two SG modes against drain voltage (without normalizing to W). The ratio is found to increase with increasing drain voltage from a value around 1.2, and becomes saturated at around 2.4. Moreover, the saturation occurs at a smaller drain voltage as V_G–V_{TH} is reduced. Similar measurements were also performed on the planar devices having a 50-nm-thick channel, and the results (not shown) show that the ratio is around unity. This suggests that, due to the thick channel film, the two opposite channels in the planar device essentially do not have any coupling during DG operation. In other words, the overlap of wave functions of the induced electrons (or electrostatic potential) in one of the channel with that of the other channel is negligible (as shown in Fig. 2-16 (a)). In such case, DG operation is simply the combination of two independent SG MOSFETs in parallel. In contrast to the characteristics of the planar device, the tremendous enhancement in current drive of the NW device shown in Fig. 2-15 (a) with DG operation is speculated to originate from the strong coupling effect of the two opposite gates on account of the use of ultra-thin NW channels, as illustrated in Fig. 2-16 (b).

To gain insight into the above phenomenon, we have re-checked the output characteristics of the NW device. In Fig. 2-15 (a), it can be noticed that the drain voltage at the onset of pinch-off (*i.e.*, the saturation drain voltage, V_{Dsat}) [2.17] is smaller in SG modes than in DG mode under the same V_G–V_{TH} condition. We re-plot the I_D-V_D curves at V_G–V_{TH} = 4 V in Fig. 2-17 and specify the position of V_{Dsat} for each mode as an example. Apparently the abnormally high drain current ratio could

be partly attributed to the lower V_{Dsat} in the two SG modes which would limit the saturation current. Such "early saturation" phenomenon in SG modes could also be described by the aforementioned back-gate effect [2.18]. Although previously some analytical I-V models for thin-film SOI devices with back-gate have already been proposed in literatures [2.18-2.20], here we utilize a different approach with the potential distribution diagrams under SG1-mode operation illustrated in Fig. 2-18 to help elucidate thee cause in a much simpler way.

As stated in Table 2-1, in SG1 mode, G2 is grounded while G1 serves as the driving gate. Fig. 2-18 (a) shows the potential distribution in the channel at the source end as V_{G1} is above V_{TH}. The surface potential (φ_S) of the channel would be pinned at φ_{TH} which is the level corresponding to the onset of strong inversion [2.17] and the voltage drop is mainly across G1 oxide. On the other hand, the inversion condition for the onset of pinch-off at the drain side of the channel is $\varphi_S \sim \varphi_{TH} + V_{Dsat}$ due to the shift of quasi-Fermi potential with the applied drain bias, as shown in Fig. 2-18 (b) [2.17]. Consequently, V_{Dsat} could be easily derived by using the similarity of the triangles formed by the potential line in Fig. 2-18 (a), expressed as:

$$V_{Dsat} = (V_G - V_{TH}) \times \frac{3T_{OX2} + T_{Si}}{3T_{OX2} + T_{Si} + 3T_{OX1}} = \frac{V_G - V_{TH}}{1+\gamma}, \qquad (2\text{-}5)$$

where $\gamma = \frac{3T_{OX1}}{3T_{OX2} + T_{Si}}$ is the back-gate-effect factor of region (i) shown in Fig. 2-14 and Table 2-2. V_{Dsat} for SG2 mode can be analogically derived with the form similar to Eq. (2-5) except $\gamma = \frac{3T_{OX2}}{3T_{OX1} + T_{Si}}$ corresponding to the region (iii) shown in Fig. 2-14 and Table 2-2. By using the gradual-channel and charge-sheet approximation [2.17], the inversion charge density (Q_i) along the channel can be described as:

$$Q_i(V) = -C_{ox}[V_G - V_{TH} - (1+\gamma)V], \qquad (2\text{-}6)$$

where C_{ox} is the gate oxide capacitance per unit area, and V is the location-dependent quasi-Fermi potential due to the drain bias. Subsequently, by integrating $Q_i(V)$ through the entire channel with the integral equation form:

$$I_D = (W/L)\mu_{eff}\int_0^{V_D}[-Q_i(V)]dV\,, \tag{2-7}$$

then the drain current (I_D) at ON state can be derived and written as:

$$I_D = K(V_G - V_{TH} - \frac{1+\gamma}{2}V_D)V_D\,, \quad \text{when } V_D \le V_{Dsat}, \tag{2-8}$$

and

$$I_{Dsat} = K\frac{(V_G - V_{TH})^2}{2(1+\gamma)}\,, \quad \text{when } V_D \ge V_{Dsat}, \tag{2-9}$$

where K is trans-conductance parameter equals to $(W/L)\mu_{eff}C_{ox}$, μ_{eff} is effective carrier mobility, L is the channel length, and W is the channel width. It should be noted that γ is equal to zero under DG mode [2.13] due to the fact that there is no back-gate effect under DG operation as long as the channel body is floating. Although the above derivation is based on the simple potential diagrams shown in Fig. 2-18, the result is actually consistent with the theoretical models presented previously [2.19, 2.20]. As compared with the commonly used drain current equation for bulk MOSFETs [2.17], Eq. (2-8) and Eq. (2-9) only replace the body-effect coefficient (m) with $1 + \gamma$. Since it has been known that m and $1 + \gamma$ correlate to subthreshold swing in a same manner ($\sim dV_G/d\varphi_S$) [2.13, 2.17], the above derivation indicates that the impact of back-gate effect on the fully-depleted DG SOI device characteristics is similar to that of the body-effect on the conventional bulk MOSFET.

In addition, by applying the γ value (extracted from the point of V_{TH}-control gate = 0 V in Fig. 2-19) for each SG mode into Eq. (2-8) and Eq. (2-9), interestingly, it is found that the measured output characteristics can be well fitted by the equations

as an appropriate K value is used in each operation mode. Such treatments are shown in Fig. 2-20, in which the output characteristics measured under different operation modes are compared with the computational I-V curves based on Eq. (2-8) and Eq. (2-9). The K values used in the computational I-V curves are 4.9×10^{-8}, 4.65×10^{-8}, and 1.15×10^{-7} S/V, for SG1, SG2, and DG modes, respectively. As can be seen in the figures, the calculation results well describe the experimental data.

The above analysis clearly explains the reason for the much higher V_{Dsat} of DG operation is the elimination of back-gate effect. Moreover, the current ratio should reach a constant as the applied drain bias is larger than V_G-V_{TH}, the V_{Dsat} of DG mode, since then the drain currents of all operation modes become saturated. This is indeed confirmed in Fig. 2-15 (b). However, one issue remained above is the assumption of a constant K value for each operation mode as we use Eq. (2-8) and Eq. (2-9) to fit the experimental I-V curves in Fig. 2-20. Since K is closely related to the transconductance and μ_{eff}, so in the next subsection we will present the measured results of these parameters and probe their influences on device characteristics.

2-4.2 Investigations on Mobility Enhancement with Double-Gated Operation

Fig. 2-21 (a) shows the transconductance (GM) of the device under different operation modes at V_D = 0.1 V. It is observed that the GM approaches a constant value as V_G is sufficiently high. The less attenuation in high vertical field region is ascribed to the fact that carrier transport in poly-Si channel is mainly affected and limited by the defect-induced potential barrier at grain boundaries [2.21-2.23]. This would answer the question why a constant K value can be used for fitting the experimental data shown in Fig. 2-20. Extracted ratio of GM of DG mode to the sum

of two SG modes (GM_{DG} / (GM_{SG1} + GM_{SG2})) as a function of $V_G - V_{TH}$ is depicted in Fig. 2-21 (b). In the same figure the data of a planar device are also included for comparison. The ratio is essentially equal to unity for the planar device, indicating the two opposite gates are operated independently. Unlike the planar counterpart, it can be seen that GM ratio of the NW device is noticeably higher than unity, and a large enhancement reaching around 40% at low vertical electric field is observed. This implies that DG operation indeed offers enhancement in effective mobility of the transport carriers in NW devices. Besides, according to a mobility extraction method proposed by Ghibaudo [2.24], normalized low-field mobility data as a function of $V_G - V_{TH}$ are shown in Fig. 2-22. Around 30% and 20% mobility enhancement at respectively low and high $V_G - V_{TH}$ for DG mode compared to SG modes are evaluated, which are totally in agreement with the result of GM ratio plotted in Fig. 2-21 (b).

In a previous work [2.22], carrier conduction in poly-Si material has been shown to be mainly governed by the potential barrier presenting at the grain boundaries, and the effective mobility contained in K (*i.e.*, $(W/L)\mu_{eff}C_{ox}$) can be expressed as:

$$\mu_{eff} = \mu_0 e^{-qV_B/k_B T}, \tag{2-10}$$

where μ_o is a constant, q is the charge of an electron, V_B is the effective grain-boundary potential barrier height, k_B is the Boltzmann constant, and T is the absolute temperature. The values of V_B can be extracted from I-V characteristics measured at different temperatures. The principle of V_B extraction method is detailed as follows.

According to Eq. (2-10), the approximate linear current equation for a poly-Si channel FET can be written as:

$$I_D = (W/L)C_{ox}(V_G - V_{TH})V_D \times \mu_o e^{-qV_B/k_BT}, \quad (2\text{-}11)$$

then the natural logarithm of Eq. (2-11) is given as:

$$\ln I_D = -qV_B/k_BT + \ln[(W/L)\mu_o C_{ox}(V_G - V_{TH})V_D]. \quad (2\text{-}12)$$

Based on Eq. (2-12), one can measure the device in two different temperatures and then extract V_B by using the following simple equation:

$$V_B = (k/q) \times \ln(\frac{I_{D2}}{I_{D1}}) \times (\frac{1}{T_1} - \frac{1}{T_2})^{-1}. \quad (2\text{-}13)$$

V_B extraction results of the independent DG NWTFT with three operation modes are shown in Fig. 2-23. For all operation modes, V_B decreases with increasing V_G–V_{TH}, owing to the increase in the concentration of inversion electrons in the channel [2.21]. However, with respect to the two SG modes, V_B is evidently lower in DG mode, confirming our inference made above that DG operation can provide mobility enhancement originating from the more effective V_B suppression and thus the higher thermionic emission efficiency. In Fig. 2-24, the GM ratio is plotted together with the ratio $(W_{DG} \times e^{-qV_{BDG}/k_BT})/(W_{SG1} \times e^{-qV_{BSG1}/k_BT} + W_{SG2} \times e^{-qV_{BSG2}/k_BT})$ against V_G–V_{TH}, where W is effective channel width for each operation mode. It is interesting to notice that the two curves are very close and follow the same trend. This observation and the above analysis confirm that the mobility enhancement due to the reduction of potential barrier height for transport carriers is another major factor responsible for the performance improvement with DG operation.

2-4.3 Impacts of Operation Modes on Series Resistance

From the previous sub-section, the V_B lowering phenomenon in poly-Si NW

channels under DG mode may suggest that the vertical electric field is able to penetrate more deeply into the NW channel in DG mode and therefore lower the potential barrier of the deep channel region. This speculation has been demonstrated by a simulation analysis in our recent study [2.25]. From another perspective, it might be appropriate to assume that the parasitic series resistance of the DG-NWTFT could also be influenced by the V_B lowering effect. Figs. 2-25 (a) and (b) schematically illustrate this assumption. For device operating under SG mode, the local conductance of NW channel adjacent to S/D junctions should be the highest near the interface of the driving gate oxide and the channel, and decrease rapidly in the direction away from the interface, as shown in Fig. 2-25 (a). In this condition, the small conducting area for current flowing through channel to S/D region would lead to a large spreading resistance. For DG mode (Fig. 2-25 (b)), however, the local conductance of NW channel away from the oxide/channel interface could still be promoted by the profound V_B lowering effect. Consequently, the resulting larger conducting area for current flow in DG mode is expected to lower the spreading resistance.

To confirm this expectation, we extracted the S/D series resistances (Rs) of the independent DG NWTFT under three operation modes with a test scheme proposed previously [2.24]. Fig. 2-26 shows the extracted S/D Rs from the I_D-V_D characteristics of each mode with different channel length at $V_G - V_{TH} = 4$ V. The Rs results are about 110 kΩ for DG mode, 280 kΩ and 370 kΩ for SG1 and SG2 modes, respectively. The much lower Rs under DG mode supports the above postulation. Moreover, the equivalent components of Rs are schematically shown in Fig. 2-27. If the V_B lowering effect is not prominent or the channel is too thick to observe this phenomenon, the Rs extracted in DG mode should be very close to the effective resistance of the two SG-mode Rs in parallel (here we assume the spreading resistance is the dominant part).

Nevertheless, as shown in Fig. 2-28, the extracted Rs ratio under various V_G-V_{TH} are all less than unity, and is obviously smaller with lower applied gate voltage, implying that the Rs reduction caused by V_B lowering effect is relatively more distinguishable at lower vertical electric field. Furthermore, this result is again consistent with the trend of GM ratio versus applied V_G-V_{TH} shown in Fig. 2-21 (b) and Fig. 2-24.

2-5 Investigations on Threshold Voltage Fluctuation of Independent Double-Gated Poly-Si NWTFTs

As mentioned in Sec. 1-3, with downscaling of transistor's dimensions and operating voltage, it is inevitable that devices as well as circuits would become more and more vulnerable to the fluctuation sources, which could drastically increase the variation of device characteristics. In this section, the variability in the characteristics of independent DG NWTFTs associated with V_{TH} fluctuation is studied. Moreover, the impacts of process treatment, channel length, and operation mode on V_{TH} fluctuation are also investigated.

2-5.1 Theory of Threshold Voltage Fluctuation and Assumptions

Since random dopant fluctuation (RDF) is regarded as one of the major variation sources and has been demonstrated to have an increasingly pronounced impact on V_{TH} fluctuation in highly-scaled MOSFETs [2.26], it is necessary to address the theory of V_{TH} fluctuation considering RDF in this sub-section. Here we adopt a simple V_{TH} fluctuation model proposed by Takeuchi *et al*. [2.27] to derive the standard deviation of V_{TH} (σV_{TH}) in an equation form associated with the structural

parameters of the device, described as follows.

In general, the V_{TH} of a conventional MOSFET can be expressed as,

$$V_{TH} = V_{FB} + 2\varphi_F - \frac{Q_{DEP}}{C_{ox}}, \tag{2-14}$$

where V_{FB} is the flat-band voltage, $2\varphi_F$ is the surface potential of the channel at the onset of inversion, Q_{DEP} is the charge within the depletion region, and C_{ox} is the gate oxide capacitance per unit area. The term Q_{DEP}/C_{ox} in Eq. (2-14) is directly connected to the dopant distribution in the depletion region. Given an extra charge sheet ΔQ placed within the channel depletion layer, the electric field E as a function of depth x, as shown in Fig. 2-29, would vary from the solid line to the dashed line due to the fact that the voltage drop between surface and the edge of the depletion region ($x = W_{DEP}$) must be constant. Consequently, the V_{TH} shift (ΔV_{TH}) caused by the additional ΔQ at depth x in the depletion region is expressed as:

$$\Delta V_{TH} = \frac{\Delta Q}{C_{ox}}\left(1 - \frac{x}{W_{DEP}}\right). \tag{2-15}$$

By assuming the distribution of dopant number in the extra charge sheet volume $LW\Delta x$ is binomial, the standard deviation of ΔQ ($\sigma\Delta Q$) at depth x can be approximated by

$$\sigma\Delta Q = \frac{q\sqrt{N_{SUB}(x)LW\Delta x}}{LW}, \tag{2-16}$$

where $N_{SUB}(x)$ is the doping concentration, W and L are the channel width and length, respectively. Then from Eq. (2-15) and Eq. (2-16), σV_{TH} can be obtained by integrating all the contributions of ΔQ in the depletion region from $x = 0$ to W_{DEP} and the result can be expressed as follows,

$$\sigma V_{TH} = \frac{q}{C_{ox}} \sqrt{\frac{N_{EFF} W_{DEP}}{3LW}}, \tag{2-17}$$

where N_{EFF} is the weighted average of $N_{SUB}(x)$ inside the depletion region, which is defined as:

$$N_{EFF} = 3 \int_0^{W_{DEP}} \frac{N_{SUB}(x)}{W_d} (1 - \frac{x}{W_{DEP}})^2 dx. \tag{2-18}$$

From Eq. (2-17), it can be observed that σV_{TH} is proportional to $(LW)^{-1/2}$, suggesting the V_{TH} fluctuation increases as device dimensions shrink.

It should be noted that, the above RDF model considers the dopant fluctuation effect in conventional MOSFETs. For the poly-Si NWTFT used in this study, no intentional channel doping was performed. However, the defect states contained in the grain boundaries of poly-Si NW act as trapping centers, and a large portion of them are occupied by the induced carriers before forming the conductive channel, thus affecting SS and V_{TH} [2.28]. Accordingly, the role played by these defects is supposed to be similar to the dopants in bulk MOSFETs, and Eq. (2-14) can be modified for devices having poly-Si channel, expressed as:

$$V_{TH} \cong V_{FB} + 2\varphi_F + \frac{qN_{Trap} W_{Deff}}{C_{ox}}, \tag{2-19}$$

where N_{Trap} is the trap states density (in cm^{-3}) in poly-Si channel and W_{Deff} is the effective depletion width at $V_G = V_{TH}$, respectively. As stated above, since the grain size of poly-Si and density of defects contained in the channel vary from place to place randomly, here we assume that the trap states may influence V_{TH} fluctuation in the same manner as impurity dopants. For this reason, N_{EFF} and W_{DEP} in Eq. (2-17) could be simply replaced by N_{Trap} and W_{Deff}, respectively, for describing σV_{TH} caused

by random defect distribution in poly-Si channel devices, expressed as follows:

$$\sigma V_{TH} = \frac{q}{C_{ox}} \sqrt{\frac{N_{Trap} W_{Deff}}{3LW}} . \qquad (2\text{-}20)$$

In Eq. (2-20), it is assumed that the trap states are distributed uniformly throughout the poly-Si channel, so that the N_{EFF} is directly equal to N_{Trap} based on Eq. (2-18). This assumption might be acceptable in the present case as the typical grain size of poly-Si film (< 50 nm) is much smaller than the channel length of the devices.

2-5.2 Impacts of NH_3 Plasma Treatment

In order to study the impact of defect concentration on variability of poly-Si NWTFTs, in this sub-section the characteristics of V_{TH} fluctuation for devices with and without NH_3 plasma treatment (for 3 hours) are compared and discussed. This treatment process has been commonly used for ploy-Si TFT performance improvement. Some detailed results and discussion about this technique can be found in [2.29]. The NH_3 plasma was generated in a diode reactor configured with a pair of parallel electrode plates powered by an RF power supply with frequency of 13.56 MHz. Note that the possible damage to the thin gate dielectric should be quite minor since the plasma treatment was performed after the device fabrication while the gate dielectric layer was surrounded by the gate electrode and the NW devices were covered with a passivation dielectric.

Fig. 2-30 and Fig. 2-31 show transfer characteristics operating in DG mode for devices with and without the plasma treatment, respectively. 20 devices were characterized in each plot. As can be seen in the figures, owing to the effective passivation of defects in the NW channels, both V_{TH} and SS are significantly reduced

with the plasma treatment. The extracted mean value and standard deviation of V_{TH} as a function of channel length under DG mode are summarized in Fig. 2-32. It is found that σV_{TH} increases with decreasing channel length, which is consistent with the modified Eq. (2-20) discussed in previous sub-section. Besides, from the linear I_D-V_G characteristics depicted in Fig. 2-30 (b) and Fig. 2-31 (b), the measured curves of devices with plasma treatment exhibit relatively tighter distribution.

To gain more understanding from the experimental results, we re-plot the extracted σV_{TH} as a function of $(LW)^{-1/2}$, which is known as "Pelgrom plot" [2.30], as shown in Fig. 2-33. The slope of linear fitting line for the devices without receiving the plasma treatment is apparently larger than that for the devices with treatment. This is ascribed to the passivation of defects by the plasma treatment, which indicates N_{Trap} reduction in Eq. (2-20), and illustrates the importance of defect control in improving the V_{TH} fluctuation. Furthermore, by extracting the mean SS values from Fig. 2-30 and Fig. 2-31, the effective trap density per unit area T_{Trap} (in cm^{-2}) can be estimated by the following expression [2.28]:

$$SS = \ln 10 \times \left(\frac{kT}{q}\right) \times \left(1 + \frac{C_{dm}}{C_{ox}}\right), \text{ where } C_{dm} = q \times T_{Trap}. \qquad (2\text{-}21)$$

The mean SS for the devices with the plasma treatment is 105 mV/dec, and the corresponding T_{Trap} is estimated to be around 8.1×10^{11} cm^{-2}. For devices without receiving the plasma treatment, the mean SS is about 188 mV/dec, hence T_{Trap} is 2.3×10^{12} cm^{-2}. Since the poly-Si NW channel is thin enough to be fully depleted, the product $N_{Trap}W_{Deff}$ in Eq. (2-20) is essentially equal to T_{Trap}. Thus we can calculate the contribution of channel defects to the V_{TH} fluctuation of devices based on the extracted T_{Trap} and Eq. (2-20). However, the slopes calculated by Eq. (2-20) are obviously smaller than the experimental data (dashed lines in Fig. 2-33), indicating

that other variation sources, such as line-edge and surface roughness of poly-Si NW channel, are also greatly responsible for the V_{TH} fluctuation of poly-Si NW devices. But if we subtract σV_{TH} calculated by modified RDF model from the experiment data, as shown in Fig. 2-34, it is interesting that the two linear fitting lines of modified data fairly coincide with each other. This outcome reveals that the modified RDF model is likely suitable for describing the defects induced V_{TH} fluctuation of devices built on poly-Si channels. It is also worth noting that the linear fitting lines of experimental data points in Fig. 2-33 and Fig. 2-34 clearly do not intersect at the origin but manifest considerable magnitude of Y-intercepts. This non-zero σV_{TH} at $(LW)^{-1/2} = 0$ may signify that there exists a variation source weakly dependent on L and W of devices. And it is possibly attributed to the wafer-scale non-uniformity of film thickness and NW dimensions induced by the variations in our deposition and etching processes, giving rise to an inherent σV_{TH} which is generally independent of L and W of the fabricated devices.

2-5.3 Impacts of Operation Modes

Since the independent gate configuration is capable of providing more than one operation mode, in this sub-section we also address the V_{TH} fluctuation issues under these different operation modes. The bias conditions of the two independent gates for the three operation modes studied in this sub-section are given in Table 2-1. Fig. 2-35 shows and compares the mean values and standard deviations of V_{TH} and SS for plasma-treated devices with channel length of 2 μm under three different operation modes. It is evident that the device operating in DG mode has the smallest variation among the three operation modes in terms of σV_{TH} and σSS. This is due to the fact that the DG operation mode can further reduce the effective depletion width W_{Deff} in

the NW channel. As illustrated in Fig. 2-36 [2.31], for a fully-depleted poly-Si channel with SG configuration (Fig. 2-36 (b)), the W_{Deff} in Eq. (2-19) and Eq. (2-20) can be replaced by the channel thickness T_{si}. As for MG configuration, W_{Deff} could be even smaller. For example, in the DG configuration shown in Fig. 2-36 (c), W_{Deff} is equal to half the T_{si}, thus leading to more improved fluctuation characteristics. Consequently, the experimental results shown in Fig. 2-35 essentially reflect the importance of gate controllability as well as channel thickness to device variation properties.

In addition, with regards to the flexible device operation, it is intriguing to investigate V_{TH} fluctuation characteristics under SG mode with various V_{TH}-control gate biases. Fig. 2-37 (a) shows typical I_D-V_G curves of 20 devices measured in SG1 mode with different applied G2 voltages (V_{G2}). Fig. 2-37 (b) summarizes the σV_{TH} as a function of V_{G2} for devices with channel length ranging from 0.8 μm to 5 μm. It is observed that the smallest fluctuation is achieved as V_{G2} is in the range between 0 V and -1 V, while the fluctuation worsens as V_{G2} shifts toward either more negative or positive direction. This is because when V_{G2} is shifted away from the optimum bias condition, the transverse electric field inside the NW would increase and thus the impact of channel film-thickness variation on the modulation of the channel potential would be magnified, leading to a larger V_{TH} variation [2.32]. Moreover, the fluctuation under large V_{G2} also worsens as the channel length shortens (Fig. 2-37 (b)). The reason is that, when applying a sufficiently high positive V_{G2}, the position of the onset of inversion layer formation would move toward the channel surface adjacent to G2, and it requires a more negative G1 bias to turn the device off (*e.g.*, see Fig. 2-37 (a)). Under this situation, G1 oxide and the fully depleted channel body form the effective gate dielectric, which is certainly thicker than the nominal gate oxide. Hence,

the aggravated short-channel effects combined with the enhanced influence of channel thickness variation bring about a much greater V_{TH} fluctuation in short-channel devices. As a result, it is concluded that the optimum bias condition occurs as the transverse electric field in the NW channel approaches zero [2.32].

2-6 Summary

In this chapter, characteristics of poly-Si NW devices featuring an independent DG configuration are characterized and analyzed. In the devices the ultra-thin NW channels are surrounded by an inverse-T gate and a top gate. With the independent DG scheme, several modes including DG and two SG modes can be implemented in the device operation. In addition, because of the strong gate-to-gate coupling due to ultra-thin NW channels, the transfer characteristics of the device driven by one of the gates are profoundly affected by the bias condition of the other gate. Therefore the DG-NWTFT can act as a functional device by applying separate biases to the two gates simultaneously, allowing the flexibility to adjust V_{TH}. The experimental results point out that the DG mode outperforms either of the two SG modes. For example, transfer curves with SS less than 100 mV/dec are only seen with the DG mode. The anomalous leakage current shown in SG1 and DG mode is attributed to GIDL mechanism. A simulation analysis with gate/drain overlap structure and vertically non-uniform S/D doping profile is performed to clarify this outcome. The simulation result shows that BTBT occurs more significantly in the drain region with lower doping concentration. According to the corresponding structure and doping condition, the experimental result of OFF-state leakage can be properly explained by the

simulation analysis.

Extraordinary enhancement in the current drive with DG mode is also observed. Based on the analysis, the above current enhancement with DG mode is mainly because of the elimination of the back-gate effect encountered in SG mode, as well as the improved effective mobility. Beside, the impacts of operation mode on device's series resistance are also investigated. The effect of grain-boundary barrier lowering may also reduce the spreading resistance, leading to a lower series resistance under DG mode.

For device variability, it is confirmed that defects contained in the channel are the dominant source for the fluctuation observed in NW DG-TFTs. Experimental results in this study also show that these defects can be effectively passivated with NH_3 plasma treatment, therefore reducing the device fluctuation in terms of σV_{TH}. Additionally, it is found that the fluctuation is closely related to the operation modes. When only one of the gates is employed as the driving gate to control the device's switching behavior, suppressing the V_{TH} fluctuation by optimizing the bias to the V_{TH}-control gate under SG mode is demonstrated in this study.

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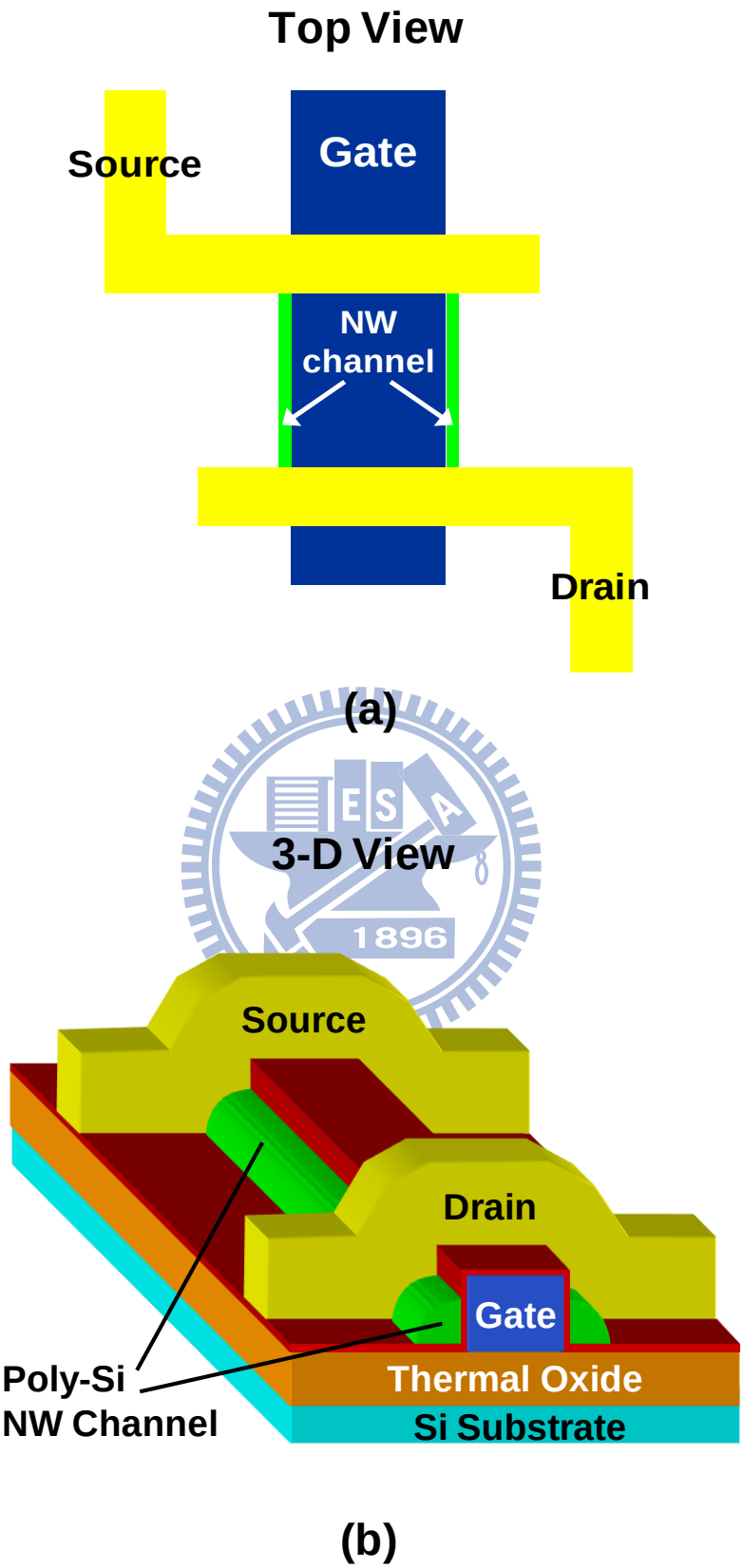


Fig. 2-1 (a) Top view and (b) 3-D structure of the novel poly-Si NWTFT featuring spacer-like NW channels and single side-gate configuration.

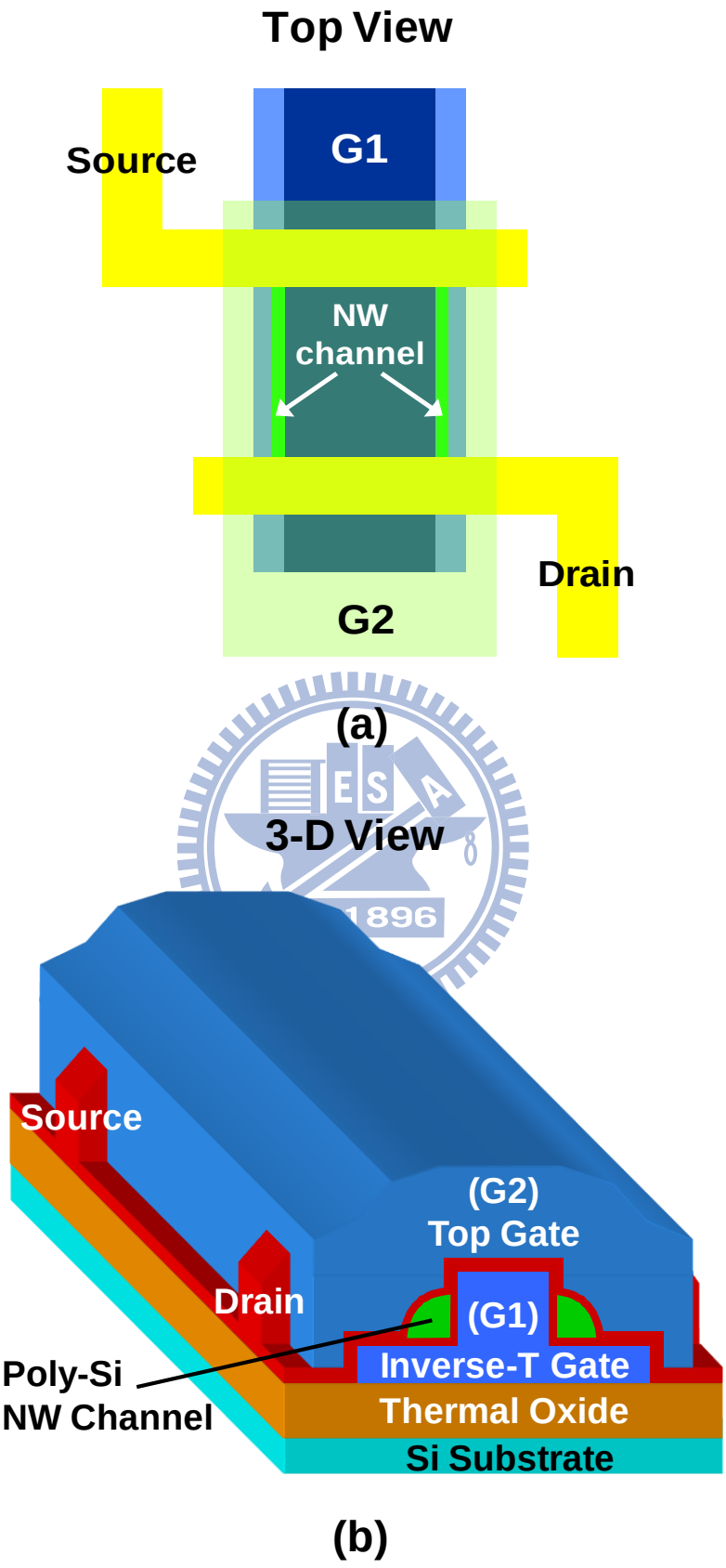


Fig. 2-2 (a) Top view and (b) 3-D structure of the poly-Si NWTFT with independent DG consisting of an inverse-T gate (G1) and a top gate (G2).

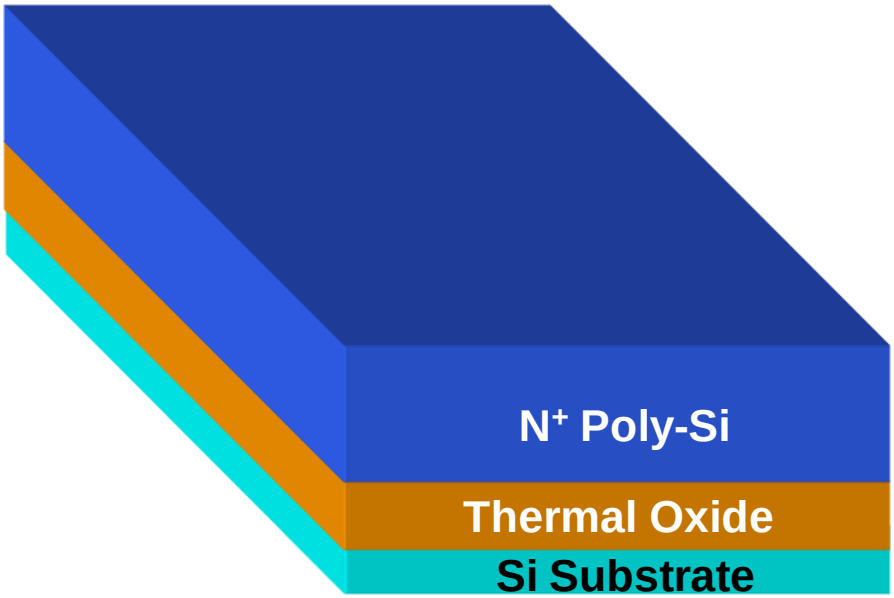


Fig. 2-3 (a) Deposition of *in situ* doped n^+ poly-Si.

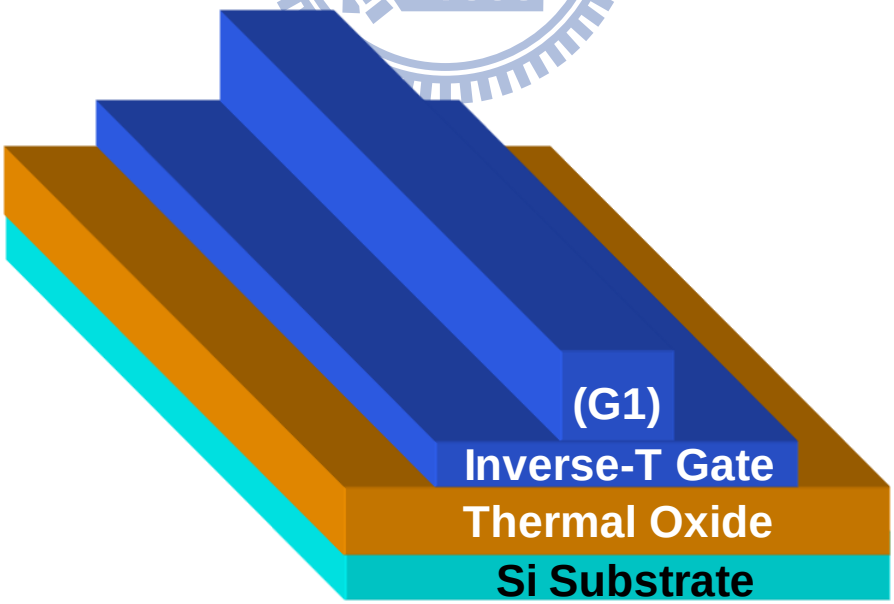


Fig. 2-3 (b) Definition and formation of the inverse-T gate (G1).

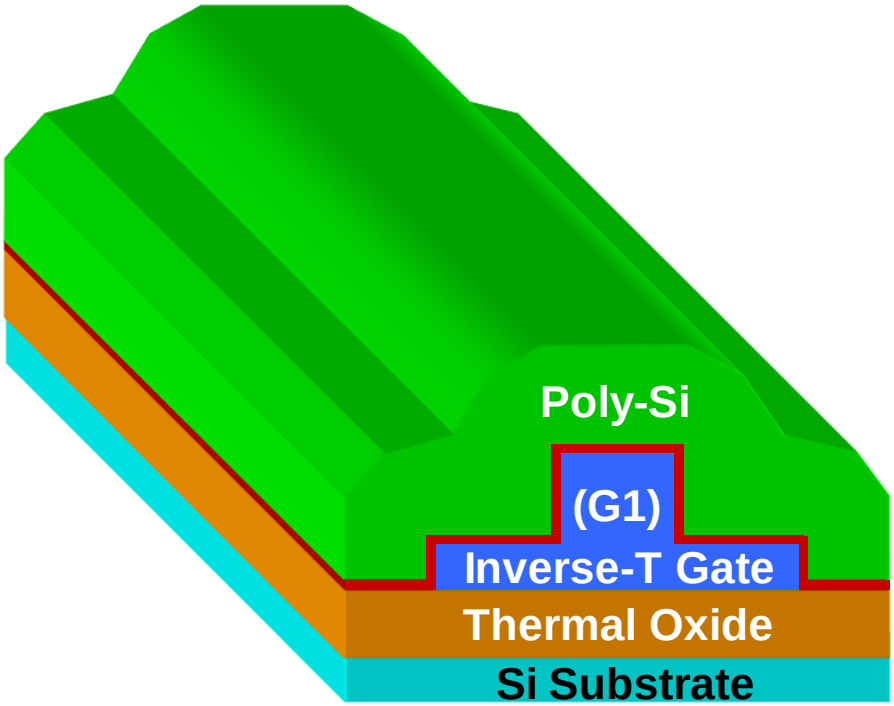


Fig. 2-3 (c) Deposition of G1 oxide and poly-Si active layer.

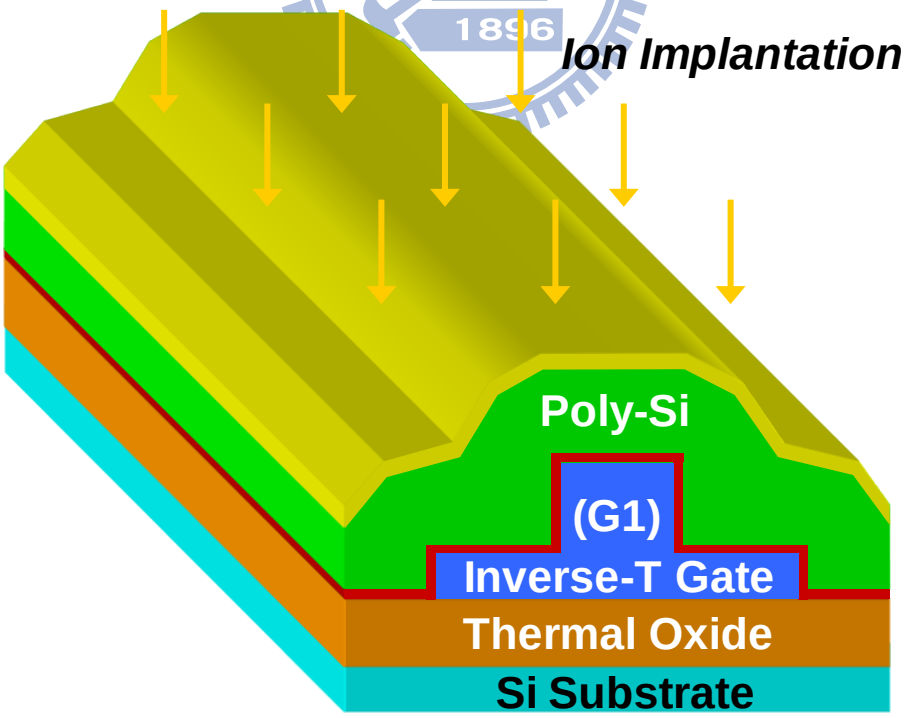


Fig. 2-3 (d) Phosphorus ion (P_{31}^{+}) implantation.

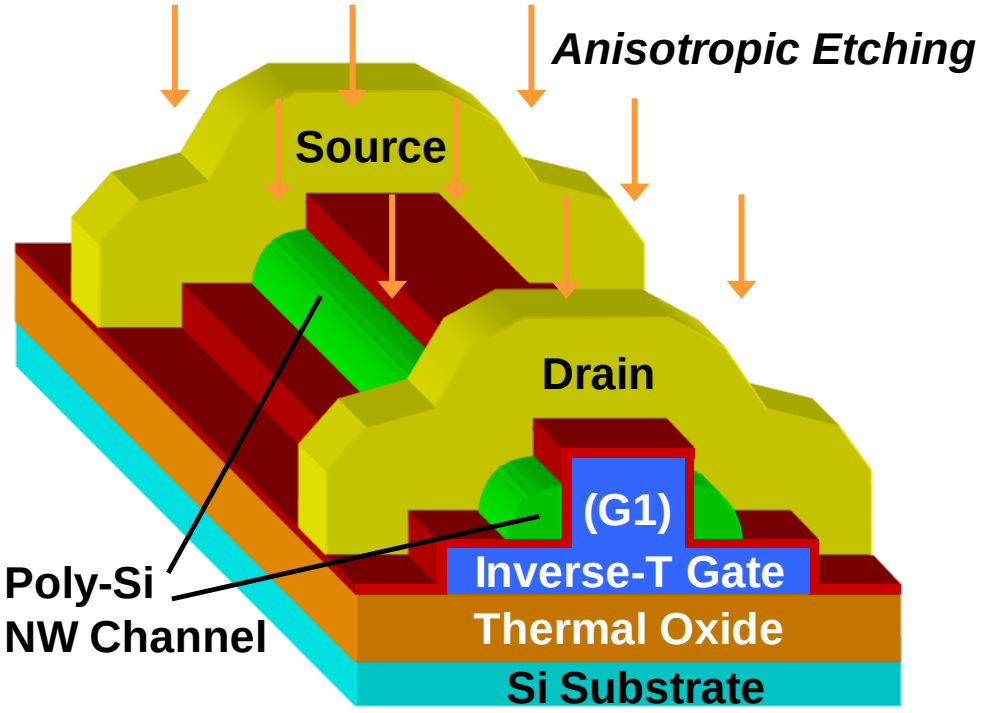


Fig. 2-3 (e) Definition and formation of source/drain (S/D) and NW channel by anisotropic etching.

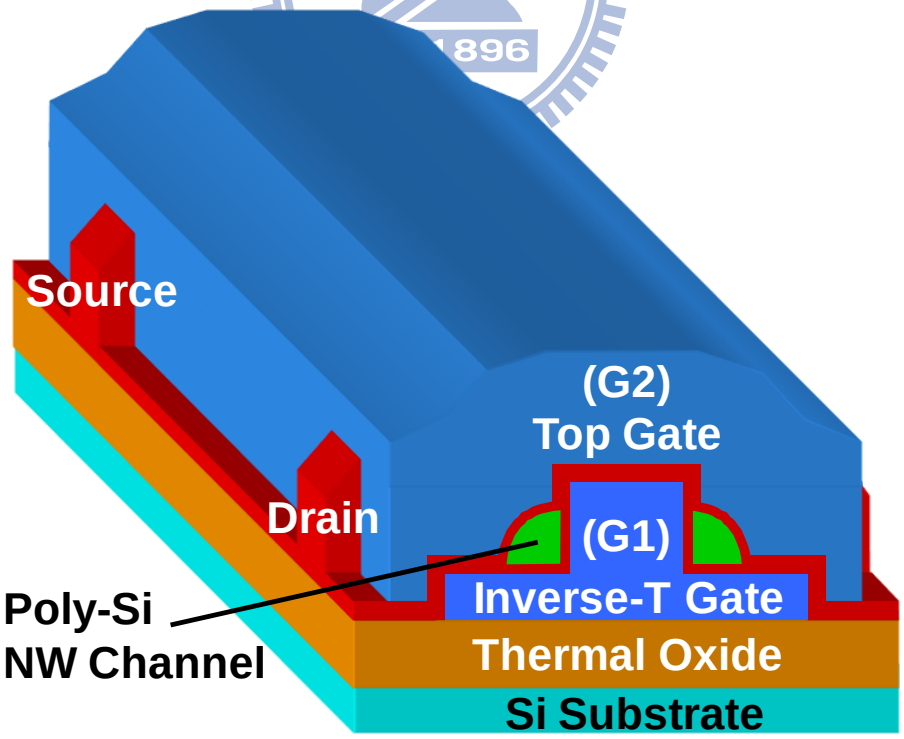


Fig. 2-3 (f) Deposition of top gate (G2) oxide and definition of G2 to form the independent DG structure.

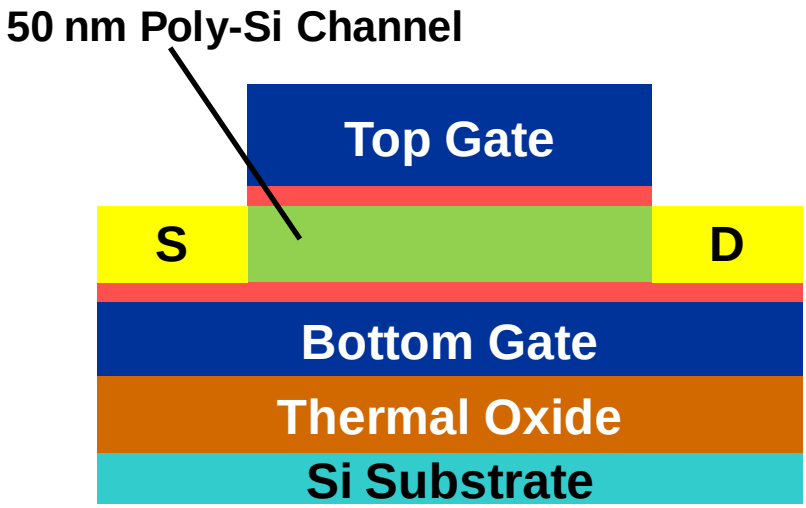


Fig. 2-3 (g) Schematic structure of the planar DG TFT with 50-nm-thick poly-Si channel.

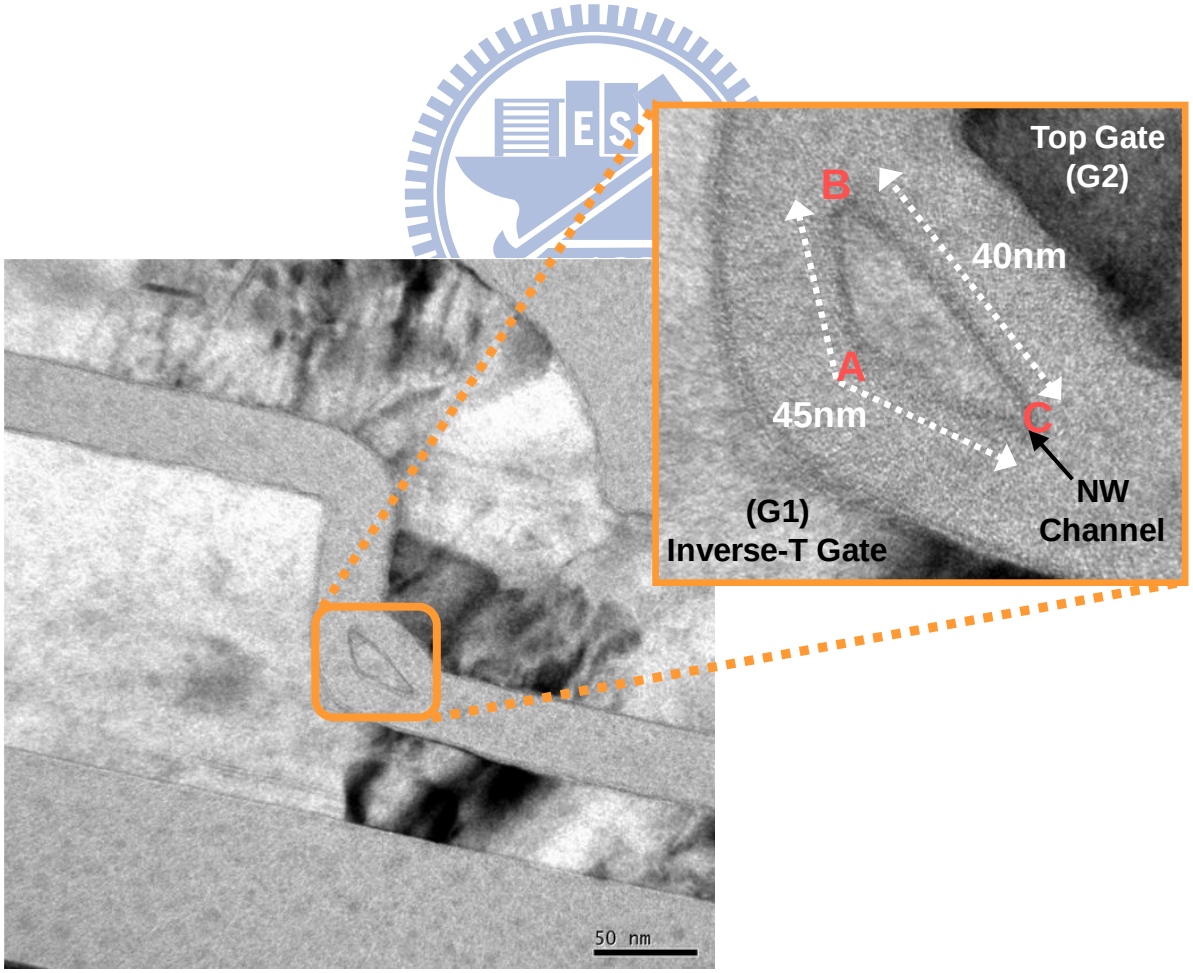


Fig. 2-4 Cross-sectional TEM images showing the cross-section profile and dimensions of the fabricated NW channel.

	DG-Mode	SG1-Mode	SG2-Mode
Inverse-T Gate (G1)	Driving Gate	Driving Gate	Grounded
Top Gate (G2)	Driving Gate	Grounded	Driving Gate

TABLE 2-1 Definition of bias conditions for DG, SG1, and SG2 operation modes.

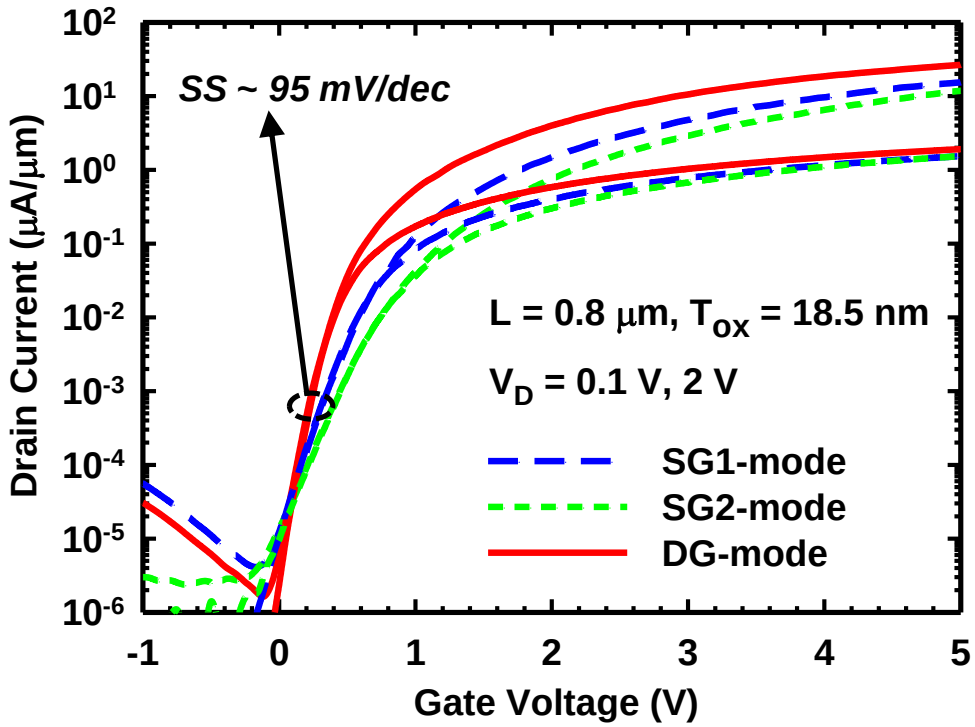


Fig. 2-5 Transfer characteristics under SG and DG modes of operations with L = 0.8 μm. SG1 and SG2 refer to SG modes with G1 and G2 serving as the driving gate, respectively.

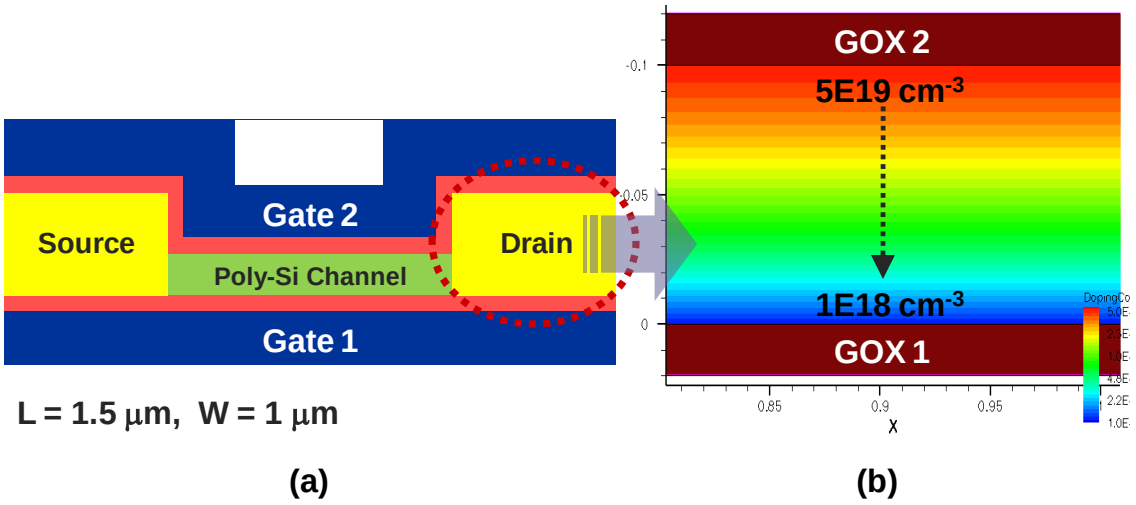


Fig. 2-6 (a) Schematic cross-sectional structure of the poly-Si DG-TFT used for TCAD simulation and (b) the designed S/D doping profile with a gradually decreased concentration from the top (N_D ~ 5×10^{19} cm^{-3}) to the bottom (N_D ~ 10^{18} cm^{-3}) of S/D regions.

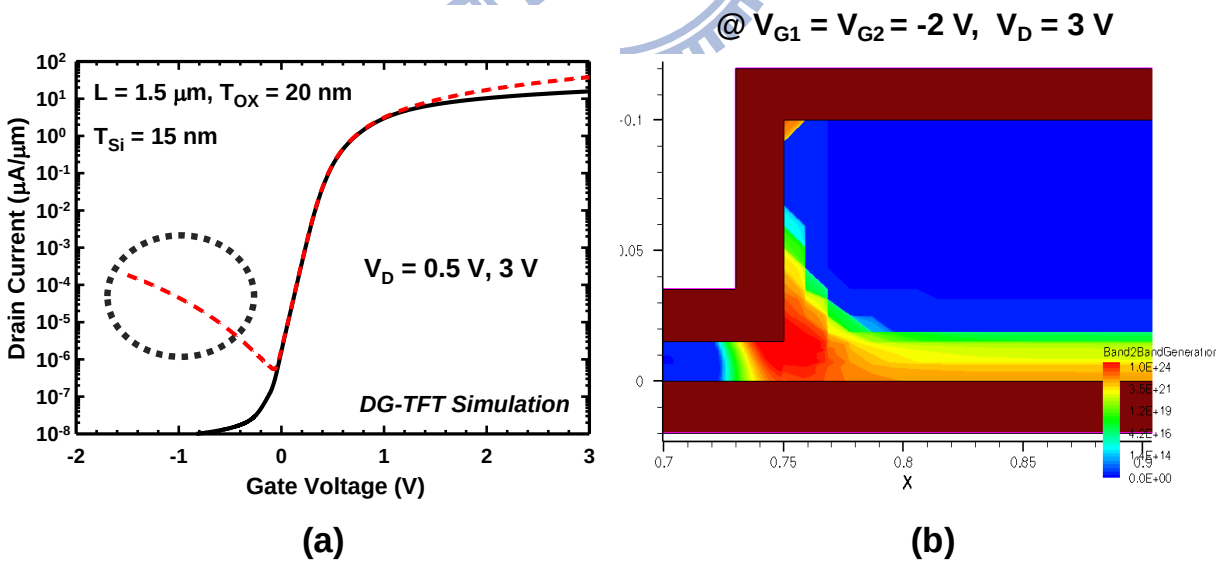
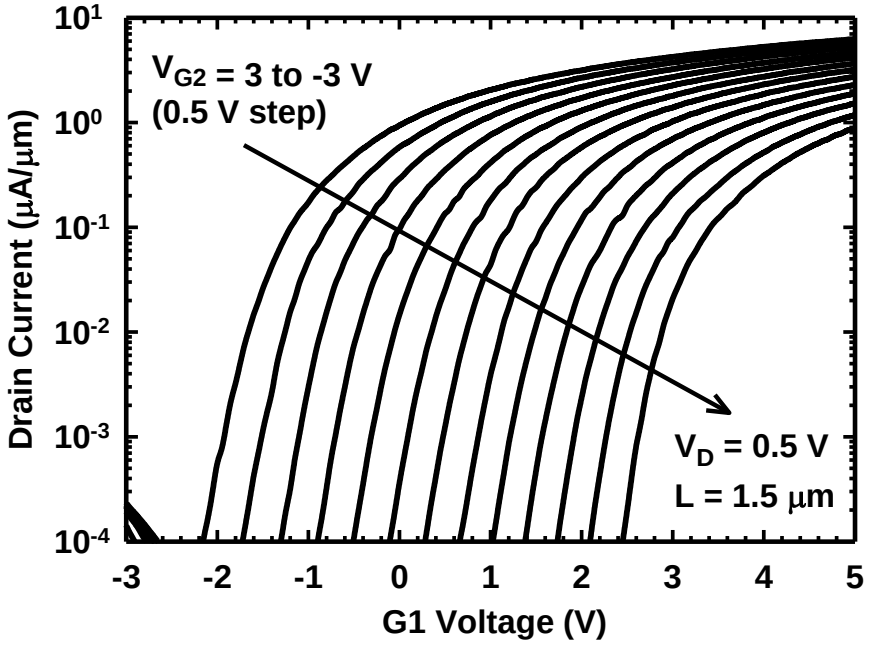
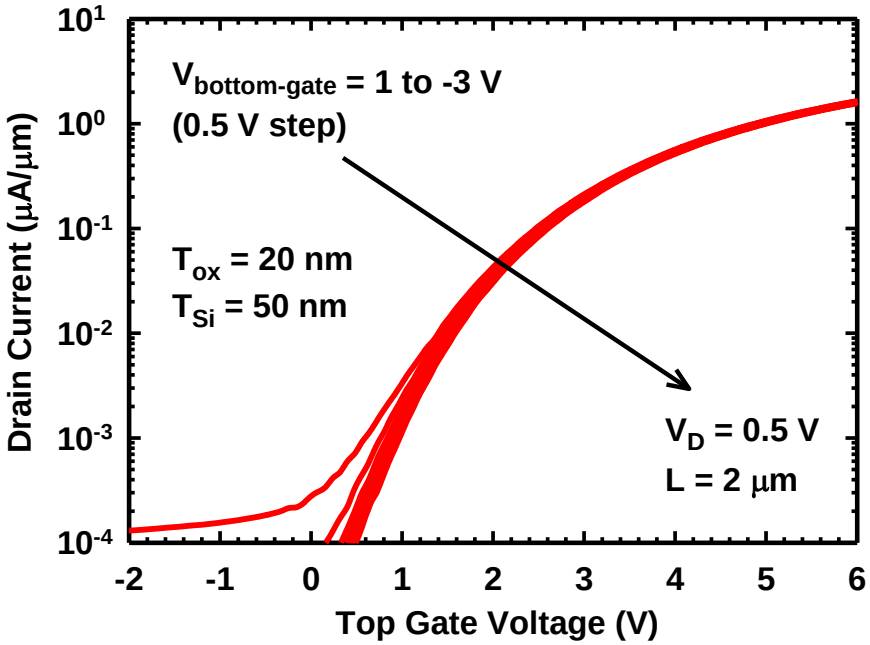


Fig. 2-7 (a) Simulated I_D-V_G characteristics of the poly-Si DG-TFT structure shown in Fig. 2-6 (a). (b) Simulated trap-assisted band-to-band tunneling (BTBT) generation rate inside the drain region at V_{G1} = V_{G2} = -2 V and V_D = 3 V.



(a)



(b)

Fig. 2-8 (a) Transfer characteristics of the NW device having G1 as the driving gate and G2 as the V_{TH}-control gate. (b) Transfer characteristics of the planar control device with T_{Si} = 50 nm driven by the top-gate with bottom-gate as the V_{TH}-control gate.

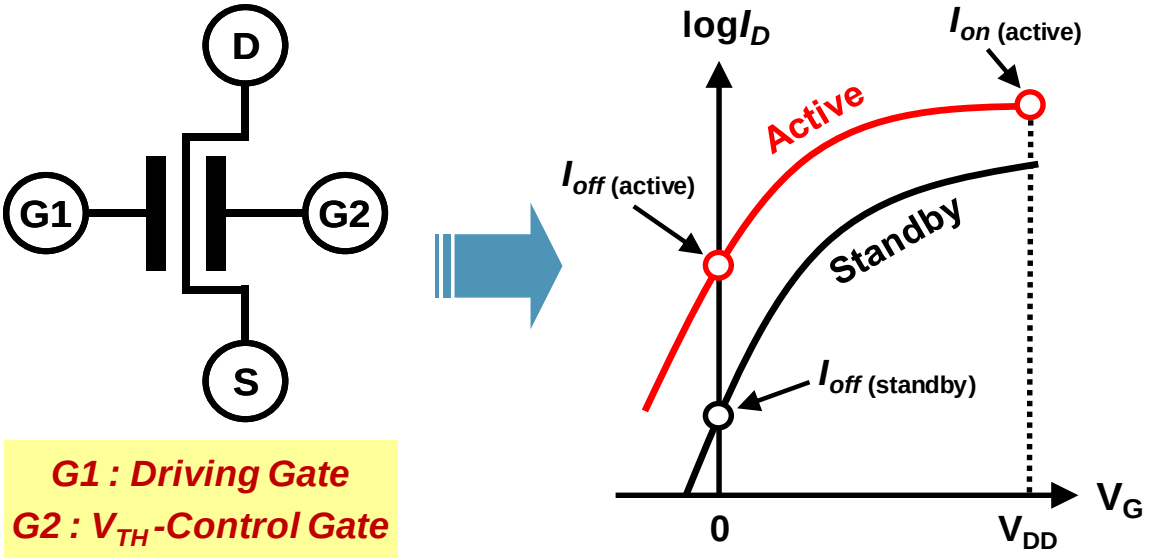


Fig. 2-9 Schematics showing an independent DG MOSFET with its I_D-V_G characteristics modulated by V_{TH}-control gate for active- and standby-modes of operation [2.13].

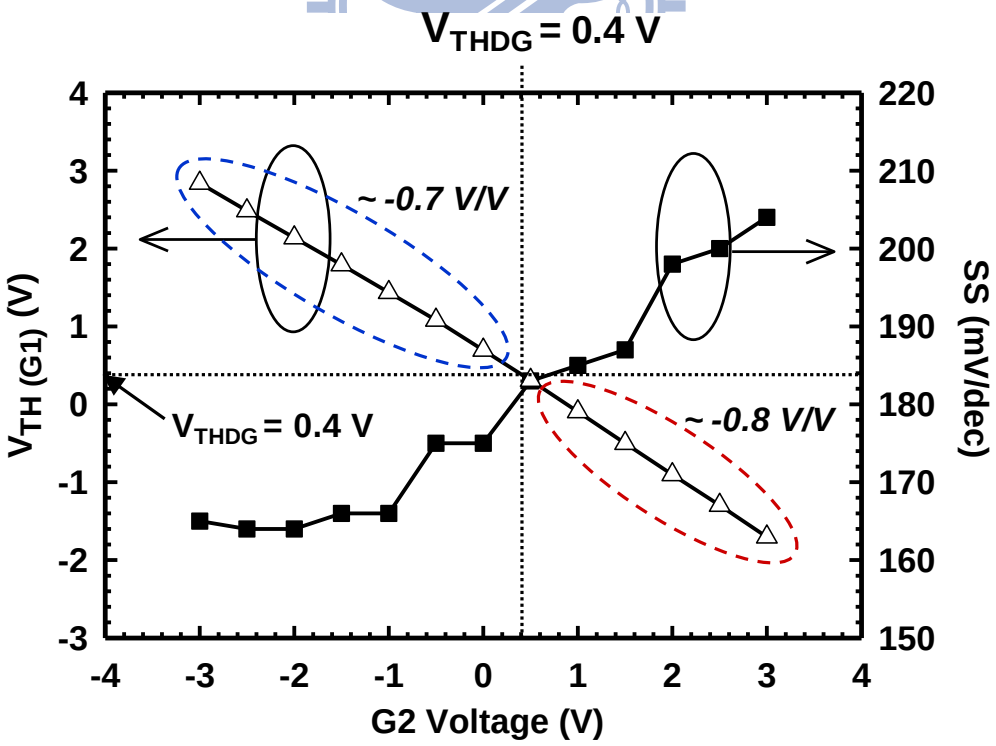


Fig. 2-10 The extracted V_{TH} and SS as functions of V_{G2} for the NW device under SG1 mode of operation. V_{THDG} denotes the V_{TH} measured in DG mode.

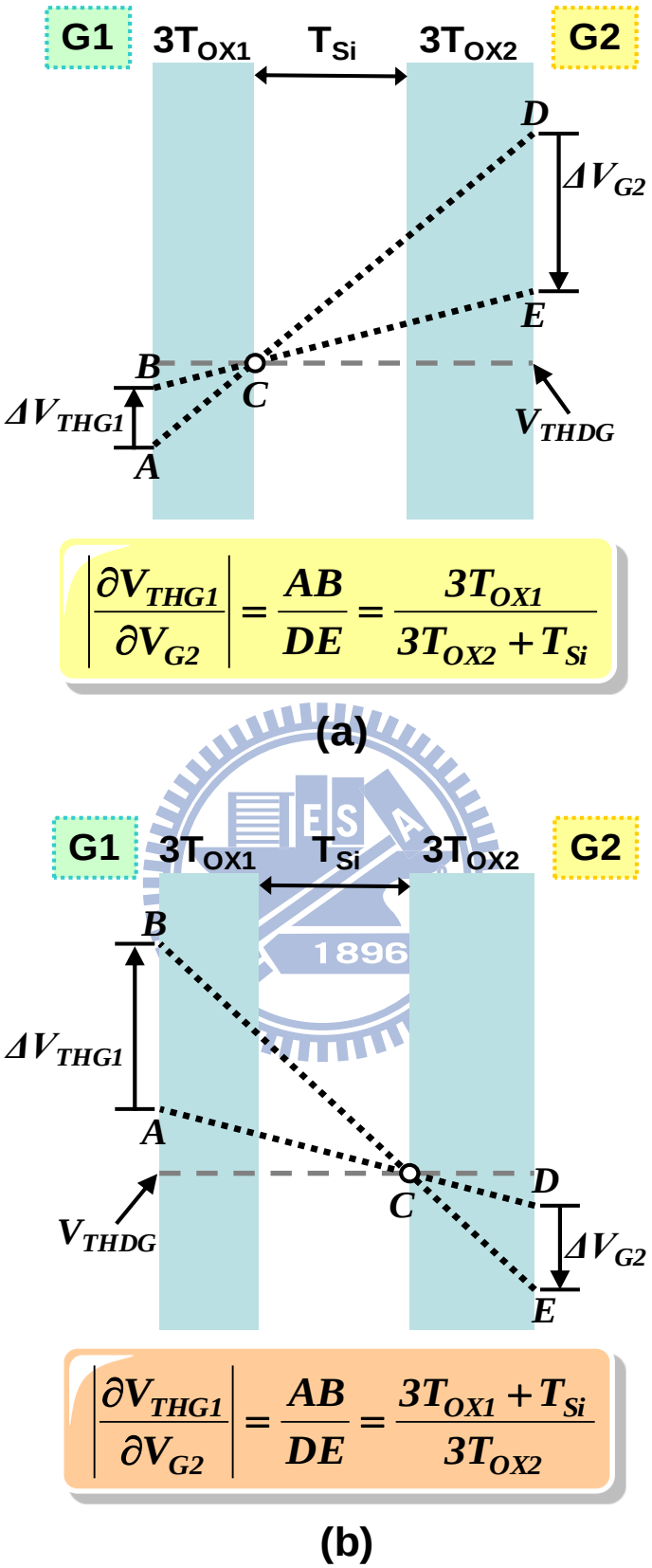


Fig. 2-11 Schematic potential distributions across the channel of an independent DG structure with ultra thin body for describing the relation between V_{TH}-shift rate and film thicknesses under different bias conditions [2.13].

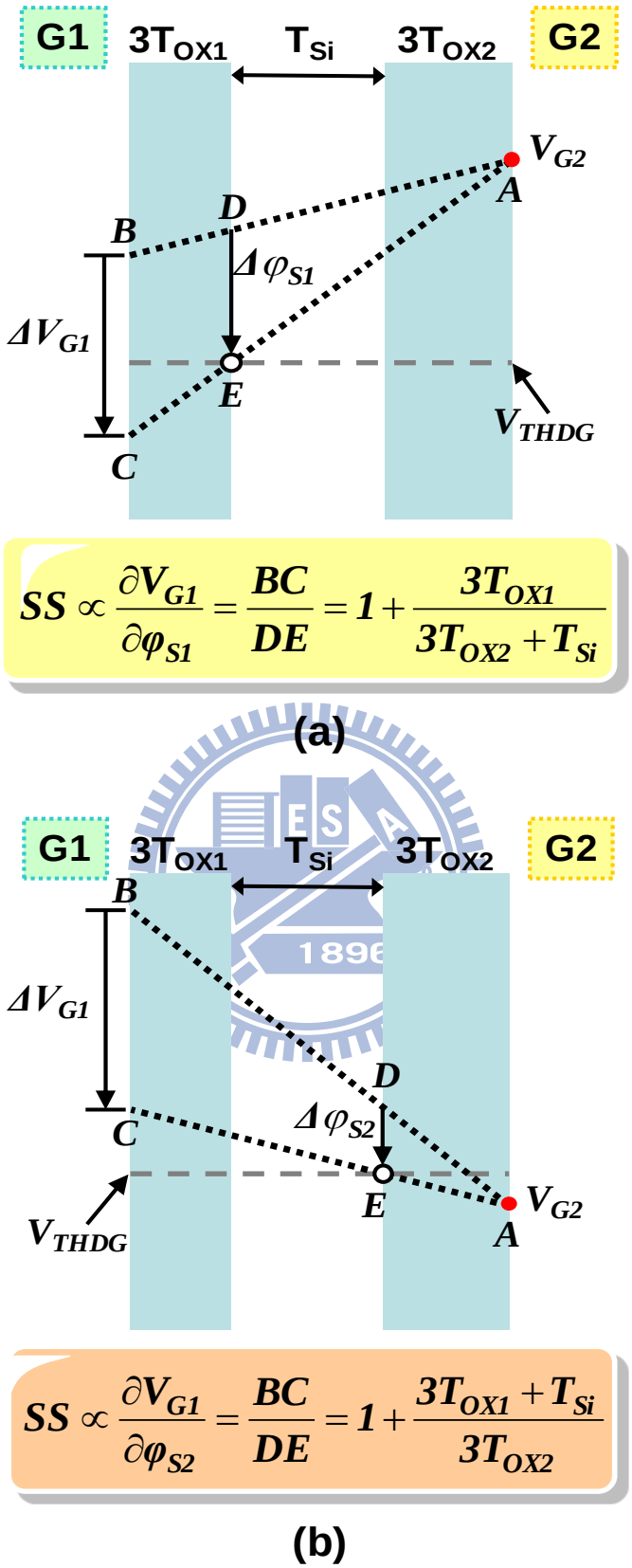


Fig. 2-12 Schematic potential distributions across the channel for describing the relation between SS and film thicknesses under different bias conditions [2.13].

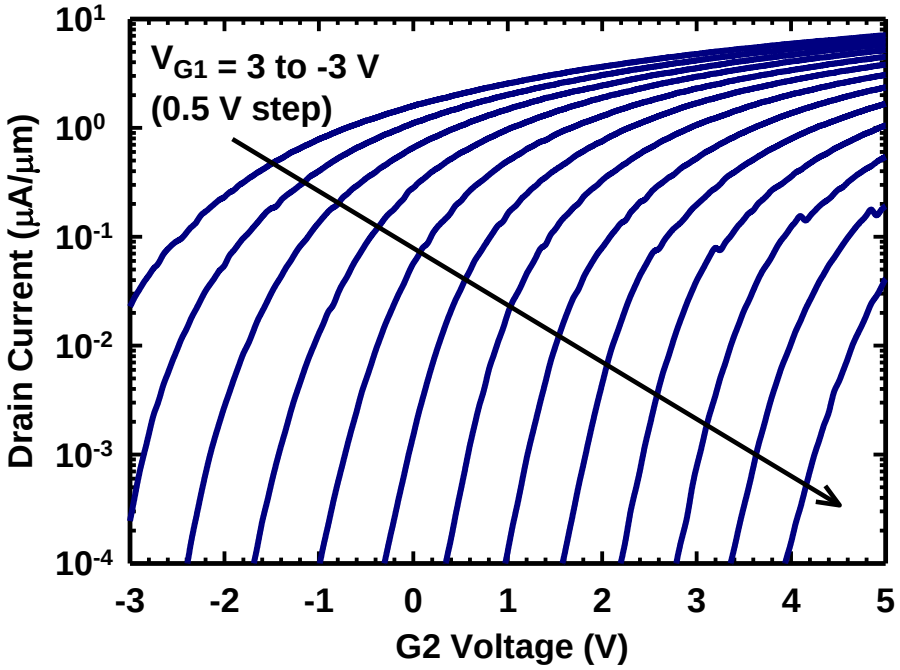


Fig. 2-13 Transfer characteristics of a NW device with G2 as the driving gate and G1 as the V_{TH}-control gate.

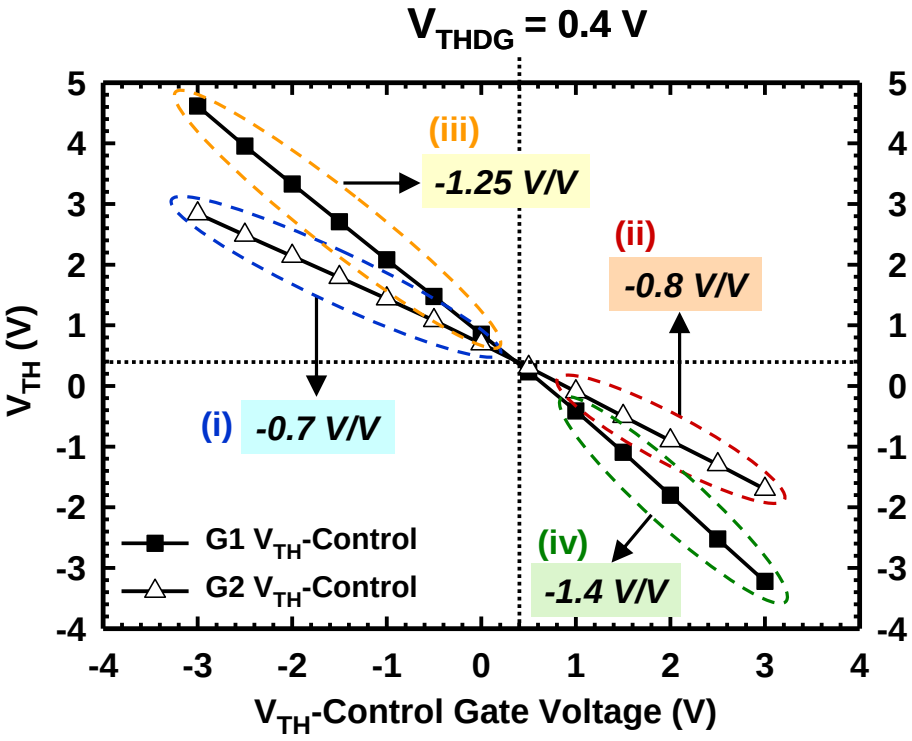
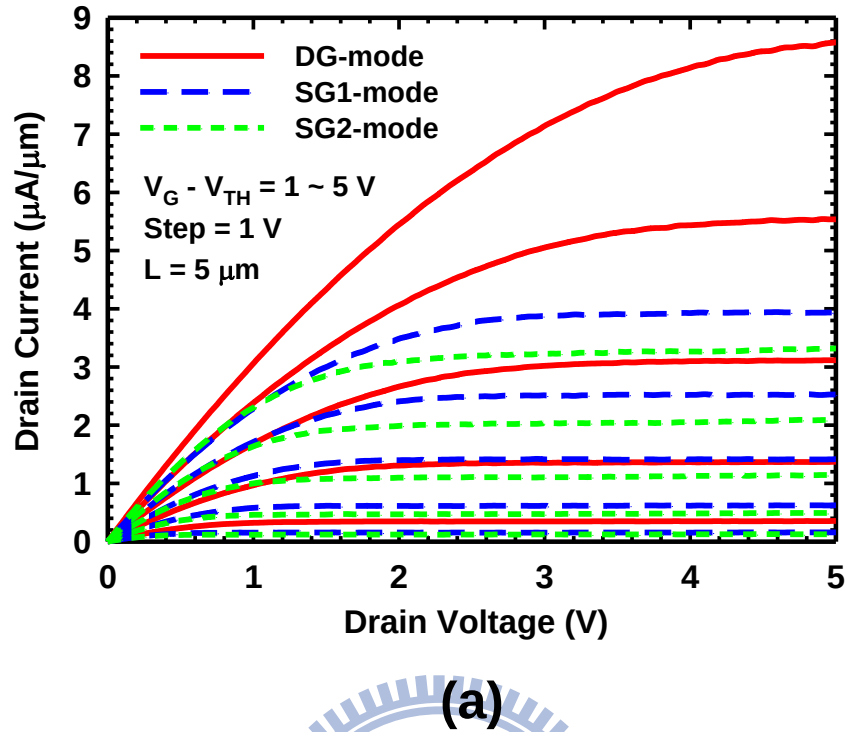


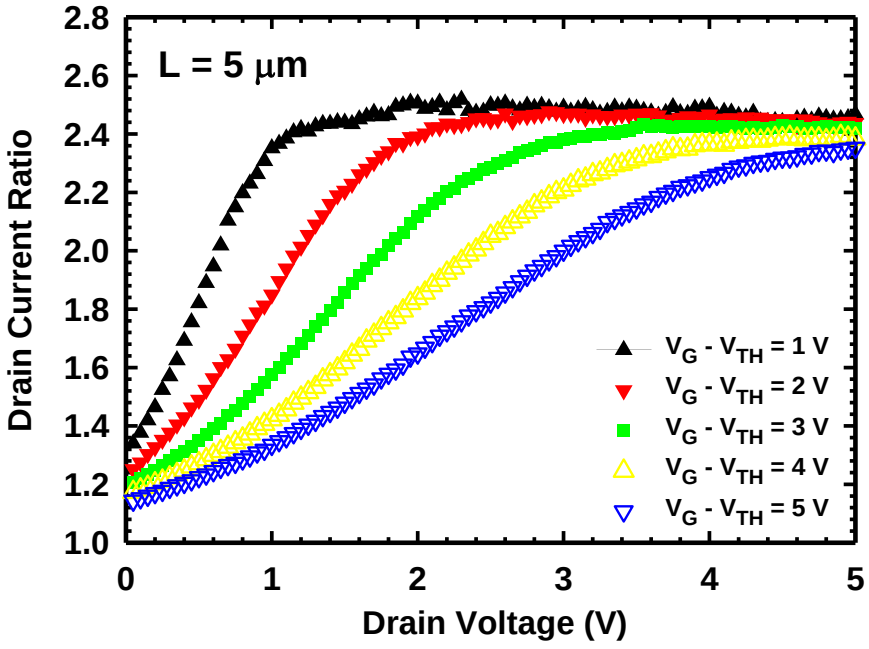
Fig. 2-14 The extracted V_{TH} as a function of V_{TH}-control gate voltage. The values of V_{TH}-shift rate for the four operation regions are also indicated.

V_{TH}-Control Gate	Top Gate (G2)		Inverse-T Gate (G1)	
Bias Condition	**(i) $V_{G2} < V_{THDG}$**	**(ii) $V_{G2} > V_{THDG}$**	**(iii) $V_{G1} < V_{THDG}$**	**(iv) $V_{G1} > V_{THDG}$**
Eqs. of V_{TH}-Shift Rate [2.13] (Back-Gate-Effect Factor γ)	$\left\|\frac{\partial V_{THG1}}{\partial V_{G2}}\right\| = \frac{3T_{OX1}}{3T_{OX2}+T_{Si}}$	$\left\|\frac{\partial V_{THG1}}{\partial V_{G2}}\right\| = \frac{3T_{OX1}+T_{Si}}{3T_{OX2}}$	$\left\|\frac{\partial V_{THG2}}{\partial V_{G1}}\right\| = \frac{3T_{OX2}}{3T_{OX1}+T_{Si}}$	$\left\|\frac{\partial V_{THG2}}{\partial V_{G1}}\right\| = \frac{3T_{OX2}+T_{Si}}{3T_{OX1}}$
Exp. Data (V/V)	***0.7***	***0.8***	***1.25***	***1.4***

TABLE 2-2 Summary of equations for V_{TH}-shift rate under different operation and bias conditions from the theoretical model [2.13], and the experimental data.



(a)



(b)

Fig. 2-15 (a) Output characteristics of the NW device under different operation modes with L = 5 μm. (b) Ratio of drain current of the DG mode to the sum of the two SG modes. V_G–V_{TH} varies from 1 V to 5 V in step of 1 V.

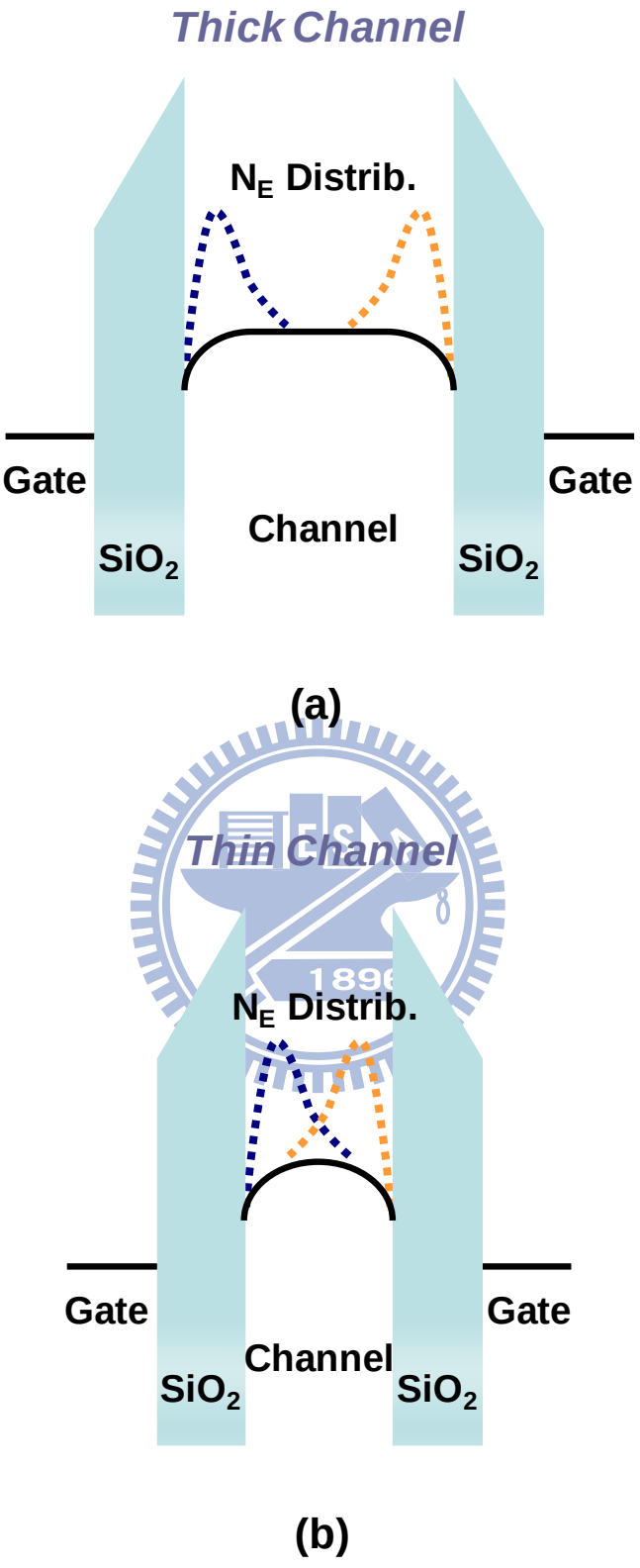


Fig. 2-16 Energy band diagrams of DG structure with (a) thick channel and (b) thin channel. Dashed lines represent the distribution of inversion charges.

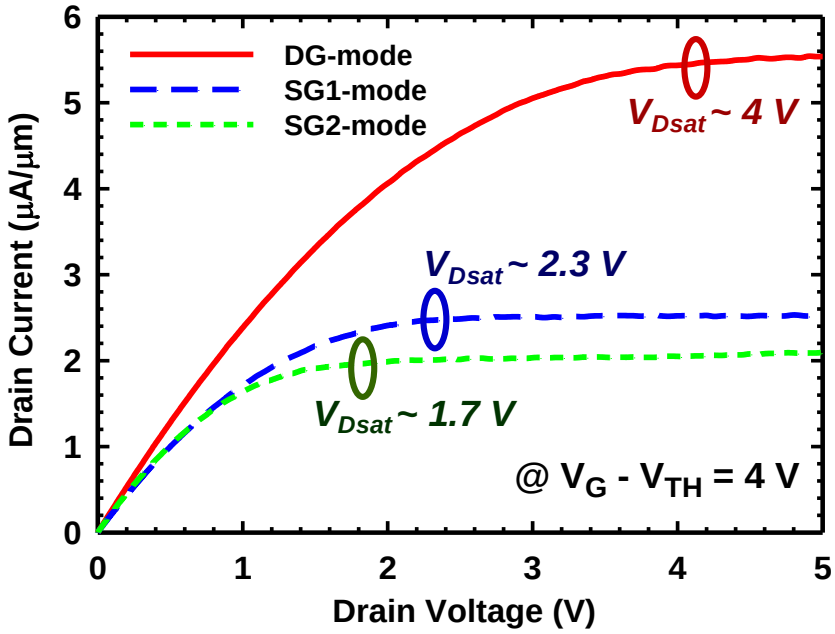
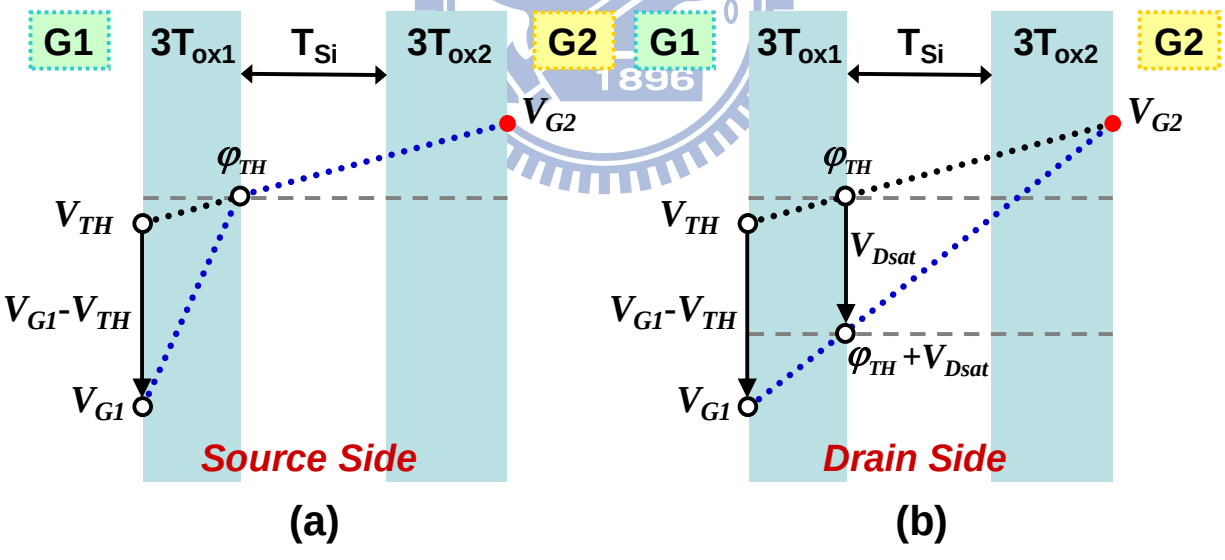


Fig. 2-17 I_D-V_D curves for the NW device operated under various modes at V_G–V_{TH} = 4 V.



$$V_{Dsat} = (V_G - V_{TH}) \times \frac{3T_{OX2} + T_{Si}}{3T_{OX2} + T_{Si} + 3T_{OX1}} = \frac{V_G - V_{TH}}{1 + \gamma}$$

Fig. 2-18 Schematic potential distribution for SG1-mode operation of the NW device at (a) source side and (b) drain side of the channel under pinch-off bias condition.

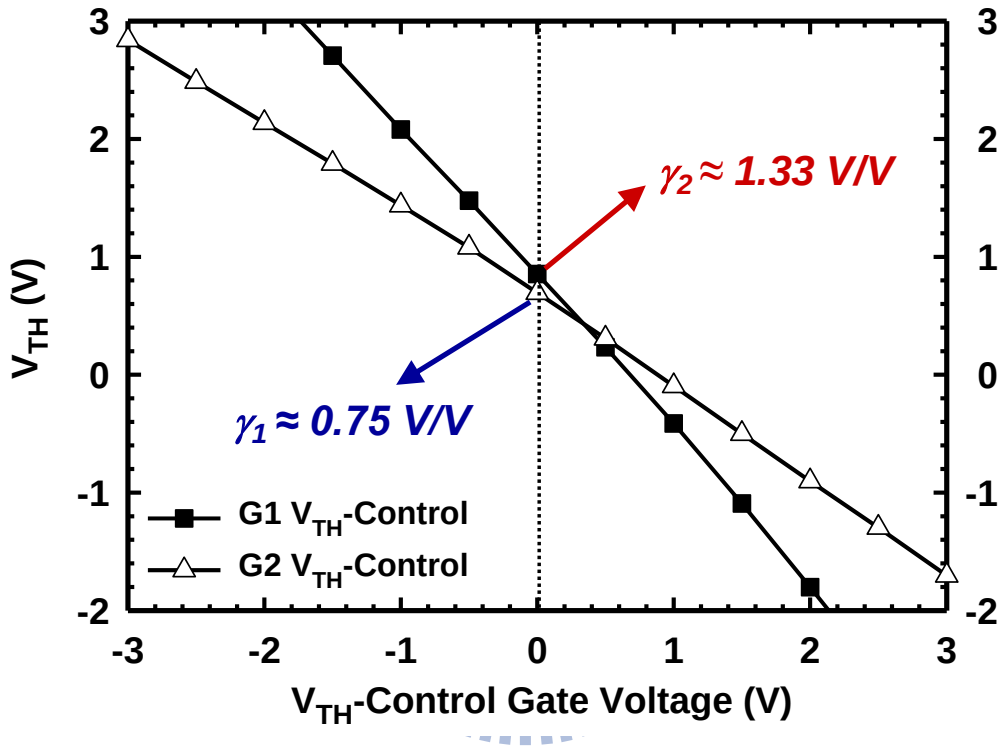


Fig. 2-19 Extraction of back-gate-effect factors for two SG modes at V_{TH}-control gate = 0 V.

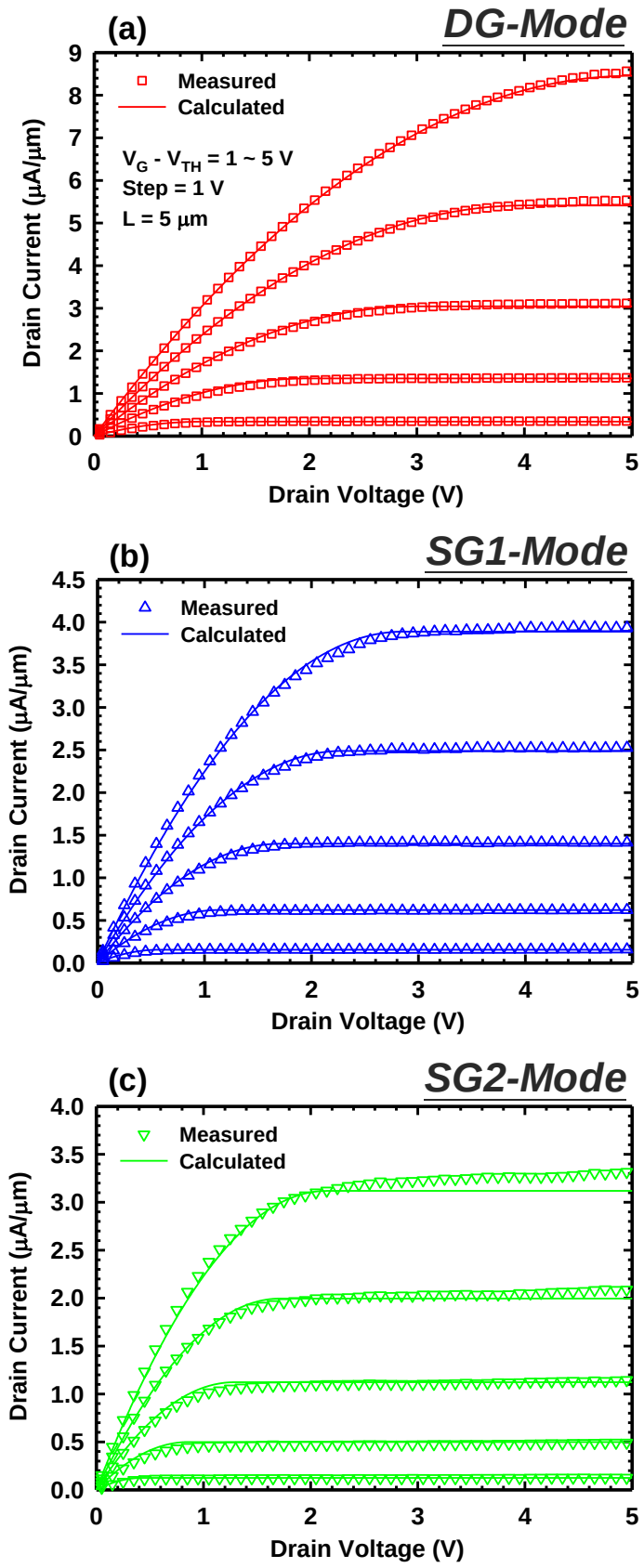
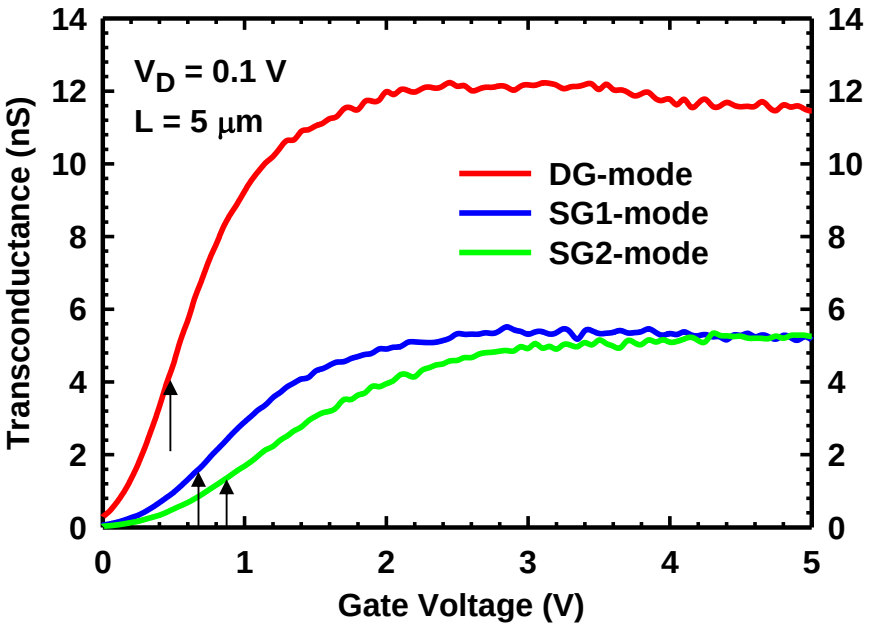
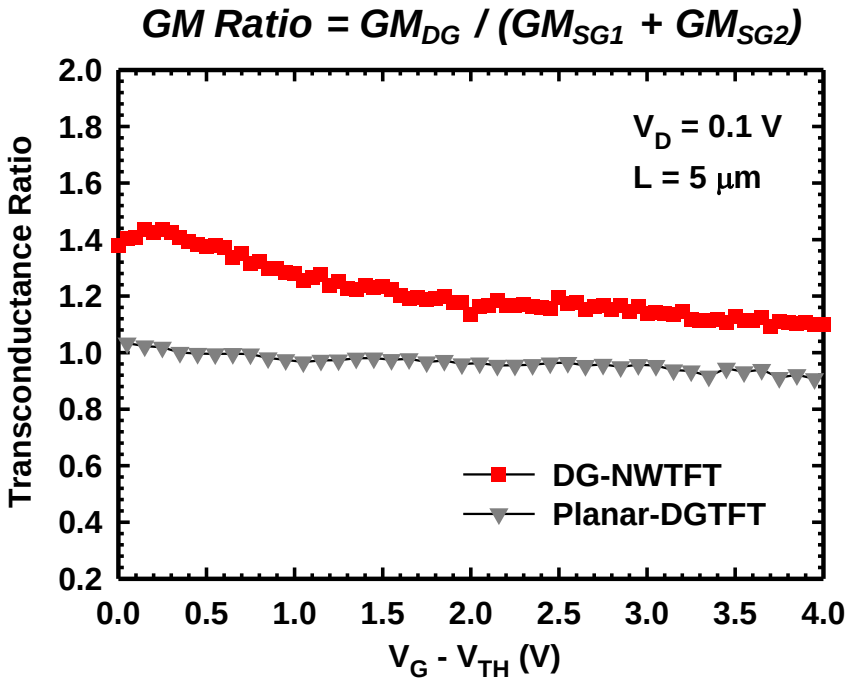


Fig. 2-20 Comparisons of output characteristics between the measured data and calculated results of each operation mode based on the proposed model.



(a)



(b)

Fig. 2-21 (a) GM of a NW device versus V_G under different operation modes. The arrows indicate the V_{TH}. (b) Ratio of GM of the DG mode to the sum of the two SG modes as a function of V_G–V_{TH}. Results for the planar device are also included for comparison.

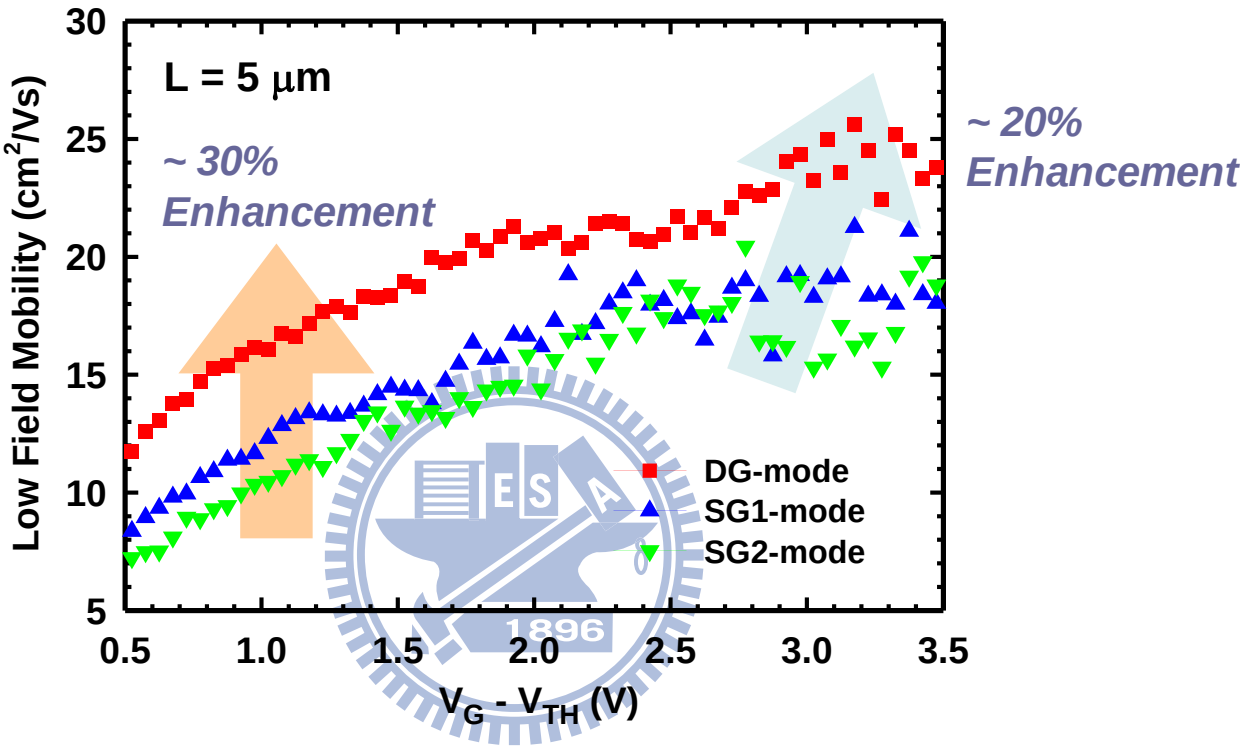


Fig. 2-22 Normalized electron mobility as a function of V_G–V_{TH}. 30% and 20% mobility enhancement at respectively low and high V_G–V_{TH} for DG mode compared to SG modes are estimated.

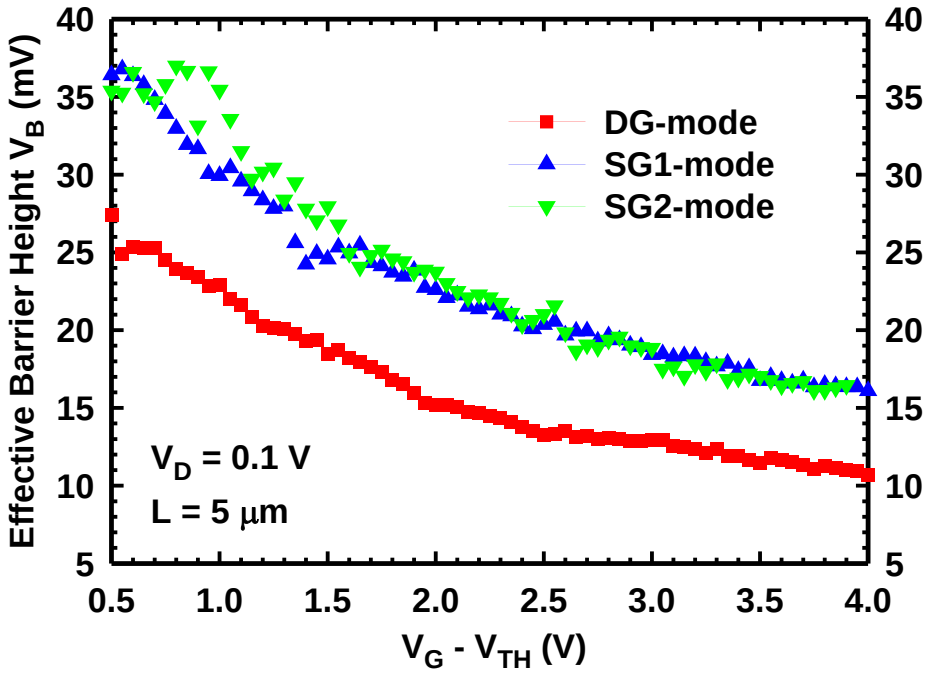


Fig. 2-23 Extracted barrier height V_B as a function of V_G–V_{TH} for the NW device operated under DG and SG modes.

$$exp(-qV_B/kT)\ Ratio = \frac{W_{DG}e^{-qV_{BDG}/kT}}{W_{SG1}e^{-qV_{BSG1}/kT} + W_{SG2}e^{-qV_{BSG2}/kT}}$$

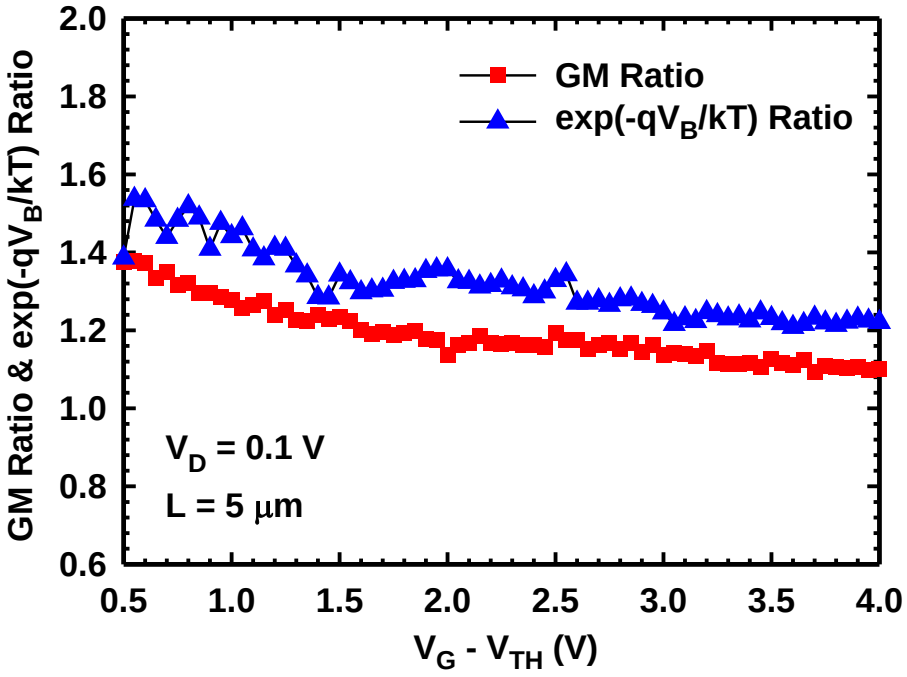


Fig. 2-24 Ratios of GM and weighted e^{-qV_B/k_BT} of DG mode to the sum of two SG modes as a function of V_G–V_{TH}.

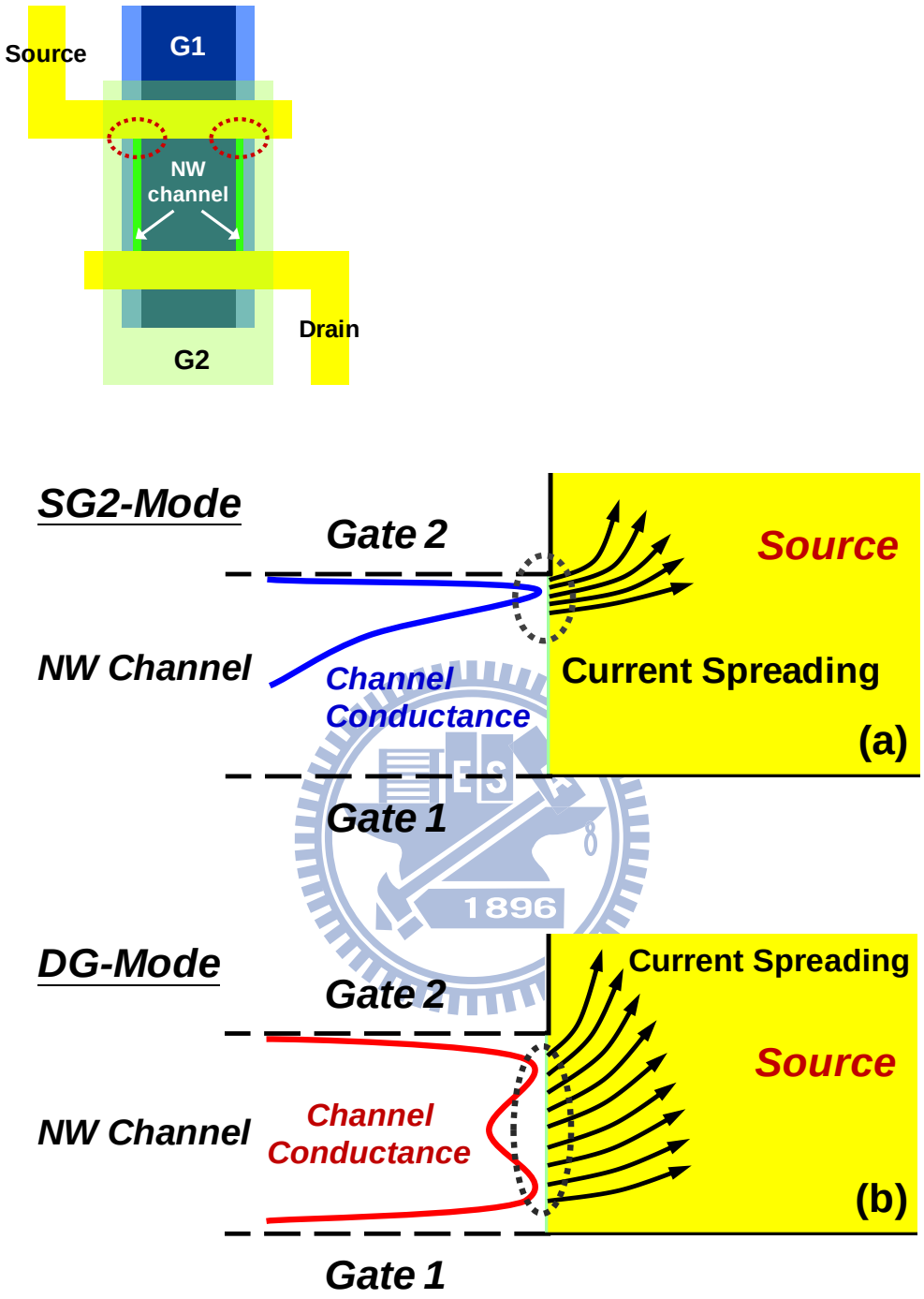


Fig. 2-25 Schematic illustrations of local conductance distribution in NW channel and current flow through channel to S/D region under (a) SG mode and (b) DG mode.

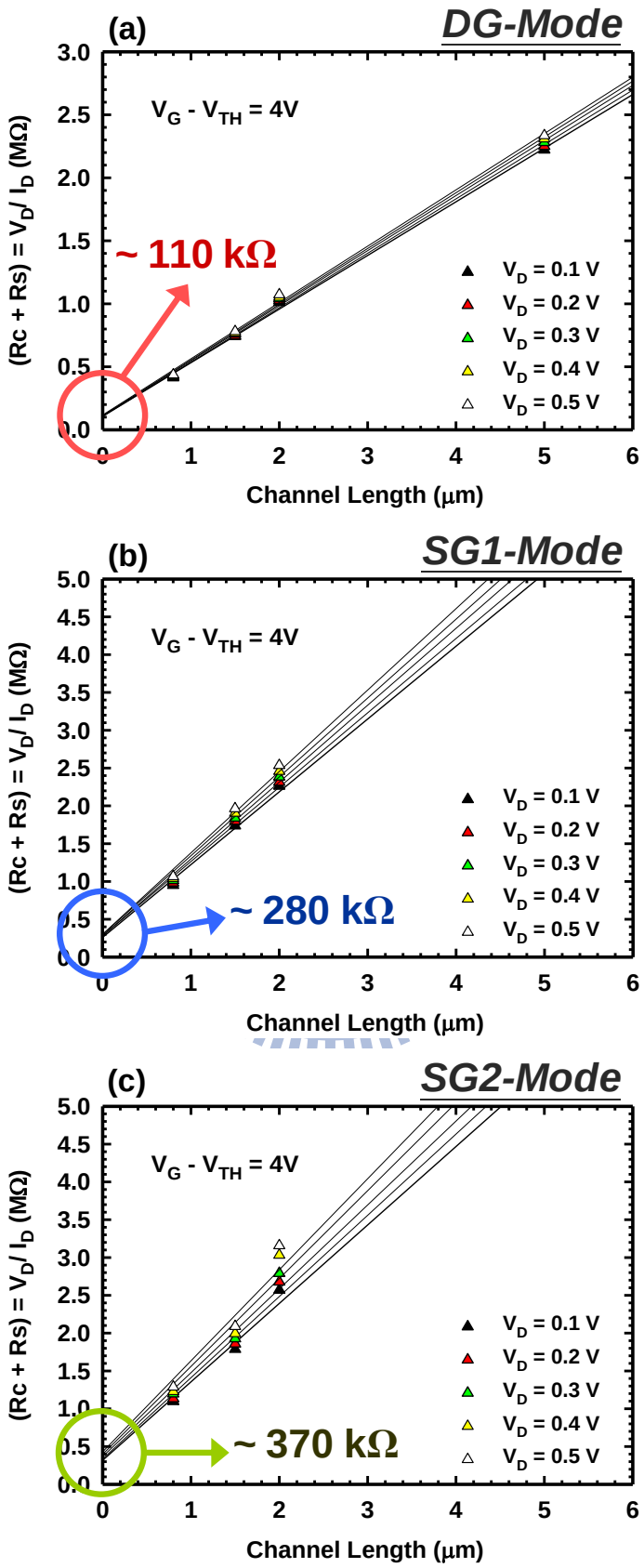


Fig. 2-26 Estimated S/D resistance in (a) DG mode, (b) SG1 mode and (c) SG2 mode. The resistance was extracted from the I_D-V_D curves with various channel lengths.

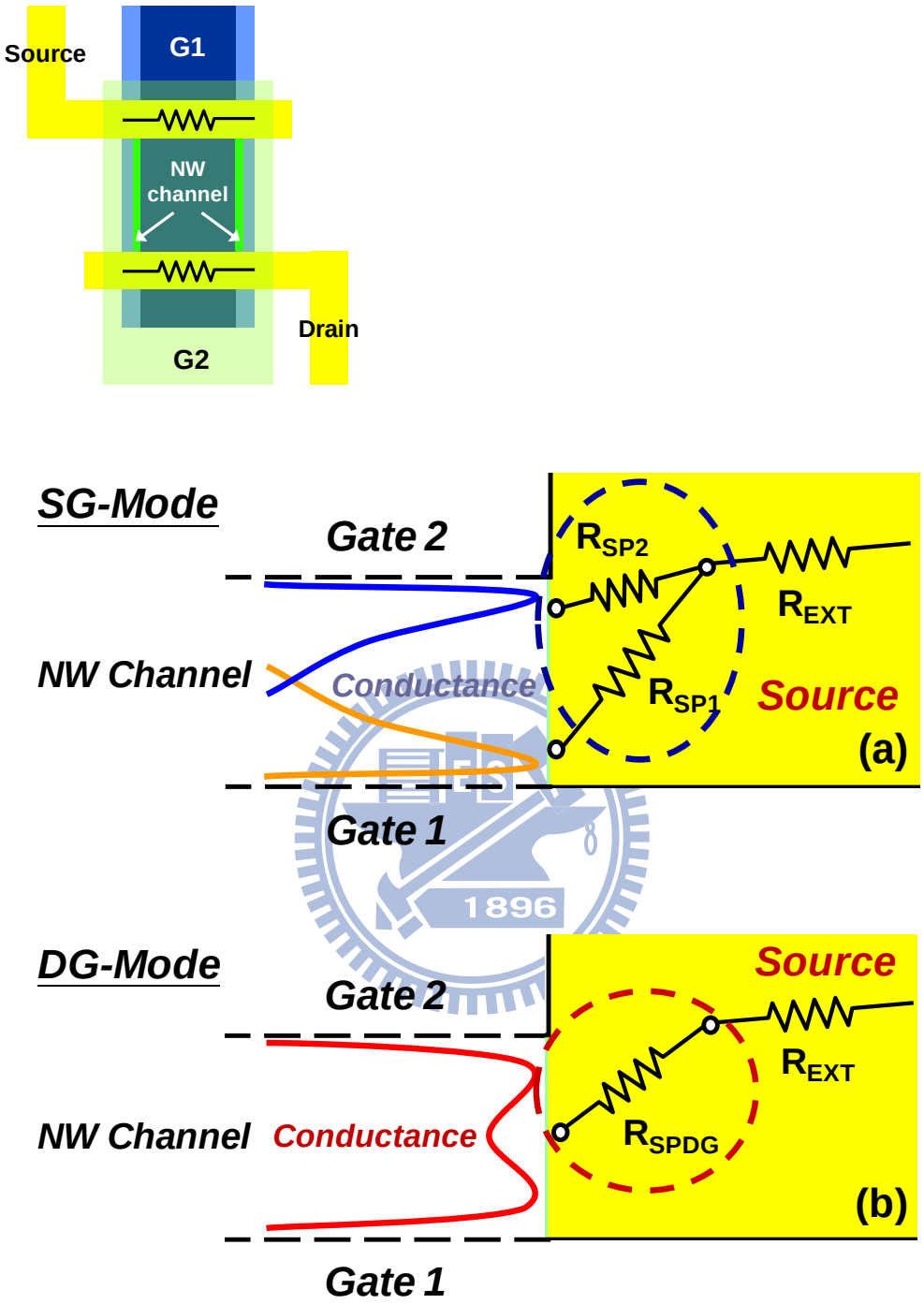


Fig. 2-27 Schematic expressions of equivalent resistance components under (a) SG mode and (b) DG mode.

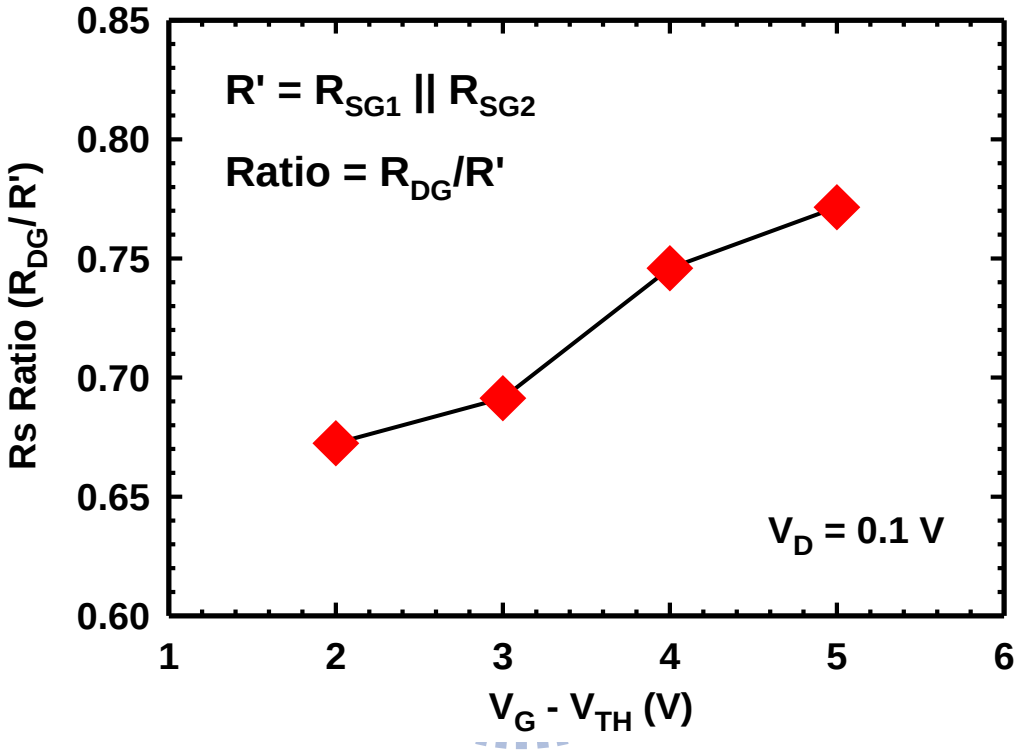


Fig. 2-28 Extracted Rs ratio as a function of $V_G - V_{TH}$. R' is defined as the parallel resistance of two Rs measured in each SG mode.

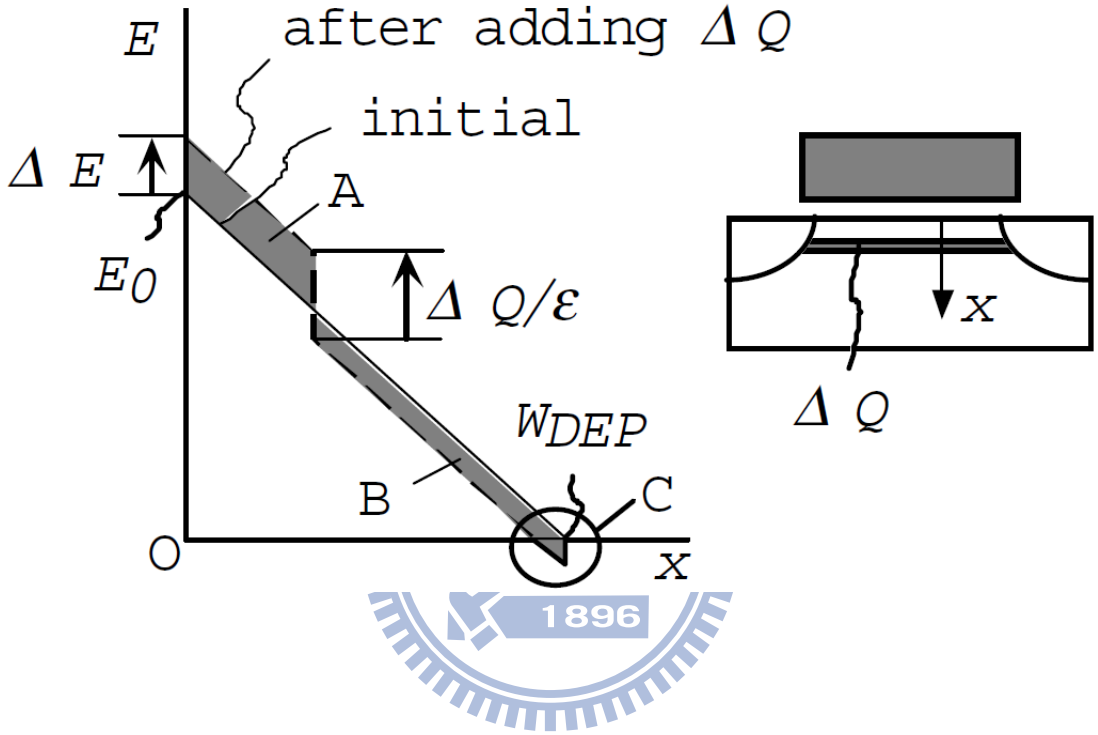


Fig. 2-29 Schematic illustration of electric field, E, as a function of depth x in the channel region of an MOSFET [2.27].

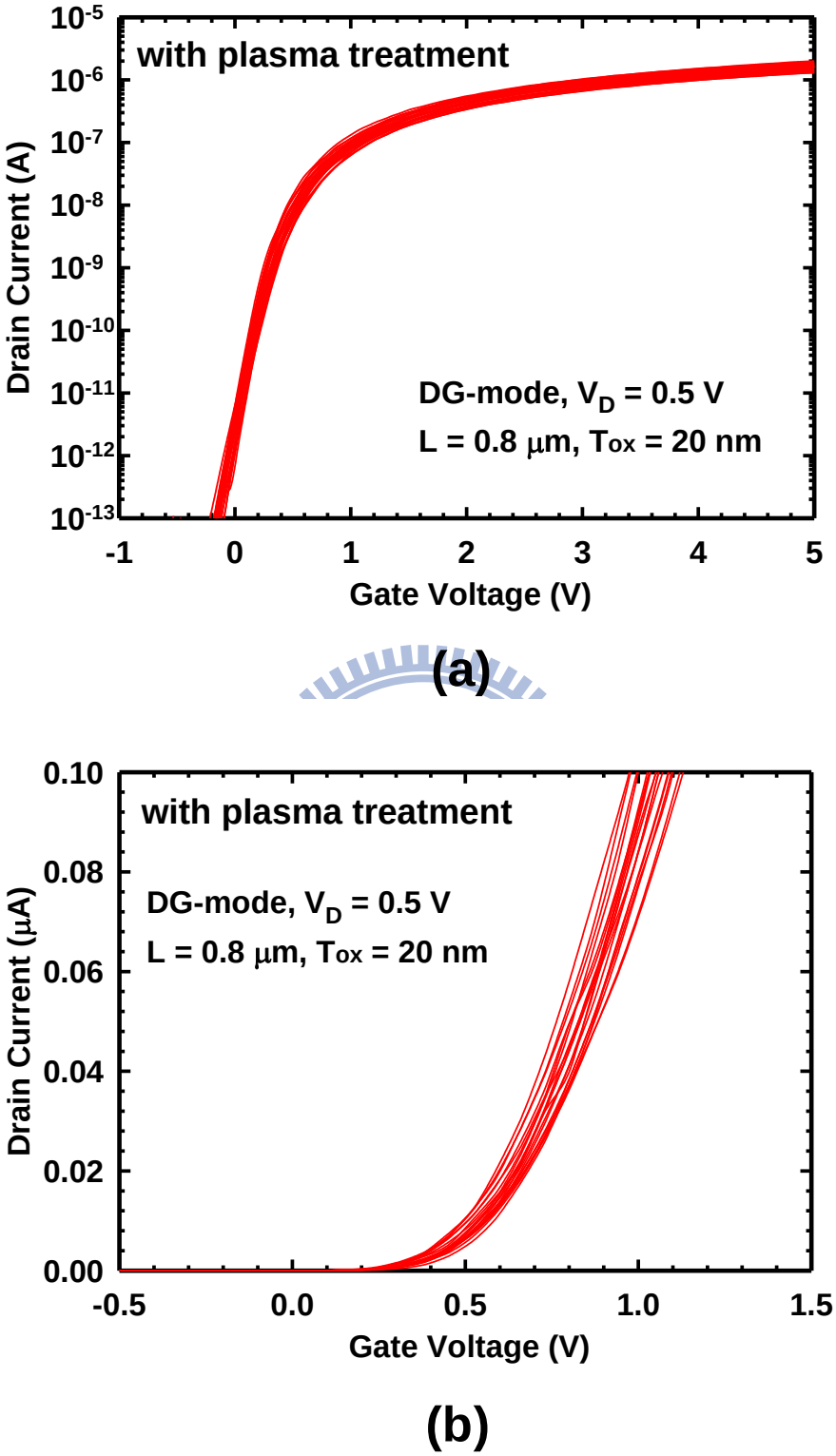


Fig. 2-30 Transfer characteristics under DG mode for poly-Si NW devices with NH_3 plasma treatment. (a) I_D in logarithmic scale. (b) I_D in linear scale. 20 devices were characterized in the plot.

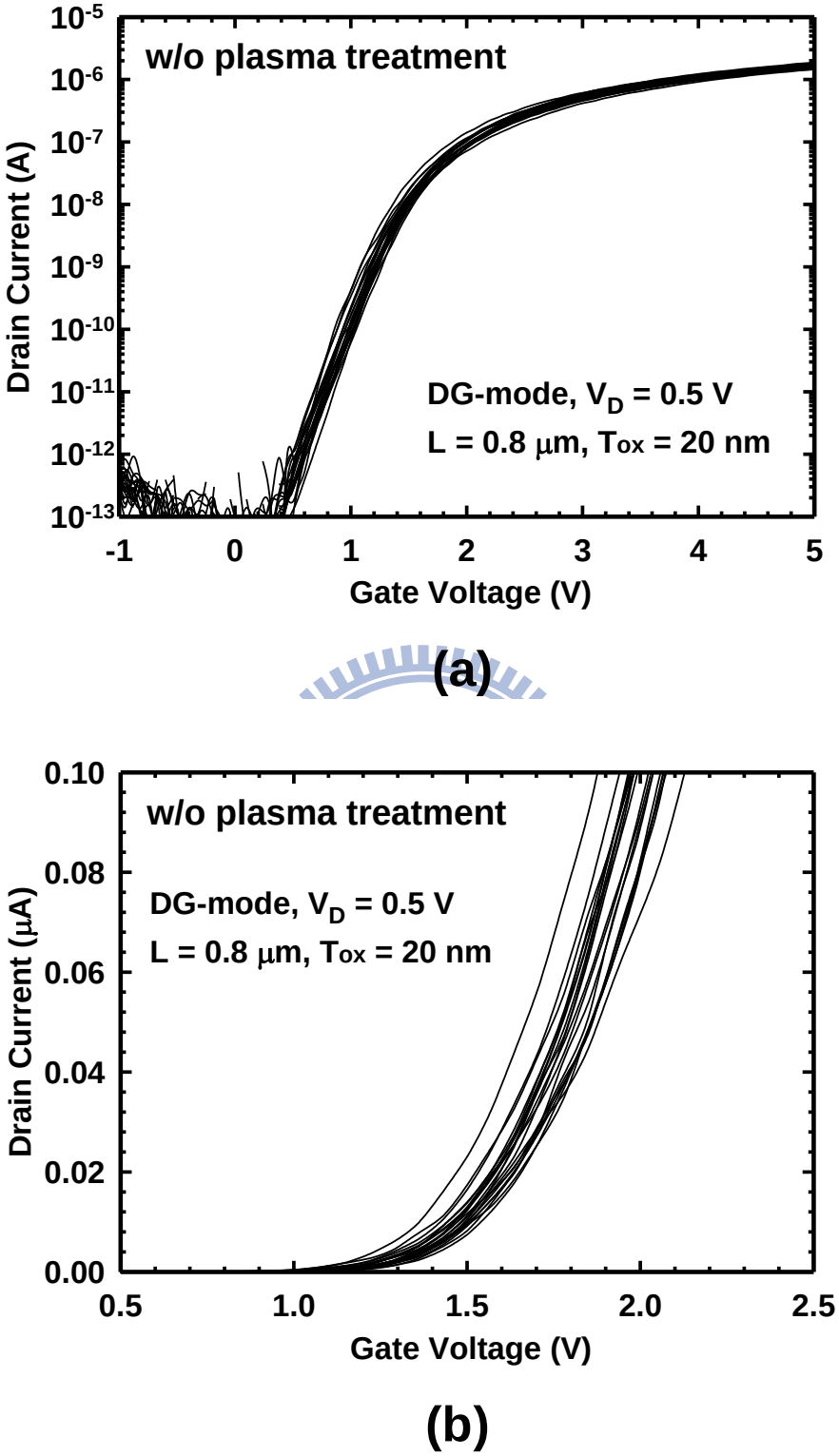


Fig. 2-31 Transfer characteristics under DG mode for poly-Si NW devices without NH_3 plasma treatment. (a) I_D in logarithmic scale. (b) I_D in linear scale. 20 devices were characterized in the plot.

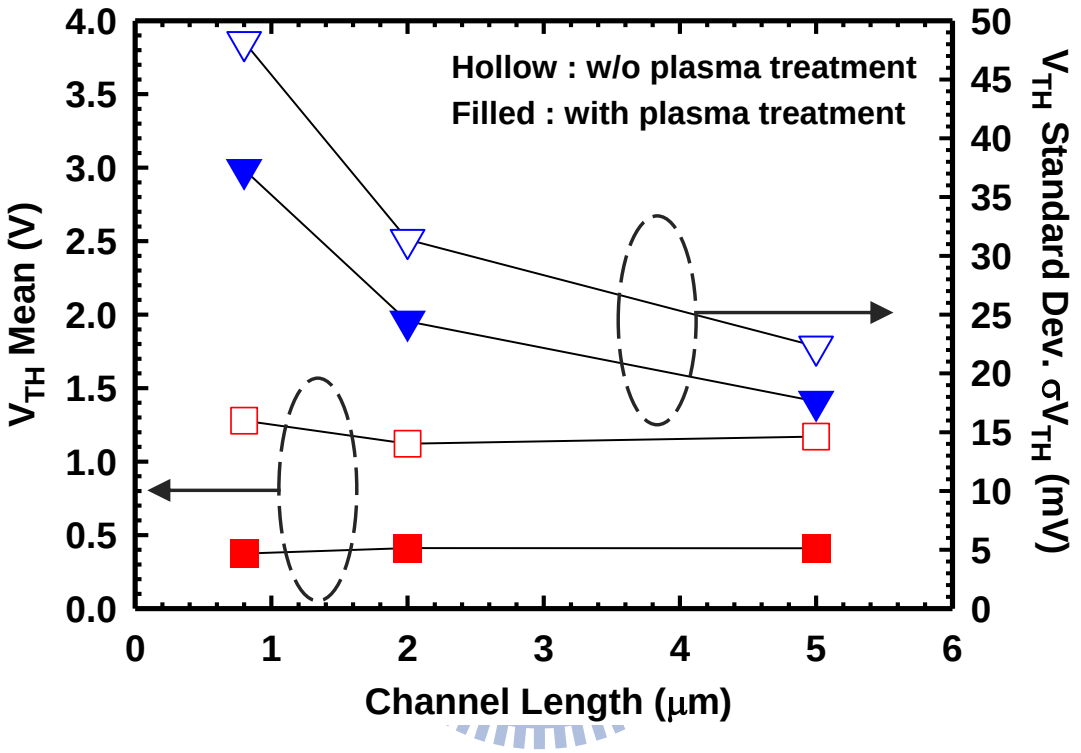


Fig. 2-32 Mean value and standard deviation of V_{TH} as a function of channel length for devices operated under DG mode.

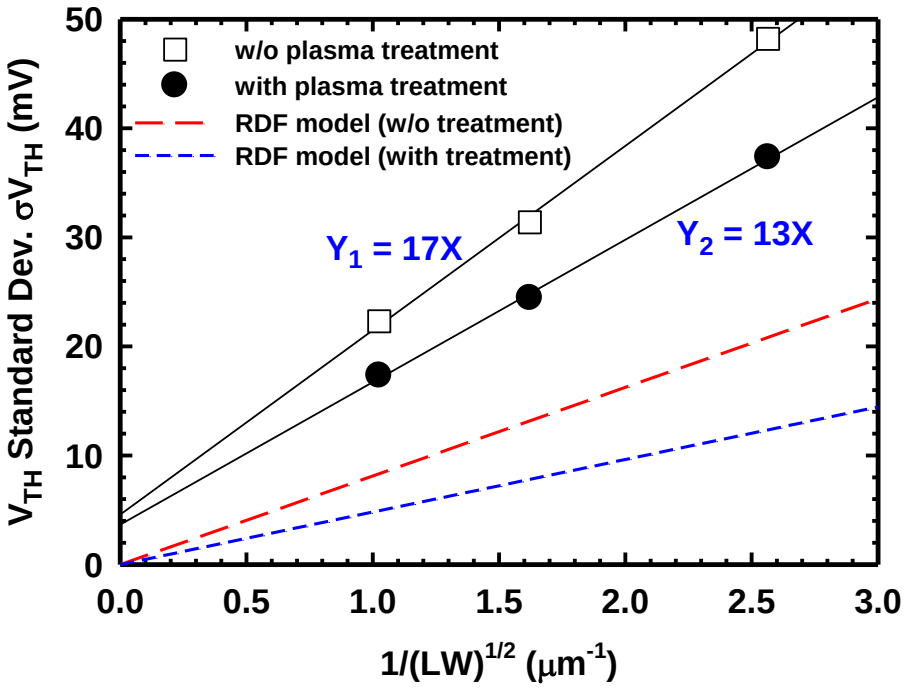


Fig. 2-33 Standard deviation of V_{TH} (σV_{TH}) as a functions of $(LW)^{-1/2}$ for devices with and without plasma treatment under DG mode of operation.

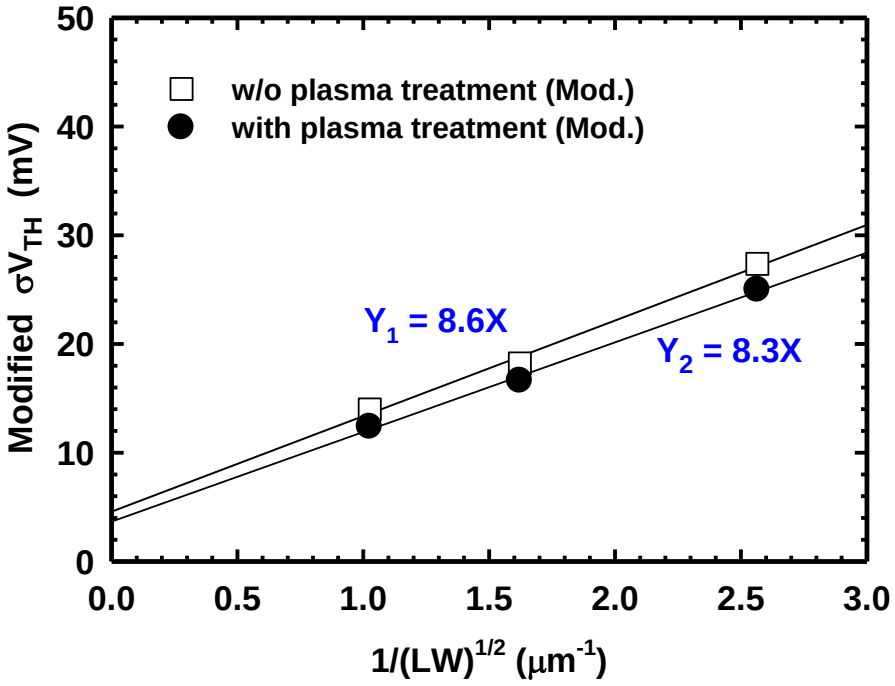


Fig. 2-34 Modified σV_{TH} as a functions of $(LW)^{-1/2}$ by deducting the calculated value of RDF model from Fig. 2-33.

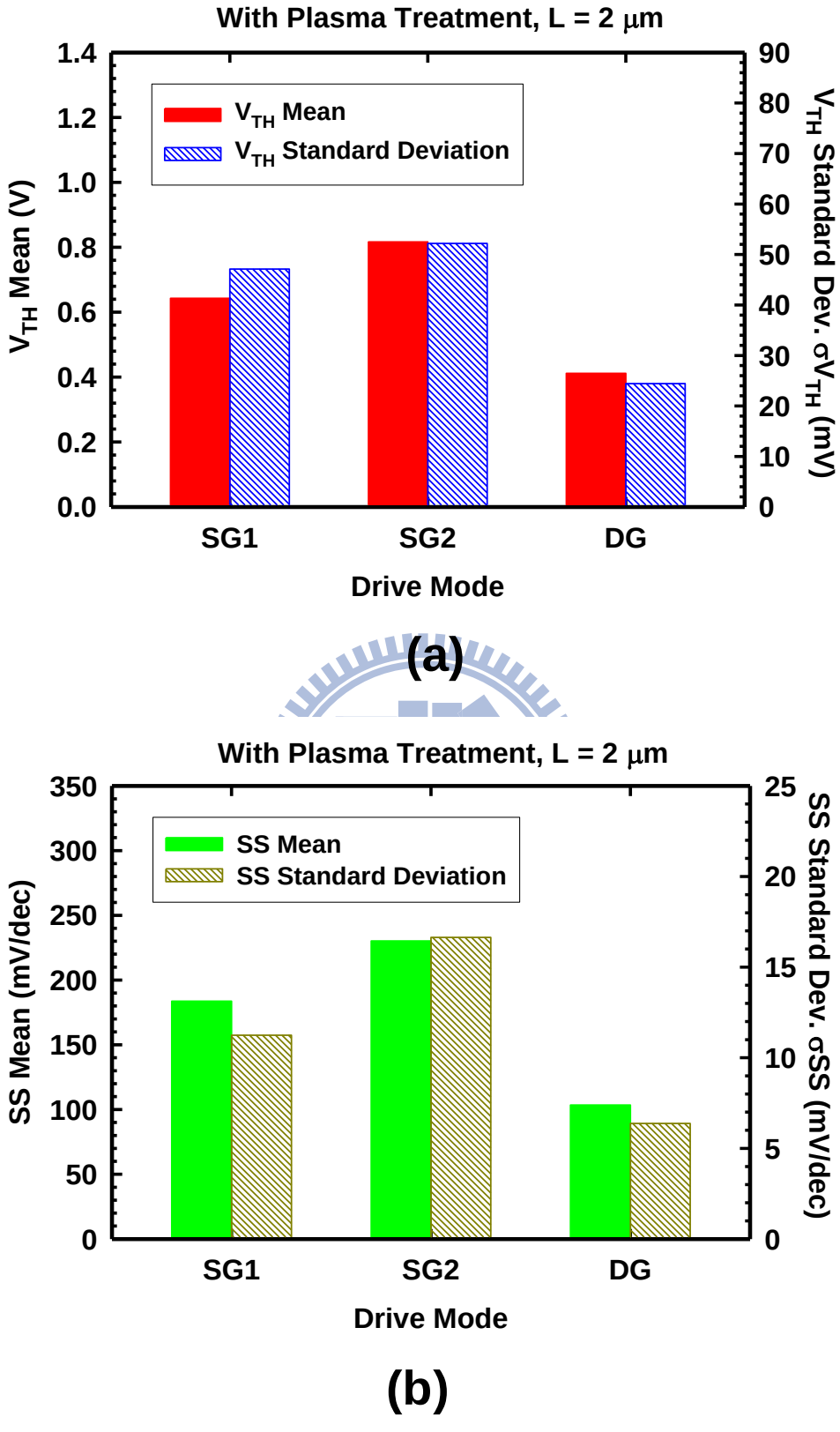


Fig. 2-35 Mean values and standard deviations of (a) V_{TH}, (b) SS for plasma-treated devices with channel length of 2 μm under three different operation modes.

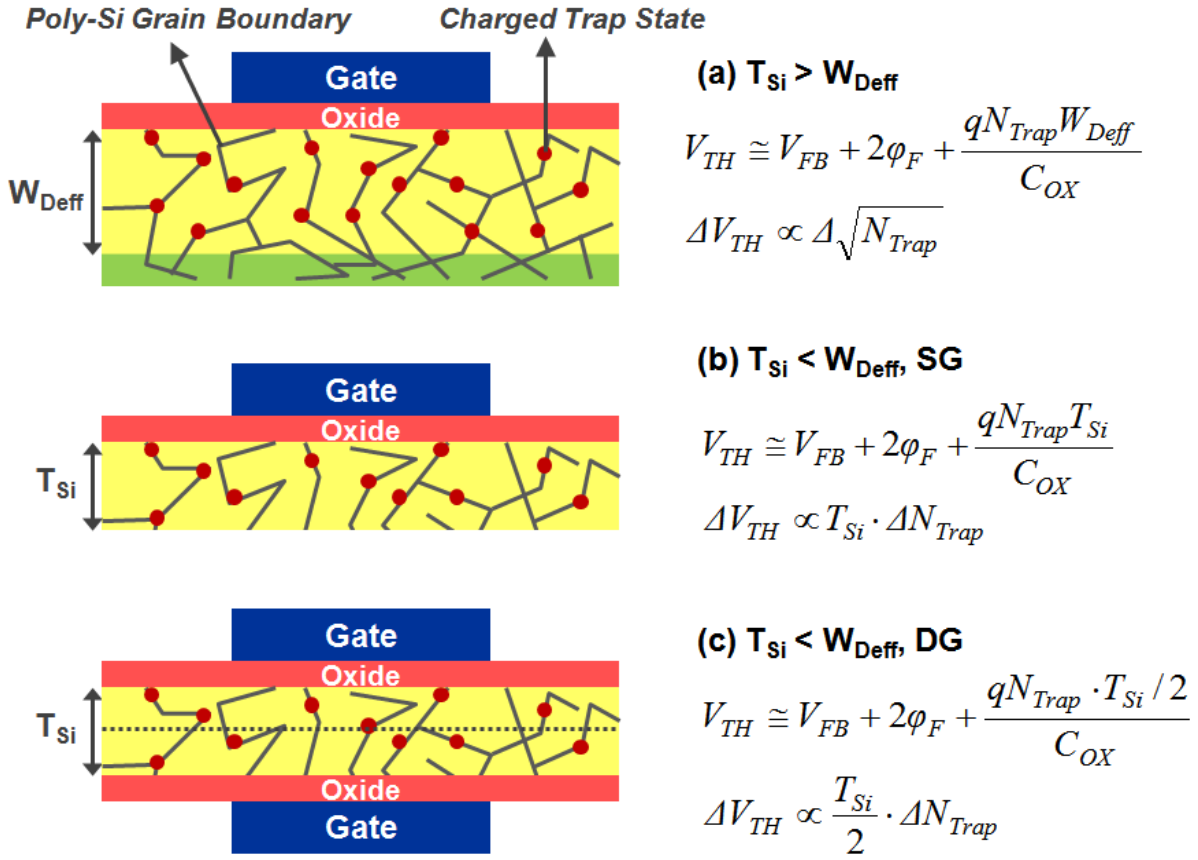
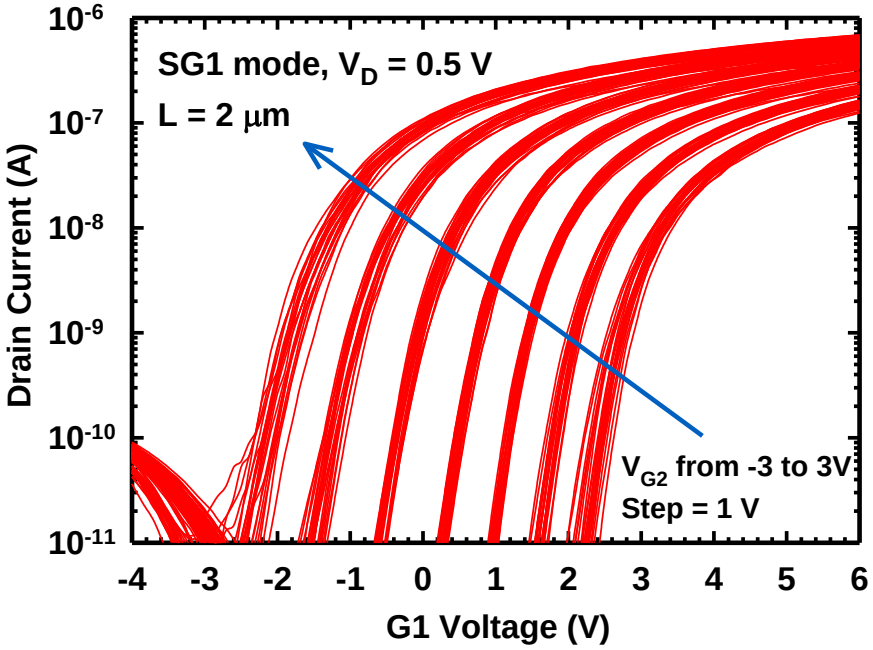
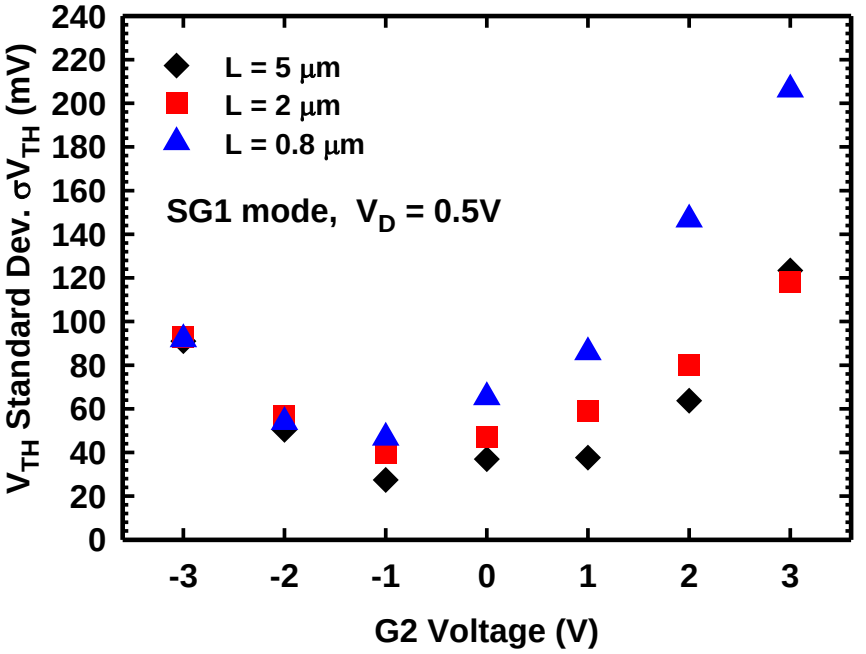


Fig. 2-36 V_{TH} dependence on the poly-Si channel thickness: (a) single-gated devices with partially depleted channel, (b) single-gated devices with fully depleted channel, and (c) double-gated devices with fully depleted channel [2.32].



(a)



(b)

Fig. 2-37 (a) Transfer characteristics of devices with channel length of 2 μm measured by sweeping G1 voltage and fixed G2 bias ranging from -3 V to 3 V. (b) σV_{TH} as a function of top-gate bias for devices with different channel length. 25 samples were characterized in each datum point.

Chapter 3

Multiple-Gated Poly-Si Nanowire Thin-Film Transistors Fabricated by Cavity Formation & Filling Technique

3-1 Introduction

The fine-grain structure of poly-Si thin-film transistors (poly-Si TFTs) is known to affect the carrier transport and device performance. Various methods have been proposed to enlarge the grain size of poly-Si thin films, including excimer laser annealing (ELA) [3.1] and metal-induced lateral crystallization (MILC) [3.2], in order to improve device characteristics. An alternative approach to minimize the negative impacts of the granular structure of the poly-Si film is to reduce the total amount of defects by thinning down the channel body. Recently, we have proposed a simple method to fabricate poly-Si NWTFTs by using sidewall spacer etching technique to define poly-Si NW channels, and the fabricated devices feature a single side-gate structure [3.3]. Improved characteristics over the planar counterparts, including reduced short channel effects (SCEs) and steeper subthreshold swing (SS) have been achieved [3.4]. However, the ON current of the proposed NW devices is limited by the small conduction width inherent with the single side-gate structure. This limitation is undesirable for practical applications. Moreover, for most NW fabrication methods, the poor controllability over nanowire dimensions and uniformity would lead to large

variations of device characteristics such as threshold voltage (V_{TH}), ON current, and SS [3.5] [3.6]. These issues must be carefully addressed before the NW devices can be inducted to practical application and mass production. In line with this, the adoption of a multiple-gated (MG) structure is promising [3.7, 3.8]. The MG configuration is expected to further improve the performance of poly-Si NWTFT devices through an increase in the effective channel width and enhanced gate controllability over the channel.

In this chapter, a new and simple method for fabricating MG poly-Si NW devices without resorting to advanced lithographic tools is proposed. In this method a novel cavity formation and filling technique is developed and implemented in the fabrication process, and its capability of patterning NW channels is also successfully demonstrated. The fabrication of the MG poly-Si TFTs is described in Section 3-2. The proposed device structures can be equipped with a tri-gate configuration, and fundamental characteristics of such tri-gate devices are presented and discussed in Section 3-3. To investigate the effectiveness of MG configurations, we also propose a clever scheme (also described in Section 3-2) to fabricate devices with identical NW channels but different gate configurations. Then, fluctuation properties of these fabricated devices are investigated and discussed in Section 3-4. Impacts of MG configurations on the variation of device performance could be unambiguously clarified with the designed test structures. In the final section, a brief summary is given.

3-2 Device Structures and Fabrication

3-2.1 Tri-Gated Poly-Si NWTFT

Figs. 3-1 (a) and (b) show top (layout) and stereo views, respectively, of the proposed tri-gated poly-Si NWTFT. It can be seen that three out of the four sides of the NW channels are modulated by the gate to ensure good gate controllability. Fig. 3-2 depicts the schematic process flow. The fabrication began on Si wafers capped with a 100-nm-thick thermal oxide. Next, a 40-nm-thick TEOS oxide and a 50-nm-thick nitride were deposited by low-pressure chemical vapor deposition (LPCVD) to serve as sacrificial layer and hard-mask layer, respectively (Fig. 3-2 (a)). After definition and formation of the dummy structure, the TEOS oxide was shrunk by a selective etching performed in an HF-containing solution in order to form cavities underneath the nitride hard-mask (Fig. 3-2 (b)). Then a 100-nm-thick conformal amorphous-Si layer was deposited to fill the cavities formed in the previous step, followed by an annealing step performed at 600 ℃ in N_2 ambient for 24 hours to transform the amorphous-Si into poly-Si. Source/drain (S/D) doping was then performed with implantation of phosphorus ion beam (P_{31}^{+}) at an energy of 30 keV and the dose of 1 × 10^{15} cm^{-2} (Fig. 3-2 (c)). Note that the portion of poly-Si filled in the cavities was shielded by the nitride hard-mask from implanted dopants during the implantation process, and therefore higher implant energy (30 keV) was used here to improve the uniformity of dopant distribution inside the S/D. After generating the S/D photo-resist patterns with standard I-line lithographic step, a reactive plasma etching step was performed to remove the poly-Si not protected by either nitride hard-mask or photo-resist. Owing to the anisotropic etching process, poly-Si NW channels underneath the nitride hard-mask were formed simultaneously during the S/D etching step (Fig. 3-2

(d)). Subsequently, the nitride hard-mask and TEOS oxide layers were selectively removed by a 2-step wet etching process using hot H_3PO_4 and diluted HF solution (Fig. 3-2 (e)) to expose the poly-Si NW, and a 20-nm-thick TEOS oxide layer was deposited to serve as the gate dielectric. Then a 100-nm-thick *in situ* doped n^+ poly-Si was deposited and patterned to serve as the gate electrode (Fig. 3-2 (f)). All devices were then covered with a 200-nm-thick TEOS oxide passivation layer. Finally, after the formation of test pads using standard metallization steps, all fabricated devices received an NH_3 plasma treatment for 2 hours.

Note that the etching rate of TEOS oxide in the shrinkage step was adjusted to a low value but with high selectivity to both nitride hard-mask and underlying thermal oxide layers. As a result, the cross-sectional dimensions of poly-Si NW channel can be easily reduced to sub-100-nm scale with a careful control of the etching time. Cross-sectional TEM images of fabricated device with a NW channel as thin as 8 nm wrapped by the tri-gate are shown in Fig. 3-3.

3-2.2 Poly-Si NWTFTs with Three Different Gate Configurations

Another clever scheme similar to the foregoing method for fabricating NW devices with identical NW channels but various gate configurations was also developed. Key steps of the device fabrication are illustrated in Fig. 3-4. First, a 100-nm-thick TEOS and a 50-nm-thick nitride layers were sequentially deposited on Si substrates capped with a thermally grown buried oxide. After patterning the top nitride layer with an anisotropic plasma etching step (Fig. 3-4 (a)), an isotropic wet etching process was executed to etch TEOS oxide layer and form cavities under the nitride layer, as shown in Fig. 3-4 (b). The following process steps before the removal of hard-mask (Fig. 3-4 (c) and Fig. 3-4 (d-1)) were basically similar to those described

in Fig. 3-2 (c) and Fig. 3-2 (d). Next is the decisive step to determine the gate configuration: For Structure 1 (denoted as S1), the nitride hard-mask and dummy TOES were retained by skipping the wet etching process (Fig. 3-4 (d-1)), so that only one side of the NW channels is modulated by the gate, as shown in Fig. 3-4 (e-1). For Structure 2 (S2), the nitride hard-mask was selectively removed with a H_3PO_4-based wet etching step, while the dummy TOES was left intact (Fig. 3-4 (d-2)). For Structure 3 (S3), both nitride hard-mask and dummy TEOS were fully removed so as to expose the entire NW channels (Fig. 3-4 (d-3)). Subsequently, a 20-nm-thick TEOS gate oxide and an n+ poly-Si gate were formed in all device structures (Fig. 3-4 (e-1) to Fig. 3-4 (e-3)), followed by the deposition of TEOS passivation layer and test pads formation. All fabricated devices then received NH_3 plasma treatment for 2 hours. Consequently, S2 and S3 devices are supposed to have respectively two and three surfaces of the NW channel able to be modulated by the gate.

Cross-sectional TEM images of S2 and S3 NW devices are shown in Fig. 3-5 (a) and (b), respectively. The NWs of the two devices successfully demonstrate nearly identical cross-sectional shape with total peripheral length of around 110 nm despite receiving different wet etching steps in the fabrication, confirming the purpose of this fabrication approach. More importantly, the three types of gated structure having NW channels of identical shape and size would allow us to investigate and clarify the impacts of MG configurations on device performance as well as the variation of device characteristics.

3-3 Electrical Characteristics of Tri-Gated Poly-Si NWTFTs

Fig. 3-6 and Fig. 3-7 depict the transfer and output characteristics of tri-gated NWTFTs with channel length of 0.4 μm and 5 μm, respectively. It can be observed that a very steep SS as low as 100 mV/dec (@V_D = 3 V) is achieved, owing to the great controllability of tri-gate over the ultra-thin NW channels. For the device with 0.4 μm channel length, excellent ON/OFF current ratio up to 4.5×10^8 is obtained, while the drain-induced barrier lowering (DIBL) is negligible even in the short channel device, despite the rather thick gate oxide being used (20 nm). The ON current is extracted at V_G-V_{TH} = 3 V and V_D = 3 V, and the OFF current is defined as the minimal point from the I_D-V_G curve with V_D = 3 V. It is also worth noting that the tri-gated NW device exhibits relatively low OFF-state leakage as compare with that of the spacer-type NW device discussed in Chapter 2 (Fig. 2-5). This could be attributed to the use of higher ion implant energy in S/D implantation process, and thus the more uniform dopant distribution in S/D region is beneficial to mitigate the GIDL current.

The effective trap density per unit area, T_{Trap}, in the poly-Si NW channel could be extracted from SS of the devices with Eq. (2-21) mentioned in Chapter 2. For the tri-gated poly-Si NWTFT fabricated in this study, T_{Trap} is found to be around 6×10^{11} cm^{-2}, and the effective trap-state concentration, N_{Trap} (= T_{Trap}/W_{Deff}), of 1.5×10^{18} cm^{-3} is roughly estimated with the approximation of 4-nm-thick W_{Deff} (half of poly-Si NW thickness in this case). The extracted N_{Trap} is virtually commensurate to the deep-state (gap-state) density in general SPC poly-Si thin-film [3.9-3.11], which is mainly responsible for the SS behavior of poly-Si devices, hence corroborating the usefulness of Eq. (2-21). The above N_{Trap} estimation result clearly indicates the capability of

suppressing the impact of trap-state density on switching properties by thinning the poly-Si channel as well as utilizing MG configuration.

In comparison with conventional planar poly-Si TFTs, NWTFTs exhibit attractive device performance in terms of steeper SS and lower leakage current. However, the ON current is limited by the small conduction width of the tiny body of NW channels. Such feature is undesirable for large-area electronics applications. In order to further effectively increase the drive current for circuit operation, tri-gated devices with multiple NW channels were also fabricated and characterized. Fig. 3-8 displays an example of such multiple-channel device with 18 (2×3×3) NW channels in a single device layout, and accordingly the drive current is expected to be multiplied with this layout design. Transfer characteristics of tri-gated NWTFTs with channel number of 18, 50, and 100 are shown and compared in Fig. 3-9. ON/OFF current ratio larger than 10^8 is achieved for devices with a large number of channels. Fig. 3-10 depicts the extracted SS and ON current of multiple-channel NWTFTs normalized to a single-channel device as a function of NW channel number. It is apparent that the ON current is simply proportional to the number of NW channels while the SS of each device is still around 100 mV/dec, demonstrating the effectiveness of this multiple-channel layout for NW devices.

3-4 Variability of Multiple-Gated Poly-Si NWTFTs

3-4.1 Impacts of Gate Configuration

Variability of the three types of NW devices shown in Fig. 3-4 is characterized in this subsection. Fig. 3-11 depicts typical transfer characteristics of NWTFTs with different gate configurations (S1, S2 and S3). For comparisons, data measured from a planar device with poly-Si channel of 50 nm and gate oxide and channel length identical to the NW devices are also included in the figure. The drain current is normalized to the channel width. From the figure it is clearly seen that the NW devices show much enhanced performance in terms of steeper SS, lower OFF-state leakage current, and higher normalized drive current as compared with the planar one. The improvements are ascribed to the reduction in the amount of defects contained in the channels with the NW structure. Among the three NW devices, S3 device exhibits the most desirable performance on account of its superior gate controllability with the gate-all-around (GAA) configuration.

The mean value and standard deviation of SS for devices of different gate configurations with channel length of 0.7 μm and 5 μm are shown in Figs. 3-12 (a) and (b), respectively. In the figures, it can be noticed that long-channel (5 μm) devices have smaller standard deviation (σSS) than the short-channel (0.7 μm) counterparts. Furthermore, S3 (GAA) structure has the smallest variation among the three gate configurations. Similar trend can also be found in V_{TH} distribution, as shown in Figs. 3-13 (a) and (b).

The above findings are consistent with the observations described in Section 2-5 as well as the previous reports that the variation of device characteristics increases

as the device shrinks [3.12]. For bulk CMOS devices, major fluctuation sources include doping concentration in the channel, uniformity of thin films, S/D resistance, and line edge roughness [3.12, 3.13]. According to the V_{TH} fluctuation model proposed in [3.14] and modified in Section 2-5, the standard deviation of V_{TH} (σV_{TH}) for devices having poly-Si channel is expressed as follows:

$$\sigma V_{TH} = \frac{q}{C_{ox}} \sqrt{\frac{N_{Trap} W_{Deff}}{3LW}}, \tag{3-1}$$

where N_{Trap} is the trap-state density in the poly-Si channel, W_{Deff} is the effective depletion width, L is the channel length and W is the channel width. As stated in Section 2-5, although no intentional channel doping is performed, the defects contained in the grain boundaries may play a similar role as dopants does in conventional MOSFETs, leading to a V_{TH} variation behavior resembling the one caused by random-dopant fluctuation (RDF) effect. Based on Eq. (3-1), σV_{TH} of the NW devices is inversely proportional to $(LW)^{-1/2}$ in the case that the change in the shape of NW cross-section is negligible. Fig. 3-14 shows σV_{TH} as a function of $(LW)^{-1/2}$ (the "Pelgrom plot" [3.15]) with different types of gate structures, and the experimental data are consistent with the model. For comparisons, the results obtained from planar devices with identical gate oxide thickness are also included in the figure. Note that the effective channel width of one NW channel in S1, S2 and S3 structure are 40 nm, 65 nm and 110 nm, respectively (Fig. 3-5). It is seen that the slopes of linear fitting lines for the NW devices are obviously lower than that of conventional planar TFTs. This is mainly due to the tiny body of NW channels which leads to a much thinner W_{Deff} than that of planar devices. Furthermore, the slope of the linear fitting line for S3 structure is the lowest among the three splits of NWTFTs. This is a clear evidence of the effectiveness of GAA structure in reducing the impact of W_{Deff}.

However, as discussed in Section 2-5, the apparent non-zero Y-intercepts of the linear fitting lines of experimental data in Fig. 3-14 indicates additional global variation sources, which could be related to wafer-scale non-uniformity of film thickness and NW dimensions caused by process variations in deposition and etching steps (*i.e.*, the formation of cavities in this case, as described in Section 3-2). Since the channel film thickness of planar TFTs did not suffer from etching variation and should be less sensitive to the deposition process because of the thicker channel body, the Y-intercept of planar device shows reasonably smaller value than those of the NW splits. This finding also suggests that the uniformity of thin-film deposition and etching processes associated with cavity formation could be another critical issue strongly affecting the variation of NW devices fabricated by this method.

3-4.2 Impacts of Multiple-Channel Configuration

Since V_{TH} fluctuation is proportional to $(LW)^{-1/2}$, further reduction in NW device variability is expected with the use of multiple-channel layout depicted in Fig. 3-8, owing to the direct increase in the total effective conduction width (W_{eff}). This proposition is demonstrated in Fig. 3-15, in which the transfer characteristics of devices with channel number of 2, 6, 20, and 100 are shown. In each figures 20 devices were measured. It is evident that the distribution of the measured I_D-V_G characteristics becomes tighter as NW channel number increases. The mean value and standard deviations of V_{TH} and SS for multiple-channel devices built with S3 structure are shown in Figs. 3-16 (a) and (b), respectively. As channel number increases, σV_{TH} and σSS both indeed become smaller. Fig. 3-17 shows a typical Pelgrom plot of the multiple channel devices, and the trend of σV_{TH} is again correspondent with the modified RDF model described in the previous subsection 3-4.1 and Section 2-5.

3-5 Summary

In this chapter, the effects of multiple-gate configurations on the characteristics of poly-Si NWTFTs are investigated. A novel tri-gate poly-Si NWTFT scheme that can be fabricated without resorting to advanced lithographic tools is proposed. The fabricated devices exhibit excellent ON/OFF current ratio higher than 10^8 and steep SS as low as 100 mV/dec. Moreover, a multiple-channel layout scheme is also proposed and demonstrated to multiply the drive current without degrading device performance. Besides, we have also proposed a clever scheme to fabricate three types of poly-Si NWTFTs with different gate configurations but identical NW channels. Such scheme allows us to investigate unambiguously the impact of multiple-gate configuration on the performance variation of poly-Si NW devices. Our results clearly indicate that the S3 structure, which has the largest portion of the NW channel surface under effective gate modulation, shows the least fluctuation in SS and V_{TH}. Additionally, with the increase in channel number of the NWTFT, the device fluctuation can be further suppressed.

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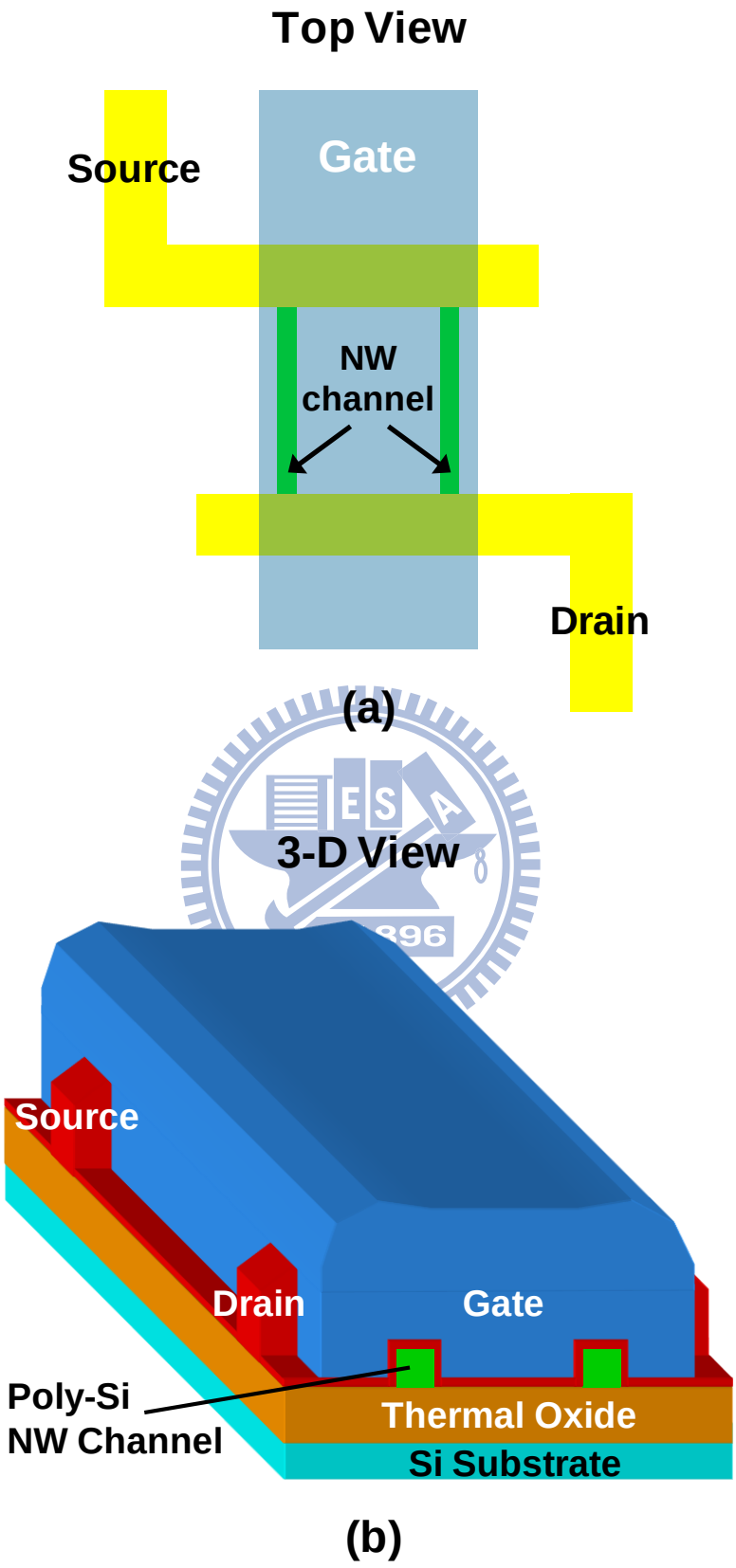


Fig. 3-1 (a) Top view and (b) 3-D structure of the tri-gated TFT device with poly-Si NW channels.

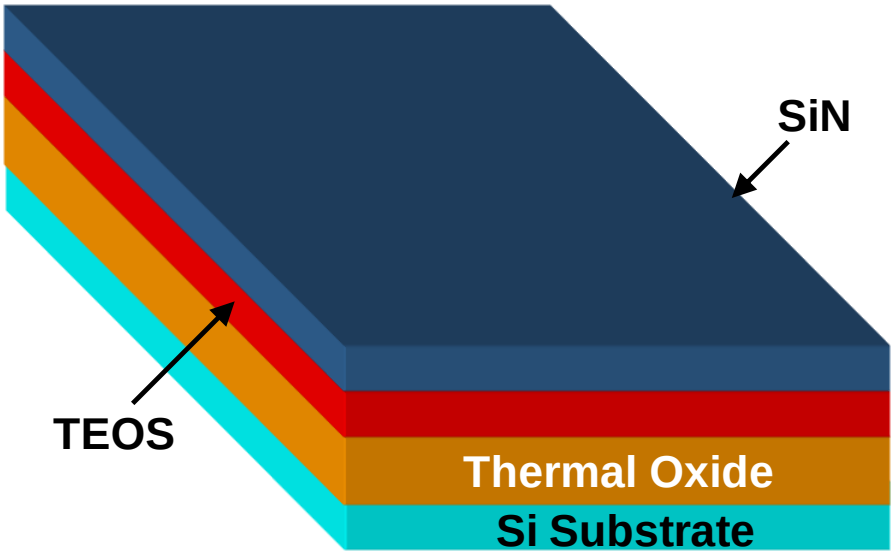


Fig. 3-2 (a) Deposition of TEOS oxide and nitride dummy layers on a Si substrate capped with a thermal oxide.

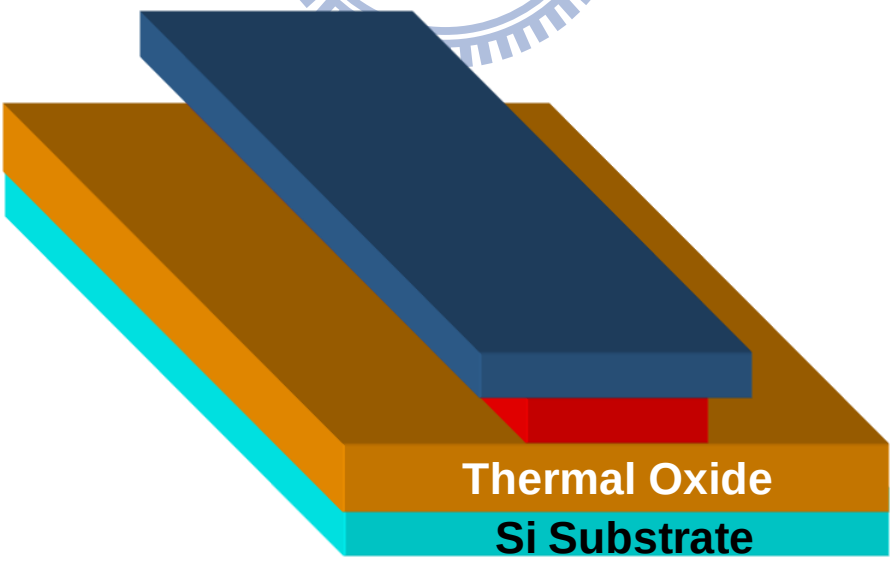


Fig. 3-2 (b) Formation of cavities by selective wet etching of the TEOS oxide.

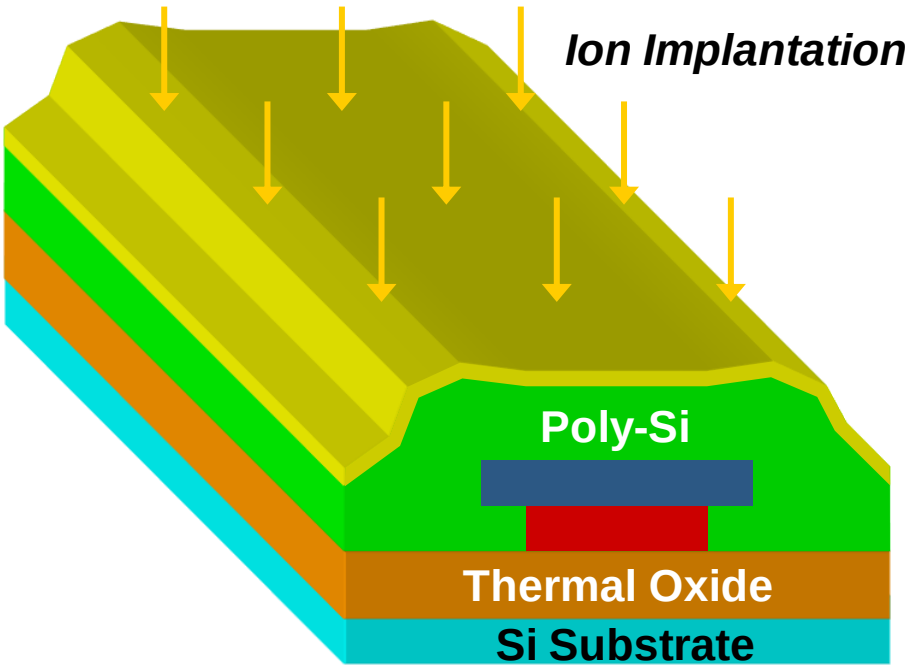


Fig. 3-2 (c) Phosphorus ion (P_{31}^{+}) implantation.

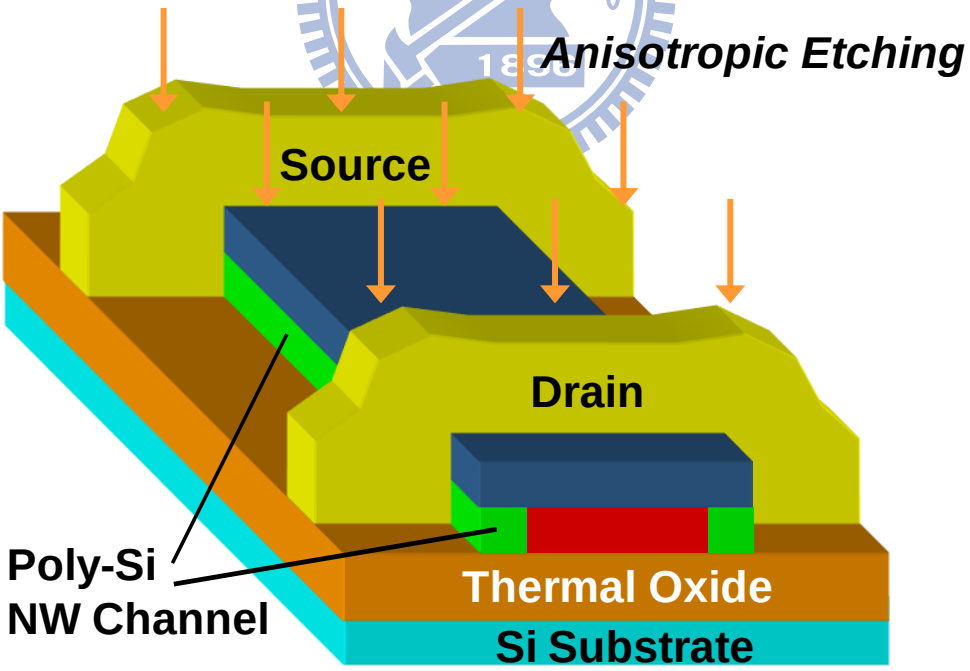


Fig. 3-2 (d) Definition and formation of source/drain (S/D) and NW channels by an anisotropic etching.

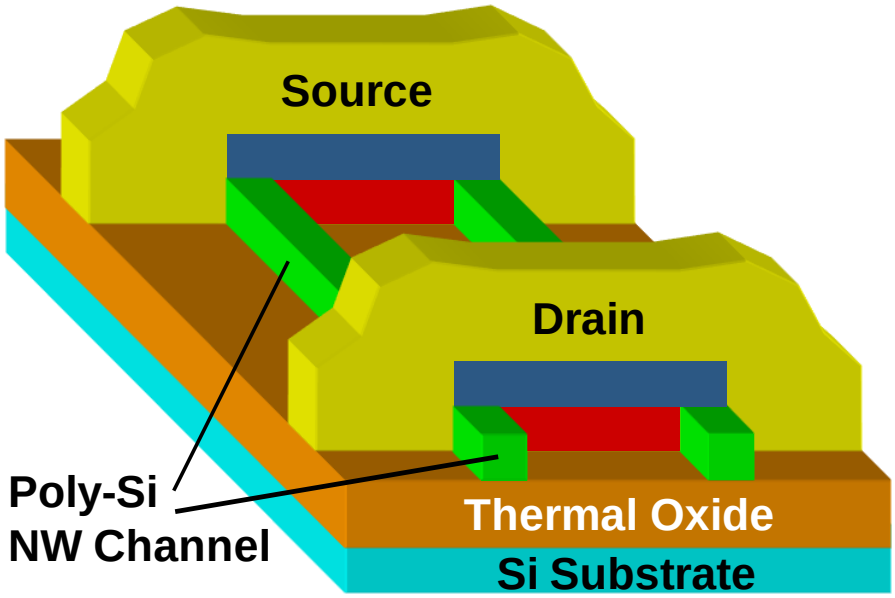


Fig. 3-2 (e) Removal of nitride hard-mask and TEOS dummy layers by a 2-step selective wet etching.

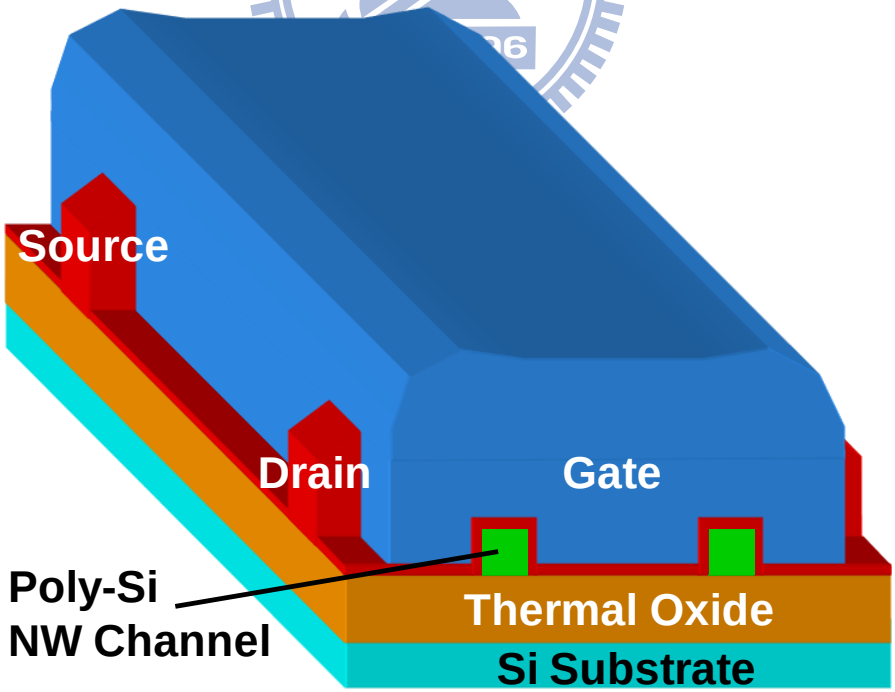


Fig. 3-2 (f) Deposition of gate oxide and formation of poly gate electrode.

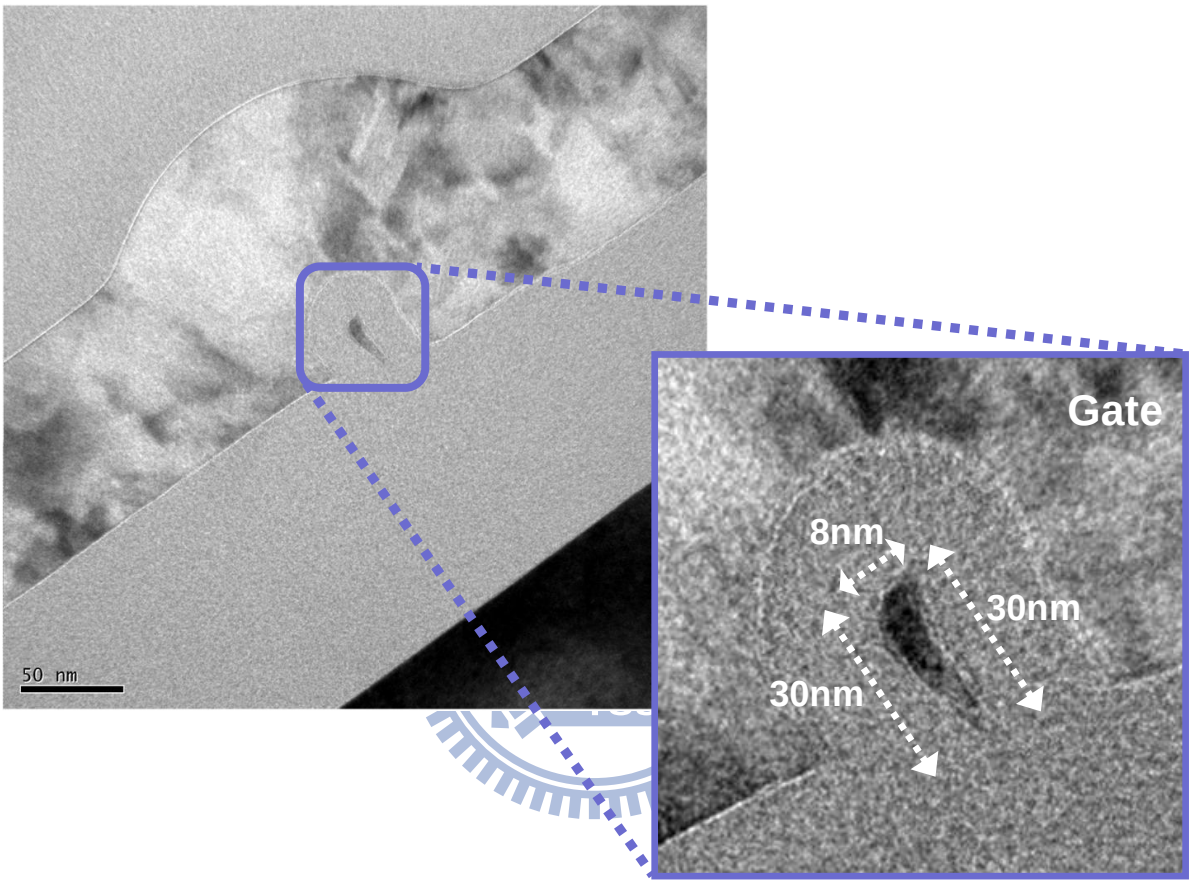


Fig. 3-3 Cross-sectional TEM images of the tri-gated NWTFT.

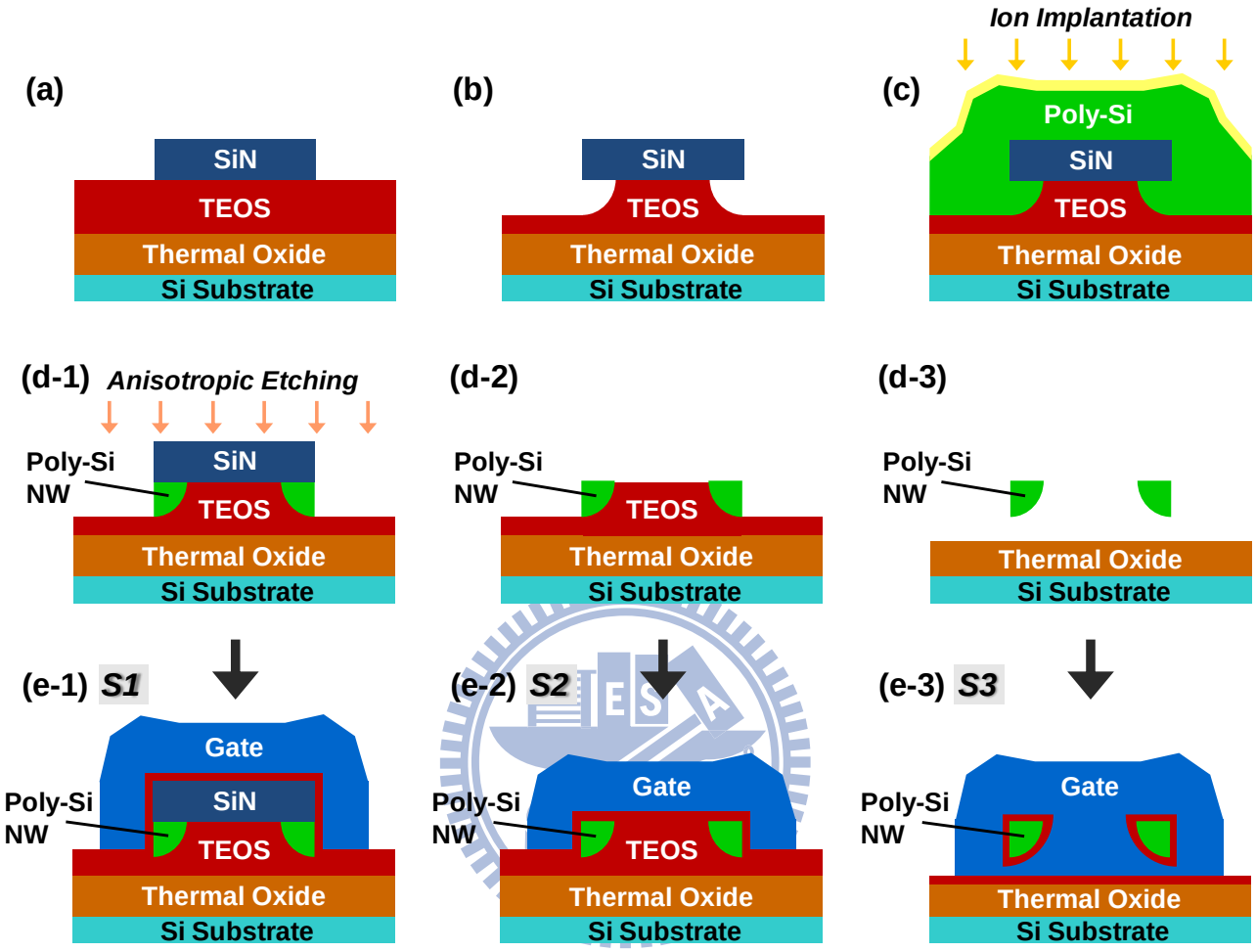


Fig. 3-4 Key steps for fabricating NWTFTs with various gate configurations. (a) Patterning nitride hard-mask by anisotropic reactive plasma etching. (b) Formation of undercut (cavity) by selective wet etching TEOS dummy layer. (c) a-Si deposition and annealing, and S/D implant. (d-1) Definition and formation of S/D and NW channel by anisotropic etching. (d-2) Nitride removal with hot H_3PO_4. (d-3) TEOS removal by DHF. (e-1 to e-3) Deposition of gate oxide and formation of poly gate for three types of NW devices (S1, S2 and S3).

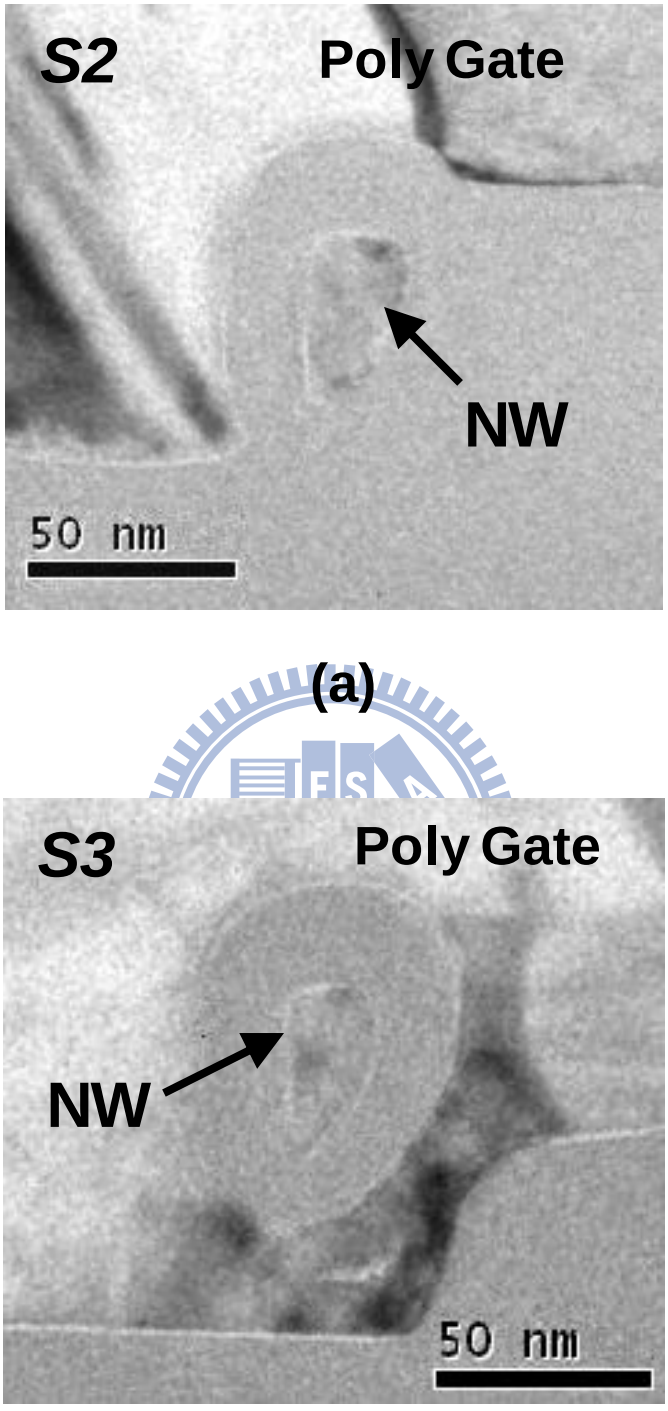


Fig. 3-5 Cross-sectional TEM images of (a) S2 and (b) S3 NWTFTs.

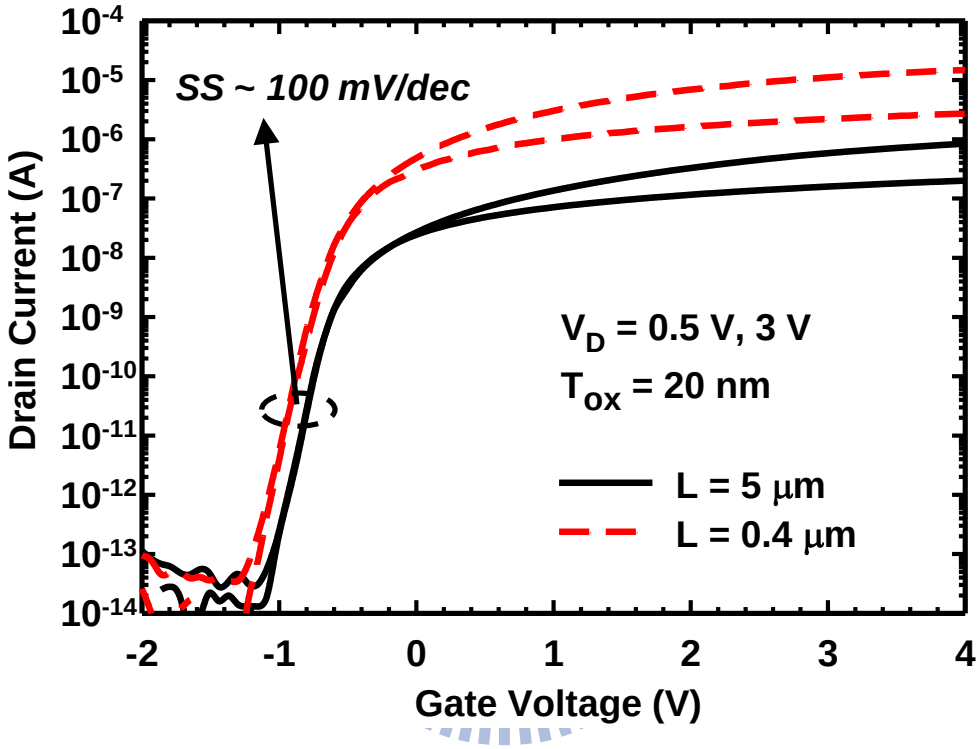
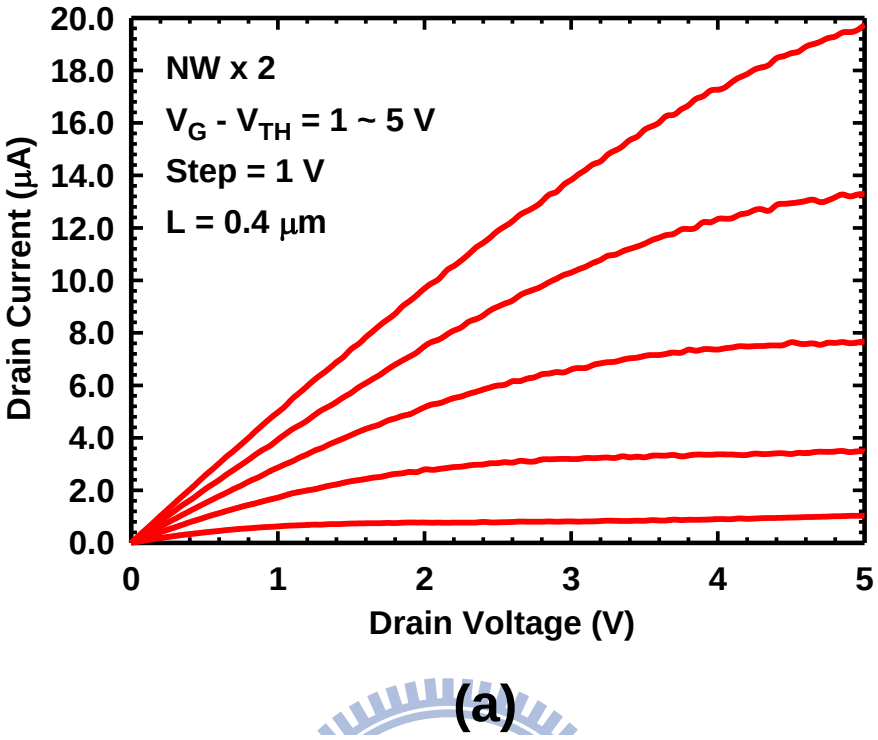
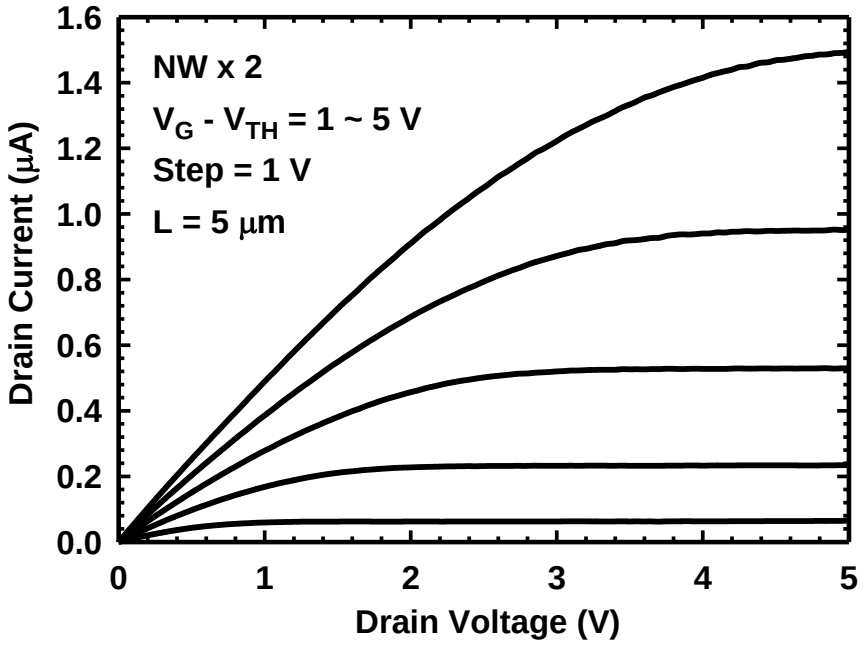


Fig. 3-6 Transfer characteristics of tri-gated NWTFT with L = 0.4 μm and 5 μm.



(a)



(b)

Fig. 3-7 Output characteristics of tri-gated NWTFT with (a) L = 0.4 μm and (b) L = 5 μm.

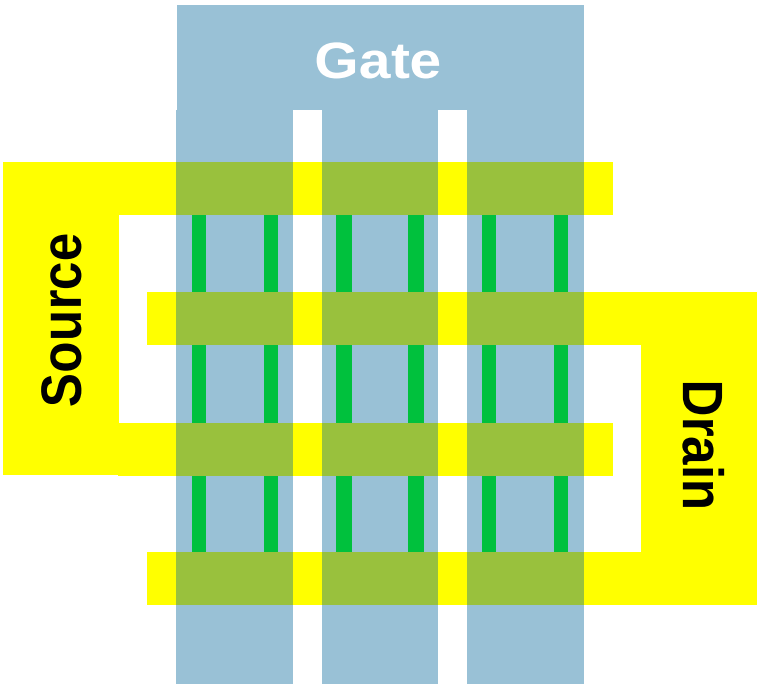


Fig. 3-8 Layout of an NWTFT with multiple channels. In this example, the number of channel is 18.

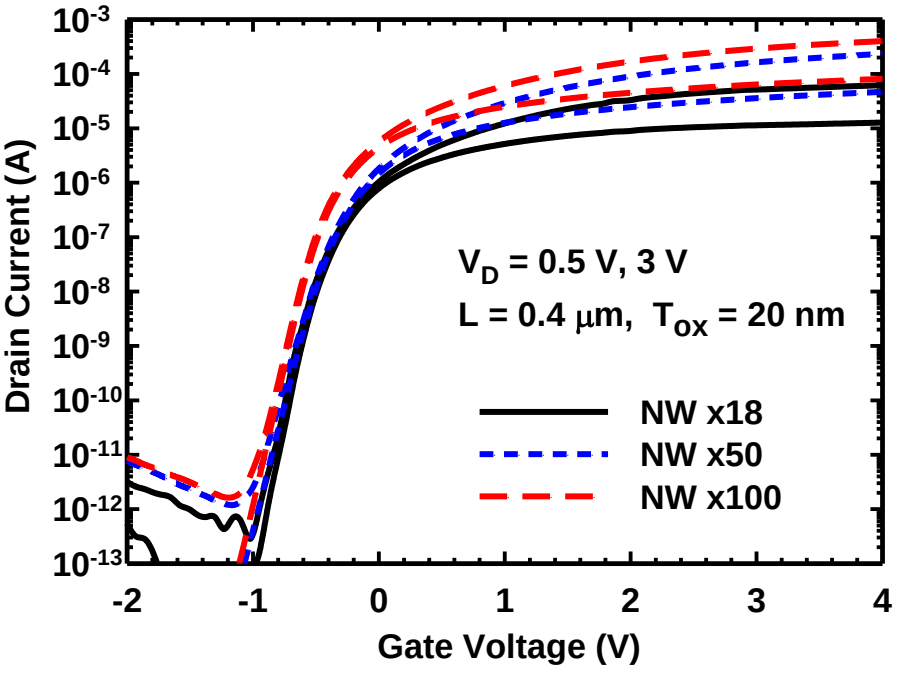


Fig. 3-9 Transfer characteristics of tri-gated NWTFT with various NW channel numbers.

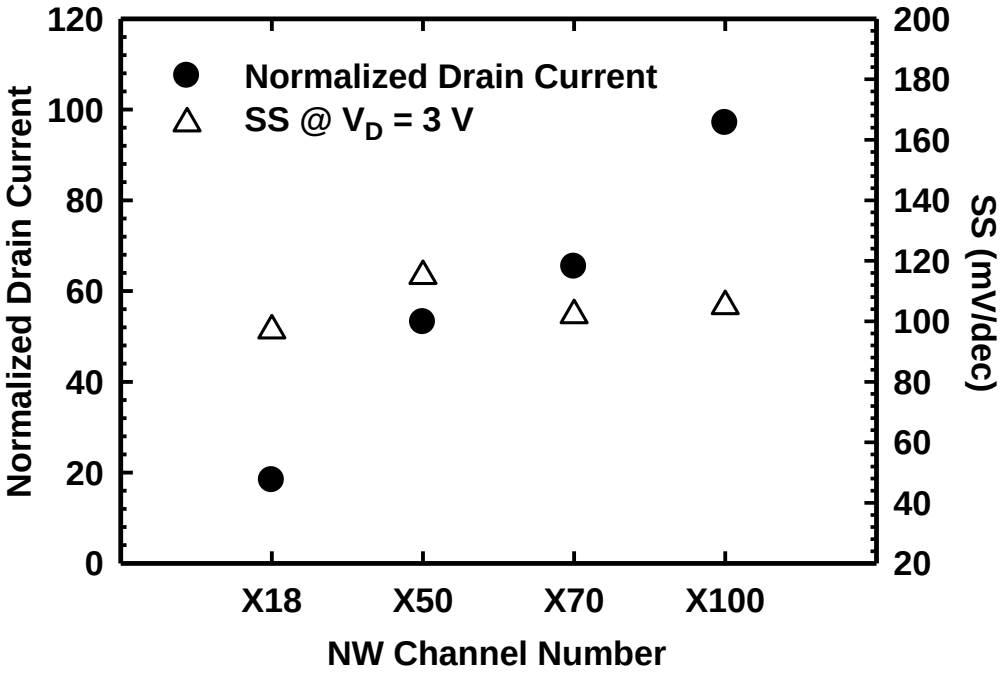


Fig. 3-10 Normalized drain current and subthreshold swing (SS) of NWTFTs as a function of channel number.

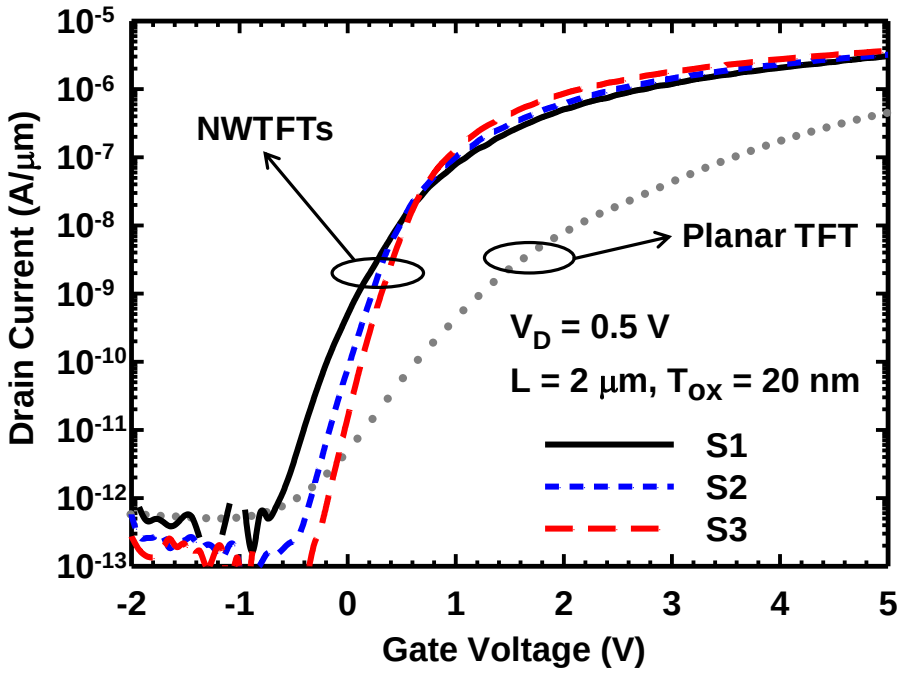


Fig. 3-11 Transfer characteristics of S1, S2, and S3 NWTFTs with L = 2 μm.

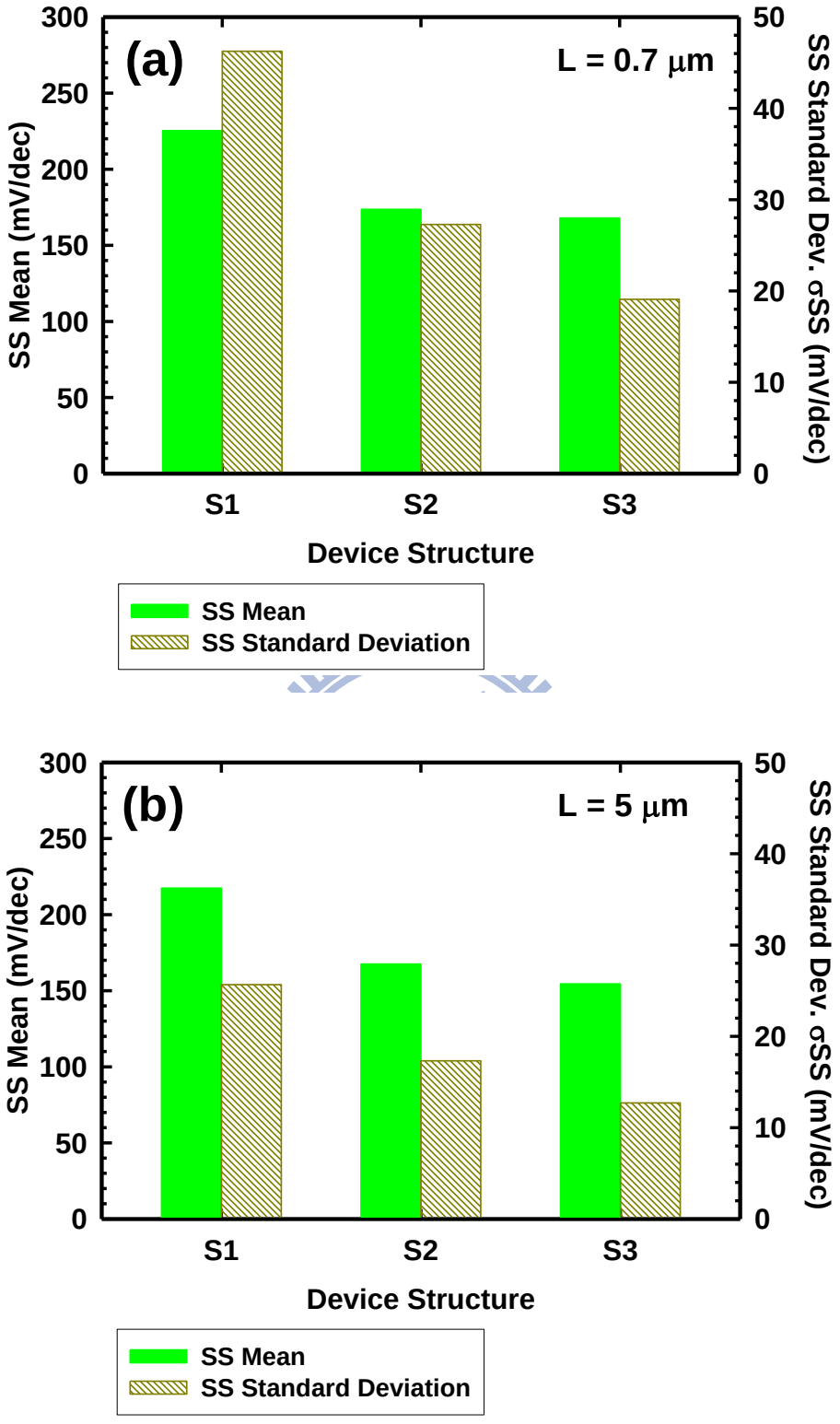


Fig. 3-12 Mean value and standard deviation of SS of NWTFTs with (a) L = 0.7 μm and (b) L = 5 μm. 20 samples were characterized for each device condition.

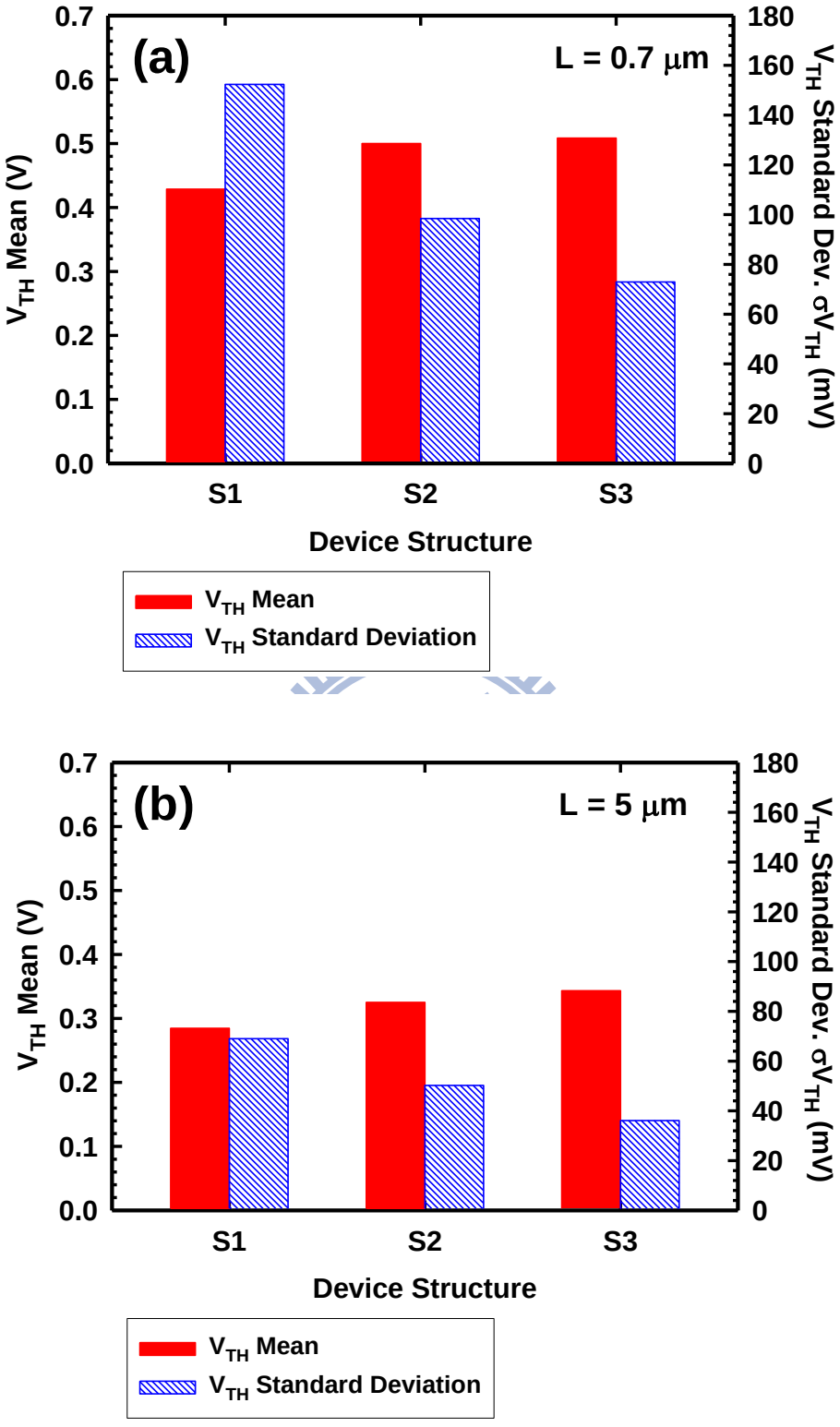


Fig. 3-13 Mean and standard deviation of threshold voltage (V_{TH}) of NWTFTs with (a) L = 0.7 μm and (b) L = 5 μm. 20 samples were characterized for each device condition.

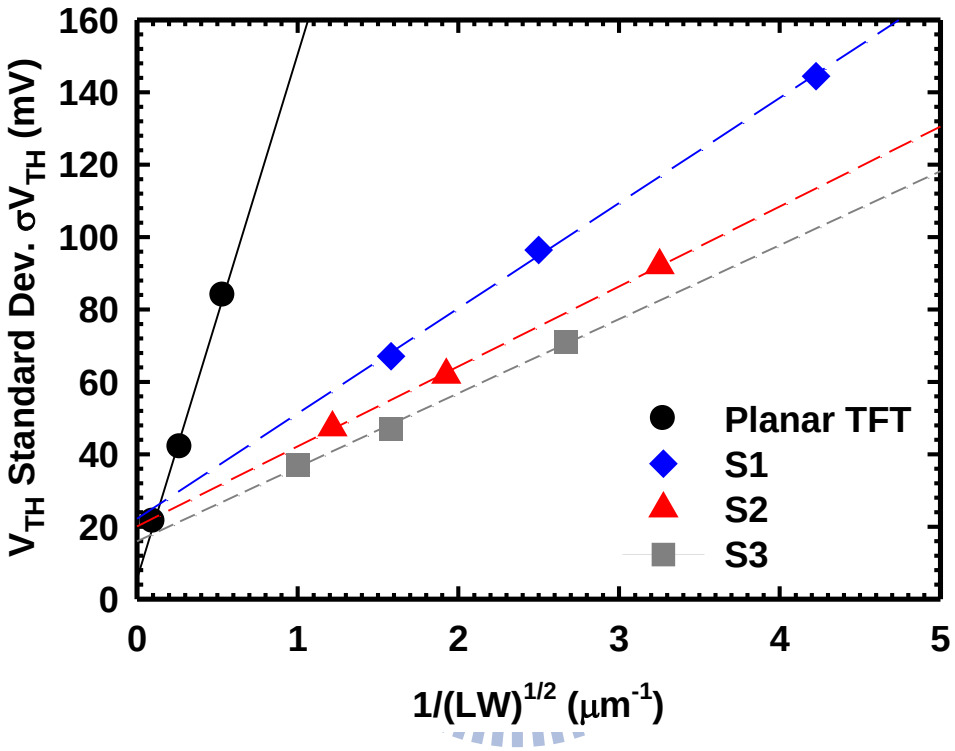


Fig. 3-14 Standard deviations of V_{TH} (σV_{TH}) as a function of $(LW)^{-1/2}$ for both planar and NW TFTs.

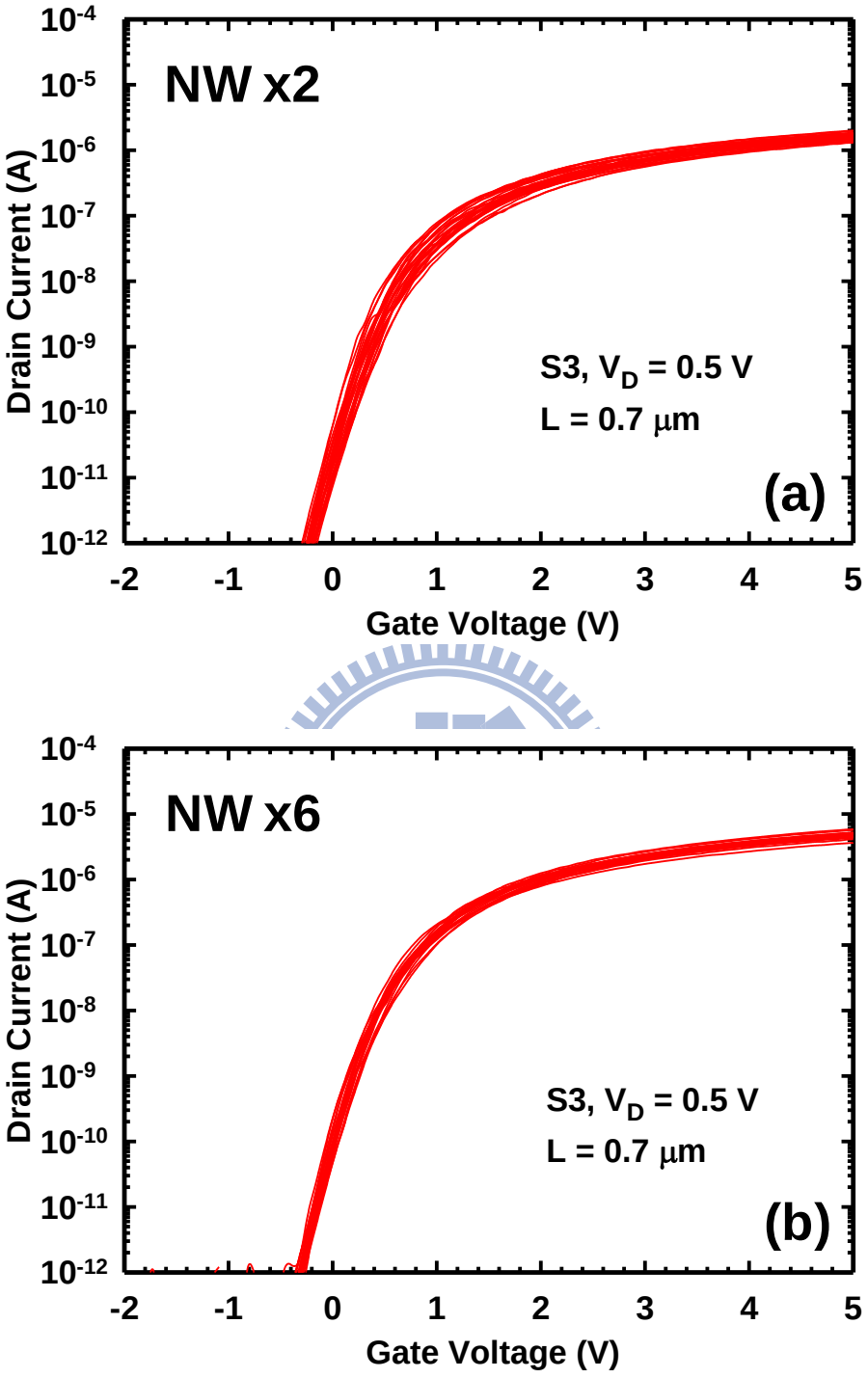


Fig. 3-15 Transfer characteristics of NWTFTs with S3 structure for channel number of (a) 2 and (b) 6. The channel length is 0.7 μm. 20 samples were characterized in each figure.

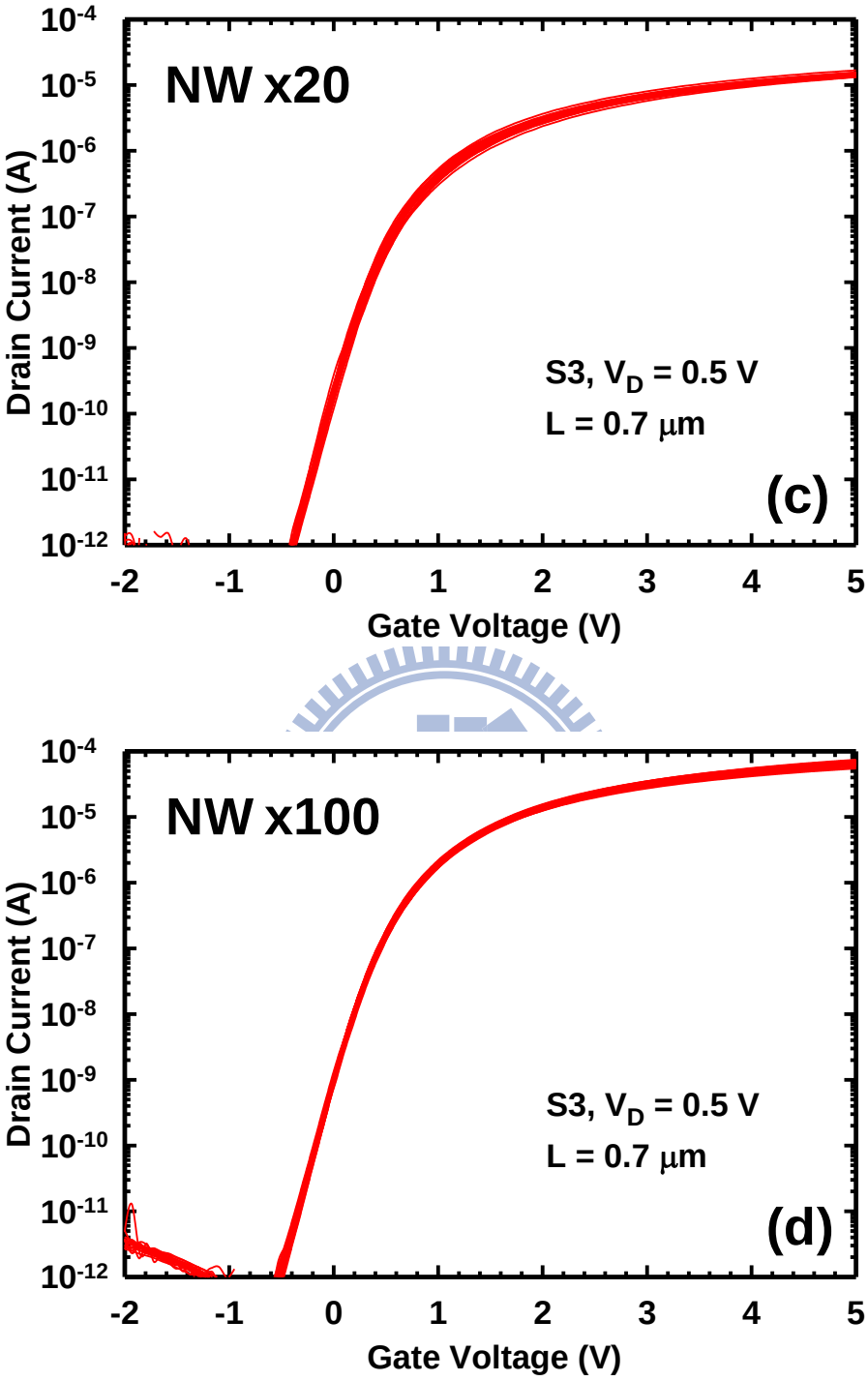


Fig. 3-15 Transfer characteristics of NWTFTs with S3 structure for channel number of (c) 50 and (d) 100. The channel length is 0.7 μm. 20 samples were characterized in each figure.

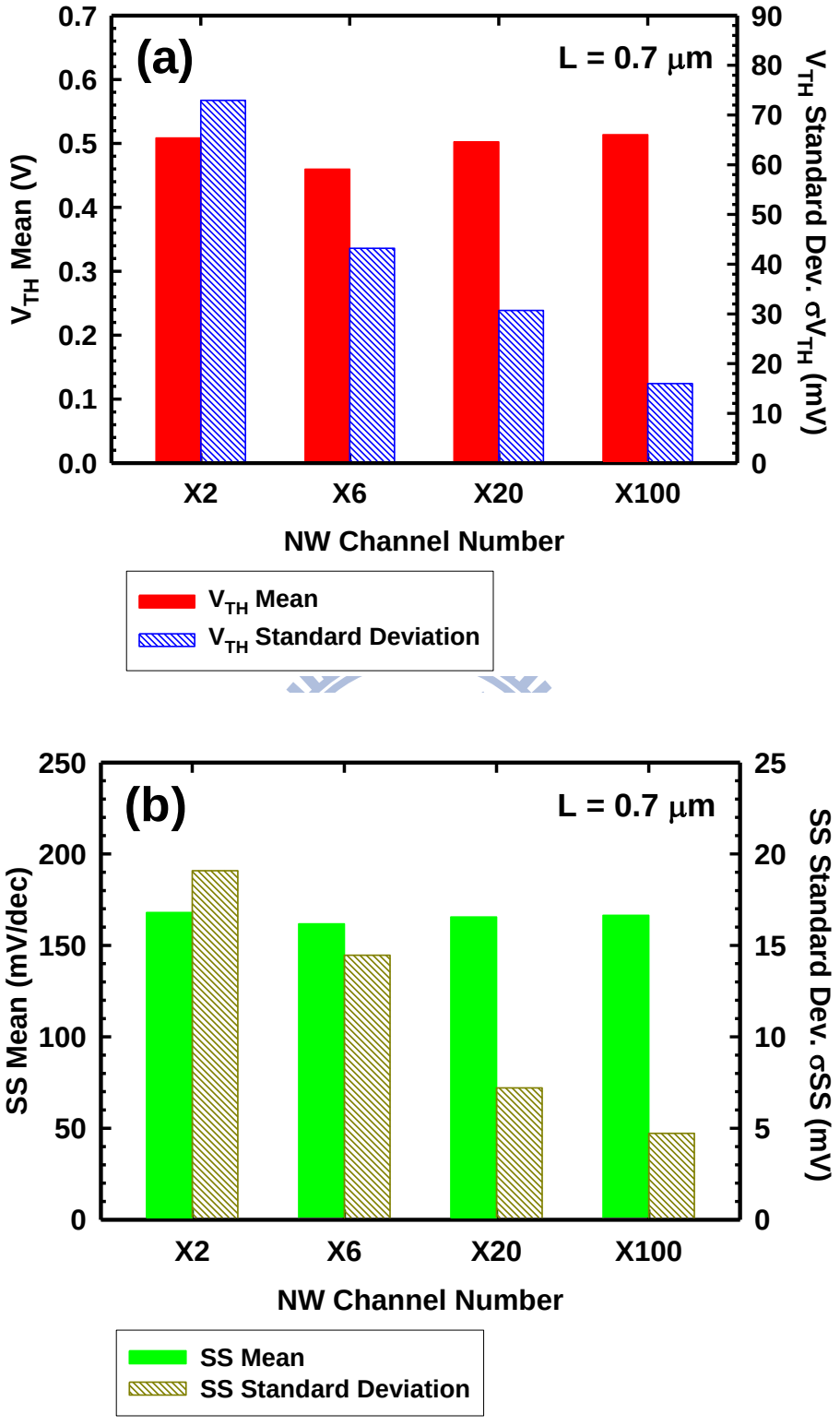


Fig. 3-16 Mean value and standard deviation of (a) V_{TH} and (b) SS for S3 devices of various channel numbers.

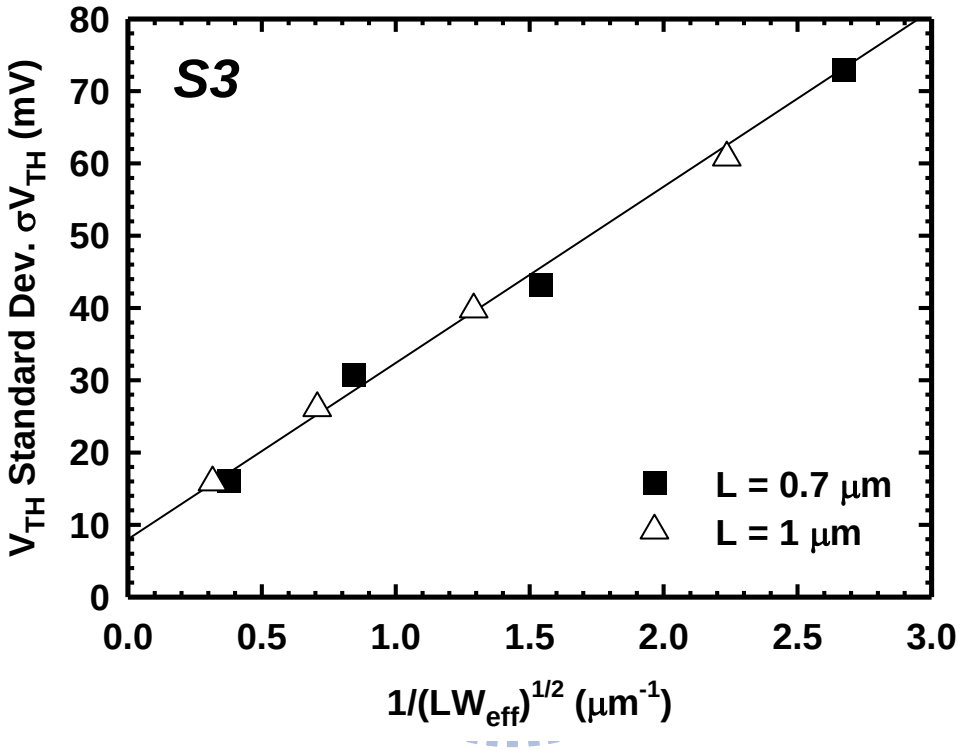


Fig. 3-17 σV_{TH} as a function of $(LW_{eff})^{-1/2}$ for S3 devices of various channel numbers.

Chapter 4

Impacts of Multiple-Gated Configuration on the Characteristics of Poly-Si Nanowire SONOS Devices

4-1 Introduction

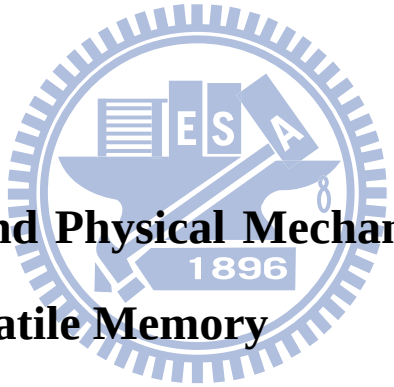
As mentioned in Chapter 1, silicon-oxide-nitride-oxide-silicon (SONOS) multi-layer structure has been widely exploited in recent charge-trapping flash (CTF) applications in view of its potential to overcome the difficulties encountered by the floating-gate flash [4.1-4.3]. SONOS devices replace the poly-Si storage layer used in floating-gate devices with a nitride trapping layer, in which the charges are discretely stored in the traps of the nitride. Unlike the case of using floating poly-Si as the storage site, a single defect generated in the tunneling oxide of a SONOS device during operation would not cause any catastrophic failure, *i.e.*, all stored charges would not leak out through the single defect, hence ameliorated data retention characteristics can be obtained. Besides, the SONOS structure has a much shorter height as compared with the floating-gate structure, and the insulating nitride-trapping layer stores trapped charges discretely between two neighboring cells, so the SONOS memory can exhibit much stronger immunity against coupling interference. This is extremely important in memory device scaling. In addition to mainstream high-density memory applications, currently many studies have been devoted to

investigating the feasibility of applying SONOS structure to thin-film-transistors (TFTs) for the purpose of system-on-chip (SOC) or system-on-panel (SOP) integration [4.4, 4.5]. The TFT-SONOS array could be stacked vertically to form a 3-D configuration, allowing increased device density without aggressive scaling of device dimensions and also reduced power consumption.

It is also imperative that SONOS-type nonvolatile memory devices possess low programming/erasing (P/E) operation voltage, high P/E speed, and excellent reliability. However, some challenging issues existing in poly-Si TFT based thin-film memory devices, such as poor subthreshold swing (SS) and large leakage current, lead to the unavoidable high applied voltages for P/E operation and raise power dissipation concern. By introducing nanowire (NW) channel into a TFT structure, the SS and leakage current can be suppressed on account of better gate controllability and much reduced cross-sectional area of the leakage path [4.6-4.11]. Furthermore, since the NW channel is sensitive to its surface condition, a small amount of charge storage is able to induce a larger change in the threshold voltage (V_{TH}) and thus a larger memory window as compared with the planar counterpart [4.12, 4.13]. In this regard, the simulation results carried out by Fu *et al*. [4.14] has pointed out that, for a SONOS device with a cylindrical NW channel and gate-all-around (GAA) configuration, the electric field at the channel/gate dielectric interface can be three times higher than that of planar devices. Hence P/E time or voltage could be dramatically decreased.

In this chapter, several novel poly-Si NW-SONOS devices fabricated by a simple method using cavity formation and filling technique are demonstrated. With slight modifications in fabrication procedure of the scheme described in Chapter 3 (Section 3-2), three different types of gate configurations, namely, side-gated (SG), Ω-shaped gated (ΩG) and GAA, were implemented in the fabricated NW-SONOS

devices. Moreover, the impacts of different gate configurations on memory characteristics such as P/E efficiency are compared and discussed. The information should be helpful to clarify how the gate configuration affects the operation of NW devices and circuits. The physical mechanisms for P/E and reliability of SONOS-type nonvolatile memory (NVM) are briefed in Section 4-2 and 4-3, respectively. Section 4-4 describes experimental procedure including device fabrication and measurement setup. Basic transistor characteristics of the fabricated devices are shown and discussed in Section 4-5. And the memory characteristics involving P/E speed as well as reliability performance are given in Section 4-6 and 4-7, respectively. Section 4-8 is a brief summary to conclude the study presented in this chapter.



4-2 Operation and Physical Mechanisms of SONOS-Type Nonvolatile Memory

4-2.1 Program/Erase Operation Mechanisms

A typical structure of an n-type SONOS memory device is depicted in Fig. 4-1 (a). Fig. 4-2 illustrates energy band diagrams of the SONOS stack under flat-band (Fig. 4-2 (a)), positive gate bias (programming) (Fig. 4-2 (b)) and negative bias (erasing) (Fig. 4-2 (c)) conditions. In general, the working principle of programming operation is to force electrons to inject from the silicon substrate across the first SiO_2 layer (tunneling oxide), and then stored (trapped) in the energy states of defects in the silicon nitride (Si_3N_4) trapping layer. The blocking oxide adjacent to the gate electrode provides a barrier to prevent trapped charges from leaking through the gate.

The stored electrons result in a positive V_{TH} shift of the memory device so that the programmed state (P-state) can be achieved. For erasing operation, the stored electrons are compelled to be detrapped from the trapping sites, or holes are injected into the trapping layer to compensate or neutralize the trapped electrons, so as to lower V_{TH} and reach the erased state (E-state) (Fig. 4-1 (b)). To read the information (memory state) of the cell, a gate voltage (V_G) between V_{TH} of P-state and V_{TH} of E-state is applied to sense the current level (high for E-state, low for P-state), and thus the memory state can be distinguished (Fig. 4-1 (b)).

Various carrier injection mechanisms for P/E operation of flash memories have been widely explored and studied, including channel hot electron injection (CHEI) [4.15], Fowler-Nordhiem (FN) tunneling [4.16], direct tunneling (DT) [4.17], band-to-band tunneling induced hot carrier (BBHC) injection [4.18], *etc*. CHEI originates from the acceleration of the channel electrons transporting from the source to the drain, due to the large lateral electric field in the pinch-off region produced by the high applied drain voltage. When electrons gain sufficient energy along the mean free path, some of the "hot" electrons can surmount the potential barrier of channel/gate oxide interface and inject into gate stack (either trapped by gate dielectric or directly injected into gate terminal) since the positive gate bias is favorable for attracting electrons. In the case of tunneling mechanisms, the carrier in the Si channel is able to directly cross the forbidden gap of a thin gate oxide due to quantum-mechanical tunneling phenomenon. Figs. 4-3 (a) and (b) illustrate the band diagrams across the tunnel oxide of the SONOS devices for FN tunneling and direct tunneling, respectively. As the voltage drop in the oxide (V_{OX}) is higher than the conduction band offset of Si substrate and gate oxide (ϕ_B), FN tunneling may occur so that the electrons in Si substrate could tunnel into the conduction band of gate oxide through

the triangular energy barrier which is thinner than the physical thickness of gate oxide, then are accelerated by the high electric field and injected into the gate nitride (Fig. 4-3 (a)). As for V_{OX} smaller than ϕ_B, direct tunneling mechanism dominates the electron injection (Fig. 4-3 (b)). This often occurs when the oxide thickness is less than 3 nm. BBHC injection mechanism is related to the gate-induced drain leakage (GIDL) effect in MOSFET operation. For an nMOSFET, the negative gate bias and positive drain bias give rise to a depletion region deep into the n^+ drain area adjacent to the gate oxide, as depicted in Fig. 4-4. Consequently, the large band bending would facilitate electron tunneling from valence band to the conduction band (BTBT) of the n^+ drain region, and the hole left in the valence band would be accelerated by the strong lateral electric field, leading to possible hole injection toward the gate.

4-2.2 Reliability Mechanisms

Retention and endurance characteristics are two of the most important indicators for the reliability of a NVM device. Data retention refers to the ability of the memory cell to keep the trapped charges from loss for a long duration to retain the stored information. The standard retention time of commercial NVM products is 10 years with memory window larger than 0.5 V [ref?]. For a SONOS-type NVM, the charge loss paths from the trapping-layer could be thermionic emission with Frenkel-Poole mechanism, or tunneling mechanisms through either blocking oxide or tunneling oxide. Fig. 4-5 illustrates the band diagram with charge loss paths in SONOS device [4.19]. The combination of Frenkel-Poole emission (FP) and field-enhanced thermal excitation (TE) can excite the trapped charges, causing them to flow into Si conduction band. For tunneling mechanisms, the trapped electrons in the nitride could tunnel back to the conduction band of Si substrate (trap-to-band

tunneling (TB)), or to the interface traps of Si channel (trap-to-trap tunneling (TT)). Besides, holes from Si valence band may tunnel into the nitride traps under the influence of the internal electric field (band-to-trap tunneling (BT)). In general, the thickness and quality of tunneling oxide in SONOS memory has pronounced impact on data retention characteristics. Although a thinner tunneling oxide would result in faster P/E speed, data retention capability could degrade remarkably due to the shorter tunneling length. As regards oxide quality, defects contained in the tunnel oxide would promote charge loss through traps-assisted-tunneling, further deteriorating the data lost rate.

Endurance characteristics refer to the reliability of a memory device in terms of the number of P/E operations that can be performed on it without failure. Since high voltages are applied during P/E operations, the energetic carriers would damage the quality of tunneling oxide and hence generate more and more oxide-trap and interface-trap states, resulting in the degradation of device performance as well as memory window. Most commercially available nonvolatile memory products nowadays are guaranteed to endure at least 10k P/E cycles. Since the memory density in a chip has been increasing year by year, certain cell in the particular memory block is less likely to be programmed and erased. Consequently, endurance requirement of flash memory chips is expected to be relaxed from 10k P/E cycles for 2GB density to 1k P/E cycles for 16GB density [4.20].

4-3 Experimental of Poly-Si NW-SONOS Devices

4-3.1 Device Structures and Fabrication

Key steps of device fabrication are illustrated in Fig. 4-6. First, three dielectric layers consisting of 50-nm-thick bottom nitride, 40-nm-thick TEOS oxide, and 30-nm-thick dummy nitride were deposited sequentially by low-pressure chemical vapor deposition (LPCVD) on Si substrate capped with a thermal oxide (Fig. 4-6 (a)). After the patterning of dummy nitride/TEOS oxide stack by anisotropic plasma etching, further highly selective etching of the TEOS oxide with diluted HF (DHF) was performed subsequently to form the encroached rectangular-shaped cavities at the two sides of the patterns (Fig. 4-6 (b)). Then an un-doped a-Si layer was deposited by LPCVD at 560 ℃. By taking advantage of the excellent filling capability of LPCVD process, the cavities formed in last step could be refilled by the deposited a-Si. An annealing step was then performed at 600 ℃ in N_2 ambient for 24 hours to transform the a-Si into polycrystalline phase. Afterwards, source/drain (S/D) doping was then executed with phosphorus ion beam (P_{31}^{+}) at the energy of 25 keV and the dose of 1×10^{15} cm^{-2} (Fig. 4-6 (c)), and then the photo-resist patterns covering the S/D regions were generated by a standard lithographic step. The main splits in this study were accomplished by the following steps: For the side-gated (SG) devices, only an anisotropic dry etch was performed to remove poly-Si everywhere except the portions covered by the photo-resist or in the cavities which were shielded by the nitride hard-mask (Fig. 4-6 (d-1)). While for the ΩG split, additional wet etch steps were performed to remove the nitride hard-mask and then the dummy TEOS by hot H_3PO_4 and DHF, respectively (Fig. 4-6 (d-2)), while a portion of the bottom nitride was left intact to sustain the NW channels. Similar treatments were also applied to the gate-all-

around (GAA) devices, but the bottom nitride was further removed so that the NW channels are hanging between the S/D regions (Fig. 4-6 (d-3)). Then, all splits were combined to receive the deposition of an ONO (4.5 nm/8 nm/10 nm) stack by LPCVD, capped with a 150 nm n^+ poly-Si. The process temperature for ONO stack deposition is 700 ℃ for SiO_2 and 780 ℃ for Si_3N_4. The dopant activation of S/D implant was performed during the ONO LPCVD process. The poly-Si was sequentially patterned to serve as the gate electrode (Fig. 4-6 (e-1) to (e-3)). Standard metallization scheme was then performed to complete the device fabrication. For comparison purpose, planar devices with poly-Si channel of 50 nm and the same ONO condition were also fabricated.

Fig. 4-7 shows the cross-sectional transmission electron microscopic (TEM) pictures of three types of NW-SONOS devices. Note that the cross-sectional dimensions of all NWs are comparable. Owing to the additional wet etching steps, the shapes of ΩG (Fig. 4-7 (b)) and GAA (Fig. 4-7 (c)) NWs look more rounded than SG split. The channel width of SG devices is about 20 nm for each NW channel, as shown in Fig. 4-7 (a). For ΩG and GAA devices, the channel width is increased to 50 nm and 60 nm, respectively, due to the fact that extra NW edges are incorporated as the conductive channel. It is worth mentioning that the proposed fabrication method can easily integrate GAA poly-Si NW devices with planar poly-Si thin-film transistors (TFT) by adding only one lithography step for the dummy gate formation (as the schematic flow shown in Fig. 4-8).

4-3.2 Measurement Setup and Operation Principles

The electrical characterization of the fabricated devices was performed on the measurement system constructed by Agilent™ 8110A pulse generator, Agilent™

4156A semiconductor parameter analyzer, Agilent™ E5250A switch, probe station, and personal computer (PC) with the HP VEE program installed. The computer acted as the controller, and coordinated all the equipments via GPIB bus. A schematic configuration of the system setup is depicted in Fig. 4-9.

For P/E operation, due to the use of poly-Si NW channel, potential barriers caused by the defects presenting in or near the grain boundaries would hinder the acceleration of the electrons from source to drain, therefore CHEI method may not be appropriate for programming operation of poly-Si NW-SONOS devices. Accordingly, in this study we employ FN tunneling mechanism for all P/E operations of the fabricated NW-SONOS devices. During the programming operations, source and drain are both grounded, and a highly positive voltage is applied to the control gate to produce a strong electric field, and a number of electrons in the channel may tunnel through the thin oxide layer and be trapped by the trapping centers in the nitride layer. In erasing operation, both source and drain are also grounded, and a highly negative voltage is applied to the control gate to detrap stored electrons and attract holes to inject into nitride trapping layer. Note that the V_{TH} of device is defined as V_G @ I_D = W/L × 5nA for simplicity.

4-4 Basic Electrical Characteristics of Poly-Si NW-SONOS Devices

Fig. 4-10 shows typical transfer characteristics of the three types of NW-SONOS devices as well as the planar counterpart. In the figure all measured devices have channel length of 0.4 μm and equivalent gate oxide thickness of around 20 nm.

It can be noticed that GAA device manifests the highest normalized ON-current and the smallest SS (~150 mV/dec). Drain-induced-barrier-lowering (DIBL) phenomenon is also negligible for both GAA and ΩG devices, while the planar one apparently has serious DIBL effect. These observations of device fundamental characteristics are expected since GAA device has its NW channels surrounded by the gate, ensuring great gate controllability and suppressing effective defect density per unit gated area. Though SG device has only one of the NW surfaces under gate modulation, resulting in the worst device performance among the three types of NW-SONOS devices, however, it still outperform the planar device in terms of better normalized ON-current, SS and DIBL.

The above comparison unambiguously demonstrates the benefit of using GAA scheme to improve the device characteristics, even though it needs extra etch steps to complete the structure as mentioned in previous section. Another issue associated with GAA devices is the failure of device characteristics as the channel is long. Specifically, it is found that the drain current of GAA devices becomes too low to be measured as the channel length is longer than 2 μm, implying that the NW channels have been broken. Such phenomenon, however, does not take place in SG and ΩG splits. Considering the difference in process steps and the resulted structure (see Fig. 4-6 (d)), the failure of long-channel GAA devices could be attributed to the collapse and breaking of the long NWs when they were released and became suspended after removing the underlying nitride.

4-5 Programming/Erasing Characteristics

Fig. 4-11 presents the P/E speed characteristics of a SG NW-SONOS device with V_G ranging from 10 V to 13 V. The characteristics of a planar TFT-SONOS counterpart with gate bias of 15 V are also shown in Fig. 4-11 (a). The experimental results clearly show that the SG NW-SONOS device has faster programming efficiency than its planar counterpart. This could be partly attributed to the use of ultra-thin NW channel which could significantly reduce the impact of the defects presenting in the channel and promote the programming current (see Fig. 4-10). Furthermore, due to the much more scaled channel width (W = 20 nm) as compared with planar one (W = 5 μm), fringing-field enhancement at the channel edge is more pronounced in SG NW device, further benefiting the programming speed [4.21]. The erasing characteristics are shown in Fig. 4-11 (b), in which the data of planar devices are not included since only negligible shift in V_{TH} was detected even as a V_G of -15 V was applied. As can be seen in the figure, the erasing characteristics show weak dependence on the applied V_G for SG devices. Such observation might be related to the non-uniform trapping events happening in this type of devices and will be addressed later.

Fig. 4-12 and Fig. 4-13 depict the P/E speed characteristics of ΩG and GAA NW-SONOS devices, respectively, with various V_G. Compared with SG device, the P/E efficiency of ΩG and GAA devices is remarkably improved. Moreover, from the comparison of P/E speed shown in Fig. 4-14, GAA device apparently exhibits the fastest P/E speed among the three types of devices, indicating that the gate controllability has great impact on NW memory characteristics. The much improved P/E efficiency with GAA and ΩG NW structures is believed to correlate with the increase in curvature of the NW channels as well as the MG configuration. Previous

works on investigating the performance of MOSFETs and SONOS with NW channel [4.14, 4.22] have shown that the electric field in the gate oxide during operation is position- and curvature-dependent, and favors the P/E operation for NW with a round-shaped NW. For example, during programming operation, the electric field in the tunnel oxide is enhanced when the curvature of the channel surface increases [4.14]. Such argument also applies to the present study. Fig. 4-15 depicts the simulated electric field distribution [4.23] based on the cross-sectional shapes of the fabricated SG and GAA devices extracted from the TEM analysis presented in Figs. 4-7 (a) and (c). In the figures, for simplicity, a SiO_2 is used as the gate dielectric instead of ONO. The strength of electric field in the oxide along the paths indicated by the arrows in the inset 2D profiles is shown and compared for the two cases with a programming voltage of 10 V. It can be observed that the magnitude of electric field strength near the NW surface of GAA structure is 60% larger than that of SG structure due to the geometry of rounded structure. This is consistent with the analysis of previous work [4.14] and thus reasonably in agreement with the result of faster P/E operations with GAA configuration.

Another factor affecting device operation is the uniformity of electric-field strength during operation. This is related to the curvature and thus the shape of the NW channel. Unlike the single-crystal Si NW, it is hard to form poly-Si NWs with their cross-sectional shape of symmetrical circle. The curvature, and thus the electric field strength, may vary from place to place at the NW surface. The non-uniform electric field may result in non-uniform charge trapping and de-trapping during P/E operations [4.24, 4.25]. For SG devices, the appearance of top and bottom corners would further worsen the situation. The simulated magnitude of electric-field strength along the channel-width direction (Y-direction) for SG device at two positions in the

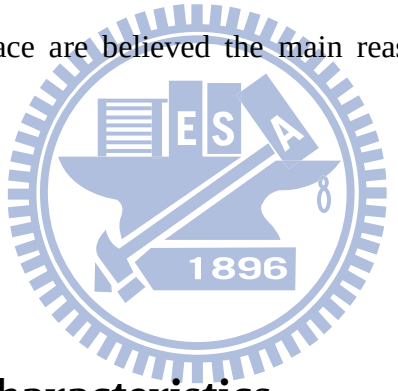
gate oxide (X = X1 and X2) are shown in Fig. 4-16. In this case a gate bias of -10V is applied. Apparently, the electric field is position-dependent and has maximums at the locations where corners exist. Such electric field distribution may provoke non-uniform gate current density across the channel surface [4.25], and therefore leads to inefficient P/E operation, as shown in Fig. 4-11. It should be noted that, for simplicity, the simulation analysis depicted in Fig. 4-15 and Fig. 4-16 are done with the assumption that the Si channel is mono-crystalline. The existence of grain boundaries in the poly-Si channel may more or less affect the practical device operation. However, we expect the influence should not be significant because of the tiny volume of the poly-Si layer in which very limited amount of defects is contained [4.6, 4.11].

In contrast, for GAA and ΩG NW devices, the average curvature at channel surface is increased while its value is relatively uniform throughout the NW channel as compared with SG case. This results in improved P/E efficiency, especially for GAA samples. It should be noticed that the erasing speed of GAA device slows down when erasing time is sufficiently long (*e.g.*, 0.1 ms with gate bias of -12 V), as shown in Fig. 4-13 (b). Moreover, the saturation (absolute) value of V_{TH} shift is the smallest for gate bias of -12 V among all bias splits. This is caused by the preponderant electron injection from the n^+ poly-Si gate, giving rise to a limited saturation level of V_{TH}. Replacing n^+ poly-Si gate with higher work-function material such as p^+ poly-Si or TaN [4.26] would be helpful to relieve this problem on account of the effectively increased energy barrier height to impede electron injection from the gate.

Transfer curves of the three types of NW-SONOS devices at fresh state and specific P/E states are shown in Fig. 4-17. A memory window of 1.2 V can be obtained for SG device with programming gate voltage V_{GP} = 13 V and erasing gate voltage V_{GE} = -9 V, with duration of 100 μs and 500 ms, respectively (Fig. 4-17 (a)).

Since ΩG device depicts higher P/E speed, increased memory window of 2 V can be achieved for ΩG device by applying V_{GP} = 13 V and V_{GE} = -10 V with smaller duration of 10 μs and 100 ms, respectively (Fig. 4-17 (b)). For GAA device, memory windows of 2.3 V, 3 V and 3.6 V can be obtained by applying V_{GP} = 11 V, 13 V and 15 V with the same duration of 10 μs, respectively (Fig. 4-17 (c)). Finally, the duration of erasing operation can be reduced to 10 ms with V_{GE} = -10 V for erasing the programmed GAA device back to the fresh V_{TH} level.

The above results clearly demonstrate the device with GAA configuration has the largest memory window and the fastest P/E speed among the three types of NW-SONOS devices. Higher average value and better uniformity of electric field at the rounded NW channel surface are believed the main reasons for the superiority of GAA devices.



4-6 Reliability Characteristics

4-6.1 Endurance Characteristics

Figs. 4-18 (a), (b) and (c) show the endurance characteristics of SG, ΩG and GAA NW-SONOS devices, respectively. The bias conditions of P/E operation are 13V(100μs)/-9V(500ms) for SG, 13V(10μs)/-10V(100ms) for ΩG, and 11V(10μs)/-9V(10ms) for GAA. Again, GAA device shows the best performance among the test samples in term of the smallest closure in memory window after 10k P/E stressing cycles (~ 0.2 V). For SG device, it can be seen that the V_{TH} values for both programmed and erased states decrease slightly after 10k P/E cycles. An opposite

trend is observed for ΩG and GAA cases—the V_{TH} values for both programmed and erased states increase with increasing cycles. Furthermore, the increasing rate becomes larger as cycle number is larger than 1k.

To gain more insight into these phenomena, the I_D-V_G characteristics of SG device for various P/E cycles (1, 1k, and 10k) are shown and compared in Fig. 4-19 (a). It is clear that the SS becomes worse with increasing cycles. The primary reason for the SS degradation in SG device could be ascribed to the non-uniform field strength during P/E operations mentioned above (see Fig. 4-16), which tends to incur non-uniform stored charges after several cycles of P/E operation. This is evidenced by the transconductance (GM) versus V_G curves extracted at erased state shown in Fig. 4-19 (b). In the figure, we can notice a plateau region appearing in V_G ranging from 2.8 V to 3.2 V after 1k and 10k cycles (the arrows shown in the figure are used to elucidate the trend), suggesting that the V_{TH} along the channel width direction is location dependent and hence supports the aforementioned inference. Accordingly, due to the long stress time of erasing operation, the corner region of SG NW should be erased into a lower V_{TH} level as compared with the flat region, resulting in the presence of tails in subthreshold region of the erased I_D-V_G curves (Fig. 4-19 (a)). Owing to the use of constant current method for determining V_{TH} in this study (see Section 4-4.2), the opposite trend of V_{TH} in endurance test for SG split (Fig. 4-18 (a)) simply stems from the tail part of the I_D-V_G characteristics.

Figs. 4-20 (a) and (b) depict the transfer characteristics during endurance tests for ΩG and GAA devices, respectively. From the figures, the I_D-V_G curves after 1k cycles appear to be parallel to that of fresh condition, indicating excessive electron storage is mainly responsible for the V_{TH} shift. Besides, the I_D-V_G curves after 10k cycles show noticeable increase in SS, representing that there exists one additional

factor accountable for the V_{TH} increase in the programmed states. Such degradation could be attributed to the generation of extra interface states at or near tunnel oxide/channel interface generated by the high-voltage stress during P/E operation. Because of the much lower P/E voltages used as compared with the planar devices (see Fig. 4-11 (a)), degradation of oxide/channel interface is not considerable until the cycle number reaches beyond 1k. Nevertheless, the GM versus V_G plot of ΩG device shown in Fig. 4-21 (a) reveals the reducing GM slope with increasing P/E cycles, implying ΩG device also suffers from the non-uniform charge injection effect which can lead to non-uniform channel conductance. This is due to the fact that the NW channel is not fully wrapped by ΩG, and the edges of ΩG are close to the NW channel (as can be seen in Fig. 4-7 (b)). In contrast to ΩG device, the GM-V_G characteristics of GAA device show only parallel shift and small amount of decay in maximum GM, signifying that GAA device has the most uniform stored-charge distribution. On the other hand, the deterioration of blocking oxide caused by stress cycles could result in more serious gate injection effect during erasing operation, giving rise to an increasing V_{TH} of erased state and thus memory window closure.

The SS versus P/E cycle numbers for the three types of NW-SONOS devices are shown and compared in Fig. 4-22. As mentioned above, because of the severe non-uniformity in trapped charge distribution originating from large variation in surface curvature of the channel, SG split exhibits conspicuous rising behavior in the beginning of P/E-cycle stress test. Such circumstance is substantially improved with ΩG and GAA devices, especially for the latter which shows the least SS degradation. Actually the SS of ΩG and GAA devices still slightly increase in the first 10k P/E cycles due to the inevitable non-uniform charge injection effect, although far less prominent as compared with SG case. Nonetheless, since sharper SS of ΩG (SS ~ 200

mV/dec) and GAA (SS ~ 150 mV/dec) devices at fresh condition represents less defect density per unit gated area, the degradation of tunneling oxide and increased interface states due to P/E-cycle stress may lead to more distinct impacts on SS as well as V_{TH} of ΩG and GAA devices than those of SG device. Therefore, the SS of ΩG and GAA devices appear to degrade drastically after 10k cycles as sufficient additional interface traps have been generated.

4-6.2 Retention Characteristics

Retention characteristics of SG, ΩG and GAA NW-SONOS devices after single and 10k P/E cycles at room temperature (25 ℃) are shown in Figs. 4-23 (a), (b), and (c), respectively. The P/E bias conditions in the retention test are identical to those in the endurance test. Among the three types of NW devices, GAA split retains the largest memory windows of about 1.7 V and 1 V, respectively, after 10 years for the devices after single and 10k P/E cycles of operation. The major reason for the shrinkage in window size is the lowering in V_{TH} of the programmed state. Since the V_{TH} decay rate in the programmed state for 10k P/E-stressed device shows similar trend compared with that for the singly-stressed device at room temperature, the trap-to-band tunneling is considered to be the major charge loss mechanisms in the excess electron state (programmed state) rather than trap-to-trap tunneling [4.19]. On the other hand, the V_{TH} of the erased state for the device after 10k P/E cycles shows larger positive shift with time than that of the device after single cycle of P/E operation. This is attributed to the de-trapping of trapped holes in the tunneling oxide near the channel surface resulted during the P/E operations [4.27].

Fig. 4-24 shows the retention behaviors of GAA devices at 85 ℃. The V_{TH} decay rate in the programmed state is observed to be greater than that at room

temperature, leading to a reduced memory window for the 10-year projection. This indicates the emission of trapped electrons from the storage nitride is accelerated by the thermal-activated process [4.28]. Since the energy level of the hole traps is relatively deep in the nitride and the de-trapping of holes contained in the tunneling oxide is mainly via tunneling mechanism [4.28], the V_{TH} shift rate of the erased state should be insensitive to the temperature for both singly and 10k P/E-stressed devices, as shown in Figs. 4-23 (c) and 4-24.

4-7 Summary

In this chapter, we have investigated the characteristics of poly-Si NW-SONOS devices with various gate configurations fabricated with an ingenious scheme. As compared with the planar counterpart, the NW devices can be operated with a much reduced P/E voltage which is essential for the demand of green electronics. This is attributed to the enhanced gate controllability with MG configuration as well as the use of ultra-thin NW structure with a reduced amount of defects in the channel. Among the three types of NW devices, GAA split shows the best performance in terms of the highest ON-current, the steepest SS, the highest P/E efficiency, the largest memory window, as well as the best endurance and retention characteristics. This is ascribed to the increase in the electric field strength at the NW/tunneling oxide interface resulting from the large curvature as well as the reduced variation in the curvature value. Hence GAA device possesses the most prominent performance among the different types of devices characterized in the study.

More importantly, the NW-SONOS fabrication process used in this study can be

easily implemented in modern flat-panel manufacturing without resorting to costly advanced lithography. Based on the results obtained in this chapter, the proposed method for fabricating MG poly-Si NW-SONOS devices appears to be very promising for the realization of SOP in the future.

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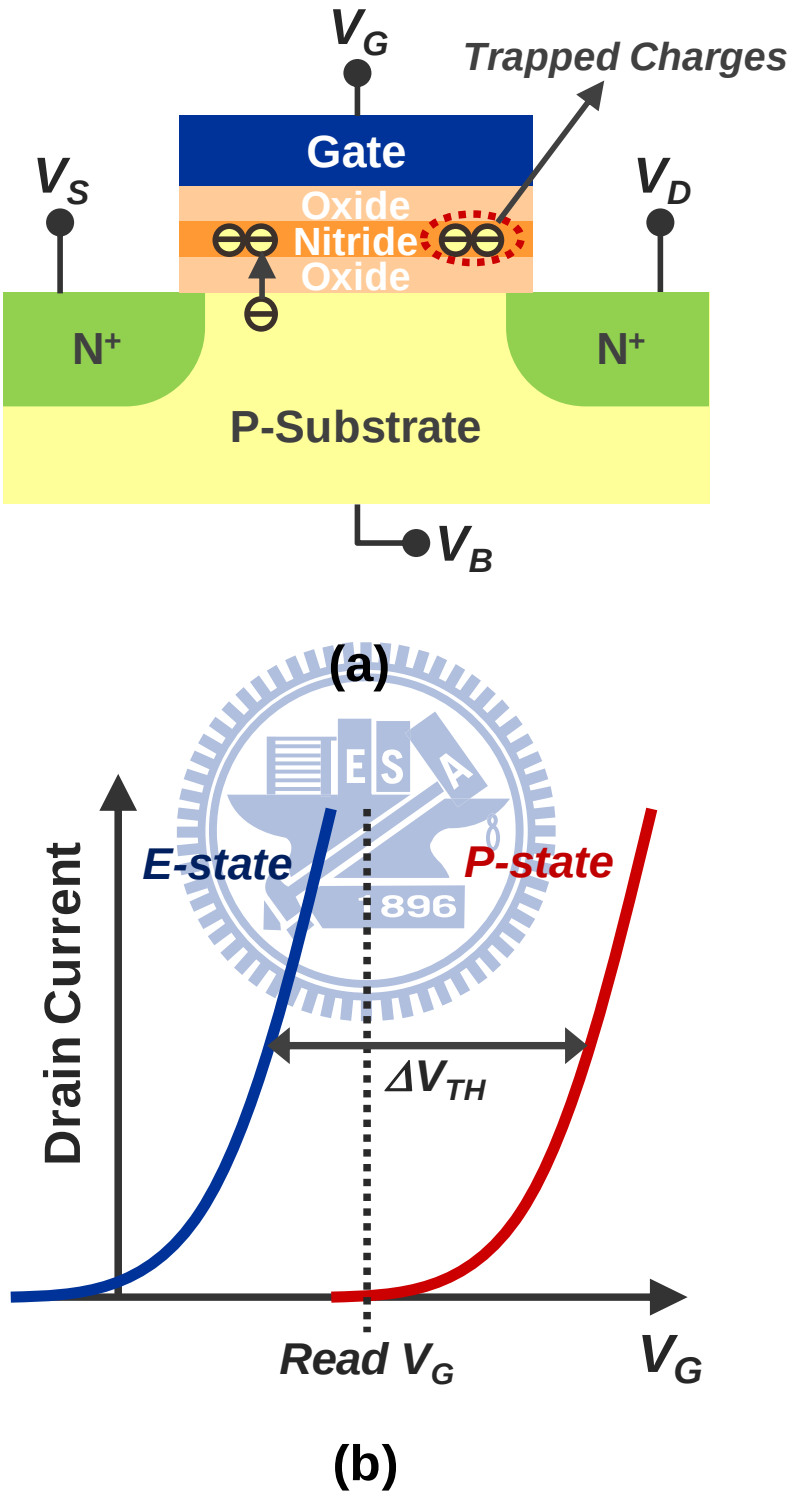


Fig. 4-1 (a) Schematic structure of a conventional n-type SONOS memory device. (b) Influence of trapped charges on V_{TH} of the SONOS memory device.

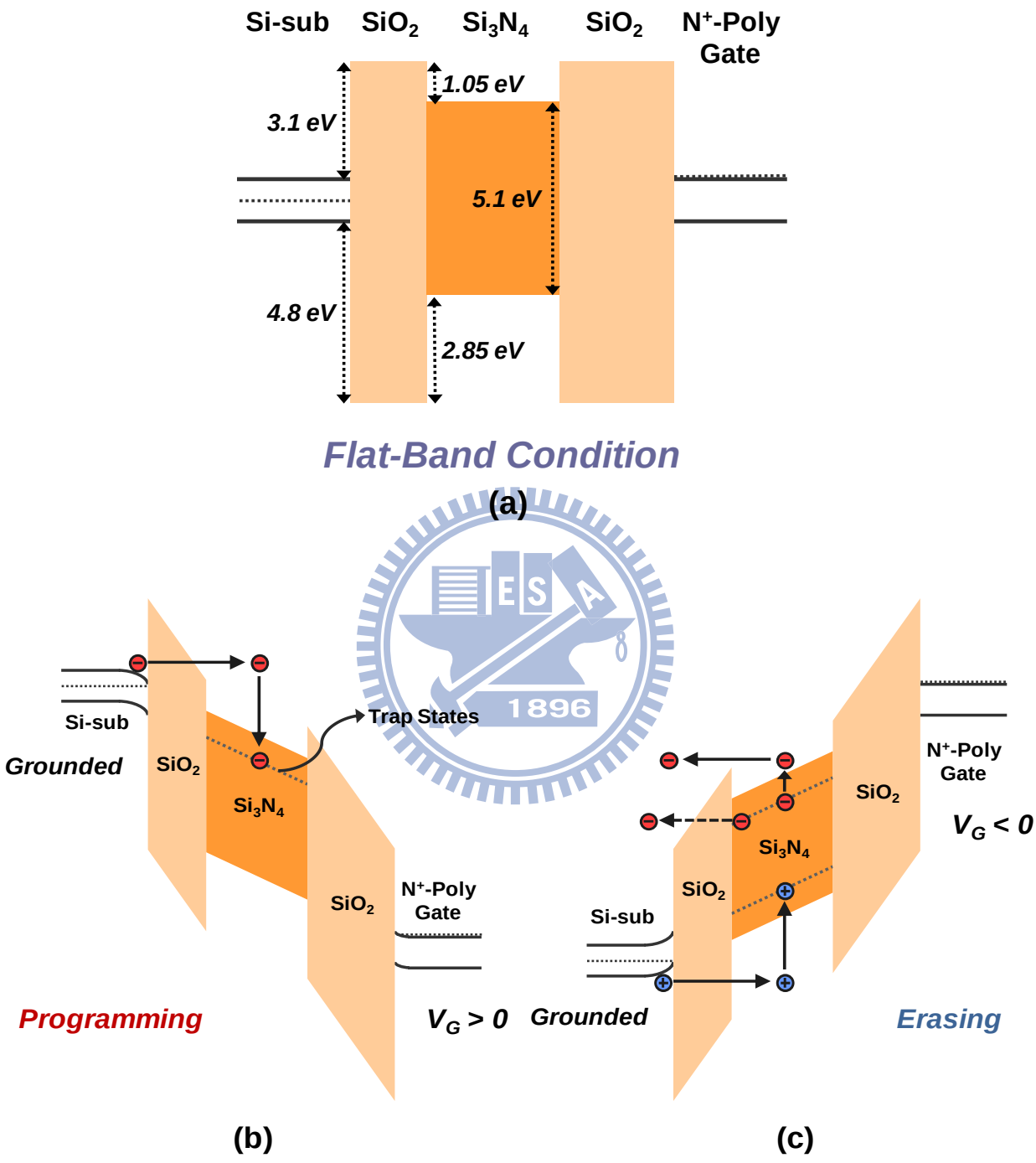


Fig. 4-2 Energy band diagrams of SONOS structures in (a) flat-band, (b) positive gate bias (programming), and (c) negative bias (erasing) conditions.

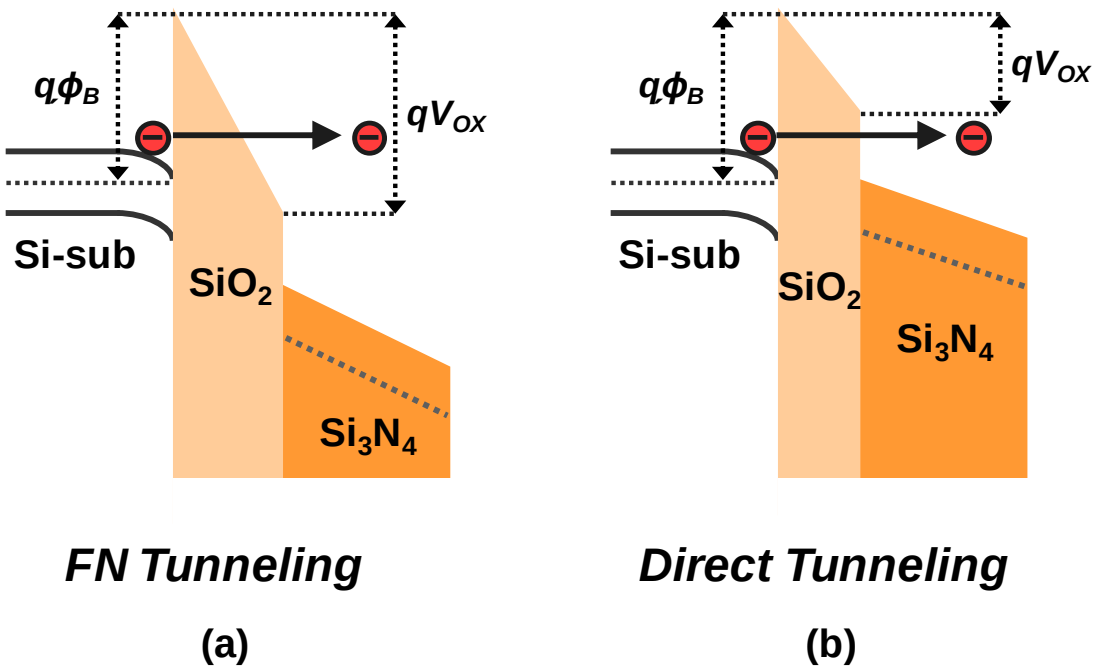


Fig. 4-3 Energy band diagrams illustrating the injection of electrons from Si substrate to nitride via (a) FN tunneling and (b) direct tunneling.

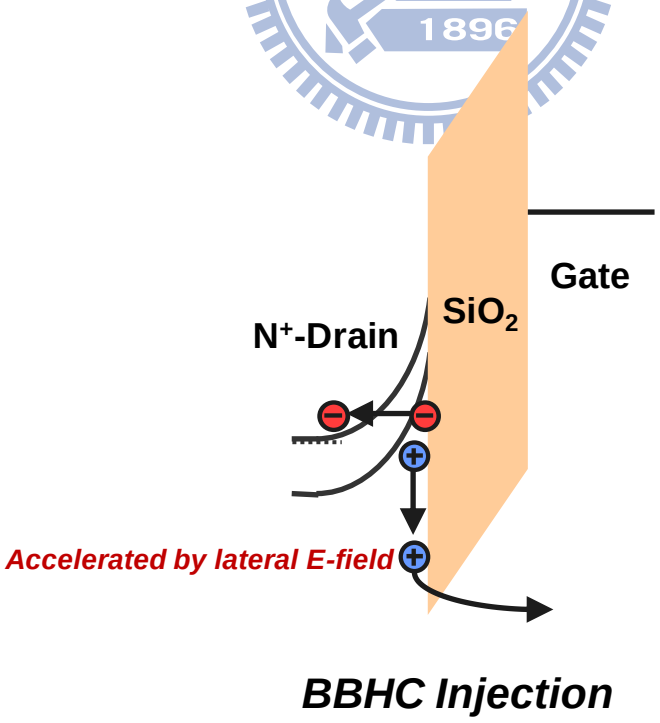


Fig. 4-4 Energy band diagram of BBHC injection at the drain side of an nMOSFET.

$$n_t(\phi_t, t) = n_t(\phi_t, 0) \bullet e^{-t/\tau}$$

Frenkel-Poole Emission

$$\tau_{FP} = \tau_0 \exp\{[\phi_N - q(qE/\pi\varepsilon)^{1/2}]/kT\}$$

Tunneling Mechanism

$$\tau_T = \tau_0 \cdot \exp(\alpha_{ox} \cdot t_{ox}) \cdot \exp(\alpha_N \cdot t_N)$$

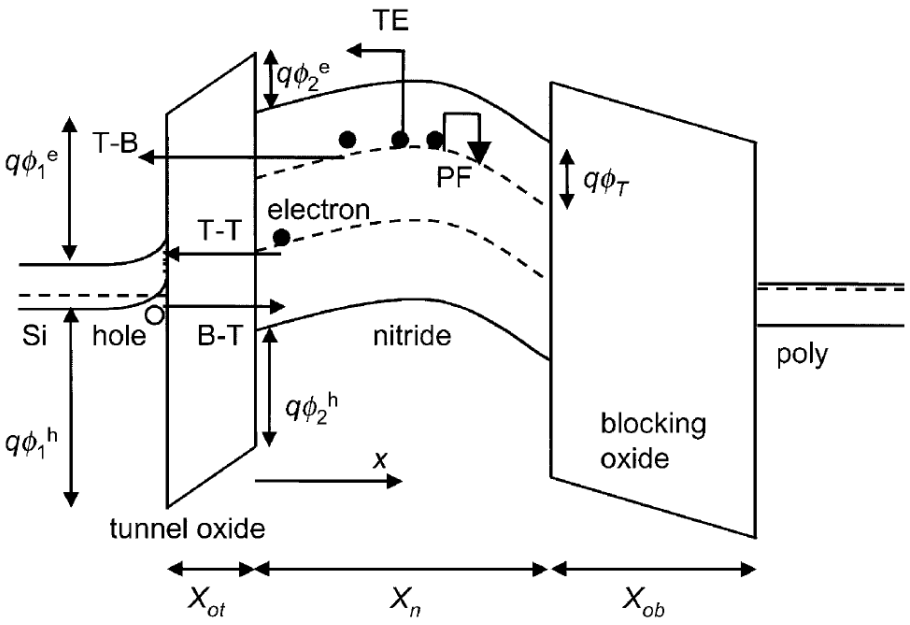


Fig. 4-5 Band diagram showing the charge loss paths in SONOS: thermal excitation (TE), Frenkel-Poole emission (FP), trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), and band-to-trap tunneling [4.19].

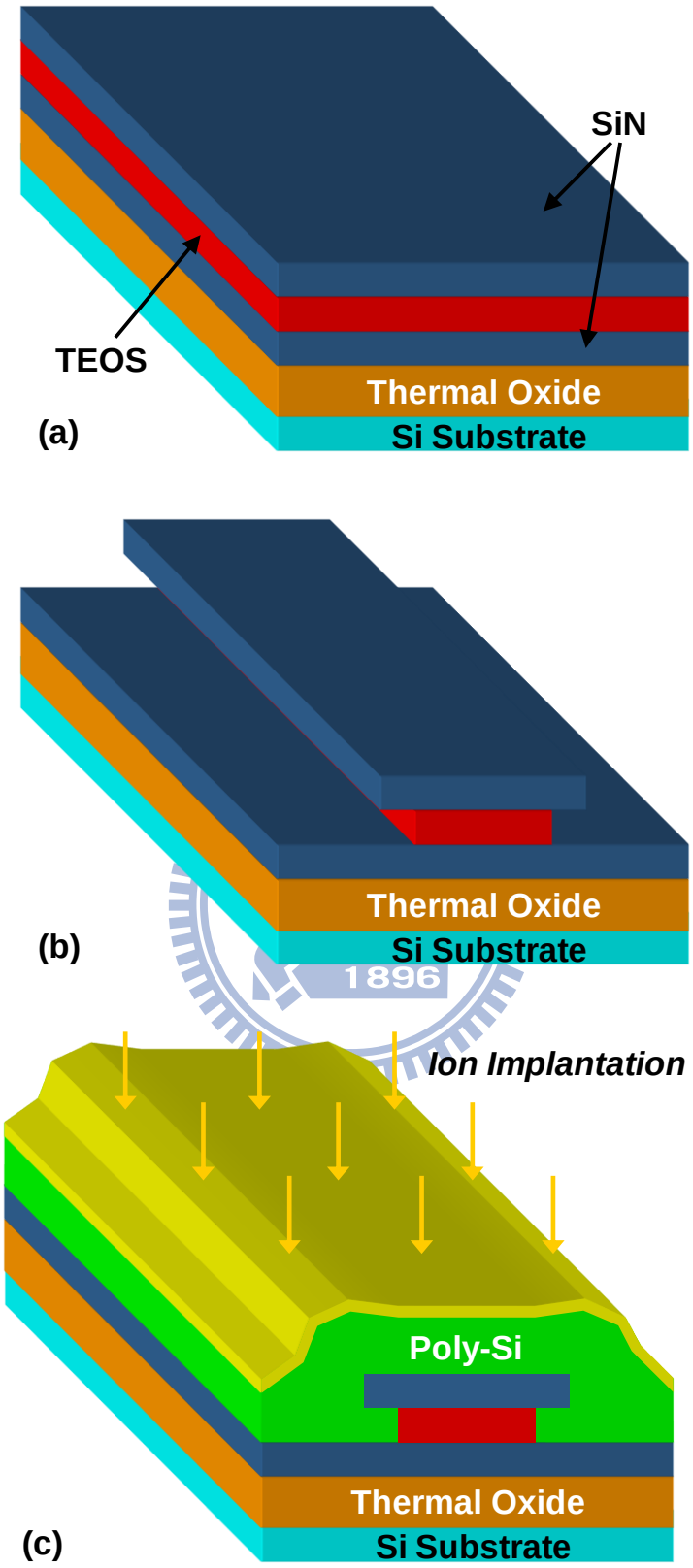


Fig. 4-6 (a) Deposition of nitride/TEOS oxide/nitride dummy layers on a Si substrate with BOX. (b) Patterning a dummy structure by anisotropic etching and formation of cavities by wet etching of the TEOS oxide. (c) a-Si deposition and annealing for crystallization, and S/D implant.

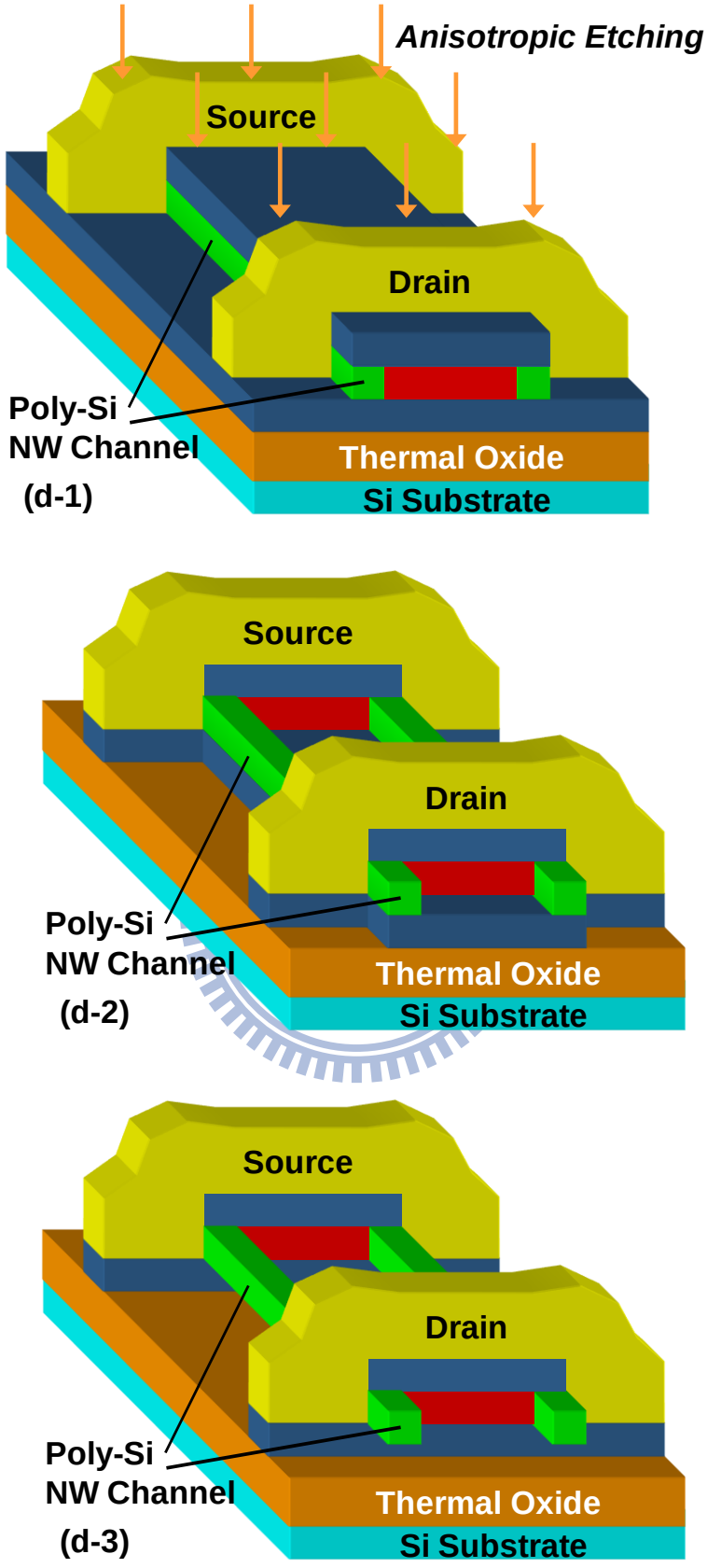


Fig. 4-6 (d-1) Definition and formation of S/D and NW channel by anisotropic etching. (d-2) Nitride and TEOS oxide removal with hot H_3PO_4 and DHF, respectively. (d-3) Bottom nitride removal by hot H_3PO_4.

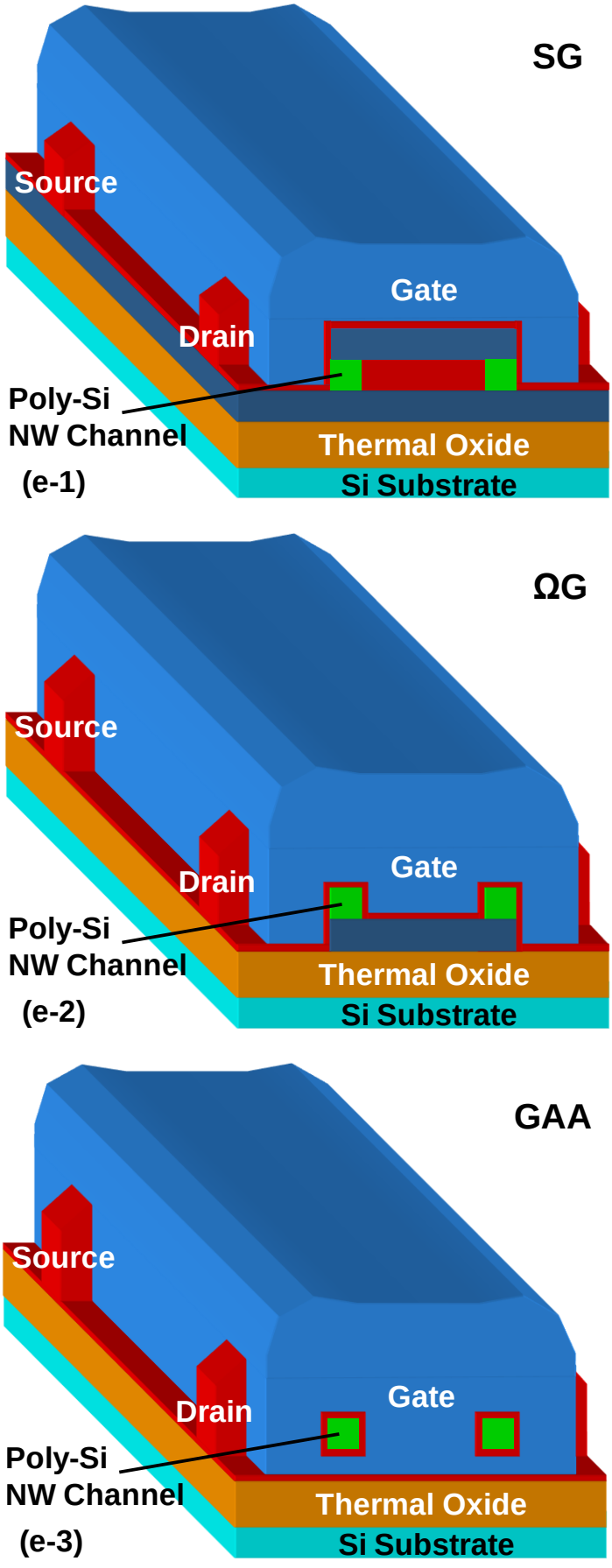


Fig. 4-6 (e-1 to e-3) Deposition of ONO stack and formation of poly gate for three types of NW-SONOS devices (SG, ΩG and GAA).

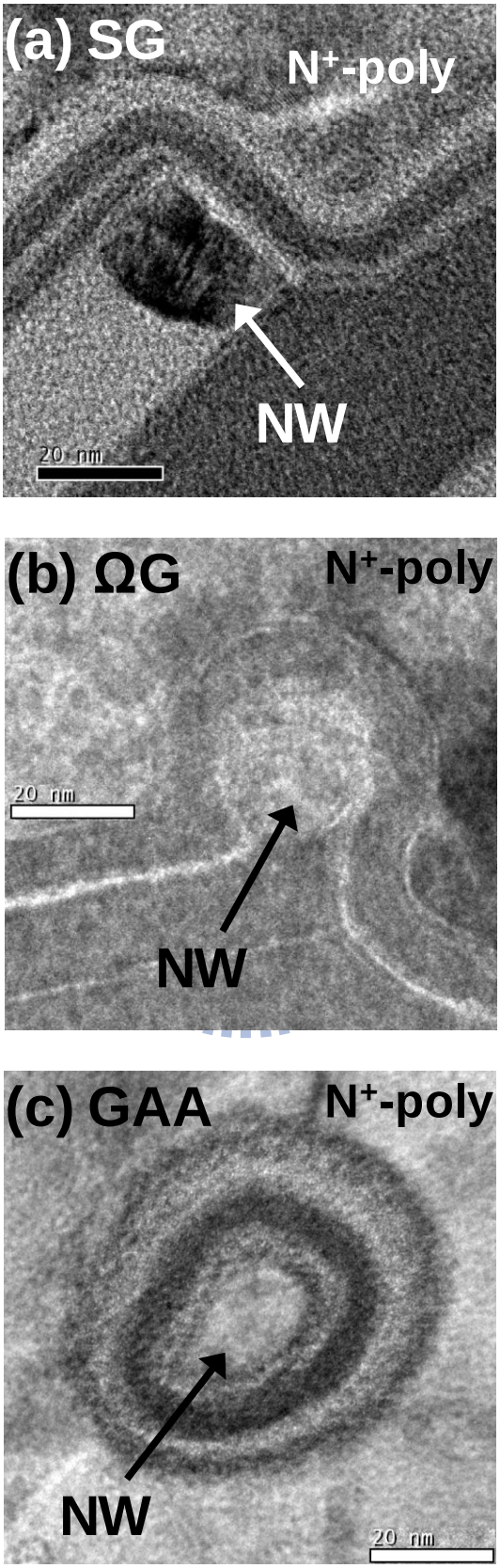


Fig. 4-7 Cross-sectional TEM images of the fabricated devices with (a) SG, (B) ΩG, and (c) GAA configurations.

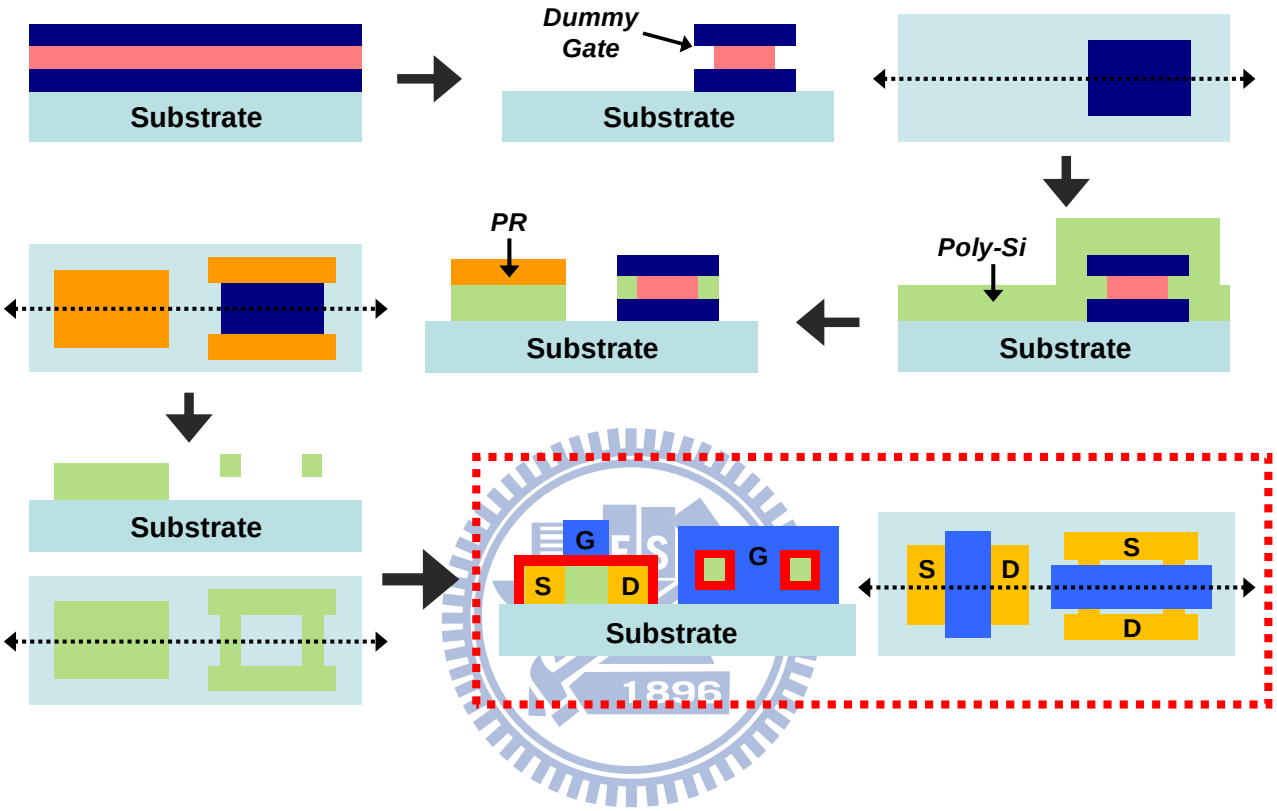


Fig. 4-8 Schematic process flow for the simultaneous fabrication of the planar and NW SONOS devices.

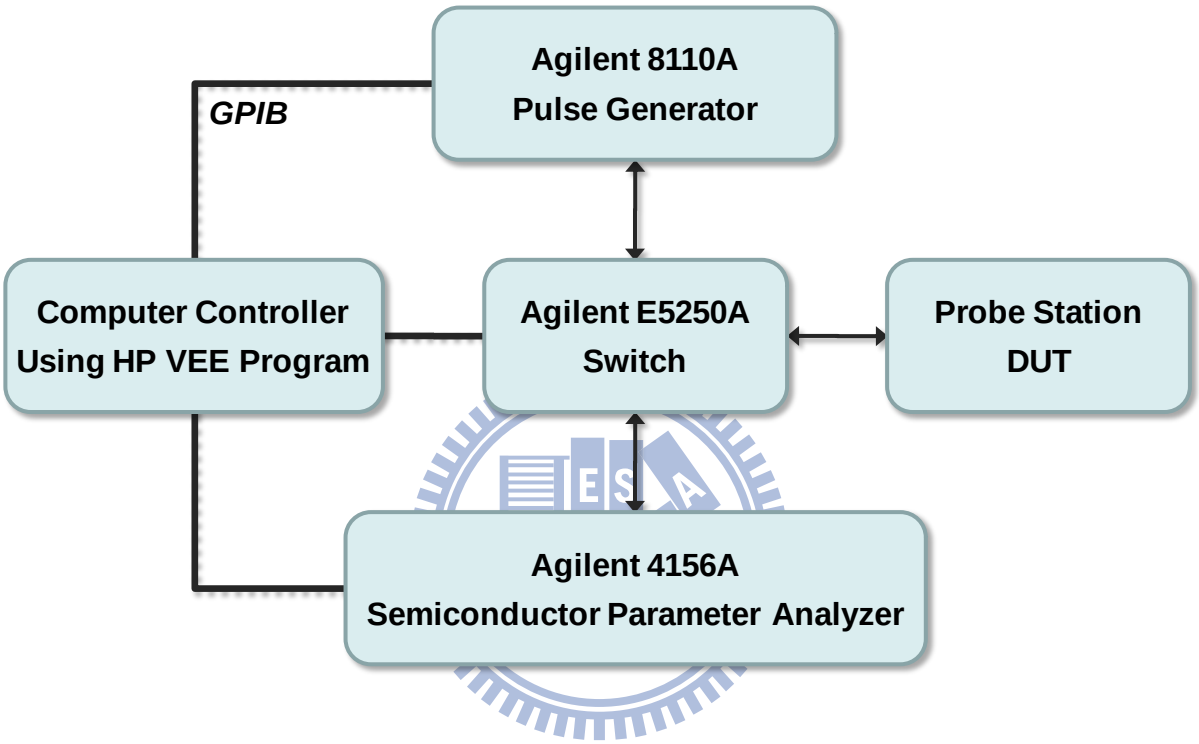


Fig. 4-9 Schematic illustration of measurement setup.

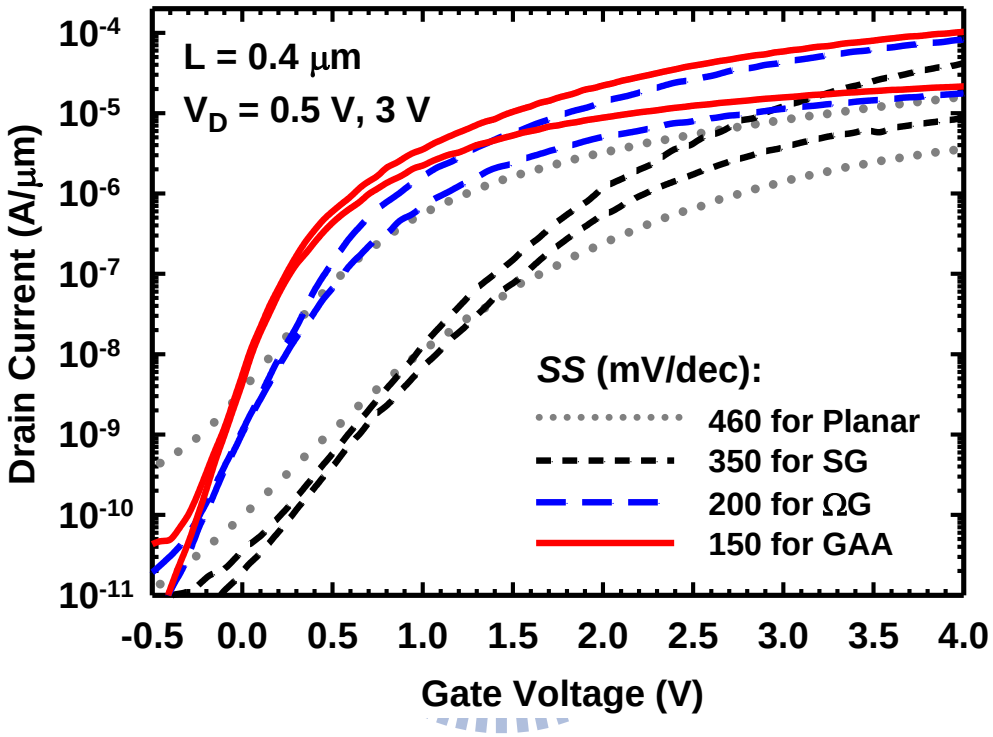


Fig. 4-10 Comparisons of transfer characteristics of the three types of poly-Si NW-SONOS and planar TFT-SONOS devices.

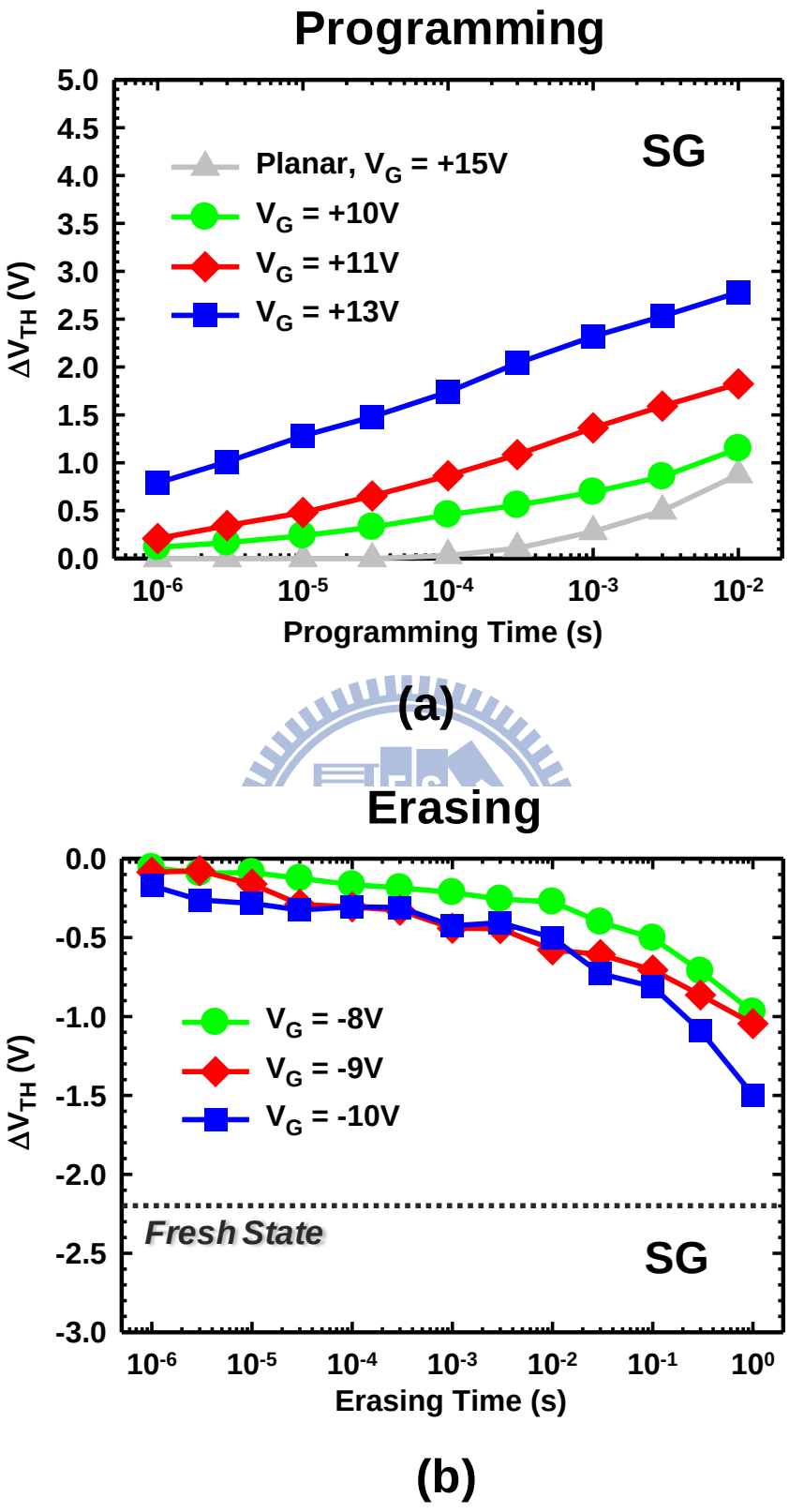


Fig. 4-11 (a) Programming and (b) erasing characteristics of the SG devices.

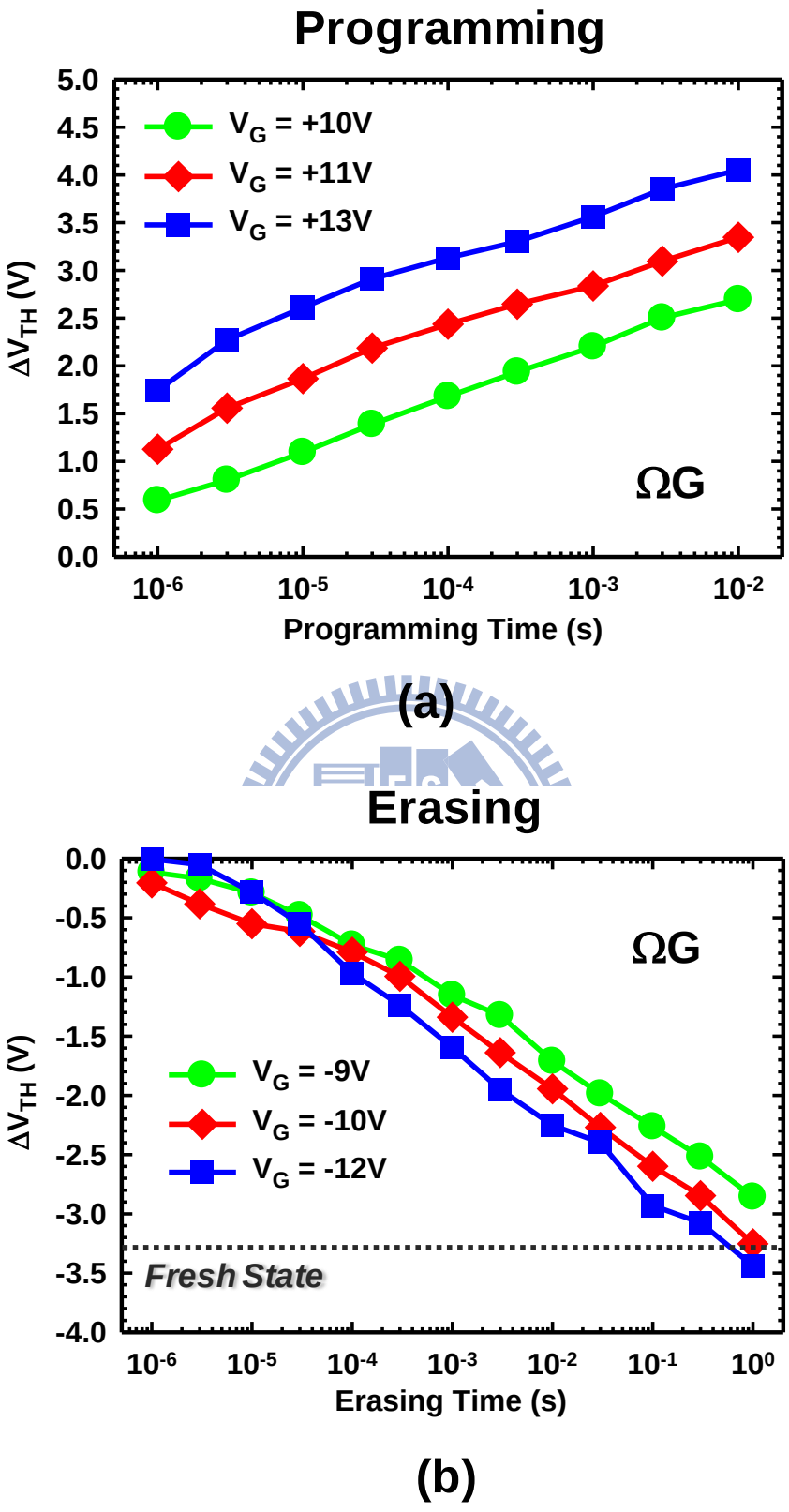


Fig. 4-12 (a) Programming and (b) erasing characteristics of the ΩG devices.

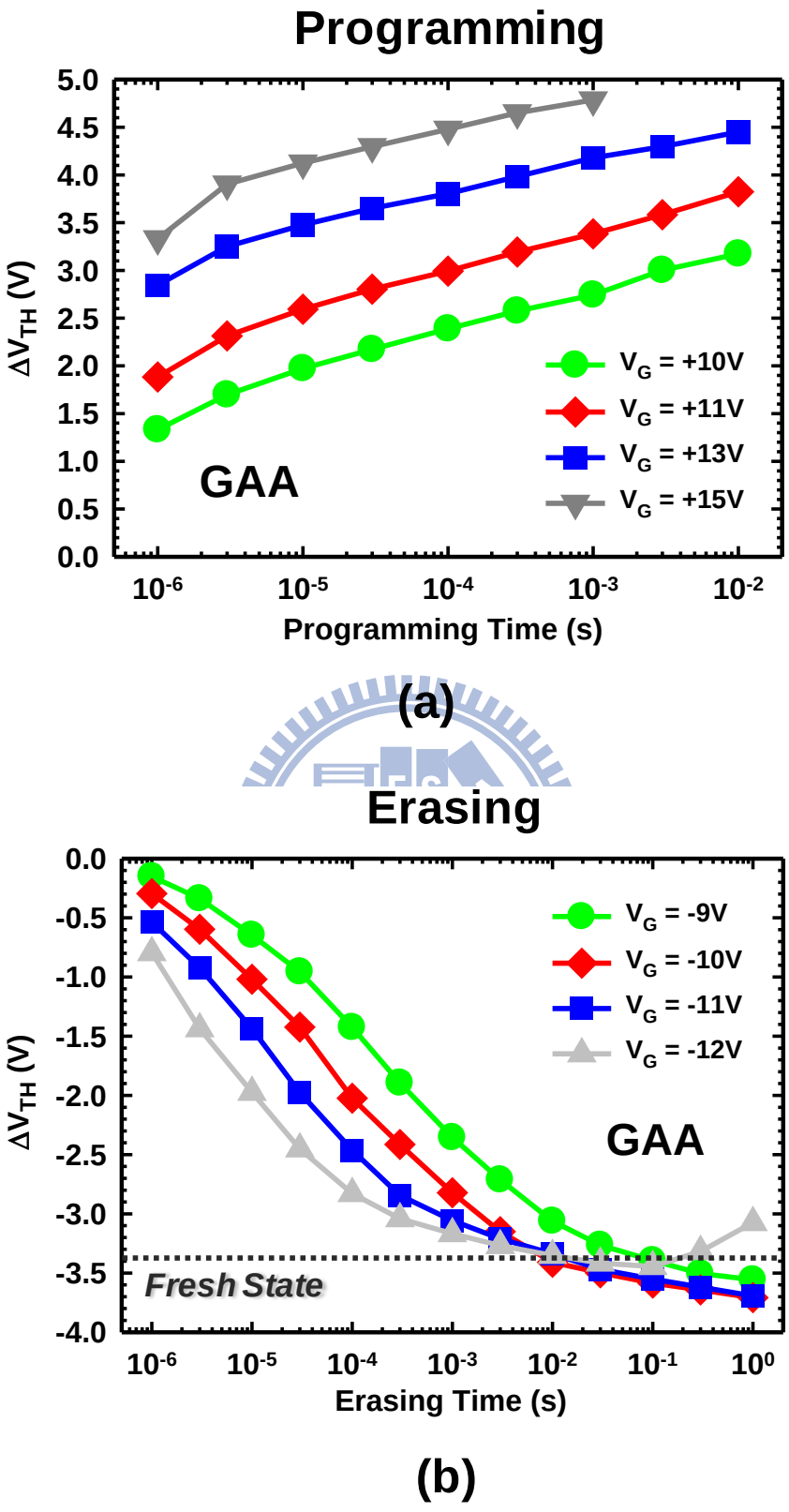


Fig. 4-13 (a) Programming and (b) erasing characteristics of the GAA devices.

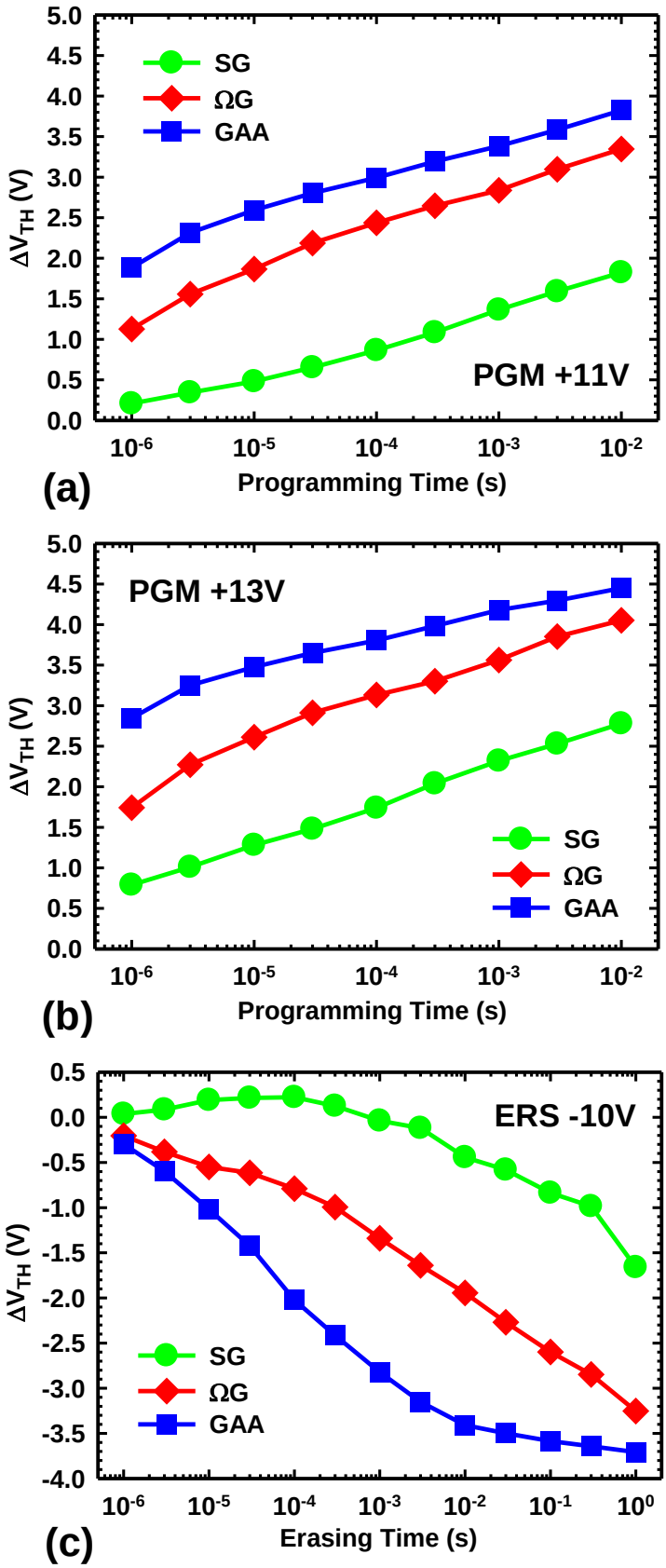


Fig. 4-14 Comparisons of P/E speed for three types of poly-Si NW-SONOS devices with (a) V_G = 11 V, (b) V_G = 13 V and (c) V_G = -10 V.

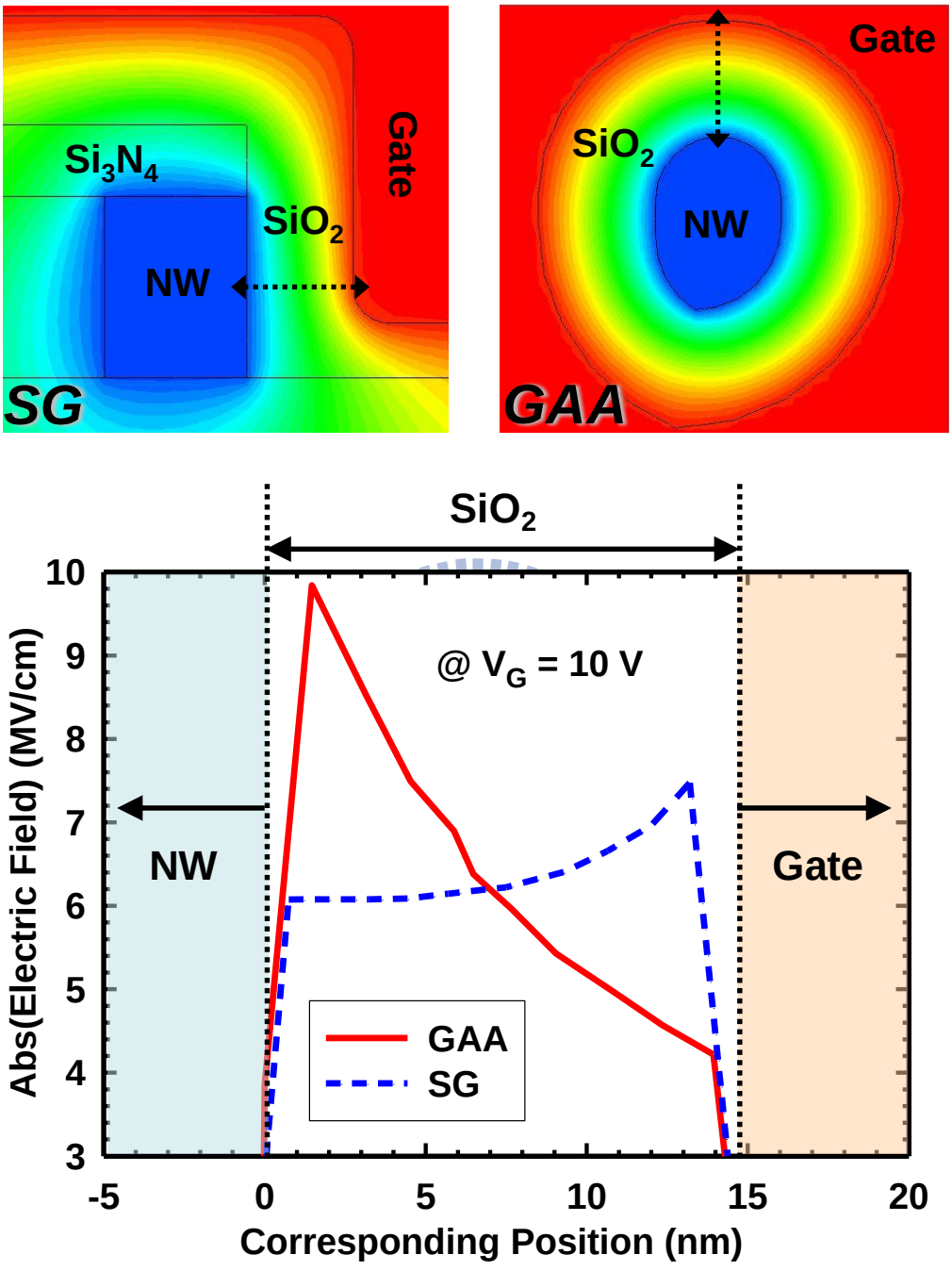


Fig. 4-15 Simulated electric field distribution (left) along the paths indicated by the arrows shown in the 2-D simulation profiles (right) of SG and GAA devices.

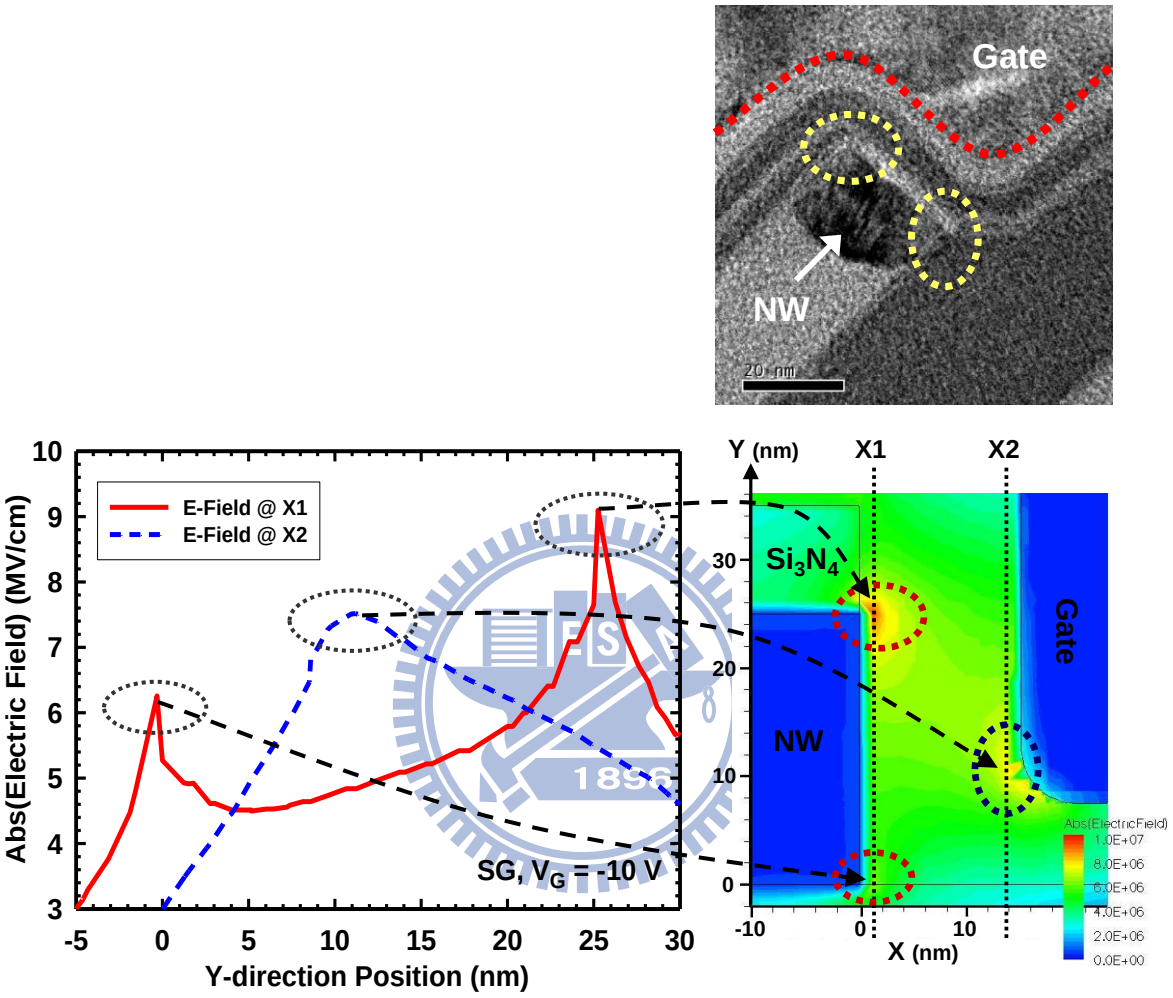


Fig. 4-16 Simulated electric field along channel-width direction (Y-direction) in the oxide at two locations, X1 (near channel surface, solid line) and X2 (near gate, dot line), for a SG device.

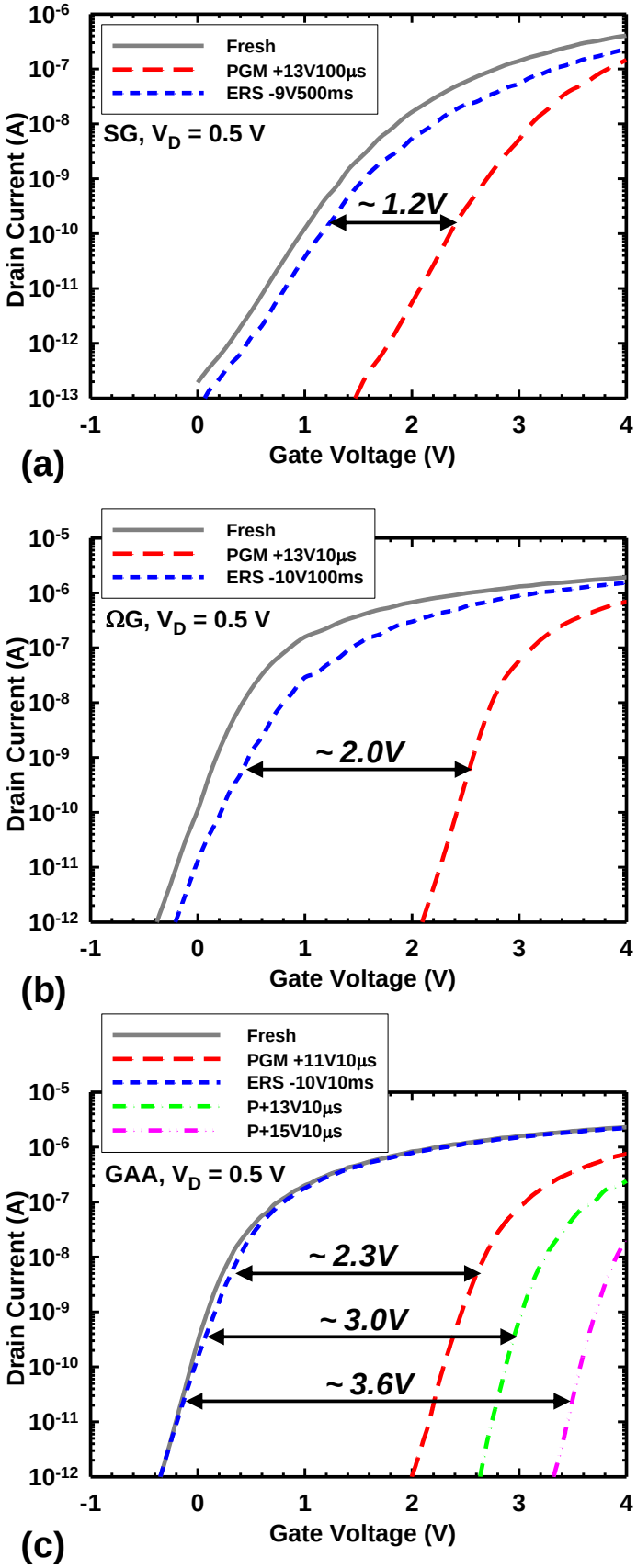


Fig. 4-17 Fresh, programmed, and erased subthreshold characteristics of (a) SG, (b) ΩG, and (c) GAA devices.

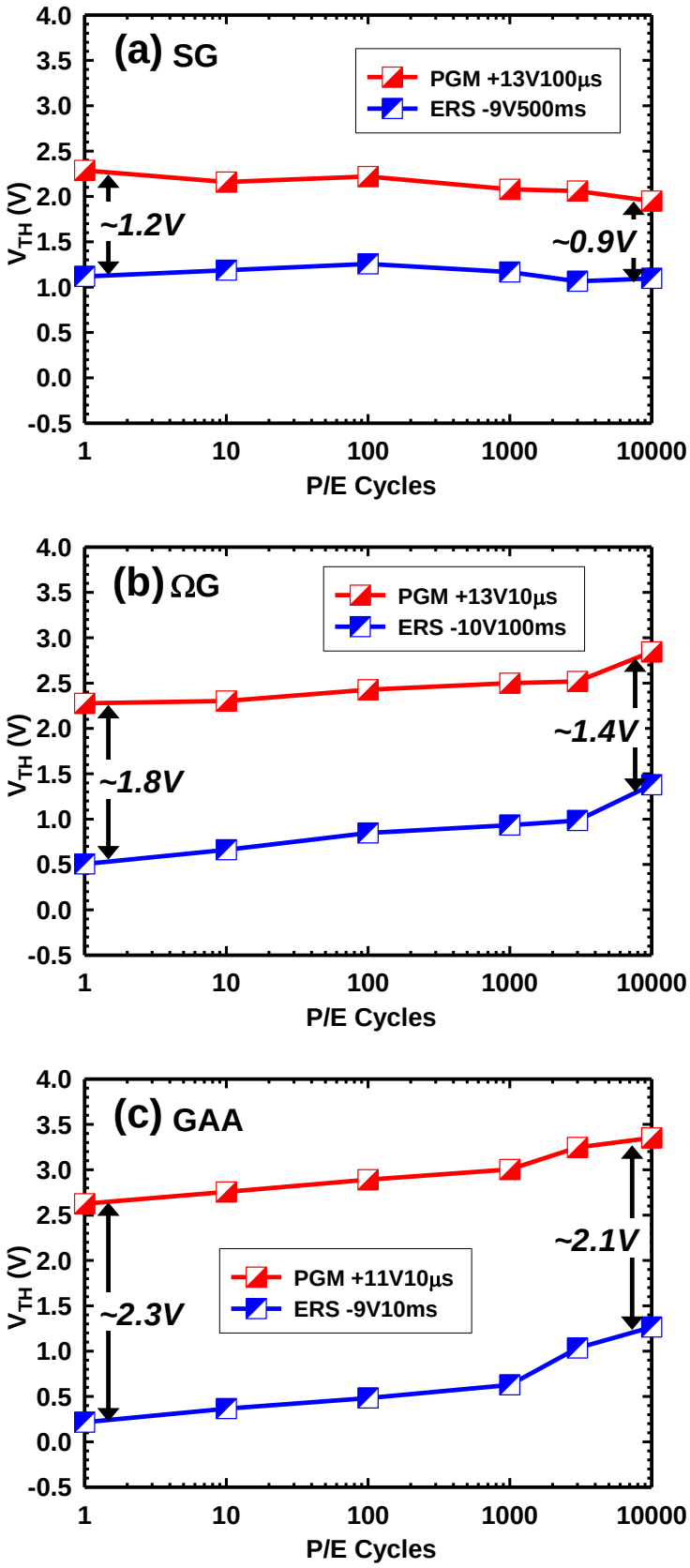


Fig. 4-18 Endurance characteristics of (a) SG, (b) ΩG, and (c) GAA devices.

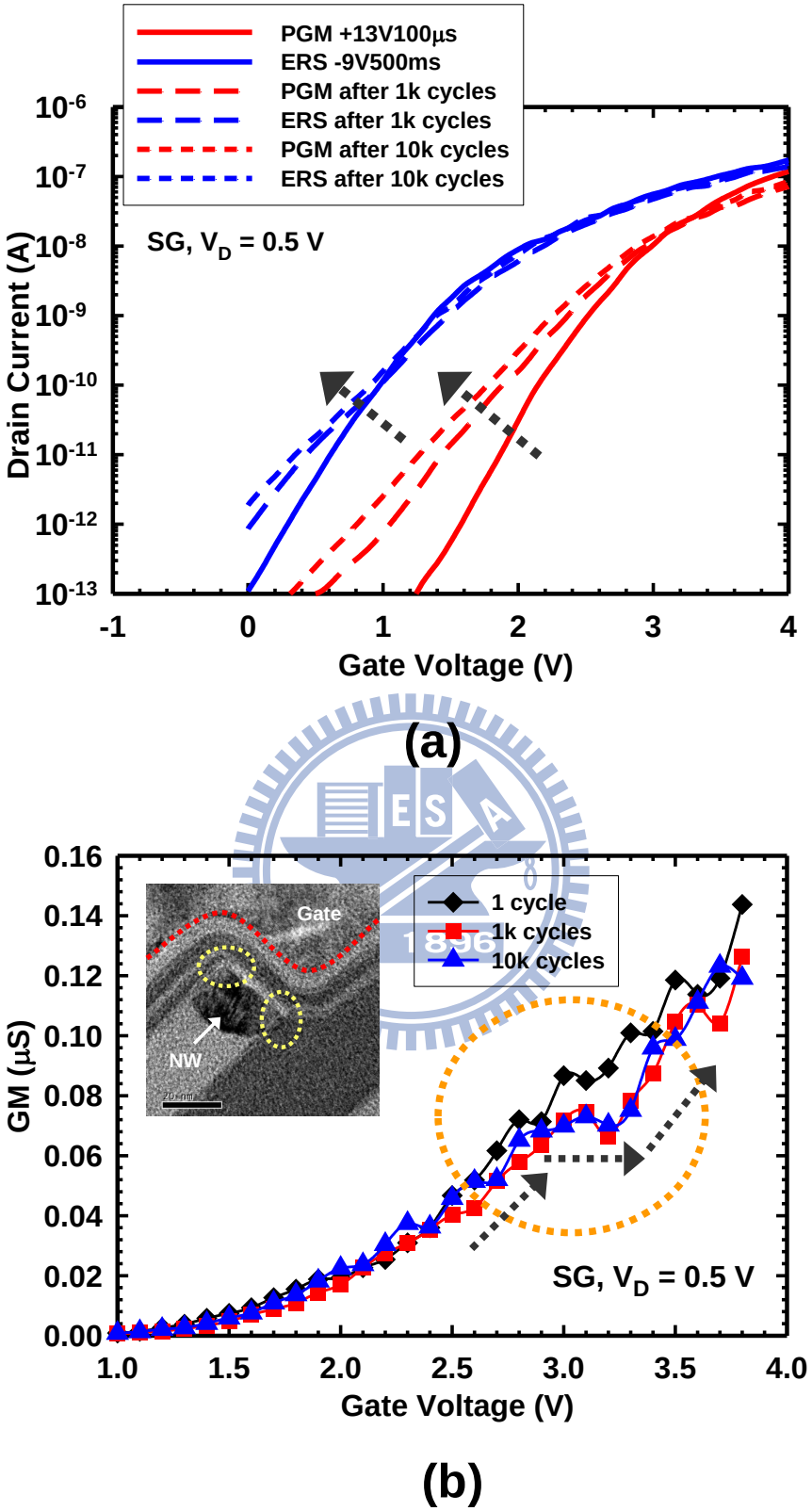


Fig. 4-19 (a) Subthreshold and (b) transconductance (GM) characteristics of a SG device after one, 1k, and 10k P/E cycles of operation.

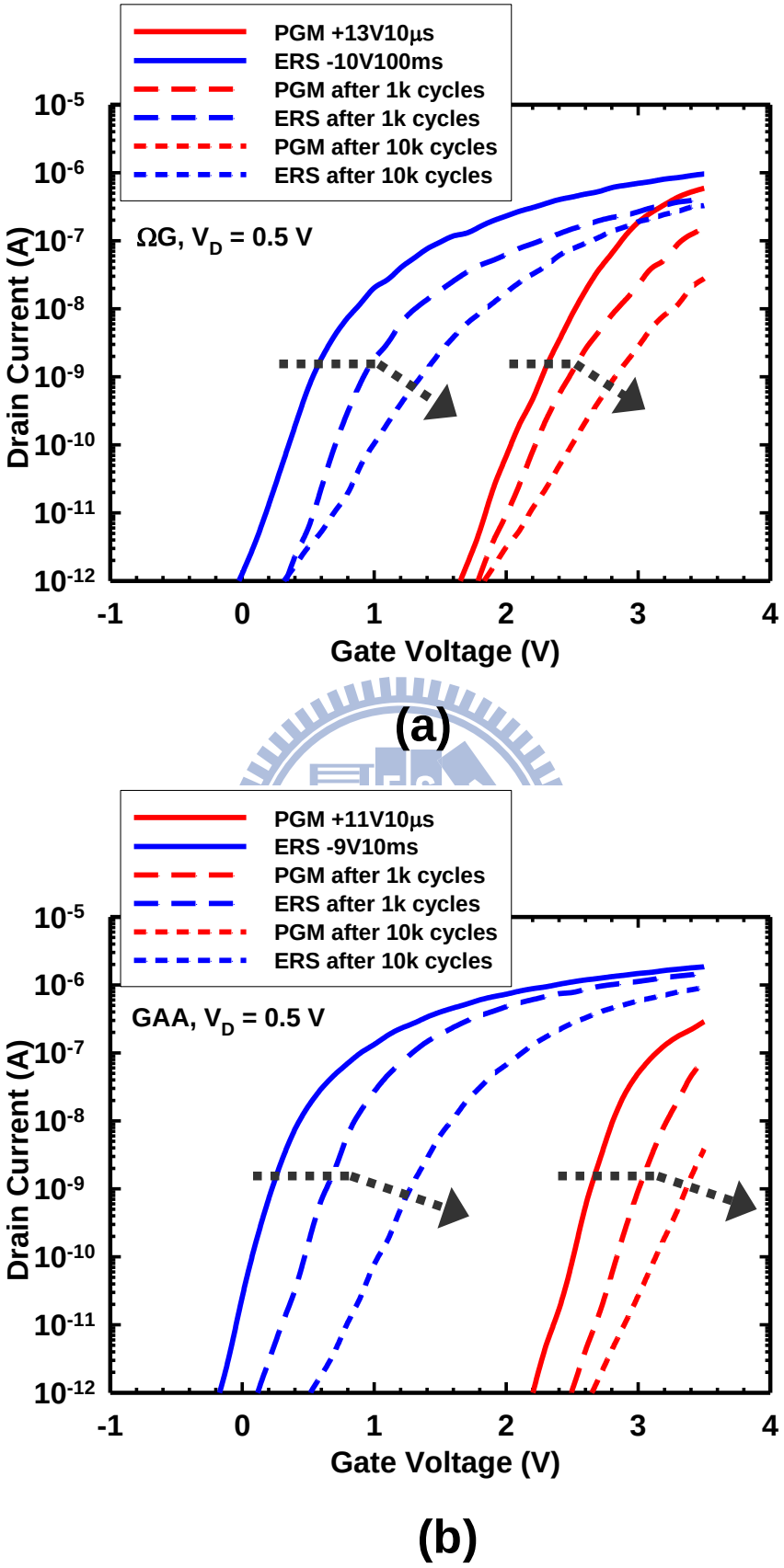
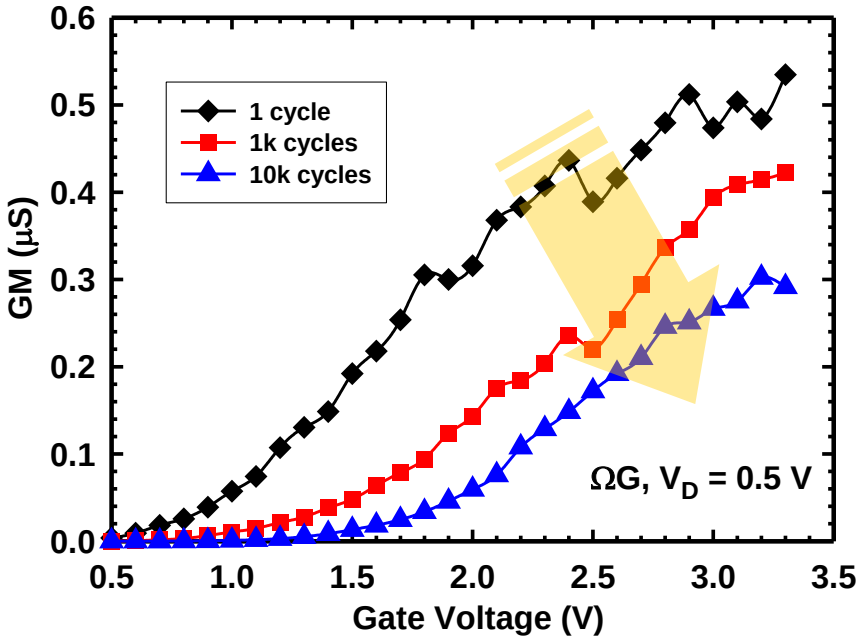
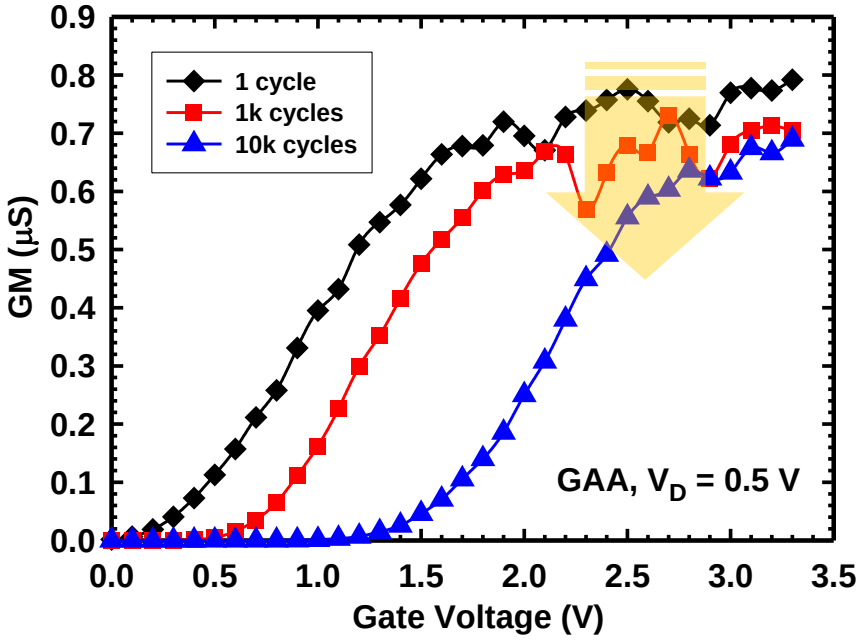


Fig. 4-20 Subthreshold characteristics of (a) ΩG and (b) GAA devices after one, 1k, and 10k P/E cycles of operation.



(a)



(b)

Fig. 4-21 GM characteristics of (a) ΩG and (b) GAA devices after one, 1k, and 10k P/E cycles of operation.

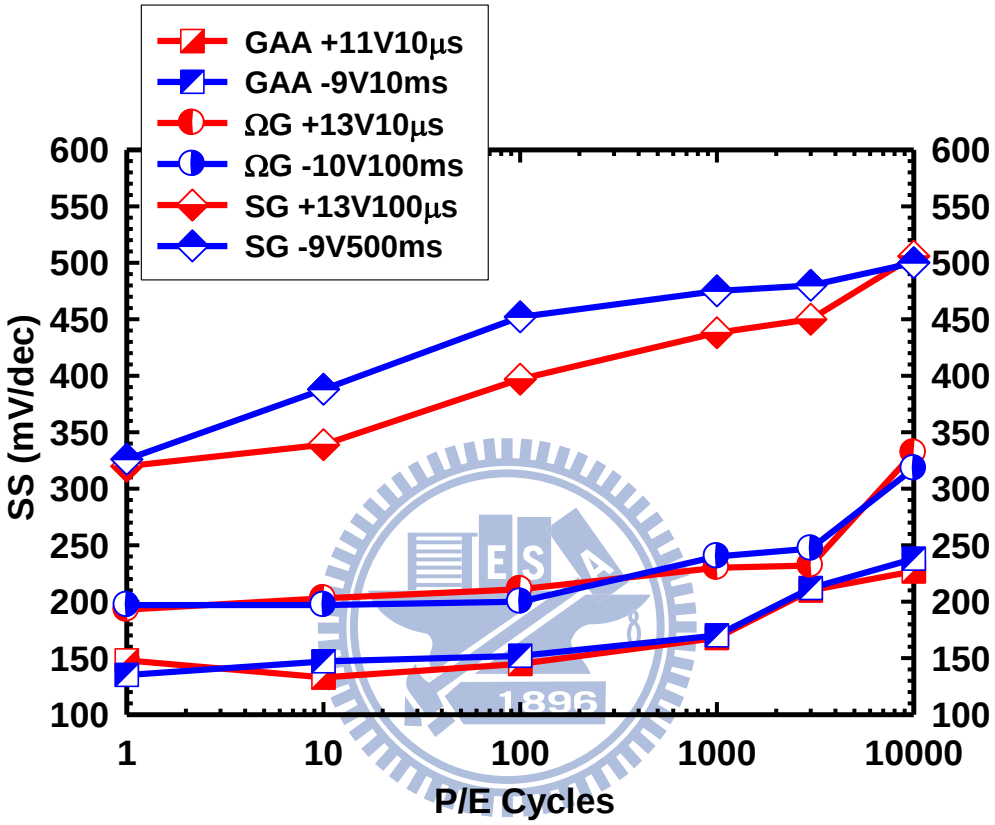
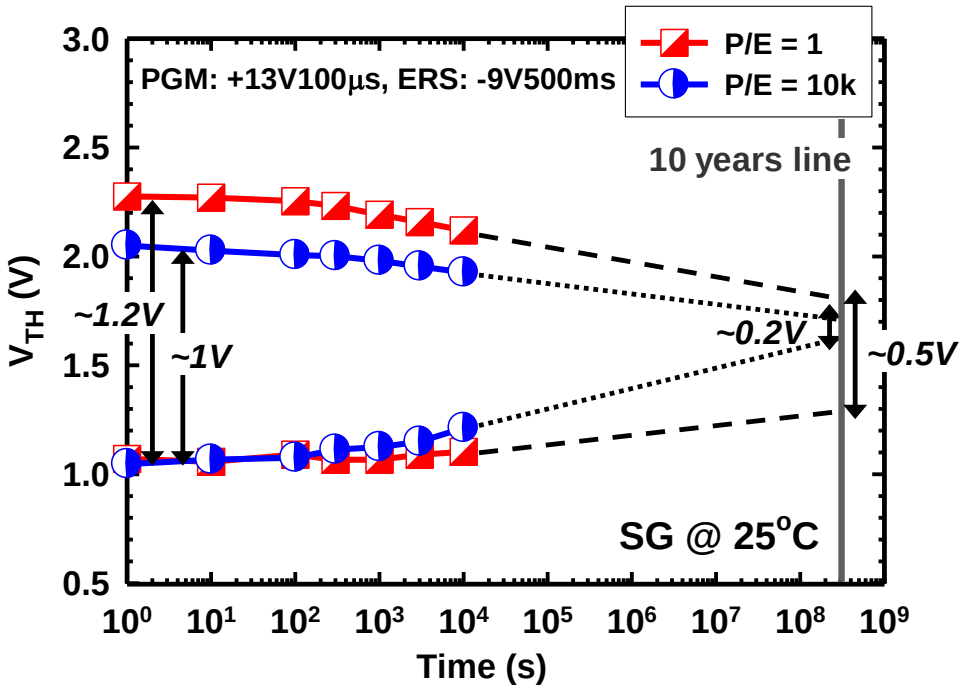
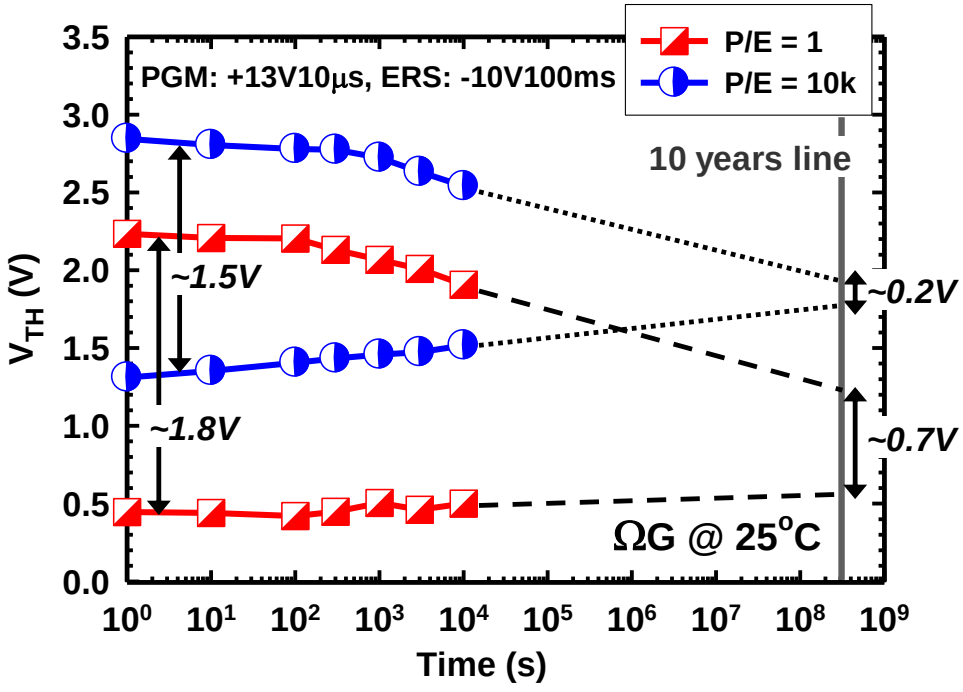


Fig. 4-22 Subthreshold swing (SS) as a function of P/E cycles for the three splits of NW devices.

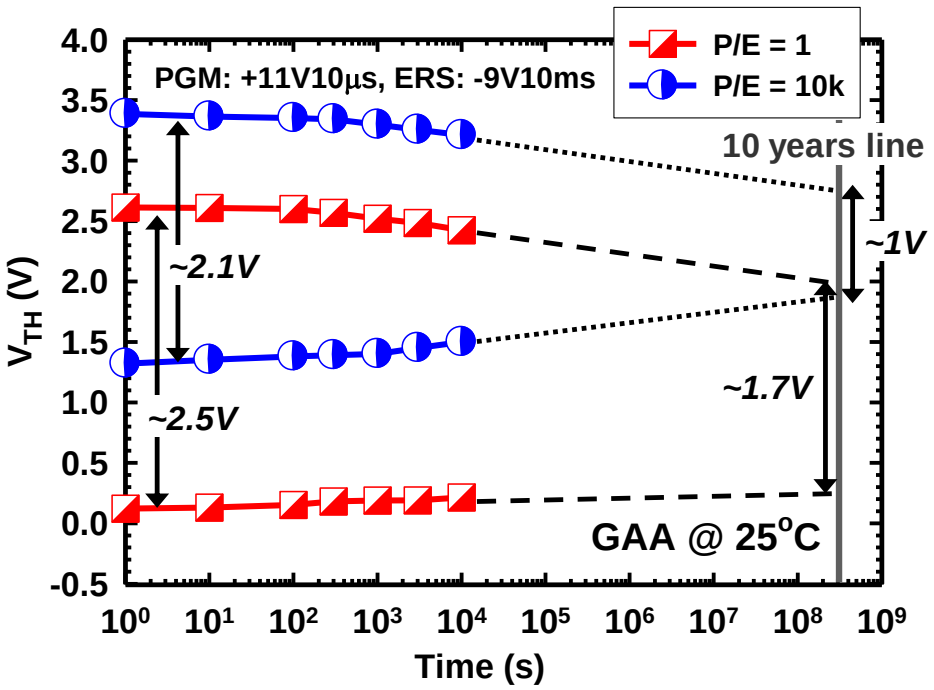


(a)



(b)

Fig. 4-23 Retention characteristics of (a) SG and (b) ΩG devices at room temperature (25 ℃) after single and 10k P/E cycles of operation.



(c)

Fig. 4-23 (c) Retention characteristics of GAA devices at room temperature (25 ℃) after single and 10k P/E cycles of operation.

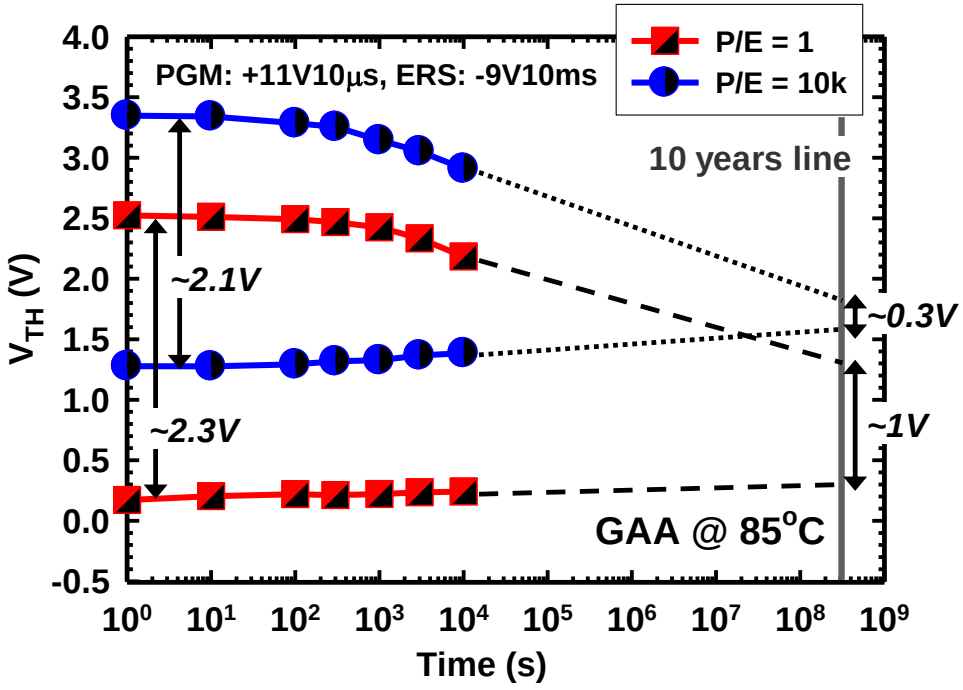


Fig. 4-24 Retention characteristics of GAA devices at 85 ℃ after single and 10k P/E cycles of operation.

Chapter 5

Poly-Si Nanowire Thin-Film Transistors Featuring an Extended Sensing Pad for Sensor Applications

5-1 Introduction

Semiconductor sensors have attracted considerable attention in the past three decades [5.1]. As described in Chapter 1, owing to their capability of miniaturization and compatibility with modern VLSI processes, numerous advantages could be obtained in terms of low cost, standardization, mass production, and applicability for simple testing equipment. These features make semiconductor-based sensors a favorable choice for medical applications. Moreover, a semiconductor sensor based on field-effect transistors (FETs) enables direct translation of the interaction between the analytes and sensing component of devices into a recognizable output signal by means of the electronic properties of the sensing element (*e.g.*, the conductance of the sensing device varies by the surface binding reaction of ions) [5.2].

With respect to bio-sensor applications, FET sensors can be categorized into three groups according to the type of receptor (also called ligand or probe) immobilized onto the sensing part of the sensing device for achieving selective recognition of specific analyte [5.3]:

1) Enzyme-modified FETs, in which catalytic reaction is usually involved to produce potential alteration of the sensing device (*e.g.*, H^+ or H_2O_2 generation or reaction between enzyme and FET's substrate);
2) Cell-based FETs, the potential is changed by the living biological system [5.4];
3) Immunologically modified FETs and DNA-modified FETs, utilizing surface polarization effects or dipole moment changes (*e.g.*, antigen-antibody binding or DNA hybridization).

Nanowire (NW) sensing devices have been demonstrated to possess much higher sensitivity as compared with that of the conventional ion-sensitive FET (ISFET) based sensor due to the high surface-to-volume ratio of NW and its critical dimensions akin to the size of biological molecules [5.4], thus enabling ultra-sensitive, real-time and label-free sensing ability for bio-molecule detection. However, challenges related to the direct immersion of the NW sensor in the aqueous environment during sample testing still remain a critical issue for the reliability and preservation of NW sensor as well as the preciseness of measurements. To address these issues, in this chapter we propose and fabricate a novel scheme combining the configurations of independent double-gated (DG) NWFET and extended-gate FET (EGFET) sensor [5.5]. This scheme takes advantages of EGFET's effective isolation of device from the chemical and biological environment, and NWFET's excellent switching properties. Section 5-2 describes the structure and fabrication process of the proposed device, as well as its operation principles. The basic electrical characteristics of fabricated devices are shown in Section 5-3, and the experimental setups for several sensing purposes are briefed in Section 5-4. In Section 5-5, preliminary experimental results of the proposed NWFET sensing scheme for various sensing

applications including pH sensing, bio-molecules detection and gas sensing are presented and discussed. Finally, a summary is given in Section 5-6.

5-2 Device Structure, Fabrication, and Operation Principles

The top and cross-sectional views of the proposed NW sensing device are illustrated is Figs. 5-1 (a) and (b), respectively, showing that the device structure has a spacer-like NW channel surrounded by two independent gates including an inverse-T gate (G1) and a top-gate (G2). Figs. 5-2 (a) to (e) depict the schematic layout views of process flow. The fabrication process was nearly identical to that of the independent DG NWTFT described in Section 2-2, except for the device layout which was designed to be feasible for sensing purposes. The G1 oxide and G2 oxide are 30- and 20-nm-thick TEOS oxide deposited by LPCVD, respectively. And the critical dimension of the NW channel is supposed to be less than 30 nm by means of the well-controlled dry etching process for NW formation. For the sensing membrane, aluminum oxide (Al_2O_3) was selected and formed by native oxidation of the Al metal pad, and the size of the sensing pad varies from 30×30 μm^2 to 200×500 μm^2. Note that all the fabricated devices for sensing received 2-hr NH_3 plasma treatment to improve their performance. To compare the robustness of different NWFET sensing scheme in aqueous condition, sensing devices with poly-Si NWs directly exposed to the sensing environment were also fabricated [5.6].

According to Chapter 2, the tiny body of NW channel leads to strong gate-to-gate coupling of two independent gates during device operation (*i.e.*, the back-gate

effect), therefore the threshold voltage (V_{TH}) of the device can be modulated by either gate, offering more flexibility in device operation. In this chapter, we explore this feature and come up with a novel sensor scheme by connecting G2 to an antenna-like sensing pad to serve as a SENSE-gate, while G1 serves as READ-gate to read out the signal. During the measurement, the SENSE-gate is used for detecting the targets entities in the test solution (or in the gas environment for gas sensing). A change in the amount of sensing charges would create a potential change and could promptly affect the characteristics of the NW devices, which can be effectively monitored with the READ-gate by sweeping G1 voltage (V_{G1}) to get the transfer curves of the device and then extract the V_{TH} difference (ΔV_{TH}). Another commonly used read-out approach is the real-time current (or conductance) monitoring method [5.6], in which the sensing device is biased at its subthreshold state or ON state during the testing and the real-time drain current (I_D) is measured. In this read-out scheme, the G1 of the NWFET sensor can perform as an auxiliary gate to assist the device so as to be biased at the optimum operation condition (*i.e.*, the highest sensitivity). Furthermore, with proper design for the structural parameters (*i.e.*, oxide thickness of G1 and G2 and NW dimension), the V_{TH} change of the READ-gate induced by the sensed entities could be magnified according to the back-gate-effect theory described in Chapter 2 [5.7]. For instance, provided that the gate oxide of both gates (T_{OX1} and T_{OX2}) are thicker than the channel (T_{Si}), the V_{TH}-shift rate of the READ-gate (G1) caused by the potential change of the SENSE-gate (G2) can be roughly given by $|dV_{THG1}/dV_{G2}| \sim T_{OX1}/T_{OX2}$. From this relation, apparently ΔV_{THG1} can be greater than ΔV_{G2} as T_{OX1} is thicker than T_{OX2}, implying that this sensor scheme is capable of amplifying the sensed signal by utilizing the coupling effect between the SENSE-gate and the READ-gate (*i.e.*, the back-gate effect). Recently this concept has been demonstrated in some literatures [5.8-5.10].

On the other hand, since the active region of the NW device can be effectively separated from the chemical environment during sensing operation by its extended-gate structure, the lifetime or reliability of this sensor scheme is expected to be much longer and more reliable than that of the conventional NWFET sensing scheme which directly immerses the NW sensor in the aqueous test solution during testing.

5-3 Experimental Setup for Sensing Purposes

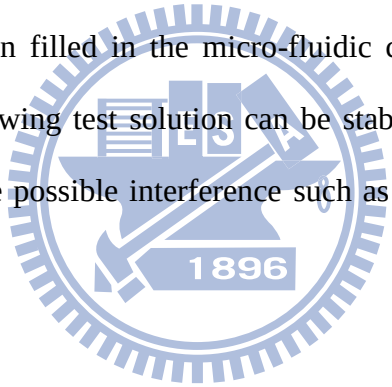
In this chapter, all electrical characterization of the NW sensing devices were measured by an automated system composed of 4200 Semiconductor Characterization System (Model 4200-SCS) with built-in control software Keithley Interactive Test Environment (KITE), switching system-708A, and a probe station.

5-3.1 Micro-Fluidic System and Measurement Settings

To perform sensing process in aqueous environment, a novel micro-fluidic channel system was applied here to provide stable and robust interface between sensor and the test solution, and also the capability of measuring a small quantity of test sample. The schematic illustration of this micro-fluidic channel system is shown in Fig. 5-3, it is constructed by a chip holder (Fig. 5-4 (a)), a flexible micro-fluidic channel made of polydimethylsiloxane (PDMS) (Fig. 5-4 (b)), and an acrylic mold (Fig. 5-4 (c)). For assembling these components, the chip with sensing devices was placed on the bottom chip holder, and the PDMS micro-fluidic channel together with the acrylic mold were sequentially put on the top of the chip, and then fastened by capping the top chip holder to prevent the micro-fluid channel from leaking. The

micro-fluid channel system is connected with inlet and outlet pipes to let the test solution flowing in and out. To transport the test solution continuously through the sensing region of the device, a pneumatic micro-pump with an injector is used (Fig. 5-5), allowing stable flow and sequential injection of the solution. The cross-sectional view and top view of the sensor chip equipped with the micro-fluid channel system is depicted in Figs. 5-6 (a) and (b), respectively.

In addition, platinum (Pt) was chosen as the material for reference electrode due to its very low chemical reactivity even in extremely high or low pH environment. In this study, a long fine Pt wire was inserted into the outlet pipe of the micro-fluid channel system, and was connected to a measurement probe to be able to apply voltages to the test solution filled in the micro-fluidic channel and pipes. With Pt reference electrode, the flowing test solution can be stabilized, and also could have better immunity against the possible interference such as static electricity during the measurement.



5-3.2 Immobilization of Bio-Molecules on Sensing Pad

To achieve selective and specific recognition of chemical or bio-molecular species, the surface of the sensing membrane needs to be functionalized with a specific molecule to allow the active compound of the target to be attached to the membrane surface. 3-Aminopropyltriethoxysilane (APTES) has been widely used in affinity-based biosensors because it can facilitate the immobilization of bio-molecules onto the sensing membrane. The structural formula of APTES is shown in Fig. 5-7 (a). The silane group of the structure can tightly bind to silicon or glass substrates, while its amine group can form covalent bonds with carboxyl groups (functional groups that are commonly found in bio-molecules), as shown in Fig. 5-7 (b) [5.11].

Fig. 5-8 briefly describes the immobilization process used in this study and detection of DNA-hybridization. To functionalize the Al_2O_3 sensing membrane for DNA detection, first the device was immersed in 2% APTES for 17 min then heated at 80 ℃ for 10 min. Then the device was treated with 2.5% glutaldehyde in the phosphate buffered silane (PBS) solution for 30 min, followed by coupling the probe-DNA to the active surface. Finally, the un-reacted aldehyde groups were blocked with ethanolamine to complete the probe-modified sensing pad. Note that all the immobilization processes were executed in the micro-fluidic channel system.

5-3.3 Gas Chamber System and Measurement Settings

Fig. 5-9 displays photographs of the gas-sensing equipment including a gas chamber used in this study. The chamber pressure can be pumped down to around 10^{-2} torr. During the measurement, the sensing device chip is placed on the sample stage located at the middle of the chamber, and the probing system is also inside the gas chamber surrounding the sample stage (Fig. 5-9 (b)). A flow meter is connected to the inlet of the pipe that transfers the gas from steel cylinder to precisely control the flow rate, thus allowing us to estimate the concentration of the gaseous molecules based on the injection time of the gas flow and the volume of the gas chamber (~ 50 liter).

5-4 Poly-Si NW Sensing Device for Various Sensor Applications

5-4.1 Basic Electrical Characteristics of Poly-Si NW Sensing Devices

Typical transfer characteristics of the independent DG poly-Si NWFET sensing devices with and without 2-hr NH_3 plasma treatment are shown in Figs. 5-10(a) and (b), respectively. The bias condition of different operation modes indicated in the figure can be found in TABLE 2-1. The extracted subthreshold swing (SS) of NW sensing device without plasma treatment (Fig. 5-10 (a)) is 180 mV/dec, 300 mV/dec and 370 mV/dec for DG, SG1 and SG2 mode, respectively. While for the device with plasma treatment (Fig. 5-10 (b)), the SS is 100 mV/dec, 170 mV/dec and 200 mV/dec for DG, SG1 and SG2 mode, respectively. Therefore, it is evident that the NW device with NH_3 plasma treatment exhibits much better switching properties in terms of lower leakage current and better SS, which are desirable for sensing application due to the fact that the higher sensitivity can be achieved as the sensing device is operated in the subthreshold region.

However, since the sensing device will be mainly operated in SG1 mode (G1 as the driving gate, G2 floating or grounded by the reference electrode in test solution), it is necessary to examine the V_{TH} modulation ability of the G2 bias to imitate the device characteristics influenced by the potential change at the surface of the sensing membrane caused by the charged chemical or bio-molecular species. The measured I_D-V_G characteristics of the DG NWFET device under SG1 mode with G2 bias ranging from -2 V to 2 V are displayed in Fig. 5-11(a), showing the V_{TH} of the SG1

mode (V_{THG1}) is linearly modulated by V_{G2}. The extracted V_{THG1} as a function of V_{G2} is depicted in Fig. 5-11(b), and the V_{TH}-shift rate is estimated to be around -0.8 V/V. Nevertheless, the original intention of this independent DG sensing scheme is to achieve an absolute V_{TH}-shift rate greater than 1 V/V for the purpose of amplifying the sensed signal, as mentioned in Section 5-2. This is the reason why the thickness of G2 oxide (20 nm) is designed to be smaller than that of G1oxide (30 nm) in this study. This unsatisfactory outcome of V_{TH}-shift rate could be caused by the larger gated width of the NW by G1 than that by G2 (see Fig 2-4 in Chapter 2), leading to better controllability of G1 over the NW channel as compared with G2. Therefore, the result simply suggests that the thickness difference between G1 oxide and G2 oxide is not sufficient (*i.e.*, G1 oxide is not thick enough or G2 oxide is not thin enough) to compensate or overcome the deficiency associated with the shorter effective gating width of G2. Even though the V_{TH}-shift rate is not desirable, the electrical properties of the fabricated devices are still quite decent and capable of realizing the sensing purposes.

5-4.2 pH Sensing

In general, pH is the value commonly used to indicate the acidity or basicity of an aqueous solution. The formal definition of pH is expressed as:

$$pH = -\log[H^+]_B, \tag{5-1}$$

where $[H^+]_B$ is the concentration of the proton (*i.e.*, H^+ ion) in the solution (*i.e.*, electrolyte). To understand the mechanism of pH sensing by the FET with sensing membrane (*i.e.*, ISFET), firstly the theories for describing the electrostatic potential at the electrolyte/sensing membrane interface are briefly introduced as follows.

Site-binding model [5.12] and Gouy-Chapman-Stern (GCS) double layer model [5.13] are the most popular theories in explaining the characteristic of the electrolyte/insulator system, and a more complete model for pH sensing using ISFET was proposed by van Hal and Eijkel [5.14] by modifying the aforementioned two theories. In site-binding model, it suggests that the protons in the electrolyte are able to react with the hydroxyl group formed at the surface of the oxide-based sensing membrane (here assuming A_xO_y), as illustrated in Fig. 5-12. The reactions can be generally written as:

$$AOH \xleftrightarrow{Ka} AO^- + H_S^+, \tag{5-2}$$

and

$$AOH_2^+ \xleftrightarrow{Kb} AOH + H_S^+, \tag{5-3}$$

where H_S^+ refers to proton at the membrane surface, K_a and K_b are dissociation (equilibrium) constants for the above chemical equilibrium equations and are given by:

$$K_a = \frac{[AO^-][H^+]_S}{[AOH]}, \tag{5-4}$$

$$K_b = \frac{[AO^-][H^+]_S}{[AOH_2^+]}. \tag{5-5}$$

From Eq. (5-4) and Eq. (5-5) one can obtain pH_{pzc}, the pH value for which the sensing membrane surface is electrically neutral, defined by $pH_{pzc} = -\log(K_aK_b)^{1/2}$. Accordingly, when $pH < pH_{pzc}$, the amount of the proton-bound site (OH_2^+) on the membrane surface would be larger than that of the proton-dissociated site (O^-), leading to a net positively charged surface, and for $pH > pH_{pzc}$ the surface condition would be simply the other way around.

In GCS double layer model (depicted in Fig. 5-13 [5.15]), the surface charge

created by binding/dissociating (or adsorption) reaction gives rise to the double layer formation close the surface, and the diffused layer is assumed to start at a small distance away from the surface. All the ion distributions in the electrolyte follow Poisson-Boltzmann equation, and thus the surface potential (ψ_S) is constructed by the charge distribution in those layers. Therefore, the relation between surface proton concentration $[H^+]_S$ and the bulk concentration $[H^+]_B$ can be expressed as:

$$[H^+]_S = [H^+]_B \cdot \exp\left(\frac{-q\psi_S}{kT}\right), \tag{5-6}$$

or

$$pH_S = pH_B + \frac{q\psi_S}{2.3kT}, \tag{5-7}$$

where k is the Boltzmann constant and T is the absolute temperature. Consequently, based on the theory proposed in [5.14], the sensitivity of the surface potential ψ_S to the change of the bulk pH can be derived and expressed as:

$$\frac{\Delta\psi_S}{\Delta pH_B} = -2.3\frac{kT}{q}\alpha, \tag{5-8}$$

where α is the dimensionless parameter that lies between 0 and 1 depending on the proton buffer capacity of the sensing membrane surface and the differential capacitance of the double layer [5.14]. According to Eq. (5-8), the ideal sensitivity (*i.e.*, the so-called Nernstian response) of 59 mV/pH at 25 ℃ can be obtain by letting α = 1, which also represents the maximum sensitivity that can be achieved by the conventional ISFETs since the V_{TH} shift (ΔV_{TH}) of the ISFET is essentially equal to -$\Delta\psi_S$. However, the independent DG NWFET sensing scheme used in this study is potentially capable of surmounting this sensitivity limitation by taking advantage of the back-gate effect as described in Section 5-2.

In the pH sensing experiment of this study, all the pH test solutions were made by mixing phosphate buffered saline (PBS) (10mM, pH7.4) with NaOH and HCl

solutions. Fig. 5-14 depicts the real-time I_D response of the DG NWFET sensor measured in the test solution with various pH values. It can be seen that the signal response in I_D is strongly dependent on pH, and the I_D is higher at lower pH value. This is due to the fact that the surface potential at the electrolyte/sensing membrane interface positively increases with decreasing pH, resulting in the reduced V_{TH} of the sensor device and hence larger I_D is sensed. The subthreshold characteristics as well as the extracted V_{TH} of the sensing device at corresponding pH values are also shown in Figs. 5-15 (a) and (b), respectively. However, an unexpected high sensitivity of around 67.5 mV/pH is obtained in this experiment, which is greater than the theoretical Nernst limit (59 mV/pH) as mentioned previously. The origin of this phenomenon is still unclear, yet it occurs in every pH sensing test during the experiment in this study.

5-4.3 Bio-Molecules Detection

For the purpose of detecting specific bio-molecule, the Al_2O_3 sensing membrane surface is functionalized with APTES and probe-DNA. The surface modification process is detailed in Section 5-3.2. Since DNA is negatively charged in the neutral pH environment, it is expected that a decrease of the surface potential at the electrolyte/Al_2O_3 interface could be induced by the hybridization of target DNA, and therefore a reduced I_D should be observed in the real-time current measurement. Fig. 5-16 shows the sensing characteristics of the DG NWFET sensor with its sensing membrane surface modified by Coxsackievirus A16 (CA16) DNA probes, and two noticeable drops in I_D (normalized to the value at the beginning of the test) are detected after injecting CA16 target DNA (100nM) into the micro-fluidic channel (at 5k sec and 9k sec), while there is no significant change in I_D after injecting the

Enterovirus 71 DNA (EV71, 100nM) at 1.8k sec. This is because only the complementarily matched DNA/DNA hybridization (CA16/CA16) is able to induce a substantial potential drop at the sensing surface, giving rise to a decreased I_D.

The experimental data more or less demonstrate that the selective bio-molecule detection for specific target DNA is achievable by using the novel DG NWFET sensor with careful modification of the sensing surface. Nevertheless, the large sensing pad area (100×500 μm^2 in this experiment) may be responsible for the slow response time (few thousand seconds) and moderate sensitivity (~100 nM) to the DNA molecules. Since the reference electrode is needed to stabilize the test solution, the change of surface potential necessitates high enough density of the target DNA bonded to the sensing membrane. As a result, the bigger sensing area implies a larger amount of bonded target DNA is required to produce the same potential shift of the sensing surface as compared to the smaller one, thus degrading the response time and also the sensitivity.

5-4.4 Gas Sensing

For gas sensing experiments conducted in the study, the real-time I_D is measured to monitor the variation of electrical performance of the DG NWFET sensor under different gaseous environment in the gas chamber. During the sensing test, the SENSE-gate of the device is floating and serves as an antenna to collect signals of the change in ambient gas, and the READ-gate is applied with a suitable bias to make the sensing device working. The detection mechanism is based on the chemical reaction and adsorption between gas molecules and sensing surface involving the transfer of some charges, which may lead to sensible electrical signal that can be read by the sensing device. The real-time I_D response measured under various conditions of the

gas chamber is shown in Fig. 5-17. Note that in the figure I_D is normalized to the value under vacuum condition at the very start of the test. A positive increase in I_D can be seen after the injection of 3 ppm ammonia gas (NH_3) uniformly mixed with air. We speculate this current increment might be due to the adsorption of NH_4^+ ion on the sensing surface, which is generated by the reaction of NH_3 with moisture in the air (humidity ~ 50%), resulting in more electron carriers induced in the NW channel by the positively charged sensing pad and thus enhancing the channel conductance. However, the I_D response exhibits no recovery after removing NH_3 gas by pumping down the gas chamber, indicating that the adsorptive positive ions are neither detached from the sensing surface nor neutralized by the negative charges.

With respect to improving the sensitivity of the sensing device to the gas, an intriguing experiment using single-stranded DNA (ssDNA) as a molecular targeting layer for gas sensing is also performed in this study [5.16-5.18]. To form the ssDNA targeting layer, a droplet containing ssDNAs was dripped onto the Al_2O_3 sensing surface (as illustrated in Fig. 5-18), then the gas chamber was pumped down to vacuum in order to evaporate the solvent in the droplet and leave the ssDNAs attached to the sensing surface. Fig. 5-19 depicts the real-time I_D response of the sensing device with ssDNA targeting layer to the variation of the condition of gas chamber. Apparently much more drastic responses can be seen in the figure compared to that in Fig. 5-17 when air (humidity ~ 50%) is being introduced into the gas chamber at 300 sec (vacuum) and 1.5k sec (3 ppm dry NH_3 gas already in the chamber). It is worth noting that without moisture in the gas chamber, the sensing device manifests no positive I_D response to the injection of NH_3 gas (from 1.2k sec to 1.5k sec) and the I_D even slightly decreases. The result sort of supports the postulation about the formation and adsorption of NH_4^+ ion on the sensing pad, and may also suggest that the

enhanced sensitivity to NH_3 gas in moist air with ssDNA targeting layer could be attributed to the negatively charged phosphate backbone ($-PO_4^-$) of DNA molecules that tend to attract the NH_4^+ ions. To confirm the impact of ssDNA layer on device sensitivity to NH_3, after cleaning the device tested in Fig. 5-19 with deionized water (DIW) to remove the attached ssDNA, the same NH_3 gas sensing experiment procedure as in Fig. 5-17 was repeated using this cleaned device and the result is shown in Fig. 5-20. Interestingly, the I_D response behavior is quite similar to that displayed in Fig. 5-17, verifying the effectiveness of ssDNA targeting layer on the sensitivity to NH_3 in moisture. Nonetheless, the detailed sensing mechanism still needs to be further explored. Plausibly the H-bonding between H_2O/NH_3 and ssDNA plays an important role in affecting the surface condition (*e.g.*, polarity) of the sensing membrane [5.19].

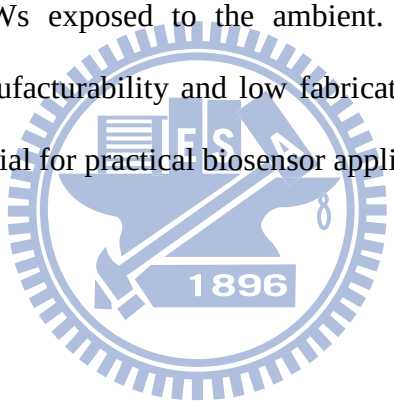
5-4.5 Robustness Test in Aqueous Environment

One of the most important incentives for exploring the sensing device scheme used in this study is to prolong the lifetime and improve the stability of the NW sensor in aqueous or moist environment, thereby making the sensing measurement more reliable. In this sub-section, the robustness and stability of the as-fabricated DG NWFET sensor (denoted as DG-NW sensor) in aqueous solution will be compared with those of NWFET sensor having poly-Si NWs exposed to the solution (denoted as ex-NW sensor) [5.6]. Fig. 5-21 and Fig. 5-22 depict the I_D-V_G curves ((a) with I_D in logarithmic scale and (b) with I_D in linear scale) of DG-NW sensor and ex-NW sensor, respectively, measured after corresponding stressing time. The stressing tests for both sensors are performed by immersing the sensing region of the device in PBS (pH = 7) with micro-fluidic channel system, and the bias condition is $V_D = V_S = V_G = 0$ V. It

can be noticed that the I_D at ON-state and the SS of the ex-NW sensor degrades with increasing stressing time (Fig. 5-22), while the SS remains nearly unchanged for the DG-NW sensor during the stressing test (Fig. 5-21). The extracted V_{TH} shift (ΔV_{TH}) and ON-current variation (ΔI_{ON}) of both sensor devices as functions of stressing time are shown in Fig. 5-23 and Fig. 5-24, respectively. The increasing V_{TH} of the ex-NW sensor (Fig. 5-23 (b)) is mainly attributed to SS worsening, and the I_{ON} (Fig. 5-24 (b)) and SS degradations clearly indicate that the quality of the NW channel deteriorates during the stressing test due to its direct contact with the aqueous surroundings. Consequently, though a previous work [5.20] has reported that a dramatic improvement in device characteristics can be obtained as FET with poly-Si NW channels is exposed to a wet environment because of the water passivation effect, here the results of the stressing test in aqueous solution (PBS) suggest that defects still keep being generated in poly-Si NW channel of the ex-NW sensor during the stressing, therefore degrading the device performance. In contrast, the DG-NW sensor evidently exhibits much more stable device characteristics in terms of ΔV_{TH}, ΔI_{ON} and SS during the stressing test in aqueous environment (Fig. 5-23 (a) and Fig. 5-24 (a)), which is commensurate with the fact that the active region of DG-NW sensor is effectively protected by this extended-gate scheme.

5-5 Summary

In this chapter, a novel DG NWFET sensing scheme featuring an extended sensing gate (SENSE-gate) and a READ-gate for various sensing purposes is proposed and fabricated. Results of the preliminary study using this DG NWFET sensor for pH sensing, bio-molecules detection and gas sensing applications are also presented and demonstrated. Owing to the effective isolation of the proposed device from the testing environment containing abundant chemical and biological species, this novel sensing scheme exhibits more stable and reliable electrical characteristics during the stressing test in aqueous solution as compared with those of NW sensor device having poly-Si NWs exposed to the ambient. This improved endurance together with its high manufacturability and low fabrication cost make this scheme extremely useful and potential for practical biosensor applications.



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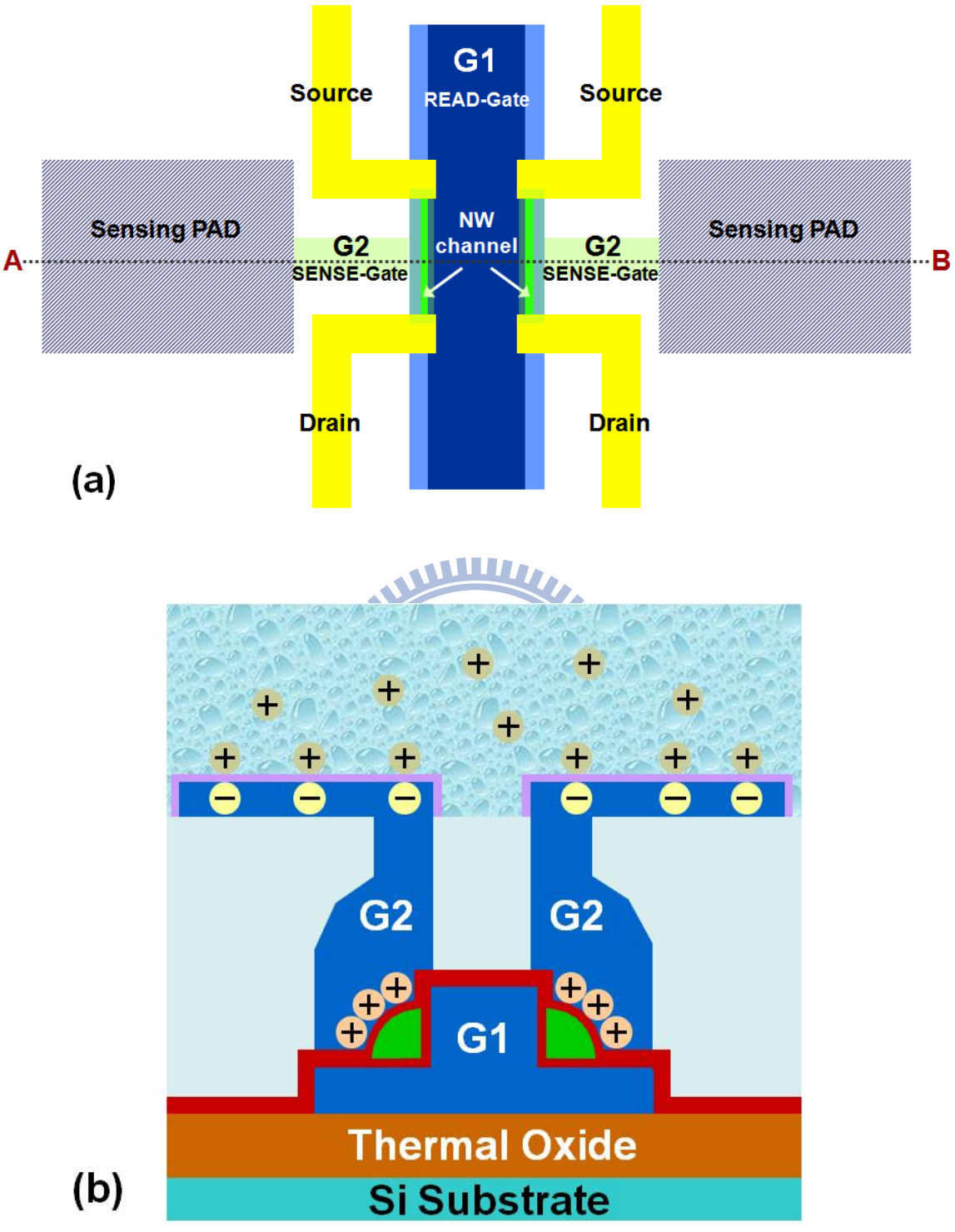


Fig. 5-1 (a) Top view and (b) cross-sectional view of the novel poly-Si NWFET sensing device featuring extended sensing pads and independent double-gated (DG) configuration.

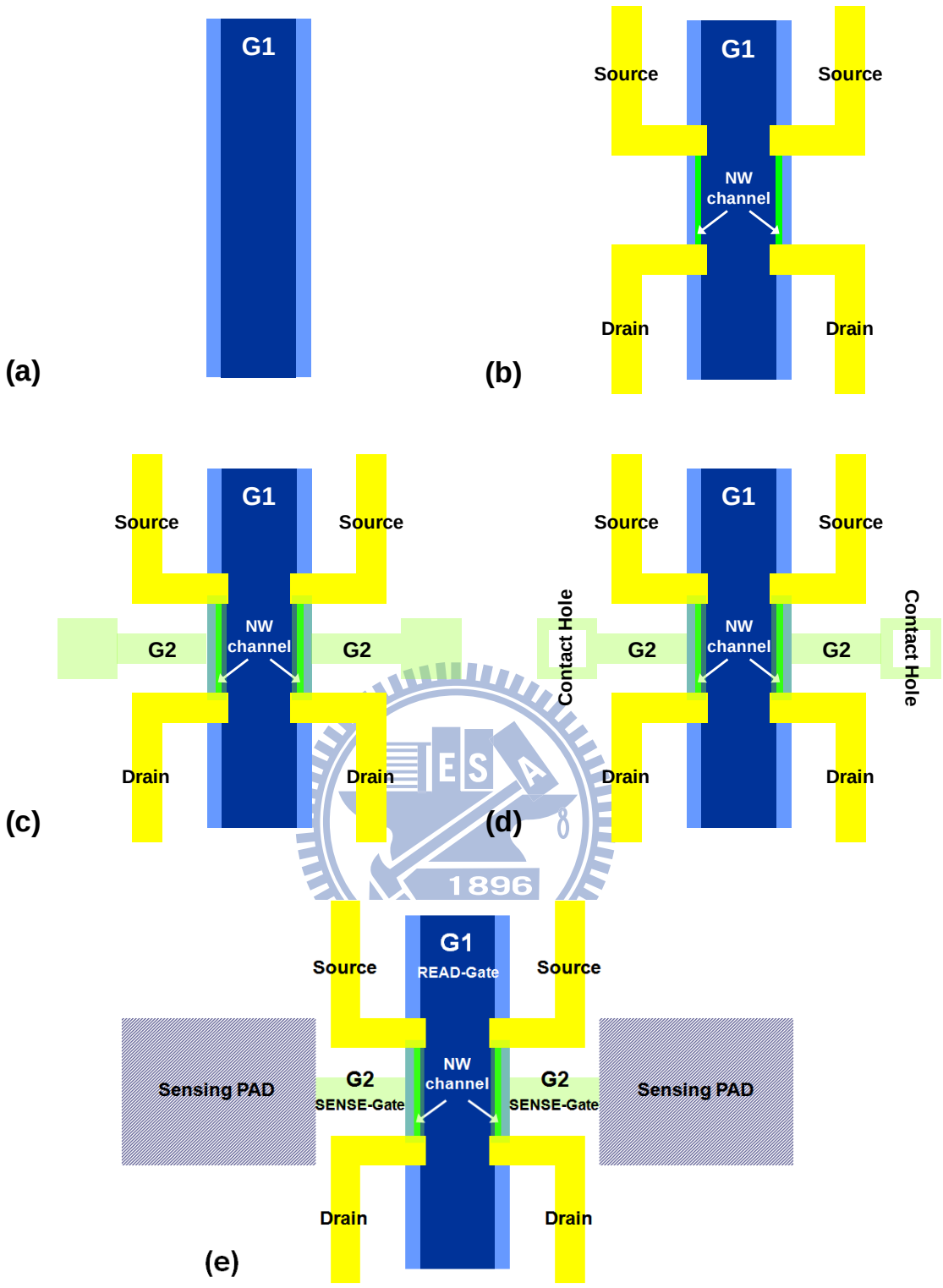


Fig. 5-2 Process flow in layout views for fabrication of the DG NWFET sensing devices with extended sensing pads. (a) Formation of an inverse-T gate. (b) Definition and formation of S/D and NW channel by anisotropic etching. (c) Deposition of G2 oxide and n^+ poly-Si, followed by definition of G2 (SENSE-gate). (d) Formation of contact holes. (e) Metallization and formation of sensing pads and Al_2O_3 sensing membrane.

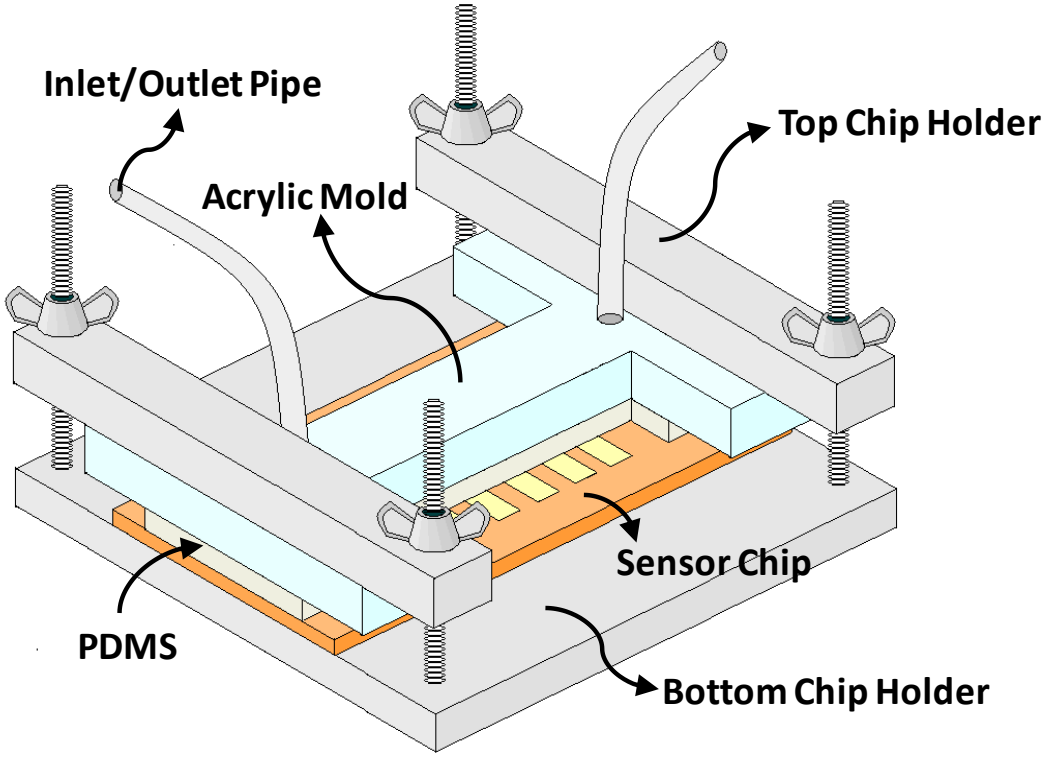
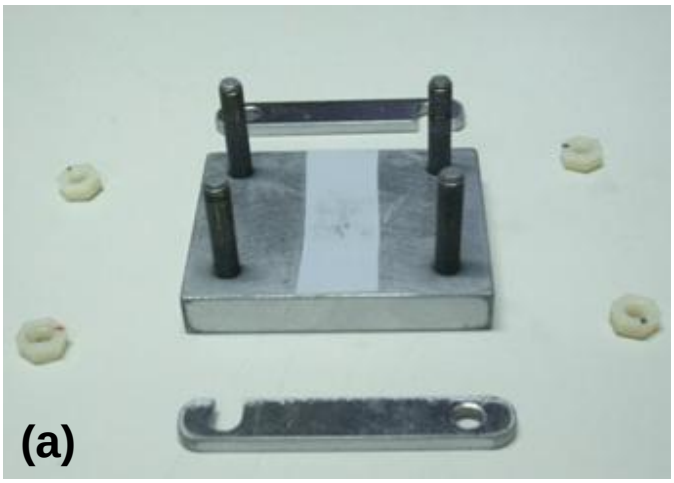


Fig. 5-3 Schematic illustration of the micro-fluidic channel system.



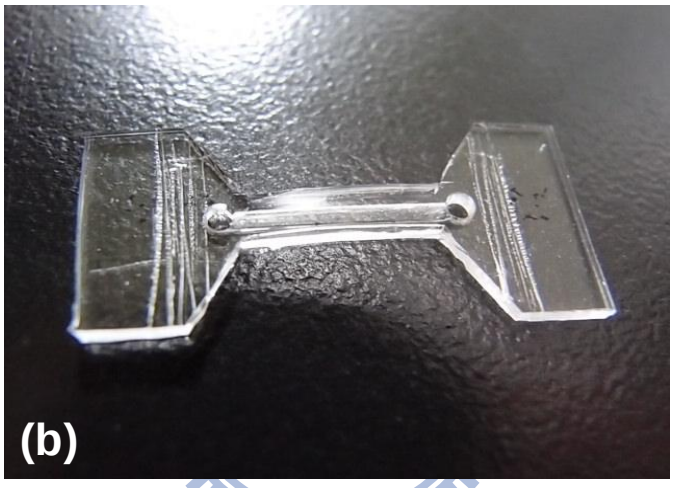


Fig. 5-4 Pictures of the components of the micro-fluidic channel system. (a) The chip holder. (b) The flexible micro-fluidic channel made of PDMS. (c) The acrylic mold.

Fig. 5-5 Pneumatic micro-pump with an injector used for injecting the sample solution into the micro-fluidic channel.

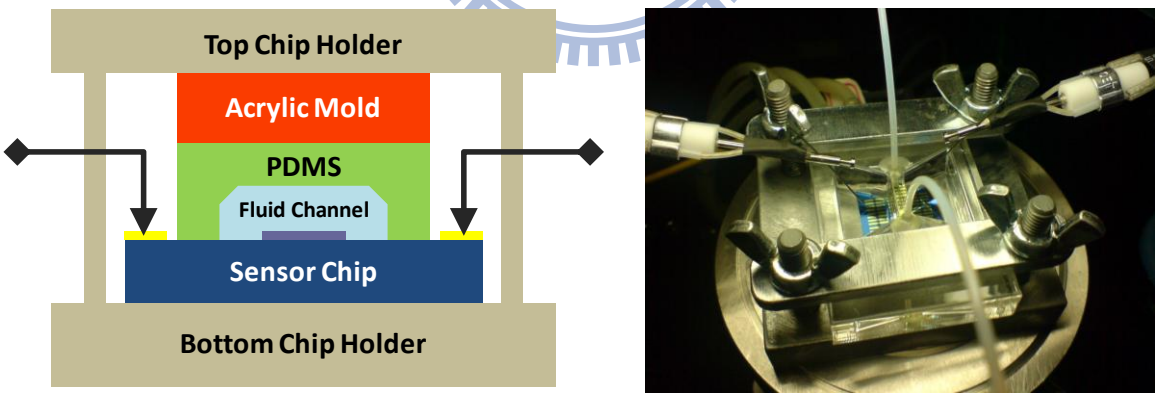


Fig. 5-6 (a) Cross-sectional view and (b) top view of the sensor chip equipped with the micro-fluid channel system.

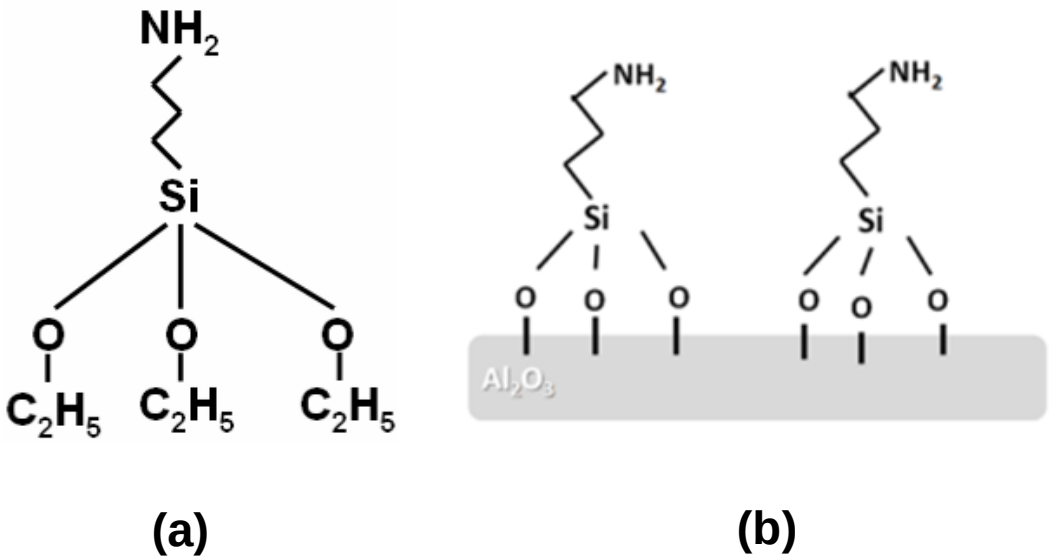


Fig. 5-7 (a) Structural formula of APTES. (b) Schematic diagram of APTES immobilized on the Al_2O_3 sensing membrane.

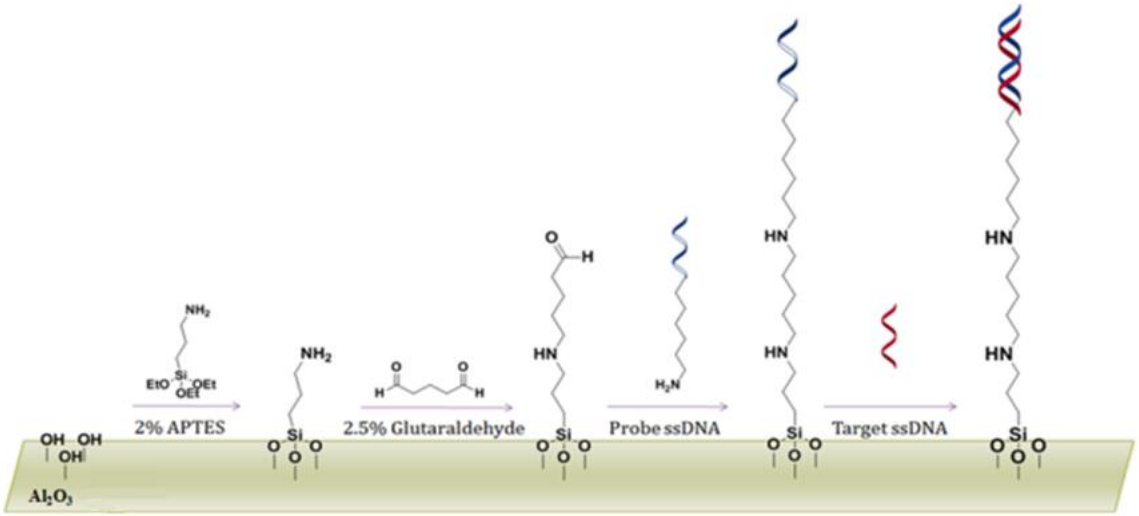
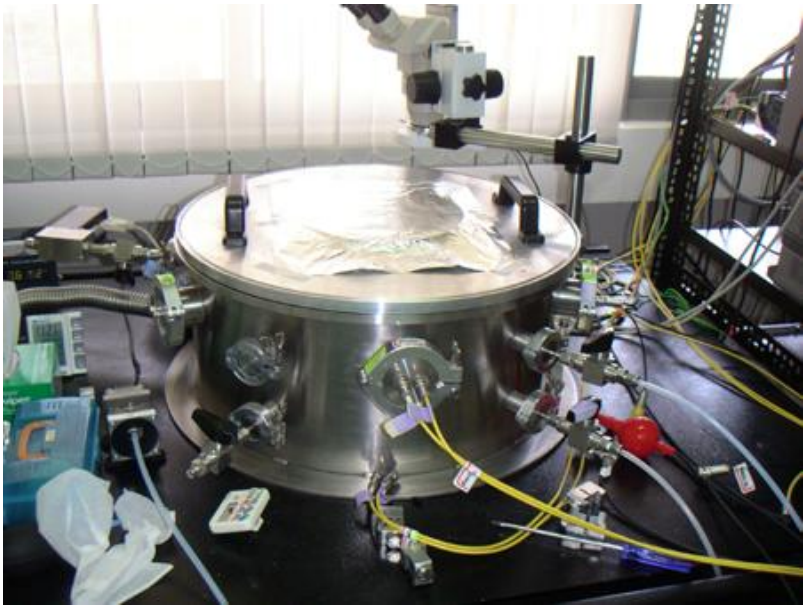
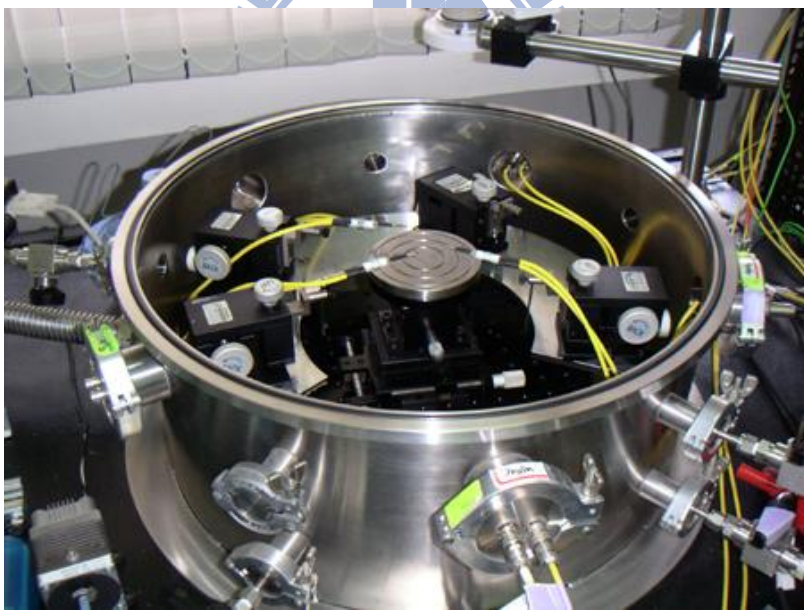


Fig. 5-8 Schematic diagram of immobilization process and detection of DNA-hybridization.



(a)



(b)

Fig. 5-9 Photographs of (a) the capped gas-sensing chamber and (b) uncapped gas-sensing chamber.

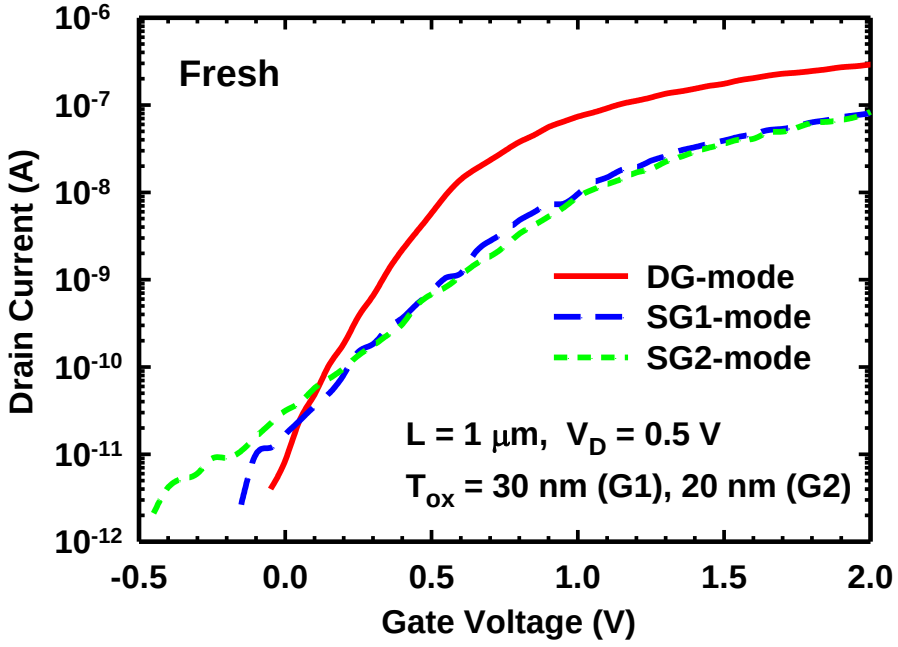


Fig. 5-10 Transfer characteristics of fabricated DG poly-Si NWFET sensing devices (a) without and (b) with 2-hr NH_3 plasma treatment.

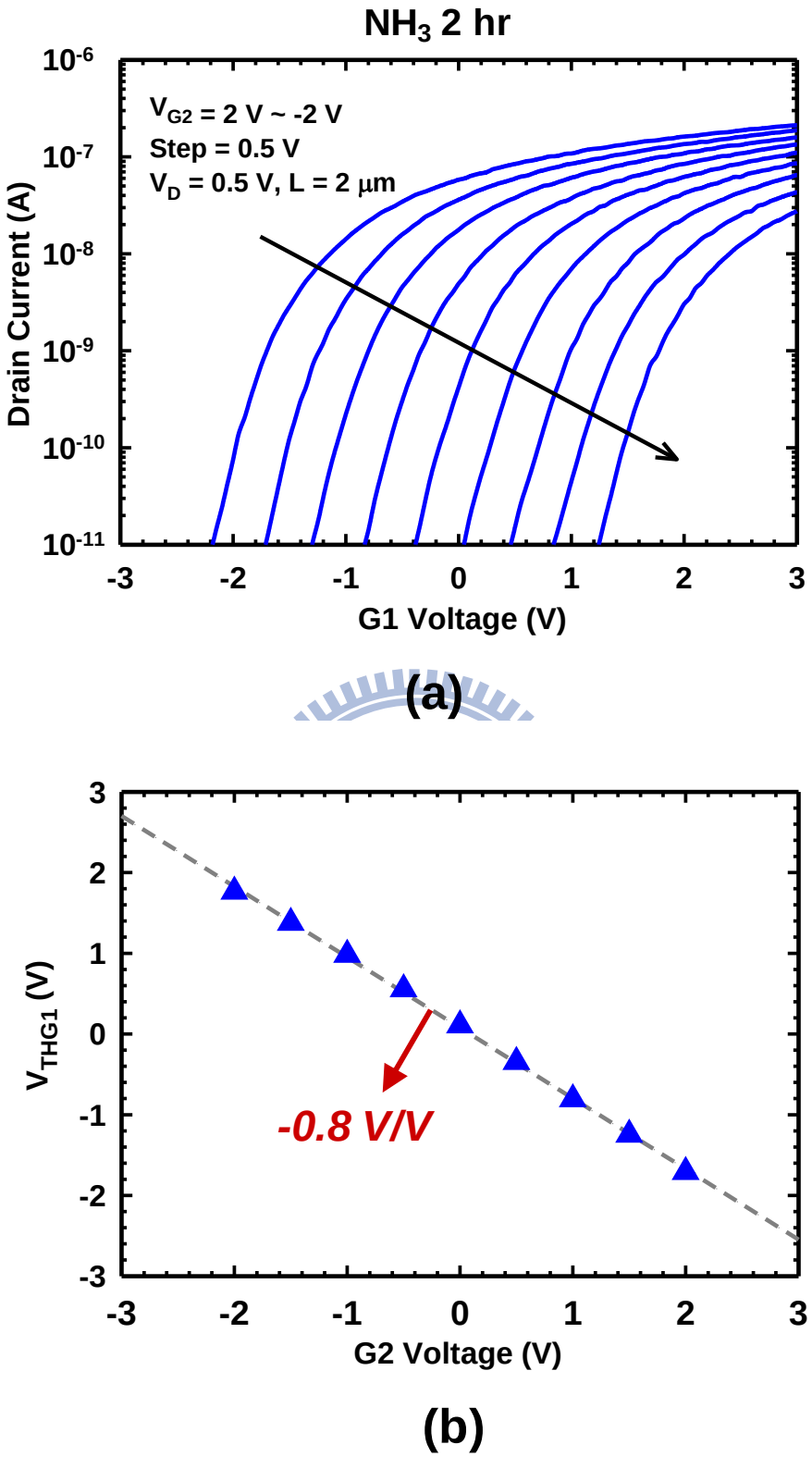


Fig. 5-11 (a) I_D-V_G characteristics of the DG poly-Si NWFET sensing device under SG1 mode with G2 bias ranging from -2 V to 2 V. (b) V_{THG1} as a function of V_{G2} extracted from Fig. 5-11(a).

Site-Binding Model

$$A\text{-}OH \xleftrightarrow{Ka} A\text{-}O^{-} + H^{+} \qquad A\text{-}OH_2^{+} \xleftrightarrow{Kb} A\text{-}OH + H^{+}$$

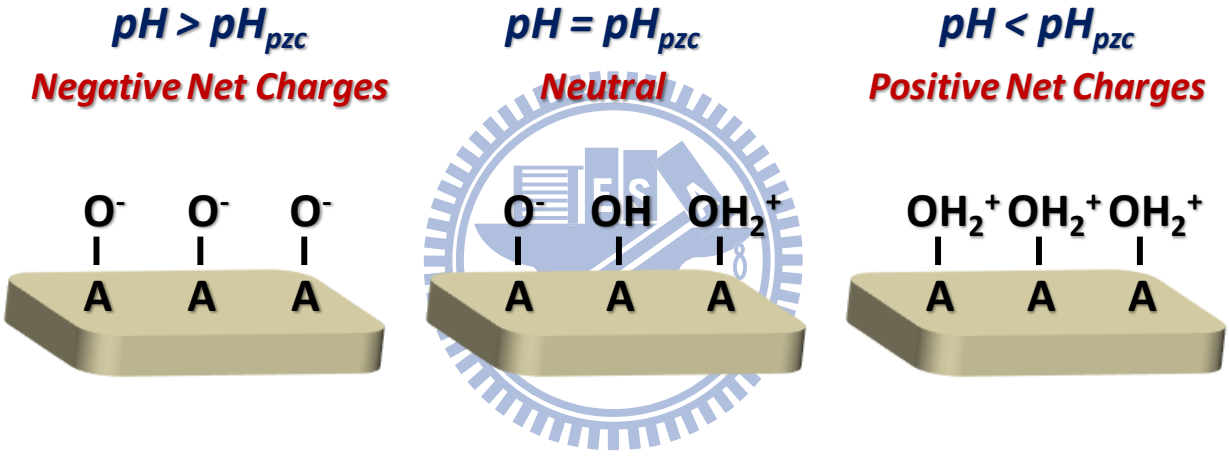
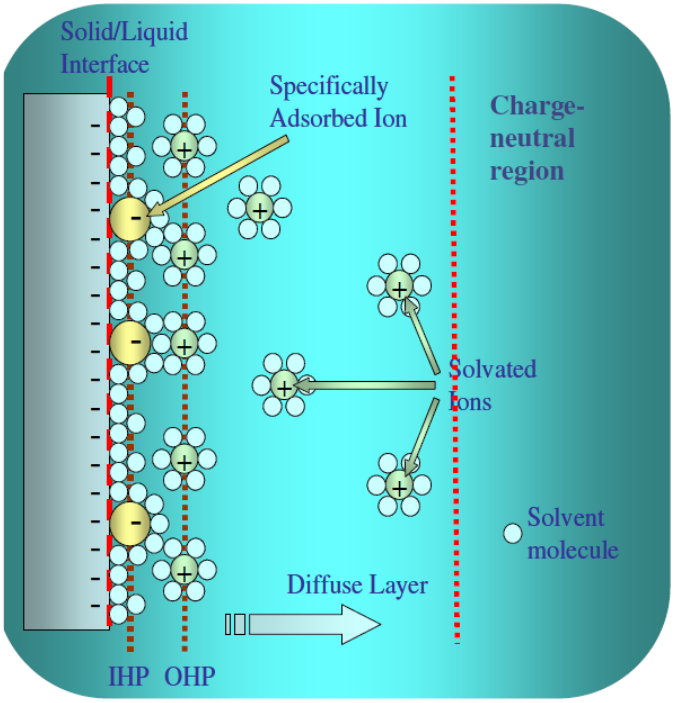


Fig. 5-12 Schematic representation of site-binding model showing the binding/dissociating reaction between the binding sites and protons on the sensing surface under different pH values.

Gouy-Chapman-Stern Double Layer Model



OHP: outer Helmholtz plane

Double-layer capacitance

$$\frac{1}{C_{EDL}} = \frac{1}{C_H} + \frac{1}{C_{DIF}}$$

C_H: Helmholtz-plane capacitance

$$C_H = \int_0^{A_{SG}} \left(\frac{\varepsilon_r \varepsilon_0}{x_{OHP}} \right) dA$$

x_{OHP}: dist. between Helmholtz planes

C_{DIF}: Diffuse-layer capacitance

$$C_{DIF} = \int_0^{A_{SG}} \left(\frac{2\varepsilon_r \varepsilon_0 z^2 q^2 n}{kT} \right)^{1/2} \cosh\left(\frac{zq\phi_{OHP}}{2kT} \right) dA$$

z: magnitude of the charge on the ions

n: concentration of the ions

ϕ_{OHP}: potential at the OHP

Fig. 5-13 Schematic representation of Gouy-Chapman-Stern (GCS) double layer model [5.15].

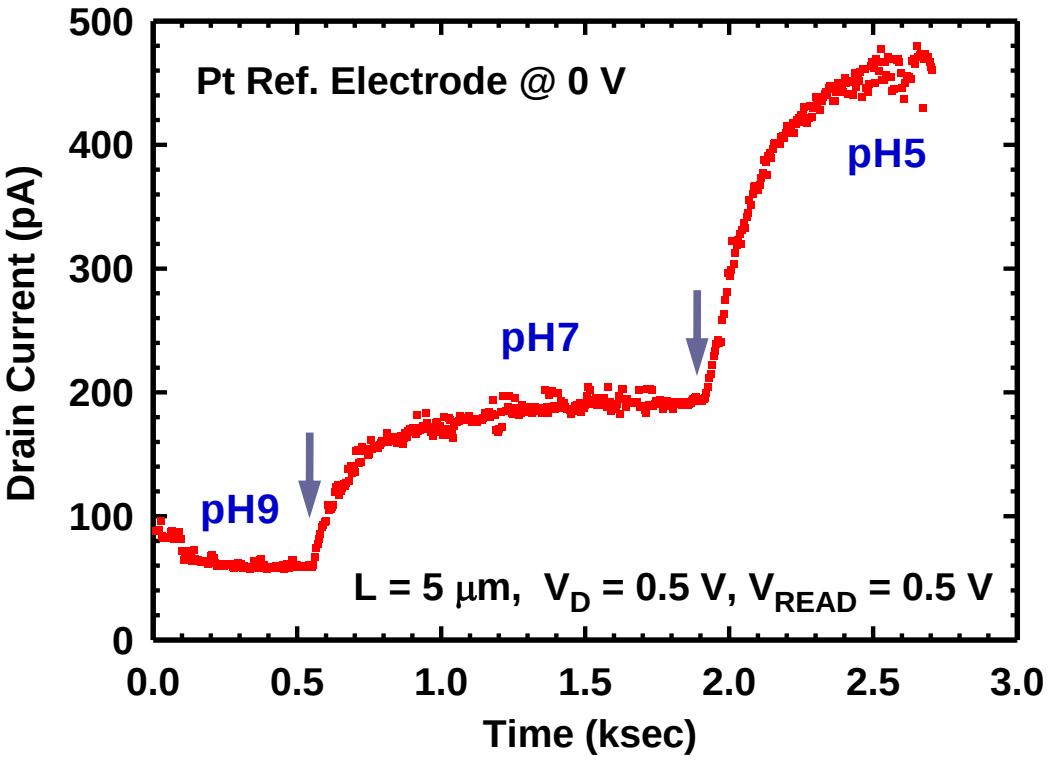
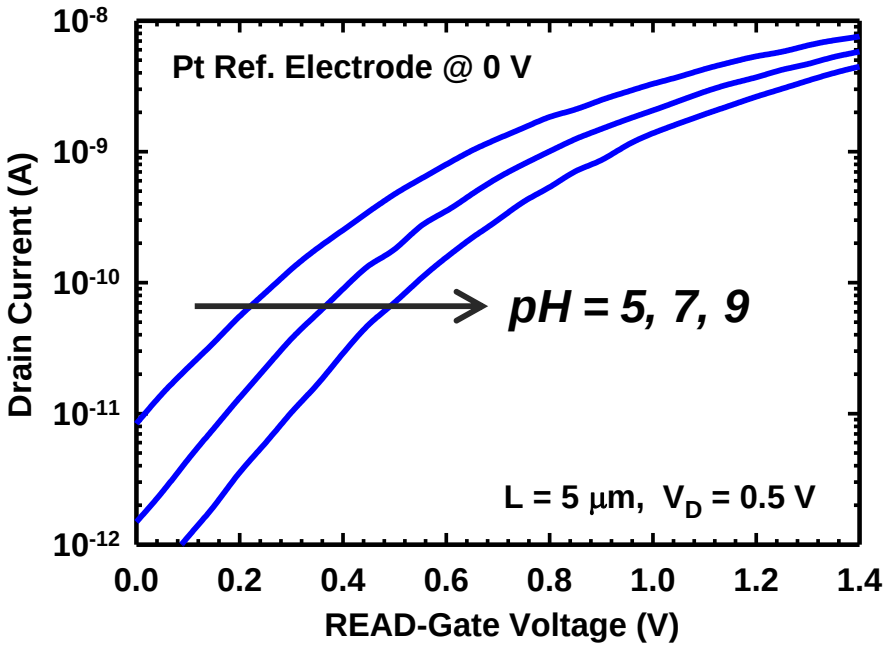
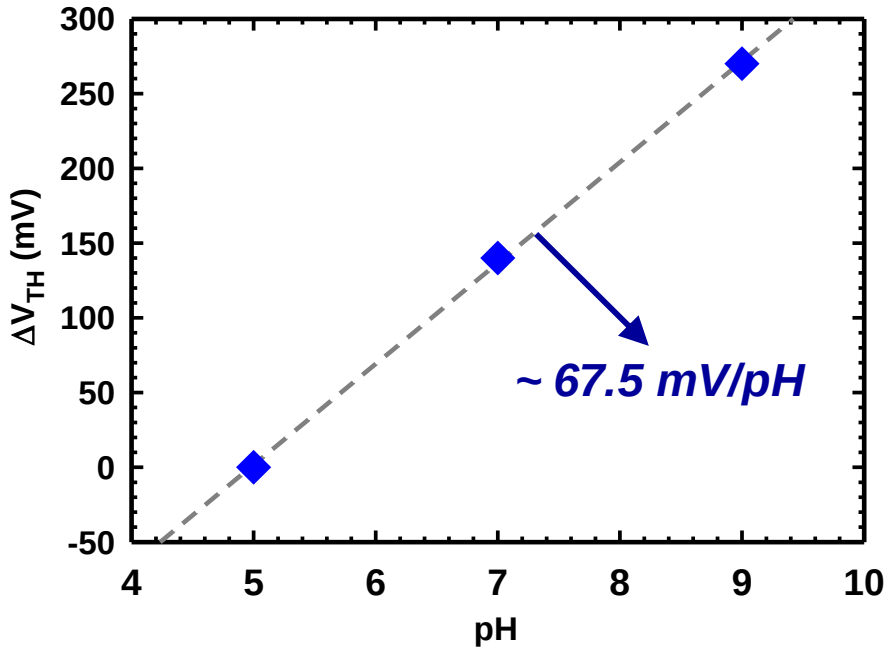


Fig. 5-14 Real-time I_D response of a DG NWFET sensor measured in the test solution with various pH values.



(a)



(b)

Fig. 5-15 (a) Subthreshold characteristics and (b) the corresponding V_{TH} of the DG NWFET sensor at corresponding pH values.

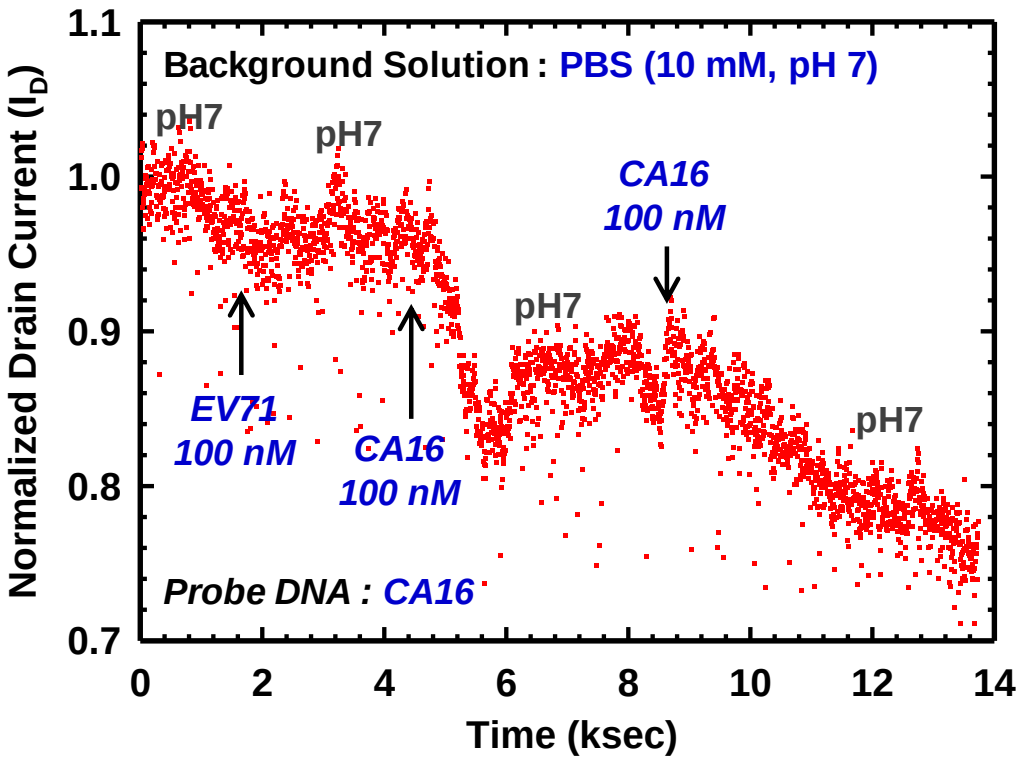


Fig. 5-16 Real-time biosensing characteristics of the DG NWFET sensor with sensing membrane surface modified by CA16 DNA probes.

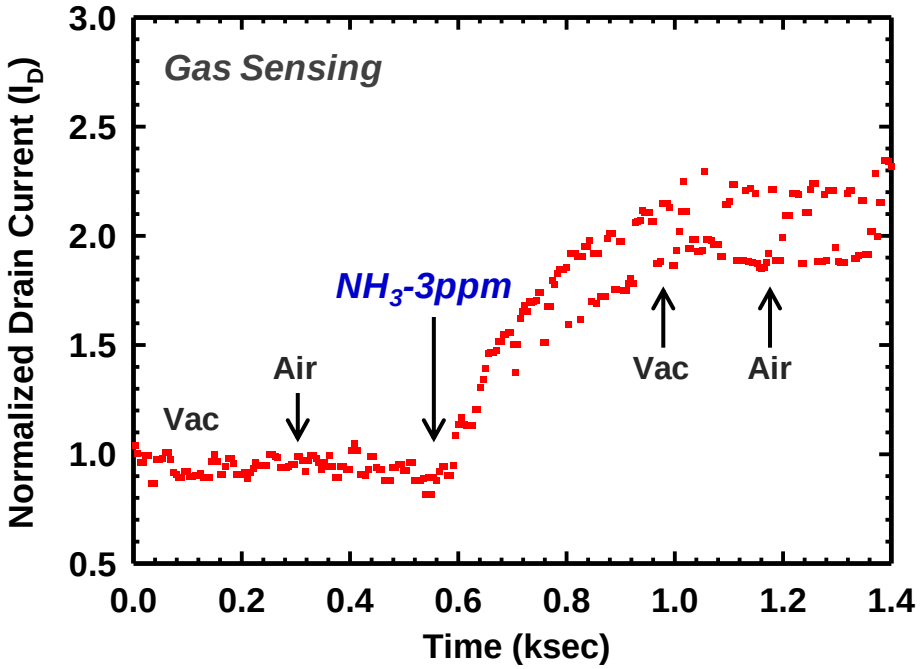


Fig. 5-17 Real-time I_D response measured under various gas conditions in the gas chamber.

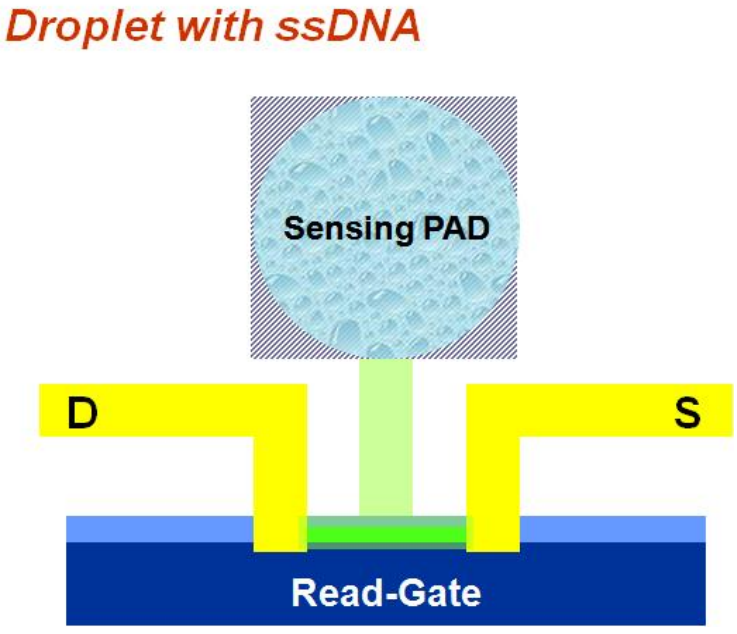


Fig. 5-18 Schematic showing an ssDNA droplet dripped onto the sensing pad of a DG NWFET sensor.

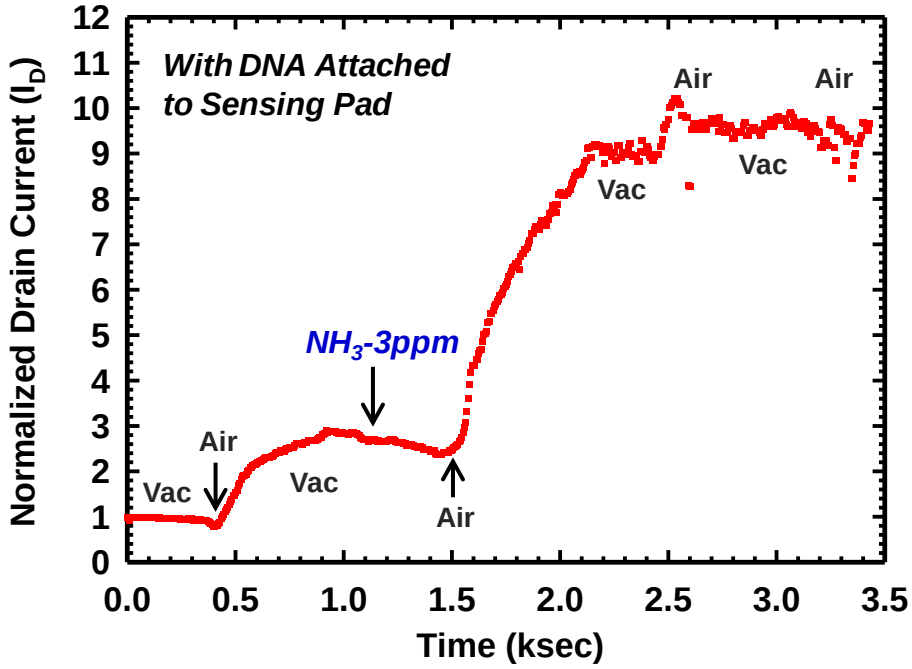


Fig. 5-19 Real-time I_D response to the condition of gas chamber using a sensing device with ssDNA targeting layer.

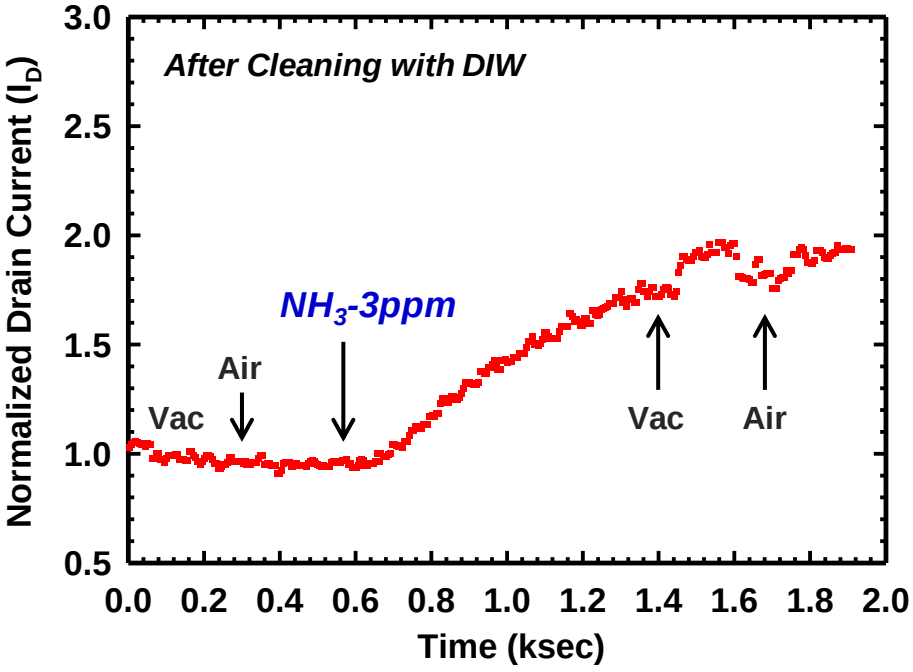


Fig. 5-20 Real-time I_D response to the condition of gas chamber using the device tested in Fig. 5-19 after removing the attached ssDNA by DIW cleaning.

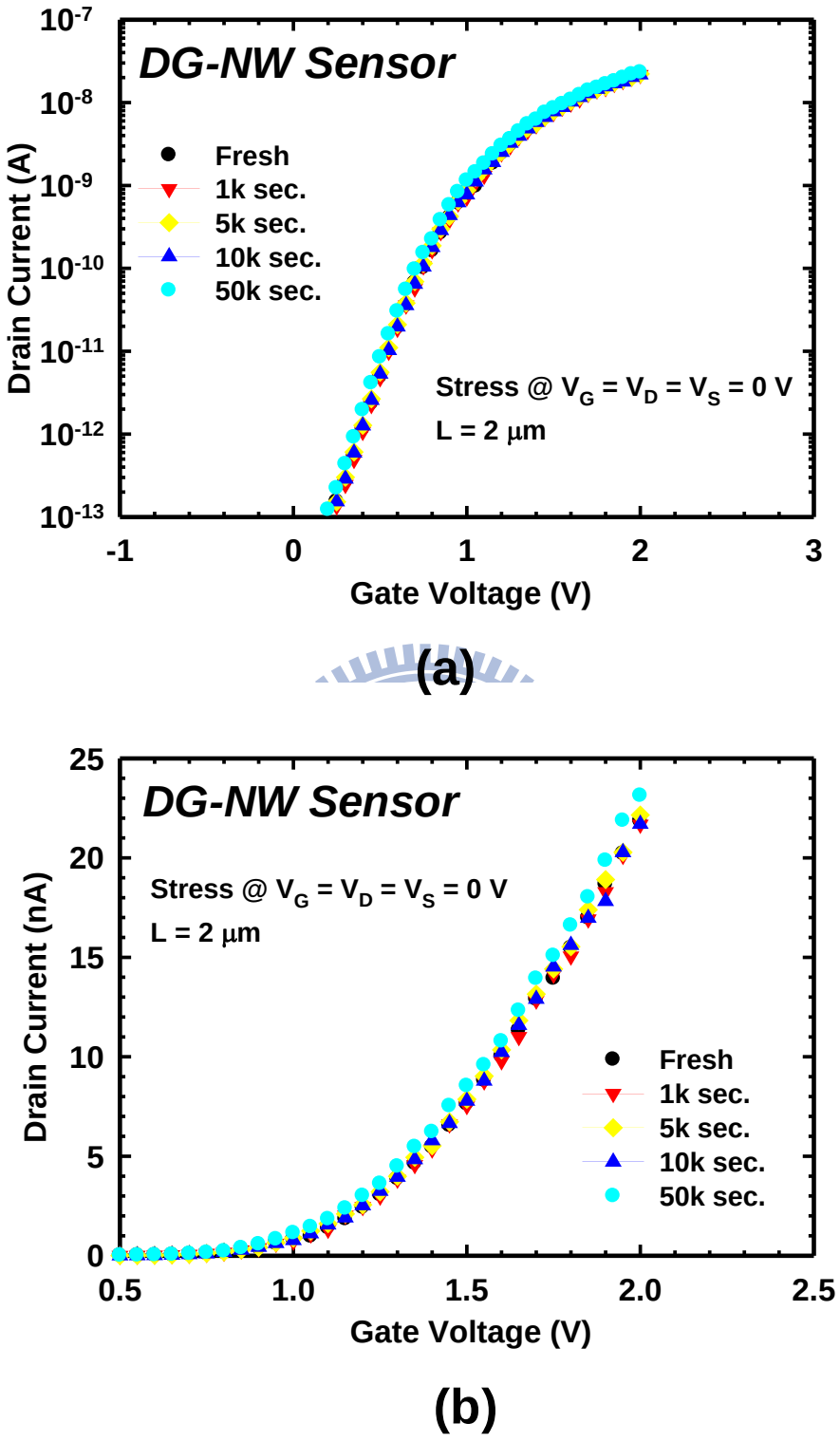


Fig. 5-21 I_D-V_G curves ((a) with I_D in logarithmic scale and (b) with I_D in linear scale) of a DG-NW sensor measured after corresponding stressing time. The stressing tests are performed by immersing the sensing region of the device in PBS (pH = 7) with micro-fluidic channel system and biased at $V_D = V_S = V_G = 0$ V.

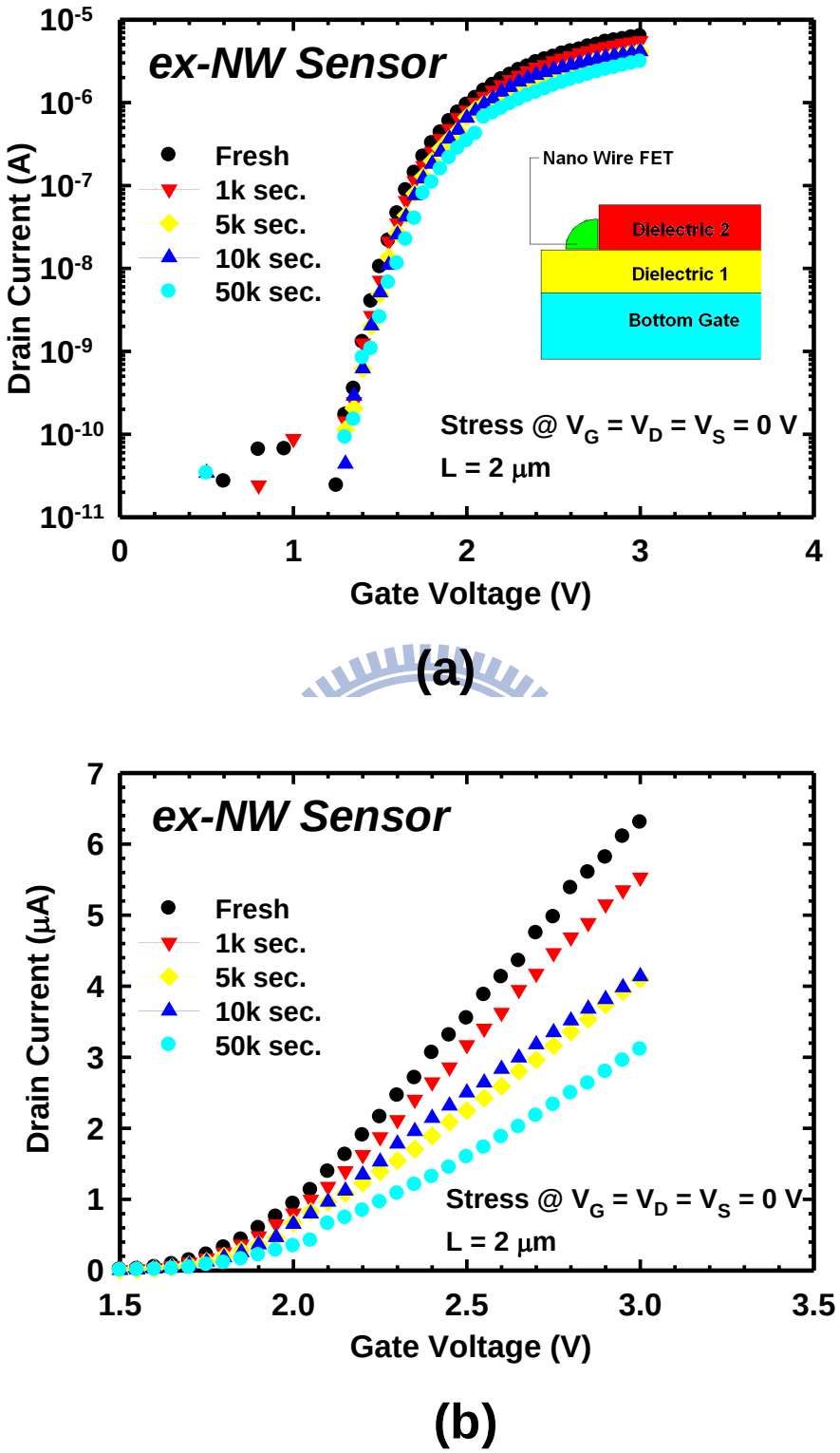


Fig. 5-22 I_D-V_G curves ((a) with I_D in logarithmic scale and (b) with I_D in linear scale) of ex-NW sensor measured after corresponding stressing time.

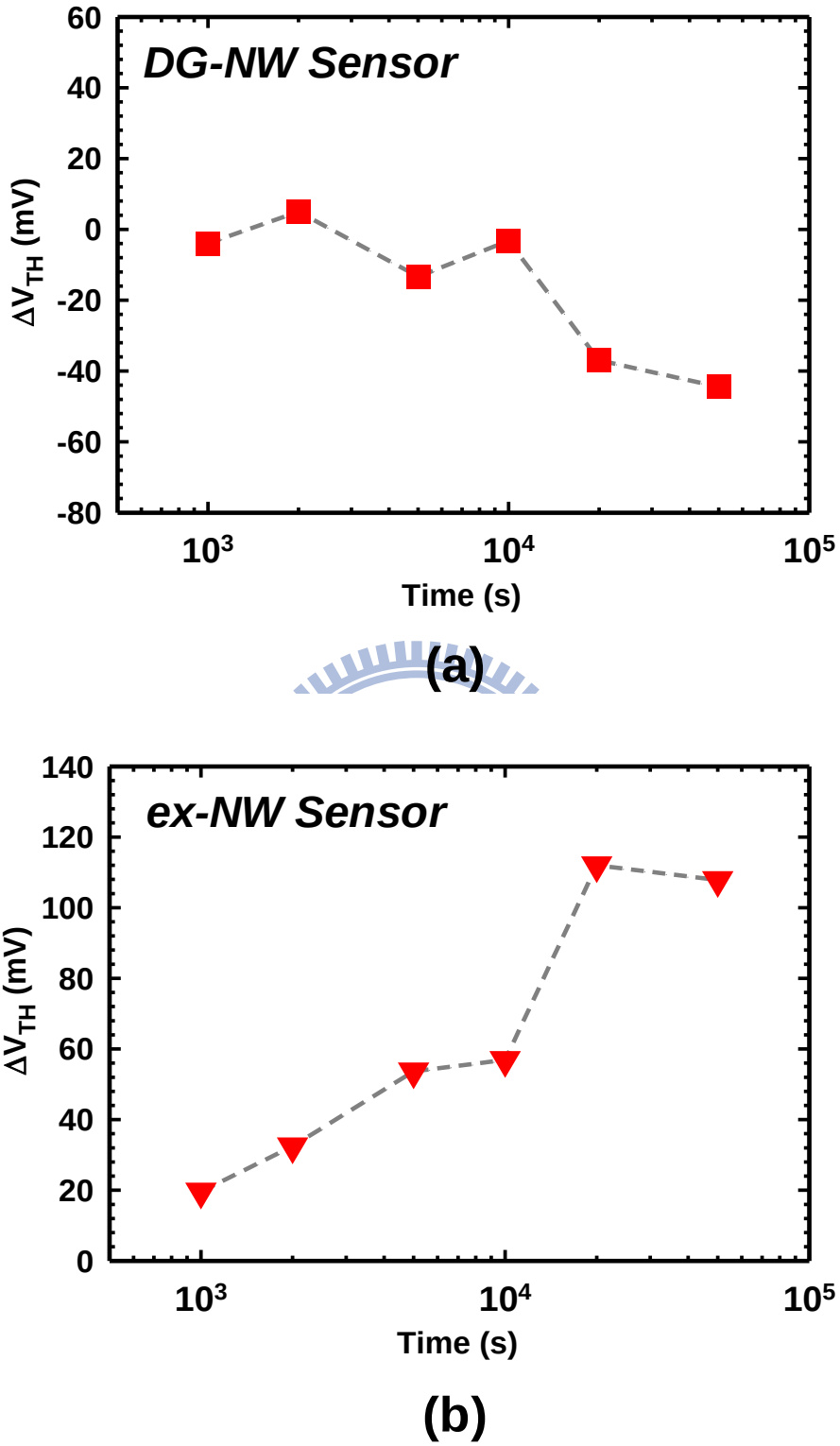


Fig. 5-23 Extracted V_{TH} shift (ΔV_{TH}) of (a) DG-NW sensor and (b) ex-NW sensor as a function of stressing time.

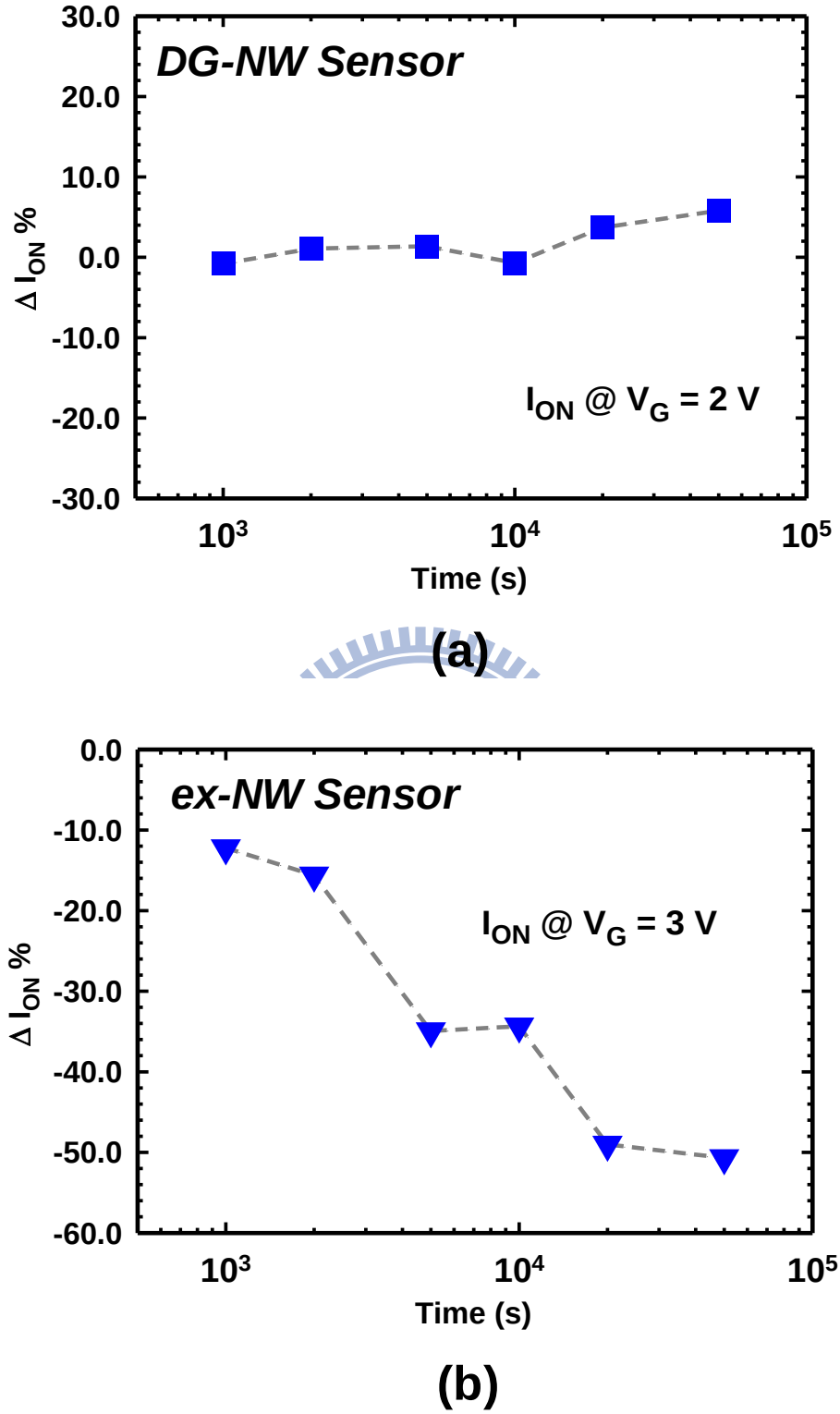


Fig. 5-24 ON-current variation (ΔI_{ON}) of (a) DG-NW sensor and (b) ex-NW sensor as a function of stressing time.

Chapter 6

Conclusions and Future Prospects

6-1 Conclusions

In this dissertation, various simple and low-cost techniques for fabricating multiple-gated (MG) poly-Si NW thin-film transistor (NWTFT) have been proposed and demonstrated. Detailed electrical characteristics and physical phenomena of the devices have also been studied. Experimental results have shown that the proposed MG ploy-Si NWTFT fabrication schemes have potential for being a favorable and economic device platform for several applications such as non-volatile memory (NVM) and bio-sensors.

In Chapter 2, characteristics of poly-Si NW devices featuring an independent DG configuration were characterized and analyzed. In the devices the ultra-thin NW channels fabricated by spacer-etching technique were surrounded by an inverse-T-shaped gate and a top gate. With this independent DG scheme, several modes including DG and two SG modes can be implemented in the device operation. Owing to the strong gate-to-gate coupling with ultra-thin NW channels, the transfer characteristics of the device driven by one of the gates were profoundly affected by the bias condition of the other gate, allowing the flexibility to adjust V_{TH}. In addition, it was found that the device under DG mode manifests significantly better performance in comparison with the two SG modes in terms of a higher drive current

over the combined sum of the two SG modes, and a smaller subthreshold swing (SS) of less than 100 mV/dec. On the other hand, the anomalous leakage current shown in SG1 and DG mode is attributed to GIDL mechanism. A simulation analysis was done for explaining the leakage behavior, showing that BTBT occurs more considerably in the drain region with lower doping concentration. Extraordinary enhancement in the current drive with DG mode was also observed and was found to be mainly because of the elimination of the back-gate effect encountered in SG mode, as well as the improved effective mobility.

Besides, the impacts of operation mode on device's series resistance were also investigated in Chapter 2. The results indicated that the spreading resistance of the device could be reduced by grain-boundary barrier lowering effect, leading to a lower series resistance under DG mode. For device variability, it was confirmed that defects contained in the channel is the dominant source for the fluctuation observed in NW DG-TFTs. Experimental results in this study also show that these defects can be effectively passivated with NH_3 plasma treatment, therefore reducing the device fluctuation in terms of σV_{TH}. Additionally, it was found that the fluctuation is closely related to the operation modes. When only one of the gates was employed as the driving gate to control the device's switching behavior, suppressing the V_{TH} fluctuation by optimizing the bias to the V_{TH}-control gate under single-gate mode was demonstrated.

In Chapter 3, a novel fabrication technique called cavity formation and filling that enables the fabrication of poly-Si NW without resorting to advanced lithographic tools was proposed, and the effects of multiple-gate configurations on the characteristics of poly-Si NWTFTs were investigated. The tri-gated NWTFT devices fabricated using cavity formation and filling technique exhibited excellent ON/OFF

current ratio higher than 10^8 and steep SS as low as 100 mV/dec. Moreover, a multiple-channel layout scheme was also proposed and demonstrated to multiply the drive current without degrading device performance. Besides, we have also proposed a clever scheme based on cavity formation and filling technique to fabricate three types of poly-Si NWTFTs with different gate configurations but identical NW channels. Such scheme allows us to investigate the impact of multiple-gate configuration on the performance variation of poly-Si NW devices. Our results indicated that the S3 structure, which has the largest portion of the NW channel surface under efficient gate modulation, showed the least fluctuation in SS and V_{TH}. Furthermore, with the increase in channel number of the NWTFT, the device fluctuation was further suppressed.

In Chapter 4, poly-Si NW-SONOS devices with various gate configurations were fabricated with cavity formation and filling technique, and their characteristics including NVM performance were also investigated. As compared with the planar counterpart, the NW devices can be operated with a much reduced P/E voltage which is essential for the demand of green electronics. This is attributed to the enhanced gate controllability with an MG configuration as well as the use of ultra-thin NW structure with a reduced amount of defects in the channel. Among the three types of NW devices, GAA split has shown the best performance in terms of the highest ON-current, the steepest SS, the highest P/E efficiency, the largest memory window, as well as the best endurance and retention characteristics. This is ascribed to the increase in the electric field strength at the NW/tunneling oxide interface resulting from the large curvature as well as the reduced variation in the curvature value. Hence GAA device possesses the most prominent performance among the different types of devices characterized in this chapter. Last but not least, the NW-SONOS fabrication

process used in this chapter can be easily implemented in modern flat-panel manufacturing without resorting to costly advanced lithography. Based on results obtained in this chapter, the proposed method for fabricating MG poly-Si NW-SONOS devices appears to be promising for the realization of system-on-panel (SOP) integration.

In Chapter 5, a novel DG NWFET sensing scheme featuring an extended sensing gate (SENSE-gate) and a READ-gate for various sensing purposes was proposed and fabricated. Results of the preliminary study using this DG NWFET sensor for pH sensing, bio-molecules detection and gas sensing applications were also presented and demonstrated. Due to the effective separation of device from aqueous chemical and biological environment, this novel sensing scheme exhibited more stable and reliable electrical characteristics during the stressing test in aqueous solution as compared with those of NW sensor devices having poly-Si NWs exposed to the ambient. Consequently, this sensing scheme is extremely useful and potential for practical biosensor applications in terms of the high manufacturability, low fabrication cost and improved reliability.

6-2 Future Prospects

Notwithstanding that several perspectives and topics of NWTFTs have been studied in this dissertation, there are still some intriguing prospects regarding further improvement of device performance and optimization for practical applications using proposed NW schemes.

6-2.1 Crystallinity Improvement for Poly-Si NWs

In this dissertation, the poly-Si used for NW channel was prepared by solid-phase crystallization (SPC) technique, which allows forming decent grain size of poly-Si and acceptable electron mobility of around 20 cm^2/Vs ~ 50 cm^2/Vs. Though in the study we've proved that poor electrical behaviors originated from the small-grain poly-Si channel such as small drive current, large SS and OFF-state leakage can be much mitigated by adopting MG NW configuration, various low-temperature poly-Si (LTPS) techniques for improving the crystallinity of poly-Si thin-film have already been proposed and successfully demonstrated, including eximer laser annealing [6.1], metal induced lateral crystallization (MILC) [6.2] and sequential lateral solidification (SLS) [6.3]. In one of our previous works [6.4], a single side-gated poly-Si NWTFT using MILC technique to promote the crystallinity was carried out and a dramatically increased field-effect mobility of larger than 250 cm^2/Vs was achieved. Therefore, since these methods are useful for greatly boosting the mobility of poly-Si film by almost an order of magnitude, much enhanced device and circuit performances in terms of higher drive current, larger ON/OFF current ratio and faster switching property are expected by implementing these methods into the proposed MG NWTFT schemes.

6-2.2 Gate Stack Engineering for NW-SONOS Devices

As for NVM application with proposed NWTFTs discussed in Chapter 4, only the conventional SONOS gate stack consisting of a standard ONO dielectric multi-layer and an n^+ poly-Si gate was applied to the NWTFT schemes. To further improve and optimize the programming/erasing (P/E) efficiency of the NW memory devices, replacing the ONO stack and n^+ poly-Si gate electrode with some advanced multi-

layer structures is highly worthy of consideration. As mentioned in Section 1-4, TANOS (TaN/Al_2O_3/Nitride/SiO_2/Si) structure [6.5] and band-gap engineered SONOS (BE-SONOS) [6.6] are the two most promising gate stack solutions for the charge-trap flash (CTF) below the 20 nm technology node. Owing to the use of high-κ Al_2O_3 blocking layer, the resultant higher gate voltage coupling ratio for TANOS NVM allows enhanced electric field in tunneling oxide, thereby facilitating carrier tunneling under P/E operation while maintaining adequate retention characteristics. Moreover, the high-work-function TaN gate is used to suppress gate-injection current during erase operation, leading to a better erasing efficiency. For BE-SONOS, the band-gap engineered ultra-thin ONO tunneling layer is able to provide thick enough energy barrier to repress direct tunneling during retention. While the tunneling barrier becomes ultrathin due to a suitable band offset at high electric field under erasing operation, allowing efficient hole direct tunneling to reach fast erasing. Consequently, by taking advantages of these advanced gate-stack structures, the proposed GAA NW NVM scheme could achieve even more preferable performance, greatly promoting the potential of being practically used in future NVM applications.

6-2.3 Three-Dimensional Integration for Poly-Si NWTFTs and NVMs

As described in Chapter 1, one of the most effective ways to increase the density of device in a chip is to stack device (active) layers in third (*i.e.*, vertical) dimension. Since the proposed poly-Si NWTFT schemes possess merits of low temperature fabrication process, it is interesting and of importance to design a feasible scheme for vertically stacking the NW devices into 3-D configuration, thereby increasing device density without aggressive scaling of device dimensions. In addition,

for the purpose of achieving system-on-chip (SOC) or system-on-panel (SOP) [6.7, 6.8], it is also worthy of integrating the NVMs and logic devices onto the same chip using the proposed poly-Si NWTFT and NVM schemes.

6-2.4 Optimization of NWFET Sensing Devices

Since only preliminary experimental results of the proposed NWFET sensing scheme are presented in Chapter 5, this scheme still has some issues in several aspects that need to be optimized in order to reach more desirable performance for different sensing applications. The optimizations could be categorized into two different perspectives, one is structural/material modifications of the sensing device, and the other one is sensing measurement improvement with more advanced measuring system or methods. For structural/material modification, one is to optimize the structural parameters, especially the gate oxide thickness for SENSE-gate and READ-gate as well as NW channel thickness, which should be designed properly considering the coupling effect between the two gates to realize effective amplification of the sensed signal. Other modifications such as changing the material composition of the sensing membrane, surface plasma treatment and post dielectric annealing (PDA) are supposed to be helpful for improving the sensitivity of the sensing membrane. For sensing measurement improvement, the differential measurement method (*e.g.*, real-time conductance) using AC input signal and lock-in amplifier is capable of reducing the environmental noise [6.9]. Furthermore, superimposing a high-frequency voltage onto the reference electrode has also been demonstrated to effectively shorten the stabilizing time of the sensed output signal (*e.g.*, I_D or GM) [6.10].

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新穎多閘極多晶矽奈米線薄膜電晶體之研製與其應用

Fabrication and Analysis of Novel Multiple-Gated Poly-Si Nanowire Thin-Film Transistors and Their Applications

Publication List

A. Journal Papers

1. C. J. Su, H. C. Lin, H. H. Tsai, **H. H. Hsu**, T. M. Wang, T. Y. Huang and W. X. Ni, "Operations of Poly-Si Nanowire Thin-Film Transistors with Multiple-Gated Configuration," *Nanotechnology, vol. 18, 215205 (2007).*

2. **Hsing-Hui Hsu**, Ta-Wei Liu, Leng Chan, Chuan-Ding Lin, Tiao-Yuan Huang and Horng-Chih Lin, "Fabrication and Characterization of Multiple-Gated Poly-Si Nanowire Thin-Film Transistors and Impacts of Multiple-Gate Structures on Device Fluctuations," *IEEE Trans. Electron Devices, vol. 55, pp.3063-3069 (2008).*

3. Horng-Chih Lin, Cheng-Hsiung Hung, Wei-Chen Chen, Zer-Ming Lin, **Hsing-Hui Hsu**, and Tiao-Yuan Huang, "Origin of Hysteresis in Current-Voltage Characteristics of Polycrystalline Silicon Thin-Film Transistors," *J. Appl. Phys., vol. 105, 054502 (2009).*

4. Horng-Chih Lin, Ta-Wei Liu, **Hsing-Hui Hsu**, Chuan-Ding Lin and Tiao-Yuan Huang, "Tri-Gated Poly-Si Nanowire SONOS Devices for Flat-Panel Applications," *IEEE Trans. Nanotechology, vol. 9, pp.386-391 (2010).*

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B. Letter Papers

1. Horng-Chih Lin, **Hsing-Hui Hsu**, Chun-Jung Su, and Tiao-Yuan Huang, "A

Novel Multiple-Gate Polycrystalline Silicon Nanowire Transistor Featuring an Inverse-T Gate," *IEEE Electron Device Letts., vol. 29, pp.718-720 (2008).*

2. **Hsing-Hui Hsu**, Horng-Chih Lin, Leng Chan, and Tiao-Yuan Huang, "Threshold-Voltage Fluctuation of Double-Gated Poly-Si Nanowire Field-Effect Transistor," *IEEE Electron Device Letts., vol. 30, pp.243-245 (2009).*

C. Conference Papers

1. **H. H. Hsu**, H. C. Lin, J. F. Huang and C. J. Su, "Poly-Si Nanowire Thin-Film Transistors with Inverse-T Gate," *Int'l Conf. Solid State Devices and Materials (SSDM), pp.818-819 (2007).*

2. **H. H. Hsu**, H. C. Lin, J. F. Huang and T. Y. Huang, "A novel poly-Si nanowire TFT for nonvolatile memory applications," *IEEE Int'l Workshop on Memory Technology, Design and Testing (MTDT), pp. 55-56 (2007).*

3. K. H. Lee, H. C. Lin, **H. H. Hsu**, T. Y. Huang, "Impacts of NH_3 Plasma Treatment on Double-Gated Poly-Si Nanowire Thin-Film Transistors," *IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), pp.125-128 (2007).*

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5. **Hsing-Hui Hsu**, Horng-Chih Lin, Tiao-Yuan Huang, "Tri-gate poly-Si thin-film transistor with nanowire channels," *IEEE Silicon Nanoelectronics Workshop, pp.1-2 (2008).*

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9. Chia-Hao Kuo, Horng-Chih Lin, Guan-Jang Li, **Hsing-Hui Hsu**, Chun-Jung Su, and Tiao-Yuan Huang, "A Novel Thin-Film Transistor with Suspended Nanowire Channels and Side-Gated Configuration," *Int'l Conf. Solid State Devices and Materials (SSDM) (2009).*

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14. Chia-Hao Kuo, Chia-Wei Hsu, **Hsing-Hui Hsu**, Horng-Chih Lin, and Tiao-Yuan Huang, "Impacts of Gap Thickness Scaling on Thin-Film Transistors with Suspended Nanowire Channels," *IEEE Int'l Symp. VLSI-TSA, pp.1-2 (2011).*

D. Patents

1. H. C. Lin, C. J. Su, **H. H. Hsu**, "具有奈米線通道之非揮發性記憶體元件及其製造方法 (Nonvolatile Memory Device with Nanowire Channel and Method for Fabricating the same)," Patent No. TWI339879, US7723789.

2. H. C. Lin, C. J. Su, **H. H. Hsu**, G. J. Lee, "具懸浮式奈米通道之電晶體結構與其製造方法 (Suspended Nanochannel Transistor Structure and Method for Fabricating the same)," Patent No. US7977755, Publication No. TW201017769, Japan patents, pending.

3. H. C. Lin, **H. H. Hsu**, "奈米線電晶體感測元件," Publication No. TW201121047, USA and Japan patents, pending.