國立交通大學

電機與控制工程學系

碩 士 論 文

應用於膽固醇液晶顯示器之單電感雙極性正負高壓
輸出直流直流電源轉換器
Single Inductor Dual/Bipolar High Voltage Outputs
DC-DC Converter Applicable to Cholesteric Liquid
Crystal Display

研究生：范銘彥

指導教授：陳科宏 博士

中 華 民 國 一 百 年 八 月

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研 究 生：范銘彥　　　　Student：Ming-Yan Fan

指導教授：陳科宏　　　　Advisor：Ke-Horng Chen

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國立交通大學電控工程研究所碩士班

摘　　　　要

　　電子設備如今不只是被工作所需要，因應娛樂與互動式介面需求，或是靜態低消耗功率的電子閱讀器被消費市場所重視且快速發展。需要擁有長時間使用與待機的電子閱讀器，類紙式閱讀器中的膽固醇液晶顯示器，有別於市面上常見液晶顯示器，具有雙穩態特性，能夠在不更新閱讀器頁面之時穩定呈現。因此，為了有效使用有限的電池能量，電源管理系統為晶片系統中非常重要的一環。故本文提出一個運用於切換式電源轉換器的技術，以期在此切換式電源轉換器的電路中提供穩定之正負電壓驅動膽固醇液晶顯示器。

　　本論文所提出的內容，是運用單一輸入與單一外部電感，產生雙極性正負高壓輸出之直流直流電源轉換器。多組輸出電壓解決傳統切換式升壓電源轉換器所需較多外部元件，耗費面積的問題；以及解決傳統電荷幫浦電路低驅動能力與低效率之原有結構的缺陷。本系統亦使用多路複用技術，在單一周期即完成輸出電壓所需能量。

　　另外提出毋需外部幫助而自我偏壓之電荷幫浦電路，提供驅動訊號以幫助上述之單電感正負輸入之切換式電源轉換器，也具備較低驅動能力之多組電壓輸出以提供液晶顯示器灰階顯示。

　　本論文所提出的方法運用於電流模式直流/直流升壓正負電壓轉換器上，並用台灣積體電路公司點二五微米製程來實現。實驗結果顯示本論文的方法可在不增加太多額外的外部元件的前提下，提供多組正負電壓輸出以驅動膽固醇液晶顯示器。

Single Inductor Dual/Bipolar High Voltage Outputs DC-DC Converter Applicable to Cholesteric Liquid Crystal Display

Student：Ming-Yan Fan   Advisor： Dr. Ke-Horng Chen

Department of Electrical and Control Engineering
National Chiao-Tung University

ABSTRACT

In this thesis, a single inductor dual/bipolar high voltage outputs technique is proposed to generate dual outputs to provide driving capability of cholesteric liquid crystal display. Accompany with slope compensation and system compensation, two channel dc-dc converter with positive and negative high voltages can be proved stable. By this technique, it largely reduces area occupation comparing with boost converter producing multiple outputs and resolves the difficulty of efficiency and driving ability in charge pumping supplying system. Besides, the technique uses its unique property and makes it possible to integrate controller and energy delivery elements facing high voltages inside one chip. In addition, the concept of fully balanced self bias switching capacitor structure is proposed to offer specific driver for single inductor structure, and to generate multiple outputs with lower driving ability to apply to gray level implementation, which provides extra two functions to compensate the drawback of lower efficiency in its born defects. The test chip was fabricated by TSMC 0.25μm BCD process, and experimental results show the verification of maximum up to nearly 7V in positive channel and minimum down to near -20V in negative channel.

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　　僅以此論文獻給我愛的人及愛我的人，家人們、同學們、朋友們和所有關心我的人。因為有你們，使本論文豐富不少，謝謝你們。

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銘彥　于　處暑

國立交通大學

中華民國一百年八月

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Chapter 1

Introduction to Cholesteric Liquid Crystal Display(Ch LCD) and Driving System

1.1 Introduction to Paper-Like Display

In the past, the invention of computer helps people with job requiring detailed computation, and trivial file processing in the office, which seems to be the specific roles of handing serious and tough work. Nowadays the popularity of internet and electronic facilities, people can search faster and get more information. Additional, considering the various requirements such as entertainment and interactive interface with people, electronic facilities are not only the demands from job, but also attached importance to consumer market such as personal digital assistant (PDA), full-motioned video and animation, or static, low power consuming electronic reader. In other words, electronic and information facilities combine work, entertainment and out life, which become the most indispensable part.

Regarding to the requirement of multi-function of electronic facilities, displays, which have directly interaction with eyes, need to coordinate with vision states, and should act corresponding to the change of vision angle, light or environment indoors and outdoors. Recently many corporations and research centers devote to the development of displays. As shown in Fig. 1 [1], followings are the principles of electronic displays: Transmissive displays

work by modulating a source of light, such as a backlight, using an optically active material such as a liquid-crystal mixture. Reflective displays work by modulating ambient light entering the display and reflecting it off of a mirror-like surface. Emissive displays such as OLEDs make use of organic materials to generate light when exposed to a current source.
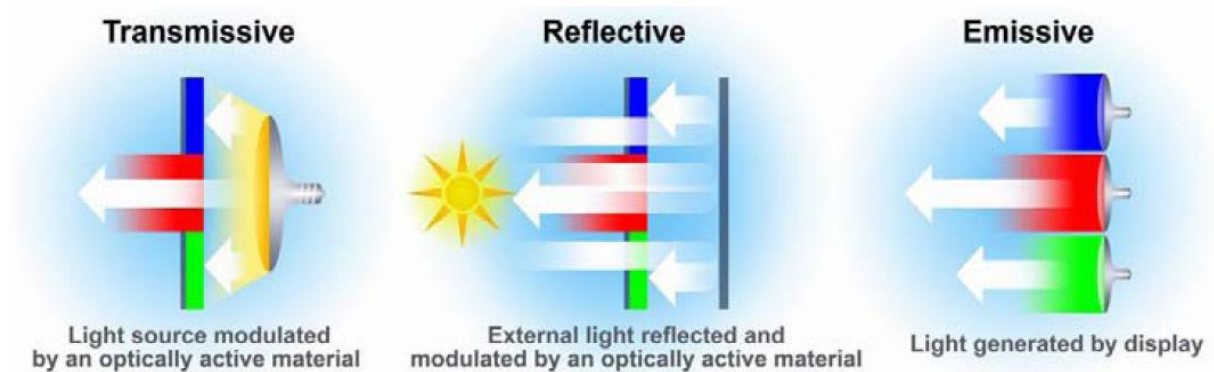
Fig. 2. Primary Approaches to Electronic Displays.

From last paragraph, we know the paper-like reading displays [2] developed continuously by various companies and research units to overcome the difficulty in reading when facing the change of light outdoors and indoors, moreover, to achieve power conservation and substrate material saving to coincide with the concept of environment protection. Additionally, improvement of readability and transient response time would be expected to consumer market.

Portable paper-like reading displays [2] have various types: Electrophoresis Displays, known as EPD, take use of colorful charged balls to have black and white appearance using external electric field. Electrochromic Displays, known as ECD, use the discoloration material caused by electricity to change the oxidation/reduction states and light absorption spectrum. Twisting Ball Displays, known as TBD, present dark and bright states using a small ball accompanied with dark/bright and different electric properties when external electric field activates. Cholesteric Liquid Crystal Displays, known as Ch-LCD, use the

cholesteric-structure liquid crystal and characteristic of bi-stable to maintain in brightness and darkness.

Take comparison of four display technology above, this thesis would focus on Ch-LCD which has bi-stable, high contrast ratio and high color appearance.

1.2 Background of Cholesteric Liquid Crystal

Shown in Fig. 2 [3], cholesteric liquid crystal (Ch-LCD), means liquid crystals have similar structure compared with cholesteric spiral structure which can be changed by electricity to present black and white. As shown in Fig. 3 [4], the electricity cross the electrode of display panel would change states of Cholesteric liquid crystal. There're two stable states in Ch-LCD. One is planar texture state, the other one is focal conic texture.
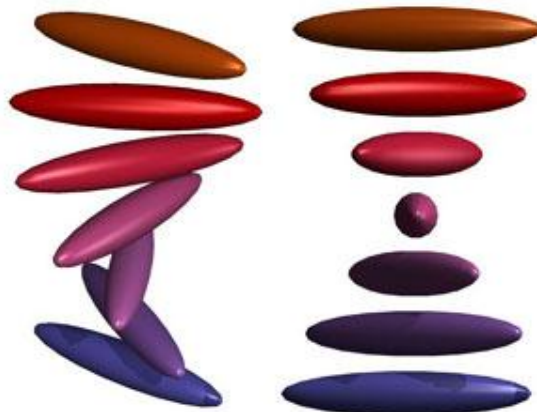
Fig. 3. Structure of Single Cholesteric Liquid Crystal

In the planar state, where the helical axis is perpendicular to the cell surface, the electric field of the incident light is parallel to the liquid crystal director in some regions, and the light is absorbed by the eyes. The focal conic texture has an optical appearance quite

different from that of the planar texture. When the liquid crystal is in the focal conic texture, which is a polydomain structure, with the helical axis more or less parallel to the cell surface, and incident light is either diffracted or scattered in the forward direction. Whenever liquid crystal is in planar state or focal conic, textures are stabilized at zero electricity field. The homeotropic texture, where the helical structure is unwound with the liquid crystal director perpendicular to the cell surface, the electric field of normal incident light is always perpendicular to the liquid crystal director, and the light passes through the material with little absorption. Homeotropic texture, which has to be activated by continuously electricity field different from planar texture and focal conic texture, usually use to act reset state in display.
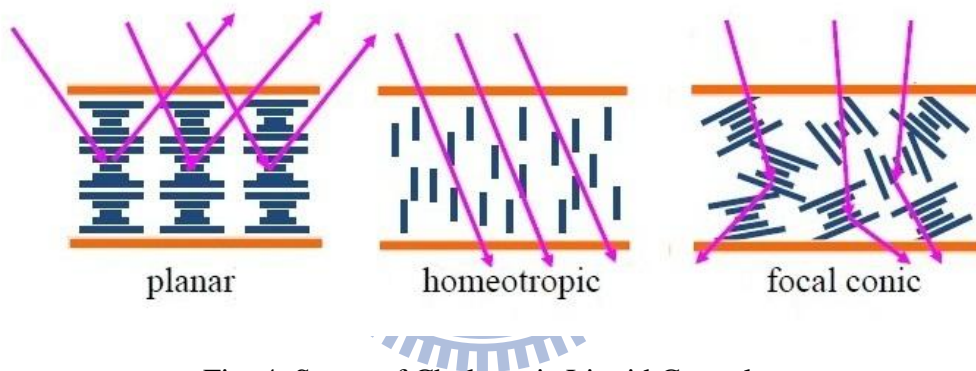
Fig. 4. States of Cholesteric Liquid Crystal

After knowing some basic proper nouns about cholesteric liquid crystal, it's important to have the flow chart of different states transitions which will be related to when and what kind of driving signals should be sent to control the state appearance.

Fig. 4 shows the transitions of cholesteric texture [4] which we can get accompany with the real use of electronic paper (e-paper). When the initial is planar texture state, in which our eyes detect the light reflected by display and interpreted as "bright" or "white", would like to change to "dark" state in the refreshing e-paper, there are two ways to process: one is to operate with a high voltage to enter into homeotropic texture as the reset state, and then a high voltage off slowly to step into focal conic texture; the other one is directly taking use of

a low voltage, but that would cause liquid crystal change slowly.

On the other side, when the initial is focal conic texture state, in which our eyes cannot detect the light reflected by display because of light scattering and diffracting interior of the liquid crystal, and interpreted as "dark" or "black", would like to change to "bright" state in the refreshing e-paper, there is only one way to go: to operate with a high voltage to enter into homeotropic texture and soon after a high voltage off quickly to step into planar texture.
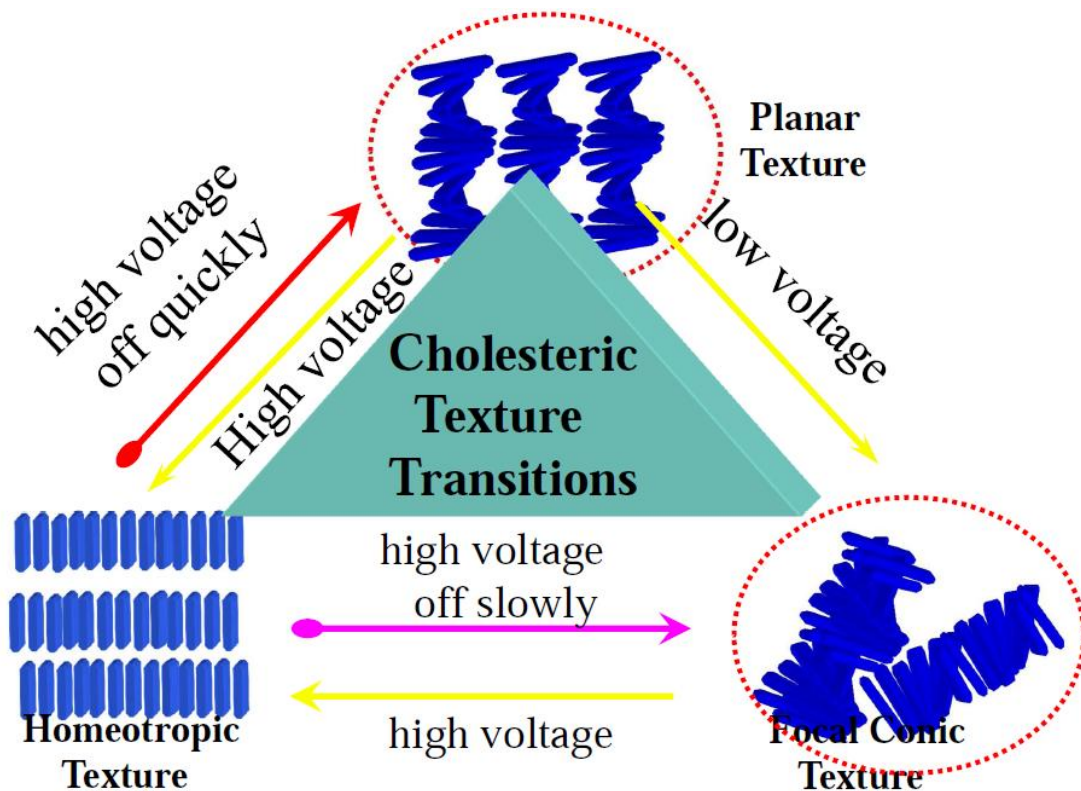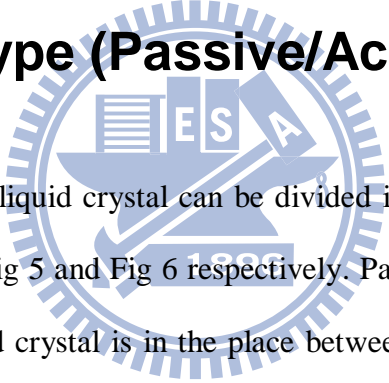
Fig. 5. Cholesteric Texture Transitions

1.3　Driving Knowledge of Cholesteric Liquid Crystal Display

After understanding the development of paper-like display such as cholesteric liquid crystal and its background, the next discussions will focus on the driving knowledge of cholesteric liquid crystal display in order to design corresponding power supply system combining part of driver function. The following paragraphs would be divided into three parts: driving type, driving signal and driving system.

1.3.1 Driving Type (Passive/Active Matrix)

The driving types for liquid crystal can be divided into two parts: passive matrix type and active matrix type in Fig 5 and Fig 6 respectively. Passive matrix type is used in earlier LCD displays, where liquid crystal is in the place between the upper plate and lower plate. Upper and lower plate's material is metal similar which can be controlled by gate driver signals (G1, G2, … Gn) and source driver signals (S1, S2, … Sn) where liquid crystal in each pixel changes states corresponding to different effective voltage levels driving. A pixel in a passive matrix type must maintain its state without active driving circuitry until it can be refreshed again.

Active matrix is a type of flat panel display, currently the overwhelming choice of notebook computer manufacturers. Comparing to passive matrix type, active matrix contains extra TFTs, known as thin film transistor, to act as switches to determine when and where to control states of liquid crystal. This method provides a much brighter, sharper display than a passive matrix of the same size. The addressing approach is to use gate driver (G_1, G_2, …G_n)

to control the TFT switches' timing to decide when and where to change states of each pixel, and source driver (S_1, S_2, …S_n) send signals from front terminals such as timing controller or microprocessor to determine which state exactly in specified pixel. From panel driver and power supplier' point, the advantage of addressing scheme in active matrix is less driving capability of gate driver since controlling TFT switches. On the other side, the drawback is the requirement of extra VCOM driver [5].
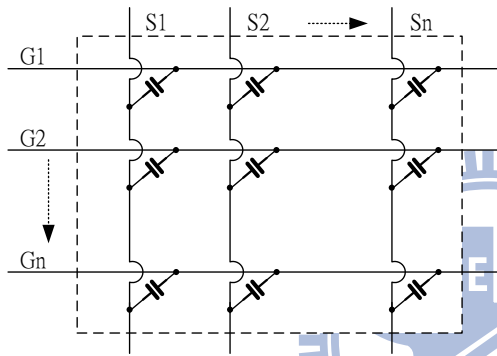
Fig. 6. Passive Matrix Type   Fig. 7. Active Matrix Type
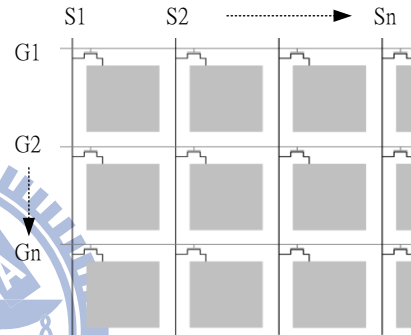
Passive matrix addressed displays such as cholesteric liquid crystal display do not need the switch-component of an active matrix display because it has a built-in bistability. Technology for electronic papers also have a form of bistability which are addressed with passive matrix addressing scheme. In this thesis, we use passive matrix as the cholesteric liquid crystal driving type based on its simple and easier addressing scheme.

1.3.2 Driving Signal

From last paragraph we decide which matrix type used in cholesteric liquid crystal display, and in Fig. 4 we know the brief voltage strength–texture states transitional flow chart. This section is based on the knowledge previous and introduces what types of gate and source driving signals would be applied and then the corresponding states in pixel.

The response of a typical bistable cholesteric liquid crystal reflective display to voltage pulses is shown in Fig. 7 [6]. The voltage pulse width was 40 ms in the condition of cell thickness was 5μ m. Curve a is the response of the material initially in the bright, planar texture and if the voltage pulse is below V_1, the material remains in the planar texture. When the voltage pulse in the region between V_1 and V_2, some liquid crystals remain in the planar texture, and the others are switched to the focal conic texture, which forms so-called "gray level" in the mixture of planar and focal conic texture. The higher the voltage pulse, the more liquid crystals are switched to the focal conic texture, and the lower the reflectance becomes. When voltage is equal to V_2, focal conic texture is acquired, and state goes into completely dark. When voltage is in the region between V_2 and V_3, some are switched to the focal conic texture, and the other are switched to the homeotropic texture during the pulse and relax back to the planar texture after the pulse. The higher the voltage, the more return to the planar texture, and the higher the reflectance becomes. When pulse is higher than V_3, the material is switched to the homeotropic texture during the pulse and relaxes to the planar texture after the pulse.
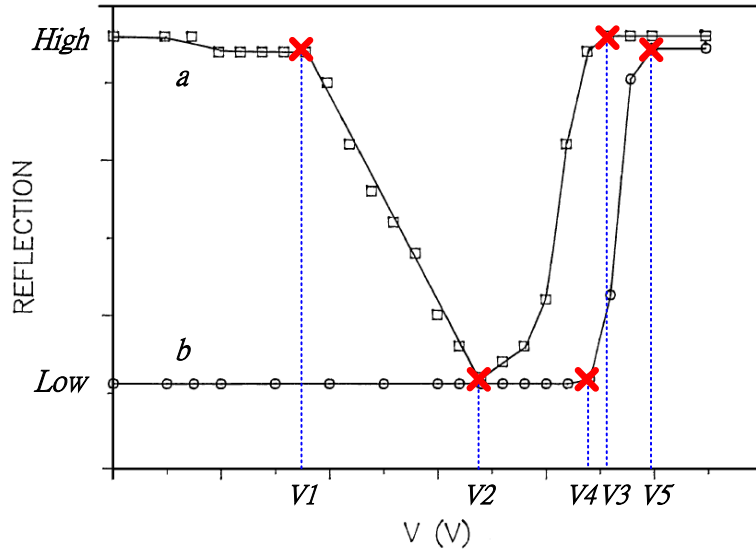
Fig. 8. Response in Bistable Cholesteric Reflective Display to Voltage Pulse.
(a) The material is in the planar texture before the use of voltage pulse.
(b) The material is in the focal conic texture before the use of voltage pulse.

Curve *b* is the response of the material initially in the focal conic texture. When the voltage is below V_4, the voltage pulse doesn't make any effect on liquid crystal and material remains in the dark, focal conic texture. When pulse is between V_4 and V_5, some are switched to the homeotropic texture during the pulse and relax to the planar texture after the pulse, and others remain in the focal conic texture, which forms gray level display. The higher the voltage, the more domains are switched to the planar texture, and the higher the reflectance becomes, in other words, gray level is near to bright image. When the voltage is above V_5, the material is switched to the homeotropic texture during the pulse and relaxes to the planar texture after the pulse.

The response of the material depends on the pulse width. For a shorter pulsing time, all the voltages, from V_1 to V_5, must be shifted to higher values based on the principles of driving liquid crystal whose two terminals rely on charge accumulation. In other words, pulsing time decreases with increasing voltage levels.

In our design, gate driving signals (G_1, G_2, …G_n) and source driving signals (S_1, S_2, …S_n) are specified as following:

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Gate Driving Signals

Select $\qquad G_k = \dfrac{1}{2}(V5 + V2)$ $\qquad\qquad k = 1 \sim n$ $\qquad$ (1)

Non-Select $\quad G_k = 0$ $\qquad\qquad\qquad k = 1 \sim n$ $\qquad$ (2)

Source Driving Signals

Planar $\qquad S_t = -\dfrac{1}{2}(V5 - V2)$ $\qquad\qquad t = 1 \sim n$ $\qquad$ (3)

Focal conic $\quad S_t = +\dfrac{1}{2}(V5 - V2)$ $\qquad\qquad t = 1 \sim n$ $\qquad$ (4)

Gray Level $\quad S_t = +\dfrac{1}{2}(V5 - V2) \sim -\dfrac{1}{2}(V5 - V2)$ $\quad t = 1 \sim n$ $\qquad$ (5)

In Fig. 8(a) and Fig. 8(b), pixels in each row are selected using equation (1), accompany with different source driving signals in equation (3),(4),(5) will generate corresponding effective voltage V_{pixel} across pixel to charge or discharge and then determine which texture state shows up. In Fig. 8(a), pixels are selected to write in data with pulse (black solid line) whose voltage level is equal to equation (1), if source driving signals (blue dash line) are using equation (3) that source and gate driving signals have the opposite polarities, the effective voltage V_{pixel} across pixel, equation (1) minus equation (3), has the equivalence to V_5 which would make liquid crystal planar texture and high reflectance display; when voltage strength in equation (4) is applied to source driving signals in Fig. 8(b), source and gate driving signals have the same polarities, and the effective voltage V_{pixel} across pixel is V_2, much lower than that in Fig. 8(a). In the circumstances, whenever cholesteric liquid crystal is initially in planar or focal conic texture, material has the stability at low reflectance state finally. In the gray level driving condition, whatever voltage level is specified in equation (5) which is in the region between positive polarity in equation (4) and negative polarity in equation (3), V_{pixel} always situates between V_2 and V_5, and the variation of reflectance between

lowest and highest position is observed.

In Fig. 8(c) and Fig. 8(d), pixels in each row are non-selected using equation (2), in which gate driving signals are terminated and pixels are inactivated whatever source driving signals are. In this moment, V_{pixel} in various pixels are always equal or smaller than the absolute value of equation (3) and (4) whose pulse magnitude is designed smaller than V_1 to keep states unchanged. In other words, when $G_k = 0V$, whatever type of source driving signals are, the display remains its appearance since the effective voltage pulse V_{pixel} across pixel smaller than V_1.
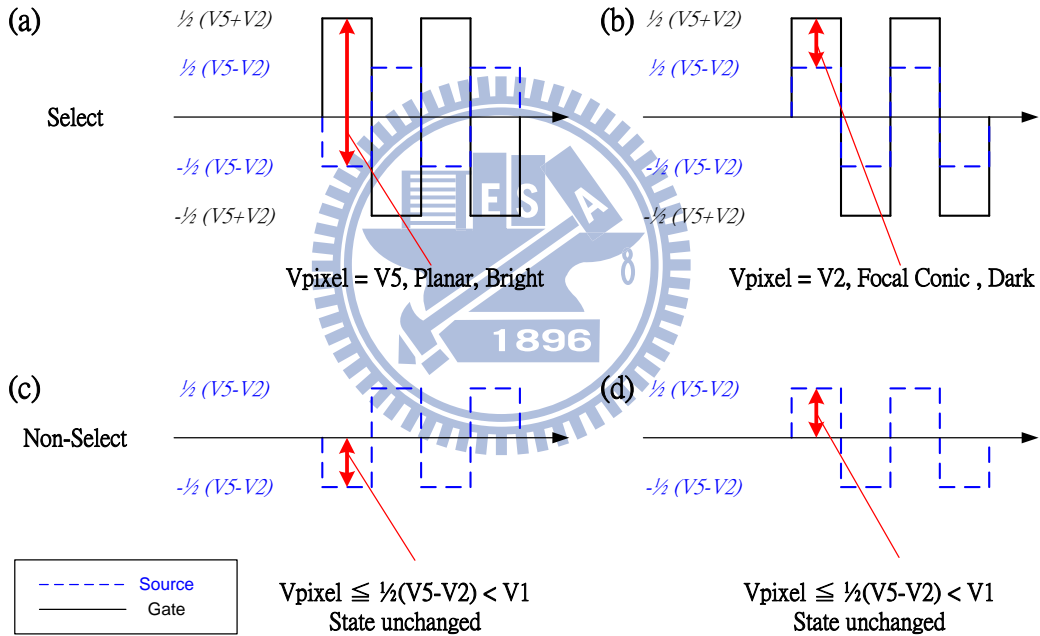
Fig. 9. Pixel States with Various Driving Voltage.

According to the document [7] released from *CHUNGHWA PICTURE TUBES, LTD*, the breaking point voltages (V_i, i= 1, 2, 3, 4, 5) consistent with that in Fig. 7 is 5V, 10V, 27V, 25V and 30V. When regarding the maximum required voltage of gate driving signals in equation (1), half of the addition V_2 to V_5 equaling to 20V is applied. Thus, in the next driving system the uppermost voltage 20V should be generated and take use in pixels driving.

1.3.3 Driving System

After understanding the principle of passive matrix addressing scheme and which type signals are used in gate/source driving, brief block diagram of driving system in Fig. 9 is introduced in this section.

First, *Timing Controller* receives input signals coming from previous stage such as microprocessor or external stimulus. After decoding in *Timing Controller*, X_{clk}, X_{start} and Y_{clk}, Y_{start}, Y_{data}, Y_{latch} send into *Gate* and *Source Driver* separately. X_{start} activates when users want to refresh Ch-LCD panel, and then addressing mechanism starts: G_1 is addressed in the first high enable of X_{clk}, and pixels in Row$_1$ are activated in the meanwhile $G_2 \sim G_n$ are inactivated with 0V driven, and $S_1 \sim S_n$ write data in simultaneously; next G_2 is addressed in the second high enable of X_{clk}, and pixels in Row$_2$ are activated in the meantime $S_1 \sim S_n$ write data in; rows by rows until the last Row$_n$ completes data writing.
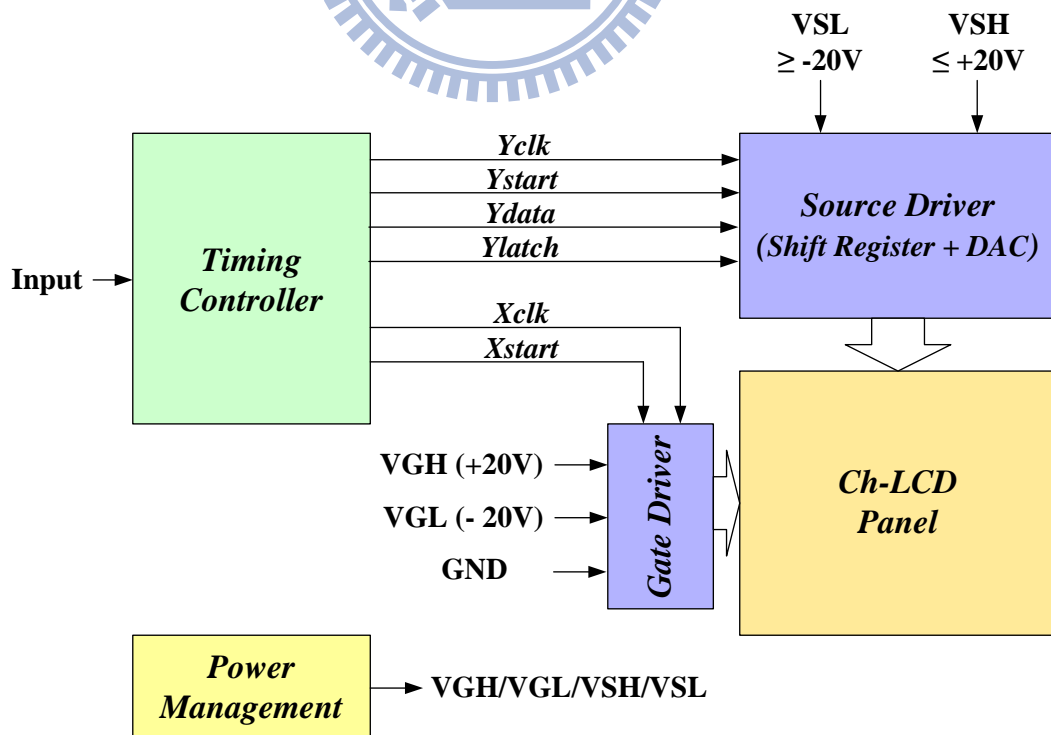
Fig. 9. Brief Block Diagram of Driving System in Cholesteric liquid Crystal Display.

One important thing worthy to notice is that liquid crystal should be driven by AC signals [8] shown as Fig. 8 in order not to accumulate too many charges on the two terminals of electrode to have bad impacts on physical and chemical characteristics, which generates blurred image, lifetime decreasing and unrecoverable damage on liquid crystal. Based on this concept, same magnitude but with opposite polarity voltage pairs are required. In other words, if $VGH = +20V$ is applied to gate driver and unavoidably $VGL = -20V$ is necessary to achieve polarity alteration on liquid crystal.

In *Source Driver* part, after Y_{start} activating, shift register starts to latch Y_{data} in every positive edge of Y_{clk}. By this way, serial data array transforms into parallel array stored in storage register. When data array transformation's done, enable of Y_{latch} would sends all data into *DAC* and buffer to driving pixels at the same time in vertical or column direction. Accompany with gate driver signals (G_1, G_2, …G_n) sent out continuously instead of simultaneously, source driver signals vary with different G_k time slot.

From equation (1), (2) and (3), we know the determination of states in planar texture, focal conic texture and gray level display depends on electrical field strength sent by *Source Driver*. And it can be found that the highest voltage *VSH* and lowest voltage *VSL* required by *Source Driver* are in the region between +20V and -20V, which are the same with *VGH*, *VGL* required by *Gate Driver* generated by *Power Management*. In other words, *Power Management* not only produces typical +20V and -20V, but also multiple voltages inside the range to make cholesteric liquid crystal in various states. Besides, it's necessary to have enough driving capability of *VGH/VGL/VSH/VSL* to satisfy the charging/discharging mechanism and speed. Next part, advantage and drawback in various power sources are discussed and analyzed, furthermore find out the most appropriate solution fit in cholesteric liquid crystal panel driving system.

1.4 Power Source

In this section, we will give a brief introduction to three types of most common regulators, linear regulators, switching capacitor circuits, and Inductor Switching Regulators. Finally, we give a comparison about these three types of regulators.

1.4.1 Linear Regulators

As shown in Fig. 10, the linear regulator [9]-[11] consist of a error amplifier to correct input and output difference, a pass device to supply load current, and a resistive feedback network. The structure is the most compact without complex control circuit, results in smaller chip size and cost. The linear regulator utilizes the feedback network to construct shut negative feedback effect to regulate the output voltage. In this way, this kind of regulator does not need switching clock, so the output noise can be minimized and the output voltage does not exist ripple. Without dual storage components, linear regulator only can be operated in buck operation. The efficiency of linear regulator is about the output voltage dividing input voltage. The highest efficiency occurs that output voltage is near input voltage, i.e. low dropout operation. The supply load ability depends on pass device's size.
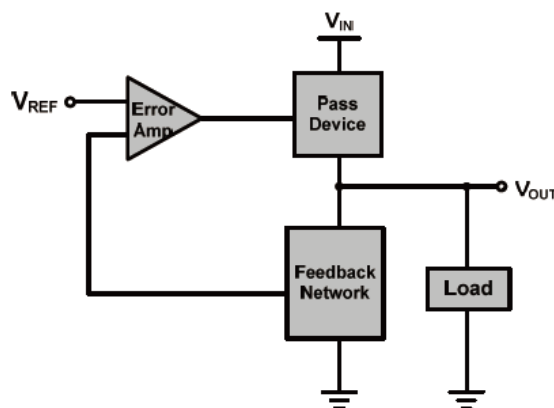
Fig. 10. The Schematic of A Low Drop-Out Linear Regulator.

1.4.2 Switching Capacitor Circuits

As shown in Fig. 11, this is a conventional charge pump converter [12]-[15]. During ψ1 phase, the input voltage charges Cs to input voltage. During ψ2 phase, the output equals to input voltage adding voltage across Cs, and gets twice input voltage. With hysteric feedback control, the output is regulated at desired output voltage. The charge pump can also be operated in buck or boost mode, but the efficiency is higher in boost mode. The control circuit is more compact than switching converters, but more complex than linear regulators. Due to switching clock, charge pump also suffers from EMI and noise problems. But these problems are slighter than switching converters', results from smaller switching frequency in the range of hundreds of Kilo-Hertz. The supply load ability of charge pump is weak, because this depends on capacitor size and switching frequency.
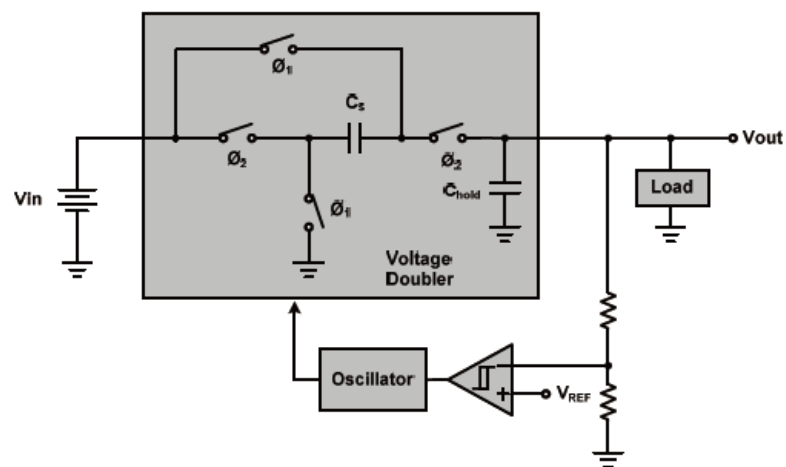
Fig. 11. The Schematic of A Close Loop Switching Capacitor Voltage Doubler.

1.4.3 Inductor Switching Regulators

As shown in Fig. 12, this is a conventional voltage mode switching buck converter [16]-[20]. It compares the output voltage with reference voltage to decide the duty cycle.

When power PMOS conducts, the supply voltage will charge the inductor and capacitor. And in the next time, the power NMOS conducts, so the inductor will be discharged to the capacitor. Due to dual storage components, inductor and capacitor, the switching converter can be operated in buck or boost operation. Generally speaking, the efficiency can be achieved above 90% under heavy load condition. Meanwhile, with higher switching frequency in the range of hundreds of Kilo-Hertz to several Mega-Hertz, the storage components can be designed smaller to save the cost. But the EMI and noise problems become critical. Depended on efficiency requirement, the control circuit is much larger than the other two and the cost is the most. The supply load ability is the largest always in the range about hundreds of milliamps to several amps.
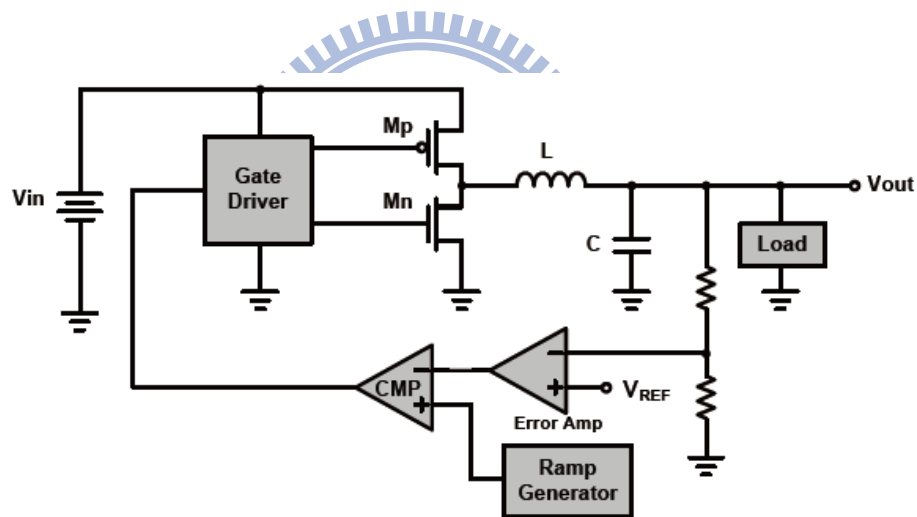
Fig. 12. The Simple Architecture of Buck Converter.

Therefore, the switching regulators can classify into three topologies as functional works. Listed in Table , are buck, boost and flyback converters.

Table I. Three architecture of switching regulators.

	Architecture	Conversion Curve
Buck		
Boost		
Flyback		

The first regulator called as buck converter because its property that step down the input voltage with respect to output node. The conversion ration $M(D)$ is written as $M(D) = D$. The second regulator called as boost converter because its property that step up the input voltage with respect to output node. The conversion ration $M(D)$ is written as $M(D) = \dfrac{1}{1-D}$. The last regulator called as flyback converter also named buck-boost converter because its property that step up or down the input voltage with respect to output node. The conversion ratio $M(D)$ is written as $M(D) = \dfrac{-D}{1-D}$.

There are many advantages of switching regulators to compare with the linear regulators and charge pumps. Switching regulator had high current efficiency because it used power MOSFET as switches and inductor, capacitors as energy stored elements. When the switched

transistor operated in the cutoff region, it had no power dissipation. When the switched transistor operated in triode region, it was nearly a short circuit with little voltage drop across it, and had little power dissipation. Hence, almost power dissipation was spent in output node; high power efficiency could be achieved numerically in the range 80% to 90%.

Switching regulator also had disadvantages. There were more complexity in circuit design than the linear regulators and also required discrete components such as inductor and capacitors. Furthermore, the transition response time and output noise were larger than the linear regulators.

A comparison table between linear regulators, charge pumps and switching regulators are listed in Table II. Switching regulators are the best choices for power supplies driving portable application because of their high efficiency and high power capability.

Table II: Comparisons of the different power supply circuits.

	Linear Regulators	*Charge Pumps*	*Switching Regulators*
Efficiency	Low	Medium	High
Power Capability	Medium	Medium	High
Footprint area	Compact	Moderate	Large
Cost	Low	Medium	High
Complexity	Low	Medium	High
Noise	Low	Medium	High

1.5 Design Motivation

When new types of display such as active matrix organic light emitting diode(AMOLED), electrochromic displays(ECD), electrophoresis displays(EPD), twisting ball displays(TBD), and cholesteric liquid crystal display(Ch-LCD) show up to change generally people's lives, which are regarded as the next generation industry, various custom-designed panel drivers are designed and manufactured corresponding to different purposed using. Many approaches are proposed [21]-[25] to enhance speed of AMOLED, and some methods even products [26], [27] are brought up to fit panel's characteristics.

In the previous discussion of general power supply methodology, boost dc-dc converters and switching capacitor circuits are usually applied to Ch-LCD due to their property of promoting voltage to much higher voltage levels, in which the laced of voltage multiple property in linear regulators cannot be used. The advantage of boost converters are obviously high efficiency and high driving capability mentioned in Table II. Thinking to uppermost ten pikofara of the capacitor loading in each cholesteric liquid crystal pixel, when panel's size becomes larger, capacitance of liquid crystal and the parasitic capacitance, parasitic resistance of bonding wires are sure to cost the speed, conducing the increasing driving capability of the power supply to compensate the transient performance, which would turn into a serious requests if switching capacitor circuits are used. Besides, if the violent approach is utilized to directly enlarge the stored capacitors and area of passing transistors in order to pass more driving current through in switching capacitor structure, there's too much energy consumes in the on-resistance of every passing transistor and lead to energy and area inefficiency. From this point of view, boost converters are the most qualified candidate for driving liquid crystal.

But considering another side, large voltage difference between two terminals of liquid crystal in Fig. 7 reaches to 40V boost converters have to supply. Under the circumstances,

high sustained, up to 40V across drain and source terminals MOSFETs both in high and low side in the right hand of inductor are unavoidably implemented. If foundry cannot support the integration circuit(IC) resources, it cannot be avoided to use two external MOSFETs to produce one channel and high voltage output, which results to the waste of area. Furthermore, conventional boost converter structure have the characteristics that one input source promote a higher voltage output counting on energy storage elements of an inductor and a capacitor. The property leads to the result that N outputs needed in gray level driving require N sets of energy storage, which doesn't gain any benefit to achieve numerous voltages by largely consuming area.

Summary of all, switching capacitor circuits can generate any composition of voltage level required when considering gray level display, but have the dilemma of driving capability and power efficiency. Boost dc-dc converters have the merits of high efficiency even with stronger current driving, but growing up in area waste when more outputs are produced.

Therefore, seeking one effective approach in dc-dc converters to satisfy all the demands of high efficient/driving capability and the use of multiple voltages is urgent in cholesteric liquid crystal display. In the following chapters, the optimum solution to the request will be proposed and discussed step by step.

1.6 Thesis Organization

The concept of single inductor multiple output dc-dc converter is organized in chapter 2. Proposed single inductor dual/bipolar positive negative high voltage outputs and self biasing switching capacitor technique are illustrated in chapter 3. Circuit implementation of the proposed technique is described in chapter 4. Experimental results are shown in chapter 5. Finally, the conclusion and future work are made in chapter 6.

Chapter 2

Introduction to Single Inductor Multi-Outputs DC-DC Converters

2.1 Concept

Today's field of power management requires high power conversion efficiency, fast line/load transient response, and small volume of the power module. In particular, cell phones, digital cameras, MP3 players, PDAs and portable products require varied voltage levels of power supplies for delivery to different sub-modules in portable products. Thus, there are different designs that provide different voltage levels as shown in Fig. 13. Low dropout (LDO) regulator arrays are one of the designs for different voltage levels as depicted in Fig. 13(a), where the index i is from 1 to n which is used to index the nth output. However, LDO regulator arrays sacrifice power conversion efficiency and greatly reduce battery life. The other solution is illustrated in Fig. 13(b), which combines with different inductive switching converters. The high power conversion efficiency is ensured by the inductive switching converter. However, the large number of inductors occupies the large footprint area and increase fabrication cost.

To achieve microminiaturization and high power conversion efficiency for a power management unit, the single inductor multiple output (SIMO) DC-DC converter has been developed as a suitable solution. The conceptual SIMO DC-DC converter is shown in Fig. 13(c). It only uses one inductor component to generate multiple voltage levels for different

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sub-modules in the portable products. The SIMO DC-DC converter not only reduces the footprint area and fabrication cost but also provides highly power conversion efficiency [28]. However, all load current conditions of the multiple output terminals arise in the current level of the inductor. When the load current condition of each output accumulates in the same inductor, the design challenges of the SIMO DC-DC converter such as cross-regulation, power conversion efficiency, system stability, and lack of flexibility of both the buck and boost must be seriously addressed.
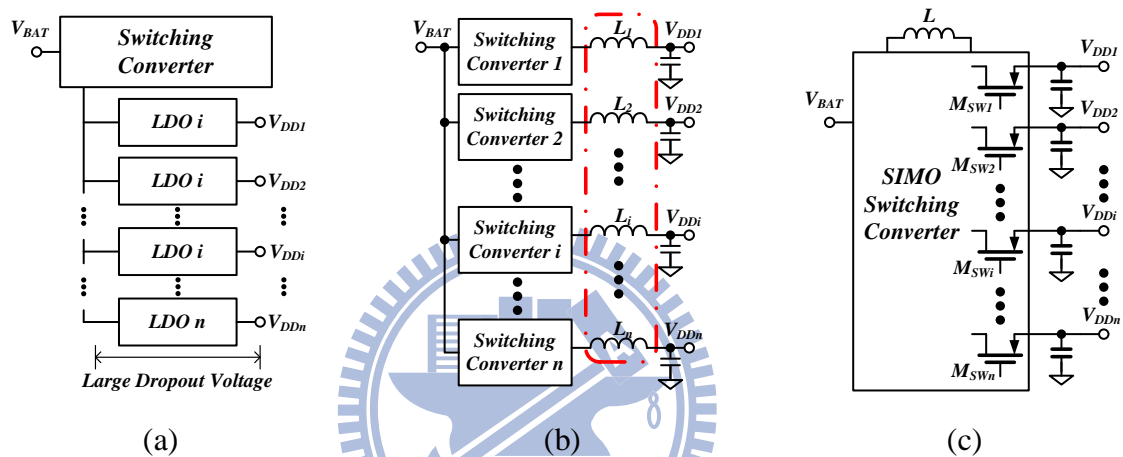
Fig. 103. Different power management designs. (a) Use of many LDO regulators. (b) Use of many switching converters. (c) Use of a single-inductor and multiple-output converter.

2.2 Literatures Review

Several topologies and control techniques have been proposed to implement SIMO DC-DC converters [29]-[40]. The SIMO DC-DC converter in [28] uses the hysteretic continuous current mode (CCM) control method and state machine to regulate output voltage. The proposed single-inductor multiple positive/negative output dual-loop DC-DC converter in Fig. 14 operates all output voltage levels (positive and negative) independently on a cycle by cycle base. The control of the individual channels is managed by a state machine (first loop) which takes care of the power stage switching pattern and allows the hysteretic converter to run in a pseudo-continuous current mode (PCCM) to guarantee a high

power conversion capability. The second loop works as a variable peak current control to minimize the inductor current. It will be demonstrated why running with a controlled peak current also yields in a small output voltage ripple and how the state-machine can help to further control the amount of energy delivered into one output channel.
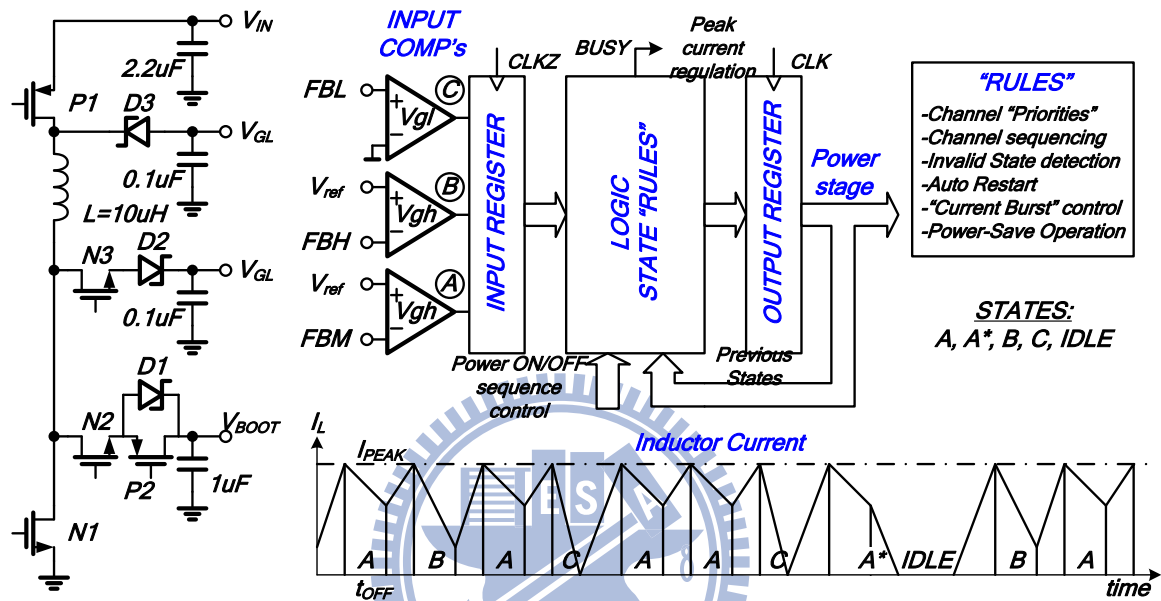
Fig. 14. The State Machine With Hysteretic CCM Control Method [28].
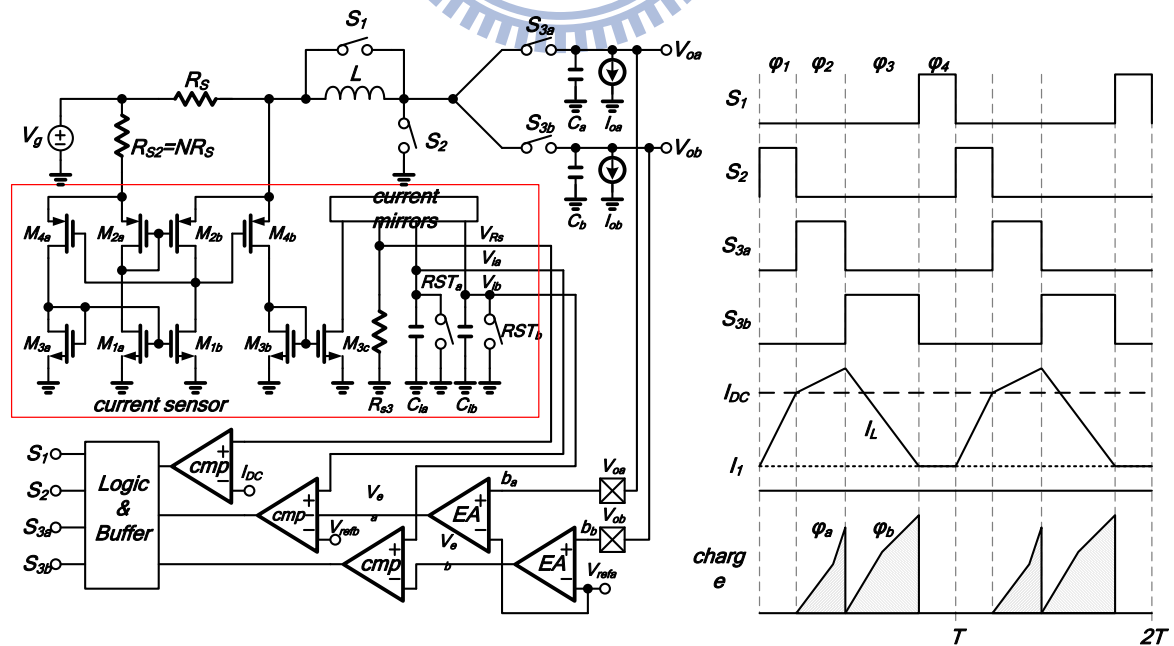
Fig. 15. The Charge Control Method of SIDO DC-DC Converter [29].

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The work in [29] proposed the charge control method and divided one period to regulate the multiple output voltages. This converter in Fig. 15 required fewer switches than the conventional design. Comparing the simulation results of the non-inverting fly-back converter with that of the buck/boost converter, a 5% improvement in efficiency is achieved with the same load condition. Also, it can be achieved good line and load regulation and minimizes cross-regulation by a pre-defined and fixed freewheeling current level I_{DC}. Owing to the high freewheeling current level, the power conversion efficiency is greatly decreased in light load condition.

The works in [30] and [37] calculate the cross-regulation problem when one period is divided to regulate the multiple boost output voltages. This converter in [30]-[35] and [39] adopts time-multiplexing (TM) control in providing two independent supply voltages using only off-chip inductor. This converter is analyzed and compared with existing counterparts in the aspects of integration, architecture, control scheme, and system stability. Implementation of the power stage, the controller, and the peripheral functional blocks is discussed. The block diagram of SIDO DC-DC converter in [30] is shown in Fig. 16. Furthermore, the work in [37] proposed the PCCM which involves the advantages of CCM and discontinuous conduction mode (DCM).
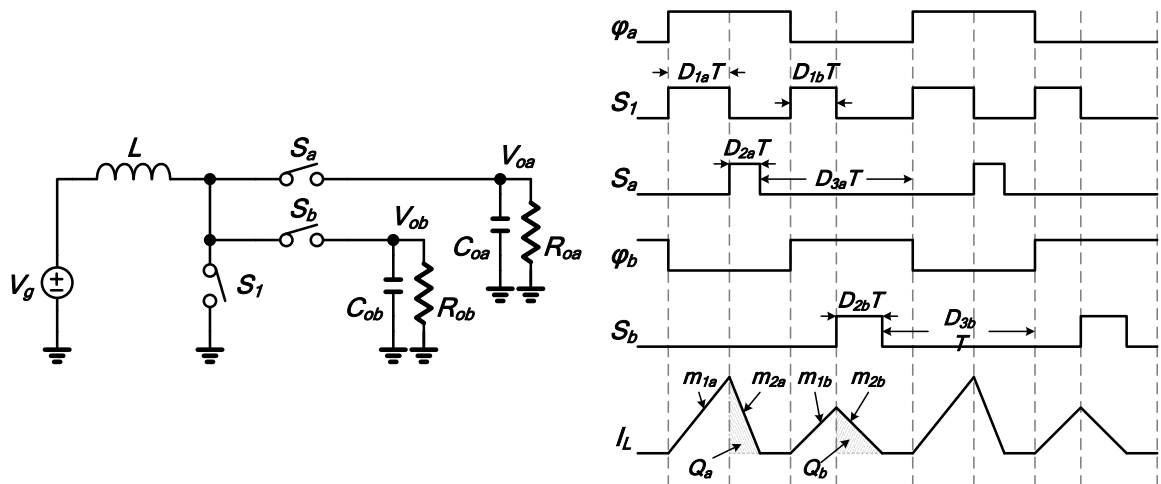
Fig. 16. The Block Diagram of SIDO DC-DC Converter [30].

The works in [38] are proposed to monitor freewheeling current as the inductor current control method for dual boost output voltages. Fig. 17 shows the architecture of a synchronous boost converter with freewheeling current feedback. Unlike conventional converters, an error amplifier, rather than the output voltage, is used to regulate the freewheeling current I_F. Since freewheeling current does not go negative however, there should be a DC offset level for the feedback loop to be controlled properly. Slope compensation is not necessary in this control loop, although the switch current, is used for duty cycle control like in a conventional current-programmed mode (CPM) converter. Because there exists a freewheeling period in every cycle, the operation is similar to that of a DCM converter.
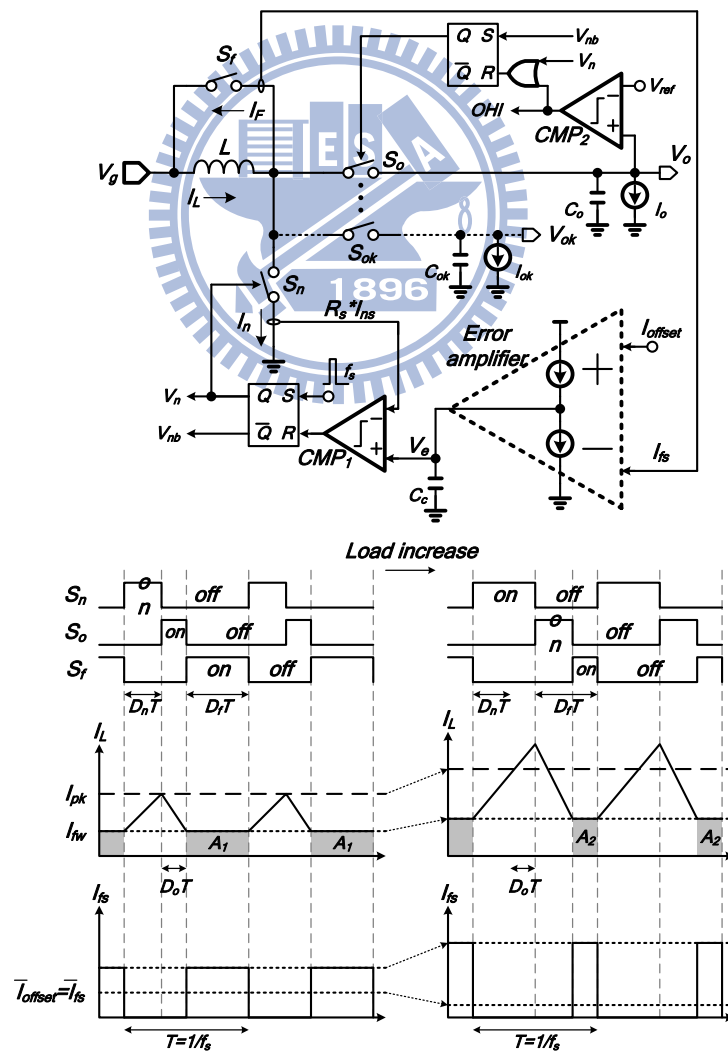
Fig. 17. The synchronous boost converter with freewheeling current feedback [38].

The work in [40] orders power distribution of four boost output voltages. The ordered power-distributive control (OPDC) arranges four boost outputs V_{o1}, V_{o2}, V_{o3}, and V_{o4} in descending order of priority to, one by one, share the charge from the inductor in every switching cycle or, more correctly, every power distribution cycle. Its first three output voltages are controlled using comparators and are thus called comparator-controlled output voltages, while the last-ordered output is proportion-integration (P-I) controlled with an error amplifier that is responsible for the converter's total charge. Therefore, in this OPDC, all of the errors of the preceding comparator-controlled outputs are transferred and accumulated to the last, which is the only one requiring a compensation network in the feedback loop. The architecture of the five-output SIMO converter is shown in Fig. 18.
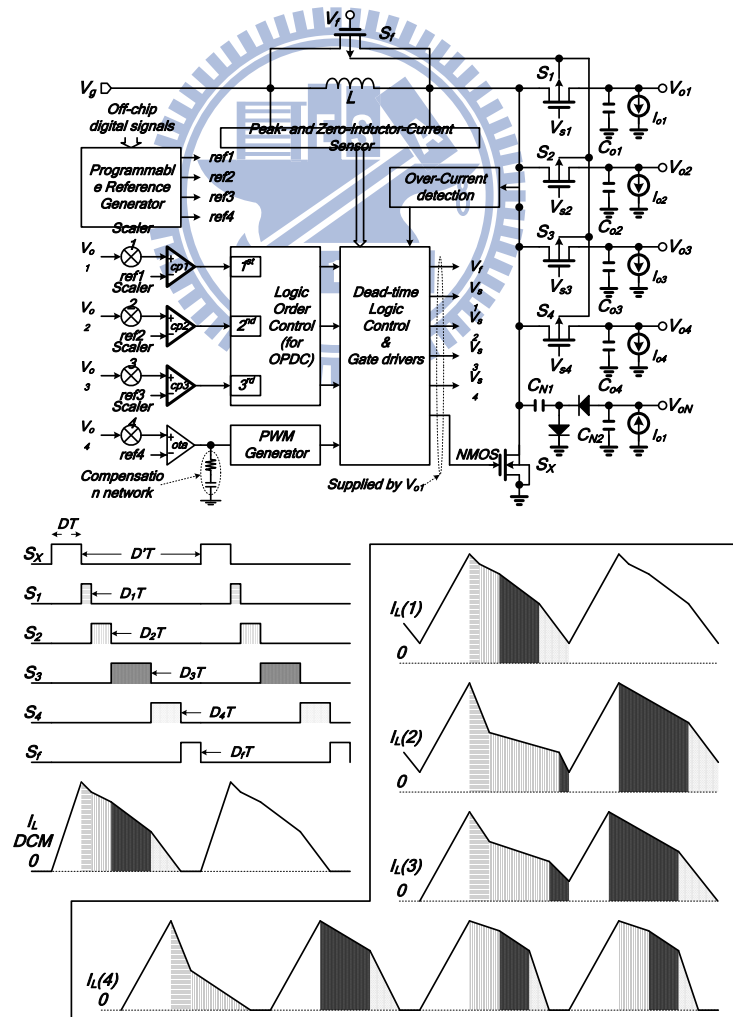
Fig. 18. The five-output SIMO converter with ordered power-distributive control [40].

Chapter 3

Balanced Dual/Bipolar Outputs Structure Based on Switching Capacitor Multi-Output Mechanism

Various types of SIMO are discussed in chapter 2, from where we can find out and conclude the most appropriate topology to meet the requirement of power supply for cholesteric liquid crystal. Besides, according to our design for energy-saving electronic paper, the proper minimum switch number structure will be used in power delivery path. Furthermore, additional function of switching capacitor multi-output mechanism is proposed in order to make the structure workable.
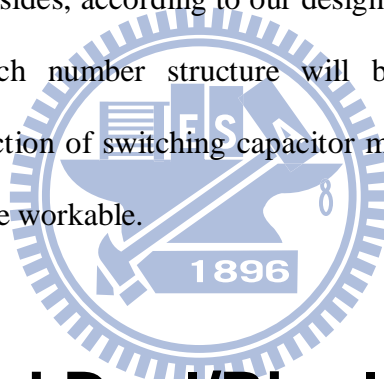
3.1 Balanced Dual/Bipolar Outputs Structure

In Chapter 1, we have a conclusion that using boost converter is more efficient comparing with the use of switching capacitor circuits even with larger current driving capability. But it consumes footprint area to generate high enough voltage output using external energy passing transistors and if we want to produce multiple outputs. Thus, the more attractive way to use in my opinion is to apply a SIMO topology having positive and negative outputs which turns uppermost +40V single output and ground into +20V and -20V bipolar outputs. The merit largely lower down the requests of anti-over stress elements and make

energy passing transistors, or power mosfet, fully integrated possible. The idea is the same as SIMO with peak current state-machine control [28] which takes use of a diode attached in the left side of inductor to generate negative voltages. But in different way, instead of using one period divided into several time slots to regulate corresponding outputs in [28], [30] and [37], which have simple structure and minimum cross regulation between various outputs but in the problem of power delivering to energy-hungry channels non-timely if heavy loading in outputs simultaneously. The proposed idea tends to implement the time-multiplexing(TM) control approach [30]-[35], [39], the advantage in which is the immediately gives power to the specific energy-hungry channel. In other words, the power delivering structure is similar to that in [28], but the controlling method is resembling in [40], which means satisfying all output channels in one period. Thus, the ideal topology is shown in Fig. 19, which has the solution to multiple sets of positive and negative outputs, and can be expanded if needed.
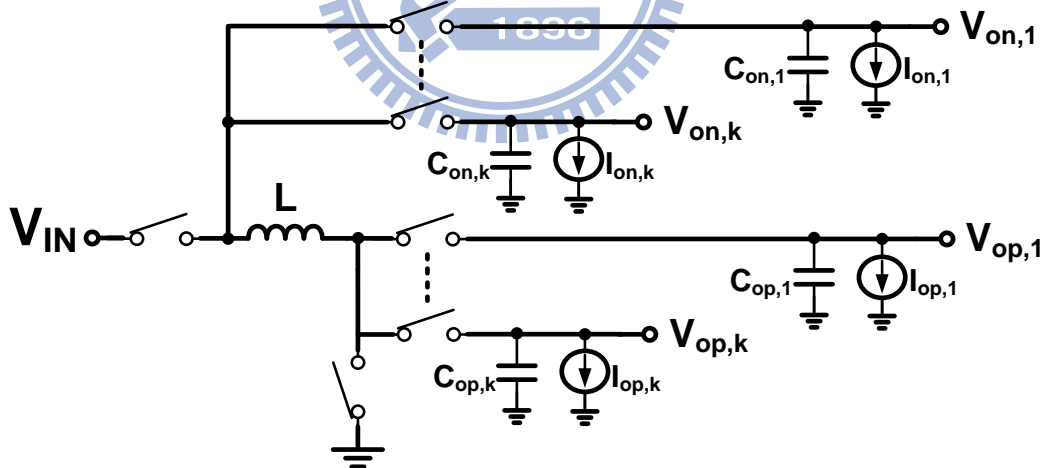

Fig. 19. Single Inductor Multiple Sets of Positive/Negative Outputs Converter.

Unfortunately, it's impossible to use the insane topology since limited footprint area prevents unrestricted extension of bipolar, multiple channels. That is, if the specification of gray level in liquid crystal is 40-level resolution in the region of ±20V, it implies 40 different

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output voltages are required and 40 power mos must be integrated into whole chip, which results in above 90% area filling with power delivering elements. Moreover, implementation of time-multiplexing control is difficult in Fig. 19 because of the dilemma in choosing ordered power-distributive control [40] or selecting power first given to the most energy-hungry channel. The property former distributes power orderly but leading to serious chaos of regulating uppermost 40 different voltage with various loading attached in each channel, and the characteristic latter gives power to most energy-hungry channel which means too many different delivering paths happen in each period, easier for instability taken place. The problem is not caused by the inapplicable of control mechanism, but in the structure of producing 40 output channels which any topology cannot take use of. Does it mean the SIMO structure is not suitable in driving cholesteric liquid crystal, making nonsense in previous discussion? The answer is no.

According to the loading in *Gate/Source Driver*, pixels of certain row are charged and discharged simultaneously by *Gate Driver* with ±20V polarity alternation row by row, which implies ±20V are more frequently demanded comparing to others' voltage levels in *Source Driver* in the refreshing state. By this way, the final structure adaptive to our power supply system is obviously presented. Driving capability in ±20V voltages are preferably emphasized that SIMO can be adjusted into dual bipolar outputs, and the switching capacitor topology applies to lower driving capability for other output channels. It may be doubted the application of lower efficiency in switching capacitor structure and the responses to the question are not only the preferable methodology comparing to the lowest efficiency in fully use of switching capacitor and comparing to large footprint area in the fully use of SIMO with uppermost to 40 voltage outputs, but also the merits mentioned in next section.

The structure in Fig. 20 is the mixture of boost converter and flyback in Table I, which generates positive and negative voltages.
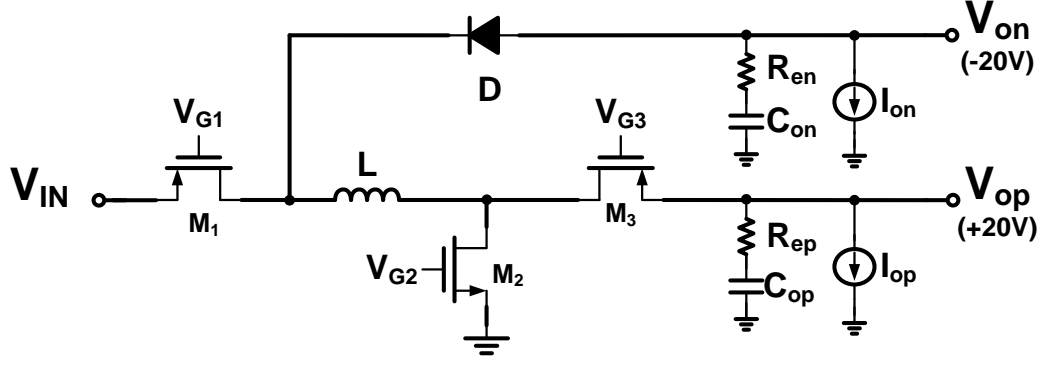
Fig. 20. Single Inductor Dual Bipolar High Positive/Negative Outputs (SIDBHO).

Since the SIDBHO Converter structure is applied, as minimum power loss as possible have to be discussed. Power loss of regulators is the combination of the switching loss and the MOSFET's conduction loss in equation (6). The conduction loss also can classify into boost high-side transistor loss, low-side transistor loss and flyback transistor loss.

$$P_{MOSFET} = P_{SW} + P_{COND} \qquad (6)$$

Calculating the boost high-side conduction loss is straightforward that the conduction loss is just the I^2R loss timing the MOSFET's duty cycle as below:

$$P_{COND} = I_{ON}^2 \cdot V_D \cdot D_{ON} \qquad (7)$$

Where I_{ON} is average loading current on negative output (V_{ON}) terminal; D_{ON} is the duty ratio for negative voltage channel conduction; V_D is the on-voltage when diode turns on. Calculating the boost high-side conduction loss is straightforward that the conduction loss is just the I^2R loss timing the MOSFET's duty cycle as below:

$$P_{COND} = I_{OP}^2 \cdot R_{DS(ON)} \cdot D_{OP} \qquad (8)$$

Where $R_{DS(ON)}$ is at the maximum operation MOSFET junction temperature ($T_{J(MAX)}$); I_{OP} is average loading current on positive output (V_{OP}) terminal; D_{OP} is the duty ratio for boost positive voltage channel conduction. Boost low-side loss are also comprised of

conduction loss and switching loss. Conduction loss for boost low-side is given by:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot (1 - D_{ON} - D_{OP}) \tag{9}$$

$$I_{OUT} = \frac{I_{OP} \cdot D_{OP}}{1 - D_{ON} - D_{OP}} + \frac{I_{ON} \cdot D_{ON}}{1 - D_{ON} - D_{OP}} \tag{10}$$

Where $(1 - I_{OP} - I_{ON})$ is the rest of one period for boost/flyback inductor charging ratio.

The switching interval begins when the low-side MOSFET driver turns on and begins to supply current power MOSFET's gate to charge its input capacitance. There is no switching loss until V_{GS} reaches the MOSFET's V_{TH} therefore power loss equal zero.
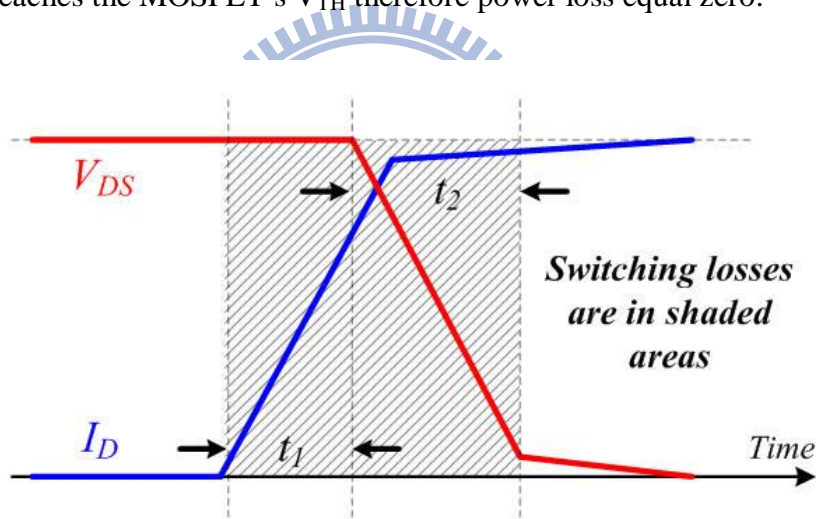
Fig. 21. Transient Waveform of V_{DS} and I_D Curve in Switching Losses on Power MOSFET.

When V_{GS} reaches V_{TH}, the input capacitance (C_{ISS}) is being charged and I_D (the MOSFET's drain current) is rising linearly until it reaches the current I_L which is presumed to be I_{out}. During this period (t_1) the MOSFET is sustaining the entire positive output voltage across it, the energy in MOSFET during t_1 is:

$$P_{t1} = t_1 \cdot \frac{(V_{OP} \cdot I_{OP})}{2} \tag{11}$$

Now, we enter t_2. At this point, I_{out} is flowing through low-side MOSFET, and the V_{DS} begin to fall. All of the gate current will be going to recharge C_{GD}. During this time the current is constant (at I_{out}) and the voltage is falling fairly linearly from V_{OP} to 0, therefore:

$$P_{t2} = t_2 \cdot \frac{(V_{OP} \cdot I_{OP})}{2} \tag{12}$$

The switching loss for any given edge is just the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval:

$$P_{SW} = \frac{(V_{OP} \cdot I_{OP})}{2} \cdot (t_1 + t_2) \cdot F_S \tag{133}$$

The efficiency of switching regulator is defined as the ratio of the output power consumption and input power supplies, formed as below:
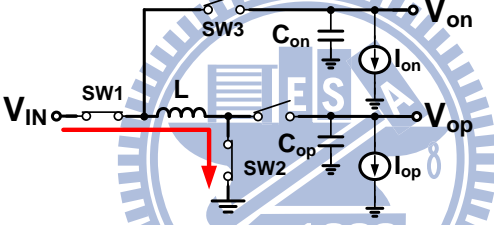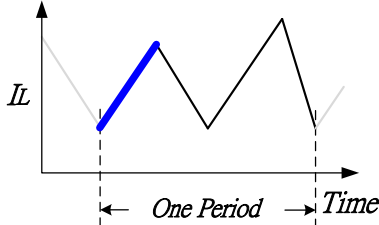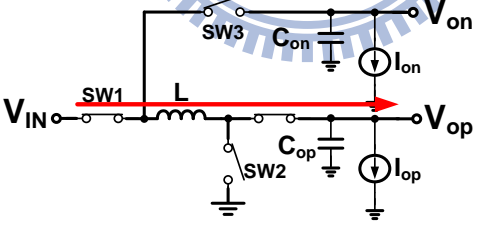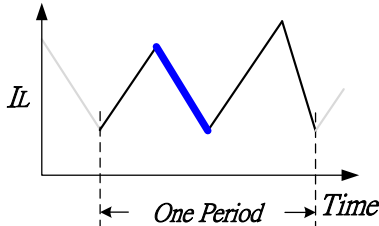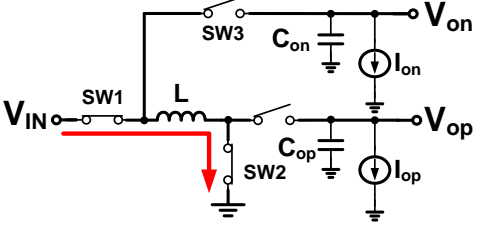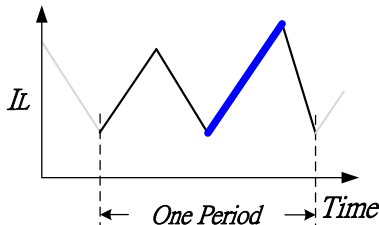
$$E_{ff} = \frac{P_O}{P_{in}} = \frac{P_O}{P_O + P_Q + P_{SW} + P_{COND} + P_{Else}} \times 100\% \tag{14}$$

The input power supplies consist of the output consumption (P_O), switching loss (P_{SW}), conduction loss (P_{COND}), quiescent loss (P_Q) and other losses (P_{Else}) in parasitic elements. quiescent loss that was consumed by controllers of switching regulators. The smaller quiescent loss had higher efficiency. A high efficiency results in a high performance extending the energy resource's life.

In order to make the power loss as small as possible, the conduction loss and switching loss must be lower and lower. Conduction loss has already determined by the sizes of energy passing transistors, that is, power mos, before designing the supply system and it depends on the range of loading condition. However, we can observe the most efficient approach for low switching-loss operation. In Table III, SIDBHO uses the control method of one period divided

into two regulating intervals. First input accumulates charge for boost required and stores in inductor and discharge into positive output by inductor's continuously property. In the second interval input charges for flyback required again and discharge into negative output. By this way, cross regulation can be suppressed down but in the problem of energy to power-hungry channel non-timely. Additional, the switching loss increases due to the higher combination of energy delivery paths.

Table III. Possible Combination for Energy Delivery Path—Type I.

	Energy Delivery Path	Inductor Current *v.s.* Time
Charging		
Boost Discharging		
Charging		

Flyback Discharging		
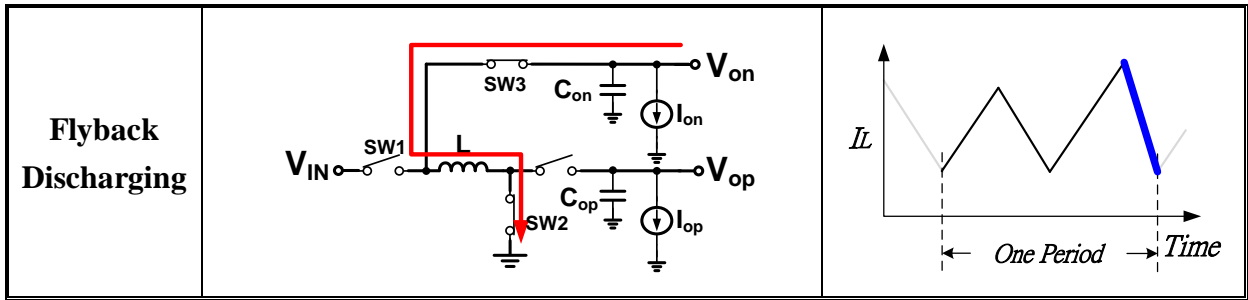
In Table IV, SIDBHO takes use of time-multiplexing control scheme. First input accumulates enough charges stored in inductor and discharge into positive output and then into negative output. By this way, the switching loss can be lower down comparing to Table III due to the lower combination of energy delivery paths

Table IV. Possible Combination for Energy Delivery Path—Type II.

	Energy Delivery Path	Inductor Current *v.s.* Time
Charging		
Boost Discharging		
Flyback Discharging		

In Table V, the energy delivery approach is similar to Table IV, but in different discharging way which exchanges the order of positive and negative outputs, whose control scheme applies to our system actually. The reason is related to the current sensors by sensing voltage of right terminal in inductor which will be discussed next chapter. By using topology in Table V, it can make the current sensor more accurate and save the anti-error circuits prevent from mistake sensing.

Table V. Possible Combination for Energy Delivery Path─Type III.

	Energy Delivery Path	Inductor Current *v.s.* Time
Charging		
Flyback Discharging		
Boost Discharging		

Table VI concludes the control scheme of energy delivery path in Table V. In first path the slope of inductor rises to store charge and at this time SW_1 and SW_2 work. Secondly, stored charge delivers to negative and inductor slope becomes negative, in which only $SW1$ changes state. Finally, the rest charges delivers to positive path and inductor waveform goes back to the same position in previous period, and SW_1, SW_2 and SW_3 changes simultaneously.

Table. VI. The Summary of Inductor Current Path in SIDBHO Converter of Type III.

Path	1	2	3
Function	*charge*	*flyback*	*boost*
Sign	$+$	$-$	$-$
I_L *Slope*	$\dfrac{V_{IN}}{L}$	$\dfrac{V_{ON}}{L}$	$\dfrac{V_{IN}-V_{OP}}{L}$
Switches	*SW1 & SW2*	*SW1*	*SW1, SW2 & SW3*
Relation	$V_{OP}\,\&\,V_{ON}$	V_{ON}	V_{OP}

3.2 Fully Symmetric Switching Capacitor Based Multi-Output with Self Biasing Mechanism

Since single inductor multiple sets of positive/negative output converter is not suitable to produce because of the complexity in control scheme, multiple outputs are still required to act as gray-level driving in liquid crystal. In conventional approach, gray level voltages are the responsible of gamma reference voltage circuits, which are formed by several resistors to composite different ratio structure in order to produce a correction curve to compensate the non-linearity for lamination versus input voltage [8] in Fig 22. The approach is unavoidable to design corresponding set of voltages in easier and straight way, but it is obviously an inefficient method to use resistor-string since there's a leakage path all the time even when no refreshing is required in displays.
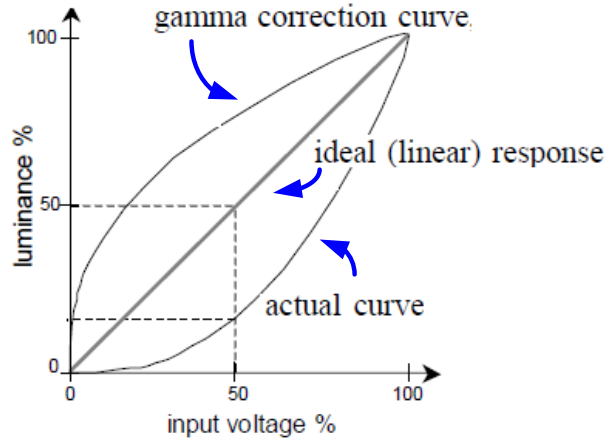
Fig. 22. Luminance versus Input Voltage.

To solve the inefficient problem and the function to drive gray level in liquid crystal, the proposed switching capacitor based multi-output structure is shown in Fig. 23. The mechanism uses charge pump concept and fully symmetric structure, where uses C_2, C_3, C_5, C_6 pumped by same amplitude, non-overlapping clock-like with opposite phase signals of V_{IN} and V_{INB}, and put charges from higher voltage level side to the middle lower side of C_1, C_4 and C_7, thus, the stable voltages of V_1, V_2 and V_3 are generated. The concept is similar to the situation that water containers in the two sides fill in enough water in the middle containers and keep constant level of water same with the amplitude of V_{IN} and V_{INB}. When V_{INB} is low and V_{IN}'s high, charges from V_{IN} flow into C_1 by M_{sw1} to keep V_1 constant and refill the voltage level of C_3 by M_{sw4} in 1st floor; at 2nd floor, V_{c1} is pumped by V_{IN} and pass charges through M_{sw5} and M_{sw8} to increase level in C_4 and C_6 respectively. In the opposite phase, when V_{IN} is low and V_{INB}'s high, charges from V_{INB} flow into C_1 by M_{sw2} to keep V_1 constant as previous action and refill the voltage level of C_2 by M_{sw3} in 1st floor; at 2nd floor, V_{c2} is pumped by V_{INB} and pass charges through M_{sw6} and M_{sw7} to increase level in C_4 and C_5 respectively. It cannot deny the switching capacitor topology has lower efficiency, too, but it does better comparing to resistor-string structure. Moreover, the topology can be expanded by module with dash line in Fig. 23 to fit the more requests of voltages.
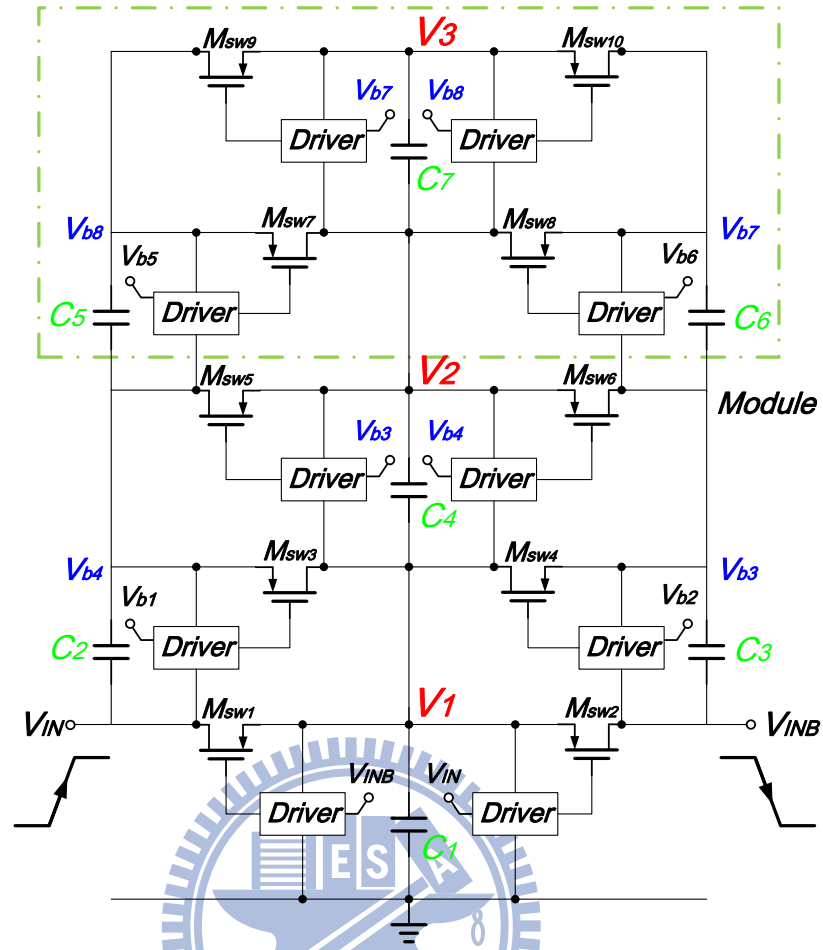
Fig. 23. Switching Capacitor Based Multi-Output Mechanism.

The bias of each passing transistor for switching capacitor would be trivial and careful in order not to make any mosfet take the risk of over-stress problem [41], [42]. To achieve every element stress free, and to overcome bias problem, Fig. 24 shows the self biasing circuit to compatible with topology in Fig. 23. The bias voltages of $Vb_1 \sim Vb_8$ are clock-like signals to drive passing transistors that charge pumping procedure works appropriately, which are generated by switching capacitor structure itself and from modules of inverter in self biasing circuit. On the contrary, the bias V_1, V_2 in modules of inverter are implemented by stable voltages of switching capacitor topology, and finally forms cross-bias fully symmetric switching capacitor circuit.
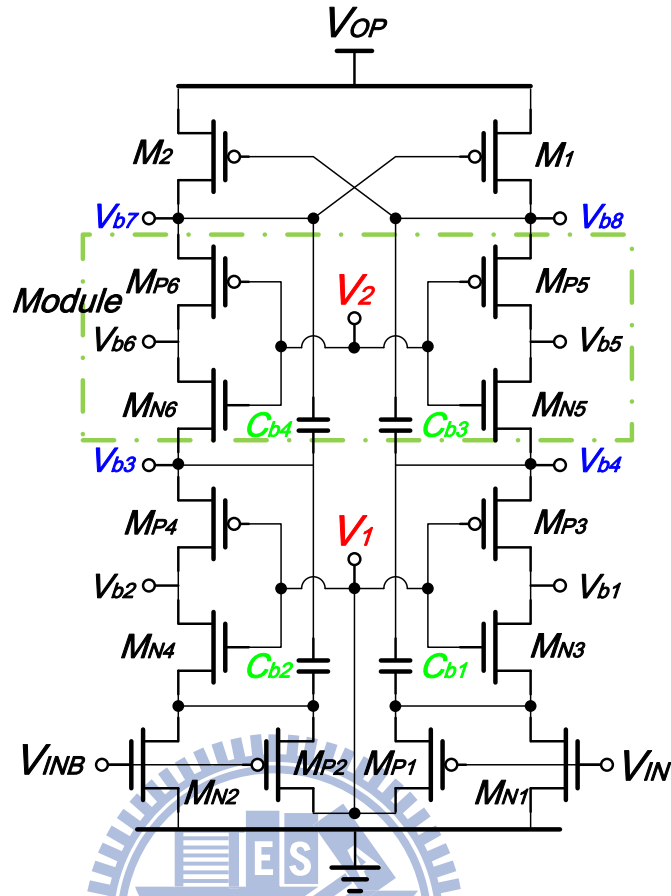
Fig. 24. Self Biasing Circuit for Switching Capacitor Structure.

The last but not least, it's applicable for Power Mosfet of M_3 in boosting positive side in Fig. 20. Because the process used in this thesis is TSMC 0.25μ m BCD, which provides mosfet having the properties of maximum 5V in V_{GS}. It means the minimum level of VG3 should not be lower than 15V since voltage in source terminal of M3 is 20V, whose power mosf's driver should not simply be composed by normal level shifter and inverter-chain, instead, switching capacitor topology can be applied as special level shifter which shift digital signals from logic with core voltage into high level, which avoid over-stress problem.

In summary, the invention of switching capacitor topology and its self basing circuit provides the special driver for boosting high side PowerMos M_3 in Fig. 20, and make a cross-bias balanced circuits, requiring no external bias voltage, and finally, another type of gamma reference generator having driving capability for gray level.

Chapter 4

Implementation of Proposed SIDBHO DC-DC Converter

The overall topology is shown as Fig. 25, which contains power delivery elements such as transistors(M_1,M_2,M_3), external inductor(L), diode(D_{ON}), and energy storage capacitors(C_{OP}, C_{ON}) we discussed previous chapter, and contains two error amplifiers(EA_P, EA_N) in two closed loops to regulate positive and negative voltages which use compensation technique we implement. Current programming mode is applied in this structure which uses current sensor producing sensing signal V_s and addition of sawtooth generator, playing the role of slope compensation producing signal V_{slope}, to prevent unstable.
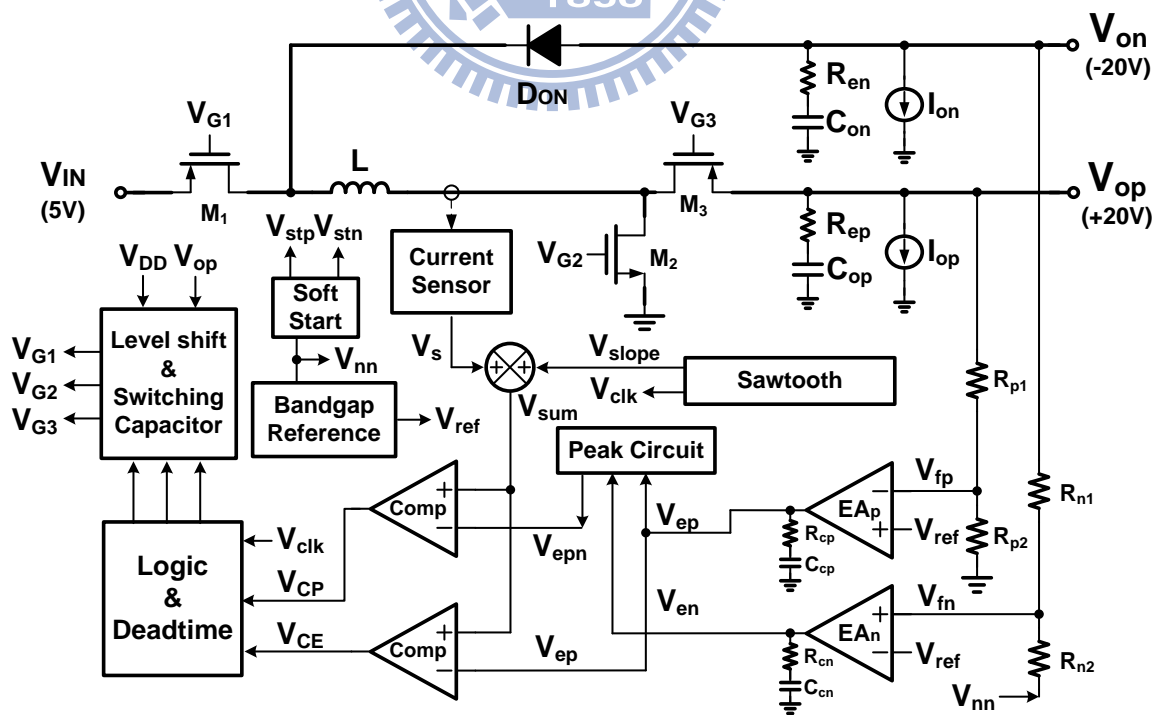
Fig. 25. Block Diagram of SIDBHO DC-DC Converter

Besides, peak circuit takes the summary of error signals (V_{ep}, V_{en}) of two channels to decide how much energy, V_{epn}, is required in each period, and then takes use of comparator (C_{omp}) and signals of V_{sum}, V_{epn} and V_{ep} in Fig. 26 to determine the transition points of inductor current in Fig. 26. When the transitions happen in comparators, the digital control signals V_{CP}, V_{CE} and V_{CLK} from clock generator would enter *Logic & Deadtime* part, then pass through *Level Shift*, *Switching Capacitor* and charge the working condition of energy delivery elements.

In this chapter, the detailed working principles of circuits will be discussed.
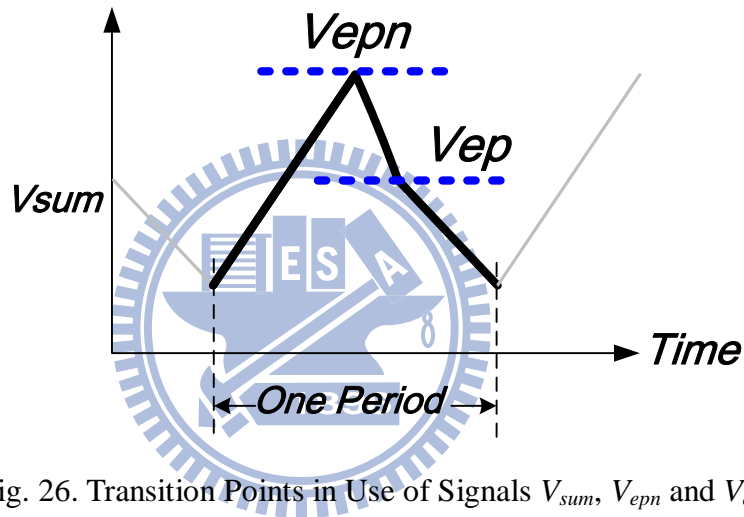
Fig. 26. Transition Points in Use of Signals V_{sum}, V_{epn} and V_{ep}

4.1 Current Sensor and Slope Compensation Circuit

SIDBHO uses current programming mode [43] which has the advantage of fast transient, low ripple and easier in system compensation comparing to voltage mode [43]. The approach to implement current programming mode is to apply current sensor which have various types such as putting sensing resistor near inductor to copy current directly [44]; using parallel

external components of sensing capacitor and resistor to re-bulid inductor current slope [44]; and applying sensing mosfet for each PowerMOS [44].

The merit of putting sensing resistor in the left or right terminal of inductor is accurate because of the capability of making a full copy of inductor slope, but may be in the problem of limited bandwidth due to the use of operational amplifier and energy waste in use of resistor. The advantage of using parallel sensing capacitor and resistor is also accurate since the tunable of external elements, but in the difficulty of delay condition and large area consumption. The drawback of applying sensing mosfet for PowerMOS is not so accurate comparing with the previous cases, but in the great properties of easier implementation and much smaller area occupation, moreover, the flexibility of choosing any PowerMos sensed you want. The last approach will be applied due to its merits and the detailed operating principles is in next paragraph.
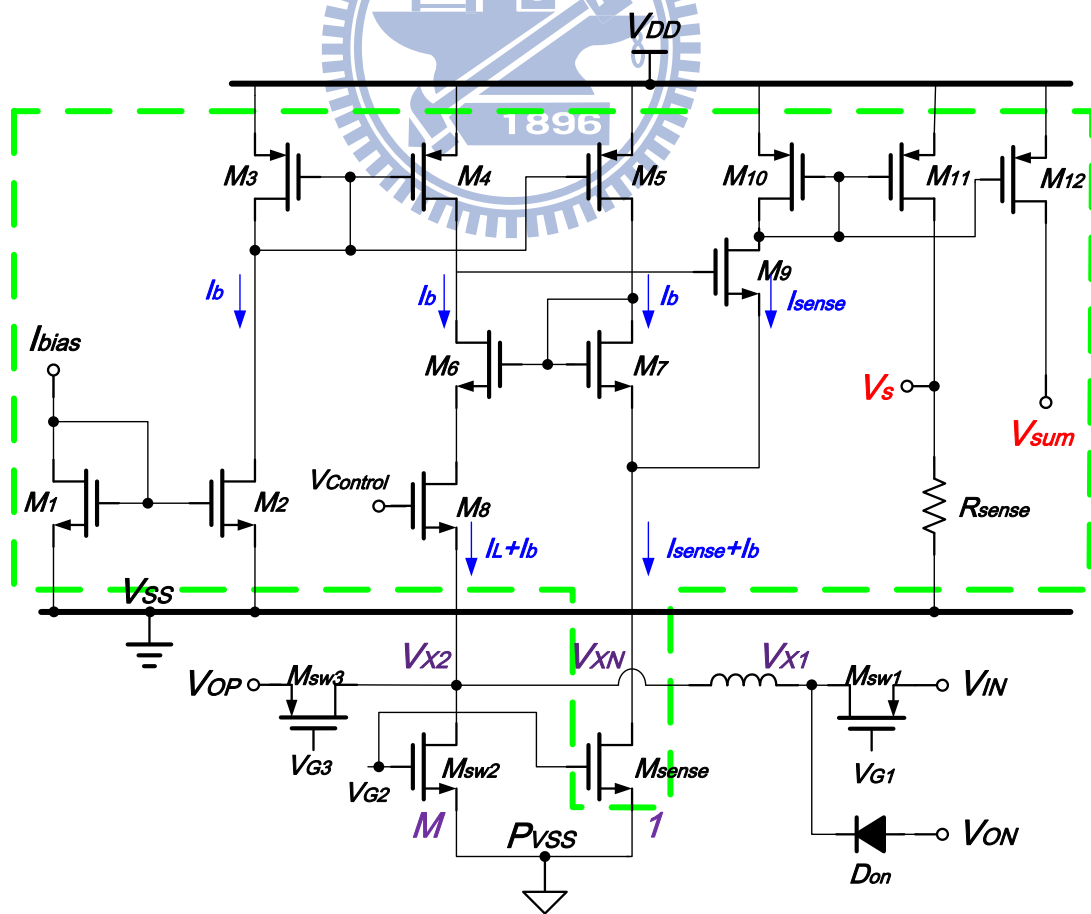
Fig. 27. Current Sensor Circuits.

The dashed green line in Fig. 27 is current sensor whereas outside are the energy delivery elements. As mentioned in last paragraph, the purpose of using sensing mosfet for PowerMOS is an economic way to go and next the determination of which side should be considered. It's very inappropriate to sense M_{sw1} in the left side of inductor since V_{X1} would face negative voltage problem that it'd better to be avoided in control circuits, or the layout of circuits is very complicated and it seemes to be in the result untouchable in the left side of inductor. Alternatively, the use of M_{sw2}, M_{sw3} is better which deicides the 1st transition point composited by V_{sum}, V_{epn} with M_{sw2} sensed and the 2nd transition point composited by V_{sum}, V_{ep} with M_{sw3} sensed in Type II in *Table IV*. But it's in the problem of requirement in blanking circuit to prevent error switching when the discontinuousness of sensing M_{sw2} and sensing M_{sw3}. Thus, to coincide with choosing *Type V* in previously, the reason for flyback first and boost later has the merit to sense M_{sw2} only to decide both transition points because of the continuousness among 1st and 2nd path.

In Fig. 27, M_1, M_2, M_3, M_4 and M_5 use current mirror topology and provide current bias for others. The path concluding M_6 M_7 and M_8 form a simple negative closed loop to force V_{XN} varying with V_{X2} and copy the sensing current I_{sense} which is M-times smaller than I_L induced by the size difference of M_{sw2} and M_{sesne}. Finally, M_9, M_{10} and M_{11} pass the sensing current Isense through sensing resistor and V_s is generated. And the formula reconstruct inductor current:

$$V_S = I_{SENSE} \cdot R_{SENSE} = \frac{1}{M} \cdot I_L \cdot R_{SENSE} \tag{15}$$
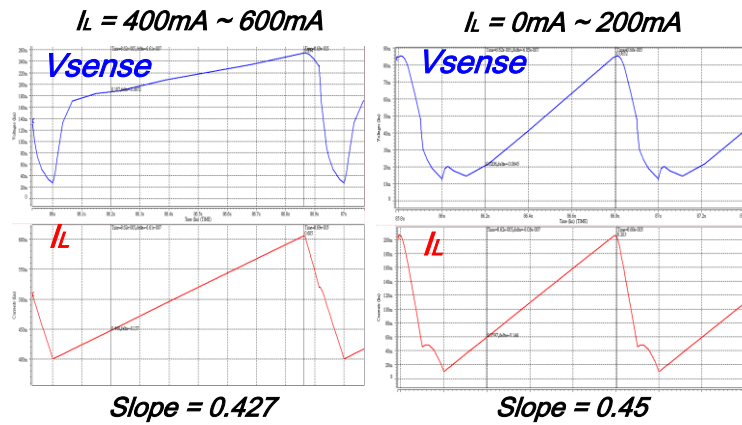
Fig. 28. Simulation Results in Current Sensor Circuits.

In the simulation result in Fig. 28, from the slope calculation, the accurate of V_{sense} is acceptable when I_L varies from 0~200mA to 400mA~600mA range.

The current programmed controller is unstable when converter operates above 50% duty cycle without compensation that shows in Fig. 29. The unstable problem called as sub-harmonic oscillation phenomena. In other words, the perturbed quantity of inductor current was large more and more during a few periods. The phenomena also occurred in other topologies such as boost and buck-boost converters. To avoid this stability problem, the control scheme is usually modified by adding an artificial ramp to the sensed current in the following descriptions.
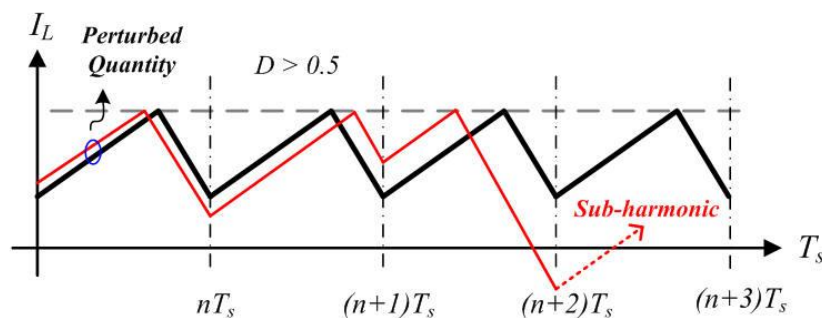
Fig. 29. Inductor Current at Stable and Unstable Oscillation in Current-Mode Converter.

The steady-state and perturbed waveform of inductor current are illustrated in Fig. 30. We can explain the phenomena of steady-state waveform and perturbed waveform with

derived formula. The steady-state waveform of inductor current with m_1 slope ramps up in first interval and ramps down with m_2 slope in second interval. When the perturbed waveform of inductor current occurred with $\hat{d}T_s$, the current difference was introduced in $m_1 \cdot \hat{d}T_s$ [45], [46].
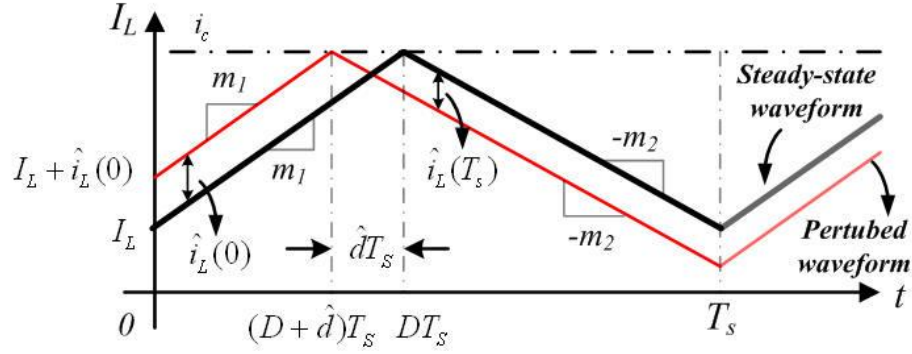
Fig. 30. The Perturbation Waveform of Inductor Current.

The slope of inductor current equals:

$$m_1 = \frac{V_{in} - V_{out}}{L} \; , \; m_2 = \frac{V_{out}}{L} \tag{16}$$

According to Fig. 30, we can derive:

$$i_L(T_s) = i_L(DT_s) - m_2 D'T_s = i_L(0) + m_1 DT_s - m_2 D'T_s \tag{17}$$

In steady-state, the above equation $i_L(0) = i_L(T_s)$ and shows as:

$$0 = m_1 DT_s - m_2 D'T_s \; , \; then : \frac{m_2}{m_1} = \frac{D}{D'} \tag{18}$$

From Fig. 30, we can use the steady-state waveform to express the current difference $\hat{i}_L(0)$ $\hat{i}_L(T_s)$ as the slope multiplied by the interval length, Hence:

$$\hat{i}_L(0) = -m_1 \hat{d}T_s \quad , \quad \hat{i}_L(T_s) = m_2 \hat{d}T_s \tag{19}$$

Elimination of the intermediate variable $\hat{d}$ from equation(19) leads to:

$$\hat{i}_L(T_s) = \hat{i}_L(0) \cdot \left(-\frac{m_2}{m_1} \right) = \hat{i}_L(0) \cdot \left(-\frac{D}{D'} \right) \tag{20}$$

A similar analysis can be performed during the next switching period, show that:

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s) \cdot \left(-\frac{D}{D'} \right) = \hat{i}_L(0) \cdot \left(-\frac{D}{D'} \right)^2 \tag{21}$$

After n switching periods, the perturbation becomes:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1) \cdot T_s) \cdot \left(-\frac{D}{D'} \right) = \hat{i}_L(0) \cdot \left(-\frac{D}{D'} \right)^n \tag{22}$$

Note that, as n tends to infinity, the perturbation $\hat{i}_L(nT_s)$ tends to zero provided that the characteristic value –D/D' has magnitude less than one. Conversely, the perturbation $\hat{i}_L(nT_s)$ becomes large in magnitude when the characteristic value $\alpha = -D/D'$ has magnitude greater than one. Hence, for the stable operation of the current mode controller, we need *D/D'*<1 or *D*<0.5.

$$\begin{aligned} \left| \hat{i}_L(nT_s) \right| &\to 0 \quad when \quad \left| -\frac{D}{D'} \right| < 1 \\ \left| \hat{i}_L(nT_s) \right| &\to \infty \quad when \quad \left| -\frac{D}{D'} \right| > 1 \end{aligned} \tag{23}$$

The stable situation with compensation ramp is presented in Fig. 32. When the converter operates with *D*<0.5, the perturbation inductor current will lead to be stable. Conversely, the perturbation inductor current will lead to be unstable to cause the sub-harmonic oscillation if converter operates with *D*>0.5 and no compensation.

The sub-harmonic oscillation is a well-known problem of current-mode controller. However, the converter can be stable at all duty cycles by adding the compensated ramp to the sensed inductor current as shown in Fig. 31. This compensated ramp has the qualitative effect of reducing the gain of the current sensing feedback loop to solve the unwanted oscillation problem in current-mode controller of dc-dc converters.
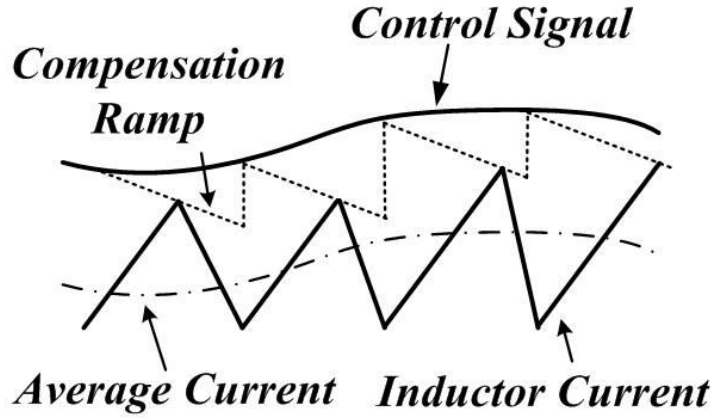
Fig. 31. Current-Mode Control Signal with the Compensation Ramp and Inductor Current.

The compensation theorem is represented in Fig. 31, the perturbation $\hat{i}_L(0)$ and $\hat{i}_L(T_s)$ can express in terms of the m_1, m_2, m_a and the $-\hat{d}T_s$ as follows:

$$\hat{i}_L(0) = -\hat{d}T_s \cdot (m_1 + m_a) \tag{24}$$

$$\hat{i}_L(T_s) = -\hat{d}T_s \cdot (m_a - m_2) \tag{25}$$
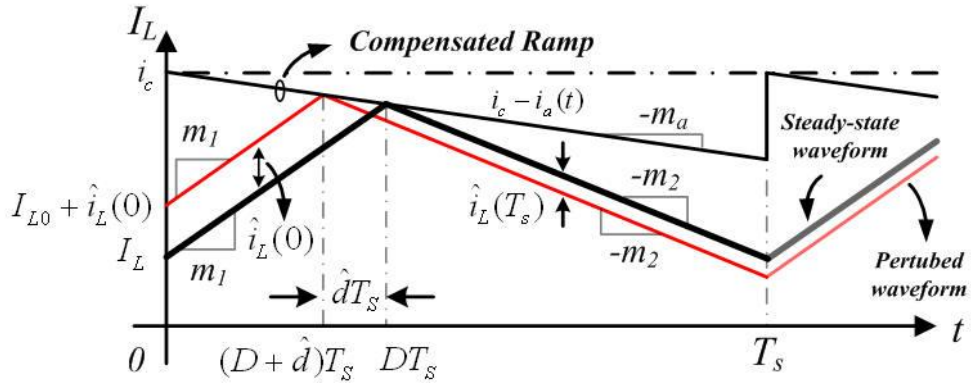
Fig. 32. Steady-State and Perturbed Inductor Current Waveforms with Compensation.

Elimination of $-\hat{d}T_s$ yields:

$$\hat{i}_L(T_s) = \hat{i}_L(0) \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a} \right) \tag{26}$$

A similar analysis can be used to the nth period, leading to:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1) \cdot T_s) \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a} \right) = \hat{i}_L(0) \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a} \right)^n = \hat{i}_L(0) \cdot \alpha^n \qquad (27)$$

For larger n periods, the perturbation magnitude $\hat{i}_L(nT_s)$ tends to equations(22). Therefore, for stability of current mode controller in CCM, it needs to choose the slope of the artificial ramp m_a such that the characteristic value α has magnitude less than one. Conversely, the perturbation $\hat{i}_L(nT_s)$ becomes larger when the characteristic value α has magnitude greater than one:

$$\left| \hat{i}_L(nT_s) \right| \rightarrow 0 \quad when \ |\alpha| < 1$$
$$\left| \hat{i}_L(nT_s) \right| \rightarrow \infty \quad when \ |\alpha| > 1$$
$$(28)$$

One common choice of the compensation ramp slop is

$$m_a = \frac{1}{2} m_2 \qquad (29)$$

This compensation ramp results in the characteristic value α to become zero for all duty cycle of the converter. Therefore, $\hat{i}_L(T_s)$ is leading to zero for any $\hat{i}_L(0)$. Besides, another common choice of m_a is:

$$m_a = m_2 \qquad (30)$$

The above characteristic causes the value α to become zero for all duty. As a result, $\hat{i}_L(T_s)$ is zero for any $\hat{i}_L(0)$. This behavior is known as *deadbeat control* when the system corrects all errors after one switching period. And the compensated inductor current shows in Fig. 33.
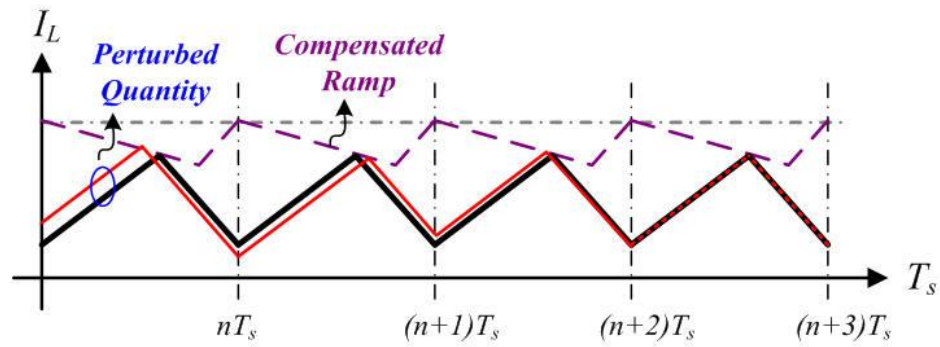
Fig. 33. Inductor Current with Compensation Ramp in DC-DC Converter.

4.2 System Compensation Technique for Boost and Flyback in Current Programming Mode

The compensation of current-mode buck converters is simpler than that of voltage-mode boost and flyback converters due to the single pole of the power stage. The control to inductor transfer function boost converter can be simplified as following:

$$\frac{v}{i_c} = \frac{D'R}{2} \cdot \frac{(1 - s\dfrac{L}{D'^2\,R})}{(1 + s\dfrac{RC}{2})} \tag{31}$$

Where $D = \dfrac{Vo - Vi}{Vo}$ and $D' = 1 - D$. Equation(31) shows in close-loop there is one pole $S_P = -\dfrac{2}{RC}$ and one RHP zero $S_{RHP} = -\dfrac{D'^2 \cdot R}{L}$, which have bad effect on phase margin in system loop. The control to inductor transfer function flyback converter can also be simplified as following:

$$\frac{v}{i_c} = \frac{D'R}{(1+D)} \cdot \frac{(1 - s\frac{DL}{D'^2 R})}{(1 + s\frac{RC}{1+D})} \tag{32}$$

Where $D = \frac{-Vo}{Vi-Vo}$ and $D'=1-D$. Equation (32) shows in close-loop there is also one

pole $S_p = -\frac{1+D}{RC}$ and one RHP zero $S_{RHP} = -\frac{D'^2 \cdot R}{DL}$, which are similar to pole-zero system

to boost converter, and compensation technique would focus on proportion-integral

compensator applied to these two-channel system.

Specifically, only the proportion-integral (PI) compensator is utilized to enhance the

low-frequency gain. The compensation zero is usually used to cancel the system pole ω_{ps},

which is located at the output node. The choice of the compensation zero will affect the

performance of current-mode buck converters due to the load variations. Compared to the

design of voltage-mode buck converters, the complexity of the compensation is reduced but

the system compensation becomes difficult due to the characteristic of the system pole's load

dependence. Owing to the variations of load current, the PI compensation technique generates

a fixed pole-zero pair to raise the low-frequency gain at the expense of transient performance.

As shown in Fig. 34(a), the compensation zero is designed to cancel the system pole at

heavy loads. When load current changes from heavy to light, the system pole moves toward

the origin due to its characteristic of load dependence. The phase margin worsens and the

system may thus suffer from the ringing problem owing to the lesser phase margin at light

loads, that is, since the compensation zero cannot be moved back to cancel the effect of the

system pole at light loads, the phase margin of the system is deteriorated at light loads. The

transient response shows the ringing problem and the long settling time when the load current

changes from heavy to light. On the other hand, what happens when the compensation zero is

used to cancel the system pole at light loads? As depicted in Fig. 34(b), if the compensation

zero is designed at the low-frequency position and the system pole moves to a higher

frequency position in case of the heavy load current, then the phase margin becomes larger than the optimal value for achieving fast transient response. The compensation zero causes the phase margin to be larger than 90 degree. The system is always stable but the transient response is not good at the heavy load condition. As shown in Fig. 34(b), the transient response is slow due to the large PM value.

Therefore, an adaptive compensation zero is needed to ensure a suitable system bandwidth and phase margin. The compensation zero should be located at a low-frequency position to cancel the effect of the system pole at light loads. Likewise, the compensation zero should be moved toward a high-frequency position to cancel the effect of the system pole at heavy loads. Thus, in order to get an adaptive phase margin, an adaptive zero is used to keep a suitable phase margin value. However, the adaptive zero is only suitable for improving the system performance in steady state because the adjustment of the adaptive compensation zero depends on the values of load current and output voltage. At the beginning of the load transient response, the compensation zero is located at a low-frequency position assuming that the load current changes from light to heavy. Thus, the bandwidth of the system becomes large at the beginning of the load transient response because the system pole moves toward a higher frequency position. Once the adaptive zero is moved to a higher frequency position for the cancellation of the system pole, the bandwidth becomes smaller than that at the beginning of the load transient response. In other words, the recovery period becomes longer owing to the small bandwidth. In order to get fast transient response, the fast transient technique is proposed to accompany with the utilization of the adaptive compensation zero. To summarize the purpose of the paper, the adaptive compensation capacitance is proposed to achieve fast transient performance. In the meanwhile, adaptive resistance is utilized to enhance the performance of the converters at steady state.
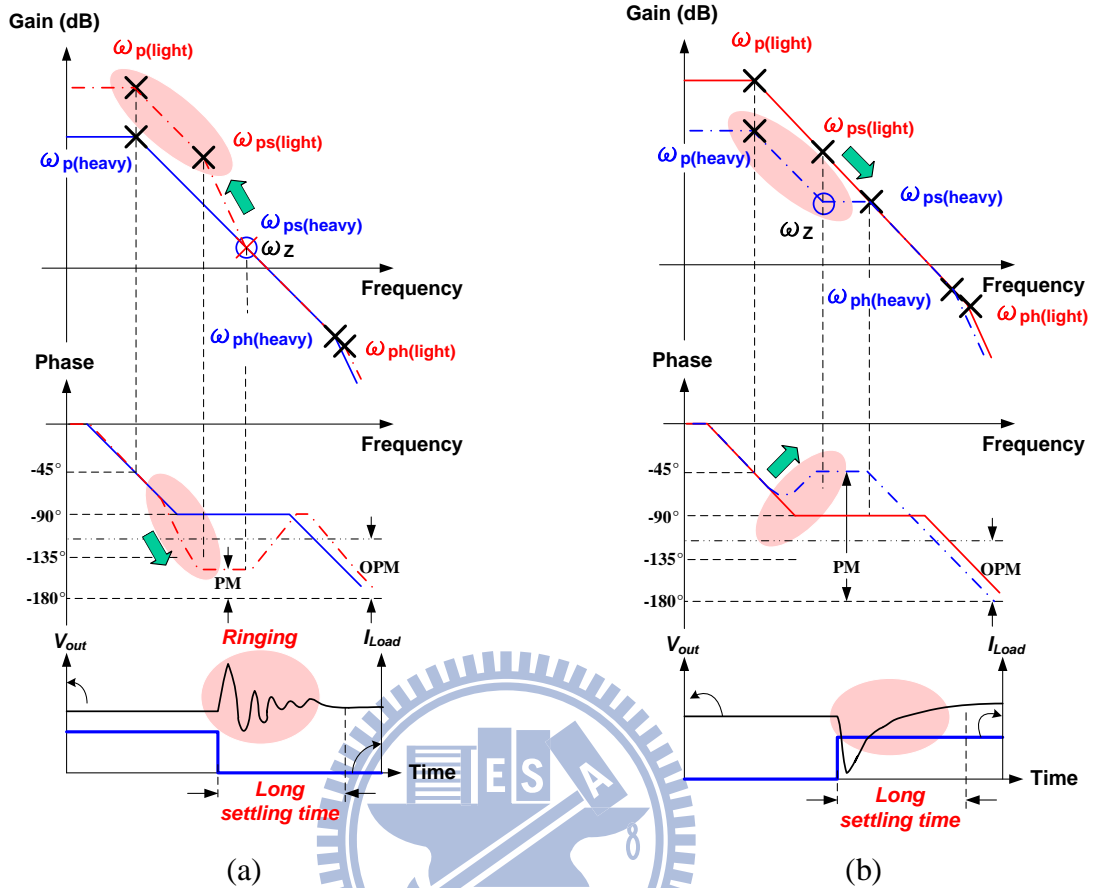
Fig. 34. The Different Positions of the Compensation Zero at Steady State. (a) The compensation zero designed at a high-frequency position to cancel the system at heavy loads causes the phase margin to worsen at light loads. (b) The compensation zero designed at a low-frequency position to cancel the system at light loads causes the phase margin to become larger than the optimum value.

During load transient period, the voltage drop depends on ESR resistance of the output capacitance and loop bandwidth of the system. The drop voltage across the ESR resistance is a material-related value. Furthermore, the system bandwidth and phase margin are important design issues in minimizing the transient voltage drop. How to maintain a high system bandwidth and suitable phase margin is therefore an urgent problem for power management IC designers. This paper proposes a fast-transient control with adaptive phase margin technique to effectively move the compensation pole-zero pair in case of load variations. At the beginning of the load transient response, the adaptive compensation capacitance (C_C) is

decreased to move the compensation pole-zero pair to a higher frequency in order to achieve a fast transient response [47], [48]. At the end of the load transient response, the pole-zero pair is moved back to an optimal position in order to extend the system bandwidth and phase margin based on the instant load condition. Hence, the combination the adaptive capacitance C_C and adaptive resistance R_Z circuits for current mode DC-DC converters has good transient performance and, at the same time, ensures stability.

4.3 Oscillator and Saw-tooth Generator

The proposed oscillator, depicted in Fig. 35, is used to generate a clock signal to periodically start the switching period. Thus, the power p-MOSFET is turned on to deliver energy to the buck output and store energy in the inductor. The saw-tooth waveforms can also be generated in the oscillator. The saw-tooth generator provides the saw-tooth waveforms with high threshold voltage V_H and low threshold voltage V_L. It is recommended that the switching frequency can be kept constant so that the electromagnetic interference (EMI) noise is easily analyzed and eliminated. The charging current I_{ramp} generated by the voltage-to-current converter is proportional to the reference voltage V_{ref} and defined as (33).

$$I_{ramp} = \frac{V_{ref}}{R_{ramp}} \tag{33}$$

The charging current for the capacitor C_{ramp} is generated by the current mirror pair M_1 and M_3. Thus, a saw-tooth waveform is generated at node V_{ramp}. When the value of V_{ramp} reaches the high threshold voltage V_H, the comparator triggers the signal *CLK* from low to high to turn on the switch M_9, thereby discharging the capacitor C_{ramp}. Moreover, in order to accurately control the switching frequency, a discharging current is also generated by another current

mirror pair M_7 and M_8 with a ratio equal to K. Thus, the falling rate is not as high as that directly connected to the ground. A constant switching frequency is generated and its value can be written as (34).

$$\frac{V_{ref}}{R_{ramp}} \cdot \frac{1}{f_{switch}} \frac{K}{(K+1)} = C_{ramp}(V_H - V_L)$$

$$\Rightarrow f_{switch} = \frac{V_{ref} K}{(K+1) R_{ramp} C_{ramp}(V_H - V_L)}$$

(34)

In practice, the switching frequency may be varied by the process due to the delay of the logic and comparator. The value of the resistor is trimmed to finely adjust the value of switching frequency.
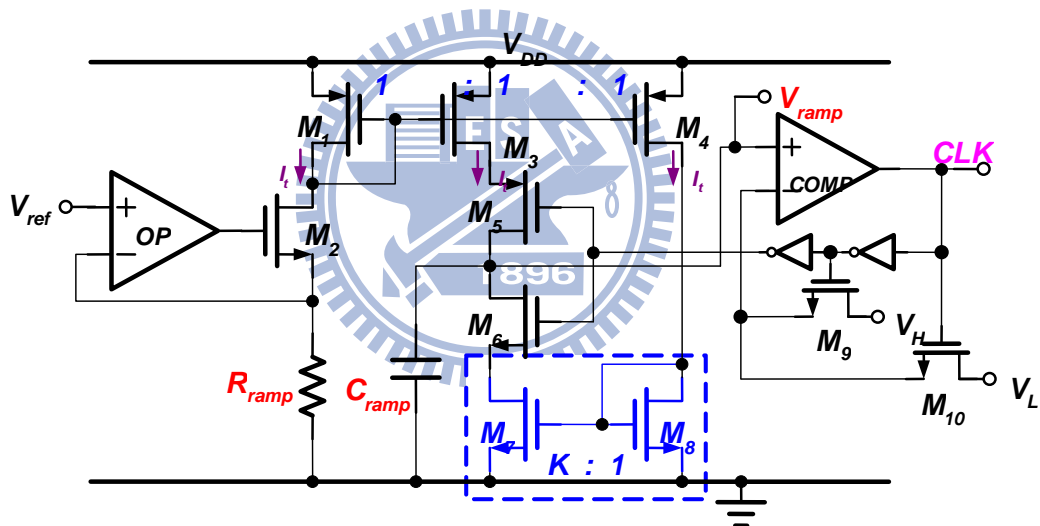
Fig. 35. Oscillator and Saw-Tooth Generator.

4.4 Soft Start-up Circuit

It is necessary for power on mechanism of dc dc converters to make sure system safety. There are many ways to prevent such as the limit of peak inductor current, named over-current protection. Here, we introduce soft start-up circuit since it can prevent in-rush current [40] which causes elements damage.

The function of soft start-up is to make the inductor current change smoothly in order not

to pass too much and sudden current through any device. The approach here is to generate a smoothly increasing slope *VST* to replace reference voltage V_{ref} used in input terminals of error amplifiers(EA_P, EA_N) in Fig. 25. By this way, the error signals V_{ep} and V_{en} would vary slowly to avoid in-rush peak current.
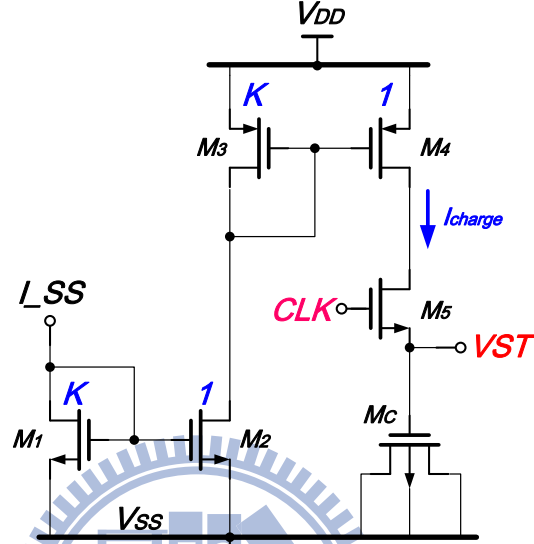
Fig. 36. Soft Start-up Circuit.

In Fig. 36, M_1, M_2 pairs and M_3, M_4 pairs scale down the magnitude of biasing current *I_SS* , and clock signal *CLK* passes small charges with only few duty in one period and charge into large MOS capacitor M_C to produce slow, rising voltage *VST*, the formula of *VST* is presented and simulation signals are shown in Fig. 36.

$$Vst = \int \dot{i}_{charge} \cdot dt$$
$$= \sum_{count} \frac{1}{k^2} \cdot Iss \cdot \frac{T_{on,M5}}{T_{preiod}} \cdot N_{count} \tag{35}$$

Where k is the scale down multiplier and T_{period} is one period between two nearby clock signals. $T_{on,M5}$ is on time of clock pulse. N_{count} is clock switching number counted from power on.
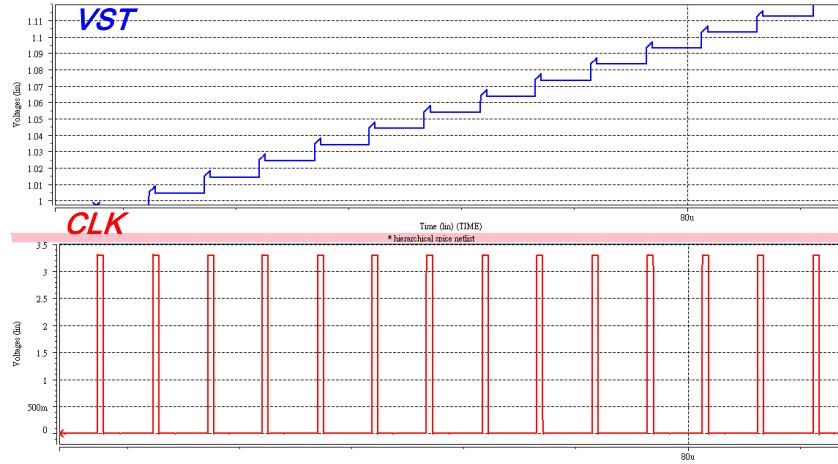
Fig. 37. Simulation Result in Soft Start-up Circuit.

4.5 Reference Voltage Source and Power-On Circuit

For accurately regulation of multiple-output terminals over the temperature range of -40 ^oC~120 ^oC, the temperature-independent reference source is essential in SIMO DC-DC converter. Two quantities having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a zero TC. Thereby, we must identify two voltages that have positive and negative TCs. The forward voltage of base-emitter junction in bipolar transistor or the forward voltage of *pn*-junction diode exhibits a negative TC. When two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature. With the negative and positive-TC voltages obtained above, we can develop reference having a nominally zero-TC. Assuming that $V_{BG} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n)$, where $V_T \ln n$ is the difference between the base-emitter voltages of two bipolar transistors operating at different current densities. Since at room temperature $\partial V_{BE} / \partial T \approx -1.5 mV / \partial T$ whereas $\partial V_T / \partial T \approx +0.087 mV /^o K$, to set $\alpha_1 = 1$ and settle $\alpha_2 \ln n$ such that $(\alpha_2 \ln n)(0.087 mV /^o K) = 1.5 mV /^o K$. That is

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$\alpha_2 \ln n \approx 17.2$. Equation (36) indicates that for zero-TC.

$$V_{BG} \approx V_{BE} + 17.2 V_T \approx 1.25V \tag{36}$$
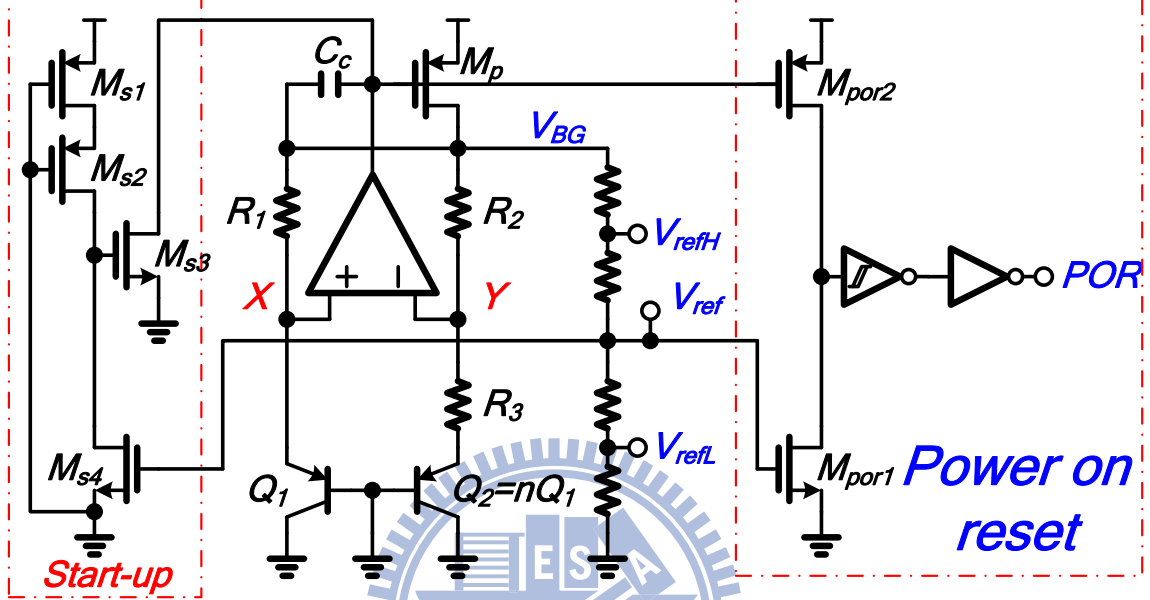
Fig. 118. The Schematic of Bandgap Reference Circuit.

The bandgap reference circuit is shown in Fig. 37. Error amplifier sense nodes V_X and V_Y, driving top terminal of R_1 and R_2 ($R_1=R_2$) such that such that X and Y settle to approximately equal voltage. The reference voltage is obtained at the output terminal of error amplifier. Hence an output voltage can be expressed as (37). For a zero-TC, we have $(1 + R_2/R_3)\ln n \approx 17.2$.

$$V_{BG} = V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) V_T \ln(n) \tag{37}$$

Transistors M_{s1}, M_{s2}, M_{s3}, and M_{s4} compose start up circuit. Transistors M_{por1} and M_{por2} compose power-on reset circuit. Before reference voltage is ready, the output voltage V_{ref} is zero level. Transistor M_{s4} and M_{por1} turn off. Transistor M_{s3} turns on to pull low the gate biasing of transistors M_p and M_{por2}. The output state of power-on reset circuit switches to high

state. Owing to transistor Mp turns on, the error amplifier starts to force voltage of node X and Y for difference of two base-emitter voltage. While the bandgap voltage V_{ref} is build, transistor M_{s4} and M_{por1} turns on. Therefore, transistor M_{s3} turns off and start up process is ended. The output signal *POR* of power-on reset circuit sets to low state and enables the clock generator.

Chapter 5

Experimental Results

5.1 Chip Micrograph & Specification Table

The proposed technique was fabricated using a TSMC 0.25μm BCD process. The chip micrograph, which has a total silicon area of about 3800μm*1720μm, including the testing pads, is shown in Fig. 38. The silicon of the control is only 1720 μm*200 μm excluding pads. The inductor and output capacitors are 20 μH and 2.2 μF, respectively. The switching frequency is 750kHz. The detailed specifications of the proposed Single Inductor Daul Bipolar High Voltage Output DC-DC converter are listed in Table VII.
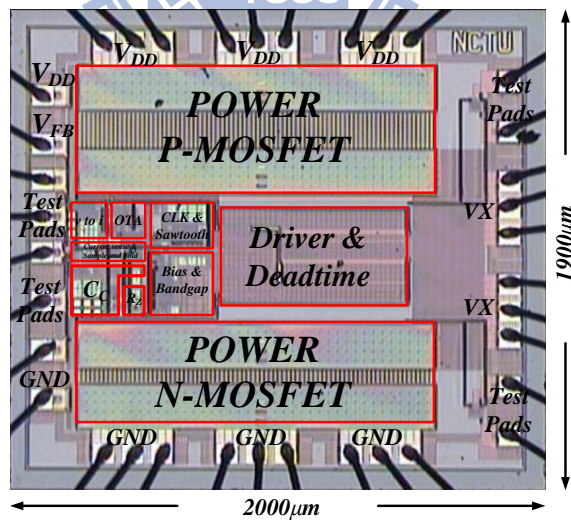
Fig. 39. Chip Micrograph.

Table VII: Specifications of the Proposed SIDBHO DC-DC Converter

Technology	TSMC 0.25μm BCD	
Inductor (off-chip)	20μH	
Input voltage	2~5V	
Converters	Boost	Flyback
Output Voltages	Maximum to +7V	Minimum to -20V
Storage Capacitor (off-chip)	2.2μF	2.2μF
ESR of Capacitor	30mΩ	30mΩ
Maximum output load current	20mA	20mA
Compensation Capacitor	220pF	220pF
Compensation Resistor	200kΩ	500kΩ
Switching frequency	700kHz~800kHz	
Die size	3800μm x 1720μm (including pads)	

5.2 SIDBHO Converter

Fig. 40 shows the measurement result of SIDBHO Converter, positive output voltage reaches nearly 5V and negative voltage nearly -9.2V in clock frequency of 770kHz.

Measure	P1:mean(C1)	P2:mean(C2)	P3:mean(C3)	P4:pkpk(C3)	P5:widn(C2)	P6:freq(C1)
value	4.957 V	1.6 mV	-9.17 V	2.3 V	631.600 ns	44.66313 MHz
status	✓	✓	✓	✓		

Fig. 40. Measured Waveform of SIDBHO-part I.

It presents the stability of high duty conversion ratio in dc dc converter combing boost and flyback function. In Fig. 41 shows the minimum voltage of negative channel achieves nearly -20V but in the problem of not high enough in positive channel since t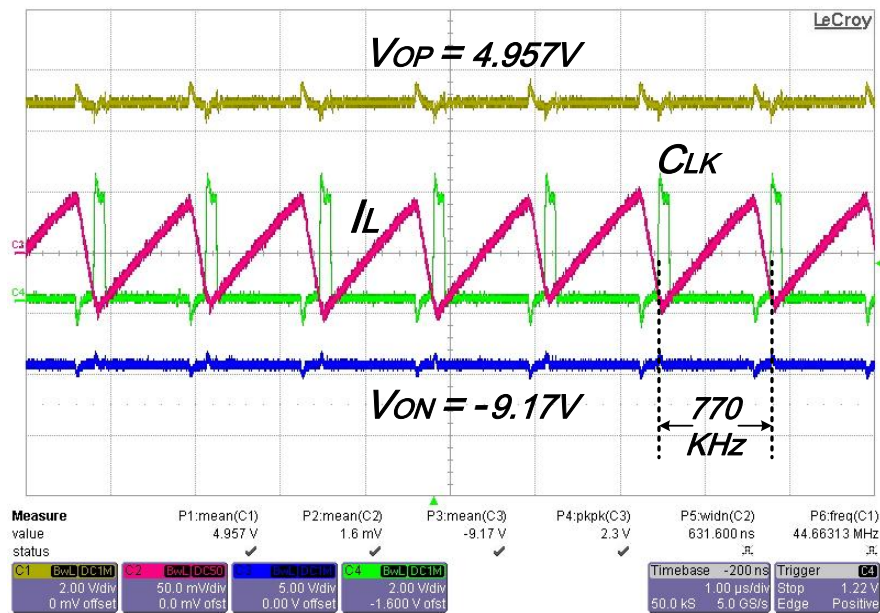he leakage current happens in switching capacitor structure which supports the driver in boost part. Instead, in the implementation environment, diode parallel to M_3 in the high-side of boost converter in Fig. 25 is applied to verify the function of close-loop, but to avoid the over-stress happens, the highest positive output voltage can only arrive nearly 7V in maximum tolerance range.

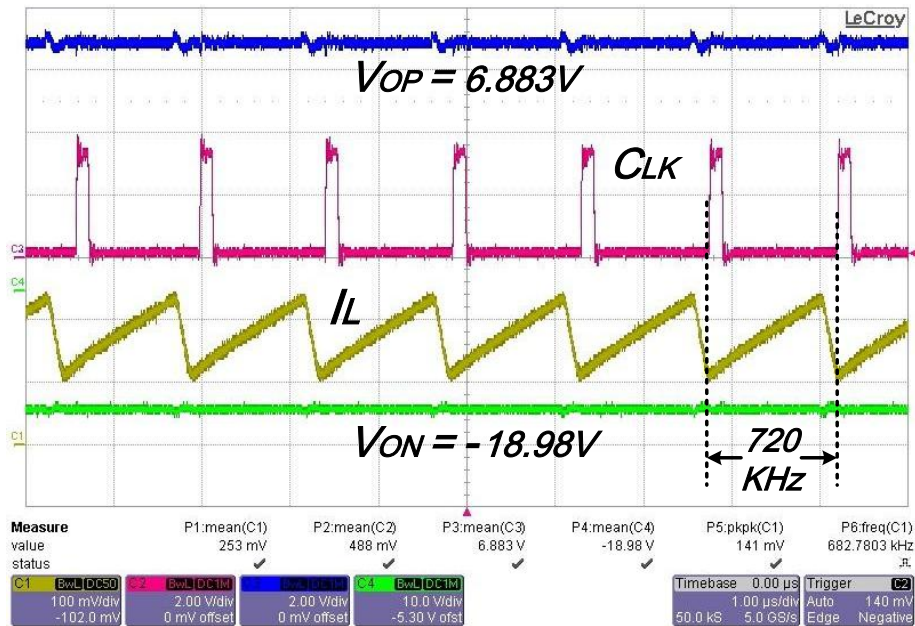Fig. 41. Measured Waveform of SIDBHO-part II.

5.3 Self Bias Switching Capacitor

As mentioned in last paragraph, leakage problem happens because the wrong biasing on body terminal of each transistor, and it causes large leakage due to the wrong voltage bias in Deep N-well and NBL. Fortunately the power of this structure separates from others to make SIDBHO workable, but still have an impact on it.
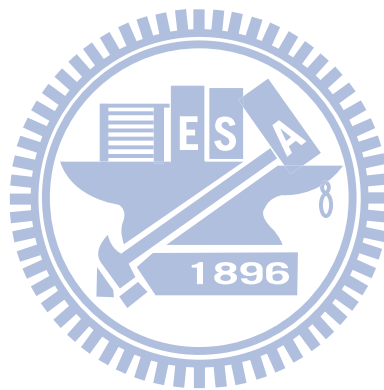
Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this work, a single inductor dual/bipolar high voltage outputs technique is proposed. Accompany with slope compensation and Type II system compensation, two channel positive and negative high voltages dc dc converter can be proved stable. Owing to the proposed technique, it largely reduces area occupation comparing to conventional boost converter and solves the dilemma of efficiency and driving capability in charge pumping power supplies. Moreover, SIDBHO uses its characteristics and makes it possible to integrate controller and energy delivery elements facing high voltages inside chip. In addition, the concept of fully balanced self biasing switching capacitor topology is proposed to not only provide specific driver for SIDBHO structure, but to generate multiple outputs with lower driving ability to apply to gray level implementation. The test chip was fabricated by TSMC 0.25μm BCD process, and experimental results show the verification of maximum up to nearly 7V in positive channel and minimum down to near -20V in negative channel.

6.2 Future Work

Proposed fully balanced self biasing switching capacitor topology support for SIDBHO and gray level driving, which overcomes the cost of charge pump and provide two extra functions and makes itself valuable. But there's problem in designing circuits when circuits' implementation. In the future works, to fix the leakage problem is the most urgent mission.

After completely verifying SIDBHO and fully balanced self biasing switching capacitor structure, highly integration of the circuits mentioned above and multi-channel Gate/Source Driver with timing control inputs is the next step to process, which finally reaches all-in-one integrated circuit to provide next generation product of paper-like cholesteric liquid crystal display.

Reference

[1] "Competitive Display Technologies White Paper," *Qualcomm International, Inc*, Jan. 2007.

[2] Ya-Ling Huang, Andy Ying-Guey Fuh, "The paper-like cholesteric liquid crystal display," *Department of Physics, National Cheng Kung University*, Jan. 2005.

[3] The Barrett Research Group, "Introduction to Liquid Crystals," *Exploring Physical Polymer Chemistry & Thin Film Optics in the Department of Chemistry, McGill University, Montréal*.

[4] Yi-Pai Huang, "Process and Module Technology in STN Liquid Crystal Flat Display" *Lecture Note 3*, Oct, 2010.

[5] Yang-Ching Lin, Ke-Horng Chen, "Dual Side Dual Output Switching Capacitor Voltage Converter for TFT-LCD Driver IC," *A Thesis Submitted to College of Electrical and Computer Engineering, National Chiao Tung University*, Dec. 2010.

[6] Deng-Ke Yang, Xiao-Yang Huang, and Yang-Ming Zhu, "BISTABLE CHOLESTERIC REFLECTIVE DISPLAYS: Materials and Drive Schemes" *Annual Review of Materials Science,* Vol. 27: 117-146, Aug., 1997.

[7] Department of New Technology, Research Center, "Driving Requirement for Cholesteric Liquid Crystal,**" *CHUNGWHA PICTURE TUBES, LTD,* Oct., 2010.

[8] David J.R.Cristaldi, Salvatore Pennisi, Francesco Pulvirenti "Liquid Crystal Display Drivers-Techniques and Circuits". *Springer ISBN 978-90-481-2254-7*, 2009.

[9] Hong-Wei Huang, Chia-Hsiang Lin, and Ke-Horng Chen, "Low-Dropout Regulators with Adaptive Reference Control and Dynamic Push-Pull Techniques for Enhancing Transient Performance," *the 34th European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2008.

[10] Huan-JenYang, Han-Hsiang Huang, Chi-Lin Chen, Ming-Hsin Huang, and Ke-Horng

Chen, "Current Feedback Compensation (CFC) Technique for Adaptively Adjusting the Phase Margin in Capacitor-Free LDO Regulators," *51th IEEE Int'l Midwest Symposium on Circuits & Systems*, Aug. 2008.

[11] Yung-Hsin Lin, Kuo-Lin Zheng, and Ke-Horng Chen, "Power MOSFET Array for Smooth Pole Tracking in LDO Regulator Compensation," *50th IEEE Int'l Midwest Symposium on Circuits & Systems/5th IEEE Int'l Northeast Workshop on Circuits & Systems*, pp. 554-557, Aug. 2007.

[12] P. Favrat, P. Deval and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.

[13] Starzyk, J.A, Ying-Wei Jan and Fengjing Qiu, "A DC-DC charge pump design based on voltage doublers," *IEEE Trans. Circuits and Systems I,* vol. 48, pp. 350-359, Mar. 2001.

[14] Chun-Yu Hsieh, Po-Chin Fan and Ke-Horng Chen**,** "A Dual Phase Charge Pump with Compact Size,**"** *the 14th IEEE International Conference on Electronics, Circuits and Systems,* pp.202-205*,* Dec., 2007.

[15] Yean-Kuo Luo, Ke-Horng Chen, and Wei-Chou Hsu, "A Dual-Phase Charge Pump Regulator with Nano-Ampere Switched-Capacitor CMOS Voltage Reference for Achieving Low Output Ripples,**"** *the 15th IEEE International Conference on Electronics, Circuits and Systems,* Sep., 2008.

[16] Cheung Fai Lee, Philip K. T. "A Monolithic Current-Mode CMOS DC-DC Converter with On-Chip Current-Sensing Technique,". *IEEE J. Solid-State Circuits*. vol. 39, pp.3-13, Jan. 2004.

[17] Chi Yat Leung, Philip K.T. Mok, "A 1-V Integrated Current-Mode Boost Converter in Standard 3.3/5-V CMOS Technologies," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, Nov. 2005.

[18] Ming-Hsin Huang, Ke-Horng Chen**,** and Wei-Hsin Wei "Single-Inductor Dual-Output DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation

for Portable Devices," *IEEE VLSI-Symposium on Technology and Circuits*, June, 2008.

[19] Hong-Wei Huang, Hsin-Hsin Ho, Chieh-Ching Chien, Ke-Horng Chen, Gin-Kou Ma, and Sy-Yen Kuo, "Dithering Skip Modulator with a Width Controller for Ultra-wide-load High-Efficiency DC-DC Converters," *2006 IEEE Custom Integrated Circuits Conference (CICC),* Sep. 10-13, 2006.

[20] Yu-Huei Lee, Shih-Jung Wang, Chun-Yu Hsieh, and Ke-Horng Chen, "Current Mode DC-DC Buck Converters with Optimal Fast-Transient Control," in *Proc. IEEE Int. Symp. Circuits Syst.*, May. 2008.

[21] G. Reza Chaji and Arokia Nathan, "A Fast Settling Current Driver Based on the CCII for AMOLED Displays," *IEEE Journal of Display Technology*, Vol. 1, No. 2, Dec 2005.

[22] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, K.S.Karim, D. Striakhilev, "Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic, " *IEEE J. of Solid State Circuits*, vol. 39, pp. 1477-1486, Sept. 2004.

[23] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *IEEE Electron Device Letters*, vol. 25, pp. 188-190, Apr. 2004.

[24] James L. Sanford and Frank R. Libsch, "TFT AMOLED Pixel Circuits and Driving Methods," *in SID Int. Symposium*, pp. 10-13, May 2003.

[25] Joon-Chul Goh, Jin Jang, Member, IEEE, Kyu-Sik Cho, and Choong-Ki Kim, "A New a-Si:H Thin-Film Transistor Pixel Circuit for Active-Matrix Organic Light-Emitting Diodes," *IEEE electron device letters*, vol. 24, pp. 583-585, Sept. 2003.

[26] "Advanced Low Power High Voltage Asic for the Development of Display Driving Schemes," *IMEC*, Jun. 2004.

[27] "MXED401-200-Column Cholesteric LCD Driver," *Clare-An IXYS Company*, Jan. 2003.

[28] Bayer, E.; Thiele, G., "A single-inductor multiple-output converter with peak current

state-machine control," *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE* , vol., no., pp. 7 pp.-, 19-23 March 2006

[29] Suet-Chui Koon, Yat-Hei Lam, and Wing-Hung Ki, "Integrated charge-control single-inductor dual-output step-up/step-down converter," *IEEE International Symposium on Circuit and Systems*, vol. 4, pp. 3071-3074, May 2005.

[30] Dongsheng Ma, Wing-Hung Ki, Chi-Ying Tsui, Philip K. T. Mok, "Single-Inductor Multiple-Output Switching Converters with Time-Multiplexing Control in Discontinuous Conduction Mode," *IEEE Journal Solid-State Circuits*, NO. 1, pp. 89-100, Jan. 2003.

[31] Bonizzoni, E., Borghetti, F., Malcovati, P., Maloberti, F., and Niessen, B., "A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter," *ISSCC Digest of Technical Papers*, pp. 526 – 619, Feb. 2007.

[32] M. W. May, M. R. May, John E. Willis, "A Synchronous Dual-Output Switching dc-dc Converter Using Multibit Noise-Shaped Switch Control," *ISSCC Digest of Technical Papers*, pp. 358-359, Feb. 2001.

[33] Pizzutelli, A. and Ghioni, M., "Novel control technique for single inductor multiple output converters operating in CCM with reduced cross-regulation," *Applied Power Electronics Conference and Exposition,* pp. 1502-1507, Feb 2008.

[34] Belloni, M., Bonizzoni, E., and Maloberti, F., "On the design of single-inductor multiple-output DC-DC buck converters," *IEEE International Symposium on Circuit and Systems*, pp. 3049-3052, May 2008.

[35] Belloni, M., Bonizzoni, E., Kiseliovas, E., Malcovati, P., Maloberti, F., Peltola, T., and Teppo, T., "A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current," *ISSCC Digest of Technical Papers*, pp. 444-626, Feb. 2008.

[36] Ming-Hsin Huang, Ke-Horng Chen**,** and Wei-Hsin Wei "Single-Inductor Dual-Output

DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices," *IEEE Symposium on VLSI Circuits*, pp. 132-133, June, 2008.

[37] Dongsheng Ma, Wing-Hung Ki, and Chi-Ying Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE Journal of Solid-State Circuits,* Volume 38, Issue 6, pp. 1007-1014, June 2003.

[38] Young-Jin Woo, Hanh-Phuc Le, Gyu-Ha Cho, Gyu-Hyeong Cho, and Seong-Il Kim, "Load-Independent Control of Switching DC-DC Converters with Freewheeling Current Feedback," *IEEE International Solid-State Conference*, pp. 446-626, Feb. 2008.

[39] Sharma, A. and Pavan, Y.S., "A single inductor multiple output converter with adaptive delta current mode control," *IEEE International Symposium on Circuit and Systems*, pp. 5643-5646, May 2006.

[40] Hanh-Phuc Le, Chang-Seok Chae, Kwang-Chan Lee, Se-Won Wang, Gyu-Ha Cho, and Gyu-Hyeong Cho, "A Single-Inductor Switching DC–DC Converter With Five Output and Ordered Power-Distributive Control," *IEEE Journal of Solid-State Circuits,* pp. 2706-2714, Dec. 2007.

[41] Saravanan Rajapandian, Kenneth Shepard, Peter Hazucha, Tanay Karnik, "High-Tension Power Delivery: Operating 0.18 m CMOS Digital Logic at 5.4V," *IEEE International Solid-State Circuits Conference*, 2005.

[42] Yusuke Kanno, Hiroyuki Mizuno, Knzuo Tanaha,and Takao Watanabe, "Level Converters with High Immunity to Power-Supply Bouncing for High-speed Sub-1-V LSIs," *IEEE Symposium on VLSI Circuits Digest of Technique Papers*, 2000.

[43] Robert W. Erickson and Dragan Maksimović, Fundamentals of Power Electronics. Norwell, MA: Kluwer, 2001.

[44] Hassan Pooya Forghani-zadeh, Gabriel A. Rincon-Mora, "Current-Sensing Techniques for DC-DC Converters" *IEEE Circuits and Systems,* Vol. 2, 2002

[45] Kaiwei Yao, Kisun Lee, Ming Xu, and Fred C. Lee, "Optimal design of the active droop

control method for the transient response," in *Proc. Applied Power Electronics Conference and Exposition*, vol. 2, pp. 718-723, Feb. 2003.

[46] Lu Chen and Bruno Ferrario, "Adaptive Frequency Compensation for DC-to-DC converter," *US Patent 20060176098*, Aug. 10, 2006.

[47] Ke-Horng Chen, Hong-Wei Huang, and Sy-Yen Kuo, "Fast-Transient DC-DC Converter with On-Chip Compensated Error Amplifier," *IEEE Trans. Circuits Syst. II*, *Exp. Briefs*, vol. 54, no. 12, pp. 1150-1154, Dec. 2007.

[48] Hong-Wei Huang, Hsin-Hsin Ho, Chieh-Ching Chien, Ke-Horng Chen, Gin-Kou Ma, and Sy-Yen Kuo, "Fast Transient DC-DC Converter with On-Chip Compensated Error Amplifier," in *Proc. European Solid-State Circuits Conference*, pp. 324-327, Sep. 2006.