國立交通大學

電控工程研究所

碩士論文

返馳式轉換器之數位式初級側感測控制

Digital Primary-Side Sensing Control for Flyback Converters

研究生：張哲瑋

指導教授：鄒應嶼 博士

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中文摘要

本論文針對返馳式轉換器之數位式初級側感測控制方法進行設計，可用於不連續導通模式之直流返馳式轉換器以及不連續導通模式、具功率因數修正之返馳式整流器。初級側感測方法可藉由輔助線圈來達到輸出電壓或電流的控制。然而，根據初級側感測誤差的分析，感測電壓會受到漏電感、線阻及次級側二極體壓降影響，因此，感測電壓只能達到有限的精準度。在不連續導通模式之直流返馳式轉換器的應用中，感測誤差可以藉由取樣時間調變來加以改善。透過取樣時間調變的方法，當負載大小從 20%變化至 100%時，輸出電壓在穩態時僅有 1%的誤差且電壓壓降於切載時亦可控制在額定輸出電壓的 4.7%。此外，將初級側感測方法用於不連續導通模式、具功率因數修正之返馳式整流器時，感測電壓在整流後輸入電壓接近零交越點時，因可供取樣的時間很短，不易取得正確的輸出電壓回授訊號。因此，採用多模式的控制演算法來克服此問題。當系統在整流後輸入電壓接近零交越點時，採用開迴路控制，而在其餘時間則採用預設的閉迴路控制。藉由此方法，輸入電流的總諧波失真在額定負載時僅有 4.5%。在本論文中，利用一顆德州儀器公司的數位訊號處理晶片 TMS320F2812 來實現初級側感測控制方法。

Digital Primary-Side Sensing Control for Flyback Converters

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Abstract

This thesis presents the design and realization of primary-side sensing (PSS) technique for discontinuous-conduction-mode (DCM) DC-DC flyback converters or flyback rectifiers with power factor correction (PFC). PSS technique can be used for the output voltage or current regulation by employing an auxiliary winding. However, by analyzing the primary-side sensing error, the sensed voltage from the auxiliary winding may be corrupted by switching noise due to leakage inductance, winding resistance, and the voltage drop of the secondary diode, therefore the sensed voltage can only achieve limited accuracy. The sensing error can be improved by sampling instant modulation for DCM DC-DC flyback converters. The voltage regulation has only 1% deviation and the voltage drop is only 4.7% of the nominal output voltage when the load power is from 20% to 100%. When utilizing PSS technique for DCM PFC flyback rectifiers, the sensed voltage is difficult to be obtained at the neighborhood of zero crossing of the rectified input voltage. Therefore, a multimode control algorithm is implemented to overcome this problem. The system is under open-loop control at the neighborhood of zero crossing and closed-loop control when the correct sensed voltage is able to be obtained. By this method, the total harmonic distortion (THD) of the ac line current is only 4.5% at the rated output power. In this thesis, PSS technique is realized by a digital signal processor (DSP), TMS320F2812 from Texas Instrument (TI).

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張哲瑋

2009 秋天 於新竹交大

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Chapter 1

Introduction

1.1 Research Background and Recent Development

Flyback converter topology gets its wide applications in low-power and low-cost isolated switching power supplies due to its low component counts without a secondary output filter inductor. Conventional flyback converters utilize an error amplifier and an opto-coupler to implement the voltage feedback compensation and galvanic isolation.

Low-cost opto-couplers suffer from the current transfer ratio (CTR) degradation due to temperature rise. This makes a serious limitation on operating temperature for flyback converters. The elimination of the opto-coupler provides significant advantages such as higher power density, cost down, and lower standby power. Therefore, primary-side sensing (PSS) technique, which senses the output voltage from the primary or auxiliary winding of the transformer without using the opto-coupling circuit, becomes an important issue for the development of more sophisticated flyback control ICs.

Another motivation to develop PSS technique is that there is a low frequency pole at 20-30 kHz from the opto-coupler. This pole complicates the feedback loop design and limits the crossover frequency. Recently, in order to get a higher bandwidth in voltage loop, engineers may implement secondary-side control, which places the controller at the secondary side and transmits the pulse-width-modulation (PWM) signal through a pulse transformer or a high-speed photodetector to eliminate the low frequency pole, but the start-up circuit for the controller at the secondary side needs the electrical isolation from the input power [1]. Hence,

PSS technique combines the advantages of primary-side control and secondary-side control to become an attractive choice.

PSS technique can extract the output voltage from the primary side because the output voltage appears on the primary winding during the power switch off state [2]-[6].

$$v_{DS} = v_{in} + \frac{N_p}{N_s} v_{o.} \tag{1-1}$$

The voltage across the switch contains the information of the output voltage during off state as shown in (1-1). With the AC line input, this method may require the implementation of high voltage sensing circuits and suffer from coupling noises due to primary leakage inductance. The schematic diagram to extract the output voltage from the voltage across the switch is shown in Fig. 1.1.

Another approach is to adopt an additional auxiliary winding to detect the output voltage [7]-[11].

$$v_{aux} = \frac{N_a}{N_s} v_o. \tag{1-2}$$

This auxiliary winding can be used for both power supplying and voltage sensing and it provides advantages such as low-voltage IC manufacturing process for the implementation of CMOS controller for cost reduction, better winding mechanism for the reduction of coupling noises, lower standby power consumption using the same IC manufacturing process. The schematic diagram to extract the output voltage from the auxiliary winding is shown in Fig. 1.2. This thesis focuses on the second approach which senses the output voltage from the auxiliary winding.

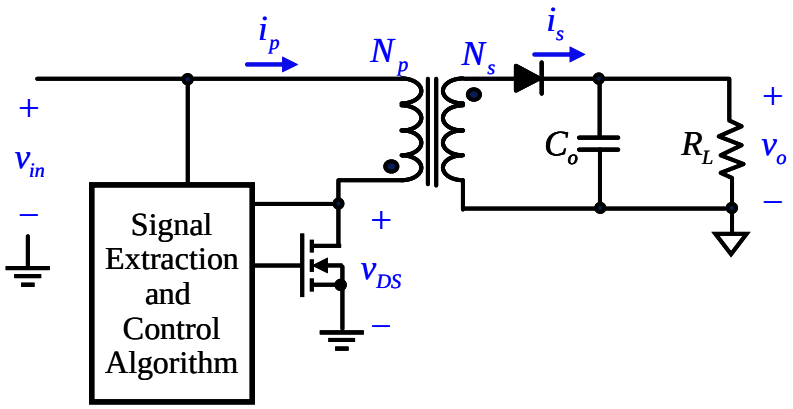


Fig. 1.1. Extract the output voltage from the voltage across the switch.

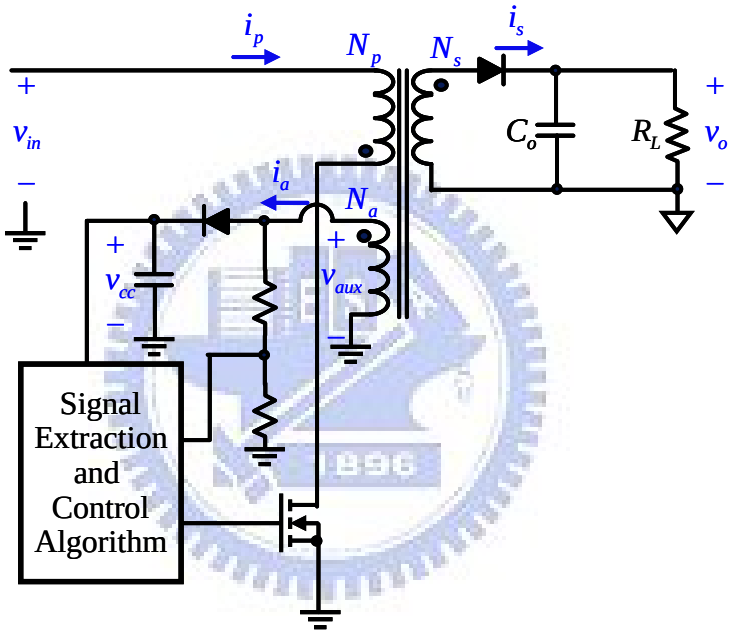


Fig. 1.2. Extract the output voltage from the auxiliary winding.

1.2 Research Motivation and Objectives

The accuracy of sensing output voltage indirectly from the auxiliary winding will be influenced by practical factors, such as cross coupling effect, voltage drop across the secondary diode, and switching oscillations induced by leakage inductance, magnetization inductance, and the output junction capacitance of the switching device. Commercial flyback transformers must provide galvanic isolation between primary and secondary in accordance with the regulatory agencies of the intended market, such as IEC950 in Europe and UL1950

in the U.S. Different approaches can be adopted to meet the required safety regulations. Cores and bobbins are usually selected large enough meet the creepage distance requirement as well as to maintain transformer coupling and reduce leakage inductance. Cross coupling between transformer windings will corrupt accuracy of the sensing voltage for output voltage detection. The cross regulation in multiple-output flyback converters is mainly affected by leakage inductances of the transformers and this effect can be reduced by proper winding arrangements of the transformers [12].

Analytical model and small-signal analysis for cross regulation of a flyback converter with multiple outputs have been developed in [13]-[14]. The auxiliary winding is identical to an output winding with very low power consumption and the analytical model can be used for the analysis of the coupling effect between the main output voltage and the voltage of the auxiliary winding. This thesis makes an error analysis of PSS technique due to the leakage inductance and other key parameters when applying to flyback converters, and presents the design and realization of PSS technique for discontinuous-conduction-mode (DCM) DC-DC flyback converters or flyback rectifiers with power factor correction (PFC).

1.3 THESIS ORGANIZATIONS

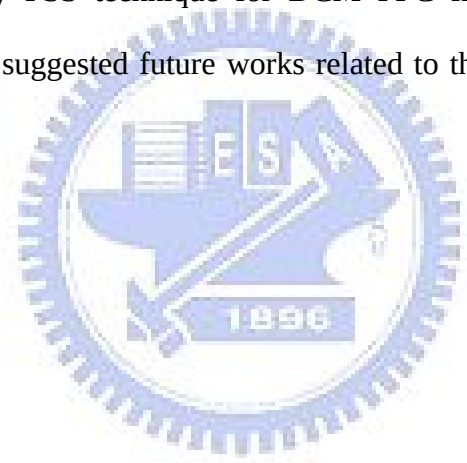
The thesis is organized as follows. The fundamentals of flyback converters are introduced in Chapter 2, and the effects with parasitic elements and the determination of components for flyback converters are also mentioned.

In Chapter 3, a proposed digital PSS technique is presented and the PSS error is analyzed in detail. In addition, the determination of the sampling instant is also described and implemented by a fixed-point digital-signal processor (DSP), TMS320F2812.

In Chapter 4, a DCM DC-DC flyback converter with the proposed PSS technique is developed to show the usability of PSS technique. The dynamic model of this system is

derived to design the digital voltage controller, and PSS control algorithm is designed with sampling instant modulation to reduce the effect of the sensing error. The experimental results are also shown in this chapter to verify PSS technique for DCM DC-DC flyback converters.

In Chapter 5, the proposed PSS technique can be extended to control a DCM PFC flyback rectifier. At the beginning of this chapter, it explains the self PFC property for flyback rectifiers operating in DCM, and then, derives the dynamic model for DCM flyback rectifiers. The PSS control algorithm is modified to adapt the conditions with a rectified input voltage. The control algorithm is separated into two modes to overcome the problem for sampling the sensed voltage at the neighborhood of zero crossing. The experimental results are also shown in this chapter to verify PSS technique for DCM PFC flyback rectifiers. Finally, Some concluding remarks and suggested future works related to this research are summarized and discussed in Chapter 6.



Chapter 2

Fundamentals of Flyback Converters

A flyback converter is also called “isolated buck-boost converter” because it is derived from a buck-boost converter. The buck-boost converter shown in Fig. 2.1(a) delivers a negative output voltage referenced to the input ground without isolation. A negative output voltage is inconvenient to implement some applications, but the property of buck-boost converters that the output voltage can be higher or lower than the input voltage is necessary to the applications which have wide input ranges. By swapping the positions of the inductor and the switch in Fig. 2.1(a), a similar arrangement is kept in Fig. 2.1(b), but the output voltage is referenced to the input rail. Then, replacing the inductor with an air-gapped transformer, we obtain an isolated flyback converter shown in Fig. 2.1(c). The flyback transformer configuration helps to adopt polarity by playing on the winding dot and the diode orientation, so the polarity of the output voltage on the flyback converter can be either positive or negative.

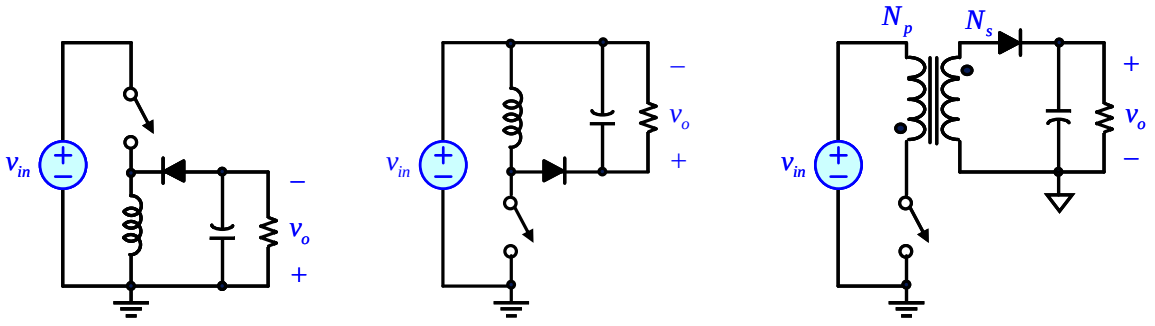


Fig. 2.1. Procedure to derive a flyback converter from a buck-boost converter: (a) buck-boost converter referenced to the input ground, (b) buck-boost converter referenced to the input rail, (c) flyback converter.

2.1 OPERATING PRINCIPLE OF DCM FLYBACK CONVERTERS

Fig. 2.2(a) portrays an ideal flyback converter without parasitic elements when the switch is closed. During this time, the voltage across the magnetizing inductance L_M is equal to the input voltage v_{in} (neglect the voltage drop across the switch). Then, the inductor current increases at a rate defined by

$$S_{on} = \frac{v_{in}}{L_M}. \tag{2-1}$$

The peak inverse voltage (PIV) on the secondary diode during the on time is

$$\text{PIV} = \frac{v_{in}}{n_{ps}} + v_o \tag{2-2}$$

where $n_{ps} = N_p / N_s$. N_p and N_s are the turns of the primary winding and the secondary winding, respectively. Fig. 2.2(b) portrays an ideal flyback converter when the switch is open. During this time, the voltage across the magnetizing inductance L_M is equal to the output voltage v_o multiplied by the turns ratio n_{ps} from the primary winding to the secondary winding. Then, the inductor current decreases at a rate defined by

$$S_{off} = -\frac{n_{ps} v_o}{L_M}. \tag{2-3}$$

Fig. 2.2(c) portrays an ideal flyback converter when the switch is open and the magnetizing inductor is reset.

In this thesis, the flyback converter always operates in DCM, so the following discussion focuses on the properties of flyback converters in DCM. When the flyback converter operates in DCM, there are three states defined as on state, off state, and reset state. The energy stored in the flyback transformer is zero in reset state. The waveforms of the primary current i_p, the secondary current i_s, and the magnetizing current i_M are shown in Fig. 2.3. The property of

voltage conversion is derived firstly, and the waveforms with parasitic elements in DCM are shown. Then, the peak value of the drain-to-source voltage of the switch during the off state is calculated, so a clamping network is necessary to protect the switch against the breakdown voltage. Finally, an *RCD* clamping network is designed.

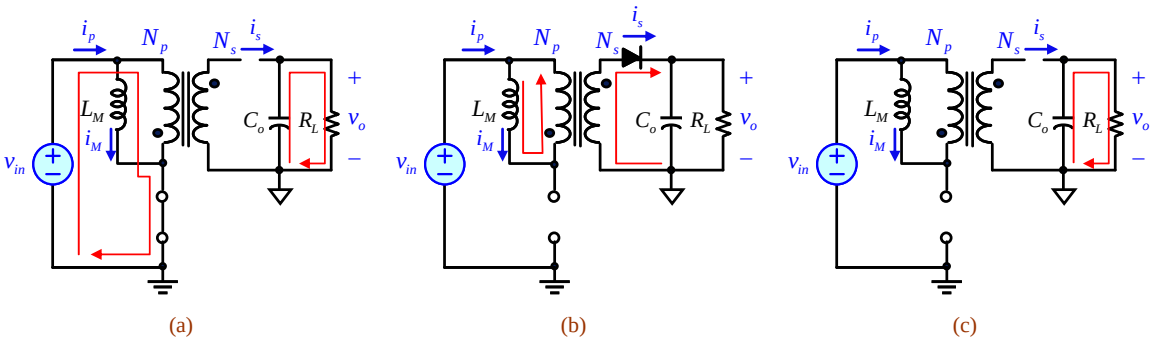


Fig. 2.2. (a) During the on time, the output capacitor supplies the load on its own. (b) During the off time, the voltage across the switch is the input voltage plus the output voltage multiplied by the turns ratio n_{ps}. (c) When the magnetizing inductor is reset, the output capacitor supplies the load on its own.

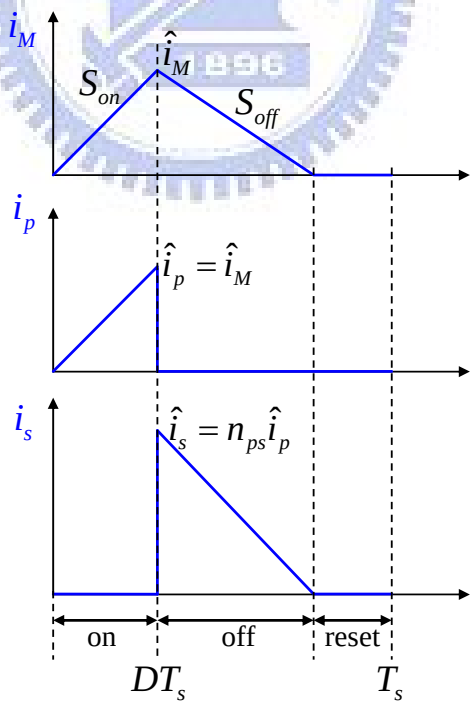


Fig. 2.3. Current waveforms of the flyback converter in DCM.

2.1.1 Voltage Conversion Ratio in DCM

To derive the voltage conversion ratio in DCM, the procedure is easy with an assumption that the input power P_{in} is equal to the output power P_o. The input power is derived from the primary current as

$$P_{in} = \frac{1}{2} L_M \hat{i}_p^2 f_s = \frac{v_{in}^2}{2L_M} D^2 T_s \tag{2-4}$$

where D is the duty ratio in steady state and T_s is the switching period. The output power can be expressed by the output voltage and the load resistance R_L as

$$P_o = \frac{v_o^2}{R_L}. \tag{2-5}$$

Combining (2-4) and (2-5), the voltage conversion ratio in DCM is derived as

$$\frac{v_o}{v_{in}} = D\sqrt{\frac{R_L T_s}{2L_M}} = \frac{D}{\sqrt{K}} \tag{2-6}$$

where $K = \frac{2L_M}{R_L T_s}$.

From (2-6), it reveals a fact that the turns ratio n_{ps} does not affect the voltage conversion ratio when the flyback converter operates in DCM. However, the turns ratio n_{ps} actually affects the critical magnetizing inductance L_{crit}, which determines the flyback converter operates in continuous-conduction mode (CCM) or DCM. The critical magnetizing inductance L_{crit} is determined by

$$L_{crit} = \frac{R_L T_s n_{ps}^2}{2\left(1 + \frac{n_{ps} v_o}{v_{in}}\right)^2}. \tag{2-7}$$

2.1.2 Effects of Parasitic Elements in DCM

In the previous section, the considered flyback converter is ideal. There are some important parasitic elements such as the leakage inductor in the primary winding, the junction capacitor of the switch, and the equivalent series resistor (ESR) of the output capacitor. The

most important waveform is the voltage on the switch. Because of the leakage inductance in the primary winding and the junction capacitor of the switch, the voltage on the switch will oscillate in off state and may destroy the switch. The voltage on the switch in off state with parasitic elements can be derived by solving the differential equations as follows

$$\begin{aligned} C_{DS}\frac{dv_{DS}(t)}{dt} &= i_p(t) \\ L_{lkp}\frac{di_p(t)}{dt} &= v_{in} + n_{ps}(v_o + v_D) - v_{DS}(t) \end{aligned} \tag{2-8}$$

where C_{DS} is the junction capacitance of the switch, L_{lkp} is the leakage inductance in the primary winding, v_D is the voltage drop of the secondary diode, and v_{DS} is the voltage on the switch. The relative circuit schematic is shown in Fig. 2.4. To solve the ODE in (2-8), the initial conditions should be obtained, which are

$$\begin{aligned} v_{DS}(0) &= v_{in} + n_{ps}(v_o + v_D) \\ \dot{v}_{DS}(0) &= \frac{i_p(0)}{C_{DS}} = \frac{\hat{i}_p}{C_{DS}}. \end{aligned} \tag{2-9}$$

The voltage on the switch in off state can be obtained from (2-8) with initial conditions in (2-9) as

$$v_{DS}(t) = v_{in} + n_{ps}(v_o + v_D) + \hat{i}_p Z_p \sin(\omega_{lk} t) \tag{2-10}$$

where Z_p is the characteristic impedance and ω_{lk} is the resonant frequency of $L_{lkp}C_{DS}$ circuit defined as

$$\begin{aligned} Z_p &= \sqrt{\frac{L_{lkp}}{C_{DS}}} \\ \omega_{lk} &= \sqrt{\frac{1}{L_{lkp}C_{DS}}}. \end{aligned} \tag{2-11}$$

The peak value of the voltage on the switch is estimated from (2-10) as

$$v_{DS,\max} = v_{in} + n_{ps}(v_o + v_D) + \hat{i}_p Z_p. \tag{2-12}$$

This should not be over the breakdown voltage, so a clamping network is necessary

when designing a flyback converter. The design of clamping network is discussed in section 2.2.

Another effect caused by the ESR of the output capacitor appears on the output voltage. If the converter operates in DCM, this effect is more obvious because the peak of the secondary current is generally higher than the condition in CCM. The AC component of the secondary current will flow through the output capacitor and cause a voltage ripple on the output voltage. The relative waveforms are shown in Fig. 2.5. The ESR r_c of the output capacitor can be estimated as

$$r_c = \frac{V_{esr}}{\hat{i}_s - I_o} \tag{2-13}$$

where V_{esr} is the peak-to-peak value observed on the output voltage ripple. The output voltage ripple has two components. One is caused by the discharge of the output capacitor and the other is caused by the ESR. The ripple caused by the ESR may be a problem to violet the specification although the output capacitor is selected very large. Therefore, in some cases, an output *LC* filter is necessary to improve the situation.

If more accurate values of the parasitic elements are needed to know, observing the drain-source waveforms of a flyback converter can teach designer a lot. A drain-source waveform in DCM is shown in Fig. 2.6. To determine the parasitic elements, there are several equations to use such as

$$S_{on} = \frac{v_{in}}{L_M + L_{lkp}} \tag{2-14}$$

$$f_{lk} = \frac{1}{2\pi\sqrt{L_{lkp}C_{DS}}} \tag{2-15}$$

$$f_{DCM} = \frac{1}{2\pi\sqrt{(L_M + L_{lkp})C_{DS}}}. \tag{2-16}$$

Solving these equations gives the parasitic elements as

$$C_{DS} = \frac{S_{on}}{4v_{in} f_{DCM}^2 \pi^2} \tag{2-17}$$

$$L_{lkp} = \frac{1}{4\pi^2 f_{lk}^2 C_{DS}} \tag{2-18}$$

$$L_M = \frac{v_{in} - S_{on} L_{lkp}}{S_{on}}. \tag{2-19}$$

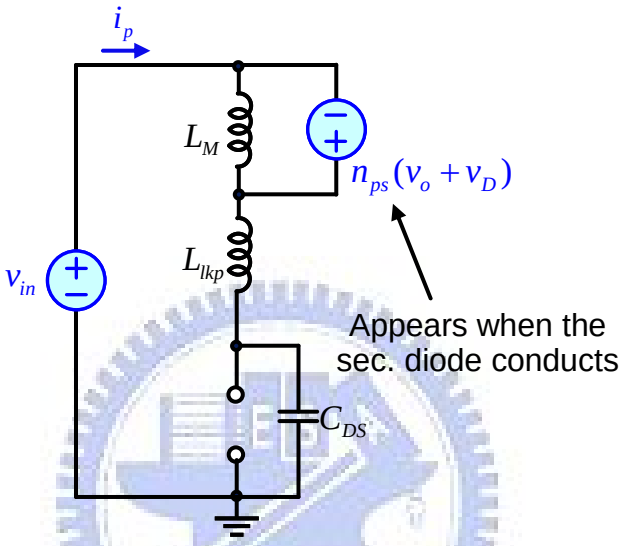


Fig. 2.4. Circuit schematic with parasitic elements after the switch is turned off.

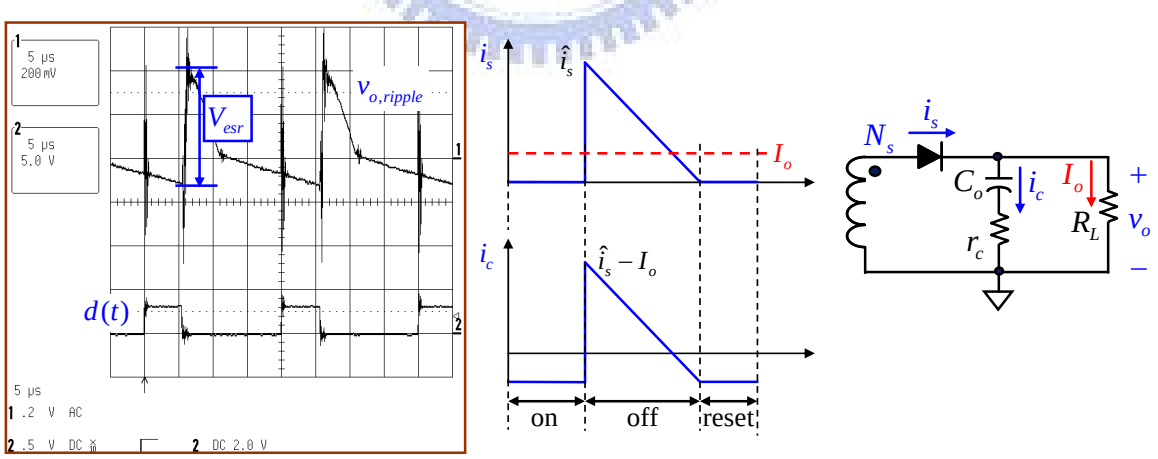


Fig. 2.5. Effect of the ESR and waveforms to estimate the value of the ESR.

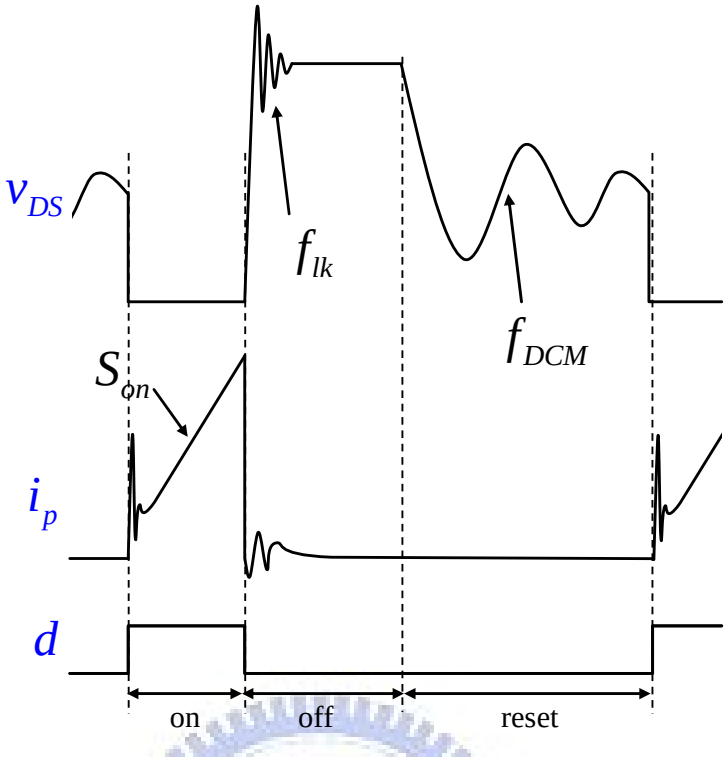


Fig. 2.6. Typical waveforms of flyback converters in DCM with parasitic elements.

2.2 DETERMINATION OF COMPONENTS FOR FLYBACK CONVERTERS

2.2.1 Clamping Network

The clamping network role shown in Fig. 2.7 is to prevent the drain-to-source voltage exceeding the breakdown voltage of a given MOSFET. In general, the breakdown voltage is selected up to 600 V or higher in flyback applications. Firstly, we need to determine the clamping voltage by the equation as follows

$$v_c = BV_{DSS} k_D - v_{in} \tag{2-20}$$

where BV_{DSS} is the breakdown voltage of a given MOSFET and the parameter k_D is a derating factor to reserve a safety margin for design. Moreover, the clamping voltage must be higher than the reflected voltage $n_{ps}(v_o + v_D)$ to authorize the quick leakage term reset in the primary-side leakage inductor. Experience shows that a proper clamping voltage selected as

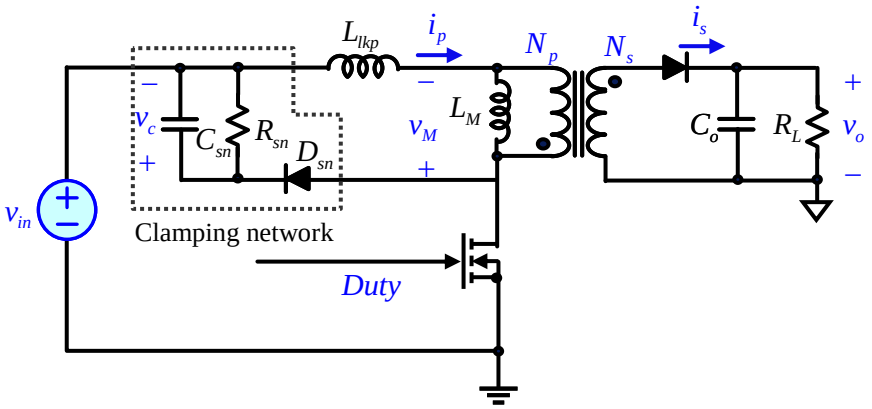


Fig. 2.7. Typical clamping network made by *RCD* circuit.

$$v_c = k_c n_{ps}(v_o + v_D) \tag{2-21}$$

where the parameter k_c is good to be selected between 1.3 to 2. Then, the resistance R_{sn} and the capacitance C_{sn} can be determined by

$$R_{sn} = \frac{2v_c\left[v_c - n_{ps}(v_o + v_D)\right]T_s}{L_{lkp}\hat{i}_p^2} \tag{2-22}$$

$$C_{sn} = \frac{v_c T_s}{R_{sn}\Delta v} \tag{2-23}$$

where Δv is the voltage ripple on the clamping capacitor, which can be selected roughly 20% of the clamping voltage. A more detailed design analysis of the *RCD* snubber can be found in [15].

2.2.2 Power Stage

There are some important components to design for a flyback converter such as the turns ratio from the primary side to the secondary side, the magnetizing inductance, the output capacitance, the power switch, and the secondary diode. The turns ratio can be derived from (2-21) yielding

$$n_{ps} = \frac{v_c}{k_c(v_o + v_D)}. \tag{2-24}$$

The magnetizing inductance is determined by the operating mode and (2-7). For operating in DCM, the magnetizing should be lower than the value in (2-7). The other

important constraints for the power switch, the output capacitor, and the secondary diode are shown in Table 2.1.

TABLE 2.1
CONSTRAINTS FOR THE POWER COMPONENTS

MOSFET	
Breakdown voltage	$BV_{DSS} > v_{in} + n_{ps}(v_o + v_D) + v_c$
RMS current in DCM	$I_{rms} = \hat{i}_p \sqrt{\frac{D}{3}}$
Secondary diode	
Peak repetitive reverse voltage	$V_{RRM} > v_o + \frac{v_{in}}{n_{ps}}$
Continuous current	$I_{F,avg} = I_o$
Output capacitor	
Capacitance	$C_o = \frac{I_o T_s}{\Delta v_o}$

Chapter 3

Digital Primary-Side Sensing (PSS) Control Technique

Fig. 3.1(a) shows the schematic of an ideal flyback converter with PSS, where v_{in} is the input voltage, v_o is the output voltage, v_{aux} is the voltage on the auxiliary winding, and N_p, N_s, and N_a are the turns of each winding respectively.

For an ideal system, assume that all leakage inductances can be ignored and the forward-biased voltage drop of the secondary diode is much smaller than v_o. v_{aux} includes the information of v_o when the power MOSFET is in its off state. If the controller samples v_{aux} in off state before the current i_s decreases to zero, the relation between v_o and v_{aux} can be ideally expressed by

$$v_{aux} = \frac{N_a}{N_s} v_o. \tag{3-1}$$

The waveform of v_{aux} is shown in Fig. 3.1(b).

A Flyback converter stores energy in its transformer when the switch is on and releases this stored energy to its secondary winding and auxiliary winding when the switch is turned off. Because of very low power dissipation of the controller compared to the output load, it can be assumed that the current i_s flowing through the secondary diode is much higher than the current i_a flowing through the auxiliary diode. Fig. 3.2(a) is the proposed system in this paper, where L_M is the magnetizing inductance of the transformer and L_{lkp}, L_{lks}, L_{lka} are corresponding to the leakage inductances in the primary winding, secondary winding and auxiliary winding, respectively. In practice, the voltage on the auxiliary winding imperfectly couples to the output voltage. It will be influenced by leakage inductances, voltage drop on

the secondary diode, and the winding resistance in the secondary winding.

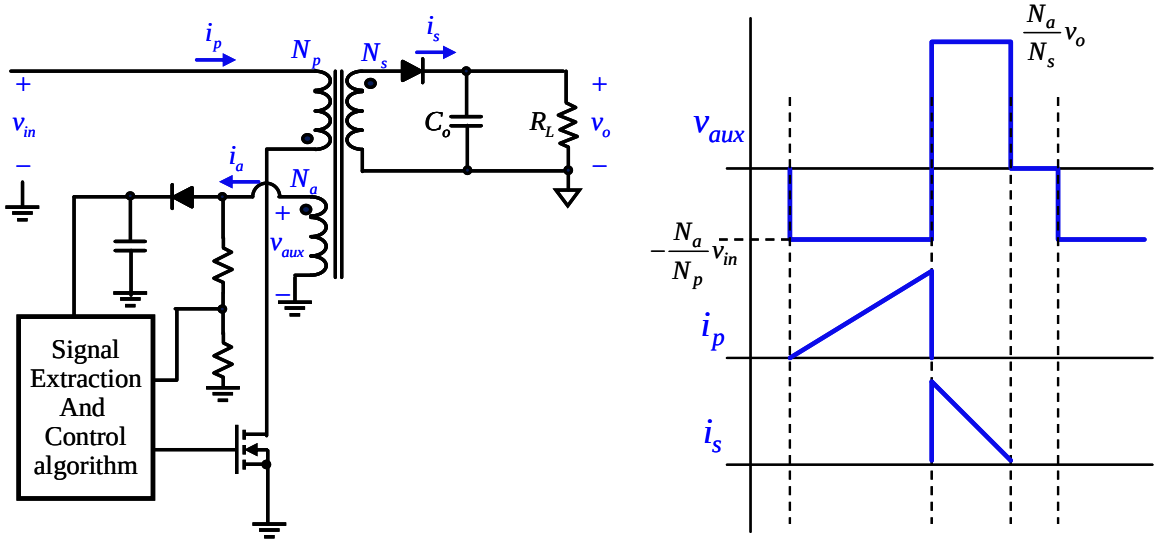


Fig. 3.1. Ideal flyback converter with PSS (a) Schematic, (b) Waveforms.

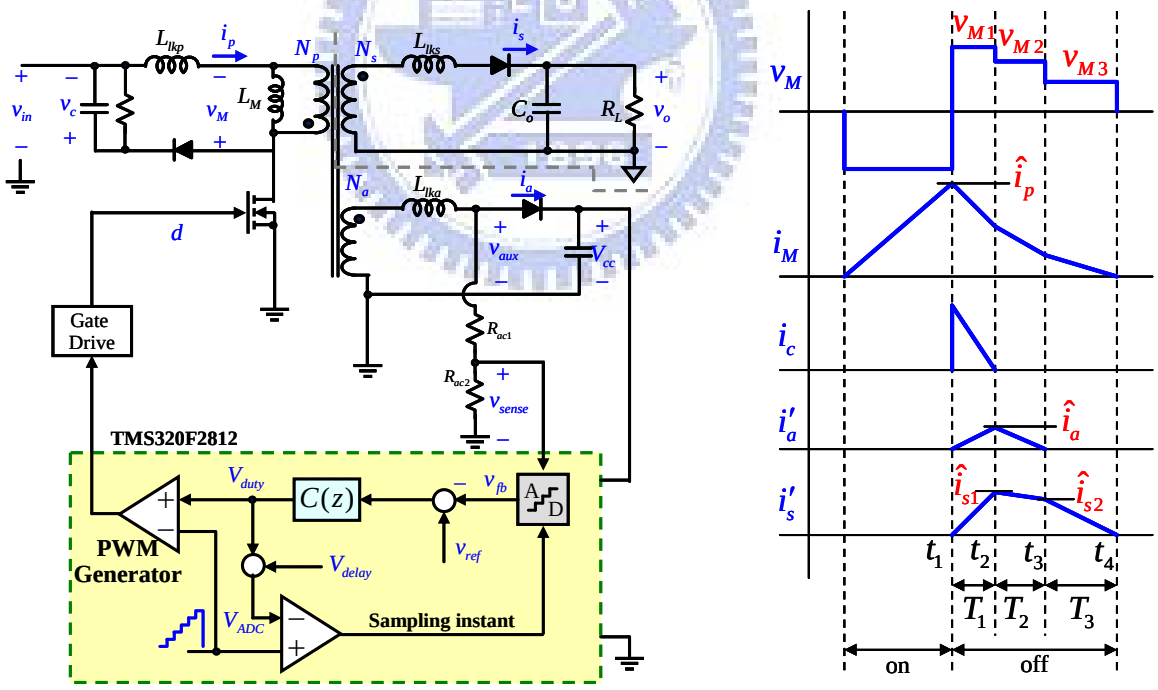


Fig. 3.2. (a) Proposed flyback converter with PSS. (b) Important waveforms through one switching period.

3.1 PRIMARY-SIDE SENSING ERROR ANALYSIS

In order to analyze the sensing error by primary-side sensing, according to [14], convert the components at the secondary side and the auxiliary side to the primary side of the transformer. All parameters converted to the primary side are noted with prime, x'. At the beginning of the error analysis, define three intervals T_1, T_2, and T_3 which are shown in Fig. 3.2(b). The equivalent circuits are derived to match the conditions when the switch is turned off as shown in Fig. 3.3.

For simplicity, assume all capacitors are large enough so that the voltages on them are constant in each interval. When the switch is turned off at the beginning of interval T_1, the equivalent circuit is shown as Fig. 3.3(a). By Kirchhoff's current law (KCL), the sum of current at node M is zero,

$$i_M = i_c + i'_s + i'_a. \tag{3-2}$$

Differentiating of (3-2) yields

$$\frac{di_M}{dt} = \frac{di_c}{dt} + \frac{di'_s}{dt} + \frac{di'_a}{dt}. \tag{3-3}$$

Substitution of the current changing rates of i_M, i_c, i'_s, and i'_a into (3-3) gives

$$-\frac{v_{M1}}{L_M} = \frac{v_{M1} - v_c}{L_{lkp}} + \frac{v_{M1} - v'_o}{L'_{lks}} + \frac{v_{M1} - v'_{aux}}{L'_{lka}}. \tag{3-4}$$

Solving (3-4) for v_{M1} yields

$$v_{M1} = \frac{K_p v_c + K_s v'_o + K_a v'_{aux}}{1 + K_p + K_s + K_a} \tag{3-5}$$

where $K_p = L_M / L_{lkp}$, $K_s = L_M / L'_{lks}$, and $K_a = L_M / L'_{lka}$. When the current i_c flowing into the *RCD* snubber decreases to zero, the system enters into interval T_2. The equivalent circuit is shown as Fig. 3.3(b). Then,

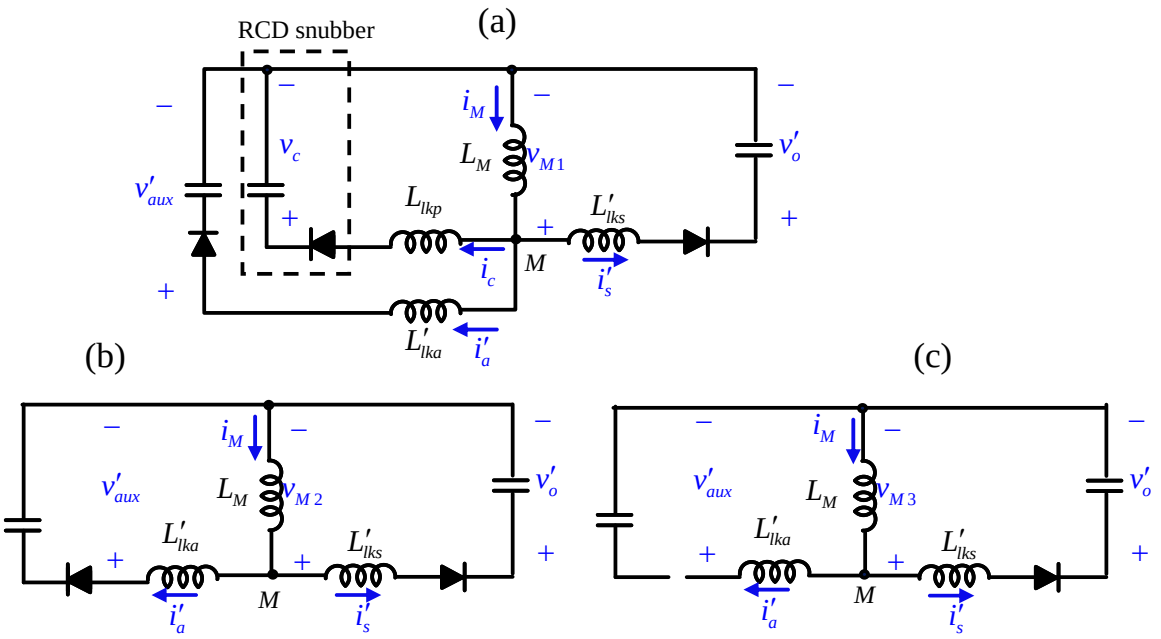


Fig. 3.3. Equivalent circuits in interval (a)T_1, (b)T_2, (c)T_3.

$$v_{M2} = \frac{K_s v'_o + K_a v'_{aux}}{1 + K_s + K_a}. \tag{3-6}$$

When the auxiliary diode is off, the system enters into interval T_3. The equivalent circuit is shown as Fig. 3.3(c). By the same procedure, solving v_{M3} yields

$$v_{M3} = \frac{K_s v'_o}{1 + K_s}. \tag{3-7}$$

Comparing with (3-5), (3-6), and (3-7), v_{M3} is a simple function of K_s and v_{aux} couples to v_{M3} perfectly because i_a is equal to zero in interval T_3. If the controller samples the voltage on the auxiliary winding in interval T_3, v_{aux} can be expressed as

$$v_{aux} = \frac{N_a}{N_p} v'_{aux} = \frac{N_a}{N_p} v_{M3} = \frac{N_a}{N_p} \frac{K_s v'_o}{1 + K_s} = \frac{N_a}{N_s} \frac{K_s}{1 + K_s} v_o. \tag{3-8}$$

K_s is infinite for an ideal system, so that the above equation is identical to (3-1).

From (3-8), it shows that the accuracy of primary-side sensing is only influenced by the leakage inductance in the secondary winding when the controller samples v_{aux} in interval T_3. Fig. 3.4 shows v_{aux} to v_o ratio versus K_s assuming N_s = N_a, where circles are the results calculated by (3-8) and stars are the results simulated by PSIM 6.0 software. This figure

indicates that v_{aux} to v_o ratio is relative to the leakage inductance in the secondary winding, so we define an effective turn ratio as follows

$$n_{eff} = \frac{K_s}{1+K_s}\frac{N_a}{N_s}. \tag{3-9}$$

Equation (3-9) makes the relationship between v_o and v_{aux} simple. In order to modify the effect caused by the leakage inductance in the secondary winding, measuring the effective turn ratio is necessary when implementing a flyback converter with PSS.

For more detailed analysis, the forward-biased voltage drop of the secondary diode and the winding resistance in the secondary winding also affect the accuracy of output voltage sensing. Referring to Fig. 3.5, v_{aux} can be re-derived below

$$i_M = i_s'. \tag{3-10}$$

Differentiating of (3-10) yields

$$\frac{di_M}{dt} = \frac{di_s'}{dt}. \tag{3-11}$$

Substitution of the current changing rates of i_M and i_s' into (3-11) gives

$$-\frac{v_{M3}}{L_M} = \frac{v_{M3} - v_o' - v_D' - i_s' R_s'}{L_{lks}'}. \tag{3-12}$$

Solving (3-12) for v_{M3} yields

$$v_{M3} = \frac{K_s(v_o' + v_D' + i_s' R_s')}{1+K_s}. \tag{3-13}$$

Finally, v_{aux} can be expressed as

$$v_{aux} = n_{eff}(v_o + v_D + i_s R_s). \tag{3-14}$$

Define that the sensing error Δv is

$$\begin{aligned} \Delta v = v_{o,est} - v_o &= \frac{v_{aux}}{n_{eff}} - v_o \\ &= v_D + i_s R_s \end{aligned} \tag{3-15}$$

where $v_{o,est}$ represents the estimated output voltage from the auxiliary winding and v_o

is the real output voltage. The voltage drop of the secondary diode v_D is almost constant, but in DCM, the current flowing through the secondary diode decreases violently in off state. If the sampling instants to sample v_{aux} are different with the same load, the sensing error is also different because the term $i_s R_s$ is dependent on the sampling instant. This will be explained in section 4.2.2.

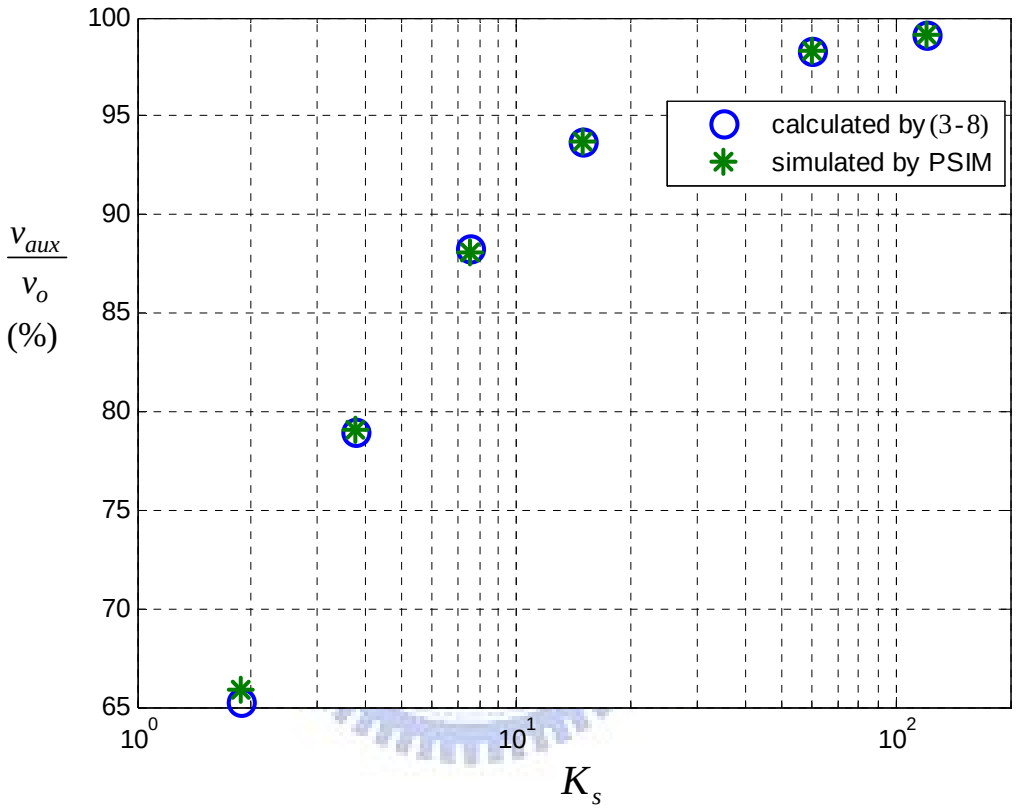


Fig. 3.4. v_{aux} to v_o ratio versus K_s assuming $N_s = N_a$.

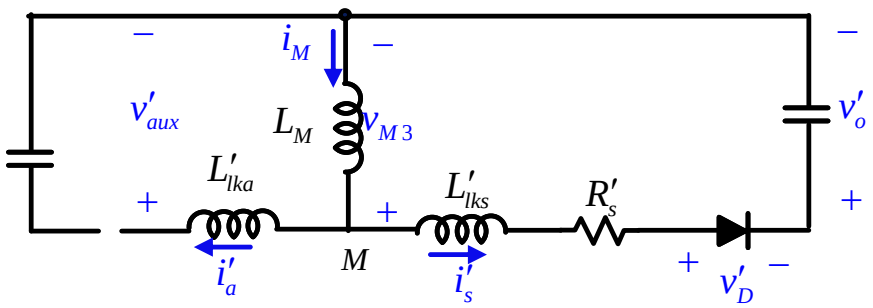


Fig. 3.5. Equivalent circuit in interval T_3 considering the forward-biased voltage drop v_D and the winding resistance R_s.

The simulation results are in Fig. 3.6. It can be recognized that when the switch is turned off, the system enters into interval T_1. In interval T_1, the magnetizing current i_M decreases because of energy releasing and the diode in *RCD* snubber conducts. When the current i_c decreases to zero, the system enters into interval T_2. In interval T_2, the energy transfers to the load and the primary-side controller with an assumption that the power dissipation of the controller is much smaller than the load. When the rectified diode at the auxiliary side is open, the system enters into interval T_3. It is mentioned before that the good timing to sample v_{aux} is in interval T_3. The sensing error Δv calculated by (3-15) and the real error signal are plotted in the last subplot in Fig. 3.6. It is clear that the calculation result and the simulation result of the sensing error are matched each other (The curve of Δv is correct only in interval T_3.).

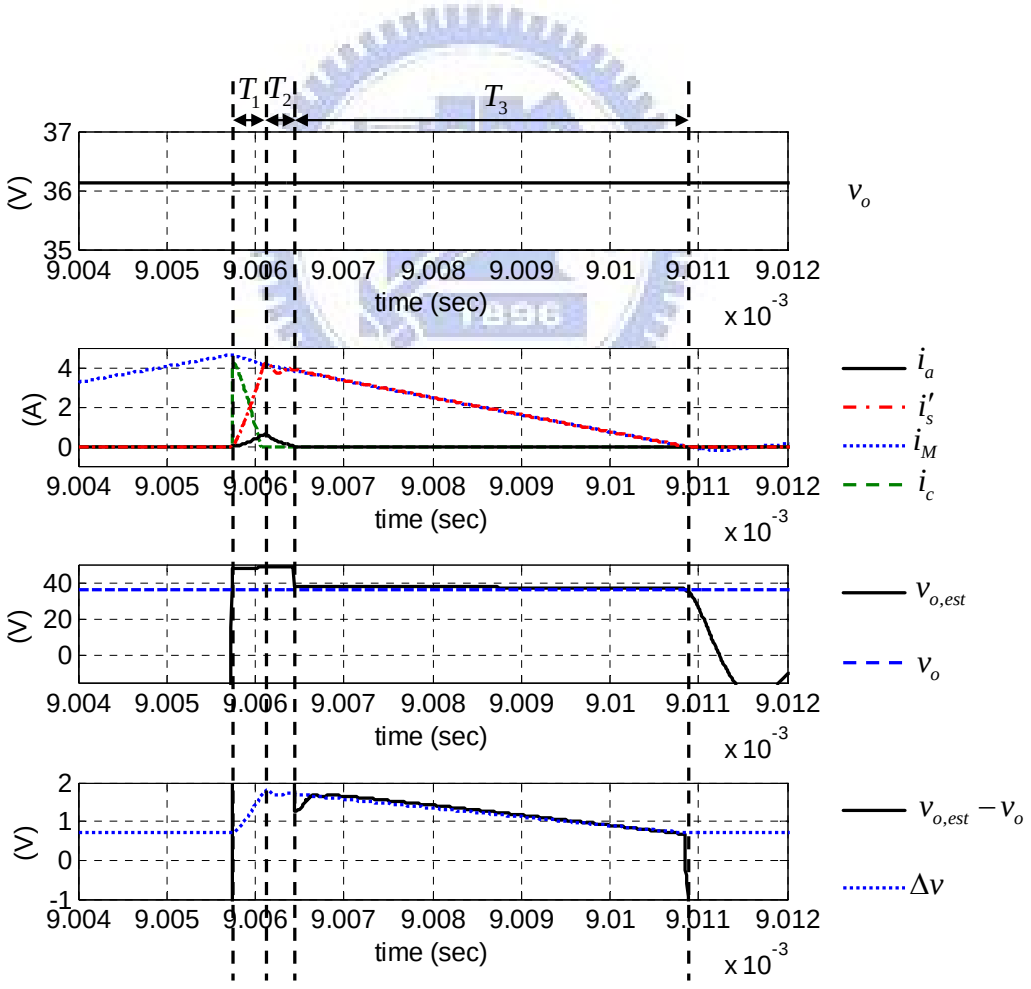


Fig. 3.6. Simulation results of flyback converter to verify the relationship between the output voltage and the estimated output voltage.

3.2 DETERMINATION OF THE SAMPLING INSTANT

Based on the analysis above, the controller needs a mechanism to set the sampling instant in interval T_3. In order to set the sampling instant correctly, we need to know the lengths of interval T_1 and T_2.

During interval T_1, the current flowing into the *RCD* snubber is

$$i_c(t) = \frac{(v_{M1} - v_c)}{L_{lkp}} t + \hat{i}_p \tag{3-16}$$

where $\hat{i}_p$ is the peak value of the magnetizing current. Letting $i_c(t) = 0$, the length of interval T_1 is obtained as

$$T_1 = \frac{L_M \hat{i}_p}{K_p} \cdot \frac{1 + K_p + K_s + K_a}{v_c(1 + K_s + K_a) - K_s v'_o - K_a v'_{aux}}. \tag{3-17}$$

The currents i'_s and i'_a during interval T_1 are

$$i'_s(t) = \frac{(v_{M1} - v'_o)K_s}{L_M} t \tag{3-18}$$

$$i'_a(t) = \frac{(v_{M1} - v'_{aux})K_a}{L_M} t. \tag{3-19}$$

At the end of interval T_1, when the current flowing into the *RCD* snubber decreases to zero, the instantaneous current in the secondary winding at t_2 is obtained by substitution of (3-17) into (3-18)

$$\hat{i}_{s1} = \frac{K_s \hat{i}_p}{K_p} \cdot \frac{(1 + K_p + K_s + K_a)(v_{M1} - v'_o)}{v_c(1 + K_s + K_a) - K_s v'_o - K_a v'_{aux}}. \tag{3-20}$$

In similar way, the peak current in the auxiliary winding can be derived as

$$\hat{i}_a = \frac{K_a \hat{i}_p}{K_p} \cdot \frac{(1 + K_p + K_s + K_a)(v_{M1} - v'_{aux})}{v_c(1 + K_s + K_a) - K_s v'_o - K_a v'_{aux}}. \tag{3-21}$$

During interval T_2, the current in the auxiliary winding is

$$i'_a(t) = \frac{v_{M2} - v'_{aux}}{L'_{lka}} t + \hat{i}_a. \tag{3-22}$$

The current $i'_a(t)$ will decrease to zero before $i'_s(t)$ does because the power dissipation in the auxiliary winding is much smaller than the power dissipation in the secondary winding, so that the length of interval T_2 can be obtained by letting $i'_a(t) = 0$ as

$$T_2 = \frac{L_M \hat{i}_p}{K_p} \cdot \frac{(1 + K_s + K_a)\left[K_s v'_o + K_p v_c - v'_{aux}(1 + K_s + K_p)\right]}{\left[v_c(1 + K_s + K_a) - K_s v'_o - K_a v'_{aux}\right](v'_{aux} + v'_{aux} K_s - K_s v'_o)}. \tag{3-23}$$

The currents i'_s during interval T_2 is

$$i'_s(t) = \frac{v_{M2} - v'_o}{L'_{lks}} t + \hat{i}_{s1}. \tag{3-24}$$

The instantaneous current in the secondary winding at t_3 when the current $i'_a(t)$ decreases to zero can be obtained by substitution of (3-23) into (3-24) as

$$\hat{i}_{s2} = \frac{K_s \hat{i}_p (v'_{aux} - v'_o)}{v'_{aux} + K_s (v'_{aux} - v'_o)}. \tag{3-25}$$

After t_3, only L_M and L'_{lks} have current, the equivalent circuit in interval T_3 is shown in Fig. 3.3(c). The currents i'_s during interval T_3 is

$$i'_s(t) = -\frac{v'_o}{L_M + L'_{lks}} t + \hat{i}_{s2}. \tag{3-26}$$

The length of interval T_3 can be obtained by letting $i'_s(t) = 0$ as

$$T_3 = \frac{\hat{i}_p L_M}{v'_o} \frac{(v'_{aux} - v'_o)(1 + K_s)}{v'_{aux} + K_s (v'_{aux} - v'_o)}. \tag{3-27}$$

So far, the lengths of intervals T_1, T_2, and T_3 can be estimated.

A well-known method to generate PWM signal is comparing a dc level with a sawtooth carrier. When the dc level is higher than the carrier, PWM signal is high. On the other hand, PWM signal is low when the carrier is higher than the dc level. The carrier generator for the digital PSS controller can be realized by using the programmable timer of a DSP controller.

Define that V_{duty} is the dc level to generate PWM signal, V_{delay} is an integer to set the delay time after the switch is turned off, and V_{ADC}, which is the sum of V_{duty} and V_{delay}, is used to determine the sampling instant. The mechanism is shown in Fig. 3.7. In the DSP controller, the mode of analog-to-digital converters (ADCs) should be set as compare interrupt flag. When the value of the counter is equal to V_{ADC}, ADC starts to convert analog inputs to digital output values. The key factor is V_{delay}. The delay time should be longer than interval T_1 plus interval T_2, so the value of V_{delay} satisfies the following inequality:

$$T_1 + T_2 < T_{CLK} \cdot V_{delay} < T_1 + T_2 + T_3 \tag{3-28}$$

where T_{CLK} is the period of the counter.

The lengths of interval T_1 and T_2 limit the maximum switching frequency. The switching period shorter than the sum of interval T_1 plus T_2 is impossible because it is unable to sample the correct signal representing the output voltage.

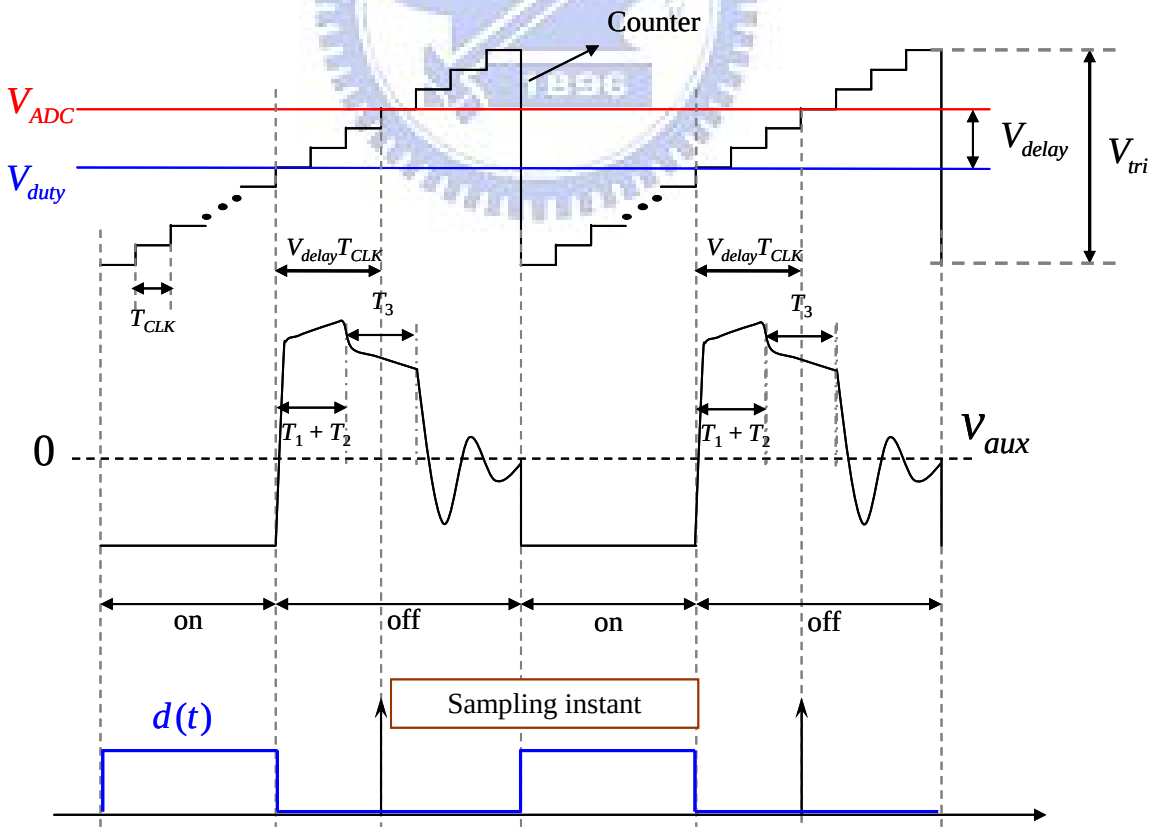


Fig. 3.7. Mechanism to set the sampling instant.

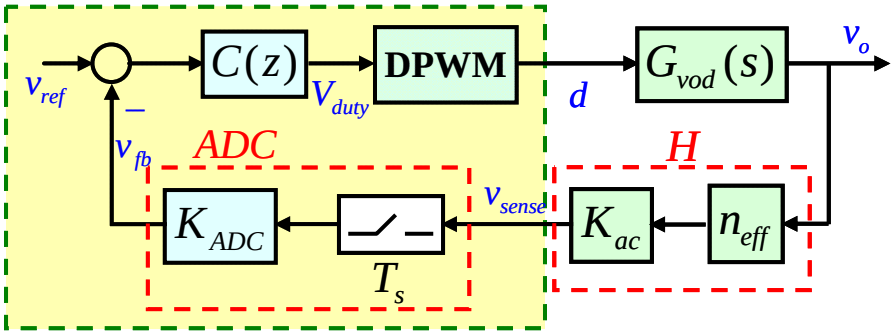
Chapter 4

Analysis and Design of DCM DC-DC Flyback Converters with PSS

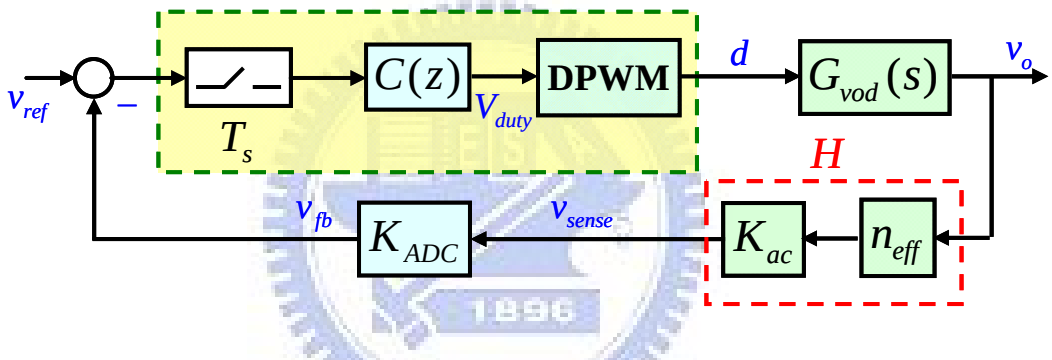
At the beginning of designing a DCM DC-DC flyback converter with PSS shown in Fig. 3.2(a), a dynamic model of the overall system is needed. Operating in DCM is given some advantages such that the secondary diode will naturally turn off without significant losses, the control-to-output transfer function is approximated to a first-order system in voltage mode, there are no turn-on losses on the MOSFET, and a quasi-resonant (QR) flyback converter can be realized.

The design methods for analog controllers are well-known and easy to apply. To implement a digital controller, it can be quite convenient to derive a digital controller from an existing analog design by the backward Euler integration or the trapezoidal (Tustin) integration methods. The application of these methods implies some loss of precision due to the approximations involved in the discretization process, as compared to a direct digital design. For simplicity, a continuous time equivalent block diagram of the proposed system is obtained. The procedure to define the continuous time equivalent block diagram is shown in Fig. 4.1. Fig. 4.1(a) is the block diagram of the system shown in Fig. 3.2. All components and parameters in the shaded part are in discrete time domain. The ADC is divided into a sample-and-hold (S/H) block and a scaling factor K_{ADC}, $C(z)$ is the digital controller, and the digital pulse-width-modulation (DPWM) block is cascaded with the digital controller. Because the scaling factor of the ADC is a constant value, it can be placed in continuous time domain with no differences. The S/H block is moved to the output of the adder shown in Fig. 4.1(b). Moreover, the digital controller $C(z)$ is transformed into an analog controller $C(s)$, so that Fig.

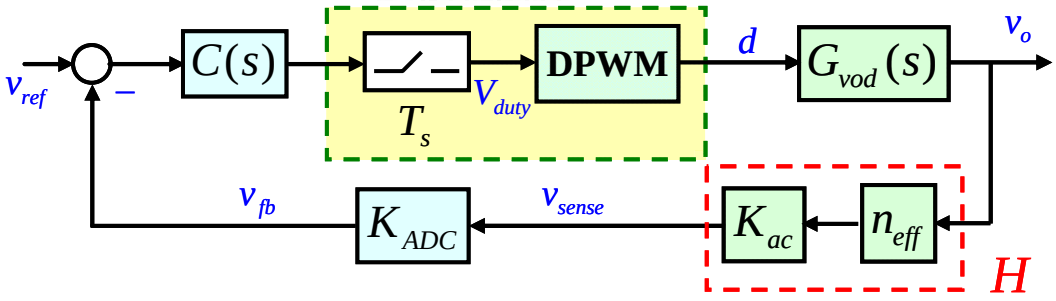
4.1(c) is obtained. In this chapter, we base on Fig. 4.1(c) to analyze DCM DC-DC flyback converters with PSS and design the control algorithm. A prototype of DCM DC-DC flyback converters with PSS is realized to verify the feasibility of PSS.



(a)



(b)



(c)

Fig. 4.1. Procedure to define the continuous time equivalent block diagram.

4.1 Dynamic Model of DCM DC-DC Flyback Converters with PSS

In order to design the control algorithm, the control-to-output transfer function is derived firstly. Then, the feedback path constructed by the flyback transformer, the voltage divider, and the ADC is developed. Finally, the DPWM is considered with a delay model.

4.1.1 Control-to-Output Transfer Function

Although the controlled system is implemented with PSS, the small-signal model of the power stage is the same as the conventional flyback converter. As the mentioned process in Fig 2.1, a flyback converter can be converted into an equivalent buck-boost converter, so that the small-signal model of the DCM buck-boost converter can be utilized to derive the control-to-output transfer function of the flyback converter. Based on [16], Figure 4.2 is the small-signal model of the DCM equivalent buck-boost converter from the flyback converter, where the parameters noted with prime are converted from the secondary side to the primary side and the ones with tilde represent perturbations of themselves without DC operating points.

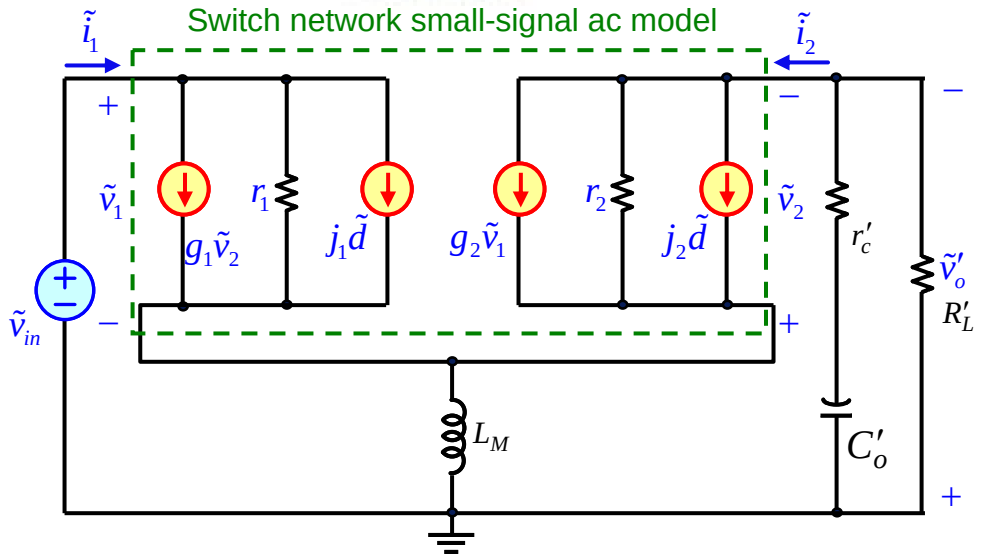


Fig. 4.2. Small-signal model of the DCM equivalent buck-boost converter from the flyback converter.

The relative parameters in the small-signal model are shown in Table 4.1. Because the average voltage on the magnetizing inductance is zero, so $V_1 = V_{in}$. R_e is the effective resistance defined as

$$R_e = \frac{2L_M}{D^2 T_s} \tag{4-1}$$

where D means the duty ratio under steady state conditions, and M is the voltage conversion ratio defined as

$$M = \frac{V_o'}{V_{in}} = \frac{n_{ps} V_o}{V_{in}} = \sqrt{\frac{R_L'}{R_e}} = n_{ps}\sqrt{\frac{R_L}{R_e}}. \tag{4-2}$$

When we derive the control-to-output transfer function, let the perturbations besides $\tilde{d}$ be zero. There are only two current sources reserved. Applying superposition principle, the procedure to derive the control-to-output transfer function is simple. Step 1 is letting $j_2\tilde{d} = 0$ to obtain $G_{vod1}(s)$:

$$G_{vod1}(s)\big|_{j_2\tilde{d}=0} = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{-j_1}{n_{ps}} \frac{r_1 \| sL_M}{\left[R_L' \| \left(\frac{1}{sC_o'} + r_c'\right)\right] + r_2 + (r_1 \| sL_M)} \frac{\frac{1}{sC_o'} + r_c'}{R + \frac{1}{sC_o'} + r_c'} R_L'. \tag{4-3}$$

Step 2 is letting $j_1\tilde{d} = 0$ to obtain $G_{vod2}(s)$:

$$G_{vod2}(s)\big|_{j_1\tilde{d}=0} = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{j_2}{n_{ps}} \frac{r_2}{\left[R_L' \| \left(\frac{1}{sC_o'} + r_c'\right)\right] + r_2 + (r_1 \| sL_M)} \frac{\frac{1}{sC_o'} + r_c'}{R + \frac{1}{sC_o'} + r_c'} R_L'. \tag{4-4}$$

TABLE 4.1

PARAMETERS OF THE SMALL-SIGNAL DCM SWITCH MODEL

g_1	j_1	r_1	g_2	j_2	r_2
0	$\frac{2V_1}{DR_e}$	R_e	$\frac{2}{MR_e}$	$\frac{2V_1}{DMR_e}$	$M^2 R_e$

Finally, the control-to-output transfer function is obtained as follows

$$G_{vod}(s) = G_{vod1}(s) + G_{vod2}(s)$$
$$\approx \frac{V_{in}}{\sqrt{K}} \frac{\left(1+\frac{s}{1/C_o' r_c'}\right)}{\left(1+\frac{s}{2/C_o'(R_L'+2r_c')}\right)\left(1+\frac{s}{R_e V_o'^2 / L_M (V_{in}^2 + V_o'^2)}\right)} \quad (4\text{-}5)$$

where $K = \frac{2L_M}{R_L T_s}$.

The small-signal model is derived by the averaged switch modeling method, so it is only correct at the frequency range lower than the switching frequency. Actually, there are two zeros during the calculation process, but the second zero is higher than the switching frequency. It is negligible when the system is concerned at the frequency much lower than the switching frequency.

The DC gain G_0 of the control-to-output transfer function is

$$G_0 = \frac{V_{in}}{\sqrt{K}}. \quad (4\text{-}6)$$

There are two poles as follows

$$f_{p1} = \frac{1}{\pi C_o (R_L + 2r_c)} \text{ (Hz)}$$
$$f_{p2} = \frac{1}{2\pi} \frac{R_e}{L_M \left(1+\frac{1}{M^2}\right)} = \frac{f_s}{\pi D^2 \left(1+\frac{1}{M^2}\right)} \text{ (Hz)} \quad (4\text{-}7)$$

where the second pole f_{p2} is close to the switching frequency depending on the duty ratio and the voltage conversion ratio.

There is only one zero we concerned as follows

$$f_{z1} = \frac{1}{2\pi C_o r_c} \text{ (Hz).} \quad (4\text{-}8)$$

This zero is often called ESR zero caused by the ESR r_c of the output capacitor. In

order to verify the derivation of the control-to-output transfer function, Fig. 4.3 shows the frequency response of the control-to-output transfer function by simulation and calculation.

4.1.2 Feedback Path

PSS technique utilizes the auxiliary winding to sense the output voltage. The sensing error is analyzed in chapter 3. In this section, we only consider the effective turns ratio n_{eff} in the feedback path. The effect of the sensing error will be discussed in the next section. The feedback path shown in Fig. 4.4 is constructed by the flyback transformer through the auxiliary winding, the voltage divider, and the ADC.

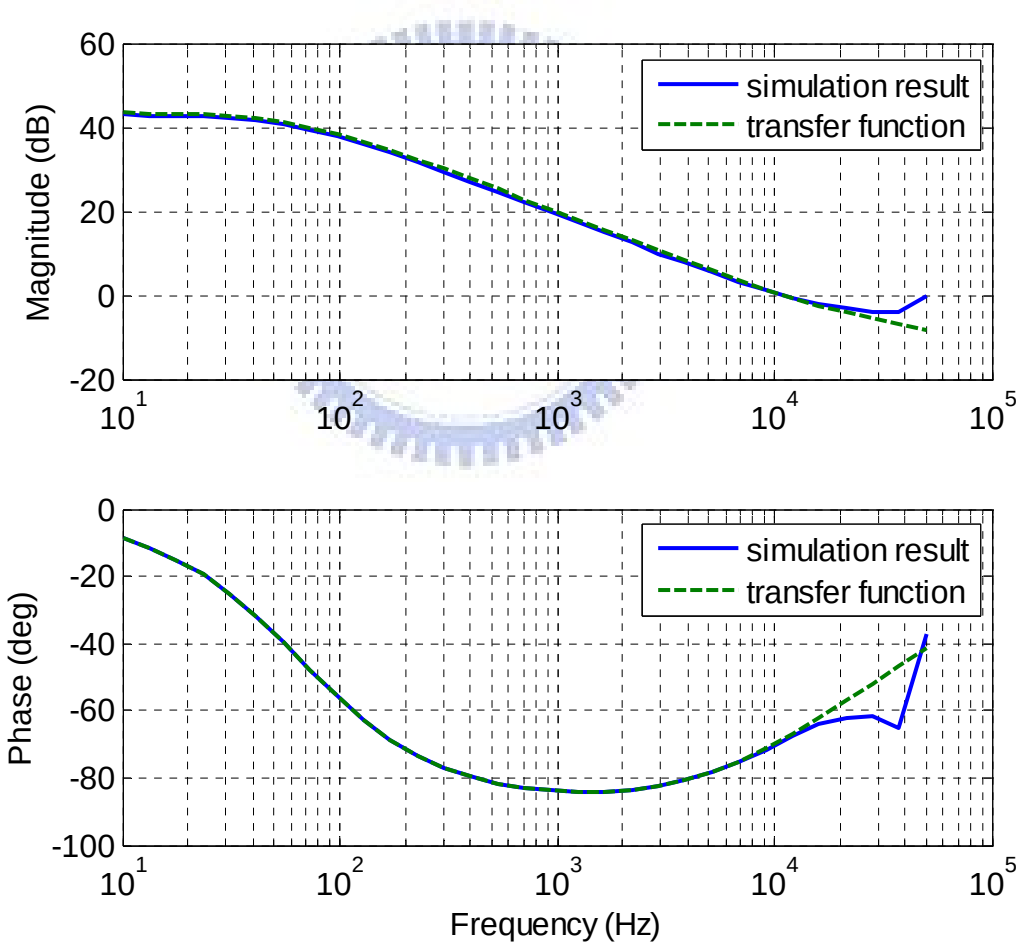


Fig. 4.3. Frequency response of the control-to-output transfer function by simulation and calculation.

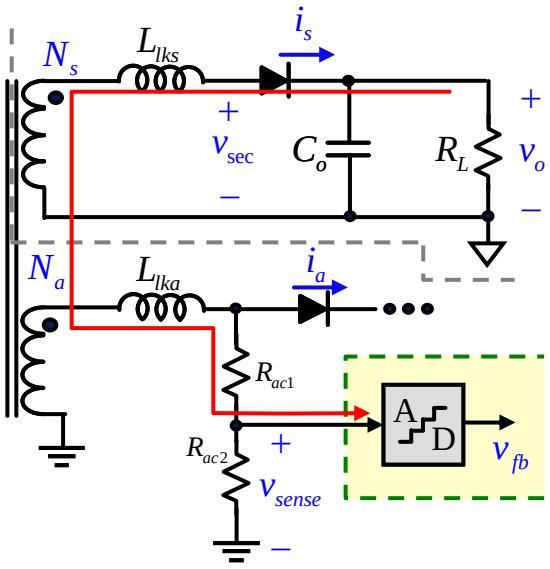


Fig 4.4. Feedback path for PSS.

When the system is during interval T_3, the voltage on the auxiliary winding contains the information of the output voltage. The relationship between these two voltages is mentioned in (3-14) where the effect of the voltage drop of the secondary diode and the winding resistance is neglected here, so the first block in the feedback path from v_o node is the effective turns ratio n_{eff}. Then, the voltage on the auxiliary winding is sent to a voltage divider. The gain of the voltage divider constructed by two resistors R_{ac1} and R_{ac2} is K_{ac} shown below

$$K_{ac} = \frac{R_{ac2}}{R_{ac1} + R_{ac2}}. \tag{4-9}$$

Combining the effect of the auxiliary winding and the voltage divider together, define a feedback gain H which is expressed by

$$H = n_{eff} \frac{R_{ac2}}{R_{ac1} + R_{ac2}}. \tag{4-10}$$

The final part of the feedback path is the ADC, which helps to convert the analog sensed voltage v_{sense} into a digital parameter v_{fb} for PSS algorithm. To avoid damaging the ADC, the range of the sensed voltage must be limited lower than the maximum input voltage of the ADC by setting a proper feedback gain H. For instance, the range must be lower than 3 volts for TMS320F2812, a DSP model of Texas Instruments (TI). The conversion ratio K_{ADC} of the

ADC is relative to the maximum input voltage v_r and the number of bits B, which is expressed by

$$K_{ADC} = \frac{2^B}{v_r}. \tag{4-11}$$

4.1.3 Digital PWM Model

For reasons of price, control circuits for low-power switching power supplies are always implemented using analog circuits before. As the price/performance ratio of DSPs has decreased rapidly during the last decade, the interest for digital control of switching power supplies has grown. The dynamics of a digital controlled converter are influenced by modulation effects. In this system, the duty command V_{duty} is updated with the switching frequency and the carrier of the DPWM is a sawtooth generated by a counter in DSP.

To derive the Laplace-domain models of the DPWM, consider the waveforms shown in Fig. 4.5 Firstly [17]. A general single-update-mode modulator has a carrier waveform v_c, a triangular waveform determined by the switching frequency and the ratio α. Choosing α equal to one allows to obtain a sawtooth carrier, where the carrier is actually an incremental counter shown in Fig. 3.6, not a triangular waveform in Fig. 4.5, which is used to make a simple sense. Normalizing the peak-to-peak value reduces quantization effects. The DPWM can be analyzed in a unified way for different type carriers.

The input of DPWM $u(t)$ is expressed by a steady-state part U and a small perturbation to this steady-state $\tilde{u}(t)$, or

$$u(t) = U + \tilde{u}(t). \tag{4-12}$$

This input is sampled at the sample rate equal to the switching frequency to produce the waveform $u_s(t)$, which is passed to the zero-order hold (ZOH). The output of the ZOH $u_H(t)$, the duty command, holds the amplitude of the input $u_s(t)$ during one switching period. The output of the DPWM is the duty ratio $y(t)$, which is also

expressed by a steady-state part Y (the response to U) and a small perturbation to this steady-state $\tilde{y}(t)$, or

$$y(t) = Y + \tilde{y}(t). \tag{4-13}$$

If we assume the sampler is ideal, the sampled waveform $u_s(t)$ can be regarded as an impulse and the small-signal output of the sampler is

$$\tilde{u}^*(t) = \left(u(t) - U\right)^* = \delta(t). \tag{4-14}$$

In order to obtain the dynamic model of the DPWM, we separate the small perturbation of the duty ratio $\tilde{y}(t)$ into two parts, $\tilde{y}_1(t)$ and $\tilde{y}_2(t)$, which are influenced by the small-signal output of the sampler $\tilde{u}^*$. Focusing on region (a) and (b) in Fig. 4.5, the perturbations $\tilde{y}_1(t)$ and $\tilde{y}_2(t)$ can be obtained by the properties of similar triangles.

$$\frac{\tilde{y}_1(t)}{\alpha T_s} = \frac{\tilde{u}(t)}{1} \tag{4-15}$$

$$\frac{\tilde{y}_2(t)}{(1-\alpha)T_s} = \frac{\tilde{u}(t)}{1}. \tag{4-16}$$

The influence of $\tilde{u}$ on $\tilde{y}_1(t)$ is at T_0 and the influence on $\tilde{y}_2(t)$ is at $(T_s - T_1)$. Finally, the perturbation of the duty ratio $\tilde{y}(t)$ is

$$\tilde{y}(t) = \tilde{y}_1(t) + \tilde{y}_2(t) = \alpha T_s \delta(t - T_0) + (1-\alpha) T_s \delta\left(t - (T_s - T_1)\right). \tag{4-17}$$

By sampling theorem, the small-signal input of the DPWM is

$$\tilde{u}^*(t) = \sum_{n=-\infty}^{\infty} \tilde{u}(nT_s)\delta(t - nT_s) \tag{4-18}$$

and the small-signal output of the DPWM in Laplace-domain is

$$\begin{aligned} \tilde{Y}(s) &= T_s\left(\alpha e^{-sT_0} + (1-\alpha)e^{-s(T_s - T_1)}\right)\tilde{U}^*(s) \\ &= \left(\alpha e^{-sT_0} + (1-\alpha)e^{-s(T_s - T_1)}\right)\sum_{n=-\infty}^{\infty} \tilde{U}(s - jn\omega_s). \end{aligned} \tag{4-19}$$

If we only concern the frequencies lower than the Nyquist frequency in the output,

the summation part in (4-19) is simplified as $\tilde{U}(s)$.

As we mentioned before, the sawtooth carrier is obtained by choosing α equal to one. The dynamic model of the DPWM with a sawtooth carrier $G_{PWM}(s)$ is

$$G_{PWM}(s) = \frac{\tilde{Y}(s)}{\tilde{U}(s)} = e^{-sDT_s}. \tag{4-20}$$

When the peak value of the sawtooth carrier is V_{tri}, the complete dynamic model of the DPWM is

$$G_{PWM}(s) = \frac{e^{-sDT_s}}{V_{tri}}. \tag{4-21}$$

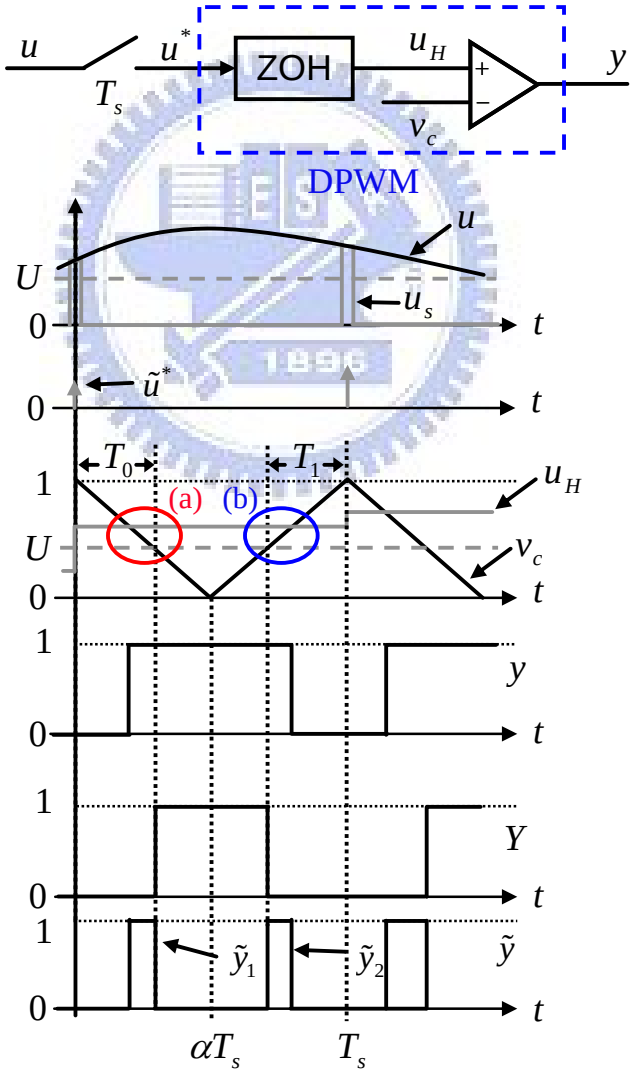


Fig 4.5. Key waveforms for a general single-update-mode modulator.

The exponential term represents a delay term, which can be simplified by the first-order Pade Approximation, so (4-21) can be simplified as

$$G_{PWM}(s) \approx \frac{1}{V_{tri}} \frac{1-\frac{1}{2}DT_s s}{1+\frac{1}{2}DT_s s} \tag{4-22}$$

where the simplified dynamic model has a constant gain $1/V_{tri}$ and is with a linear phase. Notice that this simplified model has an error in phase at frequencies near the switching frequency shown in Fig. 4.6, where the solid line is the frequency response of the exponential delay term and the dash line and the circles are the frequency responses of the first-order Pade approximated result and second-order result, respectively. For a more accurate approximation in phase, the second-order Pade approximation can be utilized.

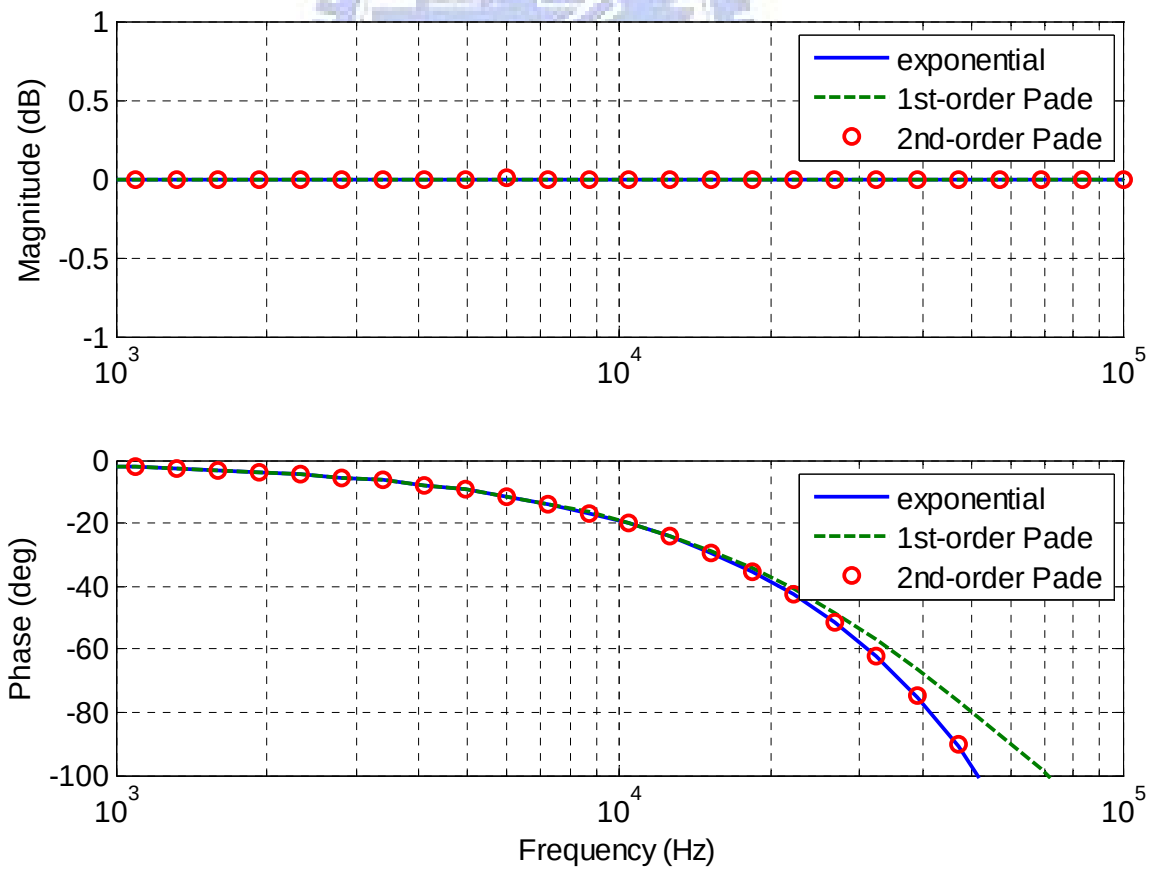


Fig. 4.6. Frequency response of the exponential delay term in the DPWM model.

4.2 PRIMARY-SIDE SENSING CONTROL ALGORITHM DESIGN

4.2.1 Digital PI Controller Design

According to the dynamic model of the proposed system and the continuous time equivalent block diagram in section 4.1, the controller can be firstly considered as an analog controller. Because the control-to-output transfer function of DCM flyback converters is almost a first-order system at low frequencies, an analog PI controller is a good choice to reduce the steady-state error and the phase margin of the loop gain is easy to be designed higher than 45 degrees at least. To design an analog PI controller, the loop gain function should be known as

$$L(s)=\left(K_P+\frac{K_I}{s}\right)G_{PWM}(s)G_{vod}(s)HK_{ADC} \tag{4-23}$$

where K_P is the proportional gain of the analog PI controller denoted with a capital P. Do not confuse K_P with K_p, which is the ratio of the magnetizing inductance to the primary-side leakage inductance defined in chapter 3.

Choose a proper crossover frequency f_{CL} and the phase margin PM according to a desired specification. To rapidly get an estimation of the searched values K_P and K_I, suppose that we can approximate the open loop gain at the crossover frequency f_{CL} with the following expression

$$\left|L(j\cdot 2\pi f_{CL})\right|=1\approx K_P\frac{1}{V_{tri}}\left|\frac{1-\frac{1}{2}DT_s\cdot j\cdot 2\pi f_{CL}}{1+\frac{1}{2}DT_s\cdot j\cdot 2\pi f_{CL}}\right|\frac{V_{in}}{\sqrt{K}}\left|\frac{1+\frac{j\cdot f_{CL}}{f_{z1}}}{1+\frac{j\cdot f_{CL}}{f_{p1}}}\right|\cdot H\cdot K_{ADC} \tag{4-24}$$

where the second pole of the control-to-output transfer function can be ignored when the crossover frequency is much lower than it, and the magnitude of the DPWM delay model is unity. Equation (4-24) is a good approximation as long as $K_I \ll 2\pi f_{CL}K_P$. Solving (4-24) for K_P, we get

$$K_P = \frac{V_{tri}}{V_{in}} \frac{\sqrt{K}}{HK_{ADC}} \sqrt{\frac{1+\left(\frac{f_{CL}}{f_{p1}}\right)^2}{1+\left(\frac{f_{CL}}{f_{z1}}\right)^2}}. \tag{4-25}$$

The parameter K_I can be calculated considering the phase margin

$$\begin{aligned} -180^\circ + PM = &-90^\circ - 2\tan^{-1}\left(\frac{2\pi f_{CL} DT_s}{2}\right) \\ &- \tan^{-1}\left(\frac{f_{CL}}{f_{p1}}\right) + \tan^{-1}\left(\frac{f_{CL}}{f_{z1}}\right) + \tan^{-1}\left(\frac{2\pi f_{CL} K_P}{K_I}\right). \end{aligned} \tag{4-26}$$

Solving (4-26) for K_I, we get

$$K_I = \frac{2\pi f_{CL} K_P}{\tan\left(-90^\circ + PM + 2\tan^{-1}\left(\pi f_{CL} DT_s\right) + \tan^{-1}\left(\frac{f_{CL}}{f_{p1}}\right) - \tan^{-1}\left(\frac{f_{CL}}{f_{z1}}\right)\right)}. \tag{4-27}$$

Finally, the analog PI controller can be transformed into a digital PI controller by the backward Euler integration. For the backward Euler integration, let

$$s = \frac{1 - z^{-1}}{T_s}. \tag{4-28}$$

Substituting (4-28) into the analog PI controller yields

$$\begin{cases} K_{P\_d} = K_P \\ K_{I\_d} = K_I T_s \end{cases} \tag{4-29}$$

where K_{P_d} and K_{I_d} are the parameters of the digital PI controller shown in Fig. 4.7.

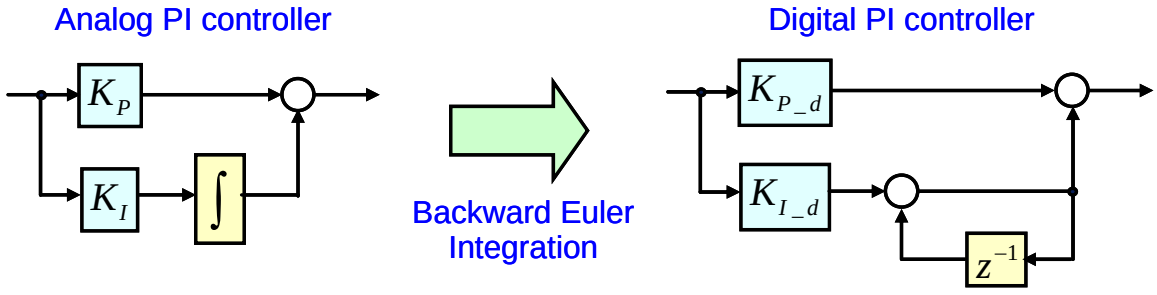


Fig. 4.7. Analog PI and digital PI controllers.

4.2.2 Sampling Instant Modulation

In section 3.1, the sensing error caused by the PSS technique is already derived as (3-15). Based on the characteristics of diodes, the forward-biased voltage drop v_D can be considered as a constant value, so it can be compensated by an offset on the voltage command v_{ref}. But in DCM, the current i_s in the secondary winding varies severely.

V_{delay} is a key parameter for PSS technique. In order to sense the output voltage in interval T_3, V_{delay} times T_{CLK} should be larger than T_1 plus T_2, where T_{CLK} is the period of the counter of the DPWM. The ADC will sample the sensed voltage at $V_{delay}T_{CLK}$ after the switch turned off. There is a problem that a steady-state error occurs when using a constant V_{delay} for different loads, which is shown in Fig. 4.8. The current i_s at heavy loads is higher than the current at light loads, so the sensed voltage in (3-14) at heavy loads is slightly higher than the sensed voltage at light loads. If we tune the voltage command v_{ref} to make the output voltage arrive at the desired level, there occurs a deviation on the output voltage when the load condition switches from heavy loads to light loads with a constant V_{delay}. The controlled output voltage at light loads will be higher than the desired level because of the slightly low sensed voltage and negative feedback. To improve the voltage regulation, a method is to modulate the sampling instant (i.e. V_{delay}) according to the load condition.

Fig. 4.9 shows the concept of sampling instant modulation. Let the conduction period of the rectified diode at the secondary side is t_{off}. Set the sampling instant at Δt before the diode is turned off, so that the current i_s is ideally the same. This forces the sensed voltage are almost identical at different loads. The V_{delay} can be set by

$$V_{delay} = \frac{t_{off} - \Delta t}{T_{CLK}}. \tag{4-30}$$

The conduction period of the rectified diode at the secondary side can be estimated from the magnetizing current i_M. The peak current $\hat{i}_p$ in the primary winding is

$$\hat{i}_p = \frac{v_{in}}{L_M} DT_s \tag{4-31}$$

and during interval t_{off}, the magnetizing current is

$$i_M(t) = \hat{i}_p - \frac{n_{ps} v_o}{L_M} t. \tag{4-32}$$

Let the magnetizing current be zero to obtain t_{off}

$$t_{off} = \frac{v_{in}}{n_{ps} v_o} \frac{V_{duty}}{V_{tri}} \frac{T_s}{T_{CLK}}. \tag{4-33}$$

According to (4-33), the sampling instant can be set to improve the voltage regulation. In fact, interval t_{off} is relative to the duty ratio, and the duty ratio is relative to the load. So, the sampling instant is actually modulated in accordance with the load conditions.

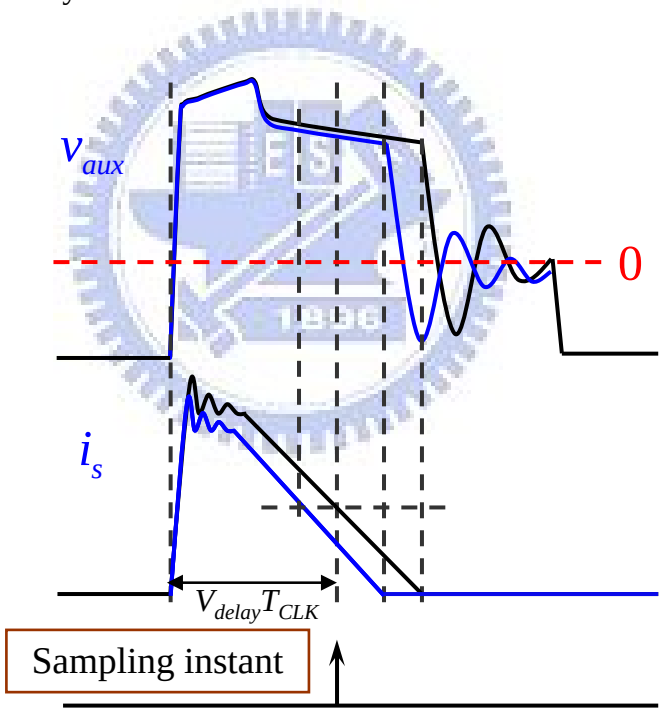


Fig. 4.8. Constant sampling instant makes the sensed voltages different between two different load conditions.

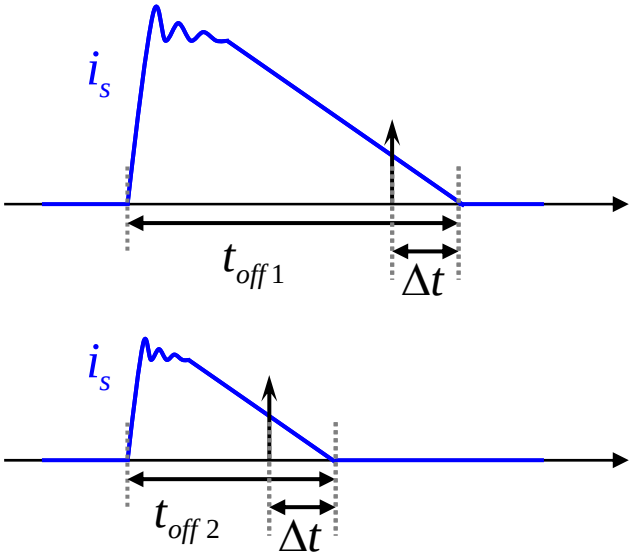


Fig. 4.9. Concept of sampling instant modulation.

4.2.3 Flowcharts of the Digital Control Algorithm

In this proposed system, we utilize a DSP chip, TMS320F2812, to implement the PSS control algorithm. The flowcharts of the control algorithm are shown in Figs. 4.10 and 4.11.

The task of main program is to keep DSP in operation. At the beginning of the control algorithm, initialize the hardware in DSP. The configuration of the general purpose input/output (GPIO) is set for one DPWM output and one PWM enable switch. There is only one interrupt service routine (ISR) program of the ADC assigned to peripheral-interrupts-extend (PIE) vector table. This program, ADC_ISR, implements PSS control algorithm and update the duty command. The timer (the counter in Fig. 3.7) is set to generate a PWM signal at 50 kHz. The ADC interrupt is set to be compared interrupt flag, so ADC_ISR will be triggered when the register V_{ADC} is equal to the counter. In Fig. 4.12, the sensed voltage is converted to digital value by ADC firstly, which costs 0.49 μs. Then, the digital PI controller calculates the next duty command according to the sensed value and the output voltage command, which costs 0.36 μs. Finally, a modulation method in (4-30) is utilized to update the next sampling instant, which costs 0.54 μs. The total duration of ADC_ISR is 1.39 μs,

which is about 7% to the switching period.

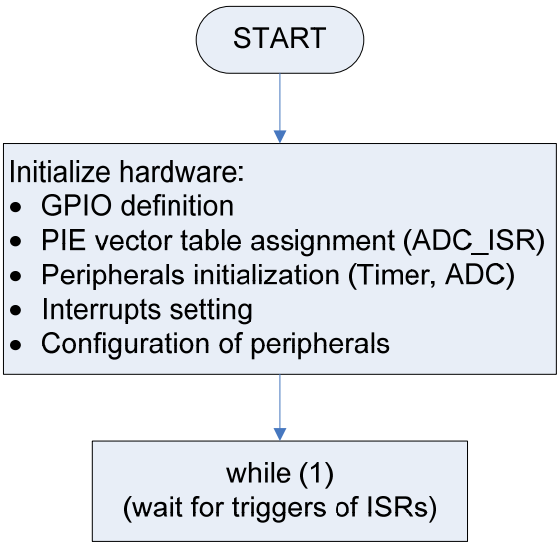


Fig. 4.10. Flowchart of main program.

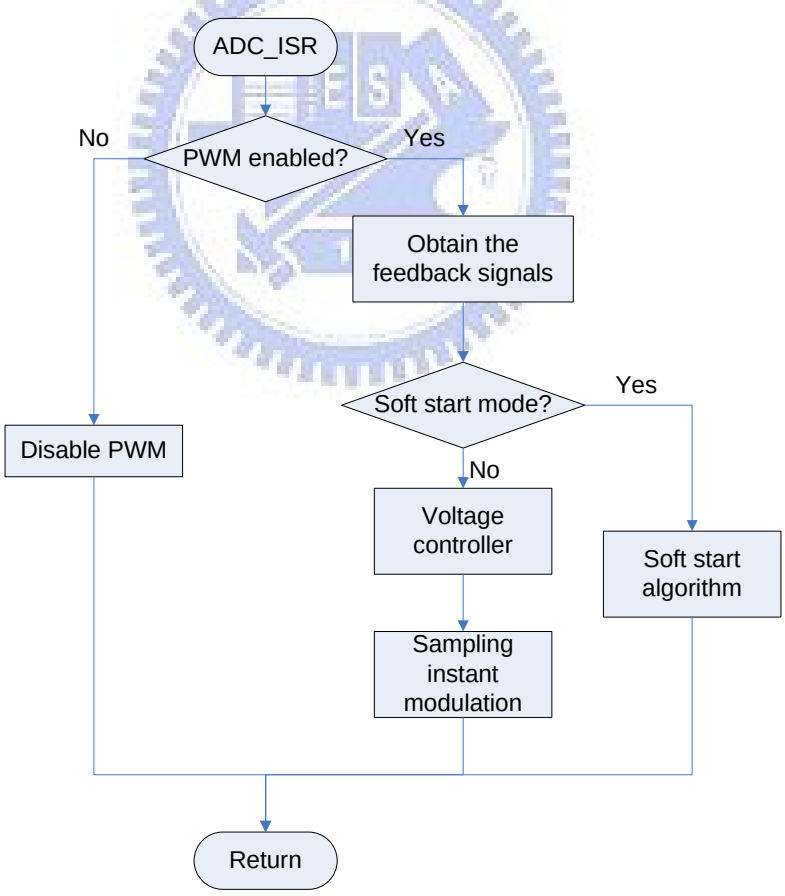


Fig. 4.11. Flowchart of interrupt service routine program.

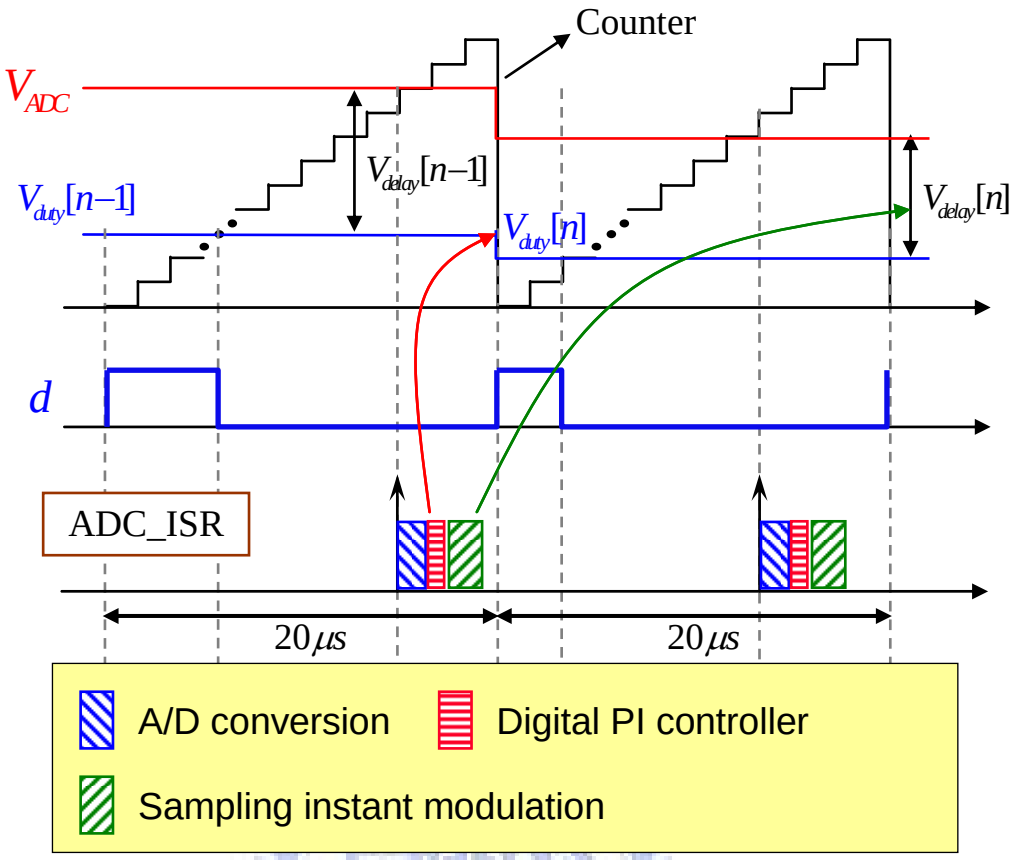


Fig. 4.12. Timing diagram of PSS algorithm in the DSP chip.

4.3 Experimental Results

To verify PSS technique, a 90 W DCM flyback converter is designed for operation from the 100 V DC line. The experimental setup for the DCM flyback converter with PSS is shown in Fig. 4.13. The nominal output voltage is 19 V, the switching frequency is 50 kHz, the magnetizing inductance is 120 μH referred to the primary side, the flyback transformer turns ratio n_{ps} is 2.9, the output capacitance is 200 μF, and the effective turns ratio n_{eff} is measured from the voltages on the secondary winding and the auxiliary winding in interval T_3, which is 1/2.97 shown in Fig. 4.14.

In section 4.2.2, the sampling instant modulation is mentioned to improve the steady-state error caused by sensing error. For further details, if V_{delay} is set as a constant, the sampling instant is always at $V_{delay}T_{CLK}$ after the switch is turned off. However, if V_{delay} is modulated

according to the output power and by (4-30), the sampling instant is at Δt before the switch is turned on in the next switching cycle. The key waveforms are shown in Figs. 4.15 and 4.16. The voltage regulation results with and without sampling instant modulation are shown in Fig. 4.17. The testing point is set from 20 W to 90 W. All results are normalized by 19 V. The voltage regulation with modulating the sampling instant has 1% deviation when the load power is from 20 W to 90 W, and the voltage regulation with constant sampling instant has about 4% deviation. As a result of modulating the sampling instant, the voltage regulation can be improved.

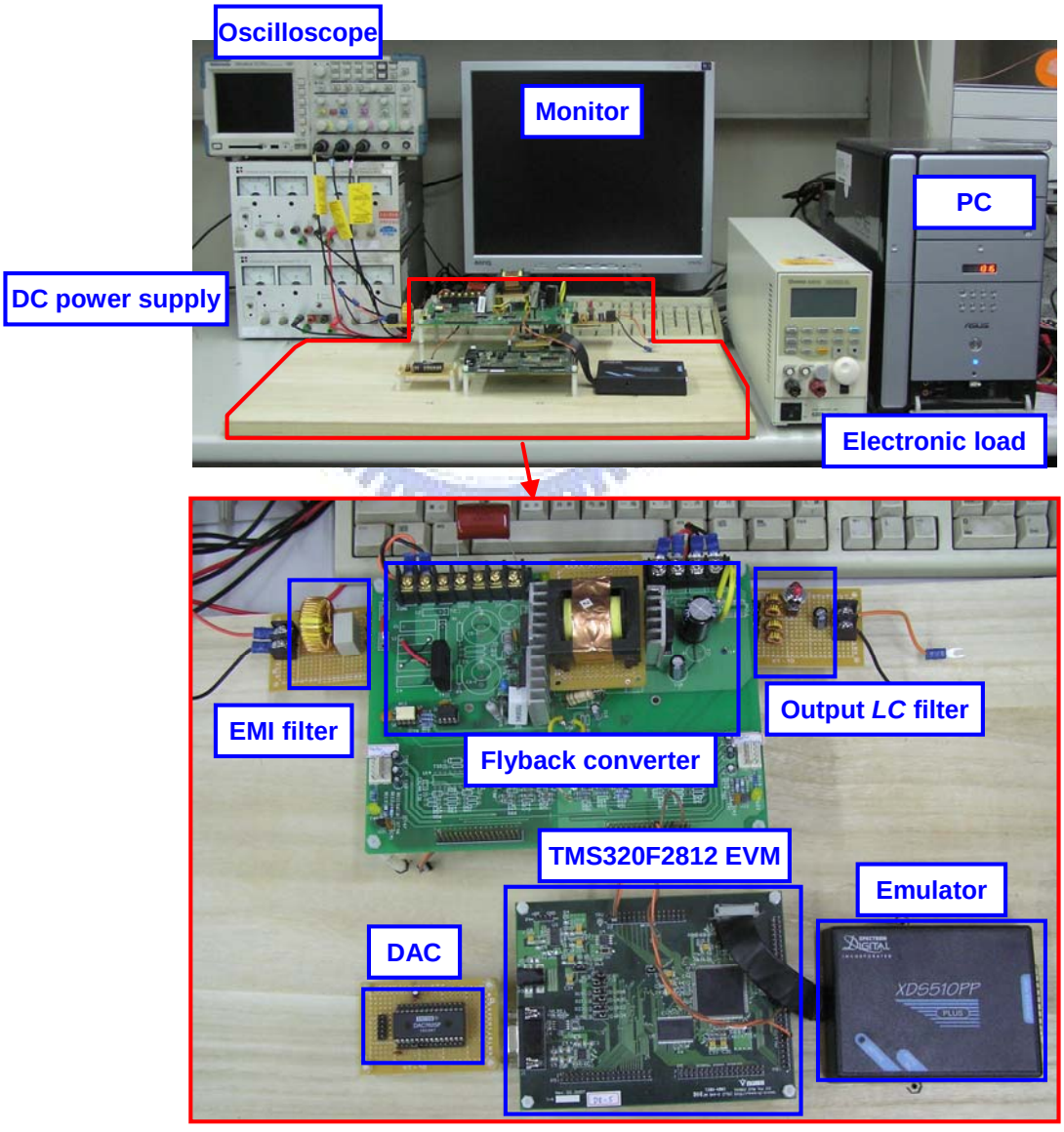


Fig. 4.13. Experimental setup for the DCM flyback converter with PSS.

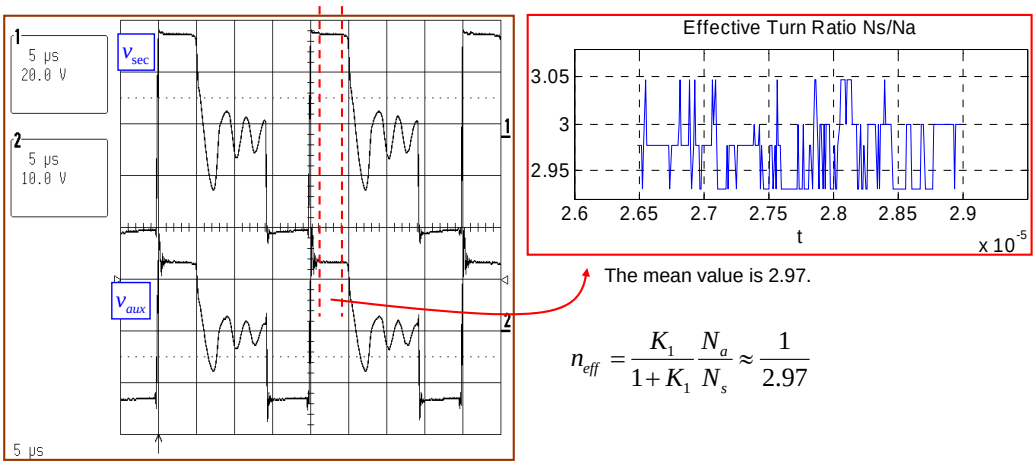
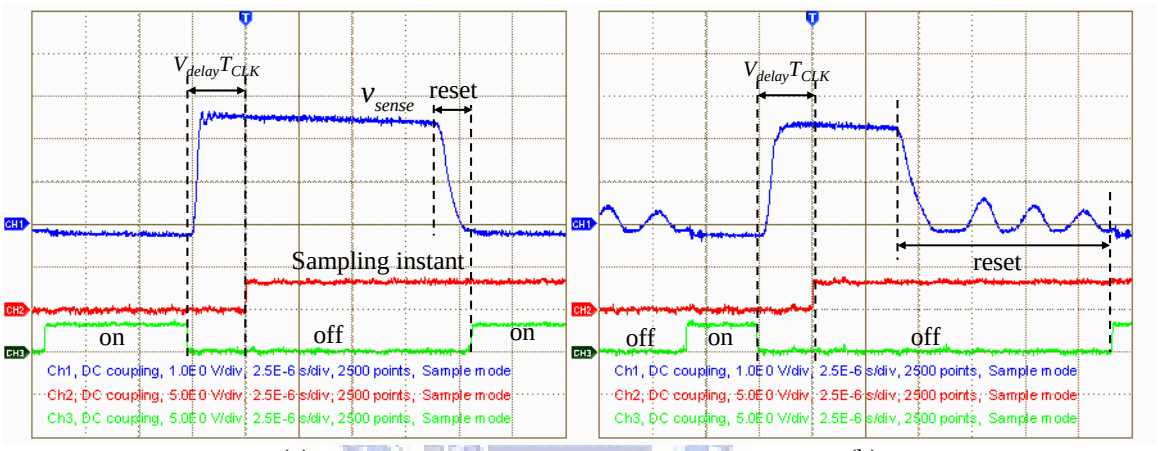
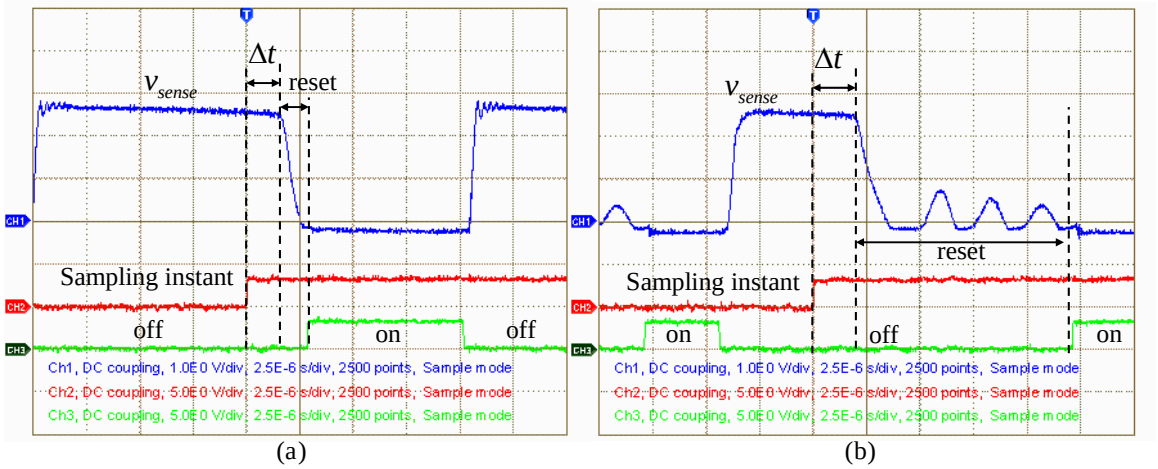


Fig. 4.14. Effective turns ratio from the auxiliary winding to the secondary winding.



(a) (b)

Fig. 4.15. Key waveforms with constant sampling instant (a) in full-load condition, (b) in light-load (20%) condition.



(a) (b)

Fig. 4.16. Key waveforms with sampling instant modulation (a) in full-load condition, (b) in light-load (20%) condition.

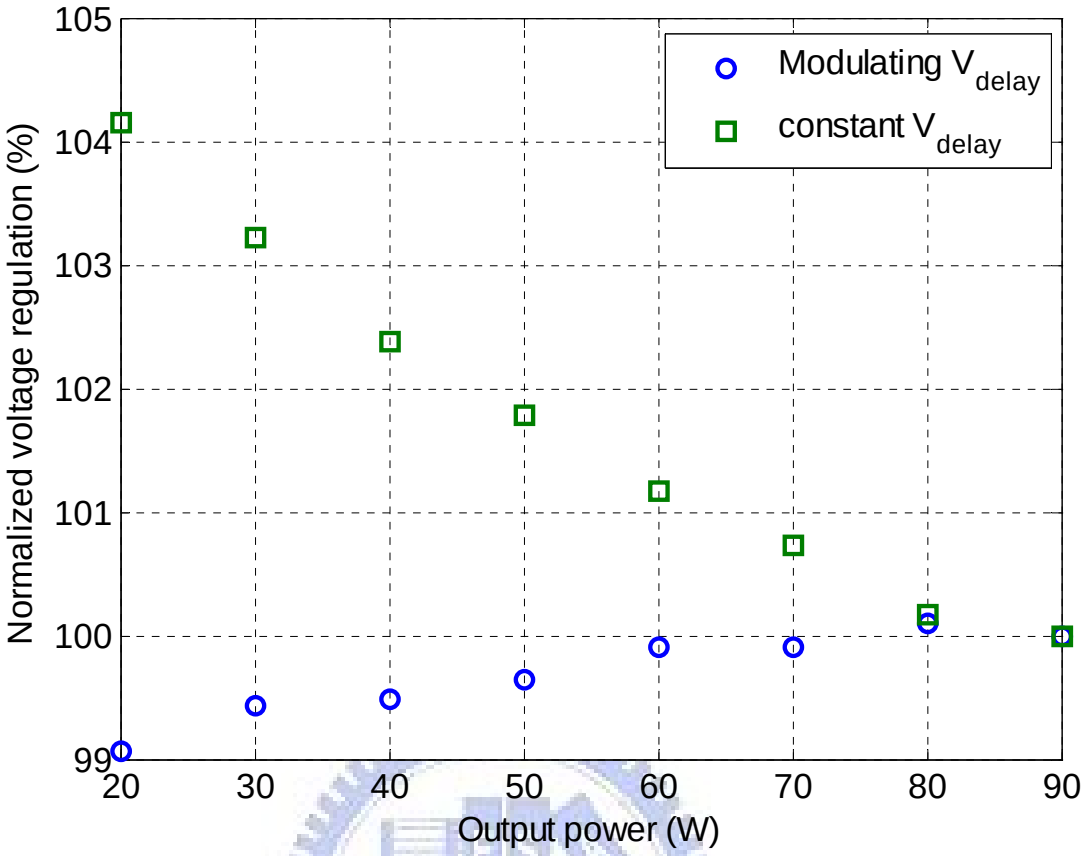


Fig. 4.17. Comparisons of voltage regulation with and without sampling instant modulation.

Then, we test the load transient from 20% to 100% with and without sampling instant modulation. Fig. 4.18 shows the result with constant sampling instant and Fig. 4.19 shows the result with modulated sampling instant. In Fig. 4.18, it is obvious that there is a steady-state error, 700 mV, which is caused by sensing error mentioned before. When the sampling instant is modulated by (4-30), the steady state error is reduced. Moreover, the sampling instant modulation does not affect the dynamic response because the waveforms in Figs. 4.18 and 4.19 are similar.

For operating in DCM, the output voltage of flyback converters suffers from the ESR of the output capacitor. To improve this situation, install a small *LC* filter at the output. Both load transient responses are shown together in Figs. 4.18 and 4.19. PSS technique senses the voltage before the *LC* filter, so the dynamic response of the *LC* filter does not affect the controller design.

The settling time in both cases is the same as 420 μs. Because of the sampling frequency is 50 kHz, the output voltage enters into steady state after 21 switching cycles. The voltage drop is 1 V in Fig. 4.18, 5.3% of nominal output while the voltage drop is 0.9 V in Fig. 4.19, 4.7% of the nominal output.

In order to check whether the sensed voltage for PSS is correct or not when the load changes from 20% to 100%, the sensed voltage in the DSP chip is transmitted to a digital-to-analog converter (DAC) immediately after the A/D conversion and scaled to the same level of the output voltage. The results are shown in Fig. 4.20(a). Because we sense the output voltage from the auxiliary winding, the output voltage after the *LC* filter can not be obtained for voltage regulation. This phenomenon is obviously shown in Fig. 4.20(a), where the sensed voltage follows the output voltage before the *LC* filter. Fig. 4.20(b) is the relation of the output voltage before the *LC* filter versus the sensed voltage. According to Fig. 4.20(b), it reveals that the sensed voltage and the output voltage before the *LC* filter are positive correlation. Fig. 4.20(c) is the relation of the output voltage after the *LC* filter versus the sensed voltage. The dots are almost below the ideal curve because the output voltage after the *LC* filter drops more than the sensed voltage when a load step occurs. The voltage deviation can be also recognized in Fig. 4.20(c).

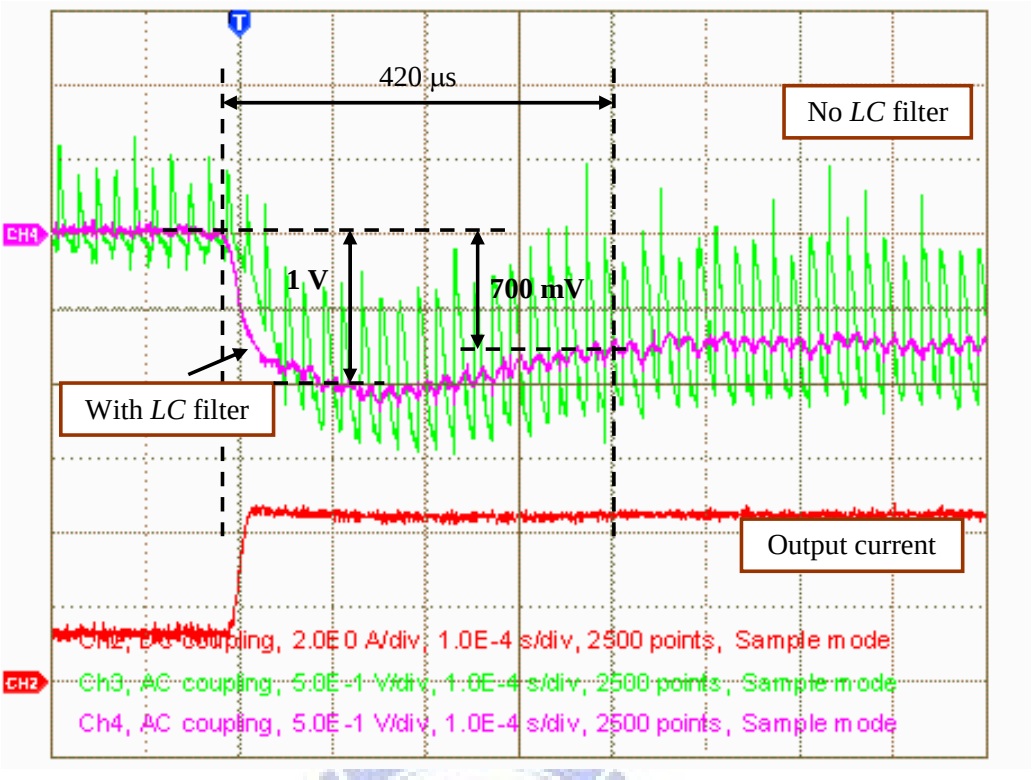


Fig. 4.18. Load transient response from 20% to 100% output power without sampling instant modulation.

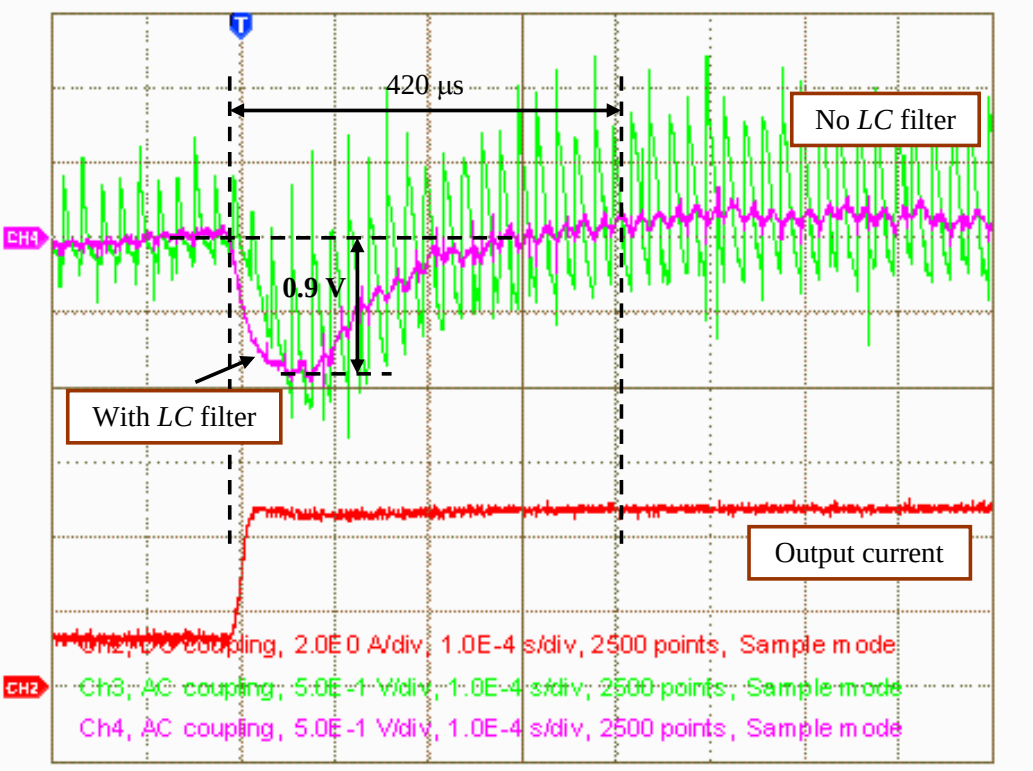


Fig. 4.19. Load transient response from 20% to 100% output power with sampling instant modulation.

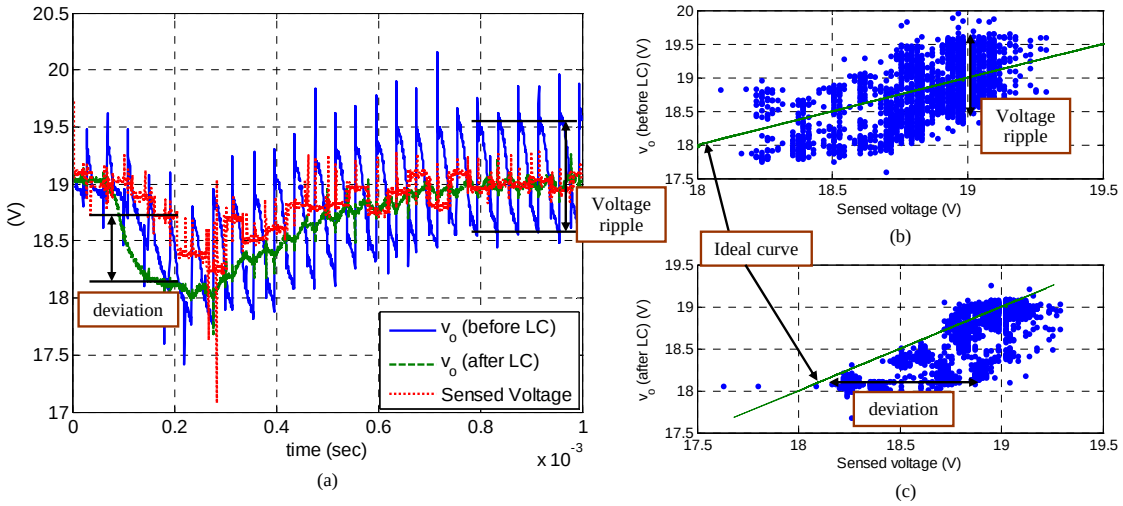


Fig. 4.20. (a) Experimental results of the output voltage and the sensed voltage by PSS. (b) Relation of the output voltage before the *LC* filter versus the sensed voltage. (c) Relation of the output voltage after the *LC* filter versus the sensed voltage.

Chapter 5

Analysis and Design of DCM PFC Flyback Rectifiers with PSS

5.1 Self Power Factor Correction (PFC) Property in DCM

Power factor is a figure of merit that measures how effectively energy is transmitted between an AC source and load network. It is defined as

$$\text{power factor} = \frac{(\text{average power})}{(\text{apparent power})}. \tag{5-1}$$

The input voltage and current are periodic in general. They may be expressed as Fourier series, so the average power can be obtained as

$$P_{av} = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos(\varphi_n - \theta_n) \tag{5-2}$$

where V_n is the amplitude of the n-th harmonic component of the input voltage, I_n is the amplitude of the n-th harmonic component of the input current, and $\cos(\varphi_n - \theta_n)$ is the displacement term which accounts for the phase difference between the n-th harmonic voltage and current. From (5-2), the net energy is transmitted to the load only when the Fourier series of the input voltage and current contain the terms at the same frequency. Therefore, for a sinusoidal input voltage, the average power is only composed by the fundamental voltage and current and the rms voltage is the fundamental voltage. On the other hand, the apparent power is composed by the rms voltage and current. The power factor can be expressed with $I_0 = 0$ as

$$\text{power factor} = \left(\frac{I_1 / \sqrt{2}}{I_{rms}} \right) (\cos(\varphi_1 - \theta_1)) \tag{5-3}$$

where if the fundamental voltage and current are in phase, the displacement term is one. Then, the power factor can be improved if the input current is similar to a sinusoidal waveform. This is a key point to PFC. To shape the input current like a sinusoidal waveform, input current feedback is usually necessary, but actually not in DCM. The following is to explain the reasons.

Basic types of converters have self PFC property when operating in DCM, that is, if these converters are connected to the rectified AC line, they have the capability to give higher power factor by the nature of their topologies. Because of self PFC property, input current feedback is unnecessary. The peak of the inductor current is sampling the line voltage automatically. Buck-boost converters are the best topology among basic types of converters with self PFC property [18]. At the beginning of chapter 2, it was mentioned that a flyback converter is called “isolated buck-boost converter” because it is derived from a buck-boost converter, so flyback converters also have the best self PFC property.

In order to explain why flyback converters have the best self PFC property, assume the line voltage is constant in a switching cycle. In steady state operation, the output voltage is almost constant and the variation in duty ratio is slight. Therefore, constant duty ratio is considered in deriving the input voltage-current characteristics. A simple topology of flyback rectifiers is shown in Fig. 5.1(a). The input current waveform is shown in Fig. 5.1(b). The relationship between the rectified input voltage $v_{rec}(t)$ and the peak of the primary current $i_p(t)$ in each switching cycle can be derived as

$$i_{p,peak}(t) = \frac{DT_s}{L_M} v_{rec}(t). \tag{5-4}$$

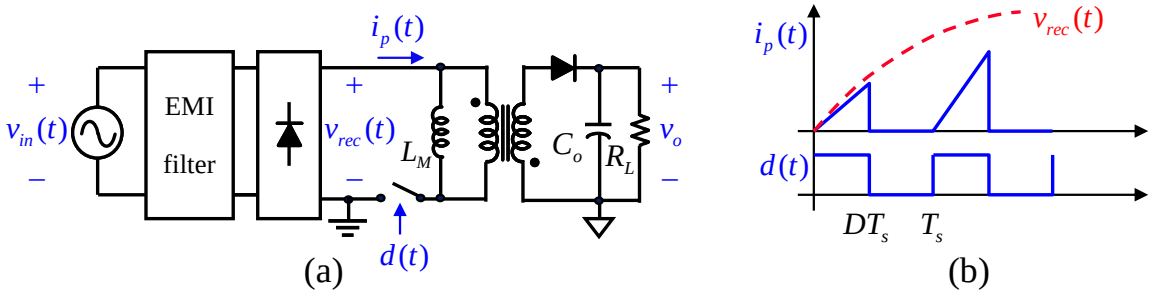


Fig. 5.1. A flyback rectifier in DCM: (a) Schematic, (b) Waveforms.

From the above equation, the average of the primary current in each switching cycle can be obtained as

$$i_{p,avg}(t) = \frac{\frac{1}{2} i_{p,peak}(t) DT_s}{T_s} = \frac{D^2 T_s}{2L_M} v_{rec}(t). \tag{5-5}$$

The average of the primary current is considered as the fundamental component of the input current from the AC source. For power factor correction, the fundamental component of the input current needs to be in phase with the input voltage. According to (5-5), the average current is a linear function with the rectified input voltage if the system operates in constant duty ratio and constant switching frequency, so the fundamental component of the input current is similar to the rectified voltage, a sinusoidal waveform. This satisfies the requests for power factor correction. The fundamental components of the input currents of three basic topologies are shown in Table 5.1.

TABLE 5.1
FUNDAMENTAL COMPONENTS OF THE AC INPUT CURRENTS OF THREE BASIC TOPOLOGIES

Buck	Boost	Buck-boost (Flyback)
$\frac{D^2 T_s}{2L_M}(v_{rec}(t) - V_o)$	$\frac{D^2 T_s}{2L_M} \frac{v_{rec}(t) V_o}{V_o - v_{rec}(t)}$	$\frac{D^2 T_s}{2L_M} v_{rec}(t)$

5.2 CHARACTERISTICS OF DCM PFC FLYBACK RECTIFIERS WITH PSS

The system schematics of a DCM PFC flyback rectifier is similar to Fig. 3.2(a), in which the differences are that the input port is replaced by an AC source, an electro-magnetic interference (EMI) filter, and a bridge rectifier. The controller $C(z)$ is replaced by a multimode digital controller shown in Fig. 5.2. The block diagram can be derived by the same procedure in Fig. 4.1, but the control-to-output transfer function is different in this case. Therefore, in this section, we derive the control-to-output transfer function of DCM PFC flyback rectifier step by step according to [19].

5.2.1 Loss-Free Resistor Model

The ideal single-phase rectifier presents a resistive load to the AC source, so that the AC line voltage and current will have the same waveshape and be in phase. In this ideal case, the power factor is unity. An equivalent circuit for the AC port of an ideal rectifier is an effective resistance R_e. This effective resistor transmits power to the output port without power loss on its own, so the equivalent circuit is called “loss-free resistor model” as shown in Fig. 5.3.

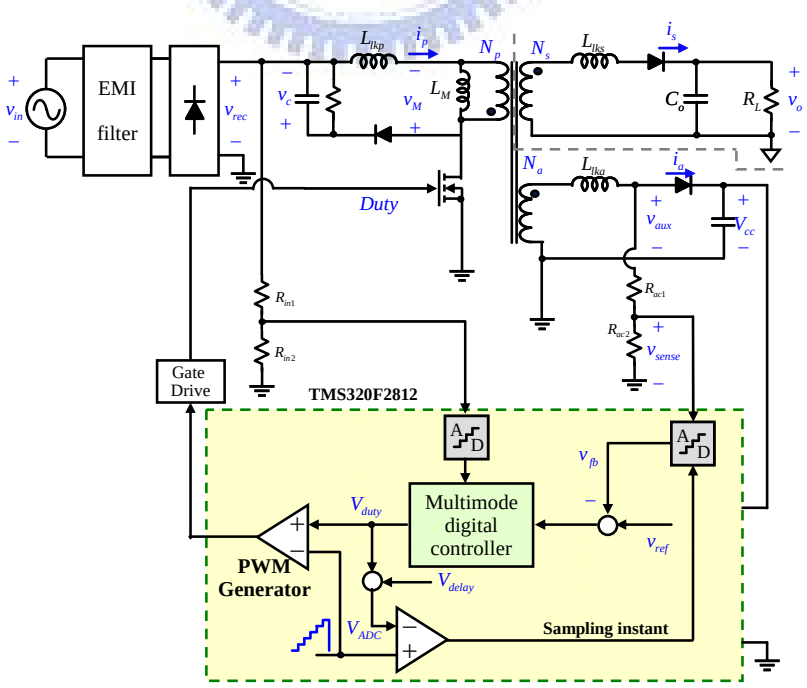


Fig. 5.2. System schematics of a DCM PFC flyback rectifier with PSS.

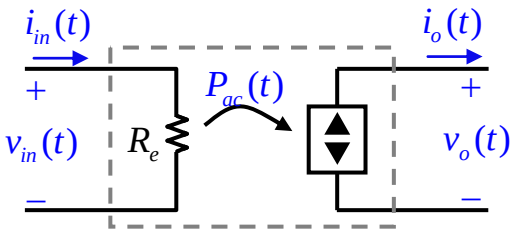


Fig. 5.3. Loss-free resistor model for an ideal rectifier.

The AC power $P_{ac}(t)$ is determined by R_e and transmitted to the output port, which is expressed as

$$P_{ac}(t) = \frac{v_{in}^2(t)}{R_e}. \tag{5-6}$$

With an assumption that the loss on the EMI filter and the bridge rectifier can be ignored compared with the output power, the AC power is also expressed by the rectified input voltage and the average of the primary current as

$$P_{ac}(t) = v_{rec}(t) i_{p,avg}(t). \tag{5-7}$$

Combining (5-6) and (5-7) by substitution of (5-5) into (5-7) gives

$$\frac{v_{in}^2(t)}{R_e} = \frac{D^2 T_s}{2L_M} v_{rec}^2(t). \tag{5-8}$$

Because $v_{rec}(t)$ is the rectified voltage of $v_{in}(t)$, their square terms are the same equation. The effective resistance R_e can be obtained as

$$R_e = \frac{2L_M}{D^2 T_s} \tag{5-9}$$

which is the same as (4-1) in the case of DCM DC-DC flyback converters. The effective resistance R_e is controllable by the duty ratio D, where D is under steady state conditions. The instantaneous input power from the AC source is

$$\begin{aligned} P_{ac}(t) &= v_{rec}(t) i_{p,avg}(t) \\ &= \frac{V_{in,pk}^2}{2R_e}(1 - \cos 2\omega_{line} t) \end{aligned} \tag{5-10}$$

where $V_{in,pk}$ is the amplitude and ω_{line} is the radian frequency of the AC line voltage.

There is a second harmonic component of the AC line frequency appearing on the instantaneous input power, which induces an output voltage ripple at $2\omega_{line}$ and is discussed in section 5.2.3. The loss-free resistor model actually removes the switching harmonics, but retains the $2\omega_{line}$ and DC components.

Output regulation is accomplished by variation of the effective resistance R_e, and hence the value of R_e must depend on the duty ratio in steady state. Assume that the efficiency of power conversion is ideal and equal to one, so the input power is equal to the output power. From (5-10), the average input power without the component at $2\omega_{line}$ is

$$P_{ac} = \frac{V_{in,pk}^2}{2R_e} = \frac{V_{in,rms}^2}{R_e} \tag{5-11}$$

and the average output power is obtained as

$$P_{out} = \frac{V_o^2}{R_L} \tag{5-12}$$

where V_o is the DC term of the output voltage v_o. Because the input power is equal to the output power, the voltage conversion ratio is estimated by combining (5-11) and (5-12) as

$$M = \frac{V_o}{V_{in,rms}} = \sqrt{\frac{R_L}{R_e}}. \tag{5-13}$$

This equation can be simplified by substitution of (5-9) to yield

$$V_o = V_{in,rms}\frac{D}{\sqrt{K}} \tag{5-14}$$

where the definition of K is equal to the one in (4-5). So far, the loss-free resistor model can be used to determine the operating point in steady state in accordance with (5-14). The next section introduces the small-signal AC model derived from the loss-free resistor model.

5.2.2 Small-Signal AC Model

Although the DCM flyback rectifier is capable of rectification when operated open-loop because of self PFC property, it is also desirable to stabilize the output voltage against variations in output power and AC line voltage. Hence, a voltage feedback loop is necessary. To design a voltage feedback loop, we need to know the control-to-output transfer function of DCM PFC flyback rectifiers.

The steps in the derivation of a small-signal AC model, suitable for design of the output voltage feedback loop, are started from the loss-free resistor model of DCM flyback rectifiers in Fig. 5.4(a). The model in Fig. 5.4(a) removes the switching harmonics, but retains the $2\omega_{line}$ and DC components. Based on self PFC property, the voltage feedback loop can not remove the $2\omega_{line}$ ripple from the output voltage, since doing so would require the duty ratio change significantly at $2\omega_{line}$, which violets the demand for constant duty ratio so that the power factor would be poor. In consequence, the crossover frequency of this voltage loop must be significantly lower than $2\omega_{line}$, so a small-signal AC model should be derived at the frequency lower than $2\omega_{line}$. The ripple at $2\omega_{line}$ can be removed by averaging over one period of $2\omega_{line}$. For instance, equation (5-11) is doing so to derive the average input power only with DC term. According to (5-12), a DC model to estimate the operating point is shown in Fig. 5.4(b) with $2\omega_{line}$ component removed. The small-signal AC model is derived by perturbing the loss-free resistor model of Fig. 5.4(a) about an operating point as follows

$$\begin{aligned} d(t) &= D + \tilde{d}(t) \\ \left\langle v_{in,rms}(t) \right\rangle_{2\omega_{line}} &= V_{in,rms} + \tilde{v}_{in,rms}(t) \\ \left\langle v_o(t) \right\rangle_{2\omega_{line}} &= V_o + \tilde{v}_o(t) \\ \left\langle i_{in,rms}(t) \right\rangle_{2\omega_{line}} &= I_{in,rms} + i_{in,rms}(t) \\ \left\langle i_o(t) \right\rangle_{2\omega_{line}} &= I_o + i_o(t) \end{aligned} \tag{5-15}$$

where all perturbations are considered at frequencies much lower than $2\omega_{line}$. The

small-signal AC model is shown in Fig. 5.4(c) and the relative parameters are shown in Table 5.2. In fact, the small-signal model is similar to the one in Fig. 4.2.

The control-to-output transfer function is

$$G_{vod}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = j_2\left(R_L \,//\, r_2\right)\frac{1}{1+sC_o\left(\left(R_L \,//\, r_2\right)\right)} = \frac{V_{in,rms}}{\sqrt{K}}\frac{1}{1+\dfrac{s}{2/R_L C_o}}. \tag{5-16}$$

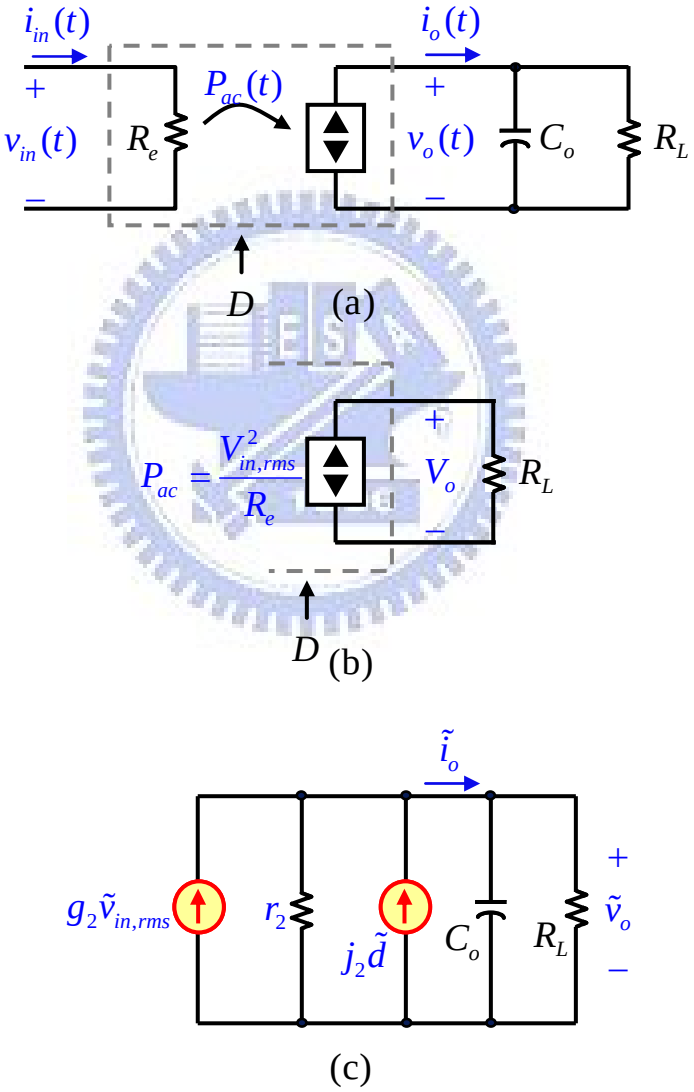


Fig. 5.4. Steps in the derivation of DC and small-signal AC model, suitable for design of the output voltage feedback loop: (a) Basic loss-free resistor model, with switching harmonics removed, but $2\omega_{line}$ and DC components retained. (b) DC model, with $2\omega_{line}$ components removed. (c) Small-signal AC model.

TABLE 5.2
PARAMETERS OF THE SMALL-SIGNAL AC MODEL

g_2	j_2	r_2
$\frac{2}{\sqrt{R_L R_e}}$	$\frac{2V_{in,rms}}{DMR_e}$	R_L

5.2.3 Output Voltage Ripple

There is a second harmonic component of the AC line frequency appearing on the instantaneous input power, which induces an output voltage ripple at $2\omega_{line}$. The current $i_o(t)$ can be expressed by

$$i_o(t) = \frac{P_{ac}(t)}{V_o} = \frac{V_{in,rms}^2}{R_e V_o}(1 - \cos 2\omega_{line} t). \tag{5-17}$$

With small voltage ripple Δv, the AC component of $i_o(t)$ flows through the output capacitor C_o while the DC component flows through the load. The output capacitor current is

$$C_o \frac{dv_o(t)}{dt} = -\frac{V_{in,rms}^2}{R_e V_o}\cos 2\omega_{line} t = -\frac{V_o}{R_L}\cos 2\omega_{line} t. \tag{5-18}$$

The output voltage ripple can be found by integration of (5-18). The result is

$$\Delta v_o(t) = \int dv_o(t) = -\frac{V_o}{C_o R_L}\int \cos(2\omega_{line} t)dt = -\frac{V_o}{C_o R_L}\frac{1}{2\omega_{line}}\sin(2\omega_{line} t). \tag{5-19}$$

So, the peak-to-peak value of the output voltage ripple is

$$\Delta v_o = \frac{V_o}{2\omega_{line} C_o R_L}. \tag{5-20}$$

This result states that the output capacitor should be chosen properly and the output $R_L C_o$ natural frequency should be significantly lower than $2\omega_{line}$ to satisfy the assumption that the output voltage ripple is much smaller than the DC term of the output voltage.

5.3 PRIMARY-SIDE SENSING CONTROL ALGORITHM DESIGN

5.3.1 Digital PI Controller Design

It is mentioned before that the crossover frequency should be significantly lower than $2\omega_{line}$ to prevent the duty ratio change significantly at $2\omega_{line}$, which violets the demand for constant duty ratio and degrades the power factor. A good choice of the crossover frequency is about one tenth to one fifteenth of $2\omega_{line}$. The design procedure is the same as in section 4.2.1.

5.3.2 Multimode Digital Control

The most important thing for PSS technique is the sampling instant. If the sensed voltage is wrong, the digital control scheme is useless to voltage regulation. In chapter 3, the duration in off state has been divided into three intervals T_1, T_2, and T_3, and the equations to estimate these three intervals are derived. However, the analysis in chapter 3 is for DCM DC-DC flyback converters, which can be modified to adapt the conditions of DCM PFC flyback rectifiers, so the lengths of intervals T_1, T_2, and T_3 are modified as

$$T_1 = \frac{L_M \hat{i}_p(t)}{K_p} \cdot \frac{1+K_p+K_s+K_a}{v_c(t)(1+K_s+K_a)-K_s v'_o - K_a v'_{aux}} \tag{5-21}$$

$$T_2 = \frac{L_M \hat{i}_p(t)}{K_p} \cdot \frac{(1+K_s+K_a)\left[K_s v'_o + K_p v_c(t) - v'_{aux}(1+K_s+K_p)\right]}{\left[v_c(t)(1+K_s+K_a)-K_s v'_o - K_a v'_{aux}\right](v'_{aux}+v'_{aux}K_s - K_s v'_o)} \tag{5-22}$$

$$T_3 = \frac{\hat{i}_p(t) L_M}{v'_o} \frac{(v'_{aux}-v'_o)(1+K_s)}{v'_{aux}+K_s(v'_{aux}-v'_o)} \tag{5-23}$$

where the peak of the primary current $\hat{i}_p$ and the clamped voltage v_c are functions of time, not constant in steady state. Because operating in DCM and with almost constant duty ratio for self PFC property, the peak of the primary current and the clamped voltage change with the rectified input voltage. Recall that the output voltage is sensed from the auxiliary winding during interval T_3, so the value of V_{delay}

to set the sampling instant should satisfy (3-28).

According to (5-21), (5-22), and (5-23), the boundary in (3-28) can be estimated and shown in Fig. 5.5. The *x*-axis of Fig. 5.5 is the phase of the rectified input voltage from 0° to 180°. There is a problem at the neighborhood of zero crossing of the rectified input voltage. The problem is that the sampling instant is no longer during interval T_3, so the sensed voltage is wrong. A method to avoid this situation is using multimode in digital control algorithm. The concept of multimode is shown in Fig. 5.6. There is a boundary value $v_{rec}(\theta_a)$ to determine the mode of the controller. If the rectified input voltage is higher than the boundary value $v_{rec}(\theta_a)$, the sampling instant is during interval T_3 and the digital control algorithm is in mode S_1. In mode S_1, the duty ratio is controlled by the designed digital PI controller. Otherwise, if the rectified input voltage is lower than the boundary value $v_{rec}(\theta_a)$, the sampling instant is out of interval T_3 and the digital control algorithm is in mode S_2. In mode S_2, the sensed voltage is no longer correct, so the duty ratio is kept constant as the value at $v_{rec}(\pi - \theta_a)$, which means the system is under open-loop control. To accomplish the multimode digital control, the rectified input voltage should be monitored by the DSP chip and the boundary of the two modes should be chosen properly. The flowchart of multimode digital control for DCM PFC flyback rectifiers is shown in Fig. 5.7.

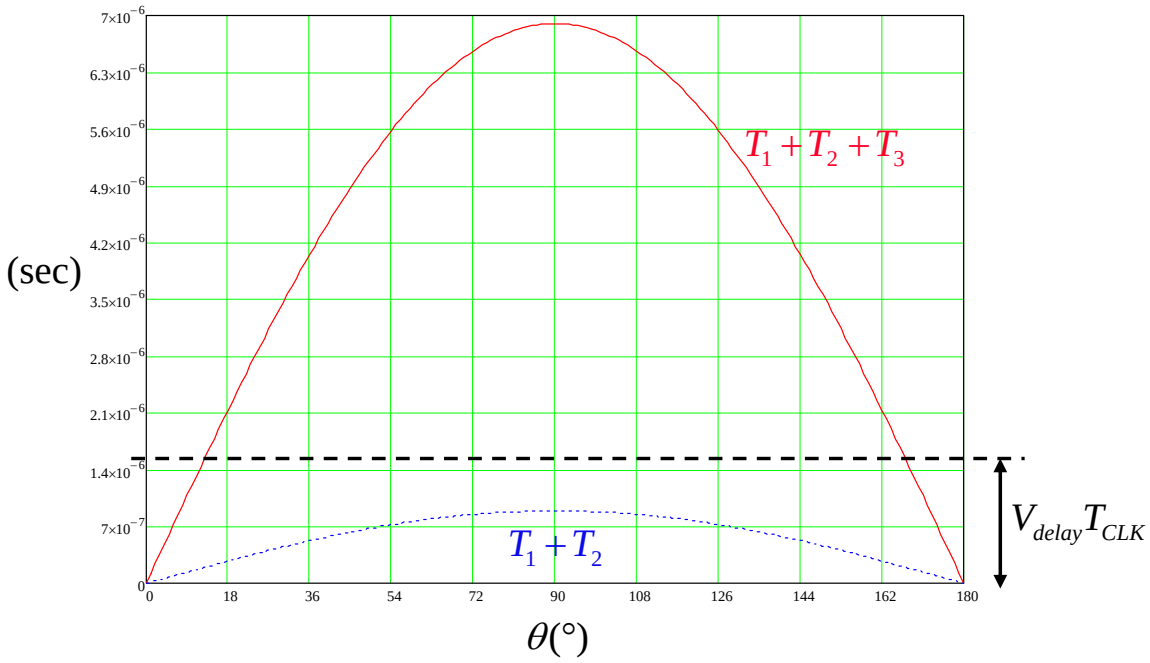


Fig. 5.5. Timing plot of intervals T_1, T_2, T_3, and the sampling instant.

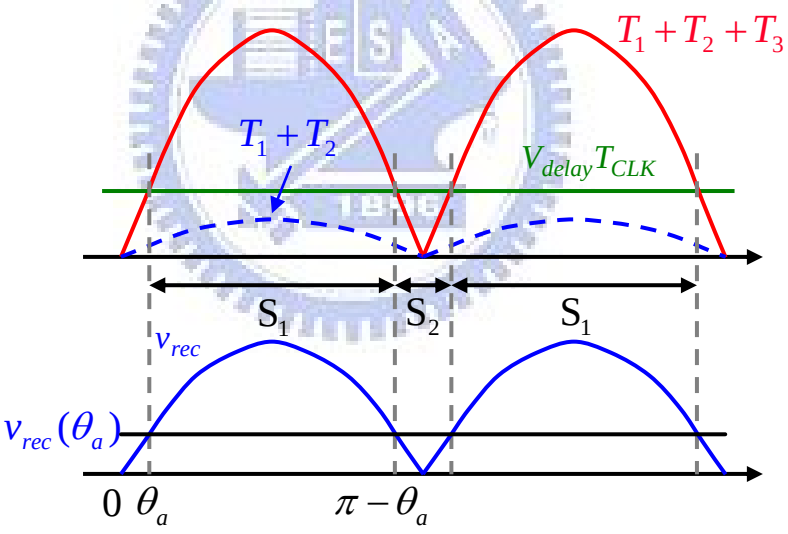


Fig. 5.6. Definition of multimode digital control.

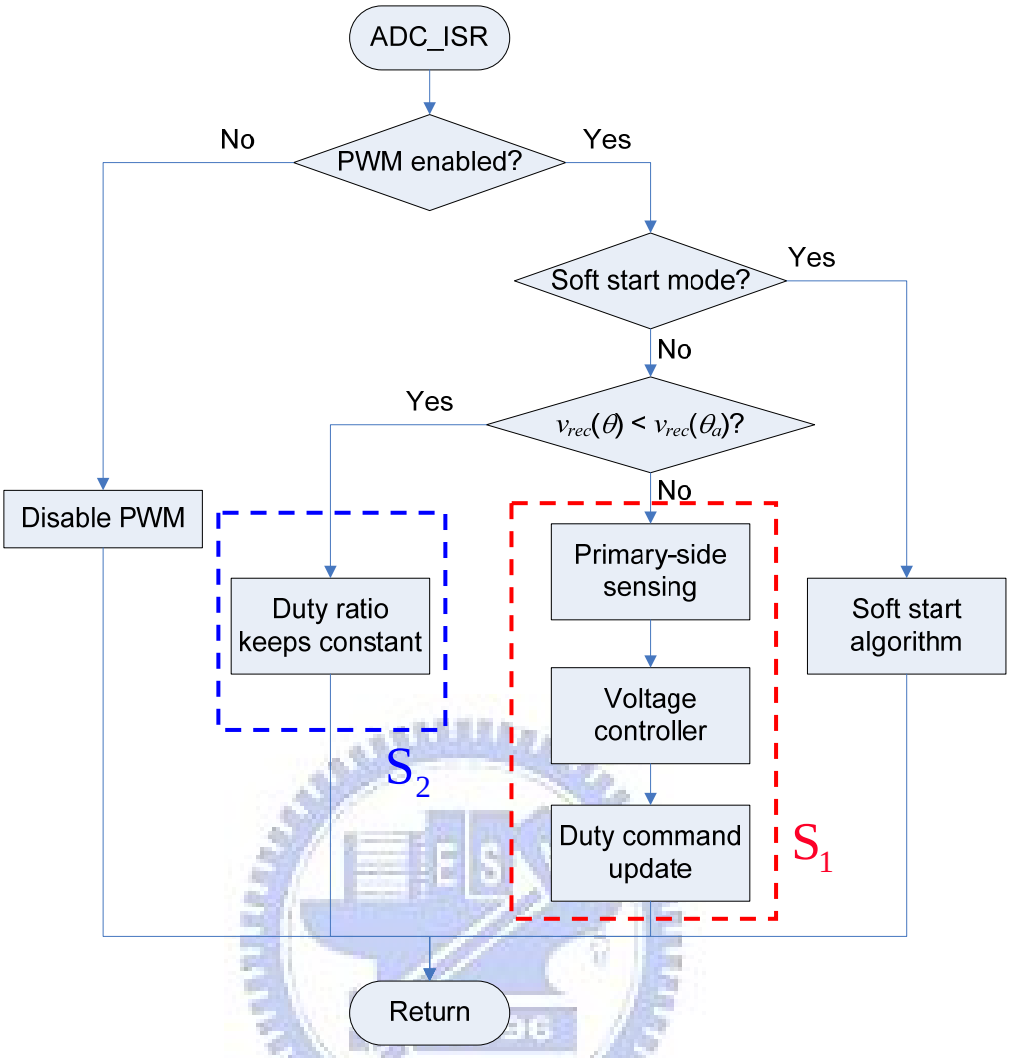


Fig. 5.7. Flowchart of multimode digital control.

5.4 Simulation and Experimental Results

To verify PSS technique for DCM PFC flyback rectifiers, a prototype of flyback rectifiers with PSS is designed at 50 W rated output power. The AC line voltage is 110 Vrms, the nominal output voltage is 19 V, the switching frequency is 50 kHz, the magnetizing inductance is 120 μH referred to the primary side, the flyback transformer turns ratio n_{ps} is 2.9, and the output capacitance is 4700 μF.

To reveal the problem at the neighborhood of zero crossing of the rectified input voltage, the AC line voltage and the voltage on the auxiliary winding are shown in Fig. 5.8. From Fig.

5.8(a), there is a flat level in off state, actually in interval T_3 defined before, to sample the output voltage, but there is no such a flat level in off state when the AC line voltage is close to zero shown in Fig. 5.8(b). Therefore, multimode digital control is necessary to overcome this situation. An open loop test is done to figure out what the proper boundary value is to determine the mode of the controller. The simulation results and experimental results are shown in Figs. 5.9 and 5.10 respectively in full-load and half-load conditions. The sensed voltage in the DSP chip is sent to a DAC to generate the signal v_{fb} in Fig. 5.10. The sensed voltage decreases strictly near the zero crossing region because the ADC samples the signal in reset state, not in off state. The waveforms named MODE show the mode of the controller. The controller is in mode S_2 when MODE is high and in mode S_1 when MODE is low. In this design case, the boundary value $v_{rec}(\theta_a)$ is chosen as 50 V. With multimode control, the voltage controller avoids to calculate a wrong duty command due to the wrong sensed voltage. In mode S_2, the duty command is constant and equal to the value at the end of mode S_1 shown in Figs. 5.9(a) and 5.9(b).

The bandwidth of this system is designed at about 6 Hz to make the duty command not change significantly at $2\omega_{line}$ to satisfy the self PFC property. The power factor and the total harmonic distortion (THD) of the AC line current are measured in steady states of half-load and full-load conditions. In Fig. 5.11, the waveforms of the AC line current and voltage are in phase, the power factor is measured as 0.99, and the THD of the AC line current is 4.5% in full-load condition and 8.8% in half-load condition. On the other hand, the load transient response from half load to full load is tested by simulation and experiement shown in Figs. 5.12 and 5.13, respectively. The output voltage is recovered after 93.7 ms when the load step occurs and the voltage drop is 2.4 V by simulation while the output voltage is recovered after 120 ms when the load step occurs and the voltage drop is 1.6 V by experiment. All results in this section show that PSS technique is applicable to a DCM PFC flyback rectifier.

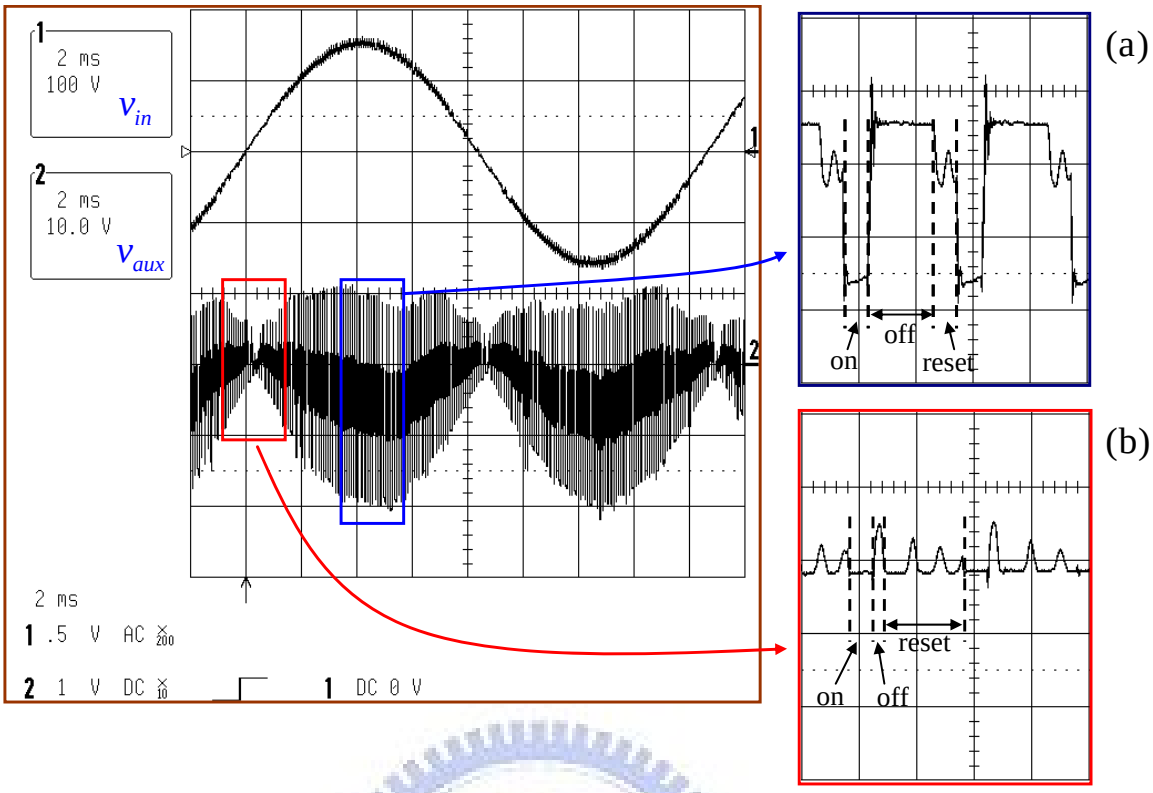


Fig. 5.8. Voltage on the auxiliary winding: (a) when the AC line voltage is maximum, (b) when the AC line voltage is close to zero.

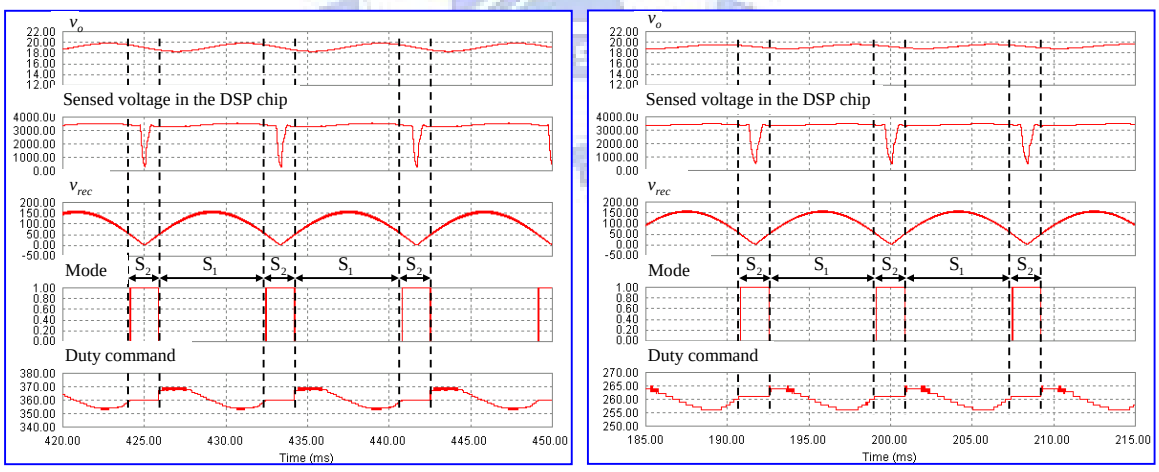


Fig. 5.9. Simulation results to show the mode switching (a) in full-load condition, (b) in half-load condition.

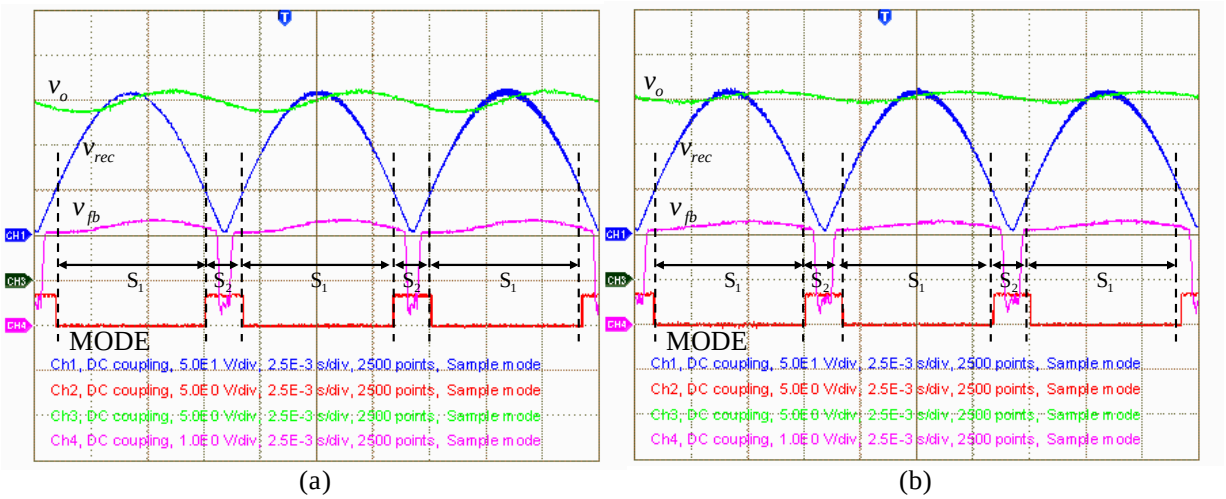


Fig. 5.10. Experimental results to show the mode switching (a) in full-load condition, (b) in half-load condition.

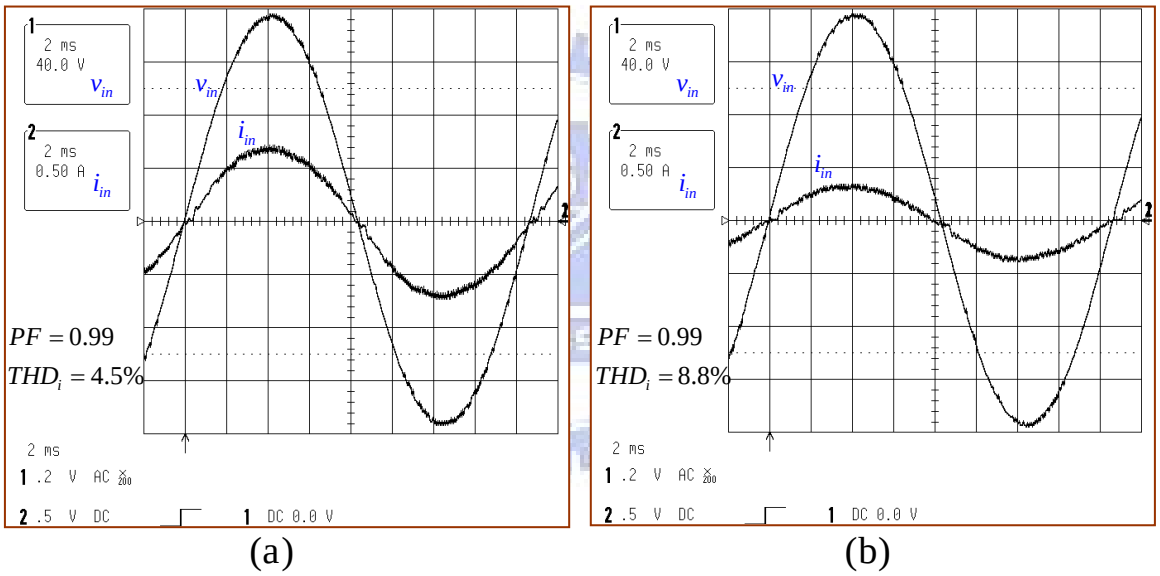


Fig. 5.11. AC line voltage and current of the designed flyback rectifier (a) in full-load condition, (b) in half-load condition.

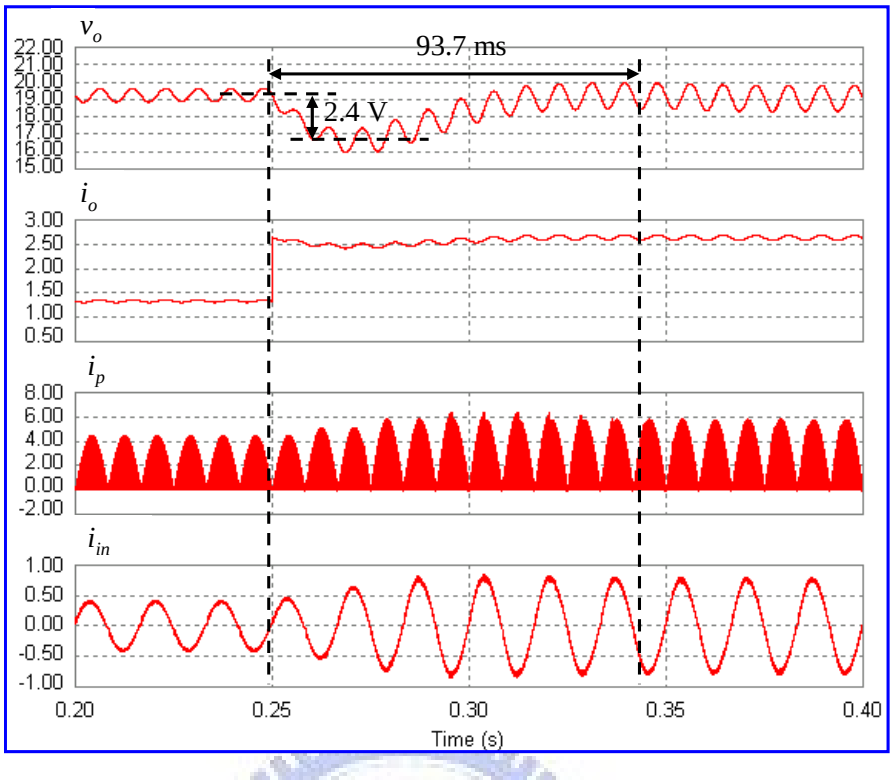


Fig. 5.12. Simulation waveforms of load transient response of the designed PFC flyback rectifier from half load to full load.

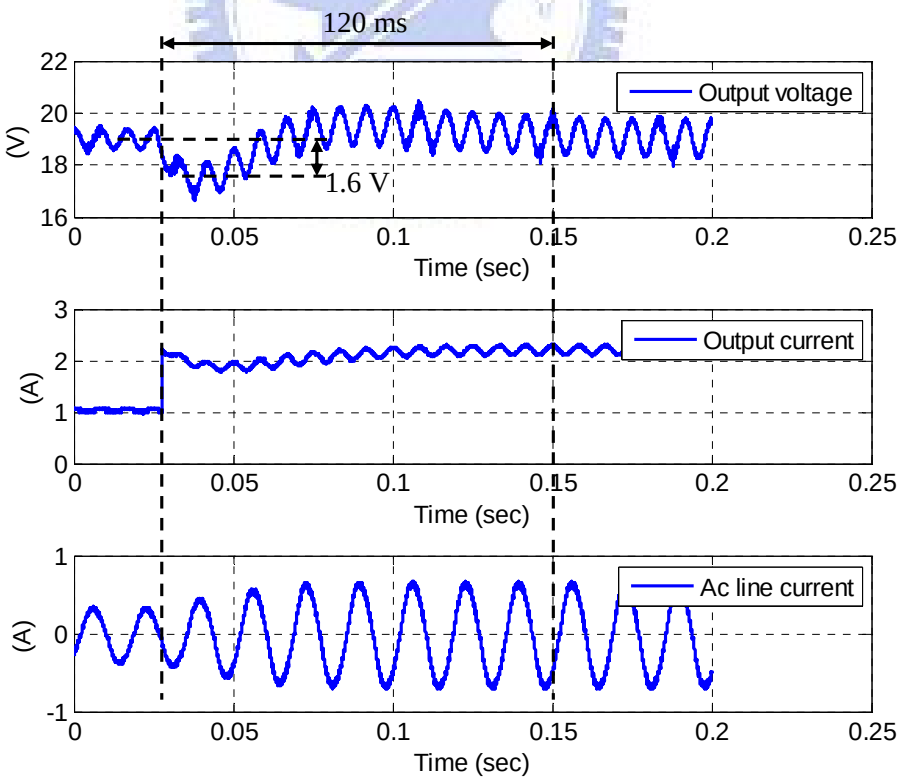


Fig. 5.13. Experimental waveforms of load transient response of the designed PFC flyback rectifier from half load to full load.

Chapter 6

Conclusion and Future Works

6.1 CONCLUSION

This work has presented the digital PSS technique for flyback converters. The proposed digital control is implemented by a DSP chip, TMS320F2812. Two popular applications of flyback converters are discussed in this thesis, where one is a DC-DC flyback converter and the other is a single-stage PFC flyback rectifier.

The analysis of the sensing error of PSS technique has been carried out for flyback converter with an auxiliary winding. An analytical model of the flyback transformer has been adopted for the sensing error analysis due to factors such as leakage inductance, winding resistance, voltage drop of the rectified diode on the secondary winding, and effective turns ratio. The sampling instant plays a key factor for correct detection of the output voltage from the auxiliary winding. The developed error analysis method provides an insight for the design of flyback transformers used for PSS applications and it also illustrates that more sophisticated PSS algorithms can be developed to improve the accuracy of PSS flyback converters.

Chapter 4 discussed the implementation of DCM DC-DC flyback converters with PSS. The sensing error caused by the winding resistance can be reduced by sampling instant modulation. For controller design, the conventional model and design procedure of flyback converters are suitable for flyback converters with PSS technique. In this chapter, we verify that the PSS technique is applicable to flyback converters. The performance of voltage

regulation is excellent with only 1% deviation. PSS technique only controls the output voltage before the output *LC* filter, which means that the output voltage after the output *LC* filter is uncontrolled. Therefore, the *LC* filter must be designed properly to avoid unstable conditions or a large voltage drop when a load step occurs.

Chapter 5 discussed the implementation of DCM PFC flyback rectifiers. In order to avoid incorrect sampling, a multimode digital control method is implemented. Although multimode digital control is under open-loop control in mode S_2, the output voltage is still regulated when a load step occurs. The THD of the ac line current is only 4.5% in full-load condition.

6.2 FUTURE WORKS

Although PSS technique can be used for flyback converters with dc or ac input voltage, there is a problem to control the output voltage at very light loads. Because the conduction time of the secondary diode is short at very light loads, the sampling instant is difficult to determine to sense the output voltage from the auxiliary winding in interval T_3. PSS technique should be improved to overcome the situations at light loads, no load, or standby mode.

QR flyback converters are getting popular for low power applications in recent years. PSS technique is very suitable to QR flyback converters because the control scheme of QR flyback converters needs valley detection to switch the power MOSFET. This may also help to set the sampling instant for PSS technique.

With the advance of power control IC realization technology, digital technique is able to implement more sophisticated control and protection for PSS technique to improve the performance of power systems.

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