國立交通大學

電控工程研究所

碩士論文

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多階非線性度的嶄新數位背景複相關估測方法

A Novel Digital Background Multi-Correlation Estimation
Method for Estimating Multiple-Order Nonlinearity
of the Residue Amplifiers in Pipelined ADCs

研 究 生：吳崑池

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中 華 民 國 九 十 九 年 七 月

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碩士論文

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中華民國九十九年七月

新竹 國立交通大學

一個用以估測導管式類比數位轉換器中殘值放大器
多階非線性度的嶄新數位背景複相關估測方法

學　　生　：吳峊池　　　　　指導教授：洪浩喬　教授

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摘要

　　隨著先進製程不斷進步，數位電路因而獲得高速與低功耗的好處。相反地，在先製進製程下因為供應電壓下降、本質增益縮小以及低輸出阻抗等因素，使得設計高效能類比電路的挑戰與日俱增。例如：在先進的CMOS技術下，要設計導管式類比數位轉換器中足夠線性的殘值放大器，變成一項艱鉅的任務。為了解決這些難題，近年許多研究便致力於發展數位校正機制，這些「數位輔助類比電路設計」的核心概念是希望透過穩健的數位電路的幫助來減輕類比電路設計的難度。

　　本篇論文提出一個可以精確估測導管式類比數位轉換器中殘值放大器多階非線性度的數位背景複相關估測方法。我們利用加入不同振幅的隨機序列，透過一個數位化的相關機制精確地粹取出帶有非線性度的訊息，而且只要使用簡單的數位電路就能實現這個估測方法，藉由這樣的方式能夠有效地降低類比電路設計的複雜度。

　　我們使用一個第一導管級中的殘值放大器具有多項奇次階非線性失真的十四位元每秒一億次取樣之導管式類比數位轉換器為例。根據模擬結果顯示：在校正前，有效位元(ENOB)為4.9位元、SNDR為31.2dB、SFDR為45.2dBc、INL為+165.50/-166.25LSB、DNL為+11.61/-1.00LSB。透過校正後，ENOB為13.1位元，有高達8.2位元之多的改善。而SNDR及SFDR則分別為80.4dB與94.7dBc，INL與DNL則分別為+0.66/-0.50LSB與+0.55/-0.59LSB。此外我們也模擬其第一導管級的殘值放大器具有多階非線性失真(包含偶次階的非線性)時的情形。模擬結果顯示，於校正前，ENOB為6.4位元、SNDR為40.1dB、SFDR為54.5dBc、INL為+89.79/-55.81LSB而DNL為+6.13/-1.00LSB。經過校正後，此導管式類比數位轉換器具有高達13.9位元的ENOB，而SNDR為85.5dB、SFDR為123.5dBc、INL為+0.46/-0.49LSB、DNL為+0.46/-0.73LSB。經由模擬結

果證實，所提出的方法確實能大幅地提升導管式類比數位轉換器之效能。

　　本篇論文也討論一個用以搭配開迴路架構設計的十二位元每秒一億次取樣導管式類比數位轉換器[1]的數位校正處理器[2]實現電路。模擬結果顯示其數位校正技術能明顯地提升導管式類比數位轉換器的效能。

A Novel Digital Background Multi-Correlation Estimation Method for Estimating Multiple-Order Nonlinearity of the Residue Amplifiers in Pipelined ADCs

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Abstract

As advanced technology scales, digital circuits benefit from advanced technologies for faster operation and lower power. On the contrary, designing high performance analog circuits in the advanced technologies becomes more challenging due to the reduced supply voltage, low intrinsic gains and low output impedances, etc. For example, it is difficult to design a linear enough residue amplifier in advanced CMOS technologies for pipelined ADCs. To address these challenges, many recent researches focus on developing digital calibration schemes. Their "digital-assist analog circuit design" concept is to alleviate the hard analog design work with the help of robust digital circuits.

This thesis presents a novel digital background multi-correlation estimation (MCE) method that can accurately estimate multiple-order nonlinear terms of the residue amplifiers' transfer functions in pipelined ADCs. By injecting several random sequences of different amplitudes alternatively, the proposed estimation method accurately extracts the information of the nonlinearity through a correlation mechanism in the digital domain. The proposed estimation scheme can be implemented with simple digital circuits and effectively reduces the complexity of the required analog circuit designs.
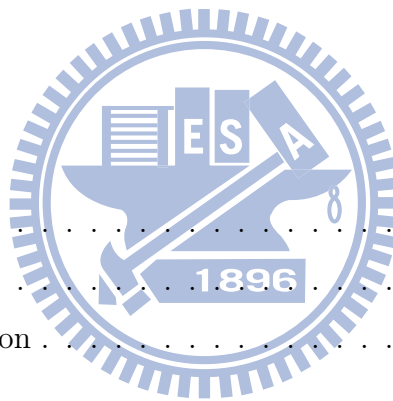
We use a 14-bit 100MS/s pipelined ADC with a multiple-odd-order nonlinearity residue amplifier in the first pipeline stage as an example. Simulation results show that before calibration, the ADC only has an effective number of bits (ENOB) of 4.9 bits, an

SNDR of 31.2 dB, an SFDR of 45.2 dBc, INL values within +165.50/-166.25 LSB, and DNL values within +11.61/-1.00 LSB. After calibration, its ENOB becomes 13.1 bits. A significant 8.2-bit ENOB improvement is achieved. The SNDR and SFDR are 80.4 dB and 94.7 dBc, respectively. The calibrated INL and DNL are +0.66/-0.50 LSB and +0.55/-0.59 LSB, respectively. Simulation results also show that the same model of the pipelined ADC but with a multiple-order (contained with even-order nonlinearity) nonlinear residue amplifier in the first stage before calibration only has an ENOB of 6.4 bits, an SNDR of 40.1 dB, an SFDR of 54.5 dBc, INL values within +89.97/-55.81 LSB and DNL values within +6.13/-1.00 LSB. After calibration, the pipelined ADC has an ENOB of 13.9 bits, an SNDR of 85.5 dB, an SFDR of 123.5 dBc, INL values within +0.46/-0.49 LSB and DNL values within +0.46/-0.73 LSB. The simulation results validate that the proposed scheme does have a significant improvement on the pipelined ADC's performance.

This thesis also discusses the circuit implementation of a digital background calibration processor [2] for a 12-bit 100MS/s pipelined ADC prototype with open-loop residue amplifiers [1]. The simulation results of this prototype show a great improvement on the pipelined ADC's performance with the digital calibration technique.

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Chapter 1

INTRODUCTION

1.1 Motivation

Fuelled by aggressive device scaling down in modern fabrication technology, digital circuits become smaller, less power consuming, and capable of operating at a high speed. On the contrary, analog circuits suffer from limited supply voltage headroom and low intrinsic device gains. Due to the challenge of designing high performance analog circuits in deep submicron technology, digital-assist analog design become a vital solution [3].

Data converters are key elements in many mixed-signal applications. Among different analog-to-digital converters (ADCs), pipelined ADCs are widely used in the applications that need medium to high resolution (10-bit to 16-bit) and a bandwidth in the range from tens to hundred MHz such as video imaging systems, portable devices, instrumentations, broadband communication transceivers and so on [4]. Generally speaking, pipelined ADCs are popular when the required signal bandwidth is too high for the oversampling sigma-delta ADCs to achieve, and the required resolution is too high for flash ADCs to be efficient [5].

Within the scope of pipelined ADC researches, the focus has been taken on the techniques to reduce the power consumption. The key building blocks in a pipelined ADC are the residue amplifiers because they need to meet the severe speed, noise, and linearity requirements. As a result, the power of the residue amplifiers usually

dominate the overall power dissipation of the pipelined ADC. Conventional approaches to reduce the power consumption include opamp sharing [6]–[9], switched opamp [10, 11], power-efficient opamp topologies[3],[12]–[16], etc. Due to replacing the power-hungry amplifiers by the power-efficient ones, the linearity becomes a critical issue which may limit the resolution of the pipelined ADCs. In fact, a pipelined ADC design usually requires some linearity enhancement techniques to achieve an effective resolution higher than 12 bits [17]. As a result, self-calibration techniques which compensate errors from the residue amplifiers for pipelined ADCs have attracted more attention nowadays.

1.2 Overview

Recent researches in low power pipelined ADC design can be classified into two categories according to the targets of the ADCs. The first category consists of the pipelined ADCs with medium resolution (about 10-bit) and very low power consumption (several mW). The researches belonging to this category usually replaces the traditional opamp-based multiplying digital-to-analog converter (MDAC) with a novel circuit topology such as dynamic source follower residue amplifiers [12]. The other one focuses on the design of the pipelined ADCs with high resolution (above 12-bit) and low power consumption (hundred mW). These pipeline ADC designs are usually implemented with opamp-based MDACs and adding some self-calibration schemes [18, 4]. Figure 1.1 shows the statistical results of ADC research from 1997 to 2009 with respect to their speed and power (versus resolution).

In general, self-calibration methods can be considered from two different points of view [19]:

- How the methods correct the errors:

    - Analog domain: trimming the circuit components or eliminating their resulting errors.

    - Digital domain: by processing the raw bits in the digital domain.

- When the calibration process takes place:
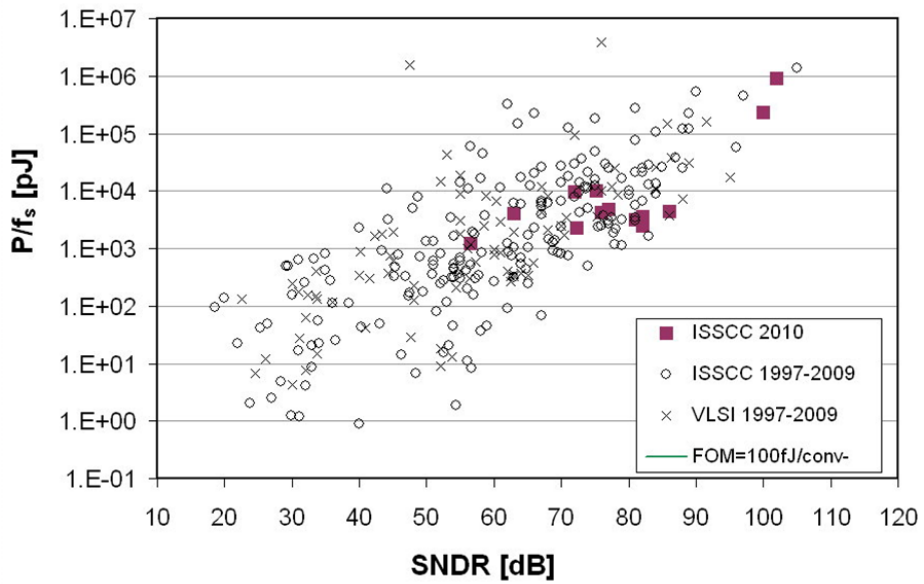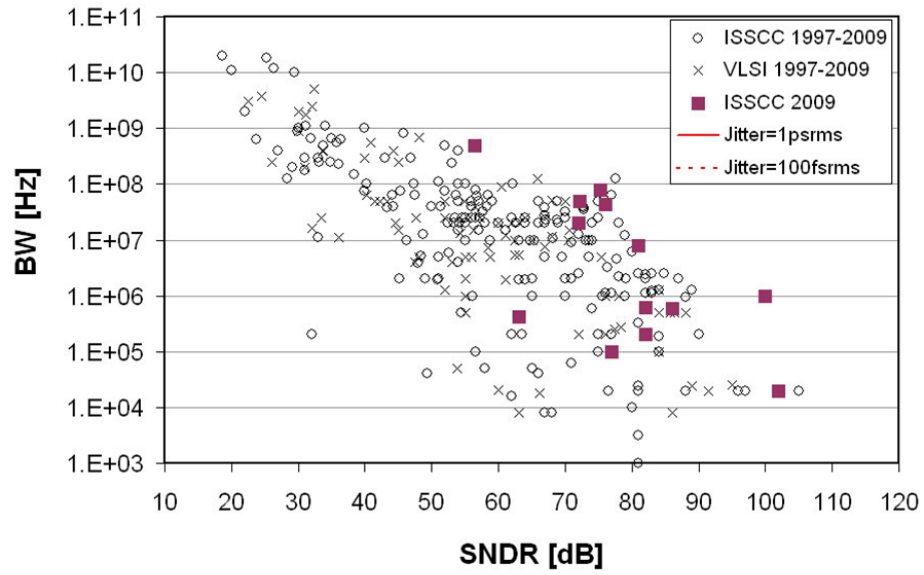
[source: Boris Murmann, Stanford University]

Figure 1.1: ADCs research tendency.

- Background calibration: the calibration process operates simultaneously with data conversion operation.

- Foreground calibration: dedicating a special time slot for the purpose of calibration before the normal data conversion operation of the ADC.

The calibration methods in digital domain are more popular than those in analog domain due to the ease and the low cost of implementing the calibration algorithms digitally. Digital calibration methods also require less additional analog components. On the other hand, analog-domain calibrations usually have to use complex analog circuits and the conversion speed is often reduced.

Background calibrations are more attractive than foreground calibrations due to background calibrations can continuously calibrate their internal pipeline stages to track environmental changes without interrupting the normal ADC conversion.

This thesis is concerned with improving the pipelined ADC performance with a digital background calibration technique to have high resolution, high speed, and low power consumption. This thesis comprises two major parts:

- A circuit implementation of the digital background calibration processor [2] for a 12-bit 100MS/s pipelined ADC prototype with open-loop residue amplifiers [1].

- A novel digital background multi-correlation estimation (MCE) method for estimating multiple-order nonlinear terms of the residue amplifiers in pipelined ADCs is proposed.

1.3   Chapter Organization

The Organization of this thesis is given as follow:

- Chapter 2 describes the ADC performance metrics and a brief discussion about the fundamentals and the error sources of the pipelined ADC.

- Chapter 3 reviews previous proposed digital background calibration schemes and gives analysis on their limitations.

- Chapter 4 introduces the adaptive signal processing and the LMS algorithm.

- Chapter 5 describes the circuit implementation of the digital background calibration processor [2] for a 12-Bit 100MS/s Pipelined ADC prototype with open-loop residue amplifiers [1].

- Chapter 6 gives the simulation results of the prototype.

- Chapter 7 aim at giving comprehension of the proposed digital background MCE method for estimating multiple-order nonlinear terms of the residue amplifiers in pipelined ADCs.

- Chapter 8 gives the simulation results that validate the proposed scheme. From the simulation results, we have shown a great improvement on the ADC's performance with the proposed scheme.

- Chapter 9 gives conclusions and recommendations for future works.
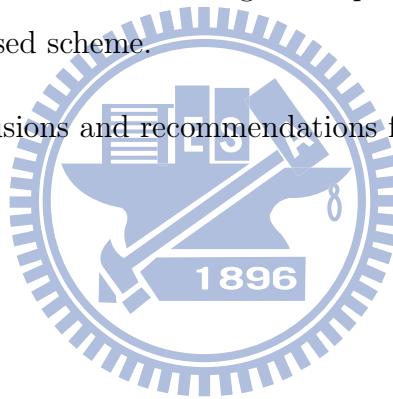
Chapter 2

PIPELINED ADC OVERVIEW

The ADC plays an important role in many mixed-signal systems because it connects the "real world" with the "digital world". There're different types of ADCs such as the sigma-delta ADC, the flash ADC, the successive-approximation-register (SAR) ADC, and the pipelined ADC. Among various structures, the pipelined ADC is the most popular one because it can simultaneously achieve a high speed and high resolution. This chapter introduces the performance metrics of ADCs and gives a review about the fundamentals of the pipelined ADC and the error sources in a pipeline stage.

2.1 ADC Performance Metrics

To characterize ADCs, some performance metrics must be defined. The discussion of the ADC's characterizations is separated into two parts including the static characterization and the dynamic characterization in the following [20, 21].

Figure 2.1 shows the input-output (I/O) characteristic for an ideal 3-bit ADC. The input voltage is from 0 to V_{REF} and converts to the corresponding output codes. The least significant bit (LSB) voltage step of the input voltage is defined as

$$V_{LSB} = \frac{V_{REF}}{2^N},\qquad(2.1)$$

where N is the number of the output bits of the ADC. Every two adjacent digital output

codes have one LSB difference as shown in Fig. 2.1.
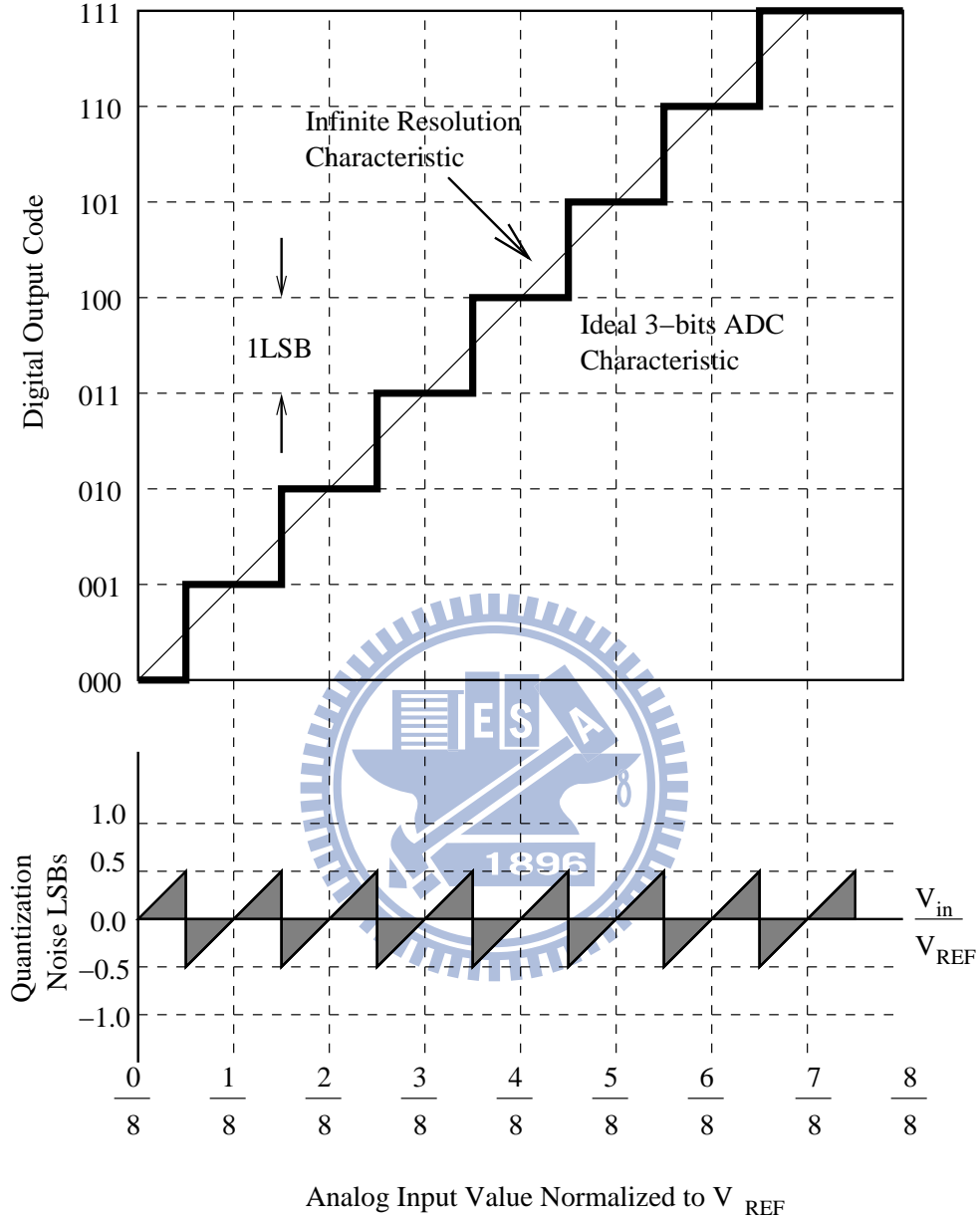
Figure 2.1: Ideal input-output characteristics of a 3-bit ADC.

The difference between the infinite resolution characteristic and the ideal 3-bits characteristic is called the quantization noise (or quantization error) of the ADC. Beneath Fig. 2.1 is the quantization noise plot as a function of the input. It's obvious that the quantization error lies between ± 0.5LSB.

2.1.1 Static Characterization

The static characterization of ADCs is signal-independent and based on the I/O characteristic of ADCs. The primary characteristics that define the static performance of an ADC are the offset error, the gain error, the integral nonlinearity (INL), and the differential nonlinearity (DNL).

2.1.1.1 Offset Error
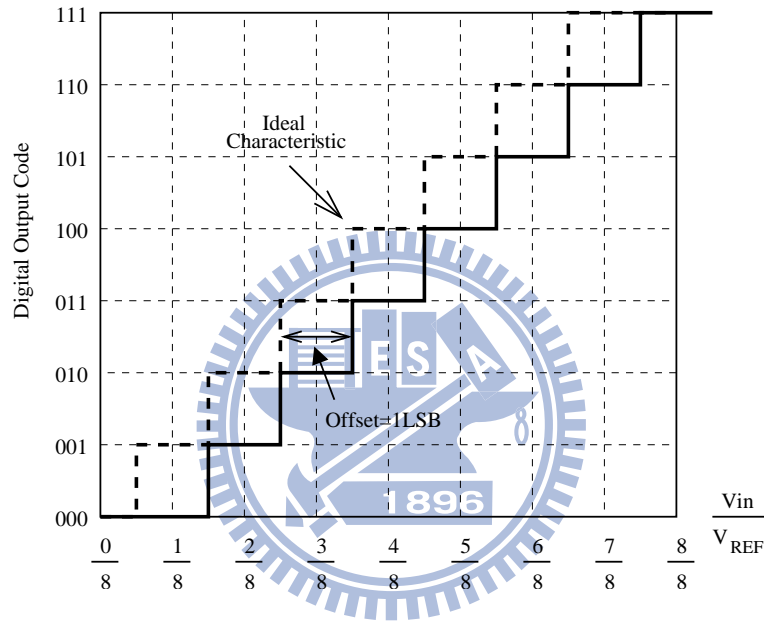
Figure 2.2: Offset error of a 3-bit ADC.

In Fig. 2.2, the offset error of an ADC is defined as the horizontal difference between the actual characteristic and the ideal characteristic that passed through the origin.

2.1.1.2 Gain Error

The gain error of an ADC is defined as the difference between the actual characteristic and the ideal characteristic which is proportional to the magnitude of the input signal as shown in Fig. 2.3. Measuring the horizontal difference in LSBs between the actual characteristic and the ideal characteristic located at the maximum code obtains the gain error of the ADC.
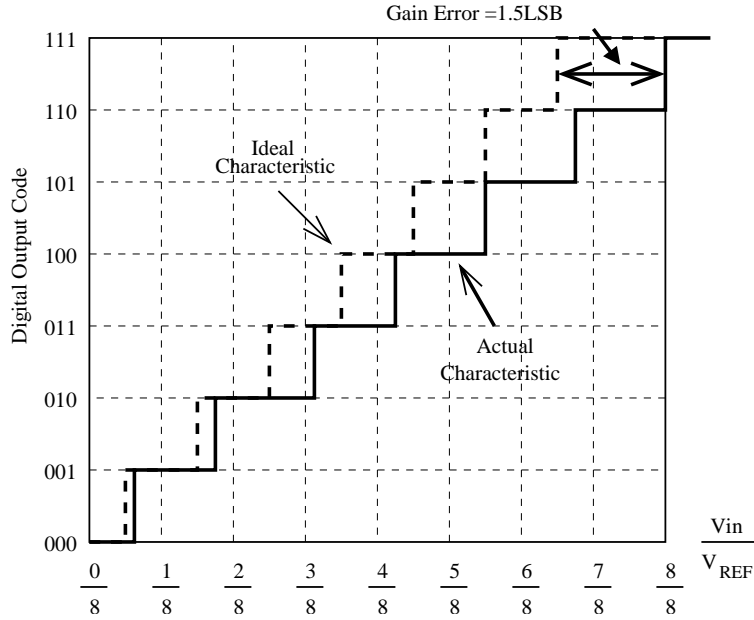
Figure 2.3: Gain error of a 3-bit ADC.

2.1.1.3 Integral Nonlinearity (INL) and Differential Nonlinearity (DNL)

After both the offset and gain errors are removed, the INL is defined as the deviation of the actual characteristic from the ideal one. That is, the separation of the code center between the actual one and the ideal one. A conservative measure of INL is to use the endpoints of the converter's transfer response and an alternative definition is to find the best-fit line such that the maximum difference is minimized.

The DNL is defined as the variation in analog step sizes away from 1 LSB,

$$DNL(n) = \frac{V_{actual}(n+1) - V_{actual}(n)}{V_{LSB}} - 1 \text{ LSB}. \tag{2.2}$$

Therefore, if DNL=-1 LSB, that means a code is missing. These two definitions are illustrated in Fig. 2.4.

2.1.2 Dynamic Characterization

The dynamic characterization is signal-dependent. The dynamic characteristics are also an important part of the characterization of ADCs. The primary dynamic characterization of ADCs is the signal-to-noise-ratio (SNR), the signal-to-noise-and-distortion-ratio
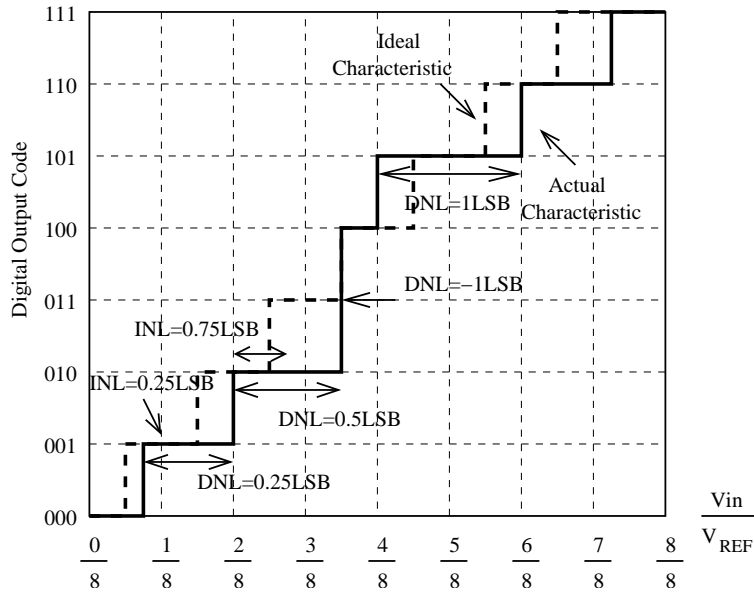
Figure 2.4: INL and DNL of a 3-bit ADC.

(SNDR), and the effective number of bits (ENOB).

2.1.2.1 Signal-to-Noise-Ratio (SNR)

The SNR is defined as the power ratio of the signal to that of the quantization noise. By stochastic approach, the quantization noise is varying rapidly as shown in Fig. 2.1 such that it can be considered as a random variable uniformly distributed between $\pm 0.5 V_{LSB}$. The probability density function (PDF) $f_Q(x)$ of the quantization noise is shown in Fig. 2.5.
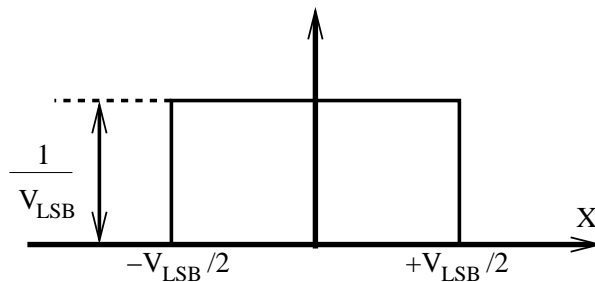
Figure 2.5: Probability density function of the quantization noise.

The root mean square (rms) value of the quantization noise can be found by

$$V_{Q,rms} = \left(\int_{-\infty}^{\infty} x^2 f_Q(x) dx \right)^{1/2} = \frac{V_{LSB}}{\sqrt{12}}. \qquad (2.3)$$

If the input signal is a sawtooth with a height of V_{REF} or a random signal uniformly distributed between 0 and V_{REF}, then the SNR can be shown to be

$$SNR = 20 log \left(\frac{V_{in,rms}}{V_{Q,rms}} \right) = 20 log \left(\frac{V_{REF}/\sqrt{12}}{V_{LSB}/\sqrt{12}} \right) = 6.02 N \, dB. \qquad (2.4)$$

A more commonly used case is to assume a sinusoidal input signal with an amplitude of $V_{REF}/2$. The SNR equation is changed to

$$SNR = 20 log \left(\frac{V_{in,rms}}{V_{Q,rms}} \right) = 20 log \left(\frac{V_{REF}/2\sqrt{2}}{V_{LSB}/\sqrt{12}} \right) = 6.02 N + 1.76 \, dB. \qquad (2.5)$$

2.1.2.2 Signal-to-Noise-and-Distortion-Ratio (SNDR)

The SNDR is defined as the power ratio of the signal to the sum of the total noise caused by both quantization noise and the harmonic distortions. In practice, given a single tone sinusoidal input signal to an ADC causes the ADC have an output spectrum containing not only the input signal component but also some harmonic distortions. The measured SNDR is usually less than the measured SNR.

2.1.2.3 Effective Number of Bits (ENOB)

The ENOB of an ADC is defined as

$$ENOB = \frac{SNR - 1.76}{6.02} \qquad (2.6)$$

according to (2.5).

2.2 Fundamentals of the Pipelined ADC
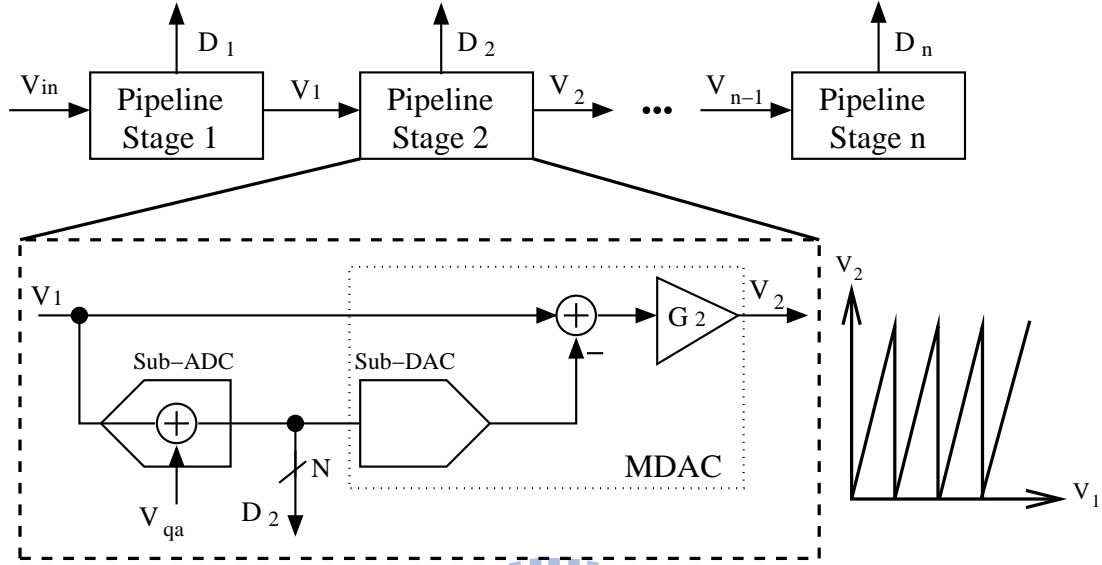
Figure 2.6: Pipelined ADC block diagram.

Figure 2.6 shows a general block diagram of a pipelined ADC which is formed by cascading several pipeline stages. Within each pipeline stage, the input signal is first sample-and-hold (S/H) and then quantized by a sub-ADC to generate an N-bit digital output code, where v_{qa} in Fig. 2.6 denotes the quantization error of the sub-ADC. The digital output code is then converted back to a corresponding analog signal by a sub-DAC. The summation node subtracts this quantized analog signal from the input signal and yields the quantization error. The quantization error is then amplified by 2^N to recover to the original full scale by a residue amplifier and passed to the next pipeline stage for the same signal processing. Its transfer curve is also shown in the figure. If it resolves two bits per stage, i.e., the transfer curve has four segments. The concept of the pipelined ADC conversion is illustrated in Fig. 2.7 which is an example that each pipeline stage is a 2-bit/stage configuration and the interstage gain is 2^2. In switched-capacitor (SC) implementation, the functions of S/H, sub-DAC conversion, subtraction and amplification are usually combined together using a circuit called the multiplying-DAC (MDAC).

Finally, the overall digital output code D_{out} can be obtained by recombining the

digital raw codes of each pipeline stage using the following expression

$$D_{out} = \sum_{i=1}^{n} \frac{D_i}{\prod_{j=0}^{i-1} G_j}, \quad (G_0 = 1 \text{ for primary input}) \tag{2.7}$$

, where D_i and G_j denote the digital raw codes and the gain of the residue amplifier in each pipeline stage and n is the total number of pipeline stages.

The number of bits for a single pipeline stage to convert depends on the applications. It's a tradeoff between speed and resolution. For a high speed requirement, a low number of bits per stage may be a better choice since the gain of each pipeline stage would be lower which allows a higher bandwidth. On the other hand, low-speed and high-resolution applications tend to have a larger number of bits per stage [22].
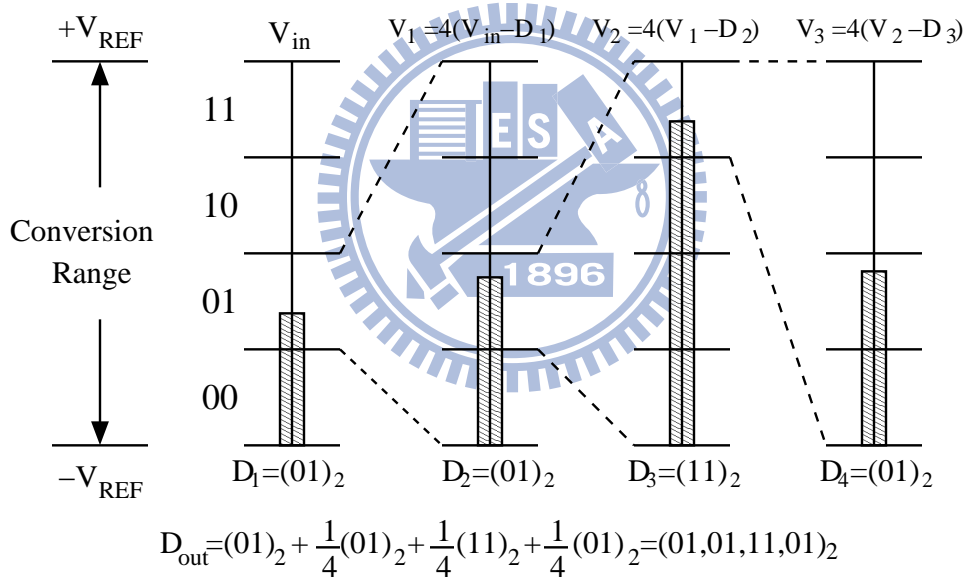
Figure 2.7: Concept of the pipelined ADC conversion.

2.3 Error Sources in a Pipeline Stage

Major error sources in a pipeline stage consist of the sub-ADC offset, the sub-DAC error, the gain error and the nonlinearity of the residue amplifier.

Variability in MOSFETs' threshold voltages leads to a comparator offset error in the sub-ADC. This error can be mitigated in the digital domain by using over-range codes,

called *digital error correction* (DEC) [23]. A detailed analysis of the DEC technique can be found in [2, 24].

The sub-DAC error in a pipeline stage is mainly due to the mismatched capacitors. The DNL of the sub-DAC due to the mismatched capacitors is inversely proportional to the square root of the total capacitance value in the sub-DAC [25]. If the capacitance values are chosen high enough to meet the kT/C consideration [26], there's no need to have a calibration scheme to overcome this problem. Furthermore, the *dynamic element matching* (DEM) technique [27] is extensively used in DACs to improve their SFDR. The DEM method tries to equalize the usage probabilities of the components in the DAC so as to spread the power of the harmonic distortion into a white noise. The idea is similar to the concept of spread spectrum in communication systems. As a result, the errors of the sub-DAC can be alleviated substantially.

According to (2.7), if the residue amplifier has a gain error or nonlinearity, the linearity of the pipelined ADC would be greatly affected. Impairments of components and the variations in ambient operating conditions such as temperature and the supply voltage may make the gain deviate far from the design target. Consequently, the linearity of a pipelined stage strongly depends on that of the residue amplifier. The transfer function of a practical residue amplifier usually can be expressed as a polynomial of the input v_x which is shown

$$v_{out} = f(v_x) = \sum_{w=1}^{n} a_w v_x^w, \qquad (2.8)$$

where a_w is the coefficient of the wth-order term and v_{out} is the output of the residue amplifier, respectively.
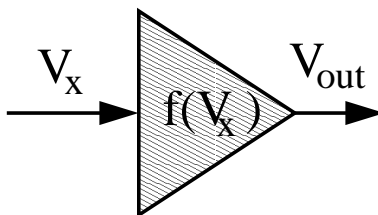
Figure 2.8: The model of the residue amplifier in a pipeline stage.

Therefore, if we want to have a high performance pipelined ADC, the errors in the

residue amplifier need to be corrected. The last decade have seen growing importance placed on research in calibrating the linear and nonlinear gain errors of the residue amplifier. The following chapter will give a review about the research which focus on background calibration scheme that corrects the linear and nonlinear gain errors of the residue amplifier in digital domain.
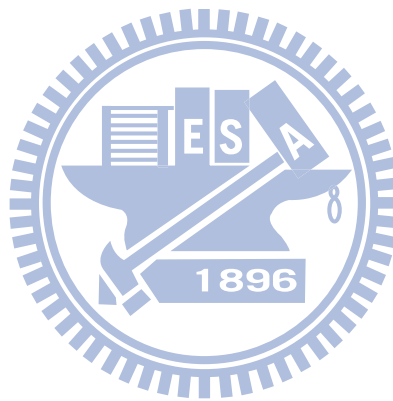
Chapter 3

PRIOR ARTS ON DIGITAL BACKGROUND CALIBRATION SCHEMES

In order to implement high resolution and low power consumption pipelined ADCs, many digital background calibration schemes have been proposed. The main idea of these calibration schemes is to translate the analog precision problems into the digital ones to relax the challenge of designing precision analog components and to save the power.

The digital background calibration schemes are popular as they enable continuous ADC operation [2]–[5],[4],[28]–[37]. Among various approaches of digital background calibration schemes, the correlation-based error estimation methods [2, 5, 4],[28]–[31] attract much attention because they provide true background calibration.

Correlation-based error estimation methods inject at least a pseudo-random (dither) signal as a part of the pipelined ADC's signal. The injected signal usually has the properties of a zero mean and being uncorrelated with the ADC's input signal. At the output side, a digital post-processor extracts the response of the injected signal from the output of the ADC based on a correlation mechanism. The response provides the characterizations of the analog components of our interests.

As has been discussed in the previous chapter, the key component in a pipeline stage

is the residue amplifier. Since the implementation of the residue amplifier is usually fully differential, even-order nonlinear terms of the residue amplifier are less significant. Therefore, the dominant nonlinearity source comes from the odd-order nonlinear terms of the residue amplifier's transfer function.

This chapter gives a review of prior arts on digital background calibration schemes that focus on the calibration of the gain error and the 3rd-order nonlinear term of the residue amplifier.

3.1   Statistic-Based Distance Estimation Method
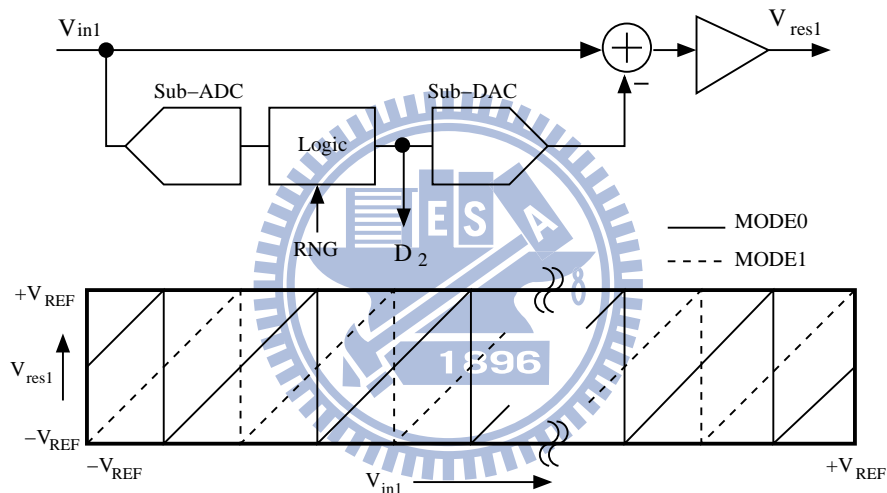
Figure 3.1: Pipeline stage with two residue transfer characteristics.

The first research about cancelling the nonlinear gain error of a residue amplifier in a pipelined ADC is published in 2003 [3]. The pipeline stage in the article is shown in Fig. 3.1. A binary random number generator (RNG) logic block is added between the sub-ADC and sub-DAC to switch the operation mode of the pipeline stage. That is, the output randomly alternates between the solid line and the dash line shown in Fig. 3.1. Redundant comparators are added to provide different comparator decision levels.

To estimate the errors, the calibration processor estimates the residue differences h_1 and h_2 shown in Fig. 3.2 for the two specific input levels near the center and the edge of the segment, respectively. If the residue amplifier is linear, h_1 equals h_2. On the
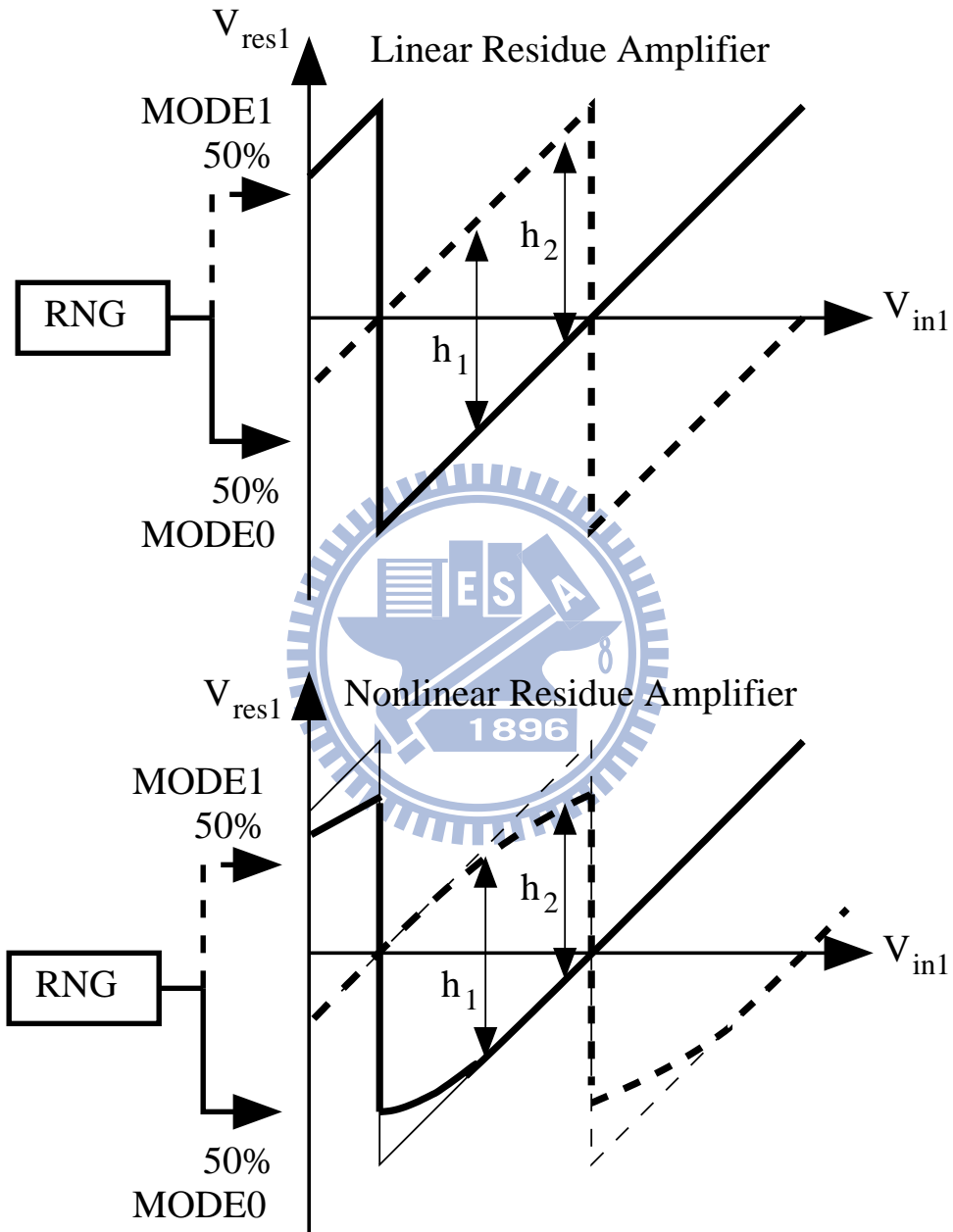
Figure 3.2: Input-output characteristic for linear and nonlinear residue amplifier.

contrary, the transfer curve of a nonlinear residue amplifier may have some deviation from the ideal one resulting in $h_1 \neq h_2$. Hence, one can reveal the nonlinear coefficient of the residue amplifier by estimating the distance between h_1 and h_2. Notice that the distance between h_1 and h_2 is the most significant at the edge of the segment, it implies taking one of the specific input level close to the edge of the segment is a good choice. After cancelling the nonlinear term, both h_1 and h_2 on the new transfer curve are precisely $1/2$ of the transition height which directly relates to the required information for linear gain error correction.

The reference proposed a statistic based estimation method to estimate the distance between h_1 and h_2. The statistical method counts the code hits to represent the heights of h_1 and h_2. Therefore, the calibration scheme cannot operate properly if the input signal is not "busy" enough around the codes of interest. The reason is that the input signal would not hits enough times around the specific codes and thus the cumulative histogram becomes flat. Moreover, this scheme needs a huge counter array to count the number of samples seen in the backend less than or equal to the specific codes.

3.2   Correlation-Based Estimation Method

A correlation-based estimation method for estimating the nonlinearity of the residue amplifier in a pipelined ADC was presented in 2005 [28]. The proposed technique allows faster convergence and has less dependence on input signal's statistical properties than the technique proposed in [3].

In [28], a calibration signal is added at the location between the sub-ADC and the sub-DAC to form D_1 (the output of the sub-DAC) in Fig. 3.3, and D_1 can be expressed as

$$D_1 = \bar{D}_1 + R\Delta D_1, \tag{3.1}$$

where $\bar{D}_1 = (1/2)(D_{1+} + D_{1-})$, D_{1+} and D_{1-} are the levels of sub-DAC, $\Delta D_1 = (1/2)|D_{1+} - D_{1-}|$, and $R \in \{+1, -1\}$ is a random sequence uncorrelated to the ADC's input signal.
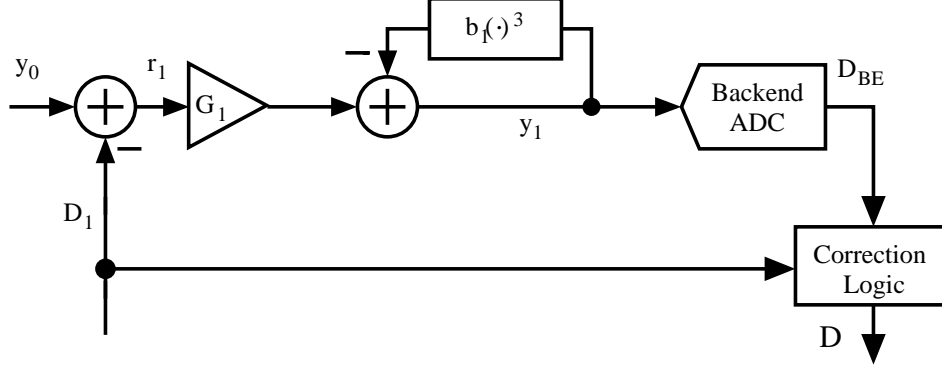
Figure 3.3: Equivalent model of a pipeline stage including a nonlinear amplifier.

Considering Fig. 3.3,

$$y_0 = D_1 + \frac{1}{G_1}(y_1 + b_1 y_1^3), \tag{3.2}$$

where G_1 is the linear gain of the residue amplifier and b_1 determines the magnitude of the 3rd-order nonlinear gain error relative to the linear gain error. If the amplifier is only weakly nonlinear $y_1 \approx D_{BE}$, (3.2) can be modified to be

$$
\begin{aligned}
D &\approx D_1 + \hat{m}_1(D_{BE} + \hat{b}_1 D_{BE}^3) \\
\Rightarrow D &\approx y_0(1 + e_m) - D_1 e_m + \hat{m}_1 G_1^3(\hat{b}_1 - b_1)(y_0 - D_1)^3, \tag{3.3}
\end{aligned}
$$

where $\hat{b}_1$ is an estimate of b_1 , D is the ADC's primary digital output (the digitized y_0), and $e_m = \frac{\hat{m}_1 - m_1}{m_1}$ is the relative error in estimating $\hat{m}_1$ of $m_1 = 1/G_1$.

Taking $z = D - \bar{D}_1$, an estimation of the nonlinearity of the residue amplifier can be shown as

$$
\begin{aligned}
B &= E[(Rz)z^2] - 3E[Rz]E[z^3] \tag{3.4} \\
\Rightarrow B &\approx -9e_b \Delta D_1 K_{Y^2 Y^2}, \tag{3.5}
\end{aligned}
$$

where $e_b = G_1^3 \hat{m}_1(\hat{b}_1 - b_1)$, $Y = y_0 - \bar{D}_1$, and $K_{Y^2 Y^2}$ is the variance of Y^2.

To find $\hat{b}_1$, an approach is using the least-mean-square (LMS) algorithm [38]. (Chapter 4 will introduce the LMS algorithm in detail.) The following equation show how to

implement the LMS algorithm to find the optimum $\hat{b}_1$.

$$\hat{b}_1[k + 1] = \hat{b}_1[k] + \mu_b B[k] \tag{3.6}$$

Once the coefficient b_1 is obtained, $b_1(D_{BE})^3$ can be compensated in the digital domain to correct the nonlinearity of the residue amplifier.

After cancelling the nonlinearity of the residue amplifier, (3.2) becomes

$$y_0 = D_1 + \frac{1}{G_1} y_1. \tag{3.7}$$

Now, taking the correlation of R and z

$$E[Rz] = -\Delta D_1 e_m \tag{3.8}$$

leads to a result proportional to $-(\hat{m}_1 - m_1)$. Therefore, it can be regarded as a noisy estimate for the error in the coefficient $\hat{m}_1$ and used to adjust $\hat{m}_1$ to be closer to its target m_1. The iteration equation for estimating $\hat{m}_1$ using LMS is

$$\hat{m}_1[k + 1] = \hat{m}_1[k] + \mu_m R[k] z[k]. \tag{3.9}$$

The μ_b and μ_m in (3.6) and (3.9) are step sizes used to determine the tracking rates and the steady-state errors of the LMS loops.

However, the nonlinearity estimation functions only when the amplifier is weakly nonlinear. If not, the estimation of nonlinear coefficient fails if a static input is applied since $K_{Y^2Y^2} = 0$ according to (3.5).

3.3 Harmonic Distortion Correction Method

Reference [5] proposed another correlation-based technique called harmonic distortion correction (HDC) that solves the main issues of [3] and [28], but still has some limitations.

Figure 3.4 shows the pipeline stage under calibration in [5]. A set of w uncorrelated, two-level, pseudo-random, digital calibration values of amplitude $\pm\triangle$ which is zero mean and independent of the pipelined ADC's input signal is injected before the sub-DAC to calibrate the wth-order nonlinear term of the residue amplifier. All the notations in Fig. 3.4 are shown as the following equations from (3.10) to (3.13).
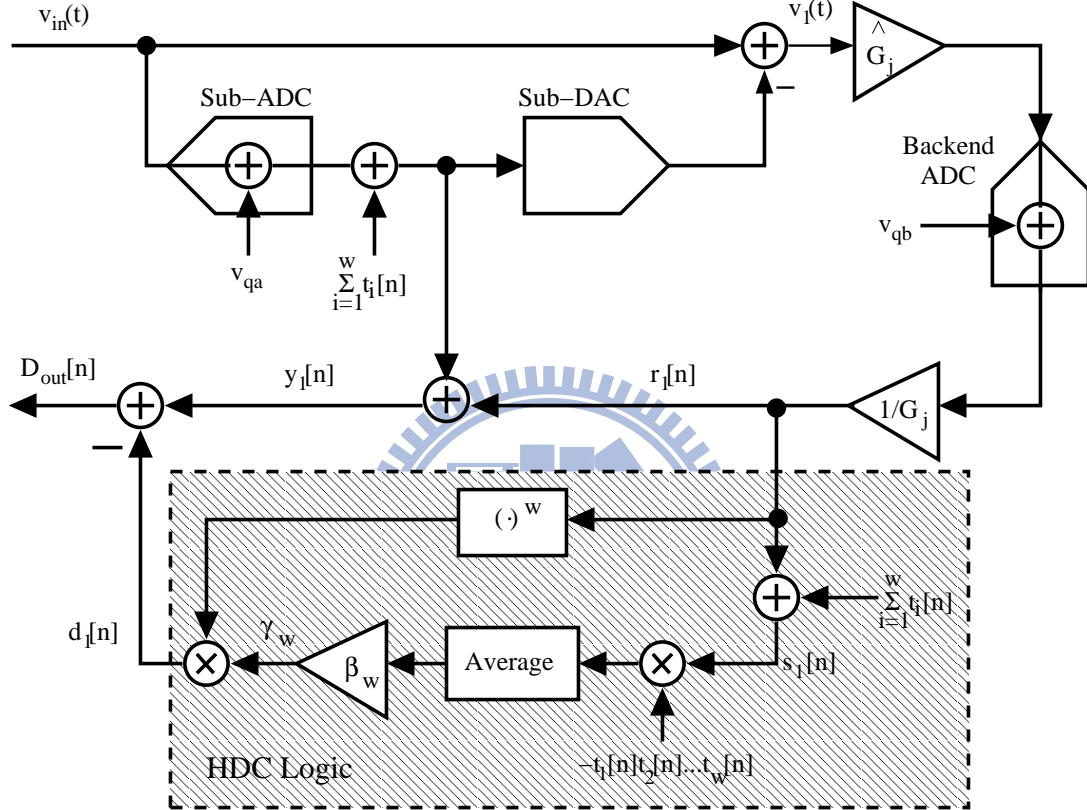
Figure 3.4: HDC technique.

$$v_1(nT_s) = -v_{qa}[n] - \sum_{i=1}^{w} t_i[n], \qquad (3.10)$$

where T_s is the sampling period, $v_{qa}[n]$ is the quantization error of sub-ADC, and $\sum_{i=1}^{w} t_i[n]$ is the calibration sequence.

$$r_1[n] = v_1(nT_s) + a_w v_1^w(nT_s) + \frac{1}{G_j} v_{qb}[n], \qquad (3.11)$$

where $a_w v_1^w(nT_s)$ is the wth-order nonlinear term relative to the linear gain G_j of the residue amplifier as Fig. 3.5, and $v_{qb}[n]$ is the quantization error of the backend ADC.
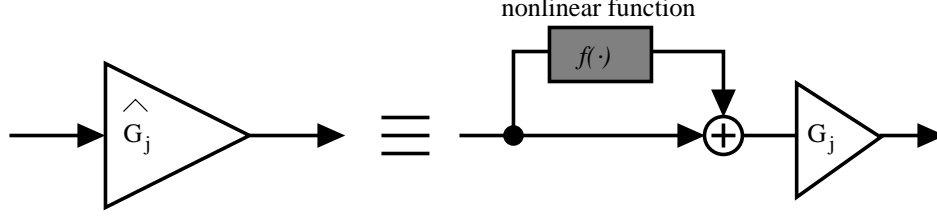
Figure 3.5: The model of the nonlinear residue amplifier.

$y_1[n]$ in Fig. 3.4 is

$$y_1[n] = v_{in}(nT_s) + a_w v_1^w(nT_s) + \frac{1}{G_j} v_{qb}[n]. \tag{3.12}$$

Combine (3.10) and (3.11), $s_1[n]$ can be written as

$$
\begin{aligned}
s_1[n] &= r_1[n] + \sum_{i=1}^{w} t_i[n] \\
&= -v_{qa}[n] + a_w v_1^w(nT_s) + \frac{1}{G_j} v_{qb}[n].
\end{aligned}
\tag{3.13}
$$

The purpose of HDC logic is to estimate $a_w v_1^w(nT_s)$ in (3.13). By expanding (3.13), it's easy to find that there's a term $(w!)t_1[n]t_2[n]...t_w[n]$. Taking the correlations of $s_1[n]$ and $t_1[n]t_2[n]...t_w[n]$, results in a value of $(w!)\Delta^{2w}a_w$. The HDC logic multiplies the output of the average by $\beta_w = \frac{1}{\Delta^{2w}w!}$ to obtain γ_w which is an estimate of a_w.

Nevertheless, if any of the a_z for $z > w$ is not negligible, the HDC cannot accurately estimate a_w due to the expansion of the higher-order nonlinear terms of the residue amplifier will have several cross terms that are correlated to the estimation of the lower-order coefficients. Therefore, a compensated matrix needs to be added to cancel these unwanted terms. The dimension of this matrix depends on the non-negligible terms of a_z where $z > w$. If there're many higher order nonlinear terms cannot be neglected, the matrix will go larger. For instance, if the residue amplifier contains the linear gain error, the 3rd-order nonlinear term and the 5th-order nonlinear term, a 3×3 compensation matrix is needed.

In Fig. 3.4, it's obvious that $r_1(nT_s)$ is used to be an approximation of $v_1[n]$. Actually, the expansion of $r_1^w[n]$ contains several significant terms due to the nonlinearity of

the residue amplifier. These errors may limit the calibration effectiveness and the reso-
lution of the pipelined ADC. This issue will be severer if more non-negligible nonlinear
terms of the residue amplifier exist. As a result, the range of successful calibration is
mightily limited.

It follows from Fig. 3.4, the calibration sequences are summed up and applied to the
sub-DAC. Therefore, to calibrate higher order nonlinear terms of the residue amplifier,
more calibration signals are needed. It implies that a larger headroom is needed for
the calibration signals to be added if more nonlinear terms of the residue amplifier are
not negligible. Moreover, the number of samples is 2^{32} for each HDC. That is, at a
sampling rate of 100 MHz, the estimation of each coefficient a_i needs approximately 43
seconds to converge. If the residue amplifier contains linear gain error and 3rd-order
nonlinear gain error, it takes 1.5 minute to converge. The convergence time may be too
long to track the ambient variation.

3.4   Multi-Correlation Estimation (MCE) Method

A novel estimation method called multi-correlation estimation (MCE) is proposed in
2006 [2]. This method is free of all the main issues mentioned in the previous sections.

Fig. 3.6 shows a pipeline stage under calibration in [2]. A pseudo-random sequence
is applied to the sub-DAC as in most correlation based techniques. Here, the residue
amplifier is also modeled to have linear and 3rd-order nonlinear gain errors. The digi-
tized residuum D_{bi} can be written as the following equation when the random sequence
is applied.

$$
\begin{aligned}
D_{bi} &= a_1(v_x) + a_3(v_x)^3 + v_{qb} \\
&= a_1(-v_{qa} - R_i v_{di}) + a_3(-v_{qa} - R_i v_{di})^3 + v_{qb}, i \in \{1, 2\}, \quad (3.14)
\end{aligned}
$$

where v_{qa} is the quantization error of the sub-ADC, v_{qb} is the quantization error of
the backend-ADC, and $R_i \in \{-1, 1\}$ is a pseudo-random number sequence which has
a uniform distribution and is uncorrelated to the ADC's input signal. Let v_{di} be the
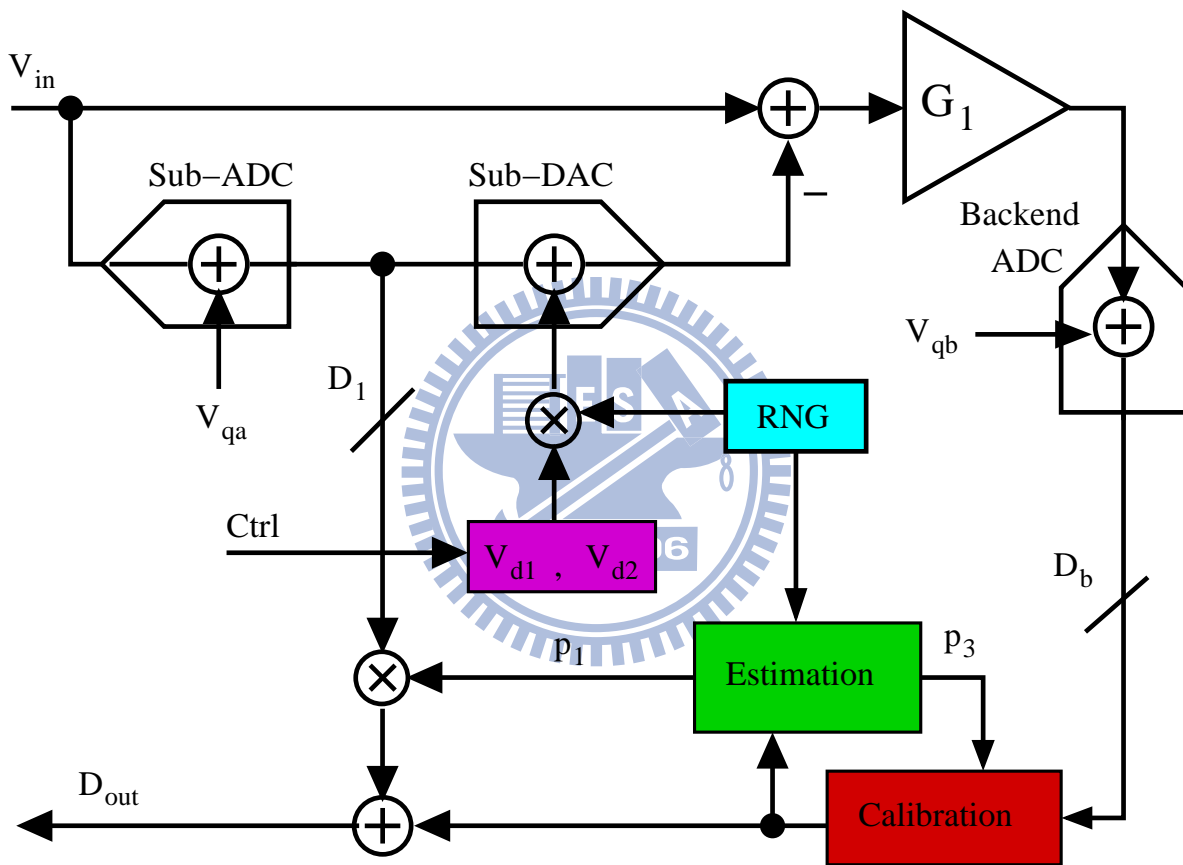
Figure 3.6: MCE technique.

amplitudes of the two calibration signals, where

$$R_1 v_{d1} \in \{+v_{d1}, -v_{d1}\},$$
$$R_2 v_{d2} \in \{+v_{d2}, -v_{d2}\}.$$

Taking the correlations of D_{bi} and R_i, we have

$$E[R_i D_{bi}] = E[a_1(-R_i v_{qa} - v_{di}) + a_3(-R_i v_{qa}^3 - 3v_{qa}^2 v_{di} - 3R_i v_{qa} v_{di}^2 - v_{di}^3) + R_i v_{qb}]. \quad (3.15)$$

Because $R_i, i \in \{1, 2\}$ are uncorrelated with the input signal, the correlations of R_i and the quantization errors v_{qa}, v_{qb} are all zero. Equation (3.15) can be further reduced to

$$E[R_i D_{bi}] = a_1(-v_{di}) + a_3(-3v_{qa}^2 v_{di} - v_{di}^3) \quad (3.16)$$

A technique called multi-correlation estimation (MCE) was proposed to eliminate the term $a_1(-v_{di})$ in Eq. (3.16), results in an output proportional to a_3. If making $v_{d1} = v_{d2}/2 = V_{LSB}/4$ (of the local sub-ADC),

$$\varepsilon_3 \equiv E[R_1 D_{b1}] - 2E[R_2 D_{b2}] = -\frac{3}{4} a_3 v_{d1}^3. \quad (3.17)$$

Let's define two arguments p_1 and p_3 which are the correction parameters to compensate for the linear and nonlinear gain errors respectively. Their optimum values can be expressed as

$$p_{3,opt} \equiv \frac{a_3}{a_1^3}, \quad (3.18)$$
$$p_{1,opt} \equiv a_1. \quad (3.19)$$

A calibration mechanism is applied to calibrate the nonlinear gain error of the residue amplifier [3]

$$e(D_b) = D_b - 2\sqrt{\frac{-1}{3p_3}} \cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_b}{2\sqrt{\frac{-1}{27p_3}}}\right)\right]. \quad (3.20)$$

A detailed derivation of equation (3.20) can be found in Appendix A.

If the correction function (3.20) is applied, equation (3.17) can be rewritten as

$$\varepsilon_3 = -\frac{3}{4}a_1^3 v_{d1}^3 (p_{3,opt} - p_3). \tag{3.21}$$

According to this result, an iterative functions, e.g., LMS algorithm, can be applied to minimize the deviation so as to obtain the ideal value of p_3.

When the nonlinear gain error has been removed, the resulting correlation is proportional to a_1 since $a_3 = 0$ in (3.16). Therefore, (3.16) becomes

$$\varepsilon_1 \equiv E[R_1 D_{b1}] = a_1(-v_{d1}), \tag{3.22}$$

it represents the linear gain error information. In order to be merged in the LMS loop, ε_1 is modified as

$$\varepsilon_1' \equiv \frac{\varepsilon_1}{p_1} + v_{d1} = \frac{-(p_{1,opt} - p_1)}{p_1} v_{d1}, \tag{3.23}$$

p_1 will approaches to $p_{1,opt}$ when $\varepsilon_1' = 0$ by using LMS algorithm.

The convergence of p_3 and p_1 are implemented by using the LMS algorithm. The following two equations show the implementation.

$$\begin{aligned} p_3(k+1) &= p_3(k) - \mu_3 \varepsilon_3 \\ p_1(k+1) &= p_1(k) - \mu_1 \varepsilon_1', \end{aligned} \tag{3.24}$$

where μ_3 and μ_1 are the step sizes used to control the convergence speeds and the steady-state errors of the LMS loops.

The MCE have many important advantages over the prior works. First, it works for any pipelined ADC input signal level while [3] requires a "busy" enough input. Second, it doesn't have restrictions with respect to dc input signal but [28] does. Third, its calibration signal is added alternatively. Therefore, the reserved headroom for the calibrations signals to be added is smaller than [5] and the number of calibration signals is less than [5]. Furthermore, the number of samples for each correlation is 2^{17}.

At a sampling rate 100 MHz, it only takes 0.3 seconds to convergent the correction parameters. It's 256 times faster than [5]. Fourth, it provides the widest calibration range since no approximation assumption is made during the derivation of (3.20). The MCE can calibrate the extreme nonlinear amplifier as long as the inverse function of the nonlinear transfer function exist. The implementation of this MCE method and a detailed analysis of the LMS loops used in this MCE method will be given in chapter 5.

We see that the LMS algorithm is popular in many estimation methods [2, 3, 28] which is usually used to update and track the correction parameters. In the following chapter, we will give a brief introduction to the adaptive signal processing and the LMS algorithm.
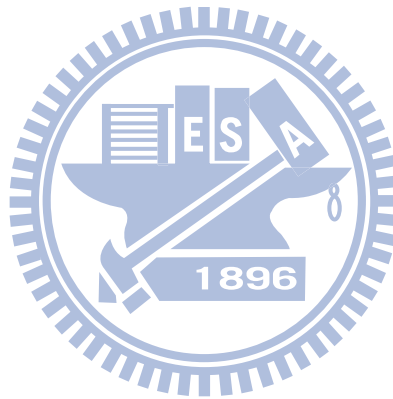
Chapter 4

ADAPTIVE SIGNAL PROCESSING

4.1 Adaptive Systems

An adaptive system is alterable or adjustable in a way such that its behavior or performance improves through contact with its environment [38]. Adaptive systems can be classified into the open-loop adaptation and the closed-loop adaptation.
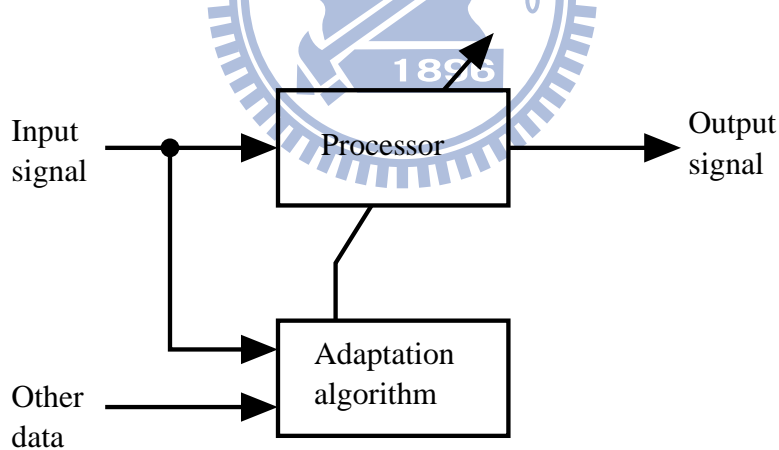
Figure 4.1: The open-loop adaption.

The open-loop adaptive process, shown in Fig. 4.1, involves making measurements of the input or environmental characteristics. Then, it applies the measured information to a formula or to a computational algorithm and sets the adjustments of the adaptive system according to the results.
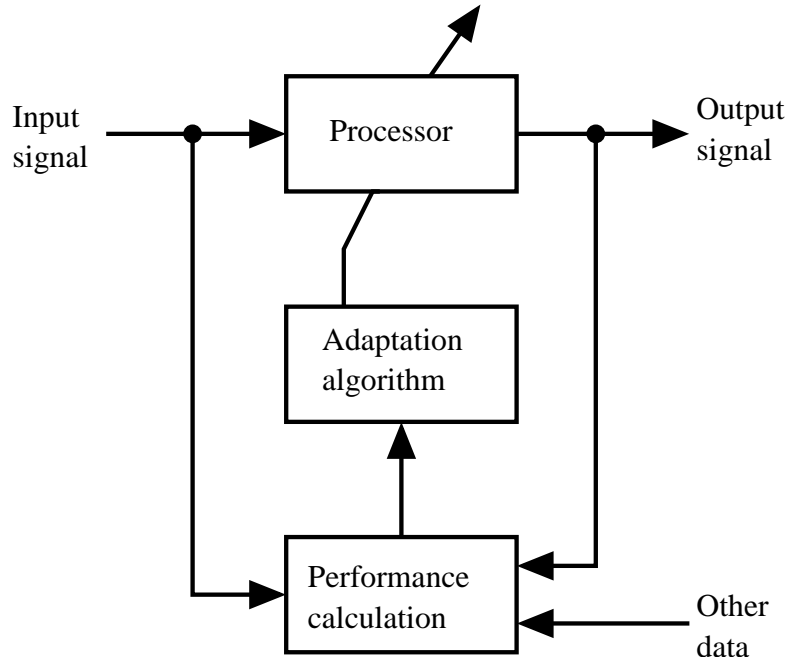
Figure 4.2: The closed-loop adaption.

The closed-loop adaptation, shown in Fig. 4.2, involves automatic experimentation with the adjustments and knowledge of their outcomes in order to optimize a measured system performance.

The closed-loop adaptation has the advantages of being workable when no analytic synthesis procedure either exists or is known, when systems are nonlinear or time variable, when signals are non-stationary, and so on [38]. Due to these reasons, the closed-loop adaption is widely used for estimating the nonlinear coefficients of the residue amplifier for a pipelined ADC [2, 3, 28].

The following sections in this chapter focus on the closed-loop processes utilizing performance feedback.

4.2 Adaptive Linear Combiner

Figure 4.3 depicts the model of the adaptive system. The aim is to estimate the parameters of the adaptive linear combiner, $P(z)$, of a target $T(z)$ [39]. A certain input $x(n)$ is applied to both the target and the adaptive linear combiner. The error signal $e(n)$ is obtained by subtracting the output of the adaptive linear combiner $y(n)$ from
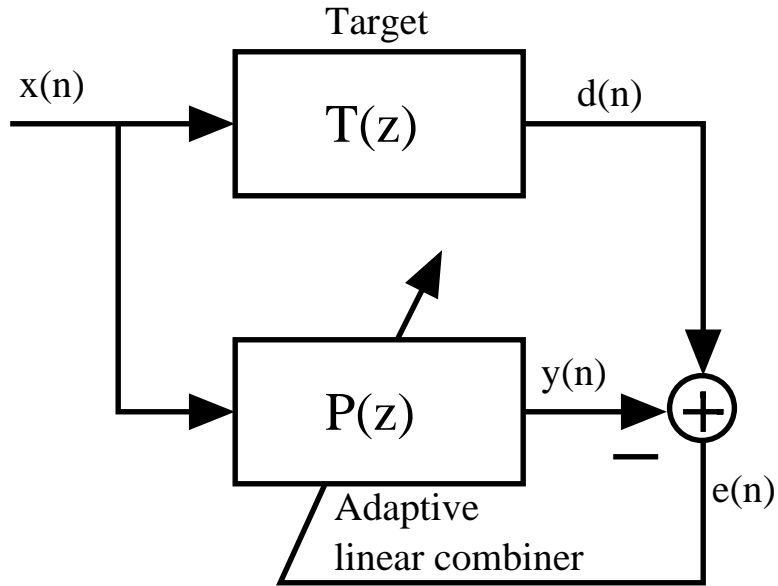
Figure 4.3: Adaptive system modeling.

the target's output (desired response) $d(n)$. Then, the error signal is fed back to $P(z)$ in order to update the parameters of the adaptive linear combiner so as to minimize the error signal. When the parameters are adjusted to be the same as the targets, the error signal will be zero.
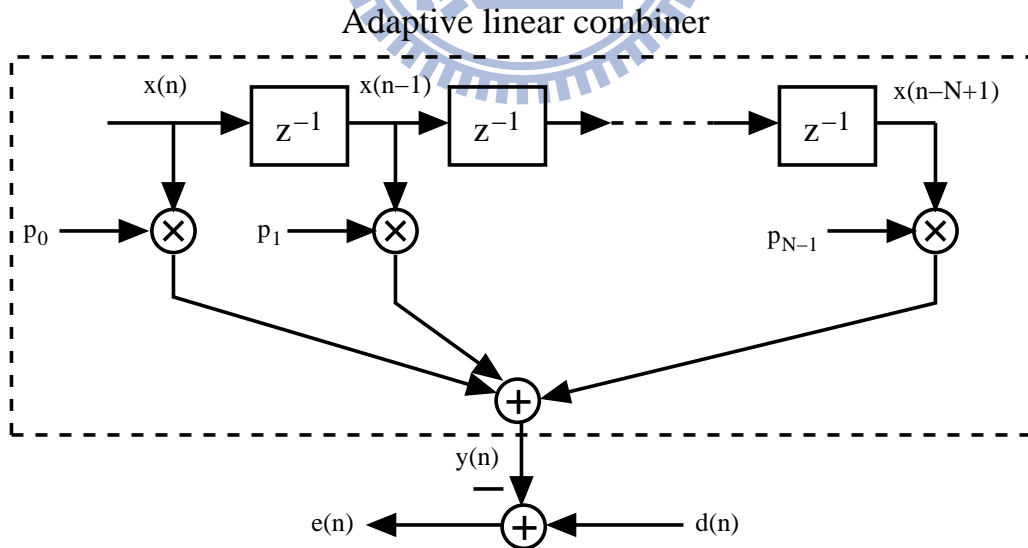
Figure 4.4: Linear combiner with desired response and error signal.

The block of the adaptive linear combiner in Fig. 4.3 is spread and shown in Fig.

4.4. The input vector is given by

$$\mathbf{x}(n) = [x(n)\ x(n-1)\ \cdots\ x(n-N+1)]^T. \tag{4.1}$$

The adaptive liner combiner with the parameters, $p_0, p_1, \ldots, p_{N-1}$, are

$$\mathbf{p} = [p_0\ p_1\ \cdots\ p_{N-1}]^T. \tag{4.2}$$

Therefore, the output of the adaptive system $y(n)$ can be expressed as

$$y(n) = \sum_{i=0}^{N-1} p_i x(n-i) = \mathbf{p}^T \mathbf{x}(n) = \mathbf{x}^T(n)\mathbf{p}. \tag{4.3}$$

According (4.1) to (4.3), the error signal is

$$e(n) = d(n) - y(n) = d(n) - \mathbf{p}^T \mathbf{x}(n) = d(n) - \mathbf{x}^T(n)\mathbf{p}. \tag{4.4}$$

4.3 The Performance Function

We now proceed to a discussion of the performance function based on the error signal just described. Let's square (4.4) to obtain the instantaneous squared error

$$e^2(n) = d^2(n) + \mathbf{p}^T \mathbf{x}(n)\mathbf{x}^T(n)\mathbf{p} - 2d(n)\mathbf{x}^T(n)\mathbf{p}. \tag{4.5}$$

Assume that $e(n), d(n), \mathbf{x}(n)$ are statistically stationary and take the mean-square-error (MSE) over n:

$$E[e^2(n)] = E[d^2(n)] + \mathbf{p}^T E[\mathbf{x}(n)\mathbf{x}^T(n)]\mathbf{p} - 2E[d(n)\mathbf{x}^T(n)]\mathbf{p}. \tag{4.6}$$

Define the "input correlation matrix" $\mathbf{C}$ by

$$
\begin{aligned}
\mathbf{C} &\equiv E[\mathbf{x}(n)\mathbf{x}^T(n)] \\
&= E \begin{bmatrix}
x_{n,n} & x_{n,n-1} & \cdots & x_{n,n-N+1} \\
x_{n-1,n} & x_{n-1,n-1} & \cdots & x_{n-1,n-N+1} \\
\vdots & \vdots & \ddots & \vdots \\
x_{n-N+1,n} & x_{n-N+1,n-1} & \cdots & x_{n-N+1,n-N+1}
\end{bmatrix},
\end{aligned}
\qquad (4.7)
$$

where $x_{n,n}$ denotes $x(n)x(n)$ and so forth. The diagonal entries are the mean squares of the input components, and the cross terms are the cross correlations among the input components. Let $\mathbf{U}$ be defined as the column vector

$$
\mathbf{U} \equiv E[d(n)\mathbf{x}(n)] = E[d(n)x(n) \quad d(n)x(n-1) \quad \cdots \quad d(n)x(n-N+1)]^T. \qquad (4.8)
$$

Now define the MSE in (4.6) to be ξ and expressed it in terms of (4.7) and (4.8) as

$$
MSE \triangleq \xi = E[d^2(n)] + \mathbf{p}^T\mathbf{C}\mathbf{p} - 2\mathbf{U}^T\mathbf{p}. \qquad (4.9)
$$

It's clear from (4.9) that ξ is a quadratic function of $\mathbf{p}$ with a single global minimum due to $\mathbf{C}$ is a *positive defined matrix* $(\mathbf{p}^T\mathbf{C}\mathbf{p} > 0)$.

An example of a typical two-dimensional MSE function is illustrated in Fig. 4.5. The horizontal axes are the values of the two parameters and the vertical axis is the MSE. The quadratic performance surface is a paraboloid. This surface must be concave upward (positive defined) because the result of the MSE is always positive. The optimal parameter vector occurs at the bottom of the "bowl" because the MSE is minimum. Now, taking the gradient of the MSE, we have

$$
\nabla \xi = \nabla(E[d^2(n)] + \mathbf{p}^T\mathbf{C}\mathbf{p} - 2\mathbf{U}^T\mathbf{p}) = 2(\mathbf{C}\mathbf{p} - \mathbf{U}). \qquad (4.10)
$$

Equation (4.10) will be zero when

$$
\mathbf{C}\mathbf{p} = \mathbf{U}. \qquad (4.11)
$$
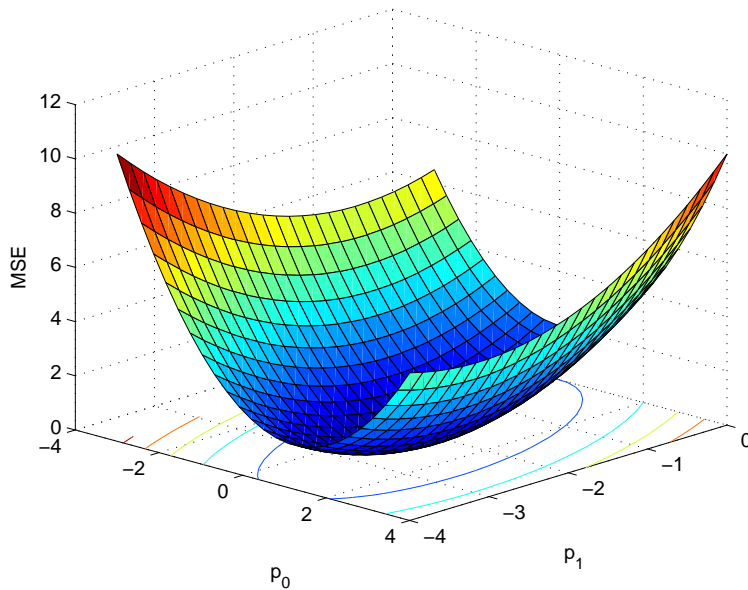
Figure 4.5: A two-dimensional quadratic performance surface.

Equation (4.11) is known as *the Wiener-Hopf equation.* Therefore, the optimal parameter vector can be expressed as (4.12) if $\mathbf{C}$ is a nonsingular matrix.

$$\mathbf{p}_{opt} = \mathbf{C}^{-1}\mathbf{U}, \tag{4.12}$$

where $\mathbf{p}_{opt}$ is the optimal parameter vector.

4.4   Searching the Performance Surface

In order to find the optimal parameter vector, directly solving the Wiener-Hopf equation is an straightforward approach but the required computation may be very complicated. Instead, an iterative search method in which starting with an initial guess for $\mathbf{p}(0)$, a recursive search method that may require many iterations to converge to $\mathbf{p}_{opt}$ is commonly used because the computation is much simpler. A search method called steepest-descent consists of the following four steps [39]:

1. Start with an initial guess of the parameters.

2. Find the gradient of the function with respect to these parameters at the present

point.

3. Update the parameters by taking a step in the opposite direction of the gradient vector obtained in step 2.

4. Repeat step 2 and 3 until no further significant change is observed in the parameters.

The steepest descent method is expressed by (4.13) in which μ represents the step size and $\mathbf{p}(k)$ denotes the parameter vector at the k-th iteration.

$$\mathbf{p}(k+1) = \mathbf{p}(k) - \mu \nabla \xi \tag{4.13}$$

An example of gradient search of univariable performance surface is illustrated in Fig.
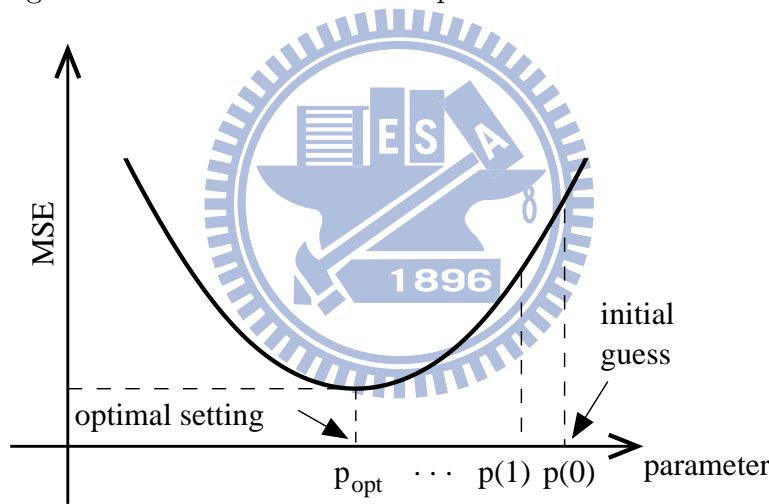
Figure 4.6: Gradient search of univariable performance surface.

4.6. Actually, Fig. 4.6 can be regarded as one of the parabola in Fig. 4.5 that go through the bottom of the bowl. This is a helpful example to understand the steepest descent algorithm described by (4.13). Let's start with the initial guess of the point $p(0)$ on the figure, the gradient at this point is a positive value toward the direction of the optimal parameter. As a result, the next update of the parameter will be more close to the optimum. Repeat the procedure, finally the updated parameter reaches the bottom of the parabola and the gradient becomes zero. It means the parameter can be set to the optimal value after several iterations.

From (4.10) and (4.12), equation (4.13) can be further expressed as

$$
\begin{aligned}
\mathbf{p}(k+1) &= \mathbf{p}(k) - 2\mu\mathbf{C}\mathbf{p}(k) + 2\mu\mathbf{C}\mathbf{p}_{opt} \\
\Rightarrow \mathbf{p}(k+1) - \mathbf{p}_{opt} &= \mathbf{p}(k) - 2\mu\mathbf{C}\mathbf{p}(k) + 2\mu\mathbf{C}\mathbf{p}_{opt} - \mathbf{p}_{opt} \\
\Rightarrow \mathbf{p}(k+1) - \mathbf{p}_{opt} &= (\mathbf{I} - 2\mu\mathbf{C})(\mathbf{p}(k) - \mathbf{p}_{opt}),
\end{aligned}
\tag{4.14}
$$

where $\mathbf{I}$ is an identity matrix (unit matrix). Now, let's define the parameter-error vector by $\mathbf{v}(k) \equiv \mathbf{p}(k) - \mathbf{p}_{opt}$. Equation (4.14) can be rewritten as

$$
\mathbf{v}(k+1) = (\mathbf{I} - 2\mu\mathbf{C})\mathbf{v}(k).
\tag{4.15}
$$

Since $\mathbf{C}$ is a symmetric matrix, it is orthogonally diagonalizable

$$
\mathbf{C} = \mathbf{Q}\mathbf{\Lambda}\mathbf{Q}^{T},
\tag{4.16}
$$

where $\mathbf{\Lambda}$ is a diagonal matrix consisting of the eigenvalues $\lambda_0, \lambda_1, \ldots, \lambda_{N-1}$ of $\mathbf{C}$, and the columns of $\mathbf{Q}$ contain the corresponding orthonormal eigenvectors. Combing (4.15) and (4.16) gives

$$
\mathbf{v}(k+1) = (\mathbf{Q}\mathbf{Q}^{T} - 2\mu\mathbf{Q}\mathbf{\Lambda}\mathbf{Q}^{T})\mathbf{v}(k),
\tag{4.17}
$$

where $\mathbf{I} = \mathbf{Q}\mathbf{Q}^{T}$. Define $\mathbf{v}'(k) \equiv \mathbf{Q}^{T}\mathbf{v}(k)$ which transforms $\mathbf{v}(k)$ to $\mathbf{v}'(k)$. Multiplying $\mathbf{Q}^{T}$ on both sides of (4.17), we have

$$
\mathbf{v}'(k) = (\mathbf{I} - 2\mu\mathbf{\Lambda})\mathbf{v}'(k).
\tag{4.18}
$$

4.4.1 Stability and Convergence

Equation (4.18) can be separated into scalar recursively,

$$
v_i'(k+1) = (1 - 2\mu\lambda_i)v_i'(k), \text{ for } i = 0, 1, \cdots, N-1.
\tag{4.19}
$$

Starting with a set of initial values $v'_0(0), v'_1(0), \cdots, v'_{N-1}(0)$ and iterating (4.19) k times, we get

$$v'_i(k) = (1 - 2\mu\lambda_i)^k v'_i(0), \text{ for } i = 0, 1, \cdots, N - 1. \tag{4.20}$$

Equation (4.20) implies that $\mathbf{v}'$ converges to zero if and only if

$$|1 - 2\mu\lambda_i| < 1, \text{ for } i = 0, 1, \cdots, N - 1. \tag{4.21}$$

Furthermore, (4.21) can be expanded as

$$0 < \mu < \frac{1}{\lambda_i}, \text{ for } i = 0, 1, \cdots, N - 1, \tag{4.22}$$

which ensures the steepest descent algorithm to be stable. In fact, the convergence (stability) of the steepest descent algorithm is guaranteed only when

$$0 < \mu < \frac{1}{\lambda_{\max}}; \tag{4.23}$$

where $\lambda_{\max}$ is the maximal eigenvalue.

A larger μ in the range of (4.23) leads to a faster convergence speed but with a larger dither. In general, a wider spread of the eigenvalues, i.e. large $\lambda_{\max}/\lambda_{\min}$, where $\lambda_{\min}$ is the minimal eigenvalue, results in a slower convergence of the steepest descent algorithm. The effects of the different choices of μ are summarized in Table 4.1 and Fig. 4.7 . The five cases shown in Table 4.1 depict the distinct ranges of μ, corresponding to the stable, overdamped, critically damped, underdamped, and unstable cases [38, 39].

Table 4.1: Effect of μ of the gradient search process.

Stable (convergent)	$0 < \mu < \frac{1}{\lambda_i}$
Overdamped	$0 < \mu < \frac{1}{2\lambda_i}$
Critically damped	$\mu = \frac{1}{2\lambda_i}$
Underdamped	$\frac{1}{2\lambda_i} < \mu < \frac{1}{\lambda_i}$
Unstable (not convergent)	$\mu \geq \frac{1}{\lambda_i}$ or $\mu \leq 0$
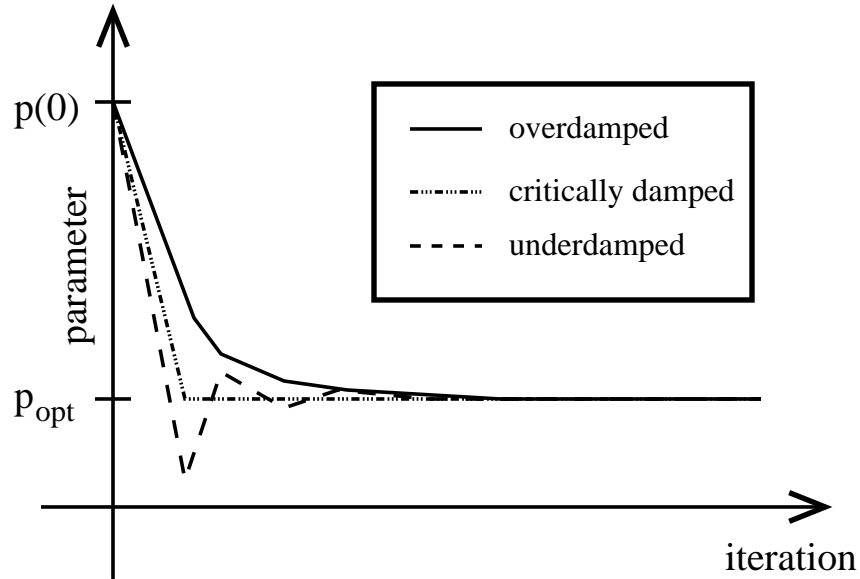
Figure 4.7: Parameter adjustment for different values of μ.

4.4.2 Time Constant

Recall (4.20), the time constant of the MSE convergence is defined as " *the time (iterations) at which the initial condition of vector* $\mathbf{v}$ *has decayed to a value of* $1/e$ *times initial value.*"

$$
\begin{aligned}
v(0)e^{-1} &= v(0)(1 - 2\mu\lambda)^{\tau} \\
\Rightarrow -1 &= \tau ln(1 - 2\mu\lambda).
\end{aligned} \tag{4.24}
$$

Since $2\mu\lambda \ll 1$, $ln(1 - 2\mu\lambda) \cong -2\mu\lambda$. Thus, the time constant can be expressed as

$$
\tau \cong \frac{1}{2\mu\lambda}. \tag{4.25}
$$

4.5 The Least-Mean-Square (LMS) Algorithm

Steepest-descent method needs to estimate the gradient. The direct estimation procedure can be quite complex and hard to implement. In 1960, Widrow and Hoff developed a simpler algorithm for descending on the performance surface, known as the least-mean-square (LMS) algorithm. The LMS algorithm has the following advantages:

- Simplicity in implementation.

- Ease of computation.

- Doesn't require off-line gradient estimation.

- Stable and robust performance against different signal conditions.

Consequently, LMS is a widely used adaptive filtering algorithm in practice.

To develop the LMS algorithm, we take the square of the error signal $e^2(n)$ as an estimate of ξ. By (4.4), the gradient of $e^2(n)$ is

$$\hat{\nabla}(n) \equiv \begin{bmatrix} \frac{\partial e^2(n)}{\partial p_0} \\ \vdots \\ \frac{\partial e^2(n)}{\partial p_{N-1}} \end{bmatrix} = 2e(n) \begin{bmatrix} \frac{\partial e(n)}{\partial p_0} \\ \vdots \\ \frac{\partial e(n)}{\partial p_{N-1}} \end{bmatrix} = -2e(n)\mathbf{x}(n). \tag{4.26}$$

From (4.13), we obtain the LMS recursion,

$$\begin{aligned} \mathbf{p}(k+1) &= \mathbf{p}(k) - \mu\hat{\nabla}(k) \\ &= \mathbf{p}(k) + 2\mu e(k)\mathbf{x}(k). \end{aligned} \tag{4.27}$$

To examine the convergence of the LMS algorithm, we first note that the gradient estimate in (4.26) can readily be shown to be unbiased when the parameter vector is held constant [38]. The expected value of (4.26) is

$$\begin{aligned} E[\hat{\nabla}(k)] &= -2E[e(k)\mathbf{x}(k)] \\ &= -2E[d(k)\mathbf{x}(k) - \mathbf{x}(k)\mathbf{x}^T(k)\mathbf{w}] \\ &= 2(\mathbf{Cp} - \mathbf{U}). \end{aligned} \tag{4.28}$$

Since the expected value of $\hat{\nabla}(k)$ is equal to the true gradient of ξ (4.10), $\hat{\nabla}(k)$ is an unbiased estimate. Due to the gradient estimate being unbiased, the LMS algorithm behaves just like the steepest descent algorithm on average. Therefore, the conclusion of the stability and time constant discussed in the previous sections can be applied to the LMS algorithm as well.

4.5.1 Stability and Convergence

The stability requirement of the LMS algorithm seems to be the same as that of the steepest-descent algorithm. However, the use of a stochastic gradient in the LMS algorithm makes it more sensitive to the value of its step size μ. Therefore, the bound of the LMS algorithm is much lower than the corresponding bound in the case of the steepest-descent algorithm. The LMS algorithm remains stable when

$$0 < \mu < \frac{1}{3\mathrm{tr}[\mathbf{C}]}, \tag{4.29}$$

where $\mathrm{tr}[\mathbf{C}]$ is the trace of the input correlation matrix $\mathbf{C}$, i.e., $\mathrm{tr}[\mathbf{C}] = \sum_{i=o}^{N-1} \lambda_i$. A detailed derivation of (4.29) can be found in [39].

The following chapter will give the circuit implementation of the MCE method [2] and an analysis of the LMS loop used in the MCE method.
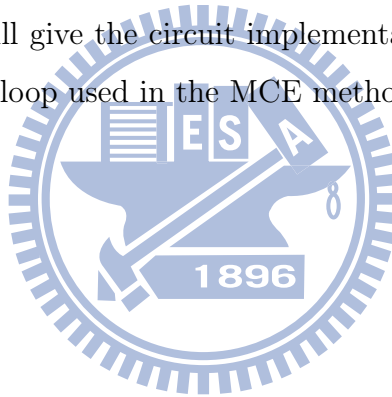
Chapter 5

CIRCUIT IMPLEMENTATION OF THE DIGITAL BACKGROUND CALIBRATION PROCESSOR FOR A 12-BIT 100MS/S PIPELINED ADC PROTOTYPE WITH OPEN-LOOP RESIDUE AMPLIFIERS

5.1 A 12-bit 100MS/s Pipelined ADC Prototype with Open-Loop Residue Amplifiers

In conventional pipelined ADC, a closed-loop opamp based MDAC is implemented in a pipeline stage. Because the feedback topology desensitizes the environmental variation, the pipeline stage can be highly linear and more robust. However, these advantages come from a high open-loop gain OPAMP and it costs large power dissipation. Moreover, designing precise analog components is very challenging in advanced CMOS technology.

On the contrary, an open-loop residue amplifier can provide a similar gain. With the open-loop topology, the demand for a high open-loop gain amplifier is no longer necessary and the power dissipation drops as well [2]. The benefits of using the open-loop residue amplifier in the pipelined ADC is recognized and demonstrated in [3, 40, 41]. However, because the absence of the feedback no longer assists desensitizing the environmental variations, some calibration scheme must be used to address the linearity issue of the pipeline stage.

Reference [1] proposes a pipelined ADC using open-loop residue amplifiers in conjunction with a digital background calibration scheme [2] to simultaneously achieve the requirements of a high speed, high resolution, and low power consumption.

Figure 5.1: A 12-bit 100MS/s pipelined ADC prototype.

The ADC prototype is shown in Fig. 5.1. The 12-bit 100MS\s pipelined ADC has the same (3+1)-bit open-loop structure for the first and the second pipeline stages. A 6-bit flash ADC follows the second pipeline stage as the backend ADC. The function of each block will be described in the following section.

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5.2 Digital Circuit Implementation

5.2.1 The Pipeline Stage under Calibration

Figure 5.2: Model of the j-th pipeline stage under calibration.

Figure 5.2 shows the model of the j-th pipeline stage under calibration.

- A nonlinear residue amplifier G_j: the nonlinear residue amplifier is assumed to have a transfer function of $v_{resj} = G_j(v_x) = a_1(v_x) + a_3(v_x)^3$. Since the open-loop residue amplifier in each stage is fully differential, the even-order nonlinear terms are less significant and thus are ignored.

- DEC: using over-range codes to alleviate the influence of the sub-ADC's offset. A detailed analysis is presented in [1].

- PCSG: Pseudo-random calibration sequence generator formed by the following three blocks.

  - N_{di}, $i \in \{1, 2\}$: for selecting one of the two calibration signals.

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- DEM: to ensure the ratio of the calibration signals accurate enough.

  - PNG: pseudo-random number generator to generate $R_i \in \{+1, -1\}$, $i \in \{1, 2\}$.

- Estimation: to provide the calibration parameters P_1 and P_3.

- Calibration: use a function $2\sqrt{\dfrac{-1}{3P_3}} \cos\left[\dfrac{\pi}{3} + \dfrac{1}{3} \cos^{-1}\left(\dfrac{D_{bi}}{2\sqrt{\frac{-1}{27P_3}}}\right)\right]$ to recover the linear term of the residue amplifier [3]. For the practical case, it's almost a gain compressive transfer function ($P_3 < 0$). Moreover, the D_{bi} is designed between ± 0.5 to avoid a complex form. In our practical implementation, the required two-dimensional calibration function is precomputed and stored in a lookup table made of a ROM.

5.2.2 The MCE Algorithm

The MCE algorithm [2] has been described in section 3.4. Using two different modulated sequences, it results in the residue having different distributions. As a result, using the statistical results associated with the residues to find the error information. Then, the error information can be applied to LMS loops to track the correction parameters.

For practical implementation, a stricter derivation must be considered. In order to distinguish the analog signals from the digital signals, we modify (3.14)

$$
\begin{aligned}
D_{bi} &= \frac{a_1}{v_{ref}}(-v_{qa} - R_i v_{di}) + \frac{a_3}{v_{ref}}(-v_{qa} - R_i v_{di})^3 + \frac{v_{qb}}{v_{ref}} + \frac{v_{ob}}{v_{ref}} \\
&= a_1\left(-\frac{v_{qa}}{v_{ref}} - R_i \frac{v_{di}}{v_{ref}}\right) + a_3 v_{ref}^2\left(-\frac{v_{qa}}{v_{ref}} - R_i \frac{v_{di}}{v_{ref}}\right)^3 + \frac{v_{qb}}{v_{ref}} + \frac{v_{ob}}{v_{ref}},
\end{aligned}
$$

(5.1)

where v_{ref} is the converter's reference voltage and here we take the offset v_{ob} of the backend ADC into account. Let the normalized analog signals to be $N_{qa} = v_{qa}/v_{ref}$, $N_{qb} = v_{qb}/v_{ref}$, $N_{ob} = v_{ob}/v_{ref}$, $N_{di} = v_{di}/v_{ref}$, $A_1 = a_1$, and $A_3 = a_3 v_{ref}^2$. Substituting

these notations into (5.1), the result is

$$
\begin{aligned}
D_{bi} &= A_1(-N_{qa} - R_i N_{di}) + A_3(-N_{qa} - R_i N_{di})^3 + N_{qb} + N_{ob} \\
&= A_1(-N_{qa} - R_i N_{di}) + \\
&\quad A_3(-N_{qa}^3 - 3N_{qa}^2 R_i N_{di} - 3N_{qa} N_{di}^2 - R_i N_{di}^3) + N_{qb} + N_{ob}.
\end{aligned}
\tag{5.2}
$$

Based on the properties of the R_i as mentioned in section 3.4, taking the correlations of R_i and D_{bi}, results in

$$
E[R_i D_{bi}] = A_1(-N_{di}) + A_3(-3N_{qa}^2 N_{di} - N_{di}^3).
\tag{5.3}
$$

This finding reveals the quantization error and the offset of the backend ADC doesn't affect the accuracy of the estimation compared with [3].

A similar derivation as mentioned in section 3.4 can be shown that the estimations of the 3rd-order nonlinear term and the linear gain error of the residue amplifier are

$$
\varepsilon_3 \equiv E[R_1 N_{d1}] - 2E[R_2 N_{d2}] = -\frac{3}{4} A_1^3 N_{d1}^3 (P_{3,opt} - P_3),
\tag{5.4}
$$

$$
\varepsilon_1 \equiv E[R_1 N_{d1}] = A_1(-N_{d1}),
\tag{5.5}
$$

where $P_{3,opt} \equiv \dfrac{A_3}{A_1^3}$. In order to save the divider in Eq. (3.23), we modify the ε_1' to be

$$
\varepsilon_1' \equiv \varepsilon_1 + P_1 N_{d1} = -N_{d1}(P_{1,opt} - P_1),
\tag{5.6}
$$

where $P_{1,opt} \equiv A_1$. After getting the error information for linear gain error and 3rd-order nonlinear gain error of the residue amplifier, the correction parameters can be found by the LMS algorithm. Based on the LMS algorithm depicted in the previous chapter, two recursions are constructed with respect to ε_3 and ε_1' and shown in Fig. 5.3.

$$
P_3(k+1) = P_3(k) - \mu_3 \varepsilon_3,
\tag{5.7}
$$

$$
P_1(k+1) = P_1(k) - \mu_1 \varepsilon_1'.
\tag{5.8}
$$

Figure 5.3: LMS loop.

5.2.3 LMS Loop Analysis

Substituting(5.4) and (5.5) into (5.7) and (5.8), respectively, the two recursions (LMS loops) can be expressed as:

$$
\begin{aligned}
P_3(k+1) &= P_3(k) + \mu_3(P_{3,opt} - P_3)\frac{3}{4}A_1^3 N_{d1}^3 \\
&= P_3(k) + 2\mu_3(P_{3,opt} - P_3)\frac{3}{8}A_1^3 N_{d1}^3, \quad (5.9) \\
P_1(k+1) &= P_1(k) + \mu_1(P_{1,opt} - P_1)N_{d1} \\
&= P_1(k) + 2\mu_1(P_{1,opt} - P_1)\frac{N_{d1}}{2}. \quad (5.10)
\end{aligned}
$$

Recall (4.4) and (4.27), if the input signal is a scalar, considering univariable pa-

rameter, (4.27) can be rewritten as

$$
\begin{aligned}
p(k+1) &= p(k) + 2\mu ex \\
&= p(k) + 2\mu(d - px)x \\
&= p(k) + 2\mu(p_{opt} - p)x^2 \\
&= p(k) + 2\mu(p_{opt} - p)\lambda.
\end{aligned}
\tag{5.11}
$$

Since the input signal is a scalar, $tr[\mathbf{C}] = x^2 = \lambda$. Comparing (5.10) and (5.9) with (5.11), an equivalent adaptive system model of the recursions is illustrated in Fig. 5.4. It's obvious that the eigenvalue of the P_3-LMS-loop is $\lambda_3 = \dfrac{3}{8} A_1^3 N_{d1}^3$ and the eigenvalue of the P_1-LMS-loop is $\lambda_1 = \dfrac{N_{d1}}{2}$.
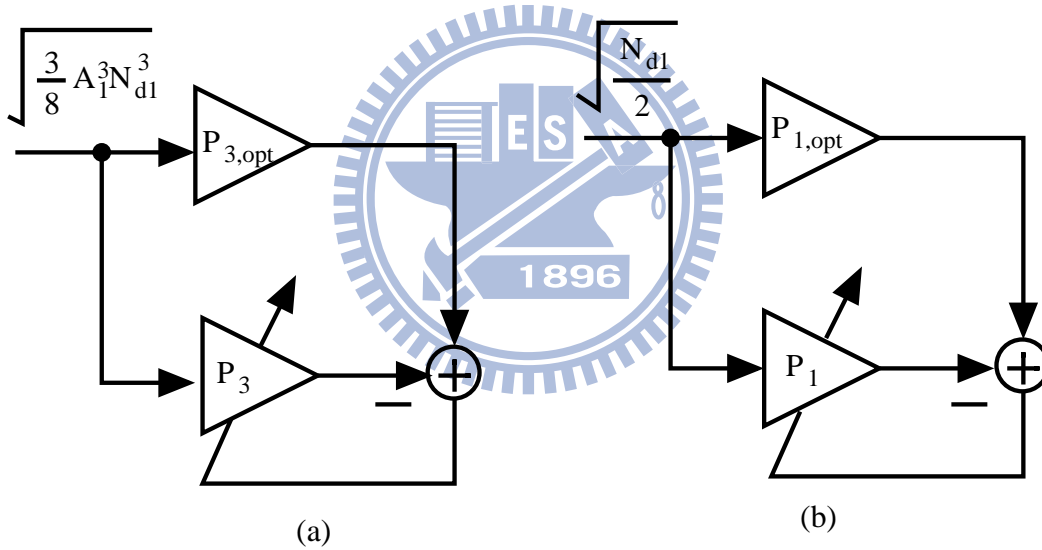

Figure 5.4: An equivalent adaptive system model of (a) Eq.(5.9) and (b) Eq. (5.10).

Based on the analysis of the LMS algorithm in the previous chapter, the stability and time constants of theses two LMS loops can be given as follow.

5.2.3.1   Stability and Convergence

In the LMS loop, the step size determines the convergent speed and stability of the loop. By (4.29), the range of the step size should be

$$0 < \mu_3 < \frac{1}{3\lambda_3}$$
$$\Rightarrow \quad 0 < \mu_3 < \frac{8}{9A_1^3 N_{d1}^3}, \tag{5.12}$$
$$0 < \mu_1 < \frac{1}{3\lambda_1}$$
$$\Rightarrow \quad 0 < \mu_1 < \frac{2}{3N_{d1}}, \tag{5.13}$$

to ensure the two LMS loops to be convergent and stable.

It's worthy noting that the results are necessary condition rather than effective ones. In reality, the step size is far smaller than the upper bound.

5.2.3.2   Time Constant

The time constants of the two LMS loops can be determined by Eq. (4.25) which are

$$\tau_3 \cong \frac{1}{2\mu_3\lambda_3} = \frac{4}{3\mu_3 A_1^3 N_{d1}^3}, \tag{5.14}$$
$$\tau_1 \cong \frac{1}{2\mu_1\lambda_1} = \frac{1}{\mu_1 N_{d1}}. \tag{5.15}$$

5.2.4   Samples of Each Correlation

From a system point of view, the injected calibration signals N_{di} is an additional noise to the pipelined ADC. The embedded signal $R_i N_{di}$ causes a fluctuation in D_{bi} within a uniform distribution between $\pm 0.5 v_{ref}$ (when $R_1 N_{d1}$ is injected). The resulting digital output D_{bi} is taken only after M cycles (samples) of each correlation. The *Law of Large Numbers* theorem[42, 43] tells

$$\sigma^2[m_{\mathrm{x}}] = \frac{1}{M}\sigma^2[\mathrm{x}], \tag{5.16}$$

where m_{x} is the M-sample expectation of an infinite-long random variable x and σ^2 denotes the variance. Hence, the variance of $E[R_i D_{bi}]$ can be expressed as

$$\sigma^2(E[R_i D_{bi}]) = \frac{1}{M}\sigma^2(R_i D_{bi}) = \frac{1}{M}\frac{v_{ref}^2}{12}. \tag{5.17}$$

To estimate the required sample numbers of each correlation, let the standard deviation of the calibration signals less than one half of the backend ADC's LSB voltage step V_{LSB} [4, 44], results in

$$M \geq \frac{1}{3} \times 2^{2B} \cong 2^{2B-1}, \tag{5.18}$$

where B is the number of bits of the backend ADC. From (5.18), the first pipeline stage in this prototype needs $M \cong 2^{17}$ samples, and the second pipeline stage needs $M \cong 2^{11}$ samples. To simplify the design of this ADC prototype, $M = 2^{17}$ is chosen for both the first and the second pipeline stage.

In [45], it was shown empirically that for an N-bit ADC, the number of required input samples is on the order of 2^{2N} to calibrate the gain errors. Therefore, we need approximately 2^7 iterations to track the correction parameters which is very close to the simulation results shown in the next chapter.

5.2.5　Discussion

The shaded blocks illustrated in Fig. 5.2 has been designed and implemented on an external FPGA using Verilog HDL. The FPGA board we used is Altera DE2-70. The synthesized result shows that 1024 logic cells are used.

If the correction table needs to cover all the percentage of the nonlinearity from 0% to 100%, a 12 M-bit ROM is need. Fortunately, the correction function is a cosine function which is a periodic data. Therefore, the table can be reduced to a quarter, i.e. 3 M-bit. In practice, there is no need to cover the full range of the nonlinear term. Simulations can show the nominal nonlinear term value. It is sufficient to add some reasonable range based on the nonminal value. For example, let the nonlinear term be 0.5 (50%) and assume the variation of the term be less than 20%. Then, the lookup

table needs to cover 0.4 to 0.6. Of course, most open-loop residue amplifiers have a nonlinear term less than 10% which means the lookup table is only few k-bit [3]. Some compression technique can be used to further minimize the required memory size [46].

The following chapter will give the simulation results of the prototype.

Chapter 6

SIMULATION RESULTS OF THE 12-BIT 100MS/S PIPELINED ADC PROTOTYPE

6.1 Simulation Setup

In this chapter, we use a behavioral model that closely resembles the pipelined ADC to validate the MCE algorithm. In order to compare the behavioral result with the register-transfer-level (RTL) result, the bit numbers in the behavioral code are truncated to be identical to the corresponding ones of the RTL code.

This model uses a fully differential (3+1)-bit/stage in the first and the second pipeline stage and then followed by an ideal 6-bit flash ADC. As a result, the total resolution of the ADC is 12-bit. In the simulation setup, the first and the second pipeline stages use the same open-loop residue amplifiers which provide non-perfect amplification. An appropriate model of the residue amplifier is

$$G_j(v_x) = a_1(v_x) + a_3(v_x)^3.$$

Table 6.1 summarizes the nominal values of a_1 and a_3 as well as the associated design

Table 6.1: Open-loop residue amplifier parameters.

Parameter	Description	Value
FS	Full scale range	1.2V
a_1	Linear gain error	7.5
a_3	3rd-order nonlinear gain error	-142.2

parameters. With the values listed in Table 6.1, the corresponding amplifier model is

$$G_j(v_x) = 7.5v_x - 142.2v_x^3 \tag{6.1}$$

which leads to the correction parameters $P_{1,opt} = 7.5$ and $P_{3,opt} = -0.485$.

6.2 Simulated ADC Performance

Figure 6.1 and 6.2 show the INL plots without and with calibration, respectively. Before calibration, the INL values are within +20.00/-20.00 LSB. After calibration, the INL is between +0.60/-0.49 LSB. A significant INL improvement is observed.

Figure 6.3 and Fig. 6.4 show the DNL plots without and with calibration, respectively. Before calibration, the DNL values are within +2.00/-1.00 LSB. Note that, a lot of missing codes exist. After calibration, the DNL reduces to be within +0.56/-0.78 LSB. The original missing codes are successfully corrected. Figure 6.5 shows the INL plot and the DNL plot after calibration in detail.

Figure 6.6 and 6.7 show the output spectra before and after calibration, respectively. Comparing Fig. 6.6 and 6.7 indicates that the simulated SNDR improves from 39.7 dB to 69.7dB and SFDR improves from 53.6 dBc to 93.4 dBc, respectively. The calibration improves the ENOB from 6.3 bits to 11.3 bits.

Table 6.2 summarizes the ADC performance without/with calibration. From the table, we see a great improvement on ADC performance after calibration.

Table 6.2: ADC performance.

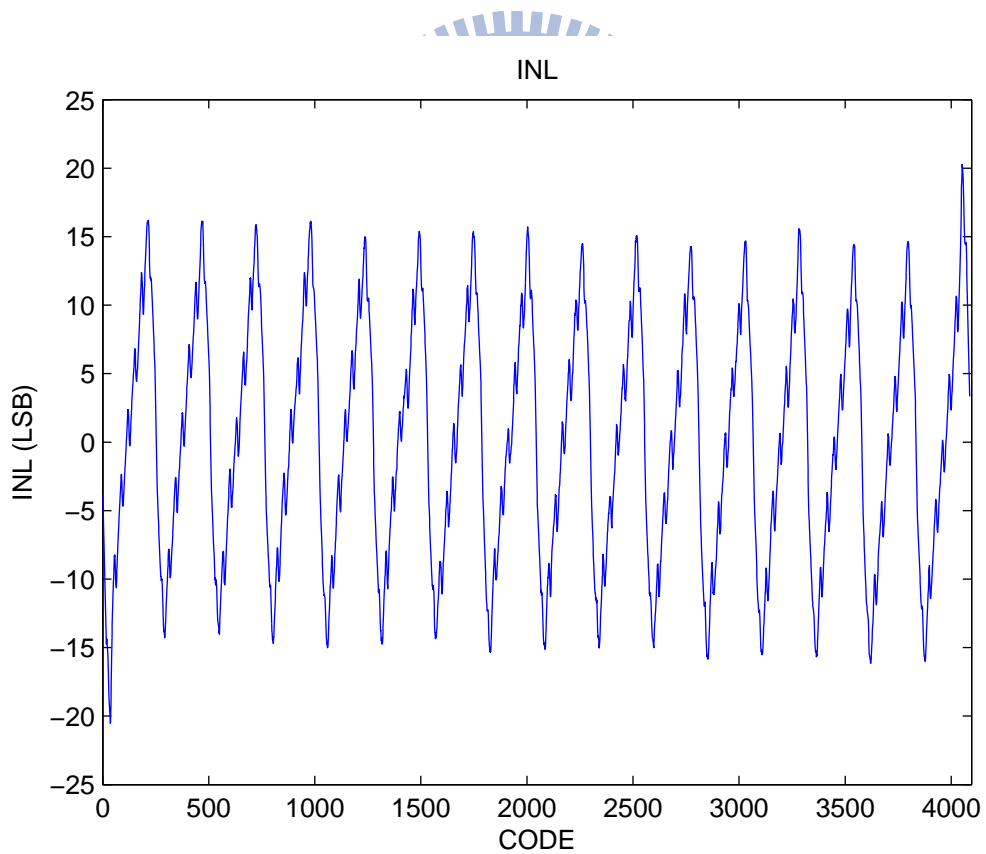| Performance metrics	Without calibration	With calibration
INL (LSB)	+20.00/-20.00	+0.60/-0.49
DNL (LSB)	+2.00/-1.00	+0.56/-0.78
SFDR (dBc)	53.6	93.4
SNDR (dB)	39.7	69.7
ENOB (bits)	6.3	11.3

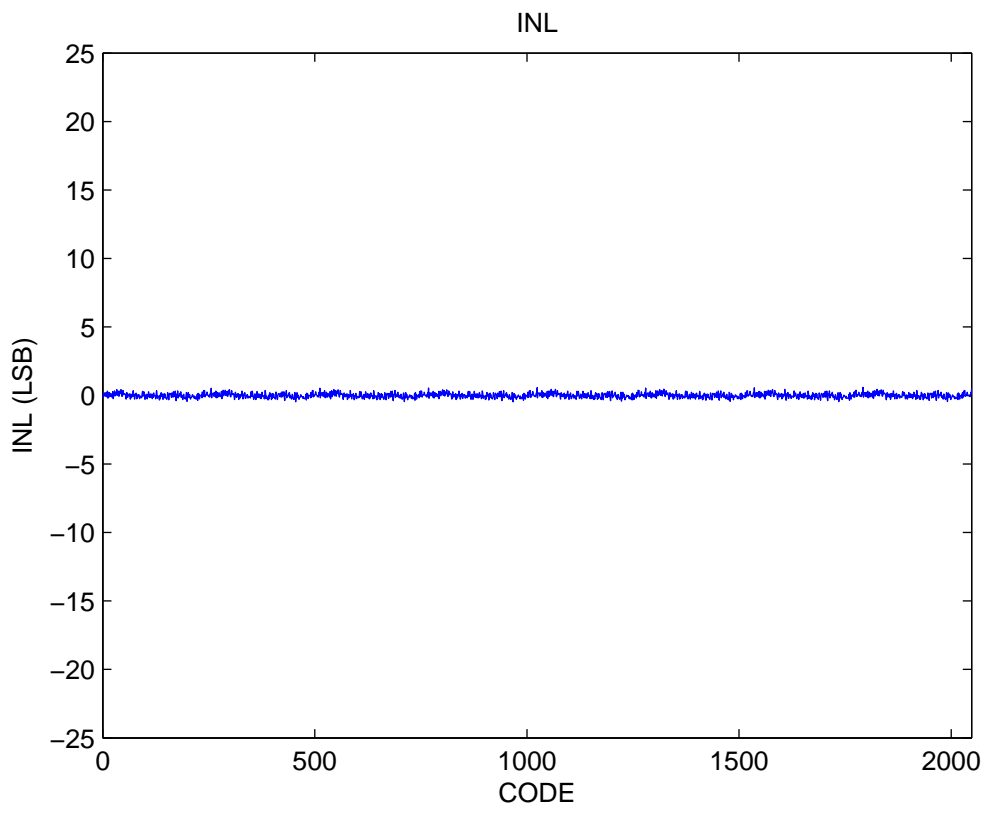Figure 6.1: INL without calibration.
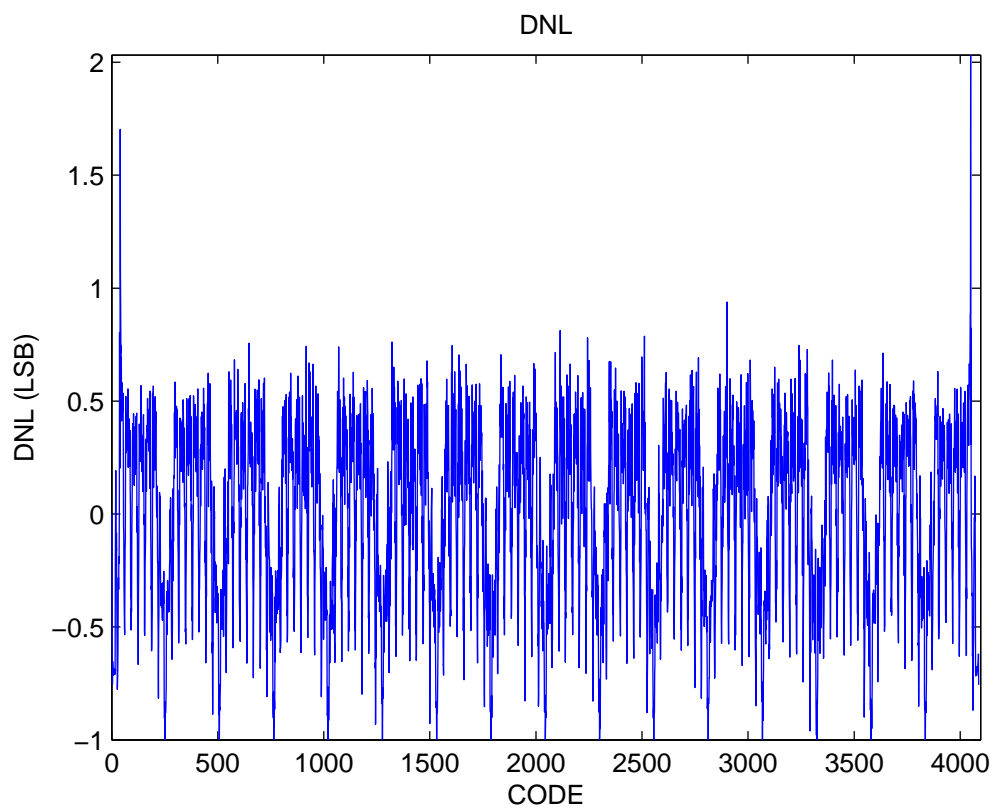
Figure 6.2: INL with calibration.
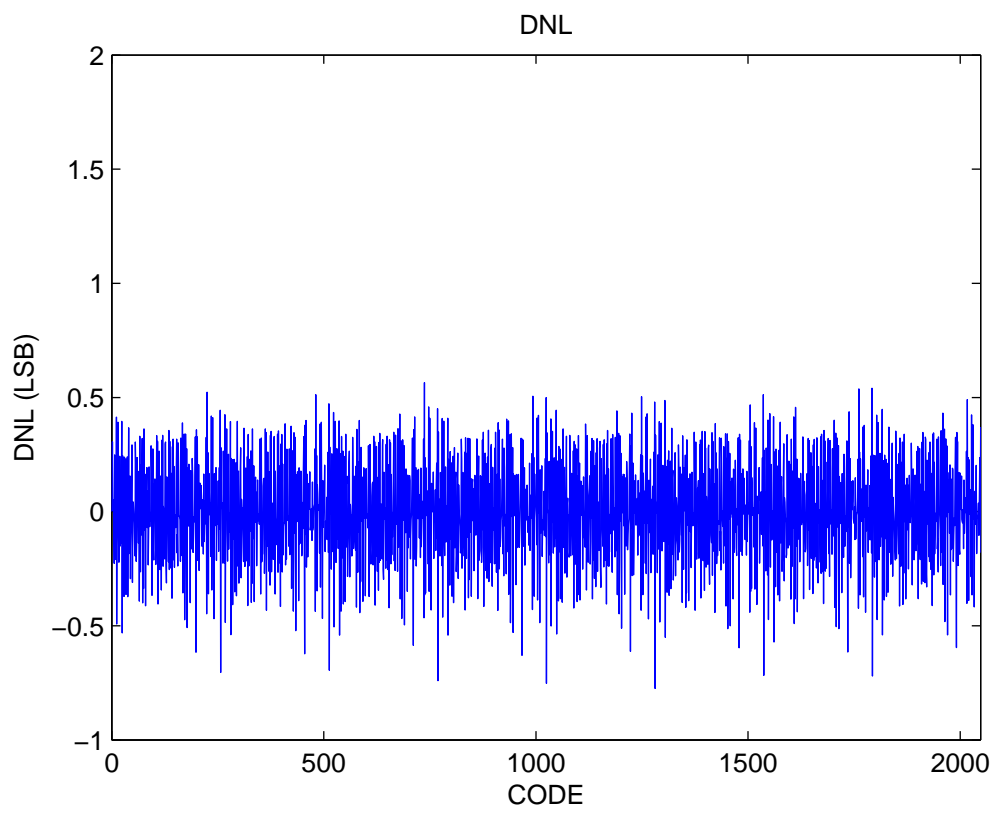
Figure 6.3: DNL without calibration.
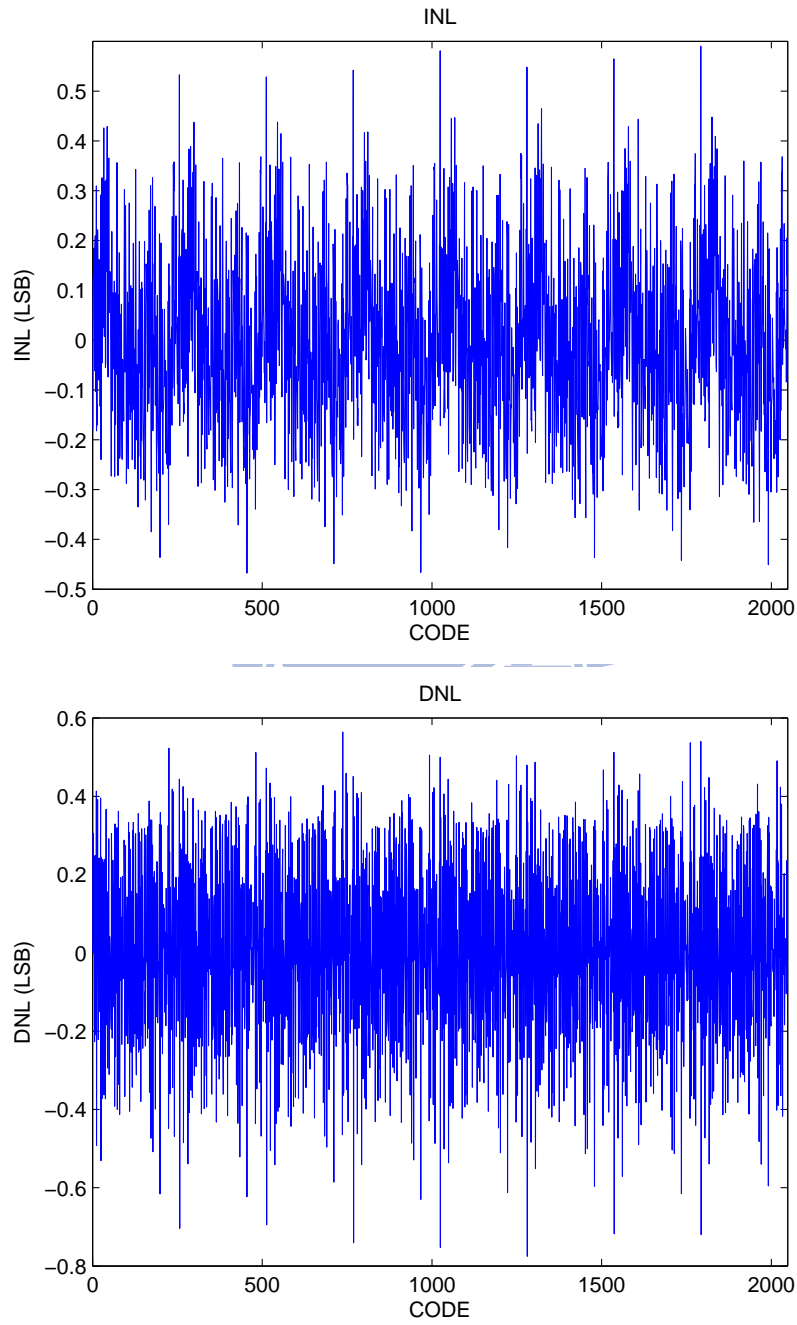
Figure 6.4: DNL with calibraiton.
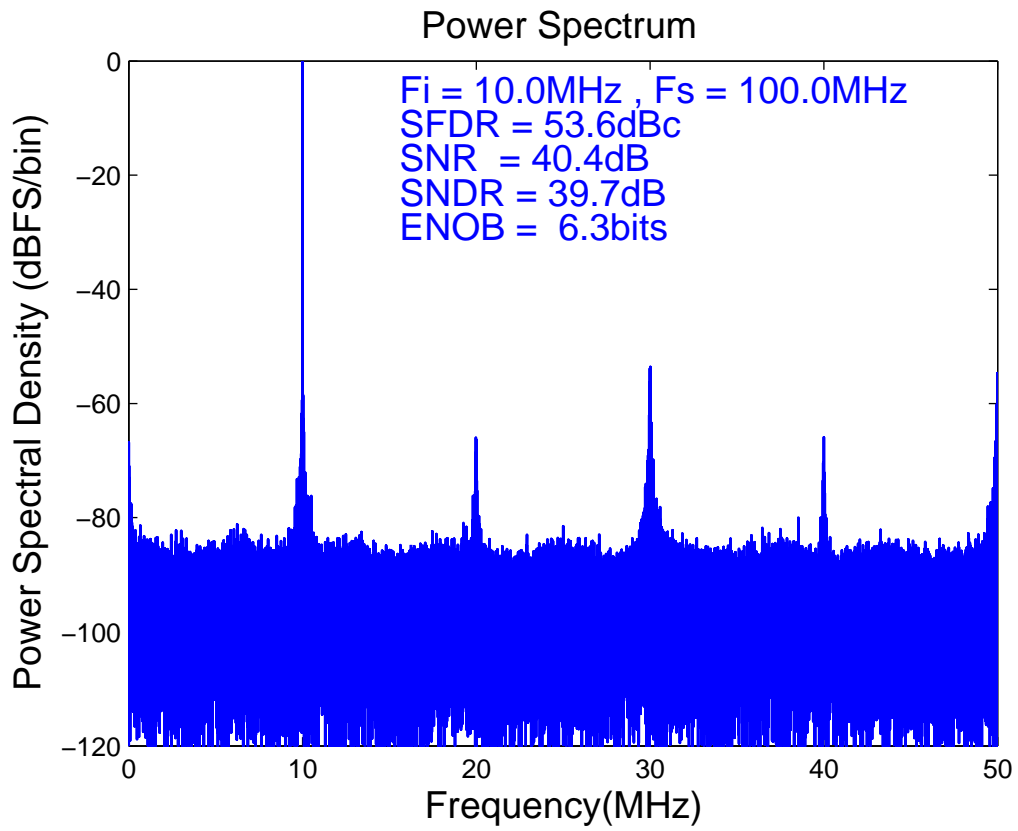
Figure 6.5: INL and DNL with calibration

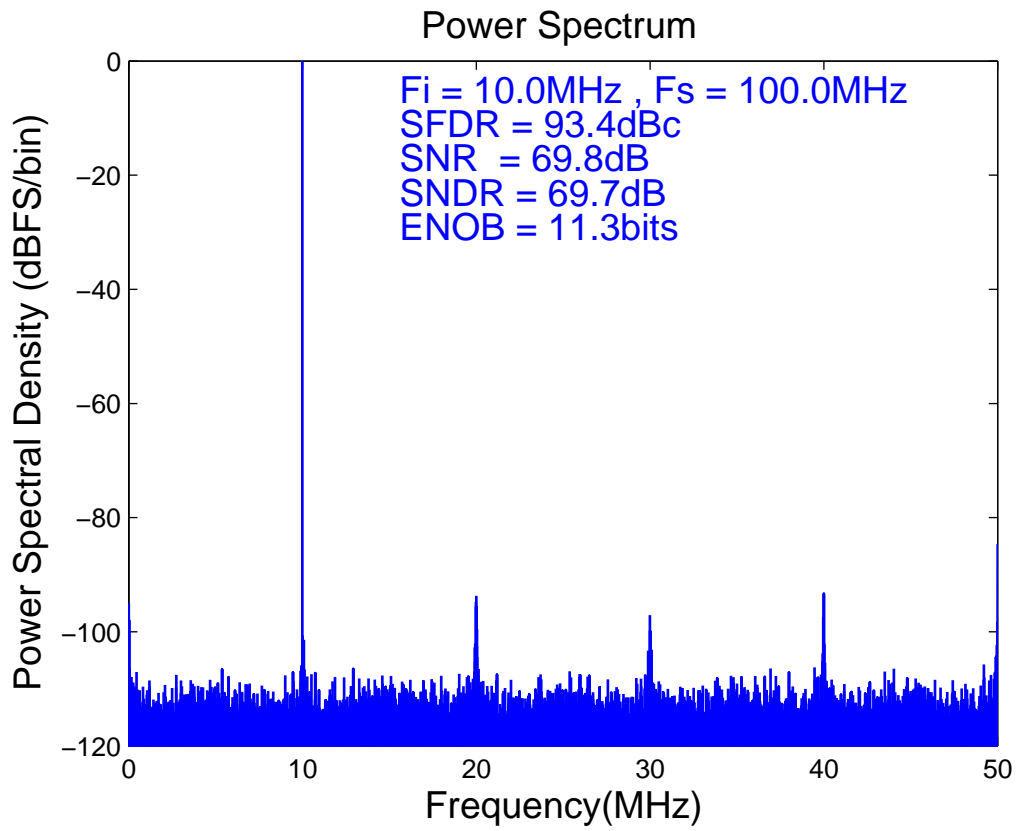Figure 6.6: FFT without calibration.

Figure 6.7: FFT with calibration.

6.3 LMS Loop Convergence

Figure 6.8 and 6.9 show the correction parameter convergence plots upon startup of P_1 and P_3 of the first and the second pipeline stage, respectively. The input signal is a full-scaled sinusoid. The samples of each correlation is 2^{17}, i.e., we take totally 2^{18} samples for each updates of P_1 and P_3.

With the help of the discussion in chapter 5, the step sizes of the P_1-LMS-loop and the P_3-LMS-loop are

$$0 < \mu_1 < 21, \tag{6.2}$$

$$0 < \mu_3 < 69. \tag{6.3}$$

Therefore, we choose the step sizes between these ranges. Also, we take the convergent speed into consideration. At the beginning, the step sizes are chosen for the time constants to be around 50 iterations. If the amplitude of the dither is small at the steady-state, the step size can be set to a larger value to speed up the convergence. Finally, the designed parameters of the LMS loops are summarized in Table 6.3. The step sizes are chosen not only suitable for the stability but also a special value to simplify the implementation (no multipliers are needed).

Table 6.3: LMS loop parameters.

Step size	Time constant
$\mu_1 = 0.5$	$\tau_1 = 64$ iterations
$\mu_3 = 2.25$	$\tau_3 = 38$ iterations

Figure 6.10 and 6.11 show the behavioral simulation results versus the RTL simulation results of the correction parameters P_1 and P_3. For the RTL simulation, it's not efficient to simulate with a sinusoidal input because the required test patterns are too large. Therefore, we apply a static input signal to make the simulations more efficient. Observing Fig. 6.10 and 6.11, the solid line is the behavioral simulation result and the dashed line is the RTL simulation result . It's obvious that the behavioral simulation results are identical to the RTL simulation results.
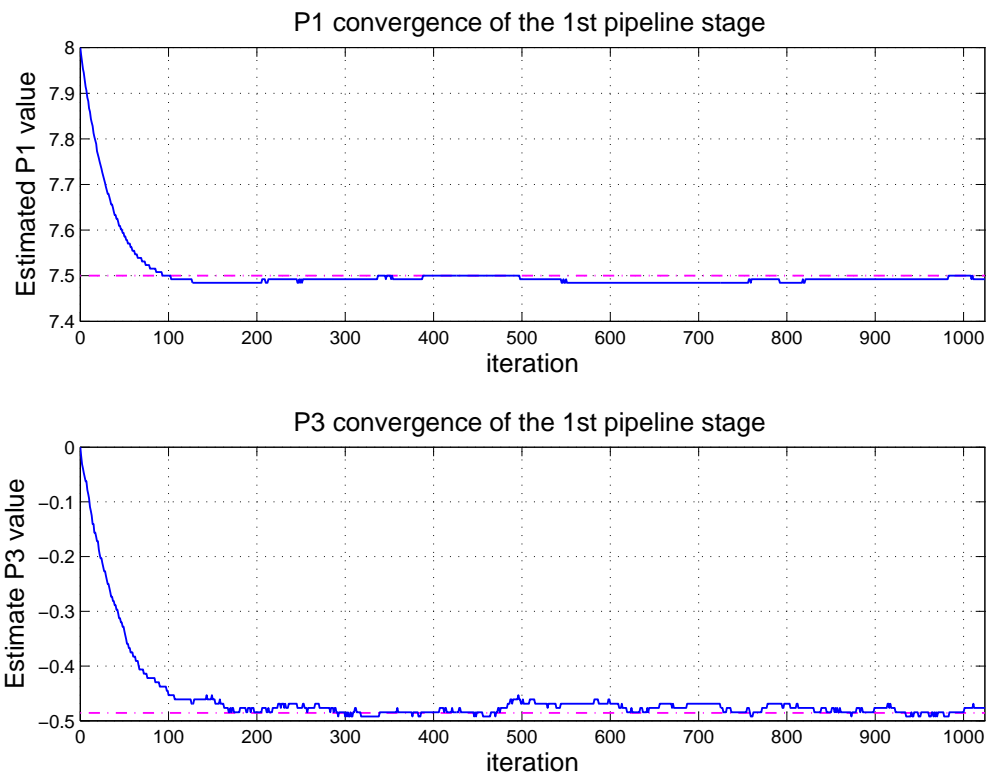
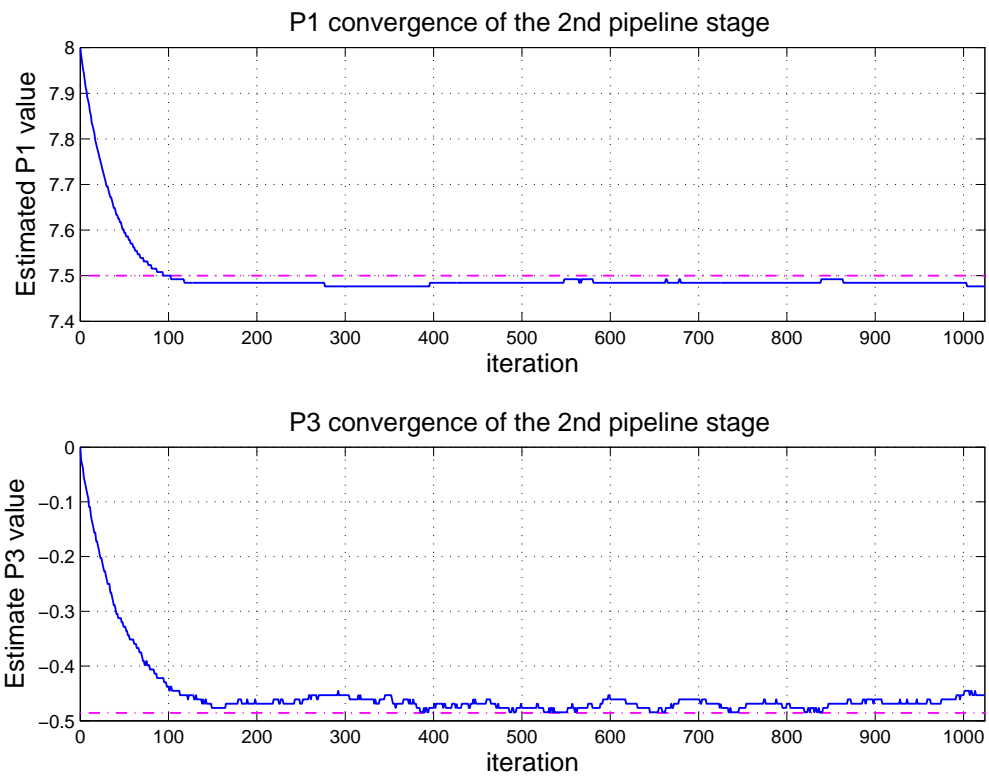Figure 6.8: LMS loop convergence of the first pipeline stage.

Figure 6.9: LMS loop convergence of the second pipeline stage.
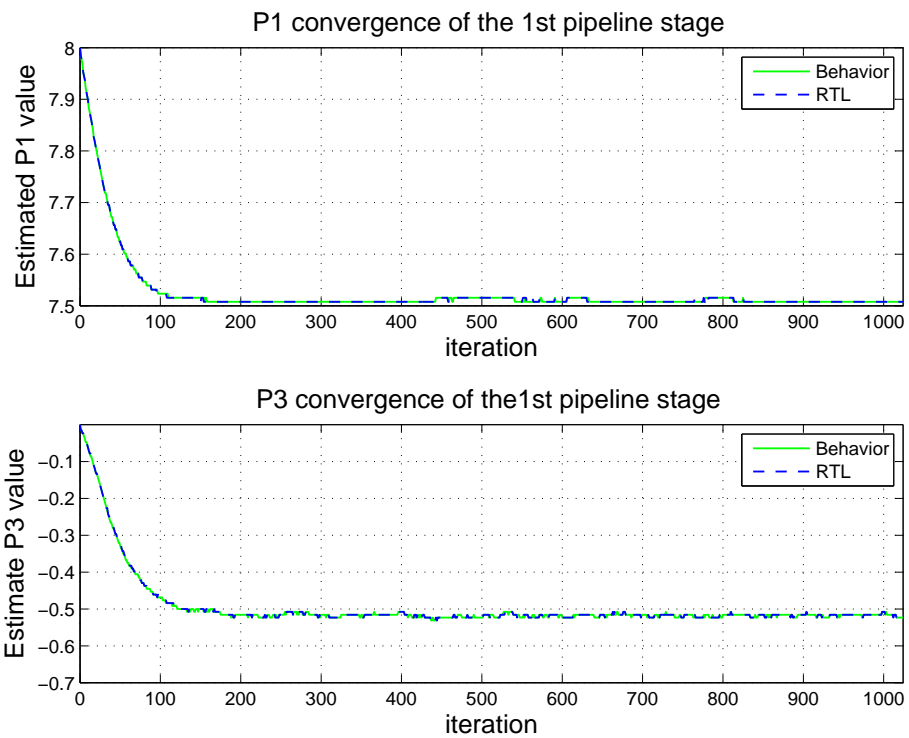
Figure 6.10: Behaviroal vs. RTL simulation result of the LMS loop convergence of the first pipeline stage.
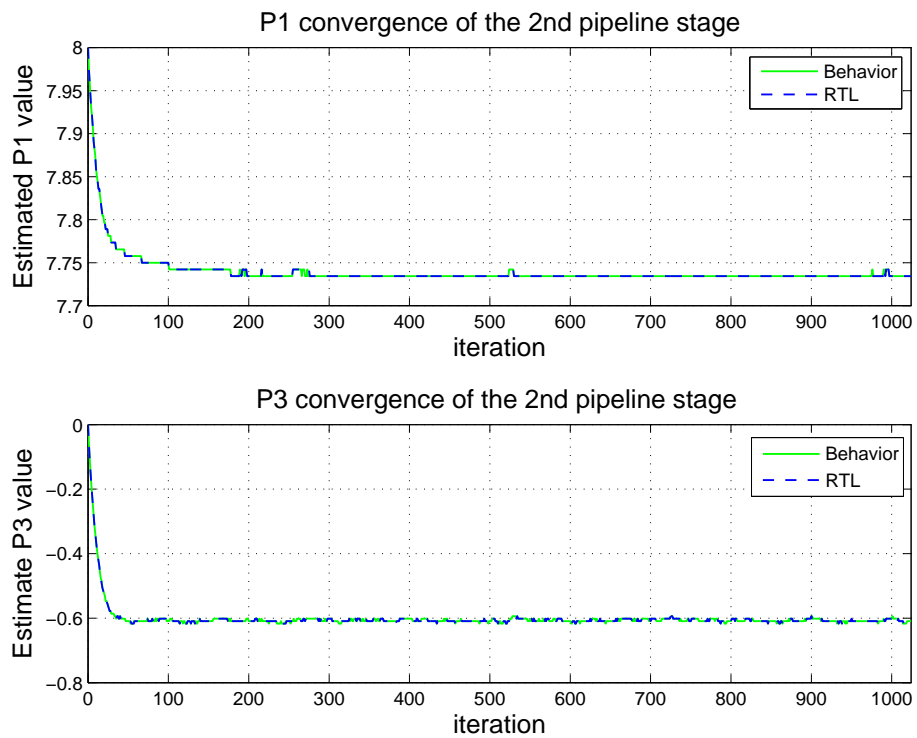
Figure 6.11: Behaviroal vs. RTL simulation result of the LMS loop convergence of the second pipeline stage.

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Chapter 7

PROPOSED DIGITAL BACKGROUND MCE METHOD FOR ESTIMATING MULTIPLE-ORDER NONLINEARITY OF THE RESIDUE AMPLIFIERS

In this chapter, we propose a novel digital background MCE method that can accurately estimate multiple-order nonlinear terms of the residue amplifiers. This proposed scheme makes use of the fact that the offsets in the sub-ADC doesn't affect the ADC conversion results based on the digital redundancy [23]. As most correlation based estimation methods, a random sequence whose values no more than the tolerable offset can be applied using either the sub-ADC or sub-DAC. To estimate the nonlinear terms lower than $(2m-1)$-order of the residue amplifiers, m calibration signals are applied to the pipeline stage under calibration.

In the remainder of this chapter, we discuss the MCE method from two points of

view, multiple-odd-order nonlinear terms and multiple-order nonlinear terms. Although the residue amplifier is usually implemented in fully differential topology, even-order nonlinear terms may exist if the circuit components are not perfectly matching. Moreover, to further reduce the power dissipation, a single-ended amplifier may be used due to the power is half of the fully differential one or a novel topology such as dynamic source follower amplifier [12] may be used. In this cases, the even-order nonlinear terms of the residue amplifier can not be ignored. Therefore, we also propose an estimation method for estimating the even-order nonlinear terms of the residue amplifiers. By this proposed estimation method with a calibration technique, it can substantially relax the precision of the analog circuit design and improve the pipelined ADC's performance.

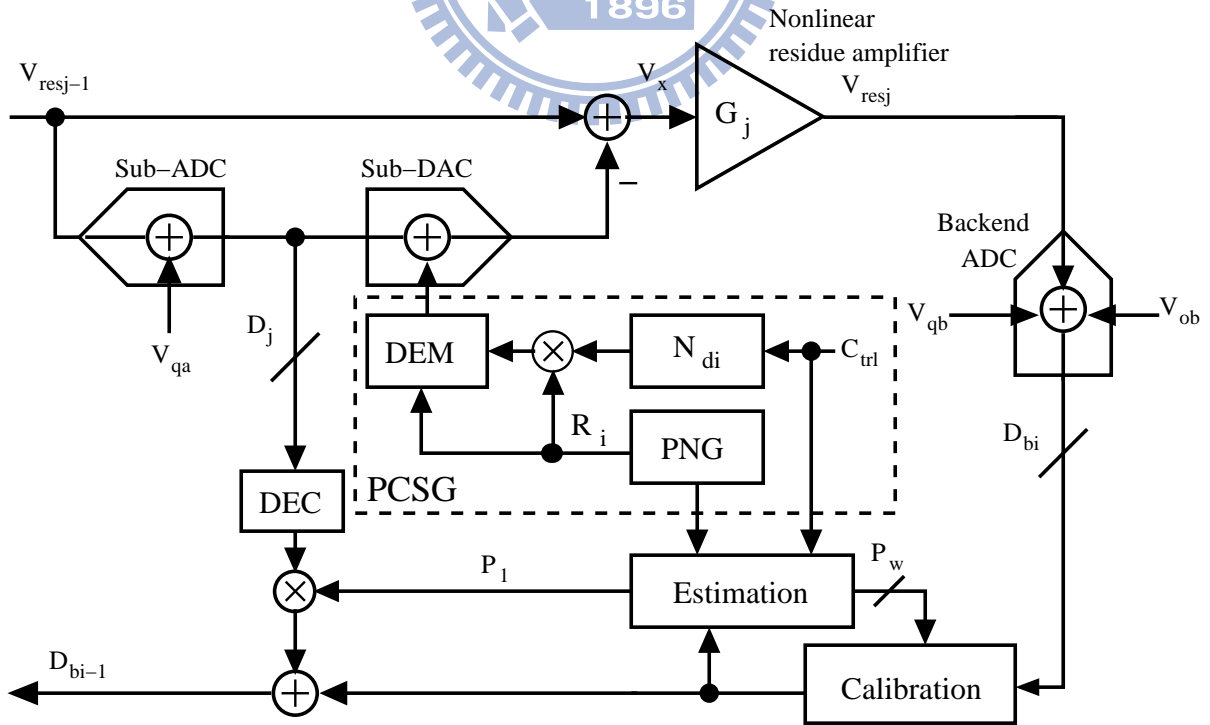## 7.1 Proposed MCE Method for Estimating Multiple-Odd-Order Nonlinear Terms of the Residue Amplifiers

Figure 7.1: Model of the j-th pipeline stage under calibration

Considering Fig. 7.1, the estimation block provides the correction parameters, P_w, where w denotes the coefficient of the w-th order term of the residue amplifier. The correction parameters are defined as

$$P_1 \equiv A_1, \tag{7.1}$$

$$P_w \equiv \frac{A_w}{A_1^w}, \quad \text{for } w > 1. \tag{7.2}$$

In order to unbiasedly estimate the nonlinearity of the residue amplifiers, the PNG is designed as a uniformly distributed pseudorandom binary sequence. That is, PNG$\in \{+1, -1\}$ and is uncorrelated with the ADC's input signal. The PCSG is continuously applied the calibration signals to the stage under calibration to estimate and track the correction parameters against environmental variations.

Now, assume the transfer function of the nonlinear residue amplifier contains the linear gain error, 3rd-order and 5th-order nonlinear gain errors. Then it can be expressed as

$$G_j(v_x) = a_1(v_x) + a_3(v_x)^3 + a_5(v_x)^5, \tag{7.3}$$

where a_5 is the coefficient of the 5th-order nonlinear term of the residue amplifier. The digitized residue D_{bi} when the random sequences are applied is

$$
\begin{aligned}
D_{bi}v_{ref} &= a_1(v_x) + a_3(v_x)^3 + a_5(v_x)^5 + v_{qb} + v_{ob} \\
\Rightarrow D_{bi} &= \frac{a_1}{v_{ref}}(-v_{qa} - R_i v_{di}) + \frac{a_3}{v_{ref}}(-v_{qa} - R_i v_{di})^3 + \\
&\quad \frac{a_5}{v_{ref}}(-v_{qa} - R_i v_{di})^5 + \frac{v_{qb}}{v_{ref}} + \frac{v_{ob}}{v_{ref}}, \ i \in \{1,2,3\} \\
\Rightarrow D_{bi} &= a_1\left(-\frac{v_{qa}}{v_{ref}} - R_i \frac{v_{di}}{v_{ref}}\right) + a_3 v_{ref}^2 \left(-\frac{v_{qa}}{v_{ref}} - R_i \frac{v_{di}}{v_{ref}}\right)^3 + \\
&\quad a_5 v_{ref}^4 \left(-\frac{v_{qa}}{v_{ref}} - R_i \frac{v_{di}}{v_{ref}}\right)^5 + \frac{v_{qb}}{v_{ref}} + \frac{v_{ob}}{v_{ref}}, \ i \in \{1,2,3\},
\end{aligned}
\tag{7.4}
$$

where $R_i \in \{+1, -1\}$ are the pseudo-random number sequences generated from the PNG block and uncorrelated with the input signal of the pipelined ADC.

For simplicity, we define the normalized analog signal $A_5 \equiv a_5 v_{ref}^4$, and use the same notations of the normalized analog signals in chapter 5. Substituting these notations

into (7.4),

$$
\begin{aligned}
D_{bi} &= A_1(-N_{qa} - R_iN_{di}) + A_3(-N_{qa} - R_iN_{di})^3 + A_5(-N_{qa} - R_iN_{di})^5 + \\
&\quad N_{qb} + N_{ob},\ i \in \{1,2,3\} \\
&= A_1(-N_{qa} - R_iN_{di}) + A_3(-N_{qa}^3 - 3N_{qa}^2 R_iN_{di} - 3N_{qa}N_{di}^2 - R_iN_{di}^3) + \\
&\quad A_5(-N_{qa}^5 - 5N_{qa}^4 R_iN_{di} - 10N_{qa}^3 N_{di}^2 - 10N_{qa}^2 R_iN_{di}^3 - 5N_{qa}N_{di}^4 - R_iN_{di}^5) \\
&\quad + N_{qb} + N_{ob},\ i \in \{1,2,3\}. \tag{7.5}
\end{aligned}
$$

As a result, R_i times N_{di} add offsets of $\pm N_{d1}$, $\pm N_{d2}$ or $\pm N_{d3}$ LSB (of the local sub-ADC) to the sub-DAC. They are

$$
\begin{aligned}
R_1 N_{d1} &\in \{+N_{d1}, -N_{d1}\} \\
R_2 N_{d2} &\in \{+N_{d2}, -N_{d2}\} \\
R_3 N_{d3} &\in \{+N_{d3}, -N_{d3}\}.
\end{aligned}
$$

Taking the correlation of D_{bi} and R_i, we have

$$
\begin{aligned}
E[R_i D_{bi}] &= E[A_1(-R_iN_{qa} - N_{di}) + A_3(-R_iN_{qa}^3 - 3N_{qa}^2 N_{di} - 3R_iN_{qa}N_{di}^2 \\
&\quad - N_{di}^3) + A_5(-R_iN_{qa}^5 - 5N_{qa}^4 N_{di} - 10R_iN_{qa}^3 N_{di}^2 - 10N_{qa}^2 N_{di}^3 - \\
&\quad 5R_iN_{qa}N_{di}^4 - N_{di}^5) + R_iN_{qb} + R_iN_{ob}]. \tag{7.6}
\end{aligned}
$$

Because R_i are uncorrelated with the input signal, the correlations of R_i and N_{qa}, N_{qb}, and N_{ob} are all zero. Therefore, (7.6) is further reduced to

$$
E[R_i D_{bi}] = A_1(-N_{di}) + A_3(-3N_{qa}^2 N_{di} - N_{di}^3) + A_5(-5N_{qa}^4 N_{di} - N_{di}^5). \tag{7.7}
$$

Equation (7.7) reveals that the quantization error and the offset of the backend ADC doesn't affect the estimation accuracy as compared with [3]. Furthermore, if the backend ADC has a conversion gain error, it can be referred to the previous stage as an additional gain factor. Therefore, the conversion gain error, the quantization error, and the offset of the backend ADC have no effect on the estimation accuracy.

By (7.7), the result is proportional to A_5 if the terms with A_1 and A_3 can be eliminated. For such a reason, we propose a technique called "multi-correlation estimation (MCE)" method that accurately estimates the error information of the residue amplifiers. This goal can be achieved by using $N_{d3} = N_{d2}/2 = N_{d1}/4 = \text{LSB}/8$ (of the local sub-ADC). The result is

$$
\begin{aligned}
\varepsilon_5 \quad &\equiv \quad E[R_1 D_{b1}] - 10E[R_2 D_{b2}] + 16E[R_3 D_{b3}] \\
&= \quad [A_1(-N_{d1}) + A_3(-3N_{qa}^2 N_{d1} - N_{d1}^3) + A_5(-5N_{qa}^4 N_{d1} - 10N_{qa}^2 N_{d1}^3 - N_{d1}^5)] \\
&\quad -10 \quad [A_1(-N_{d2}) + A_3(-3N_{qa}^2 N_{d2} - N_{d2}^3) + A_5(-5N_{qa}^4 N_{d2} - 10N_{qa}^2 N_{d2}^3 - N_{d2}^5)] \\
&\quad +16 \quad [A_1(-N_{d3}) + A_3(-3N_{qa}^2 N_{d3} - N_{d3}^3) + A_5(-5N_{qa}^4 N_{d3} - 10N_{qa}^2 N_{d3}^3 - N_{d3}^5)] \\
&= \quad [A_1(-N_{d1}) + A_3(-3N_{qa}^2 N_{d1} - N_{d1}^3) + A_5(-5N_{qa}^4 N_{d1} - 10N_{qa}^2 N_{d1}^3 - N_{d1}^5)] \\
&\quad -10 \quad \left[A_1(-\frac{N_{d1}}{2}) + A_3(-3N_{qa}^2 \frac{N_{d1}}{2} - \frac{N_{d1}^3}{8}) + A_5(-5N_{qa}^4 \frac{N_{d1}}{2} - 10N_{qa}^2 \frac{N_{d1}^3}{8} - \frac{N_{d1}^5}{32})\right] \\
&\quad +16 \quad \left[A_1(-\frac{N_{d1}}{4}) + A_3(-3N_{qa}^2 \frac{N_{d1}}{4} - \frac{N_{d1}^3}{64}) + A_5(-5N_{qa}^4 \frac{N_{d1}}{4} - 10N_{qa}^2 \frac{N_{d1}^3}{64} - \frac{N_{d1}^5}{1024})\right] \\
&= \quad A_5(-N_{d1}^5 + \frac{5}{16}N_{d1}^5 - \frac{1}{64}N_{d1}^5) \\
&= \quad -\frac{45}{64}N_{d1}^5 A_5.
\end{aligned}
$$

Therefore, ε_5 is directly proportional to A_5 and it gives an unbiased estimation. Assume the inverse function of the nonlinear residue amplifier $G_j^{-1}(v_{resj})$ exists. A further derivation of this nonlinear inverse function is beyond the scope of this thesis. We use an equivalent model of the inverse function as shown in Fig. 7.2, where D_{bx} is the digitized linear term of the residue amplifier. The calibration scheme can be modeled as

$$
D_{bi} - P_3 D_{bx}^3 - P_5 D_{bx}^5. \tag{7.8}
$$

Based on this assumption, the 3rd-order and 5th-order nonlinear terms can be cancelled in the digital domain. If the correction function (7.8) is applied, we obtain

$$
\varepsilon_5 = -\frac{45}{64}N_{d1}^5 A_1^5 (P_{5,opt} - P_5). \tag{7.9}
$$

This result indicates the deviation of the correction parameter P_5 from its ideal value is

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directly proportional to ε_5. Therefore, it can be applied to the LMS loop to minimize the deviation so as to obtain the ideal value of the P_5.
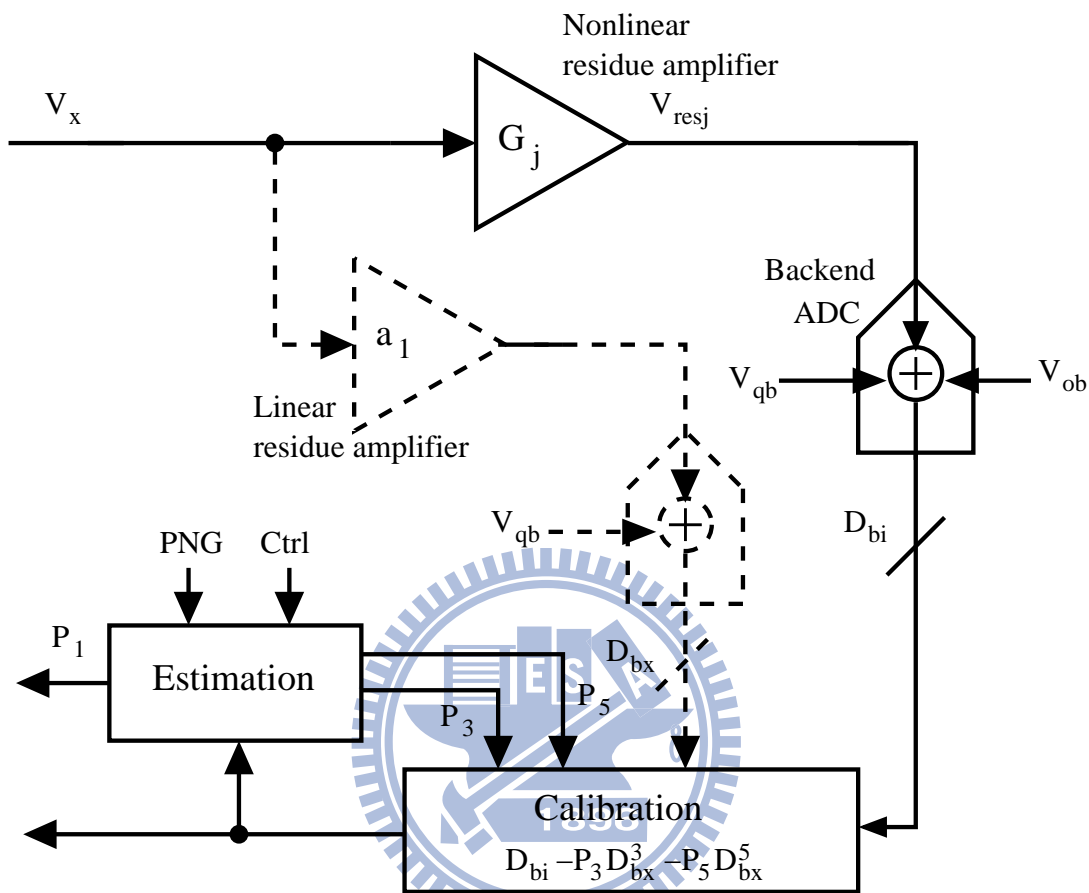

Figure 7.2: Equivalent model of the calibration scheme for multiple-odd-order nonlinear terms.

Once the 5th-order nonlinear term is cancelled, A_5 in (7.7) will be zero. As a result,

$$E[R_i D_{bi}] = A_1(-N_{di}) + A_3(-3N_{qa}^2 N_{di} - N_{di}^3). \qquad (7.10)$$

Notice that (7.10) is the same as (5.3). Therefore, the same estimations of the 3rd-order nonlinear term and the linear gain error of the residue amplifier shown by (5.4) and (5.5) hold.

Table 7.1: Coefficients C_{oi} of the MCE method for the estimation of the odd-order nonliner terms if the ratios of the calibration signals are geometric series of 2.

$(2m-1)$-order	3rd-order	5th-order	7th-order
m	2	3	4
$\varepsilon_{(2m-1)}$	$-\frac{3}{4}N_{d1}^3 A_3$	$-\frac{45}{64}N_{d1}^5 A_5$	$-\frac{2835}{4096}N_{d1}^7 A_7$
C_{o1}	$(-2)^0$	$(-2)^0$	$(-2)^0$
C_{o2}	$(-2)^1$	$(-2)^1 \times 5$	$(-2)^1 \times 3 \times 7$
C_{o3}	0	$(-2)^4$	$(-2)^4 \times 3 \times 7$
C_{o4}	0	0	$(-2)^9$

7.1.1 Discussion

The estimation of the $(2m-1)$-order nonlinear term is

$$\varepsilon_{2m-1} \equiv \sum_{i=1}^{m} C_{oi} E[R_i D_{bi}], \tag{7.11}$$

where m indicates m calibration signals are applied and C_{oi} are the coefficients of the MCE method for the estimation of the odd-order nonlinear terms.

Any other odd-order nonlinear term estimation of the residue amplifier can be determined similarly as mentioned above. For example, if we inject four calibration signals $N_{d4} = N_{d3}/2 = N_{d2}/4 = N_{d1}/8 = \text{LSB}/16$ (of the local sub-ADC), the estimation of the 7th-order nonlinear term can be expressed as

$$\varepsilon_7 \equiv E[R_1 D_{b1}] - 42E[R_2 D_{b2}] + 336E[R_3 D_{b3}] - 512E[R_4 D_{b4}] = -\frac{2835}{4096}N_{d1}^7 A_7,$$

where $A_7 = a_7 v_{ref}^6$ and a_7 is the coefficient of the 7th-order nonlinear term of the residue amplifier. Table 7.1 summarizes the coefficients C_{oi} of the MCE method for estimating the odd-order nonlinear terms when the ratios of the calibration signals are geometric series of 2. In fact, there's no need to choose the ratios of the calibration signals to be geometric series of 2. The coefficients of the MCE can be adjusted to suit any selected ratios of the calibration signals.

7.2 Proposed MCE Method for Estimating Multiple-Order Nonlinear Terms of the Residue Amplifiers

Now, let's take the even-order nonlinear term into account. Assume the nonlinearity of the residue amplifier contains the linear gain error and the 2nd-order and 3rd-order nonlinear gain errors, i.e., the transfer function of the residue amplifier is

$$G_j(v_x) = a_1(v_x) + a_2(v_x)^2 + a_3(v_x)^3, \tag{7.12}$$

where a_2 is the coefficient of the 2nd-order nonlinear term of the residue amplifier. The digitized residuum D_{bi} when the random sequences are applied is

$$
\begin{aligned}
D_{bi} &= A_1(-N_{qa} - R_i N_{di}) + A_2(-N_{qa} - R_i N_{di})^2 + A_3(-N_{qa} - R_i N_{di})^3 \\
&\quad + N_{qb} + N_{ob} \\
&= A_1(-N_{qa} - R_i N_{di}) + A_2(N_{qa}^2 + 2N_{qa}R_i N_{di} + N_{di}^2) + A_3(-N_{qa}^3 \\
&\quad -3N_{qa}^2 R_i N_{di} - 3N_{qa}N_{di}^2 - R_i N_{di}^3) + N_{qb} + N_{ob}, \ i \in \{1, 2\}, \tag{7.13}
\end{aligned}
$$

where $A_2 \equiv a_2 v_{ref}$. Other notations in (7.13) are the same as those in chapter 5.

Similar to the derivation in section 7.1, taking the correlations of D_{bi} and R_i gives

$$E[R_i D_{bi}] = A_1(-N_{di}) + A_2(2N_{qa}N_{di}) + A_3(-3N_{qa}^2 N_{di} - 3N_{di}^3). \tag{7.14}$$

Assume $N_{d2} = N_{d1}/2 = \text{LSB}/4$ (of the local sub-ADC), the estimation of the 3rd-order nonlinear term is the same as (5.4).

From (7.14), it's obvious that the 2nd-order nonlinear term doesn't affect the estimation of the 3rd-order nonlinear term because the term $A_2(2N_{qa}N_{di})$ is eliminated during the MCE procedure.

The calibration scheme of the 3rd-order nonlinear term is similar to that in section 7.1 and is shown in Fig. 7.3. If the 3rd-order nonlinear term is cancelled, A_3 in (7.13)
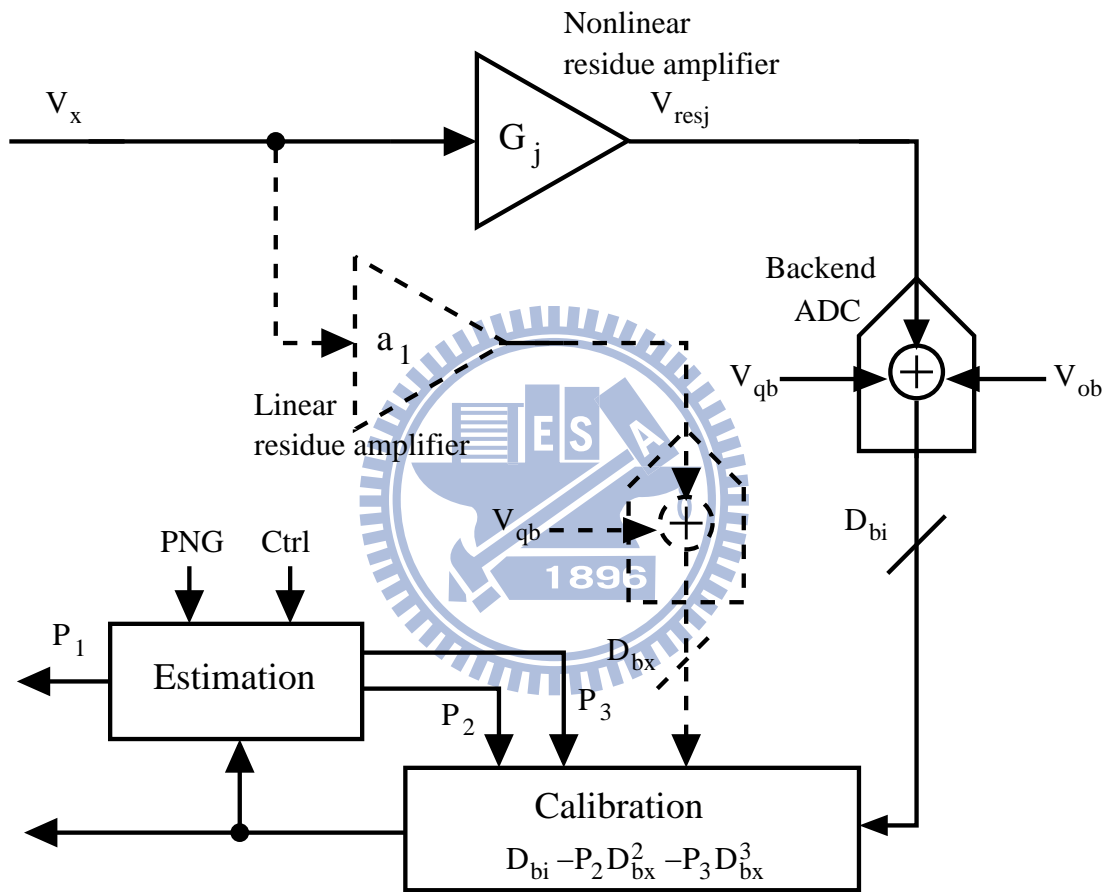
Figure 7.3: Equivalent model of the calibration scheme for multiple-order nonlinear terms.

becomes zero. As a result,

$$D_{bi} = A_1(-N_{qa} - R_i N_{di}) + A_2(N_{qa}^2 + 2N_{qa}R_i N_{di} + N_{di}^2) + N_{qb} + N_{ob}. \qquad (7.15)$$

To find the estimation of the 2nd-order nonlinear term of the residue amplifier, we seek a result that is directly proportional to A_2. By (7.14), the terms contained with A_1 and A_2 are all proportional to N_{di}. If we still take the correlations of R_i and D_{bi}, the estimation of the 2nd-order nonlinear term by MCE method is hard to find. Fortunately, observing (7.15), there's a term in the expansion of A_2 which is directly proportional to N_{di}^2. Therefore, we can take the expected value of D_{bi}

$$E[D_{bi}] = A_1(-N_{qa}) + A_2(N_{qa}^2 + N_{di}^2) + N_{qb} + N_{ob}. \qquad (7.16)$$

As a result, it's obvious that the estimate of the 2nd-order nonlinear term can be easily found by

$$\varepsilon_2 \equiv E[D_{b2}] - E[D_{b1}] = -\frac{3}{4}N_{d1}^2 A_2 = -\frac{3}{4}N_{d1}^2 A_1^2(P_{2,opt} - P_2). \qquad (7.17)$$

After the 3rd-order and the 2nd-order nonlinear terms are all removed, the estimation of linear gain error is given by (5.5) as well.

7.2.1 Discussion

The estimation of the $(2m - 2)$-order nonlinear term is

$$\varepsilon_{2m-2} \equiv \sum_{i=1}^{m-1} C_{ei}(E[D_{bi+1}] - E[D_{bi}]), \qquad (7.18)$$

where C_{ei} are the corresponding coefficients of the MCE method for the estimation of the even-order nonlinear terms.

Any other even-order nonlinear term estimation of the residue amplifier can be derived in a similar way. Table 7.2 summarizes the coefficients C_{ei} of the MCE method for the even-order nonlinear term estimation when the ratios of the calibration signals are geometric series of 2.

Table 7.2: Coefficients C_{ei} of the MCE method for the estimation of the even-order nonliner terms if the ratios of the calibration signals are geometric series of 2.

$(2m-2)$-order	2nd-order	4th-order	6th-order
m	2	3	4
$\varepsilon_{(2m-2)}$	$-\frac{3}{4}N_{d1}^2 A_2$	$-\frac{45}{64}N_{d1}^4 A_4$	$-\frac{2835}{4096}N_{d1}^6 A_6$
C_{e1}	$(-1)^0$	$(-1)^0$	$(-1)^0$
C_{e2}	0	$(-1)^1 \times 2^2$	$(-1)^1 \times 2^2 \times 5$
C_{e3}	0	0	$(-1)^2 \times 2^6$

An important property of this MCE method is that the even-order nonlinear terms doesn't affect the accuracy of the estimation of the odd-order nonlinear term. For instance, if an residue amplifier contains the linear gain error and the 2nd-order to 5th-order nonlinear gain errors, the correlation of R_i and D_{bi} will be

$$
\begin{aligned}
E[R_i D_{bi}] =& A_1(-N_{di}) + A_2(2N_{qa}N_{di}) + A_3(-3N_{qa}^2 N_{di} - N_{di}^3) + A_4(4N_{qa}^3 N_{di} \\
& +4N_{qa}N_{di}^3) + A_5(-5N_{qa}^4 N_{di} - 10N_{qa}^2 N_{di}^3 - N_{di}^5).
\end{aligned}
\tag{7.19}
$$

To derive ε_5, we can expect that the unbiased estimation result is proportional to a scalar times $A_5 N_{di}^5$. That is, the terms with N_{di}^z in (7.19) where $z < 5$ will be cancelled by the MCE method. From (7.19), it's obvious that the term related to A_2 is proportional to N_{di} and the terms relative to A_4 are N_{di} and N_{di}^3. The order of these terms are all lower than 5 and all of them can be cancelled by the MCE method. Therefore, the 2nd-order and the 4th-order nonlinear terms do not affect the estimation of the 5th-order nonlinear term.

In general, if we focus on deriving the unbiased estimation ε_{2m-1}, the correlations of R_i and the even-order nonlinear term only contain terms with N_{di}^z, where $z < 2m - 1$. These terms can be eliminated by the MCE process. As a result, the even-order nonlinear terms have no impact on the accuracy of the estimation of the odd-order nonlinear terms. In other words, the coefficients C_{oi} of the MCE method for estimating odd-order nonlinear term remain the same even though we take the even-order nonlinear terms into account.

7.3   LMS Loop Analysis

We use an example in which the residue amplifier's transfer function contains a 2nd-order and a 5th-order term to demonstrate how to employ the LMS algorithm to update correction parameters P_5 and P_2. Based on the LSM algorithm, two recursions are constructed with respect to ε_5 and ε_2.

$$
\begin{aligned}
P_5(k+1) &= P_5(k) - \mu_5 \varepsilon_5 \\
&= P_5(k) + \mu_5 \frac{45}{64} N_{d1}^5 A_1^5 (P_{5,opt} - P_5) \\
&= P_5(k) + 2\mu_5 (P_{5,opt} - P_5) \frac{45}{128} N_{d1}^5 A_1^5
\end{aligned}
\tag{7.20}
$$

$$
\begin{aligned}
P_2(k+1) &= P_2(k) - \mu_2 \varepsilon_2 \\
&= P_2(k) + \mu_2 \frac{3}{4} N_{d1}^2 A_1^2 (P_{2,opt} - P_2) \\
&= P_2(k) + 2\mu_2 (P_{2,opt} - P_2) \frac{3}{8} N_{d1}^2 A_1^2
\end{aligned}
\tag{7.21}
$$

The eigenvalue of the P_5-LMS-loop is $\lambda_5 = \frac{45}{128} N_{d1}^5 A_1^5$ and the eigenvalue of the P_2-LMS-loop is $\lambda_2 = \frac{3}{8} N_{d1}^2 A_1^2$.

7.3.1   Stability and Convergence

The step size can be determined by Eq. (4.29). The criteria,

$$
0 < \mu_5 < \frac{1}{3\lambda_5}
$$
$$
\Rightarrow \quad 0 < \mu_5 < \frac{128}{135 N_{d1}^5 A_1^5},
\tag{7.22}
$$
$$
0 < \mu_2 < \frac{1}{3\lambda_2}
$$
$$
\Rightarrow \quad 0 < \mu_2 < \frac{8}{9 N_{d1}^2 A_1^2},
\tag{7.23}
$$

ensure the two LMS loops to be convergent and stable.
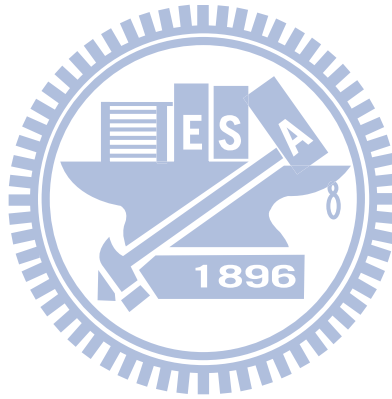
7.3.2 Time Constant

Recall (4.25), the time constants of the two LMS loops are

$$\tau_5 \quad \cong \quad \frac{1}{2\mu_5\lambda_5} = \frac{64}{45\mu_5 N_{d1}^5 A_1^5}, \tag{7.24}$$

$$\tau_2 \quad \cong \quad \frac{1}{2\mu_2\lambda_2} = \frac{4}{3\mu_2 N_{d1}^2 A_1^2}, \tag{7.25}$$

respectively.

The following chapter will give behavioral simulation results of the proposed MCE-based nonlinear-term estimating scheme.

Chapter 8

SIMULATION RESULTS

8.1 Simulation Results of the Proposed MCE Method for Estimating Multiple-Odd-Order Nonlinear Terms of the Residue Amplifiers

8.1.1 Simulation Setup

We build a behavioral model of an example ADC to validate the propose scheme. This example is a 14-bit 100MS/s pipelined ADC formed by a (3+1)-bit pipeline stage and then followed by an ideal 11-bit backend ADC. Hence, the ADC has a resolution of 14 bits. The first pipeline stage of the ADC has 1-bit redundancy for the injection of the random sequences. In this section, we aim at verifying the estimation of multiple-odd-order nonlinear terms. As a result, the residue amplifier in the first pipeline stage is modeled to have the linear gain error, the 3rd-order and the 5th-order nonlinear terms. Table 8.1 summarizes the associated values of the design parameters. With the value

Table 8.1: Open-loop residue amplifier parameters.

Parameter	Description	Value
FS	Full scale range	1.2V
a_1	linear gain error	7.6
a_3	3rd-order nonlinear gain error	-142.2
a_5	5th-order nonlinear gain error	-126420

listed in the table, a polynomial expression of the residue amplifier's transfer function is

$$G_j(v_x) = 7.6(v_x) - 142.2(v_x)^3 - 126420(v_x)^5. \tag{8.1}$$

The optimal correction parameters for this example are $P_{1,opt} = 7.6$, $P_{5,opt} = -0.467$, $P_{5,opt} = -10$.

8.1.2 Simulated ADC Performance

Figure 8.1 and 8.2 compare the INL plots of the ADC without and with calibration, respectively. By activating the calibration, the INL values improve from +165.50/-166.25 LSB to +0.66/-0.50 LSB. Figure 8.3 and 8.4 show the DNL plots of the ADC without and with calibration, respectively. After calibration, the DNL values improve from +11.61/-1.00 LSB to +0.55/-0.59 LSB. In addition, the original missing codes are successfully corrected after calibration. Figure 8.5 shows the INL plot and the DNL plot after calibration in detail.

Figure 8.6 and 8.7 show the output spectra of the ADC at an input frequency around 10 MHz. The SNDR improves from 31.2 dB to 80.4 dB and the SFDR improves from 45.2 dBc to 94.7 dBc. The ENOB improves from 4.9 bits to 13.1 bits.

Table 8.2 summarizes the ADC performance without/with calibration. It verifies the proposed calibration scheme achieves a great improvement on ADC performance.

Table 8.2: ADC performance.

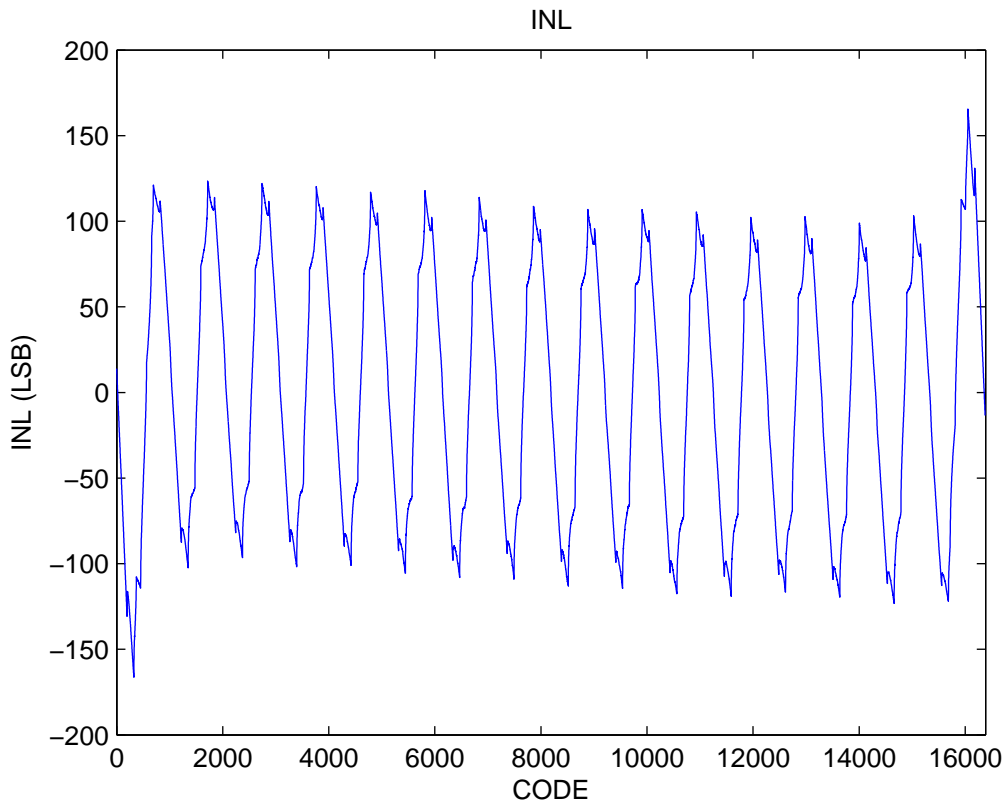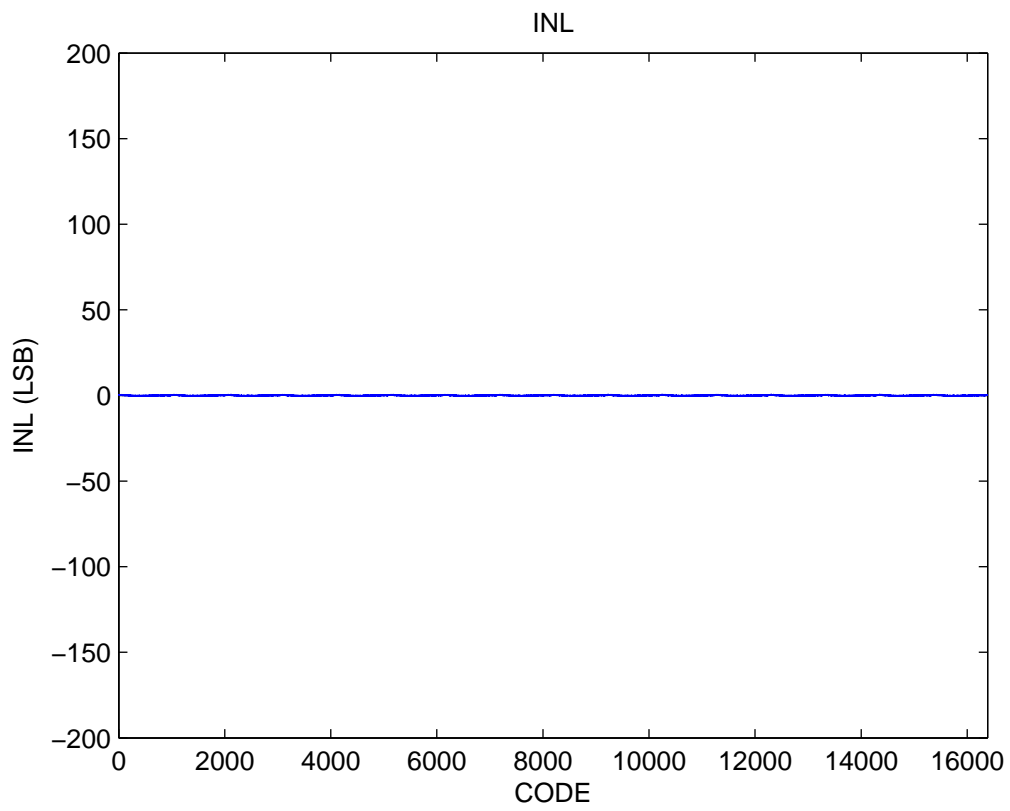| Performance metrics	Without calibration	With calibration
INL (LSB)	+165.50/-166.25	+0.66/-0.50
DNL (LSB)	+11.61/-1.00	+0.55/-0.59
SFDR (dBc)	45.2	94.7
SNDR (dB)	31.2	80.4
ENOB (bits)	4.9	13.1

Figure 8.1: INL without calibration.
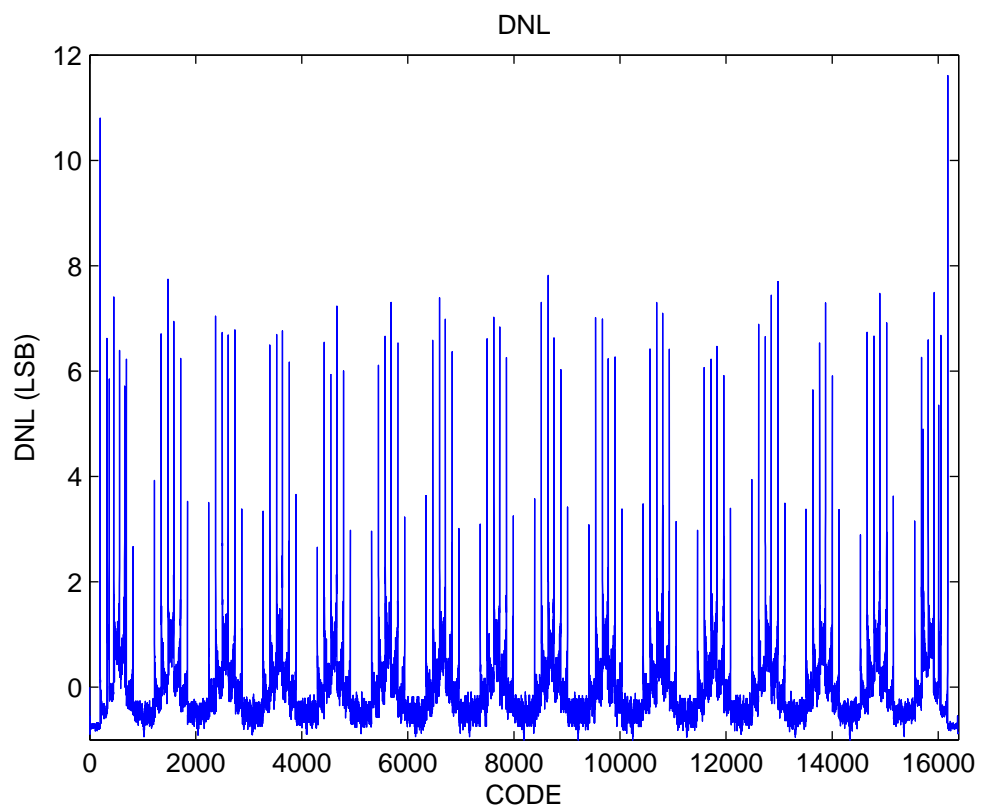
Figure 8.2: INL with calibration.
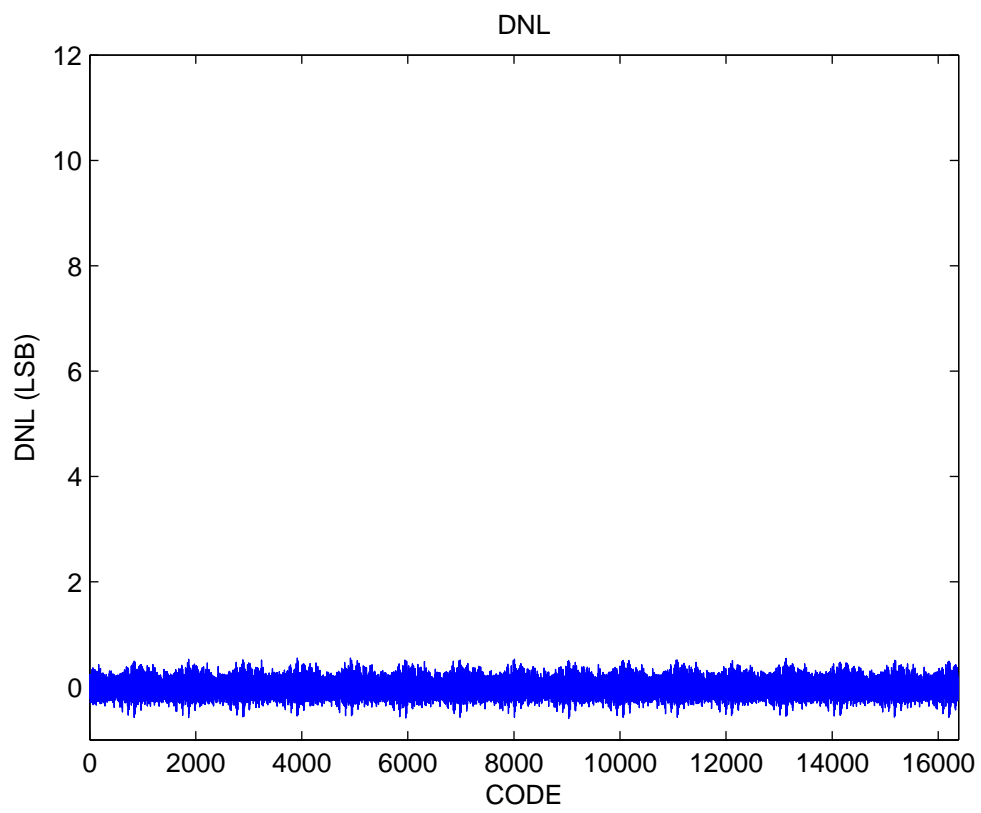
Figure 8.3: DNL without calibration.

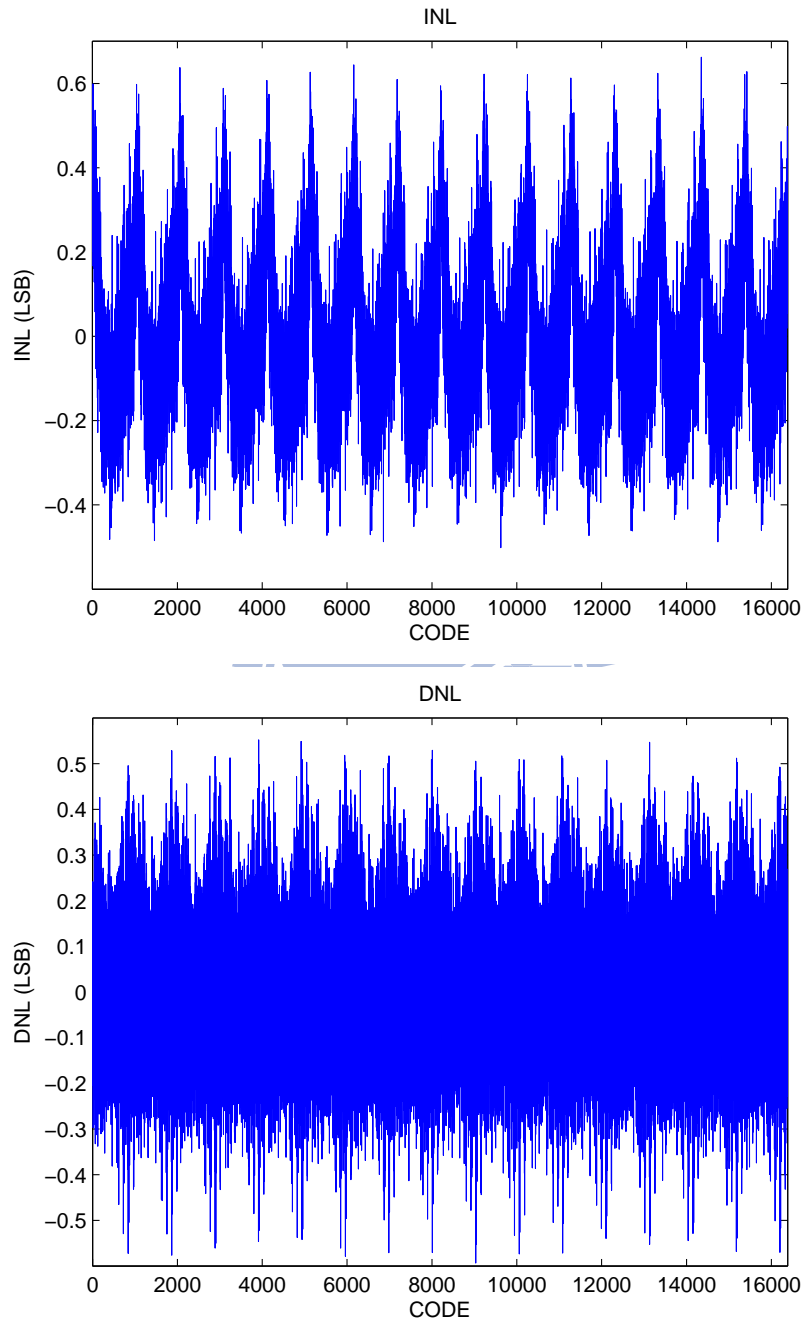Figure 8.4: DNL with calibration.

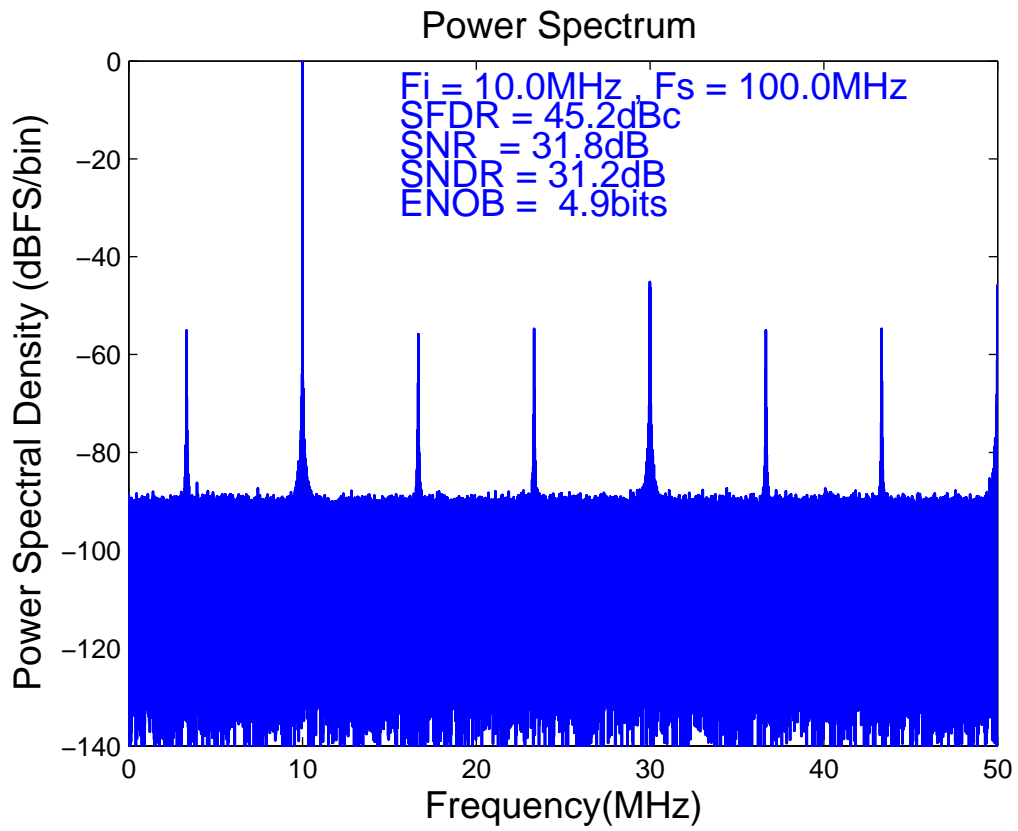Figure 8.5: INL and DNL with calibration.
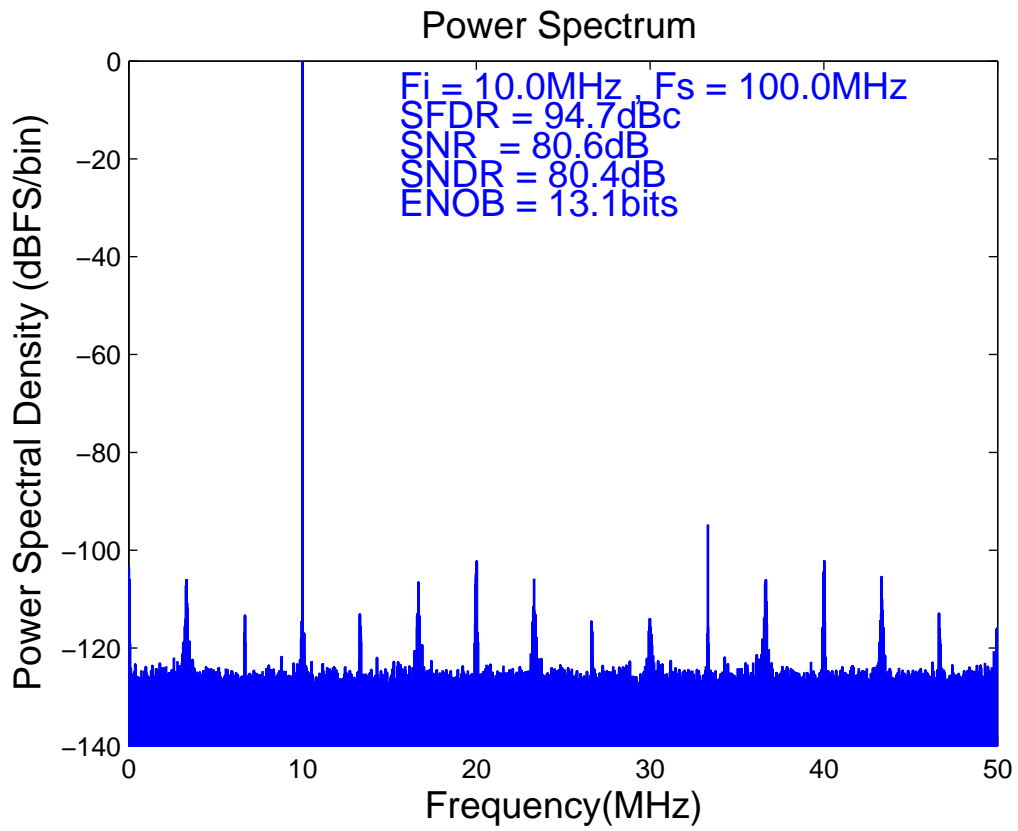
Figure 8.6: FFT without calibration.

Figure 8.7: FFT with calibration.

8.1.3 LMS Loop Convergence

The convergence of the correction parameters, P_1, P_3, P_5, are illustrated in Fig. 8.8, 8.9 and 8.10, respectively. The input signal is a full-scaled sinusoid. With the discussion of the stability and the time constant of the LMS loops in chapter 7, the ranges of the step sizes for the LMS loops to be stable are

$$0 < \mu_1 < 21, \tag{8.2}$$

$$0 < \mu_3 < 66, \tag{8.3}$$

$$0 < \mu_5 < 2688. \tag{8.4}$$

The step sizes are chosen to be $\mu_1 = 0.05$, $\mu_3 = 0.125$ and $\mu_5 = 32$. First, we set the step size μ_5 to make the time constant τ_5 between 50 to 150 iterations. Because the three LMS loops converge simultaneously, we should set the time constants of the low-order ones τ_1, τ_3, to be larger than the value of τ_5; otherwise, they will underdamp.
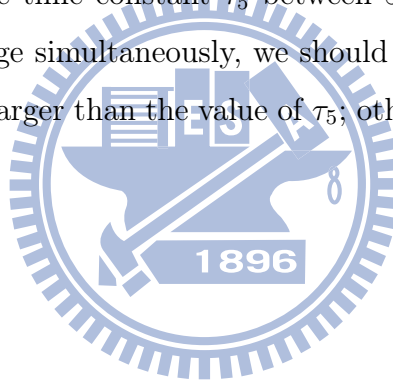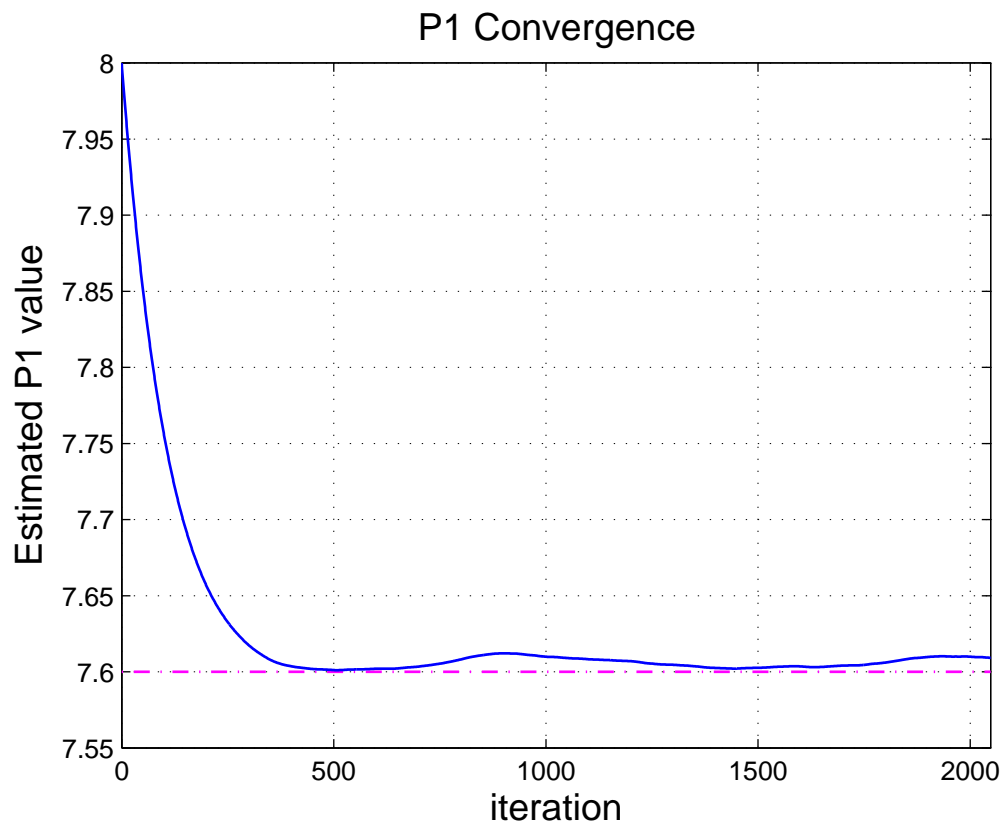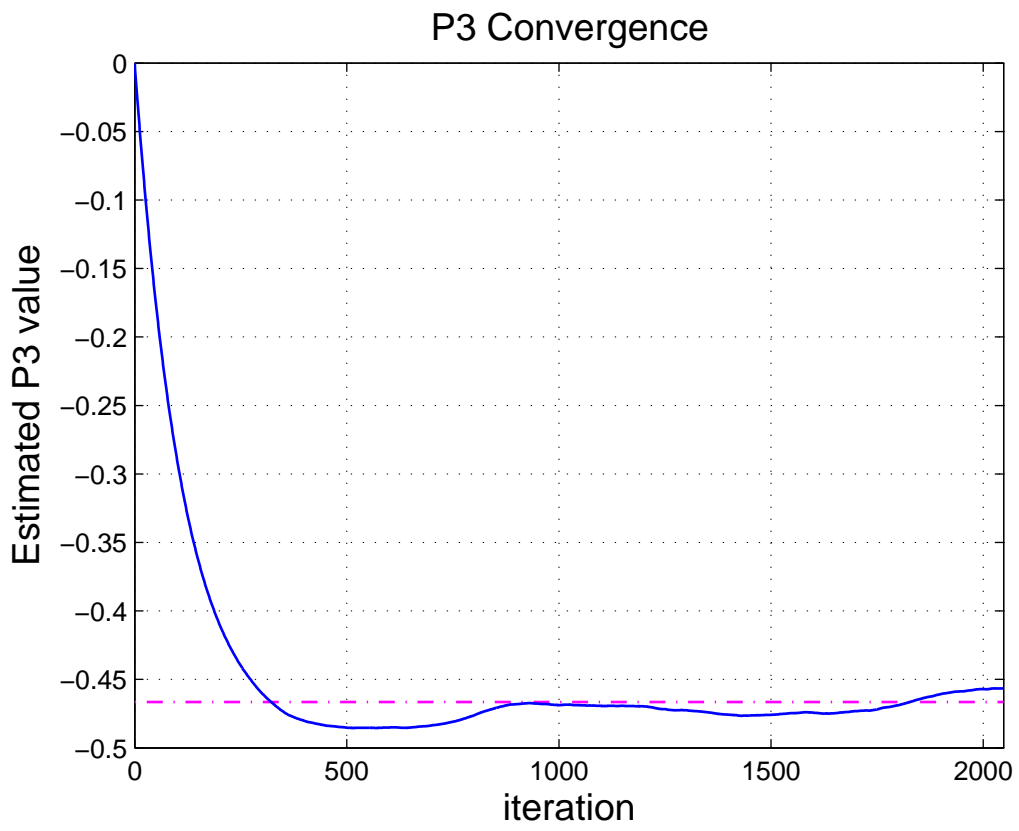
Figure 8.8: P1 convergence.
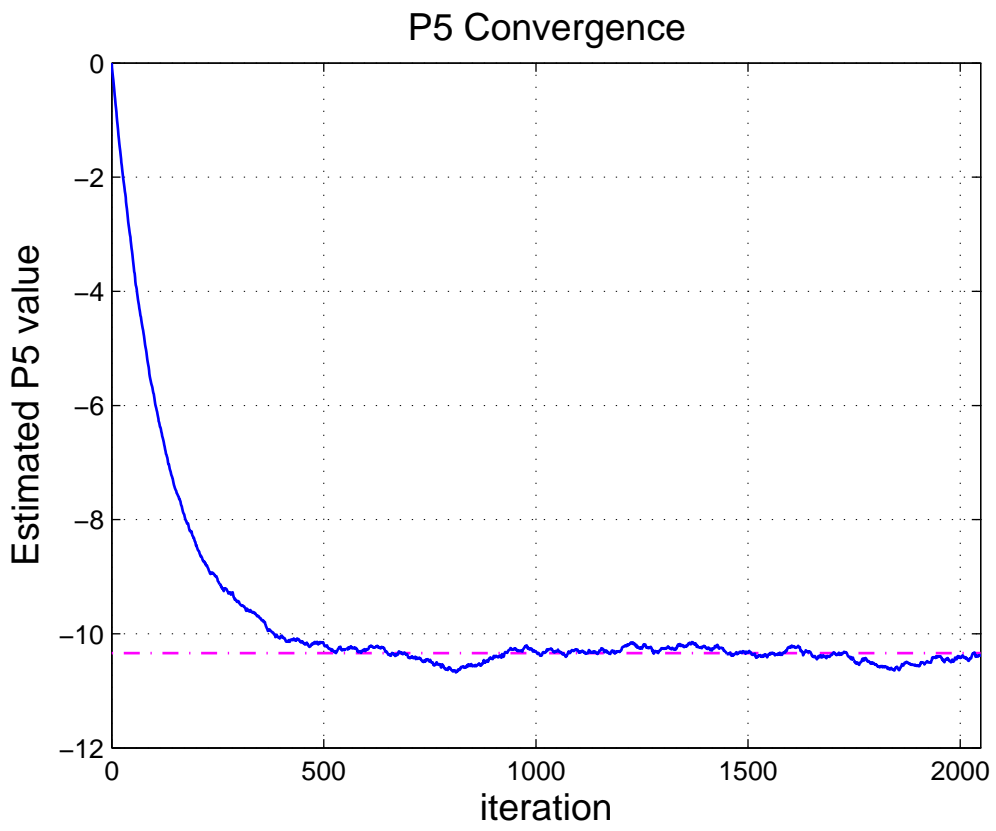
Figure 8.9: P3 convergence.

Figure 8.10: P5 convergence.

8.2 Simulation Results of the Proposed MCE Method for Estimating Multiple-Order Nonlinear Terms of the Residue Amplifiers

8.2.1 Simulation Setup

In this section we use the same pipelined ADC example as described in the previous section but with a different transfer function of the residue amplifier to validate the proposed MCE method for multiple-order nonlinear terms. Table 8.3 summarizes the associated parameters of the nonlinear residue amplifier in the first pipeline stage. With the values listed in the table, the corresponding residue amplifier model is

$$G_j(v_x) = 7.6(v_x) - 7.47(v_x)^2 - 142.2(v_x)^3. \tag{8.5}$$

Consequently, the optimal correction parameters are $P_{1,opt} = 7.6$, $P_{2,opt} = -0.155$, $P_{3,opt} = -0.467$.

Table 8.3: Open-loop residue amplifier parameters.

Parameter	Description	Value
FS	Full scale range	1.2V
a_1	Linear gain with error	7.6
a_2	2nd-order nonlinear gain error	-7.47
a_3	3rd-order nonlinear gain error	-142.2

8.2.2 Simulated ADC Performance

Figure 8.11, 8.12, 8.13 and 8.14 show the INL plots and the DNL plots of the ADC without and with calibration, respectively. The proposed calibration scheme significantly improves the INL values from +89.97/-55.81 LSB to +0.46/-0.49 LSB and the DNL values from +6.13/-1.00 LSB to +0.46/-0.73 LSB. Furthermore, the original missing codes are successfully corrected after calibration. Figure 8.15 shows the INL plot and the DNL plot after calibration in detail.

Figure 8.16 and 8.17 show the output spectra of the ADC with a 10MHz input before
and after calibration, respectively. It clearly illustrates the great improvement on the
ADC's performance afforded with calibration. The SNDR improves from 40.1 dB to
85.5 dB and the SFDR improves from 54.5 dBc to 123.5 dBc. The ENOB improves
from 6.4 bits to 13.9 bits.

Table 8.4 summarizes the ADC performance without/with calibration. From the
table, we see a great improvement on ADC performance after calibration.

Table 8.4: ADC performance.

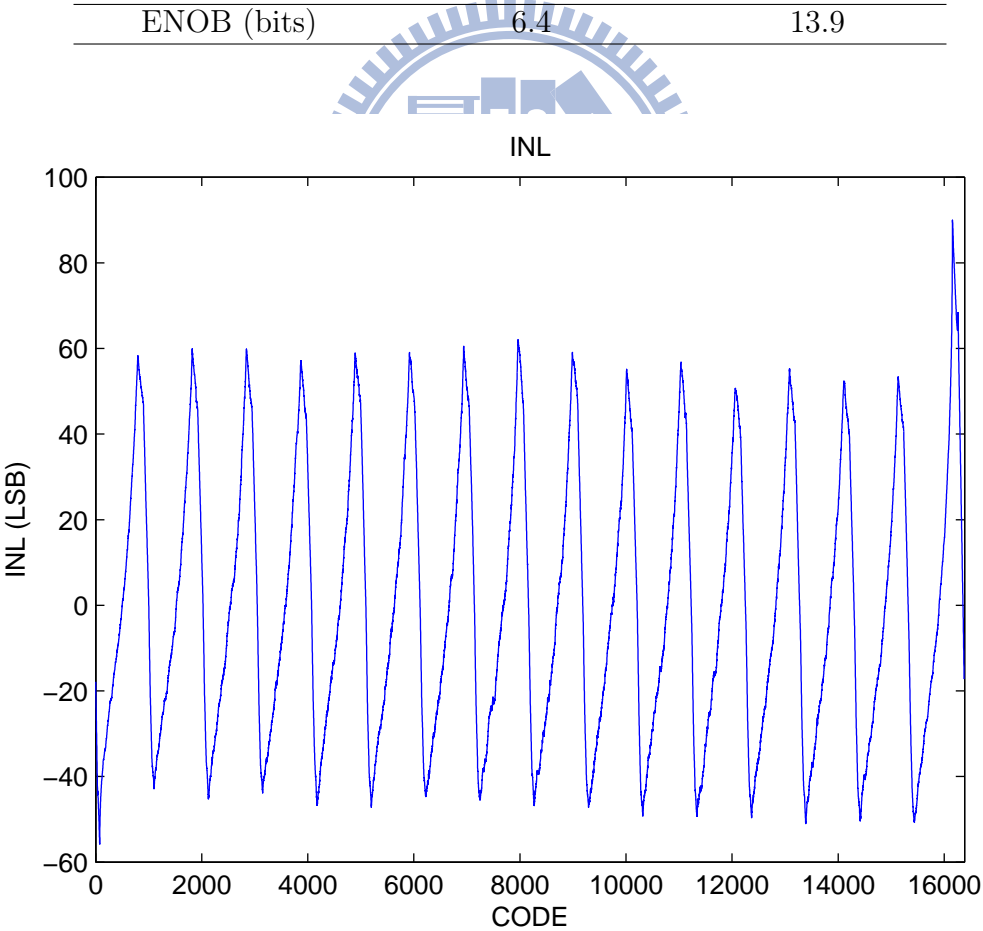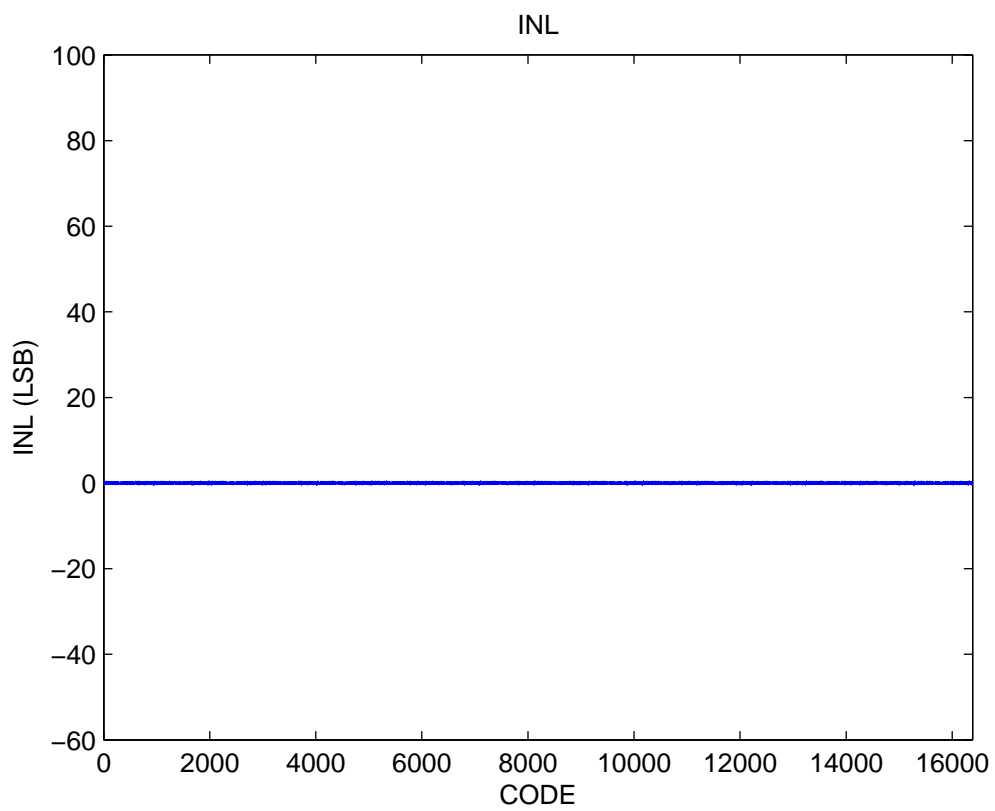| Performance metrics	Without calibration	With calibration
INL (LSB)	+89.97/-55.81	+0.46/-0.49
DNL (LSB)	+6.13/-1.00	+0.46/-0.73
SFDR (dBc)	54.5	123.5
SNDR (dB)	40.1	85.5
ENOB (bits)	6.4	13.9

Figure 8.11: INL without calibration.
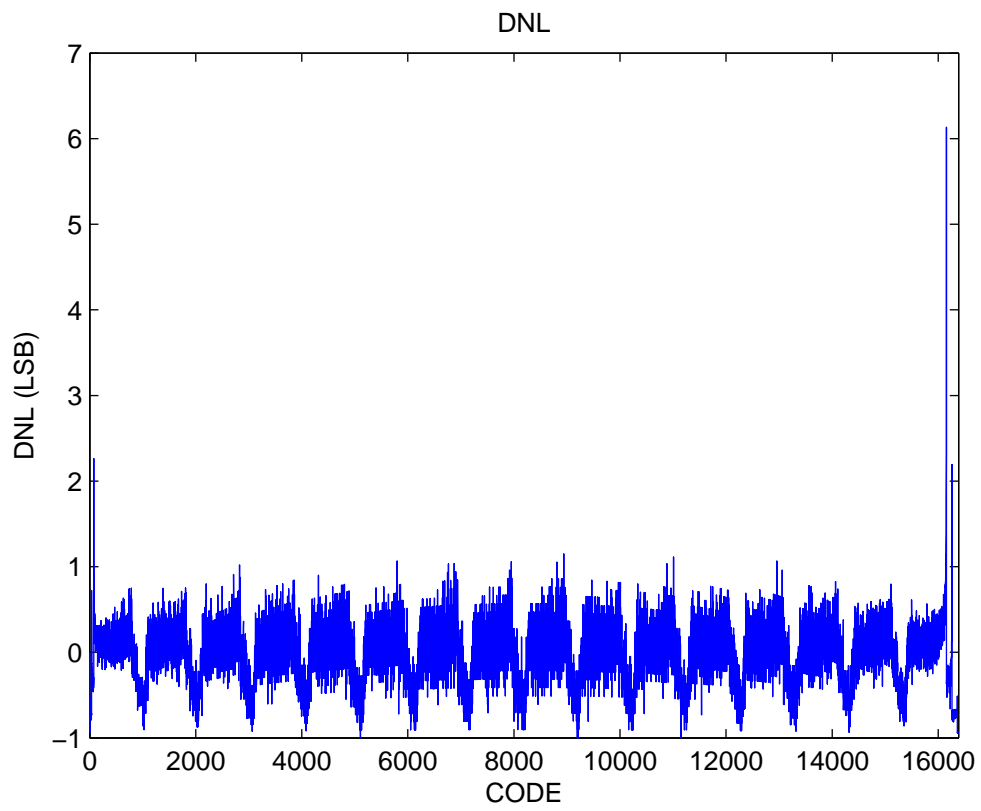
Figure 8.12: INL with calibration.

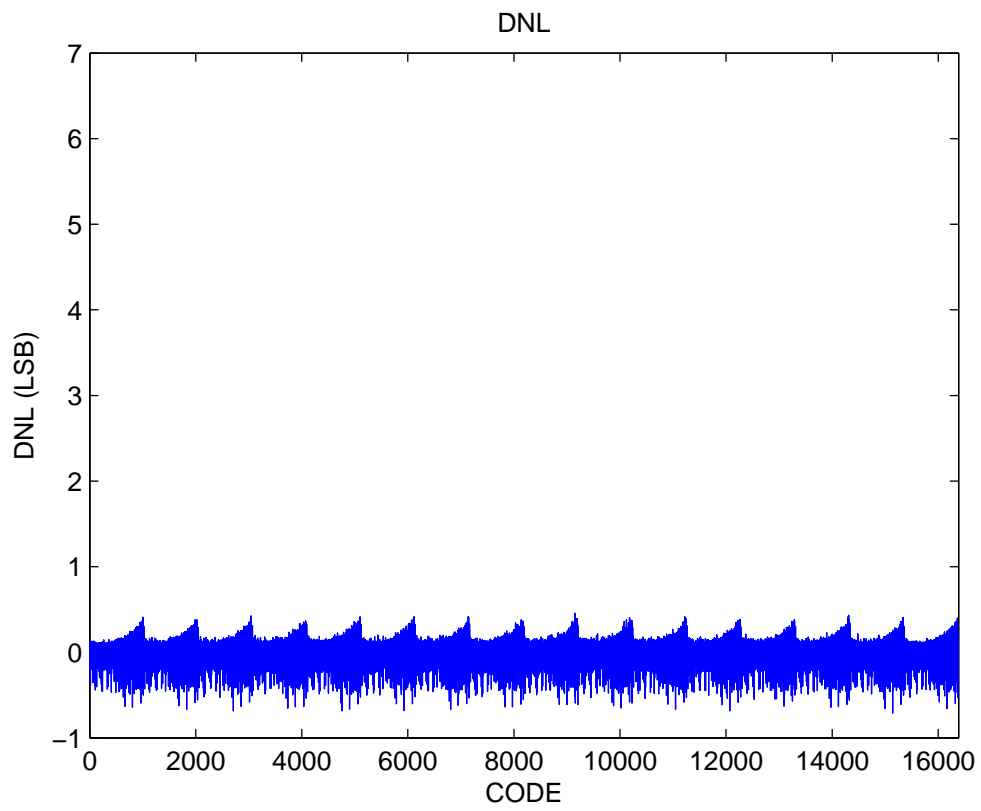Figure 8.13: DNL without calibration.

Figure 8.14: DNL with calibration.
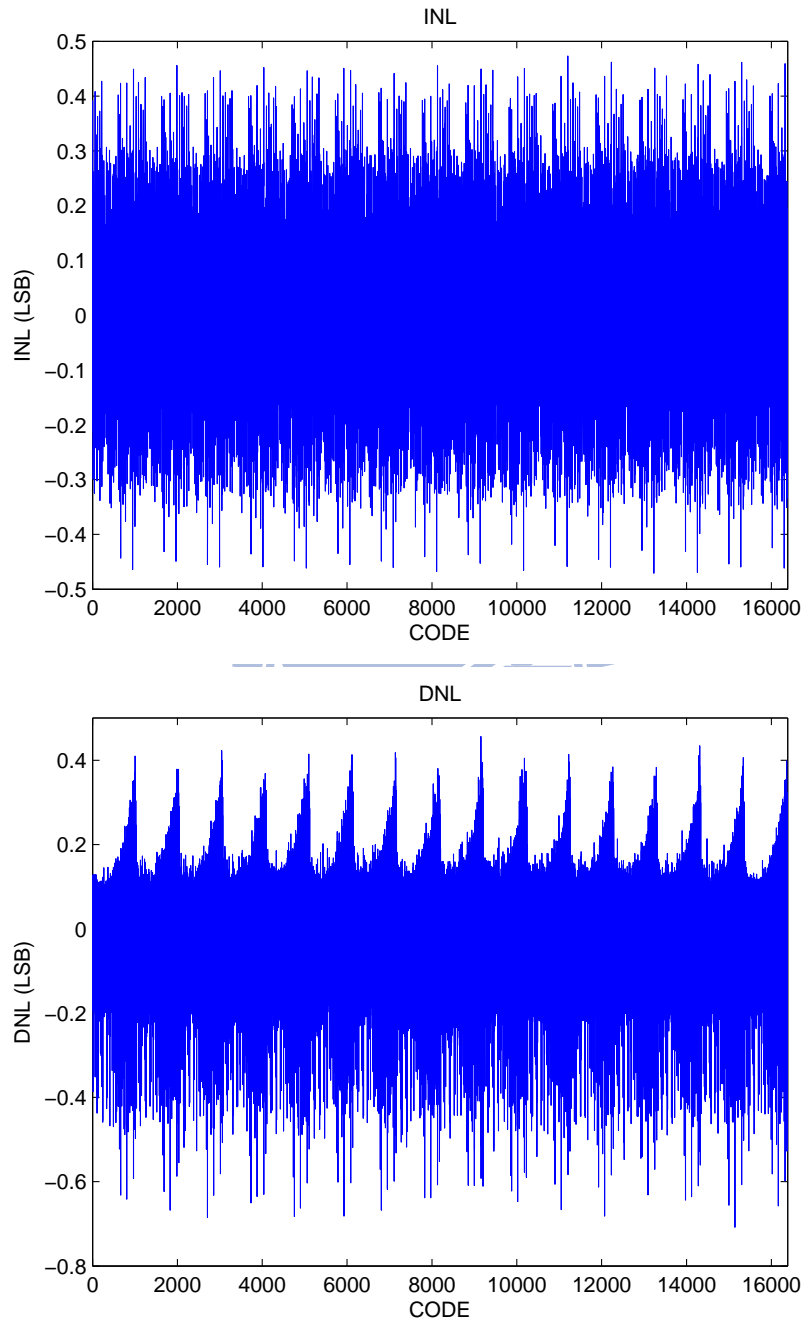
Figure 8.15: INL and DNL with calibration.
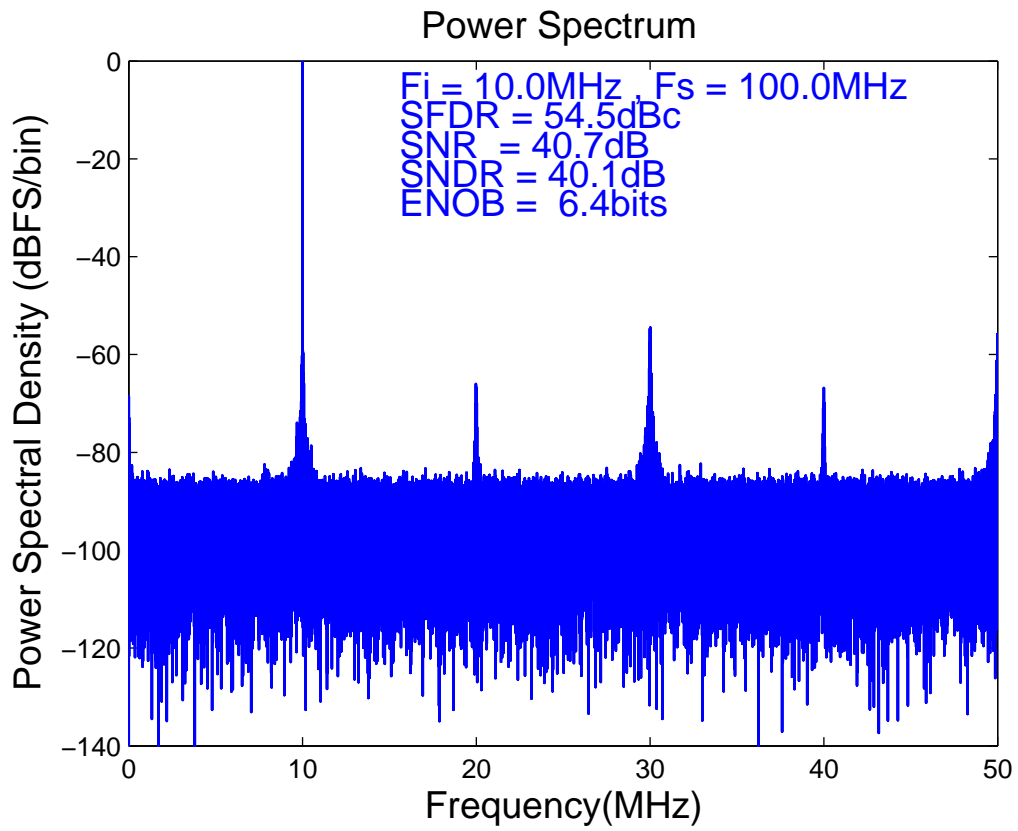
Figure 8.16: FFT without calibration.
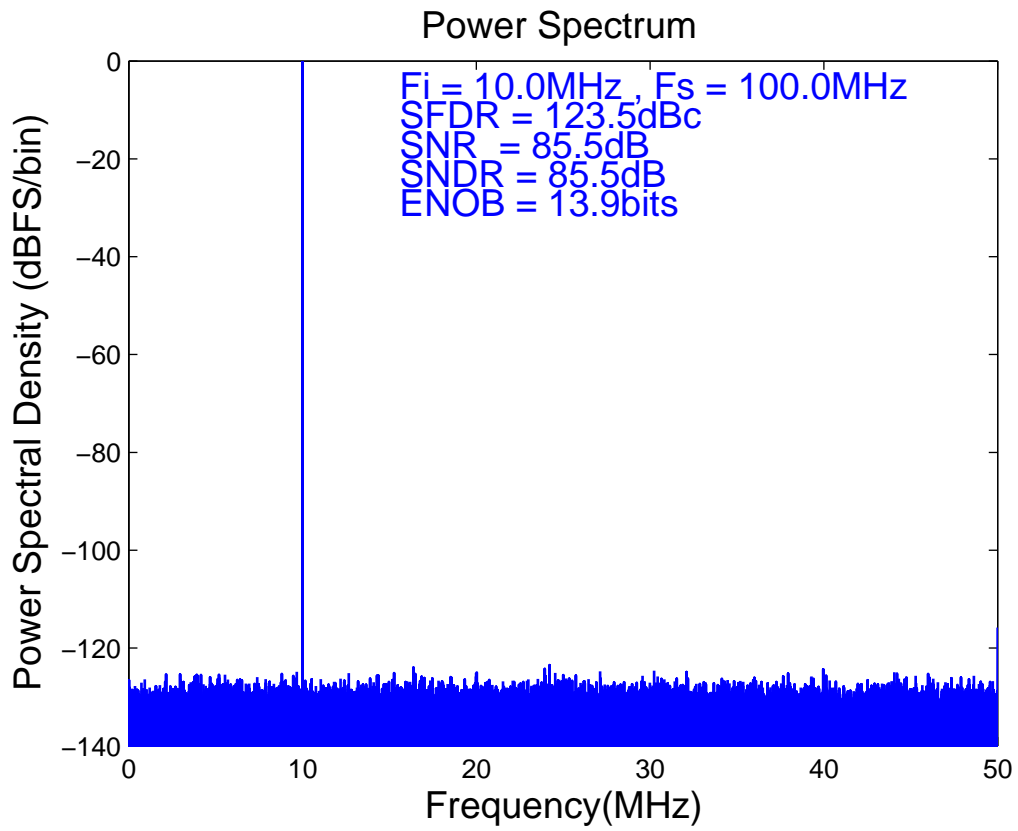
Figure 8.17: FFT with calibration.

8.2.3   LMS Loop Convergence

Figure 8.18, 8.19 and 8.20 show the correction parameter convergence plots of P_1, P_2 and P_3. The input signal is a full-scaled sinusoid. The range of the step sizes for the LMS loops to be stable are

$$0 < \mu_1 < 21, \tag{8.6}$$

$$0 < \mu_2 < 15, \tag{8.7}$$

$$0 < \mu_3 < 66. \tag{8.8}$$

The step sizes are determined by a similar consideration as mentioned in the previous section. Finally, the values of the step sizes are set to be $\mu_1 = 0.25$, $\mu_2 = 0.3125$, $\mu_3 = 1.5$.

Figure 8.18: P1 convergence.
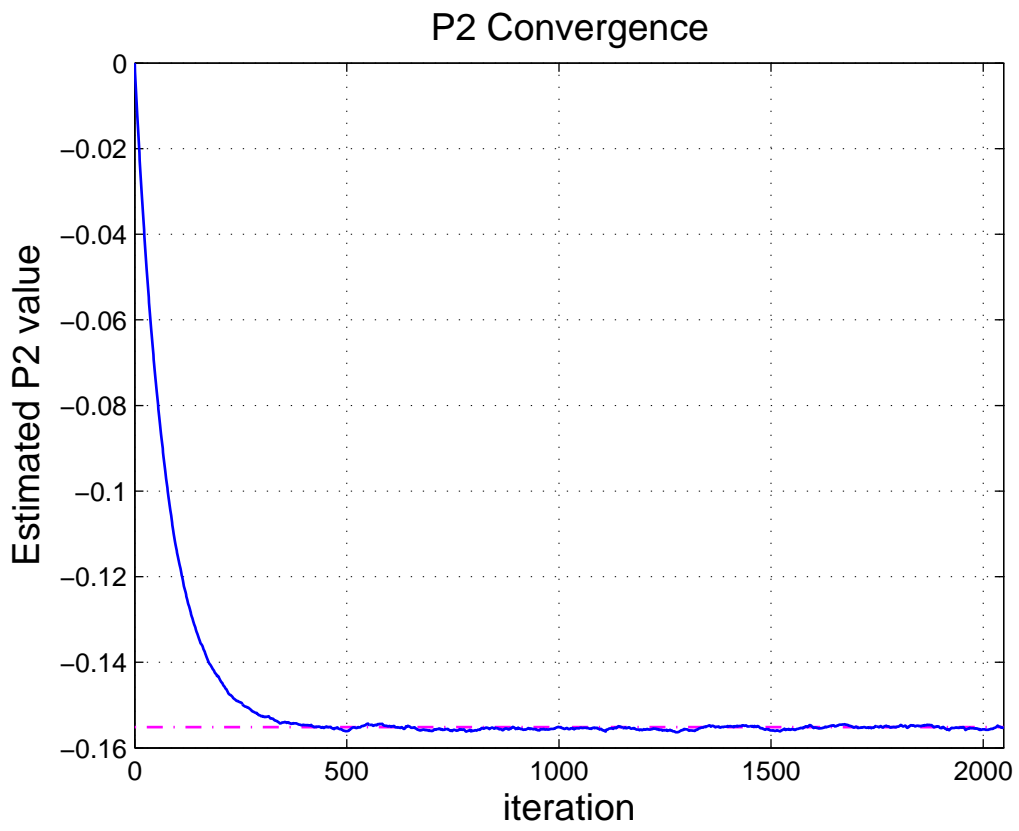
Figure 8.19: P2 convergence.
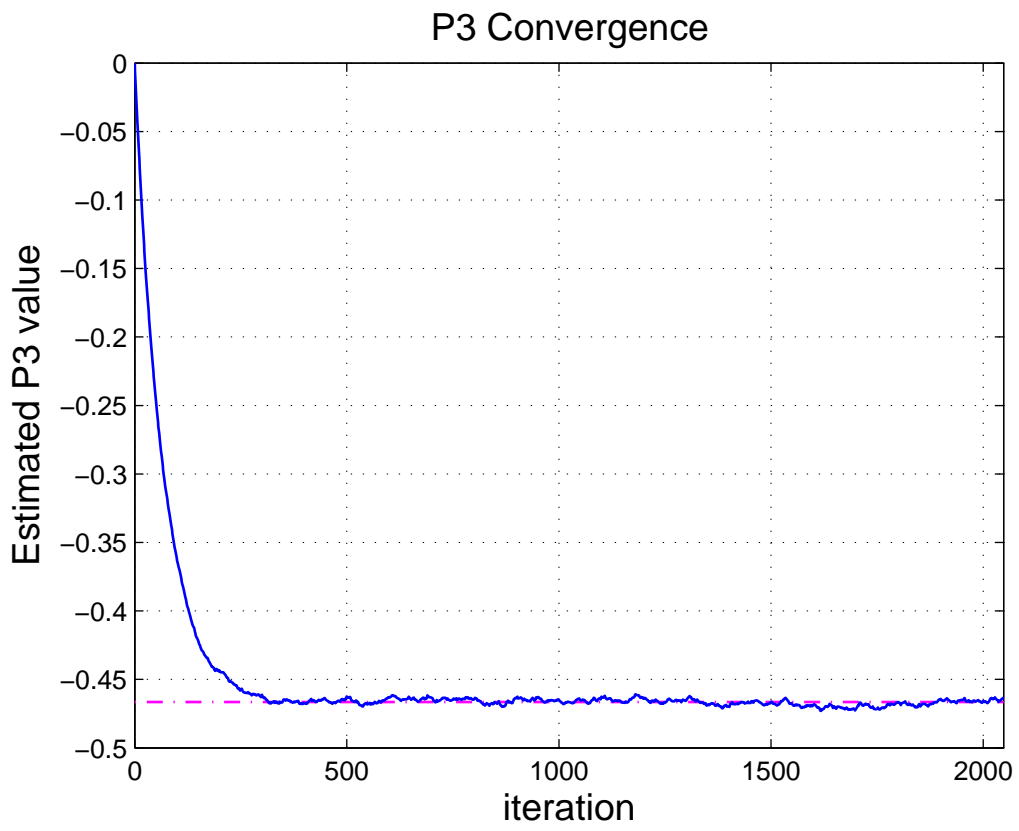
Figure 8.20: P3 convergence.

Chapter 9

CONCLUSION AND FUTURE WORKS

9.1 Conclusion

The performance of the pipelined ADC is limited by the accuracy of the linear gain and the nonlinearity of the residue amplifier. In order to have high performance, the pipelined ADC needs to be calibrated. In this thesis, a novel digital background MCE method for estimating multiple-o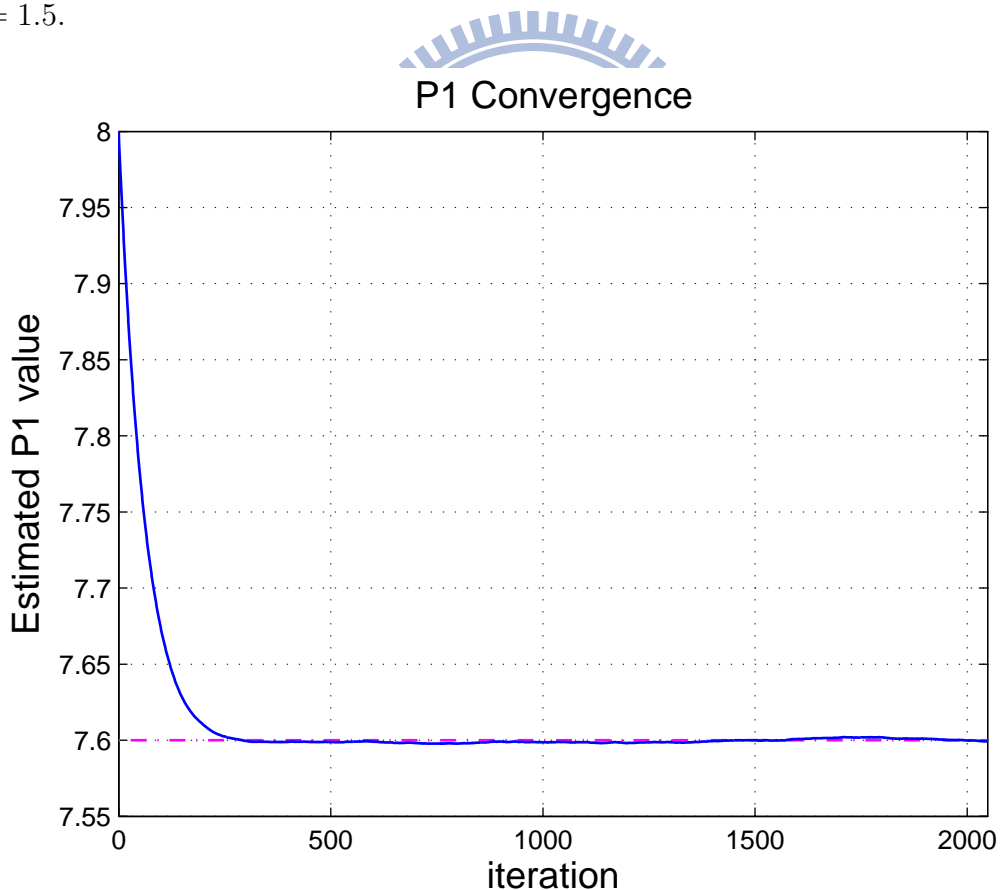rder nonlinear terms of the residue amplifiers in pipelined ADCs is presented. The proposed method can accurately estimate any order nonlinear term of the residue amplifier. Since the accuracy and linearity requirements are alleviated, less complex and lower-power analog circuits can be used. Most hardware overhead is on the digital circuits, whose area and power consumption are small in advanced technology. This feature makes the design of the high-performance ADCs much easier. Compared with the similar digital background estimation techniques discussed previously [3, 28, 5], the proposed algorithm is favorable in many aspects, where they are summarized in Table 9.1.

Table 9.1: Comparison of the estimation techniques

	[3]	[28]	[5]	proposed
Applying static input	fails	fails	works	works
Input statistic dependence	yes	no	no	no
Residue amplifier limitation	no restriction	only suitable for weakly nonlinear	no restriction	no restriction
Nonlinear terms estimation capability	only suitable for 3rd-order	only suitable for 3rd-order	any order	any order
Correction range	limited by analog and digital circuits	limited by analog circuit	limited by analog circuit	theoretical maximum
Multi-stage calibration capability	no	yes	yes	yes
Hardware cost	moderate	large	large	small
Tracking time	$\approx 2^{24}$ cycles	$\approx 2^{20}$ cycles	$\approx 2^{32}$ cycles	$\approx 2^{24}$ cycles

9.2 Future Works

In this thesis, the MCE algorithm [2] is implemented on an external FPGA using Verilog HDL. An obvious future work is SoC that integrates the digital calibration processor and the pipelined ADC on a single chip. The offset of the backend ADC must be address because the inverse function can not tolerate it.

Second, exploring a more efficient estimation method that has less dependence on the ratio of the calibration signals may be a future research topic.

Other opportunities exist in developing a novel calibration scheme. Although there're many researches focus on digital background calibration scheme for pipelined ADC, they usually only concern the estimation of the linear and the nonlinear coefficients of the residue amplifier. However, how to cancel the obtained nonlinear terms is another important issue. Except for directly using an inverse function [3], most calibration techniques use the backend ADC's digital output as an approximation of the linear term of the residue amplifier [5, 18, 28, 47]. They use the backend ADC's digital output to gen-

erate an approximation of the nonlinear errors of the residue amplifier and then cancel it from the pipelined ADC's primary digital output. This kind of calibration schemes inject some additional error terms due to the nonlinearity of the residue amplifier. As a result, the correction range of the nonlinearity may be significantly limited.

APPENDIX A

Derive the calibration Eq. (3.20):

$$4cos^3\phi - 3cos\phi = cos3\phi$$

Let $cos3\phi = C$

then $4cos^3\phi - 3cos\phi = C$ \hfill $(A.1)$

$$cos3\phi = C$$

$$\Rightarrow \quad \phi = \frac{1}{3}cos^{-1}C \hfill (A.2)$$

$$a_1v_x + a_3v_x^3 = D_bv_{ref}$$

$$\Rightarrow \quad a_1\frac{v_x}{v_{ref}} + a_3v_{ref}^2\left(\frac{v_x}{v_{ref}}\right)^3 = D_b$$

Let $\dfrac{v_x}{v_{ref}} = X = Rcos\theta$; $A_1 = a_1$; $A_3 = a_3v_{ref}^2$

$$A_1X + A_3X^3 = D_b$$

$$\Rightarrow \quad A_1Rcos\theta + A_3(Rcos\theta)^3 = D_b$$

$$\Rightarrow \quad 3\left(\frac{A_1}{3}\right)cos\theta + (-4)\left(\frac{A_3}{-4}\right)R^2cos^3\theta = \frac{D_b}{R}$$

$$\Rightarrow \quad 3cos\theta + (-4)\left(\frac{3A_3}{-4A_1}\right)R^2cos^3\theta = \frac{D_b}{\frac{A_1}{3}R}$$

Let $R^2 = \dfrac{-4A_1}{3A_3} \Rightarrow R = \sqrt{\dfrac{-4A_1}{3A_3}}$

$$\Rightarrow \quad 4cos^3\theta - 3cos\theta = \frac{-D_b}{\frac{A_1}{3}\sqrt{\frac{-4A_1}{3A_3}}} \hfill (A.3)$$

Comparing (A.1) with (A.3), the right hand side of these two equations is only different in the polarity if $C = \dfrac{D_b}{\frac{A_1}{3}\sqrt{\frac{-4A_1}{3A_3}}}$. To modify this difference, let $\theta = \phi + \frac{\pi}{3}$.

$$4cos^3(\phi + \frac{\pi}{3}) - 3cos(\phi + \frac{\pi}{3}) = cos3(\phi + \frac{\pi}{3})$$

$$\Rightarrow \quad 4cos^3(\phi + \frac{\pi}{3}) - 3cos(\phi + \frac{\pi}{3}) = -cos3\phi$$

$$X = Rcos\theta$$

$$\Rightarrow \quad X = Rcos(\phi + \frac{\pi}{3})$$

from equation (A.2)

$$\Rightarrow \quad X = \sqrt{\frac{-4A_1}{3A_3}}cos\left[\frac{\pi}{3} + \frac{1}{3}cos^{-1}\left(\frac{D_b}{\frac{A_1}{3}\sqrt{\frac{-4A_1}{3A_3}}}\right)\right]$$

the linear term :

$$A_1X = A_1\sqrt{\frac{-4A_1}{3A_3}}cos\left[\frac{\pi}{3} + \frac{1}{3}cos^{-1}\left(\frac{D_b}{\frac{A_1}{3}\sqrt{\frac{-4A_1}{3A_3}}}\right)\right]$$

$$\Rightarrow \quad A_1X = 2\sqrt{\frac{-A_1^3}{3A_3}}cos\left[\frac{\pi}{3} + \frac{1}{3}cos^{-1}\left(\frac{D_b}{2\sqrt{\frac{-A_1^3}{27A_3}}}\right)\right]$$

Let $P_3 = \dfrac{A_3}{A_1^3}$

$$\Rightarrow \quad A_1X = 2\sqrt{\frac{-1}{3P_3}}cos\left[\frac{\pi}{3} + \frac{1}{3}cos^{-1}\left(\frac{D_b}{2\sqrt{\frac{-1}{27P_3}}}\right)\right]$$

Consequently, the nonlinear term A_3X^3 can be expressed as:

$$A_3X^3 \;=\; D_b - A_1X$$

$$\Rightarrow A_3X^3 \;=\; D_b - 2\sqrt{\frac{-1}{3P_3}}cos\left[\frac{\pi}{3} + \frac{1}{3}cos^{-1}\left(\frac{D_b}{2\sqrt{\frac{-1}{27P_3}}}\right)\right] \qquad (A.4)$$

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