國立交通大學

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碩士論文

以固定工作週期的控制方式運用在升壓型轉換器以達到減輕右半部平面零點效應

A Right-Half-Plane (RHP) Zero Alleviating Skill in the Solid-Duty-Control (SDC) Boost Converter

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摘　要

本論文提出一個以固定工作周期控制(solid-duty-control)為基礎的切換式升壓轉換器，當負載變化時保持一樣的工作周期，它可以改善傳統切換式升壓轉換器受到系統右半平面零點(right-half-plane zero)影響，而無法有快速暫態響應(transient response)的問題。藉由適當的遲滯空間調變(adaptive hysteresis window)來控制轉換器的開關時間以便在負載變化時得到固定的工作周期。除此之外，基於可變暫態提升(variable transient enhancement)控制器來提升暫態響應。

此固定工作周期控制(solid-duty-control)為基礎的控制技術可提供 LED 被剛系統穩地的輸出。篇論文使用 TSMC 0.25um CMOS 製程技術來進行模擬和製作。經實驗結果顯示，與傳統的電流控制切換式升壓轉換器比較起來，在負載由輕載(50mA)轉為重載(250mA)時，輸出電壓下降變化與穩壓時間較傳統方式分別提升 30 % 和 80 %。

關鍵字：固定工作周期控制(solid-duty-control)，暫態響應(transient response)，右半平面零點(right-half-plane zero)，適當的遲滯空間調變(adaptive hysteresis window)，遲滯空間調變(adaptive hysteresis window)

A Right-Half-Plane (RHP) Zero Alleviating Skill in the Solid-Duty-Control (SDC) Boost Converter

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Abstract

This paper proposes a solid-duty-control (SDC) technique to keep a constant duty value to reduce dip voltage during load transient period. It'll improve the transient response of DC-DC boost converters, which suffer from low bandwidth due to the existence of right-half-plane (RHP) zero. In order to reduce the RHP effect, two controllers are proposed to enhance transient performance. To get contain duty value during load transient period, using adaptive hysteresis window (AHW) modulator control the on-time and off-time of the converter. Besides, due to variable transient enhancement (VTE) controller, the transient response is achieved.

The proposed SDC technique can provide a stable and regulated output for edge-lit LED backlight systems. This converter has been implemented in a 0.25-μm CMOS process. Compared to conventional design without any fast transient technique, experimental results show the undershoot voltage and recovery time are improved about 30 % and 80 % as load current suddenly changes from 50mA to 250mA, respectively.

Keywords—solid-duty-control (SDC), transient response and right-half-plane zero, adaptive hysteresis window, adaptive hysteresis window.

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吳典融

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Chapter 1

Introduction

1.1 Background and Review

Recently the high efficiency, compact system size, and minimal components are increasingly important for today's portable applications. For example, the function of the multimedia in mobile phone is stronger. In particular, the video and audio performances attracted more attention. Due to the demand of decent display, the light emission diode (LED) backlight becomes more popular in today's green power mainstream.

In addition, LED does not contain infrared and ultraviolet rays in its optical spectrum. That is, it only generates minimal heat and harmful radiation making it environmentally friendly. As depicted in Fig. 1, LED lighting systems can be used on large billboards, traffic lights, streetlamps, backlighting devices [1-4], and other similar applications. Furthermore, it is very convenient to control the brightness that depends on the current flowing through LEDs. Recently, automotive electric devices with LED displays have become very popular. Thus, a high efficiency and accuracy LED driving circuit is needed in order to get an accurate control on LED brightness. Generally speaking, one of characteristics that may affect image quality is mainly determined by the backlight uniformity. Therefore, the boost converter is widely utilized for LED.

To make the power supply circuits with small size, high efficiency and better dynamic responses further, integrating some external components in chip to provide a sizable reduction in supply circuit; operate in different controlled modes with relative load current ranges and enable some machines for specific conditions are analyzed in later chapter .

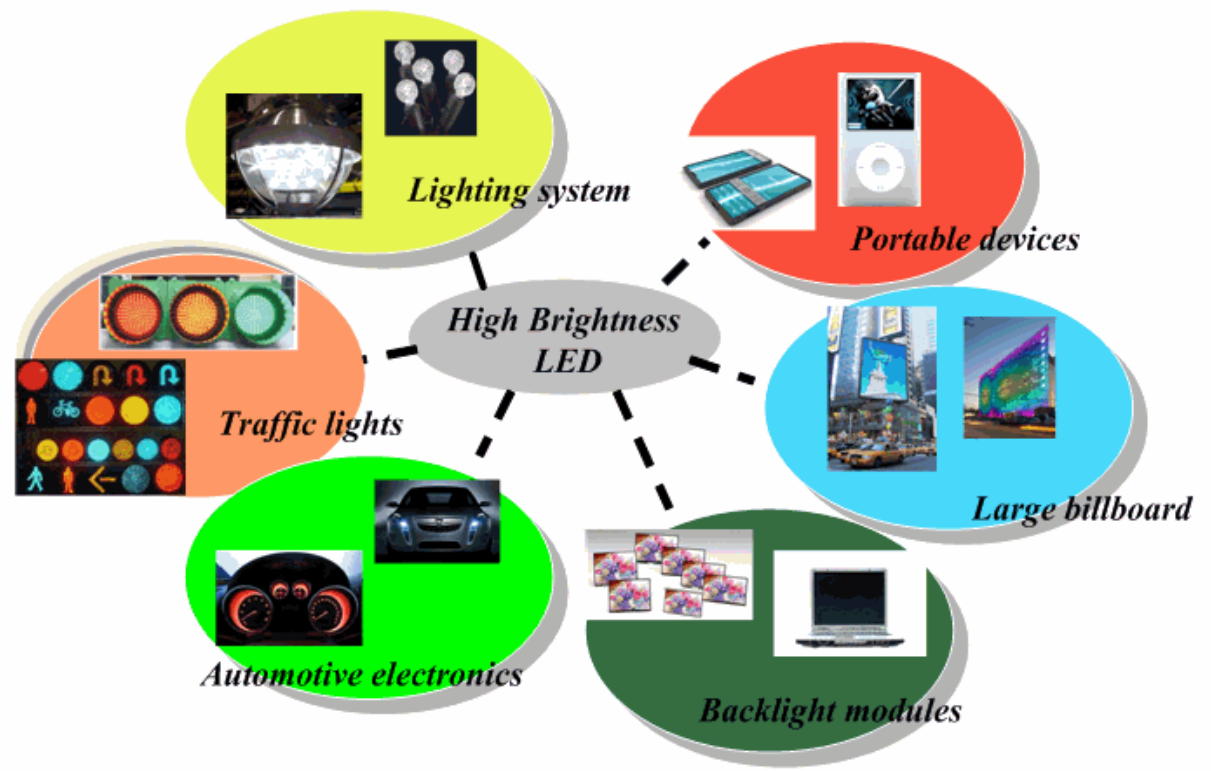


Fig. 1. Application of LED lighting systems.

1.2 Classification of Voltage Regulator

General power supply circuits used in portable applications can be classified into three technologies: linear regulators, switched capacitor circuits, and switching regulators. In the following subsections, these technologies are briefly introduced and described. Finally, a brief comparison will be given about three types of voltage regulators. The comparisons included circuit complexity, cost, efficiency, load ability and so on.

1.2.1 Linear Regulators

Fig. 2 shows the schematic of a linear regulator with a pass transistor operates M_1 used as a variable resistor, which operates linearly to maintain the output according to the value of the reference. It also called low drop-out (LDO) voltage regulator because there is a drop out voltage ($V_{dropout}$) between input and output pin. The linear regulators use a pass device (a

power MOSFET with equivalent resistor (R_{DS})) between the input supply voltage and the regulated output voltage. An error amplifier controls the gate voltage of the pass resistance with respect to a reference voltage. With the error amplifier, it could adopt output voltage information form resistive feedback network (V_{FB}) then compare to reference voltage (V_{REF}). After error amplifier operation, it could immediately adjust input and output difference then control the gate of power MOSFET to supply load current.

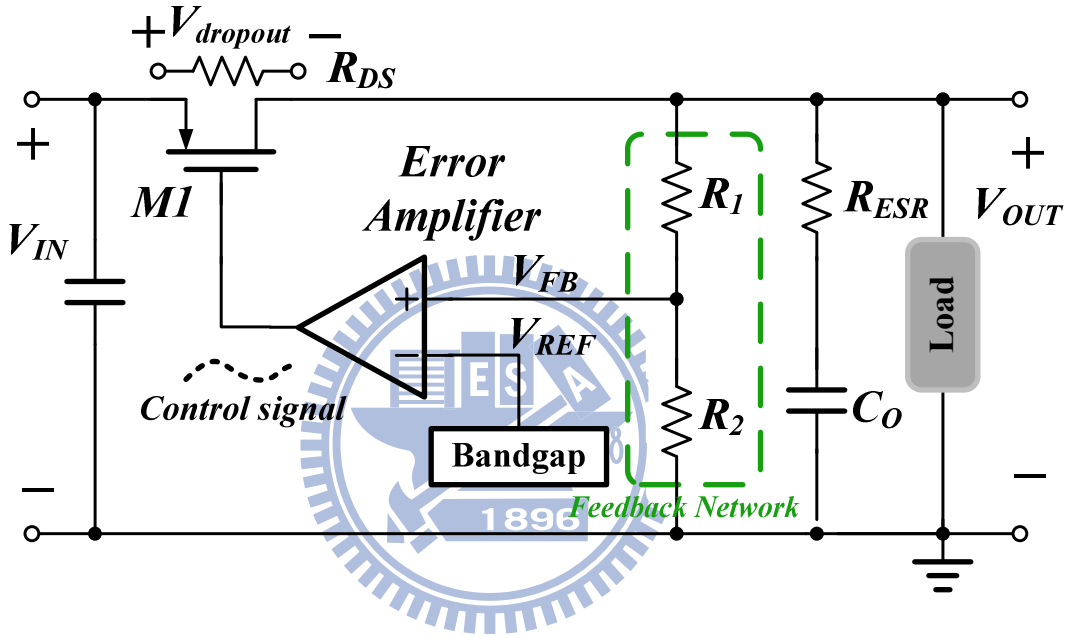


Fig. 2. The schematic of a linear regulator.

The features of linear regulator are described as follows. Firstly, the linear regulator whole circuit is simple and compact, so the die size is smaller than other voltage regulators. And secondly, linear regulator is easy to use, instead of using inductor to transfer energy, the linear regulator just adding two capacitors at input and output pin respectively. As a result, it not only can reduces Printed-circuit board (PCB) area but also cost down. Thirdly, linear regulator only uses resistive feedback network and error amplifier output analogy signal to control power MOSFET, it doesn't use any switching base circuits. So this kind of regulator has no Electro Magnetic Interference (EMI) and no output ripple, there are very suit for audio, analog and RF circuit applications.

But since the output current must pass through the series transistor which consumes the dropout voltage between the output and input voltages, the efficiency is low for large voltage difference between input and output voltages. The efficiency that depends on the difference of input and output voltages is given by (1):

$$\text{Efficiency} = \frac{V_{OUT} \cdot I_{LOAD}}{V_{OUT} \cdot I_{LOAD} + (V_{IN} - V_{OUT}) \cdot I_{LOAD}} \cong \frac{V_{OUT}}{V_{IN}} \quad (1)$$

1.2.2 Switched Capacitor Circuits

The switched capacitor circuit, also known as charge pumps, is usually used to obtain a dc voltage higher or lower than the supply voltage or opposite in polarity to the supply voltage in low power applications. Charge pump circuits use capacitors as energy storage devices. The capacitors are switched in such a way that the desired voltage conversion occurs.

The basic structure of two-phase charge pump regulator is shown in Fig. 3. Power stage consists of capacitors ($\boldsymbol{C_1}$ $\boldsymbol{C_2}$) and switches ($\boldsymbol{S_1}$ $\boldsymbol{S_2}$ $\boldsymbol{S_3}$ $\boldsymbol{S_4}$). Detailed operation is described as follows. The switches $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$ turn on and the switches $\boldsymbol{S_3}$ and $\boldsymbol{S_4}$. turn off during the first interval of the switching period, charging capacitor C_S to the input voltage level ($\boldsymbol{V_{IN}}$). During the second interval of the switching period, the switches $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$ turn off and the switches $\boldsymbol{S_3}$ and $\boldsymbol{S_4}$. turn on, the voltage that across capacitor C_S is placed in series with the input to generate an output voltage that is twice the input voltage.

The most straightforward method is to use a control circuit and an error amplifier. The error amplifier senses the output voltage variations via the feedback resistors. The control circuit fed from the error amplifier controls switches $\boldsymbol{S_1}$ ~ $\boldsymbol{S_4}$ to regulate output voltage to a stable value through a voltage control oscillator.

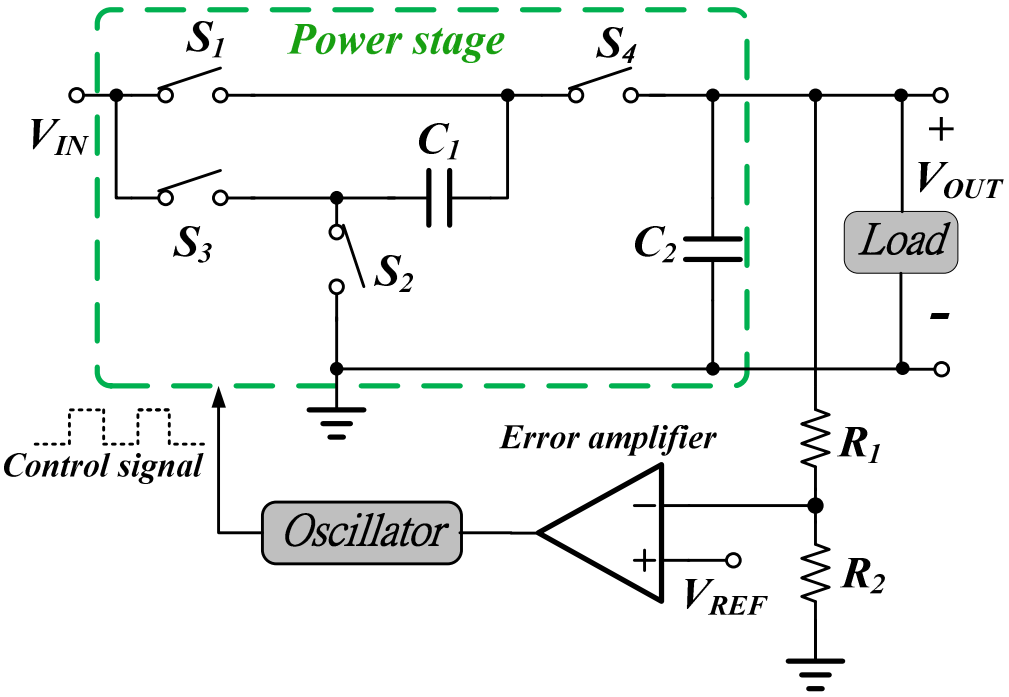


Fig. 3. The schematic of a switched capacitor voltage doubler.

The features of charge pump are described as follows. Firstly, the circuit complexity of charge pump is between linear regulator and switching regulator, which is more compact than switching regulator but more complicated than switching regulator. Secondly, due to digital rail-to-rail switching clock control, the charge pump suffers from EMI and output noise problems. But this problem doesn't heavier than switching regulator because of lower operation frequency. Finally, the load ability of charge pump is weak because the ability depends on the output capacitor C_2 and switching frequency. That is to say, the larger output capacitor causes the powerful load ability. Because of light load ability typically, the charge pump is very suit for displaying applications, such as driving the gate of MOSFET to on or off.

1.2.3 Switching regulators

Switching regulators are widely used in power supply design, because it has high efficiency and power handing capability. The basic structure of boost type voltage mode switching regulator is shown in Fig. 4. The power stage of switching regulator consists of a

couple of complementary power MOSFET (M_P M_N), passive storage elements inductor (L) and capacitor (C_O) and resistive feedback network (R_1 R_2). Detailed operation is described as follows; the resistors R_1 and R_2 sensing the variation of output voltage as the feedback signal (V_{FB}), the error amplifier receives the voltage variation information then brings the error signal (V_C). The comparator's inputs receive the error signal from error amplifier and the ramp signal (V_{RAMP}) from ramp generator, then compares the quantity between the error signal and the ramp signal to decide the duty cycle. After generating the control signal, the PWM generator control the detail timing to avoid short through current. At last, the purposes of gate drivers are driving huge complementary power MOSFET. At the first subinterval, lower power MOSFET (M_N) turns on and upper power MOSFET (M_P) turns off then input voltage source charge the inductor. At the second subinterval, lower power MOSFET (M_N) turns off and upper power MOSFET (M_P) turns on then the inductor will discharge to the capacitor and load. By the above-mentioned, the switching regulator adjusts the output voltage error and regulates to correct voltage.

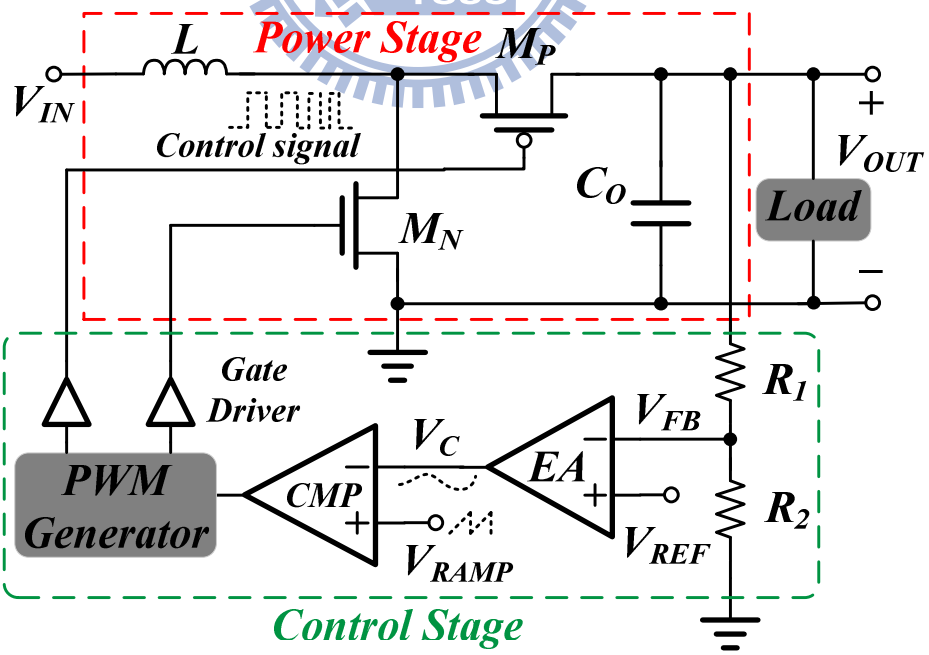


Fig. 4. The schematic of a boost type switching regulator.

Switching regulators transfer energy to the load in discrete current pulses by turning

on/off two power transistors M_1 and M_2, alternately. These current pulses are then converted to continuous or discontinuous current by means of an inductive and capacitive filter.

The features of switching regulator are described as follows. Firstly, due to the storage components such as inductor and capacitor, the switching regulator can operate in three kinds of type including buck, boost and buck-boost mode. But the more external components cause the bigger PCB size and cost. Secondly, because of switching based circuits, it suffers from EMI and noise problems critically, it will take circuit layout into consideration to avoid EMI and noise problems.The most advantage of switching regulators over the linear regulators is the higher efficiency because the output pass transistors are operated as switches. When the output pass transistor is operated in the cutoff region, it dissipates no power. When the output pass transistor is operated in triode region, it is nearly a short circuit with little voltage drop across it, and it dissipates little power. In this manner, almost all power from input supply voltage is transferred to load, and high power efficiency can be achieved typically in the range from 80% to 90%, relatively independent of input to output voltage differences.

1.2.4 Comparison

A comparison table of power supply is listed in Table 1. From Table 1, we can conclude that switching regulators are best choices for power supplies driven portable application because of their high efficiency and large power handling capability.

Table 1. Comparative table of power supply circuits.

Characteristics	*Linear Regulator*	*Switching Regulator*	*Charge Pump*
Regulation Type	***Buck***	***Buck/boost/buck-boost***	***Buck/boost***
Chip Area	***Compact***	***Large***	***Moderate***
Efficiency	***Minimum***	***Maximum***	***Medium***

EMI/Noise	***Minimum***	***Maximum***	***Medium***
Load ability	***Medium***	***Maximum***	***Minimum***
Complexity	***Simplest***	***Complicated***	***Medium***
Cost	***Low***	***High***	***Medium***

1.3 Thesis Organization

The LED backlight driver, which is widely composed of boost converters, must demands the requirements of fast-transient, high-stability, power-efficient, and space-minimized to handle large instant load variation without sacrificing the image quality and increasing the motion blur effects. Unfortunately, unlike the design of buck converters, the transient response of the boost converter is limited by the existence of a right-half-plane (RHP) zero in the continuous conduction mode (CCM) since the RHP zero remains the same in the design of voltage-mode or current-mode PWM and the HCC technique [5]. In conventional boost converter design, the discontinuous conduction mode (DCM) is widely used in order to get a simple compensation since the RHP zero appears at high frequency in DCM operation. But, the slow response can't meet the requirement of the LED backlight. Thus, the better solution is to speed the transient response without being affected by RHP zero.[11-16]

Chapter 2

Basic concepts of Switching Regulators

The basic topology and modulation technology of switching regulators will be introduced in this section. In the chapter 2.1, the topologies and principle of basic switching regulator topologies will be introduced. In section 2.2, we will review some modulation technologies that were used in switching regulators. In section 2.3, analysis of current mode boost switching regulator and its small signal modeling. The closed-loop with the PI compensation is also introduced in this section.

2.1 The topologies and principles of basic switching regulators

In this section some basic topology and modulation technology of switching regulators will be introduced. Following are three basic switching regulators as shown in Fig. 5 to Fig. 7 which are the buck, boost, and buck-boost converter respectively. They consist of storage element, such as an inductor (L) and a output capacitor (C_O) to store and transfer energy cycle by cycle to regulate the output voltage. The power MOSFET (M_1) is controlled by the control signal and the duty ratio is depend on the difference between the reference voltage and feedback signal from output voltage.

2.1.1 Buck converter

The fundamental operations of the three kinds of regulator are described as follow. In Fig. 5 it shows the basic structure of a buck converter. The buck converter can generate output voltage smaller than its' input voltage. Due to the property of conversion ratio it is also called a step down converter.

Assume the magnitude of the switching ripple is much smaller than the dc component. Therefore, the output voltage $V_{OUT}(t)$ is well approximated by its dc component V_{OUT}. This approximation is known as the small-ripple approximation. The steady-state inductor voltage and current waveforms are given in Fig. 6. According to the principle of inductor volt-second balance (the net change in inductor current over one switching period is zero), given the defining relation of an inductor：

$$i_L(T_S) - i_L(0) = \frac{1}{L}\int_0^{T_S} v_L(t)dt \tag{2}$$

In steady-state, the initial and final values of the inductor current are equal, and hence the left-hand side of Eq. (2) is zero. Therefore, in steady-state the integral of the inductor voltage must be zero. ($\int_0^{T_S} v_L(t)dt = 0$). Dividing both sides of Eq. (2) by the switching period T_S：

$$0 = \frac{1}{T_S}\int_0^{T_S} v_L(t)dt = < v_L > \tag{3}$$

$< v_L >$ is recognized as the average value, or dc component, of $v_L(t)$. In Fig. 6 the area under the $v_L(t)$ curve during time period T_S ：

$$\int_0^{T_S} v_L(t)dt = (V_{IN} - V_{OUT})(DT_S) + (-V_{OUT})(D'T_S) \tag{4}$$

By equating $< v_L >$ to zero,

$$(V_{IN} - V_{OUT})(DT_S) = (V_{OUT})(D'T_S) \tag{5}$$

Then the relationship between input-voltage (V_{IN}) and input-voltage (V_{OUT}) is ：

$$\frac{V_{OUT}}{V_{IN}} = D = M(D) \tag{6}$$

Fig. 7 shows the DC conversion ratio $M(D)$ of the buck converter.

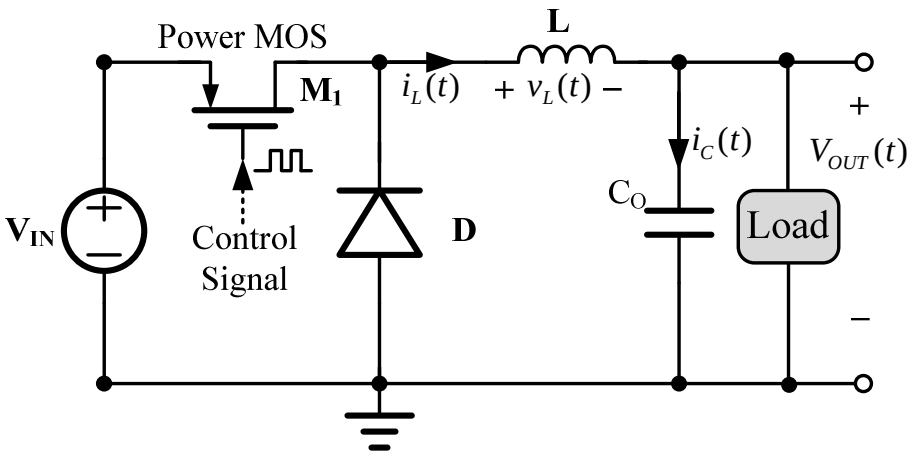


Fig. 5 The schematic of a buck type switching regulator.

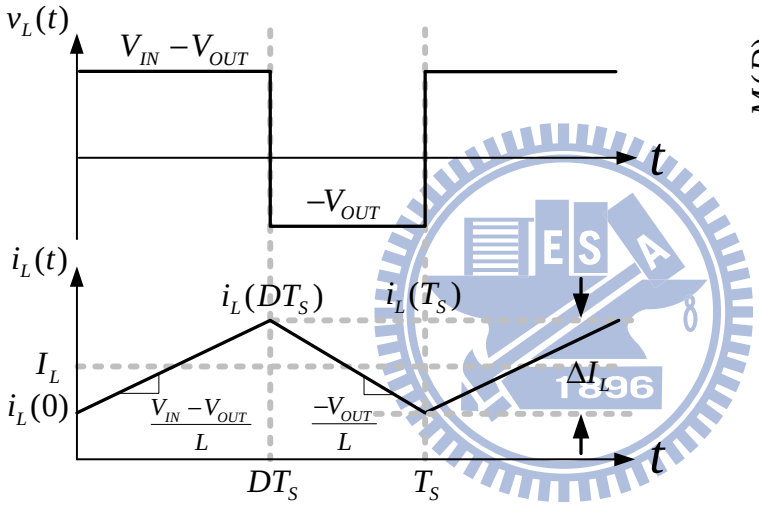


Fig. 6. Steady-state inductor voltage and current waveforms, buck type switching regulator.

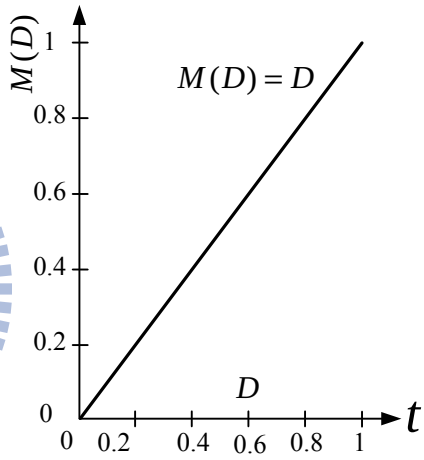


Fig. 7 The dc conversion ratio $M(D)=V_{OUT}/V_{IN}$ of buck converter.

2.1.2 Boost converter

In Fig. 8 it shows the basic structure of a boost converter. The boost converter can generate output voltage higher than its' input voltage. Due to the property of conversion ratio it is also called a step up converter.

The steady-state inductor voltage and current waveforms are given in Fig. 9. Like above buck converter has been introduced, and by using the principle of inductor volt-second balance. In steady-state, the initial and final values of the inductor current for boost converter

are equal, and hence the left-hand side of Eq. (7) is zero.

$$i_L(T_S) - i_L(0) = \frac{1}{L}\int_0^{T_S} v_L(t)dt = 0 \tag{7}$$

Dividing both sides of Eq. (7) by the switching period T_S：

$$0 = \frac{1}{T_S}\int_0^{T_S} v_L(t)dt = < v_L > \tag{8}$$

$< v_L >$ is recognized as the average value, or dc component, of $v_L(t)$. In Fig. 9 the area under the $v_L(t)$ curve during time period T_S ：

$$\int_0^{T_S} v_L(t)dt = (V_{IN})(DT_S) + (V_{IN} - V_{OUT})(D'T_S) \tag{9}$$

By equating $< v_L >$ to zero,

$$(V_{IN})(DT_S) = (V_{OUT} - V_{IN})(D'T_S) \tag{10}$$

Then the relationship between input-voltage (V_{IN}) and input-voltage (V_{OUT}) is ：

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} = M(D) \tag{11}$$

Fig. 10 shows the DC conversion ratio $M(D)$ of the buck converter.

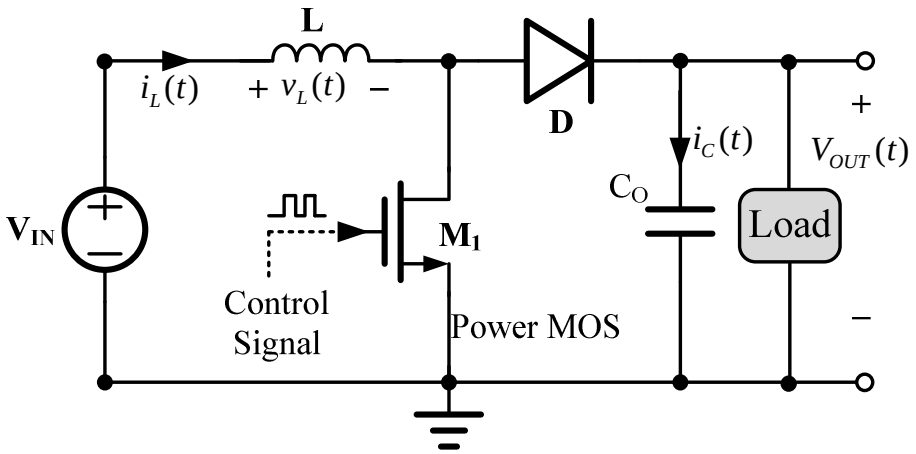


Fig. 8. The schematic of a boost type switching regulator.

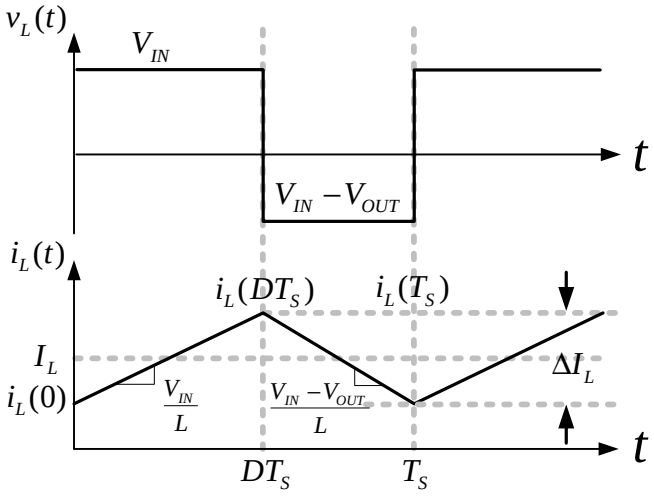


Fig. 9. Steady-state inductor voltage and current waveforms, boost type switching regulator.

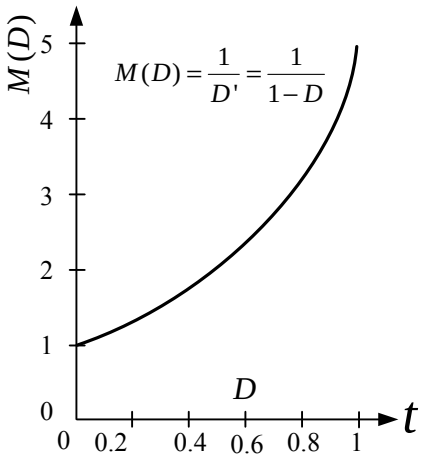


Fig. 10. The dc conversion ratio $M(D)=V_{OUT}/V_{IN}$ of boost converter.

2.1.3 Buck-Boost converter

Fig. 11 shows the basic structure of a buck-boost converter. The buck-boost converter has both the characteristic of buck and boost converter. Thus, it is also called a step up-down converter. The steady-state inductor voltage and current waveforms are given in Fig. 12. As before, we use the principle of inductor volt-second balance to find the relationship between input-voltage (V_{IN}) and input-voltage (V_{OUT}) in steady-state ：

$$\int_0^{T_S} v_L(t)dt = (V_{IN})(DT_S) + (V_{OUT})(D'T_S) \tag{12}$$

$$(V_{IN})(DT_S) = (-V_{OUT})(D'T_S) \tag{13}$$

Then the relationship between input-voltage (V_{IN}) and input-voltage (V_{OUT}) is ：

$$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D} = M(D) \tag{14}$$

Fig. 13 shows the DC conversion ratio $M(D)$ of the buck converter.

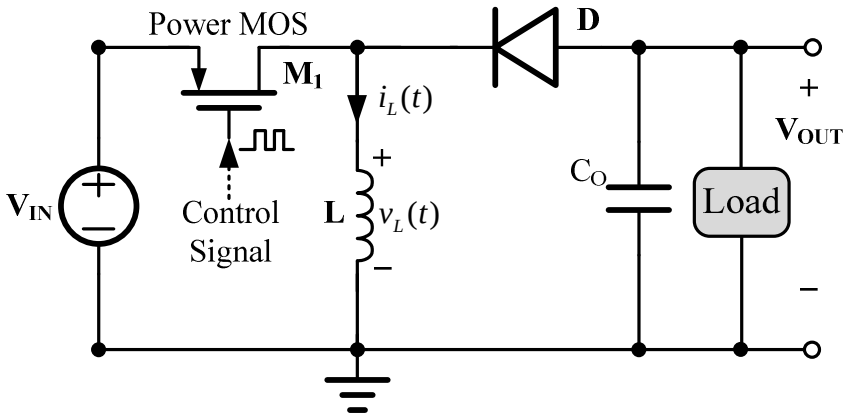


Fig. 11. The schematic of a buck-boost type switching regulator.

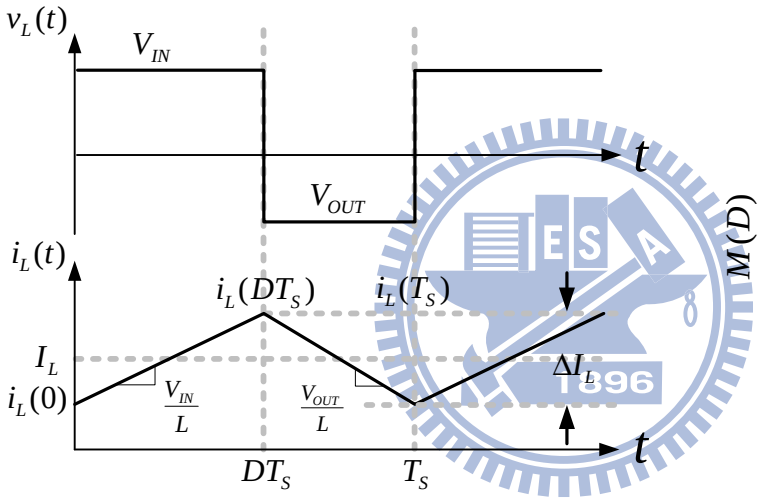


Fig. 12. Steady-state inductor voltage and current waveforms, buck-boost type switching regulator.

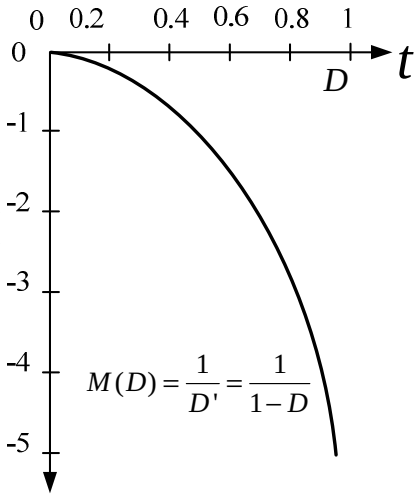


Fig. 13. The dc conversion ratio M(D) of buck-boost converter.

2.2 Analysis of current-mode Boost Switching regulator

Current-mode control DC-DC converter is already surpassed 30 years history until now. Current-mode control in power supplies is difficult to be analyzed because of its multi-loop architecture. In the current-mode control technique, the output voltage of the converter is not only controlled by the voltage feedback loop but also the peak transistor switch current. The power transistor duty cycle is not directly controlled by voltage loop, but also depends on the converter inductor current, capacitor voltages and power input voltage.

The current feedback loop results in some unique advantages compared to the voltage-mode controller. These advantages contain: line regulation is improved, the compensation network is simple, dynamic performance traits change little between CCM and DCM operation, and current limiting mechanism is also built into the architecture. In many cases the current mode control technique can enhance performance of the switching regulators.

2.2.1 The Operation Theorem of Current Mode Control

The block diagram of current mode boost converter is shown in Fig. 14. There are two operation modes for switching converter, which are voltage mode and current mode.

In voltage mode controlling, the converter only uses a voltage feedback loop to regulate the output voltage. The duty ratio of pulse-width modulation is produced by output signal of error amplifier and the original ramp signal.

In current mode controlling, it includes both voltage and current loop. The advantage of current mode is its simpler dynamics and wide-bandwidth. The inductor and capacitor of power stage offer only one low frequency pole. Otherwise, current mode control should be used of the current sensing information during the normal operation to obtain simpler dynamics.

In Fig. 14 the PWM signal is generated by clock generator with a pulse of small duty ratio. The output of the SR latch should be set to high when the output signal of clock generator is high. In this state, the power MOSFET (M_1) is turned on and diode off. The inductor current increases with a positive slope depend on the input voltage and the value of inductor. The artificial ramp is added to the current sensing signal to avoid unstable problem when duty ratio is larger than 0.5. The error signal and the sum of ramp and current sensing are compared by the analog comparator. When the sum of ramp and current sensing is larger than error signal (V_{EA}), the output of comparator is high to reset the SR latch and turn off the

power MOSFET. Therefore, the duty cycle of power MOSFET (M_1) is controlled by not only feedback voltage but also inductor current.

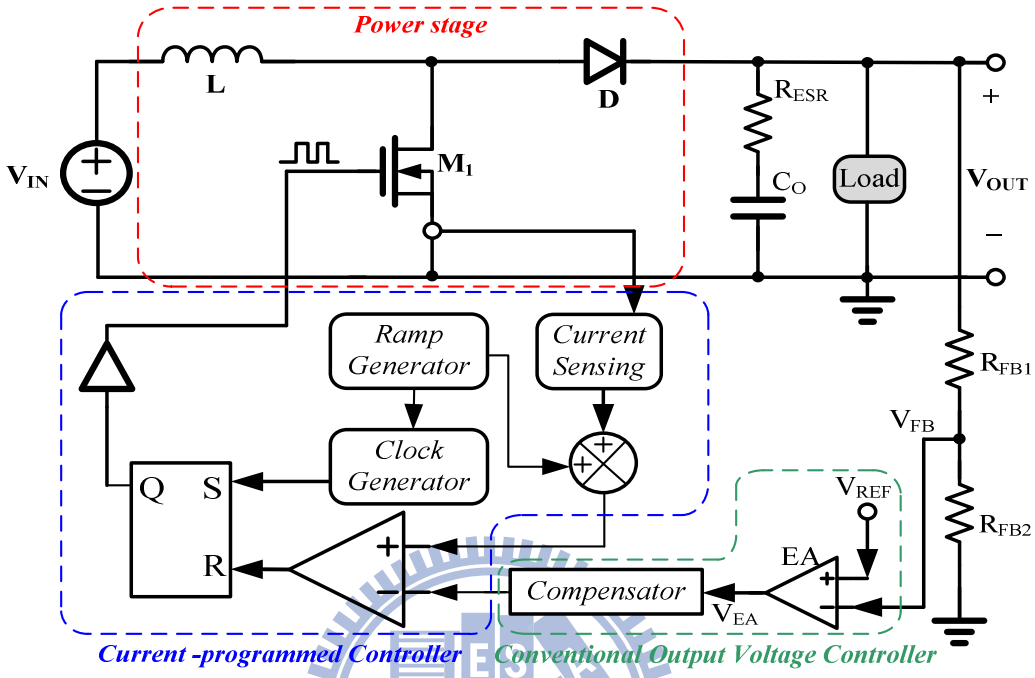


Fig. 14. Diagram of current-mode boost converter.

2.2.2 Continuous Conduction Mode (CCM)

In the CCM operation the inductor current has a minimum level above zero and operates continuously. Therefore, there are only two subintervals for switching converter in CCM operation. The two equivalent circuits of first and second subintervals are as shown in Fig. 15.

Fig. 15 (a) shows the first subinterval operation in CCM. When converter operating in first subinterval the low side NMOS turns on and inductor current increasing. During this subinterval the inductor voltage and output capacitor current can be derived as equation (15) and (16).

$$v_L(t) = L\frac{di_L}{dt} = V_{in} \tag{1}$$

$$i_{C_O}(t) = C_O\frac{dv_{C_O}}{dt} = \frac{-V_{out}}{R_L} \tag{16}$$

Fig. 15 (b) shows the second subinterval operation in CCM. When converter operating in first subinterval the high side PMOS turns on and inductor current delivering to output. During this subinterval the inductor voltage and capacitor current can be derived as equation (17) and (18).

$$v_L(t) = L\frac{di_L}{dt} = V_{in} - V_{out} \tag{17}$$

$$i_{C_O}(t) = C_O\frac{dv_{C_O}}{dt} = i_L - \frac{V_{out}}{R_L} \tag{18}$$

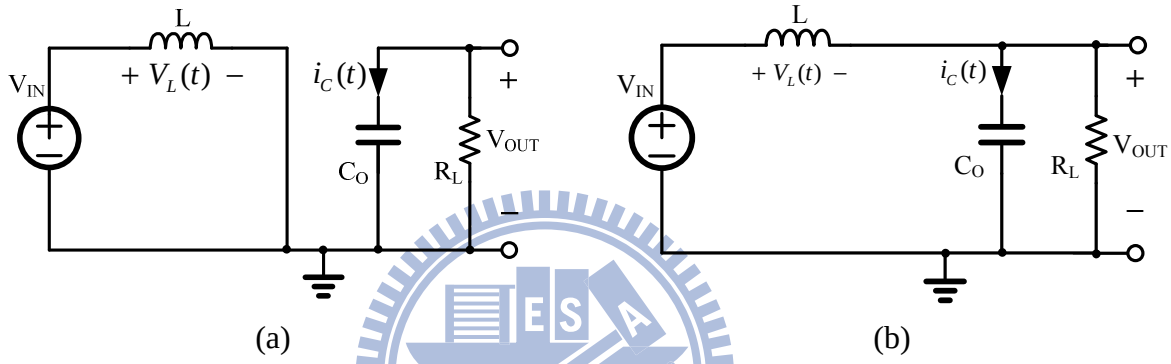


Fig. 15 (a) Equivalent circuits of the first subinterval in CCM. (b) Equivalent circuits of the second subinterval in CCM

By capacitor charge balance, the steady-state current in the switching converter can be calculated as shown in equation (19).

$$\left(\frac{-V_{out}}{R_L}\right)\cdot DT_S + \left(i_L - \frac{V_{out}}{R_L}\right)(1-D)\cdot T_S = 0\ ,\quad i_L = \frac{V_{out}}{D'R_L} = \frac{V_{in}}{D'^2 R_L} \tag{19}$$

The inductor current in equation (18) is equal to the input current of converter. Its' magnitude is greater than the load current. By combining the equation (15) and (16) the inductor current ripple and output voltage ripple can be calculated as equation (20) and (21) respectively:

$$\Delta i_L = \frac{V_{in}}{2L}\cdot DT_S \tag{20}$$

$$\Delta v_{C_O} = \frac{V}{2R_L C_O}\cdot DT_S \tag{21}$$

2.2.3 Discontinuous Conduction Mode (DCM)

In the DCM operation the inductor current has a minimum level equal to zero. Therefore, the operation region will be defined as three subintervals for switching converter in DCM operation. However, the first and second subinterval are as the same as CCM operation. Thus, the equivalent circuit in Fig. 16 has just shows the third subinterval. In the third subinterval the power MOSFET and diode are both turn off, the energy store in output capacitor to discharge to load. Owing to the three subintervals in the DCM operation, one switching cycle has divided into three parts, D_1T_S , D_2T_S and D_3T_S . The operation waveform of boost converter is shown in Fig. 17.

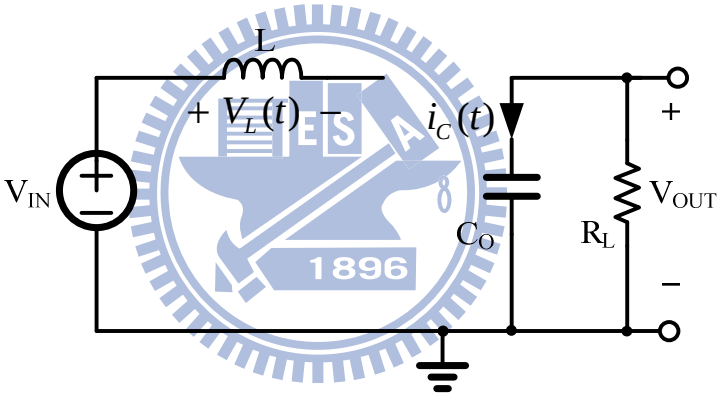


Fig. 16. Equivalent circuits of the third subinterval in DCM

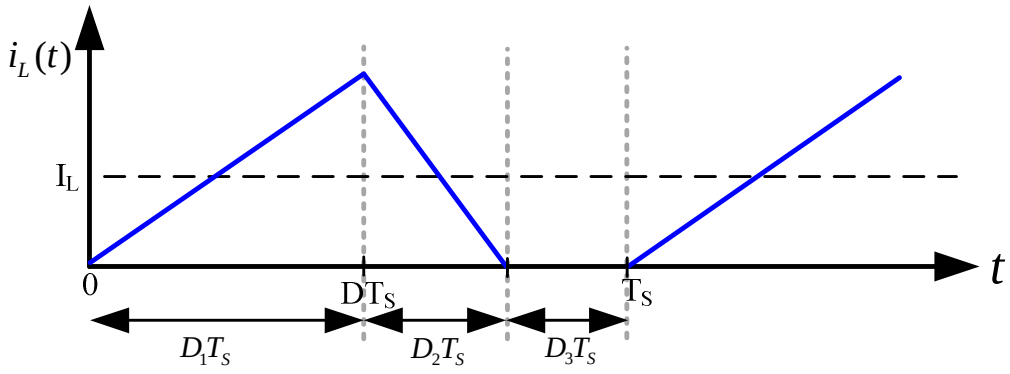


Fig. 17. Operation waveform of boost converter in DCM.

In the DCM operation the inductor voltage and capacitor current of first and second subinterval are the same as equation (15) (16) (17) (18). The relative equations of the third

subinterval are shown in equation (22) and (23).

$$v_L = 0 \tag{2}$$

$$i_C = -\frac{V_{out}}{R_L},\ i_L = 0 \tag{3}$$

By inductor voltage second balance, equation (24) can be derived. The conversion ratio is relative to the duty ratio of the first and second subintervals.

$$V_{in} \cdot D_1 T_s + (V_{in} - V_{out}) \cdot D_2 T_s + 0 \cdot D_3 T_S = 0\ ,\ \frac{V_{out}}{V_{in}} = \frac{D_1 + D_2}{D_2} \tag{4}$$

By capacitor charge balance, the steady-state current in the switching converter can be calculated as shown in equation (25).

$$I_{out} = \frac{V}{R_L} = \frac{1}{T_S} \cdot \left[\frac{1}{2} \left(\frac{V_{in}}{L} D_1 T_S \right) \cdot D_2 T_S \right] = \frac{V_{in} D_1 D_2 T_S}{2L} \tag{25}$$

By replacing equation (25) into (24) the output voltage can be obtained as:

$$\frac{V_{out}}{V_{in}} = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}\ ,\ where\ K = \frac{2 \cdot L}{R_L T_S} \tag{26}$$

As mention in 2.2.2 the conversion ratio in CCM operation only depends on input voltage and duty cycle. However, in DCM operation the voltage conversion ratio depends on the inductor, load resistance, switching frequency and input voltage.

2.3 The Small Signal Modeling of the HCC Boost Converter

Owing to low power consumption requirement, the hysteretic current control (HCC) technique is selected as the modulation method for LED backlight. A simple structure is illustrated in Fig. 18.

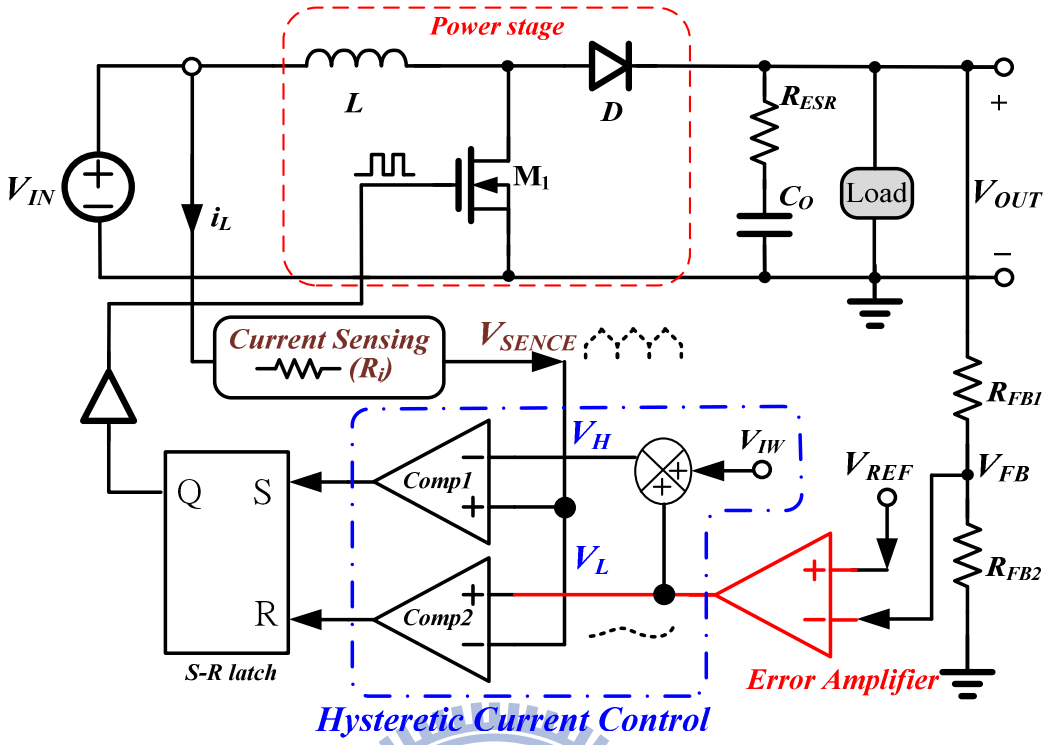


Fig. 18. The HCC technique uses an error amplifier to enhance the regulation accuracy.

2.3.1 The Small Signal Analyzing

The basic hysteretic current control is depicted in Fig. 18. This technique control the inductor current sensed with current sensing circuit within a hysteresis window. The hysteresis window is defined by the output signal of error amplifier. Fig. 19 shows the control behavior of inductor current. The inductor current rises until it reaches the upper band of hysteresis window during t_{on} period when the high-side MOSFET turns on [7]. When the low-side MOSFET turns on during t_{off} period, the inductor current falls to reach the lower band of hysteresis window This HCC technique is simple and has fast dynamic characteristics due to its unlimited on-time value, but it is poor on electromagnetic interference (EMI) issue.

As in Fig. 19 the converter operate in CCM mode, the switching period t_s expressed in (27) is the summation of on-time t_{on} and off-time t_{off}. The value of t_{off} and t_{on} can be written as (28) according to the waveform in the phase 2.

$$t_s = t_{on} + t_{off} \tag{27}$$

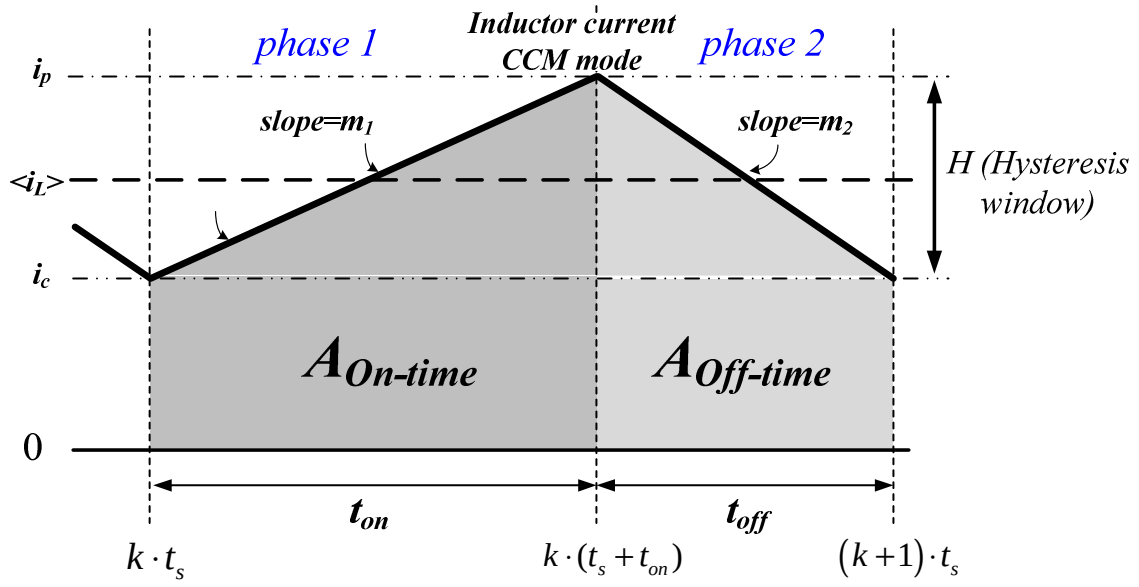


Fig. 19. The inductor current waveform is limited with the hysteresis window defined by the HCC technique.

$$t_{on} = \frac{LH}{v_{in}}, t_{off} = \frac{LH}{(v_o - v_{in})} \tag{28}$$

The peak inductor current, i_p, can be expressed as (29) and the average inductor current $\langle i_L \rangle$.

$$i_p = \langle i_L \rangle + \frac{v_{in}}{2L} t_{on} = \langle i_L \rangle + \frac{(v_o + v_{in})}{2L} t_{off} \tag{29}$$

Now, let's consider the small signal analysis. The value of each variable can be written as the summation of two components the DC term and its AC perturbation. The duty cycle, *d*, and its complementary value, *d'* are shown in (30) and (31).

$$t_s = T_s + \hat{t}_s, \; t_{on} = T_{on} + \hat{t}_{on}, \text{ and } \; t_{off} = T_{off} + \hat{t}_{off} = d' t_s \tag{30}$$

$$d = D + \hat{d} \;\text{ and }\; d' = 1 - d = D' - \hat{d} \tag{31}$$

Hence, (27) and (28) can be re-written as (32) and (33), respectively.

$$(T_s + \hat{t}_s) = (T_{on} + \hat{t}_{on}) + (T_{off} + \hat{t}_{off}) \tag{32}$$

$$T_{off}+\hat{t}_{off}=\frac{LH}{\left(V_o+\hat{v}_o-V_{in}-\hat{v}_{in}\right)} \tag{33}$$

By keeping the first-order ac terms, (30) and (29) can be re-written as (34) and (35), respectively. The small-signal equations can be derived in (34).

$$\hat{t}_s=\hat{t}_{on}+\hat{t}_{off},\ \hat{d}=\frac{\hat{t}_{on}-D\hat{t}_s}{T_s},\text{ and }\ \hat{t}_{off}=-\frac{LH}{\left(V_o-V_{in}\right)^2}\left(\hat{v}_o-\hat{v}_{in}\right) \tag{34}$$

$$\hat{t}_{on}=\frac{2L}{V_{in}}\left(\hat{i}_p-\hat{i}_L\right)-\frac{T_{on}}{V_{in}}\hat{v}_{in}\text{ and }\hat{i}_p=\hat{i}_L+\frac{\left(V_{in}\hat{t}_{on}+T_{on}\hat{v}_{in}\right)}{2L} \tag{35}$$

Therefore, the small-signal duty cycle is derived as (36).

$$\hat{d}=\frac{2\cdot D\cdot D'}{H}(\hat{i}_P-\hat{i}_L)-\frac{1}{V_o}\hat{v}_{in}+\frac{D'}{V_o}\hat{v}_o \tag{36}$$

By using the DC equivalent equations, (36) can be simplified as (37).

$$\hat{d}=F_m\left(\hat{v}_C-R_i\cdot\hat{i}_L\right)-\frac{1}{V_O}\cdot\hat{v}_{in}+\frac{D'}{V_O}\cdot\hat{v}_o \tag{37}$$

$$where\ F_m=\frac{2DD'}{HR_i} \tag{38}$$

As a result, the small-signal model of the hysteretic current mode boost converter is illustrated in Fig. 20. The control-to-output transfer function is shown in (39). R_{OUT} is the output impedance. R_i is the current sensing equivalent resistance. R_{ESR} is the equivalent series resistance of output capacitor, C_o.

$$G_{vc}=\frac{\hat{v}_o}{\hat{v}_c}=\frac{F_m\cdot G_{vd}}{1-\frac{D'}{V_O}\cdot G_{vd}+F_m\cdot G_{id}\cdot R_i} \tag{39}$$

$$G_{vd}=\left.\frac{\hat{v}_o}{\hat{d}}\right|_{\hat{v}_{in}=0}=\frac{V_o}{D'}\cdot\frac{\left(1-s\frac{L}{D'^2R}\right)\left(1+sR_{ESR}C_o\right)}{1+s\frac{L}{RD'^2}+s^2\frac{LC_o}{D'^2}}\text{ and }\ G_{id}=\left.\frac{\hat{i}_L}{\hat{d}}\right|_{\hat{v}_{in}=0}=\frac{2\cdot V_o}{D'^2R}\cdot\frac{\left(1+s\frac{RC_o}{2}\right)}{1+s\frac{L}{RD'^2}+s^2\frac{LC_o}{D'^2}} \tag{40}$$

Because of that $F_m \cdot G_{id} \cdot R_f >> 1 - k_r \cdot G_{vd}$, (39) can be simplified as (41)

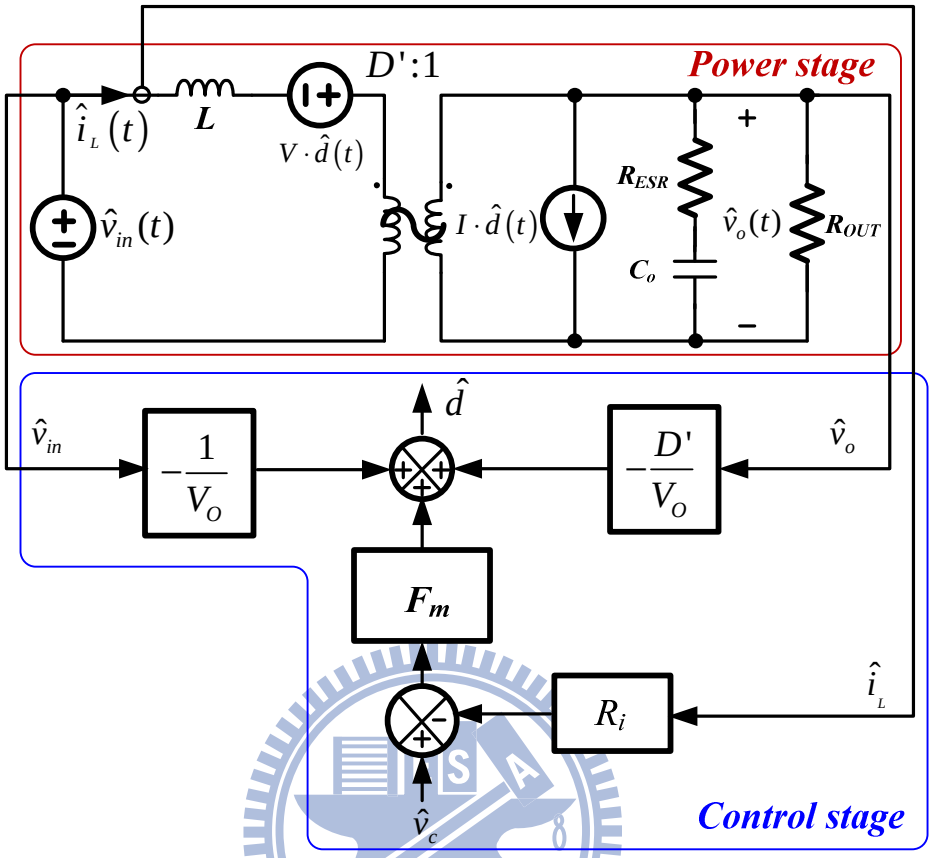


Fig. 20. The small-signal model of the boost converter under the hysteretic current mode control.

$$G_{vc} = \frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m \cdot G_{vd}}{F_m \cdot G_{id} \cdot R_f} = \frac{1}{R_f}\frac{G_{vd}}{G_{id}} = \frac{D' R_{OUT}}{2R_f}\frac{\left(1-\frac{s}{\omega_{z(RHP)}}\right)\left(1+\frac{s}{\omega_{z(ESR)}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)} \tag{41}$$

$$pole: \omega_{p1} = \frac{2}{R_{OUT} C_o}$$
$$zero: \omega_{z(RHP)} = \frac{D'^2 R_{OUT}}{L}, \omega_{z(ESR)} = \frac{1}{R_{ESR} C_o} \tag{42}$$

It is obvious to find that there are one dominant pole (ω_{p1}) and two zeros (one RHP zero, $\omega_{z(RHP)}$, and one LHP zero, $\omega_{z(ESR)}$). The frequency response of the HCC technique is similar to that of the current-mode PWM technique. Hence, the proportional-integral (PI) compensation is enough to choice. The PI compensator has a transfer function as shown in (43). ω_{zc1} is used to cancel the effect of power stage pole (ω_{p1}). And ω_{pc1} replaces ω_{p1} to forms

the new dominant pole to determine the system bandwidth. The role of ω_{pc2} is used to decrease the high-frequency gain due to the existence of $\omega_{z(RHP)}$.

$$G_c = G_{c0}\frac{\left(1+\frac{s}{\omega_{zc1}}\right)}{\left(1+\frac{s}{\omega_{pc1}}\right)\left(1+\frac{s}{\omega_{pc2}}\right)} \tag{43}$$

Comparing to conventional current-mode PWM controller, the HCC technique doesn't need slope compensation to reduce sub-harmonic oscillation when perturbation happened. In other words, the compensation in the HCC technique is much simpler than the current-mode PWM technique. However, the RHP zero which seriously affects the system stability still exists in both techniques

2.3.2 Right Half Plane (RHP) zero

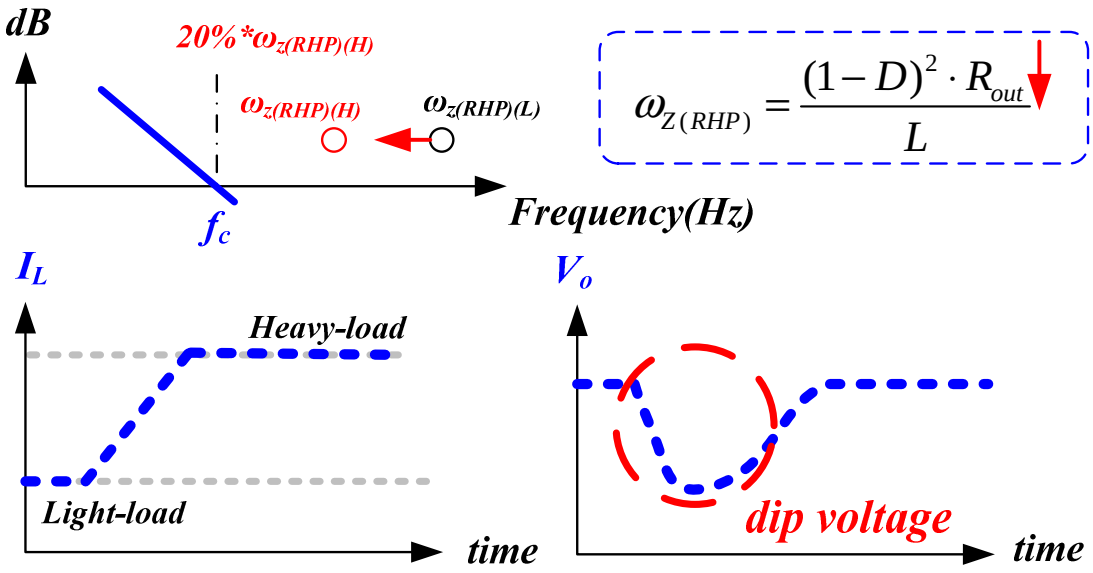
RHP zeros are a property of a special class of active circuits which have a tendency to respond initially in the wrong direction when given a changed input. Eventually, the output will move in the direction commanded by the input. How fast it starts moving in the right direction is determined by the frequency location of the RHP zero. Boost and flyback converters are very popular circuits in use in the industry today, and both have RHP zero characteristics when operating in continuous conduction mode.

The cause of the RHP zero for these converters is the same and intuitive. The output capacitor of the converter is charged by the inductor current, but only when the power switch is turned off. An initial increase in duty cycle of the power switch increases the current in the inductor within one cycle, but the net charge to the output capacitor (product of the inductor current and off-time) is initially less. Hence, an increase in command to the system results in a temporary droop in the output voltage.

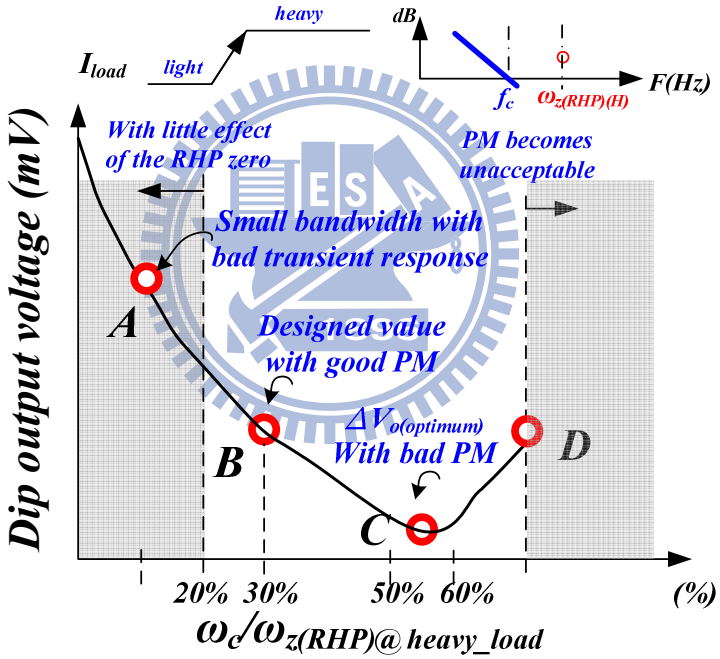
This can be confusing for a controller that is monitoring the output voltage to make control decisions. There is no alternative but to wait and see where the long-term trend is before adjusting the duty cycle.

2.3.3 The effect of the RHP zero

When heavy loads happened, the RHP zero effect becomes worse to affect the system stability as illustrated in Fig. 21(a) and (41). A reasonable design limitation on the crossover frequency, ω_c, should be below 1/10 of the switching frequency. When the designed crossover frequency is higher, more issues with noise will arise. In addition, the designed crossover frequency is also considered the influence of RHP zero. To reduce this effect it should be smaller than the 10~20% RHP zero, which is the RHP zero at heavy loads, as the illustrated in Fig. 21(a). When the crossover frequency is far away the RHP zero, the output voltage (V_o,) has no dip voltage in case of load current variation. That is, the RHP zero has little effect on the undershoot output voltage. However, because of small bandwidth the transient response is too slow and thus the output voltage has a large dip voltage. Although, a large bandwidth can shorten the transient response and get a small dip voltage. An increasing crossover frequency may have a large dip voltage due to the existence of the RHP zero. In order to get a smallest dip output voltage. It need to confer the relationship between ω_c and $\omega_{z(RHP)}$ and to. There exists an optimum ratio between the ω_c and $\omega_{z(RHP)}$, which is labeled as $\Delta V_{o(optimum)}$ at point C. But the phase margin at this optimum dip voltage is not good enough due to $\omega_{z(ESR)}$ and one high-frequency pole from the compensator. Therefore, the system bandwidth needs to be extended to compensate the dip voltage due to the RHP zero and not be limited by 10~20% RHP zero. The designed value is set at point B, which is about 30% of the RHP zero.



(a)



(b)

Fig. 21. The influence of the RHP zero effect. (a) The variation of the load may cause a dip output voltage due to the existence of the RHP zero. (b) The relationship between dip output voltage and the ratio of the ω_c and $\omega_{z(RHP)}$.

2.4 The Closed-loop Analysis with the PI Compensation

Fig. 22 is a closed-loop diagram of the boost converter with the HCC technique. The loop gain is *T(s)* as shown in (44). *H(s)* is the sensor gain, which is equal to $R_2/(R_1+R_2)$. $G_c(s)$

is the compensation transfer function that is composed of an error amplifier and a PI compensator.

$$T(s) = H(s) \cdot G_c(s) \cdot G_{vc}(s) \tag{44}$$

Fig. 23 shows the PI compensator which contributes one low-frequency pole-zero pair, (ω_{pc1}, ω_{zc1}), and one high-frequency pole, ω_{pc2} (to avoid switching noise). The transfer function from the feedback signal (V_{FB}) *to* the error amplifier output (V_C) is shown as equation (45).

$$\frac{V_C}{V_{FB}} = g_m \cdot [R_O // (R_{Z1} + \frac{1}{sC_{C1}})] = g_m \cdot R_O \cdot \frac{(1 + s \cdot C_{C1} \cdot R_{Z1})}{(1 + s \cdot C_{C1} \cdot R_O)} \quad ,if \;\; R_O >> R_{Z1} \tag{45}$$

Where g_m and R_O are the transconductance and the output resistance of the error amplifier, respectively. Therefore, the pole and zero contributed by the compensation network are as follow.

$$zero: \omega_{zc1} = \frac{1}{C_{C1} \cdot R_{Z1}}, \;\; pole: \omega_{pc1} = \frac{1}{C_{C1} \cdot R_O}, \omega_{pc2} = \frac{1}{C_{C2} \cdot R_{Z1}} \tag{5}$$

To make sure the stability of the system, in this kind of compensation technique the pole which is used to replace the system pole and becomes the dominate pole. Furthermore, the unit gain frequency of the loop is determined by the compensation resistance. Thus, the frequency response of the system can be improved by choosing an optimal compensation resistance.

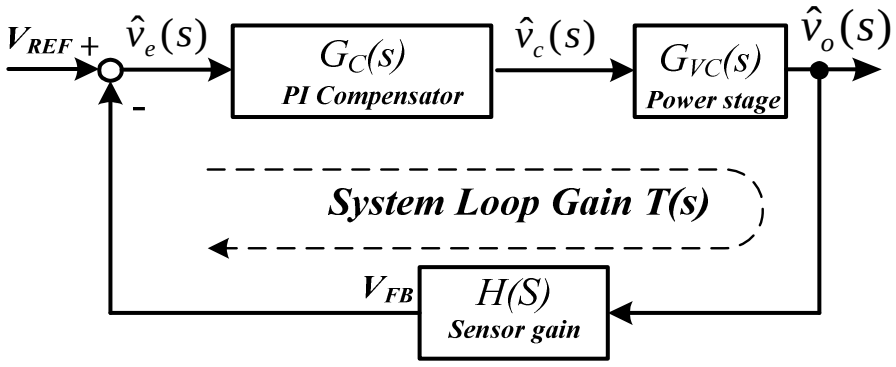


Fig. 22. The simplified feedback system of the HCC regulator.

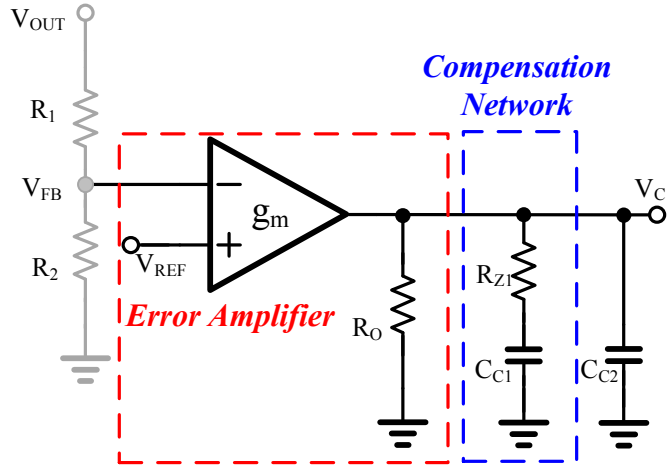
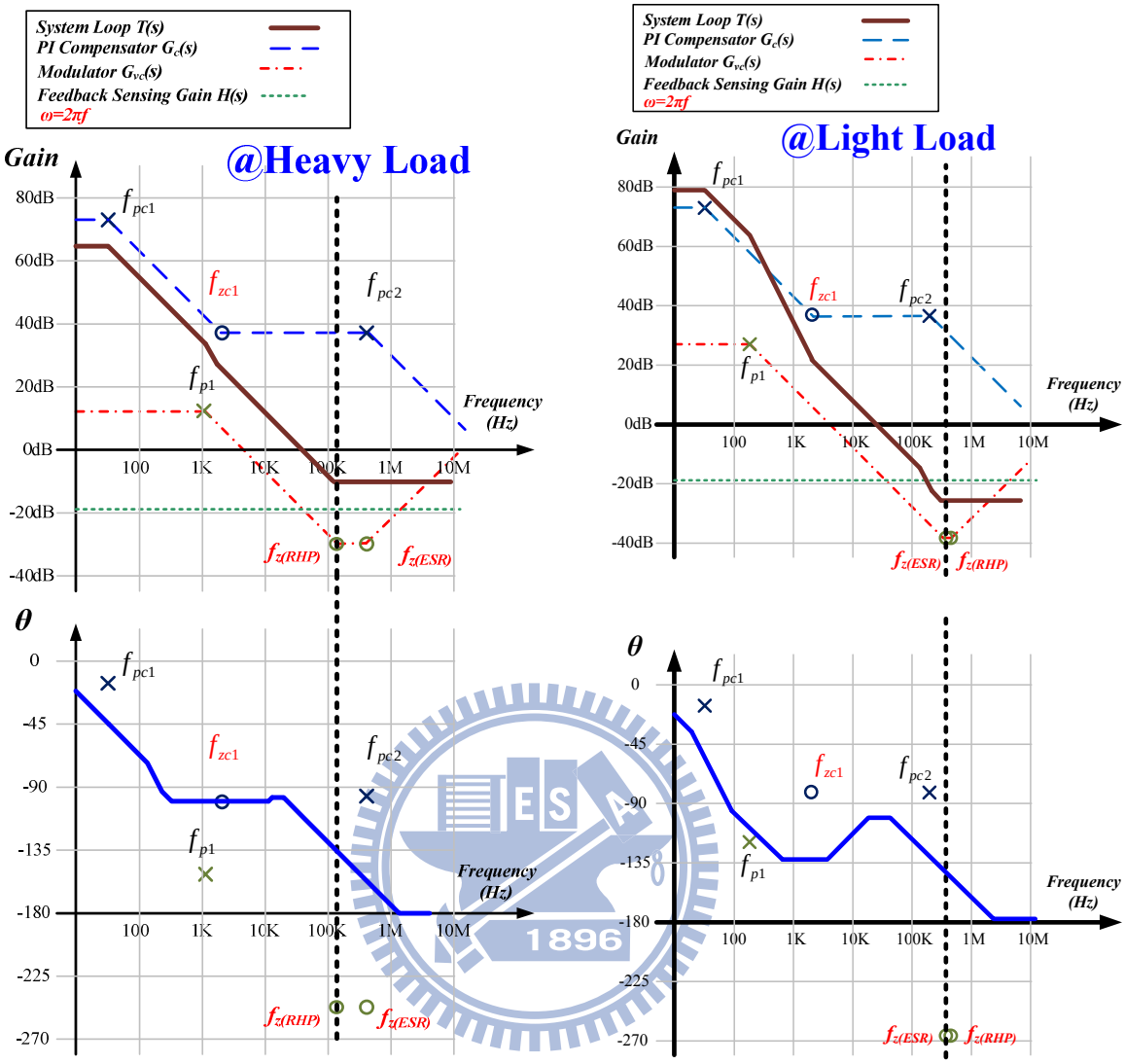


Fig. 23. The PI compensator of HCC dc-dc converter

The loop gain T(s) can be illustrated in Fig. 24 at light and heavy loads. Using the compensation zero (f_{zc1}) in the PI compensator to cancel the pole of power stage of the converter (ω_{p1}), then the system bandwidth will be extended. The RHP zero $\omega_{z(RHP)}$ will decrease at heavy loads, which is represented by a solid dash line in Fig. 24(a). According to Fig. 24(b), the ratio of ω_c and $\omega_{z(RHP)}$ has an optimum value when the dip output voltage is the major concern. That is the compensation zero ω_{zc1} is decided at heavy loads.The bandwidth becomes worse due to the decrease of ω_{p1} at light loads. As the reason explained before, the crossover frequency is limited by $\omega_{z(RHP)}$ at heavy loads.



(a) (b)

Fig. 24 The compensated loop gain *T(s)* (a) at heavy loads and (b) at light loads.

Chapter 3

The Proposed RHP Zero Alleviating Technique in the SDC Boost Converter

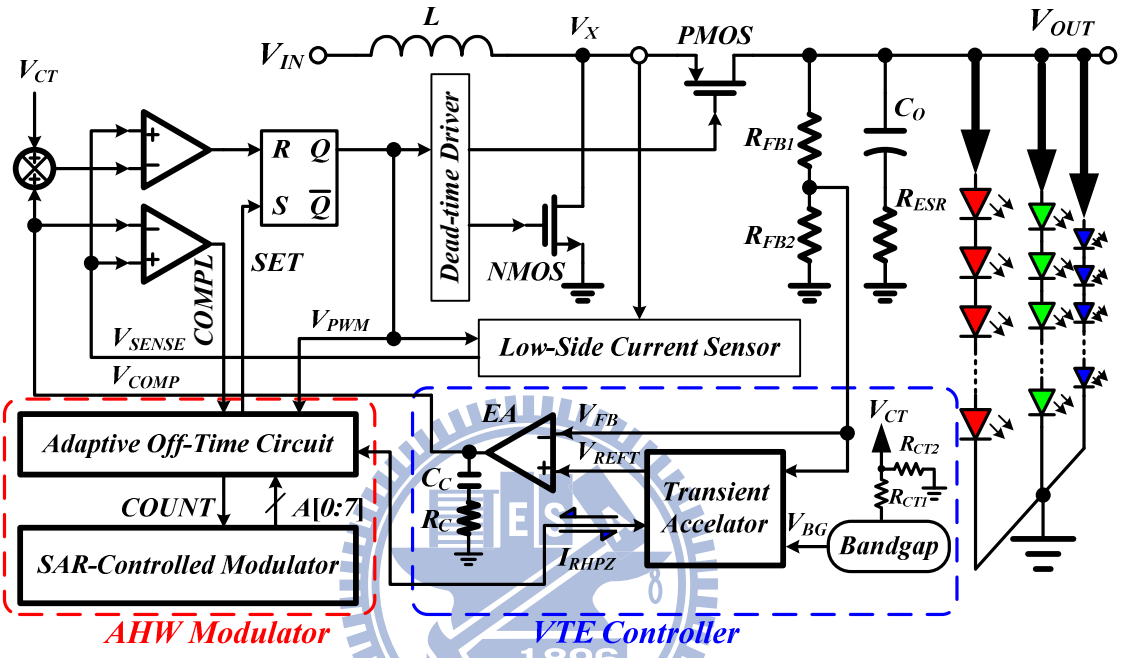


Fig. 25. The system architecture of the proposed boost converter with the proposed SDC technique.(LED Backlight Driver with the SDC Controller)

The proposed SDC architecture is shown in Fig. 25. The circuit implementation with a hysteresis window formed by the value of V_{CT}, which is generated by the voltage divider from the bandgap circuit, allows the output ripple to be limited within this hysteresis window and adjust the trailing and leading edges for fast transient response. In case of heavy load condition, the on-time period suddenly increases while the off-time period decreases. The energy, delivered to the output decreases in the beginning, seriously causes the output has a large voltage drop. After the inductor current increases to a higher value, the output voltage can be pulled back to its regulated value. In other words, the RHP zero effect induces a large dip voltage and long transient response. Thus, the SDC controller includes the VTE controller to decrease the drop voltage and improve the transient response time.

3.1 The Constant duty Analysis for Boost converter

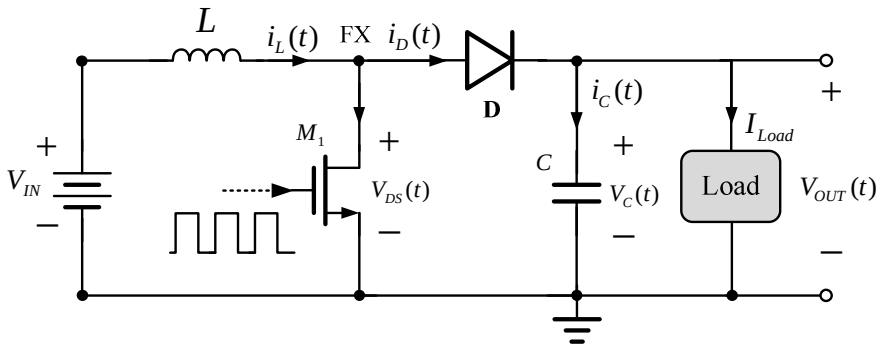


Fig. 26. A conventional boost converter

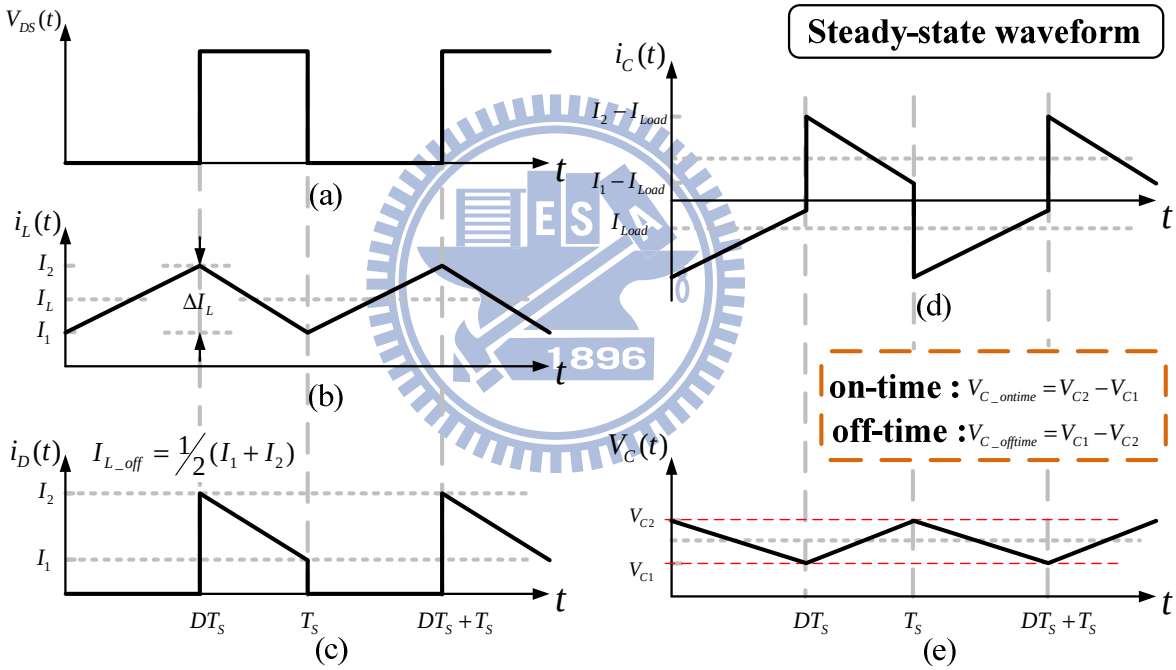


Fig. 27. (a). $V_{DS}(t)$ is the net voltage at FX. (b). $i_L(t)$ is the inductor current. (c). $i_D(t)$ is the current pass through the diode. (d). $i_C(t)$ is the output capacitor current. (e). $V_C(t)$ is the voltage between V_{OUT} and ground.

The SDC method could reduce the RHP effect due to the extension of the on-time and the off-time periods during transient response. A conventional boost converter is illustrated in Fig. 26, including Fig. 26 the current and voltage waveform are shown in Fig. 27. Here we assume all switching devices and passive elements are ideal. In the other words, the voltage

across is zero when the Power NMOS (M1) and the diode are turned on. The voltage variation on the output capacitor during the on-time and off-time periods can be expressed as (47) and (48), respectively. These two equations also indicate the output voltage variation during the on-time (V_{C_ontime}) and off-time ($V_{C\_offtime}$) periods.

$$V_{C\_ontime} = \frac{I_{Load}}{C} DT_S \tag{47}$$

$$V_{C\_offtime} = \frac{(I_{L\_offtime} - I_{Load})}{C} D'T_S \tag{48}$$

Where I_{Load} is the load current, and $I_{L\_offtime}$ is the current value pass to output through diode during off-time periods. The total voltage drop on the capacitor can be shown as (49) by subtracting equation (47) and (48).

$$\Delta V_C = -V_{C\_ontime} + V_{C\_offtime} = -V_{outdrop} \tag{49}$$

Section 3.1.1 and 3.1.2 will compare two different methodology used in boost converter when the load step happened. They are conventional duty-increasing method and constant duty method, respectively.

3.1.1 Type 1：Duty Increasing Methodology

The output voltage $V_{OUT}(t)$ and inductor current $i_L(t)$ waveforms for duty increasing boost converter is shown in Fig. 28. The output capacitor of the converter is charged by the inductor current only when the power switch is turned off. When load transient happened, an initial increase in duty cycle of the power switch increases the current in the inductor within one cycle, but the net charge to the output capacitor (product of the inductor current and off-time) is initially less. Hence, an increase in command to the system results in a large temporary droop in the output voltage.

As depicted in Fig. 28, $t_{on_{n-1}}$, $t_{off_{n-1}}$, and $T_{S_{n-1}}$ are the one-time, off-time and switching period value at light-load, respectively.

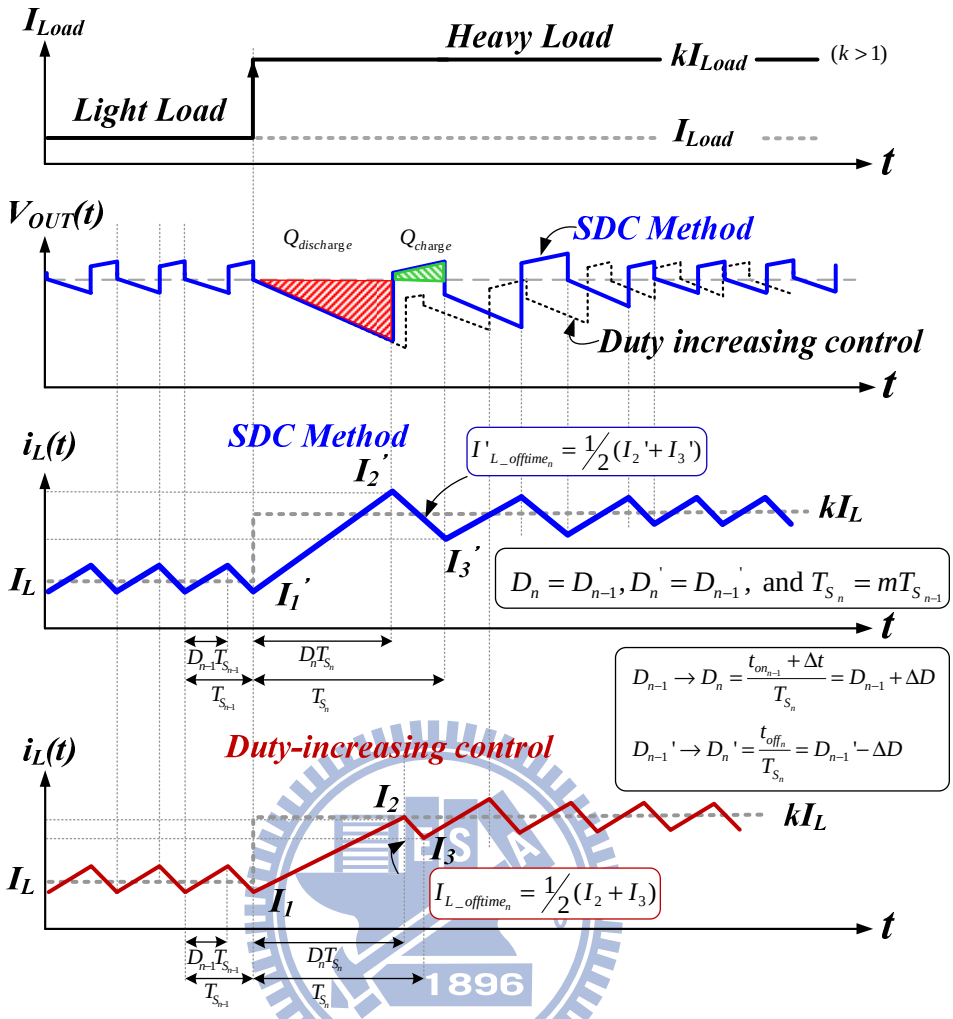


Fig. 28. The inductor current $i_L(t)$ and the output voltage $V_{OUT}(t)$waveforms of the SDC control method and the duty-increasing control.

For duty-increasing method the on-time will increase when load step happened at time t_1, the value of on-time, off-time and switching period will change to equation (50).

$$\begin{aligned} t_{on_n} &= t_{on_{n-1}} + \Delta t \\ t_{off_n} &= t_{off_{n-1}} \\ T_{S_n} &= mT_{S_{n-1}}, m > 1 \end{aligned} \tag{50}$$

Δt is the on-time increasing value at heavy-load. The duty cycle can be expressed as $D_n = D_{n-1} + \Delta D$ and $D_n' = D_{n-1}' - \Delta D$. Then the output voltage variation during this time period is shown as (51).

$$\Delta V_{C\_duty-incre_n} = -V_{drop\_duty-increasing} = -\frac{I_{Load_n}}{C}(t_{on_{n-1}} + \Delta t) + \frac{(I_{L\_offtime_n} - I_{Load_n})}{C} t_{off_{n-1}} \tag{51}$$

$I_{L\_offtime_n}$ is the off-time average inductor current value when load variation happened, and it's equal to the half sum of I_2 and I_3 in (52). ΔI_L is the inductor current variation before load transient which is equal to $\Delta I_{L_{n-1}} = V_{IN} / L\, D_{n-1} T_{S_{n-1}}$.

$$
\begin{aligned}
I_1 &= I_L - \frac{\Delta I_L}{2} \\
I_2 &= I_1 + \frac{V_{IN}}{L} D_n T_{S_n} \\
I_3 &= I_2 + \frac{(V_{IN} - (V_{out_{n-1}} - \Delta V_{out_n}))}{L} D_n{}' T_{S_n} \\
I_2 + I_3 &= 2I_1 + \frac{V_{IN} T_{S_n} D_n}{L} + \frac{\Delta V_{out_n} D_n{}' T_{S_n}}{L}
\end{aligned}
\tag{52}
$$

Where the $V_{out_{n-1}} - \Delta V_{out_n}$ means the output voltage dc component during time period t_1 and t_2 , and ΔV_{out_n} can be expressed as (53).

$$
\Delta V_{out_n} = \frac{I_{Load_n}}{C} D_n T_{S_n} - \frac{(I_{L\_offtime_{n-1}} - I_{Load_{n-1}})}{C} D_{n-1}{}' T_{S_{n-1}} \tag{53}
$$

$I_{L\_offtime_{n-1}}$ is the off-time average inductor current value before load variation happened, which equal the inductor current dc component at light-load. By replacing equation (52) into $I_{L\_offtime_n}$ the off-time average inductor current can be obtained as:

$$
I_{L\_offtime_n} = I_L + \frac{V_{IN}}{2L} [D_n T_{S_n} - D_{n-1} T_{S_{n-1}}] + \frac{\Delta V_{out_n} D_n{}' T_{S_n}}{2L} \tag{54}
$$

In order to simplify the equation, we let the demand inductor current at light-load and heavy-load are I_L and $kI_L\,(k>1)$, respectively. So (53) can be simplified to (55).

$$
\begin{aligned}
\Delta V_{out_n} &= \frac{D_{n-1}{}' k I_L}{C} D_n T_{S_n} - \frac{(I_L - D_{n-1}{}' I_L)}{C} D_{n-1}{}' T_{S_{n-1}} \\
&= \frac{I_L D_{n-1}{}'}{C} [D_n k T_{S_n} - D_{n-1} T_{S_{n-1}}]
\end{aligned}
\tag{55}
$$

According to (54) and (55), we will get (56)：

$$
\Delta V_{C\_duty-incre_n} = -V_{drop\_duty-increasing} = \frac{T_{S_n}}{C} [I_{L\_offtime_n} D'_n - I_{Load_n}]
$$

$$= \frac{mT_{S_{n-1}}}{C}\{\frac{V_{IN}T_{S_{n-1}}}{2L}[D_{n-1}(m-1)+m\Delta D]\cdot(D_{n-1}{}'-\Delta D)+I_L[(1-k)D_{n-1}{}'-\Delta D]$$
$$+\frac{(D_{n-1}{}'-\Delta D)mT_{S_{n-1}}}{2L}\cdot\frac{I_L D_{n-1}{}'T_{S_{n-1}}}{C}[km(D_{n-1}{}'+\Delta D)-D_{n-1}]\} \quad (56)$$

Equation (56) means the output voltage total drop value during first transient period with duty increasing method. Next section will analyze another way using in boost converter when load step happened. That's constant duty methodology.

3.1.2 Type 2：Solid-Duty-Control Methodology

Fig. 28 shows the output voltage $V_{OUT}(t)$ and inductor current variation waveforms for SDC boost converter which the value of duty is constant. As above has been shown, at the timing the load transient happened, the duty cycle of the power switch increases to get enough inductor current within one cycle, but the net charge to the output capacitor is initially less. Hence, an increase in command to the system results in a large temporary droop in the output voltage. In order to avoid this condition, we maintain the original duty cycle before load transient. That means not only increasing the on-time but also increasing the off-time by the same value.

As depicted in Fig. 28, $t_{on_{n-1}}$, $t_{off_{n-1}}$, and $T_{S_{n-1}}$ are the one-time, off-time and switching period value before load step happened, respectively. For constant duty method the duty cycle will keep in the same value when load transient happened (from $I_{Load_{n-1}}$ to I_{Load_n} at time t_1), so the value of on-time, off-time and switching period will change to equation (57).

$$t_{on_n} = t_{on_{n-1}} + \Delta t$$
$$t_{off_n} = t_{off_{n-1}} + \Delta t \quad (57)$$
$$T_{S_n} = mT_{S_{n-1}}, m > 1$$

Then the output voltage variation during this time period is shown as (58).

$$\Delta V_{C\_SDC_n} = -V_{drop\_SDC_n}$$

$$= -\frac{I_{Load_n}}{C} D_n T_{S_n} + \frac{(I'_{L\_offtime_n} - I_{Load_n})}{C} D_n' T_{S_n} = \frac{T_{S_n}}{C}[I'_{L\_offtime_n} D_n' - I_{Load_n}] \quad (58)$$

$I'_{L\_offtime_n}$ is the off-time average inductor current value when load variation happened, and it's equal to the half sum of I'$_2$ and I'$_3$ in (59). ΔI_L is the inductor current variation before load transient which is equal to $\Delta I_{L_{n-1}} = V_{IN} / L\, D_{n-1} T_{S_{n-1}}$.

$$\begin{aligned} I'_1 &= I_L - \frac{\Delta I_{L_{n-1}}}{2} \\ I'_2 &= I'_1 + \frac{V_{IN}}{L} D_n T_{S_n} \\ I'_3 &= I'_2 + \frac{(V_{IN} - (V_{out\,n-1} - \Delta V_{out_n}))}{L} D_n' T_{S_n} \\ I'_2 + I'_3 &= 2I'_1 + 2\frac{V_{IN}}{L} D_n T_{S_n} + \frac{(V_{IN} - V_{out\,n-1})}{L} D_n' T_{S_n} + \frac{\Delta V_{out_n}}{L} D_n' T_{S_n} \end{aligned} \quad (59)$$

As above the ΔV_{out_n} can be expressed as (60).

$$\Delta V_{out_n} = \frac{I_{Load_n}}{C} D_n T_{S_n} - \frac{(I'_{L\_offtime_{n-1}} - I_{Load_{n-1}})}{C} D_{n-1}' T_{S_{n-1}} \quad (60)$$

$I'_{L\_offtime_{n-1}}$ is the off-time average inductor current value before load variation happened, which equal the inductor current dc component at light-load. By replacing equation (59) into $I'_{L\_offtime_n}$ the off-time average inductor current can be obtained as:

$$I'_{L\_offtime_n} = \frac{1}{2}(I'_2 + I'_3) = I_L - \frac{\Delta I_L}{2} + \frac{1}{2}\frac{V_{IN} D_n T_{S_n}}{L} + \frac{\Delta V_{out_n}}{L} D_n' T_{S_n} \quad (61)$$

To simplify the equation, we let the demand inductor current at light-load and heavy-load are I_L and $kI_L\,(k>1)$, respectively. So (60) can be simplified to (62).

$$\Delta V_{out_n} = \frac{I_L D_{n-1}'}{C}[D_n k T_{S_n} - D_{n-1} T_{S_{n-1}}] \quad (62)$$

According to (61) and (62), we will get (63)：

$$\begin{aligned} \Delta V_{C\_SDC_n} &= -V_{drop\_SDC_n} = \frac{T_{S_n}}{C}[I'_{L\_offtime_n} D_n' - I_{Load\,n}] \\ &= \frac{mT_{S_{n-1}} D_{n-1}'}{C}[\frac{V_{IN} D_{n-1} T_{S_{n-1}}}{2L}(m-1) - I_L(k-1) + \frac{mI_L D_{n-1}(D_{n-1}' T_{S_{n-1}})^2}{2LC}(mk-1)] \end{aligned} \quad (63)$$

Equation (63) means the output voltage total drop value during first transient period with

constant duty method. Comparing these two type controller, we want to know what a value of "m" will get to result in a much smaller output voltage drop when load step happened. In Table 1 organizes the comparative table of these two type control methods for boost converter.

Table 2. Comparative table of these two type control methods for boost converter.

Control Type / Parameter		***Duty-increasing***		***SDC***	
Time parameter (L=>H)	On-time	$t_{on_{n-1}}$	$t_{on_n} = t_{on_{n-1}} + \Delta t$	$t_{on_{n-1}}$	$t_{on_n} = t_{on_{n-1}} + \Delta t$
	Off-time	$t_{off_{n-1}}$	$t_{off_n} = t_{off_{n-1}}$	$t_{off_{n-1}}$	$t_{off_n} = t_{off_{n-1}} + \Delta t$
	Switch period ($1/F_S$)	$T_{S_{n-1}}$	$T_{S_n} = mT_{S_{n-1}}, m > 1$	$T_{S_{n-1}}$	$T_{S_n} = mT_{S_{n-1}}, m > 1$
Duty cycle (L=>H)	On-time	D_{n-1}	$D_n = D_{n-1} + \Delta D$	D_{n-1}	$D_n = D_{n-1}$
	Off-time	D_{n-1}'	$D_n' = D_{n-1}' - \Delta D$	D_{n-1}'	$D_n' = D_{n-1}'$
Load current：		$I_{Load_{n-1}}$	$I_{Load_n} = k \cdot I_{Load_{n-1}}$ $= k \cdot D_{n-1}' I_{Load_{n-1}}$	$I_{Load_{n-1}}$	$I_{Load_n} = k \cdot I_{Load_{n-1}}$ $= k \cdot D_{n-1}' I_{Load_{n-1}}$
Light-Load	Heavy-Load				
Indeed inductor current：		I_L	$I_L = k \cdot I_L (k > 1)$	I_L	$I_L = k \cdot I_L$ $(k > 1)$
Light-Load	Heavy-Load				
Off-time average inductor current ($I_{L\_offtime}$)		$I_{L\_offtime_n} = I_L + \frac{V_{IN}}{2L}[D_n T_{S_n} - D_{n-1} T_{S_{n-1}}] + \frac{\Delta V_{out_n} D_n' T_{S_n}}{2L}$		$I'_{L\_offtime_n} = I_L - \frac{\Delta I_L}{2} + \frac{1}{2}\frac{V_{IN} D_n T_{S_n}}{L} + \frac{\Delta V_{out_n}}{L} D_n' T_{S_n}$	
The V_{OUT} total drop value during first transient period ($\Delta V_C = -V_{drop}$)		$\Delta V_{C\_duty-increasing_n} = -V_{drop\_duty-increasing}$ $= \frac{T_{S_n}}{C}[I_{L\_offtime_n} D'_n - I_{Load_n}]$ $= \frac{mT_{S_{n-1}}}{C}\{\frac{V_{IN} T_{S_{n-1}}}{2L}[D_{n-1}(m-1) + m\Delta D] \cdot (D_{n-1}' - \Delta D) + I_L[(1-k)D_{n-1}' - \Delta D]$ $+ \frac{(D_{n-1}' - \Delta D) m T_{S_{n-1}}}{2L} \cdot \frac{I_L D_{n-1}' T_{S_{n-1}}}{C}[km(D_{n-1}' + \Delta D) - D_{n-1}]\}$		$\Delta V_{C\_SDC_n} = -V_{drop\_SDC_n}$ $= \frac{T_{S_n}}{C}[I'_{L\_offtime_n} D_n' - I_{Load_n}]$ $= \frac{mT_{S_{n-1}} D_{n-1}'}{C}[\frac{V_{IN} D_{n-1} T_{S_{n-1}}}{2L}(m-1) - I_L(k-1)$ $+ \frac{mI_L D_{n-1}(D_{n-1}' T_{S_{n-1}})^2}{2LC}(mk-1)]$	

3.1.3 The Switching Period Ratio "m"

In order to get less voltage drop by using constant duty method in transient state, we subtract (56) and (63) and find an available value "m".

$$\Delta V_{C\_SDC_n} - \Delta V_{C\_duty-increasing_n} = -V_{drop\_SDC_n} - (-V_{drop\_duty-increasing}) > 0 \qquad (64)$$

$$\Rightarrow m^2[kI_L D_{n-1}{}'T_{S_{n-1}}^2(\Delta D^2-\Delta D-D_{n-1}^2 D_{n-1}{}')]+m[V_{IN}\Delta DT_{S_{n-1}}C\cdot(2D_{n-1}+\Delta D-1)+$$

$$I_L T_{S_{n-1}}^2 D_{n-1}{}'\cdot(D_{n-1}^2 D_{n-1}{}'-D_{n-1}\Delta D)]+[2LCI_L\Delta D-V_S\Delta DD_{n-1}T_{S_{n-1}}C]>0 \quad (65)$$

Because there are square factor ($T_{S_{n-1}}^2$) in the first and second parts of equation (65) which are too small, we can ignore these parts with square factor ($T_{S_{n-1}}^2$) and just analyze the leaving portions. Equation (65) can be simplified as (66).

$$-V_{drop\_SDC_n}-(-V_{drop\_duty-increasing})$$

$$\cong m[V_{IN}\Delta DT_{S_{n-1}}C\cdot(2D_{n-1}+\Delta D-1)]+[2LCI_L\Delta D-V_S\Delta DD_{n-1}T_{S_{n-1}}C]>0 \quad (66)$$

From equation (66), we will get the minimum value of Switching Period Ratio "m" (67).

$$m\cdot V_{IN}\Delta DT_{S_{n-1}}C(2D_{n-1}+\Delta D-1)>V_S\Delta DD_{n-1}T_{S_{n-1}}C-2LCI_L\Delta D$$

$$\Rightarrow m>\frac{D_{n-1}-\dfrac{2LI_L}{V_{IN}T_{S_{n-1}}}}{2D_{n-1}+\Delta D-1} \quad (67)$$

That means if we choose "m" at least larger than the value as show in (67), then the voltage drop (V_{OUT}) in constant-duty method will be smaller than in constant-duty method. But the factor "m" is not an infinite value. Next we try to find the maximum value of factor "m", and then an available range will be defined.

3.1.4 The maximum value of factor "m"

In constant duty method, we assume the output voltage of the boost converter will recover to its original value during first time period (from t'$_1$ to t'$_3$) as show in Fig. 29. At this condition, the total charges that transfer from output capacitor to the load during off-time are equal to the amount of received charges output to capacitor during on-time.

$$Q_{discharge}=Q_{charge} \quad (68)$$

Then find the maximum value of factor "m". Replace transferring charges ($Q_{discharge}$ and

Q_{charge}) by the output capacitor (C_O) and the voltage variation across the output capacitor (ΔV_{C_on} and ΔV_{C_off} during on-time and off-time, respectively.).

$$\begin{aligned} &Q_{discharge} = Q_{charge} \\ &\Rightarrow C_O \cdot \Delta V_{C\_on} = C_O \cdot \Delta V_{C\_off} \\ &\Rightarrow \Delta V_{C\_on} = \Delta V_{C\_off} \end{aligned} \tag{69}$$

As above sections have been shown, the voltage variation (ΔV_{C_on} and ΔV_{C_off}) can be shown as (70) and (71.).

$$\Delta V_{C\_on} = \frac{I_{Load_n}}{C} D_n T_{S_n} \tag{70}$$

$$\Delta V_{C\_off} = \frac{(I_{L\_offtime_n} - I_{Load_n})}{C} D_n' T_{S_n} \tag{71}$$

$I_{L\_offtime_n}$ is the off-time average inductor current value when load variation happened. T_{S_n} is the new switching period by increasing on-time and off-time with the same ratio to keep duty cycle constant. Now we define ΔV_{C_n} a total voltage variation across output capacitor during the first time switching period after load changed.

$$\Delta V_{C_n} = -\frac{I_{Load_n}}{C} D_n T_{S_n} + \frac{(I_{L\_offtime_n} - I_{Load_n})}{C} D_n' T_{S_n} = \frac{T_{S_n}}{C} [I_{L\_offtime_n} D_n' - I_{Load_n}] \tag{72}$$

As section 3.1.2,

$$I_{L\_offtime_n} = \frac{1}{2}(I_4 + I_5) = I_L - \frac{\Delta I_L}{2} + \frac{1}{2}\frac{V_{IN} D_n T_{S_n}}{L} + \frac{\Delta V_{out_n}}{L} D_n' T_{S_n} \tag{73}$$

Finally ΔV_{C_n} is replacing by (73)

$$\Delta V_{C_n} = \frac{m T_{S_{n-1}} D_{n-1}'}{C} [\frac{V_{IN} D_{n-1} T_{S_{n-1}}}{2L}(m-1) - I_L(k-1) + \frac{m I_L D_{n-1} (D_{n-1}' T_{S_{n-1}})^2}{2LC}(mk-1)] \tag{74}$$

We assume that the output voltage variations during on-time and off-time at first time period are the same, so ΔV_{C_n} will equal to zero. So as show in (75)：

$$\frac{V_{IN} D_{n-1} T_{S_{n-1}}}{2L}(m-1) - I_L(k-1) + \frac{m I_L D_{n-1} (D_{n-1}' T_{S_{n-1}})^2}{2LC}(mk-1) = 0 \tag{75}$$

After organizing equation (75) then we will get the maximum value of factor “m”.

$$m^2[kI_L D_{n-1}(D_{n-1}{}'T_{S_{n-1}})^2]+m[V_{IN}D_{n-1}T_{S_{n-1}}C-I_L D_{n-1}(D_{n-1}{}'T_{S_{n-1}})^2]-[2\mathrm{I_L}\mathrm{LC(k\text{-}1)}+V_{IN}D_{n-1}T_{S_{n-1}}C]=0$$

$$\Rightarrow m=\frac{V_{IN}D_{n-1}T_{S_{n-1}}C+2\mathrm{I_L}\mathrm{LC(k\text{-}1)}}{V_{IN}D_{n-1}T_{S_{n-1}}C}=1+\frac{2\mathrm{I_L}\mathrm{L(k\text{-}1)}}{V_{IN}D_{n-1}T_{S_{n-1}}} \tag{76}$$

From section 3.1.3 and 3.1.4, the available range of time ratio “m” is：

$$\frac{D_{n-1}-\dfrac{2LI_L}{V_{IN}T_{S_{n-1}}}}{2D_{n-1}+\Delta D-1}<m<1+\frac{2\mathrm{I_L}\mathrm{L(k\text{-}1)}}{V_{IN}D_{n-1}T_{S_{n-1}}} \tag{77}$$

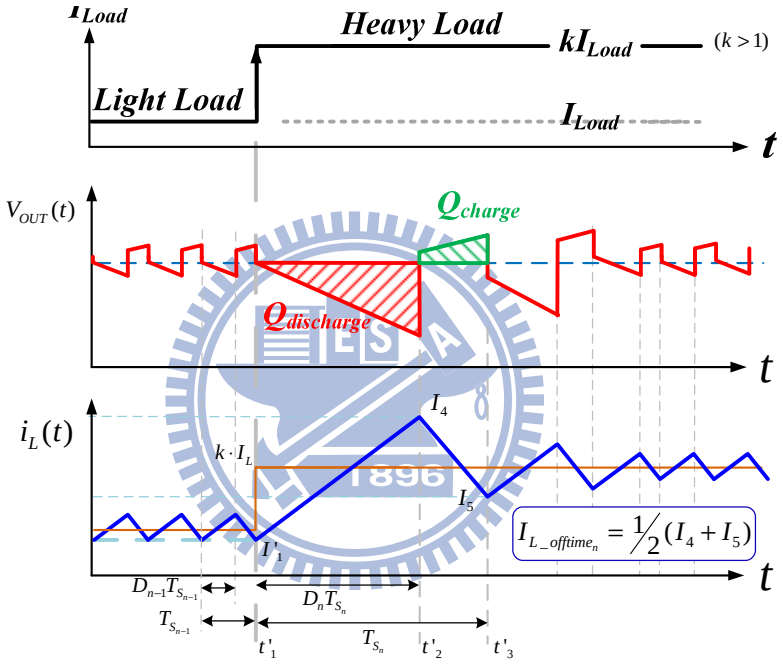


Fig. 29. Boost converter $V_{OUT}(t)$ and $i_L(t)$ waveforms using in constant duty

Moreover, we want the factor “m” be at least larger than 1. To achieve this requirement , some limitations are needed.

$$\frac{D_{n-1}-\dfrac{2LI_L}{V_{IN}T_{S_{n-1}}}}{2D_{n-1}+\Delta D-1}<1 \tag{78}$$

$$\Rightarrow T_{S_{n-1}}<\frac{2LI_L}{V_{IN}[1-(D_{n-1}+\Delta D)]} \tag{79}$$

$$\Rightarrow F_{S_{n-1}}>\frac{V_{IN}[1-(D_{n-1}+\Delta D)]}{2LI_L} \tag{80}$$

For example, a boost converter with V_{IN}=4V, V_{OUT}=12V, duty cycle D=2/3, inductor L=6.8uH, and the load step change from 50mA to 250mA (so the k=5). If we want achieve

(78), we should design the switching frequency at least 0.45MHz.

The larger ratio factor “m” we choose, the less the switching frequency happened at load state. As we know a reasonable limitation on the crossover frequency, ω_c, should be below 1/8 of the switching frequency. As you push the switching frequency lower, more issues with noise will arise (ringing and oscillation at output voltage (V_{OUT})) and influence the control system.

3.2 The Design Methodology

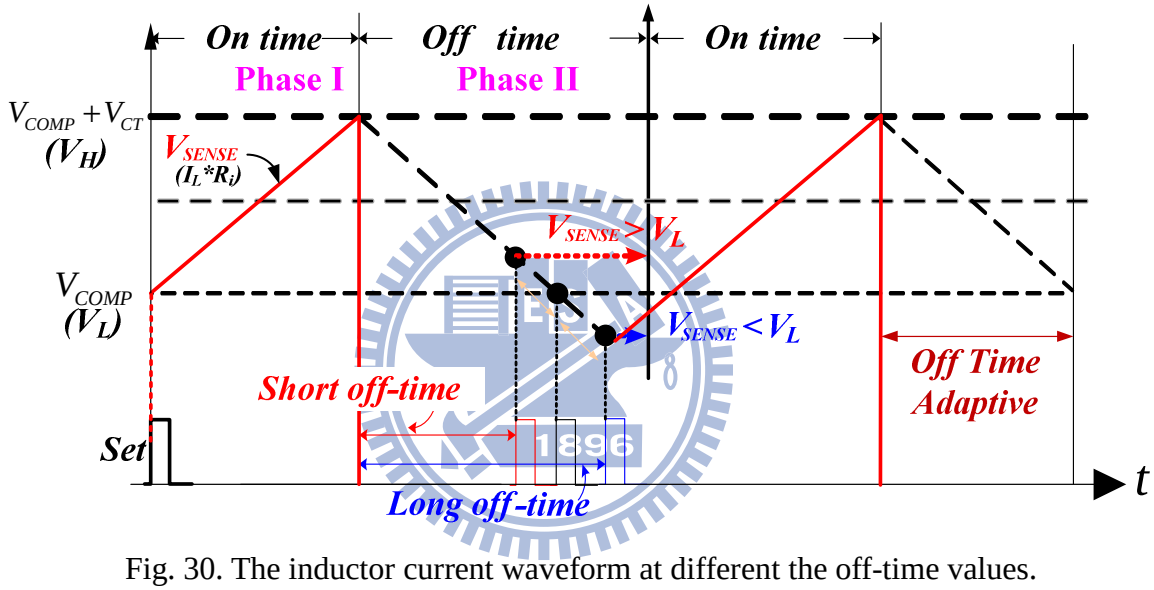


Fig. 30. The inductor current waveform at different the off-time values.

The signal V_{SENSE} is the transfer information about inductor current during on-time (phase I) sensed by the on-chip up-side current sensing circuit. The value of the off-time needs to be adaptively adjusted to ensure the accurate inductor current that can be controlled between the peak and bottom current levels. To adaptively adjust the value of the off-time, it is proposed that the SAR-controlled adaptive off-time calibrate the off-time value. That is, the duration of the off-time can be adjusted to regulate the bottom current level.

In Fig. 31 is the flow chart of the SAR-controlled adaptive off-time technique. The 8-bit SAR signal code A[7:0] is used to decide the duration of the off-time. At the beginning, the initial value of SAR code A[7:0] is “1000,0000” and the gain code G[7:0] is set to “0100,0000”. Adding or subtracting the gain code G[7:0] leads to the accurate calibration

values of the SAR code A[7:0] in the following eight switching cycles. When the current sensing signal V_{SENSE} at the beginning of the next switching cycle is larger than the expected value of V_{COMP} that means the duration of the off-time is too short, as shown in Fig. 30. Thus, the average inductor current is larger than expected value. At this moment, adding the gain codes G[7:0] to the SAR signal code A[7:0] to prolong the off-time. On the other hand, if the off-time is too long, the current sensing signal (V_{SENSE}.) at the beginning of the next switching cycle will be smaller than the V_{COMP}. That means, the average inductor current is relatively smaller than expected value, and therefore, the SAR signal code A[7:0] will subtract the gain code G[7:0].

After the eight switching cycles, the adaptive off-time can be get from SAR signal code A[7:0] adjusted by a minimum value of the gain code G[7:0], which is "0000,0001," according to the value of the comparison result of the voltage V_{SENSE} and the reference voltage V_{COMP}. Consequently, after the calibration duration, the adaptive off-time can ensure that the bottom level of the inductor current will be close to the expected value.

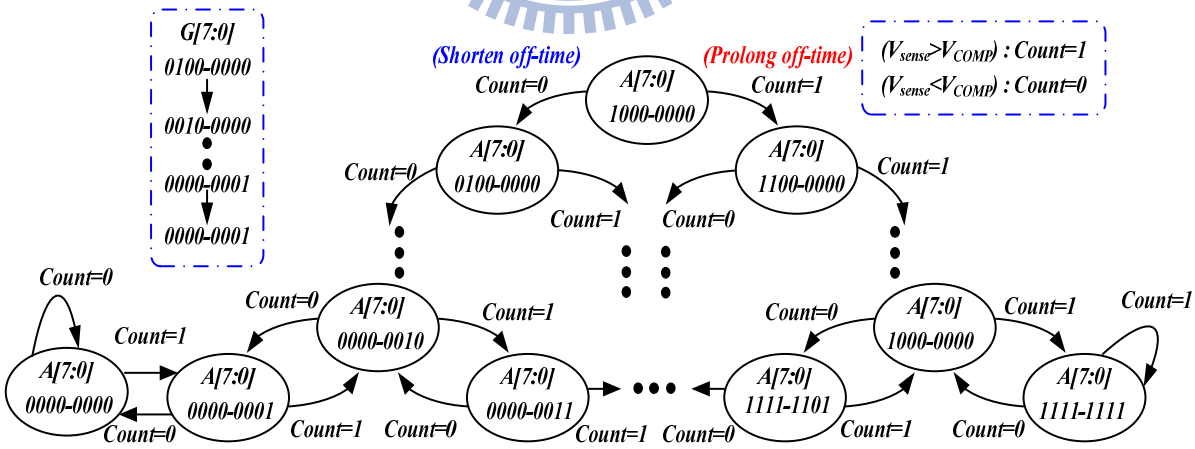
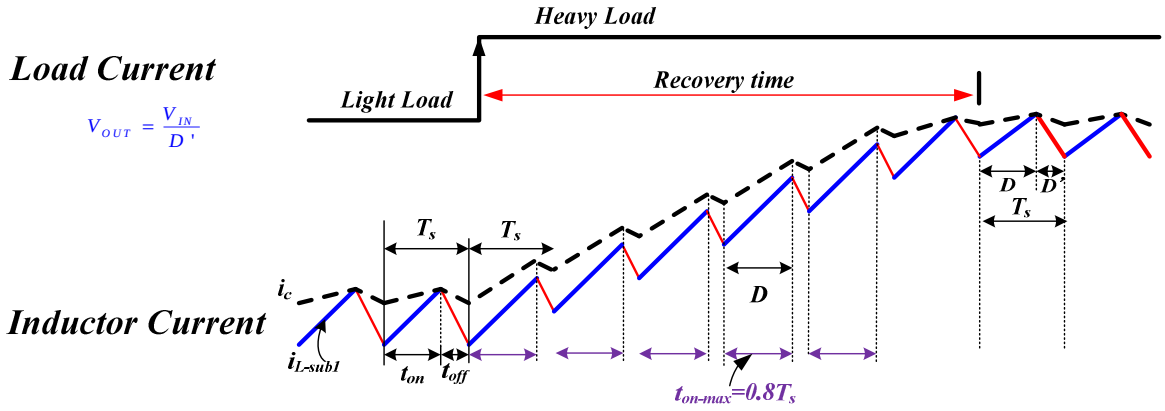


Fig. 31. The operation of the adaptive SAR code A [7:0] by means of the gain code G[7:0].

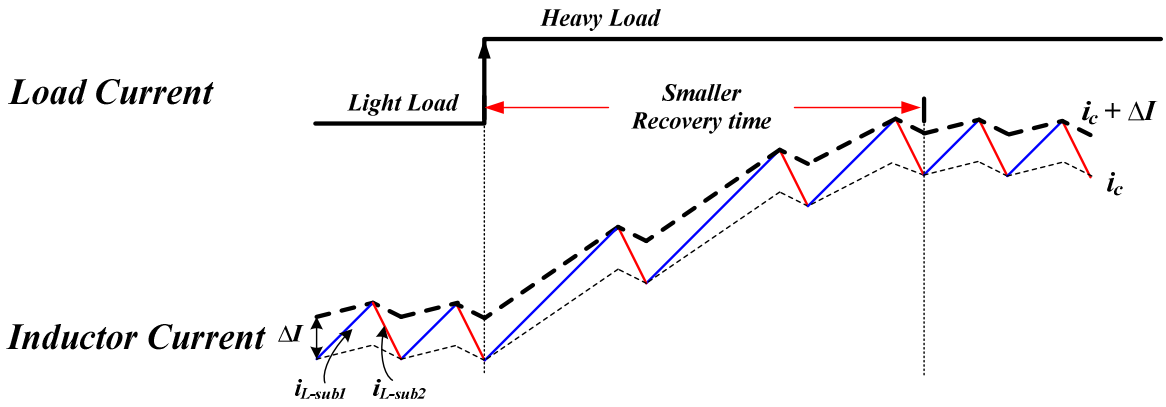
3.3 The AHW and VTE Techniques in SDC

The converters operate in PWM mode have fixed switching frequency, the switch has to

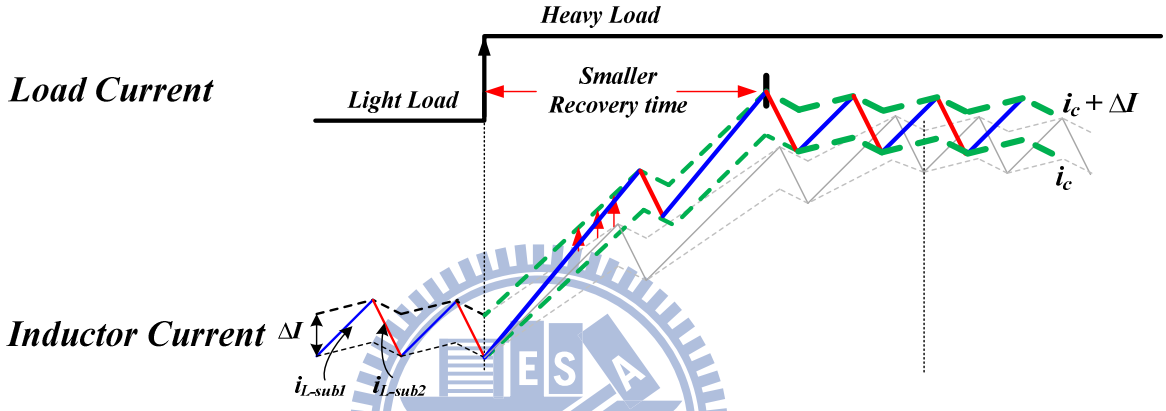
turn on and off during every switching cycle. The average inductor current takes a longer time to reach to needed value as shown in Fig. 32(a) when the load current changes from light to heavy. So does the output voltage recovery time. When the converter works in HCC technique, the inductor current is controlled within two boundaries $\boldsymbol{i_c}$, which is determined by the error amplifier, and $\boldsymbol{i_c}$ +Δ*I* as depicted in Fig. 32(b). The Δ*I* is the current hysteresis window. Unlike the PWM control technique, because the on-time value can be extended and does not be limited, the recovery time will be shortened. The switching period can also be extended and thus the inductor current can be rapidly increased to the regulated level. The current of $\boldsymbol{i_{L\_sub1}}$ gets more time to reach the top boundary ($\boldsymbol{i_c}$ +Δ$I_)$. Hence, the boost converter slows down the system frequency when load current varies from light to heavy. This is the reason why he HCC technique has smaller recovery time than that of the current-mode PWM technique. When the converter works in HCC technique and contains transient enhancement (VTE) controller. Like in HCC technique the inductor current is controlled within two boundaries $\boldsymbol{i_c}$. The VTE controller instantly increases the slope of the hysteresis window to further increase the speed of transient response when the load changes from light to heavy. The behaviour waveform is shown in Fig. 32(c).



(a)



(b)



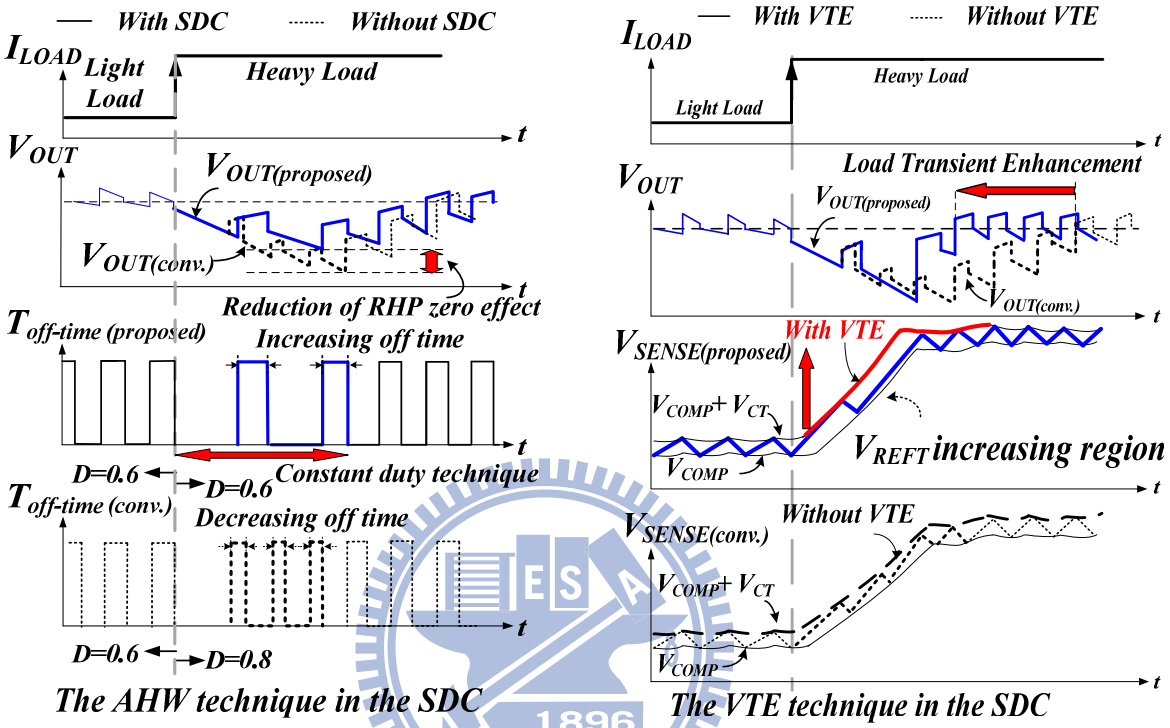
(c)

Fig. 32. Recovery time during light load to heavy load: (a) The waveforms controlled by the PWM technique. (b) The waveforms controlled only by the new HCC technique.

When the converter works in HCC technique and contains transient enhancement (VTE) controller. Like in HCC technique the inductor current is controlled within two boundaries $\boldsymbol{i_c}$. The VTE controller instantly increases the slope of the hysteresis window to further increase the speed of transient response when the load changes from light to heavy. The behaviour waveform is shown in Fig. 32(c).

As shown in Fig. 33(a), the increasing on time results in the off-time and the energy delivered to the output initially decrease in conventional design when load current changes from light to heavy. The output voltage, V_{OUT}(conv.), has a large drop voltage since the RHP zero causes the output initially tends in wrong direction during transient response. The adaptive hysteresis window (AHW) controller keeps the duty constant during load transient

period since the increasing on-time accompanies the increasing off-time. Therefore, the output voltage, V_{OUT} (proposed), has a smaller dip voltage compared to conventional designs. That is, the AHW technique reduces the RHP zero effect.



(a) (b)

Fig. 33. (a) The reduction of drop voltage and transient response are achieved by the AHW controller. (b) The reduction of drop voltage and transient response are achieved by the VTE controller.

However, it is obvious to see that the transient response time doesn't change owing to the same bandwidth. The proposed variable transient enhancement (VTE) controller can instantly increases the slope of the hysteresis window to further increase the speed of transient response. As depicted in Fig. 33(b), the inductor current can be raised to the rated value to reduce transient response time. A fast transient boost converter with a small dip voltage can be guaranteed by the SDC and VTE controllers.

Chapter 4

The System Implementations and Simulation Results

The proposed MHCC technique contains two main blocks. One is the HCC circuit and the other one is ACC circuit. The current sensor and the fixed hysteretic current window circuit constitute the HCC circuit. The adaptive compensation resistance and capacitance circuits and the ACC controller constitute the ACC circuit. []

4.1 Constant Transconductance Bias Circuit

The constant transconductance bias circuit is shown in Fig. 34. First, it is assumed that $(W/L)_{6,7} = (W/L)_{9,8}$. This equality results in both sides of the circuit having the same current due to the current-mirror pair M6~M9. As a result, we also must have $I_{D2}=I_{D3}$. Now, around the loo consisting of M2, M3, and R_B, we have

$$V_{GS3} = V_{GS2} + I_{D2} \cdot R_B \tag{81}$$

and recalling the overdrive voltage ($V_{OV}=V_{GSi}-V_t$), Subtract the threshold voltage, V_t, from both sides, resulting in

$$V_{OV13} = V_{OV15} + I_{D2} \cdot R_B \tag{82}$$

This equation can also be written as

$$\sqrt{\frac{2I_{D3}}{\mu_n C_{OX}(W/L)_3}} = \sqrt{\frac{2I_{D2}}{\mu_n C_{OX}(W/L)_2}} + I_{D2} \cdot R_B \tag{83}$$

Rearranging, we obtain

$$\frac{2}{\sqrt{2\mu_n C_{OX}(W/L)_3 I_{D3}}}[1-\sqrt{\frac{(W/L)_3}{(W/L)_2}}]=R_B \tag{84}$$

And recalling that $g_{m3}=\sqrt{2\mu_n C_{OX}(W/L)_3 I_{D3}}$ results in the important relationship

$$g_{m3}=\frac{2[1-\sqrt{\frac{(W/L)_3}{(W/L)_2}}]}{R_B} \tag{85}$$

Thus, the transconductance of M3 is determined by geometric ratios only, independent of power-supply voltage, process parameters, temperature, or any other parameters with large variability. Not that, not only is g_{m3} stabilized, but all other transconductances are also stabilized, since all transistor currents are derived from the same biasing network, and, therefore, the ratios of the currents are mainly dependent on geometry. We thus have, for all n-channel transistors,

$$g_{mi}=\sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_3 I_{D3}}}\cdot g_{m3} \tag{86}$$

And for all p-channel transistors

$$g_{mi}=\sqrt{\frac{\mu_p}{\mu_n}\cdot\frac{(W/L)_i I_{Di}}{(W/L)_3 I_{D3}}}\cdot g_{m3} \tag{87}$$

The bias circuit just presented is an example of a circuit having positive feedback. It is stable as long as the loop gain is less than unity, which is the case when $(W/L)_2/(W/L)_3>1$. The n-channel wide-swing cascade current mirror consists of transistors M1~M4, along with the diode-connected biasing transistor M5. The current for this biasing transistor is actually derived from the bias loop via M10 and M11. Similarly, M14 is the biasing transistor for current mirror consists of transistors M6~M9, which has a bias current derived from the bias loop via M12 and M13. The start-up circuit consists of transistors M15~M18 that affects only

the bias-loop in the case that all currents in the loop are zero. In the event that all currents in the bias loop are zero, M17 will be turn off. Since M18 operates as a high-impedance load that is always on, the gates of M15 and M16 will be pulled high. These transistors then will inject currents into bias loop, which will start-up the circuit. Once the loop start-up, M17 will turn on, sinking all of the current from M18, pulling the gates of M15 and M16 low, and thereby turning them of so they no longer affect the bias loop.

It is of interest to not that the bias circuit shown consists of four different loops – the main loop with positive feedback, the start-up loop that eventually gets the two loops used for establishing the bias voltages for the cascade transistors. These latter two loops also constitute positive feedback but with very little gain.

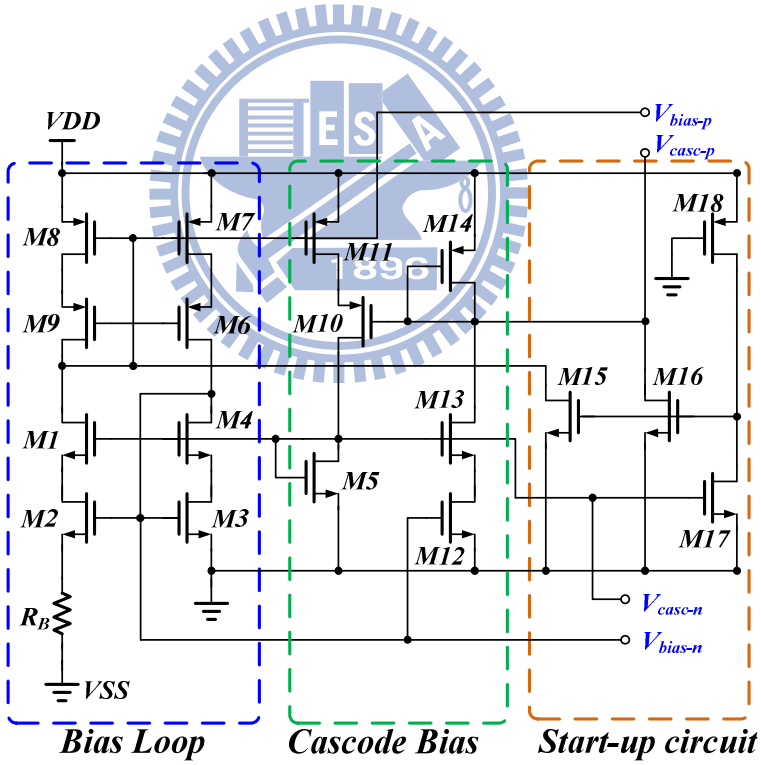


Fig. 34. A constant-transconductance bias circuit having wide-swing cascode current.

4.2 The Implementation of the SAR-controlled Modulator

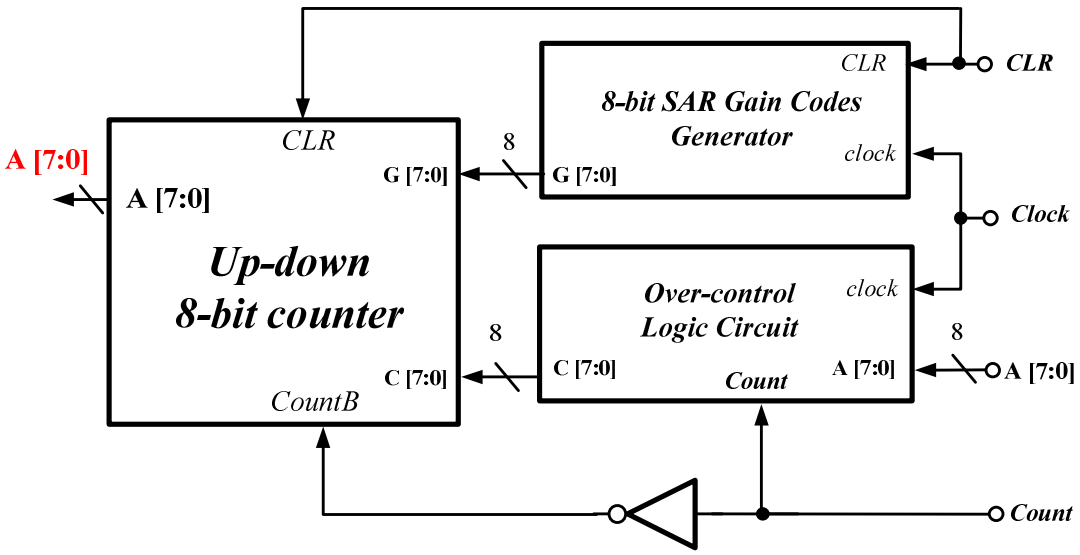


Fig. 35. The structure of the SAR-controlled modulator.

The implementation of the SAR-controlled modulator is used to control the off-time value of the converter. The modulator is consisted by three sub-modules as shown in Fig. 35. They are the up-down 8-bit counter, the 8-bit SAR gain code generator, and the over-control logic circuit. The up-down 8-bit counter is used to calculate a new 8-bit SAR code A[7:0] and a gain code G[7:0] according to the digital signal *Count*. The 8-bit SAR gain code generator provides G[7:0] to the up-down 8-bit counter to calculate the precise A[7:0]. The C[7:0] is generated by over-control logic circuit to detects A[7:0] to avoid the overflow issue.

4.2.1 The Up-down 8-bit counter

The up-down 8-bit counter circuit is consisted by eight full-adders and eight XOR as shown in Fig. 36. The SAR signal code A[7:0] starts from '10000000', the gate DFF8 utilizes the complement of the *Q* signal when the signal *CLR* is high. Therefore, A[7:0] starts from '10000000' after the clear state. The signal "*Count B*" is decided by whether the V_{SNESE} is smaller than V_{COMP}, or not. According to the signal "*Count B*", the eight XOR will be decided the operation ins an addition or a subtraction. Additionally, "*Count B*" is also used as the carry-in signal of the first full-adder to achieve the correct calculation. When V_{SENSE} is larger than V_{COMP} (off-time is too long), "*Count B*" is '1'. The G[7:0] will be converted into its 2's

complement value. Hence, A[7:0] subtracts G[7:0] to shorten the off-time duration. On other hand, if "*Count B*" is '0' (off-time is too short), G[7:0] is not complemented. That is, the addition is proceeded by the SAR-controlled modulator and A[7:0] is equal to the sum of the previous value and G[7:0] to prolong the off-time duration. Fig. 37 shows the simulation result of the up-down 8-bit counter.

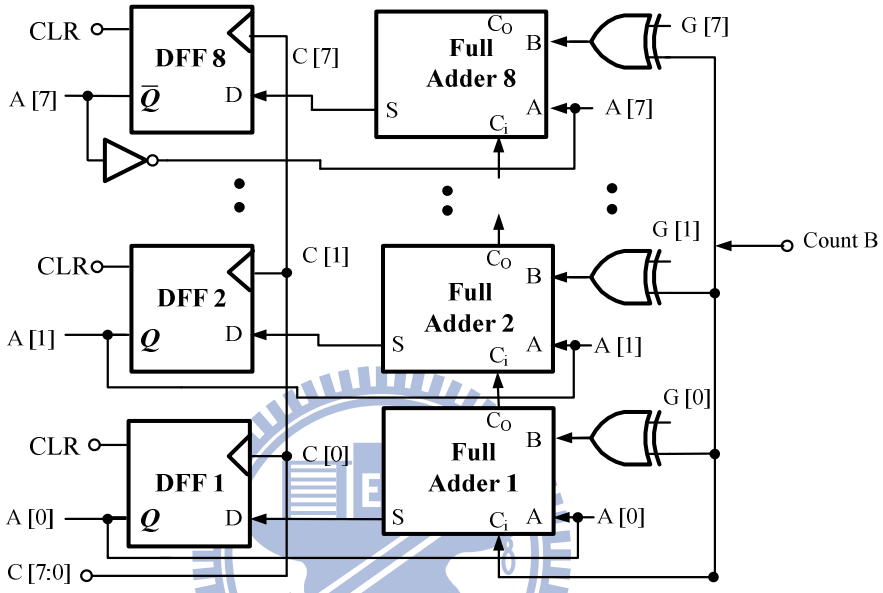


Fig. 36. The up-down 8-bit counter.

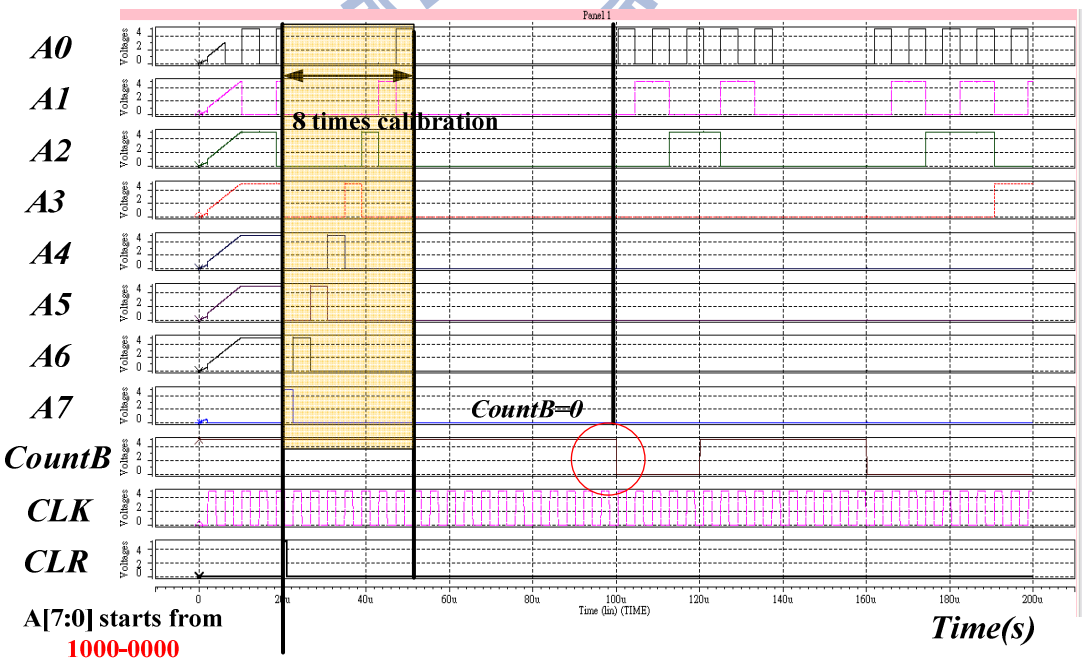


Fig. 37. Simulation result of the up-down 8-bit counter.

4.2.2 The 8-bit Gain Code Generator

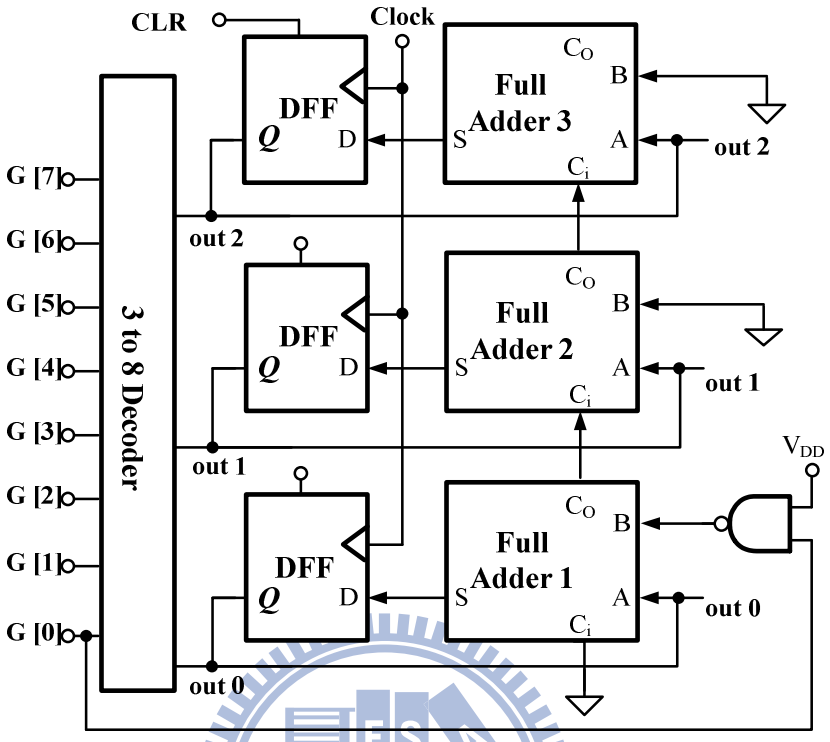


Fig. 38. The 8-bit SAR gain code generator.

The 8-bit gain code generator is consisted in three full adders and three D flip flop shown in Fig. 38. The gain code G[7:0] starts from ‘01000000’ to ‘00000001’. At the beginning, set the binary code [out2, out1, out0] to ‘000’ and converted by the 3-to-8 decoder so that G[7:0] can be set as ‘01000000’. The full adders are used to generate the increasing binary code [out2, out1, out0] from ‘000’ and G[7:0] is converted from ‘01000000’ to ‘00000001’ by the 3-to-8 decoder. Until the gain code G[0] is changed from ‘0’ to ‘1’, the input B of the full adder 1 becomes ‘0’ and the binary code [out2, out1, out0] will be settled. This indicates the end point of the calibration of the SAR operation. After eight cycles, the SAR-controlled modulator starts to slightly adjust A[7:0] by setting the minimum G[7:0] as ‘00000001’.

4.2.3 The Over-control Logic Circuit

Fig. 39 is the over-control logic circuit. The AND gate array is used to block the clock *CLK* when the overflow issue happens. When V_{SENSE} is higher than V_{COMP} (value of the signal

CountB is ‘1’), the operation of the up-down 8-bit counter is in the adding operation. If A[*7:0*] is ‘11111111’, the output of the XOR gate array is ‘0’ to block the clock signal *CLK*. Thus the over-control signal C[7:0] holds to ‘00000000’. For the subtraction function, the up-down 8-bit counter needs to prevent the value of the SAR code A[7:0] from continuously decreasing when A[7:0] is ‘00000000’. When the function of subtraction is enabled by the *CountB*, it also prevents the overflow issue from happening through the XOR gate array. The SAR-controlled modulator with three sub-modules can generate A[7:0] through the digital signal *Count* to adjust the dynamic off-time. When *Count* is ‘0’ or ‘1’, the SAR code will subtract or add G[7:0] as ‘00000001’.

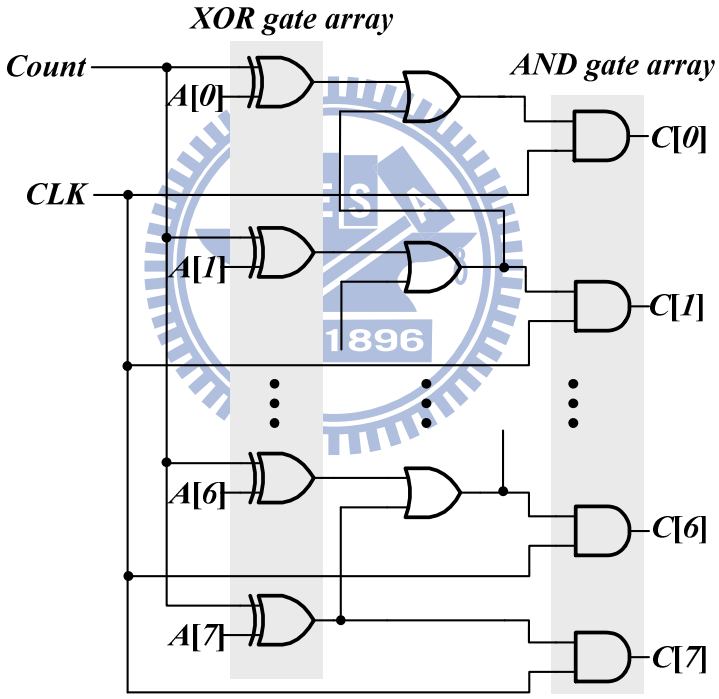


Fig. 39 The over-control logic circuit.

4.3 The Implementation of the Adaptive Off-time Circuit

The simple implementation of the adaptive off-time circuit is depicted in Fig. 40. After this circuit calculation, the off-time can be dynamically adjusted to get the accurate average inductor current. When the signal control is high (V_{PWM} = 1), the non-inverting input of

comparator V_{ca} is discharged to ground and the output of comparator is low (*Set* = zero). When the signal control is changed to low, the constant biasing current I_B will flow into the capacitor C_{off} to increase V_{ca}. Once V_{ca} is larger than the voltage V_{BG}, the output of comparator is low (*Set* = 1) to start the next switching cycle. Thus, the off-time duration can be expressed as (88).

$$t_{off} = \frac{C_{off} V_{BG}}{I_B} \tag{88}$$

Where t_{off} is proportional to the value of the capacitor C_{off}. Therefore, the adaptive off-time circuit as illustrated in Fig. 40 utilizes the SAR codes to adjust the value of the capacitor for the suitable off-time t_{off}. A[7:0] turns on/off the switches in the SAR-controlled capacitor array to decide the total value of C_{off} when the input enable signal *EN* is high. Each bit in A[7:0] indicates the additional capacitor. As such, C_{off} can be expressed as (89):

$$C_{off} = C \times (2^0 \cdot A_7 + 2^{-1} \cdot A_6 + \ldots + 2^{-7} \cdot A_0 + 2^{-7}) \tag{89}$$

Thus, the maximum and minimum values of the capacitor are *2C* and *C/128*, respectively.

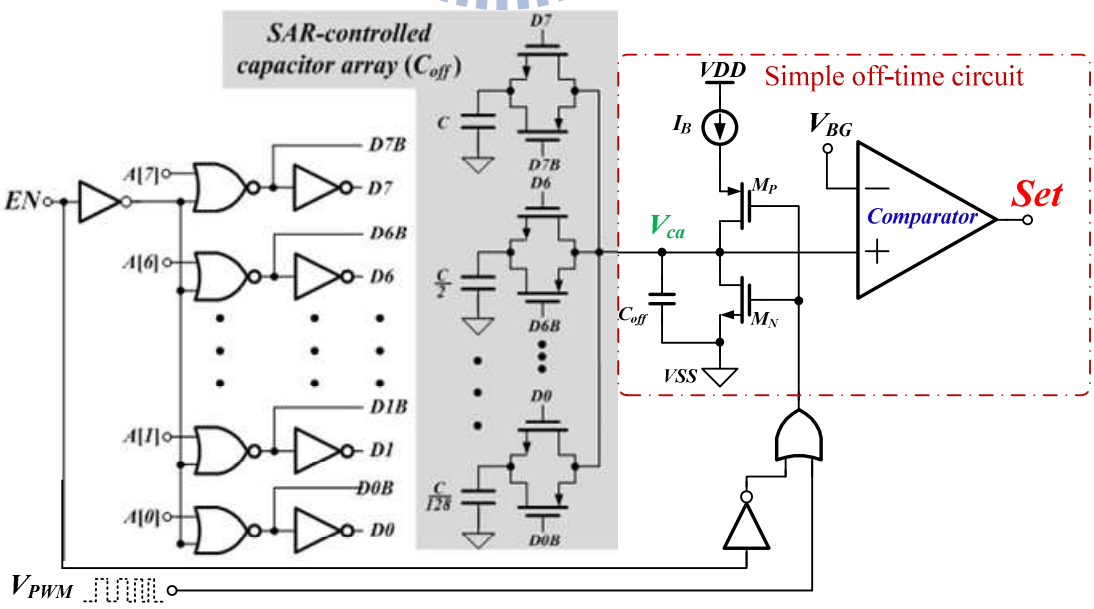


Fig. 40. The schematic of the adaptive off-time circuit and the corresponding capacitor according to each bit of the SAR code A[7:0].

4.4 P-Compensator Circuit

The P-compensator circuit structure is shown in Fig. 41. This circuit can be seen as one of transconductance (Gm) amplifier structure, the main function is transferring the input error voltage to the output current.

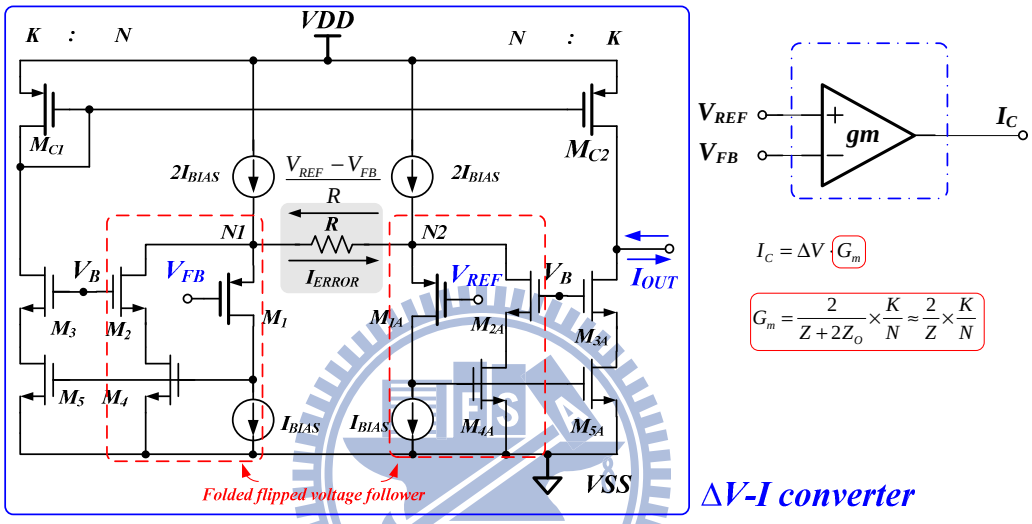


Fig. 41. Schematic of the P-Compensator.

When the input voltage V_{FB} is equal to V_{REF}, the node N_1 is equal to the node N_2 (due to voltage follower). Thus, no current pass through the resistor R. The current on the transistor M_{B3} and M_{B4} equal to the summation of the current on the transistor M_1, M_{1A} and M_2, M_{2A} respectively, the current on the transistor M_{C2} equals to the current on the transistor M_{3A} and M_{5A}. As a result, the output current I_{OUT} equals to zero.

When the input voltage V_{FB} is smaller than V_{REF}, the node N_1 is larger than the node N_2. There is an error current I_{ERROR} flows from the node N_1 to node N_2 across the resistor R. Hence, the output stage current I_{OUT} can sink the current. On the contrary, when the input voltage V_{FB} is larger than V_{REF}, the output stage current I_{OUT} can source the current.

The transconductance amplifier can transform the voltage difference to error current. The trnasconductance of P-Compensator can be written as Eq. (90). The trnasconductance has to

consider the output impedance $\boldsymbol{Z_o}$ of node $\boldsymbol{N_1}$ and the node $\boldsymbol{N_2}$.

$$G_m \approx \frac{2}{Z + 2Z_O} \times \frac{K}{N} \tag{90}$$

As shown in Eq. (90), the factor ***2(K/N)*** is generated by current mirror circuits including the transistor $\boldsymbol{M_2}$, $\boldsymbol{M_3}$, $\boldsymbol{M_{2A}}$, $\boldsymbol{M_{3A}}$, $\boldsymbol{M_{C1}}$ and $\boldsymbol{M_{C2}}$.

As shown in Fig. 42, the input stage of P-Compensator is voltage follower. In Fig. 42(a), the output impedance of original voltage follower is shown as Eq. (91). To reduce the output impedance and improves the P-Compensator linearity, the folded voltage follower is implemented, as illustrated in Fig. 42(b). This structure can reduce output impedance effectively and the output impedance is shown in Eq. (92). But the main disadvantage is input swing depends on the threshold voltage, it becomes very small in modern CMOS technology. The input swing can be written as Eq. (93). For a wider input swing range, the folded flipped voltage follower is implemented, as illustrated in Fig. 42(c). This structure not only reduces output impedance but also improves the input swing range. The output impedance of the folded flipped voltage follower and the input swing range is shown in Eq. (94) and Eq. (95) respectively. By using the folded flipped voltage follower as P-Compensator input stage, the output impedance on the node $\boldsymbol{N_1}$ and node $\boldsymbol{N_2}$ in Fig. 41 is greatly reduced, and the linearity of P-Compensator approaches to ideal value.

$$Z_O \approx \frac{1}{gm_1} \tag{91}$$

$$Z_O \approx \frac{1}{gm_2} \frac{1}{gm_1 r_{o1}} \tag{92}$$

$$V_{in}^{swing} = V_{GSM1} - V_{DSM2}^{sat} - V_{DSM1}^{sat} = V_T - V_{DSM2}^{sat} \tag{93}$$

$$Z_O \approx \frac{1}{gm_2} \frac{1}{gm_1 r_{o1}} \tag{94}$$

$$V_{in}^{swing} = V_{dd} - V_{GSM1} - V_{DS2Ib} \tag{95}$$

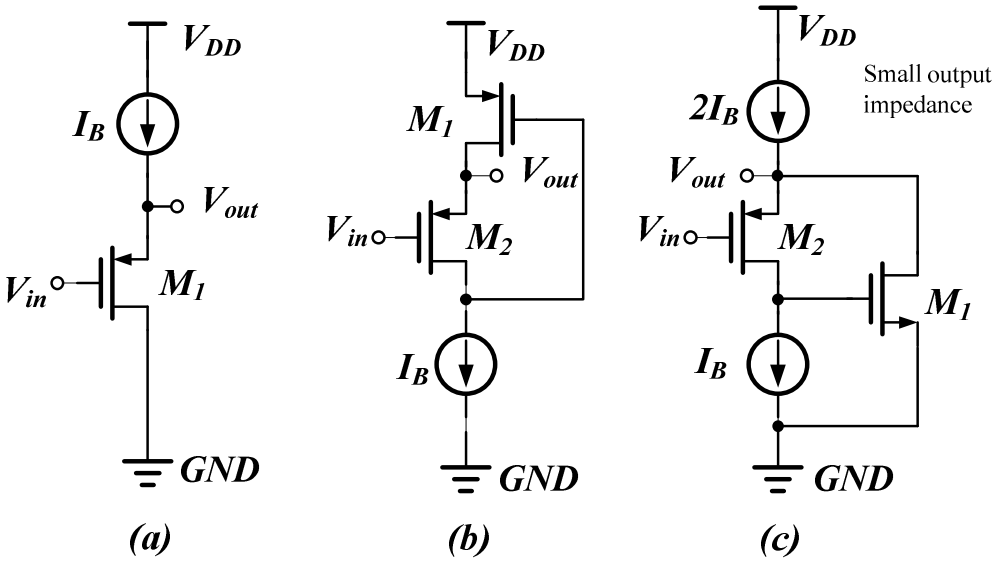


Fig. 42. Schematic of different P-Compensator input stages. (a) Voltage follower. (b) Folded voltage follower. (c) Folded flipped voltage follower.

The simulation result is shown on Fig. 43, where the upper wave is feedback and reference voltage respectively; the lower wave is an output current I_{OUT}.

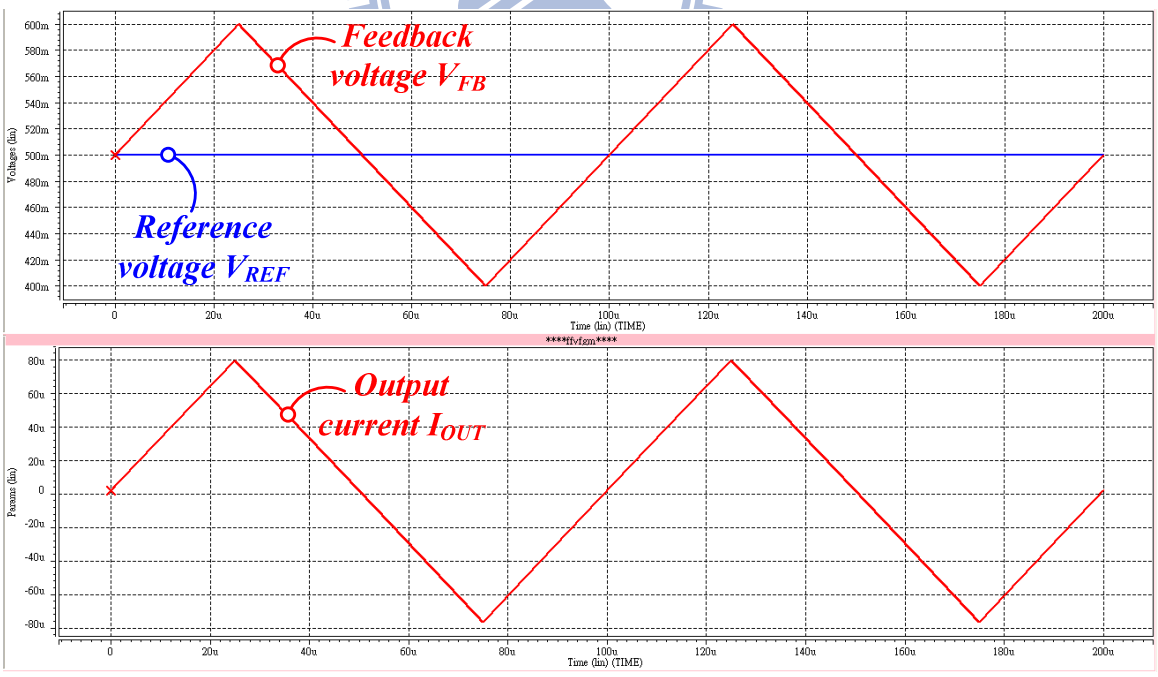


Fig. 43. The simulation result of P-Compensator

The comparison result of linearity between ideal and actual transconductance is shown on TABLEV, the accuracy is about 95%.

Table 3. The linearity between ideal and actual transconductance.

Ideal transconductance	***800 μA/V***
Actual transconductance	***761.2 μA/V***
Accuracy	***95.15%***
Test waveform	***Triangular form with 0.2V amplitude***

4.5 Error Amplifier Circuit

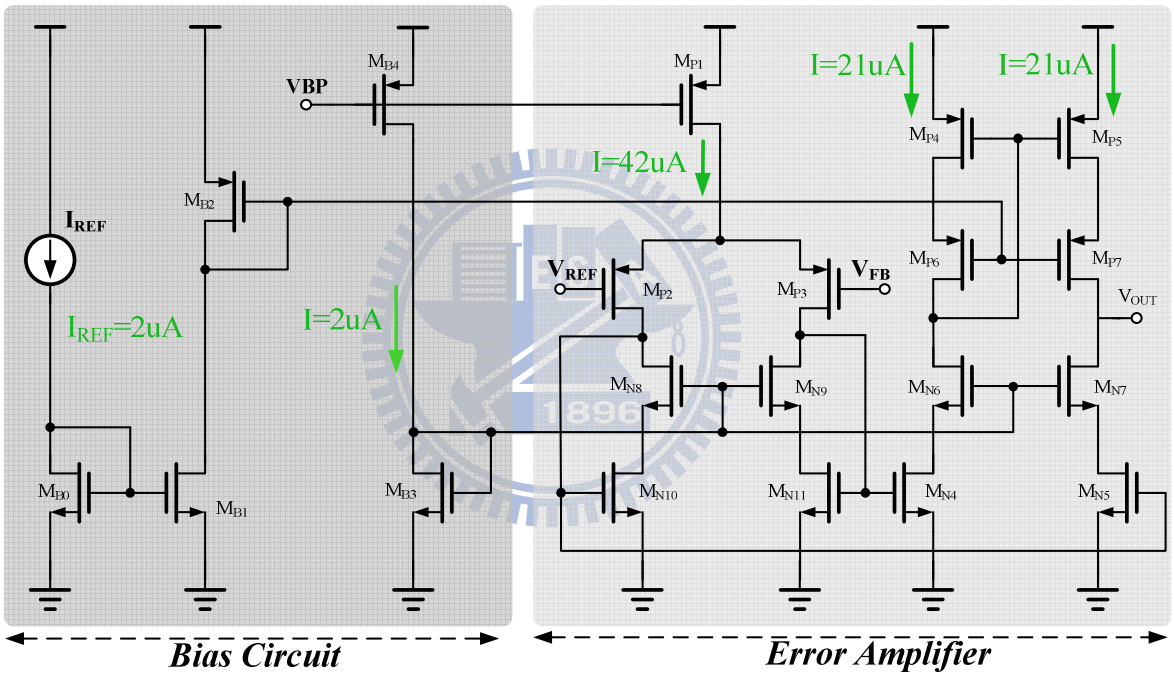


Fig. 44. The schematic of error amplifier

The error amplifier is used to amplify the error of feedback voltage (V_{FB}) and reference voltage (V_{REF}). The error amplifier is as the operational transconductance amplifier (OTA). The high current driving ability is the characteristic of OTA. Therefore, the OTA is suitable for the boost converter with large compensate capacitor. The circuit structure of the operational transconductance amplifier is shown in Fig. 44 The transistors M_{B0}-M_{B4} produce the biasing current to bias the error amplifier. The transistors M_{P2} and M_{P3} form the input differential pair with cascode-mirror loads that are constructed by the transistors M_{N4}-M_{N11}

and M_{P4}-M_{P7}.

The simulation result of the operational transconductance amplifier is shown in Fig. 45. The dc gain of the error amplifier in this design is about 74dB for all corners. The unity gain frequency is 0.67 MHz and the phase margin is 88° with the capacitive load 10pF. Other details about this OTA are shown in table 4.

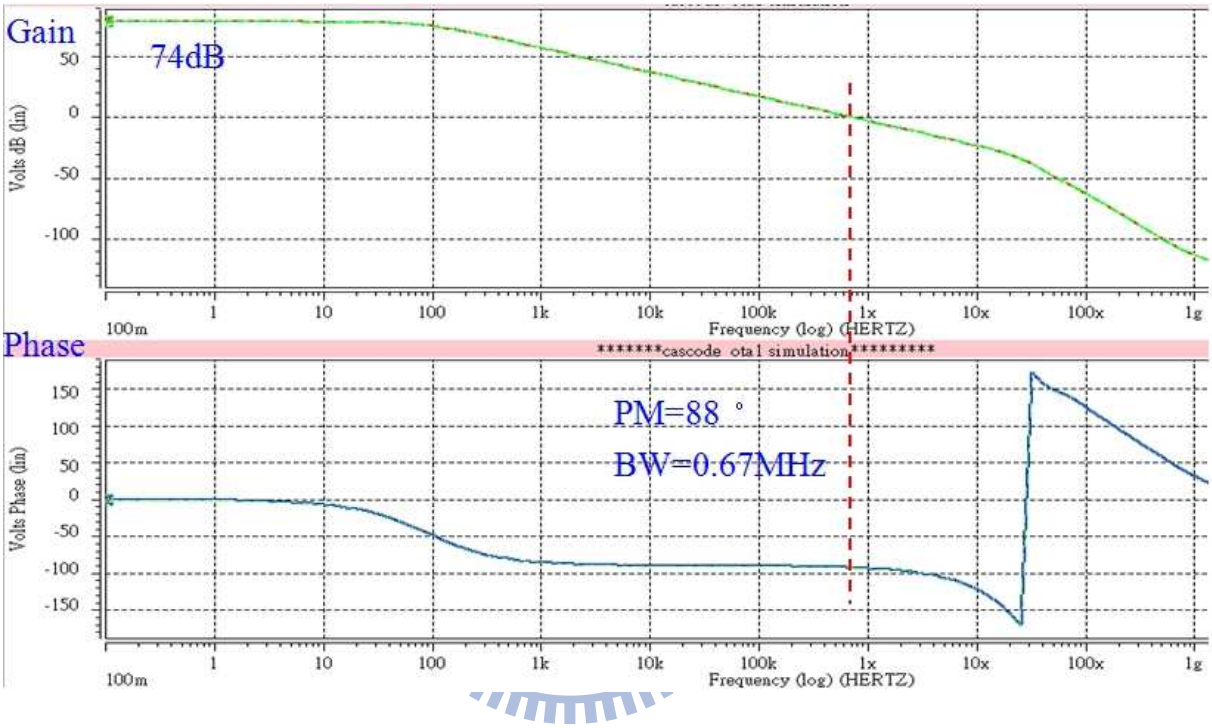


Fig. 45. The simulation result of error amplifier.

Table 4. The specifications of the error amplifier

Specifications	***Value***
Supply Voltage (V_{IN})	3.3V-4V
Temperature	0℃-120℃
Input Common-Mode Range (ICMR)	0.3V~3.5V
Output Swing	1.13~3.3V
Minimum Voltage Gain (A_V)	78.4dB
Transconductance	276.6u

4.6 The Structure of the VTE Controller

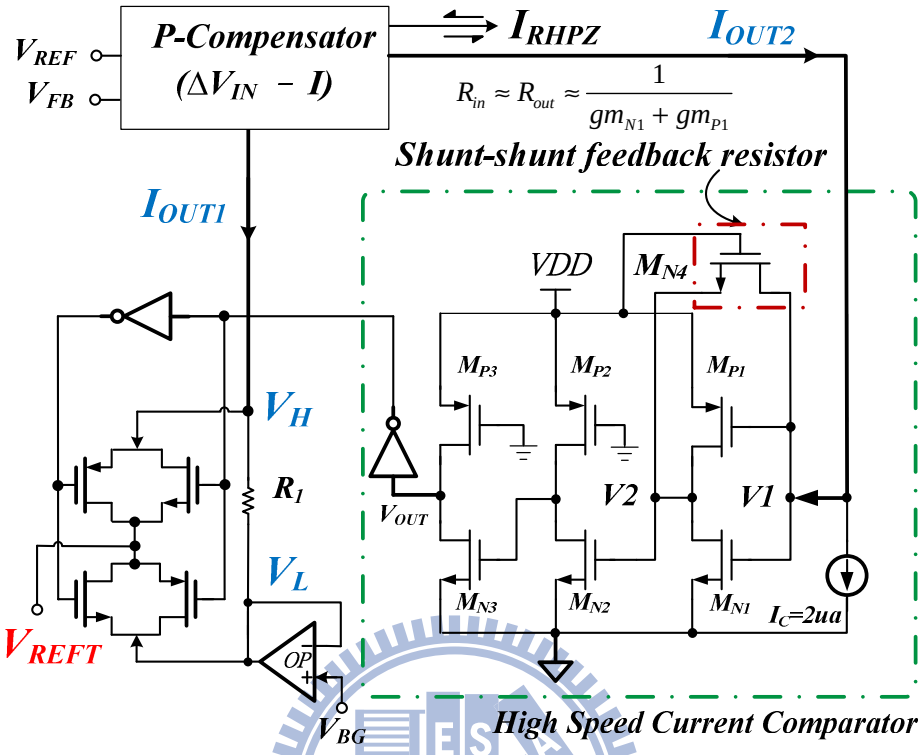


Fig. 46. The structure of the VTE controller.

The proposed variable transient enhancement (VTE) circuit is shown in Fig. 46 [10], it consists of two parts, the high speed current comparator circuit and the p-compensator. The high speed current comparator circuit comprises one CMOS complementary amplifier (M_{N1}–M_{P1}), two resistive-load amplifiers (M_{N2}, M_{N3}, M_{P2}, M_{P3}) and one CMOS inverters .M1 and M2 both work in saturation region, and the transistor M5 working in linear region which acts as the negative feedback resistor of the CMOS complementary amplifier. According to small-signal analysis, the input and output resistances of the CMOS complementary amplifier with a feedback resistor can be expressed as

$$R_{in} = \frac{R_4 + R_P}{1 + (g_{m1} + g_{m2})R_P} \tag{96}$$

$$R_{out} = \frac{R_4 + R_C}{1 + (g_{m1} + g_{m2})R_C + (g_4 + g_C)/R_P} \tag{97}$$

where $R_P = (r_{ds1} // r_{ds1})$, g_{m1} and g_{m2} are the transconductances of M1 and M2 respectively, R_4 is the on-resistance of M4, R_C is output resistance of input current source. Because generally R5 << R_P, R5 << R_C, and ($g_{m1} + g_{m2}$) R_P,>>l exist, it can be concluded as follows

$$R_{in} \cong R_{out} \cong \frac{1}{g_{m1} + g_{m2}} \tag{98}$$

These small input and output resistances can reduce the voltage swings at node 1 and 2, so the response time of the comparator will be greatly decreased. To amplify the small voltage swing at node 2, two resistive-load amplifiers are used to provide additional gains. The last one CMOS inverters can output a rail-to-rail compared result signal. This current comparator has no external bias currents and bias voltages, so the process deviation immunity is enhanced. The simulation of the high speed current comparator is shown in Fig. 47

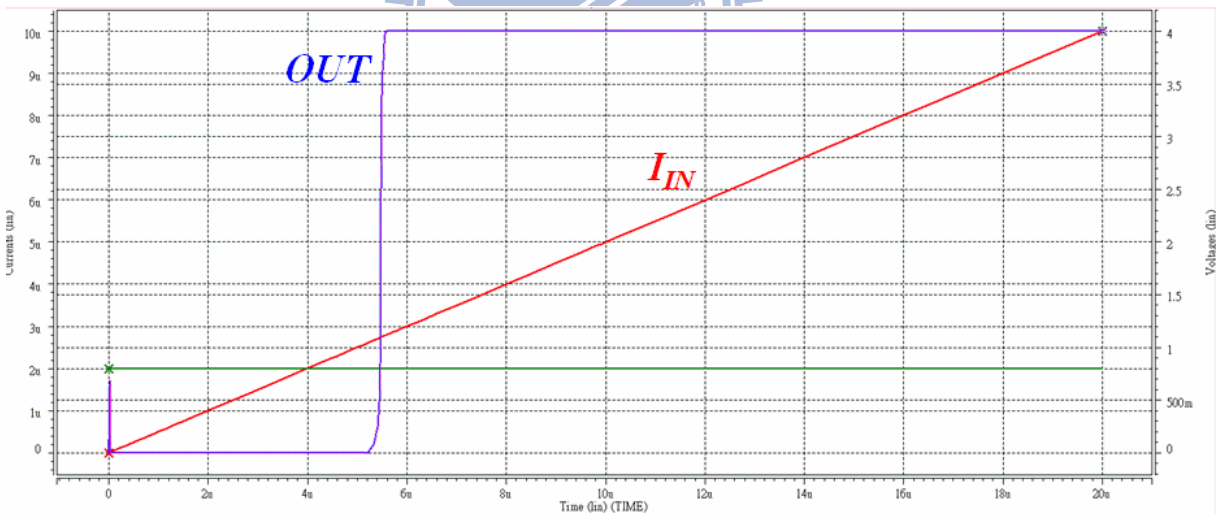
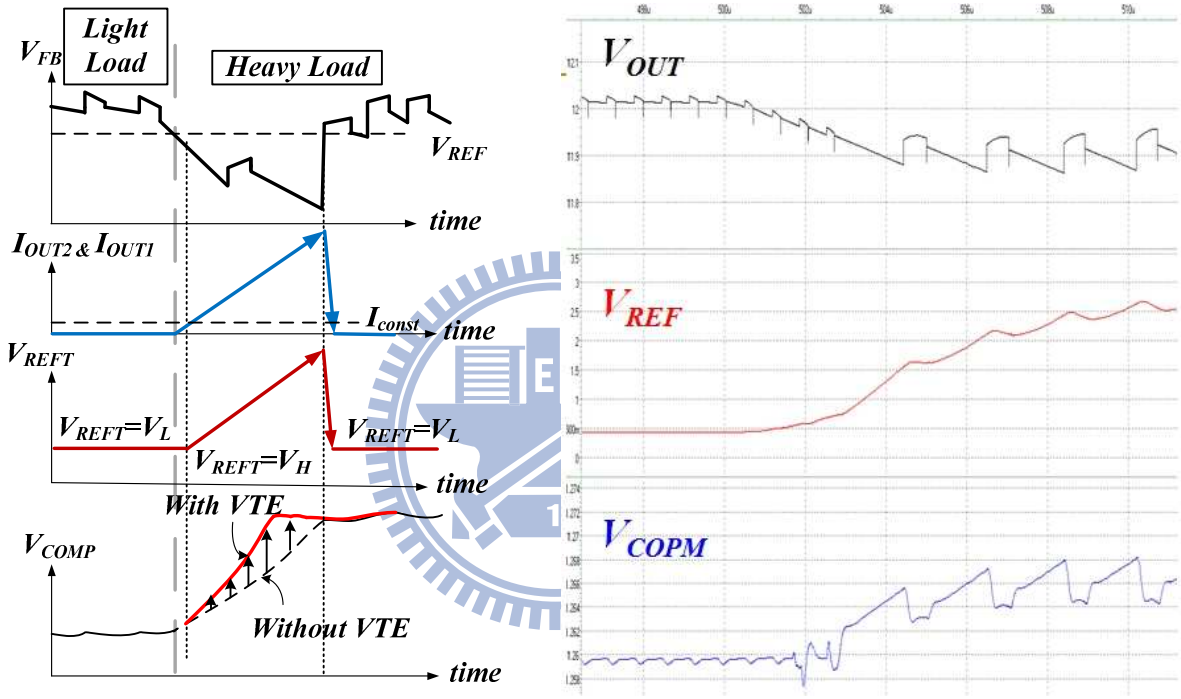


Fig. 47. The simulation waveforms of the high speed current comparator.

The p-compensator converts the voltage difference between V_{REF} and V_{FB} to three current signals, which are I_{OUT1}, I_{OUT2}, and I_{RHPZ}. The sign of the I_{RHPZ} is opposite to I_{OUT1} and I_{OUT2}. I_{OUT1} flows through the resistor R_1 to form two threshold voltages, V_H and V_L. The current I_{OUT2} compares with a pre-defined constant current, I_C to decide the start of the transient

period. During the transient period, the reference voltage, V_{REFT} changes from $V_L(=V_{BG})$ to $V_H(=V_L+I_{OUT1}\cdot R_1)$. It causes the reference voltage, which is injected into the non-inverting terminal of the error amplifier, increases to enhance the transient response time. The high speed current comparator, which is speeded up due to the shunt-shunt feedback resistor formed by the transistor M_{N4}, decides the beginning of the transient response. The theoretical and simulation waveforms are shown in Fig. 48.



(a) (b)

Fig. 48. The theoretical (a) and simulation (b) waveforms.

4.7 The Structure of the AHW Controller

Fig. 49 illustrates the adaptive hysteresis window (AHW) controller. According to the successive approximation register (SAR) conversion has been shown in section 4.2 and 4.3, the adaptive off time is controlled by the capacitor array, C_{off}, to decide the off time, t_{off}. In steady state, t_{off} is kept constant. Once the load current changes, t_{off} of the conventional boost

converter decreases. Unfortunately, it causes a large drop voltage. Thus, the AHW controller prolongs t_{off} through the decreasing charging current, I_{CONST}+I_{RHPZ}, and increasing V_R due to the injection of I_{RHPZ}. t_{off} is controlled by the current I_{RHPZ} that comes from the VTE controller as shown in Fig. 46.

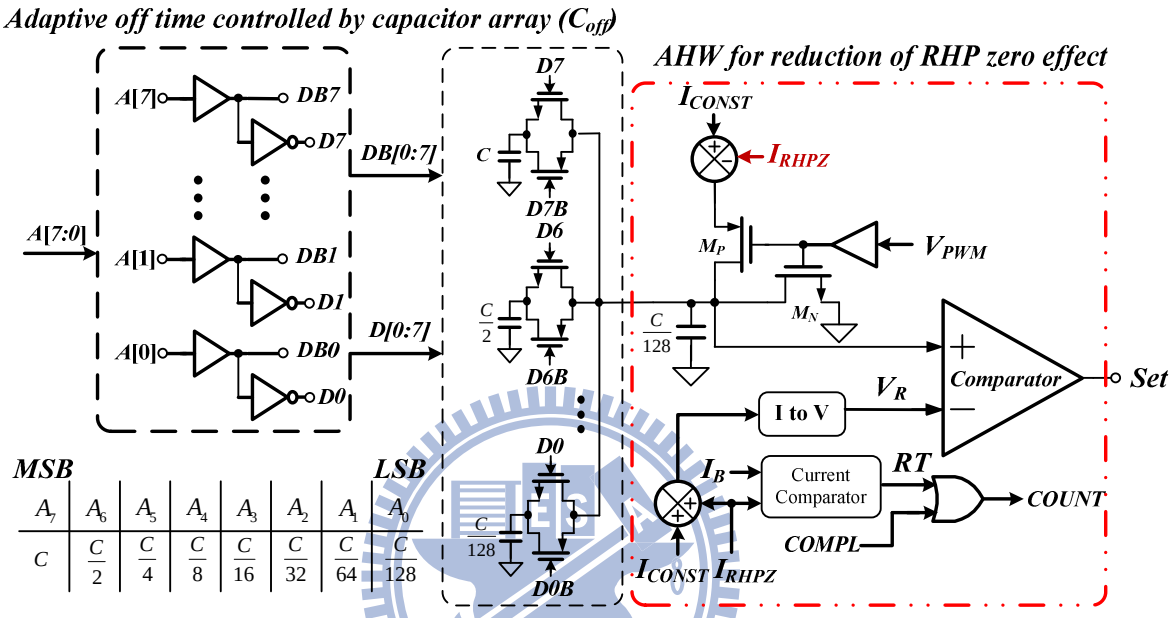


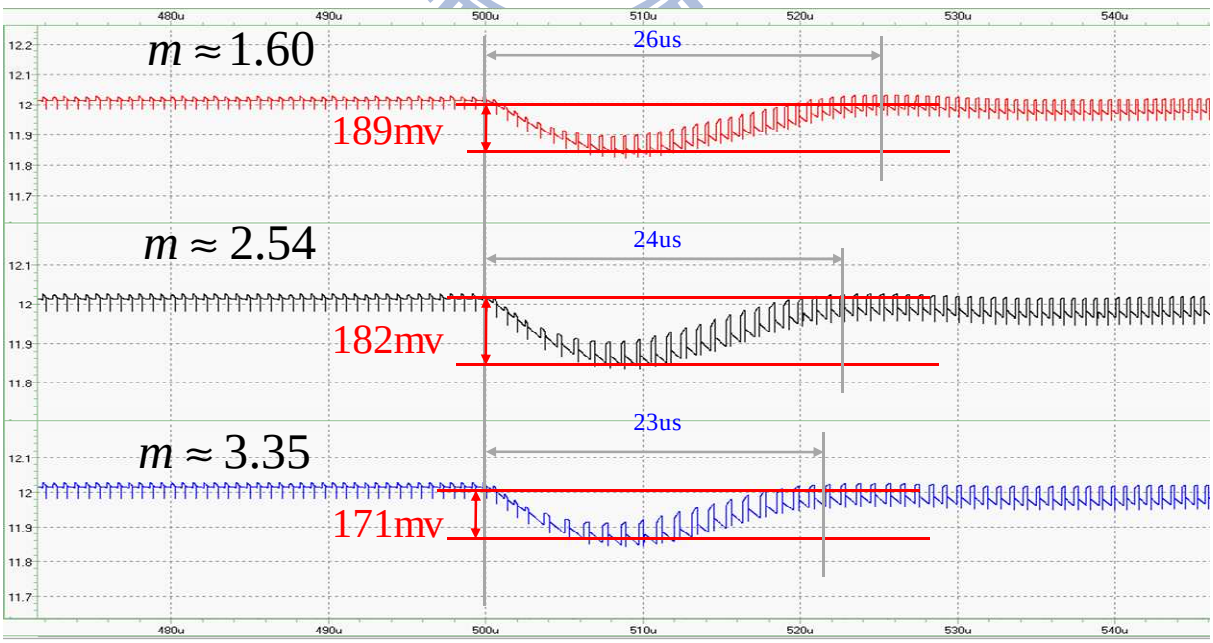
Fig. 49. The structure of the AHW modulator circuit .

Chapter 5

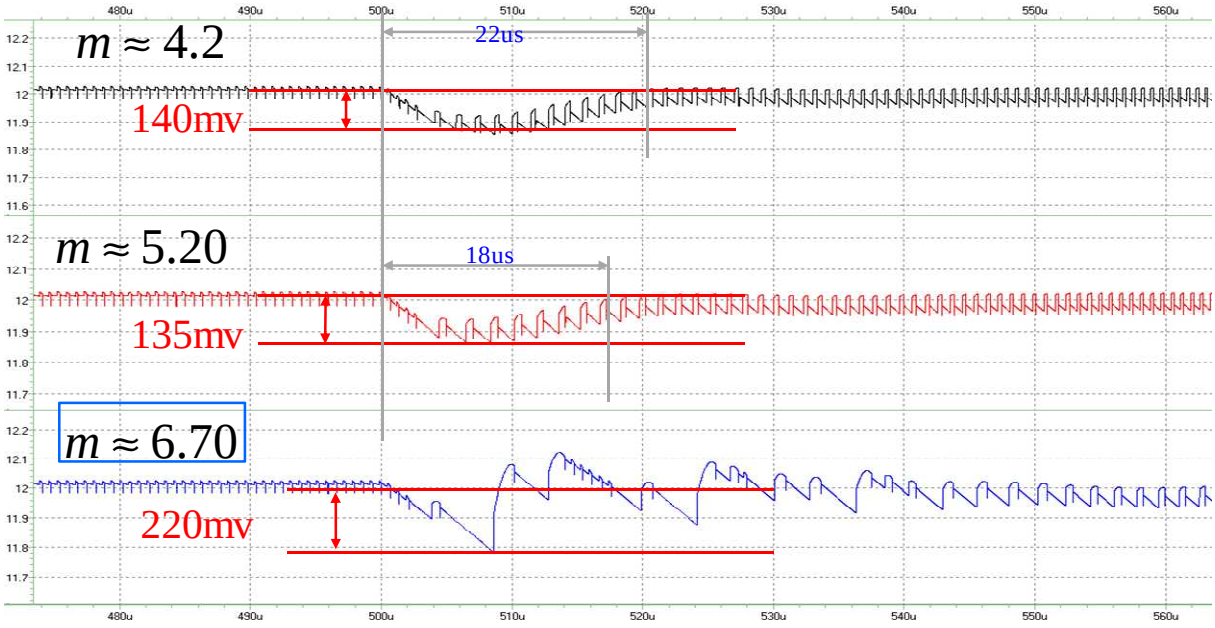
Simulation Results, Conclusions and Future work

5.1 Simulation Result

The whole chip simulation results of the designed SDC controller boost converter circuit are shown in Fig. 50 and Fig.51. In order to get much smaller voltage drop when load change happened for boost converter, the time ratio “m” should be selected in the ideal range which is the equations (80) and (81) we have proof in 3.1.4. We are now to design a boost converter with V_{IN}=4V, V_{OUT}=12V, duty cycle D=2/3, inductor L=6.8uH, and the load step change from 50mA to 250mA (so the k=5). According to these equations, the range of factor “m” is from 1 to 5.28. The simulation results about the load regulation have been shown in Fig. 50 in different time ratios “m”.



(a)



(b)

Fig. 50. The load regulation simulation results for boost converter in different time ratios (m).

The switching frequency of the convert is 1.4MHz. The frequency of RHP zero is 624KHz and 125KHz at light load and heavy load, respectively. To keep the system stable, we choice the system crossover frequency are 21KHz and 28KHz (about 20% RHP zero frequency at heavy load) at light load and heavy load, respectively.

The larger ratio factor “m”, the less voltage drop and the less the switching frequency happened at load state. According to the equation (80) and (81) in section 3.1.4. When the ratio factor m=6.70. Then the switching frequency will become 208KHz which is smaller than reasonable the crossover frequency (10 W_C).

By calculating the phenomenon of voltage drop with different time ratios “m” during first period after load step happened is shown in Fig. 51.

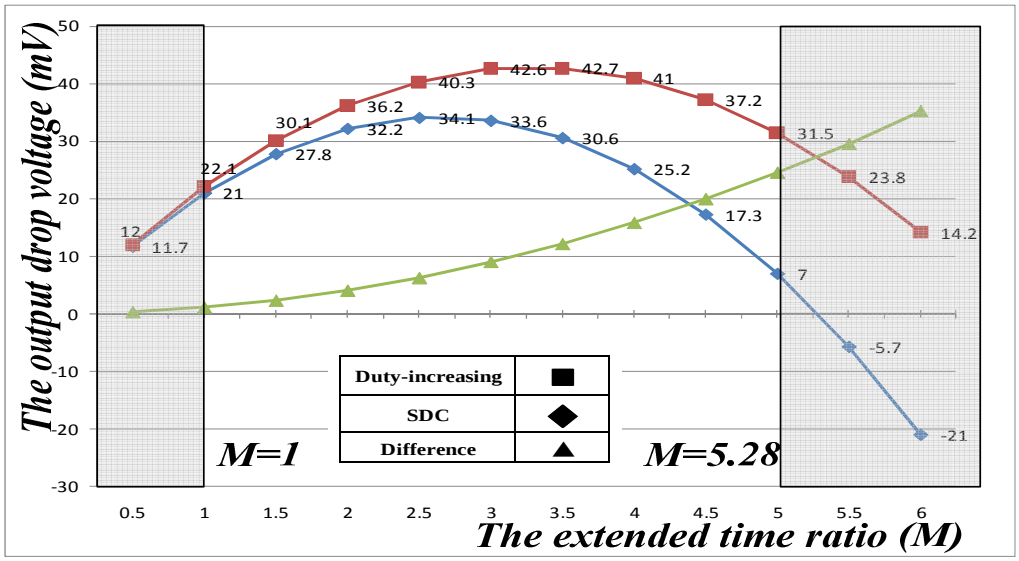
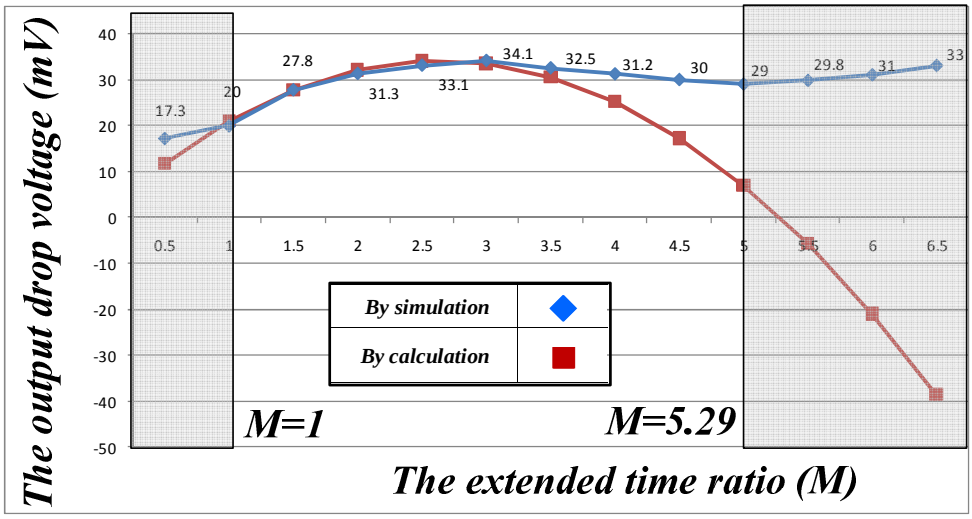
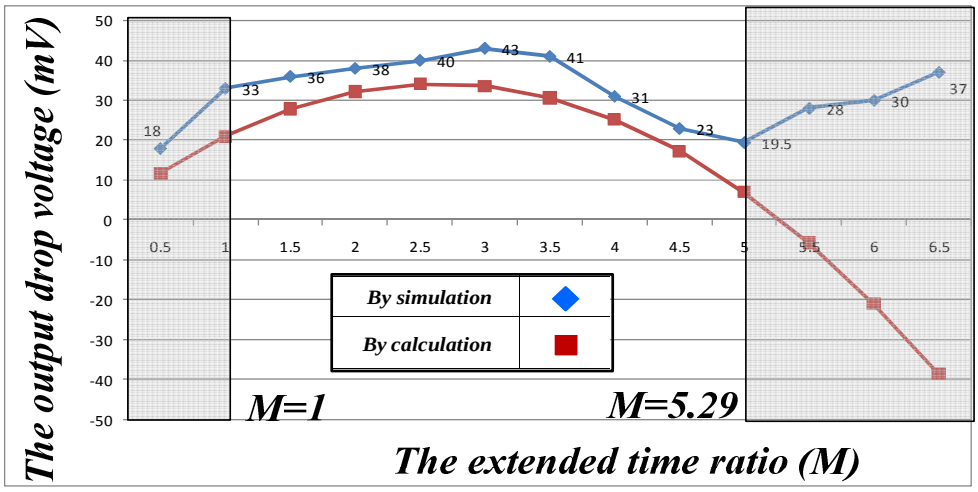


Fig. 51. The voltage drop calculation results for boost converter by comparing duty-increasing and SDC methods.

In SDC method, the simulation and calculation results are shown in Fig. 52. Fig. 52 (a) and (b) are the simulation results without and with output capacitor ESR (R_{ESR}), respectively. As we observed, the curve in Fig. 52 (a) is more similar because we ignore the output capacitor ESR when we analyzed in section 3.1.4. Because of the output voltage will drop during on-time. If chose time ratio "m" is greater than the maximum value that means the on-time is also large, so the drop voltage during will increase.



(a)



(b)

Fig. 52. The simulation and calculation results of output voltage drop value during first time period from heavy load to light load. (a) Without R_{ESR}. (b) With R_{ESR}.

And the total dip values of output voltage (V_{OUT}) without R_{ESR} are also shown in Fig. 53. To get better we chose time ratio range from m=1 to m=5.28.

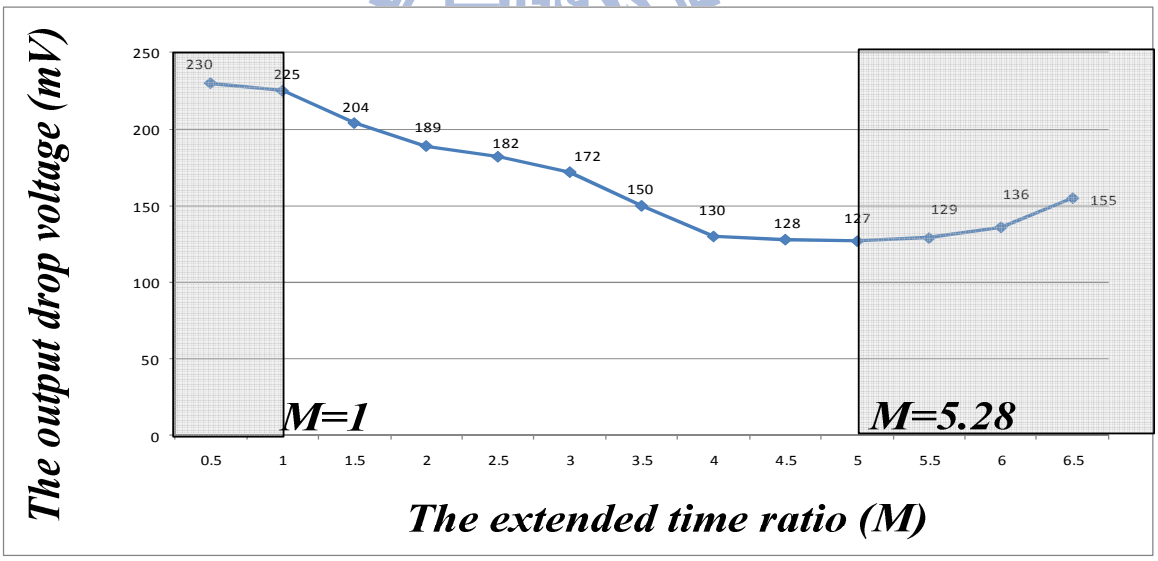


Fig. 53. The total dip values of output voltage (V_{OUT}) without R_{ESR}.

As we know a reasonable limitation on the crossover frequency, ω_c, should be below 1/8 of the switching frequency. As you push the switching frequency lower, more issues with noise will arise (ringing and oscillation at output voltage (V_{OUT})) and influence the control system. This phenomenon is shown in Fig. 50 (b) when we choose time ratio m=6.70. In Fig. 54 and Fig.55, the output voltage and inductor current waveforms for boost convert when the

load changed from 50mA to 250mA at t=500us is shown (m=5.20).

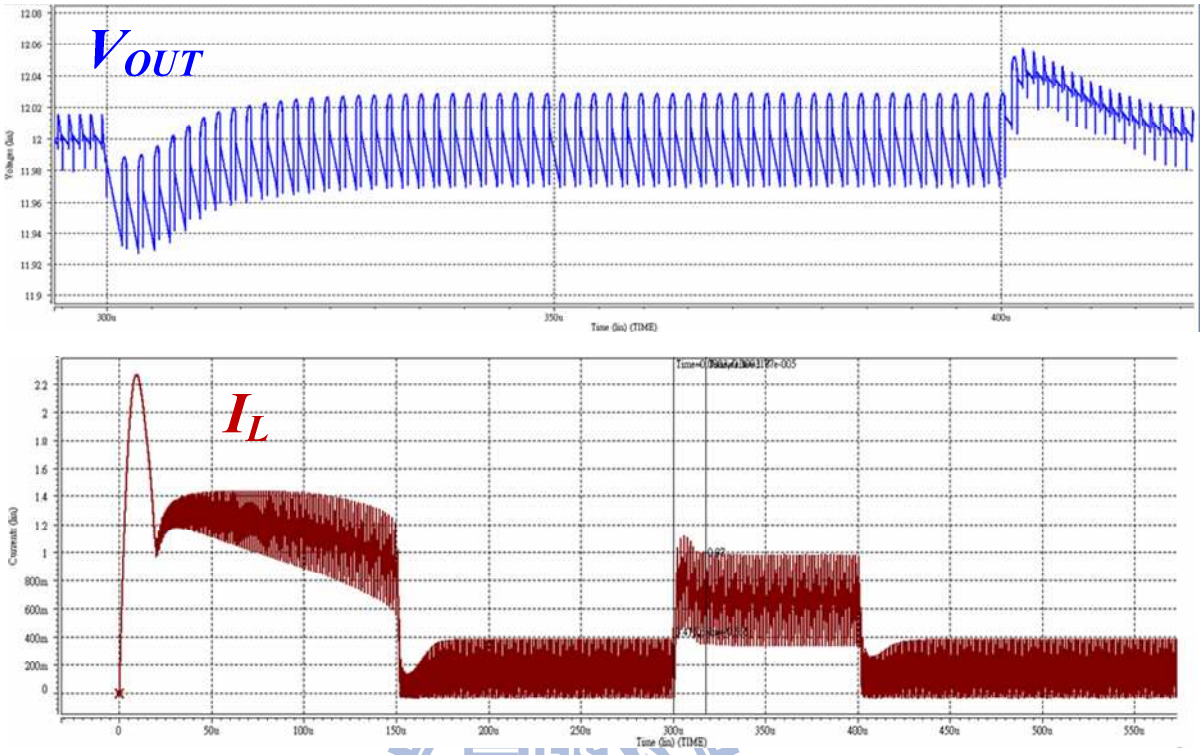


Fig. 54. The output voltage (V_{OUT}) and inductor current (I_L) waveforms.

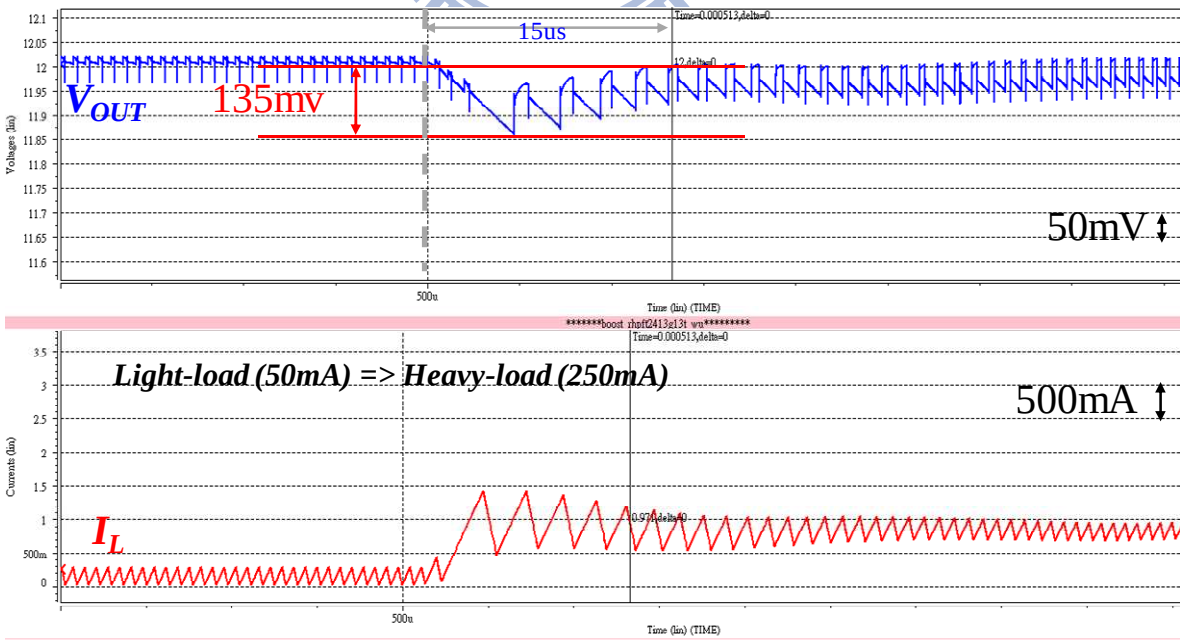


Fig. 55. The output voltage and inductor current waveforms for boost convert when the load changed from 50mA to 250mA.

The proposed SDC controller for edge-lit LED backlight systems was fabricated by TSMC 0.25um BCD process. Fig. 56 shows the chip micrograph with a silicon area of 2850 μm × 1512 μm. The detailed specifications are listed in Table 5. The LED driver provides a 12V regulated output voltage with a maximum loading current of 250mA.

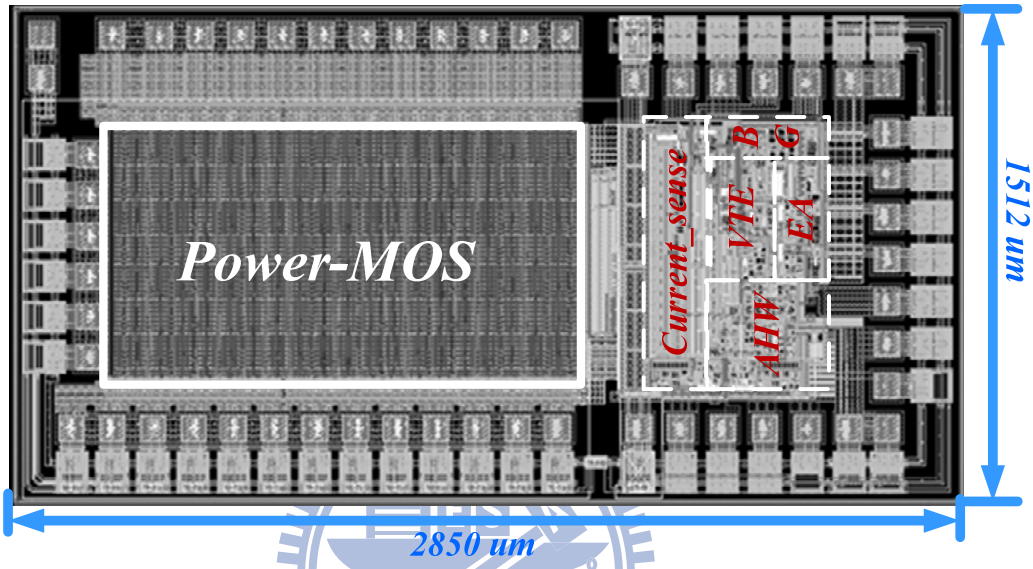


Fig. 56. Chip micrograph.

Table 5. The design specification

Characteristics	***Typ.***	***Unit***
Supply Voltage (V_{in})	*3.5~4.5*	*V*
Output Voltage (V_o)	*12*	*V*
Output Current (I_{load})	*50~250*	*mA*
Input Inductor (L)	*6.8*	*μH*
Equilibrium series Resistance of the inductor (DCR)	*45*	*mΩ*
Output capacitor (C_O)	*6.8*	*μF*
Equilibrium series resistance of the output capacitor (R_{ESR})	*50*	*mΩ*
Chip size	*2.16*	mm^2
Switching Frequency (F_S)	*1.4*	MHz
f_{RHP_zero} (light-load)=> (heavy-load)	*624 => 125*	*KHz*

Crossover frequency (light-load)=> (heavy-load)	*21 => 28*	*KHz*

The comparison between the proposed technique with the HCC and PCC techniques is listed in Table 6. The proposed SDC technique can achieve 30 % 80 % improvement for undershoot and recovery time, respectively.

Table 6. The summaries of the conventional duty-increasing and the SDC technique

Characteristics	***Conditions***	***Duty-increasing Technique***	***SDC Technique***
Supply Voltage	--	*4V*	*4V*
Output Voltage	--	*12V*	*12V*
Output Current Variation	--	*200mA*	*200mA*
Overshoot Voltage	I_{load}*=250mA→50mA within 2μs*	*308mV*	*135mV*
Undershoot Voltage	I_{load}*=50mA→250mA within 2μs*	*338mV*	*150mV*
Recovery time of heavy-to-light load	I_{load}*=250mA→50mA @ 0.1% rated voltage within 2μs*	*141μs*	*15μs*
Recovery time of light-to-heavy load	I_{load}*=50mA→250mA @ 0.1% rated voltage within 2μs*	*141μs*	*28μs*
Load Regulation	--	*0.16mV/mA*	*0.07mV/mA*

5.2 Conclusions

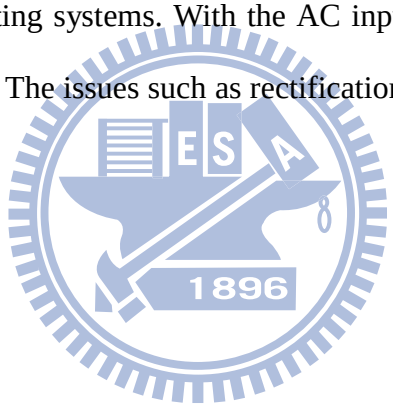
This paper proposed a solid-duty-control technique in the boost converter to keep a constant duty to reduce dip voltage during load transient period. Besides, due to variable transient enhancement controller, fast transient response can be achieved. For edge-lit LED backlight systems, a stable and regulated output driving can be provided by the proposed SDC technique. Compared to conventional design without any fast transient technique,

experimental results show the undershoot voltage and recovery time are enhanced 30 % and 80 %, respectively.

5.3 Future work

In this thesis, the proposed circuit is only using an approximation way to realize the thesis about the output voltage variation during load transient for boost converter. The analyzed results are already proofed by simulation.

In the future, the SDC boost converter can be accurate realized by using some circuit like the analog-multiplier and the analog-divider. This SAR-controlled adaptive off-time technique may extend to the AC-DC circuit application. Grid-connected power source driving is now the most valuable for LED lighting systems. With the AC input, supply voltage is 80V to 260V sine wave in 50Hz to 60 Hz. The issues such as rectification, power factor, and total harmonic distortion must be solved.



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