Chapter 3

Effects of Channel Width on Electrical Characteristics of High–performance Polysilicon Thin Film Transistors with Multiple Nanowire Channels

Abstract

This work studies the electrical characteristics of a series of polysilicon thin-film transistors (poly-Si TFTs) with different numbers of multiple channels of various widths, with lightly-doped drain (LDD) structures. Among all investigated TFTs, the nano-scale TFT with ten 67 nm-wide split channels (M10) has superior and more uniform electrical characteristics than other TFTs, such as a higher ON/OFF current ratio (>10^9), a steeper subthreshold slope (*SS*) of 137 mV/decade, an absence of drain-induced barrier lowering (*DIBL*) and a suppressed kink-effect. These results originate from the fact that the active channels of M10 TFT has best gate control due to its nano-wire channels were surrounded by tri-gate electrodes. Additionally, experimental results reveal that the electrical performance of proposed TFTs enhances with the number of channels from one to ten strips of multiple channels sequentially, yielding a profile from a single gate to tri-gate structure. Devices that contain the proposed M10 TFT are highly promising for use in active-matrix liquid-crystal-display technologies without any additional processing.

3.1 Introduction

Polysilicon thin-film transistors (poly-Si TFTs) have attracted much considerable attention because they can be applied in active-matrix liquid-crystal-displays (AMLCDs), since they perform very well and can be integrated with peripheral driving circuits on a low-cost glass substrate [1], [2]. Also, poly-Si TFTs have the potential to be used in three-dimensional (3D) circuits, including vertically integrated SRAMs [3] and DRAMs [4]. Conventional top single-gate poly-Si TFTs, however, exhibits some non-ideal effects when applied. First, they suffer from anomalous leakage current in the OFF-state, which correlates with the drain voltage and the gate voltage [5], [6]. This undesirable large OFF-state leakage current limits the application of poly-Si TFTs in switching devices. The dominant mechanism by which the leakage current in poly-Si TFTs is induced involves the field emission of carriers in grain boundary traps, due to the high electric field near the drain junction [7]. An effective method for reducing the electric field in the drain region is to incorporate a lightly-doped drain (LDD) region between the heavily doped region and the active channel region [8]. Second, the presence of polysilicon grain boundary defects in the channel region of TFTs drastically affects the electrical characteristics [9], [10], especially when the device dimension is scaled down; Therefore, reducing the number of polysilicon grain boundary defects will improve the performance of poly-Si TFTs.

TFTs with several multiple channels have been reported to effectively reduce grain boundary defects [11]-[13]. Additionally, scaling down of TFT's dimension is a continuous trend since its benefits in performance. Smaller device size enables higher device density in SRAMs and DRAMs, and increases the driving current in peripheral driver circuits in AMLCD applications. However, as a TFT's dimensions are reduced, influences from the drain side of the channel becomes significant, (i.e. gate control becomes lower), which will arise severe short-channel effect, including threshold voltage roll-off, a large subthreshold slope (*SS*), a large drain-induced barrier lowering (*DIBL*) and the occurrence of kink-effect. These effects are major limitations in realizing a system on panel (SOP). In CMOS technology, many high-performance surrounding gate structures in a silicon-on-insulator (SOI) MOSFET, such that double-gate [14], tri-gate [15], FinFET [16] and gate-all-around [17], have been reported to exhibit superior gate control over the channel than a conventional single-gate MOSFET, to reduce short-channel effects.

In this paper, we apply the tri-gate structure on short-channel (gate length = 0.5 um) TFTs design, also employed multi-channel with different widths and LDD structures. Experimental results show that the electrical characteristics are highly depended on channels width dimension. The ten nano-wire channels TFT shows best gate control, and its short-channel effects are highly reduced than other TFTs, which is

responsible for excellent performance.

3.2 Devices structure, simulation and fabrication

In this work a series of TFTs, with a gate length of 0.5 um, consisting of ten strips of multiple 67 nm wire channels (M10) TFT, five strips of multiple 0.18 um channels (M5) TFT, two strips of 0.5um channels (M2) TFT and a single-channel structure (S1) with W = 1 um TFT, were fabricated, as listed in Table I. Figure 1a presents the structure of the M10 TFT. Figure 1b presents the cross-section of the M10 TFT perpendicular to the AA' direction. This M10 TFT has a conventional top-gate LDD MOSFET structure. Figure 1c presents cross-section of the M10 TFT perpendicular to the BB' direction, in which the channels were surrounded by the gate electrode as tri-gate structure. Figure 2 presents device electrical characteristics simulation results using the DESSIS software package from ISE. The double-gate TFT simulation results serve to tri-gate TFT due to the similar dimension. Figure 2a shows the encroachment of electrical field from drain side of S1 TFT. However, in Fig. 2b, M10 TFT can confine the electrical field due to its superior tri-gate control. Therefore, it is expected that the M10 TFT tri-gate structure can suppress effectively short channel effects.

The devices were fabricated on 6-inch silicon wafers with a 400 nm-thick layer of thermal oxide layer substrate. A thin 50 nm-thick undoped amorphous-Si (a-Si)

layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The deposited a-Si layer was then recrystallized by at 600 ^{0}C for 24 hours in nitrogen ambient. After electron beam (Ebeam) direct writing and reactive ion etching (RIE), the device active islands were formed. Then, a 26 nm-thick layer of tetra-ethyl-ortho-silicate (TEOS) oxide and a 150 nm-thick layer of undoped polysilicon were deposited by LPCVD, and transferred to a gate electrode by Ebeam direct writing and RIE. Phosphorous ions were implanted in the lightly-doped source and the drain region at a dose of 5×10^{13} cm^{-2}. A 200 nm-thick layer of TEOS oxide was then deposited by LPCVD, and anisotropically etched by RIE to form a sidewall spacer that abutted the polysilicon gate. Then, the self-aligned source and drain regions were formed by the implantation of phosphorous ions at a dose of 5×10^{15} cm^{-2}. The dopant was activated by rapid thermal annealing at 1000 ^{0}C. After source and drain (S/D) implantation, a 300 nm-thick TEOS oxide layer was deposited as the passivation layer by LPCVD. Next, the contact hole was defined and Al metallization was performed. The devices were then sintered at 400°C in nitrogen ambient for 30 min. Finally; each device was passivated by NH_3 plasma treatment for 1 hr at 300 ^{0}C.

3.3 Results and discussion

Figure 3a presents a after etching investigation (AEI) scanning electron microscope (SEM) photograph of the poly-Si active region of the M10 TFT, including

the source, the drain and ten multiple nano-wire channels. Figure 3b presents a magnified area of the multiple nano-wire channels in the M10 TFT, each of which is 67-nm-wide. Figure 3c presents a plane view of transmission electron micrograph (TEM) photograph of the active region of the proposed TFTs. The average grain size in the polysilicon channel formed by solid phase crystallization is approximately 30 nm. Figures 3 to 6 present the electrical characteristics of proposed poly-Si TFTs with various numbers of channels of different widths. Figures 4(a) to 7(a) plot typical transfer curves, while Figs. 4(b) to 7(b) plot output curves of poly-Si TFTs. In Fig. 3(a), the single-channel TFT (S1 TFT) shows significant short-channel effect, including *DIBL*, large subthreshold slope (*SS*) of 334 mV/dec., and large leakage current of 4×10^{-12} A. In Figs. 4(b), S1 TFT shows a severe kink-effect in output characteristics. By comparing of all studied TFTs in this work, however, the transfer characteristics reveal that the TFT with ten strips of nano-wire channels (M10) performs best, as shown in Fig. 7(a), with the lowest OFF-state leakage current of 3×10^{-13} A, the highest drain current ON/OFF ratio of 7.36×10^{9}, the smallest subthreshold slope (*SS*) of 137 mV/dec. and an absence of drain-induced barrier lowering (*DIBL*). In addition, in Figs. 4(b) to 7(b), the kink-effect is reduced form S1, M2, M5 to M10 TFT. The M10 TFT even exhibits almost kink-free characteristics, indicating that the thin 50 nm-thick, and 67 nm-wide channels of M10 TFT are

fully-depleted by the tri-gate electrode. Therefore, at high drain bias (V_{ds}), the impact ionization is lower than that on other TFTs. Device performance uniformity is another important issue for realization of large-glass poly-Si AMLCD. The uniformity of device performance can be revealed by measuring the statistical variation of device parameters. For the investigation of device performance uniformity, in this work, each dimension including five TFTs in different areas on the 6-inch wafer were characterized. Table II lists all the parameter of the poly-Si TFT, including average and standard deviation of field effect mobility (μ_{FE}), the ON/OFF ratio, the threshold (V_{th}), the subthreshold slope (*SS*), and the drain-induced barrier lowering (*DIBL*). μ_{FE} is extracted from the linear region (V_d = 0.05V) of transcendence (g_m). V_{th} is defined as the gate voltage required to yield normalized drain current of I_d / (W/L) = 10^{-7} A at V_d = 2 V. I_{ON} is defined as the maximum drain turn-on current at V_d = 2 V. I_{OFF} is defined as the minimum drain turn-off current at V_d = 2 V. Thus, the ON/OFF ratio is defined as I_{ON} / I_{OFF}. *DIBL* is defined as ΔV_g / ΔV_d at I_d = 10^{-10} A. Figure 8 plots the TFTs' μ_{FE} versus the multi-channel with different widths. This curve reveals that the S1, M2, M5 and M10 poly-Si TFTs yield almost the same carrier mobility, indicating that the carrier mobility and the turn-on current are not degraded in TFTs with various numbers of channels. Figure 9 plots the TFTs *ON/OFF* ratio (left) and the leakage current I_{OFF} (right) versus the multi-channel with different widths. The leakage

current is reduced significantly in the OFF-state from 10^{-12} (A/um) to 10^{-13} (A/um) in order from the S1 TFT to the M10 TFT. The enhanced performance in electrical characteristics of M10 TFT can be explained that it has a split nano-wire structure (Fig. 3b), most of which is exposed to NH_3 plasma passivation, further reducing the number of grain boundary defect density (N_t) as shown in Fig. 10, which is responding for achieving low leakage current. Thus, the M10 TFT has a higher ON/OFF ratio (>10^9) than those of other TFTs in this work. Figure 11 plots the TFTs' V_{th} versus the multi-channel with different widths. The average V_{th} value for each TFT devices is between 0 and 0.2 V. Notably, the value of V_{th} for the M10 TFT has the smallest standard deviation, indicating that the M10 TFT is a relatively stable structure; the fabrication thus involves smaller variations, which fact is crucial key in the uniform lager-glass AMLCD applications. Figure 12 plots the TFTs' *SS* versus the multi-channel with different widths. The average and standard deviation of *SS* both increase with the number of channels. The M10 TFT has a smaller average (137mV/dec.) and standard deviation (23mV/dec.) of *SS* than those of the other TFTs. The steep *SS* of M10 TFT is desirable for the ease of switching the transistor off. The steep *SS* of the M10 TFT is also explained by the fact that M10 exhibits the best NH_3 plasma passivation due to its ten split nano-wires, which is responsible for reducing N_t and achieving the steep *SS*. Figure 13 plots the TFTs' *DIBL* versus the

multi-channel with different widths. Such a barrier-lowering effect leads to a substantial increase in electron injection from the source to the drain. Therefore, the threshold voltage decreases since subthreshold current increases. However, the M10 TFT has an average and standard deviation of *DIBL* of zero. The ten nano-wires of M10 TFT are strongly controlled by their tri-gate electrodes (Fig. 1c). Simulation results of Fig. 2b further reveal that the tri-gate TFT has superior gate control, which can confine the electrical field penetrated from drain. Figures 11, 12 and 13 all reveal that the M10 TFT performs best in switching applications, with the most stable V_{th} and the smallest *SS*, and without the *DIBL* effect. These results are summarized by stating that the active channels around the tri-gate of the M10 TFT exhibit the best gate control to highly reduced short-channel effect, as determined by its nano-wire structure. Additionally, experimental results also indicate that the gate control increases with the number of channels from S1, M2, and M5 to M10, as similar as the structure changes from a single-gate to tri-gate sequentially. Additionally, NH_3-plasma passivation more efficiently affects M10 TFT than it does other TFTs. The M10 TFT has a split nano-wire structure, most of which is exposed to NH_3 plasma passivation, further reducing the number of grain boundary defects.

3.4 Conclusion

This work studied the relationship between electrical characteristics and channel width dimension in multi-channel poly-TFT with nano-wires devices. Experimental results indicate that the device performance enhances with the increasing of number channels, from S1, M2, M5 to M10 TFTs, because their structures vary from single-gate to tri-gate controlled devices gradually. Therefore, M10 TFT exhibits superior and uniform characteristics, including low leakage current in the off-state, a high *ON/OFF* drain current ratio, a steep subthreshold slope, an absence of *DIBL* and favorable output characteristics. The fabrication of multi-channel TFTs with nano-wires is easy and involves no additional processes. Such TFTs are thus very promising candidates for use in future high-performance poly-Si TFT applications.

References

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Multi-Channel Dual-Gate Poly-Si TFT Employing Excimer Laser Annealing Recrystallization on pre-patterned a-Si thin film," in *IEDM Tech. Dig*., pp. 561-564, 2002.

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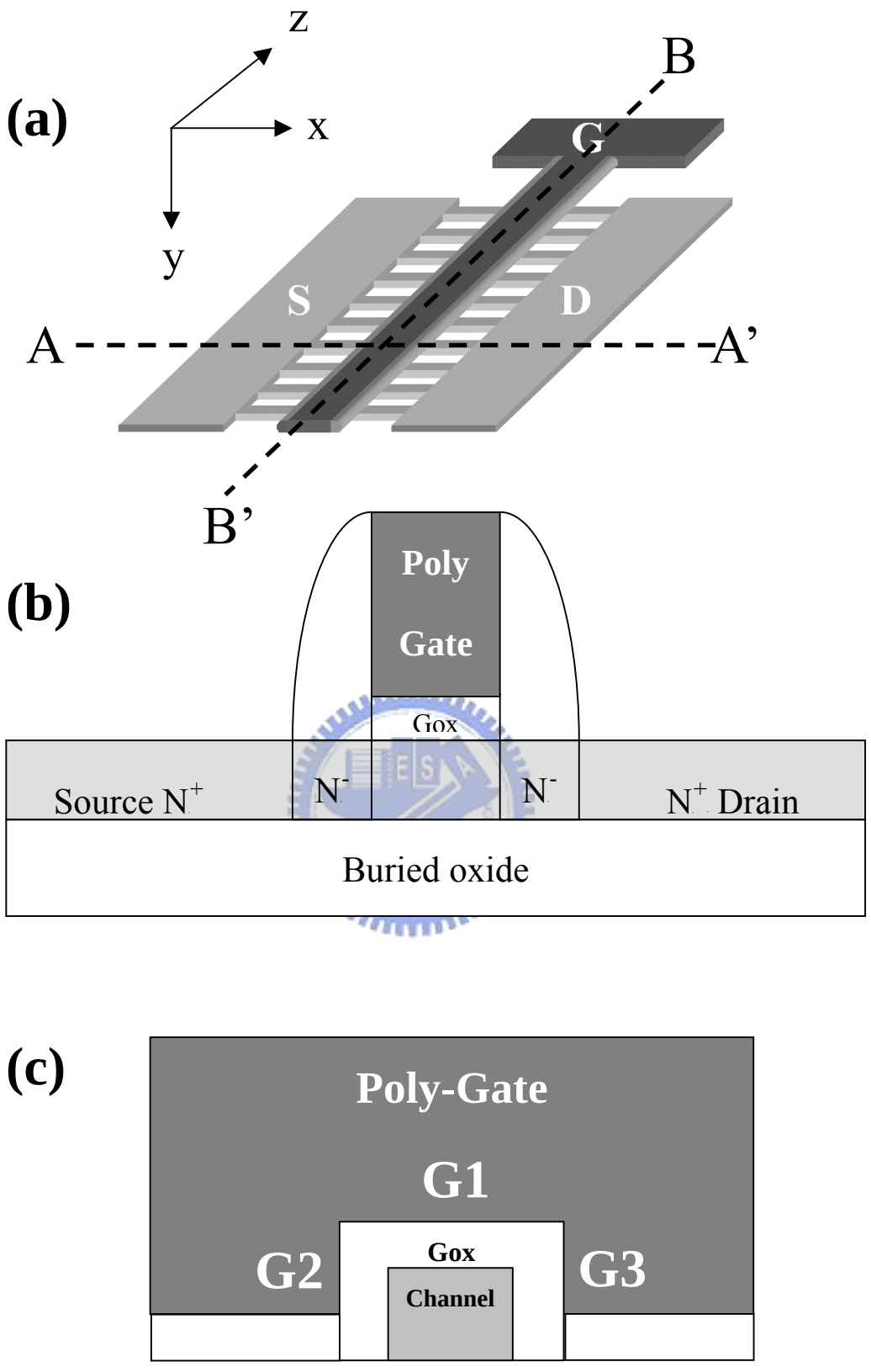

FIG. 1. (a) Schematic diagram of M10 poly-Si TFT. (b) Cross-section view of Fig. 1a AA' direction, as a conventional top-gate LDD MOSFET structure. (c) One of channel cross-section view of Fig. 1a BB' direction, as a tri-gate structure. Active layer, gate oxide, and poly-gate thickness are 50 nm, 26 nm and 150 nm, respectively.

Table I Devices dimension of M10, M5, M2 and S1. All devices have the same active channel thickness 50 nm and gate oxide thickness 26 nm.

Device name	Gate length (L)	Channel Number	Each channel width (W)
M10	0.5 um	10	67 nm
M5	0.5 um	5	0.18 um
M2	0.5 um	2	0.5 um
S1	0.5 um	1	1 um

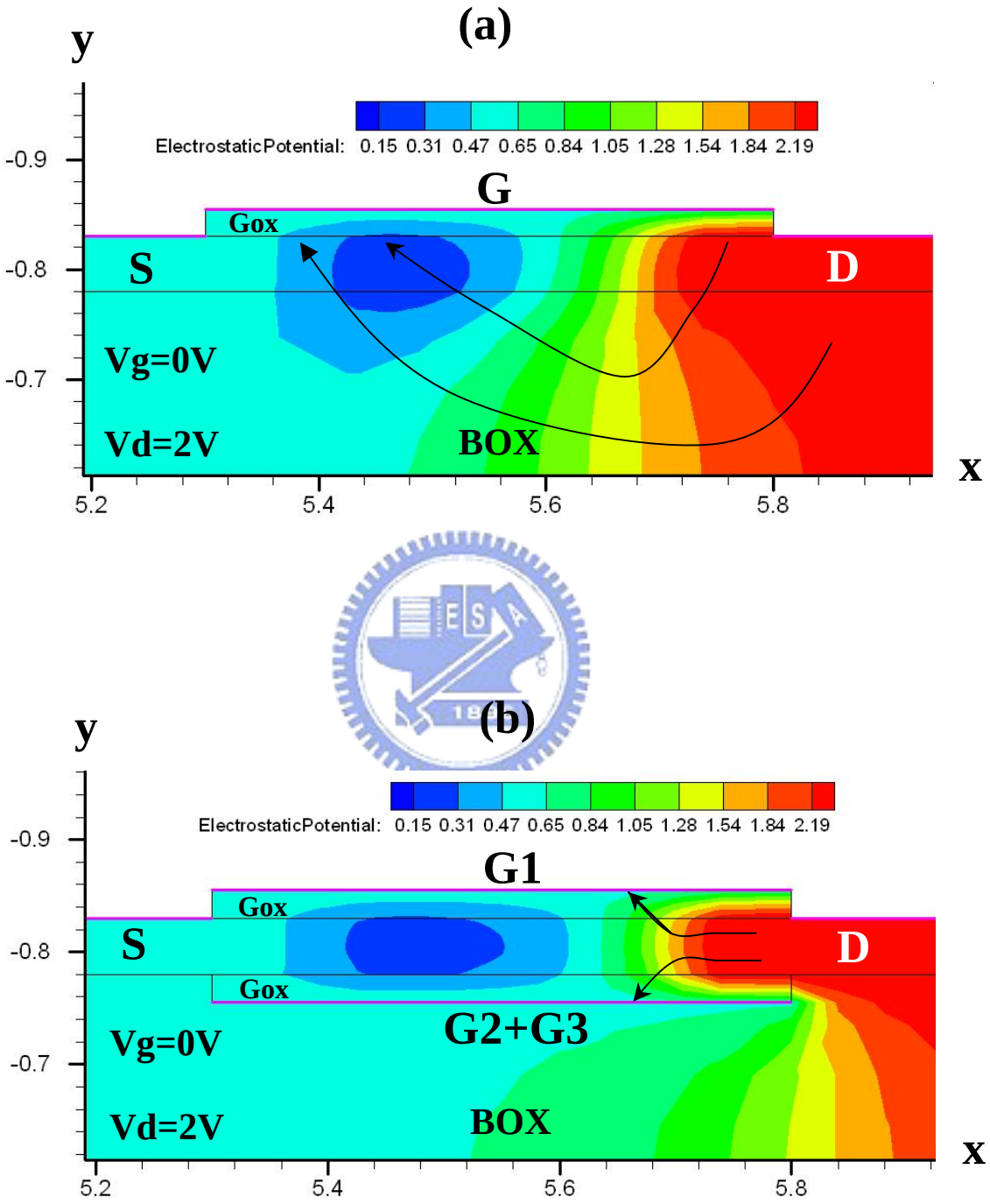

Fig. 3-2. Simulation results of potential contour plots and electrical field lines of (a) single-top-gate TFT (b) tri-gate TFT with L = 0.5 um, gate oxide = 26 nm, channel thickness = 50 nm at $V_g = 0\ V$, $V_d = 2\ V$.

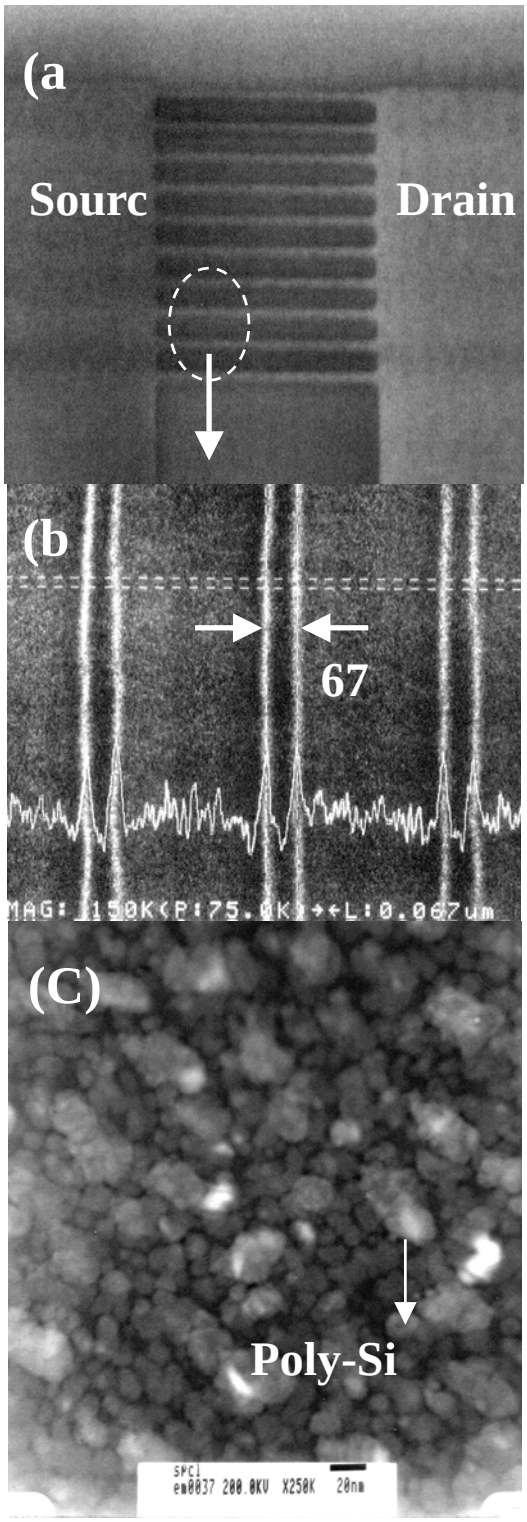

Fig. 3-3.(a) Scanning electron microscopy (SEM) photography of active pattern with the source, the drain and multiple nano-wire channels of M10 TFT. (b) Magnified area of multiple nano-wire channels. The each nano-wire width is 67 nm. (c) Transmission electron microscopy (TEM) photography of poly-Si grains by solid phase crystallization. The average poly-Si grain size is about 30 nm.

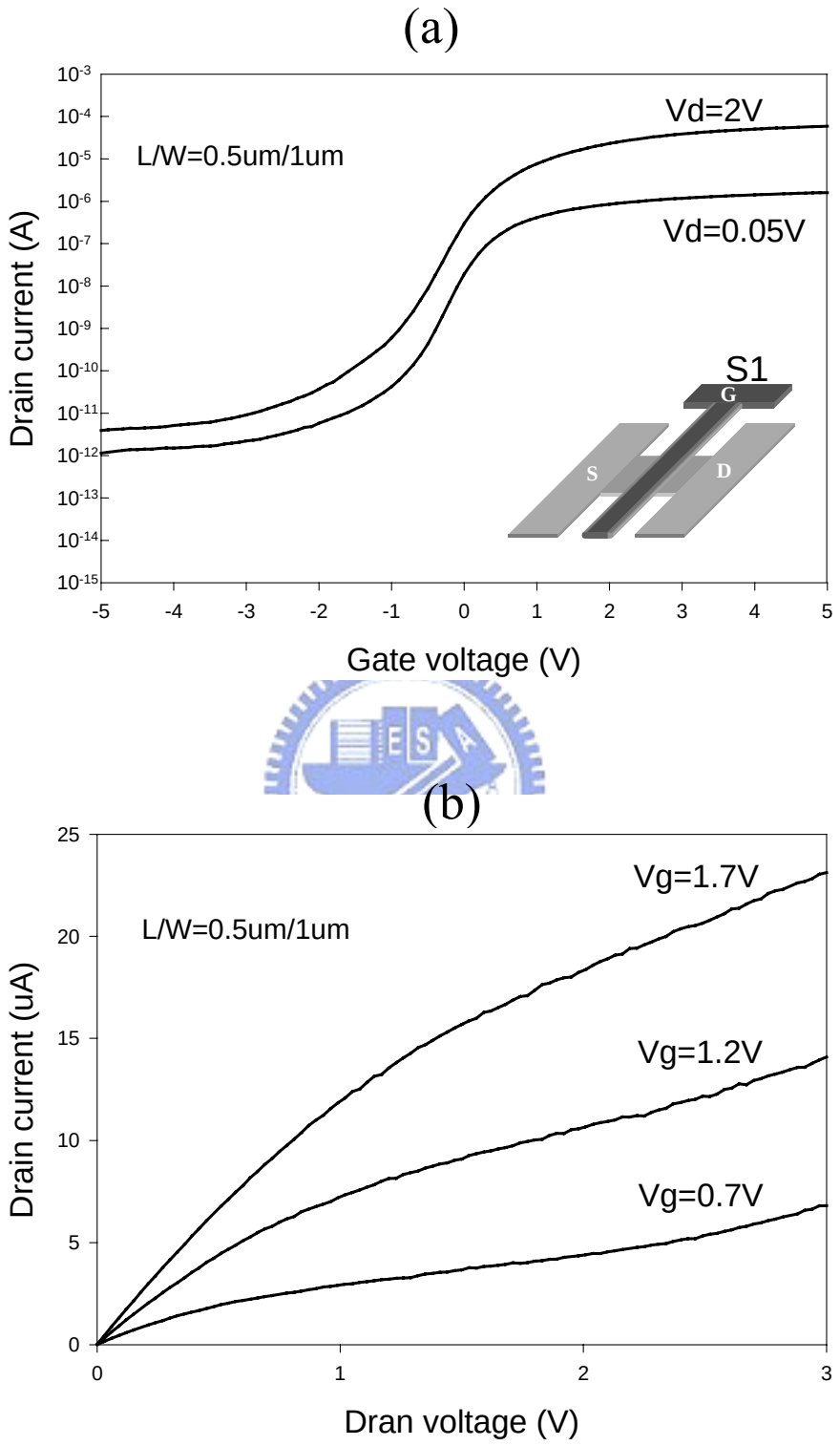

Fig. 3-4. Device characteristics of S1 (L / W = 0.5 um / 1 um) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

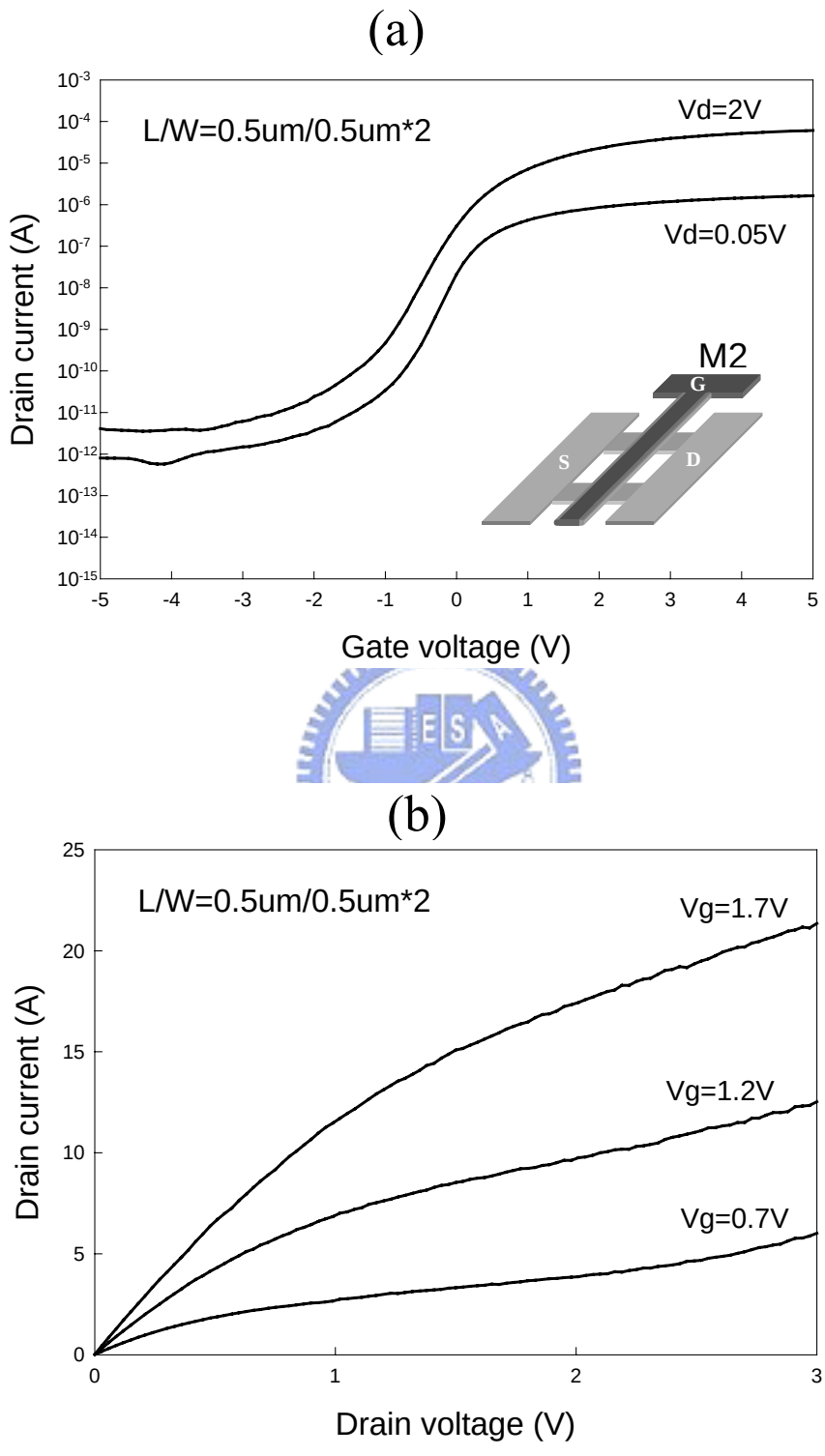

Fig. 3-5. Device characteristics of M2 (L / W = 0.5 um / 0.5 um × 2) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

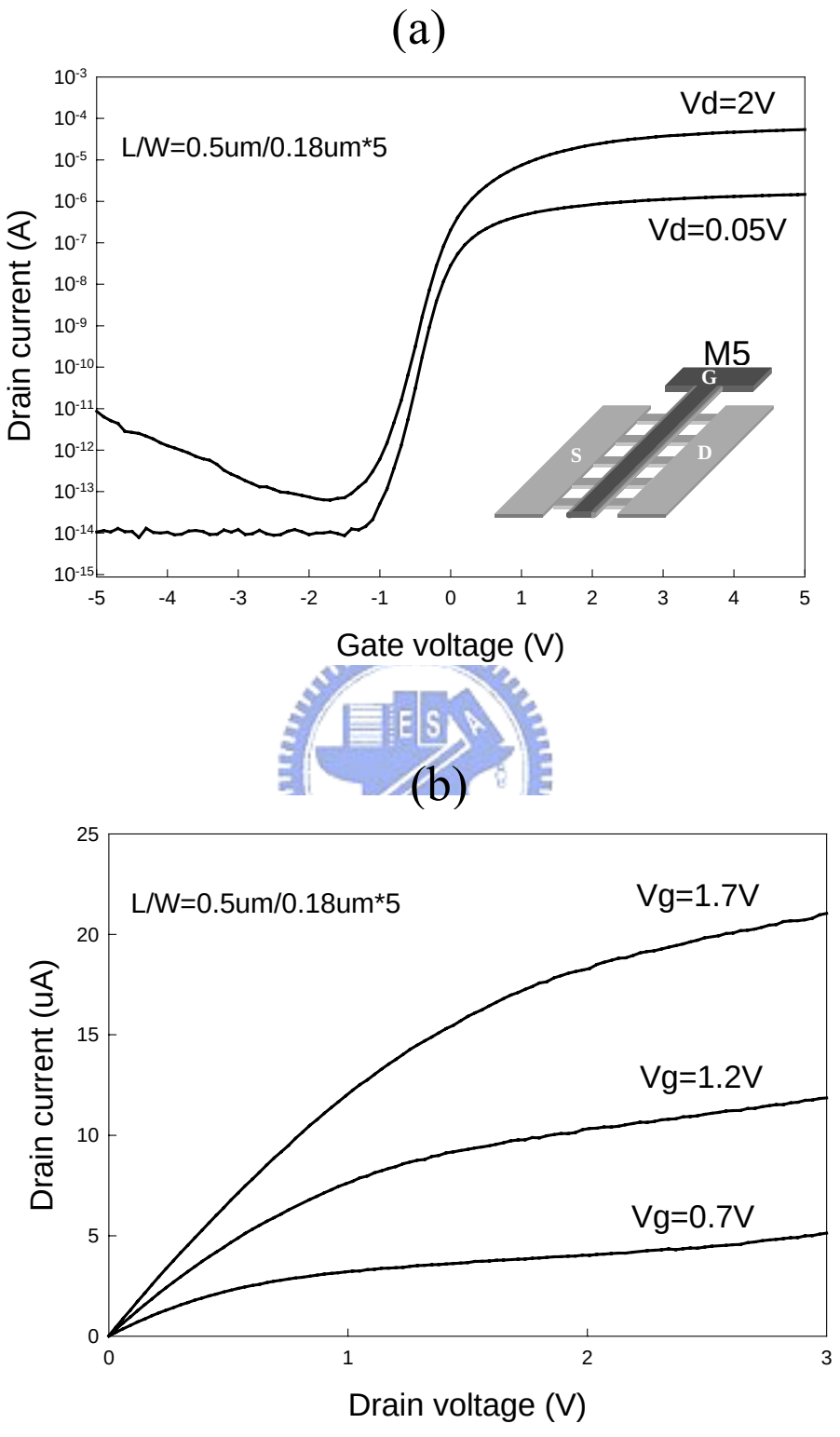

Fig. 3-6. Device characteristics of M5 (L / W = 0.5 um / 0.18 um × 5) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

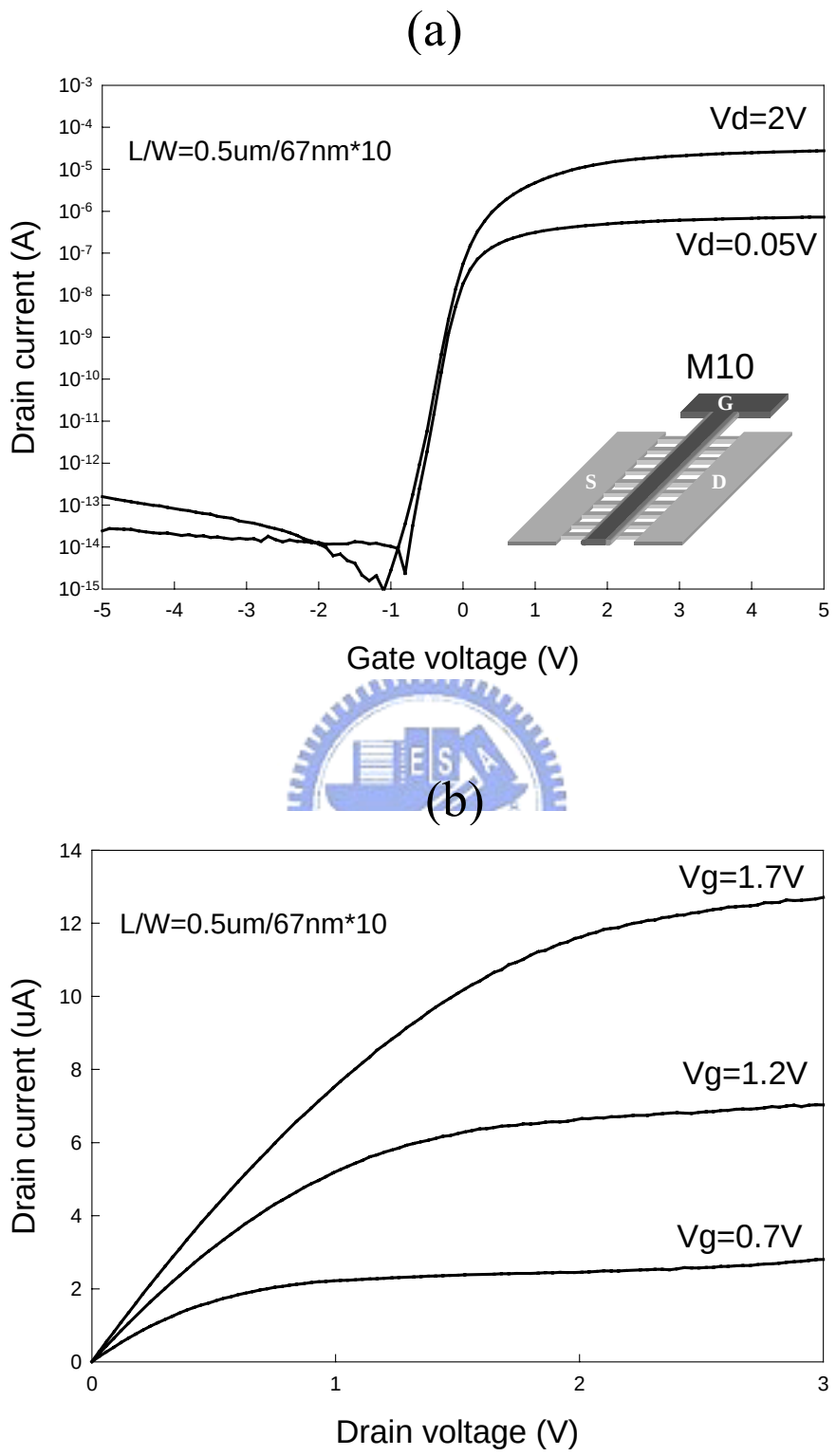

Fig. 3-7. Device characteristics of M10 (L / W = 0.5 um / 67 nm × 10) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

Table 3-2. Devices average and standard deviation parameters of S1, M2, M5 and M10. Number inside the bracket is parameter's standard deviation. All parameters were extracted at V_d = 2V, except for the field-effect mobility which were extracted at V_d = 0.05 V.

Device Name	Mobility (cm^2/VS)	V_{th} (V)	SS (mV/dec.)	Ion / Ioff	DIBL (V/V)
M10	37.95 (3.97)	0.15 (0.11)	137 (23)	7.36×10^9	0
M5	41.77 (3.91)	0.06 (0.15)	172 (56)	1.60×10^9	0.06(0.02)
M2	37.21 (2.88)	0.11(0.39)	324 (75)	6.69×10^7	0.25(0.09)
S1	38.44 (3.39)	0.03 (0.23)	334 (140)	2.23×10^8	0.32(0.09)

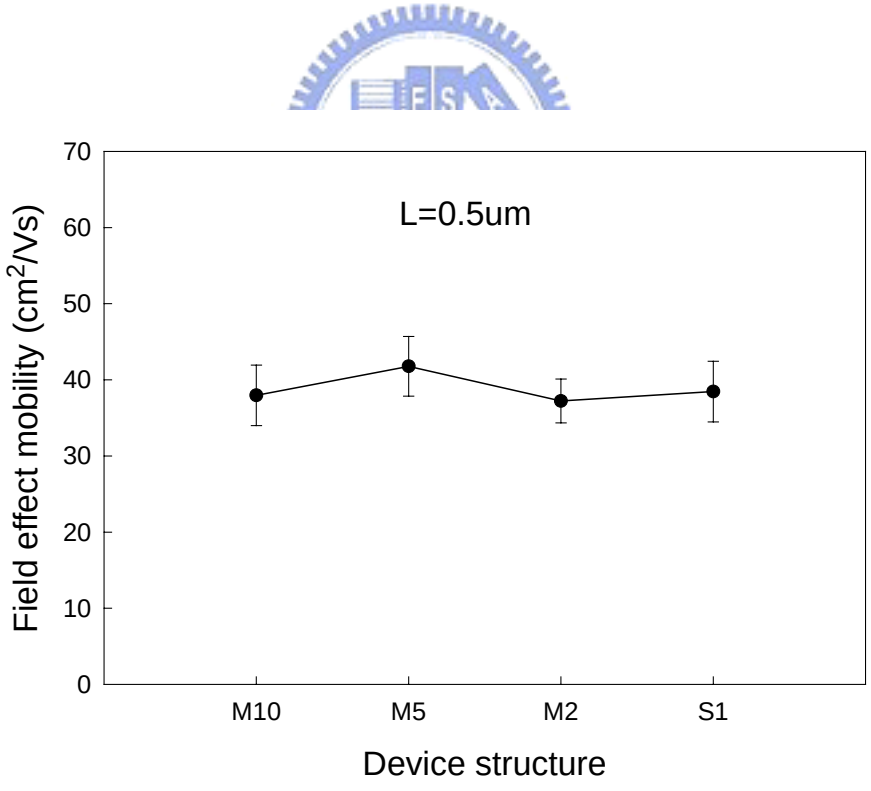

Fig. 3-8. Field effect mobility (μ_{FE}) versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

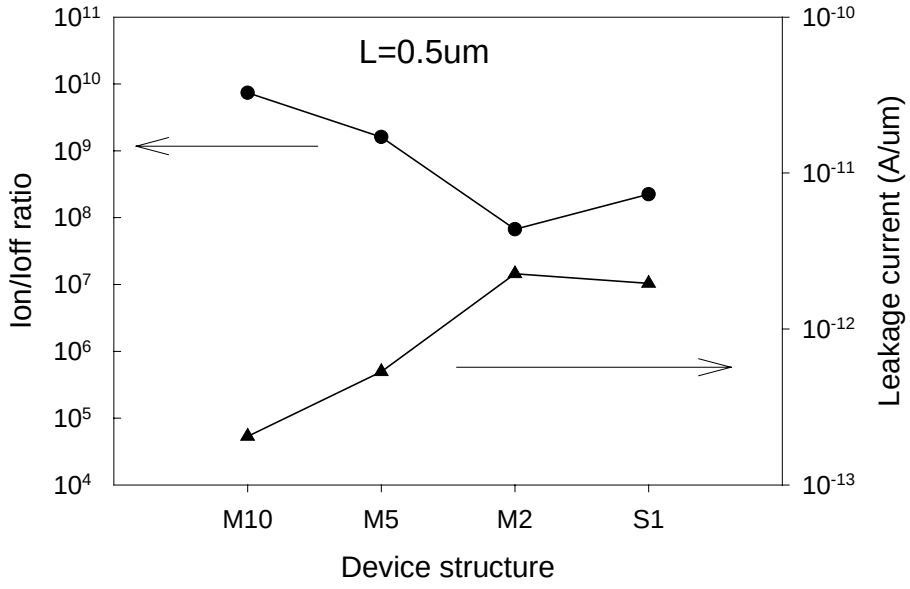

Fig. 3-9. Drain ON/OFF current ratio (R) and drain leakage current versus multi-channel with different widths poly-Si TFTs. The dots value present average value.

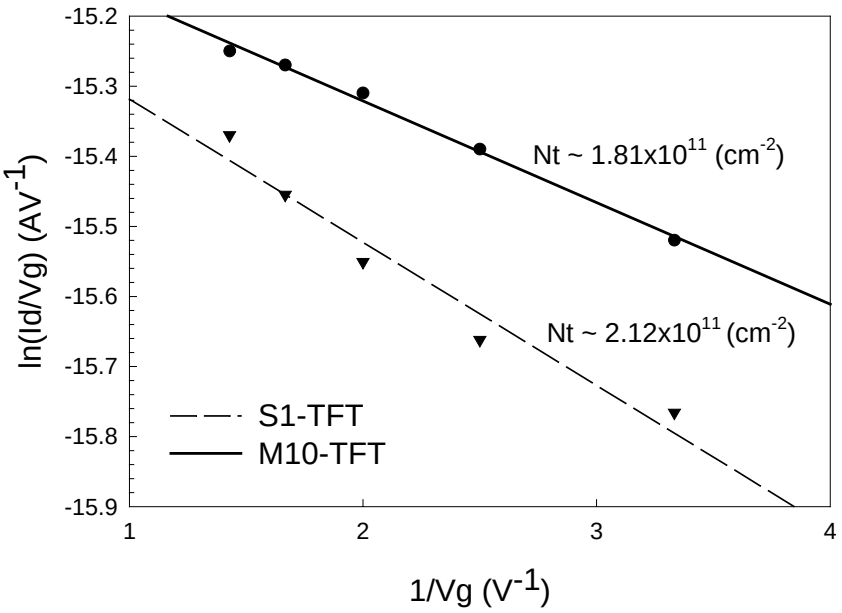

Fig. 3-10. Effective polysilicon grain boundary trap state density (N_t) of M10 and S1 poly-Si TFTs.

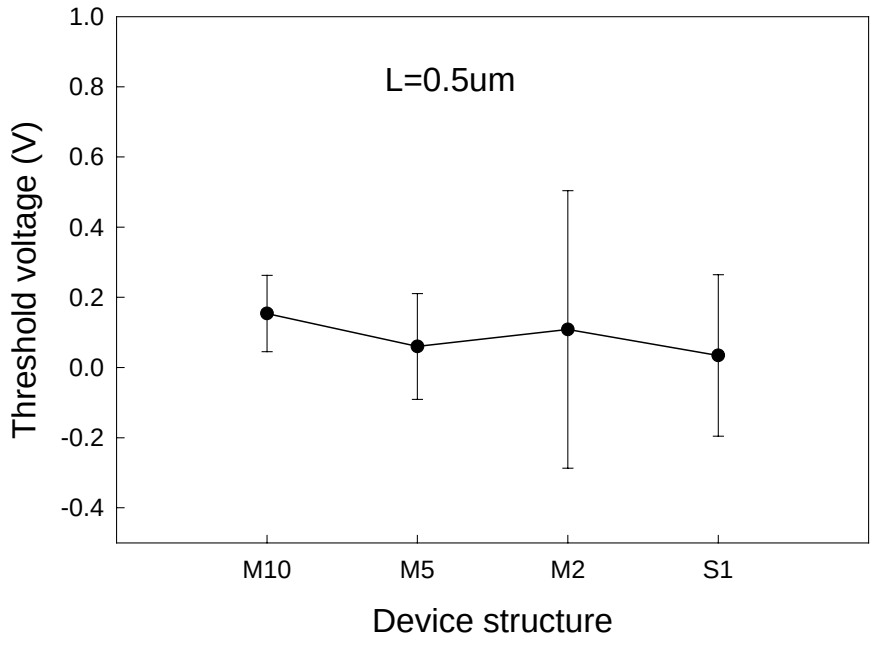

Fig. 3-11. Threshold voltage (V_{th}) versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

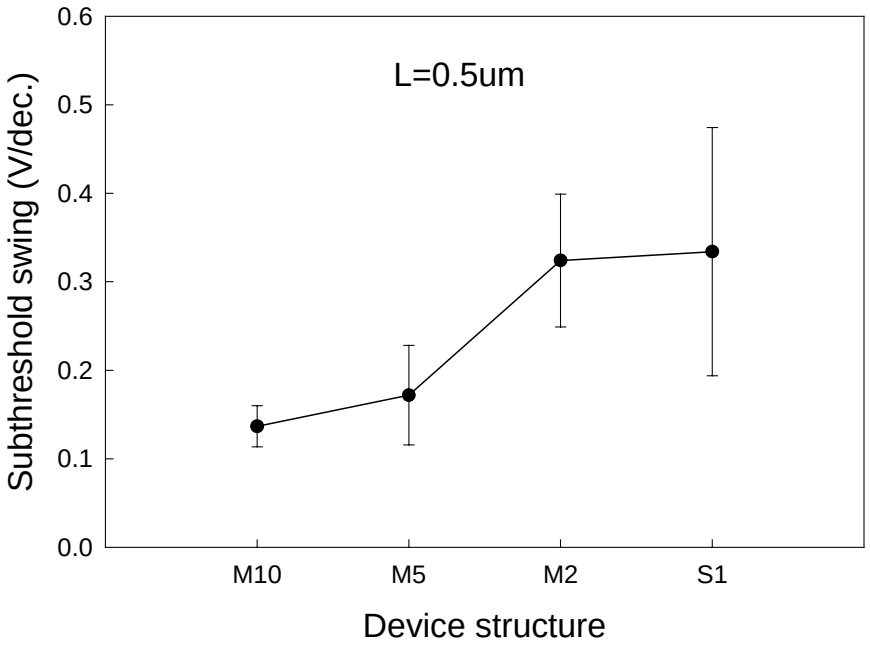

Fig. 3-12. Subthreshold slope (*SS*) versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

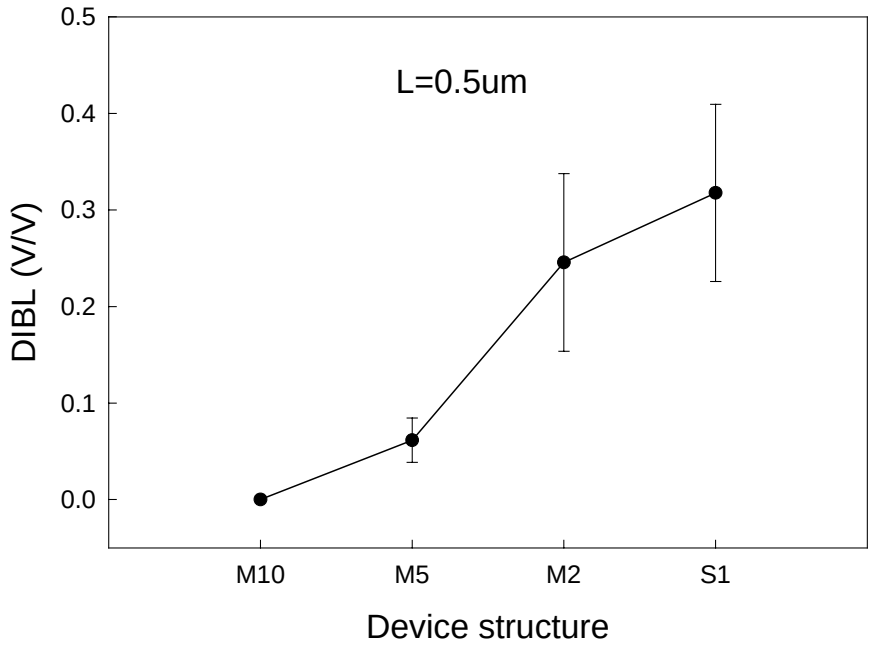

Fig. 3-13. Drain induced barrier lowering (*DIBL*) value versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.