Chapter 4

Reliability Study of Poly-Si TFTs with Multiple Nanowire Channels under DC and AC Hot-Carrier Stress

4.1 Introduction

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1], and organic light-emitting diodes (OLEDs) [2]. Except large area displays, poly-Si TFTs also have been applied for memory devices such as dynamic random access memory (DRAM) [3], static random access memory (SRAM) [4]. However, reliability of ploy-Si TFT is one of the main constraints toward this direction. In comparison with single-crystalline silicon, granular structure of poly-Si is rich in grain boundary defects arising from lattice discontinuities between different oriented grains as well as intra-grain defects. Moreover, a low process temperature, i.e. less than 600 ^{0}C, also produces numerous defects at the poly-Si\SiO_2 interface and poly-silicon boundaries. Under the operation of high drain voltage and a relatively high gate voltage (hot-carrier condition), the defects acting as trapping centers lead to hot-carrier injection that generates trap states. Thus, those generated trap states are strongly influenced the performance of poly-TFTs and causes

severe device characteristics degradation, such as threshold voltage (Vth), subthreshold swing (SS), ON current (Ion), and transconductance (Gm). The Gm degradation and Vth variation during stress application which results in improper operation and circuit failure is of great importance for circuit designers in order to integrate TFTs in flat-panel displays or VLSI circuits. In AMLCD application, unlike pixel TFTs, TFTs in the driver circuits are subject to high-frequency voltage pulses [5]. The degradation behavior under dynamic stress is closer to real operation condition than the static stress. Therefore, improvement of TFTs degradation under dynamic stress is most important requirements in realization of system-on-panel (SOP).

Accordingly, the reliability of poly-Si TFTs under dc [6]-[9], and ac [10]-[12] stress has been investigated. However, to our knowledge, improvement of poly-Si TFT degradation under ac stress by device structure modulation has not been addressed. Therefore, in this work, we develop a poly-Si TFT with ten nanowire channels and LDD structure to study the degradation mechanism; also a single-channel poly-Si was fabricated for comparison.

4.2 Poly-Si TFTs Hot-Carrier Stress effect theory background

4.2.1 Static Hot-Carrier Stress

According to the operation of poly-TFTs with grain boundary defects and intra-grain defects in Poly-Si film and a large number of interface states at the poor

SiO_2/poly-Si interface, most of the applied voltage drops across the grain boundaries since they have much larger resistances than the grains. The lateral electric field in the grain boundaries will be much higher than in the grains, and at large drain voltages, impact ionization may occur. Thus, unlike to the hot-carrier effect in MOSFETs, the poly-Si TFT electrical parameters such as threshold voltage (V_{th}), maximum transconductance ($G_{m,max}$), ON current (I_{on}), and subthreshold slope (SS) could depend on grain, grain boundaries, and/or interface properties. The deep traps existing in grain boundaries have been demonstrated to affect mainly threshold voltage and much less $G_{m,max}$ [13], [14]. On the other hand, tail states from grain regions in the interface and/or from grain boundaries mainly contribute to the decrease of gm max [15]. The subthreshold slope depends mainly on intra-grain traps distributed uniformly inside the poly-Si film and also on the deep interface states [16]. Therefore, it is obvious that depending on the nature of state generation after stress, electrical parameters can provide useful information in order to clarify poly-Si TFTs degradation under hot carrier stress conditions. These points are systemically summarized on the Table I [8].

Moreover, the poly-TFTs' non-ideal effect, Kink effect, which is due to the holes injected and stored in a floating body to cause the reduction of the threshold voltage and a parasitic bipolar element is resulting in positive-feedback effect to enhance the

generation of the hot-carriers [16]. This kink effect associated with float-body is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons.

4.2.2 Dynamic Hot-carrier Stress

Dynamic stress is closer to real operation condition than the static stress. It is reported that the reliability evaluation method proposed under the static stress conditions may not be suitable for the reliability evaluation under the dynamic stress [10]. According the pervious reports, the dynamic stress degradation mainly depends on the stress frequency (f), stress temperature, and falling time (Tf) [10]-[12], [17]. The dynamic stress degrades the poly-Si TFT more seriously than the static stress. The impact ionization generation hot electrons and hot holes near drain at ON state. However, as the device is changed from ON state to OFF state, the drain avalanche hot carrier will occur to cause serious degradation and generate more hot electrons and hot holes near drain [10]. At the switching period, a transient current ($I = C\,dV/dt$) can be observed to damage the device, and degradation is mainly dependent on falling time rather than rising time [17]. .

4.3 Device structure and fabrication

The single-channel and ten-nanowire channel poly-Si TFT structure and theirs fabrications are the same as described in chapter 3.2.

4.4 Results and discussion

The static hot carrier stress condition is determined at kink-effect occurrence, Vd = 6 V and Vg = 3V, and the source potential is common. The dynamic pulse train stress is defined at constant Vd = 6 V and dynamic Vg = 3V (ON), -3V (OFF) with the duty cycle of 50%, and the source potential is grounded. The waveform of the pulse train is shown in Fig. 4-1. In this section, we discuss the device reliability after a series of stress frequency (f), rising time (tr), falling time (tf) and substrate temperature (T) conditions.

Fig. 4-2 (a) depicts typical M10 poly-Si TFT I_d-V_g curves before and after dc hot carrier stress at 10000 second. Fig.4-2 (b) depicts typical S1 poly-Si TFT I_d-V_g curves before and after dc hot carrier stress at 10000 second.

Figure 4-3 depicts maximum conductance (Gm,max) degradation of S1 and M10 TFT as a function of the stress time with different frequencies (dc, f = 1K Hz, and f = 1M Hz). The S1 and M10 TFT show the similar Gm degradation. These results reveal that the S1 and M10 have similar tail state generation.

Figure 4-4 and 4-5 depict the threshold voltage and subthreshold swing variation of S1 and M10 TFT as a function of the stress time with different frequencies, respectively. For M10 TFT the Vth and SS variation is much lower than the S1 TFT. According to table I, these results indicate that the M10 TFT has less deep states

generation after dc and ac stress. Firstly, the M10 TFT has more effective NH_3 plasma passivation than that of S1 TFT due to the ten split nanowire channels of M10 TFT has wide NH_3 plasma passivation area. Secondly, M10 TFT has robust tri-gate control, thus the additional two side-gate surface scattering (Fig. 3b) reduce the hot carrier effect. Therefore, the deep-states generation of M10 TFT by the hot carrier impaction is lower than which of S1 TFT. Notably, for S1 TFT, the Vth and SS variation increase with the frequency increasing from 1 K Hz to 1 MHz. These results reveal that the device reliability is strongly dependent on the transient current Id (displace current).

$$I_d = C_{ox} \cdot \frac{dV_g}{dt} \approx C_{ox} \cdot f \cdot \overline{V_g}$$

where f is frequency, $\overline{V_g}$ is average gate voltage.

Thus, the transient current induced hot carrier is dependent on the frequency.

Figure 4-6 and 4-7 depict the ON current (I_{ON}) variation and ON/OFF ratio of S1 and M10 TFT as a function of the stress time with different frequencies, respectively. The M10 TFT shows lower I_{ON} variation than S1 TFT. These results reveal that the S1 TFT has high Vth variation and increase with the frequency increasing. Thus, the I_{ON} of S1 TFT is much lowering than that of M10 TFT. For the ON/OFF ratio, although the S1 and M10 TFT have the similar degradation behavior, the ON/OFF ratio of M10 still remains exceed 10^8, under different frequencies.

Figure 4-8 depicts Gm degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

For S1 TFT (dash-line) with the same falling time of 100 ns, the S1 TFT has the similar Gm degradation. However, for the same rising time of 100 ns, as the falling time increasing from 100 ns to 1 us, the Gm degradation is reduced from 40% to 20% at the stress time at 1000 second. These results reveal that the device reliability is strongly dependent on the transient current. According to the Uraoka et al. report [17], only the transient current induced by the falling period would cause more damage near the drain. Figure 4-9 indicates clearly that the amount of the hot carriers generated depends on the pulse falling time. Therefore, using the dynamic stress with longer falling time will be helpful for the reliability improvement in the poly-Si TFTs. On the other hand, for M10 TFT, however the Gm degradation dependent on falling time is not significant. These results indicate that M10 TFT has highly effective NH_3 plasma passivation and robust tri-gate control to screen the transient current hot carrier effect, which induced by the falling period.

Figure 4-10 and 4-11 depicts Vth variation and ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz. For the same reason, the Vth variation and ON current (Ion) degradation of S1 TFT (dash-line) is highly dependent on the falling time rather than rising time. As the falling time increasing from 100 ns to 1 us, the Vth variation and ON current (Ion) degradation are reduced. Again, M10 TFT has

highly effective NH_3 plasma passivation and robust tri-gate control to screen the transient current hot carrier effect, which induced by the falling period.

Figure 4-12 depicts Gm degradation of S1 and M10 TFT as a function of the stress time with different subtract temperature with 25^0C, and 75^0C under the same frequency of 1 KHz, and the same Tr = Tf =100 ns. For both S1 and M10 TFT, the Gm degradation is reduced with the temperature increasing from 25^0C to 75^0C. These results reveal that hot carrier effect is reduced with the temperature increasing. As the temperature increasing, the mean free path (λ) [18] is decreasing.

$$\lambda = \lambda_0 \cdot \tanh(\frac{E_P}{2kT})$$

Thus, that hot carrier energy is reduced as the mean free path (λ) is decreasing.

Figure 4-13 and 4-14 depicts Vth variation and ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with 25^0C, and 75^0C under the same frequency of 1 KHz, and the same Tr = Tf =100 ns. For both S1 and M10 TFT, the Vth variation and ON current (Ion) degradation is reduced with the temperature increasing from 25^0C to 75^0C. For the same reason, hot carrier effect is reduced with the temperature increasing as the mean free path (λ) decreasing.

4.5 Conclusion

The performance and ac and dc reliability of multiple nanowire poly-Si TFTs are investigated. The experiment results reveal that the multiple nanowire poly-Si TFTs

has higher performance than single-channel TFT, including a high ON/OFF current ratio, a low subthreshold slope, an absence of DIBL and favorable output characteristics. In static and dynamic hot-carrier stress experiments, the multiple nanowire poly-Si TFTs reduces the degradation of Vth, SS, Ion, On/OFF ratio and DIBL, for all kind of frequency, rising time, falling time and temperature, compared to single-channel TFT. These high reliability results of multiple nanowire poly-Si TFTs can be explained by its robust tri-gate control and its superior channel NH_3 passivation on the poly-Si grain boundary. The fabrication of this novel multiple nanowire channels structure TFTs is easy and involves no additional processes. Such TFTs are thus highly promising for use in future high-performance poly-Si TFT applications.

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Table 4-1. Variation of experimental electronic parameters and corresponding possible degradation mechanics.

Electrical parameters after stressing	**Mainly depending on**
Δg_{mmax}	Interface state generation State generation in the grain boundaries (tail state)
ΔVon	Charge injected into the gate oxide Interface state generation (deep states) State generation in the grain boundaries(deep states)
ΔS (subthreshold swing)	Intra-grain defect density generation (bulk state) Interface state generation (deep states)

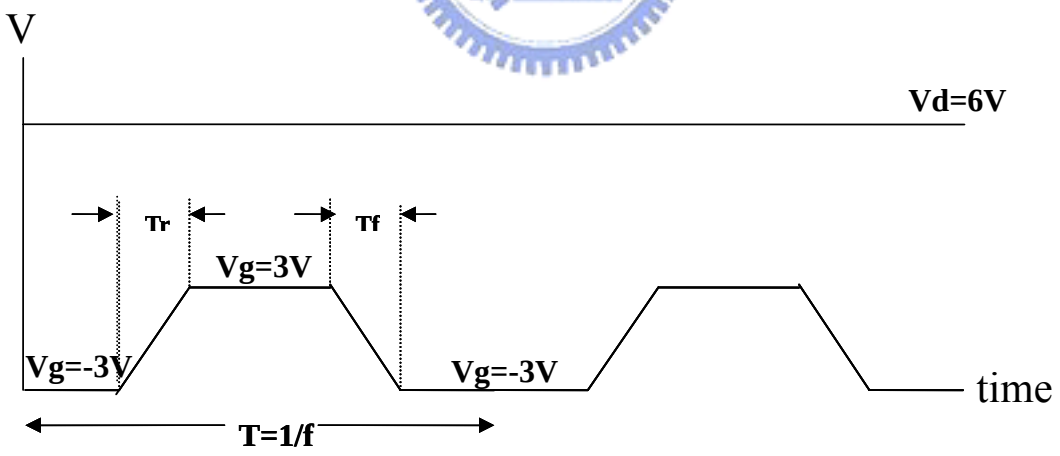

Fig. 4-1. The dynamic pulse train stress is defined at constant Vd = 6 V and dynamic Vg = 3V (ON), -3V (OFF) with the duty cycle of 50%, and the source potential is common.

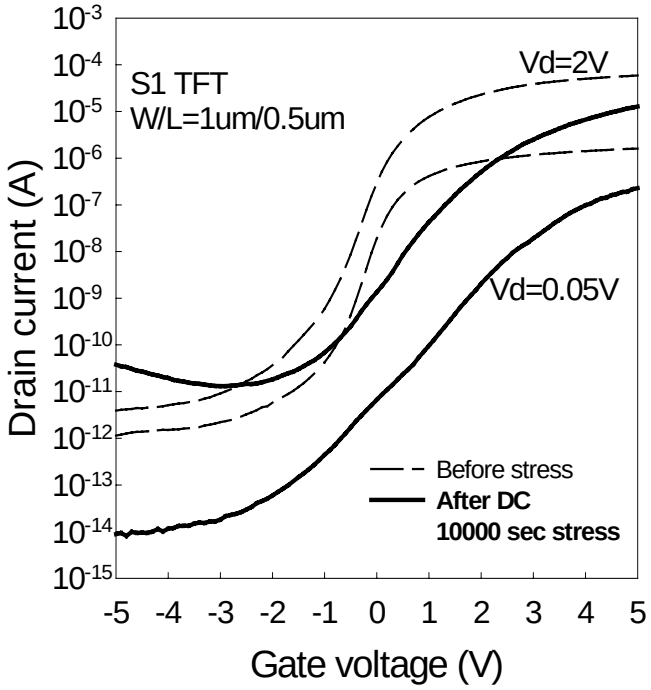

Fig. 4-2a Typical M10 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

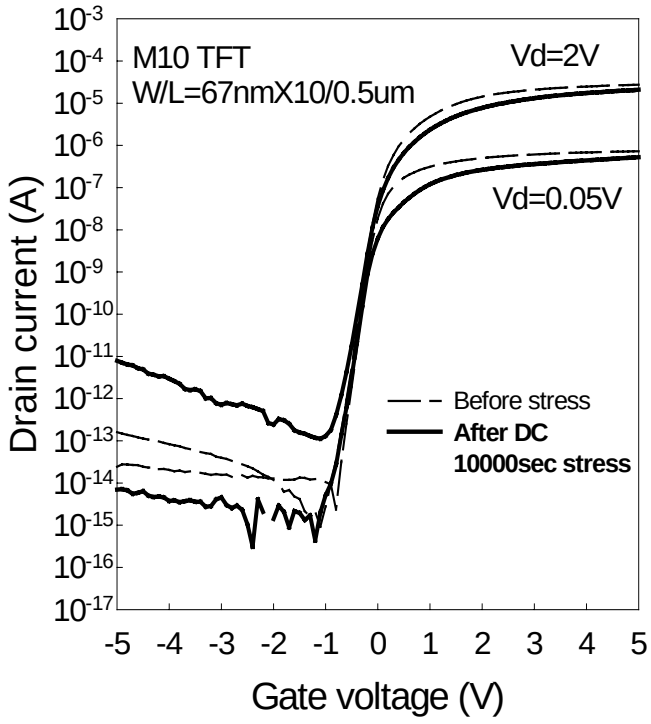

Fig. 4-2b Typical S1 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

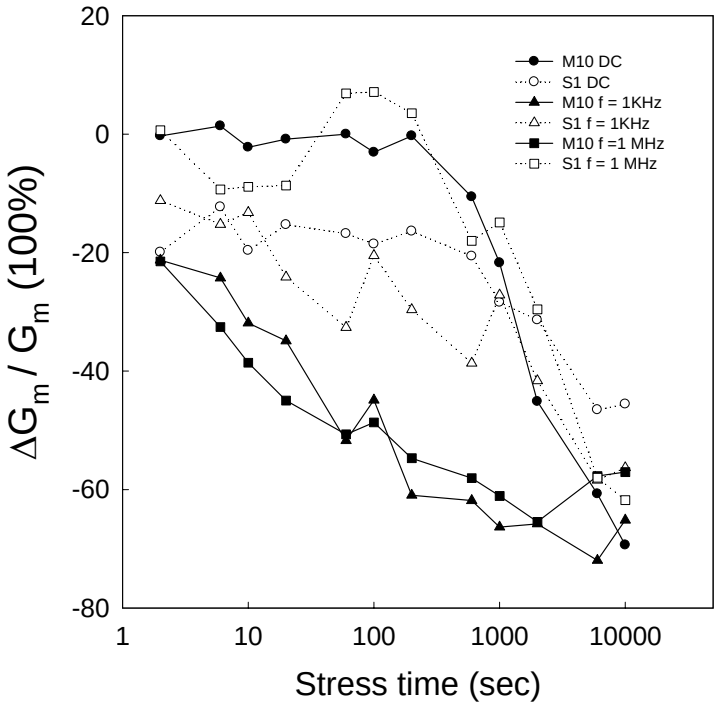

Fig. 4-3 Maximum conductance (Gm,max) degradation of S1 and M10 TFT as a function of the stress time with different frequencies (DC, f = 1K Hz, and f = 1M Hz).

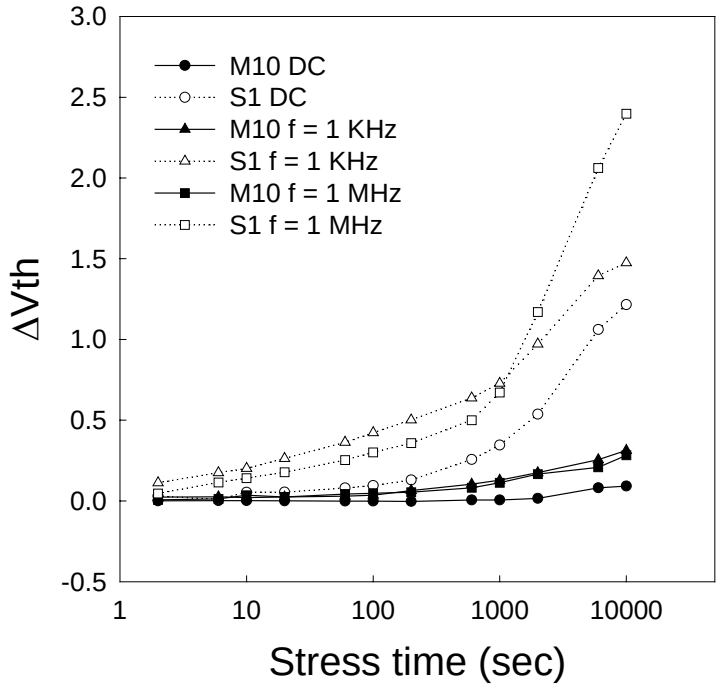

Fig. 4-4. Threshold voltage of S1 and M10 TFT as a function of the stress time with different frequencies.

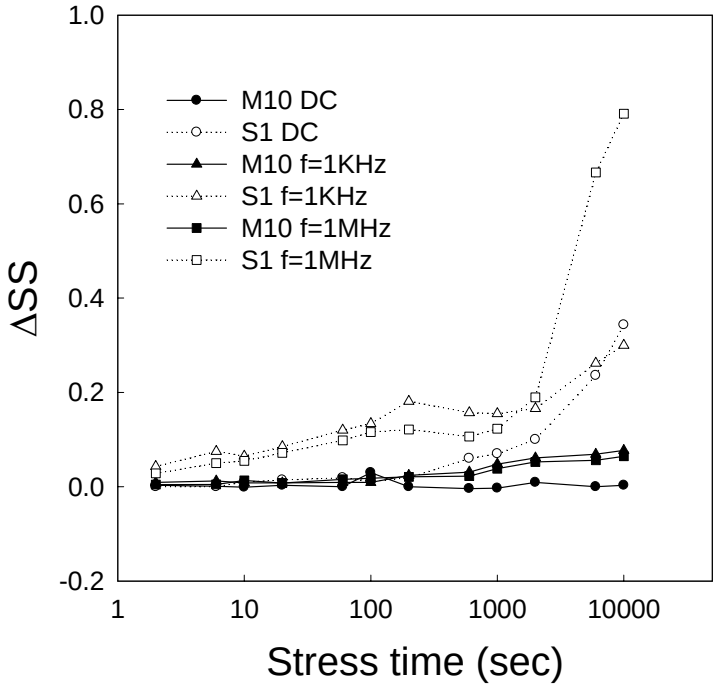

Fig. 4-5. Subthreshold swing variation of S1 and M10 TFT as a function of the stress time with different frequencies.

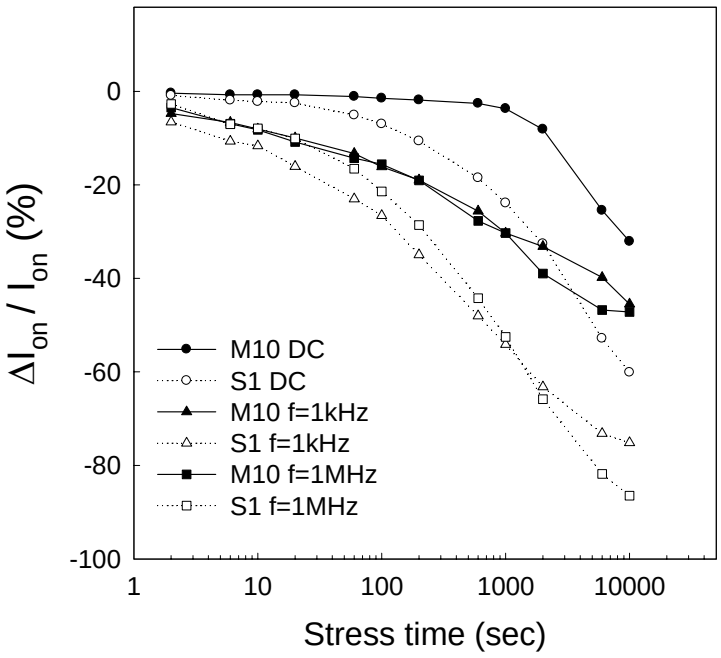

Fig. 4-6. ON current (I_{ON}) variation of S1 and M10 TFT as a function of the stress time with different frequencies.

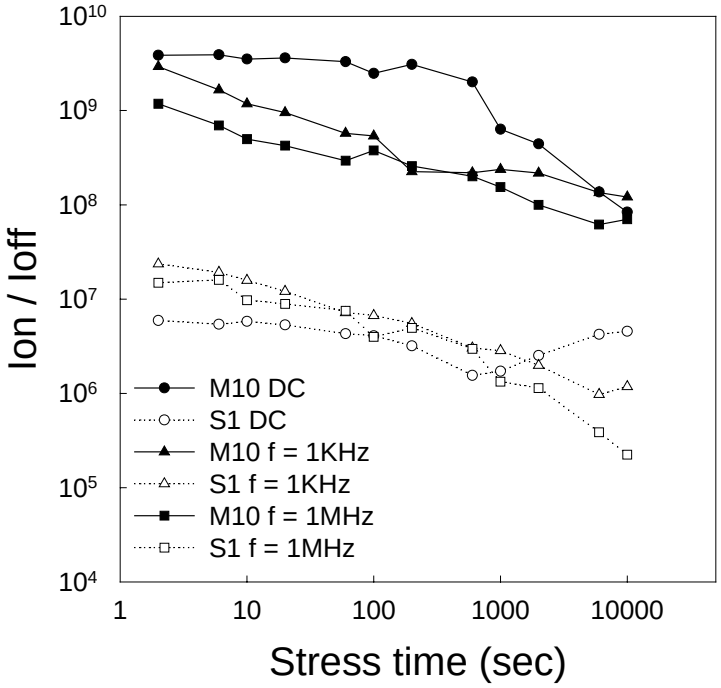

Fig 4-7. ON/OFF ratio of S1 and M10 TFT as a function of the stress time with different frequencies.

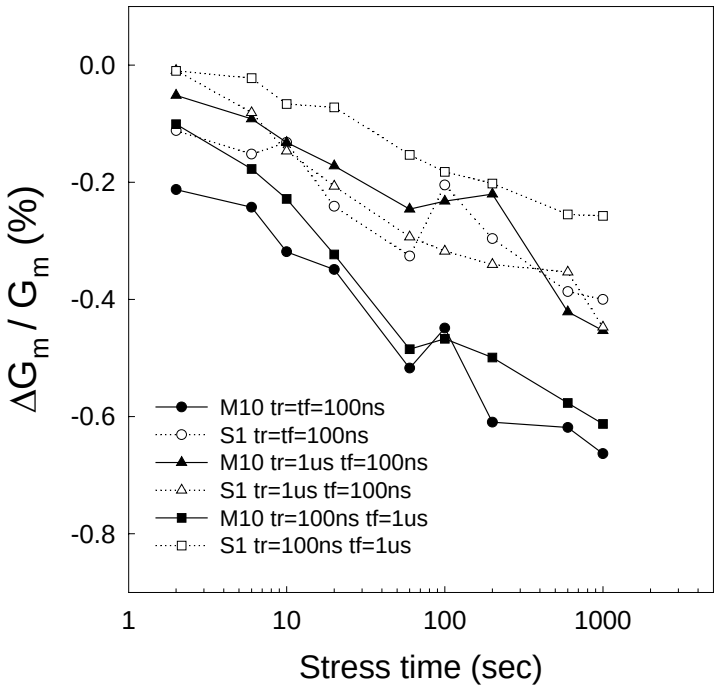

Fig. 4-8. Gm degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

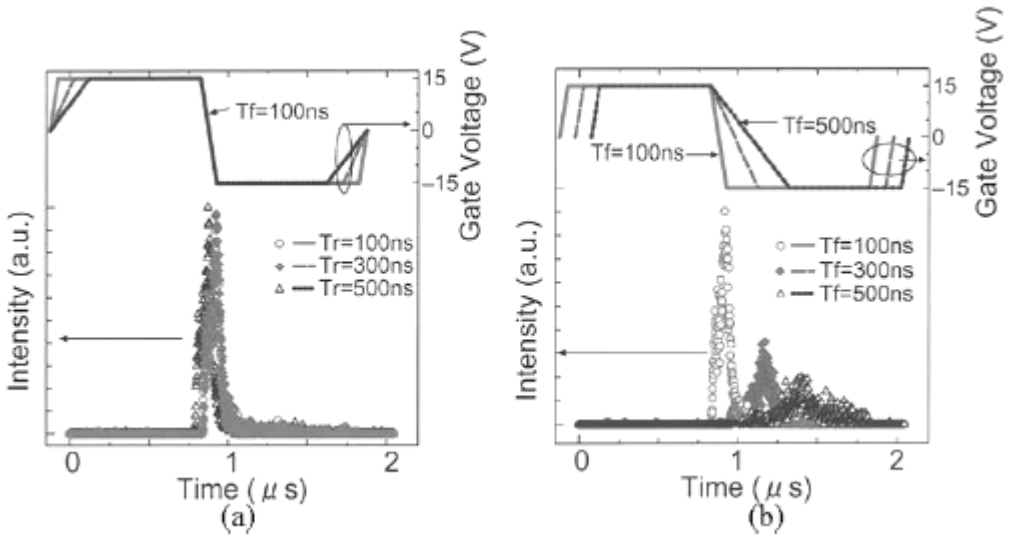

Fig. 4-9. Dependence of emission intensity on (a) pulse rise time and (b) pulse fall time. Emission intensity is independent of the pulse rise time. However, we have found that it strongly depends on the fall time [17].

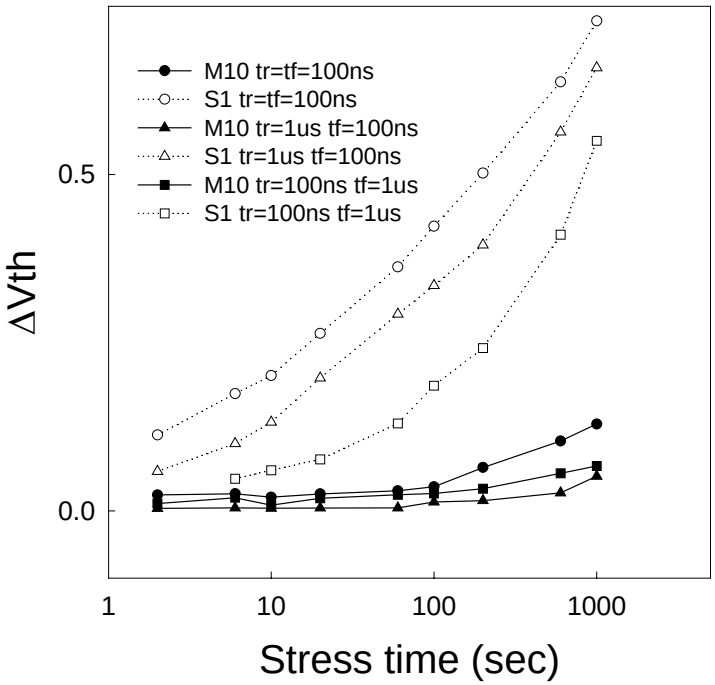

Fig. 4-10. Vth variation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

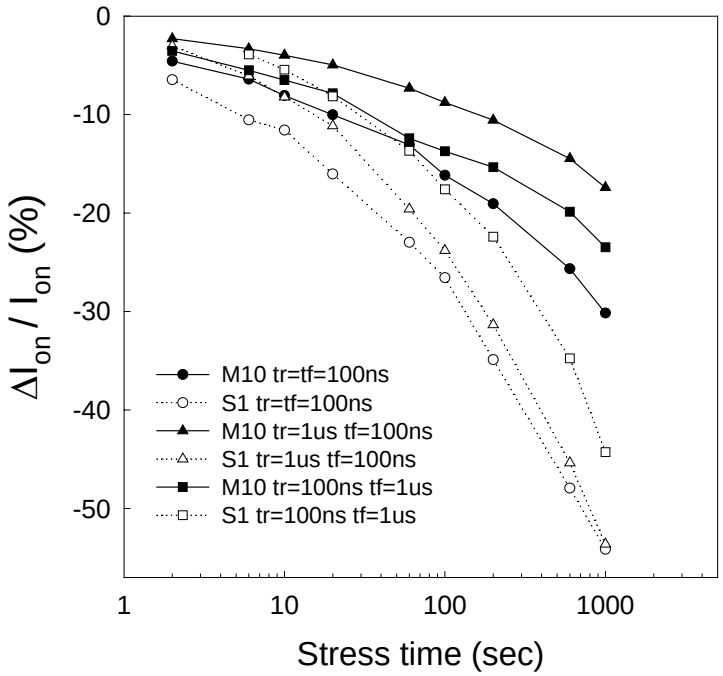

Fig 4-11. ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

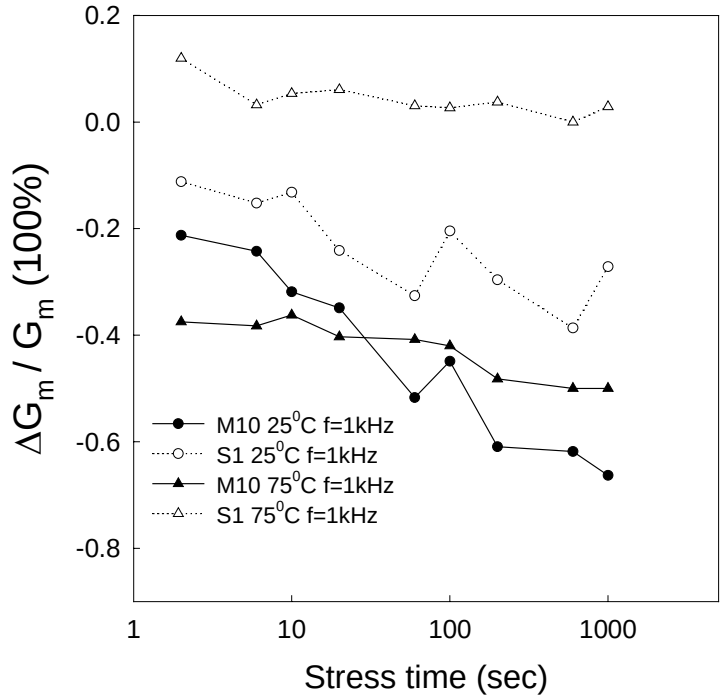

Fig. 4-12. Gm degradation of S1 and M10 TFT as a function of the stress time with different subtract temperature with 25^{0}C, and 75^{0}C under the same frequency of 1 KHz.

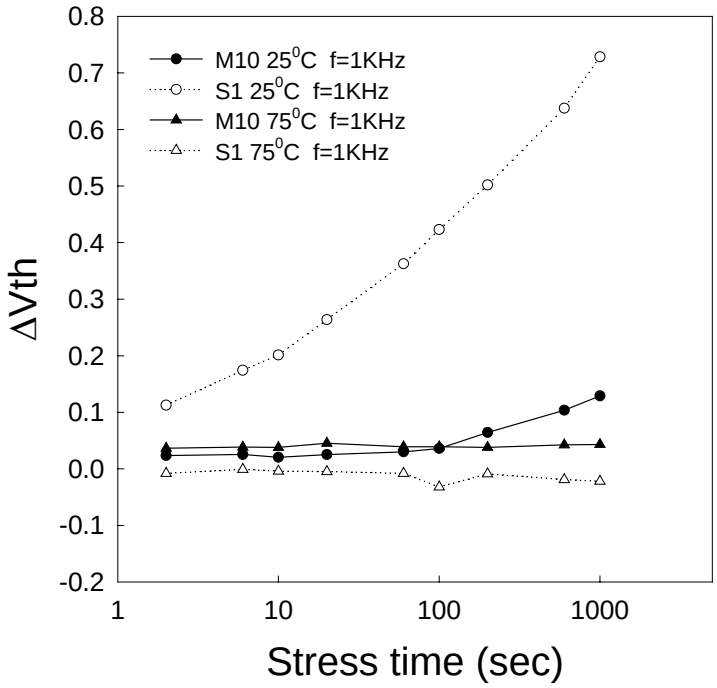

Fig. 4-13. Vth variation of S1 and M10 TFT as a function of the stress time with 25^0C, and 75^0C under the same frequency of 1 KHz

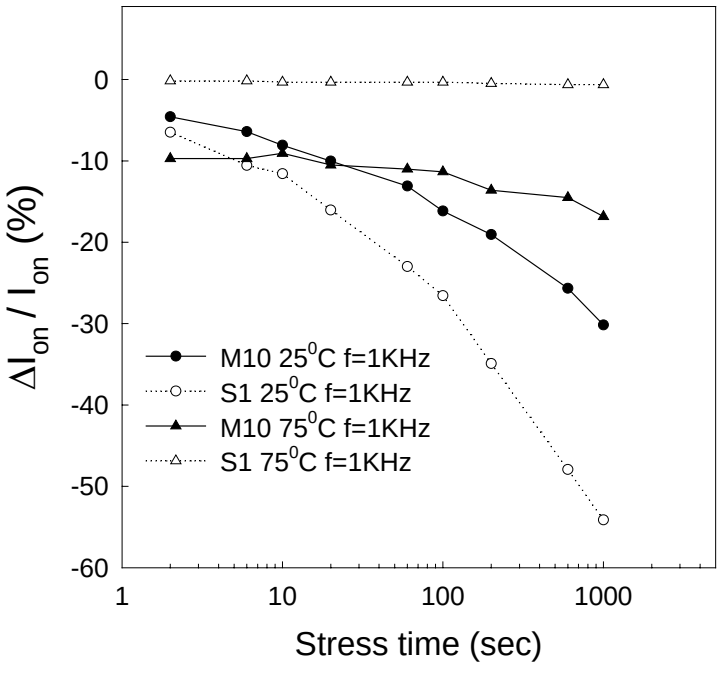

Fig 4-14. ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with 25^0C, and 75^0C under the same frequency of 1 KHz