

Chapter 5

Mobility Enhancement of Polysilicon Thin-Film Transistor using Nanowire Channels by Pattern-dependent Metal-Induced Lateral Crystallization

Abstract

A method for enhancing the mobility of the polysilicon thin-film transistor (poly-Si TFT) by pattern-dependent metal-induced-lateral-crystallization (PDMILC) using nanowire channels was demonstrated and characterized. The experimental results indicate that the field-effect mobility of PDMILC TFT was enhanced as the channel width decreased, because the lateral length of its poly-Si grain was increased. The ten nanowire channels (M10) PDMILC poly-Si TFT had the greatest field-effect mobility of $109.34 \text{ cm}^2/\text{Vs}$ and the smallest subthreshold swing (SS) of 0.23 V/dec at the gate length of $2 \text{ }\mu\text{m}$. The field-effect mobility also increased with the decline in the gate length in the M10 PDMILC poly-Si TFT device, because the number of poly-Si grain boundary defects was reduced.

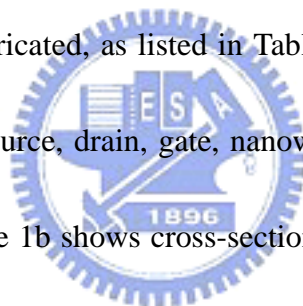
5.1 Introduction

The main benefit of applying polysilicon thin-film transistors (poly-Si TFTs) in the active matrix liquid crystal display (AMLCDs) is the greatly improved carrier mobility (larger than $10 \text{ cm}^2/\text{Vs}$) in the poly-Si film, the capacity to integrate the pixel switching elements and the capacity to integrate the panel array and the peripheral driving circuit on the same substrates¹⁻³. bring the era of system-on-panel (SOP). For making high performance poly-Si thin film transistors (TFTs), low-temperature recrystallization for poly-Si thin-film technology is required for the realization of commercial flat-panel displays (FPD) on inexpensive glass substrates, since the maximum process temperature is less than 600°C . There three major low-temperature amorphous-Si crystallization methods for producing high-performance poly-Si thin films are solid phase crystallization (SPC)⁴, excimer laser crystallization (ELC)⁵ and metal-induced lateral crystallization (MILC)⁶⁻¹⁰. MILC technology was originally developed as a low-temperature crystallization technique, and it is superior because, unlike ELC, it is a low-cost batch process and unlike SPC, it yields a higher quality poly-Si thin film.

However few reports on MILC poly-Si TFT have addressed the effects of the device dimensions on the field-effect mobility. Besides, the applications of TFTs are mainly limited to low-temperature flat-panel displays because the grain boundaries in

the channel region substantially degrade performance. The electrical properties of the TFTs can be improved by enlarging the grains, and the number of grain boundaries in the channel region can be minimized^{11, 12}. Therefore, in this work, we develop a series of multi-channel with different widths pattern-dependent MILC TFTs (PDMILC TFTs) to study the relationship between the device dimensions and the field-effect mobility.

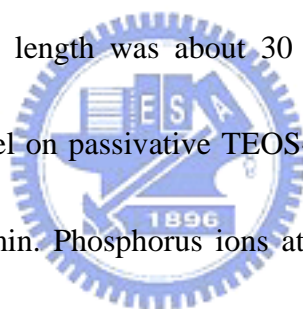
In this work, a series of PDMILC TFTs, with a gate length of 2 μm , consisting of ten strips of 67 nm wire channels (M10) TFT, five strips of 0.18 μm channels (M5) TFT, two strips of 0.5 μm channels (M2) TFT and a single-channel structure (S1) with width of 1 μm TFT, were fabricated, as listed in Table I. Figure 1a shows schematic plot of PDMILC TFT with source, drain, gate, nanowire channels, contact holes and MILC seeding window. Figure 1b shows cross-section view of PDMILC TFT, which was a conventional top-gate offset MOSFET structure.



5.2 Device structure and fabrication

6-inch p-type single crystal silicon wafers were coated with 400 nm-thick SiO_2 as the starting materials. Undoped 50 nm-thick amorphous-Si (a-Si) layer were deposited by low-pressure chemical vapor deposition (LPCVD) at 550 $^{\circ}\text{C}$. Then the active islands, including source, drain and ten nanowire channels were patterned by Electron Beam lithography (EBL) and transferred by reactive ion etching (RIE). After defining the active region, the 25 nm-thick tetra-ethyl-ortho-silicate oxide

(TEOS-SiO₂) was deposited by LPCVD as gate insulator. Then, 150 nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100 nm-thick TEOS-SiO₂ layer as passivation layer was deposited by LPCVD. Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Then, a thin 10 nm-thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550 °C for 48 hrs in an N₂ ambient. The average lateral crystallization length was about 30 μm (Fig. 2b). After long time annealing, the unreacted nickel on passivative TEOS-SiO₂ were removed by H₂SO₄ solution at 120 °C with 10 min. Phosphorus ions at a dose of 5×10^{15} cm⁻² were implanted through the passivative TEOS-SiO₂ to form the n+ gate, source/drain regions and the self-aligned offset region of 0.1 μm width were formation in the same process step (Fig. 1b). Then, the dopants were activated by rapid thermal annealing (RTA) at 850 °C with 30 sec. The 300 nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain and gate metal pads. Then, the finished devices were sintered at 400 °C for 30 minutes in an N₂ ambient. Finally, each device was passivated by NH₃ plasma treatment for 2 hours at 300 °C.



5.3 Results and discussion

Figure 2a shows scanning electron microscopy (SEM) photography of active pattern of M10 TFT with the source, the drain, ten nanowire channels and MILC seeding window. The inset SEM photography depicts a magnified area of ten nanowire channels in the TFT, each of which is 67 nm wide. Figure 2b shows SEM photography of active channel of single-channel MILC poly-Si TFT grain structure after Secco etching¹³. The average poly-Si lateral grain size is about 250 nm. The inset optical microscopy photography in Fig. 2b depicts a MILC length of 30 μm , which is longer than 16 μm (Fig. 1a) to promise the whole active channel was crystallized by MILC process. Figure 2c shows SEM photography of grain structure in one of ten nanowire MILC poly-Si TFT (M10) after Secco solution etching. The average poly-Si lateral grain size is about 520 nm in M10 TFT, which is larger than those of S1 TFT. This result reveals that the nanowire of M10 TFT enhanced the poly-Si grain growth laterally during the MILC process. Figure 3 compares the transfer curves and the field-effect mobility of a series of PDMILC TFT of multi-channel with different widths at the gate length (L) of 2 μm . The field-effect mobility (μ_{FE}) was extracted from the peak linear trans-conductance (g_m) at $V_d = 0.1$ V:

$$\mu_{FE} = \frac{L}{C_{ox} \cdot W \cdot V_d} g_m \quad (1)$$

The results in Fig. 3 reveal that the μ_{FE} of PDMILC TFT was enhanced with each channel width decreasing. The M10 TFT had the highest μ_{FE} value of 107.79 cm^2 / Vs , which was almost triple the S1 TFT of 46.62 cm^2 / Vs . According to the poly-Si TFT mobility model¹⁴, the effective field-effect mobility (μ_{FE}) is given by,

$$\mu_{FE} = \mu_G \frac{1}{1 + (\mu_G / \mu_{GB}) [(nL_{GB}) / L] \exp(qV_b / kT)} \quad (2)$$

μ_{FE} effective field-effect mobility;

L_{GB} average grain boundary length;

$n = L/L_G$ average grain-boundary number;

L_G average intra-grain length.

The results reveal that during the MILC process, the poly-Si grain lateral length (L_G) increases as the channel width declines. Therefore, the average grain-boundary number (n) was reduced, and the mobility was increased. Moreover, M10 TFT had the highest μ_{FE} . During the MILC process, a nanowire width of 67 nm strongly limited the growth of poly-Si grains in the z-direction (Fig. 1a) than others TFTs. Therefore, the poly-Si grains tended to grow laterally in the x-direction, becoming large, as shown in Fig. 2c. For investigation of device performance uniformity, each dimension including three TFTs in different areas on the 6-inch wafer were characterized. Table II lists all of the poly-Si TFTs parameters with average and

standard deviation value, including the field-effect mobility (μ_{FE}), the threshold voltage (V_{th}) and the subthreshold swing (SS). The values of Table II indicate that the μ_{FE} is uniform distribution of this PDMILC fabrication. Notably, the grain enhancement in M10 TFT not only increased μ_{FE} , but also reduced SS to 0.23 V/dec.

The parameter SS is directly related to the total trap states density (N_T) by,¹⁵

$$SS = \left(\frac{kT}{q}\right) \ln 10 \left(1 + \frac{q^2 t_{Si} N_T}{C_{ox}}\right) \quad (3)$$

where kT is thermal energy, C_{ox} is the gate oxide capacitance per unit area and t_{Si} is the poly-Si layer thickness. Thus, the decline of SS as the channel width decreased reveals that increasing the lateral size of the poly-Si grain reduces N_T .

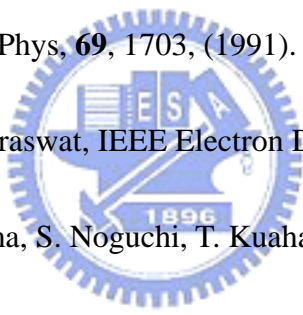
Figure 4 plots μ_{FE} average and stand deviation value versus the gate length, for a particular M10 TFT structure. When the TFTs' channel width dimensions were equal, the mobility substantially increased as the gate length was reduced. These results suggest that the number of poly-Si grain boundary defects decreased, as the gate length was reduced⁷.

5.4 Conclusion

A method of enhancing the mobility of poly-Si TFTs using nanowire channels by pattern-dependent metal-induced lateral crystallization was proposed and the TFTs fabricating using such a method were characterized. The pattern-dependent metal-induced lateral crystallization of poly-Si TFTs increased the field-effect

mobility by reducing the channel width. The PDMILC poly-Si TFT with the ten nanowire channels (M10) has the highest field-effect mobility and the lowest subthreshold swing. This method of fabrication of PDMILC TFTs with enhanced mobility is easily implemented; involves no additional mask and is compatible with CMOS technology. Such a PDMILC TFT is thus highly suitable for use in future system-on-panel (SOP) applications and three-dimensional (3-D) integrated circuits applications.

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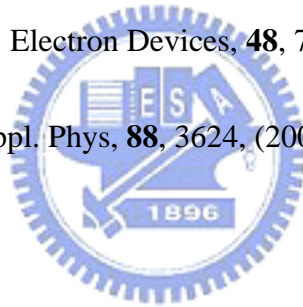


Table 5-1. Devices dimension of S1, M2, M5 and M10 PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm, gate TEOS-oxide thickness of 25 nm and gate length of 2 μm .

Device name	Gate length (L)	Channel number	Each channel width (W)	Effective channel width (W_{eff})
S1	2 μm	1	1 μm	1 μm
M2	2 μm	2	0.5 μm	1 μm
M5	2 μm	5	0.18 μm	0.9 μm
M10	2 μm	10	67 nm	0.67 μm



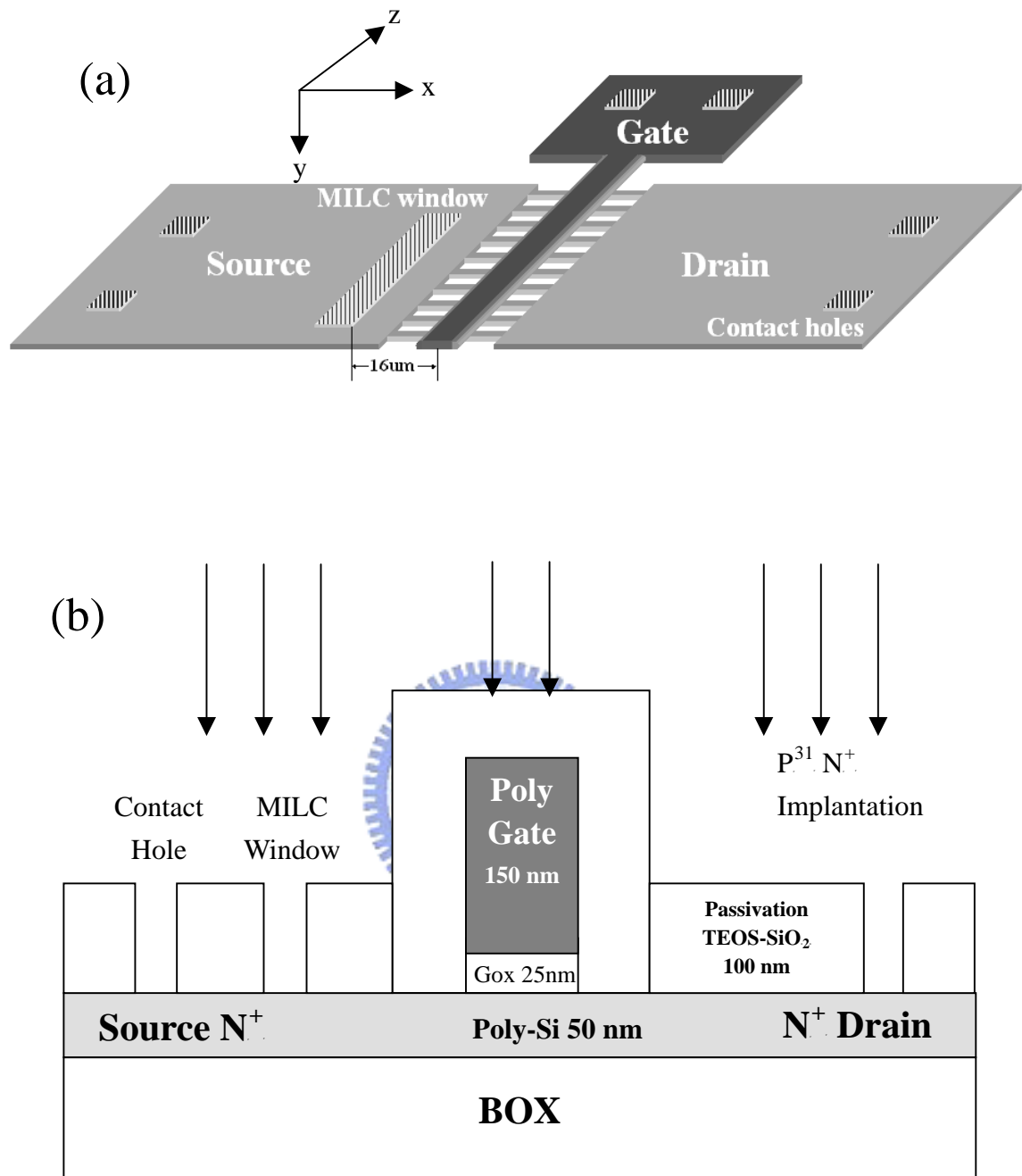


Fig. 5-1. (a) Schematic plot of PDMILC M10 poly-Si TFT with source, drain, gate, ten nanowire channels, contact holes and MILC seeding window. The distance between the MILC seeding window edge and middle of active channel is 16 µm. (b) Cross-section view of PDMILC TFT, which was a conventional MOSFET with offset structure.

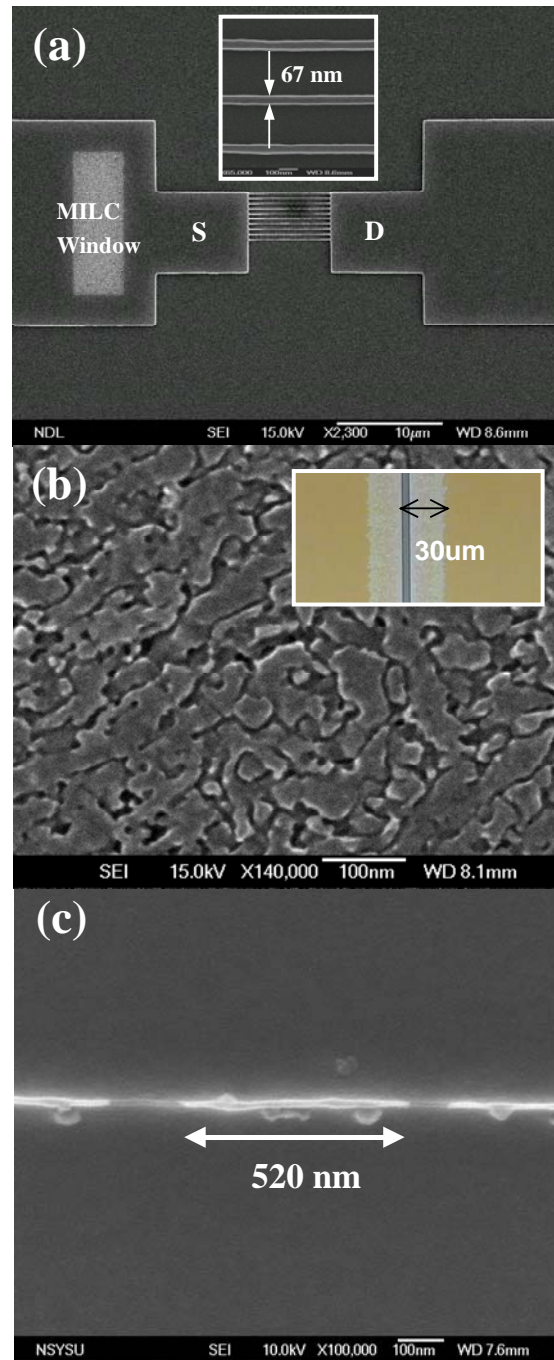


Fig. 5-2. (a) Scanning electron microscopy (SEM) photograph of active pattern with the source, the drain, ten nanowire channels and MILC seeding window. The inset SEM photograph shows the each nanowire width of 67 nm. (b) SEM photograph of poly-Si grain structure in active channel of S1 MILC poly-Si TFT after Secco solution etching. The average poly-Si lateral grain size is 250 nm. The inset optical microscopy photograph depicts a MILC length of 30 μm. (c) SEM photograph of grain structure in one of ten nanowire MILC poly-Si TFT (M10) after Secco etching. The poly-Si lateral grain length is 520 nm.

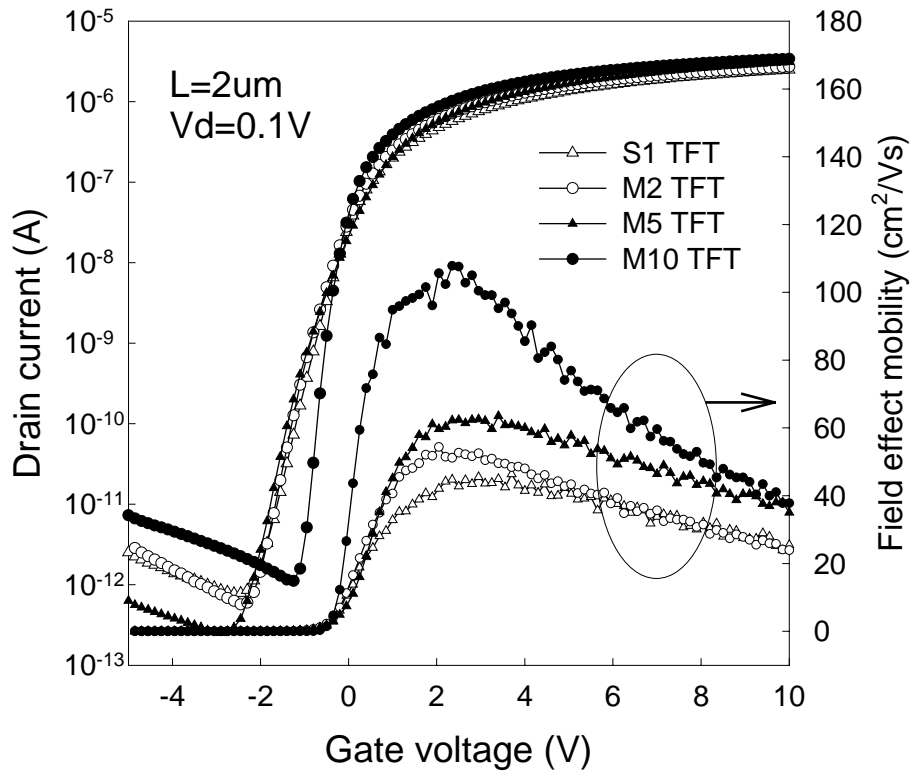


Fig. 5-3. Transfer $I_d - V_g$ curves (left) and field-effect mobility (μ_{FE}) (right) of a series of PDMILC TFT of multi-channel with different widths at the gate length of 2 μm .

Table 5-2. Device parameters average and standard deviation value of M10, M5, M2 and S1 TFTs with gate length (L) of 2 μm . The V_{th} is defined as the gate voltage required to achieve a normalized drain current of $I_d / (W/L) = 10^{-8}$ A at $V_d = 0.1$ V.

Device name	μ_{FE} (cm^2/Vs)	V_{th} (V)	SS (V/dec.)
S1	46.41 ± 0.41	-0.55 ± 0.20	0.73 ± 0.13
M2	53.79 ± 1.16	-0.59 ± 0.41	0.63 ± 0.06
M5	65.69 ± 1.99	-0.37 ± 0.14	0.70 ± 0.15
M10	109.34 ± 1.46	-0.34 ± 0.03	0.23 ± 0.02

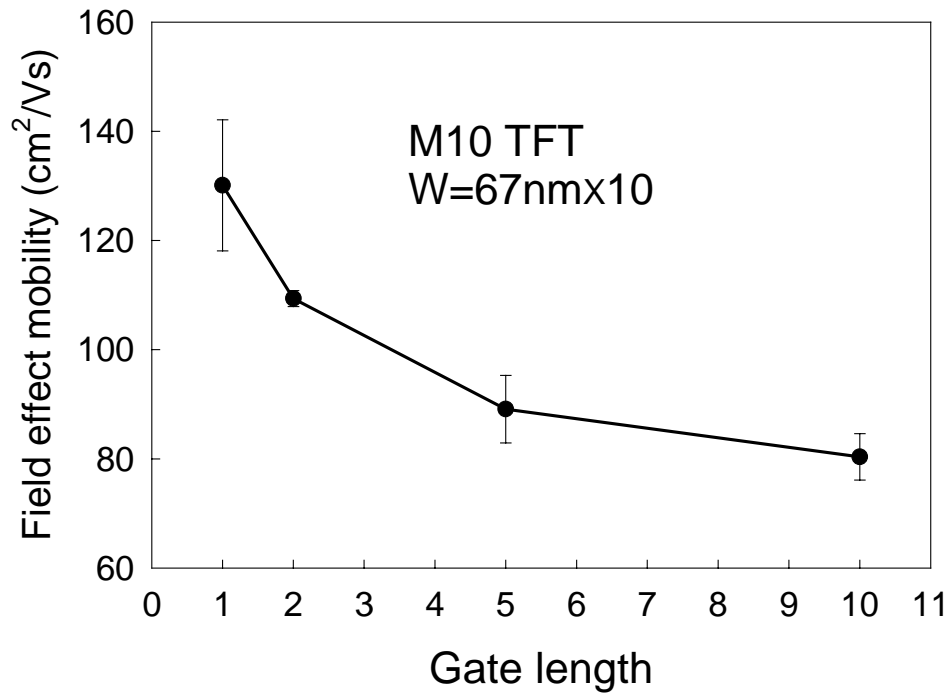


Fig. 5-4. Field-effect mobility (μ_{FE}) average and standard deviation value versus the gate length, for a particular M10 TFT ($W = 67 \text{ nm} \times 10$) structure.

