Chapter 6

Effects of Channel Width and NH_3 Plasma Passivation on Electrical Characteristics of Pattern-dependent Metal-Induced Lateral Crystallization of Polysilicon Thin-Film Transistors

Abstract

This work studies effects of NH_3 plasma passivation on the electrical characteristics of a series of pattern-dependent metal-induced lateral crystallization (PDMILC) polysilicon thin-film transistors (poly-Si TFTs) with various numbers of multiple channels structures. PDMILC TFTs with NH_3 plasma passivation outperforms without such passivation, resulting from the effective hydrogen passivation of the grain-boundary dangling bonds, and the pile-up of nitrogen at the SiO2/poly-Si interface. Additionally, the performance of such devices improves as the number of multi-channels increase. In particular, the electrical characteristics of a nano-scale TFT with ten 67 nm-wide split channels (M10) are superior to those of other TFTs. For example, the former include a higher field effect mobility of 84.63 cm^2/Vs, a higher ON/OFF current ratio (>10^6), a steeper subthreshold slope (*SS*) of 230 mV/decade, an absence of drain-induced barrier lowering (*DIBL*) and favorable

output characteristics. These findings originate from the fact that the active channels of the M10 TFT have exhibit best NH_3 plasma passivation, because it has split nano-wire channels structure.

6.1 Introduction

The major attraction of applying polycrystalline silicon thin-film transistors (poly-Si TFTs) in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility (larger than 10 cm^2/Vs) in poly-Si film and the capability of integrating the pixel switching elements and the capability to integrate panel array and peripheral driving circuit on the same substrate[1-3], bring the era of system-on-panel (SOP) technology. For making high performance poly-Si thin film transistors (TFTs), low-temperature technology is required for the realization of commercial flat-panel displays (FPD) on inexpensive glass substrate, since the maximum process temperature is limited to less than 600 ^{0}C. There three major low-temperature amorphous-Si crystallization methods to achieve high performance poly-Si thin film, solid phase crystallization (SPC)[4], excimer laser crystallization (ELC)[5], and metal-induced lateral crystallization (MILC)[6-10]. MILC technology was initially developed as a low-temperature crystallization technique compared to other low temperature poly-Si technologies such as excimer laser crystallization (ELC) or conventional solid-phase crystallization (SPC), MILC is superior because, unlike ELC,

it is a low-cost batch process and unlike SPC, better quality poly-Si thin film can be obtained. Second, the presence of polysilicon grain boundary defects in the channel region of TFTs drastically affects the electrical characteristics, especially when the device dimension is scaled down. Therefore, reducing the number of polysilicon grain boundary defects will improve the performance of poly-Si TFTs. Poly-Si TFTs with several multi-channels have been reported to effectively reduce grain boundary defects[11,12]. In addition, NH_3 plasma passivation[13] has been reported to reduce the number of trap–states in poly-Si grain boundaries, yielding high-performance poly-Si TFTs. Therefore, in this work, the effects of NH_3 plasma passivation on the electrical characteristics of a series of multi-channels with PDMILC poly-Si TFT structures of various (pattern-dependent) widths are initially investigated.

6.2 Device structure and fabrication

In this work a series of PDMILC TFTs, with a gate length of 5 um, consisting of ten strips of multiple 67 nm wire channels (M10) TFT, five strips of multiple 0.18 um channels (M5) TFT, two strips of 0.5um channels (M2) TFT and a single-channel structure (S1) with W = 1 um TFT, were fabricated, as listed in Table I. Figure 1a shows schematic plot of PDMILC TFT with source, drain, gate, nano-wires channels and MILC seeding window. Figure 1b shows top view of PDMILC TFT with source,

drain, gate, nano-wires channels and MILC seeding window. Figure 1c shows AA' direction cross-section view of PDM-TFT which was a conventional top-gate offset MOSFET structure.

6-inch p-type single crystal silicon wafers were coated with 400 nm-thick SiO_2 as the starting materials. Undoped 50 nm-thick amorphous-Si (a-Si) layer were deposited by low-pressure chemical vapor deposition (LPCVD) at 550 ^{0}C. Then the active islands, including source, drain and ten nano-wire channels were patterned by Electron Beam lithography (EBL) and transferred by reactive ion etching (RIE). After defining the active region, the 25 nm-thick tetra-ethyl-ortho-silicate (TEOS) SiO_2 was deposited by LPCVD as gate insulator. Then, 150 nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100 nm-thick TEOS-SiO_2 layer as passivation layer was deposited by LPCVD. Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Then, a thin 10 nm-thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550 ^{0}C for 48 hrs in an N_2 ambient. The average lateral crystallization length was about 30 um. After long time annealing, the unreacted nickel on passivative TEOS-SiO_2 were removed by H_2SO_4 solution at 120 ^{0}C with 10

min. Phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted through the passivative TEOS-SiO_2 to form the n+ gate, source/drain regions and the self-aligned offset region were formation in the same process step [Fig. 1(c)]. Then, the dopants were activated by rapid thermal annealing (RTA) at 850 ^{0}C with 30 sec. The 300 nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain and gate metal pads. Then, the finished devices were sintered at 400 ^{0}C for 30 minutes in an N_2 ambient. Finally, each device was passivated by NH_3 plasma treatment for 2 hours at 300 ^{0}C.

6.3 Results and discussion

Figure 2a presents a after etching investigation (AEI) scanning electron microscope (SEM) photograph of the poly-Si active region of the M10 TFT, including the source, the drain, ten multiple nano-wire channels and MILC seeding window. Inset plot presents a magnified area of the multiple nano-wire channels in the M10 TFT, each of which is 67-nm-wide. Figure 2b presents SEM photograph of the MILC poly-Si grains in active region of the proposed TFTs. The average grain size in the polysilicon channel formed by MILC is approximately 250 nm. Figures 3(a) to 6(a) show that the PDMILC TFTs that has undergone NH_3 plasma passivation outperforms that without NH3 plasma passivation. The former has a higher field effect mobility (μ_{FE}), a higher *ON/OFF* ratio, a lower threshold voltage (V_{th}), a lower subthreshold

slope (*SS*) and lower drain-induced barrier lowering (*DIBL*). Figures 3(b) to 6(b) show that the PDMILC TFT that had undergone NH_3 plasma passivation has a higher output current than that without NH_3 plasma passivation. In particular, the M10 PDMILC TFT has the highest output current, because it has the highest μ_{FE}. Table II lists all the parameter of the PDMILC poly-Si TFTs, including μ_{FE}, the *ON/OFF* ratio, the V_{th}, the *SS*, and the grain boundary defects density (N_t). The μ_{FE} is extracted from the linear region (V_d = 0.1 V) of transcendence (g_m). The V_{th} is defined as the gate voltage required to yield normalized drain current of I_d / (W/L) = 10^{-7} A at V_d = 5 V. The I_{ON} is defined as the maximum drain turn-on current at V_d = 5 V. The I_{OFF} is defined as the minimum drain turn-off current at V_d = 5 V. Thus, the ON/OFF ratio is defined as I_{ON} / I_{OFF}. The device parameters versus multi-channel with different widths are plotted to elucidate the effect of NH_3 plasma passivation on each of the dimensions of PDMILC TFTs. Figure 7 plots the PDMILC TFTs' μ_{FE} versus the multi-channel with different widths, with and without NH_3 plasma passivation. This curve reveals that NH_3 plasma passivation improves the μ_{FE} of a PDMILC TFT, suggesting that the NH_3 plasma effectively hydrogen-passivated the dangling bonds at the grain-boundary and the pile-up of nitrogen at the SiO2/poly-Si interface. The M10 PDMILC TFT has the highest μ_{FE} of 84.63 cm^2/Vs, because it has a split nano-wire structure, which is exposed effectively to an atmosphere of NH3 plasma. Figure 8

plots the PDMILC TFTs' *ON/OFF* ratio against the multi-channel with different widths, with and without NH_3 plasma passivation. This curve reveals that the *ON/OFF* ratio of all PDMILC TFTs after NH_3 plasma passivation, except S1 TFT, is increased. NH3 plasma is effectively passivated on poly-Si grain boundaries reducing leakage current, which is generated by the thermionic field emission of grain boundary defects in the off-state. Because hydrogen passivated the grain boundary defect states, and the strong Si-N bond formatted to terminate the dangling bonds at the grain boundaries of the poly-Si films. Figure 9 plots the PDMILC TFTs' V_{th} versus the multi-channel with different widths. After NH_3 plasma passivation, the V_{th} of each TFT device was approximately 4 V lower. NH_3 plasma passivation reduced the barrier height (E_B) of the poly-Si grain boundary, so the electrons can easily overcome E_B, producing a high current and allowing the TFT to be easily turned on. Such a low value of V_{th} of the PDMILC TFTs is appropriate in low-power AMLCD applications. Figure 10 plots the PDMILC TFTs' subthreshold swing (*SS*) versus the multi-channel with different widths, with and without NH_3 plasma passivation. NH_3 plasma passivation reduces the *SS*, because the pile-up of nitrogen at the SiO2/poly-Si interface is of major importance, while the hydrogen-passivation of the dangling bonds at the grain-boundary is of minor importance. Moreover, *SS* decreases gradually from S1, M2 and M5 to M10 TFT, and M10 TFT has the smallest *SS* of 230

mV/decade. A steep *SS* of M10 PDMILC TFT is desired to facilitate the switching off of the transistor, because M10 exhibits the greatest NH_3 plasma passivation because it has ten split nano-wires, most of which are exposed to the NH_3 plasma passivation. The amount of effects of NH_3 plasma passivation on PDMILC TFTs poly-Si grain boundaries can be evaluated from the by grain boundary defects density (N_t)[14]. Figure 11 plots extraction curves of N_t of M10 PDMILC TFTs, with and without NH_3 plasma passivation. Figure 12 plots PDMILC TFTs' N_t versus the multi-channel with different widths, with and without NH_3 plasma passivation. The N_t decreases gradually from S1, M2 and M5 to the M10 PDMILC TFT with the TFTs' channel numbers increasing. Moreover, after NH_3 plasma passivation substantially reduces N_t, providing high electrical performance. In addition, the M10 TFT has the lowest N_t (3.07×10^{12} cm^{-2}), which value is consistent with its best performance.

6.4 Conclusion

Experimental results indicate that the performance of devices improves as the number of channels increases from the S1, M2 and M5 to the M10 PDMILC TFT, with the increase in the strength of the effect of the NH3 plasma passivation. The defect density (N_t) in the grain boundary reveals a strong consistency between theory and experimental results. Additionally, NH_3 plasma passivation more strongly influences M10 TFT than it does other TFTs. Because the M10 TFT has a split

nano-wire structure, most of which undergoes NH_3 plasma passivation, further reducing the number of defects at grain boundaries. These high performance NH_3 plasma passivation PDMILC TFTs are compatible with complementary metal oxide semiconductor (CMOS) technology, thus highly suitable for use in future SOP applications.

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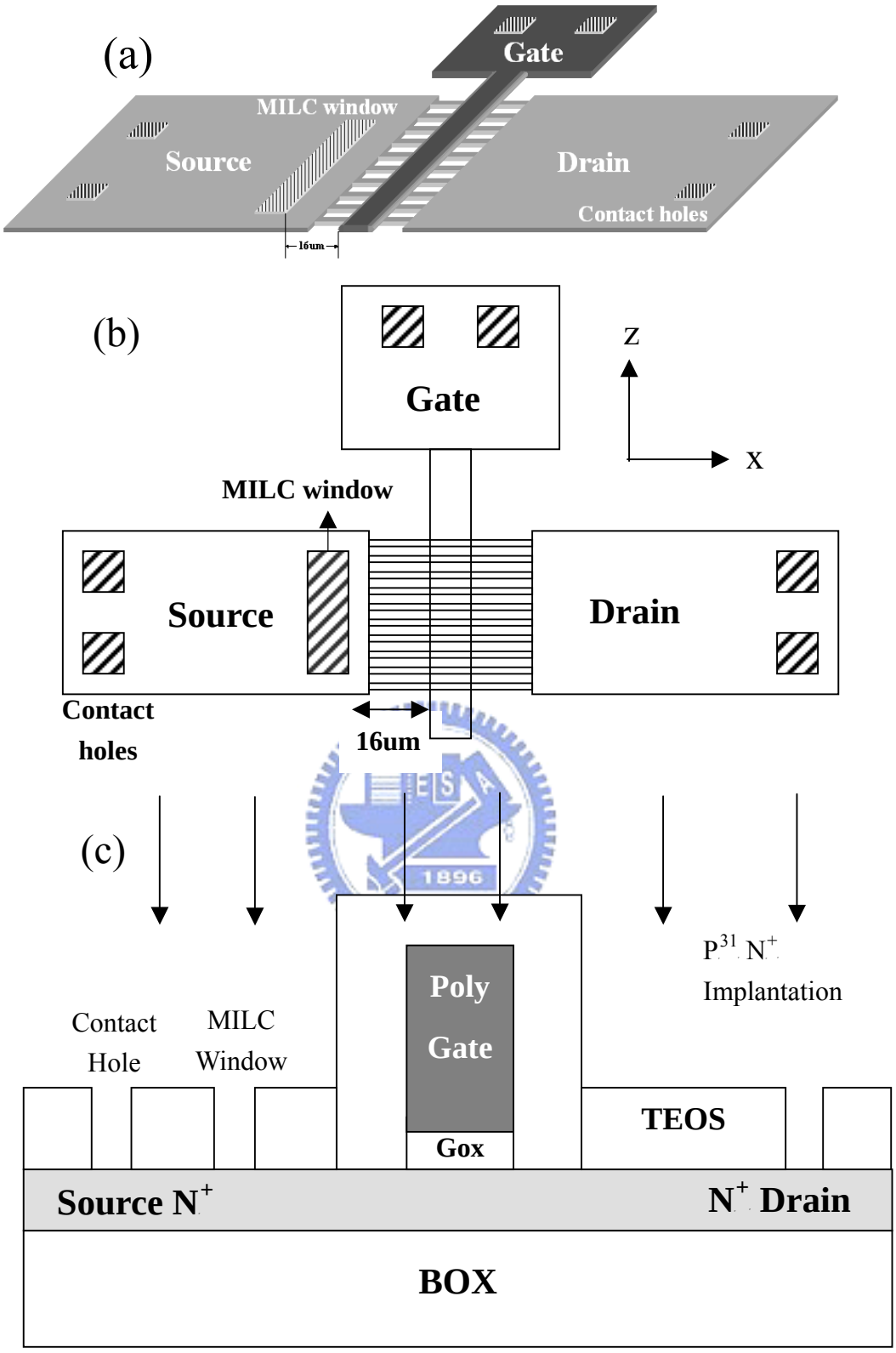
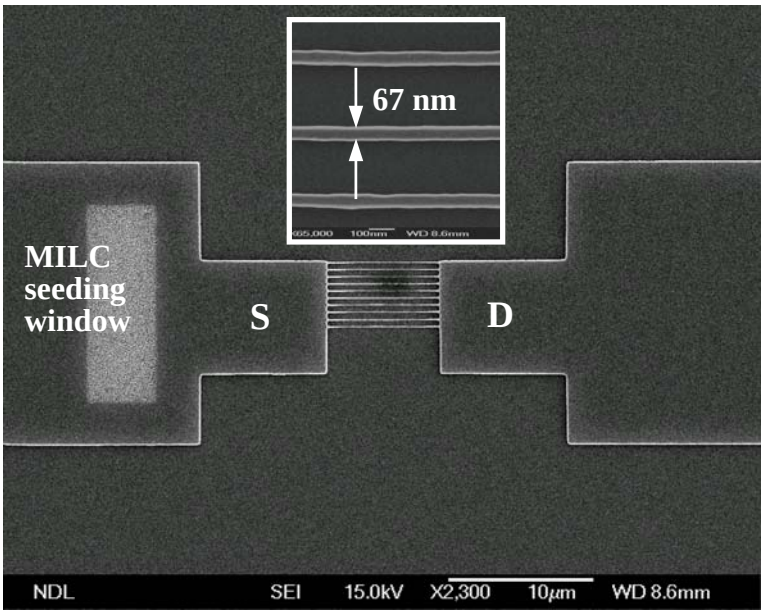


Fig. 6-1. (a) Schematic plot of PDMILC poly-Si TFT with source, drain, gate, ten nano-wires channels, contact holes and MILC seeding window. (b) Top-view of PDMILC poly-Si TFT. The key process flows are active region pattering, gate patterning, MILC seeding window and contact holes patterning, and all metal pads pattering. (c) Cross-section view of PDMILC poly-Si TFT, which was a conventional MOSEFET with offset structure.

Table 6-1. Devices dimension of S1, M2, M5 and M10 PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 25 nm.

Device name	Gate length (L)	Channel number	Each channel width (W)	Effective channel width (W_{eff})
S1	5 um	1	1 um	1 um
M2	5 um	2	0.5 um	1 um
M5	5 um	5	0.18 um	0.9 um
M10	5 um	10	67 nm	0.67 um

(a)



(b)

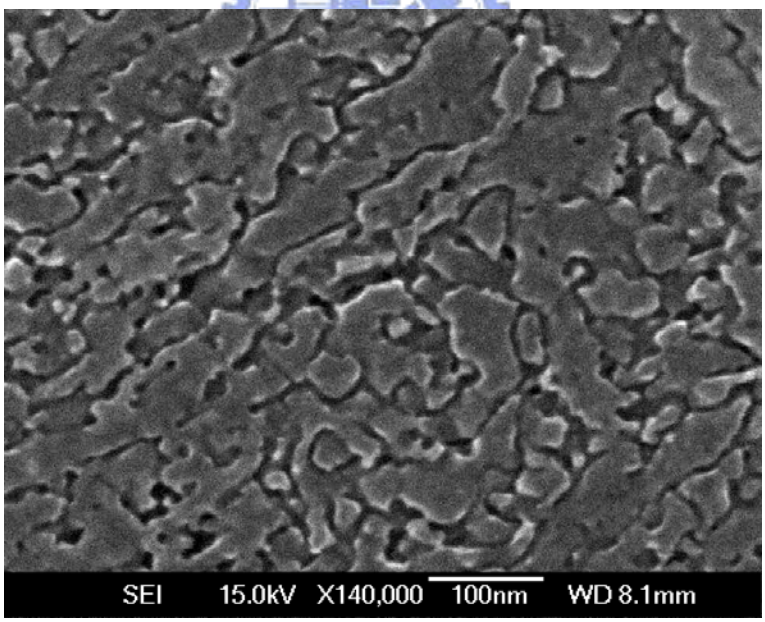


Fig. 6-2. (a) Scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nano-wire channels and MILC seeding window. The inset plot shows the each nano-wire width of 67 nm. (b) SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm.

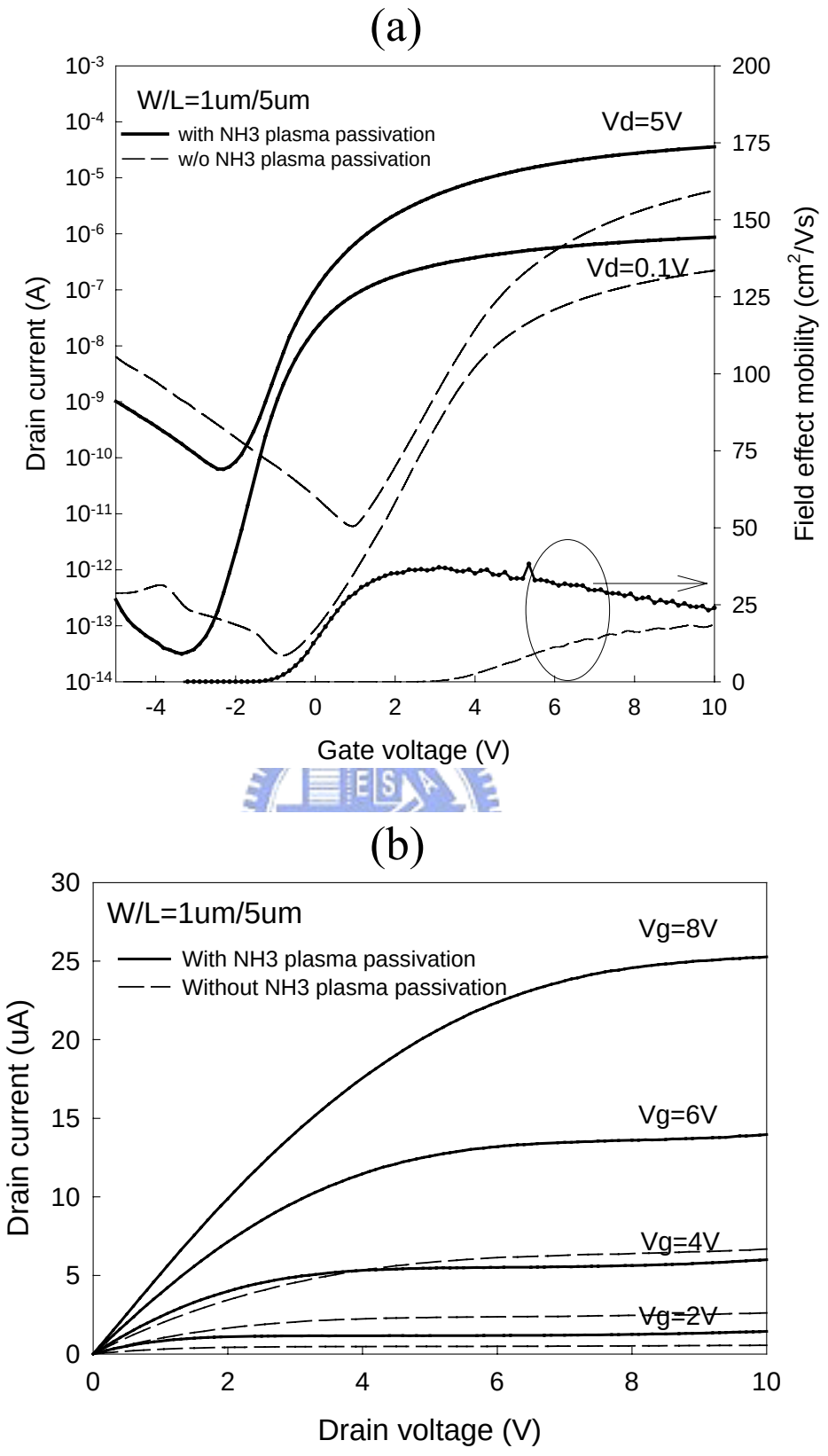


Fig. 6-3. Device characteristics of S1 (W / L = 1 um / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

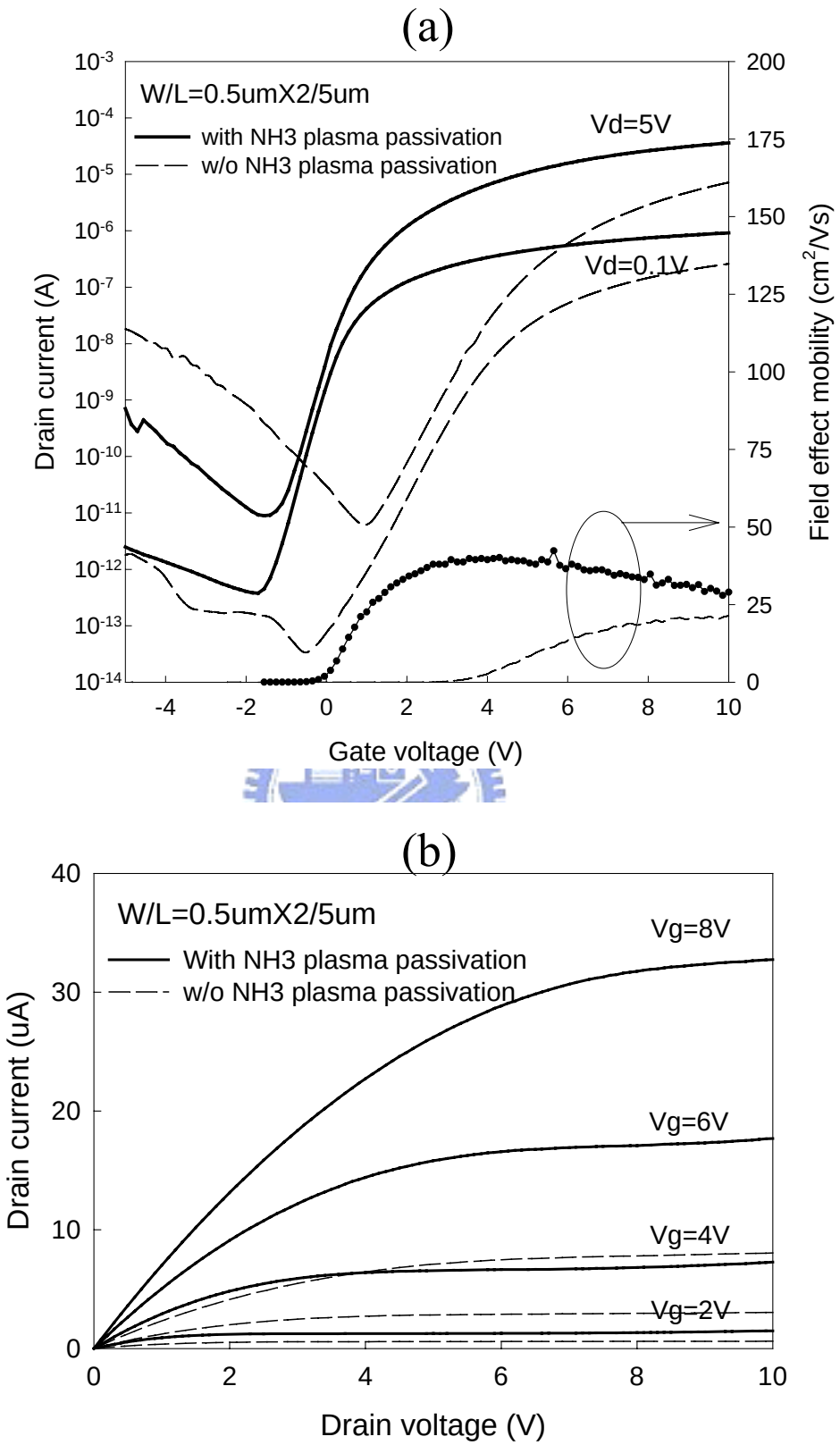


Fig. 6-4. Device characteristics of M2 (W / L = 0.5 um × 2 / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH3 plasma passivation.

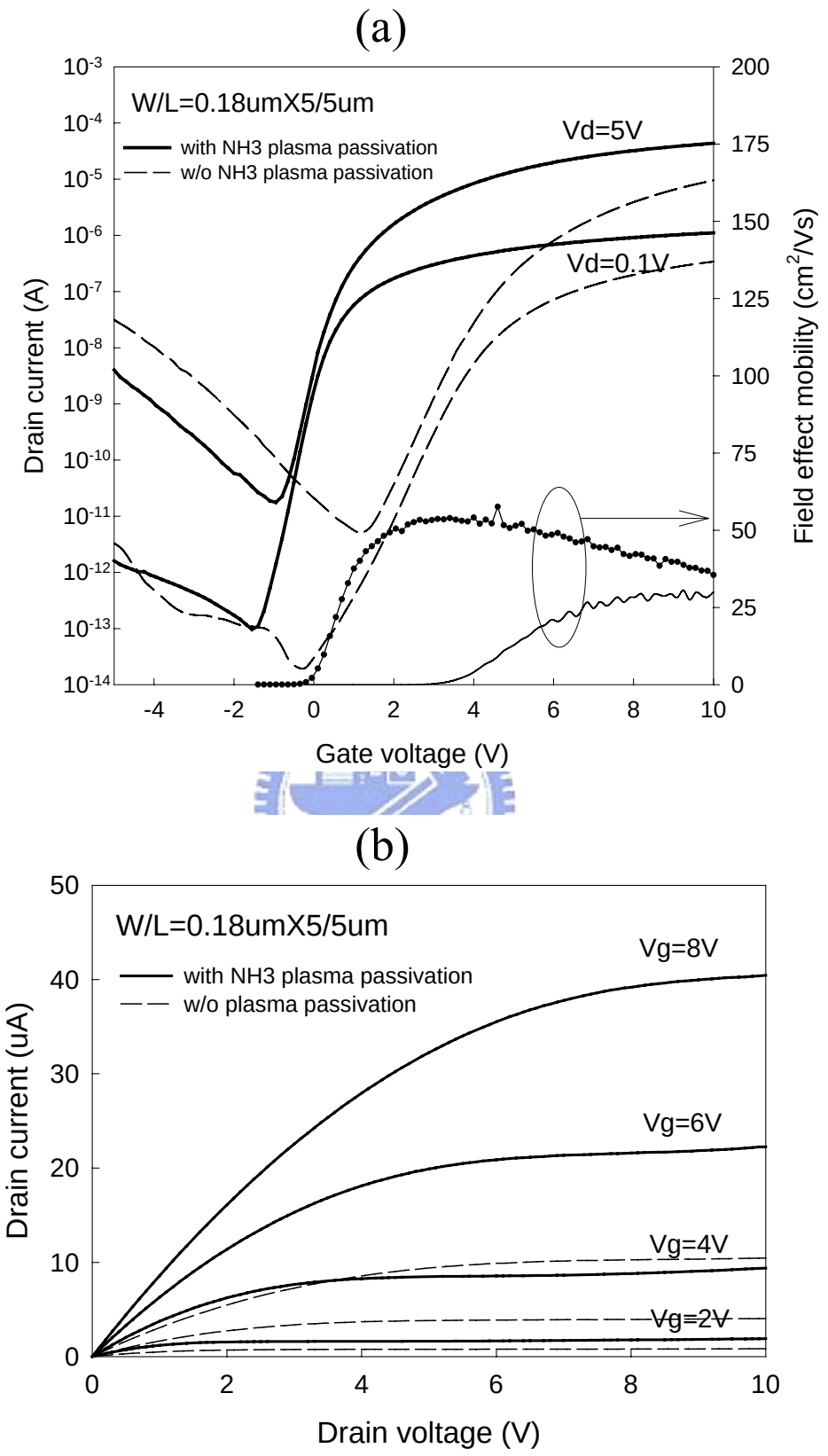


Fig. 6-5. Device characteristics of M5 (W / L = 0.18 um × 5 / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

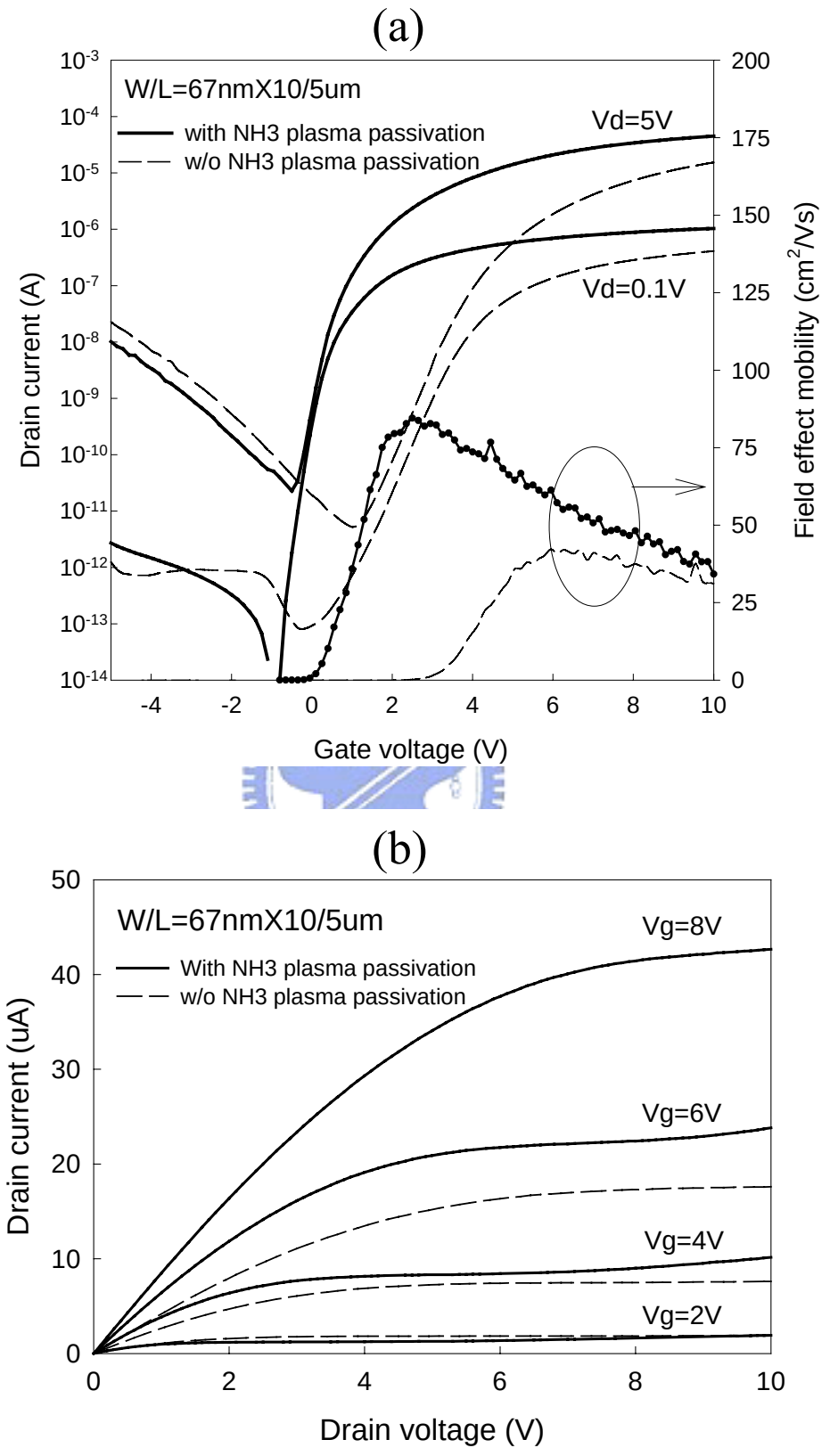


Fig. 6-6. Device characteristics of M10 (W / L = 67 nm × 10 / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

Table 6-2. Device parameters of PDMILC TFTs with the same L = 5 um at different widths. All parameters were extracted at V_d = 5 V, except for the field-effect mobility (μ_{FE}) which were extracted at V_d = 0.1 V.

Device name	NH3-plasma passivation	μ_{FE} (cm^2/VS)	V_{th} (V)	SS (V/dec.)	I_{ON}/I_{OFF} x10^6	N_t x10^{12} (cm^{-2})
S1	w/o	18.11	4.79	0.80	2.93	10.60
	with	38.25	0.31	0.48	1.87	3.66
M2	w/o	21.39	4.70	0.78	1.15	9.87
	with	42.37	0.27	0.40	4.02	3.81
M5	w/o	30.62	4.56	0.67	1.87	8.87
	with	57.54	0.24	0.32	2.46	3.51
M10	w/o	42.29	4.05	0.59	2.93	7.92
	with	84.63	0.06	0.23	4.61	3.07

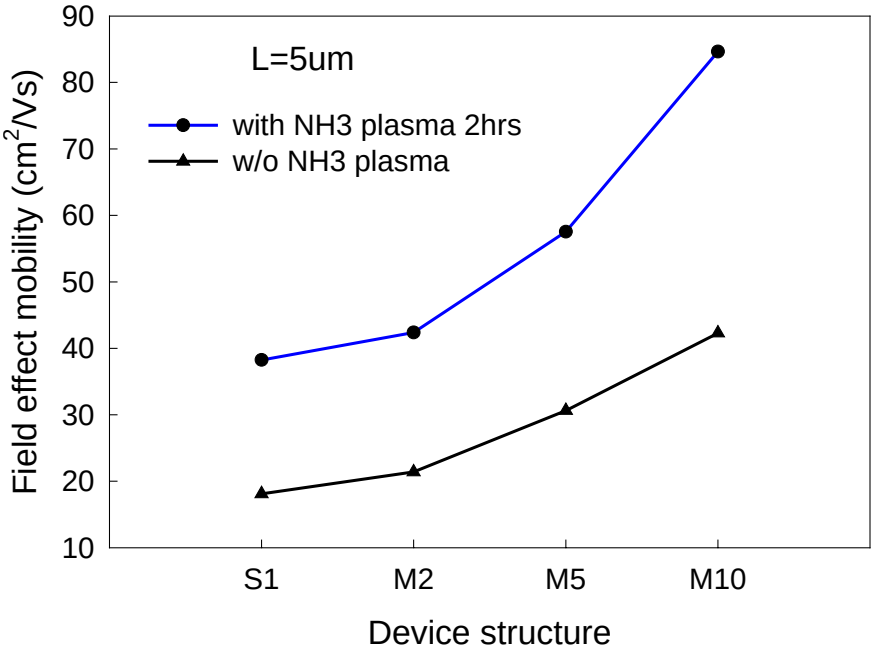


Fig. 6-7. PDMILC poly-Si TFTs' μ_{FE} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

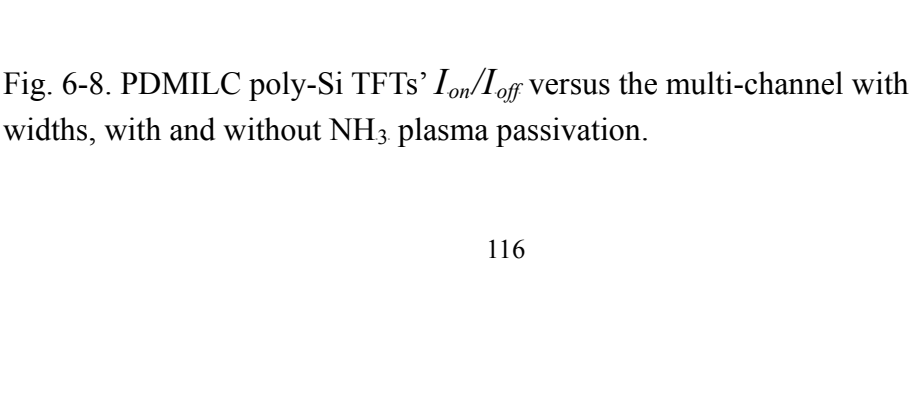


Fig. 6-8. PDMILC poly-Si TFTs' I_{on}/I_{off} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

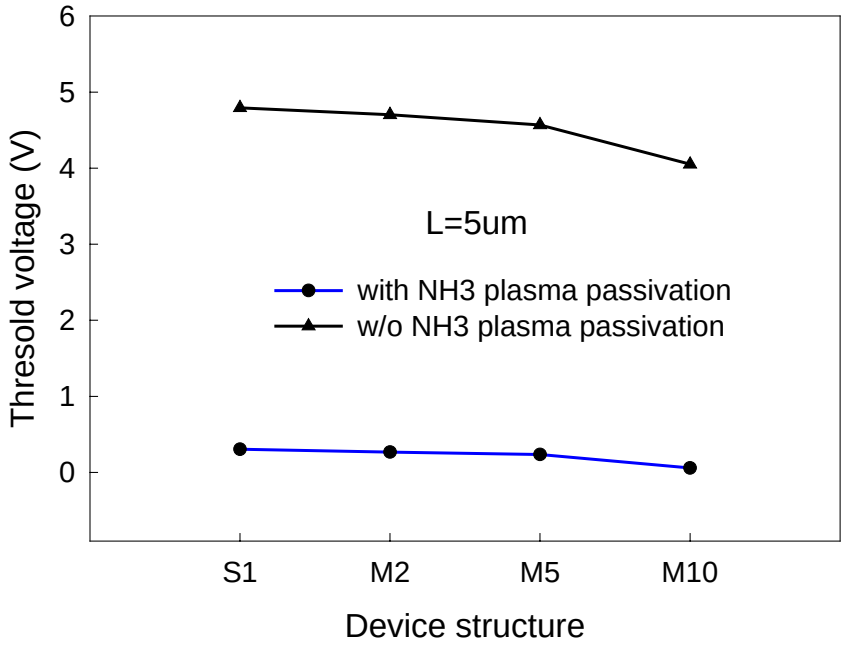


Fig. 6-9. PDMILC poly-Si TFTs' V_{th} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

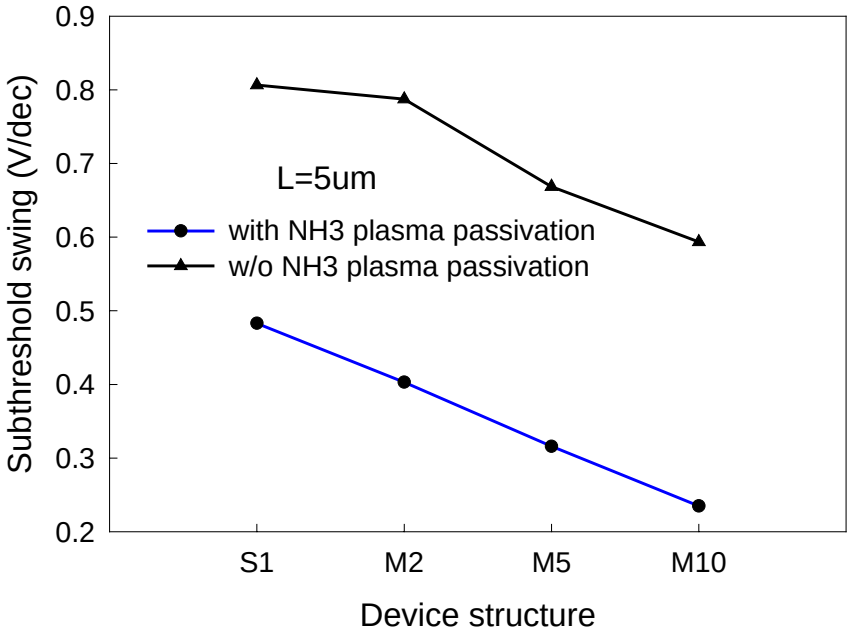


Fig. 6-10. PDMILC poly-Si TFTs' *SS* versus the multi-channel with different widths, with and without NH_3 plasma passivation.

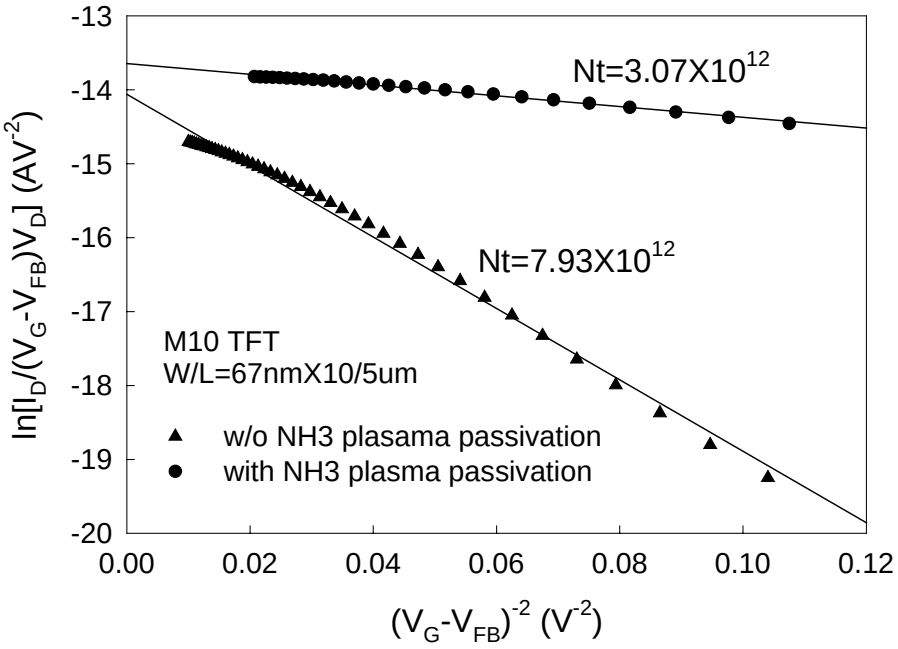


Fig. 6-11. Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

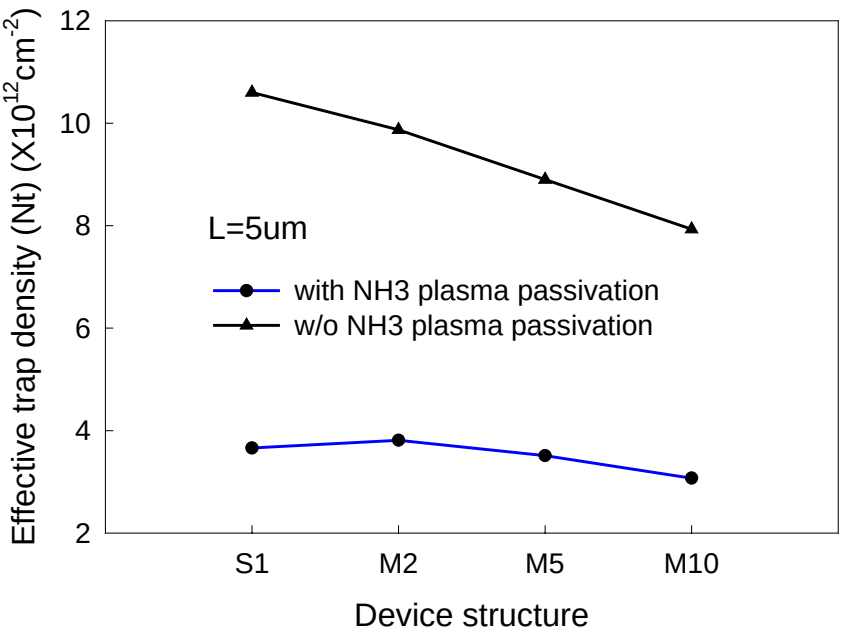


Fig. 6-12. PDMILC poly-Si TFTs' N_t versus the multi-channel with different widths, with and without NH_3 plasma passivation.