

Chapter 7

High performance Metal-induced Lateral Crystallization Polysilicon Thin-Film Transistors with Multiple Nanowire Channels and Multiple Gates

Abstract

In this work, pattern-dependent nickel (Ni) metal-induced lateral crystallization (Ni-MILC) polysilicon thin-film transistors (poly-Si TFTs) with ten nanowire channels and multi-gate, were fabricated and characterized. Experimental results reveal that applying ten nanowire channels improves the performance of Ni-MILC poly-Si TFT, which thus has a higher ON current, a lower leakage current and a lower threshold voltage (V_{th}) than single-channel TFTs. Furthermore, the experimental results reveal that combining the multi-gate structure and ten nanowire channels further enhances the entire performance of Ni-MILC TFTs, which thus have a low leakage current, a high ON/OFF ratio, a low V_{th} , a steep subthreshold swing (SS) and kink-free output characteristics. The multi-gate with ten nanowire channels NI-MILC TFTs has few poly-Si grain boundary defects, a low lateral electrical field and a gate channel shortening effect, all of which are associated with such high-performance characteristics.

7.1 Introduction

High-performance thin-film transistors (TFTs) fabricated on a polysilicon film formed by metal-induced lateral crystallization (MILC) using Ni have attracted much interest because of their potential use in three-dimensional circuit technology [1], liquid-crystal display (LCD) drivers and system-on-panel (SOP) applications [2]. It is a low-cost batch process that yields superior poly-Si films. However, the applications of Ni-MILC poly-Si TFTs remain limited, because the grain boundaries of poly-Si in the channel region substantially degrade performance. The electrical characteristics of the TFTs can be improved by reducing the number of defects in the poly-Si grain boundaries in the channel, and poly-Si TFTs with several multi-channels have been reported to effectively reduce grain boundary defects [3], [4]. The Ni-MILC poly-Si TFT suffers from severe leakage current because of Ni contamination during MILC annealing [2], [5], [6], which is directly related to the lateral electrical field in the drain depletion region in the off-state. This is another major limitation on Ni-MILC poly-Si TFT applications. According to previous report, the poly-Si TFTs adopted multi-gate can effectively reduce leakage current, addressing this leakage issue [7].

This work develops a single-gate with a single-channel, a single-gate with ten nanowire channels, and three different multi-gate numbers with ten nanowire channels in the Ni-MILC poly-Si TFT to study their performance. The device simulation results

are also performed to investigate the relation between the electrical field and leakage current of multi-gate structure TFTs.

7.2 Device structure, simulation, and fabrication

In this work, a series of Ni-MILC poly-Si TFTs, one with a single-gate length of 5 μm and a single-channel width of 1 μm (G1S1), one with a single-gate length of 5 μm and ten strips of 84 nm wire channels (G1M10), one with two-gate, each gate with a length of 2.5 μm and ten strips of 84 nm wire channels (G2M10), one with three-gate, each gate with a length of 1.7 μm and ten strips of 84 nm wire channels (G3M10), one with four-gate, each gate with a length of 1.25 μm and ten strips of 84 nm wire channels (G4M10) were fabricated, as listed in Table I. Figure 1a presents the schematic plot of G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, an Ni-MILC seeding window and a dual-gate. Figure 1b presents the top-view of G2M10 Ni-MILC poly-Si TFT. Figure 1c presents the cross-sectional view of Ni-MILC poly-Si TFT, with a conventional top dual-gate, self-aligned offset MOSFET structure with critical device dimensions. As the anomalous off-current (leakage current) in the poly-Si TFTs is related to the lateral electrical field in the channel. Figure 2a presents the simulation results obtained using an ISE TCAD 2-D device simulator of the lateral electrical field of the single-gate (G1) and dual-gate (G2) TFTs with the same device dimension and bias condition. The peak lateral

electrical field (E_m) of the dual-gate TFT is lower than that of the single-gate TFT, indicating that the dual-gate (G2) structure effectively reduces the leakage current of poly-Si TFTs. Figure 2b presents E_m versus different gate number TFT structure. The E_m is decreasing with the gate number increasing.

The 6-inch p-type single crystal silicon wafers were coated 400 nm-thick SiO_2 as the starting materials. Undoped 50 nm-thick amorphous-Si (a-Si) layer were deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then the active islands, including source, drain and ten nanowire channels were patterned by Electron Beam lithography (EBL) and transferred by reactive ion etching (RIE). After defining the active region, the 50 nm-thick tetra-ethyl-ortho-silicate oxide (TEOS- SiO_2) was deposited by LPCVD as gate insulator. Then, 150 nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100 nm-thick TEOS- SiO_2 layer as passivation layer was deposited by LPCVD. The poly-Si gate sidewall TEOS- SiO_2 was formed self-aligned offset spacer with the width of 0.1 μm , as shown in Fig. 1b. Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Then, a thin 10 nm-thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550 °C for 48 hrs in an N_2

ambient. After annealing, the unreacted nickel on passivative TEOS-SiO₂ were removed by H₂SO₄ solution at 120 °C with 10 min. Phosphorus ions at a dose of 5×10^{15} cm⁻² were implanted through the passivative TEOS-SiO₂ to form the n+ gate, source/drain regions and the self-aligned offset region were formation in the same process step, as shown in Fig. 1b. Then, the dopants were activated by rapid thermal annealing (RTA) at 850 °C with 30 sec. The 300 nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain and gate metal pads. In this study, no other H or NH₃ plasma passivation was performed. This allowed the intrinsic behavior of the devices to be compared and studied.

7.3 Results and discussion

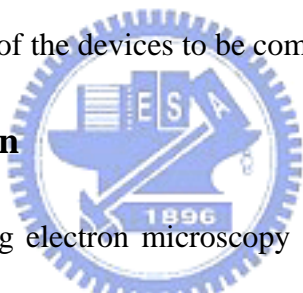


Figure 3a shows scanning electron microscopy (SEM) photography of G2M10 Ni-MILC TFT active pattern with the source, the drain, ten nanowire channels and dual-gate. The each dual-gate length is 2.5 μm. Figure 3b shows SEM photography of magnified area of multiple nanowire channels. The each nanowire width is 84 nm. Figure 3c shows SEM photography of Ni-MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm. The inset optical microscopy photography depicts a MILC length of 30 μm, which is longer than 16 μm (Fig. 1a) to promise the whole active channel was crystallized by MILC process.

Figure 4a compares typical transfer curves of all proposed Ni-MILC poly-Si

TFTs. Firstly, comparing the single-gate, the single-channel (G1S1) and the ten nanowire channels (G1M10) TFTs reveals that the G1M10 has a higher ON current, a lower leakage current, and a lower threshold voltage than the G1S1 TFT. These data indicate that the multiple nanowire channels have fewer defects at the grain boundaries. Because the G1M10 TFT, during the MILC process, its nanowire width of 84 nm strongly limited the growth of poly-Si grains in the z-direction (Fig. 1a) than single-channel G1S1 TFT. Therefore, the poly-Si grains tended to grow laterally in the x-direction, becoming large to reduce the grain boundary defects. In our previous report [8], the poly-Si grain enhancement effect was significant as the channel width less than poly-Si grain size. However, both G1S1 and G1M10 exhibit severe leakage current and large subthreshold swing. Secondly, comparing the single-gate (G1M10) and multi-gate (G2M10, G3M10, and G4M10) with the same ten nanowire channels Ni-MILC poly-Si TFTs reveal that the electrical performance is significantly improved as the multi-gate number increasing. Figure 4b presents the transfer curve of G4M10 TFT with linear and saturation regions. The inset SEM photograph shows the G4M10 TFT active region. The G4M10 outperforms the other TFTs, having a low leakage current, a high *ON/OFF* ratio ($>10^7$), a low V_{th} , a steep *SS*, and near-free drain-induced barrier lowering (*DIBL*).

Figure 5 compares the output curves of all proposed Ni-MILC poly-Si TFTs with

the same gate length of 5 μm . The kink-effect associated with multi-gate (G2M10, G3M10 and G4M10) is suppressed relative to those of the other TFTs (G1S1 and G1M10). Accordingly, the multi-gate structure effectively reduces the lateral electrical field (Fig. 2b), reducing the impaction ionization in the active channel of the Ni-MILC poly-Si TFTs.

Figure 6 presents the leakage current and ON/OFF ratio versus different structure of the Ni-MILC TFTs. The leakage current is defined as the drain current at $V_d = 5\text{ V}$ and $V_g = -7\text{ V}$, and the ON/OFF ratio is defined as the maximum drain current value of I_{ON} / I_{OFF} at $V_d = 5\text{ V}$. For single-gate TFT, nanowire channels (G1M10) can be applied to yield a low leakage current by reducing the number of defects at the poly-Si grain boundaries below the number in a single-channel TFT (G1S1). Additionally, comparing single-gate (G1M10) and multi-gate (G2M10, G3M10, and G4M10) TFTs with the same ten nanowire channels Ni-MILC poly-Si TFTs reveal that the leakage current decreases and the ON/OFF ratio increases as with the number of multi-gate increasing. The G4M10 has the lowest leakage current of $5.12 \times 10^{-12}\text{ A}$ and the highest ON/OFF ratio of 1.81×10^7 . These findings reveal that the multi-gate structure can reduce the peak lateral electrical field in the drain depletion region. Therefore, the leakage current that arises from the field emission of carriers through the poly-Si grain traps, and the number of defects associated with Ni contamination

was reduced. This finding is consistent with the simulated value of the lateral electrical field of multi-gate TFTs in Fig. 2b.

Figure 7 plots the V_{th} and SS versus the structure of the TFTs. V_{th} is defined as the gate voltage to yield a normalized drain current, $I_d/(W/L)$ equal to 10^{-7} A at $V_d = 5$ V. Comparing G1S1 and G1M0 TFT reveals that the ten nanowire channels structure has a lower V_{th} , indicating that the ten nanowire channels structure has fewer defects at the poly-Si grain boundaries than the single-channel structure. Moreover, the multi-gate structure is associated with an even lower V_{th} , and the G4M10 has the lowest V_{th} of -0.41 V. The results reveal that the multi-gate structure exhibits channel length-shortening effect for easy turning on the TFT. The effective channel length (L_{eff}) decreases as the number of multi-gate increases ($L_{eff} = L_{tot} - 2n \times \Delta L$, where n is the number of multi-gate and ΔL is the overlap of the source/drain dopant region and the gate). The SS specifies the capacity of transistor to switch. These results reveal that the SS declines as the number of multi-gate increases, and the G4M10 has the lowest SS of 0.44 V/dec. For the same channel length-shortening effect is responsible for the lowering of the SS .

Figure 8 plots a series of G1M10 TFT transfer curves after various hot-carrier stress conditions with 1000 second. Until the extreme hot-carrier stress conditions of $V_d = 45$ V and $V_g = 22.5$ V are reached; only the transfer curve of G1M10 TFT shows

degradation. The results indicate that the ten nanowire channels structure of the Ni-MILC TFT supports excellent hot-carrier immunity and potential use in high-voltage applications. The similar hot-carrier stress results are also found in others multi-gate with ten nanowire channels Ni-MILC TFT. Figure 9 plots the maximum transconductance (G_m) degradation with dc hot-carrier time of all ten nanowire TFTs. These results reveal that the all Ni-MILC TFTs with ten nanowire structure have similar G_m degradation. However, the G4M10 still has lighter G_m degradation than others TFTs due to its lowest lateral electrical field. Figure 10 plots the *ON/OFF* ratio degradation with dc hot-carrier time of all ten nanowire TFTs. These results reveal that the degradation of *ON/OFF* ratio improves with the gate number increasing. Again, the multi-gate structure can reduce the peak lateral electrical field, which is responsible to this degradation of *ON/OFF* ratio improvement. In brief, combining the multi-gate structure and ten nanowire channels can effectively enhance the entire performance of Ni-MILC TFTs. Obviously, the device performance can be further improved by declining the gate length before the short-channel effect occurrence. However, according to this study, the multi-gate number is properly within 2 to 4. Because the more gate number increase, the more additional parasitic resistance will be generated between the each gate. The additional parasitic resistance will reduce the device performance.

7.4 Conclusion

Experiment results show that applying ten nanowire channels enhances the Ni-MILC poly-Si TFT performance. Moreover, using the multi-gate structure can further enhance the TFT performance, including a lower leakage current, a higher ON/OFF ratio, a lower V_{th} , and a lower SS than single-gate TFT. In output characteristics, the multi-gate with ten nanowire TFT can reduce the kink-effect. This novel multi-channel and dual-gate Ni-MILC poly-Si TFTs is quite easy and involves no additional processes, thus highly suitable for high-performance MILC poly-Si TFT applications.



References:

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Table I. Devices dimension of all proposed Ni-PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 50 nm.

Device name	Gate number	Each gate length (L)	Total length (L_{tot})	Channel number	Each width (W)	Total width (W_{tot})
G1S1	1	5 μ m	5 μ m	1	1 μ m	1 μ m
G1M10	1	5 μ m	5 μ m	10	84 nm	0.84 μ m
G2M10	2	2.5 μ m	5 μ m	10	84 nm	0.84 μ m
G3M10	3	1.7 μ m	5 μ m	10	84 nm	0.84 μ m
G2M10	4	1.25 μ m	5 μ m	10	84 nm	0.84 μ m



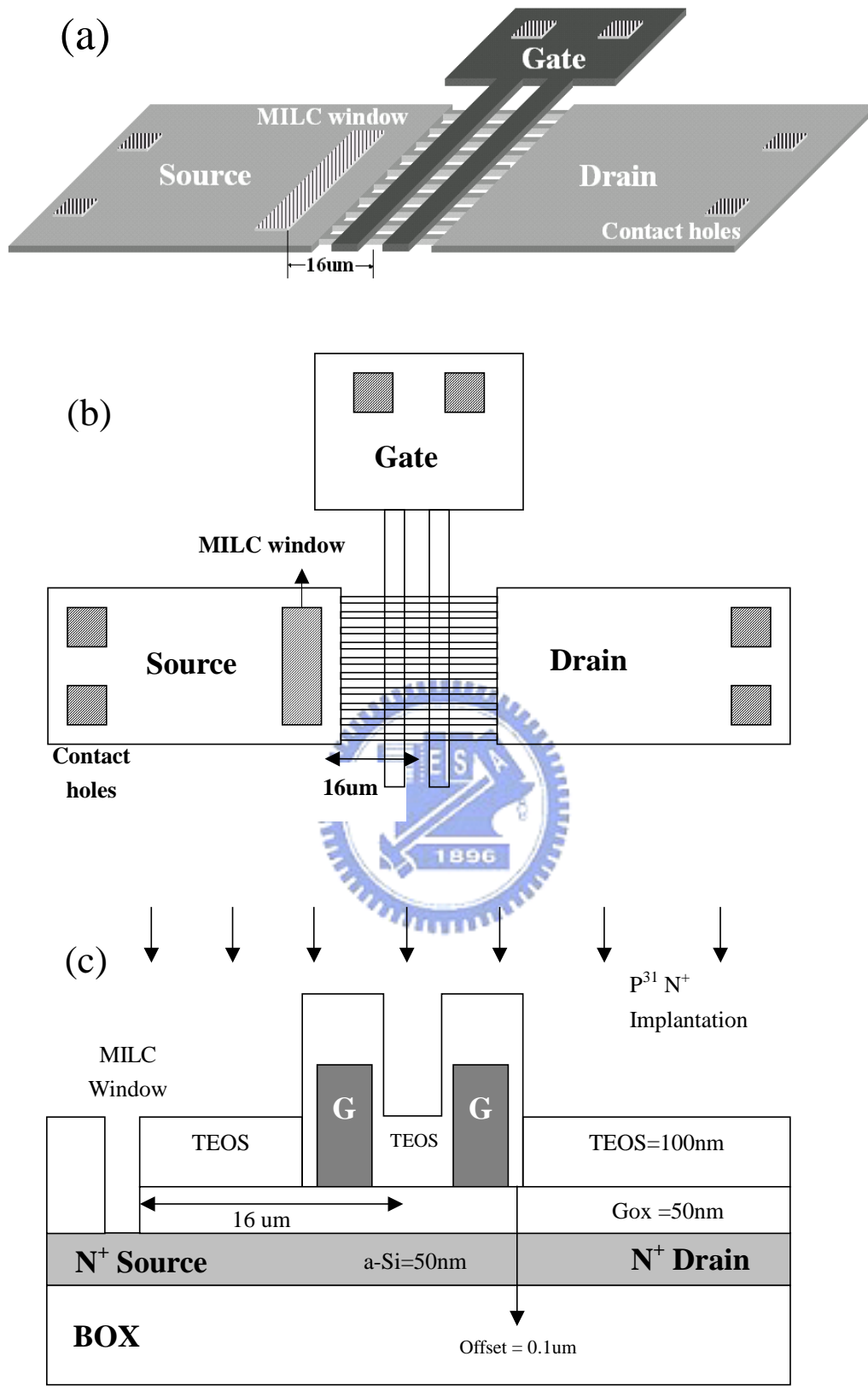


Fig. 7-1. (a) The schematic plot of G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, an Ni-MILC seeding window and the dual-gate. (b) Top-view plot of G2M10 Ni-MILC poly-Si TFT. (c) Cross-section view of Ni-MILC poly-Si TFT, which was a conventional top-gate, self-aligned offset MOSFET structure.

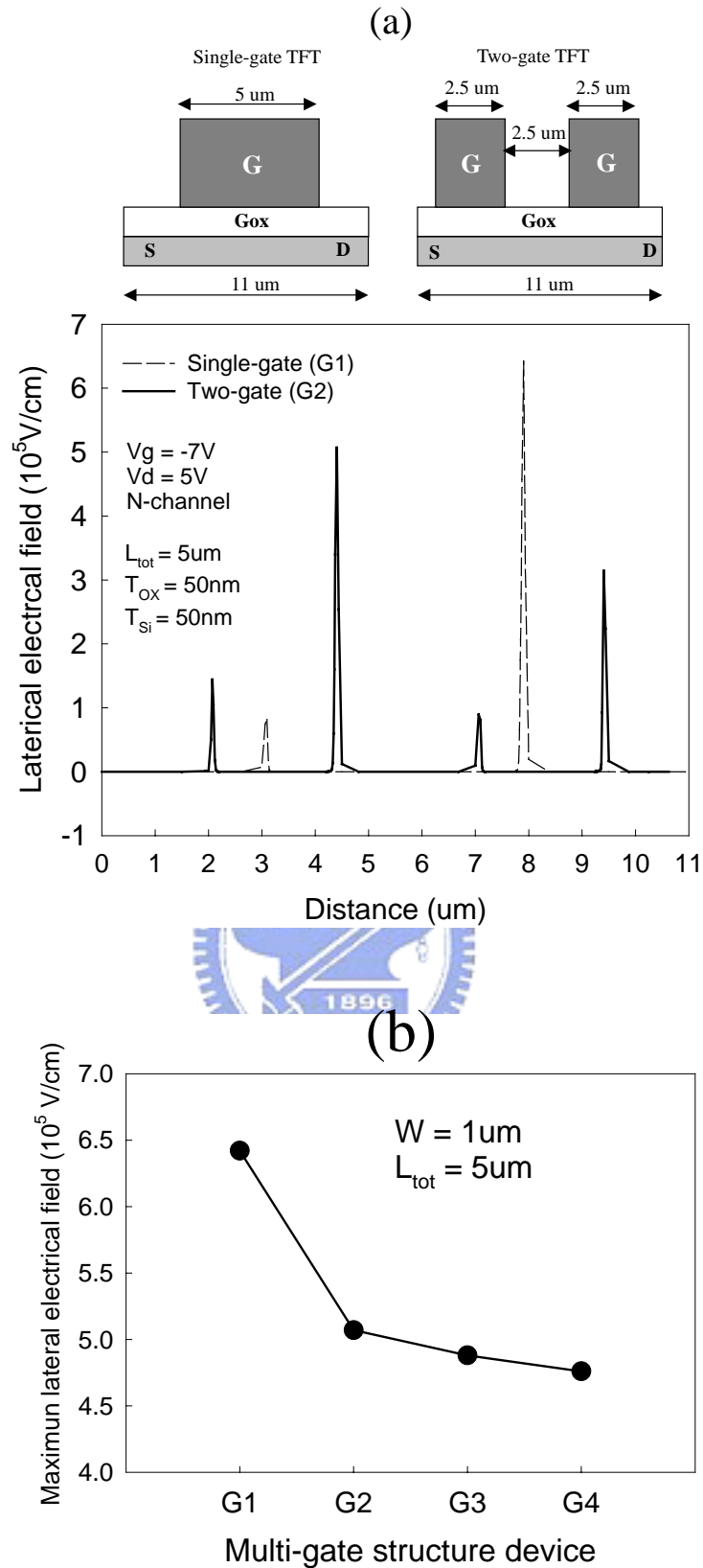


Fig. 7-2. (a) Off-state electrical field simulation results of single-gate and dual-gate poly-Si TFT by ISE TCAD v. 7 (a 2-D device simulator). (b) The peak lateral electrical field (E_m) versus different gate number TFT structure.

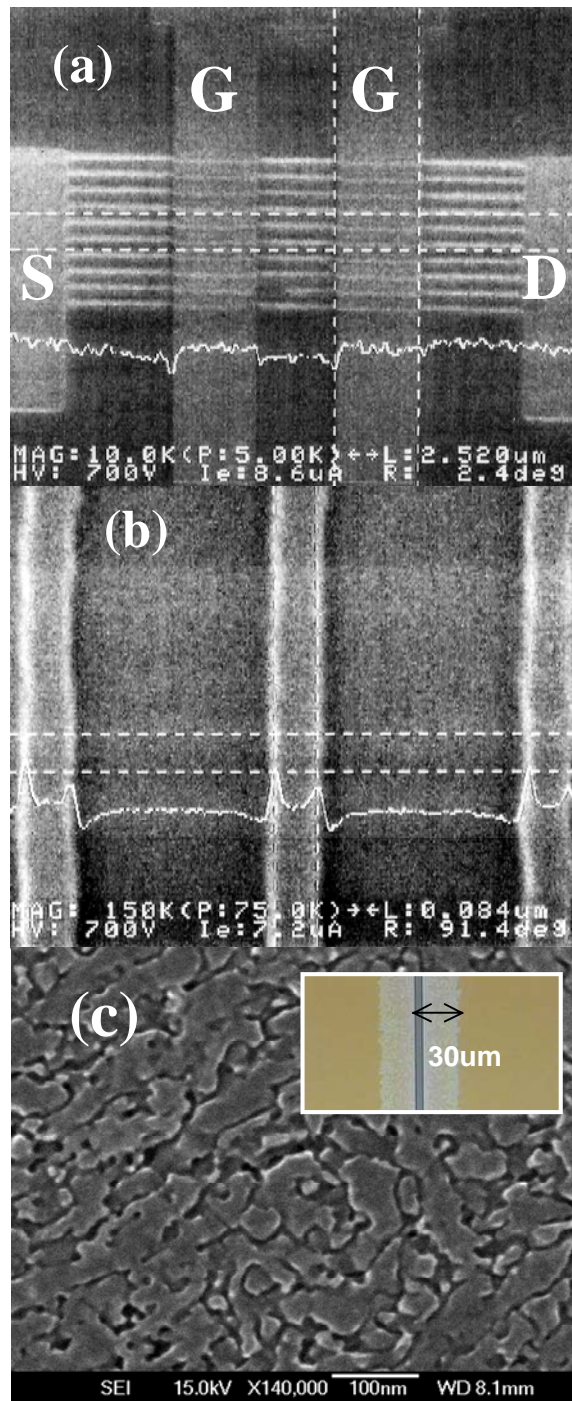


Fig. 7-3. (a) Scanning electron microscopy (SEM) photography of active pattern with the source, drain, ten nanowire channels and dual-gate. (b) SEM photography of magnified area of multiple nanowire channels. The each nanowire width is 84 nm. (c) The SEM photography of Ni-MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm. The inset optical microscopy photography depicts a MILC length of 30 μm

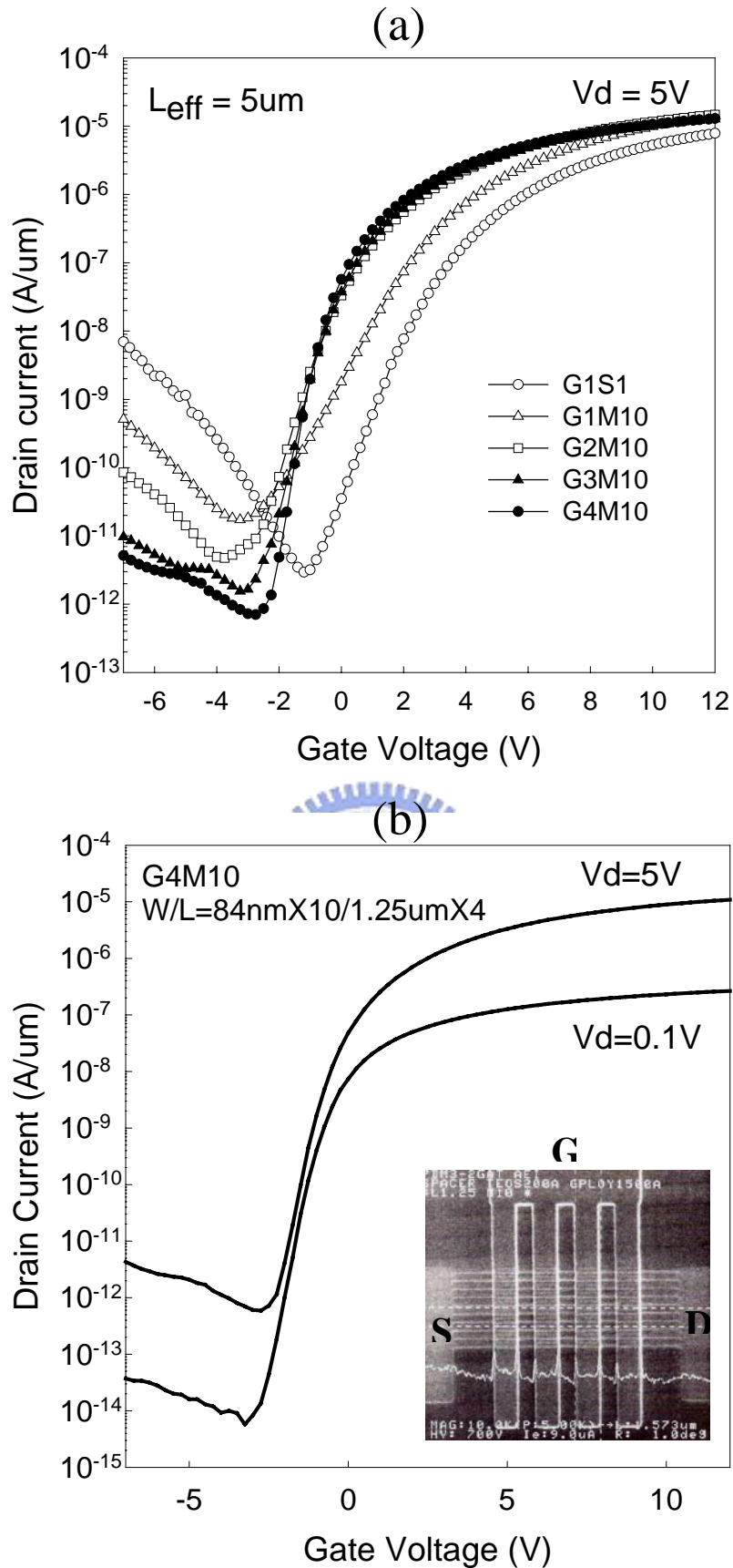


Fig. 7-4. (a) Comparison of $I_d - V_g$ transfer characteristics of all proposed Ni-MILC poly-Si TFT with the same device length (L_{tot}) of 5 μm . (b) The transfer curve of G4M10 TFT with linear and saturation region. The inset SEM photography shows the G4M10 TFT active region.

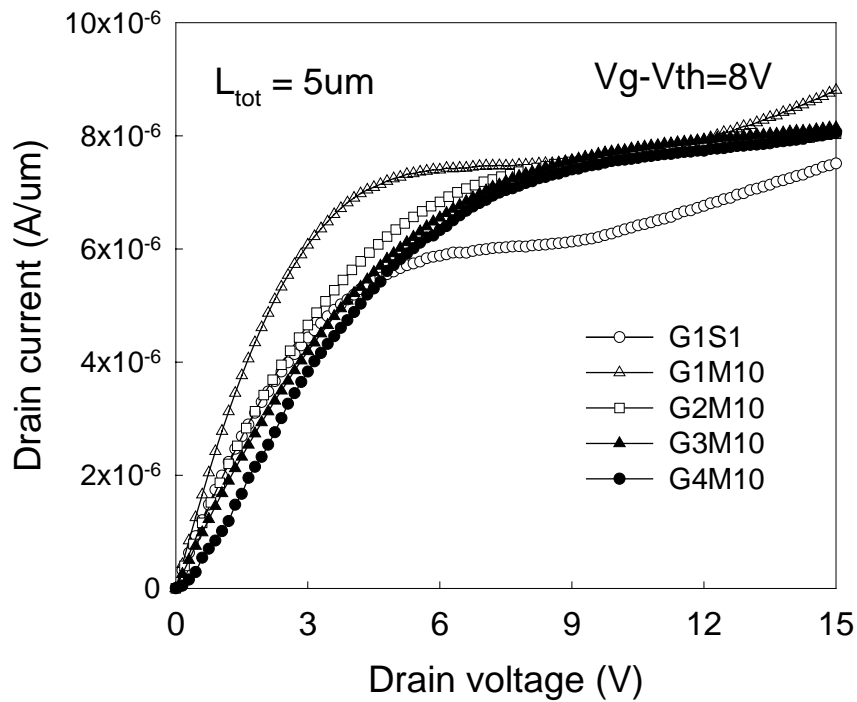


Fig. 7-5. Comparison of $I_d - V_d$ output characteristics of all proposed Ni-MILC poly-Si TFTs with the same device length (L_{tot}) of 5 μm .

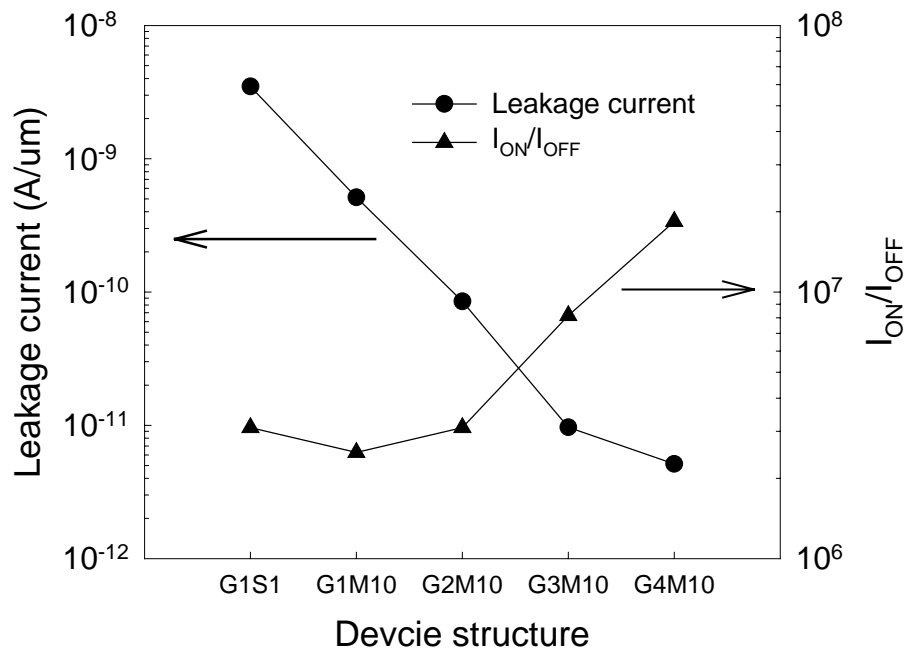


Fig. 7-6. Leakage current and ON/OFF ratio versus all proposed TFTs, operated in the saturation regime ($V_d = 5V$).

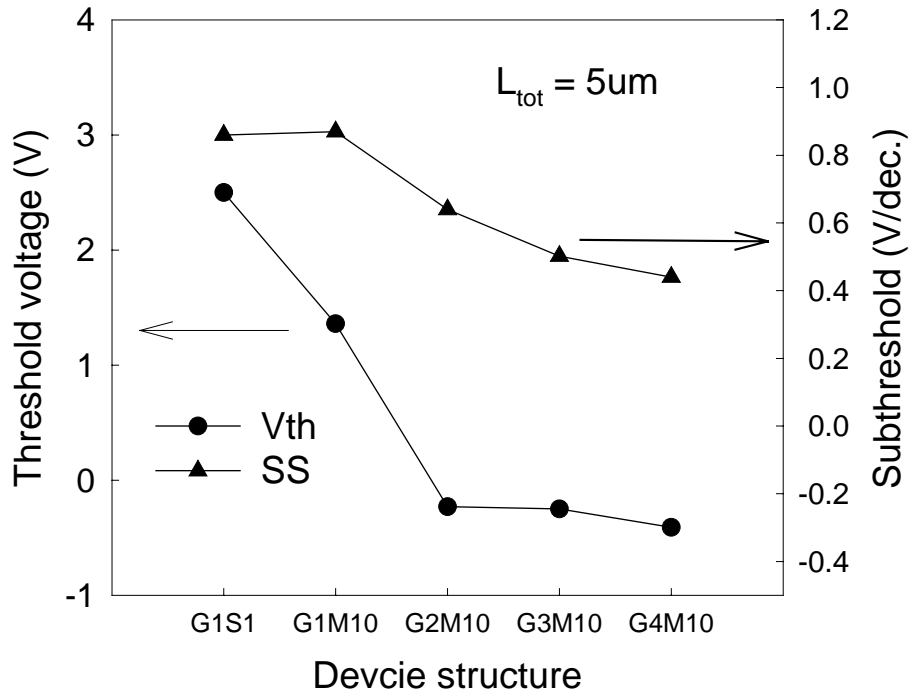


Fig. 7-7. Threshold voltage and subthreshold swing versus all proposed TFTs, operated in the saturation regime ($V_d = 5$ V).

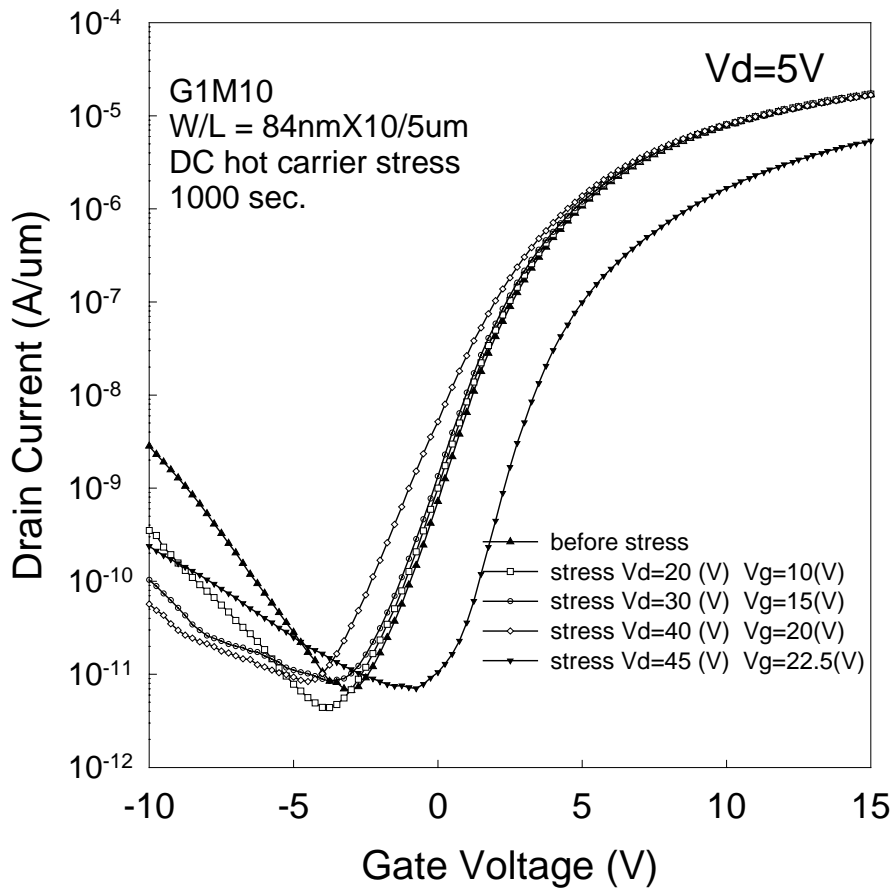


Fig. 7-8. A series of G1M10 TFT transfer curves after different hot-carrier stress conditions with 1000-second duration.

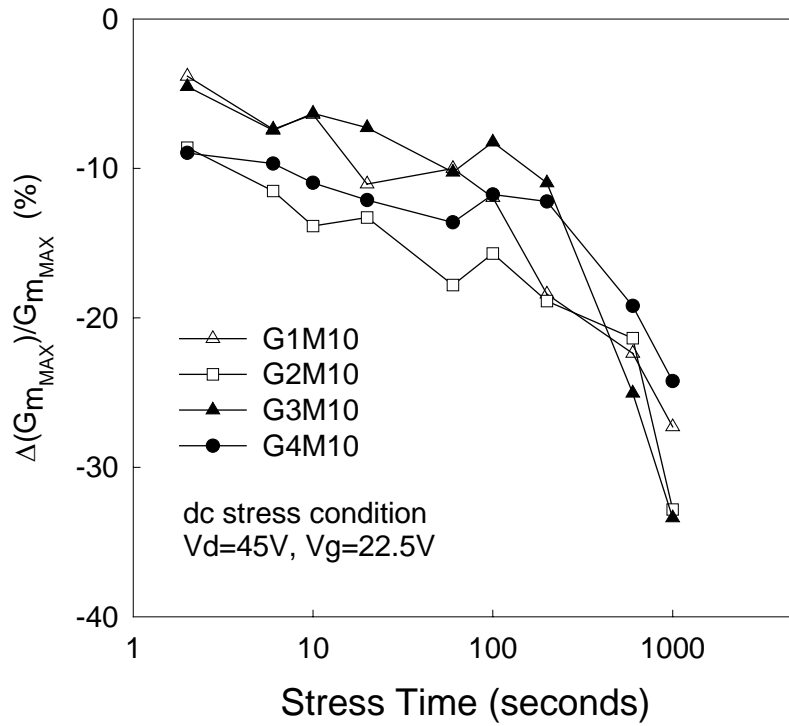


Fig. 7-9. Maximum transconductance (G_m) degradation versus dc hot-carrier time with all ten nanowire channels TFTs, extracted in the saturation regime ($V_d = 5$ V).

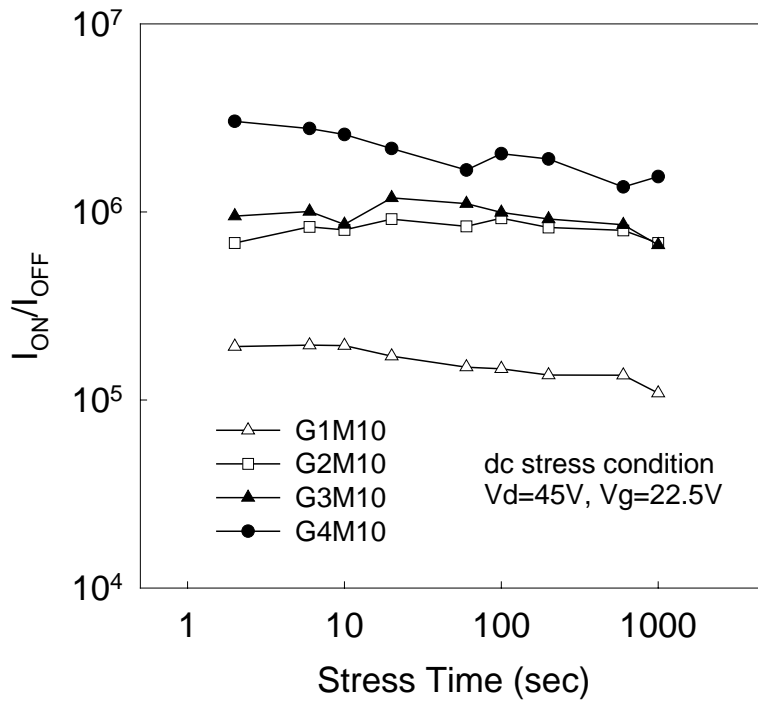


Fig. 7-10. ON/OFF ratio versus dc hot-carrier time with all ten nanowire channels TFTs, extracted in the saturation regime ($V_d = 5$ V).