Chapter 8

Conclusion

For the conclusion of this thesis, firstly in chapter 3, we studied the relationship between electrical characteristics and channel width dimension in multi-channel poly-TFT with nano-wires devices. Experimental results indicate that the device performance enhances with the increasing of number channels, from S1, M2, M5 to M10 TFTs, because their structures vary from single-gate to tri-gate controlled devices gradually. Therefore, M10 TFT exhibits superior and uniform characteristics, including low leakage current in the off-state, a high *ON/OFF* drain current ratio, a steep subthreshold slope, an absence of *DIBL* and favorable output characteristics. The fabrication of multi-channel TFTs with nano-wires is easy and involves no additional processes. Such TFTs are thus very promising candidates for use in future high-performance poly-Si TFT applications.

In chapter 4, we studied the reliability after dc and ac hot-carrier stress of poly-Si TFTs with multiple nanowire channels and lightly-doped drain structure. The experiment results reveal that the multiple nanowire poly-Si TFTs has higher performance than single-channel TFT, including a high ON/OFF current ratio, a low subthreshold slope, an absence of DIBL and favorable output characteristics. In static

and dynamic hot-carrier stress experiments, the multiple nanowire poly-Si TFTs reduces the degradation of Vth, SS, Ion, On/OFF ratio and DIBL, for all kind of frequency, rising time, falling time and temperature, compared to single-channel TFT. These high reliability results of multiple nanowire poly-Si TFTs can be explained by its robust tri-gate control and its superior channel NH_3 passivation on the poly-Si grain boundary.

In chapter 5, we discussed a novel method of enhancing the mobility of poly-Si TFTs using nanowire a channel by pattern-dependent metal-induced lateral crystallization was proposed and the TFTs fabricating using such a method were characterized. The pattern-dependent metal-induced lateral crystallization of poly-Si TFTs increased the field-effect mobility by reducing the channel width. The PDMILC poly-Si TFT with the ten nanowire channels (M10) has the highest field-effect mobility and the lowest subthreshold swing.

In chapter 6, we discussed the width and NH_3 plasma passivation effect on electrical characteristics of pattern-dependent metal-Induced lateral crystallization of polysilicon thin-film transistors (PDMILC poly-Si TFTs). The experimental results indicate that the performance of devices improves as the number of channels increases from the S1, M2 and M5 to the M10 PDMILC TFT, with the increase in the strength of the effect of the NH3 plasma passivation. The defect density (N_t) in the grain

boundary reveals a strong consistency between theory and experimental results. Additionally, NH_3 plasma passivation more strongly influences M10 TFT than it does other TFTs. Because the M10 TFT has a split nano-wire structure, most of which undergoes NH_3 plasma passivation, further reducing the number of defects at grain boundaries. These high performance NH_3 plasma passivation PDMILC TFTs are compatible with complementary metal oxide semiconductor (CMOS) technology, thus highly suitable for use in future SOP applications.

In chapter 7, we discussed the metal-induced lateral crystallization polysilicon thin-film transistors with multiple nanowire channels and multiple gates. The experiment results show that applying ten nanowire channels enhances the Ni-MILC poly-Si TFT performance. Moreover, using the multi-gate structure can further enhance the TFT performance, including a lower leakage current, a higher ON/OFF ratio, a lower Vth, and a lower SS than single-gate TFT. In output characteristics, the multi-gate with ten nanowire TFT can reduce the kink-effect. This novel multi-channel and dual-gate Ni-MILC poly-Si TFTs is quite easy and involves no additional processes, thus highly suitable for high-performance MILC poly-Si TFT applications.