著作目錄 (Publication List)

（畢業點數：19點）

International conference:

1. （2點會議論文集）**Yung-Chun Wu**, Chun-Yen Chang, Ting-Chang Chang, Po-Tsun Liu, Chi-Shen Chen, Chun-Hao Tu, Hsiao-Wen Zan, Ya-Hsiang Tai, and Simon Min Sze,"High Performance and High Reliability Polysilicon Thin-Film Transistors with Multiple Nano-Wire Channels", p. 777-780, 2004 ***International Electron Device Meeting (IEDM)***, San Francisco USA.
2. **Yung-Chun Wu**, Yuan-Chun Wu, Cheng-Wei Chou, Chun-Hao Tu, Jen-Chung Lou, Ting-Chang Chang, Po-Tsun Liu, and Chun-Yen Chang "Mobility Enhancement of Pattern-dependent Metal-Induced Lateral Crystallization Polysilicon Thin-Film Transistors with different dimensions", p. 268-271, 2005 ***Society for Information Display (SID)***, Boston, USA.
3. **Yung-Chun Wu,** Che-Yu Yang, Chi-Shen Chen, Ting-Chang Chang, Po-Tsun Liu, and Chun-Yen Chang, "The Effects of Electrical Stress and Temperature on the Properties of Polysilicon Thin-Film Transistors with Multiple Nano-Wire Channels", p. 151-154, ***1st Internatioal TFT conference***, Seoul, Korea, 2005.
4. **Yung-Chun Wu**, Ting-Chang Chang, Cheng-Wei Chou, Yuan-Chun Wu, Chun-Hao Tu, Po-Tsun Liu, and Chun-Yen Chang, "High performance Metal-induced Lateral Crystallization Polysilicon Thin-Film Transistors with Multiple Nano-Wire Channels and Multiple Gates", ***The 2005 Silicon Nanoelectronics Workshop*** *(SNW)*, Kyoto, Japan, 2005.

International Journals:

1. （3點短文）**Yung-Chun Wu**, Ting-Chang Chang , Po-Tsun Liu, Chi-Shen Chen, Chun-Hao Tu, Hsiao-Wen Zan, Ya-Hsiang Tai, and Chun-Yen Chang, "High-Performance Polycrystalline Silicon Thin-Film Transistor with Multiple Nano-Wire Channels and Lightly-Doped Drain Structure" ***Appl. Phys. Lett.***, **19**, pp. 3822-3824, 2004.
2. （3點長文）**Yung-Chun Wu**, Ting-Chang Chang, Cheng-Wei Chou, Yuan-Chun Wu, Po-Tsun Liu, Chun-Hao Tu, Jen-Chung Lou, Chun-Yen Chang "Effects of Channel Width Dimension on Electrical Characteristics of Polysilicon Thin Film Transistors with Multiple Nano-Wire Channels", ***Journal of The Electrochemical Society***, **152**, G545-549, 2005.

3. （3點短文）**Yung-Chun Wu**, Ting-Chang Chang, Po-Tsun Liu, Chang-Wei Chou, Yuan-Chun Wu, Chun-Hao Tu, and Chun-Yen Chang, “Reduction of Leakage Current in Metal-Induced Lateral Crystallization Polysilicon Thin-Film Transistors with Dual-Gate and Multiple Nanowire Channels”, ***IEEE Trans. Electron Device, Lett*** *vol. 26, no. 9, pp. 646-648, 2005.*

4. （2點短文）**Yung-Chun Wu**, Ting-Chang Chang, Po-Tsun Liu, Chi-Shen Chen, Chun-Hao Tu, Hsiao-Wen Zan, Ya-Hsiang Tai, Chun-Yen Chang, “Effects of Channel Width on Electrical Characteristics of Polysilicon Thin-Film Transistors with Multiple Nanowire Channels” ***IEEE Trans. Electron Device****, Volume 52, Issue 10, pp. 2343 – 2346, Oct. 2005.*

5. （3點長文）**Yung-Chun Wu**, Ting-Chang Chang, Po-Tsun Liu, Cheng-Wei Chou, Yuan-Chun Wu, Chun-Hao Tu, and Chun-Yen Chang, “High performance Metal-induced Lateral Crystallization Polysilicon Thin-Film Transistors with Multiple Nano-Wire Channels and Multiple Gates” ***IEEE Trans. Nanotechnology***, 2005 (in press).

6. （3點短文）**Yung-Chun Wu**, Ting-Chang Chang, Po-Tsun Liu, Yuan-Chun Wu, Cheng-Wei Chou, Chun-Hao Tu, Jen-Chung Lou, Chun-Yen Chang “Mobility Enhancement of Polysilicon Thin-Film Transistor using Nanowire Channels by Pattern-dependent Metal-Induced Lateral Crystallization” ***Appl. Phys. Lett.****, **87**, pp. 143504, 2005,*

7. Shu-Fen Hu, **Yung-Chun Wu**, Chin-Lung Sung, Chun-Yen Chang, Member, IEEE, and Tiao-Yuan Huang, “A Dual-Gate-Controlled Single-Electron Transistor Using Self-Aligned Polysilicon Sidewall Spacer Gates on Silicon-on-Insulator Nanowire” ***IEEE Trans. Nanotechnology,*** *vol.3, pp.93-97, March, 2004.*

8. Chun-Hao Tu, Ting-Chang Chang, Po-Tsun Liu, Hsiao-Wen Zan, Ya-Hsiang Tai, Li-Wei Feng, **Yung-Chun Wu**, and Chun-Yen Chang, “Improvement of Reliability for Polycrystalline Thin-Film Transistors Using Self-Aligned Fluorinated Silica Glass Spacers”, ***Electrochem. Solid-State Lett****. 8, G209, 2005.*

9. Chun-Hao Tu, Ting-Chang Chang, Po-Tsun Liu, Hsiao-Wen Zan, Ya-Hsiang Tai, Che-Yu Yang, **Yung-Chun Wu**, Hsin-Chou Liu, Wei-Ren Chen, and Chun-Yen Chang, “Enhanced Performance of Poly-Si Thin Film Transistors Using Fluorine Ions Implantation”, ***Electrochem. Solid-State Lett****. 8, G246, 2005.*

專利:

1. 薄膜電晶體及其製造方法，中華民國及美國專利申請中
2. 多晶矽薄膜電晶體及其製造方法，中華民國及美國專利申請中