Fabrication and Characterization of Novel Structure with Nano-Scale Low-Temperature High-Performance Polysilicon Thin-film Transistors

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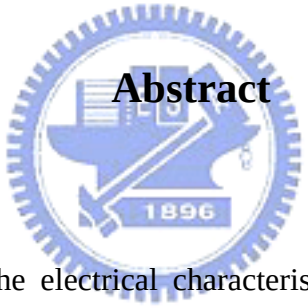

Abstract

In first part, we study the electrical characteristics of a series of polysilicon thin-film transistors (poly-Si TFTs) with different numbers of multiple channels of various widths, with lightly-doped drain (LDD) structures. Among all investigated TFTs, the nano-scale TFT with ten 67 nm-wide split channels (M10) has superior and more uniform electrical characteristics than other TFTs, such as a higher ON/OFF current ratio (>10^9), a steeper subthreshold slope (*SS*) of 137 mV/decade, an absence of drain-induced barrier lowering (*DIBL*) and a suppressed kink-effect. These results originate from the fact that the active channels of M10 TFT has best gate control due to its nano-wire channels were surrounded by tri-gate electrodes. Additionally,

experimental results reveal that the electrical performance of proposed TFTs enhances with the number of channels from one to ten strips of multiple channels sequentially, yielding a profile from a single gate to tri-gate structure. Additionally, NH_3-plasma passivation more efficiently affects M10 TFT than it does other TFTs. The M10 TFT has a split nano-wire structure, most of which is exposed to NH_3 plasma passivation, further reducing the number of grain boundary defects. On the other hand, the ac and dc reliability of ten-nanowire poly-Si TFTs are investigated. In static and dynamic hot-carrier stress experiments, the ten-nanowire poly-Si TFTs reduces the degradation of Vth, SS, Ion, On/OFF ratio and DIBL, for all kind of frequency, rising time, falling time and temperature, compared to single-channel TFT. These high reliability results of multiple nanowire poly-Si TFTs can be also explained by its robust tri-gate control and its superior channel NH_3 passivation on the poly-Si grain boundary. Devices that contain the proposed M10 TFT are highly promising for use in active-matrix liquid-crystal-display and 3-D CMOS technologies without any additional processing.

In second part, the effects of channel width and NH_3 plasma passivation on the electrical characteristics of a series of a novel 4-mask pattern-dependent metal-induced lateral crystallization (PDMILC) polysilicon thin-film transistors (poly-Si TFTs) were studied. The mobility and device performance of PDMILC TFTs improves as the each channel width decreasing. Furthermore, PDMILC TFTs with

NH_3 plasma passivation outperforms without such passivation, resulting from the effective hydrogen passivation of the grain-boundary dangling bonds, and the pile-up of nitrogen at the SiO2/poly-Si interface. In particular, the electrical characteristics of a nano-scale TFT with ten 67 nm-wide split channels (M10) are superior to those of other TFTs. The former include a higher field effect mobility of 84.63 cm^2/Vs, a higher ON/OFF current ratio (>10^6), a steeper subthreshold slope (*SS*) of 230 mV/decade, an absence of drain-induced barrier lowering (*DIBL*). These findings originate from the fact that the active channels of the M10 TFT have exhibit most poly-Si grain enhanced to reduce the grain boundary defects and best NH_3 plasma passivation due to its split nanowire structure. Both effects can reduce the number of defects at grain boundaries of poly-Si in active region for high performances.

In addition, we have also studied the multi-gate combining the pattern-dependent nickel (Ni) metal-induced lateral crystallization (Ni-MILC) polysilicon thin-film transistors (poly-Si TFTs) with ten nanowire channels. Experimental results reveal that applying ten nanowire channels improves the performance of Ni-MILC poly-Si TFT, which thus has a higher ON current, a lower leakage current and a lower threshold voltage (Vth) than single-channel TFTs. Furthermore, the experimental results reveal that combining the multi-gate structure and ten nanowire channels further enhances the entire performance of Ni-MILC TFTs, which thus have a low

leakage current, a high ON/OFF ratio, a low Vth, a steep subthreshold swing (SS) and kink-free output characteristics. The multi-gate with ten nanowire channels NI-MILC TFTs has few poly-Si grain boundary defects, a low lateral electrical field and a gate channel shortening effect, all of which are associated with such high-performance characteristics. The PDMILC TFTs process is compatible with CMOS technology, and involves no extra mask. Such high performance PDMILC TFTs are thus promising for use in future high-performance poly-Si TFT applications, especially in AMLCD and 3D MOSFET stacked circuits.

Key words: Polysilicon thin-film transistors (poly-Si TFTs), Nanowire, Tri-gate, Pattern-depended metal induced lateral crystallization (PDMILC), Multi-gate, AMLCD.