Figure Captions

Chapter 2

Fig. 2-1 (a) Model for the crystal structure of polysilicon films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure of the polysilicon crystallites.

Fig. 2-2 Energy band diagram in the lateral direction along the channel of a n-channel polysilicon TFTs.

Fig. 2-3 A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

Fig. 2-4 Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

Fig. 2-5 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling.

Fig. 2-6 The kink effect in the output characteristics of an *n*-channel SOI MOSFET.

Fig. 2-7 MILC polysilicon formation during annealing process. (a) At the beginning of the annealing process, many nickel atoms are trapped and nickel silicide is formed at the grain boundaries of the MILC polysilicon region. Those nickel silicide grain boundaries at the MIC to a-Si interfaces, which are reactive regions, are responsible for MILC formation. (b) During the annealing process, the nickel silicide RGB absorbs silicon atoms from the a-Si region and rejects them to the MIC polycrystalline silicon region. As a result, the polysilicon grain grows up in lateral direction.

Fig. 2-8 MILC polysilicon formation mechanism. (i) Most of nickel atoms are trapped at the nickel silicide RGB, which is a layer between the amorphous silicon (a-Si) and MILC crystalline silicon regions. (ii) The nickel atoms in

the nickel silicide RGB diffuse to the a-Si region and bonds with silicon atoms. The activation energy of the a-Si crystallization is lowered by the nickel impurities. (iii) The silicon atoms are dissociated from the nickel silicide RGB and then bond to the MILC crystalline silicon region. (iv) Nickel atoms diffuse to the a-Si region and crystallize the a-Si atoms continuously. This leads the shift of nickel silicide RGB and the growth of MILC polysilicon. (v) Only few nickel atoms are left and trapped inside the MILC silicon grain.

Fig. 2-9 Epitaxial silicon growth using nickel silicide, in which, the nickel silicide consumes the a-Si stoms at the leading edge and rejects the Si atoms to the crystalline silicon region.

Chapter 3

Fig. 3-1 (a) Schematic diagram of M10 poly-Si TFT. (b) Cross-section view of Fig. 1a AA' direction, as a conventional top-gate LDD MOSFET structure. (c) One of channel cross-section view of Fig. 1a BB' direction, as a tri-gate structure. Active layer, gate oxide, and poly-gate thickness are 50 nm, 26 nm and 150 nm, respectively.

Fig. 3-2 Simulation results of potential contour plots and electrical field lines of (a) single-top-gate TFT (b) tri-gate TFT with L = 0.5 um, gate oxide = 26 nm, channel thickness = 50 nm at $V_g = 0\ V$, $V_d = 2\ V$.

Fig. 3-3 (a) Scanning electron microscopy (SEM) photography of active pattern with the source, the drain and multiple nano-wire channels of M10 TFT. (b) Magnified area of multiple nano-wire channels. The each nano-wire width is 67 nm. (c) Transmission electron microscopy (TEM) photography of poly-Si grains by solid phase crystallization. The average poly-Si grain size is about 30 nm.

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Fig. 3-4 Device characteristics of S1 (L / W = 0.5 um / 1 um) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

Fig. 3-5 Device characteristics of M2 (L / W = 0.5 um / 0.5 um × 2) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

Fig. 3-6 Device characteristics of M5 (L / W = 0.5 um / 0.18 um × 5) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

Fig. 3-7 Device characteristics of M10 (L / W = 0.5 um / 67 nm × 10) poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve.

Fig. 3-8 Field effect mobility (μ_{FE}) versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

Fig. 3-9 Drain ON/OFF current ratio (R) and drain leakage current versus multi-channel with different widths poly-Si TFTs. The dots value present average value.

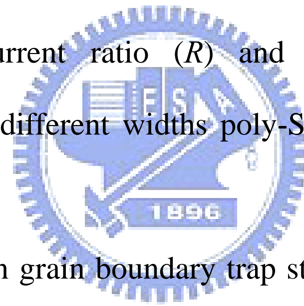

Fig. 3-10 Effective polysilicon grain boundary trap state density (N_t) of M10 and S1 poly-Si TFTs.

Fig. 3-11 Threshold voltage (V_{th}) versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

Fig. 3-12 Subthreshold slope (SS) versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

Fig. 3-13 Drain induced barrier lowering ($DIBL$) value versus multi-channel with different widths poly-Si TFTs. The dots value present average value and error bars present standard deviation.

Chapter 4

Fig. 4-1 The dynamic pulse train stress is defined at constant Vd = 6 V and dynamic Vg = 3V (ON), -3V (OFF) with the duty cycle of 50%, and the source potential is common.

Fig. 4-2a Typical M10 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

Fig. 4-2b Typical S1 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

Fig. 4-3 Maximum conductance (Gm,max) degradation of S1 and M10 TFT as a `function of the stress time with different frequencies (DC, f = 1K Hz, and f = 1M Hz).

Fig. 4-4 Threshold voltage of S1 and M10 TFT as a function of the stress time with different frequencies.

Fig. 4-5 Subthreshold swing variation of S1 and M10 TFT as a function of the stress time with different frequencies.

Fig. 4-6 ON current (I_{ON}) variation of S1 and M10 TFT as a function of the stress time with different frequencies.

Fig. 4-7 ON/OFF ratio of S1 and M10 TFT as a function of the stress time with different frequencies.

Fig. 4-8 Gm degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

Fig. 4-9 Dependence of emission intensity on (a) pulse rise time and (b) pulse fall time. Emission intensity is independent of the pulse rise time. However, we have found that it strongly depends on the fall time.

Fig. 4-10 Vth variation of S1 and M10 TFT as a function of the stress time with

different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

Fig. 4-11 ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

Fig. 4-12 Gm degradation of S1 and M10 TFT as a function of the stress time with different subtract temperature with 25^{0}C, and 75^{0}C under the same frequency of 1 KHz.

Fig. 4-13 Vth variation of S1 and M10 TFT as a function of the stress time with 25^{0}C, and 75^{0}C under the same frequency of 1 KHz

Fig. 4-14 ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with 25^{0}C, and 75^{0}C under the same frequency of 1 KHz

Chapter 5

Fig. 5-1 (a) Schematic plot of PDMILC M10 poly-Si TFT with source, drain, gate, ten nanowire channels, contact holes and MILC seeding window. The distance between the MILC seeding window edge and middle of active channel is 16 um.

(b) Cross-section view of PDMILC TFT, which was a conventional MOSFET with offset structure.

Fig. 5-2 (a) Scanning electron microscopy (SEM) photograph of active pattern with the source, the drain, ten nanowire channels and MILC seeding window. The inset SEM photography shows the each nanowire width of 67 nm. (b) SEM photography of poly-Si grain structure in active channel of S1 MILC poly-Si TFT after Secco solution etching. The average poly-Si lateral grain size is 250 nm. The inset optical microscopy photography depicts a MILC length of 30 um. (c) SEM photography of grain structure in one of ten

nanowire MILC poly-Si TFT (M10) after Secco etching. The poly-Si lateral grain length is 520 nm.

Fig. 5-3 Transfer I_d - V_g curves (left) and field-effect mobility (μ_{FE}) (right) of a series of PDMILC TFT of multi-channel with different widths at the gate length of 2 um.

Fig. 5-4 Field-effect mobility (μ_{FE}) average and standard deviation value versus the gate length, for a particular M10 TFT (W = 67 nm × 10) structure.

Chapter 6

Fig. 6-1 (a) Schematic plot of PDMILC poly-Si TFT with source, drain, gate, ten nano-wires channels, contact holes and MILC seeding window. (b) Top-view of PDMILC poly-Si TFT. The key process flows are active region pattering, gate patterning, MILC seeding window and contact holes patterning, and all metal pads pattering. (c) Cross-section view of PDMILC poly-Si TFT, which was a conventional MOSEFET with offset structure.

Fig. 6-2 (a) Scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nano-wire channels and MILC seeding window. The inset plot shows the each nano-wire width of 67 nm. (b) SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm.

Fig. 6-3 Device characteristics of S1 (W / L = 1 um / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

Fig. 6-4 Device characteristics of M2 (W / L = 0.5 um × 2 / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH3 plasma passivation.

Fig. 6-5 Device characteristics of M5 (W / L = 0.18 um × 5 / 5 um) PDMILC

poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

Fig. 6-6 Device characteristics of M10 (W / L = 67 nm × 10 / 5 um) PDMILC poly-Si TFT, (a) transfer I_d - V_g curve and (b) output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

Fig. 6-7 PDMILC poly-Si TFTs' μ_{FE} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

Fig. 6-8 PDMILC poly-Si TFTs' I_{on}/I_{off} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

Fig. 6-9 PDMILC poly-Si TFTs' V_{th} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

Fig. 6-10 PDMILC poly-Si TFTs' *SS* versus the multi-channel with different widths, with and without NH_3 plasma passivation.

Fig. 6-11 Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

Fig. 6-12 PDMILC poly-Si TFTs' N_t versus the multi-channel with different widths, with and without NH_3 plasma passivation.

Chapter 7

Fig. 7-1 (a) The schematic plot of G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, an Ni-MILC seeding window and the dual–gate. (b) Top-view plot of G2M10 Ni-MILC poly-Si TFT. (c) Cross-section view of Ni-MILC poly-Si TFT, which was a conventional top-gate, self-aligned offset MOSFET structure.

Fig. 7-2 (a) Off-state electrical field simulation results of single-gate and dual-gate poly-Si TFT b y ISE TCAD v. 7 (a 2-D device simulator). (b) The peak lateral electrical file (E_m) versus different gate number TFT structure.

Fig. 7-3 (a) Scanning electron microscopy (SEM) photography of active pattern with the source, drain, ten nanowire channels and dual-gate. (b) SEM photography of magnified area of multiple nanowire channels. The each nanowire width is 84 nm. (c) The SEM photography of Ni-MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm. The inset optical microscopy photography depicts a MILC length of 30 um

Fig. 7-4 (a) Comparison of I_d - V_g transfer characteristics of all proposed Ni-MILC poly-Si TFT with the same device length (L_{tot}) of 5 um. (b) The transfer curve of G4M10 TFT with linear and saturation region. The inset SEM photography shows the G4M10 TFT active region.

Fig. 7-5 Comparison of I_d - V_d output characteristics of all proposed Ni-MILC poly-Si TFTs with the same device length (L_{tot}) of 5 um.

Fig. 7-6 Leakage current and ON/OFF ratio versus all proposed TFTs, operated in the saturation regime (Vd = 5 V).

Fig. 7-7 Threshold voltage and subthreshold swing versus all proposed TFTs, operated in the saturation regime (Vd = 5 V).

Fig. 7-8 A series of G1M10 TFT transfer curves after different hot-carrier stress conditions with 1000-second duration.

Fig. 7-9 Maximum transconductance (Gm) degradation versus dc hot-carrier time with all ten nanowire channels TFTs, extracted in the saturation regime (Vd = 5 V).

Fig. 7-10 ON/OFF ratio versus dc hot-carrier time with all ten nanowire channels TFTs, extracted in the saturation regime (Vd = 5 V).