Table Captions

Chapter 3

Table 3-1 Devices dimension of M10, M5, M2 and S1. All devices have the same active channel thickness 50 nm and gate oxide thickness 26 nm.

Table 3-2 Devices average and standard deviation parameters of S1, M2, M5 and M10. Number inside the bracket is parameter's standard deviation. All parameters were extracted at V_d = 2V, except for the field-effect mobility which were extracted at V_d = 0.05 V.

Chapter 4

Table 4-1 Variation of experimental electronic parameters and corresponding possible degradation mechanics.

Chapter 5

Table 5-1 Devices dimension of S1, M2, M5 and M10 PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm, gate TEOS-oxide thickness of 25 nm and gate length of 2 um.

Table 5-2 Device parameters average and standard deviation value of M10, M5, M2 and S1 TFTs with gate length (L) of 2 um. The V_{th} is defined as the gate voltage required to achieve a normalized drain current of I_d / (W/L) = 10^{-8} A at V_d = 0.1 V.

Chapter 6

Table 6-1 Devices dimension of S1, M2, M5 and M10 PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 25 nm.

Table 6-2 Device parameters of PDMILC TFTs with the same L = 5 um at different widths. All parameters were extracted at V_d = 5 V, except for

the field-effect mobility (μ_{FE}) which were extracted at V_d = 0.1 V.

Chapter 7

Table 7-1 Devices dimension of all proposed Ni-PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 50 nm.