Chapter 1

Introduction

1.1 Overview of polysilicon thin-film transistor technology

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1], and organic light-emitting diodes (OLEDs) [2]. Except large area displays, poly-Si TFTs also have been applied for memory devices such as dynamic random access memory (DRAM) [3], static random access memory (SRAM)[4], electrically programmable read only memory (EPROM) [5], electrically erasable programmable read only memory (EEPROM) [6], linear image sensor [7], thermal printer head [8], photo-detector amplifier [9], scanner [10], and neutral network [10]. Lately, some superior performances of poly-Si TFTs have been reported by scaling down device dimensions or utilizing novel crystallization technologies to enhance poly-Si film quality [11-12]. These approaches provide an opportunity of using poly-Si TFTs for three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary important, leading to rapid development of poly-Si TFT technology.

The major attraction of applying polycrystalline silicon thin-film transistors

(poly-Si TFTs) in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility in poly-Si film, the capability of integrating the pixel switching elements, and the capability to integrate panel array and peripheral driving circuit on the same substrates [13-15]. In poly-Si film, carrier mobility larger than 10 cm^2/Vs can be easily achieved, that is high enough for peripheral driving circuit including n- and p-channel devices. This enables the fabrication of peripheral circuit and TFT array on the same glass substrate [16]-[18], bring the era of system-on-panel (SOP) technology. The process complexity can be greatly simplified to lower the cost. In addition, the mobility of poly-Si TFTs is much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density, high resolution AMLCDs, and the aperture ratio in TFT array could be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that the device channel width can be scaled down while meeting the same pixel driving requirements as in α-Si TFT AMLCDs.

For making high performance poly-crystalline silicon (poly-Si) thin film transistors (TFTs) [19], low-temperature technology is required for the realization of commercial flat-panel displays (FPD) on inexpensive glass substrate, since the maximum process temperature is limited to less than 600^0C. There are three major low-temperature amorphous-Si (a-Si) crystallization methods to achieve high

performance poly-Si thin film: solid phase crystallization (SPC) [20], excimer laser crystallization (ELC) [21], and metal-induced lateral crystallization (MILC)[22]. MILC technology was initially developed as a low-temperature crystallization technique compared to other low temperature poly-Si technologies such as laser crystallization (LC) or conventional solid-phase crystallization (SPC).

1.2 Motivation

1.2.1 High performance and high reliability polysilicon thin-film transistors with multiple nanowire channels

Conventional top single-gate poly-Si TFTs, however, exhibits some non-ideal effects when applied. First, they suffer from anomalous leakage current in the OFF-state, which correlates with the drain voltage and the gate voltage [23], [24]. This undesirable large OFF-state leakage current limits the application of poly-Si TFTs in switching devices. The dominant mechanism by which the leakage current in poly-Si TFTs is induced involves the field emission of carriers in grain boundary traps, due to the high electric field near the drain junction [25]. An effective method for reducing the electric field in the drain region is to incorporate a lightly-doped drain (LDD) region between the heavily doped region and the active channel region [26]. Second, the presence of polysilicon grain boundary defects in the channel region of

TFTs drastically affects the electrical characteristics [27], [28], especially when the device dimension is scaled down; Therefore, reducing the number of polysilicon grain boundary defects will improve the performance of poly-Si TFTs. TFTs with several multiple channels have been reported to effectively reduce grain boundary defects [29]-[31].

Additionally, scaling down of TFT's dimension is a continuous trend since its benefits in performance. Smaller device size enables higher device density in SRAMs and DRAMs, and increases the driving current in peripheral driver circuits in AMLCD applications. However, as a TFT's dimensions are reduced, influences from the drain side of the channel becomes significant, (i.e. gate control becomes lower), which will arise severe short-channel effect, including threshold voltage roll-off, a large subthreshold slope (*SS*), a large drain-induced barrier lowering (*DIBL*) and the occurrence of kink-effect. These effects are major limitations in realizing a system on panel (SOP). In CMOS technology, many high-performance surrounding gate structures in a silicon-on-insulator (SOI) MOSFET, such that double-gate [32], tri-gate [33], FinFET [34] and gate-all-around [35], have been reported to exhibit superior gate control over the channel than a conventional single-gate MOSFET, to reduce short-channel effects.

Therefore, in this thesis, we first apply the tri-gate structure on short-channel

(gate length = 0.5 um) TFTs design. A series of multi-channel with different widths and LDD structure poly-Si TFTs were fabricated and characterized.

On the other hand, the reliability of ploy-Si TFT is one of the main constraints toward this direction. In comparison with single-crystalline silicon, granular structure of poly-Si is rich in grain boundary defects arising from lattice discontinuities between different oriented grains as well as intra-grain defects. Those generated trap states are strongly influenced the performance of poly-TFTs and causes severe device characteristics degradation, such as threshold voltage (Vth), subthreshold swing (SS), ON current (Ion), and transconductance (Gm). The Gm degradation and Vth variation during stress application which results in improper operation and circuit failure is of great importance for circuit designers in order to integrate TFTs in flat-panel displays or VLSI circuits. In AMLCD application, unlike pixel TFTs, TFTs in the driver circuits are subject to high-frequency voltage pulses [36]. The degradation behavior under dynamic stress is closer to real operation condition than the static stress. Therefore, improvement of TFTs degradation under dynamic stress is most important requirements in realization of system-on-panel (SOP). Accordingly, the reliability of poly-Si TFTs under dc [37]-[40], and ac [41]-[43] stress has been investigated. However, to our knowledge, improvement of poly-Si TFT degradation under ac stress by device structure modulation has not been addressed. Therefore, in this work, we

develop a poly-Si TFT with ten nanowire channels and LDD structure to study the degradation mechanism; also a single-channel poly-Si was fabricated for comparison.

1.2.2 High performance pattern-depended Metal-induced Lateral Crystallization Polysilicon Thin-Film Transistors using Multiple Nanowire Channels and Multiple Gates

By comparing the three low-temperature a-Si crystallization methods, SPC, ELC, and MILC, MILC is superior because, unlike LC, it is a low-cost batch process and unlike SPC, better quality poly-Si thin film can be obtained [19]. However, most of all previous report of MILC TFTs [19], [44]-[46], additional MILC trench mask process is necessary. In a practical of view, the additional mask will cause the fabrication complexity and decrease the product yield. On the other hand, applications of Ni-MILC poly-Si TFTs are still limited, because the grain boundaries of poly-Si himself in the channel region substantially degrade performance. However, the grain boundary effects can be reduced mainly by two techniques: (1) by passivating the dangling silicon bonds at the grain boundaries and thus reducing the density of the grain boundary states in the film; (2) by enhancing the grain size and, thus, reducing the number of grain boundaries present within the active channel of the TFT device. [47] The poly-Si TFTs with several multi-channels has been reported to effectively

reduce grain boundary defects [48, 49]. Besides, the Ni-MILC poly-Si TFT was suffered from severe leakage current due to Ni contamination during MILC annealing process [50, 51], which is directly related to lateral electrical field in drain depletion region. This is another major limitation of Ni-MILC poly-Si TFT application. The poly-Si TFTs with multi-gates has been reported to effectively reduce leakage current [52, 53]. On the other hand, the NH_3 plasma passivation [54] has been reported to reduce the number of trap–states in poly-Si grain boundaries, yielding high-performance poly-Si TFTs.

Therefore, in this work, we first develop novel four-masks pattern-depended Ni-MILC poly-Si TFT with a series of multi-gate with multiple nanowire channels to overcome above limitations. The experiment results demonstrate that applying multi-gate with multiple nanowire channels structure can significantly reduce the leakage current, while keeping in high performance of Ni-MILC TFT. In addition, NH_3 plasma passivation has applied to reduce the number of trap–states in poly-Si grain boundaries, yielding high-performance poly-Si TFTs. In this work, the effects of NH_3 plasma passivation on the electrical characteristics of a series of multi-channels with PDMILC poly-Si TFT structures of various (pattern-dependent) widths are initially investigated. Besides, in device reliability study, the novel PDMILC TFT under static stress considering different stressing conduction is also analyzed in

chapter 7 of this dissertation.

1.3 Organization of the thesis

In chapter 1, a brief overview of the poly-Si TFTs background and motivation are introduced.

In chapter 2, we first introduce the poly-Si TFT carrier transportation mechanism. According the poly-Si TFT current-voltage model based on carrier transportation mechanism, the methods of typical parameters extraction, including threshold voltage (V_{th}), subthreshold slope (*SS*), drain current *ON/OFF* ratio**,** field-effect mobility (μ_{FE}), and the trap density (N_t) are introduced. Then, the two major non-ideal effects: leakage current, and kink-effect, which limit the TFTs application are introduced. Finally, the metal-induced lateral crystallization formation mechanism is introduced.

In chapter 3, we study the electrical characteristics of a series of polysilicon thin-film transistors (poly-Si TFTs) with different numbers of multiple channels of various widths, with lightly-doped drain (LDD) structures. Among all investigated TFTs, the nano-scale TFT with ten 67 nm-wide split channels (M10) has superior and more uniform electrical characteristics than other TFTs, such as a higher ON/OFF current ratio (>10^9), a steeper subthreshold slope (*SS*) of 137 mV/decade, an absence of drain-induced barrier lowering (*DIBL*) and a suppressed kink-effect.

In chapter 4, we study the poly-Si TFT with ten nanowire channels and LDD structure to investigate the degradation mechanism under dc and ac stress; also a single-channel poly-Si was fabricated for comparison.

In chapter 5, we introduce method for enhancing the mobility of the poly-Si TFTs by pattern-dependent metal-induced-lateral-crystallization (PDMILC) using nanowire channels was demonstrated and characterized. The experimental results indicate that the field-effect mobility of PDMILC TFT was enhanced as the channel width decreased, because the lateral length of its poly-Si grain was increased.

In chapter 6, we introduce the channel width and of NH_3 plasma passivation effects on the electrical characteristics of a series of pattern-dependent metal-induced lateral crystallization (PDMILC) polysilicon thin-film transistors (poly-Si TFTs) with various numbers of multiple channels structures.

In chapter 7, a series of pattern-dependent nickel (Ni) metal-induced lateral crystallization (Ni-MILC) polysilicon thin-film transistors (poly-Si TFTs) with ten nanowire channels and multi-gate, were fabricated and characterized. Experimental results reveal that applying ten nanowire channels improves the performance of Ni-MILC poly-Si TFT, which thus has a higher ON current, a lower leakage current and a lower threshold voltage (Vth) than single-channel TFTs. Moreover, using the multi-gate structure can further enhance the TFT performance, including a lower

leakage current, a higher ON/OFF ratio, a lower Vth, and a lower SS than single-gate TFT.

In chapter 8, we conclude all experiments results briefly.

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