Chapter 2

Poly-Si TFT conduction mechanism and Metal-Induced Lateral Crystallization formation mechanism

2.1 Poly-Si TFT transportation mechanisms

As mentioned in section 1.1 and 1.2, the device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Even though the inversion channel region is also induced by the gate voltage as in MOSFETs, the existence of grain structure in channel layer bring large differences in carrier transport phenomenon. Many researches studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. A simple grain boundary-trapping model has been described by many authors in details [1]-[3]. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_g and the grain boundary trap density N_t (cm^{-3}). The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When the dopant/carrier density n (or N_D) (cm^{-3}) is small, the poly-Si grains will be

fully depleted. The width of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of the boundary, and the voltage barrier height V_B can be expressed as

Fully depleted:

$$V_B = \frac{qn}{2\varepsilon_S} x_d^{\ 2} = \frac{qnL_g^{\ 2}}{8\varepsilon_S} \tag{2-1}$$

As the dopant/carrier concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, making carrier transport form one grain to another more difficult. When the dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to spear inside the grain region. The depletion width and the barrier height can be expressed as

Partially depleted:

$$x_d = \frac{N_t}{2n} \tag{2-2}$$

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^{\ 2}}{8\varepsilon_s n} \tag{2-3}$$

The depletion width and the barrier hight turn to decrease with increasing dopant/carrier density, leading to improved conductivity in carrier transport.

The carrier transport in **fully depleted** poly-Si film can be described by the **thermionic emission** over the barrier. Its' current density can be written as [4]

$$J = qnv_c \exp\left[-\frac{q}{kT}(V_B - V_a)\right] \tag{2-4}$$

where **n** is the free-carrier density, $\boldsymbol{v_c}$ is the collection velocity ($v_c = \sqrt{kT/2\pi m^*}$), $\boldsymbol{V_B}$ is the barrier height without applied bias, and $\boldsymbol{V_a}$ is the applied average bias across the one grain boundary region. For small-applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_a/2$. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qnv_c \cdot \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_a)] \tag{2-5}$$

$$J_R = qnv_c \cdot \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_a)] \tag{2-6}$$

Thus the net current density is then given by

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_a}{2kT}) \tag{2-7}$$

At low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage kT/q, thus Eq. (2-7) can be simplified as

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\frac{qV_a}{2kT} = \frac{q^2 nv_c V_a}{kT}[\exp(-\frac{qV_B}{kT})] \tag{2-8}$$

the average conductivity $\sigma = J/\xi = JL_g/V_a$, and the effective mobility $\sigma = qn\mu_{eff}$ then the average conductivity can be obtained as

$$\sigma = \frac{q^2 nv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \tag{2-9}$$

$$\mu_{eff} = \frac{qv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT}) \tag{2-10}$$

where μ_0 represents the carrier mobility inside grain regions. It is found that the

conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap density.

Applying gradual channel approximation to poly-Si TFTs, which assumes that the variation of the electric field in the y-direction (along the channel) is much less than the corresponding variation in the y-direction (perpendicular to the channel), as shown figure 2-2. The carrier density n per unit area (cm^{-2}) induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{TH})}{qt_{ch}} \quad (2\text{-}11)$$

where

t_{ch} is the thickness of the inversion layer,

V_{TH} is the threshold voltage,

C_{ox} is gate oxide capacitance per unit area.

$$I_D = J \cdot W \cdot t_{ch} \quad (2\text{-}12)$$

$$J = n \cdot q \cdot \mu_{eff} \cdot \xi \quad (2\text{-}13)$$

$$\xi = \frac{V_a}{L_g} = \frac{V_D}{N_g L_g} = \frac{V_D}{\frac{L}{L_g} L_g} = \frac{V_D}{L}; \quad N_g \text{ is the grain number} \quad (2\text{-}14)$$

Therefore, by replacing Eq. (2-11), (2-13) and (2-14) into Eq. (2-12), the drain current of poly-Si TFT then can be given by

$$I_D = C_{ox} \frac{W}{L} (V_G - V_{TH}) \cdot V_D \cdot \mu_o \exp(-\frac{qV_B}{kT}) \quad (2\text{-}15)$$

Obviously, this I-V characteristic is very similar to that linear region of

MOSFETs, except that the mobility is modified.

2.2 Methods of Device Parameter Extraction

In this section, we will introduce the methods of typical parameters extraction such as threshold voltage (V_{th}), subthreshold slope (SS), drain current *ON/OFF* ratio**,** field-effect mobility (μ_{FE}), and the trap density (N_t).

2.2.1 Determination of the threshold voltage

Many ways are used to determinate the V_{th} which is the most important parameter of semiconductor devices. In poly-Si TFTs, the method to determinate the threshold voltage is *constant drain current method.* The gate voltage at a specific drain current I_N value is taken as the threshold voltage. This technique is adopted in most studies of TFTs. Typically, the threshold current $I_N = I_D / (W / L)$ is specified 100 nA for $V_D = 5$V (saturation region) in this thesis.

2.2.2 Determination of the subthreshold slope

Subthreshold slope $SS_{(\text{V/dec.})} = dV_G/d(\log I_D)$ is a typical parameter to describe the gate control toward channel. And in intrinsic polysilicon TFTs the parameter SS is directly related with the total trap states density N_T by the relationship

$$SS = \left(\frac{kT}{q}\right)\ln 10\left(1+\frac{q^2 t_{si} N_T}{C_{OX}}\right) \tag{2-16}$$

where

kT is the thermal energy,

t_{si} is the polysilicon layer thickness.

Thus, the decrease of *SS* with stressing suggests a decrease in the total trap states density, which includes both bulk and interface traps. The *SS* should be independent of drain voltage and gate voltage. However, in reality, *SS* might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The *SS* is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, the *SS* is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from 10^{-8} A to 10^{-10} A).

2.2.3 Determination of *On/Off* Current Ratio

Drain *On/Off* current ratio is another important factor of TFTs. High *On/Off* ratio represents not only large turn-on current but also small off current (leakage current). It affects gray levels (the bright to dark state number) of TFT AMLCD directly.

There are many methods to specify the on and off current. The practical one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage is applied at 5V.

2.2.4 Determination of the field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain voltage (V_d = 0.1V, V_G-V_{th}>> V_d). The transfer I-V characteristics of

poly-Si TFT can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{TH}) V_D] \tag{2-17}$$

where

W is channel width,
L is channel length,

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D = const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D \tag{2-18}$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \tag{2-19}$$

2.2.5 Modification of effective field-effect mobility

According Seto model [5], in uniform small grain poly-Si TFT, the effective field-effect mobility can be expressed:

$$\mu_{eff} = \frac{q v_c L_g}{kT} \exp(-\frac{q V_B}{kT}) \equiv \mu_0 \exp(-\frac{q V_B}{kT})$$

However, in poly-Si films with enlarged grains, the uniform trap distribution model fails to give reliable results due to high nonuniformity of the polycrystalline material. According to Farmakis *et al.* [6] model, the μ_{eff} depend on the number of grain boundaries present within the channel of the transistor. Figure 2-2 represents the energy band structure of the polysilicon in the neighborhood of the grain boundaries of a n-channel polysilicon TFT along the channel in the linear region of operation (low drain voltage V_D). This energy band structure has two resistances R_G and R_{GB}

equivalent to the grain region and the grain boundary respectively, both modulated by the gate voltage V_G. The grain region is considered to behave as in a bulk MOSFET. Therefore, considering an average number of n *GB's* and n entire grains within the channel, according to the standard MOSFET theory, the total channel resistance R_{ch} will be

$$R_{ch} = \frac{L}{W\mu_{eff}Q_{invG}} = nR_G + NR_{GB} = \frac{nL_G}{W\mu_G Q_{invG}} + \frac{nL_{GB}}{W\mu_{GB}Q_{invGB}} \tag{2-20}$$

where

μ_{eff} effective electron mobility；
μ mobility；
Q_{inv} charge in the inversion layer；
L_G average intra-grain length;
L_{GB} average grain boundary length

Throughout the text, the indices *G* and *GB* will be referred to the intra-grain and grain boundary region respectively. Assuming that the main conduction mechanism through the grain boundaries is the thermionic emission over the grain-boundary energy potential barrier V_b, the charge in the grain boundaries Q_{GB} will be given by the relationship [6]：

$$Q_{invGB} = e^{-qV_b(V_G)/kT} Q_{invG} \tag{2-21}$$

When the potential barrier V_b is high, $Q_{invGB} \ll Q_{invG}$ and according to Eq.(2-17) μ_{eff} is practically controlled by the grain boundary mobility being normally very low. When V_b is lowered enough by increasing the gate potential V_G, Q_{invGB}=Q_{invG} and

$\mu_{eff} \approx \mu_{eff}$ .By taking into account that $L = nL_G + nL_{GB}$, from Eq. (2-17) and (2-18), it is obtained

$$\frac{L}{\mu_{eff}} = \frac{L\text{-}nL_{GB}}{\mu_G} + n\frac{L_{GB}}{\mu_{GB}e^{-qV_b/kT}} \tag{2-22}$$

The average grain-boundary number inside the channel is

$$n = \frac{L}{L_G} \tag{2-23}$$

$$\frac{L}{nL_{GB}} = \frac{L_G}{L_{GB}} \tag{2-24}$$

For polysilicon TFTs with gate length and width of the same order of the grain size , n takes small values. In this case, for typical values of L_{GB} = 1-2 nm and L = 4-20 um, it is：

$$\frac{\mathrm{L}}{\mathrm{nLGB}} \gg 1 \tag{2-25}$$

Equation (2-19) is further simplified when Eq. (2-22) is taken into account：

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_G} + \frac{nL_{GB}}{L}\frac{1}{\mu_{GB}e^{-qV_b/kT}} \tag{2-26}$$

So according to the polysilicon TFTs mobility model with separating grain and grain boundaries taking into account the average number of grain boundaries into the channel, in general the effective field-effect mobility (μ_{FE}) is given by,

$$\mu_{FE} = \mu_G \frac{1}{1 + (\mu_G / \mu_{GB})[(nL_{GB})/L]\exp(qV_b/kT)} \tag{2-27}$$

where $n = L/L_G$ is the average grain-boundary number.

2.2.6 Determination of the trap density

In **partially depleted** condition, as described in Eq. (2-3), the grain boundary

potential barrier height V_B is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson *et al.* [7], the *I-V* characteristics including the trap density can be obtained by replacing Eq. (2-3) and (2-11) into Eq. (2-15):

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \exp(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}) \quad (2\text{-}28)$$

This equation had been further corrected by Proano *et al*. by considering the mobility under low gate bias [8]. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness t_{ch} in an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by

$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \quad (2\text{-}29)$$

The drain current of poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^2 (V_G - V_{FB})^2}) \quad (2\text{-}30)$$

The effective trap state density then can be obtained from the slope of the curve $ln[I_D/(V_G-V_{FB})]$ versus $(V_G-V_{FB})^{-2}$ as in figure 2-4.

2.3 Poly-Si TFTs non-ideal effect

There are two major non-ideal effects will limit the TFTs application, including

leakage current, and kink-effect. The mechanism of these three non-ideal effects is described briefly as bellow.

2.3.1 Leakage current

In AMLCD, TFTs play a switching device to turn *ON/OFF* the current path for charging/discharging the liquid crystal capacitor. Thus, the leakage current should be low enough to remain a pixel gray level before it must be refreshed. The leakage current mechanism in poly-Si has been studied by Olasupe [9]. The leakage current resulted from carrier generation from the poly-Si grain boundary defects. There are three major leakage mechanisms, as shown in figure 2-5. The dominant mechanism is a function of the prevailing drain bias. They pointed out carrier generation from grain boundary defects via thermionic emission and thermionic field emission to be prevalent at a low and medium drain biases, and carrier pure tunneling from poly-Si grain boundary defects to be the dominant mechanism at higher drain bias. In 1997, Angelis give a concise analytical equation [10] for describing the leakage current.

$$I_L = I_{L0} e^{\beta\sqrt{E_m}} = qA_j W_D \sigma v_{th} N_t n_i e^{\beta_{PF}\sqrt{E_m}} e^{\beta_{TFE}\sqrt{E_m}} \qquad (2\text{-}31)$$

$$E_m = \frac{\left|V_G - V_D - V_{fb}\right|}{t_{ox}(\varepsilon_{Si}/\varepsilon_{ox})} \qquad (2\text{-}32)$$

Where E_m is the peak electrical field, A_j is the junction area, W_D is the reversed-biased drain junction depletion width, v_{th} is the carrier thermal velocity, and β_{PF} and β_{TFE} are the field-enhancement factors arising from Poole-Frenkel effect and

thermal field emission. **Thus, the most effective way to reduce the leakage current, which is decrease the E_m.**

2.3.2 Kink effect [11]

During devices operation, a high field near the drain could induce impact ionization there. Majority carriers, holes in the p-substrate for an n-channel poly-Si TFTs, generated by impact ionization will be stored in the substrate, since there is no substrate contact to drain away these charges. Therefore the substrate potential will be changed and will result in a reduction of the threshold voltage. This, in turn, may cause an increase or a kink in the current-voltage characteristics. The kink phenomenon is shown in figure 2-6. This float-body or kink effect is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons. The kink effect can be reduced in TFTs by lowering lateral field inside the channel.

2.4 Metal-Induced Lateral Crystallization formation mechanism [12], [13]

In the last few years, several articles have been devoted to study of the growth mechanism of metal-induced-lateral-crystallization (MILC). Earlier observation of Ni induced crystallization of a-Si revealed that the onset temperature for crystallization

of a-Si was significantly reduced in presence of $NiSi_2$ precipitates and crystallization occurred at around 500^0C. The $NiSi_2$ precipitates acts as a good nucleus of Si, which has similar crystalline structure (the fluorite type, CaF_2) and a small lattice mismatch of 0.4% with Si. In the case of Ni induced crystallization, the growth of crystallites depends strongly on the migration of $NiSi_2$ precipitates, and the driving force for the migration of $NiSi_2$ precipitates is the reduction in free energy associated with the transformation of metastable a-Si to stable c-Si.

In the MILC process, nickel deposited onto the seed window first reacts with silicon to form a thin nickel silcide film, which reduces the activation energy for a-Si crystallization. Thus, a-Si under the silicide is thermally crystallized into polysilicon, and this is called the initial nucleation of crystalline Si on nickel silicide. As this polysilicon is formed by a direct metal induced method, it is also referred as metal-induced-crystallization (MIC) polysilicon. There are many grain boundaries inside the MIC polysilicon layer and these grain boundaries provide good locations for trapping the metal atoms. Due to the fast nickel diffusion in crystalline silicon structure and good nickel trapping property at the crystalline silicon to a-Si interface, most of nickel atoms in the MIC region diffuse to and are trapped at the grain boundaries. The trapped metal atoms react with silicon atoms to form thin layers of nickel silicide at the grain boundaries. At the MIC to a-Si interface, the nickel silicide

at grain boundaries exist as a continuous sandwich layer between MIC polysilicon and a-Si as illustrated in figure 2-7a and figure 2-7b This continuous nickel silicide layer is a reactive layer, which will be responsible for the grain growth, so it is called nickel silicide reactive grain boundary (*RGB*). The nickel silicide *RGB* propagates toward the a-Si region during MILC annealing and a-Si will then be crystallized.

The nickel concentration at the *RGB* is higher than the neighboring a-Si. Continuous annealing after MIC leads metal atom diffusion to the a-Si layer in lateral directions. Once the nickel atoms are pushed toward the a-Si region, those atoms repair the intrinsic traps and form a new nickel silicide *RGB*. The nickel atoms lower the activation energy of a-Si crystallization and construct the silicon atoms into a crystalline structure. Since the nickel diffusion in crystalline silicon region is relatively faster, the nickel atoms in the polysilicon region then diffuse to the new silicon grain boundary quickly. This increases the nickel concentration at the *RGB* and subsequently pushes the nickel atoms to the a-Si again and again. As a result, the a-Si is crystallized to polysilicon in the lateral direction, and this polysilicon is called metal-induced-lateral-crystallization (MILC) polysilicon. As the MILC formation is led by the propagation of the nickel silicide *RGB*, the MILC polysilicon grains grow along the direction of nickel diffusion. Figure 2-8 illustrates the silicon crystallization process during the MILC annealing. The mechanism described does not only explain

the polysilicon growth of MILC, but also help to explain the epitaxial silicon growth mechanism by nickel silicide layer propagation from crystalline silicon toward a-Si (refer to figure 2-9) proposed by other researches. It tells us why the nickel silicide absorbs silicon atoms from the a-Si region and rejects the excess Si atoms to the crystalline silicon area during epitaxial silicon growth.

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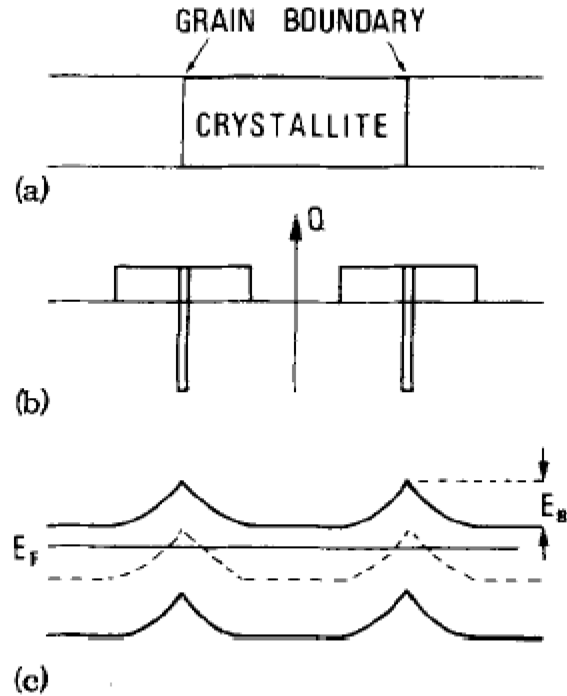

Fig. 2-1. (a) Model for the crystal structure of polysilicon films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure of the polysilicon crystallites.

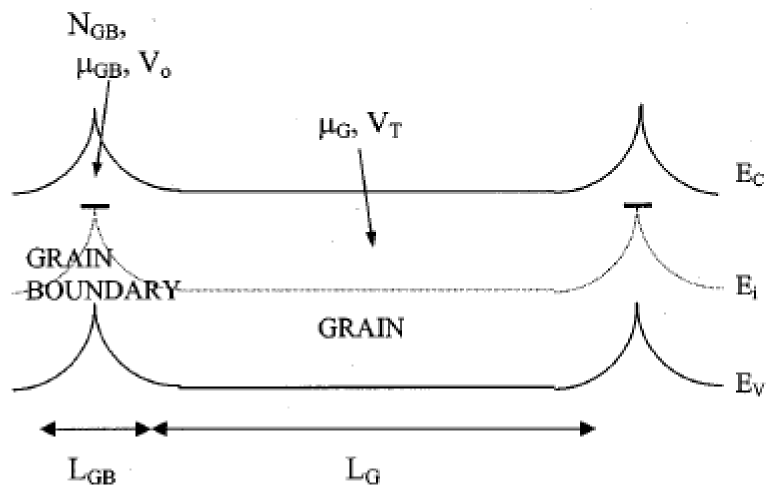

Fig. 2-2. Energy band diagram in the lateral direction along the channel of a n-channel polysilicon TFTs.

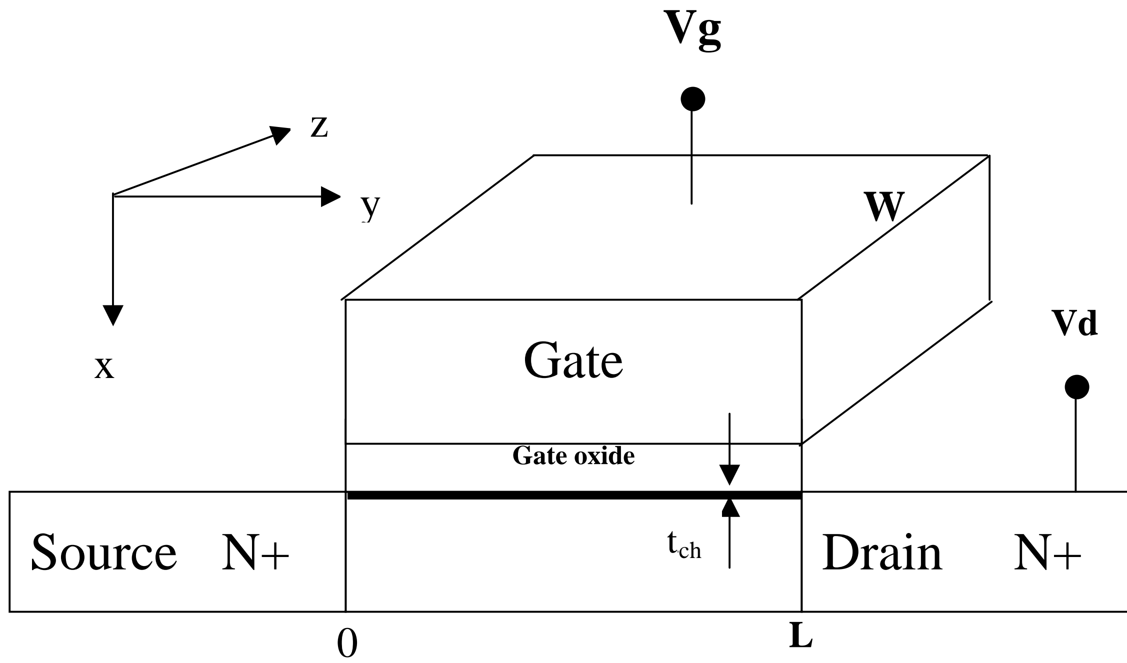

Fig. 2-3. A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

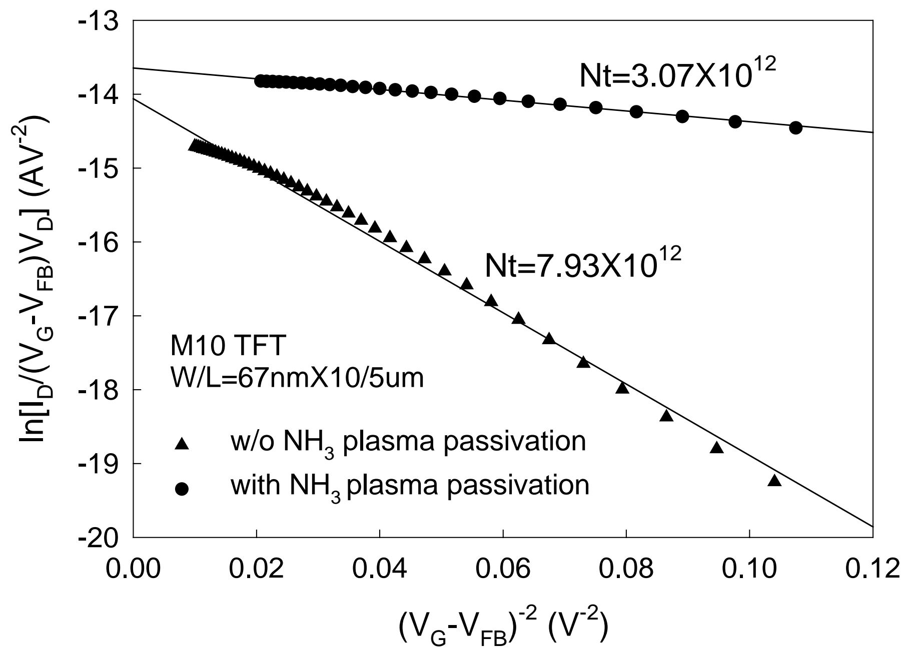

Fig. 2-4. Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

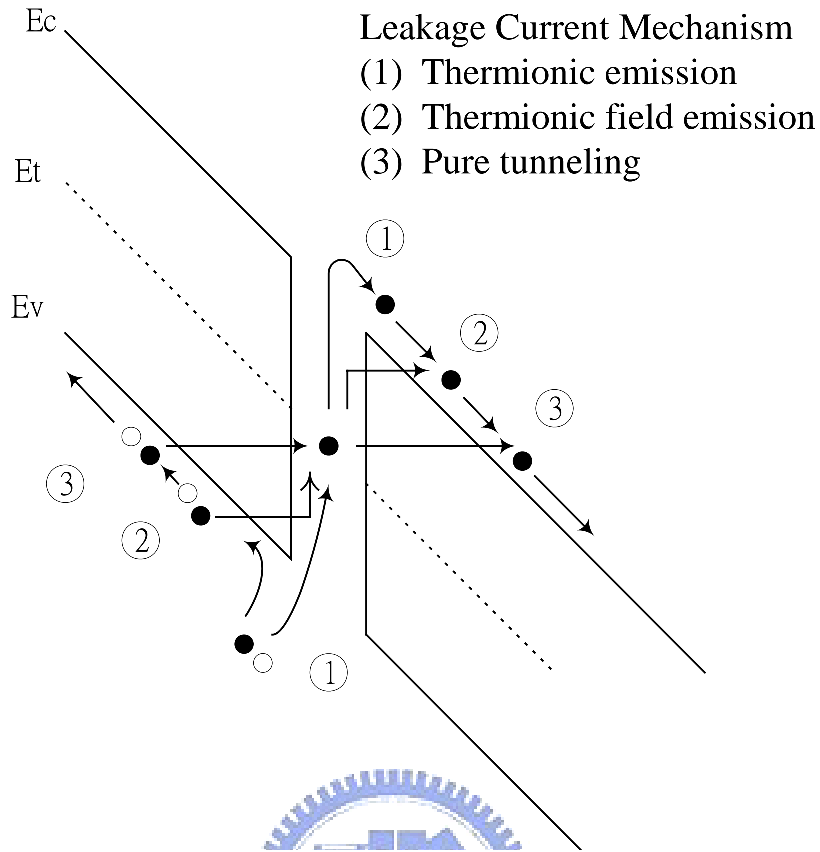

Fig. 2-5. Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling.

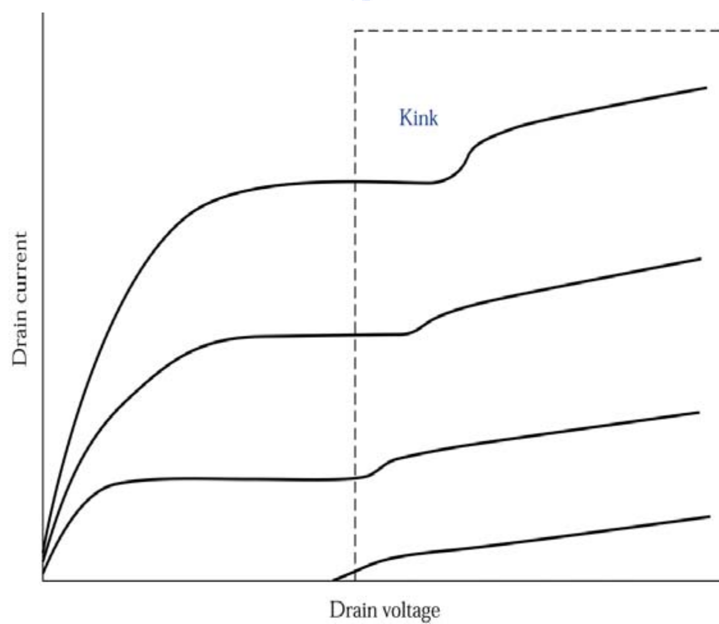

Fig. 2-6 The kink effect in the output characteristics of an *n*-channel SOI MOSFET.

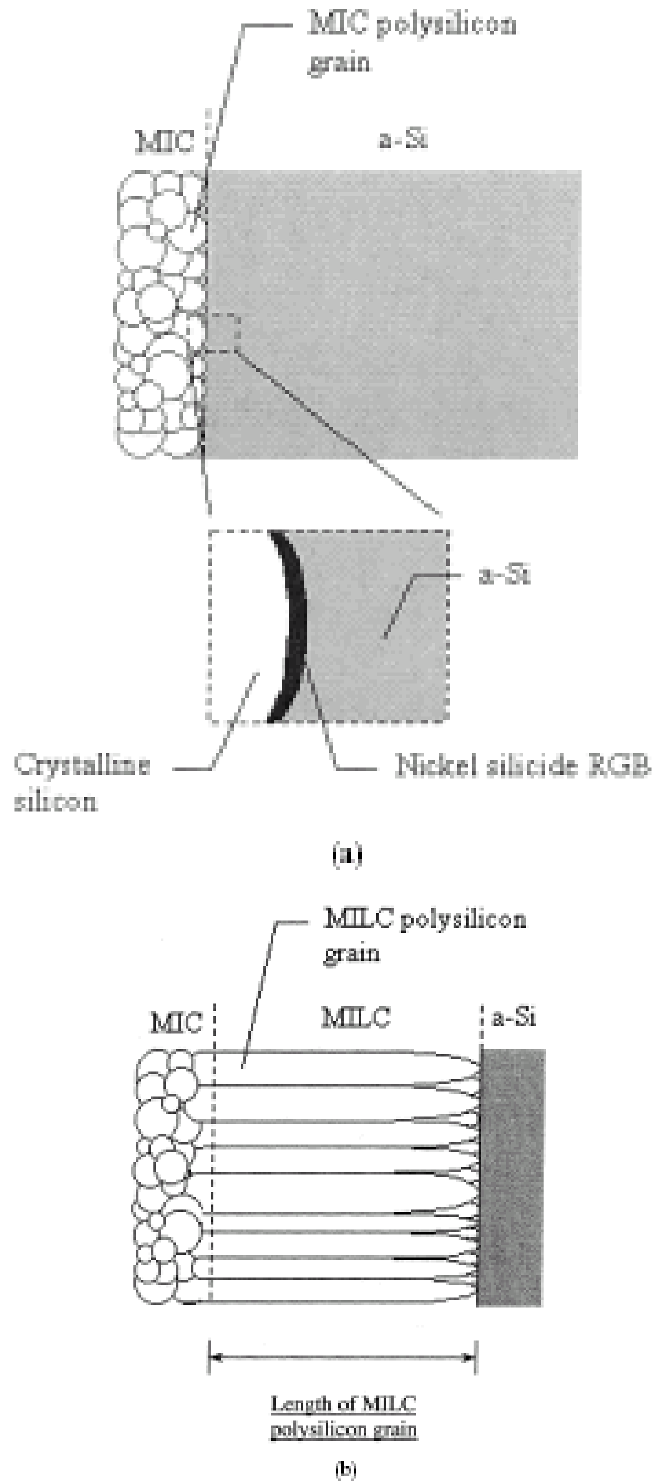

Fig. 2-7 MILC polysilicon formation during annealing process. (a) At the beginning of the annealing process, many nickel atoms are trapped and nickel silicide is formed at the grain boundaries of the MILC polysilicon region. Those nickel silicide grain boundaries at the MIC to a-Si interfaces, which are reactive regions, are responsible for MILC formation. (b) During the annealing process, the nickel silicide RGB absorbs silicon atoms from the a-Si region and rejects them to the MIC polycrystalline silicon region. As a result, the polysilicon grain grows up in lateral direction.

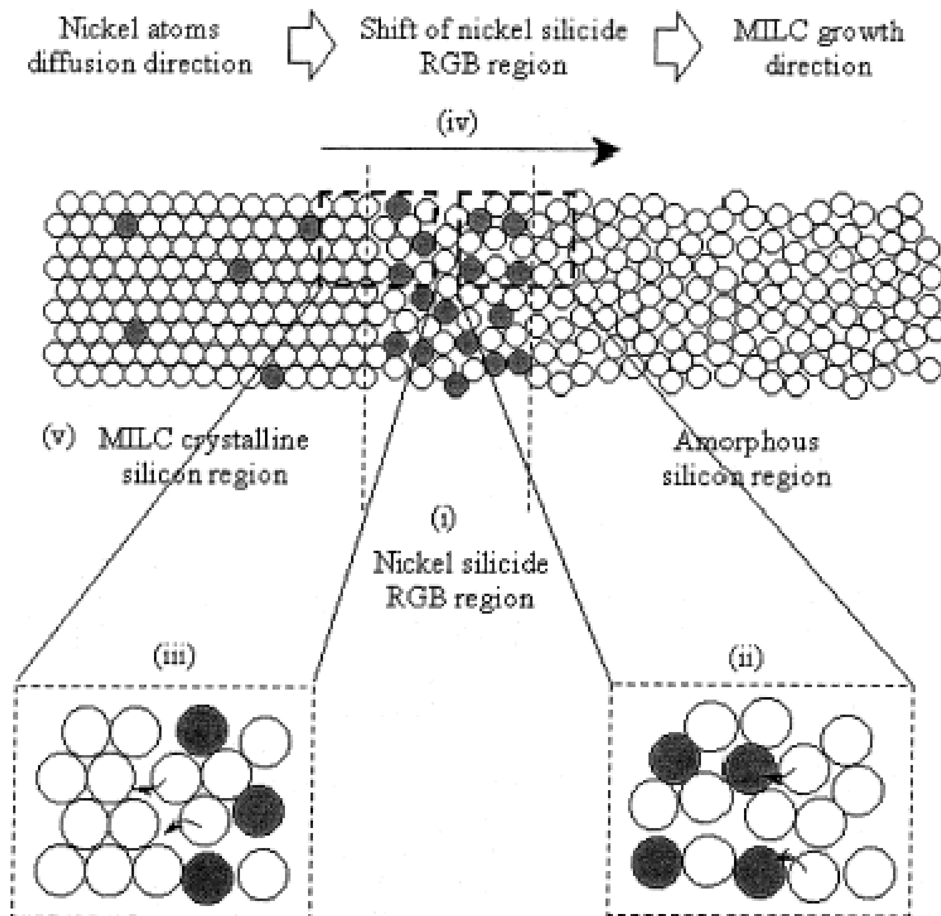

Fig. 2-8 MILC polysilicon formation mechanism. (i) Most of nickel atoms are trapped at the nickel silicide RGB, which is a layer between the amorphous silicon (a-Si) and MILC crystalline silicon regions. (ii) The nickel atoms in the nickel silicide RGB diffuse to the a-Si region and bonds with silicon atoms. The activation energy of the a-Si crystallization is lowered by the nickel impurities. (iii) The silicon atoms are dissociated from the nickel silicide RGB and then bond to the MILC crystalline silicon region. (iv) Nickel atoms diffuse to the a-Si region and crystallize the a-Si atoms continuously. This leads the shift of nickel silicide RGB and the growth of MILC polysilicon. (v) Only few nickel atoms are left and trapped inside the MILC silicon grain.

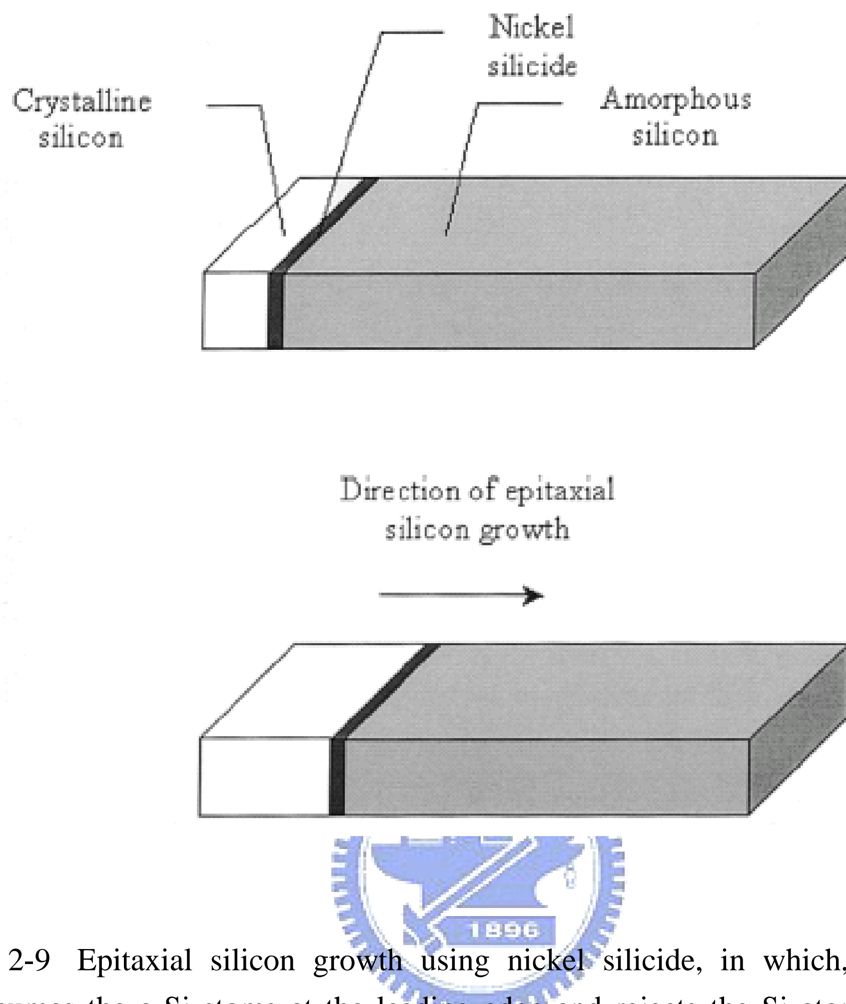

Fig. 2-9 Epitaxial silicon growth using nickel silicide, in which, the nickel silicide consumes the a-Si stoms at the leading edge and rejects the Si atoms to the crystalline silicon region.