國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

高頻被動元件在矽基板和多層介電質基板之模型與特性

The Characteristics and Models of High Frequency Passive Devices on Silicon and PCB Substrates

研 究 生 ：陳家忠

指導教授 ：荊鳳德 博士

中華民國九十五年五月

高頻被動元件在矽基板和多層介電質基板之模型與特性

研究生:陳家忠　　指導教授:荊鳳德教授

國立交通大學電子工程系電子研究所

摘要

隨著行動無線通訊系統需求日益增加，對高性能、低成本、低功率、以及小體積之射頻/微波電路之需要更顯得迫切。由於現今積體化之 CMOS 晶片不斷地微縮化，使得主動元件可震盪頻率不斷地提高，若再能結合高性能化的高頻被動元件，會使得 CMOS 矽製程儼然成為可應用於射頻/微波領域的半導體技術之一，故改善高頻被動元件特性為其研究之重點。

然而，CMOS 製程所使用之標準低阻值矽基板 (ρ ~10 Ω-cm) 而言，其上的傳輸線以及被動元件皆有著相當高的訊號損失。這些損失不但造成元件本身特性變差，更會破壞 CMOS 射頻/微波電路的效能。這些低性能的被動元件，正是目前 CMOS 射頻/微波電路最大的致命傷之一。因此，如何克服此問題，對未來 CMOS 射頻/微波電路的研究與發展將有著關鍵性的影響。

本論文中首先採用高阻值的矽基板，來降低其上元件之訊號在基板中的損耗，進而提升射頻/微波性能及改善 CMOS 射頻/微波電路系統之特性，並能使用 3D 之技術能來整合被動元件在同一晶片中，也是最終之目的。此外，也針對在多層介電板中之高頻被動元件，利用半導體之製程技術來改善其高頻特性，因為現今高頻被動元件都仍外掛於晶片外中在印刷電路板中，改善其元件效能，也

是本篇聚焦之貢獻。

本論文以射頻/微波電路中最常見之收發器 (transceiver) 電路出發，架構分別為:高頻被動元件在矽基板之研究；高頻被動元件在多層介電板之研究;傳輸線在晶片中損耗的影響；及結合 3D 技術整合微波被動元件四方面來探討。包括：共平面 (CoPlanar Waveguide， CPW) 傳輸線、 微波帶通 (band-pass); 分散式 (distributed) 濾波器，耦合器(Couplers)元件等等;最後亦探討了晶片內之傳輸和整合被動元件於晶片系統中。研究內容主要在於基板阻值對元件特性的影響，包括功率耗損、頻寬的延伸、能量的傳輸，和低耗損的共振。最後，仍朝著結合這些被動元件於收發器電路中，作出高性能高度整合之 CMOS 收發器為目標來邁進。

The Characteristics and Models of High Frequency Passive Devices on Silicon and PCB Substrates

Student: C. C. Chen **Advisor: Prof. Albert Chin**

Department of Electronics Engineering & Institute of Electronics National Chiao-Tung University

Abstract

As mobile microwave communication development increases, high performance, low-cost, low power, small size RF integrated circuits (RFICs) are required. This is because the maximum oscillation frequency increases as down-scaling CMOS technology (for 90 nm RF CMOS). However, transmission lines and passive circuit components on standard low-resistivity silicon substrates such as those used in CMOS processing have high power loss, which degrade the characteristics of devices and further damage the performance of CMOS RF/Microwave circuits. To overcome this problem, we have developed a method of high resisvity silicon substrate technology, which is capable of converting the standard low-resistivity Si to high-resistivity for large substrate loss improvement with full VLSI technology process compatibility.

In this work, we have applied the high-resistivity Silicon substrate to almost all of the passive components used in a common transceiver on Si, including: coplanar waveguide (CPW) transmission lines, resonators, microwave band-pass distributed

filters and couplers. In addition, the standard VLSI process is used to improve RF characteristics on high frequency printed circuit board (PCB) passive devices. The superior RF characteristics of extending bandwidth, lower insertion loss, and high coupling correspond with advanced wireless system demands. Hence, we have successfully demonstrated the excellent characteristics of RF passive devices on both silicon substrate and printed circuit board by decreasing power and coupling losses. Moreover, with the development of three dimensional technology, combing with interconnects and high resistivity substrate, these passive devices on standard VLSI process have been embedded into ICs. These device characteristics on silicon or PCB substrates, such as measured power loss, bandwidths, return loss, and insertion loss and coupling effect have presented in whole chapters. These enhanced RF performance methods on RF passive devices can contribute to applications in the advanced wireless systems.

ACKNOWLEDGMENTS

I would first like to thank my adviser Prof. Albert Chin for his illuminative suggestions and discussions during the period of my working toward PhD degree. His inspiration benefits me a lot on the creative ideas, effective schedule control and the integrity to the processing tasks. And I must say thanks to Prof. J. T. Kuo in Dept. of Communication Eng., National Chiao Tung University (NCTU), for the precious instructions and supports on the filters and couplers research.

I appreciate the financial and equipment supports from National Science Council (NSC 94-2215-E-009-062**)**, National Nano Device Lab. and Semiconductor Center of NCTU. I am also grateful to those who ever assisted this work: the crew of ED633 Lab. (especially to, H. L. Kao, B. F. Hung, C. H. Chen, C. H. Lai, and K. C. Chiang); Mr. Meshon Jiang at Dept. of Communication Eng., NCTU for the filter work.

Finally, much gratitude must be expressed to Dept. of Electronics Eng., NCTU, for the 4-year training, to my dear friends for the encouragement and to my family who always support me and give me all their love. This work can't be finished without them.

CONTENTS

FIGURE CAPTIONS

TABLE CAPTIONS

Table 3.2.1. Performance of the fabricated coupler at design frequency $f_O = 5$ GHz.

Table 4.2.1 Measured and simulated values of S_{21} and the Power loss at 20 GHz for various structures having 1 or 0.25 mm lengths. The spacing of the lines were 2 or 10 μm and the thicknesses of the oxide were 0.7 μm or 6 μm,. HRS: High resistance substrate. Decreasing the line length by 1/4 can reduce the unwanted S_{21} coupling by more than 10 dB and is much more effective than increasing line spacing by 5 times from 2 μm to 10 μm.

Chapter 1

INTRODUCTION

1.1 Si Substrate for RF CMOS Technology

Millimeter-wave frequencies are being proposed for high-volume low-cost/ small size/ mass commercial communication applications. These applications include sensors for vehicle monitoring and control, local radio area networks (LAN's), secure cellular-radio systems and short-range wide-band radio. To achieve low cost with moderate-to-high-volume circuit production, monolithic circuitry is preferred. At microwave frequencies monolithic microwave integrated circuit (MMIC's) employ GaAs technology with integrated active devices. However, GaAs real estate is expensive, especially when passive devices occupying large areas are required, e.g., filters, couplers, diplexers, and antennas, etc.

A number of alternative substrates can be considered for planar millimeter-wave circuits or interconnect designs. Silicon technology is expected to be an effective strategy instead of GaAs. However, RF CMOS circuits suffer from serious power losses when considering some performance parameters such as

substrate and power losses. Besides, significant coupling effects may occur between parallel conductive lines or nearby devices due to the low substrate resistivity. The large RF signal leakage may damage the circuit performance through the parasitic capacitance of the conductive substrate. These drawbacks definitely increase the difficulties in designing Si CMOS RFICs and also limit the expansion of CMOS circuits for RF applications [1.1.1].

In order to overcome these problems, several methods have been explored, including: using high resistivity silicon [1.1.2], sapphire [1.1.3], silicon-on-insulator (SOI) wafers [1.1.4], thick oxide isolation layers, micromachined structures [1.1.5]-[1.1.6], silicon-metal-polymide (SIMPOL) structures [1.1.7] and porous Si [1.1.8]. The cost of Sapphire is expensive [1.1.9] and processes variations are difficult to control. The isolation for RF crosstalk on SOI and thick oxide isolation layer are constrained by process limitations, and becomes worse especially at higher frequencies. Micromachined, SIMPOL structures and porous Si suffer from incompatibility with CMOS processes. The high process costs and difficulties of integration with modern VLSI technology are serious drawbacks of these methods.

In order to overcome this technological challenge, we have used high resistivity silicon substrates to selectively convert the standard Si (10 Ω-cm) to high resistivity substrates with full current VLSI technology process. The major advantage of the high

resistivity silicon substrates is its simplicity and low cost. And, it has been reported that transmission lines on silicon substrate material have acceptable RF losses even in the microwave-frequency regime.

Based on this technology, we demonstrated the effectiveness of the high resistivity silicon substrates for reducing RF substrate loss in the Si passive devices, such as CoPlanar Waveguide (CPW) transmission lines, couplers, distributed broad-band band-pass filters, which are very important components for fully integrated Si RF transceivers. The novelty of using VLSI backend interconnect with high resistivity substrate also provides an attractive solution for RF passive devices embedded into low-cost high-performance wireless systems.

1.2 PCB Substrate for High-Speed circuit

1.2.1 Printed Circuit Board Substrate

The printed circuit board (PCB) used to physically mount and connect the circuit components in a high frequency product will have a significant impact on the performance of that product [1.2.1]. The potential magnitude of the effect of the PCB design increases with frequency as the parasitic elements tend to a similar magnitude to the typical lumped components used [1.2.2]. This leads to the requirement for increased inclusion of electrical models representing PCB structures into the circuit simulation. In practical radio products the requirements on the PCB design can sometimes be in conflict with 'best manufacturing' practice. In order to achieve the most optimum solution in all respects the radio designer, the PCB designer and the manufacturing engineer must all have some appreciation of each others requirements [1.2.3]. The most common processes used in the fabrication of PCBs are drilling, plating, bonding and etching [1.2.4]. Some new developments are underway where lasers are utilized to distinguish conducts. The principle advantage of this development has the ability to use smaller dimensioned features including track widths down to 0.05 mm. In all the lowest cost radio products multilayer PCBs are used and these comprise of a number of laminates of boards individually etched and bonded, the principle advantages of this having the ability to use more than two

conductor layers reducing the required board space. Also, the type of via structure used will have a major effect on the processes required to fabricate the PCB and consequently the cost of the finished board [1.2.5]-[1.2.6].

1.2.2 PCB Process Limitation

In order to design a product using a PCB, it is important to understand the practical limitations of the fabrication process [1.2.7]. The manufacturing processes were used to etch the tracks, drill the holes and assemble the laminates have limitations. Exceeding these limitations will significantly increase the cost of the PCB as manufacturing yields reduce. The typical minimum limit on track thickness for a high volume, complex product is around 0.2 mm. A similar minimum limitation applies to the minimum gap between two different conducts. Some PCB manufacturers offer to etch track widths down to 0.125 mm. The minimum via hole size was used that can be drilled as a stack. It will have a significant effect on the cost of the board as the via hole size limits the number of PCBs. Not withstanding the radio performance implications of small diameter via holes, typical minimum sizes of 0.25 mm are commonly used.

In this paper, we present that the improved process flow to product the good performance on printed circuit board by lithography technology on VLSI. It can fabricate the passive devices without the problems of via-hole and designing. The

scaling gap-spacing and conductor width can help the designers to design wider range and product better RF characteristics. The original process limitation to product devices on PCB can be solved.

1.3 Backend Interconnect and Integrated with 3D

The strong demand on advanced wireless communication services for advanced system-on-a-chips has attracted a great deal of attention [1.3.1]. This is due to their significant benefits such as overall chip size reduction, lower fabrication cost, as well as enhanced system performance. Meanwhile, significant progress in advanced VLSI technology has made it possible to realize system-on-a-chip at millimeter-wave frequencies with three-dimensional technology [1.3.2]. The concept of integrating parallel coupled-line filters with CMOS integrated circuit on silicon (Si) substrate is appealing because shorter coupling-line has shown on backend local or globe interconnects with CMOS scaling down. This requirement becomes even more urgent as the operation frequency of Si communication integrated circuits (ICs) increases. However, the performance of microwave filters integrated on Si suffers from the high frequency losses and crosstalk of the low resistivity Si substrate. For local lines (especially in array structures such as cache RAMs) a key limitation is cross-talk. Cross-talk will progressively become worse in the future because of the increasing coupling capacitance among neighboring lines. Therefore, we study the test structure of coupled-line interconnect in ULSIs for measuring and characterizing of multi-layered interconnect capacitance. With the high resistivity silicon substrate, the substrate coupling successfully can be reduced; therefore, improving the RF

characteristics, the superior performance of the passive devices can be used as advanced millimeter-wave wireless communication systems.

Chapter 2

Transmission Lines and Ring Resonators

2.1 Bulk and Thin-Film Microstrip Transmission Lines on VLSI-Standard Si Substrates

2.1.1 Motivation

Scaling of Si device technology into the nm-scale regime yields Si transistors with performance reaching into the sub-THz range [2.1.1]. However, the performance of MMICs on Si substrates is inferior to those on semi-insulating GaAs (~107 Ω-cm) owing to the large loss of passive devices on the low resistivity Si (10 Ω-cm) substrates [2.1.2]-[2.1.3]. To overcome this problem, we have previously proposed and demonstrated a method to reduce the large RF loss in standard Si substrates using ion implantation which can selectively form high resistivity (106 Ω-cm) regions in VLSI-standard Si substrates (10 Ω-cm) [2.1.4]-[2.1.7]. Excellent coplanar waveguide (CPW) transmission lines with only 0.6 dB loss at 110 GHz [2.1.8] as well as

CPW-based broadband filters with small insertion loss (1.6 dB) and 10 GHz bandwidth at 91 GHz [2.1.9]- [2.1.10] have been demonstrated using this technique. In this section, we have successfully demonstrated high performance microstrip lines on Si substrates. Using ion implantation of proton, the power loss of the microstrip transmission line was reduced significantly from 6.7 dB/mm to only 0.4 dB/mm at 50 GHz. In addition, we have also fabricated thin-film microstrip transmission lines using current VLSI backend interconnect processes with a loss of ~0.9 dB/mm at 20 GHz. This approach has the inherit merit of being fully compatible with current VLSI technology without requiring additional masks or process steps.

2.1.2 Design Process

Standard 10 Ω-cm resistivity Si wafers with 200 μm thickness were used in this study. Bulk microstrip transmission lines were fabricated on 1.5-μm-SiO_2/Si substrates using 4 μm thick Al with 3 mm long and 60 μm wide. Thick Al was deposited on the backside of the wafer to form the bulk microstrip transmission line. For thin-film microstrip transmission lines, a 0.75 mm length and 20 μm width strip was formed using the top metal layer (metal-6) of a conventional VLSI backend process with the first metal layer used as the ground plane. Two-port S-parameters were measured up to 50 GHz using an HP8510C network analyzer.

2.1.3 Bulk Microstrip Lines on Si

Figure 2.1.1 shows the power loss for a 3 mm long microstrip line on 1.5 μm SiO_2-isolated Si, where the loss increases from 2.8 dB/mm to 6.7 dB/mm as the frequency increases to 50 GHz. This loss is greater than that of the CPW transmission line, as shown in Figure 2.1.1, over the same frequency range. The larger loss in the microstrip transmission line than in the CPW line is due to the vertical EM field being fully inside the lossy Si substrate, whereas the horizontal EM field in CPW line is only partially within the Si substrate.

The increasing power loss at high frequency is an issue for Si RF IC technology since future wireless communications require higher frequencies and bandwidths. As shown in Figure 2.1.1, our microstrip transmission lines with proton implantation show an improved power loss of ≤ 0.4 dB/mm at 50 GHz. This value is similar to that of CPW transmission lines with the same ion implantation [6, 8] and comparable to the loss in semi-insulating GaAs obtained from EM simulation using IE3D.

2.1.4 Thin-film Microstrip Lines on Si

Using the same approach of forming a high resistivity layer by proton implantation, we have also designed and fabricated thin-film microstrip transmission lines. The isolation layer is from the multiple layers of SiO_2 used in the VLSI backend process. Figure 2.1.2 shows the measured and EM-simulated power loss. As can be

seen, the power loss is ~0.9 dB/mm at 20 GHz which is much lower than that of the un-implanted bulk CPW and microstrip lines shown in Figure 1. Although the loss of thin-film microstrip line at 20 GHz is larger than the 0.25 dB/mm in ion-implanted bulk microstrip lines, this process used simple layout technology without adding additional mask and process.

Because the transmission line is a passive device, the RF loss (L) is equivalent to the generated noise with equivalent noise temperature by $(L-1)T_0$. The noise from advanced 0.18 and 0.13 μm MOSFETs is ~2.5 dB at 20 GHz, whereas the un-implanted CPW and microstrip transmission lines typically show larger noise and would dominate the overall noise floor of an RF system. However, the noise floor can be significantly reduced by using the thin-film microstrip line, even for a length as long as 1 mm. Further improvement may be possible by improving the dielectric loss of the low-temperature-formed SiO_2 or by increasing the thickness of the dielectric layer. This will be possible using the advanced 1-poly-9-metal layer (1P-9M) process of the 90 nm technology node and beyond. This will further reduce the performance gap with the bulk microstrip transmission line using proton implantation or that on GaAs, with the inherit merit of only changing the layout of current VLSI.

2.1.5 CONCLUSION

We have achieved extremely low power loss for both bulk (0.4 dB/mm at 50

GHz) and thin-film (0.9 dB/mm at 20 GHz) microstrip transmission lines on VLSI-standard Si substrates. Proton implantation selectively transforms the low resistivity Si substrates of bulk microstrip transmission line into a high resistivity state. The high performance of thin-film microstrip line results from the high-resistivity SiO_2-dielectric being inside the microstrip line body. Both transmission lines can be integrated into RF circuits and distributed devices at a reduced size compared with using CPW lines.

2.2 CPW and Microstrip Ring Resonators on Silicon Substrates

2.2.1 Motivation

Integrated ring resonators are desirable due to their compact size, low cost, and easy fabrication. Owing to the narrow passband bandwidth and low radiation loss, ring resonators have been applied to band-pass filters, oscillators, mixers, and antennas [2.2.1]-[2.2.3]. Integrating a ring resonator in a CMOS circuit, on a Si substrate has advantages in producing low-cost and compact MMICs. However, the most difficult challenge in integrating such resonators is the large substrate loss from the low resistivity Si. To overcome this problem, high-resistivity Si [2.1.4] and MEMS [2.1.5] technology have been developed. Previously, we proposed an alternative method to reduce the large RF loss from standard Si substrates using simple ion implantation, which can selectively translate the VLSI-standard Si substrates (10 Ω–cm) into high resistivity material (10^6 Ω–cm) [2.1.6]-[2.1.10]. Excellent RF passive devices such as inductors, transmission lines, filters, and antennas have been integrated into CMOS-based Si technology. In this section, we have successfully implemented high performance 40-GHz coplanar and 30-GHz microstrip ring resonators into Si technology using ion implantation. The resonators on conventional Si, without implantation, show large insertion loss from the substrate.

This is the first successful demonstration of integrated mm-wave ring resonators on Si with a process employing a VLSI-compatible technology.

2.2.2 Design Process

The ring resonators were designed using IE3D employing coplanar waveguide (CPW) and microstrip structures with 50-Ω input impedances. The CPW structure is widely used in Si RF ICs technology because of its lower loss than microstrip type structures. VLSI-standard Si wafers with typical 10 Ω-cm resistivity were used in this study. The substrate thickness was 525 μm or 200 μm for CPW or microstrip type resonators, respectively. To reduce the RF loss from the low resistive Si substrate, a 1.5 μm SiO_2 layer from the VLSI backend process was first deposited. The ring resonators were fabricated on SiO_2/Si substrates using 4 μm thick Al and standard VLSI processing for patterning. The coplanar coupled lines were laid out to form resonators, with the length (λ/2) of the coplanar resonator being dependent on the resonant frequency. For microstrip-type resonators, 2 μm Al was also deposited on the backside of the 200 μm thick Si, as the ground plane. Figures 2.1.2 (a) and (b) are the images of the fabricated CPW and microstrip ring resonators designed at 40 GHz and 30 GHz, respectively. After ring resonator device fabrication, ion implantation of protons was applied to reduce the RF substrate loss. The device RF characteristics

were measured using an HP 8510C Network Analyzer and a probe station to 50 GHz.

2.2.3 Experimental Results

Figures 2.2.1 (a) and (b) present the RF characteristics of CPW ring resonators on VLSI-standard oxide-isolated Si, with and without the ion implantation respectively. For comparison, the IE3D-designed characteristics are also shown in Figure 2(a). The implanted ring resonator has excellent RF performance, with only –1.35 dB S_{21} insertion loss at the peak transmission of 39.2 GHz and a broad ~13 GHz bandwidth. The small insertion loss is due to the large surrounding stubs being close to the ring that enhance the coupling efficiency. The measured transmission and bandwidth are close to the ring resonator simulation, using IE3D, for an ideal lossless Si substrate. This is the first report of high performance ring resonators on Si substrates at mm-wave regime. The merit of this ion implantation method is the simple process and it being compatible with current VLSI technology. In contrast, the ring resonator device on the same 1.5-μm isolated Si substrate, without ion implantation, shows much worse insertion loss of 15-20 dB over the whole frequency range. Such high loss and poor resonator performance makes the devices unusable.

Figures 2.2.3 (a) and (b) present the RF characteristics of the microstrip ring resonators, shown in Figure 2.2.1 (b), on conventional oxide-isolated Si, with and

without the ion implantation respectively. For comparison, the EM- designed characteristics from an IE3D simulation are also plotted in Figure 3(a). For the ring resonator with ion implantation, good RF performance is achieved with only –3.37 dB S_{21} insertion loss at the peak transmission of 28.3 GHz and a broad ~6 GHz bandwidth. This successful microstrip type ring resonator on Si is much more difficult to achieve than the CPW resonator because of the EM field being fully inside the lossy Si substrate. In contrast, the un-implanted microstrip ring resonators show large ~40 dB insertion loss, which prohibits their integration into any RF circuit.

2.3 Modeling and Mechanisms

2.3.1 Analysis from Modeling

We use the physically-based equivalent circuit model shown in Figure 2.3.1 to simulate the S-parameters. Lt and Rt are the series inductor and parasitic resistor from the long microstrip transmission line body, respectively. The symmetrical Rs and Cs at the input and output ports represent the RF signal loss to the ground plane, which should be large for the bulk microstrip line formed on VLSI-standard low resistivity Si substrate (10 Ω-cm) without ion implantation.

The measured and simulated S-parameters of the bulk and thin-film microstrip transmission lines, with or without implantation, are shown in Figure 2.3.2 (a) and Figure 2.3.2 (b). Good agreement is obtained between the measured and modeled S-parameters, suggesting that the equivalent circuit model in Figure 2.3.3 is appropriated.

The extracted substrate impedances, deduced from the Rs-Cs sub-circuits for both bulk and thin-film microstrip transmission lines, are shown in Figure 2.3.3. For the bulk microstrip lines on standard Si, the proton implantation can increase the substrate impedance by more than one order of magnitude. For the thin-film microstrip lines, the relatively high substrate impedance arises from the high resistivity SiO_2 dielectric inside the microstrip line body.

We have also used a physically-based equivalent circuit model, shown in Figure 2.3.4 to simulate the RF characteristics of the ring resonator. The shunt Rs and Cs sub-circuits simulate the substrate loss, and Cox is the parasitic oxide capacitor underneath the resonator of the 1.5 μm SiO_2 on the Si substrate. The capacitor C1 represents the gap-coupling capacitor, while the series L and R are the parasitic inductor and resistor from the ring and coupling metal stub. The series LC forms the resonator realized by these coupling lines and the ring body. Figure 2.3.4 shows the equivalent circuit simulated and measured RF characteristics of both the CPW and microstrip ring resonators with ion implantation. Excellent agreement between the measured and simulated S-parameters, shown in Figure 2.3.2 for both CPW and microstrip resonators, was achieved. This indicates the accuracy of the equivalent circuit model. Similar good matching between circuit-simulated and measured S-parameters was also obtained for the resonators without proton implantation in Figure 2.3.2 (b) and Figure 2.3.3 (b). Thus the equivalent circuit can be used to extract the substrate loss from Rs-Cs sub-circuits.

The extracted substrate impedance from the Rs-Cs sub-circuits is shown in Figure 2.3.5. Proton implantation increases the substrate impedances by more than an order of magnitude. The decreasing substrate impedance with increasing frequency is due to the effect of shunt capacitance to ground, which is also consistent with the

higher loss at higher frequency of the transmission line and filter loss in our previous publications.

2.4 Conclusions

We have achieved extremely low power loss for both bulk (0.4 dB/mm at 50 GHz) and thin-film (0.9 dB/mm at 20 GHz) microstrip transmission lines on VLSI-standard Si substrates and fabricated CPW and microstrip ring resonators on Si substrates with good RF performance at ~40 and ~30 GHz, was close to that for ideal IE3D-designed resonators. Proton implantation selectively transforms the low resistivity Si substrates of bulk microstrip transmission line into a high resistivity state. The high performance of thin-film microstrip line results from the high-resistivity SiO_2-dielectric being inside the microstrip line body. Both transmission lines can be integrated into RF circuits and distributed devices at a reduced size compared with using CPW lines. Without implantation such resonators have worse insertion and reflection loss and completely fail. By using equivalent circuit models and EM simulation we conclude that the substrate impedances are the major cause of the poor RF performance.

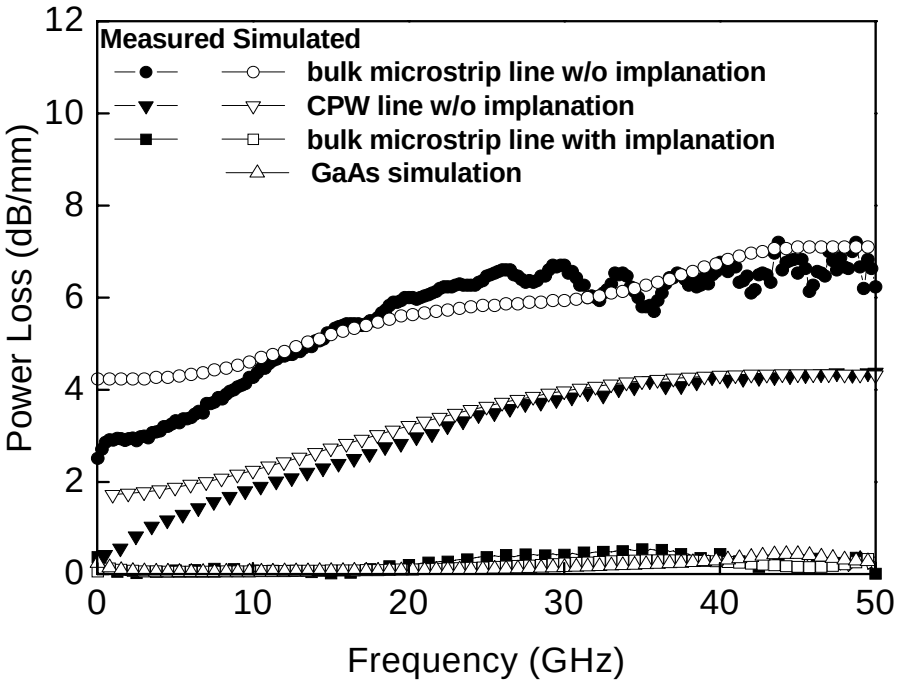


Fig. 2.1.1 The measured and EM-simulated power loss of 3 mm long bulk microstrip transmission lines. For comparison, results for a 1 mm long CPW line are included. Implantation produces a large loss reduction, from 6.7 dB/mm to 0.4 dB/mm at 50 GHz.

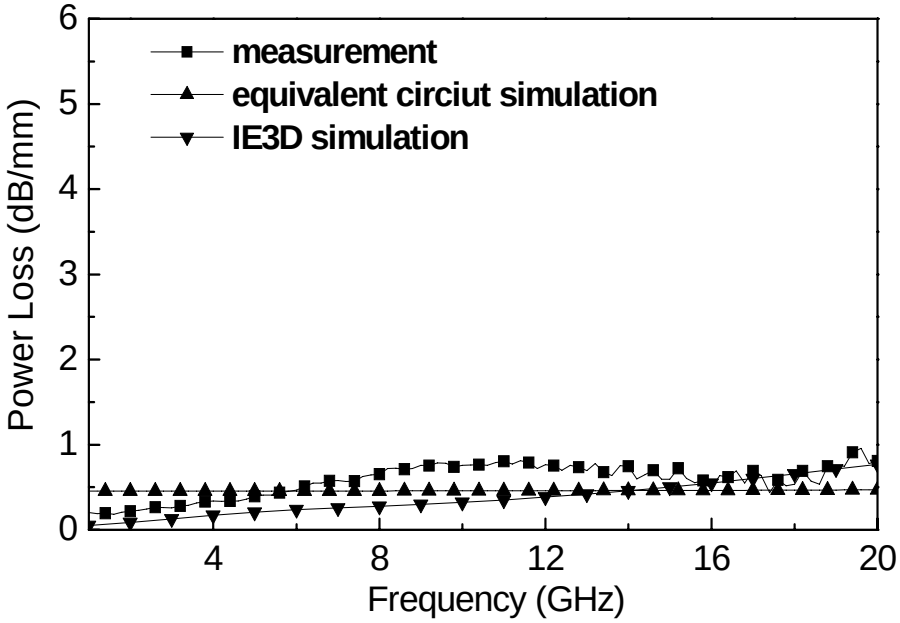
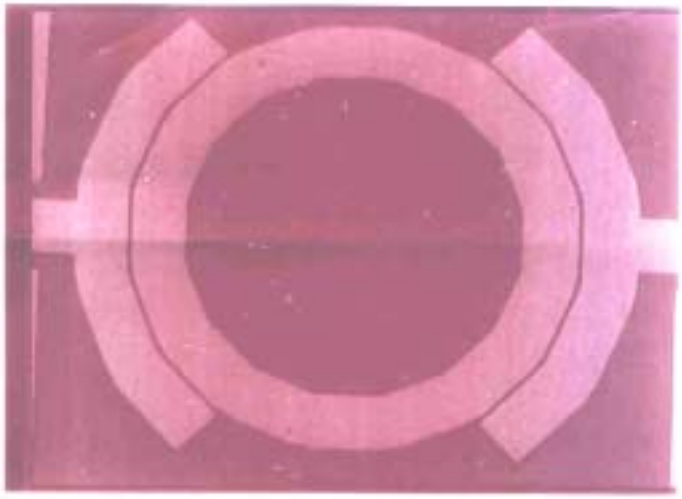
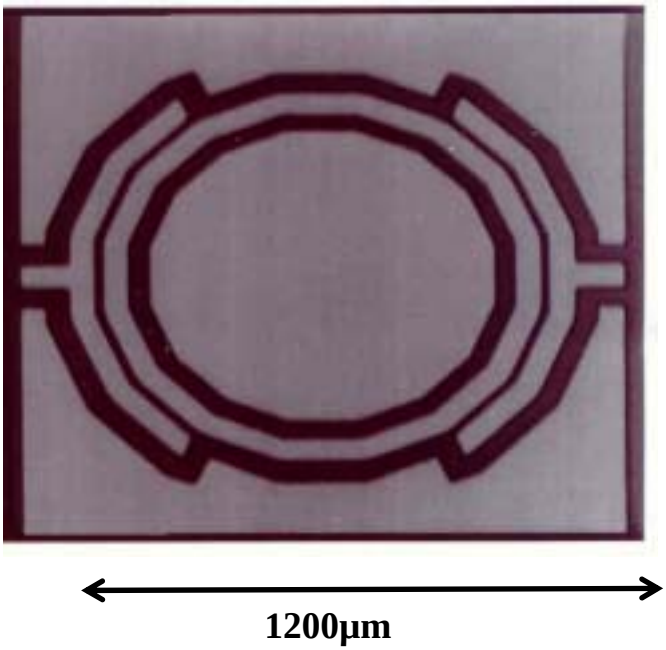


Fig. 2.1.2 The measured and EM-simulated power loss of 0.75 mm long thin-film microstrip transmission lines. The measured loss at 20 GHz is < 1 dB/mm, i.e. much lower than the bulk CPW (3 dB/mm) and microstrip lines (6 dB/mm) in Figure 1 without implantation.

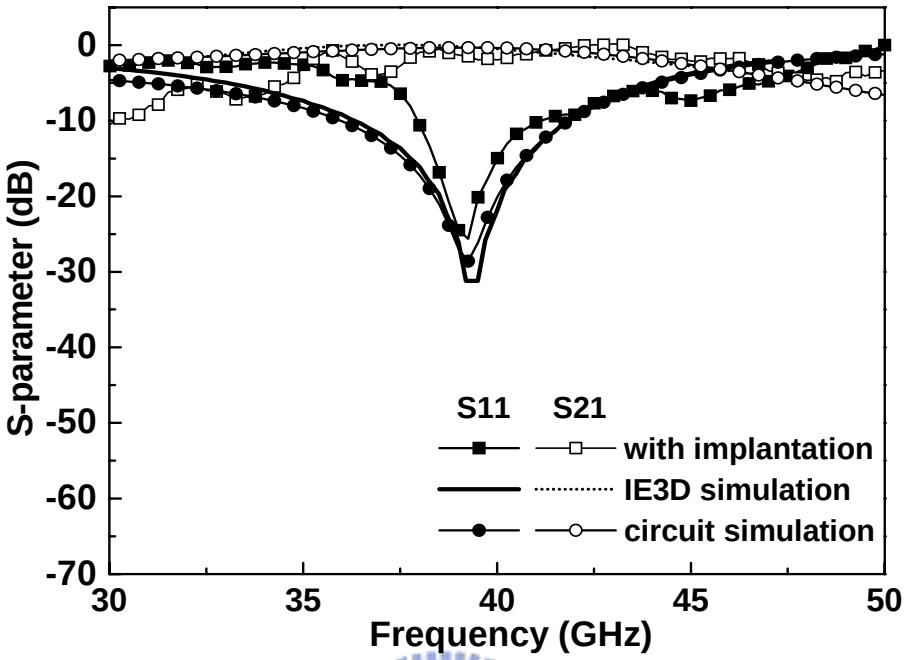


(a)

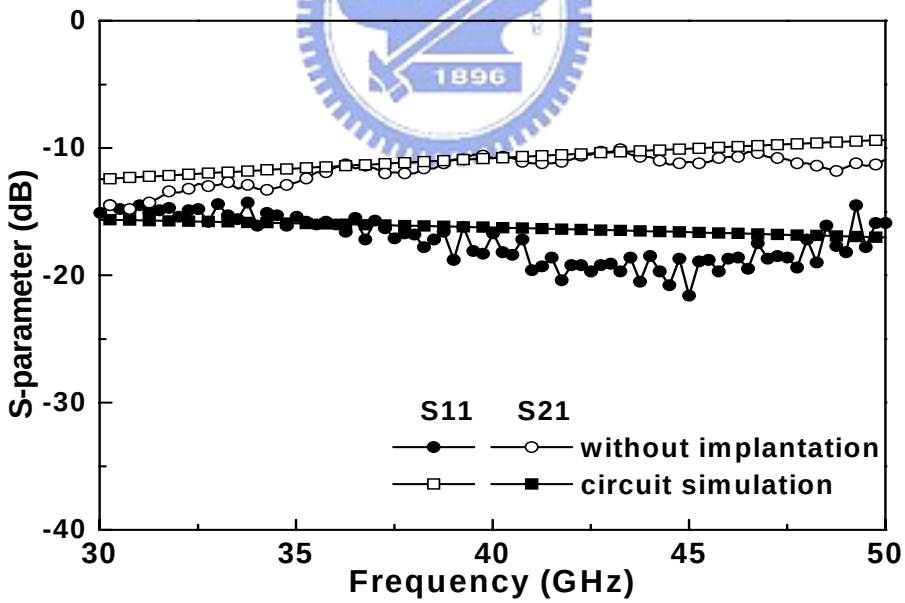


(b)

Fig. 2.2.1Images of fabricated (a) CPW and (b) microstrip ring resonators designed at 40 GHz and 30 GHz, respectively. The long surrounded stubs near the ring are to enhance the coupling efficiency.

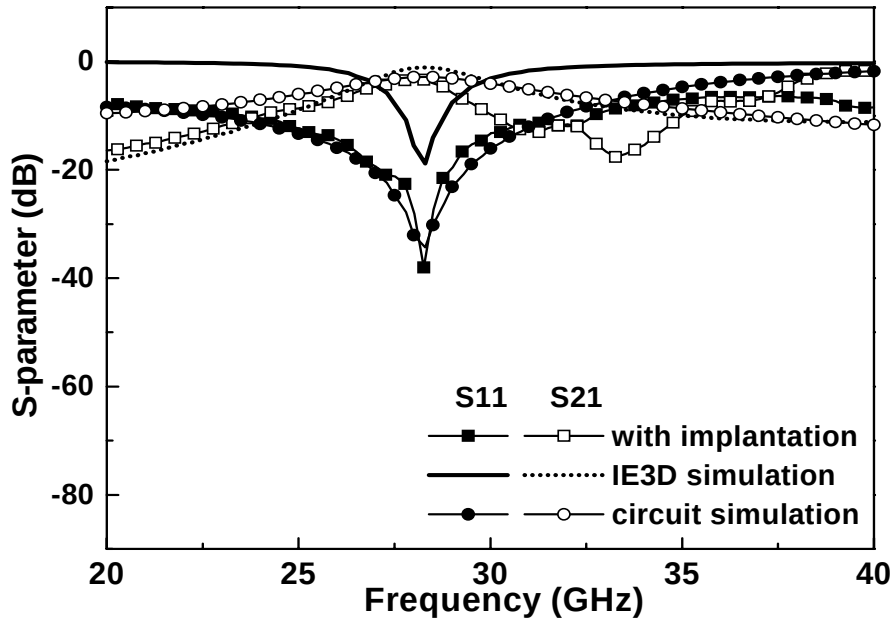


(a)

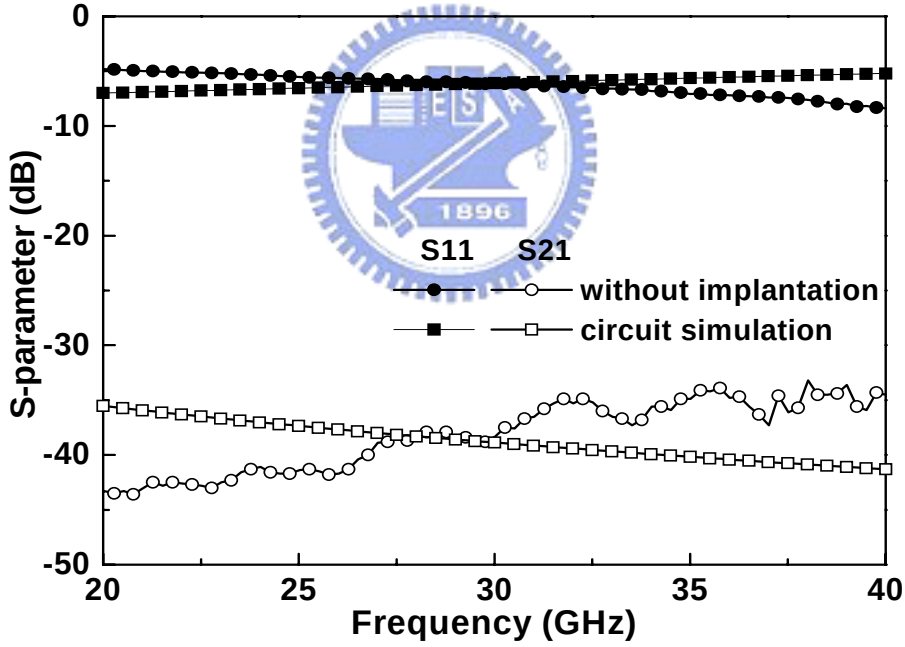


(b)

Fig. 2.2.2 The measured S-parameters of CPW ring resonators (a) with and (b) without proton implantation. The EM and circuit simulated filter characteristics are shown for reference.



(a)



(b)

Fig. 2.2.3 The measured S-parameters of 30 GHz microstrip line ring resonators (a) with and (b) without proton implantation. The EM-simulated and the equivalent circuit simulated filter characteristics are also shown for reference. No resonance is observed in (b) due to the substrate loss of ~40 dB.

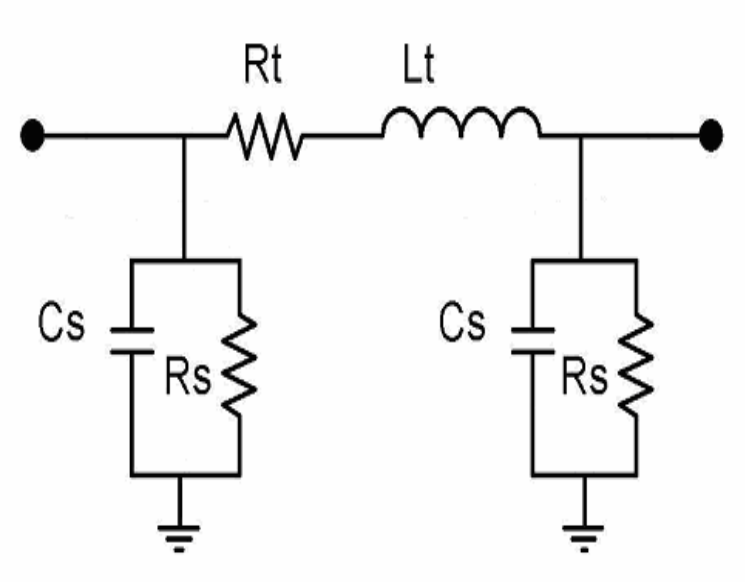
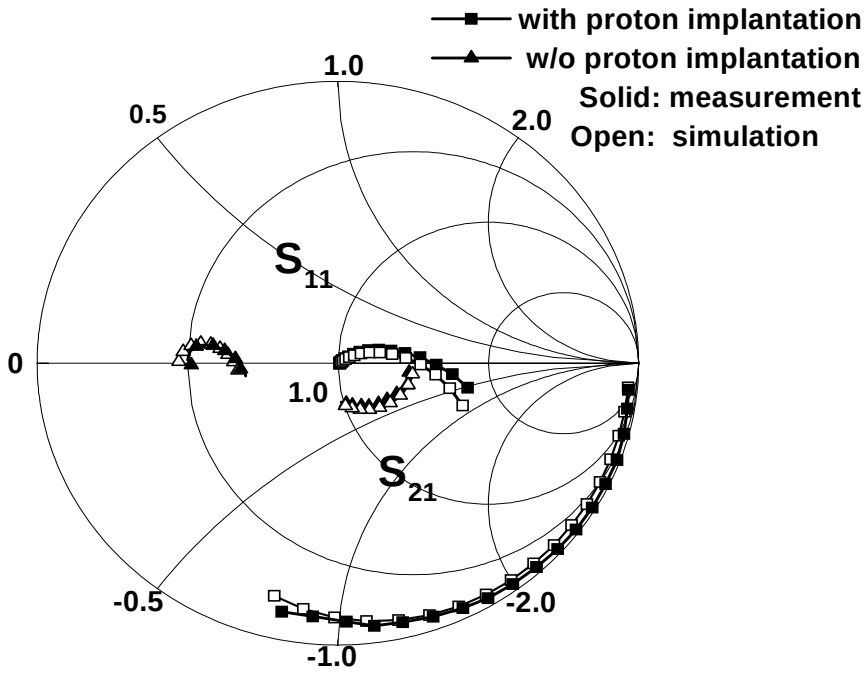
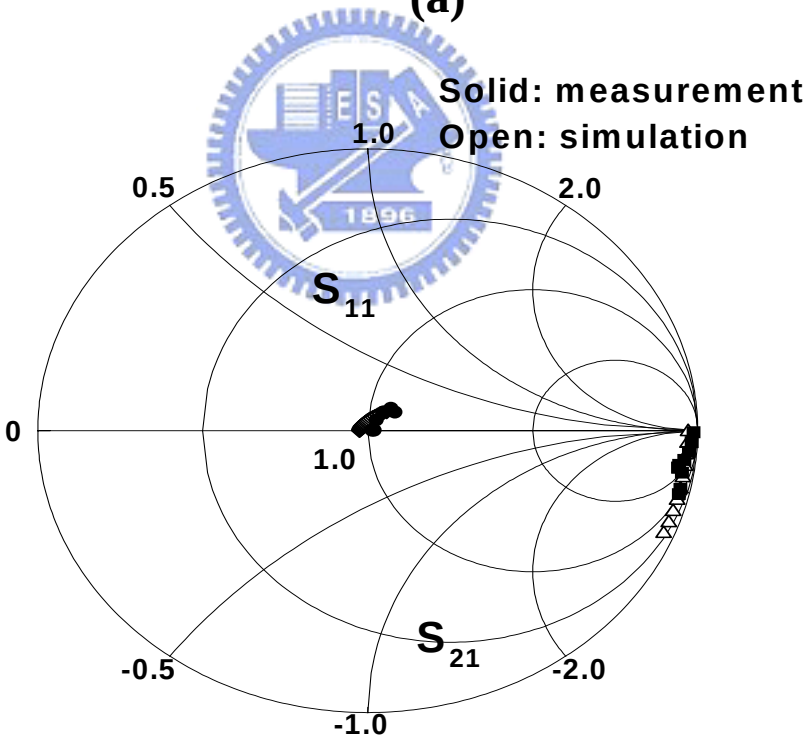


Fig. 2.3.1 The physically-based equivalent circuit for the microstrip transmission lines. The Lt represents the line inductor, and Rt the parasitic resistor of the transmission line. The substrate loss is modeled by the shunt Rs and Cs to ground.



(a)



(b)

Fig. 2.3.2 The measured and equivalent-circuit modeled S-parameters of (a) bulk and (b) thin-film microstrip transmission lines on Si substrates. The effect of proton implantation is shown in (a). The different curve lengths are due to different frequency ranges: 50 GHz in (a) and 20 GHz in (b).

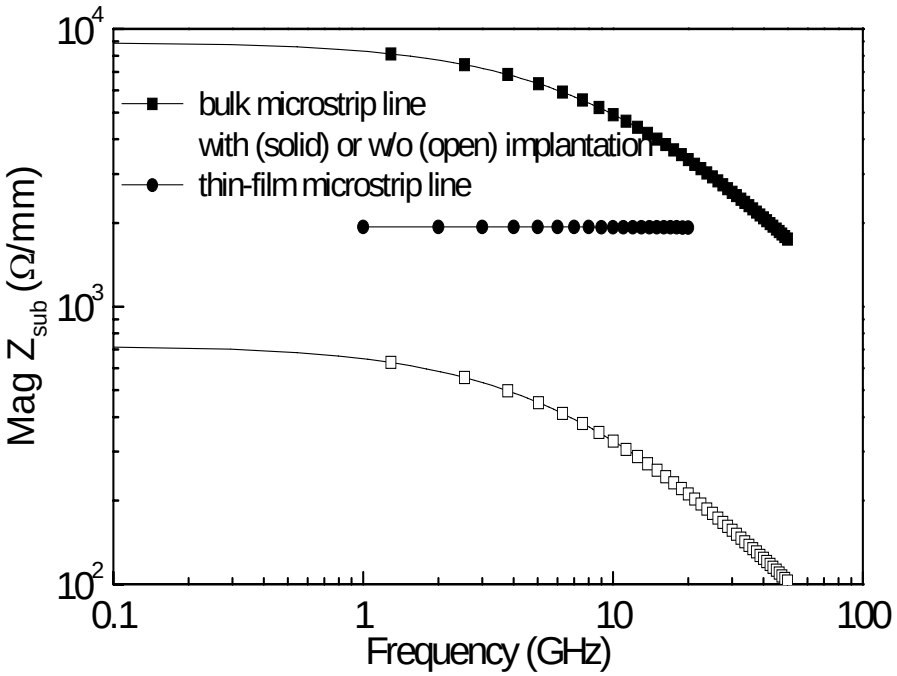


Fig. 2.3.3 The extracted magnitude of the substrate-impedance/mm derived from the bulk and thin-film microstrip transmission lines. The effect of proton implantation is to increase the substrate impedance and thus reduce the loss of the bulk microstrip transmission line.

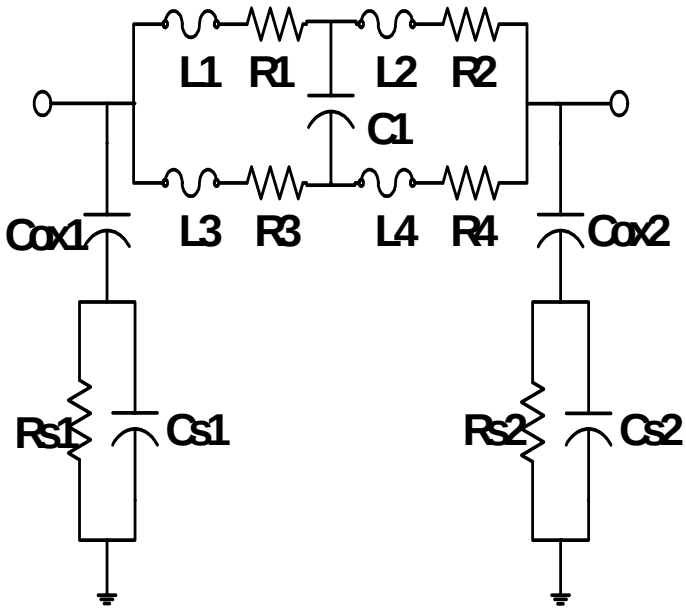
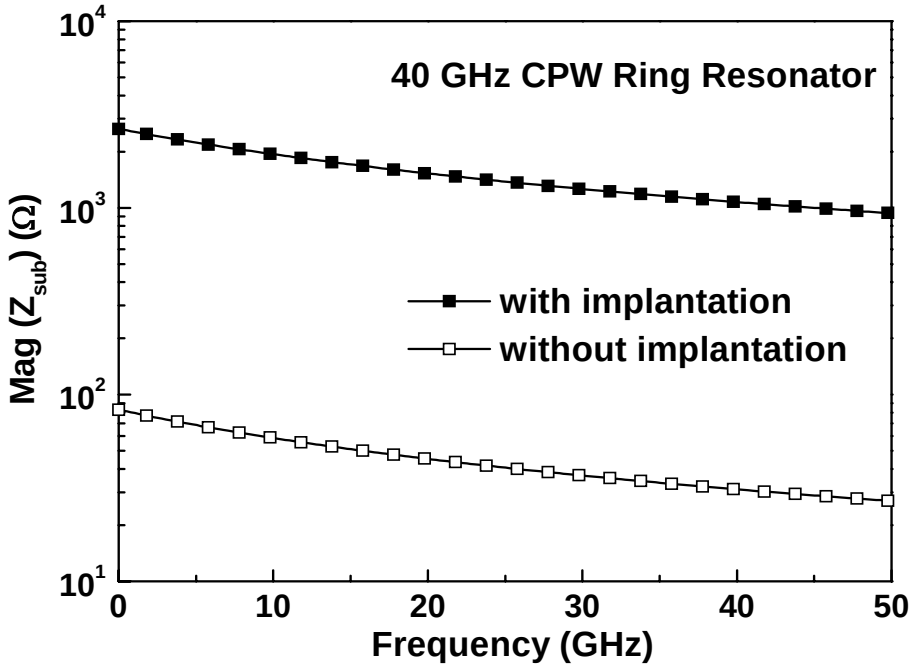
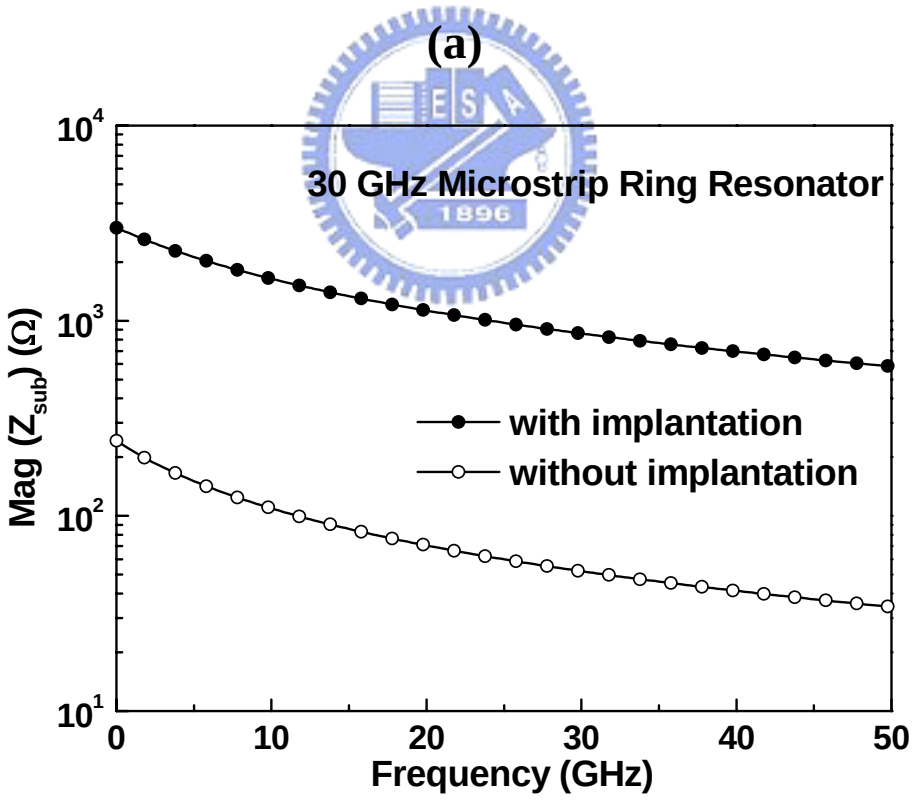


Fig. 2.3.4 The physically-based equivalent circuit of ring resonators. The L expresses the metal stub, and the C_1 is the fringing coupling capacitance of the ring. The substrate loss is modeled by the shunt Rs and Cs to ground.



(a)



(b)

Fig. 2.3.5 The extracted magnitude of the substrate impedance from (a) CPW ring resonators and (b) microstrip ring resonators with or without implantation.

Chapter 3

Microwave Filters and Couplers

3.1 Microwave Band-pass Filters on PCB

3.1.1 Motivation

Microstrip ring resonator filters are been widely used in RF front end of a microwave transceiver [3.1.1]. From circuit design point of view, ring resonators have many attractive features, like compact size, low cost, easy fabrication and good out-of-band rejection [3.1.2]. This device has been widely employed and integrated with oscillators, mixers, and antennas. The stepped impedance design [3.1.3]-[3.1.5] can further control the odd- and even-mode resonant frequencies by adjusting geometric parameters of the resonator. This makes ring resonator filters applicable for designing dual-mode bandpass filters with a fractional bandwidth up to 10% [3.1.6]. Due to the need of newly proposed ultra wide band (UWB) specifications, bandpass filters with GHz bandwidth will be required. Microstrip ring resonator filters fabricated on a PCB usually have a relatively small bandwidth. This is mainly due to the lower coupling gap limit by conventional fabrication methods. The limits for wet

chemical etching process and dry etching are about 100 – 150 μm. There are still few papers devoted in investigating microstrip passive devices with coupling gaps less than 100 μm. Previously, we have shown CPW and microstrip ring resonators, broadband and narrow band filters, antenna and transmission lines on ion-implanted Si substrates with excellent RF performance up to 100 GHz [3.1.7]-[2.1.10]. The achievement is partially due to a sufficiently small gap size fabricated on a low RF loss Si substrate generated by ion-implantation by lithography technique. We apply lithography technique to realize a dual-mode ring resonator filter on PCB. The purpose is to make a sufficiently narrow gap between the resonator and feed lines, so that the fractional bandwidth of a dual-mode ring resonator filter can be pushed up to 30%. It is found that the pass band of the fabricated filter has not only good flatness but also a very low insertion loss.

3.1.2 Filter Design and Fabrication

The dual-mode ring resonator shown in Fig. 3.1.1 has two stepped impedance junctions. If there is no impedance junction, the leading two resonances will degenerate into one frequency, and the use of this kind of resonator will be limited. Here, the junctions are symmetric about the skew symmetric plane, the dashed line in Fig. 3.1.1, and make the degenerated resonant frequencies split up into even- and

odd-mode resonant frequencies, foe and foo. When the circuit operates in even- and odd-modes, the symmetric plane is an open circuit and grounded plane, respectively. Let the microstrip line section of electrical length of 2θp has a characteristic impedance ZL and the remaining part has ZH. Define an impedance ratio

$$K_z = \frac{Z_L}{Z_H} \tag{1}$$

At respective resonances, the admittance sum of the microstrip sections seen at the impedance junction should be zero. Thus, the resonant frequencies foe and foo can be respectively determined by solving the following transcendental equations:

$$K_z \tan\left[\frac{f_{oe}}{f_o}(\pi-\theta_p)\right] + \tan\left[\frac{f_{oe}}{f_o}\theta_p\right] = 0 \tag{2}$$

$$K_z \tan\left[\frac{f_{oo}}{f_o}\theta_p\right] + \tan\left[\frac{f_{oo}}{f_o}(\pi-\theta_p)\right] = 0 \tag{3}$$

Fig. 3.1.2 plots normalized frequencies f_{oo}/f_o and f_{oe}/f_o as a function of $2\theta_p$. It can be seen that frequencies of the even-mode are always higher than those of the odd-mode when $K_z < 1$. Also, the smaller the impedance ratio K_z is, the larger separation between the resonant frequencies is. The plots are used to approximate coupling coefficient C_{12} of the filter:

$$C_{12} = \frac{f_{oe}^2 - f_{oo}^2}{f_{oe}^2 + f_{oo}^2} \tag{4}$$

Note that this coefficient has also to be specified by the formula of filter synthesis:

$$C_{12} = \frac{\Delta}{\sqrt{g_1 g_2}} \tag{5}$$

where g_1 and g_2 are element values of the low-pass filter prototype and Δ is the fractional bandwidth. Thus, for achieving a filter with broad bandwidth, it is important to choose a proper θ_p with the largest separation between the even- and odd-modes. In our design, θ_p and K_z are chosen to be 50^o and 0.4, respectively.

The second step of the design is to establish proper couplings between the ring resonator and input /output feeding networks. This is important since the passband response will be destroyed due to either over or under coupling. The external quality factor Q_e and the fractional bandwidth Δ are related by

$$Q_e = \frac{g_0 g_1}{\Delta} \tag{6}$$

The coupling capacitance can be found to be

$$C = \frac{1}{Z_o} \frac{1}{\sqrt{\frac{Z_H}{\pi Z_o} Q_e - 1}} \tag{7}$$

Where Z_o is the system reference impedance. It can be expected that if a large bandwidth is required, the coupling capacitance C can be quite large so that a small coupling gap will be required.

3.1.3. Results and Discussion

Two dual-mode ring resonator filters are designed, fabricated and characterized by an HP 8720C vector network analyzer. The first one has a gap size 240 μm for design a Chebyshev filter with Δ = 10%, and the other has a gap 40 μm for design a filter with Δ = 30%. Both filters have a center frequency fc = 1.9 GHz. Figs. 3.1.3 (a) and 3.1.4(b) show the simulated responses.

Figs. 3.1.4(a) and 3.1.4(b) show the measured $|S_{21}|$ and $|S_{11}|$ responses of the filters with 240 μm and 40 μm, respectively. In Fig.3.1.4 (a), the measured fractional bandwidth is found to be only 9.5%. In the passband, the best insertion return losses are 1.3 dB and -13 dB, respectively. In Fig.3.1.4 (b), the measured fractional bandwidth is 30% which is the same as the simulation. The best in-band insertion and return losses are only 0.50 dB and -17 dB, respectively. It can be observed that the simulation and measured results have a good agreement, which is mainly due to a good process control with small variation. The small coupling gap is the key factor for achieving small insertion loss and broadband characteristics of band-pass filter.

3.1.4 Conclusions

We have fabricated a broadband (30% bandwidth) dual-mode ring resonator filter with a performance closely matching with ideal EM simulation. A small coupling gap realized by using the IC lithography technique, low insertion loss is also obtained. In contrast, the conventional large gap size of the same filter structure has much smaller fractional bandwidth (10%) and larger insertion loss. This technology can be further applied to design microwave passive devices with even smaller coupling gap.

3.2 Microwave Couplers on PCB

3.2.1 Motivation

Directional couplers are important elements in microwave integrated circuits (MIC's) [3.2.1]. It can be used in design of baluns, power dividers/combiners, filters, attenuators and instrumentation systems. A hybrid coupler, i.e. a coupler with 3-dB coupling, is found useful in building a power distributed amplifier [3.2.2], a balanced mixer [3.2.3], etc. A fully planar conventional microstrip coupler has a coupling less than 10 dB due to lower realizable limit of slot width in microstrip technology. This leads to the development of many methods. In the vertically installed planar (VIP) circuit [3.2.4], coupled lines are constructed perpendicularly to the main microstrip circuit board. In [3.2.5]- [3.2.6], a semi reentrant microstrip section is used to realize the tight coupling. In [3.2.7], couplers are designed in a multilayer structure with two- and three-strip couplings. These approaches rely on the broadside coupling through a dielectric layer between the microstrip lines.

It is also possible to use an original or unfolded Lange coupler for 3 dB coupling. The design concept is based on multifold constructive edge couplings to enhance the coupling capacitance between the two main lines in multiple coupled microstrip. It is found that bond wires are inevitably required in circuit realization, since nonadjacent lines are assumed to have identical potentials.

In this paper, we try to make a conventional single-stage microstrip coupler with a coupling level as high as possible. The high-level coupling is achieved by fabricating a narrow gap between the coupled microstripe using low cost IC process. The design is based on the structure of a 3-dB coupler. Measurement shows that the fabricated coupler has a 4-dB coupling. The measured good results are due to the small coupling gap used in our previous RF passive devices. Note that the entire circuit is fully planar, requires no bond wire, and retrieves the simplicity of the original circuit design.

3.2.2 Filter Design and Fabrication

For a coupler with coupling C, the even and odd mode impedances are required to be [1]

$$Z_{oe} = Z_o \sqrt{\frac{1+C}{1-C}} \tag{1}$$

$$Z_{oo} = Z_o \sqrt{\frac{1-C}{1+C}} \tag{2}$$

The Z_0 are chosen to be 50 and 42.3 Ω for Device 1 and 2 respectively, where additional λ/4 converter impedance (Z_t) of 46.0 Ω is used for Device 2 to match the 50 Ω. The smaller Z_0 and Z_t in Device 2 are smaller for the conductor loss in transmission lines at the design frequency 5 GHz. The RT/Duroid 6010 substrate with

ε_r = 10.2 and thickness = 1.27 mm is chosen to realize the circuit. The EM simulator IE3D [10] is used to validate the circuit design before the circuit is fabricated. The required line width are 309 μm and 4 μm; the interline spacing are 560 μm and 4 μm for Device 1 and 2, respectively. The circuit is fabricated by conventional low cost IC process with a >1-μm resolution and standard FeCl etching. An infrared red aligner is used for pattern exposure, and HFD5 solution for circuit development. The solution is heated up to 50 – 60 ^{o}C to have a better etching in the valley of the central gap. Circuit measurements are performed by an Agilent/HP 8720C vector network analyzer.

3.2.3 Results and Discussion

Figure 3.2.1(a) shows the photo of the fabricated coupler where an enlarged pattern of a part of the coupled lines is displayed in Figure 3.2.1 (b). Transmission line sections with 50Ω characteristic impedance are used to extend the circuit ports for saving an enough spaces of the SMA connectors for measurement. Since the chemical solution etching is isotropic, the fabricated circuit inevitably has a V-shape coupling gap. From the enlarged circuit picture in Figure 3.2.1 (b), the upper opening of the V-shape gap can be estimated to be 24 μm, since total distance between the outer edges of the strips is 620 μm. The performance of the coupler is simulated by using 90^{o} metal edges of gap size 14 μm, which is average of the upper opening and 4

μm width at valley. Figure 3.2.2 compares the simulated and measured responses of Device 1. In Figure 3.2.2 (a), the measured $|S_{21}|$ (through) and $|S_{31}|$ (coupling) responses have very good agreement over a frequency range from 3 to 9 GHz. In Figure 2 (b), the isolation and return loss responses of the fabricated coupler are better than 20 dB.

Figure 3.2.3 (a) and 3.2.3 (b) show the measured coupling response, return loss and isolation loss of Device 2, respectively. Good coupler characteristics of high coupling of 3.8 dB, small insertion loss of -3.9 dB and very wide bandwidth (1dB) of 52% are achieved that are comparable to even better than the reported very wide bandwidth data. The slightly inferior return loss of -24.3 dB and directivity of -21.0 dB may be due to small power reflection in non-ideal impedance transformer. The reason of good agreement between measured and modeled coupler characteristics is due to the sharp and accurate etching profile close to EM simulation shown in the insert picture of Figure 3.2.1. However, since the used IC technology is ~2 decades old with only line definition of >1μm, this process may provide simple and low cost solution for fabricating high performance coupler and other RF devices.

Table 3.2.1 summarizes the measured and simulated data of the couplers at 5GHz. The Device 1 has a coupling level ($|S_{31}|$) of 3.8 dB in simulation and 4.0 dB in measurement. The measured isolation and return loss data of the fabricated coupler

are better than 20 dB, and the 1 dB bandwidth of the circuit is more than 50%. The Device 2 also has a coupling level ($|S_{31}|$) of 3.8 dB in simulation and 3.9 dB in measurement. These simultaneously measured high coupling, high directivity, and broad bandwidth are simply due to the smaller coupling gap from the fundamental theory analysis that was justified by the close match between measurements to EM simulations.

3.2.4 Conclusions

A microstrip coupler with a 4-dB coupling level is fabricated on PCB. It is achieved by etching a 14-μm gap. Entire circuit is fully planar and needs no bond wire. This simple technology will have applications to high performance RF passive devices on PCB.

3.3 Conclusions

A fully planar microstrip coupler with a high coupling level up to 4 dB is fabricated on PCB. Based on the conventional coupled-line structure, a gap size of coupled lines about 14 μm is realized by low cost IC process. It has a single stage and requires no bond wire. In measurement, a bandwidth more than 50% and isolation and return loss better than -20 dB are achieved. The measured responses have good agreement with EM simulation data. A high-performance ring resonator filter is fabricated on PCB with aid of the IC lithography technique. The filter, designed at 1.9 GHz, has a very large fractional bandwidth (up to 30%), an insertion loss of 0.50 dB, a flat $|S_{21}|$ response in pass-band, a return loss better than ~30 dB at two transmission poles and a rejection level of –40 dB at attenuation poles. In addition, the measured characteristics are very close to ideal design by EM simulation. The achieved excellent broadband device characteristics are due to a small coupling gap in the filter. In contrast, the conventional method can only have a large coupling gap with relatively small bandwidths and relatively large insertion losses. The excellent device performance reflects that this technique makes the ring resonator filter applicable from narrow band to broadband designs.

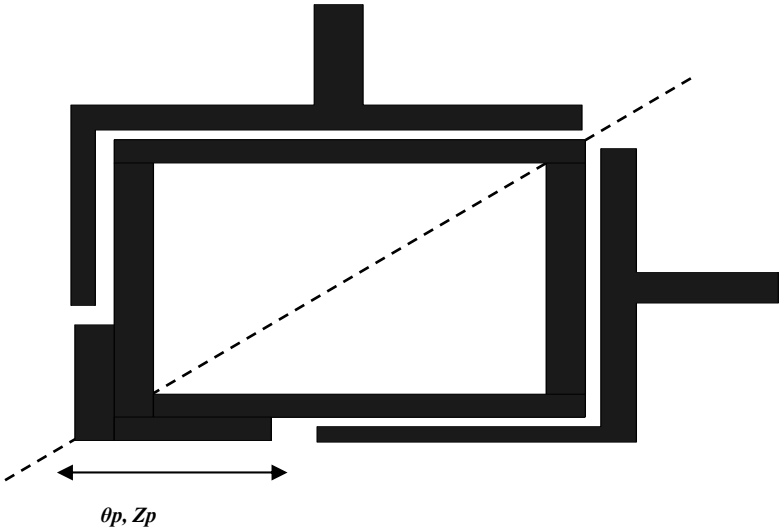


Fig. 3.1.1 Structure of a dual-mode ring resonator filter

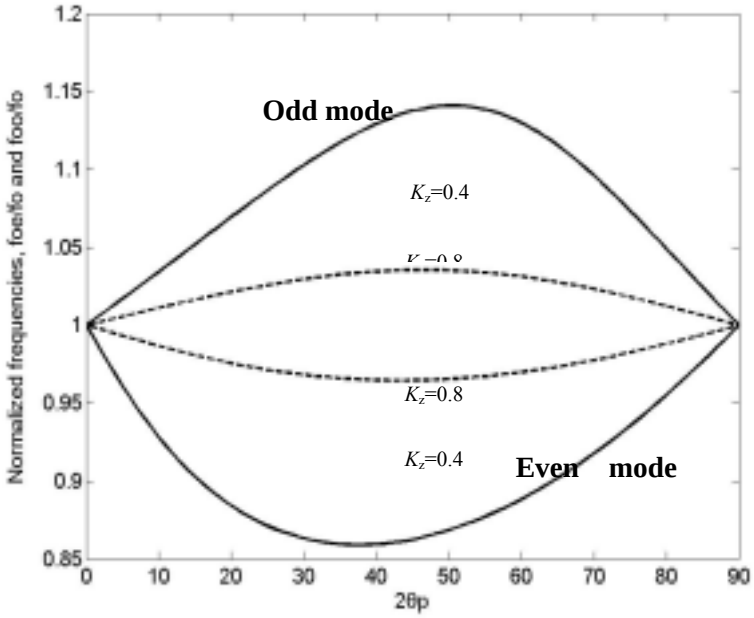
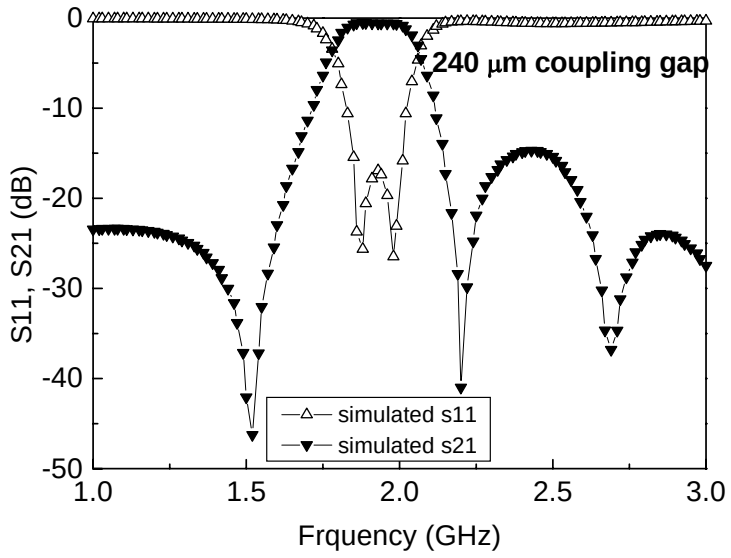
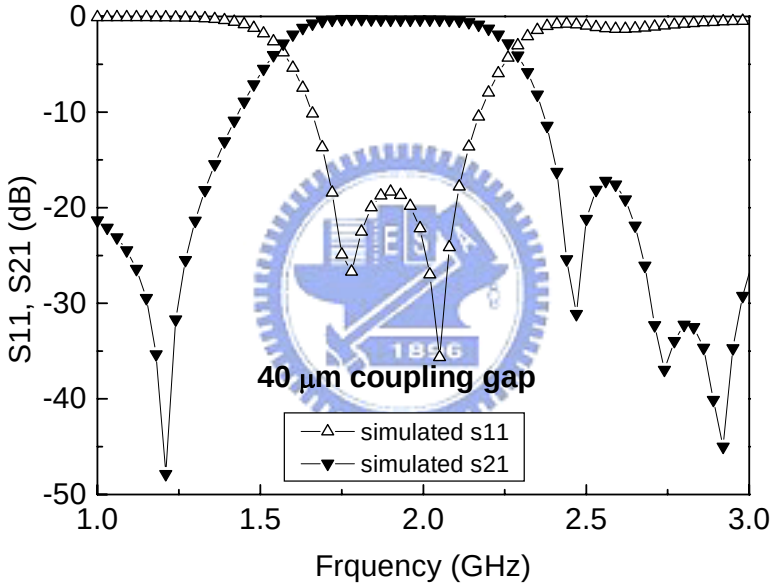


Fig. 3.1.2 Normalized frequencies f_{oe}/f_o and f_{oe}/f_o as a function of electrical length $2\theta_p$

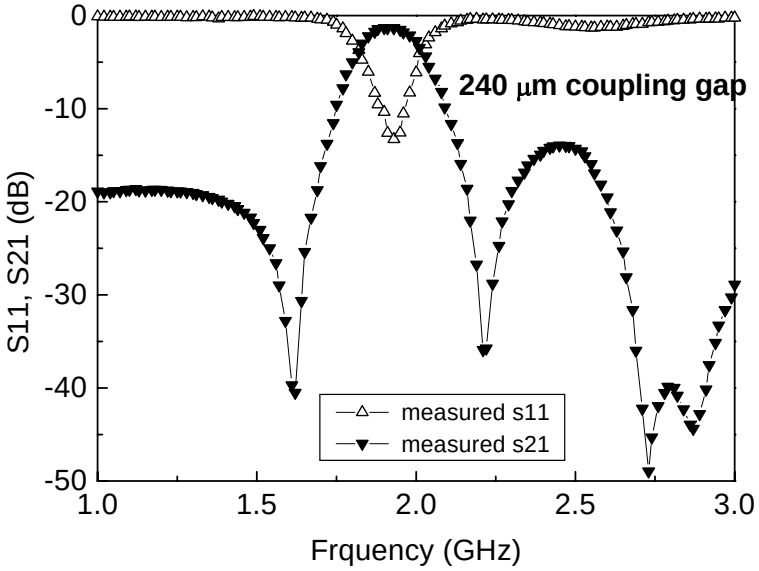


(a)

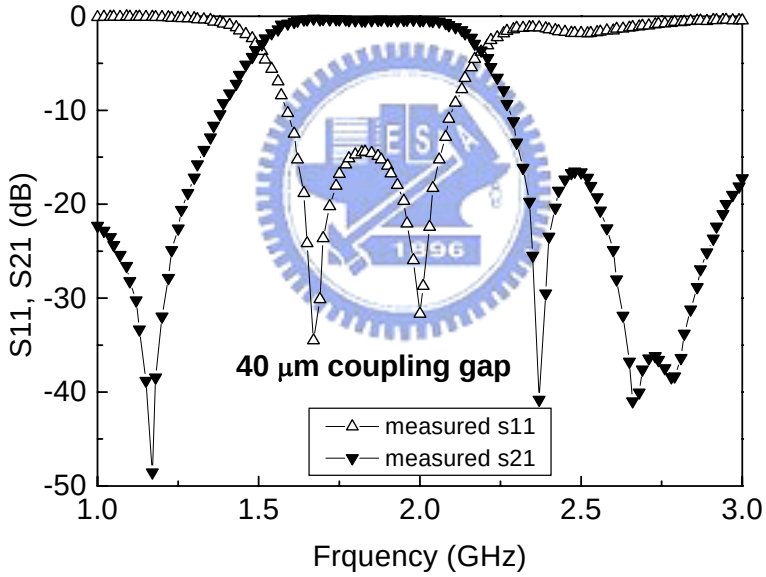


(b)

Fig. 3.1.3 Simulated responses of the dual-mode ring resonator filter with center frequency f_c = 1.9 GHz. (a) Coupled gap = 240 μm, Δ = 10%. (b) Coupling gap = 40 μm, Δ = 30%.

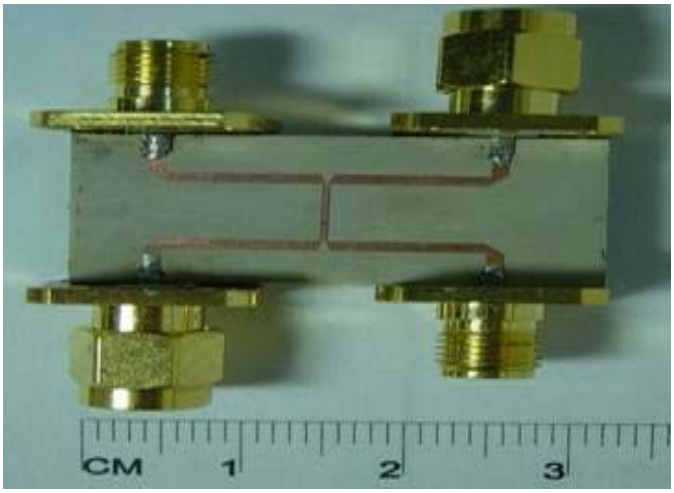


(a)

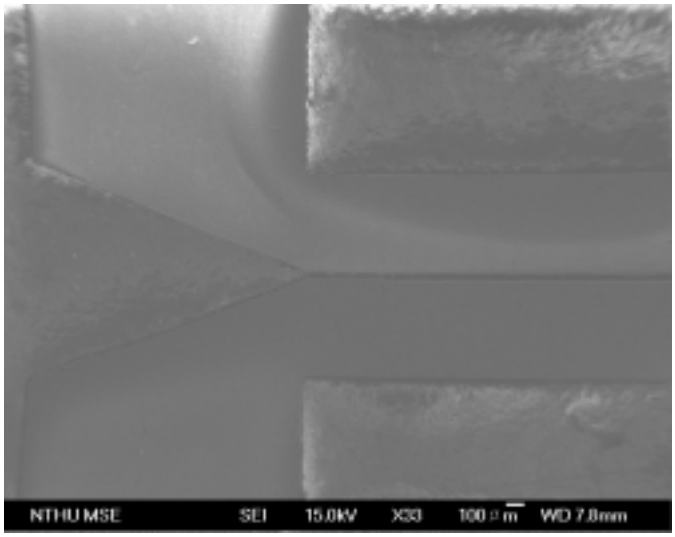


(b)

Fig. 3.1.4 responses of the dual-mode ring resonator filter with center frequency f_c = 1.9 GHz. (a) Coupled gap = 240 μm, Δ = 10%. (b) Coupling gap = 40 μm, Δ = 30%.

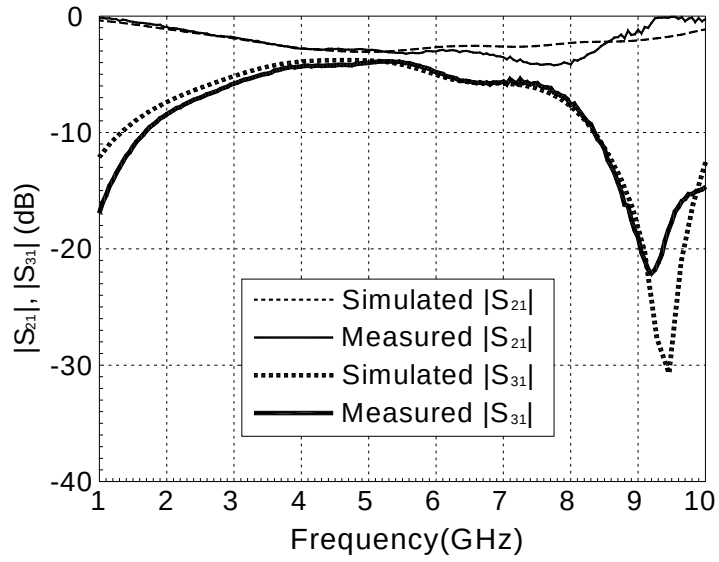


(a)

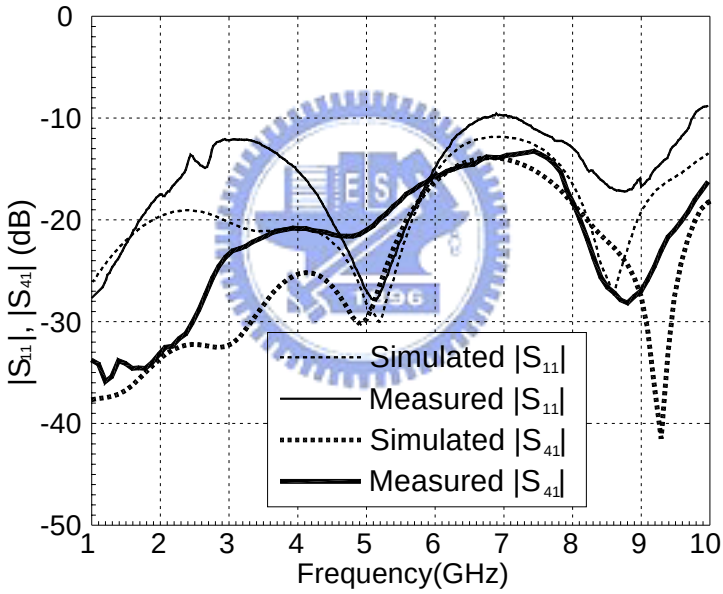


(b)

Fig. 3.2.1 The fabricated coupler. (a) Photo of the entire circuit. (b) Enlarged picture of the coupled lines.

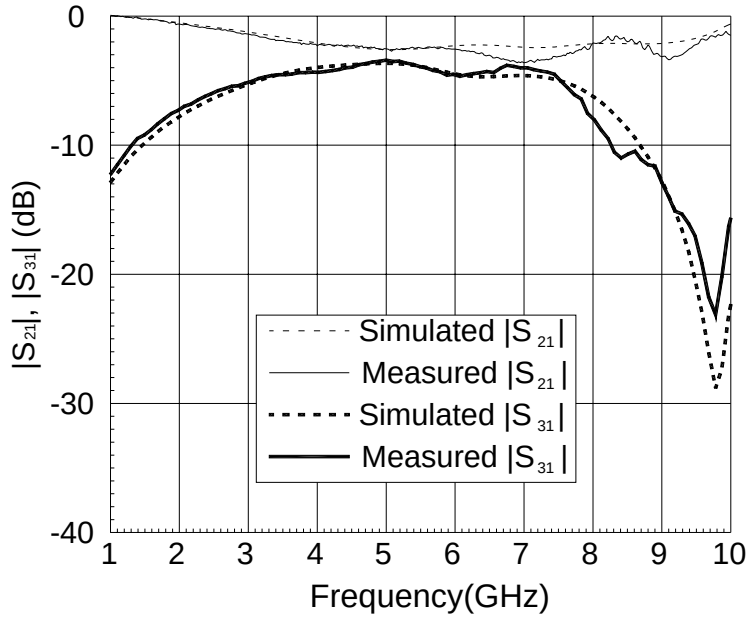


(a)

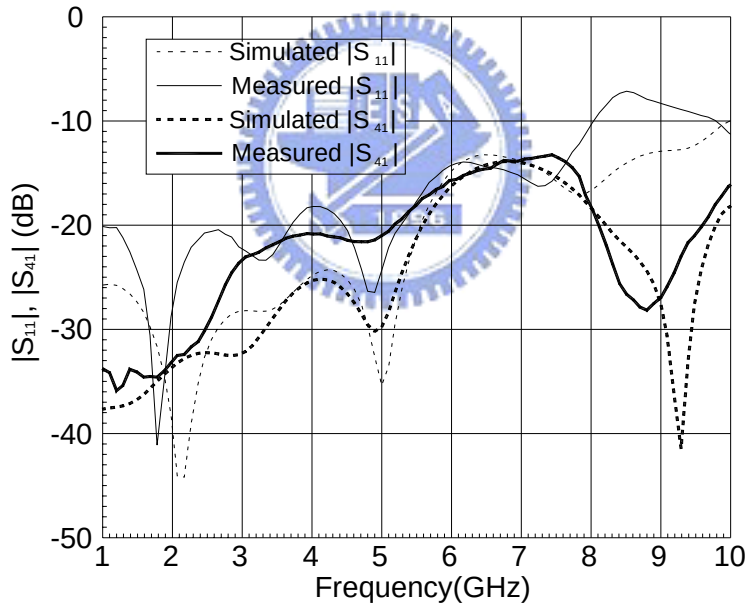


(b)

Fig. 3.2.2 The measured and simulated responses of the fabricated Device 1. (a) $|S_{21}|$ (through) and $|S_{31}|$ (coupling). (b) $|S_{11}|$ (return loss) and $|S_{41}|$ (isolation)



(a)



(b)

Fig. 3.2.3 The measured and simulated responses of the fabricated Device 2. (a) $|S_{21}|$ (through) and $|S_{31}|$ (coupling). (b) $|S_{11}|$ (return loss) and $|S_{41}|$ (isolation)

Device1	*Simulated*	*Measured*
S11(dB)	*-28.2*	*-26.9*
S21(dB)	*-3.07*	*-2.91*
S31(dB)	*-3.82*	*-4.02*
S41(dB)	*-30.0*	*-21.0*
1 dB BW (GHz)	*3.1-6.0* *58%*	*3.4-6.0* *52%*
Device2	*Simulated*	*Measured*
S11(dB)	*-35.4*	*-24.3*
S21(dB)	*-2.90*	*-2.90*
S31(dB)	*-3.90*	*-3.80*
S41(dB)	*-29.8*	*-21.0*
1 dB BW (GHz)	*3.3-6.2* *58%*	*3.7-6.3* *52%*

Table 3.2.1 Performance of the Fabricated Coupler at Design Frequency F_O = 5 GHz.

Chapter 4

Coupling and Dynamic Power Losses in VLSI Interconnects

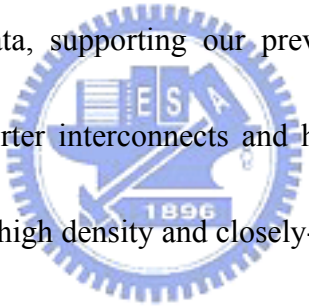
4.1. AC Power Loss and Signal Coupling

4.1.1 Motivation

The down-scaling of silicon device technology into the sub-100nm regime results in the static and dynamic power consumption becoming a major impediment for high-performance integrated circuits (ICs). The importance of the dynamic power consumption issue has been prominent recently [4.1.1]-[4.1.2], because the dynamic power loss is an even more difficult challenge than for the DC power case [4.1.1]-[4.1.4]. The latter can be reduced by using a high-κ gate dielectric and alternative device designs, such as FinFETs. The dynamic power at high frequency (f) mainly arises from the parasitic capacitance (C) of both the MOSFETs and the backend interconnects, and is essentially described by the term $Cv^2f/2$, where the v is the operation voltage. The parasitic capacitance of the MOSFETs which is the main

concern of dynamic power loss in the interconnects can be reduced by using Si-on-Insulator (SOI) [4.1.2], [4.1.5]. The trend in high performance ICs, such as microprocessors and communication ICs, is towards higher operation frequencies and interconnect densities which exacerbate the problem.

Recently we proposed and demonstrated a three-dimensional (3D) VLSI integration structure to address this issue, by using shorter interconnects [4.1.4]. Here we report measurements of the dynamic power loss and also the coupling loss in VLSI backend interconnects. We found good agreement between Electro-Magnetic (EM) simulations and the data, supporting our previous conclusions [4.1.4]. The integration scheme yields shorter interconnects and helps reduce both the coupling and dynamic power losses for high density and closely-spaced interconnect lines.



4.1.2 Experimental Procedure

To imitate the parasitic loss in the interconnects, such as those shown schematically in Fig. 4.1.1. The two long parallel lines with lengths of 0.25, 0.5 and 1 mm and with different line-spacings of 2, 5, and 10 μm are depicted in Fig. 4.1.1(b). The 3D integration [4.1.3]-[4.1.4] can reduce parasitic effects of the interconnects by as much as a half or ¼, by folding the 2D IC once or twice. Different inter-metal dielectric (IMD) thickness of 0.7 or 6 μm were used to simulate the local or global

interconnects using metal-1 (M1) or metal-6 (M6) layers of the 1-Poly-6-Metal (1P6M) structures shown in Fig. 4.1.1(a). Figs. 4.1.2(a) and 4.1.2(b) show the images of fabricated parallel lines, where additional co-planar waveguide (CPW) structure and 150 μm spacing GSG probing pads were used to study the power loss and signal coupling loss. The CPW transmission lines were fabricated using 2 μm thick Al metal on PECVD deposited IMD SiO_2 above the Si substrate. The RF power loss $(1-|S_{21}|^2-|S_{11}|^2)$ was directly obtained from the S-parameters measured with an 8510C network analyzer [4.1.6]-[4.1.9]. This approach was necessary due to the open and shorts being non-ideal in the RF regime. The EM method avoids using complicated equivalent circuit models that can be difficult to solve for the intricate interconnects [4], which are distributed. For comparison we also studied the dynamic power loss and coupling of parallel lines on high-resistivity Si (HRS) substrates [4.1.10]-[4.1.11] which had a resistivity of 1.5×10^4 Ω-cm

4.2 1-Poly-1-Metal 0.18-μm Si MOSFETs

4.2.1 Experimental Results and Discussion

Figures 4.2.1(a), 4.2.1(b) and 4.2.1(c) show the simulated and measured S_{21}, S_{11} and dynamic power loss, respectively, of 1 mm and 0.25 mm long parallel M1 lines with 2 μm gap widths. The M1 lines with 0.7 μm IMD SiO_2 imitate the local interconnects in VLSI ICs. There is good agreement between the measured S_{21} coupling, S_{11} and power loss with the simulation data, suggesting that the 3D EM simulation is valid. Such good matching is difficult to achieve using an equivalent circuit model with discrete elements, due to the complicated parasitics and distributed circuit effects that must be accounted for. The S_{21} coupling increases with increasing frequency resulting in signal loss in the parent transmission line and creates signal disturbances (cross-talk) in nearby lines. The power loss also increases with increasing frequency which is an important issue for future high performance circuits. We define the maximum operation frequency of an IC to be where either the power or signal coupling loss is 3 dB. Then the maximum operation frequency is limited to 3 GHz by the power loss if 1 mm long local M1 parallel lines are used. This can be increased to 20 GHz by using shorter parallel interconnect lines of 0.25 mm in length. Thus the performance of high frequency ICs is limited by the total length of local interconnects, and by the line spacing to other interconnection lines. One method to

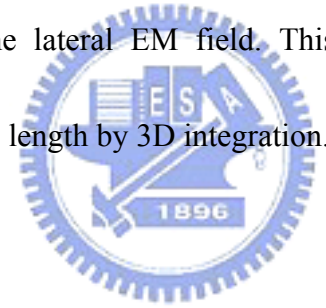
overcome this problem is to use higher resistivity substrates, compared with VLSI-standard 10 Ω-cm resistivity ones. The power loss improves significantly for the same parallel lines on HRS substrates. This is due to the reduced power loss in the parasitic substrate RC networks [7], [9]. This power loss reduction comes at the cost of increased S_{21} coupling, so that the maximum operation frequency is limited to ~16 GHz by the 3 dB coupling loss of 1 mm long M1 lines. Decreasing the line length from 1 mm to 0.25 mm is the most effective way to reduce both the coupling and dynamic power losses and can be achieved by a 3D integration scheme shown in Fig. 1(b).

We also measured structures that had the (M1) line spacing increased to 10 μm. Good agreements between the measurements and the EM simulation was also obtained, with data similar in functional form to those shown in Fig. 3. Table 1 details the values of the parameters for various structures, at 20 GHz. Increasing the line spacing from 2 to 10 μm improves the coupling loss slightly but the improvement at the cost of a reduction of the interconnect density. By using HRS the dynamic power loss can be reduced but the coupling loss unfortunately increases. This suggests that the best way to reduce both coupling and dynamic power losses in high density interconnects is to use shorter interconnect lengths, as provided by 3D integration and HRS substrates.

4.3 1-Poly-6-Metal 0.18-μm Si MOSFETs

4.3.1 Experimental Results and Discussion

We have also investigated the coupling and power losses of global interconnect lines using M6. Figures 4.3.1(a), (b) and (c) show the simulated and measured S_{21}, S_{11} and dynamic power loss, respectively, of 1 mm and 0.25 mm long parallel M6 lines with a 2 μm gap width. Since the parallel lines have 6 μm thick SiO_2 isolation above the Si substrate, the power loss was significantly reduced, compared with those for the 0.7 μm SiO_2 case. The coupling loss was only slightly improved due to the strong gap-width dependence of the lateral EM field. This confirms the importance of reducing the interconnect line length by 3D integration.



4.3.2 Signal Coupling Loss and Power Loss

Figures 4.3.2(a) and 4.3.2(b) show the measured signal coupling loss and dynamic power loss, respectively, with different line length, gap width, and substrate resistivity dependences. Only M1 local interconnects were studied since the losses are more severe than those using M6. The signal coupling loss improves with increasing gap spacing from 2 μm to 10 μm; however this in conflict with the increased interconnect density provide by down-scaling.

Decreasing the line length through 3D integration is much more effective in

reducing the coupling loss than increasing the line spacing and can also preserve the high interconnect density. The HRS substrates help reduce the power loss but not the undesired coupling and cross-talk (Fig. 4.3.2(a)), and the maximum operation frequency is limited to only ~16 GHz, for 1 mm long and 2 μm width parallel lines. As shown the schematic analysis of two coupling lines on low resistivity Si substrate in Fig. 4.3.3 (a), the electric field penetrates deeply into high loss Si substrate (>100 μm) and causes both AC power loss and coupling loss. Here the dash-line presents line-to-line coupling, dot-line is for line-to-ground coupling, and solid-line is for substrate coupling. However, the substrate coupling caused power loss is the dominant effect. By using HRS substrate shown in Fig. 4.3.3 (b), the substrate coupling loss is greatly decreased due to the increasing substrate resistance, resulting in enhanced signal coupling between two coupled lines. The shorter interconnect lengths provided by 3D integration, combined with HRS substrates, should provide both low coupling and dynamic power losses in advanced sub-100nm high interconnect density ICs.

4.3 CONCLUSIONS

We have measured the coupling and dynamic power losses in VLSI interconnects in the RF regime. The losses can be improved by increasing the parallel line spacing, reducing the line length, and increasing underlying SiO_2 isolation thickness. By using HRS wafers the dynamic power loss is better but it is a trade-off with unwanted increase of coupling loss and cross-talk. We conclude that since ICs need to operate at increasingly higher frequencies 3D IC integration which provides shorter interconnect distances can be an effective way to help reduce both the coupling and dynamic power loss.

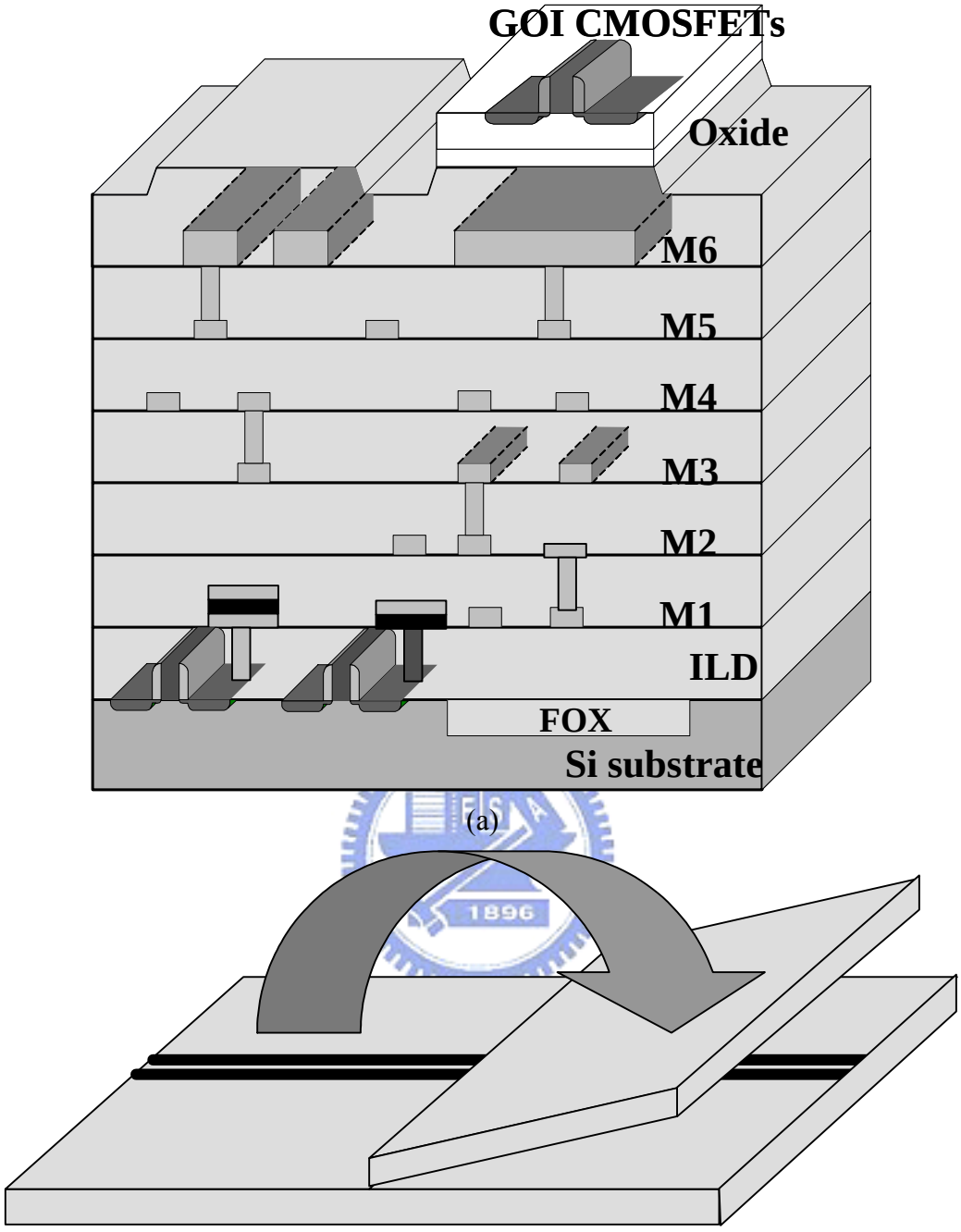
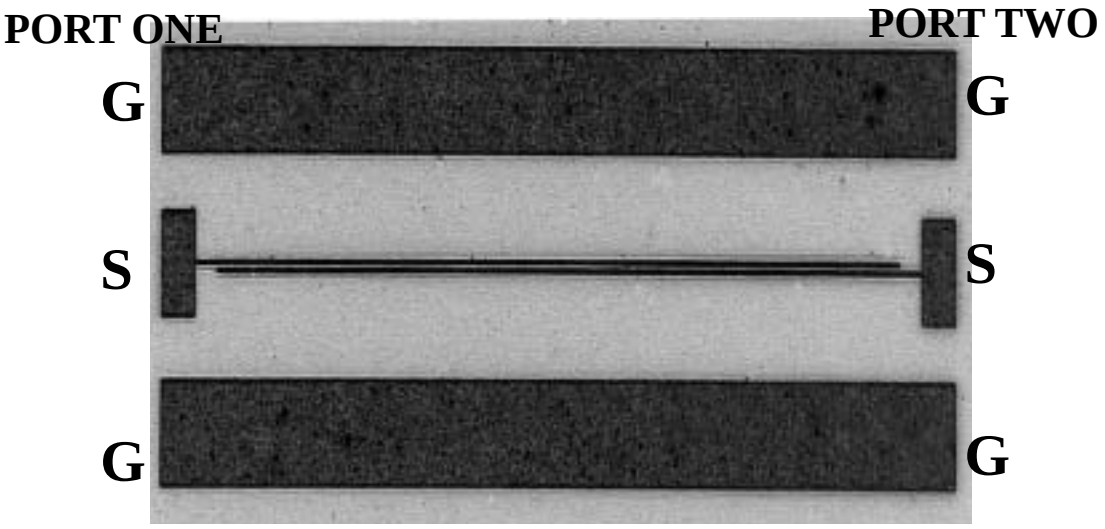
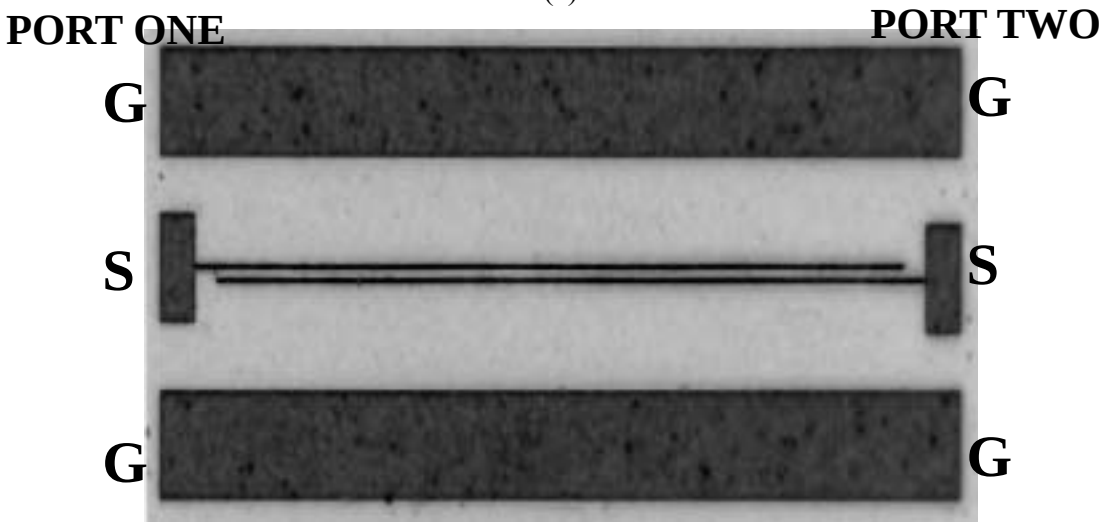


Fig. 4.1.1 (a) The VLSI device integration scheme for Germanium-on insulator devices on a Si technology showing multi-level parallel interconnect lines. The AC power consumption in the parasitic CRL ($Cv^2f/2$, $Li^2f/2$, and $i^2Rf/2$) can be simulated by using the two parallel long lines as in (b). The 3D device integration in (a) is equivalent to folding the 2D IC into 3D as in (b).

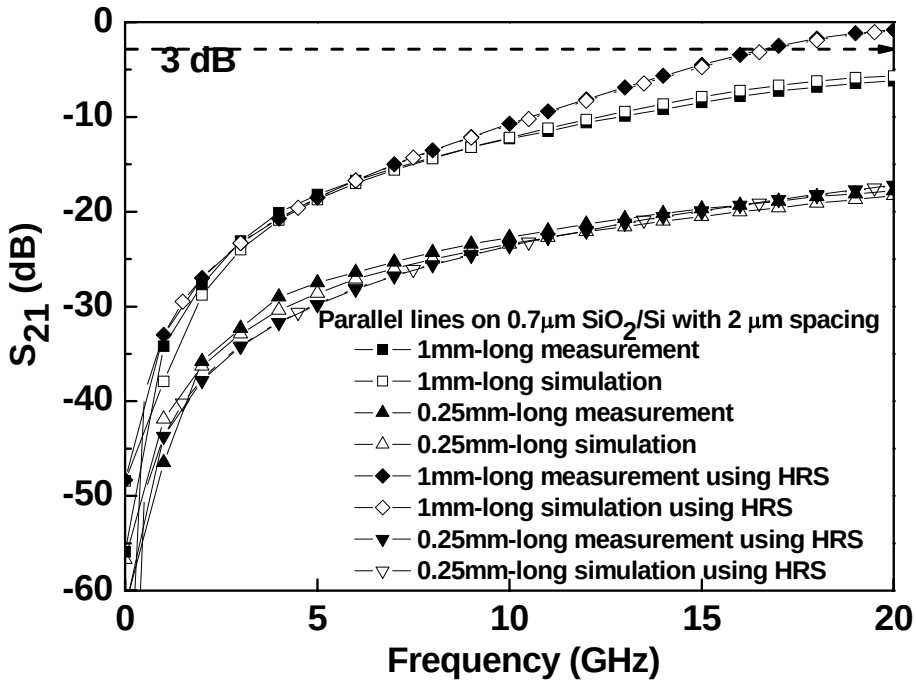


(a)

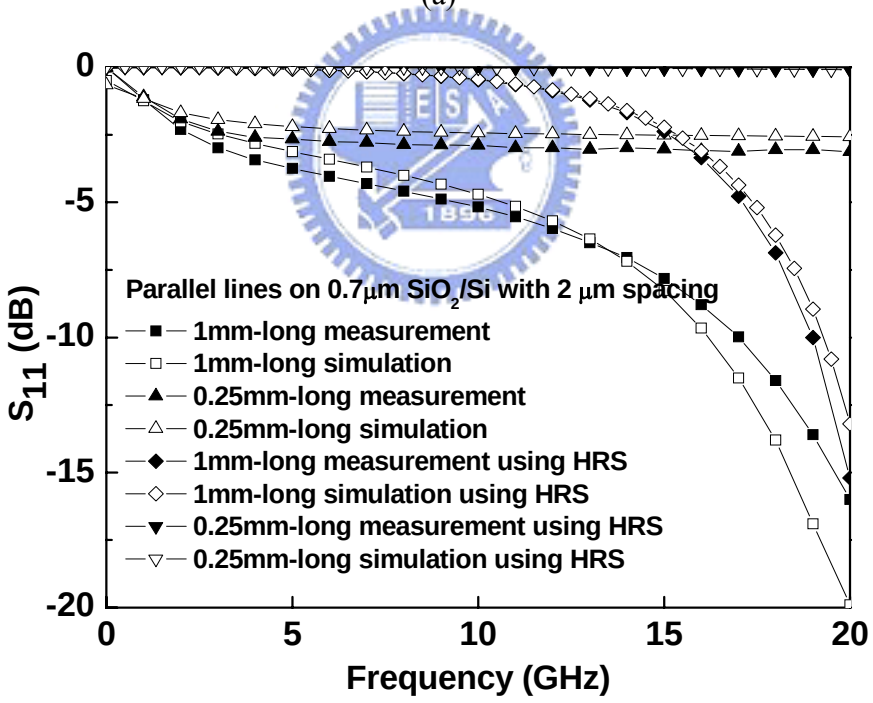


(b)

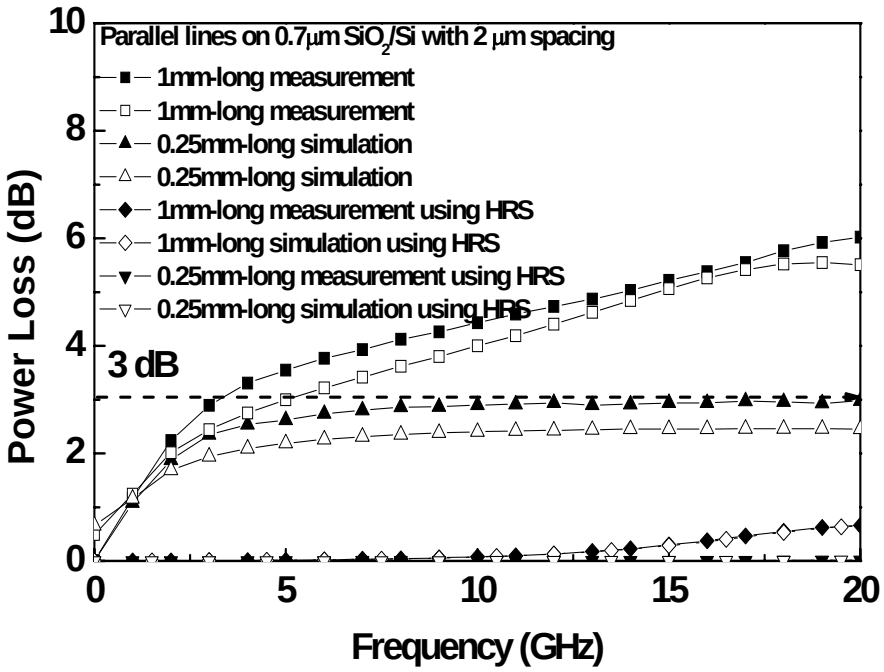
Fig. 4.1.2 Images of fabricated parallel lines with (a) 2 μm and (b) 10 μm width and 1 mm length. The CPW layout and 150 μm pitch probing pads are used for RF measurements.


3 dB
Parallel lines on 0.7μm SiO2/Si with 2 μm spacing
1mm-long measurement
1mm-long simulation
0.25mm-long measurement
0.25mm-long simulation
1mm-long measurement using HRS
1mm-long simulation using HRS
0.25mm-long measurement using HRS
0.25mm-long simulation using HRS
S21 (dB)
Frequency (GHz)
0
-10
-20
-30
-40
-50
-60
0
5
10
15
20

(a)

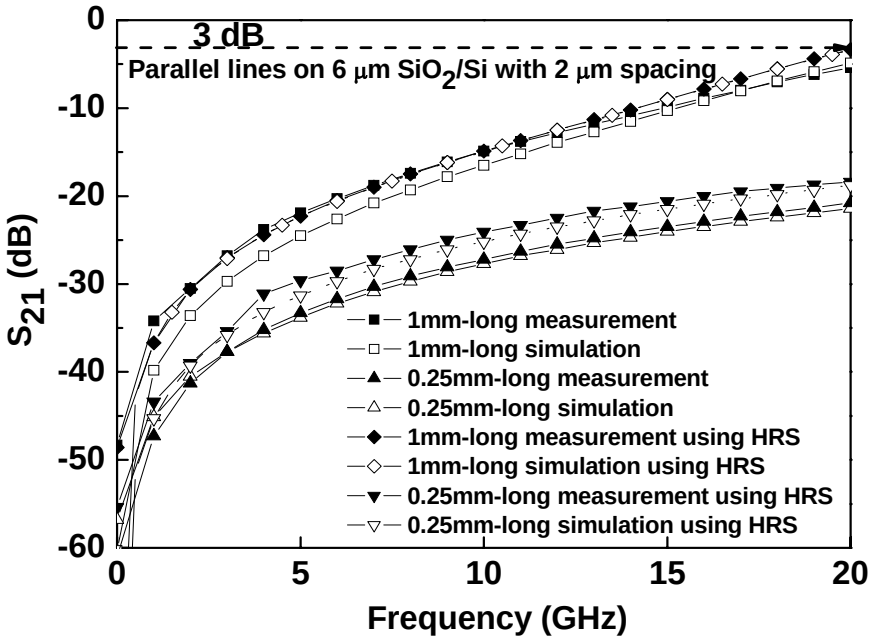

Parallel lines on 0.7μm SiO2/Si with 2 μm spacing
1mm-long measurement
1mm-long simulation
0.25mm-long measurement
0.25mm-long simulation
1mm-long measurement using HRS
1mm-long simulation using HRS
0.25mm-long measurement using HRS
0.25mm-long simulation using HRS
S11 (dB)
Frequency (GHz)
0
-5
-10
-15
-20
0
5
10
15
20

(b)

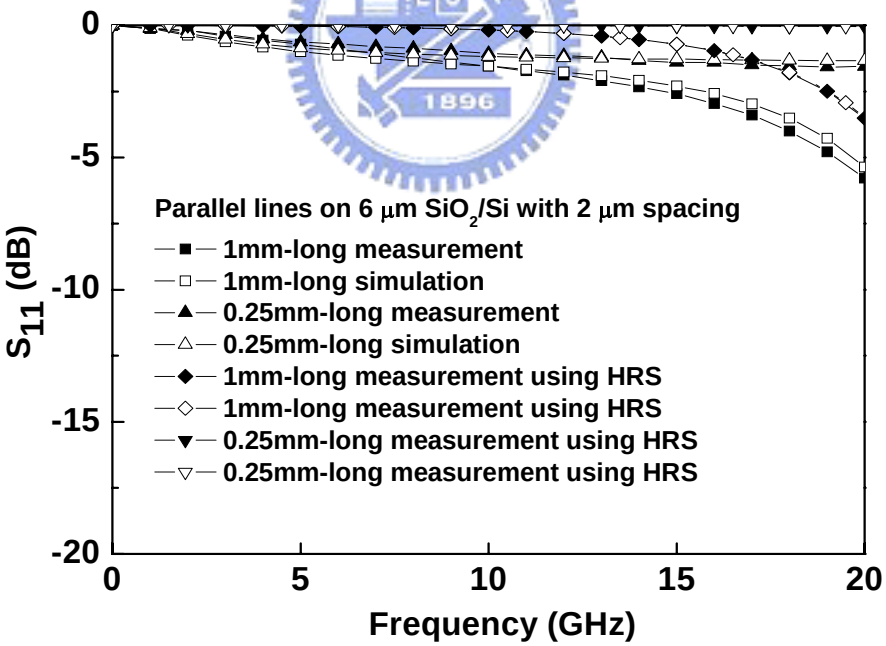


(c)

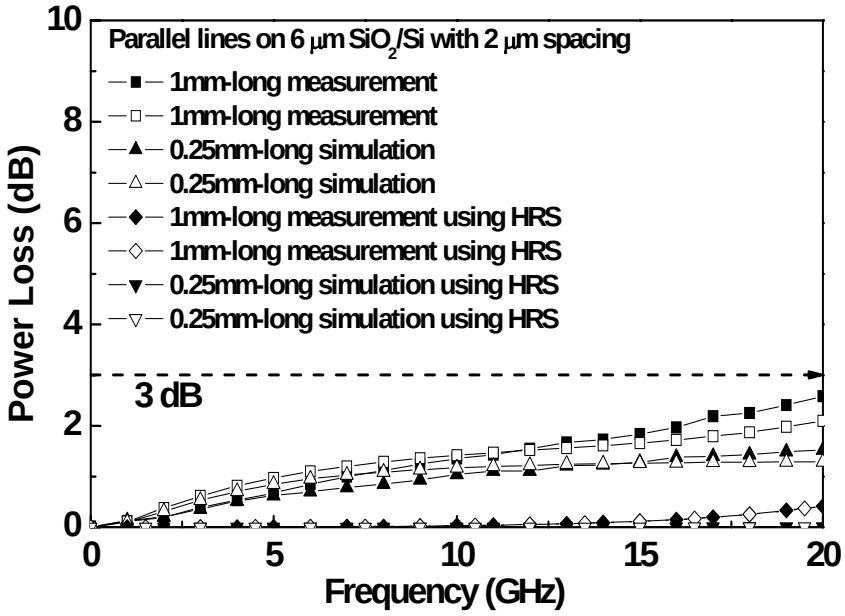
Fig. 4.2.1 The measured and simulated (a) S_{21}, (b) S_{11} and (c) power loss up to 20 GHz of 1 mm and 0.25 mm long parallel interconnect lines on 0.7 μm SiO_2-isolated Si substrates. The line spacing was 2 μm.


3 dB
Parallel lines on 6 μm SiO2/Si with 2 μm spacing
S21 (dB)
Frequency (GHz)
1mm-long measurement
1mm-long simulation
0.25mm-long measurement
0.25mm-long simulation
1mm-long measurement using HRS
1mm-long simulation using HRS
0.25mm-long measurement using HRS
0.25mm-long simulation using HRS

(a)

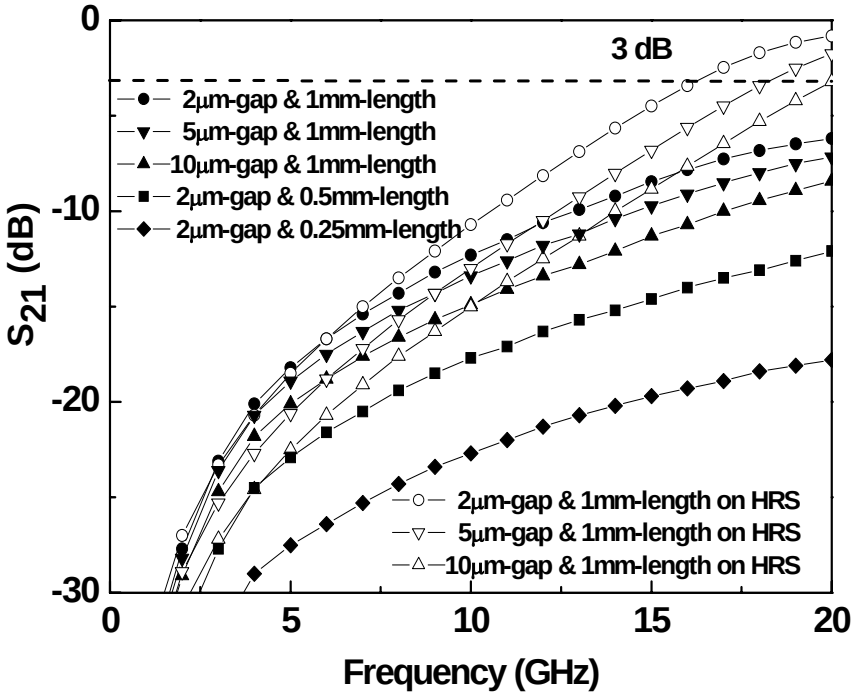

Parallel lines on 6 μm SiO2/Si with 2 μm spacing
S11 (dB)
Frequency (GHz)
1mm-long measurement
1mm-long simulation
0.25mm-long measurement
0.25mm-long simulation
1mm-long measurement using HRS
1mm-long measurement using HRS
0.25mm-long measurement using HRS
0.25mm-long measurement using HRS

(b)

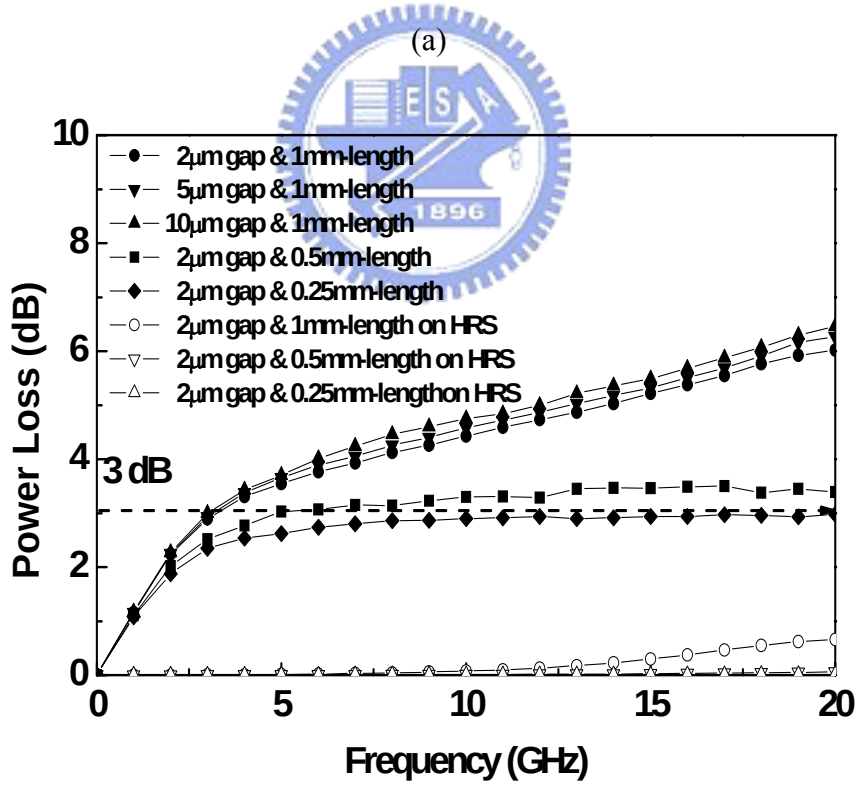


(c)

Fig. 4.3.1 The measured and simulated (a) S_{21}, (b) S_{11} and (c) power loss up to 20 GHz of 1 mm and 0.25 mm long parallel interconnect lines on 6 μm SiO_2-isolated Si substrates. The line spacing was 2 μm.

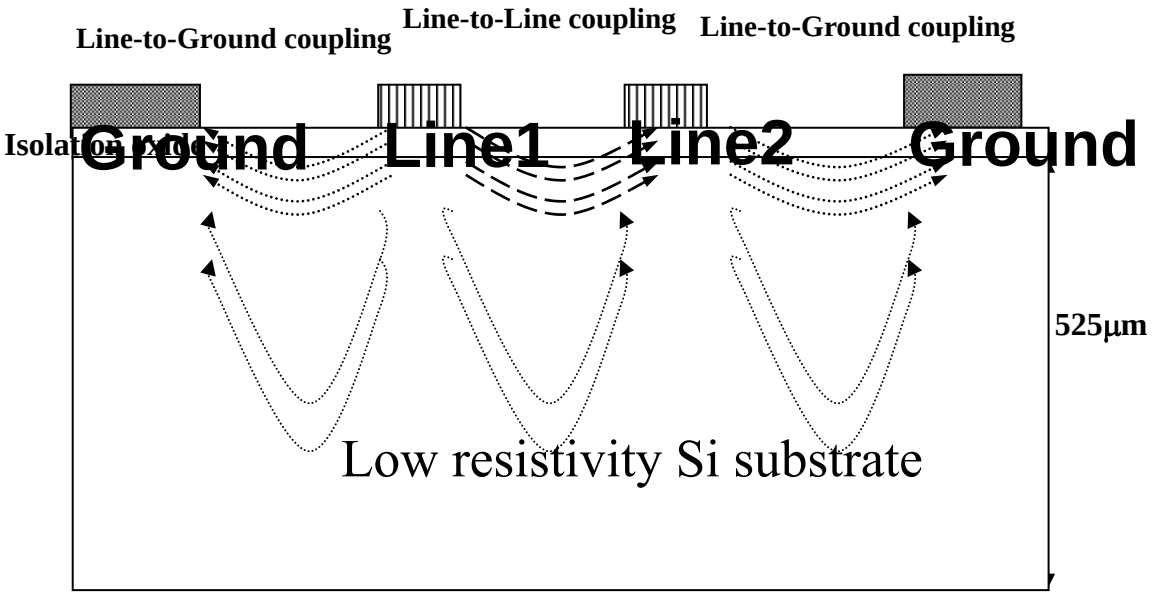


(a)

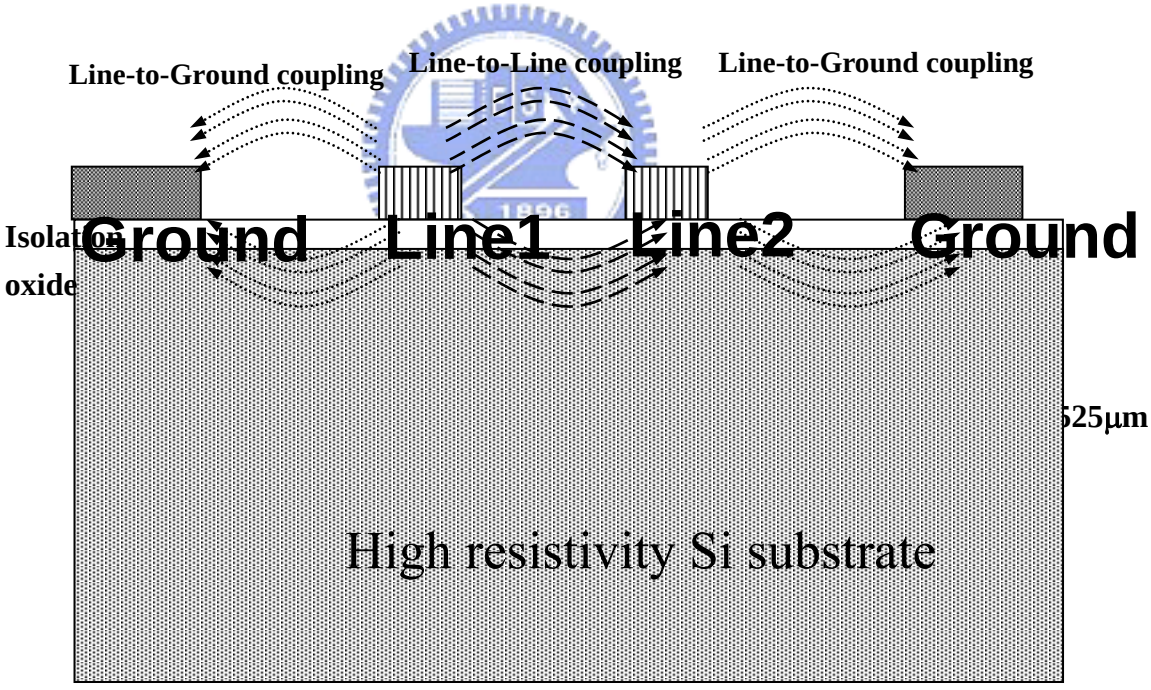


(b)

Fig. 4.3.2 The measured (a) S_{21} coupling and (b) power loss of two parallel interconnect lines, using M1, with different lengths, widths and Si substrate resistivity.



(a)



(b)

Fig. 4.3.3 shows the schematic diagram to show the power and coupling losses in (a) LRS substrate and (b) HRS substrate.

	S_{21} (dB)			Power loss (dB)		
Spacing μm	2	10	2	2	10	2
SiO_2 Thickn μm	0.7	0.7	6	0.7	0.7	6
1mm Meas.	-6.1	-8.4	-5.6	6.0	6.5	2.6
Sim	-5.6	-8.4	-4.8	5.5	6.5	2.1
0.25mm Meas.	-17.8	-18.6	-18.6	3.0	2.8	1.5
Sim.	-18.2	-19.5	-21.4	2.5	2.5	1.3
1mm HRS Meas.	-0.66	-3.1	-2.9	0.6	0.5	0.4
0.25mm HRS Meas.	-16.9	-20.9	-20.5	0.1	0.06	0.05

Table 4.2.1 Measured and simulated values of S_{21} and the power loss at 20 GHz for various structures having 1 or 0.25 mm lengths. The spacing of the lines were 2 or 10 μm and the thicknesses of the oxide were 0.7 μm or 6 μm,. HRS: High resistance substrate. Decreasing the line length by 1/4 can reduce the unwanted S_{21} coupling by more than 10 dB and is much more effective than increasing line spacing by 5 times from 2 μm to 10 μm.

Chapter 5

Band-Pass Filter Using VLSI Backend Interconnects and High Resistivity Silicon Substrate

5.1 Band-Pass Filter Using VLSI Backend Interconnects

5.1.1 Motivation

System-on-a-chip (SoC) designs provide integrated solutions to a wide range of telecommunications, multimedia, and consumer electronics applications [5.1.1]. However, RF passive components have limited its application for SoCs due to the significant losses from conductive silicon substrate. Previously, on-chip antennas have been successfully realized by VLSI interconnects [5.1.2]. In this paper, as the interconnects design on the three-dimension system-on-a-chip, we promote our developing program that parallel coupled-lines band-pass filters fabricated by using

coupling-lines on backend local or global interconnects [5.1.3]. In addition, high frequency losses and crosstalk suffering from Si substrate can be overcome with high resistivity substrate technology [5.1.4]. Hence, combined with the backend interconnects and high resistivity substrate, superior performance of the parallel coupled-line filter [5.1.5] can be accomplished. The established equivalent circuit model also helps band-pass filters to contribute to the development of RF passive devices integrated into SoCs.

5.1.2 Experimental Procedure

The increasing coupling or cross-talk effect between interconnects is unavoidable due to the increasing density and the scaling minimum feature size on SoCs. To imitate these effects, interconnects driven by a transistor and connected to the next gate with modern VLSI CMOS design. Fig. 5.1.1 shows that interconnects are described as resistance at the driving port and capacitance at the load port [5.1.6]. Different inter-metal dielectric (IMD) thickness of 0.7 or 6 μm were used to simulate the local or global interconnects using metal-1 (M1) or metal-6 (M6) layers of the 1-Poly-1-Metal (1P1M) and the 1-Poly-6-Metal (1P6M) structures on CMOS 0.18μm standard process.

5.1.3 Results and Discussion

Fig. 5.1.2 shows the simulated and measured results for a 1 mm interconnect parallel coupled-line filter with a 10 μm spacing-gap on 0.7 μm SiO_2-isolated low-resistivity Si (M1). At the resonating frequency of 25 GHz, the RF characteristics of the measured band-pass filter, such as the insertion loss of 3.6 dB and the return loss of 20 dB, are carried out. From measured and simulated results, it has been demonstrated that parallel coupled-line filters based on VLSI backend interconnects has been successfully embedded into the SoCs. The measured results are consistant with the simulated results, which imply that the IE-3D simulator is reliable.

We also made a study of a 1 mm interconnect parallel coupled-line filter with spacing-gaps of 2.5 μm, 5 μm, and 10 μm on 6 μm SiO_2-isolated low-resistivity Si substrates (M6) in Fig. 5.1.3. It shows that the resonating frequency increases from 25, 28, or 31 GHz with the increasing of the spacing-gap to 2.5 μm, 5 μm, and 10 μm. This represents that optimized design of spacing-gap geometry has benefits from extending the design range.

Using a high resistivity silicon substrate (HRS), we measured S_{21} and S_{11} responses of a 1 mm interconnect parallel coupled-line filter with a 10 μm spacing-gap. The results are shown in Fig. 5.1.4. The simulation for ideal designed filters is included for comparison. From this figure, the S_{11} response of the measured

parallel coupled-line filters on 0.7 μm SiO_2-isolated HRS shows a good performance in enhancing its stop-band characteristics that have two transmission zeros at 26 GHz and 41 GHz with an attenuation level of 23.4 dB and 19.7 dB. The S_{21} response is as small as 1.1 dB at the central frequency of 33.5 GHz. The in-band insertion loss has a minimum of 0.3 dB at 26 GHz and increases smoothly with frequency. The simulated and measured S_{21} and S_{11} responses of 1 mm interconnect parallel coupled-line filters with a 10 μm spacing-gap on 6 μm SiO_2-isolated HRS are also plotted in Fig. 6. The central frequency of this measured parallel coupled-line filter is shifted to 38.5 GHz with the measured S_{21} of 1.4 dB, and the two rejection bands of that are centered at frequencies of 30 and 46 GHz, respectively. The flat insertion loss in the pass-band, with a minimum of 0.4 dB, is suitable for wide-band application at the millimeter-wave range.

5.1.4 Equivalent Circuit Modeling

Fig. 5.1.5 shows the equivalent circuit model of interconnects filters. The equivalent circuit of the substrate RC network includes the C_{ox}, the R_{sub} and the C_{sub}, which are the capacitance contributed by the IMD SiO_2, the shunt resistance and capacitance modeling the effect of lossy silicon substrate, respectively. In the equivalent circuit of the two coupled line, L_1 and R_1 are the series inductance and

parasitic resistance of the interconnect line body, L_2 and R_2 are the series inductance and parasitic resistance of the nearby interconnect line body. The C_{couple} is the coupling capacitance between the two parallel coupled-lines and $C_{fringing}$ is the fringing capacitance to the ground.

Fig. 5.1.6 shows the measured and modeled S_{21} and S_{11} results for a 1 mm interconnect parallel coupled-line filter with a 10 μm spacing-gap on 6 μm SiO_2-isolated low resistivity silicon substrate (LRS). The consistency between the measured and modeled results from S-parameter proves that the equivalent circuit agrees with the modeled parallel-coupled line filter on standard VLSI process.

Fig. 5.1.7 and Fig.5.1.8 show the measured and modeled S_{21} and S_{11} results for a 1 mm long interconnect parallel coupled-line filter with a 10 μm spacing-gap on 6 μm SiO_2-isolated high resistivity silicon substrate. The modeled results are almost completely matched with the measured results that can demonstrate the reliability of this model. As compared with Fig. 8, the increased S_{21} coming from the reduced substrate coupling, and enhancing the mutual coupling effect on interconnects itself. From the plot of S-parameter, we can also see that the increasing capacitive and decreasing resistive effects up to 50 GHz. The measured and modeled S_{11} also have the same trend on the Smith chart. From 24 GHz to 45 GHz shown in Fig. 5.1.8, the resonating frequency often stays nearby the characteristic impedance, which means

the fabricated characteristics of lower insertion loss and wider bandwidth with the less reflection. Meanwhile, the increased S_{21} and decreased S_{11} results make an agreement with Fig. 5.1.4.

5.1.5 Conclusions

High performance band-pass filters based on standard VLSI backend process are successfully demonstrated. This novelty of using VLSI backend interconnect with high resistivity substrate provides an attractive solution for RF passive devices embedded into low-cost high-performance wireless systems.

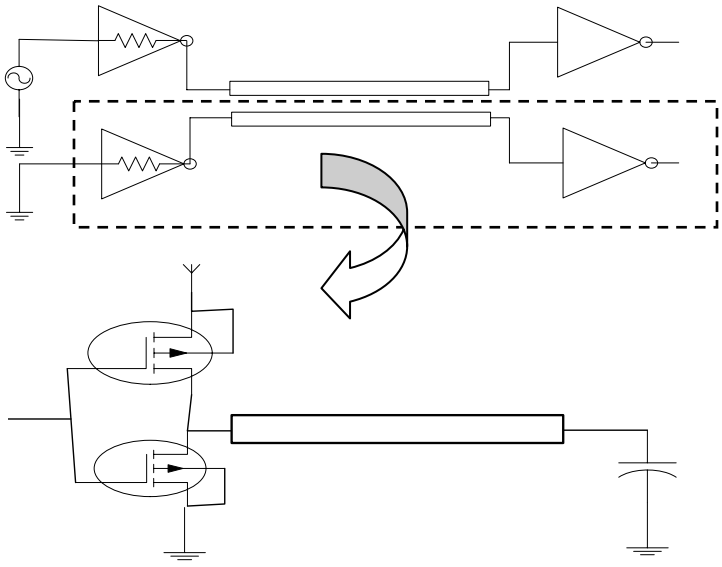


Fig. 5.1.1 shows interconnects driven by a transistor and connected to the next gate on CMOS circuits.

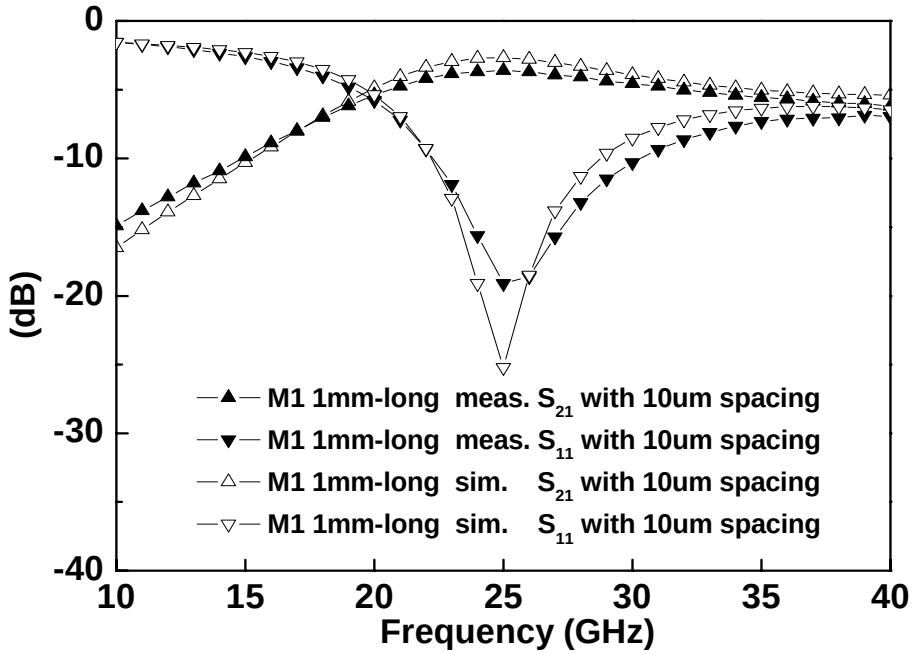


Fig. 5.1.2 shows the measured and simulated S_{21} and S_{11} results of 1 mm coupled-line on M1.

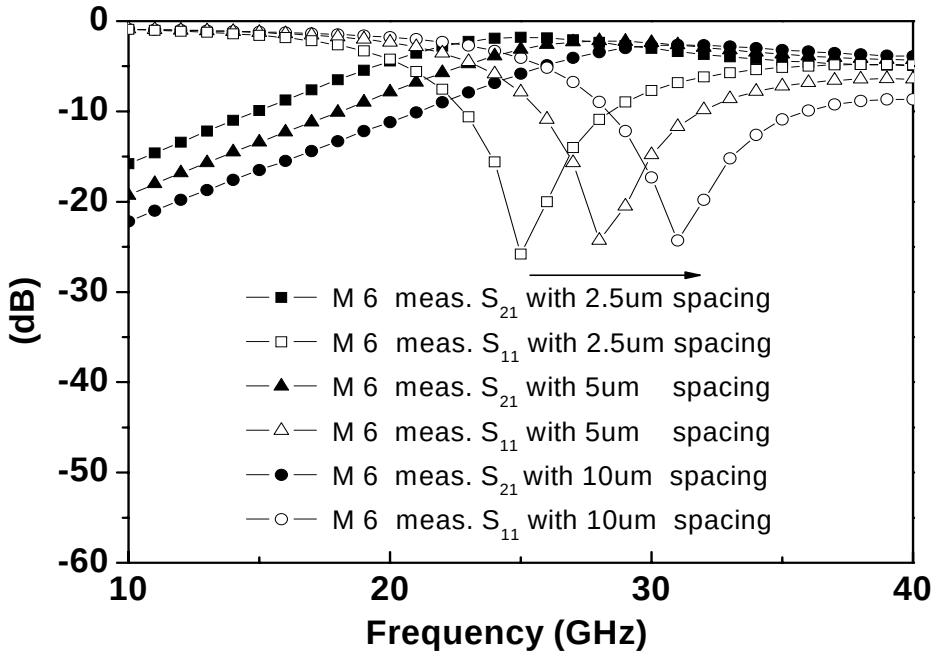


Fig. 5.1.3 shows the measured S_{21} and S_{11} results of a 1 mm coupled-line with 2.5 μm, 5 μm, and 10 μm spacings on M6.

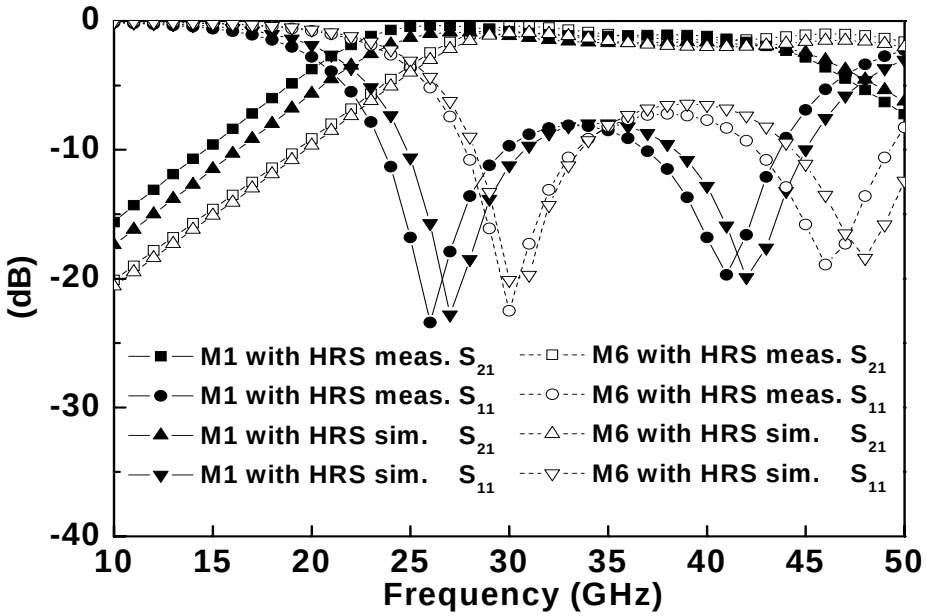


Fig. 5.1.4 shows the measured and simulated S_{21} and S_{11} results of a 1 mm coupled-line on M1 and M6 with HRS.

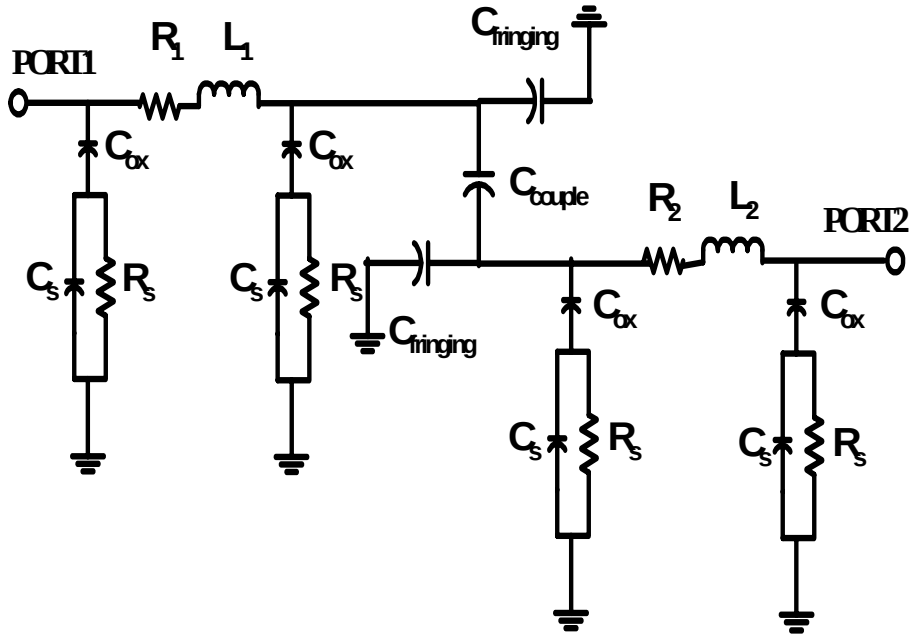


Fig. 5.1.5 shows equivalent circuit of coupled-lines using interconnects on VLSI process.

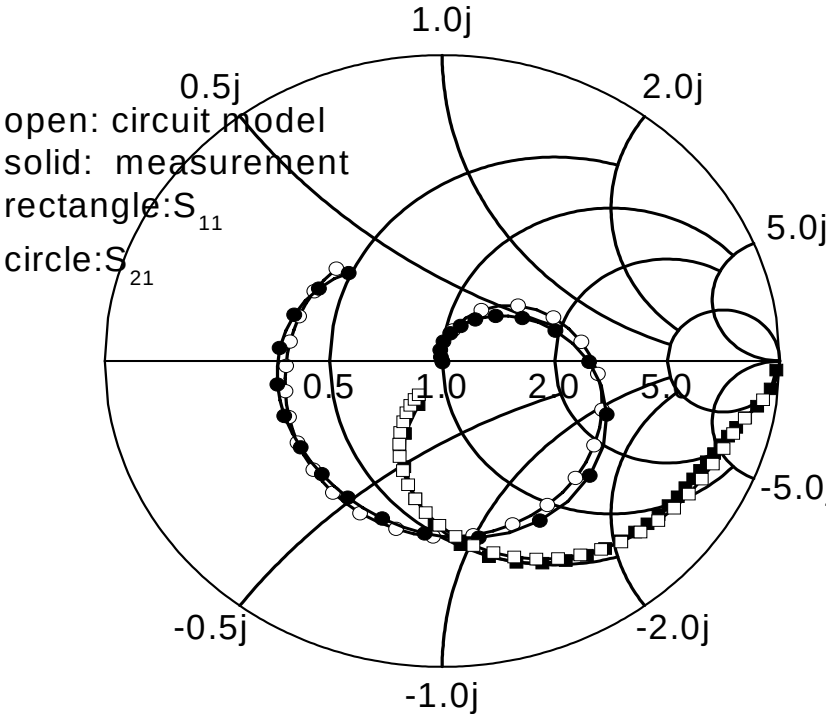


Fig. 5.1.6 shows measured and modeled S_{21} and S_{11} results of 1mm coupled-lines on LRS.

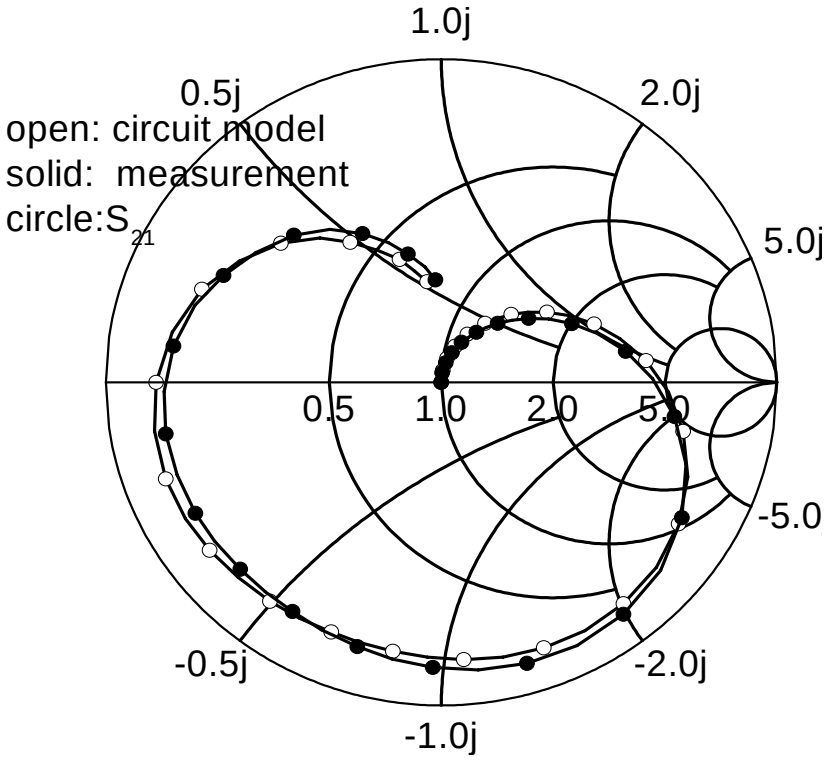


Fig. 5.1.7 shows measured and modeled S_{21} results of 1mm coupled-lines on HRS.

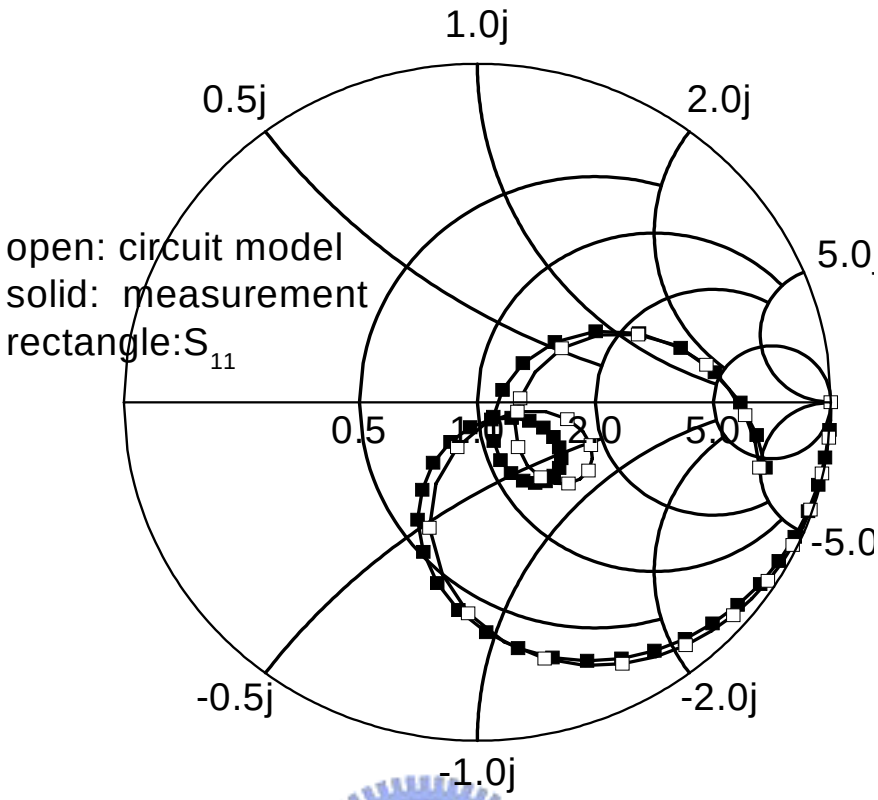


Fig. 5.1.8 shows measured and modeled S_{11} results of 1mm coupled-lines on HRS.

Chapter 6

CONCLUSIONS AND FUTURE WORKS

6.1 Conclusions

For high frequency applications, the characteristics of Si-based RF components degrade with increasing operation frequency due to the high loss of Si substrate and the parasitic effect. The passive device characteristics also change tremendously with operation frequencies, therefore, circuit performance is degraded seriously. In this thesis, we introduce a simple method to convert the standard Si to high resistivity substrate.

We have achieved extremely low power loss for both bulk (0.4 dB/mm at 50 GHz) and thin-film (0.9 dB/mm at 20 GHz) microstrip transmission lines on VLSI-standard Si substrates. The fabricated CPW and microstrip ring resonators on Si substrates with good RF performance at ~40 and ~30 GHz was also obtained which is closed to that for ideal IE3D-designed resonators.

On the other hand, we also achieved good RF performance of a broadband (30% bandwidth) dual-mode ring resonator filter with a performance closely matching with ideal EM simulation and a microstrip coupler with a 4-dB coupling level is fabricated on printed circuit board. The excellent RF performance is even close to IE3D designed ideal filters. It has a great potential for integrating microwave passive devices into printed circuit board where the cost and size can be optimized.

We have measured the coupling and a dynamic power loss in VLSI interconnects in the RF regime. The losses can be improved by increasing the parallel line spacing, reducing the line length, and increasing underlying SiO_2 isolation thickness. By using HRS wafers the dynamic power loss is better but it is a trade-off with unwanted increase of coupling loss and cross-talk. We conclude that since ICs need to operate at increasingly higher frequencies 3D IC integration which provides shorter interconnect distances can be an effective way to help us reduce both the coupling and dynamic power loss. In addition, high performance band-pass filters based on standard VLSI backend process are successfully demonstrated. This novelty of using VLSI backend interconnect with high resistivity substrate provides an attractive solution for RF passive devices embedded into low-cost high-performance wireless systems.

6.2 Future Works

Since the great improvement in the RF/microwave passive devices has been demonstrated with very low loss since it is urgent to investigate the effects of substrate coupling on the performance of CMOS RFIC's and systems. More works to optimize the design and accurate simulation are worth to realize the circuit level applications. Beside, the structures of passive devices can be further designed to achieve optimized performance. If the combination of integrating the passive devices with 3D coming, it shall be very useful to realize the fully integrated high performance CMOS RF/microwave circuit or system.

REFERENCES

[1.1.1] L. E. Larson, “Integrated circuit technology options for RFIC’s? Present status and future directions,” *IEEE J. Solid-State Circuits*, vol. 33, 1998, pp. 387-399.

[1.1.2] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, “High Q inductors for wireless applications in a complementary silicon bipolar process”, *IEEE J. Solid-State Circuits*, vol. 31, 1996, pp. 4-9.

[1.1.3] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, and Y. H. Kwark, “Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low-loss substrates,” *IEEE Trans. Microwave Theory Tech*, vol. 45, 1997, pp. 1961-1968.

[1.1.4] J. P. Raskin, A. Viviani, D. Flandre and J.-P. Colinge, “Substrate crosstalk reduction using SOI technology,” *IEEE Trans. Electron Devices*, vol. 44, 1997, pp. 2252-2261.

[1.1.5] J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, and C.-K. Kim, “Surface micromachined solenoid on-Si and on-glass inductors for RF applications,” *IEEE Electron Device Lett.*, vol. 20, 1999, pp. 487-489.

[1.1.6] R. F. Drayton, R. M. Henderson, and L. P. B. Katehi, “ Monolithic

packaging concepts for high isolation in circuits and antennas," *IEEE Trans. Microwave Theory Tech.*, vol. 46, 1998, pp. 900-906.

[1.1.7] J. Kim, Y. Qian, G. Feng, P. Ma, M. F. Chang, and T. Itoh, "Millimeter-wave silicon MMIC interconnect and coupler using multilayer polymide technology," *IEEE Trans. Microwave Theory Tech.*, vol. 48, 2000, pp. 1482-1487.

[1.1.8] M. Marso, M. Wolter, R. Arens-Fischer, P. Kordos, and H. Luth, "Formation of laterally displaced porous silicon filters using different fabrication methods," in *IEEE Advanced Semiconductor Devices and Microsystems Dig.*, 2000, pp, 95-98.

[1.1.9] M. F. Chang, Y. Qian, P. Ma, and T. Itoh, "Silicon/metal polymide (SIMPOL) interconnects for broadband mixed signal silicon MMICs," *Electronics Lett.*, vol. 34, 1998, pp. 1670-1671.

[1.2.1] Ling Yun, "On current carrying capacities of PCB traces," *Electronic Components and Technology Conference, Proceedings*. May 2002, pp.1683-1693.

[1.2.2] E. Waffenschmidt, B. Ackermann, J.A. Ferreira,"Design method and material technologies for passives in printed circuit Board Embedded circuits" *IEEE Transactions on Power Electronics*, Vol. 20, Issue 3, May

2005, pp. 576 – 584.

[1.2.3] S. Hata, “Vision systems for PCB manufacturing in Japan,” *16th Annual Conference of IEEE Industrial Electronics Society*, vol.1. 1990, pp. 792 – 797.

[1.2.4] A. R. Hidde, A. Gierse, ”An AI-based manufacturing design rule checker and path optimizer for PCB production preparation and manufacturing” Components, Hybrids, and Manufacturing Technology, *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, B, C]* Vol. 15, Issue 3, June 1992, pp. 299 – 305.

[1.2.5] Jun So Pak, Jingook Kim, Jung-Gun Byun, Heejae Lee, Joungho Kim,”Coupling of through-hole signal via to power/ground resonance and excitation of edge radiation in multi-layer PCB” *IEEE International Symposium on Electromagnetic Compatibility*, Vol. 1, ,2003, pp. 231 – 235.

[1.2.6] E. K.W. Gan, H.Y. Zheng, G.. C. Lim,”Laser drilling of micro-vias in PCB substrates,” *Proceedings of Electronics Packaging Technology Conference*, 2000, pp.321 – 326.

[1.2.7] G. Smithson,” Practical RF printed circuit board design,” *IEE Training Course 5. How to Design RF Circuits*, pp. 11/1 - 11/6, 2000.

[1.3.1] D. S. Yu, Albert Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C.

Zhu, M.-F. Li, W. J. Yoo, S. P. McAlister, and D. L. Kwong, “3D GOI CMOSFETs with Novel IrO2(Hf) Dual Gates and High-k Dielectric on 1P6M-0.18 μm-CMOS,” *in IEDM Tech. Dig.*, 2004, pp. 181-184.

[1.3.2] J. W. Joyner, P. Z. Ha, J. D. Meindl, "Global interconnect design in a three-dimensional system-on-a-chip." *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 12, Issue 4 , 2004, pp.367 – 372.

[2.1.1] B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, M.-R. Lin, 15nm gate length planar CMOS transistor, *International Electron Devices Meeting (IEDM) Tech Dig*, 2001, pp. 937-939.

[2.1.2] T. Ohguro, K. Kojima, H. S. Momose, S. Nitta, T. Fukuda, T. Enda, and Y. Toyoshima, Improvement of high resistivity substrate for future mixed analog-digital application, *VLSI Tech Symp Dig*., pp. 158-159. 2002.

[2.1.3] E. C. Park, S. H. Baek, T. S. Song, J. B. Yoon, and E. Yoon, Performance Comparison of 5GHz VCOs Integrated by CMOS Compatible High Q MEMS Inductors, *IEEE MTT-S Int Microwave Symp Dig*, 2003, pp. 721-724.

[2.1.4] A. Chin, K. Lee, B. C. Lin, and S. Horng, Picosecond photoresponse of carriers in Si ion-implanted Si, *Appl Phys Lett*. vol.69, 1996, pp. 653-656.

[2.1.5] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, S. C. Pai, C. C. Chi, and C. P.

Liao, RF loss and cross talk on extremely high resistivity (10K-1M-cm) Si fabricated by ion implantation, *IEEE MTT-S Int Microwave Symp Dig.*, 2000, pp. 241-244.

[2.1.6] K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin, Transmission line noise from standard and proton-implanted Si, *IEEE MTT-S Int Microwave Symp Dig.*, 2001, pp. 763-766.

[2.1.7] K. T. Chan, A. Chin, Y. B. Chen, Y.-D. Lin, D. T. S. Duh, and W. J. Lin, Integrated Antennas on Si, Proton-Implanted Si and Si-on-Quartz, *International Electron Devices Meeting (IEDM) Tech Dig.*, 2001, pp. 903-906.

[2.1.8] K. T. Chan, A. Chin, S. P. McAlister, C. Y. Chang, V. Liang, J. K. Chen, S. C. Chien, D. S. Duh, and W. J. Lin, Low RF loss and noise of transmission lines on Si substrates using an improved ion implantation process, *IEEE MTT-S Int Microwave Symp Dig.*, Vol. 2, 2003, pp. 963-966.

[2.1.9] K. T. Chan, A. Chin, J. T. Kuo, C. Y. Chang, D. S. Duh, W. J. Lin, C. X. Zhu, M. F. Li, and D. L. Kwong, "Microwave Coplanar Filters on Si Substrates, *IEEE MTT-S Int Microwave Symp Dig.*, vol. 3, 2003, pp. 1909-1912.

[2.2.1] K. Chang, Microwave ring circuits and antennas, New York: John Wiley &

Sons, 1996.

[2.2.2] L. Zhu, and K. Wu, A joint field/circuit model of line-to-ring coupling structures and its application to the design of microstrip dual-mode filters and ring resonator circuits, *IEEE Trans Microwave Theory Tech.*, (1999), vol. 47, No. 10, 1938-1948.

[2.2.3] H. Yabuki, M. Sagawa, M. Matsuo, and M. Makimoto, Stripline dual-mode ring resonators and their application to microwave devices, *IEEE Trans. Microwave Theory Tech.*, (1996), Vol. 44, No. 5, 723 -729.

[2.2.4] T. Ohguro, K. Kojima, H. S. Momose, S. Nitta, T. Fukuda, T. Enda, and Y. Toyoshima, Improvement of high resistivity substrate for future mixed analog-digital application, *VLSI Tech Symp Dig.*, 2002, pp. 158-159.

[2.2.5] E. C. Park, S. H. Baek, T. S. Song, J. B. Yoon, and E. Yoon, Performance comparison of 5GHz VCOs integrated by CMOS compatible high Q MEMS inductors, *IEEE MTT-S Int Microwave Symp Dig.*, 2003, pp. 721-724.

[2.2.6] K. T. Chan, A. Chin, J. T. Kuo, C. Y. Chang, D. S. Duh, W. J. Lin, C. X. Zhu, M. F. Li, and D. L. Kwong, Microwave coplanar filters on Si substrates, *IEEE MTT-S Int Microwave Symp.*, 2003, pp. 1909-1912.

[2.2.7] K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin, Transmission

line noise from standard and proton-implanted Si, *IEEE MTT-S Int Microwave Symp. Dig.*, 2001, pp. 763-766.

[2.2.8] K. T. Chan, A. Chin, Y. B. Chen, Y.-D. Lin, D. T. S. Duh, and W. J. Lin, Integrated antennas on Si, proton-implanted Si and Si-on-quartz, *Int Electron Devices Meeting (IEDM) Tech. Dig.*, 2001, pp. 903-906.

[3.1.1] T. Edwards, Foundations for Microstrip Circuits Design, New York: John Wiley & Sons, 2nd Ed., chap. 5. (1992)

[3.1.2] J.-T. Kuo and E. Shih, Wideband band-pass filter design with three-line microstrip structures, *Int'l Microwave Symp. Dig.,* Phoenix, Arizona, USA, 2001.

[3.1.3] G. L. Mattaei, L. Young, and E. M. T. Jones, Microwave Filters, Impedance-Matching Network, and Coupling Structures. Norwood, MA: Artech House, 1980.

[3.1.4] K. C. Gupta, R. Garg, and I. J. Bahl, Microstrip Lines and Slotlines. Norwood, MA: Artech House, 1979, chap. 3.

[3.1.5] D. M. Pozar, Microwave Engineering, New York: John Wiley & Sons, 2nd Ed., 1998, chap. 8.

[3.1.6] M. Velazquez-Ahumada, J. Martel, F. Medina, Parallel coupled microstrip filters with ground-plane aperture for spurious band suppression and

enhanced coupling, *IEEE Trans. Microwave Theory Tech.52*, 2004, pp. 1082-1086.

[3.1.7] K. Chang, Microwave ring circuits and antennas, New York: John Wiley & Sons, 1996.

[3.1.8] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, S. P. McAlister and D. L. Kwong, RF Passive devices on Si with excellent performance close to ideal devices designed by electromagnetic simulation, *Int'l Electron Devices Meeting (IEDM) Tech. Dig*., 2003, pp. 375.

[3.1.9] K. T. Chan, A. Chin, J. T. Kuo, C. Y. Chang, D. S. Duh, W. J. Lin, C. X. Zhu, M. F. Li, and D. L. Kwong, Microwave Coplanar Filters on Si Substrates, *IEEE MTT-S Int'l Microwave Symp. Dig.,* 2003, pp. 1909-1912.

[3.1.10] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, S. C. Pai, C. C. Chi, and C. P. Liao, "RF loss and cross talk on extremely high resistivity (10K-1MΩ-cm) Si fabricated by ion implantation," in *IEEE MTT-S Int'l Microwave Symp*. Dig 1, 2000, pp. 221-224

[3.1.11] K. T. Chan, A. Chin, S. P. McAlister, C. Y. Chang, V. Liang, J. K. Chen, S. C. Chien, D. S. Duh, and W. J. Lin, Low RF loss and noise of transmission lines on Si substrates using an improved ion implantation process, *IEEE*

MTT-S Int'l Microwave Symp. Dig., 2 2003, pp. 963-966.

[3.2.1] D. M. Pozar, Microwave Engineering, John Wiley & Sons, New York, (1998), 2nd Ed.

[3.2.2] S. D'Agostino and C. Paoloni, Design of high-performance power-distributed amplifier using Lange couplers, *IEEE Trans. Microwave Theory Tech.*, vol. 42, 1994, pp. 2525 – 2530.

[3.2.3] C. Y. Chi and G. M. Rebeiz, Design of Lange-couplers and single-sideband mixers using micromachining techniques, *IEEE Trans. Microwave Theory Tech.*, vol. 45, 1997, pp. 291 – 294.

[3.2.4] Y. Konishi, I. Awai, Y. Fukuoka and M. Nakajima, "A directional coupler of vertically installed planar circuit structure," *IEEE Trans. Microwave Theory Tech.*, vol. 36, 1988, pp. 1057 – 1063.

[3.2.5] M. Nakajima and E. Yamashita, "A quasi-TEM design method for 3 dB hybrid couplers using a semi-reentrant coupling section," *IEEE Trans. Microwave Theory Tech.*, vol. 38, 1990, pp. 1731 – 1737.

[3.2.6] F. Masot, F. Medina and M. Horno, Analysis and experimental validation of a type of three-microstrip directional coupler, *IEEE Trans. Microwave Theory Tech.*, vol. 42, 1994, pp. 1624 – 1631.

[3.2.7] K. Sachse and A. Sawicki, Quasi-Ideal multilayer two- and three-strip

sirectional couplers for monolithic and hybrid MIC's, *IEEE Trans. Microwave Theory Tech.*, vol. 47, 1999, pp. 1873 – 1882.

[3.2.8] K. T. Chan, A. Chin, Y. D. Lin, C. Y. Chang, C. X. Zhu, M. F. Li, D. L. Kwong, S. McAlister, D. S. Duh, and W. J. Lin, Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process, *IEEE Microwave & Wireless Components Lett.*, vol. 13, 2003, pp. 487-489.

[3.2.9] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, RF passive devices on Si with excellent performance close to ideal devices designed by Electro-Magnetic simulation, in *Int'l Electron Devices Meeting (IEDM) Tech. Dig.,* (2003), pp. 375-378.

[3.2.10] Zeland Software Inc., IE3D simulator, (1997).

[4.1.1] H. Iwai, "Future semiconductor manufacturing- Challenges and opportunities," in *IEDM Tech. Dig.*, 2004, pp. 11-16

[4.1.2] M. Brillouët, "Emerging technologies on silicon," in *IEDM Tech. Dig.*, 2004, pp. 11-16.

[4.1.3] A. Chin and S. P. McAlister, "The power of functional scaling: beyond the power consumption challenge and the scaling roadmap," *IEEE Circuit &*

Devices Magazine, Jan/Feb. 2005.

[4.1.4] D. S. Yu, Albert Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, W. J. Yoo, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with Novel IrO_2(Hf) Dual Gates and High-κ Dielectric on 1P6M-0.18μm-CMOS," in *IEDM Tech. Dig.*, 2004, pp. 181-184.

[4.1.5] B. P. Shieh, L. C. Bassman, D.-K. Kim, K. C. Saraswat, M. D. Deal, J. P. McVittie, R. S. List, S. Nag, and L. Ting, "Integration and reliability issues for low capacitance air-gap interconnect structures," in *IEEE Int. Interconnect Technology Conference (IITC)* Dig., 1998 , pp. 125-127.

[4.1.6] D. S. Yu, K. T. Chan, A. Chin, S. P. McAlister, C. Zhu, M. F. Li, and Dim-Lee Kwong, "Narrow-Band Band-pass Filters on Silicon Substrates at 30 GHz," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2004, vol. 3, pp. 1467-1470.

[4.1.7] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "RF passive devices on Si with excellent performance close to ideal devices designed by Electro-Magnetic simulation," in *IEDM Tech. Dig.*, 2003, pp. 375-378.

[4.1.8] K. T. Chan, A. Chin, Y. B. Chen, Y.-D. Lin, D. T. S. Duh, and W. J. Lin,

"Integrated Antennas on Si, Proton-Implanted Si and Si-on-Quartz," in *IEDM Tech. Dig.*, 2001, pp. 903-906.

[4.1.9] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, S. C. Pai, C. C. Chi, and C. P. Liao, "RF loss and cross talk on extremely high resistivity (10K-1MΩ-cm) Si fabricated by ion implantation," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2000, vol. 1, pp. 221-224.

[4.1.10] T. Ohguro, K. Kojima, H. S. Momose, S. Nitta, T. Fukuda, T. Enda, and Y. Toyoshima, "Improvement of high resistivity substrate for future mixed analog-digital application," in *Symp. On VLSI Tech. Dig.,* 2002, pp. 158-159.

[4.1.11] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, C. Jahnes, C. Uzoh, E. J. O'Sullivan, K. K. Chan, M. Soyuer, P. Roper, and S. Cordes, "Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrates," in *IEDM Tech. Dig.*, 1996, pp. 99-102.

[5.1.1] J. Kim, Y. Qian, G. Feng, P. Ma, M. F. Chang, and T. Itoh, "Millimeter-wave silicon MMIC interconnect and coupler using multilayer polymide technology," *IEEE Trans. Microwave Theory Tech.*, vol. 48, 2000, pp. 1482-1487.

[5.1.2] A. Triantafyllou, A. Farcy, P. Benech, F. Ndagijimana, J. Torres, O. Exshaw, C. Tinella, O. Richard, C. Raynaud, "High transmission performance integrated antennas on SOI substrate for VLSI wireless interconnects," *Int. Interconnect Technology Conference (IITC)*, 2005, pp. 80-82.

[5.1.3] J. W. Joyner, P. Z. Ha, J. D. Meindl, "Global interconnect design in a three-dimensional system-on-a-chip." *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 12, Issue 4, pp.367 – 372, 2004.

[5.1.4] K. T. Chan, A. Chin, Y. B. Chen, Y. D. Lin, T. S. Duh, and W. J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-quartz," *IEDM Tech. Dig*., 2001, pp. 903-906.

[5.1.5] S. B. Cohn, "Parallel-Coupled Transmission-Line-Resonator Filters," *IEEE Trans. Microwave Theory Tech.*, vol. 6, pp. 223-231, 1958.

[5.1.6] Y. Eo, W. R. Eisenstadt, J. Y. Jeong, and Oh-Kyong Kwon, "A New On-Chip Interconnect Crosstalk Model and Experimental Verification for CMOS VLSI Circuit Design, *IEEE Trans. on Electron Devices*, vol. 47, 2000, pp. 129-140.

VITA

姓名：陳家忠

性別：男

出生年月日：民國 67 年 11 月 16 日

籍貫：台灣省基隆市

住址：基隆市信二路 174 巷 39 號 4 樓

學歷：中原大學電子工程系

（85 年 9 月~89 年 7 月）

中原大學電子工程研究所碩士班

（89 年 7 月~91 年 9 月）

交通大學電子工程研究所博士班

（91 年 9 月入學）

論文題目：

高頻被動元件在矽基板和多層介電質基板之模型與特性

(The Characteristics and Models of High Frequency Passive Devices on Silicon and PCB Substrates)

PUBLICATION LISTS

(A) International Journal:

[1]. **C. C. Chen**, H. L. Kao, A. Chin, S. P. McAlister and C. C. Chi, "AC Power Loss and Signal Coupling in VLSI backend Interconnects," in Journal of Japanese Applied Physics (JJAP), Vol. 45. 4B, 2006.

[2]. **C. C. Chen**, H. L. Kao, K. C. Chiang**,** A. Chin, "A Parallel Coupled-Line Filter Using VLSI Backend Interconnect with High Resistivity Substrate," in International Journal of Infrared and Millimeter wave, Feb. ,2006.

[3]. H. L. Kao, A. Chin, C. C. Liao, **C. C. Chen**, S. P. McAlister, C. C. Chi, "Electrical Stress Effects and Devices Modeling of 0.18 μm RF MOSFETs," in IEEE Transaction on Electron Devices, pp. 636-642, 2006.

[4]. D. S. Yu, C. C. Liao, **C. C. Chen,** C. F. Lee, C. F. Cheng, A. Chin, S. P. McAlister, and, "Reducing AC Power Consumption by Three-Dimensional Integration of Ge-On-Insulator CMOS on 1-Poly-6-Metal 0.18-μm Si MOSFETs," J. Electrochem. Soc., 148**,** pp. F73-F75, 2001.

[5]. **C. C. Chen**, B. F. Hung, Albert Chin, and S. P. McAlister, "High Performance Bulk And Thin-Film Microstrip Transmission Lines On VLSI-Standard Si Substrates". Microwave & Optical Technology Letter, pp. 148-151, 2004.

[6]. **C. C. Chen**, B. F. Hung, Albert Chin, and S. P. McAlister, "High Performance CPW and Microstrip Ring Resonators on Silicon Substrates". Microwave & Optical Technology Letter, pp. 511-514, 2004.

[7]. **Chia-Chung Chen**, Jen-Tsai Kuo, Meshon Jiang, Albert Chin, "A Fully Planar Microstrip Coupled-Line Coupler with a High Coupling Level". Microwave & Optical Technology Letter, pp.170-172, 2006.

[8]. **Chia-Chung Chen**, Jen-Tsai Kuo, Meshon Jiang, Albert Chin, "Study on Parallel Coupled-Line Microstrip Filter in Broadband". Microwave & Optical Technology Letter, pp. 373-375, 2006.

[9]. **C. C. Chen**, H. L. Kao, Albert Chin, "Electric Stress Effect of DC-RF Performance Degradation 0.18 μm MOSFETs". Microwave & Optical Technology Letter, October, 2006.

(B) International Conference:

[1]. **C. C. Chen**, Albert Chin, M. T. Yang, Sally Liu, "High Performance Band-Pass Filter Embedded into SoCs Using VLSI Backend Interconnects and High Resistivity Silicon Substrate," IEEE International Interconnect Technology Conference (IITC), 2006.

[2]. **C. C. Chen**, C. C. Liao, H.L. Kao, A. Chin, S.P. McAlister and C.C. Chi, "AC Power Loss and Signal Coupling in VLSI backend Interconnects," in

International Solid State Devices and Materials (SSDM), pp. 570-571, 2005.

[3]. **Chia-Chung Chen**, Jen-Tsai Kuo, Chih-Yuan Tsai and Albert Chin, "High performance ring resonators on PCB with a large bandwidth and low insertion loss," in Asia-Pacific Microwave Conference Proceedings (APMC), pp. 1042-1045, Nov. 19-22, 2003.

[4]. Albert Chin, H. L. Kao, Y. Y. Tseng, D. S. Yu, **C. C. Chen**, S. P. McAlister, C. C. Chi, "Physics and Modeling of Ge-on-Insulator MOSFETs," European Solid State Device Research Conf, (ESSDERC), Grenoble-France, September 12-16, 2005.

[5]. Albert Chin, **C. C. Chen**, C. C. Laio, D. S. Yu, K. C. Chiang, W. J. Chen, M. F. Li, W. J. Yoo, C. Zhu, and G. Samudra,"3D Integration Metal-Gate/High-k CMOS for Both DC and AC power Consumption Solution" Symposium on Nano Device Technology (SNDT), May 3~5,2005.