國立交通大學

電控工程研究所

碩士論文

量化器超載模型與模組設計最佳化運用

在離散時間積分三角類比數位轉換器

Quantizer Overload Model and Model-based Design Optimization for Discrete-Time Sigma-Delta Modulators

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中華民國九十九年九月

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摘要

摘要:

在離散時間積分三角調變器規格設計上，通常都依賴模擬化設計方法。然而，由於在模擬化設計中會需要進行積分三角調變器的行為模擬，因此如果使用模擬化方法去設計積分三角調變器則十分的耗時。然而使用演算法去降低資料的數量，存在著結果可能不夠理想的風險。本論文中，我們提出模組化積分三角調變器最佳化設計方法。此方法可以在極短時間之內計算出積分三角調變器所需要的規格，使得積分三角調變器可以得到最小的功率消耗以及最大的訊號對雜訊和失真比例。而且因為模組化設計方法非常的省時，因此在做積分三角調變器最佳化當中，不需要使用演算法去降低計算量。不過，使用模組化積分三角調變器最佳化設計上，會出現量化器超載問題；此問題我們將在之後的章節進行討論。此外，本論文還會提出一個數位類比電路失真模型。最後將針對兩個已發表的設計範例去驗證模組化積分三角調變器設計的可行性。

Quantizer Overload Model and Model-based Design Optimization for Sigma-Delta Modulators

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ABSTRACT

The conventional high-level SDM synthesis is mainly based on behavior simulation which is very time-consuming. This paper is the first one in the literature to propose model-based SDM synthesis. Model-based approach can be at the order of 10^4 times faster than simulation-based approach, but it is never realized before due to the incompleteness of non-ideality models. The recent establishment of settling noise model and OTA distortion model facilitates model-based SDM designs. Nonetheless, new problems associated with model-based approaches arise, notably overload on quantizers. In this paper, a SDM input estimator is proposed to avoid quantizer overload. In addition, a SDM design optimization scheme is proposed, which incorporates a DAC distortion model. Either the DAC distortion model is used, or data weighting average (DWA) power is estimated. This model-based optimization is tested against two published SDM designs, achieving higher *SNDR* and lower power results in a much shorter design time.

誌謝 Acknowledgment

我要將此論文獻給

我親愛的母親-李淑美 女士

最疼我的父親-歐聰榮 先生

若沒有他們，我不可能有機會完成此篇論文，並且從交通大學碩士班畢業。此外，必須感謝指導教授陳福川博士兩年來嚴格的督促與指導，讓我學會做研究的方法與心態，以及英文程度上的提升。另外，也要感謝口試委員廖德誠教授、洪浩喬教授與趙昌博教授對本篇論文所給予的建議與指導。

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Symbols

V_{LSB}	Quantizer step size
V_{OS}	Maximum output swing of op-amp
OSR	Oversampling ratio
n	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling frequency
f_B	Signal bandwidth
V_{ref}	Reference voltage of the quantizer
A_0	Finite gain of OTA
f_{in}	Frequency of the input signal
A_{in}	Amplitude of input signal
$\sigma_{jit.}$	Standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
V_S	Input signal plus feedback DAC signal
T	Absolute temperature
R_{on}	Switch on resistance
$\sigma_{cap.}$	Standard deviation of mismatch of unit capacitance
K	Boltzmann's constant (1.38×10^{-23}) J/K
Erf	Error Function
SR	Op-amp slew-rate
GBW	Op-amp gain bandwidth
h	Comparator hysteresis
V_{ov}	Overdrive voltage
f_{cr}	Corner frequency
$\varepsilon_{cap.}$	Capacitor mismatch error
C_U	Unit DAC capacitor
a_1	The gain of first stage integrator in 2nd order SDM
V^2_{nOTA}	Input-referred PSD of OTA
$\overline{a}$	The value of activated unit DAC
$-\overline{a}$	The value of deactivated unit DAC

e_k	Activated mismatch error of unit DAC
$-e_k$	Deactivated mismatch error of unit DAC
μ	Finite dc-gain error
σ	Standard deviation
V_{SW}	Swing of quantizer input node
C_{eq}	Equivalent capacitor of integrator

1
Introduction

1.1 Background, Current Status, Motivation and Aims

Sigma-Delta modulator (SDM) A/D converter is the most popular topology for high resolution applications because the SDM is implemented by feeding back quantization signal which reduces the quantization noise power [1]. Besides, the SDM is essential for system-on-chip (SoC) design, due to smaller area and lower power consumption [2]. The SDM can be implemented by continuous-time (CT) or discrete-time (DT). DT SDM with switch-capacitor (SC) implementation is much more popular than CT SDM because CT SDM suffers from problems such as sensitivity of clock jitter and excess loop delay [3]. We will focus on the design of SC SDM in this research.

In SDM designs, the designer needs to adjust design parameters so that high *SNR* or *SNDR* [4] can be achieved. The design parameters include oversampling ratio (OSR), sampling capacitor, op-amp gain bandwidth, op-amp slew-rate, op-amp DC-gain, quantizer bit number, etc. The variation of any single design parameter can potentially affect several noises and distortions in different ways, and may change system power consumption. For example, increasing OSR can reduce quantization noise, but increases settling noise and power consumption. It is typically a complex task to adjust all design parameters to come up with a good design. Currently, the design tasks rely heavily on simulation tools. Conventional circuit simulator (SPICE) provides high accuracy, but it takes too long simulation time. In order to overcome this problem, various SDM simulators have been developed such as circuit-based macro models [5], time-domain macro models [6], finite difference equation [7], table-lookup models [8] and behavior simulation technique [9], [10]. The circuit-based macro models are equivalent circuits made from components available in the circuit simulator. It increases the

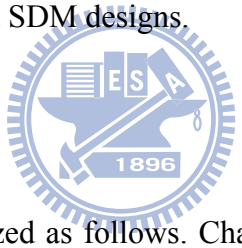
speed over circuit simulator but still needs too much time for simulation. The time-domain macro models are based on the time-domain equations used to describe the circuit transient behavior. Although it produces quick simulation and can model dynamic error, this approach is not flexible. The finite difference equations model is based on the z-transfer function of SDM. It produces the quickest simulation time. However, the capability for modeling non-idealities is poor. The table-lookup model is quick, but not flexible [11], [12]. Recently, behavior simulation technique provides good accuracy, high speed and more flexibility [2], [11]. In the early period, the behavior simulator used event-driven behavior simulation techniques [13]-[15]. In these techniques, the behavior simulators are implemented in C-language. Therefore, the block models can't be easily modified [2]. Recently, in order to overcome this problem, the most popular approach is to implements the behavior simulation in MATLAB Simulink environment [2], [3], [16]-[18]. On the other hand, there exist behavior simulations by using VHDL-AMS and Verilog-A [19]-[23]. The VHDL-AMS behavior simulation provides faster simulation time than MATLAB Simulink [23] and the Verilog-A behavior simulation can provide many choices between accuracy and efficiency [22]; however, to date, both simulations are not popular enough for SDM designs. Since behavior simulation is very time consuming, in order to search for adequate design parameter combinations at much lesser cost, recently techniques related to simulated annealing [2] and generic algorithm [14], [24] have been employed. However, the designs obtained in such cases are suboptimal.

This thesis is the first one in the literature to propose model-based SDM design method. In contrast to simulation-based designs reviewed above, model-based designs can potentially be at the order of 10^4 times faster. Model-based designs can also explicitly compute each noise power and distortion power, greatly enhancing design process, while simulation-based designs only generates sum of noise and distortion powers.

Model-based designs require that all relevant noise models and distortion models be available. During the past two decades, most non-ideality models have been developed [4, 13,

27, 28, 29], except that models for op-amp nonlinear DC-gain distortion and settling noise were critically lacking. This is the reason model-based SDM design has never materialized. Recently, however, both the nonlinear DC-gain distortion power model and the settling noise power model have been proposed in [25] and [26] respectively. Thus model-based design becomes possible. Nonetheless, new problems associated with model-based design surface, notably the overload problem.

The overload issue is due to quantizer overload may seriously degrades SDM performance. In this research, we establish model to estimate maximum SDM input signal allowed such that quantizer overload problem can be avoided. A model-based design optimization algorithm is also proposed, which is applied to a previously published SDM design task to demonstrate capability and advantage of model-based design method. The model can significantly improve model-based SDM designs.



1.2 Organization

The rest of chapters are organized as follows. Chapter 2 describes all non-idealities noise and distortion power models of 2nd order single loop SDM and MASH SDM. Chapter 3 presents the new problems associated to model-based designs. Chapter 4 presents the design optimization scheme and two examples for high-level synthesis of DT SDM based on model-based design. Chapter 5 presents the conclusion of this thesis.

2

Discussion about Non-idealities Noise and Distortion Models of 2nd Order Single Loop SDM and MASH SDM

Model-based high-level SDM designs employ only mathematical models. In this chapter, we will first check about the availability of noise and distortion models against all non-idealities in SDM, which are functions of design parameters. Important design parameters are listed in TABLE 2.1. Modification to existing models will be made wherever needed. We will propose a DAC distortion power model since no DAC distortion model is available up to date. The models discussed in this section are for the popular single-loop two-stage SDM structure shown in Fig. 2.1. Models for MASH and other SDM structures are also discussed in the rest of section of this chapter.

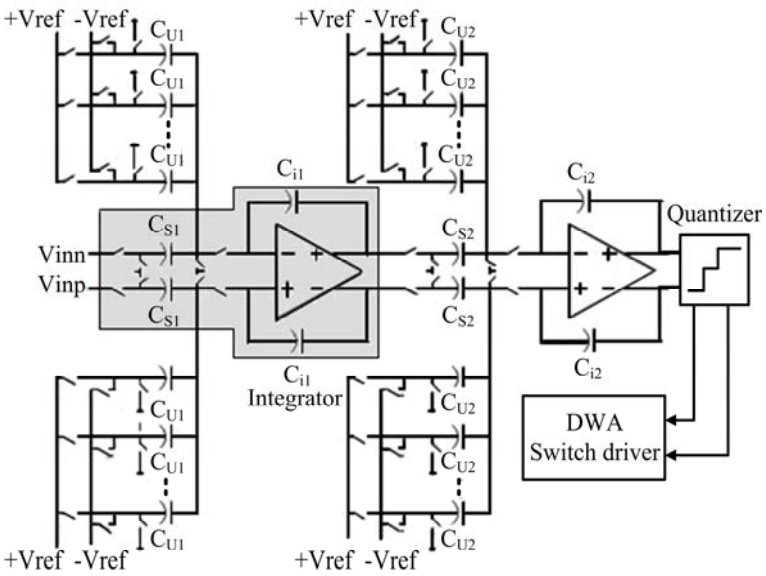
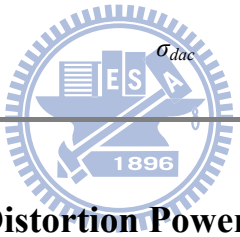


Fig. 2.1 Circuit topology of 2nd order single loop SC SDM

TABLE 2.1

Important SDM design parameters

Symbol	Design parameters	Symbol	Design parameters
B	bit number	V_{ov}	overdrive voltage
OSR	oversampling ratio	V_{ref}	quantizer reference voltage
GBW	op-amp gain bandwidth	f_{cr}	corner frequency
SR	op-amp slew-rate	R_{on}	switch on resisance
C_S	first stage integrator sample capacitance	ε_{cap}	capacitor mismatch error
A_{in}	input signal amplitude	f_B	input signal frequency
A_0	op-amp DC-gain	V_{os}	op-amp output swing
σ_j	sampling uncertainty	C_i	first stage integrator integral capacitance
h	comparator hysteresis	σ_{dac}	standard deviation of DAC capacitor mismatch error



2.1 SDM Noise Power and Distortion Power Models

For the 2nd-order switch capacitor SDM shown in Fig. 2.1, major circuit non-idealities are listed below:

1) Switches non-idealities;
2) Capacitors non-idealities;
3) Finite and nonlinear DC-gain;
4) Bandwidth and slew rate;
5) OTA noises;
6) Clock jitter effect;
7) Comparators;
8) Multi-bit DAC non-idealities.

The non-idealities of (1)-(5) are related to integrators. The non-idealities of (6)-(8) are from

outside of integrators. In the following, noises and distortions power models related to each of eight nonidealities are discussed.

1) *Switch Non-idealities*

- *Switch thermal noise power model* ($P_{Switch\_thermal}$) [4, 13]. $P_{Switch\_thermal}$ from switches before C_U and C_S. The Power Spectrum Density (PSD) of switch thermal noise at SDM output is derived as $8KT/C_S$. Therefore, the in-band switch thermal noise power is

$$P_{Switch\_thermal} = \int_{-f_B}^{f_B} \frac{8KT}{C_S} df = \frac{1}{OSR} \frac{8KT}{C_S} \qquad (2.1)$$

- *Nonlinear switch resistance distortion power model* ($P_{Switch\_distortion}$) [4]. The switch on-resistance is nonlinear because its value depends on input signal. The related SDM output distortion power $P_{Switch\_distortion}$ can be obtained from [27].

- *Clock-feedthrough*. The clock-feedthrough is caused by the charge of the gate-to-source capacitors of the switch that is injected to the sampling capacitor when switch turns off. This error can be attenuated by fully differential integrator [3].

- *Charge injection*. Charge injection is due to the charge of mobile channel injected to the sampling capacitor when the switch turns off. This error can be solved by widely used circuit technology [3].

2) *Capacitors Non-idealities*

- *Capacitor mismatch noise power model* ($P_{Cap\_mismatch}$). ε_{cap} can alter integrator gain from its nominal value, resulting in SDM output noise power $P_{Cap\_mismatch}$ [13].

- *Capacitor nonlinearity distortion power model* ($P_{Cap\_distortion}$). The capacitor C_S

introduces harmonic distortion because its capacitance depends on the input signal. The related SDM output distortion power $P_{Cap\_distortion}$ is derived in [13] under the assumption that the gain of the second stage equals to 1.

3) *Finite and Nonlinear DC-gain*

- *Finite DC-gain noise power model* ($P_{Finite\_DC\text{-}gain}$). A_0 affects the noise transfer function, resulting SDM output noise power $P_{Finite\_DC\text{-}gain}$ [13].

- *Nonlinear op-amp DC-gain distortion power model* ($P_{DC\text{-}gain\_distortion}$). A_0 is nonlinear because it varies with integrator output voltage. The related SDM output distortion power $P_{DC\text{-}gain\_distortion}$ can be obtained from [25] related to A_0 and V_{os}.

4) *Bandwidth and Slew-Rate*

- *Settling noise power model* ($P_{Settling\_noise}$). The limited integrator *GBW* and *SR* make the voltage charge and discharge incomplete at integrator output, which causes SDM output noise power $P_{Settling\_noise}$ [26].

- *Slew-rate distortion power model* ($P_{Settling\_distortion}$). If input signal of integrator is so large that it exceeds the integrator *SR* limitation, a dependency of the settling error on its input is created, which results slew-rate distortion. The related SDM output distortion power $P_{Settling\_Distortion}$ can be obtained from [13].

5) *OTA Noises*

- *OTA thermal noise power model* ($P_{OTA\_thermal}$). The OTA thermal noise originates from the MOSFET non-idealities of OTA. The input-referred noise PSD is formed as V_{nOTA}^2 [4, 38]. the in-band OTA thermal noise power at SDM output can be derived as

$$P_{OTA\_thermal} \cong \frac{1}{a_1^2 OSR}\int_0^{\infty} V_{nOTA}^2 \cdot (\left|H_{samp}(f)\right|^2 + \left|H_{\text{int}}(f)\right|^2)df \qquad (2.2)$$

where a_1 is equal to $C_{S1}/C_{i1,}$ and $H_{samp}(f)$ and $H_{int}(f)$ are the transfer functions from noise source to integrator output in sampling phase and integration phase respectively.

- *Flicker* $(1/f)$ *noise power model* ($P_{OTA\_flicker}$). The flicker noise also originates from the MOSFET non-idealities of OTA. The related SDM output noise power $P_{OTA\_flicker}$ can be obtained from [28] related to f_{cr}.

- *Reference circuit noise power model* (P_{Ref_noise}). Reference circuit noise usually contains OTA thermal noise and flicker noise, appearing at reference voltage of DAC circuit in Fig. 2.1. The related SDM output noise power can be obtained from [28] and [4].

6) *Clock Jitter Effect* (P_{Jitter_noise}).

The clock jitter noise originates from σ_j in sampling phase, resulting in non-uniform sampling of converter input signal. The related noise power P_{Jitter_Noise} can be obtained from [29].

7) *Comparator Hysteresis*($P_{Hysteresis}$)

The h is defined as the minimum overdrive to change the comparator's output, which leads to a loss of performance of SDM. The related SDM output noise power $P_{Hysteresis}$ can be obtained from [29].

8) *Multi-bit DAC Non-idealities*

- *DAC noise power model* (P_{DAC_noise}). The DAC noise originates from the σ_{dac} (C_U). The related SDM output noise power P_{DAC_noise} can be obtained from [4].

- *DAC distortion power model* ($P_{DAC\_distortion}$). The DAC is nonlinear because the transfer function of DAC depends on the capacitance of C_U. A DAC nonlinear distortion power model is proposed in next section.

2.2 DAC Nonlinear Distortion Power Model

DAC distortion is related to component mismatch which is random in nature. Fig. 2.2 shows a block diagram of a common B-bit flash DAC [4]. The output $y_k(nT)$ of the kth unit DAC is defined as

$$y_k(nT) = \begin{cases} \bar{a} + e_k, & g_k(n) = 1 \\ -\bar{a} - e_k, & g_k(n) = 0 \end{cases} \qquad (2.3)$$

where $\bar{a}$ and $-\bar{a}$ are the values of the activated and deactivated kth unit DAC respectively, and e_k and $-e_k$ are the activated and deactivated mismatch error of the kth unit DAC respectively. The errors e_k and $-e_k$ are assumed to be Gaussian random variables with zero mean and same standard deviation $V_{ref} \cdot \sigma_{dac}$.

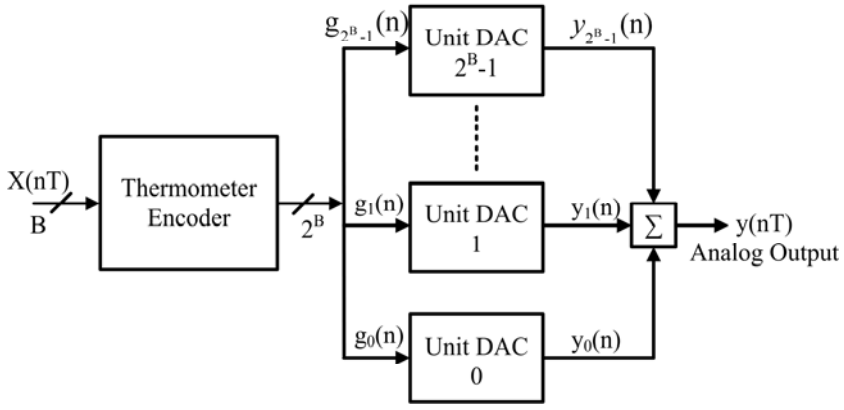


Fig. 2.2 A block diagram of a B-bit flash DAC

The DAC's analog output $y(nT)$ can be written as

$$y(nT) = \sum_{k=0}^{2^B-1} y_k(nT) \qquad (2.4)$$

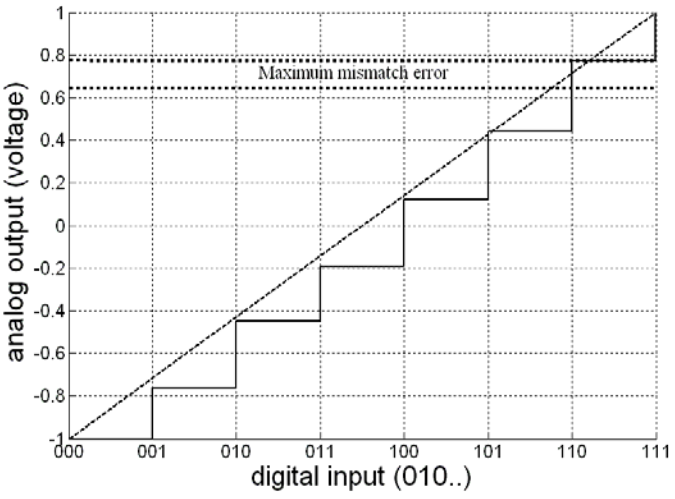
Assuming the thermometer encoder activates $x(n)$ unit DACs and deactivates the remaining 2^B-$x(n)$ unit DACs, (2.4) can be written as

$$y(nT) = \chi(n)\cdot\bar{a} + \sum_{k=1}^{x(n)} e_k - \left(2^B - \chi(n)\right)\cdot\bar{a} - \sum_{k=x(n)+1}^{2^B} e_k$$
$$= 2\chi(n)\cdot\bar{a} - 2^B\bar{a} + \sum_{k=1}^{x(n)} e_k - \sum_{k=x(n)+1}^{2^B} e_k \quad (2.5)$$

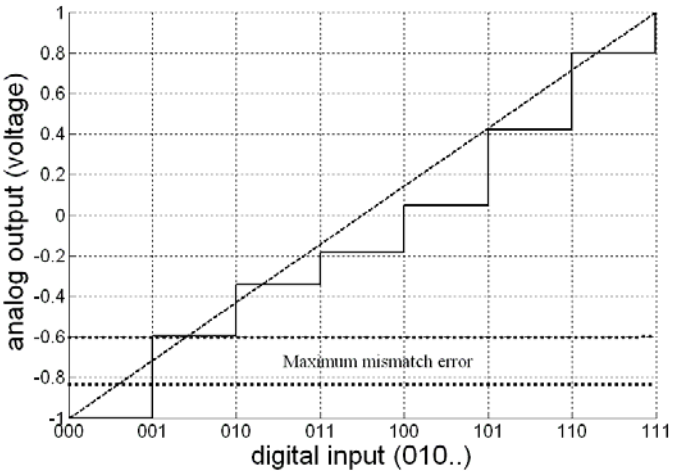
The variance of error in *y(nT)* is

$$\sigma^2[y(nT)] = \sigma^2[\sum_{k=1}^{x(n)} e_k + \sum_{k=x(n)+1}^{2^B} (-e_k)] = 2^B \cdot {V_{ref}}^2 \cdot {\sigma_{dac}}^2 \quad (2.6)$$

The characteristic of nonlinear DAC I/O transfer curve depends on two factors. The first is the DAC output error variance (2.6), as is demonstrated by Fig. 2.3 that larger output errors would result in an I/O curve which is more nonlinear. The second factor is the number of DAC output levels. Fig. 2.4 shows two I/O curves with the same output error variance, but Fig. 2.4 (b) is more nonlinear than Fig. 2.4 (a) because more levels in Fig. 2.4 (b) result in more variation.

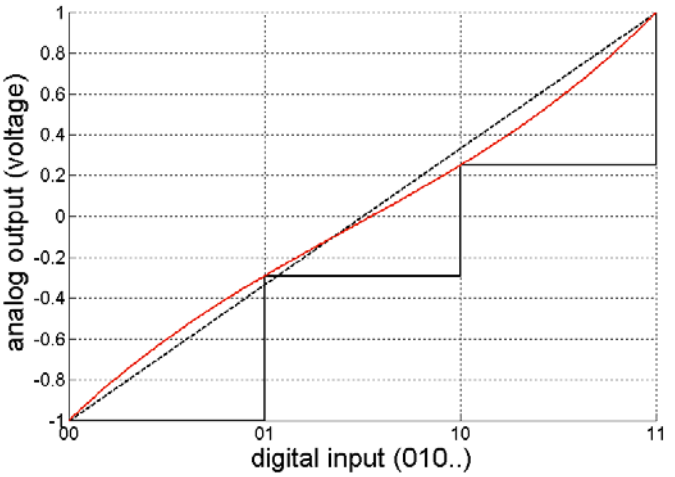


(a)

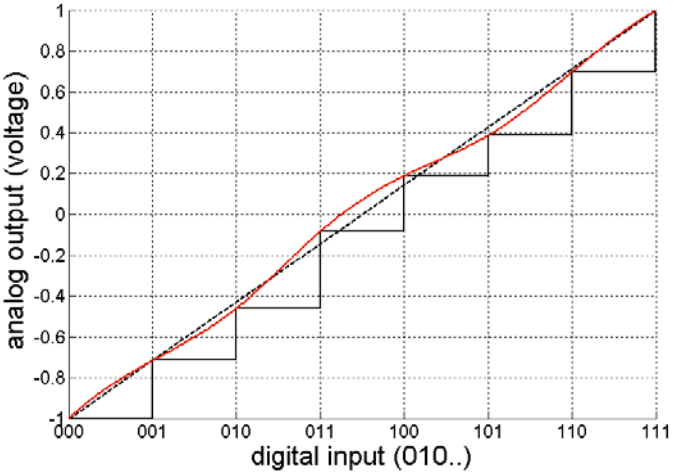


(b)

Fig. 2.3 DAC transfer curve: (a) DAC with smaller DAC output error, and (b) DAC with larger DAC output error



(a)



(b)

Fig. 2.4 DAC transfer curve: (a) DAC with fewer output levels, and (b) DAC with more output levels.

Accordingly, we propose to model DAC I/O relationship as

$$y(nT) = x(nT) + \Delta_{cap} \cdot \sin(a \cdot x(nT) + \theta) \qquad (2.7)$$

where Δ_{cap} is related to variation magnitude demonstrated by Fig. 2.3, a is related to variation frequency, and θ is a uniformly distributed random variable in $[0,2\pi]$ representing possible horizontal shift. Then, utilizing Taylor's series, (2.7) can be expanded as follows:

$$\begin{aligned} &\Delta_{cap} \cdot \sin(a \cdot x + \theta) \\ &= \Delta_{cap} \cos\theta \times \sum_{n=0}^{\infty} (-1)^n \frac{(ax)^{2n+1}}{(2n+1)!} + \Delta_{cap} \sin\theta \times \sum_{n=0}^{\infty} (-1)^n \frac{(ax)^{2n}}{(2n)!} \\ &= a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + \ldots \end{aligned} \qquad (2.8)$$

Suppose x in (2.8) is a sinusoidal input. The harmonics distortion powers in y of (2.7) can be derived as follows:

$$\begin{aligned} HD2_{DAC} &= \frac{1}{2}\left(\frac{a_2}{2\sin\theta} A_{in}^2 + \frac{a_4}{2\sin\theta} A_{in}^4 + \frac{15a_6}{32\sin\theta} A_{in}^6 + \cdots \right)^2 \cdot \sin^2\theta \\ HD3_{DAC} &= \frac{1}{2}\left(\frac{a_3}{4\cos\theta} A_{in}^3 + \frac{5a_5}{16\cos\theta} A_{in}^5 + \cdots \right)^2 \cdot \cos^2\theta \\ HD4_{DAC} &= \frac{1}{2}\left(\frac{a_4}{8\sin\theta} A_{in}^4 + \frac{3a_6}{16\sin\theta} A_{in}^6 + \cdots \right)^2 \cdot \sin^2\theta \end{aligned} \qquad (2.9)$$

Then, expressing the harmonics powers as their expected values, one obtains

$$\begin{aligned} E[HD2_{DAC}] &\cong 20\log\Delta_{cap} \cdot |-0.125a^2 A_{in}^2 + 0.010415a^4 A_{in}^4 - 0.0003255a^6 A_{in}^6| \\ E[HD3_{DAC}] &\cong 20\log\Delta_{cap} \cdot |-0.02083a^3 A_{in}^3 + 0.00130208a^5 A_{in}^5| \\ E[HD4_{DAC}] &\cong 20\log\Delta_{cap} \cdot |0.002604a^4 A_{in}^4 - 0.00013021a^6 A_{in}^6| \end{aligned} \qquad (2.10)$$

The expressions (2.10) suggest that, once Δ_{cap}, a, and A_{in} are fixed, DAC distortion powers are determined, and can be expressed as $P_{DAC\_distotion} = HD2_{DAC} + HD3_{DAC} + HD4_{DAC}$. For (2.10) to be useful, we need to establish Δ_{cap} and a as functions of σ_{dac} and u ($=2^B$) is the number of unit DAC in Fig. 2.2. Behavior simulations are employed for this task, which is shown in

Fig. 2.5,

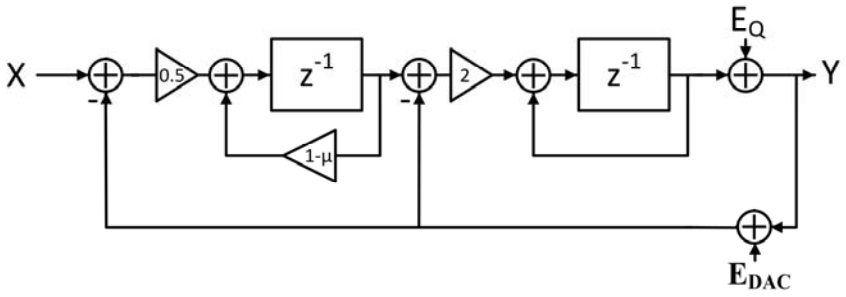


Fig. 2.5 Behavior simulation for DAC nonlinearity

where E_{DAC} is obtained from Eq. (2.4) for each level and μ represents the finite DC-gain error. The simulation results of various σ_{dac} and u combinations are shown in Table 2.2. Each harmonic distortion power listed in Table 2.2 is the average of results from twenty simulation runs. These twenty simulations differ only in DAC mismatch errors e_k which are generated from random number generators.

Table 2.2

Simulation results for various σ_{dac} and u combinations with A_{in}=0.5v

Std. deviation (σ_{dac})	Unit DAC number (u)	HD2 (dB)	HD3 (dB)	HD4 (dB)
0.3%	4	-56.43	-66.62	-76.01
0.3%	8	-47.46	-57.32	-61.71
0.1%	4	-69.88	-75.00	-87.92
0.1%	8	-60.16	-63.76	-75.12
0.025%	4	-83.58	-87.35	-108.7
0.025%	8	-72.77	-79.25	-84.60

By marking use of (2.10) and Table 2.2, after some efforts on comparison and calculation, we come up with the following equations:

$$\Delta_{cap} = 0.707 \cdot \sqrt{u} \times \sigma_{dac}$$

$$a = (0.59 A_{in}^{-0.8} + 0.263) \cdot (1.4667 + 0.125 \cdot u + 0.0084 \cdot u^2) \qquad (2.11)$$

Therefore, (2.10) and (2.11) constitute the complete model of our DAC distortion power

model. In order to check our model to see if it is generally correct, we compare our model (2.10), (2.11) with behavior simulation results for other σ_{dac} and u combinations to see if they closely match each other. Theoretical results from our model (2.10) and (2.11) and the corresponding simulation results are tabulated in Table 2.3.

Table 2.3

Theoretical results and simulation results for various σ_{dac} and u combinations with A_{in}=0.7v

σ_{dac} (%)	u	HD2 (dB) Simulation results	HD2 (dB) Theoretical results	HD3 (dB) Simulation results	HD3 (dB) Theoretical results	HD4 (dB) Simulation results	HD4 (dB) Theoretical results
0.2	4	-61.34	-57.24	-67.85	-68.68	-82.16	-82.68
0.2	8	-54.23	-49.91	-55.87	-58.09	-63.85	-68.57
0.125	4	-60.89	-61.32	-71.71	-72.76	-84.42	-86.77
0.125	8	-57.83	-53.99	-62.98	-62.18	-70.96	-72.65
0.05	4	-73.85	-69.28	-80.96	-80.72	-88.30	-94.73
0.05	8	-64.91	-61.95	-74.15	-70.14	-76.45	-80.61

The theoretical and simulation results are mostly close and they confirm that our DAC distortion model is reasonable one.

2.3 Non-idealities Models for MASH SDM Architecture

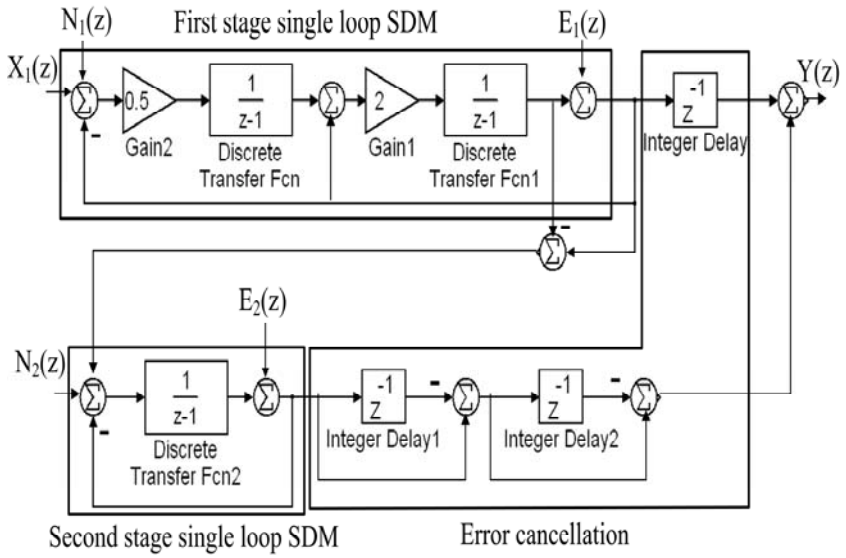


Fig. 2.6 2-1 Mash architecture of SDM

MASH architecture shown in Fig. 2.6 cascades low order single loops modulator in order to get high order noise shaping effect. The output can be derived as follow:

$$Y(z) = z^{-3}X_1(z) + z^{-3}N_1(z) + (1-z^{-1})^2 z^{-1}N_2(z) \qquad (2.12)$$

where $N_1(z)$ and $N_2(z)$ are the noises and equivalent distortions generated by first and second stage single loop SDM respectively. According to equation (2.12), the noises and equivalent distortions generated by second stage single loop SDM are subjected to noise shaping effect. Furthermore, the quantization noise of first stage single loop SDM is the input of second stage single loop SDM; hence SDM input signal will not affects the integrators of second stage single loop SDM. The harmonic distortion due to non-idealities in second stage single loop SDM can be significantly reduced [40]. For these reasons, the MASH output noise powers and nonlinear distortion powers are dominated by those of the first stage single loop modulator. Therefore, most MASH output non-ideality power models are the same as those discussed in Chapter 2, except finite DC-gain noise and capacitor mismatch noise. Models of finite DC-gain noise and capacitor mismatch noise need to be re-derived and they can be obtained from [28].

2.4 Non-idealities Models for Other Architecture

The Single-loop and MASH SDM discussed above are by far the most popular architectures. Non-ideality models for other special-purpose SDM architectures can also be systematically derived. In general, SDM non-idealities can be separated into two categories. Those in the first category are due to some noise sources; related power models can be derived by

$$Non\text{-}ideality\ Power = \int_{-f_B}^{+f_B} S_{noise}(f) \cdot |H(f)|^2 df \quad (2.13)$$

where $H(f)$ is the transfer function from noise source to SDM output, and $S_{noise}(f)$ is the PSD of noise source. Non-idealities in the second category involve some nonlinearity. Techniques used in [25], [26] and Appendix A can be reapplied to obtain power and distortion models.

3

Discussion of New Problems Associated to Model-Based Designs

The SDM design spec. is typically given in terms of *SNDR* (3.1). *SNDR* is defined as

$$SNDR = \frac{P_S}{P_N + P_D} \qquad (3.1)$$

where P_S represents the signal power, P_N the total noise power and P_D the total distortion power. In simulation-based high level SDM designs, P_N and P_D are generated from behavior simulations. In model-based approach, P_N is computed by summing up each SDM output noise power models described in Chapter 2, and P_D is computed by summing up each SDM output distortion power models described in Chapter 2. However, there are two issues associated with the computation of P_N and P_D:

1) Identifying essential models for model-based designs

   Not every noise or distortion power model discussed in Chapter 2 should be included in P_N or P_D because some noise or distortion power models can be greatly suppressed by various techniques. This issue will be discussed this chapter.

2) Quantizer overload problem

   Ideally, *SNDR* is proportional to input signal amplitude A_{in}. In practice, quantizer overload can significantly reduce *SNDR* after A_{in} grows certain point, as is shown in Fig. 3.1. This issue will be discussed this chapter.

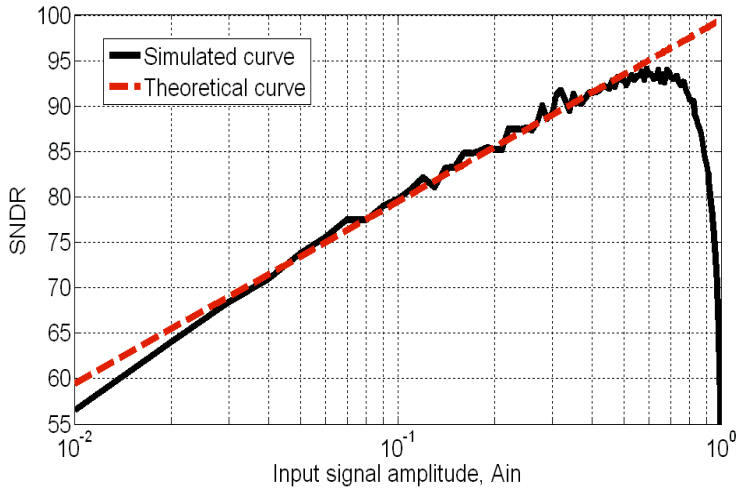


Fig. 3.1 The performance of *SNDR* versus SDM input signal amplitude

3.1 Identifying Essential Non-idealities Models for Model-Based Designs

Among the models reviewed in Chapter 2, $P_{Cap\_mismatch}$, $P_{OTA\_flicker}$, $P_{Cap\_distortion}$, $P_{Switch\_distortion}$, P_{Ref_noise}, $P_{Hysteresis}$ and $P_{Settling\_distortion}$ can be largely suppressed by various techniques. $P_{Cap\_mismatch}$ can be greatly limited by the present CMOS technologies providing the capacitor mismatch as good as 0.05%~1% [28]. $P_{OTA\_flicker}$ can be improved by decreasing the corner frequency, and can be further reduced by the cancellation techniques such as correlated double sampling, chopper stabilization, and autozeroing [28]. Recently, $P_{Cap\_distortion}$ can be improved by using stacked insulator structure of high-*K* and SiO_2 dielectrics such as HfO_2/SiO_2 stacked MIM capacitors [30]. $P_{Switch\_distortion}$ can be improved in many ways. One way is to adjust switches size; another way is to improve linearity by using low V_T devices or clock boosting techniques [35], [36], [37]. P_{Ref_noise} can be improved by connecting the large bypass capacitor to the voltage reference buffer [31]. $P_{Hysteresis}$ can be neglected in many cases because it subjects to the same noise shaping effect as quantization noise in SDM [12]. Finally, we verified that $P_{Settling\_distortion}$ is either negligible or orders smaller than $P_{Settling\_noise}$.

On the other hand, some of the models reviewed in Chapter 2 can be combined together. Due to finite-dc-gain may produce changes in noise transfer function and increase in-band quantization noise, $P_{Finite\_DC\text{-}gain}$ and $P_{Quantization\_noise}$ should be considered together and,

eventually, the modified quantization noise power for single-loop 2nd-order SDM could be formed as [13]:

$$P_{Modified\_quantization\_noise} = (\frac{V_{LSB}{}^2}{12})(\frac{\pi^4}{5OSR^5} + \frac{2\mu^2\pi^2}{3OSR^3}) \qquad (3.2)$$

where μ represents the finite DC-gain error, and $V_{LSB} = \frac{2V_{ref}}{2^B}$ represents the quantizer step size for mid-tread quantizer.

From the discussion above, the P_N and P_D in (3.1) can be determined as

$$\begin{aligned} P_N = {} & P_{Modified\_quantization\_noise} + P_{Switch\_thermal} \\ & + P_{OTA\_thermal} + P_{Jitter\_noise} + P_{DAC\_noise} + P_{Settling\_noise} \end{aligned} \qquad (3.3)$$

and

$$P_D = P_{DC\text{-}gain\_distortion} + P_{DAC\_distortion} \qquad (3.4)$$

3.2 Quantizer Overload Problem

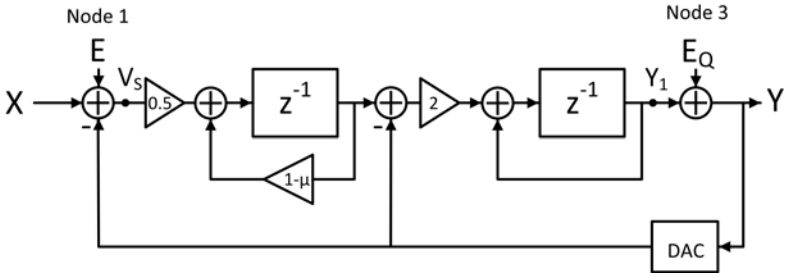


Fig. 3.2 The block diagram of 2nd-order single-loop SDM

If quantizer input amplitude exceeds V_{ref}, the $P_{Quantization\_noise}$ and $P_{Quantization\_distortion}$ will increase significantly, resulting in overload problem shown in Fig. 3.1. Overload problem can be easily avoided in behavior simulation because the magnitude of quantizer input can be easily observed. For model-based SDM designs, however, a method is needed to estimate the maximum SDM input amplitude allowed, in order to avoid quantizer overload problem.

To check the occurrence of overload, we need to observe signal Y_1 in Fig 3.2, which can be expressed as

$$Y_1(z) = z^{-2}X(z) + (z^{-2} - 2z^{-1})E_Q(z) + z^{-2}E(z) \qquad (3.5)$$

In (3.5), $Y_1(z)$ consists of three parts. First part is the SDM input $X(z)$ followed by unity gain transfer function; hence $X(z)$ directly affects Y_1 swing. Second part is white noise $E(z)$ followed by unity gain transfer function. This part can be neglected due to the magnitude of E is typically very small for median to high resolution SDM. For example, a 15 effective number of bit design results in white noise smaller than -80dB which equals to the variance of E; hence the standard deviation of E is

$$\sigma(E) = \sqrt{10^{-8}} = 10^{-4} \qquad (3.6)$$

Since E is typically of Gaussian distribution, the three sigma magnitude contains 99.73% of random number. The magnitude of E can be set as

$$3\sigma(E) = 3\sqrt{10^{-8}} = 0.0003 \qquad (3.7)$$

which is very small compared with X. Third part is the sum of two independent time sequences $e_q(n-2)$ and $2e_q(n-1)$, denoted by $q_1(x)$ and $q_2(y)$. The probability density functions (pdf) of q_1 and q_2 are shown in Fig. 3.3. Suppose $q(n)=q_1(x)+q_2(y)$, the distribution function of $q(n)$ is

$$F_q(n) = P(q_1 + q_2 \le n) = \int_{-\infty}^{\infty} \int_{-\infty}^{n-y} f_{q_1 q_2}(x, y)\,dx\,dy \qquad (3.8)$$

Taking the derivation with to the random variable n, we obtained

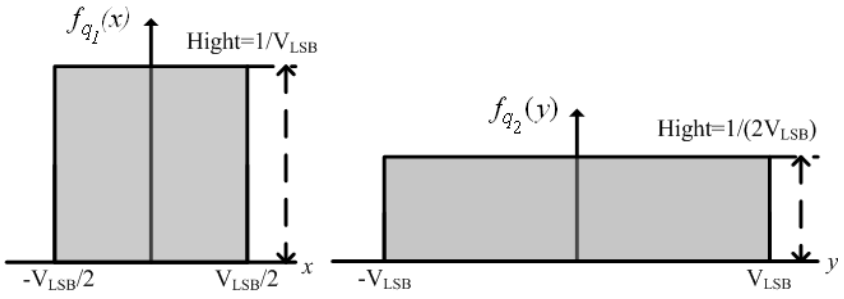
$$f_q(n) = \frac{d[F_q(n)]}{dn} = \int_{-\infty}^{\infty} f_{q_1 q_2}(n-y, y)\,dy \qquad (3.9)$$

Due to the random variable $q_1(x)$ and $q_2(y)$ are statistically independent, Eq. (3.9) is modified to be

$$f_q(n) = \int_{-\infty}^{\infty} f_{q_1 q_2}(n-y, y)\,dy = \int_{-\infty}^{\infty} f_{q_1}(n-y) f_{q_2}(y)\,dy \qquad (3.10)$$

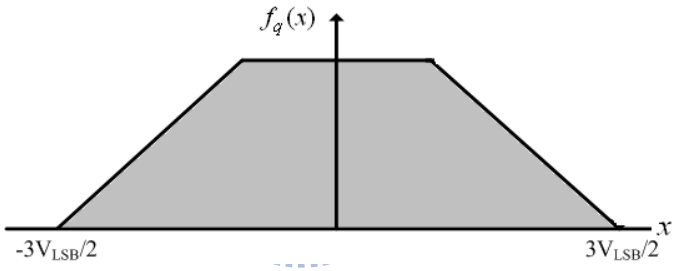
Eq. (3.10) indicates that the swing of node Y_1 can be obtained by convoluting $f_{q_1}(x)$ and $f_{q_2}(y)$, which is shown in Fig. 3.4 (a). Thus, the swing of node Y_1 due to quantization noise can be characterized as $3V_{LSB}/2$, where V_{LSB} has been defined before. This result has

been verified by behavior simulation. For V_{ref}=1 and B=2, the corresponding simulation result is shown in Fig. 3.4 (b).

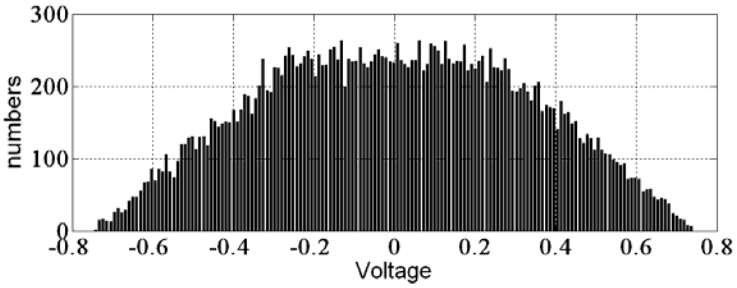


(a) (b)

Fig. 3.3 (a) $f_{q_1}(x)$ The pdf of $q_1(n)$ (b) $f_{q_2}(y)$ The pdf of $q_2(n)$.



(a)



(b)

Fig. 3.4 (a) The theoretical pdf of $q(n)$ (b) The simulated distribution of $q(n)$.

From discussions above, the signal swing at quantizer input can be estimated to be

$$V_{SW} = \frac{3V_{LSB}}{2} + A_{in} \qquad (3.8)$$

In order to avoid quantizer overload, V_{SW} needs to satisfy

$$V_{SW} \le V_{ref} + \frac{V_{LSB}}{2} \qquad (3.9)$$

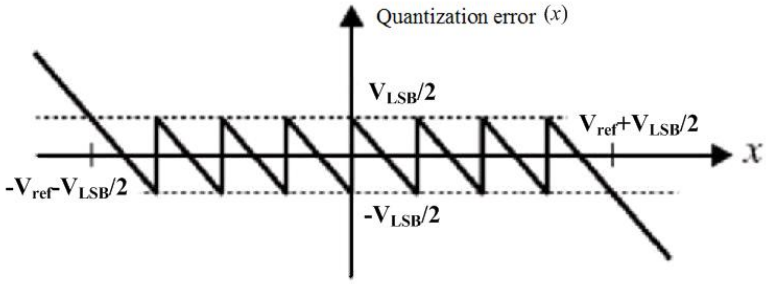


Fig. 3.5 Quantizer error function v.s quantizer input signal

Eq. (5) comes from the fact shown in Fig. 3.5 that quantizer error grows unbounded when V_{SW} exceeds the RHS of (3.9). When $B \geqq 2$, Eq. (3.9) determines the largest allowed A_{in} to be

$$A_{in} \le V_{ref} - V_{LSB} \qquad (3.10)$$

Eq. (3.9) is verified by behavior simulation w. r. t. different bit number with V_{ref}=1. The result is listed in Table 3.1.

TABLE 3.1

Simulation results and theoretical results for various B

Bit number	Simulation result of maximum allowed A_{in}	Theoretical result of maximum allowed A_{in}
2	0.56	0.5
3	0.81	0.75
4	0.9	0.875

The case for B=1 needs special attention, since quantizer overloads for all A_{in} except A_{in}=0. But it is indicated in [12] that the excess noise due to overloading the quantizer increases quite slowly; hence there is a margin linearly related to V_{ref} for one bit quantizer. We evaluated

this margin to be 0.36 V_{ref} by behavior simulation. Therefore, for one bit case, Eq. (3.10) is modified to be

$$A_{in} \leq 1.36V_{ref} - V_{LSB} \qquad (3.11)$$

4

An Example for High-Level Synthesis of DT SDM Based On Model-Based Designs

In this Chapter, we propose a methodology for model-based SDM design optimization. This design method is applied to a published design task [34]. Compared with the MASH SDM reported in [34], the SDMs designed by our method achieves much higher *SNDR* and significantly lower power consumption. This shows that our method can effectively achieve more balanced designs for piratical applications.

4.1 Design Optimization Schemes

A typical SDM design optimization algorithm is reference to [41]

4.2 Example for ΣΔ ADC for 14-bit 2.2-MS/s

The MASH SDM design specs reported in [34] to be achieved are

- Peak *SNDR* : 72 *dB*
- Signal bandwidth : 1.1 M*Hz*

According to [34], V_{ref} and V_{DD} are set at 1V and 3.3V for the 0.35-μm CMOS technology. Design parameter space searched by our model-based optimization scheme is

- *B*: 1 ~ 4
- *OSR*: 4~24
- C_S: 0.1 ~1.32 *pF*
- A_0: 45 ~ 53 *dB*
- *GBW*: 120 ~ 1000 *MHz*

- SR: 50 ~ 475 $V/\mu s$
- A_{in}: 0.1 ~ 1 V

The results published in [34] and that achieved from our methodology are all listed in Table VII.

TABLE 4.1
COMPARISONS OF OUR DESIGN RESULTS WITH THOSE IN [34]

Design parameters	**Reference [34]**	**K = 1**	**Unit**
B (second stage)	5	1	-
B (first stage)	1	2	
OSR	24	24	-
C_S	1.32	1.19	pF
A_0	53	53	dB
GBW	**1000**	**120**	MHz
SR	**475**	**150.8**	$V/\mu s$
A_{in}	0.55	0.47	V
$SNDR$ reported in [34]	72	-	dB
$SNDR$(Our model)	**75.64**	**82.897**	dB
$SNDR$(Simulink)	76.585	82.66	dB
$POWER$(Our model)	**207.14**	**24.0304**	mW

1. The optimization result compared to [34] demonstrates that our methodology helps designers to design MASH SDM. The concepts for designing MASH SDM focus on the optimization design of first stage single loop SDM and relax the design parameters on second stage single loop SDM, and the analysis of the optimization result compared to [34] is almost the same as the previous one. In addition, the modified quantization noise needs to be carefully taken into account due to the quantization noise rely heavily on the leakage of MASH SDM.

5
Conclusions

The main contributions in this paper are described in the following. First, an overview of the non-idealities power models of 2^{nd} order single loop SDM and MASH SDM was presented, which shows that mathematical models were quit complete for model-based designs. Then, the quantizer overload model could provide that the obtained results of A_{in} and *SNR* from model-based designs could be more similarly to realistic DT SDM, and could indicate the distribution of different nodes of SDM, which maybe helpful in statistical properties. Furthermore, model-based designs can potentially be at the order of 10^4 times faster, which can search much more design parameters combination than simulation-based designs over the same period. Model-based designs also can explicitly compute each noise and distortion power, which could demonstrate the dominate non-idealities for designers to reduce the non-idealities by adjusting design parameters or using some circuit techniques. The non-idealities power models are currently being developed for other SDM architectures.

Appendix

A.1 an Approach for Extracting Sine Wave Signal from Any Order SDM Output (Behavior Simulation)

The sine wave signal from the SDM output can be extracted by the following equations.

$$[\frac{T}{\int_0^T w(t)dt}\int_0^T 2*w(t)*(\sin(\omega(t-c))+N(t))*\cos(\omega t)dt]*\cos(\omega t)$$

$$+[\frac{T}{\int_0^T w(t)dt}\int_0^T 2*w(t)*(\sin(\omega(t-c))+N(t))*\sin(\omega t)dt]*\sin(\omega t)$$

$$=\{\frac{T}{\int_0^T w(t)dt}\int_0^T 2*w(t)*[\sin(\omega t)*\cos(\omega c)-\cos(\omega t)*\sin(\omega c)+N(t)]*\cos(\omega t)dt\}*\cos(\omega t)$$

$$+\{\frac{T}{\int_0^T w(t)dt}\int_0^T 2*w(t)*[\sin(\omega t)*\cos(\omega c)-\cos(\omega t)*\sin(\omega c)+N(t)]*\sin(\omega t)dt\}*\sin(\omega t)$$

$$=\{\frac{T}{\int_0^T w(t)dt}\int_0^T [2*w(t)*\sin(\omega t)*\cos(\omega t)*\cos(\omega c)-2*w(t)*\cos^2(\omega t)*\sin(\omega c)+2*w(t)*N(t)*\cos(\omega t)]dt\}*\cos(\omega t)$$

$$+\{\frac{T}{\int_0^T w(t)dt}\int_0^T [2*w(t)*\sin^2(\omega t)*\cos(\omega c)-2*w(t)*\cos(\omega t)*\sin(\omega t)\sin(\omega c)+2*w(t)*N(t)*\sin(\omega t)]dt\}*\sin(\omega t)$$

$$=\{0-2*0.5*\sin(\omega c)+0\}*\cos(\omega t)+\{2*0.5*\cos(\omega c)-0+0\}*\sin(\omega t)$$

$$=-\sin(\omega c)*\cos(\omega t)+\cos(\omega c)*\sin(\omega t)=\sin(\omega(t-c))$$

The SDM output expresses as $Sin(\omega(t-c))+N(t)$, $N(t)$ is the noise in SDM, $w(t)$ indicates window function and c is constant delay depending on the SDM order.

The MATLAB code is written as

```
signal=(N/sum(w))*sinusx(vout(1:N).*w,fnormal,N);
```

```
% Function of sinusx is used to extract sinusoidal
```

Function of sinusx:

```
function outx = sinusx(in,fnormal,n)
% in:           Input data vector
sinx=sin(2*pi*fnormal*[1:n]); % sin(W*N*T)
cosx=cos(2*pi*fnormal*[1:n]); % cos(W*N*T)
in=in(1:n);
a1=2*sinx.*in';
a=sum(a1)/n;
b1=2*cosx.*in';
b=sum(b1)/n;
outx=a.*sinx + b.*cosx;
```

A.2 Error Function

Settling noise power model [26] contains many integral equations which can be expended to increase the speed for model-based design. The hardest integral equation for expending is

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt.$$

Fortunately, such error function can be expended by Taylor series as

$$\mathrm{erf}(z) = \frac{2}{\sqrt{\pi}} \sum_{n=0}^{\infty} \frac{(-1)^n z^{2n+1}}{n!(2n+1)} = \frac{2}{\sqrt{\pi}} \left(z - \frac{z^3}{3} + \frac{z^5}{10} - \frac{z^7}{42} + \frac{z^9}{216} - \cdots \right)$$

This alternate form is very useful for increasing the speed for optimization designs.

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