國立交通大學

電機學院　電機與控制學程

碩士論文

應用在全載範圍高效率直流對直流升壓轉換器的電流模式合成控制技術

Current-Mode Synthetic Control (CSC) Technique for High Efficiency DC-DC Boost Converters Over a Wide Load Range

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中華民國九十九年十月

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摘　要

可攜式電子產品如手機、膝上型電腦和不同的多媒體設備使用電池作為主要能源。為了要延長電池壽命，攜帶式的裝置在待機時會進入睡眠模式，因此需要快速喚醒時間。所以快速的暫態響應和全載範圍維持高效率是常被要求的規格。

近年來，合成波調變機制常被用來增加系統的噪音餘度，使系統近乎一個無雜訊的漣波且系統的負載穩壓也可以藉由誤差放大器加入而提升。但是他導致系統包含了兩個極點而需要較複雜的補償方式。所以，本論文提出一個包含電流資訊的技術來簡化補償方式。

本論文提出一個運用在升壓轉換器的電流模式合成控制技術(current-mode synthetic control technique)可以加速升壓轉換器的暫態響應速度並在全載範圍維持高的轉換效率。這個技術類似於電流模式控制可以達到高的負載穩壓而且簡化電路不需要額外斜率補償機制。除此之外，由於類似遲滯電流模式控制，系統暫態響應可以提升。輕載時，由於與負載相關的頻率可達到高轉換效率。實驗結果顯示，載變化在 0A 到 400mA 時，輸出電壓的漣波可以維持在小於 50mV 且在負載在 10mA 時效率可以達到 90%以上。

關鍵字：遲滯電流調變控制(modulated hysteretic current control)，暫態響應(transient response)，波寬調變(pulse frequency modulation)

Current-Mode Synthetic Control (CSC) Technique for High Efficiency DC-DC Boost Converters Over a Wide Load Range

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Abstract

Portable electronics products such as cellular phones, laptops and diverse multimedia equipments use battery as the main power source. To extend battery life, portable devices stay in sleep mode with a very low static current but require a fast wake-up to reach the normal mode with a much higher operational current. Therefore, the suitable converter for the portable devices needs fast transient response from the standby mode to the normal mode, meanwhile, high efficiency is guaranteed over a wide range.

Recently, the synthetic-ripple modulator (SRM) is proposed to improve the noise immunity through the synthetic current ripple, which is a nearly noise-free ripple signal. The accuracy also can be enhanced by the error amplifier. But it causes the system contains two poles and needs a complex compensation network. Therefore, this paper presents a current-mode synthetic control (CSC) technique to include the current information to simplify the compensation network.

The proposed current-mode synthetic control (CSC) technique in the design of boost converters can improve the transient response time and maintain high conversion efficiency over a wide load range. The CSC technique has high accuracy similar to the current-mode control and doesn't need the slope compensation for simplicity. Besides, the transient response is also improved due to the current-mode hysteresis control. The load-dependent switching frequency at light loads results in high power conversion efficiency. Experimental results show that the output voltage ripple can be kept smaller than 50mV over a wide load current range from 0mA to 400mA with power conversion efficiency higher than 90% at load current of 10mA.

Keywords—modulated hysteretic current control (MHCC), transient response and frequency modulation.

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陳逸群

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Chapter 1

Introduction

Portable electronics products such as cellular phones, laptops and diverse multimedia equipments use battery as the main power source. To extend battery life, portable devices stay in sleep mode with a very low static current but require a fast wake-up to reach the normal mode with a much higher operational current. Therefore, the suitable converter for the portable devices needs fast transient response from the standby mode to the normal mode operation while high efficiency is guaranteed over a wide range. In this chapter, we will show the background and basic knowledge of power management system in chapter 1.1 firstly. The classification of power management circuits which including switching converters, linear regulators, and charge pump converters will show in chapter 1.2. The motivation will give in chapter 1.3. Finally, the thesis organization will show in chapter 1.4.

1.1 Background of Power Management System

With recent advances in integrated mixed-signal circuits and an increasing demand for low-power multifunction system-on-a-chip (SOC) and extended battery runtime, there is a strong need for the development of efficient on-chip power regulation and distribution. As shown in **Fig. 1**, the growing of battery energy is not enough to supplying power of chips in the future. That is to say, as increasing chip functionality and complexity will overrun available battery energy budget. To solve this problem, the straightforward method is increasing the quantity of power source. Unfortunately, it is not permitted for portable devices

because of convenience. In order to decrease the expenses, the power management systems are utilized to provide the specific regulated voltages without consuming unnecessary batteries.

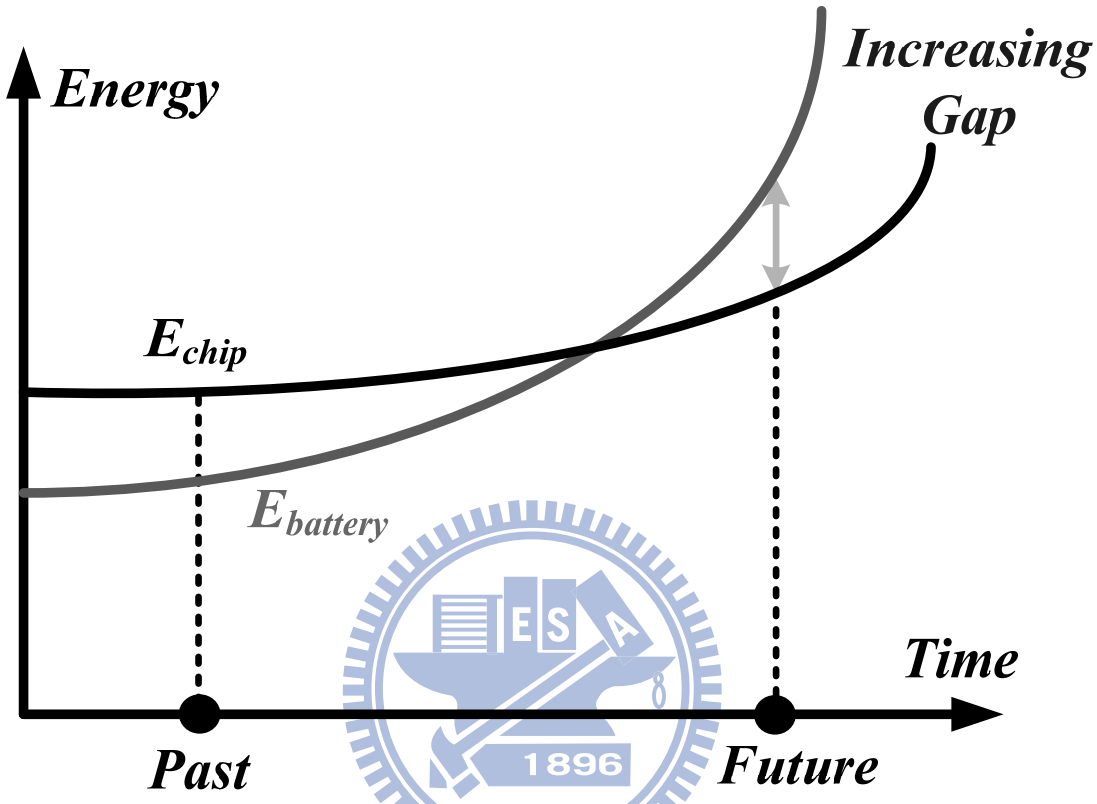


Fig. 1.Energy constrained operation.

As mention before, the best method of power saving and efficiency increasing is constructs power management system. The advantage of power management system not only generate regulated supply voltage for different specific integration circuits but also suppress the noise which is coupling from battery to electronic devices to extend battery's lifetime. Take cell phone for example, the basic power management system diagram of cell phone is shown in **Fig. 2 [1]**, a mobile phone may need at least five regulated voltages, one buck converter for DSP core CPU, high PSRR LDO regulators for RF power amplifier and low noise amplifier, one boost converter for color LCD panel, LDO regulators for analog base-band, audio and interface applications, and one charge pump for white light LED driver. The system of cell phone will operate in different modes, such as sleeping mode,

communication mode and so on. The control unit is needed to control the internal power management block enable or disable, respectively. That is to say, by using control unit can enhance system efficiency of power supply circuits, such as linear regulators, switching regulators and charge pumps. The ability of saving power and efficiency increasing, that is why power management system playing an important roles in the field of electronics, especially for portable devices.

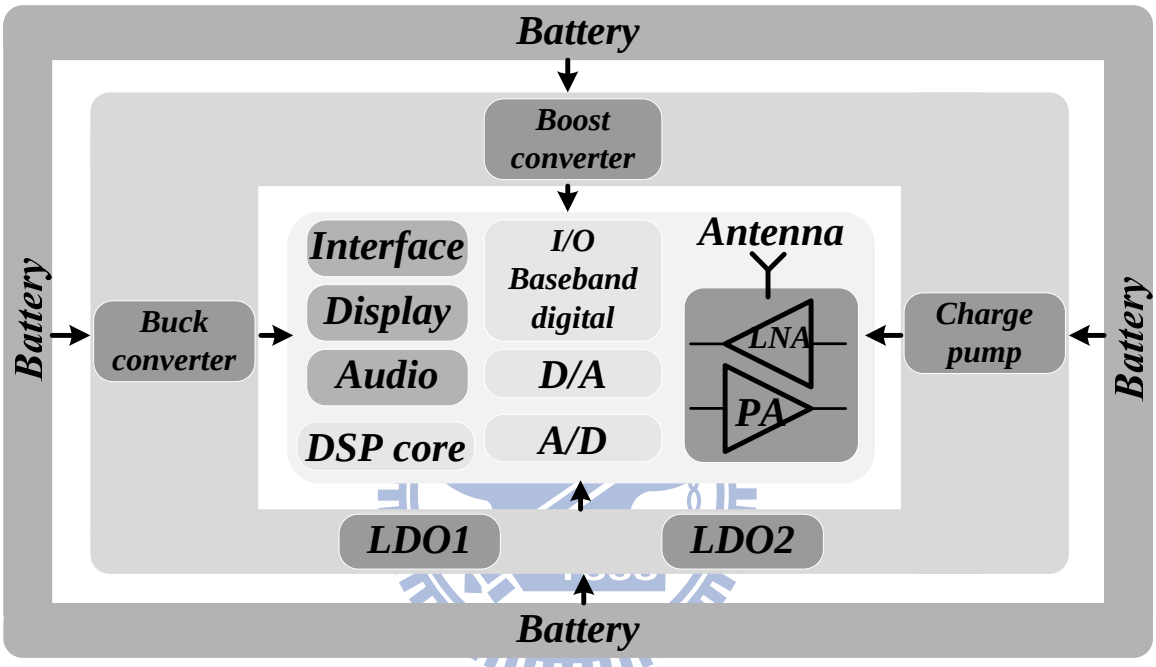


Fig. 2. Power management system diagram of cell phone.

1.2 Classification of Voltage Regulators

In this section, three kinds of voltage regulators will be introduced briefly, including linear regulators, switched capacitor circuits and switching regulators. Finally, a brief comparison will be given about three types of voltage regulators. The comparisons included circuit complexity, cost, efficiency, load ability and so on.

1.2.1 Linear Regulator

The basic structure of linear regulator is shown in **Fig. 3 [2]**, it also called low drop-out

(LDO) voltage regulator because there is a drop out voltage ($V_{dropout}$) between input and output pin about 100~500mV. The power MOSFET has equivalent resistor (R_{DS}) from input to output, so the power MOSFET size should be well designed to fit the regulated output voltage and load ability. The linear regulator main control circuit was error amplifier, it could adopt output voltage information form resistive feedback network (V_{FB}) then compare to reference voltage (V_{REF}). After error amplifier operation, it could immediately adjust input and output difference then control the gate of power MOSFET to supply load current.

The features of linear regulator are described as follows. Firstly, the linear regulator whole circuit is simple and compact, so the die size is smaller than other voltage regulators. And secondly, linear regulator is easy to use, instead of using inductor to transfer energy, the linear regulator just adding two capacitors at input and output pin respectively. As a result, it not only can reduces Printed-circuit board (PCB) area but also cost down. Thirdly, linear regulator only uses resistive feedback network and error amplifier output analogy signal to control power MOSFET, it doesn't use any switching base circuits. So this kind of regulator has no Electro Magnetic Interference (EMI) and no output ripple, there are very suit for audio, analog and RF circuit applications. Finally, because of without dual storage components, the linear regulator only can do buck regulation. The efficiency is proportional to output voltage and the highest efficiency occurs that output voltage is near to input voltage.

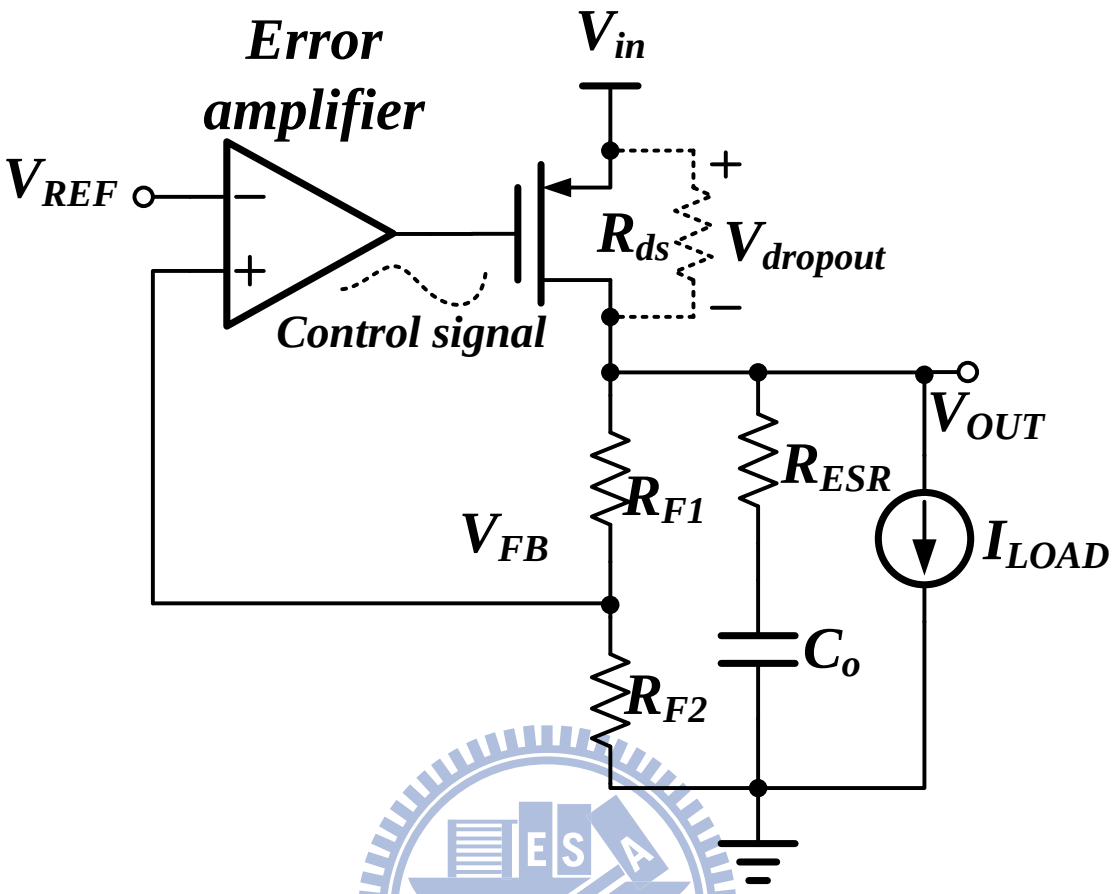


Fig. 3. The basic structure of linear regulator.

1.2.2 Charge Pump

The basic structure of two-phase charge pump regulator is shown in **Fig. 4 [3] [4]**. Power stage consists of capacitors (C_1 C_2) and switches (S_1 S_2 S_3 S_4). Detailed operation is described as follows, during the first phase, switches S_1 and S_2 turn on and switches S_3 and S_4. The input voltage charges capacitor C_1 to the input voltage level (V_{IN}). Than during the second phase, switches S_3 and S_4 turn on and switches S_1 and S_2. Because the capacitor C_1 still maintained the charge from the previous phase, the output voltage equals to input voltage adding voltage across the capacitor C_1, ideally obtains twice input voltage. Adding hysteric feedback control, the output can be regulated at desired voltage level.

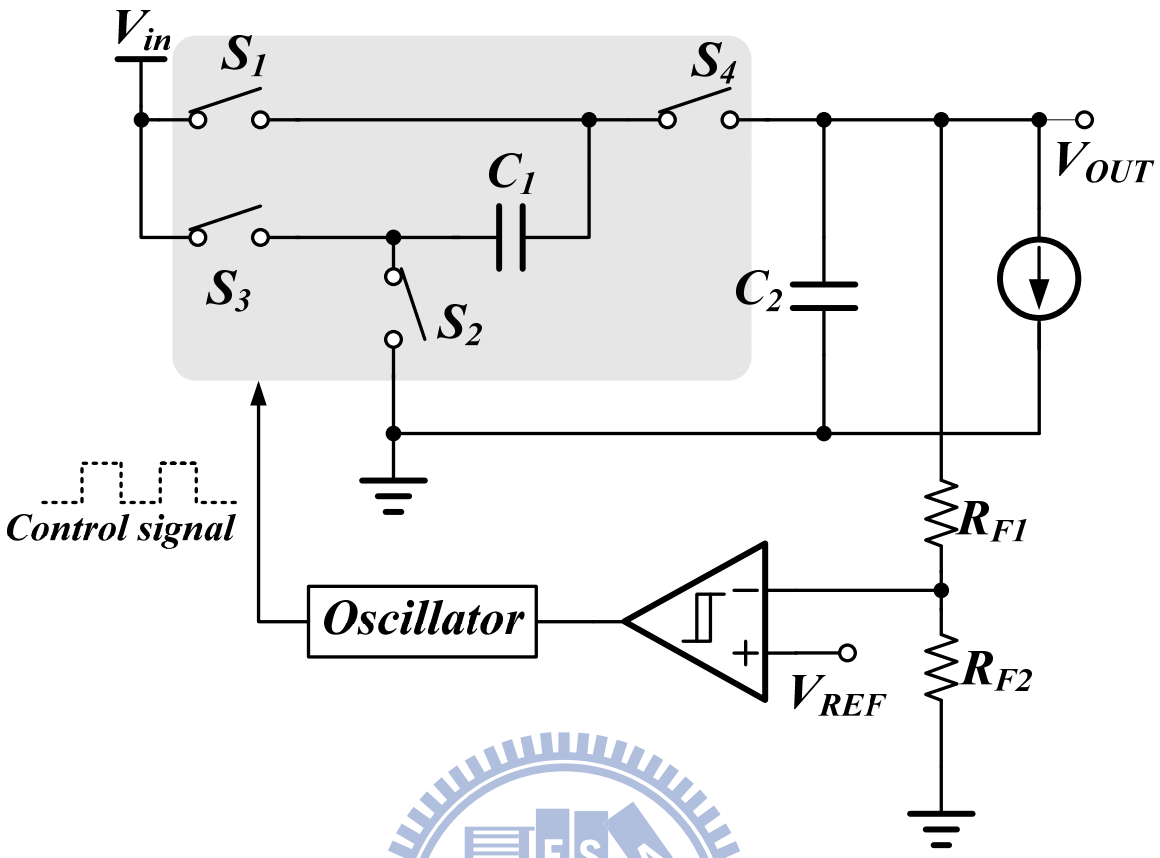


Fig. 4. The basic structure of charge pump.

The features of charge pump are described as follows. Firstly, the charge pump can be operated in both buck and boost types, it depended on the hysteric feedback control and reference voltage, but it's more efficiently at boost type. Secondly, the circuit complexity of charge pump is between linear regulator and switching regulator, which is more compact than switching regulator but more complicated than switching regulator. Thirdly, due to digital rail-to-rail switching clock control, the charge pump suffers from EMI and output noise problems. But this problem doesn't heavier than switching regulator because of lower operation frequency. Finally, the load ability of charge pump is weak because the ability depends on the output capacitor C_2 and switching frequency. That is to say, the larger output capacitor causes the powerful load ability. Because of light load ability typically, the charge pump is very suit for displaying applications, such as driving the gate of MOSFET to on or off.

1.2.3 Switching Regulator

The basic structure of boost type voltage mode switching regulator is shown in **Fig. 5 [5]**. The power stage of switching regulator consists of a couple of complementary power MOSFET ($\boldsymbol{SW_P}$ $\boldsymbol{SW_N}$), passive storage elements inductor ($\boldsymbol{L}$) and capacitor ($\boldsymbol{C_o}$) and resistive feedback network ($\boldsymbol{R_{F1}}$ $\boldsymbol{R_{F2}}$). Detailed operation is described as follows; the resistors $\boldsymbol{R_{F1}}$ and $\boldsymbol{R_{F2}}$ sensing the variation of output voltage and error amplifier receives the voltage variation information then brings the error signal ($\boldsymbol{V_{comp}}$). The comparator's inputs receive the error signal from error amplifier and the ramp signal ($\boldsymbol{V_{RAMP}}$) from ramp generator, then compares the quantity between the error signal and the ramp signal to decide the duty cycle. After generating the control signal, the PWM generator control the detail timing to avoid short through current. At last, the purposes of gate drivers are driving huge complementary power MOSFET. At the first subinterval, upper power MOSFET ($\boldsymbol{SW_P}$) turns off and lower power MOSFET ($\boldsymbol{SW_N}$) turns on then input voltage source charge the inductor. At the second subinterval, lower power MOSFET ($\boldsymbol{SW_N}$) turns off and upper power MOSFET ($\boldsymbol{SW_P}$) turns on then the inductor will discharge to the capacitor and load. By the above-mentioned, the switching regulator adjusts the output voltage error and regulates to correct voltage.

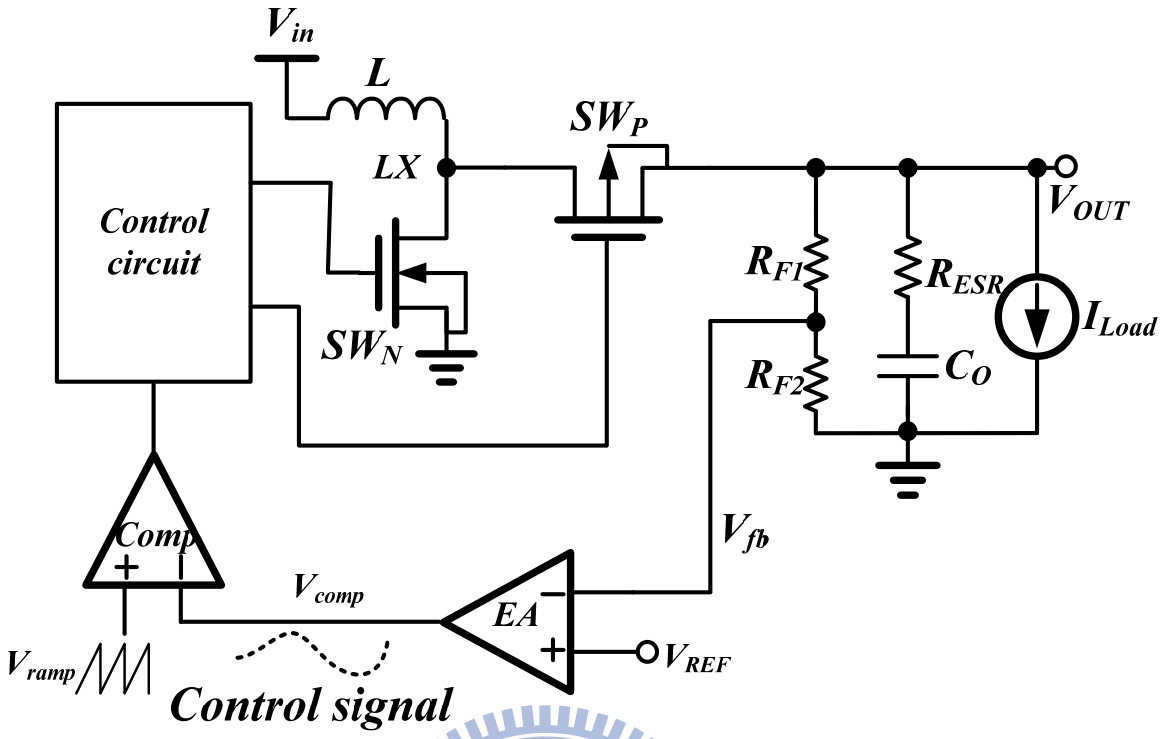


Fig. 5. The basic structure of boost type voltage mode switching regulator.

1.2.4 Comparison

As the above description, three types of voltage regulator have its own advantages and disadvantages. How to choose the best voltage regulator as power supply depend on the electronic applications characteristics and specifications. The comparison of different type voltage regulator is listed in **Table I**.

Table I. COMPARISONS OF DIFFERENT TYPE REGULATORS

Characteristics	*Linear Regulator*	*Switching Regulator*	*Charge Pump*
Regulation Type	***Buck***	***Buck/boost/buck-boost***	***Buck/boost***
Chip Area	***Compact***	***Large***	***Moderate***
Efficiency	***Minimum***	***Maximum***	***Medium***
EMI/Noise	***Minimum***	***Maximum***	***Medium***

Load ability	***Medium***	***Maximum***	***Minimum***
Complexity	***Simplest***	***Complicated***	***Medium***
Cost	***Low***	***High***	***Medium***

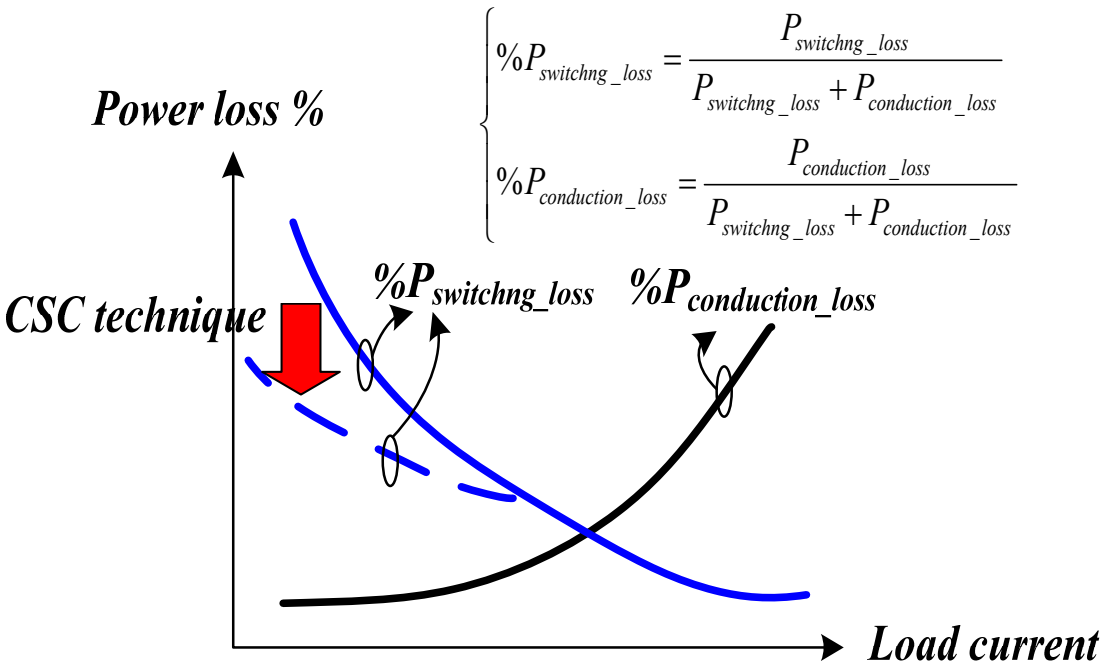
1.3 Motivation

Basically, the hysteresis control, which contains current-mode and voltage-mode controls, can meet the requirement since hysteresis control is self-stabilized and doesn't need any compensator if the equivalent series resistance (ESR) of output capacitor is large enough.

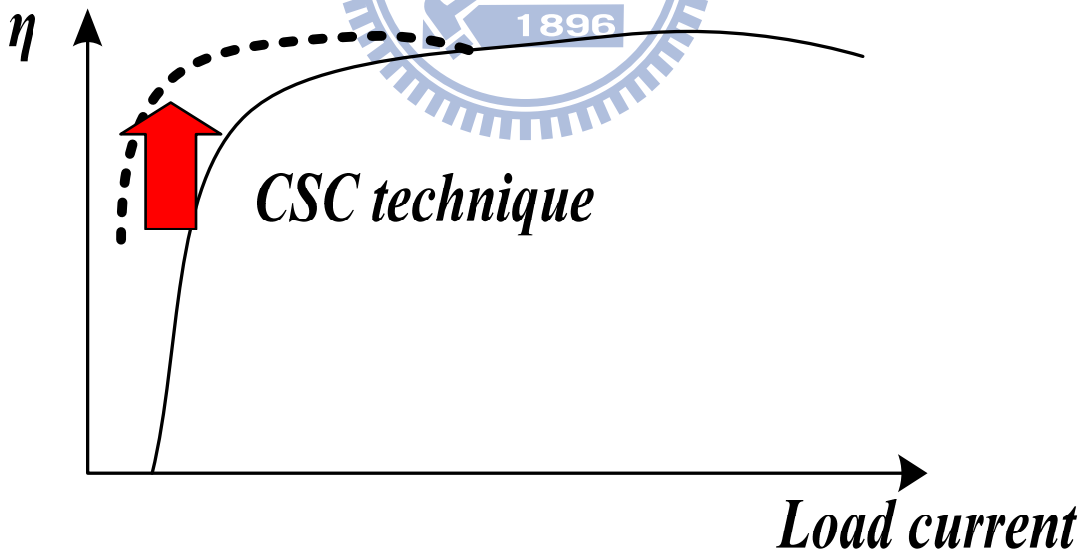
Current-mode and voltage-mode hysteresis controls have the advantages of simple structure and fast transient response. However, both controls have the accuracy problem owing to the lack of error amplifier. Besides, the current-mode control with fast line transient response has low noise immunity and worse load regulation owing to inductor current sensing and the lack of voltage loop, respectively, compared to the voltage-mode control. For example, the hysteresis current ripple regulator as depicted in **Fig. 7** has low noise immunity because of the full range inductor current sense. The noise immunity can be improved by the synthetic-ripple modulator (SRM) technique **[6]** as depicted in **Fig. 8** to generate a noise-free ripple signal. However, the SRM control system still contains two poles and thus has a complex compensation network.

Therefore, this paper presents a current-mode synthetic control (CSC) technique to include the current information to decide the charging time of the inductor current. Besides, the CSC technique contains the synthetic clock generator (SCG) to decide the switching frequency. The SCG circuit can maintain a constant switching frequency for the normal operation of the portable devices. On the other hand, in the standby mode, the SCG circuit can prolong the switching period to reduce the switching power loss. The high driving capability and high accuracy due to the usage of error amplifier can be ensured in the proposed CSC

technique. The performance is similar to the operation in current-mode pulse width modulation (PWM). At light loads, the decreasing switching frequency can effectively improve the power conversion efficiency. However, in the current-mode PWM control, the operation enters the discontinuous conduction mode (DCM) with a constant switching frequency. The switching power loss is still large. The prior arts provide multiple operation modes to achieve high efficiency over a wide load range **[7]**. Some literatures use the pulse frequency modulation (PFM) to reduce the switching frequency. But the optimum transition between PWM and PFM becomes another serious problem for high power conversion efficiency. Circuit complexity and power conversion efficiency need to be considered at the same in the design of high switching converters. Thus, the proposed CSC technique can reduce the switching frequency with the decreasing load condition. The CSC technique can smoothly change the variable switching frequency at light loads to the constant switching frequency at heavy loads without any complex circuit implementation. Different to the multiple operation modes, the transition point between the nearly constant switching frequency and the adjusted switching frequency is decided by the occurrence of zero inductor current. As depicted in **Fig. 6**, the switching power loss can be reduced and thus the power conversion efficiency can be greatly improved to maintain high efficiency over a wide load range.



(a)



(b)

Fig. 6. The CSC technique can (a) reduce the switching power loss and thus (b) improve the power conversion efficiency.

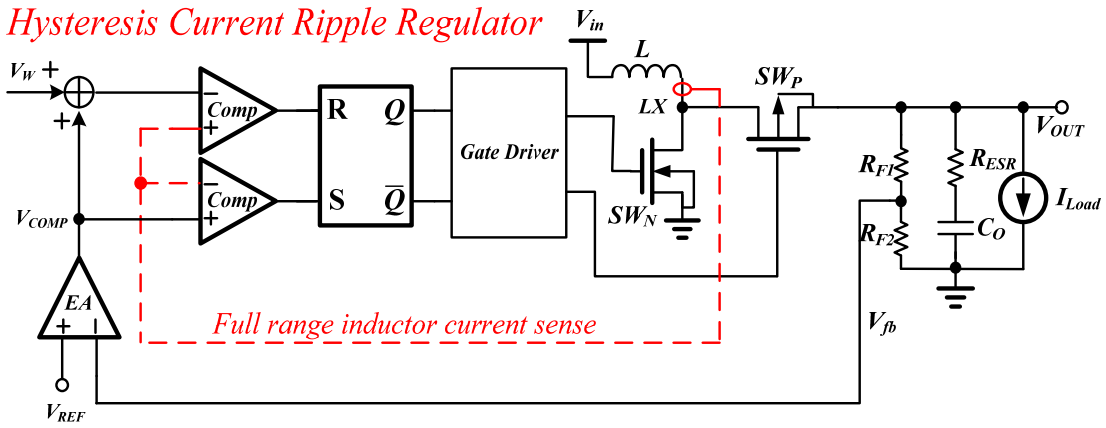


Fig. 7. The Hysteresis Current Ripple Regulator.

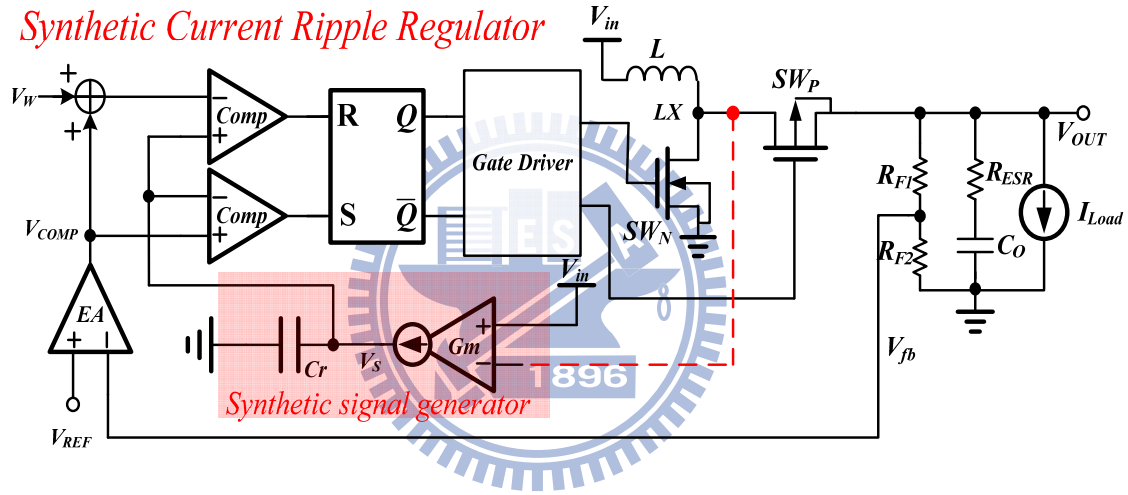


Fig. 8. The Synthetic Current Ripple Regulator.

1.4 Organization

The organization of this paper is as follows. Chapter 2 shows the small-signal analysis of the synthetic ripple control and improved CSC technique to propose the compensation method to ensure the system stability. Chapter 3 describes the operation of the proposed CSC technique. The internal overall circuit implementation and simulation results are shown in Chapter 4. Experimental results are shown in Chapter 5 to prove the performance and correctness of the proposed MHCC technique. Finally, a conclusion is made in Chapter 6.

Chapter 2

The Small-Signal Analysis and Compensation in CSC Technique

In the chapter 2, the topologies and principle of synthetic current ripple control and improved CSC technique presented. In section 2.1, the basic operation and disadvantage of Synthetic Current Ripple Regulator is introduced. In section 2.2, the small signal modeling of the traditional synthetic ripple control is introduced including. In section 2.3, the small signal modeling of the CSC technique modified is introduced including. The closed-loop with the PI compensation is introduced in the section 2.4.

2.1 Basic operation and disadvantage of Synthetic Current Ripple Regulator

As depicted in **Fig. 8**, the synthetic signal generator is used to generate synthetic signal for emulating inductor current ripple. The transduction, g_m, is used to transfer inductor voltage to current flow through capacitor, C_r. As a result, the inductor voltage is integrated then inductor current ripple is formed. Obviously, the DC level of inductor current is not involved in V_s. In other word, the path through transduction and C_r is not a current loop in the system. As a result, the system is still a voltage mode that has to be compensated by type III compensator. It will cause the huge area occupied by output component that we do not like to see. In section 2.3, a current path will be added to improve the compensate method, and the small signal modeling of synthetic current ripple regulator and current mode synthetic control will be

showed in next two sections.

2.2 Small Signal Modeling of the synthetic current ripple control

As depicted in **Fig. 9**, the synthetic current ripple control generate synthetic signal, i_S, and limits it within a hysteresis window, which defines the upper and lower current bands. The synthetic signal rises to reach the upper band of hysteresis window when the high-side MOSFET turns on during t_{on} period [8]. On the other hand, the synthetic signal falls to reach the lower band of hysteresis window when the low-side MOSFET turns on during t_{off} period. This synthetic current ripple control is simple and has fast dynamic characteristics except for electromagnetic interference (EMI) issue.

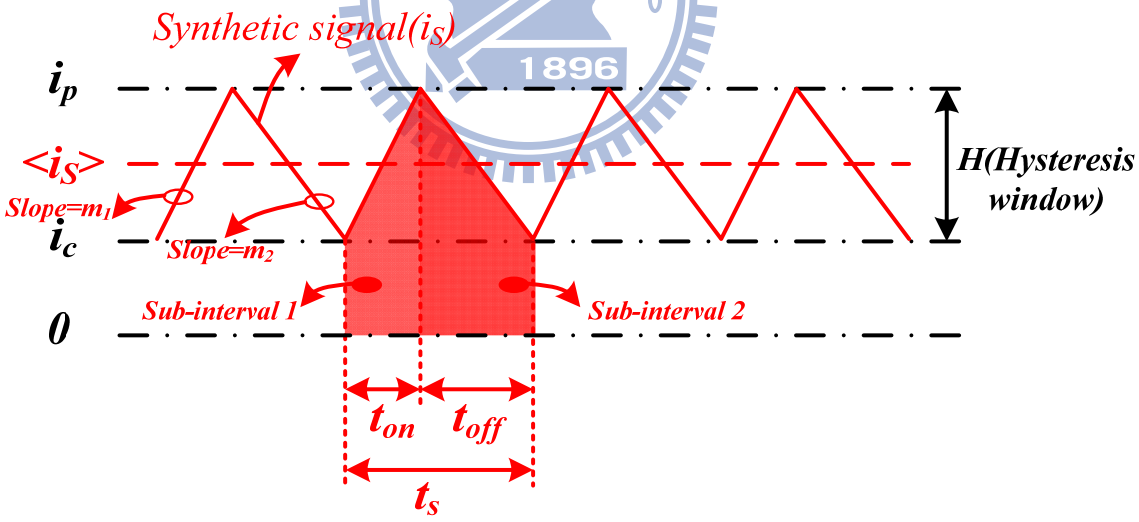


Fig. 9. The synthetic waveform is limited with the hysteresis window defined by the synthetic ripple control.

The switching period t_s as expressed in (1) is equal to the summation of on-time t_{on} and off-time t_{off} in the CCM operation. The value of t_{off} can be written as (2) according to the waveform in the sub-interval 2.

$$t_s = t_{on} + t_{off} \tag{1}$$

$$t_{off} = \frac{L \cdot H}{(v_{out} - v_{in})} \tag{2}$$

Considering the small signal analysis, the value of each variable can be written as the summation of the DC term and its perturbation as shown in (3) and (4).

$$\begin{aligned} T_s + \hat{t}_s &= T_{on} + \hat{t}_{on} + D'(T_s + \hat{t}_s) \\ &= T_{on} + \hat{t}_{on} + (1 - D - \hat{d})(T_s + \hat{t}_s) \end{aligned} \tag{3}$$

$$(T_{off} + \hat{t}_{off}) = \frac{L \cdot H}{(V_{out} + \hat{v}_{out} - V_{in} - \hat{v}_{in})} \tag{4}$$

Keeping the first-order ac terms, the small-signal equations of (3) and (4) can be derived in (5) and (6).

$$\hat{d} = \frac{\hat{t}_{on} - D\hat{t}_s}{T_s} \tag{5}$$

$$\hat{t}_{off} = -\frac{T_{off}(\hat{v}_{out} - \hat{v}_{in})}{V_{out} - V_{in}} = -\frac{H \cdot L \cdot (\hat{v}_{out} - \hat{v}_{in})}{(V_{out} - V_{in})^2} \tag{6}$$

Similarly, (1) can be written as the summation of the DC term and its perturbation, and keeping the first-order ac terms as shown in (7).

$$\hat{t}_s = \hat{t}_{on} + \hat{t}_{off} \tag{7}$$

Using (6), (7) can be derived in (8).

$$\hat{t}_s = \hat{t}_{on} - \frac{H \cdot L \cdot (\hat{v}_{out} - \hat{v}_{in})}{(V_{out} - V_{in})^2} \tag{8}$$

Similarly, the peak inductor current, i_p, can be expressed as (9) by $\boldsymbol{t_{on}}$ and the average synthetic signal $\langle i_S \rangle$.

$$i_p = \langle i_S \rangle + \frac{v_{in}}{2L} t_{on} \tag{9}$$

(9) can be written as the summation of the DC term and its perturbation, and keeping the first-order ac terms as shown in (10).

$$\hat{i}_p = \hat{i}_S + \frac{(V_{in}\hat{t}_{on} + T_{on}\hat{v}_{in})}{2L} \tag{10}$$

(10) can be derived in (11).

$$\hat{t}_{on} = \frac{2L}{V_{in}}(\hat{i}_P - \hat{i}_s) - \frac{T_{on}}{V_{in}}\hat{v}_{in} \tag{11}$$

Using (5), (8) and (11), the small-signal duty cycle is derived as (12).

$$\hat{d} = \left(D'\left(\frac{2L}{V_{in}}\left(\hat{i}_p - \hat{i}_S\right) - \frac{T_{on}}{V_{in}}\hat{v}_{in} \right) + \frac{L \cdot H \cdot D}{\left(V_{out} - V_{in}\right)^2}\left(\hat{v}_{out} - \hat{v}_{in}\right) \right) \cdot \left(T_s\right)^{-1} \tag{12}$$

(12) can be simplified as (13) through the use of the DC equivalent equations by assuming $\hat{i}_S$ and $\hat{i}_p$ have same perturbation degree.

$$\hat{d} = F_m \cdot \hat{v}_C + F_g \cdot \hat{v}_{in} + F_v \cdot \hat{v}_{out} \tag{13}$$

$$F_m = \frac{2K \cdot D \cdot D'}{H}, F_g = -\frac{1}{V_{out}}, \text{ and } F_v = \frac{D'}{V_{out}} \tag{14}$$

As a result, the small-signal model of the boost converter with the synthetic current ripple control is illustrated in Fig. 5 and the control-to-output transfer function is shown in (15). R is the output impedance. K is the coefficient constant between v_C and i_C. R_{ESR} is the equivalent series resistance of output capacitor, C_o.

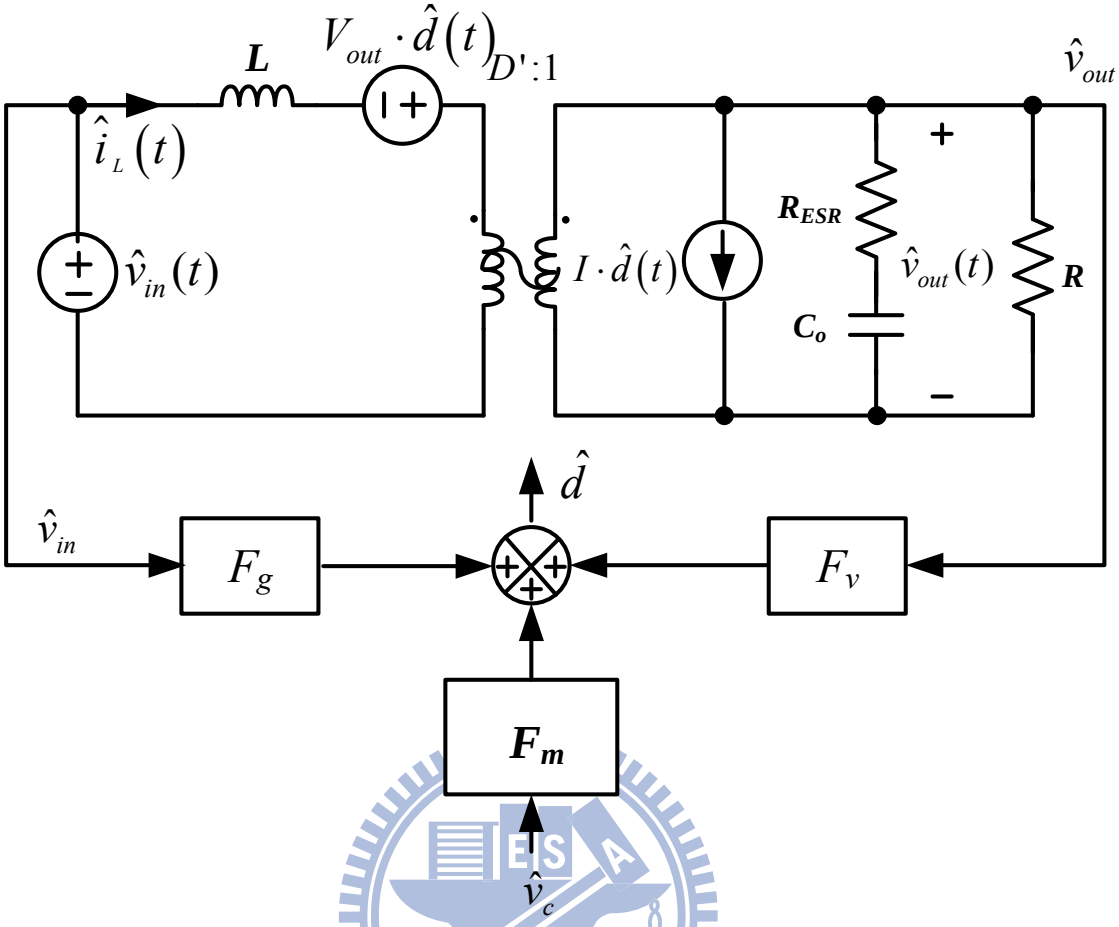


Fig. 10. The small-signal model of the boost converter under the synthetic current ripple control.

$$G_{vc}=\frac{\hat{v}_{out}}{\hat{v}_c}=\frac{F_m\cdot G_{vd}}{1-F_v\cdot G_{vd}} \tag{15}$$

Where

$$G_{vd}=\frac{\hat{v}_{out}}{\hat{d}}\bigg|_{\hat{v}_{in}=0}=\frac{V_{out}}{D'}\cdot\frac{(1-s\frac{L}{D'^2R})(1+sR_{ESR}C_o)}{1+s\frac{L}{RD'^2}+s^2\frac{LC_o}{D'^2}} \tag{16}$$

Furthermore, (14) can be derived as (16).

$$G_{vc}=\frac{\hat{v}_{out}}{\hat{v}_c}=\frac{F_m\cdot\frac{V_{out}}{D'}(1-s\frac{L}{(D')^2R})(1+sR_{ESR}C_o)}{1+s[\frac{L}{R(D')^2}+(\frac{L}{(D')^2R}-R_{ESR}C_o)]+s^2(\frac{LC_o}{(D')^2}+\frac{L}{(D')^2R}R_{ESR}C_o)} \tag{17}$$

$$=\frac{G_{vc0}(1-\frac{s}{\omega_{z(RHP)}})(1+\frac{s}{\omega_{z(ESR)}})}{1+\frac{2\zeta}{\omega_0}s+\frac{s^2}{\omega_0^2}}$$

It is obvious to find that the system contains two complex pole, and two zeros, which include one RHP zero, and one LHP zero. The parameters of small signal model are showed in **Table II**. The frequency response of the synthetic current ripple control is similar to that of the voltage-mode PWM technique **[9]**. In other words, the type III compensation must be used for the stability of the system.

Table II. THE PARAMETERS OF SMALL SIGNAL MODEL OF SYNTHETIC CURRENT RIPPLE CONTROL

F_m	F_g	F_v	G_{vc0}	$\omega_{z(RHP)}$	$\omega_{z(ESR)}$	ω_{p1}*(double pole)*
$\frac{2K \cdot D \cdot D'}{H}$	$-\frac{1}{V_{out}}$	$\frac{D'}{V_{out}}$	$F_m \cdot \frac{V_{out}}{D'}$	$\frac{(D')^2 R}{L}$	$\frac{1}{R_{ESR} C_o}$	$\frac{-\frac{2\zeta}{\omega_0} + \sqrt{(\frac{2\zeta}{\omega_0})^2 - \frac{4}{\omega_0^2}}}{2(\frac{1}{\omega_0^2})} \approx \omega_0$

2.2 Small Signal Modeling of the proposed CSC technique

As depicted in **Fig. 11**, the CSC technique generate synthetic signal, i_r and limits it within a hysteresis window, which defines the upper and lower current bands. The synthetic signal rises to reach the upper band of hysteresis window quickly. On the other hand, the synthetic signal falls to reach the lower band of hysteresis window with the slope as same as the inductor discharge slope.

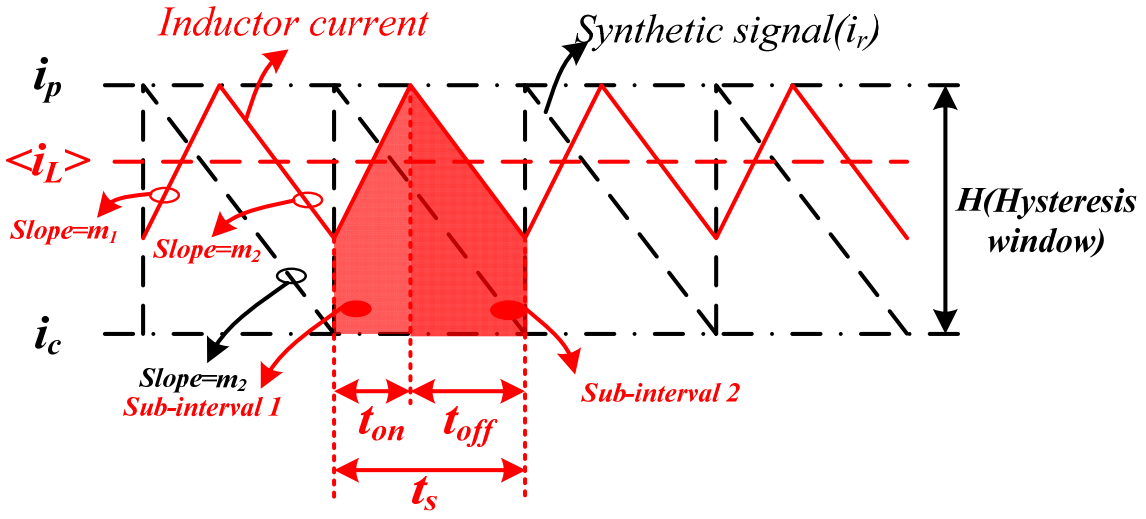


Fig. 11**.** The synthetic waveform is limited with the hysteresis window defined by the CSC technique.

As same as the analysis in section 2.1, the value of t_{off} can be written as (18).

$$t_{off} = \frac{L \cdot H}{(v_{out} - v_{in})} - t_{on} \tag{18}$$

$$(T_{off} + \hat{t}_{off}) = \frac{L \cdot H}{(V_{out} + \hat{v}_{out} - V_{in} - \hat{v}_{in})} - T_{on} - \hat{t}_{on} \tag{19}$$

(18) can be written as the summation of the DC term and its perturbation as shown in (19).

Keeping the first-order ac terms, the small-signal equations can be derived in (20).

$$\hat{t}_{off} = -\frac{T_{off}(\hat{v}_{out} - \hat{v}_{in})}{V_{out} - V_{in}} - \hat{t}_{on} = -\frac{H \cdot L \cdot (\hat{v}_{out} - \hat{v}_{in})}{(V_{out} - V_{in})^2} - \hat{t}_{on} \tag{20}$$

Similarly, $\hat{t}_s$ and $\hat{t}_{on}$ are expressed in (21) and (22).

$$\hat{t}_s = -\frac{H \cdot L \cdot (\hat{v}_{out} - \hat{v}_{in})}{(V_{out} - V_{in})^2} \tag{21}$$

$$\hat{t}_{on} = \frac{2L}{V_{in}}(\hat{i}_P - \hat{i}_L) - \frac{T_{on}}{V_{in}}\hat{v}_{in} \tag{22}$$

Using (5), (21) and (22), the small-signal duty cycle is derived as (23).

$$\hat{d} = \frac{V_{out} - V_{in}}{H \cdot L}\left(\frac{2L}{V_{in}}(\hat{i}_P - \hat{i}_L) - \frac{T_{on}}{V_{in}}\hat{v}_{in} + D\frac{H \cdot L \cdot (\hat{v}_{out} - \hat{v}_{in})}{(V_{out} - V_{in})^2}\right) \cdot (T_s)^{-1} \tag{23}$$

(23) can be simplified as (24) through the use of the DC equivalent equations.

$$\hat{d} = F_m \cdot (\hat{v}_C - R_i \cdot \hat{i}_L) + F_v \hat{v}_{out} - F_g \hat{v}_{in} \tag{24}$$

$$F_m = \frac{2 \cdot D}{H \cdot D^{'} \cdot R_i}, F_g = \frac{1}{D^{'} V_{out}}, \text{ and } F_v = \frac{1}{V_{out}} \tag{25}$$

As a result, the small-signal model of the boost converter with the CSC technique is illustrated in **Fig. 12** and the control-to-output transfer function is shown in (26). R is the output impedance. R_i is the current sensing gain. R_{ESR} is the equivalent series resistance of output capacitor, C_o.

$$G_{vc} = \frac{\hat{v}_{out}}{\hat{v}_c} = \frac{F_m \cdot G_{vd}}{1 - F_v \cdot G_{vd} + F_m \cdot G_{id} \cdot R_i} \tag{26}$$

Because of $F_m \cdot G_{id} \cdot R_i >> 1 - F_v \cdot G_{vd}$, we can get

$$G_{vc} = \frac{\hat{v}_{out}}{\hat{v}_C} = \frac{F_m \cdot G_{vd}}{F_m \cdot G_{id} \cdot R_i} = \frac{1}{R_i} \frac{G_{vd}}{G_{id}} = \frac{D^{'} R}{2R_i} \frac{(1 - s\frac{L}{(D^{'})^2 R})(1 + sR_{ESR}C_o)}{(1 + s\frac{RC_o}{2})}$$
$$= \frac{G_{vc0}(1 - \frac{s}{\omega_{z(RHP)}})(1 + \frac{s}{\omega_{z(ESR)}})}{1 + \frac{s}{\omega_{p1}}} \tag{27}$$

It is obvious to find that the system contains one dominate pole only, and two zeros, which include one RHP zero, and one LHP zero. The parameters of small signal model are showed in **Table III**. The frequency response of the CSC technique is similar to that of the current-mode PWM technique **[10]**. In other words, the PI compensation is suitable and easily implemented on the chip **[11]**. Besides, the advantage of the proposed CSC technique is the remove of the slope compensation in the conventional current-mode PWM control. That is, the proposed CSC technique simplifies the compensation and improves the power conversion efficiency at light loads due to the load-dependent switching frequency. It is more suitable for portable devices.

Table III. THE PARAMETERS OF SMALL SIGNAL MODEL OF PROPOSED CSC TECHNIQUE

F_m	F_g	F_v	G_{vc0}	$\omega_{z(RHP)}$	$\omega_{z(ESR)}$	ω_{p1}(single pole)

$\frac{2 \cdot D}{H \cdot D^{'} \cdot R_i}$	$\frac{1}{D^{'} V_{out}}$	$\frac{1}{V_{out}}$	$\frac{D^{'} R}{2R_i}$	$\frac{(D^{'})^2 R}{L}$	$\frac{1}{R_{ESR} C_o}$	$\frac{2}{RC_o}$

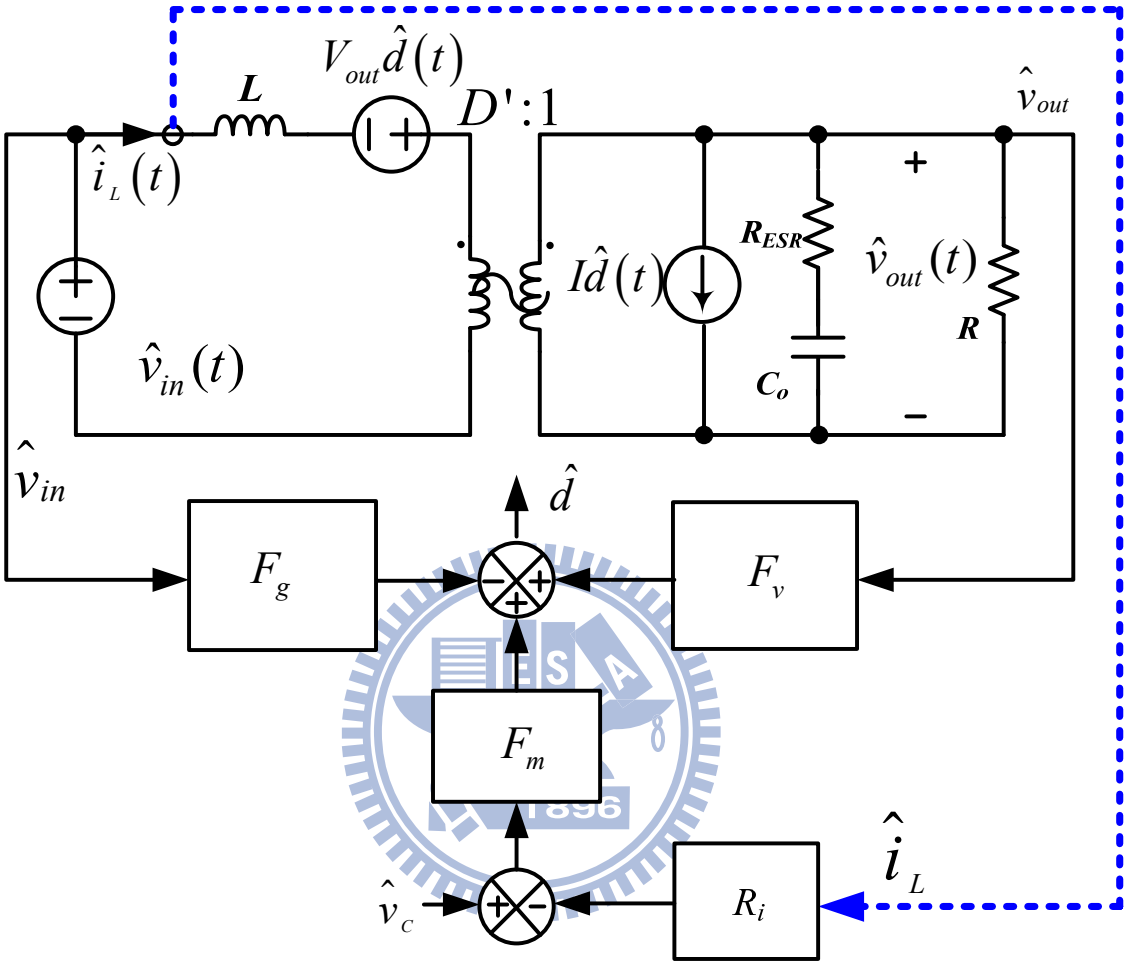


Fig. 12**.** The small-signal model of the boost converter under the CSC technique.

2.3 The loop gain analysis with PI compensator for stability of the system

A closed-loop diagram of the boost converter with the CSC technique is shown in **Fig. 13**.

The loop gain is *T(s)* as shown in (28). β is the sensor gain, which is equal to $R_{F2}/(R_{F1}+R_{F2})$. $G_c(s)$ is the compensation transfer function. Generally, $G_c(s)$ is composed of an

error amplifier and a proportional-integral (PI) compensator. The PI compensator contributes one low-frequency pole-zero pair, (ω_{pc}, ω_z).

$$T(s) = \beta \cdot G_{vc}(s) \cdot G_c(s) \tag{28}$$

By way of the PI compensator, the original dominate pole of the system will be replace by $\omega_{pc,}$ and original dominate pole will be cancelled by $\omega_{z.}$ As a result, the Gain-Bandwidth of the system will be expanded. Simultaneously, the DC gain of the system will be enlarged to enhance the load regulation of the system because of the high gain of the error amplifier. The bode plot of the system with compensator, original system, and compensated system are showed in **Fig. 14**. Where

$$f_{p1} = \frac{1}{\pi \cdot R \cdot C_o} \tag{29}$$

$$f_{z(RHP)} = \frac{(D')^2 R}{2\pi \cdot L} \tag{30}$$

$$f_{z(ESR)} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_o} \tag{31}$$

The structure of PI compensator is shown in **Fig. 13**. It is composed of a transduction, g_m, the output impedance of the transduction, R_o, a resistance, R_z, and a capacitance, C_c.

The relationship between g_m, R_o, R_z, C_c, $\omega_{pc,}$ and ω_z are showed below.

$$f_{pc} = \frac{1}{2\pi \cdot R_o \cdot C_c} \tag{32}$$

$$f_z = \frac{1}{2\pi \cdot R_z \cdot C_c} \tag{33}$$

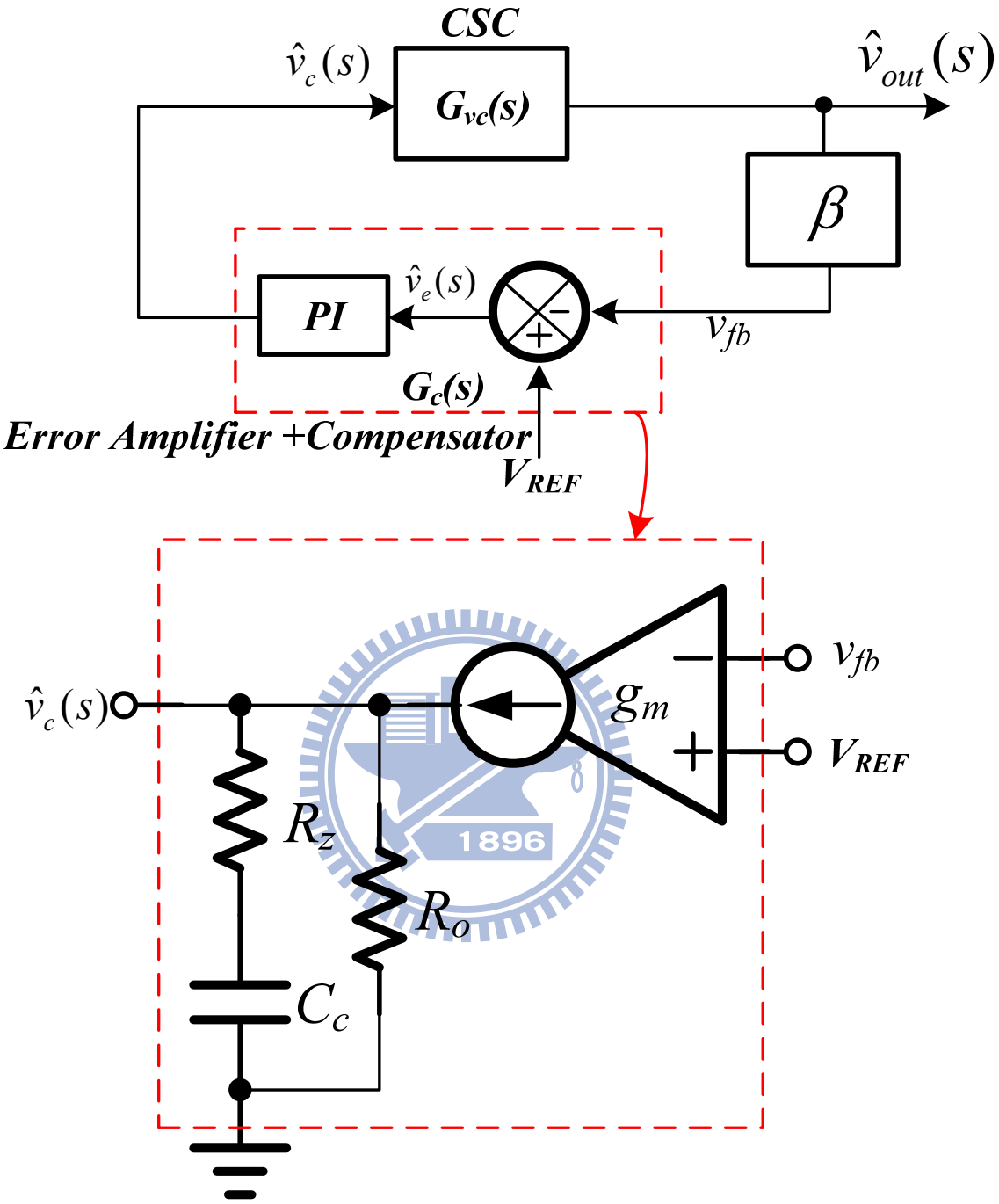

CSC
$\hat{v}_c(s)$
$G_{vc}(s)$
$\hat{v}_{out}(s)$
β
$\hat{v}_e(s)$
PI
v_{fb}
$G_c(s)$
Error Amplifier +Compensator
V_{REF}
$\hat{v}_c(s)$
g_m
v_{fb}
V_{REF}
R_z
R_o
C_c

Fig. 13. The simplified feedback system of the CSC technique.

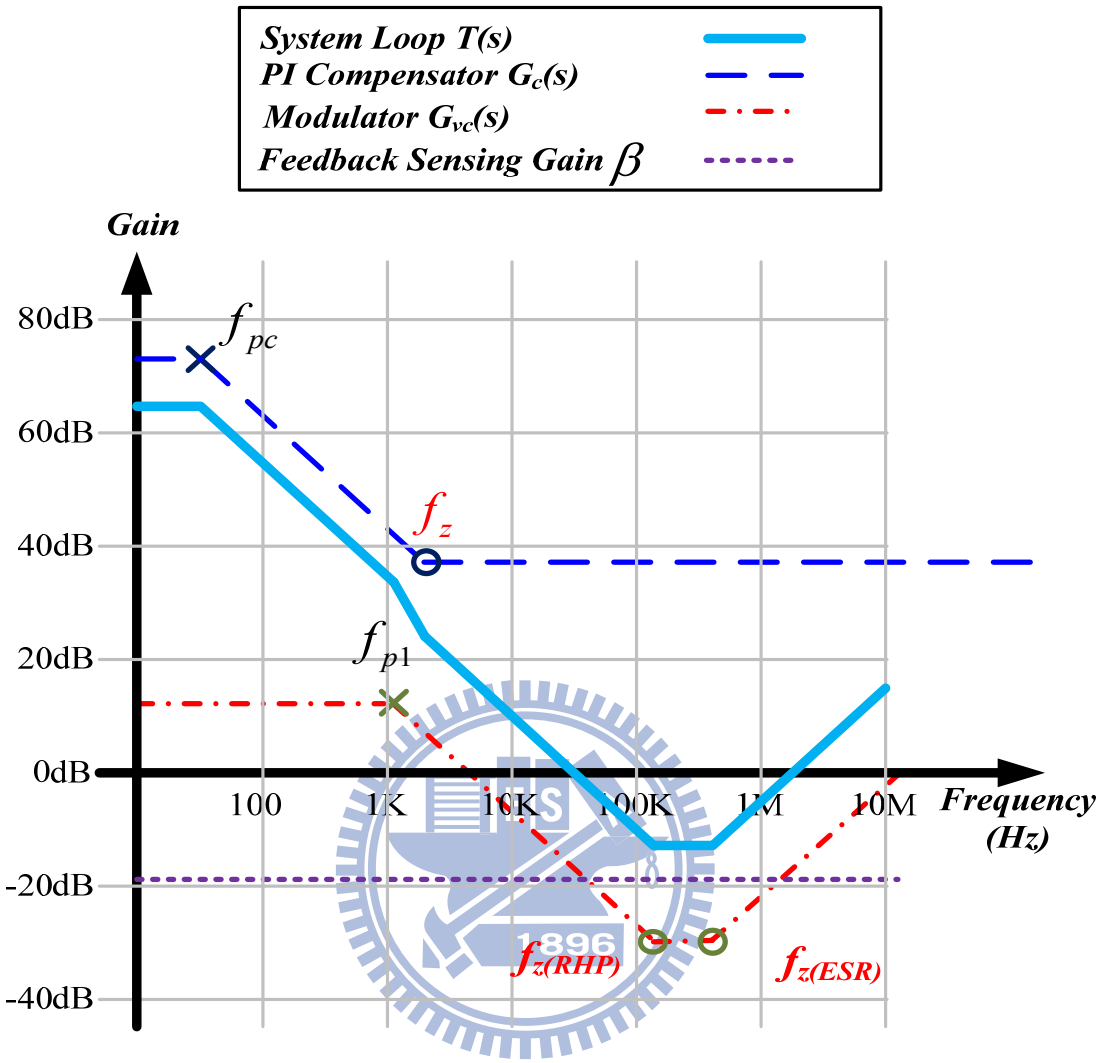


Fig. 14. The compensated loop gain *T(s)*.

Chapter 3

The Proposed CSC Technique

Fig. 15 shows the architecture of proposed current-mode hysteresis DC-DC boost converter with the CSC technique. The synthetic signal V_{clk} is used to decide the time to store energy in the inductor. The adjustment of the synthetic clock signal can improve the power conversion efficiency according to the load current condition. On the other hand, the energy stored in the inductor begins to release to the output load when the current sensing signal V_{sense} is larger than the hysteresis upper bound, V_H. The V_{sense} signal provides a current path as dash line showed in **Fig. 12** to convert traditional synthetic current ripple control with voltage mode to current mode. As a result, the input current information can be used to control the converter to behave as a constant current source. The dynamics of the inductor is pushed to high frequencies. The system order becomes one to reduce the complexity of compensator. Therefore, the proposed CSC technique can use the proportional-integral (PI) compensation method. In additional, due to the separate of V_{ramp} and V_{sense}, the low noise immunity problem in **Fig. 7** can be solved.

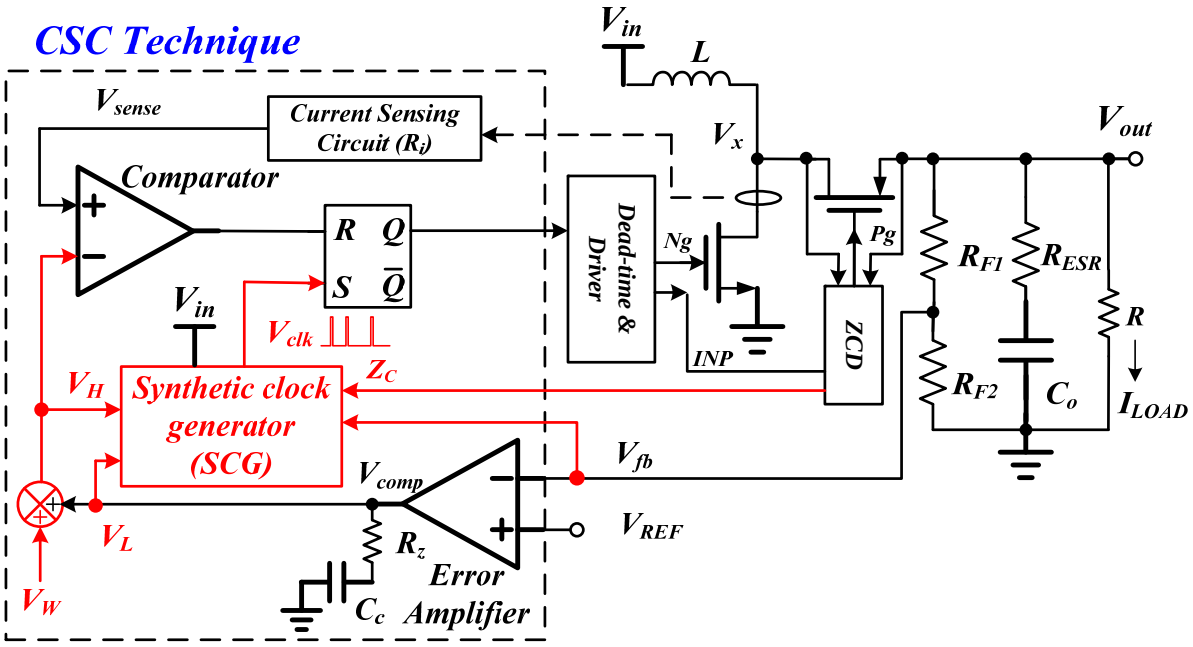


Fig. 15. The proposed architecture.

3.1 The proposed current-mode synthetic waveform

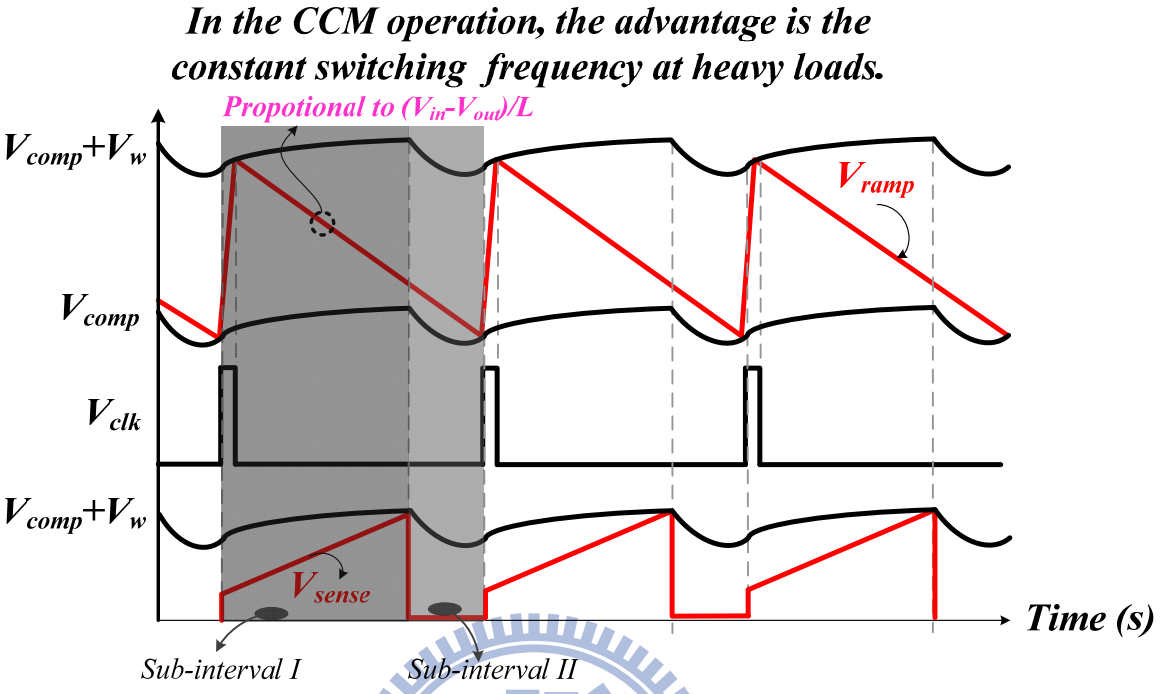
During the sub-interval II of the inductor current as depicted in **Fig. 16(a)**, the inductor current slope is shown in **(34)**, which can be synthesized by the two signals, V_{in} and V_{out}, to decide the synthetic signal, V_{clk}, in the CCM operation.

$$V_{in} - V_{out} / L \tag{34}$$

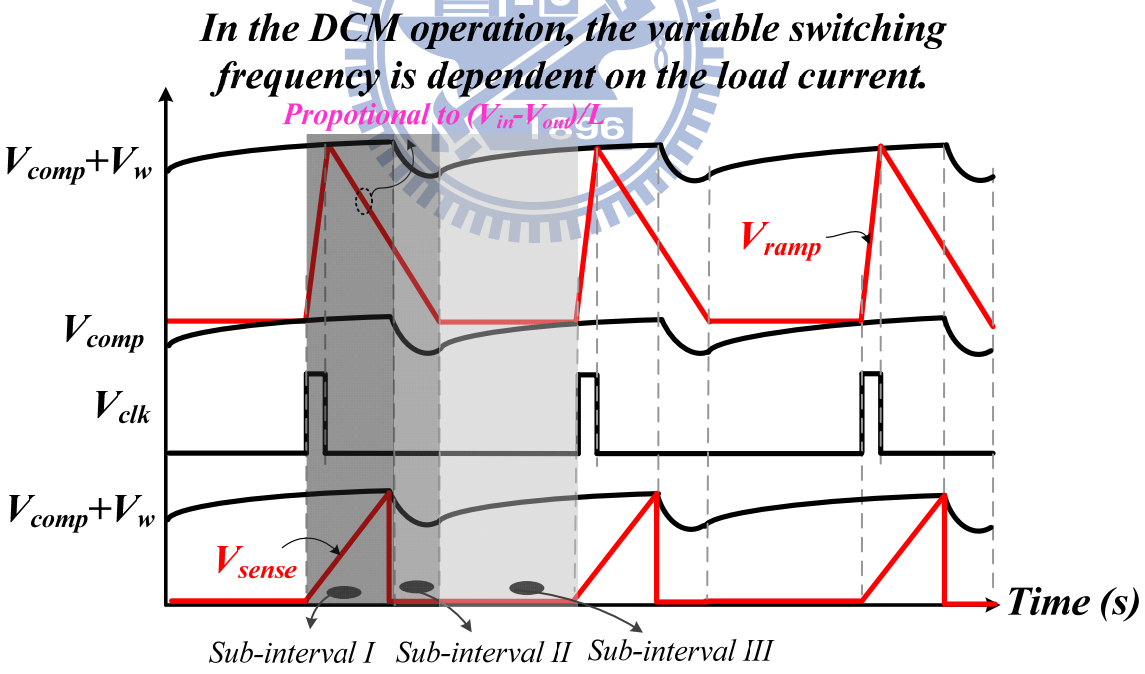
The current-mode hysteresis window is composed of the upper bound V_H and the lower bound V_L. The value of V_L is equal to the output, V_{comp}, of the error amplifier in order to improve the load regulation performance since worse load regulation in conventional current-mode hysteresis control comes from its lack of voltage regulation loop. Thus, the definition of 'V_L= V_{comp}' can improve the load regulation.

The hysteresis window of the proposed current-mode control is designed as V_w, which is a constant value. The relationship between V_H and V_L can be expressed as **(35)**.

$$V_H = V_L + V_w = V_{comp} + V_w \quad \textbf{(35)}$$



(a)



(b)

Fig. 16**.** The CSC technique force the system operates in (a) the CCM operation at heavy loads and (b) the DCM operation at light loads for power saving.

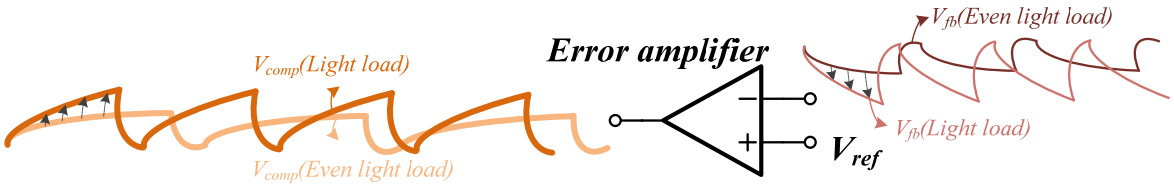


Fig. 17**.** Output energy detect mechanism for switching frequency modulation.

3.2 Modulation method at different loads

At heavy loads, the system operates in the continuous conduction mode (CCM). Thus, the system switching frequency is dependent on the hysteresis window V_w. As illustrated in **Fig. 16(a)**, the advantage is the switching frequency is a constant value in the CCM operation for high driving capability.

On the other hand, the system operates in the discontinuous conduction mode (DCM) at light loads. As depicted in **Fig. 16(b)**, in the DCM operation, the synthetic current-mode waveform V_{ramp}, is kept constant once the inductor current becomes zero, which is detected by the zero current detector (ZCD) in **Fig. 15**. Owing to the constant V_{ramp} if the signal Z_C is equal to one, the off-time period is extended. Simultaneously, the output capacitor can't gain energy and the output of error amplifier V_{comp} increases to be higher than V_{ramp}, again. The output energy detect mechanism is shown in **Fig. 17**. The speed of V_{comp} increasing higher than V_{ramp} is dependent on the load condition. When load current becomes light, the speed of V_{comp} increases quicker than even light load current. Then V_{comp} takes shorter to hit V_{ramp} to initial the next period. As a result, the switching frequency increases with the frequency of V_{ramp} increasing. The switching frequency is reduced in the DCM operation to save much switching power loss at light loads. In other words, the switching frequency, which depends on the value of load current, causes the switching power loss is inversely proportional to the switching frequency. That is, the variable switching frequency in the DCM operation can

reduce the switching loss and thus improve the power conversion efficiency at light loads.

3.3 Modulation method at transient response

Furthermore, the new CSC technique has fast transient response since the trailing and leading edges can rapidly react to the output load variation. As shown in **Fig.18** , the on time of the pulse width signal adaptively increases or decreases when the load current suddenly increases or decreases, respectively. Similarly, the off time can be modulated to improve the transient response time due to the CSC window controlled by the error amplifier.

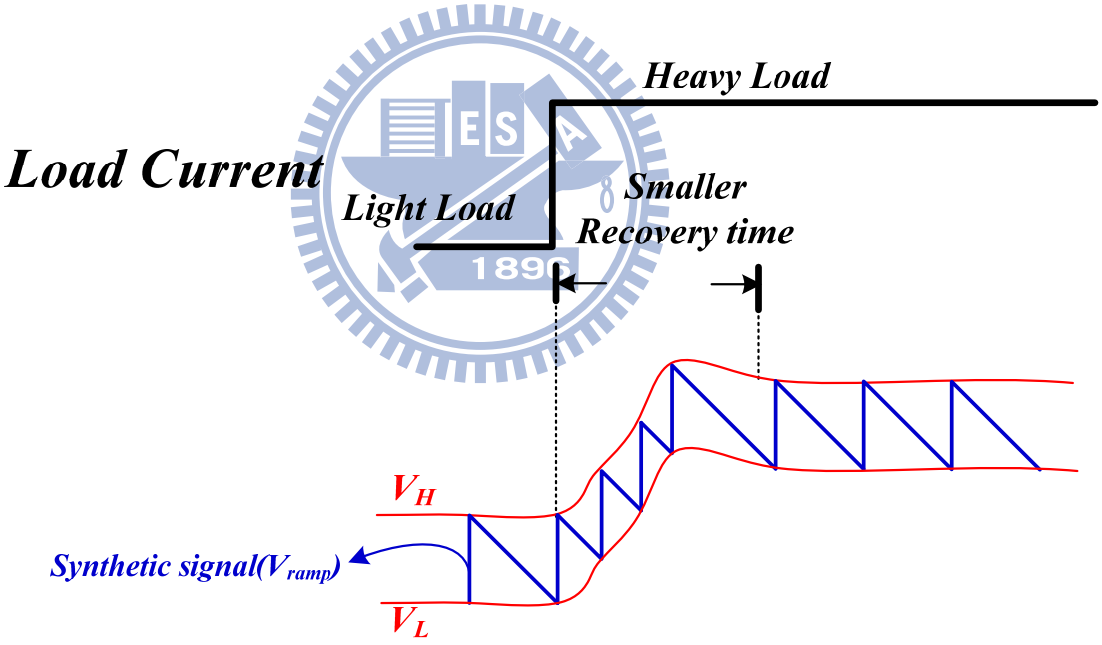


Fig. 18. The transient response waveform of CSC technique.

Chapter 4

The Circuit Implementation

The CSC technique in **Fig. 15** contains two parts. The first part is the insertion of current information, which is implemented by the comparison of the low-side NMOSFET current sensing signal V_{sense} with the upper bound signal V_H. The second part as depicted in **Fig. 21** is the synthetic clock generator (SCG). The SCG circuit can ensure the switching frequency nearly constant if the converter operates in the CCM operation. On the other hand, the SCG circuit can adjust the switching frequency to reduce the switching power loss at light loads if the converter operates in the DCM operation. In brief, constant switching frequency ensure low electromagnetic interference (EMI) and high driving capability at heavy loads while the decreasing switching frequency can improve the power conversion efficiency at light loads.

4.1 Current Sensor

The CSC technique needs to sense the charging interval of inductor current. Thus, an accurate current sensor is required. As depicted in **Fig. 19**, the transistors M_1 and M_2 are biased by the same current I_B. Thus, $V_{GS1}=V_{GS2}$. When the inductor current charges, the *PowerNMOS* turn on with the signal, N_g, pull high. At the same time, M_{S3}, M_{S4} turn on to make *PowerNMOS* and M_{S3} form a current mirror pair with $\left(\frac{W}{L}\right)_{PowerMOS}:\left(\frac{W}{L}\right)_{M_{S3}}=N:1$.

And M_2, M_3 form a negative feedback to make sure source nodes of M_1, M_2 tight to V_x for accuracy of current mirror. Finally, $\frac{(I_L+I_B)}{N}=I_B+I_{sense}$. When I_B is small, $\frac{I_L}{N}=I_{sense}$. On

the other hand, *PowerNMOS* turn off with the signal, N_g, pull low, M_{S1}, M_{S2} turn on to provide I_B paths to flow for reducing react time. The current sensing gain, R_i, can be derived in (36).

$$R_i = \frac{R_{sense}}{N} \tag{36}$$

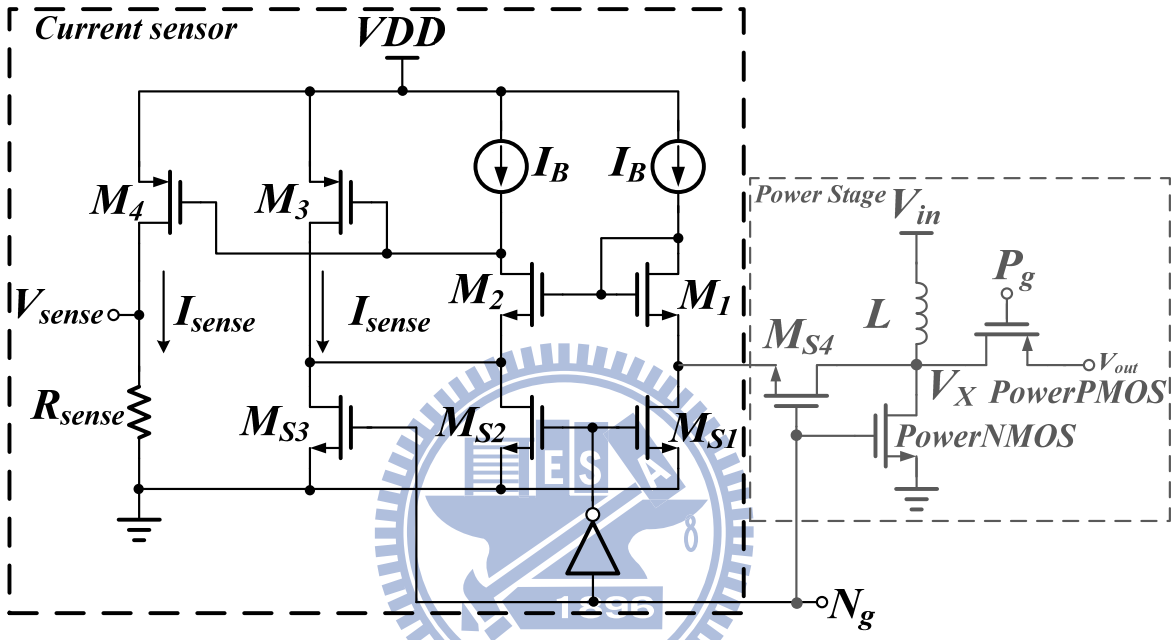


Fig. 19**.** The schematic of current sensor.

4.2 Fixed Hysteretic Current Window Circuit

In **Fig. 20**, the fixed hysteretic current window circuit is designed to accurately control the output ripple for ensuring the regulation performance. The low band of the fixed hysteretic current window is controlled by the output of the error amplifier, which is V_{comp}. Thus, a unity-gain buffer used to filter out the switching noise can generate the low band V_L. The hysteretic window is easily generated by adding an IR-drop to the low band V_L. The value of

IR-drop is derived by a constant current flowing through a hysteresis resistor R_w. As a result, the upper band V_H can be expressed by (37).

$$V_H = V_L + I_w \times R_w \tag{37}$$

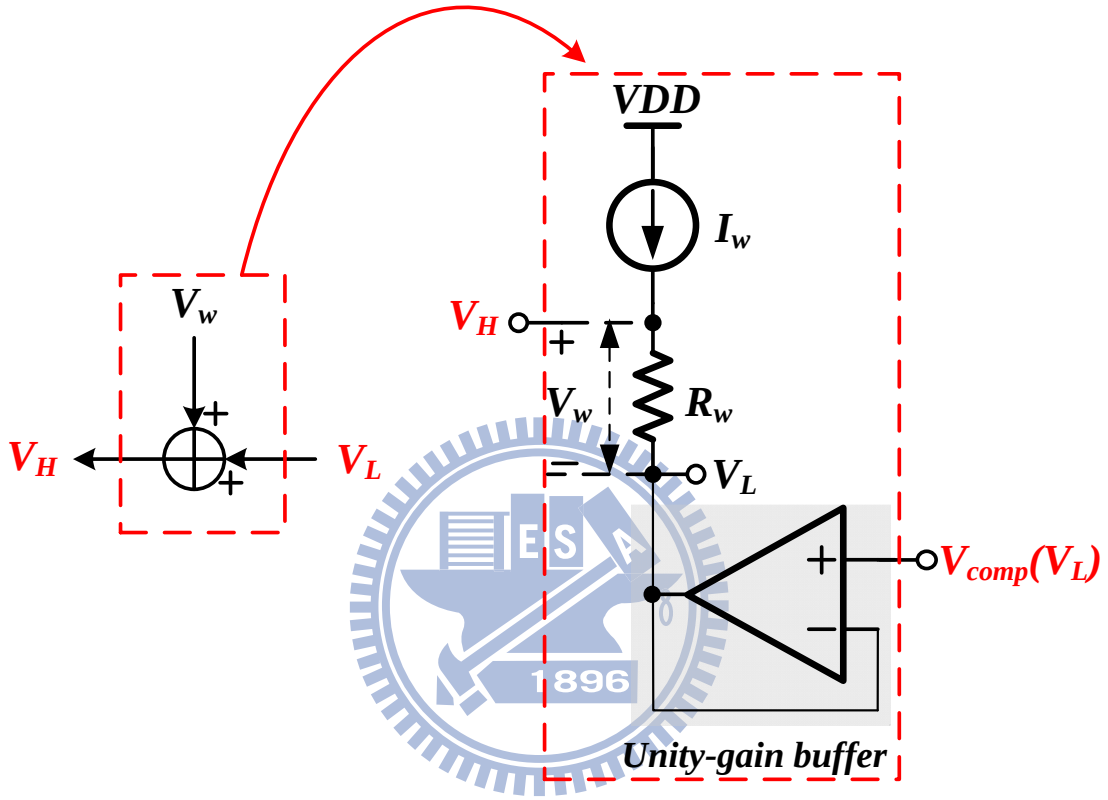


Fig. 20. The fixed hysteretic current window circuit.

4.3 The synthetic clock generator (SCG)

As the SCG circuit depicted in **Fig. 21**, in the beginning of the switching period, a current I_c introduced by the transistor M_4 flows into the capacitor C_{ramp} to ramp up the signal V_{ramp}. V_{ramp} is rapidly charged to be higher than V_H **since I_c is much higher than I_d.** Thus, the output of the SR-latch is triggered from high to low to turn on switch M_6. The discharging period of the inductor current is emulated by the discharging current I_d to generate the synthetic clock. The in-out subtractor generates a current signal I_d, which is proportional to the voltage

difference of the input and output voltages **[12]**. The discharging current, I_d can be expressed as **(38)**. The input stage of in-out subtractor is voltage follower, as shown in **Fig. 22**. In **Fig. 22(a)**, the output impedance of original voltage follower is shown as (40). To reduce the output impedance and improves the in-out subtractor linearity, the folded voltage follower is implemented, as illustrated in **Fig. 22(b)**. This structure can reduce output impedance effectively and the output impedance is shown in (41). But the main disadvantage is input swing depends on the threshold voltage, it becomes very small in modern CMOS technology. The input swing can be written as (43). For a wider input swing range, the folded flipped voltage follower is implemented, as illustrated in **Fig. 22(c)**. This structure not only reduces output impedance but also improves the input swing range. The output impedance of the folded flipped voltage follower and the input swing range is shown in (42) and (44) respectively. By using the folded flipped voltage follower as in-out subtractor input stage, the output impedance on the node N_1 and node N_2 in **Fig. 21** is greatly reduced, and the linearity of in-out subtractor approaches to ideal value.

$$I_d = 2I_{ERROR} = 2\frac{V_{fb} - V_{inFF}}{R_{gm}} = 2\beta\frac{V_{out} - V_{in}}{R_{gm}} \quad \textbf{(38)}$$

$$\text{where } \beta = \frac{R_{F2}}{R_{F1} + R_{F2}} \text{ and } V_{inFF} = \beta V_{in} \quad \textbf{(39)}$$

And then, the signal V_{ramp} begins to ramp off and compare with the lower bound V_L to decide the next switching period. The slope of the discharging period is proportional the negative inductor current slope. Once the value of V_{ramp} is lower than that of V_L, the switch M_6 is turned off to ramp up the V_{ramp}, again. The signal V_{ramp} is limited with the hysteresis window, which is defined by V_H and V_L. In conclusion, the SCG circuit decides the switching frequency. In the CCM operation, the inductor current will not be smaller than zero. Thus, the switching frequency is basically decided by the hysteresis window. If the value of the input and out voltages is not changed, the switching frequency can be kept constant in the CCM

operation.

On the other hand, in the DCM operation, the signal Z_C is set to high when the zero-current detector (ZCD) senses the inductor current is equal to zero. The transistor M_1 will directs the discharging current I_d to ground and the signal V_{ramp} is clamped at a constant value. The switch M_7 and C_{sample} are used to balance the DC level of V_{ramp} at different periods in the DCM operation to ensure the switching period regularity. When ZCD is high, the voltage V_{ramp} is clamped. At the same time, M_7 turns on to connect C_{sample} and C_{ramp}. With the mechanism, the voltage error of V_{ramp} between two periods will be cancelled with $C_{sample} >> C_{ramp}$. And the "dummy" switch M_8, M_9, driven by $\overline{ZCD}$ are added to the circuit such that after M_7 turns off and M_8, M_9 turns on, the channel charge deposited by M_7 on C_{ramp} and C_{sample} is absorbed by M_8, M_9 to create a channel. In other word, the charge injection effect is cancelled **[11]**.

As a result, the switching frequency is decreased to reduce the switching power loss as shown in **Fig. 16(b)**. The switching frequency of the boost converter is dependent on the load current.

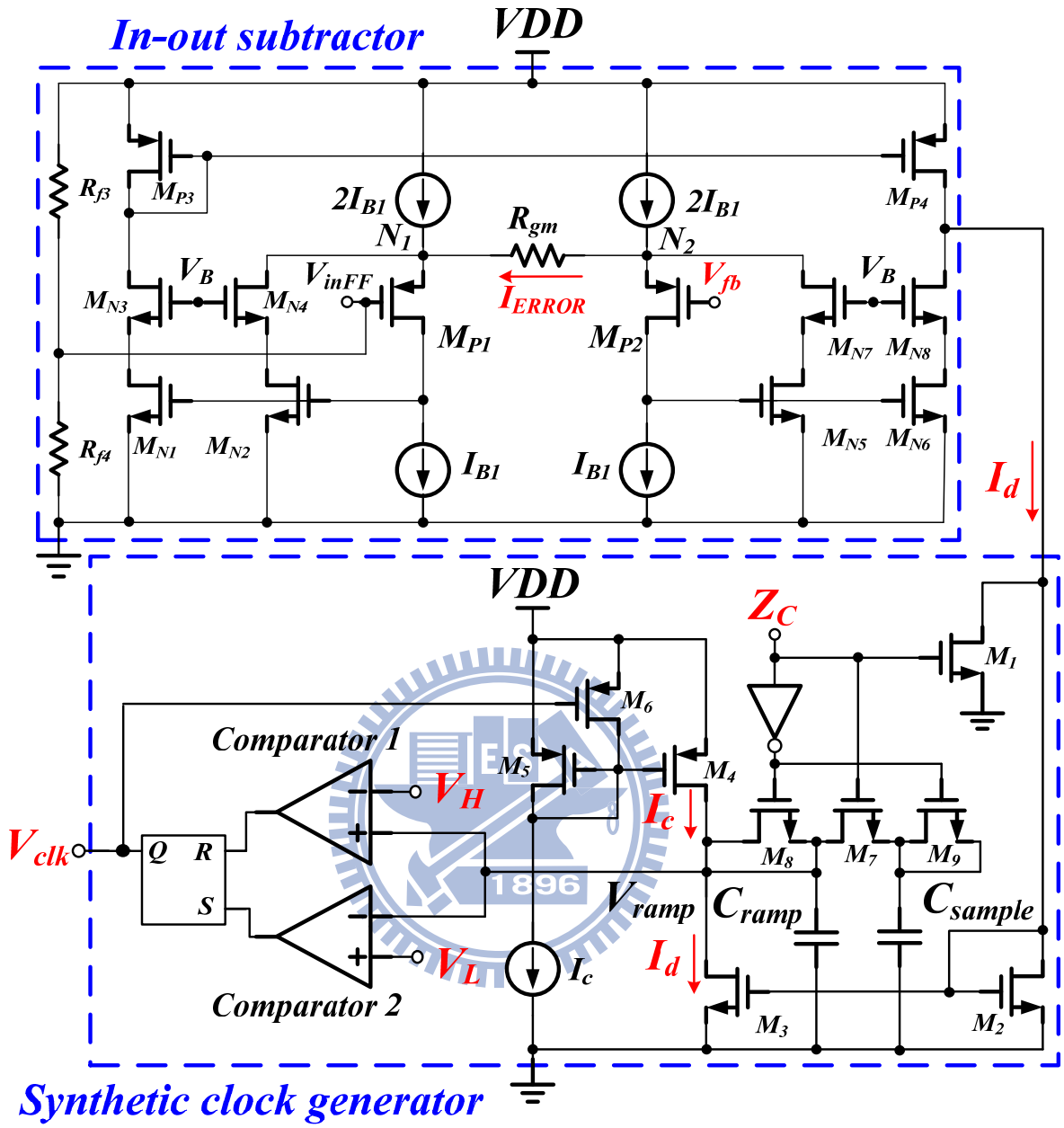

In-out subtractor
VDD
R_{f3}
M_{P3}
$2I_{B1}$
N_1
R_{gm}
$2I_{B1}$
N_2
M_{P4}
V_B
M_{N3}
M_{N4}
V_{inFF}
I_{ERROR}
V_{fb}
V_B
M_{P1}
M_{P2}
M_{N7}
M_{N8}
R_{f4}
M_{N1}
M_{N2}
I_{B1}
I_{B1}
M_{N5}
M_{N6}
I_d
VDD
Z_C
M_1
M_6
Comparator 1
M_5
M_4
V_H
I_c
V_{clk}
Q
R
S
M_8
M_7
M_9
V_{ramp}
C_{ramp}
C_{sample}
V_L
I_c
I_d
Comparator 2
M_3
M_2
Synthetic clock generator

Fig. 21**.** The proposed SCG circuit in the CSC technique.

$$(b)V_{in}^{swing} = (VDD - V_{DSM1}^{sat} - V_{SGM2}) - (VDD - V_{SGM1} - V_T) = V_T - V_{DSM2}^{sat} \quad (43)$$

$$(c)V_{in}^{swing} = (VDD - V_{DS2I_B}^{sat} - V_{SGM2}) - (V_{GSM1} - V_T) = VDD - V_{DS2I_B}^{sat} - V_{SGM2} - V_{DSM1}^{sat} \quad (44)$$

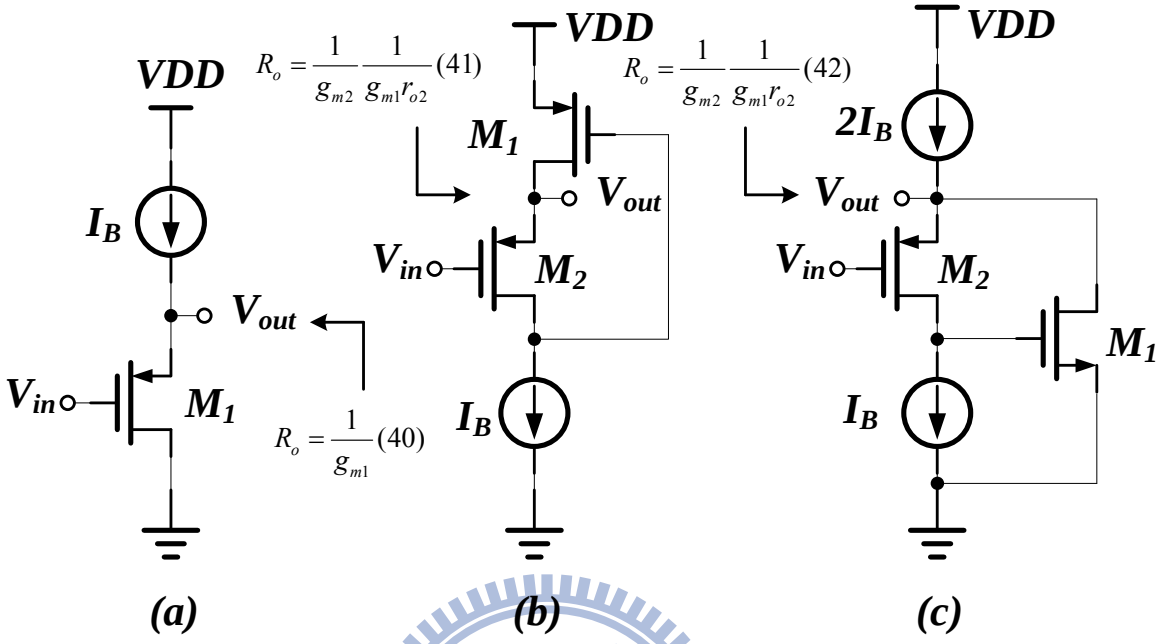
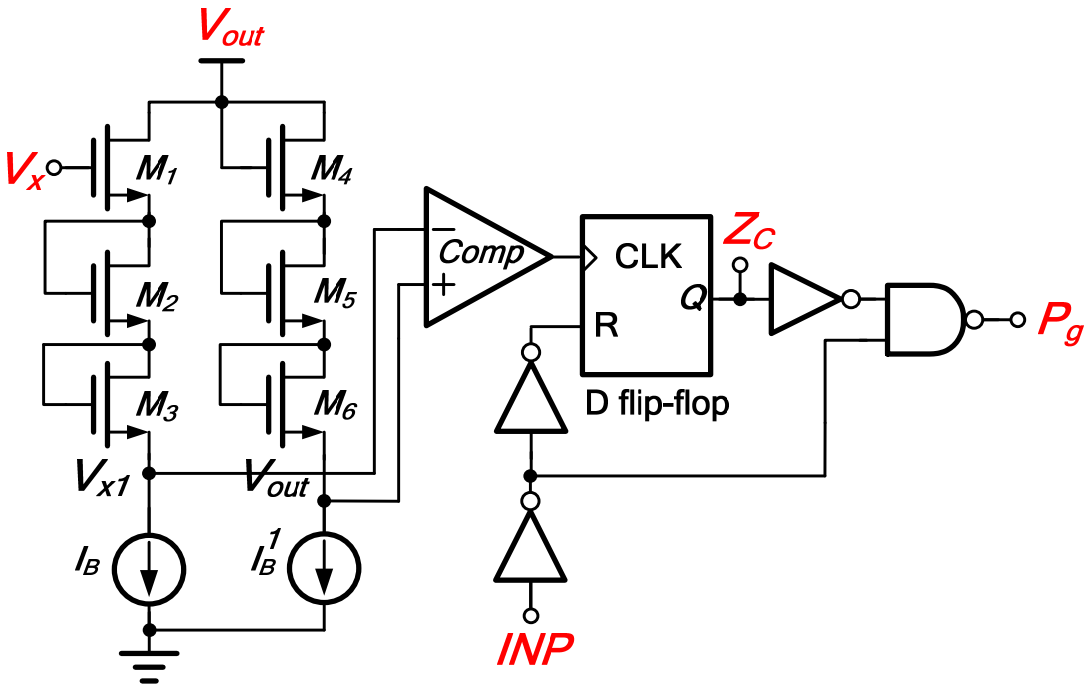


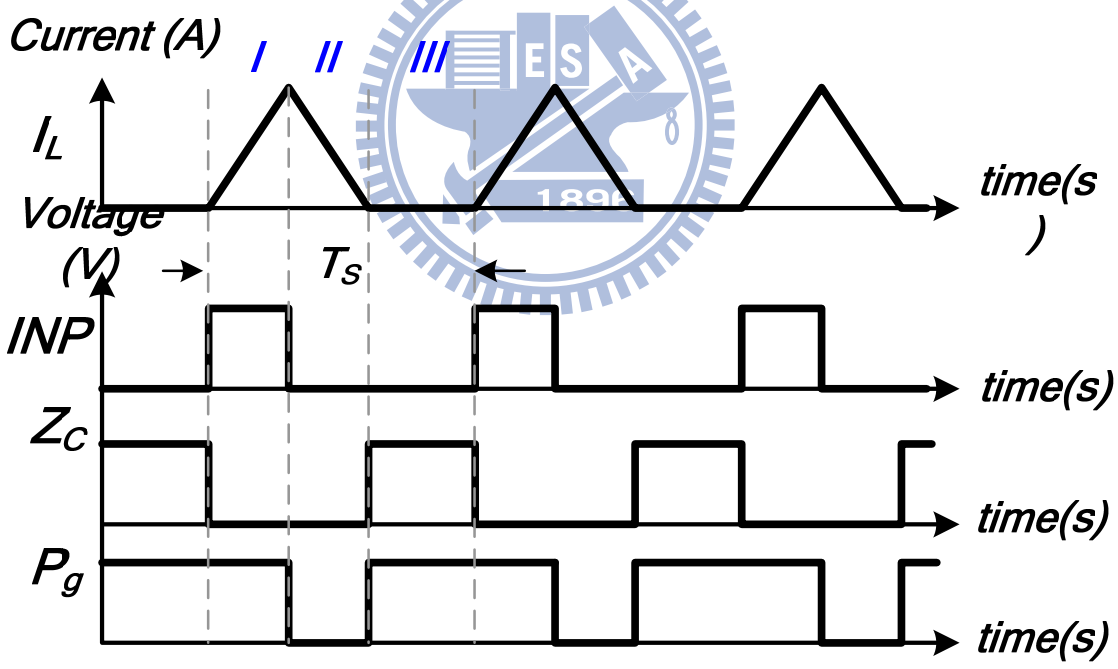
Fig. 22**.** Schematic of different In-Out subtractor input stages. (a) Voltage follower. (b) Folded voltage follower. (c) Folded flipped voltage follower.

4.4 The zero current detector (ZCD)

The proposed ZCD is illustrated in **Fig. 23(a)** to control the switching frequency in the SCG circuit. The transistors M_1-M_3 and M_4-M_6 construct the level shifters to shift the signals V_X and V_{out} to the V_{X1} and V_{out1}, respectively, to meet the input common-mode range of the comparator. In the first interval of each switching period, the *INP* is logic high to keep the P_g high and reset the D-flip-flop to pull the Z_C low. In the second interval of each switching period, the *INP* is triggered to logic low to turn on the power PMOSFET if the signal Z_C is still low. Once the reverse inductor current occurs, V_X is smaller than V_{out} corresponding to V_{X1} is smaller than V_{out1}. Simultaneously, the output of the comparator is triggered from low to high to set the signal Z_C high to indicate the zero current condition. The signal P_g is changed from low to high to turn off the power PMOSFET and avoid the occurrence of the reverse inductor current.



(a)



(b)

Fig. 23. (a) The proposed ZCD circuit. (b) The timing diagram.

Chapter 5

Whole chip experimental Results

The proposed boost convert with the CSC technique was fabricated by TSMC 0.25 μm CMOS process. The threshold voltages of nMOSFET and pMOSFET are 0.477 V and -0.596 V, respectively. The off-chip inductor and output capacitor are 1 μH and 6.8 μF, respectively. The output voltage V_o is 4.5V. The specification is listed in Table IV. The chip micrograph is shown in Fig. 24 and the chip area is about 1564 μm × 1813 μm including the test pads.

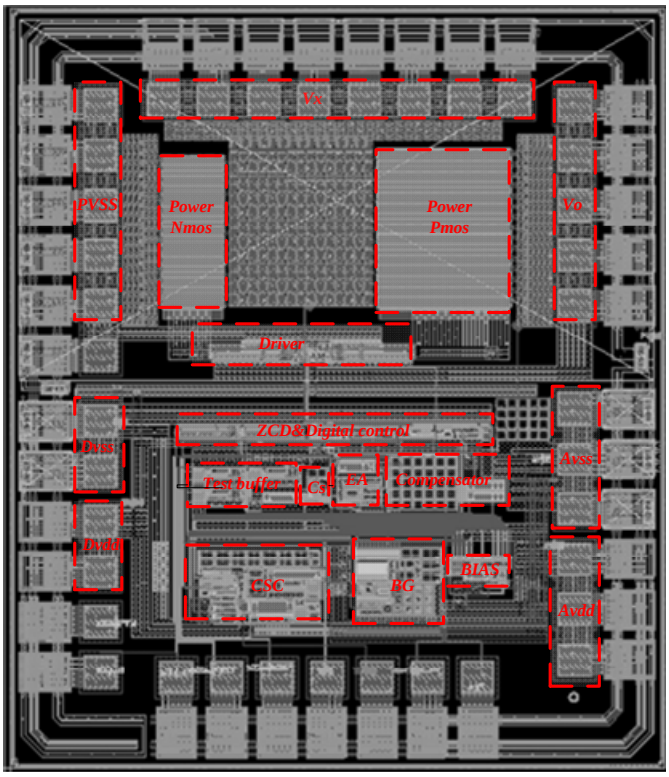


Fig. 24**.** Chip micrograph.

Fig. 25 shows the output waveforms at different load current condition when the converter operates at the CCM mode and DCM mode. Fig. 25(a) and (b) show that the proposed CSC technique adjusts the switching frequency of the boost converter dynamically according to the load current condition. Fig. 25(c) shows the switching frequency maintain 1.7MHz to enhance

system performance when inductor current enter into CCM mode. The relationship between load current, switching frequency and output ripple is listed in Table V. It demonstrates that the switching frequency with different load is almost the same at CCM mode. On the other hand, the switching frequency reduces with the load current decrease at DCM mode.

Fig. 26 demonstrates the waveform at the transition point. It is seamless between PFM and PWM mode, and the overshoot which ordinary pfm mode will occur is also reduced

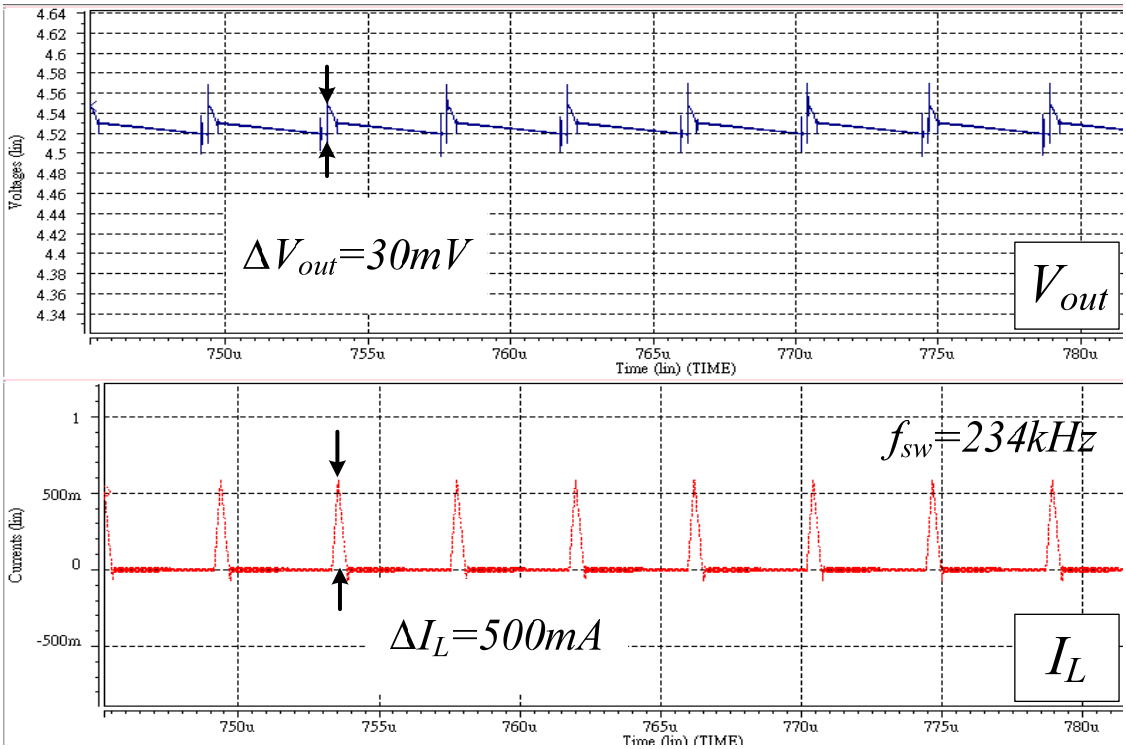
The waveforms of the output voltage and the inductor current during load transient response are shown in Fig. 27. The settling times are about 26μs and 27μs for V_{in} = 2.7V and the change in load current from 200mA to 400mA and from 400mA to 200mA, respectively. It demonstrates the CCM mode operation.

Fig. 28 shows the simulation efficiency of proposed structure. The switching frequency of the boost converter can be effectively reduced at light load. As a result, the efficiency can be kept larger than 90% at load current= 10mA. It demonstrates that the efficiency can be kept high due to the implementation the technique.

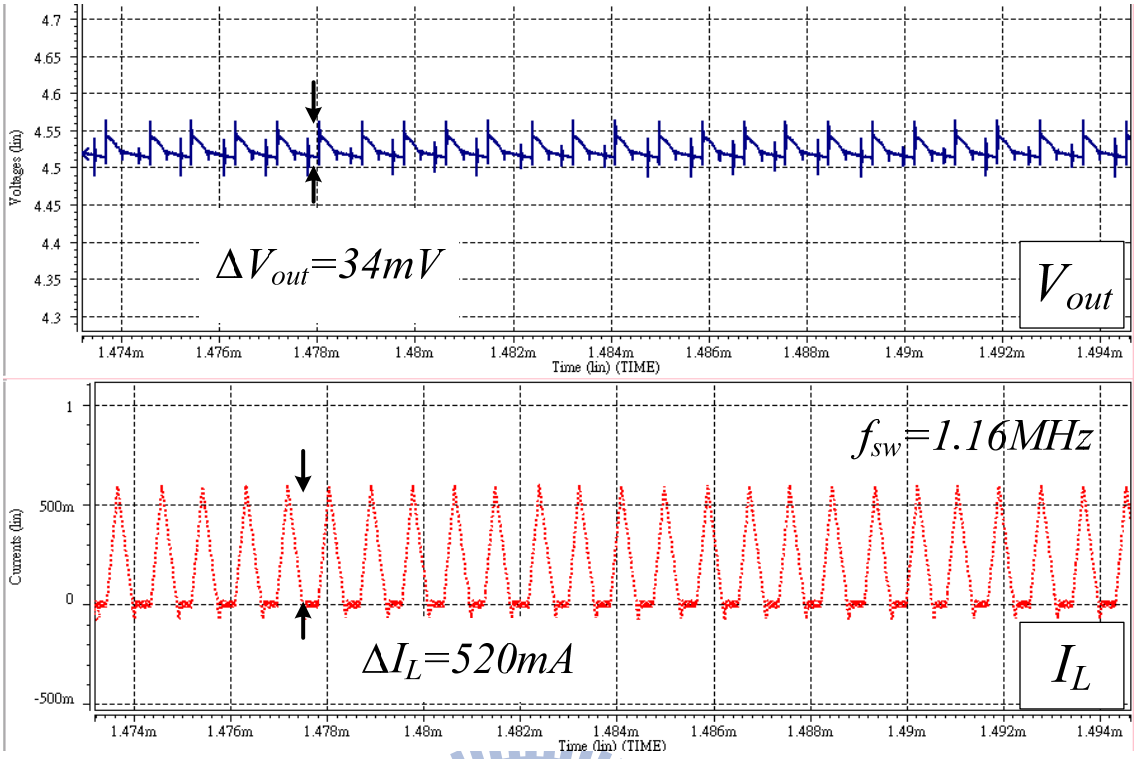
Table IV. THE DESIGN SPECIFICATION

SPECIFICATIONS	
Technology	TSMC 0.25μm 1P3M
Chip size	1700μm × 1800μm
Supply variation (V_{IN})	2.7V - 4.5V
Output voltage (V_{OUT})	4.5V
Maximum output loading current	400mA
Inductor (L)	1μH
Output capacitor (C_O)	6.8μF

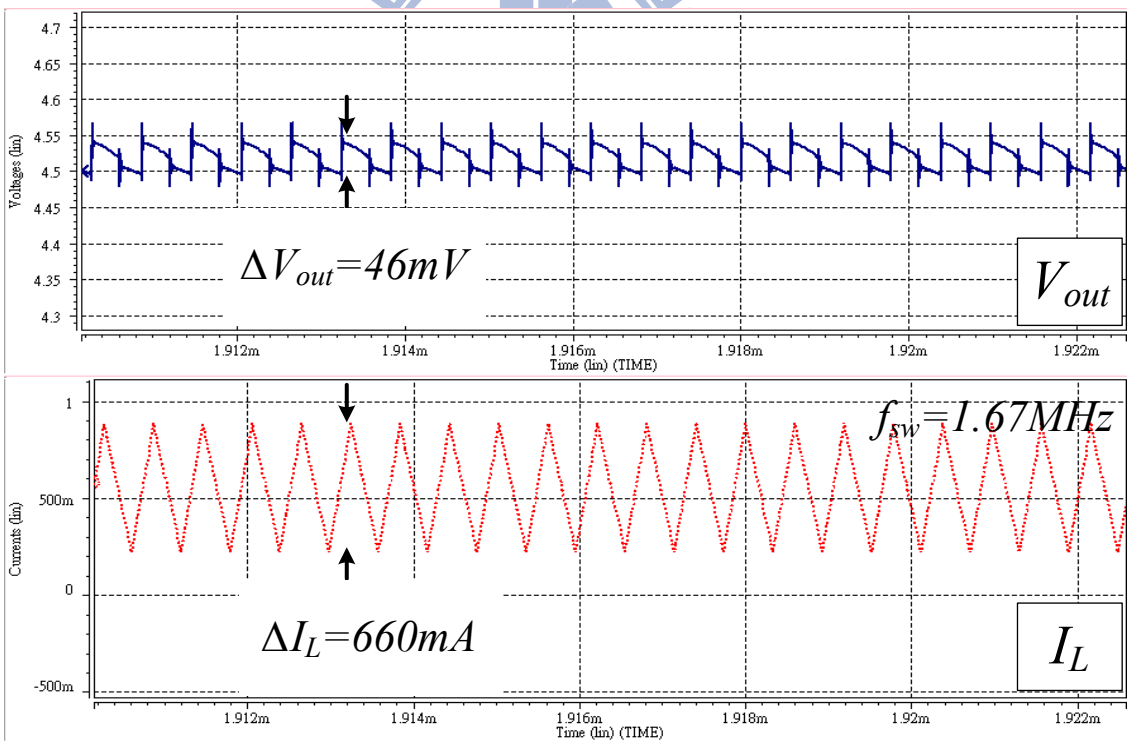
Equilibrium series resistance of the output capacitor (R_{ESR})	50mΩ
Operation temperature	0~100℃
PFM range	0mA - 150mA



(a)



(b)



(c)

Fig. 1. Waveforms in conventional boost converter with hysteresis control when load current changes from 70mA to 270mA within 2μs.

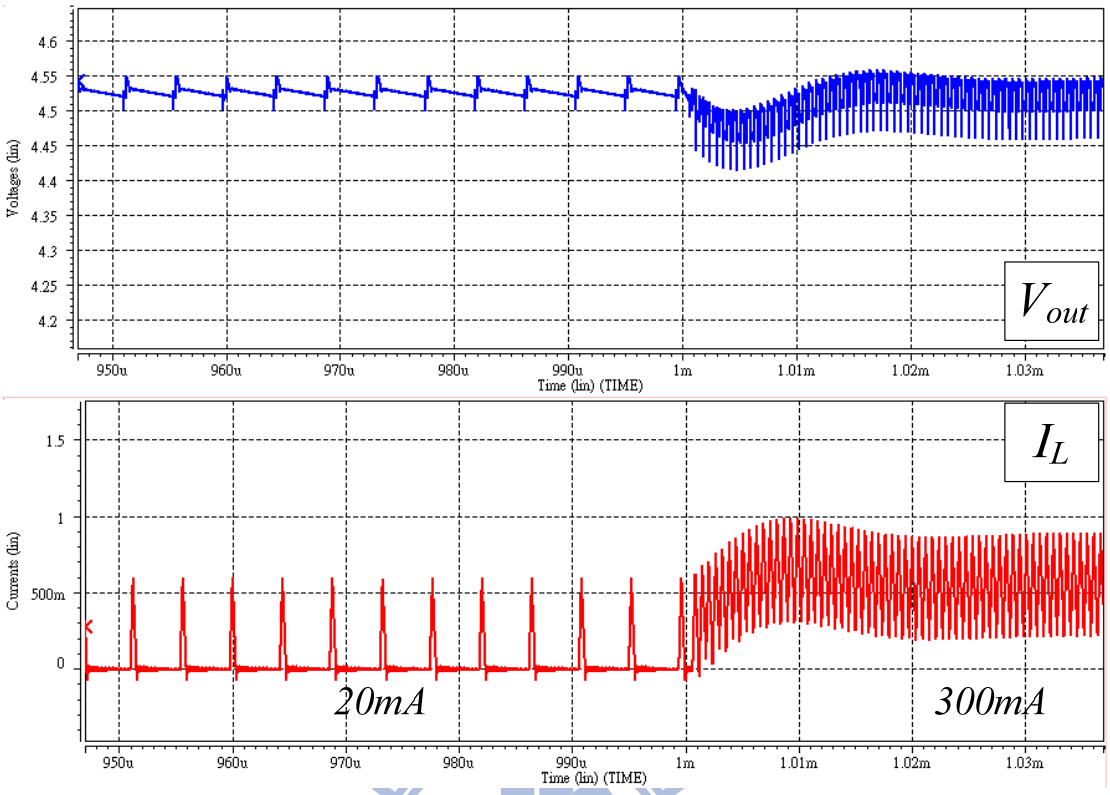
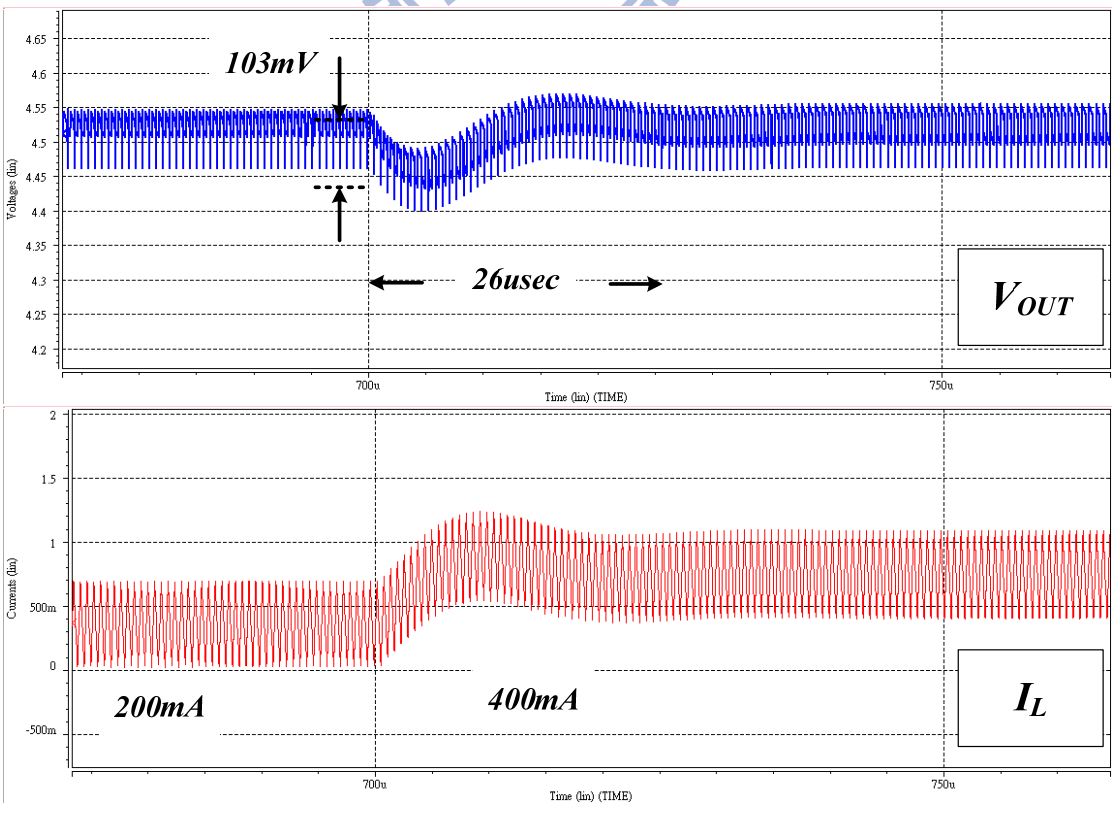
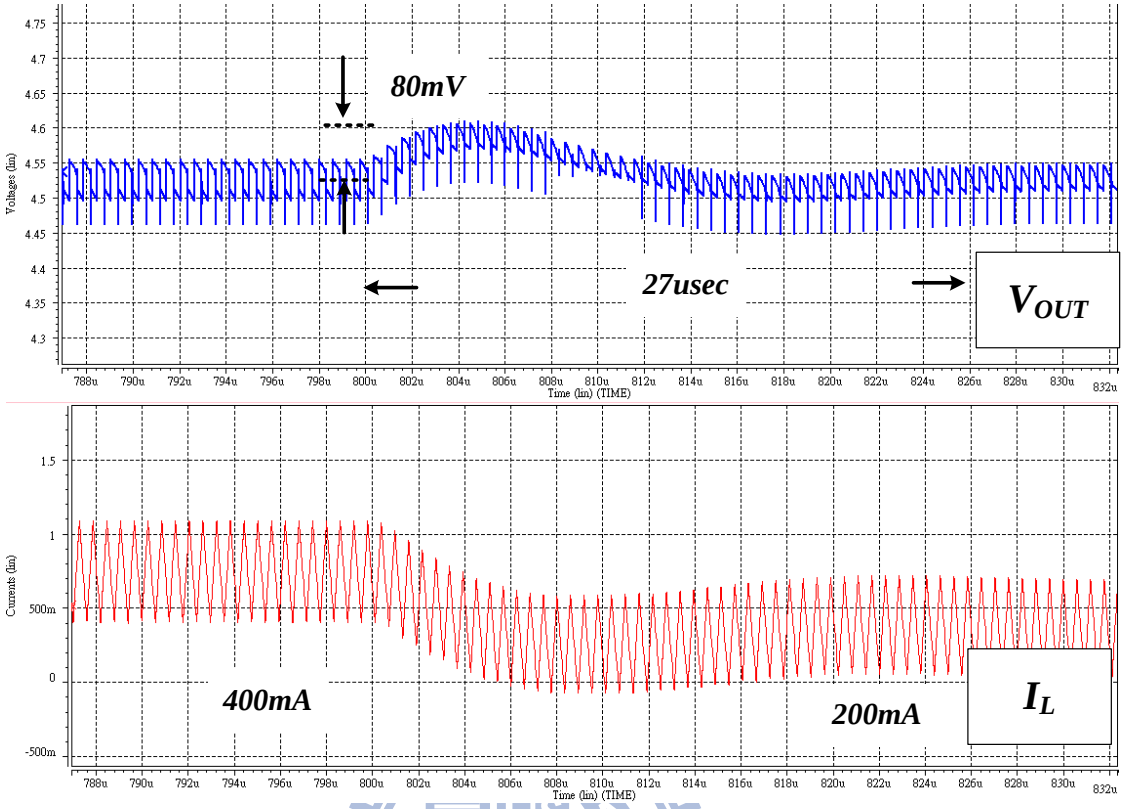


Fig. 252. Transition state waveform.



(a)



(b)

Fig. 26. Waveforms in the proposed boost converter with the CSC technique (a) when load current changes from 200mA to 400mA within 2μs and (b) when load current changes from 400mA to 200mA within 2μs.

Table V. COMPARED WAVEFORMS

IL	fs	Vout ripple
4mA	55kHz	34mV
6mA	71kHz	31mV
8mA	97kHz	30mV
10mA	114kHz	31mV
20mA	234kHz	30mV

40mA	460kHz	31mV
60mA	714kHz	32mV
80mA	909kHz	31mV
100mA	1.16KHz	34mV
200mA	1.66MHz	37mV
300mA	1.67MHz	46mV
400mA	1.7MHz	50mV

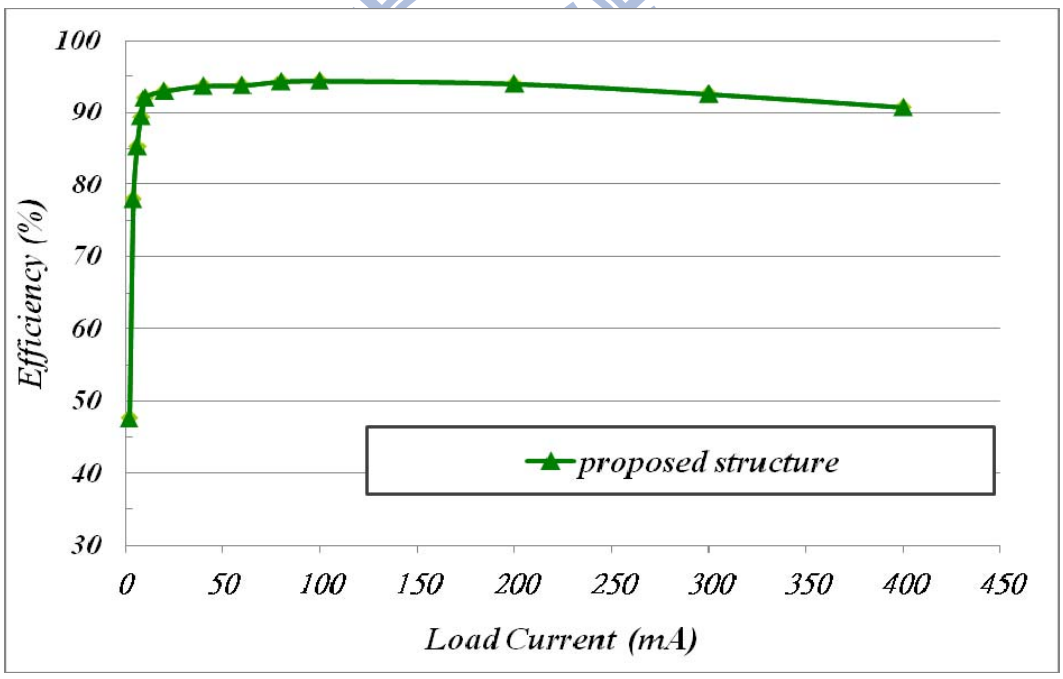


Fig. 27**.** Power conversion efficiency.

Chapter 6

Conclusion

The proposed CSC technique in boost converters can speed up transient response due to the current-mode hysteresis control and improve efficiency over a wide load range. The CSC technique behaves high accuracy similar to the current-mode control without the need of slope compensation for simplicity. The load-dependent switching frequency at light loads results in high power conversion efficiency. Experimental results show that the output voltage ripple can be kept smaller than 50mV over a wide load current range from 0mA to 400mA with power conversion efficiency higher than 90% at load current of 10mA.

6.1 Future Work

The CSC technique also minimizes the external components and thus it has the advantage of small footprint. But the CSC has the same disadvantage of the complex design the EMI filters because of the frequency variation along with the input supply and output voltage. Therefore, the improvement of EMI issue is important in the future.

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