# 國立交通大學

## 電機與控制工程學系

## 碩士論文

# 減少等效串聯電感效應且不須等效串聯電阻補償的固定導通時間控制直流直流降壓轉換器

# Reduction of Equivalent Series Inductor Effect in Constant On-Time Control DC-DC Converter without ESR Compensation

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碩 士 論 文

A Thesis
Submitted to Department of Electrical and Control Engineering
College of Electrical Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Master
in

Electrical and Control Engineering

October 2010

Hsinchu, Taiwan, Republic of China

中華民國九十九年十月

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## 摘　要

隨著可攜式產品的需求逐漸增加，用來提供可攜式產品系統電源且具有高效能以及小體積的電壓穩壓器變得越來越重要。常見於實際應用的固定導通時間控制法電壓穩壓器具有幾項優點，如快速暫態反應、系統結構簡單，以及在輕負載時具有高效率的優點。一般來說，固定導通時間控制法穩壓器是利用輸出端訊號的漣波來穩壓，但是傳統的控制法使用具有小等效串聯電阻的輸出電容時，由於輸出端訊號的漣波僅有電容的成分，故漣波很小系統易受雜訊影響。因此傳統上須使用大等效串聯電阻的輸出電容才可有效控制系統。

本文提出之固定導通時間直流轉換器不須使用等效串聯電阻補償且可消除輸出電容上的等效串聯電感效應。此外快速暫態反應與小電壓降變化皆可達成。並且由於導通時間可隨輸入及輸出電壓調整，操作在連續導通模式時的系統切換頻率可以在廣泛的輸入電壓裡維持幾乎定值。模擬結果顯示出輸出電壓漣波維持小於 5 mV，在負載變動範圍為 500 mA 時輸出電壓的回復時間小於 10 μs。此時使用的等效串聯電阻小於5 mΩ。

Reduction of Equivalent Series Inductor Effect in Constant On-Time Control DC-DC Converter without ESR Compensation

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## Abstract

With the growing demand of portable devices, voltage regulators which have high performance and compact size become more important to provide system power. Constant on-time control regulators are preferred in practice for some important advantages, such as fast response time, simple system structure and good efficiency for light load. In general, constant on-time control regulators regulate their output voltage based on the ripple component in the output signal. However, in conventional constant on-time control with small ESR value on the output capacitor, the regulator is easily affected by the noise due to small output ripple, which is dominated by the ripple on the output capacitor. Thus, for constant on-time control regulators, an output capacitor with a large ESR has to be used so that effective ripple control can be realized.

The proposed constant on-time control DC-DC converter removes the need of conventional equivalent series resistor (ESR) compensation and simultaneously aims to eliminate equivalent series inductor (ESL) effect of the output capacitor. Besides, fast transient response and small dip voltage variation can be achieved. Furthermore, since the on-time period is set simply by input and output voltages, the switching frequency in continuous conduction mode (CCM) operation is relatively constant over a wide input voltage range. Simulation results show that the output ripple and the recovery time keep smaller than 5mV and 10μs, respectively, when load current step is 500mA and ESR is smaller than 5mΩ.

# 誌 謝

首先要感謝我的指導老師陳科宏博士，有老師在這兩年多來的細心指導，才得以讓這篇論文順利的完成。在研究所的這兩年多，老師教導我許多電路上的知識，以及作電路的技巧，充實了我許多的專業知識。此外，平時還會教導我許多待人處事的道理，讓我的知道在畢業之後如何在社會上立足。非常感謝老師在研究所時期的諄諄教誨。

同時要感謝實驗室的小乖、輝哥、小契、小菜、國林學長，在我研究遇到困難時，都會細心解惑，分享了許多坐電路的經驗，讓我受益良多。接著，要感謝小瑛瑛、小群群、五點、士偉，你們在我求學過程中，一起討論、一起研究，在研究之餘，也一起玩樂，有了你們陪伴，讓我的研究所回憶增添不少色彩，感謝你們。再來，要感謝 Lab 912 的學長、同學以及學弟妹們，有了你們的幫助，讓我在實驗室研究順利。

感謝我的女友雅萍，對我的支持與包容，以及在實驗室的陪伴，在繁雜的課業以及研究進度下，讓我減輕許多壓力，才得以繼續朝目標努力，順利的畢業，往下個目標邁進。最後要感謝我的父母，以及家人，有了你們的支持與關心，讓我無憂無慮地作研究，專心在課業上的進度，感謝你們。

謹以此篇論文獻給我身邊的每位好朋友。

# Contents

# Figure Captions

# Table Captions



# Chapter 1

# Introduction

Portable devices such as cellular phones, laptops, and PDAs are widely used in today's life. For the electronic device application, compact size and high performance voltage regulator plays an important role to provide system power. To extend the battery life of the battery-operated devices is the important issue for power management module in portable devices.

In this chapter, we will show the background and basic knowledge of power management system in chapter 1.1 firstly. The classification of power management circuits which including switching converters, linear regulators, and charge pump converters will show in chapter 1.2. The motivation will give in chapter 1.3. Finally, the thesis organization will show in chapter 1.4.

## 1.1 Power Management System

According to increasing demand for low-power multifunction system-on-a-chip (SOC), more and more functions are embedded in a device to meet the requirement. However, the growing of battery energy is not satisfied to chip requirement. As shown in Fig. 1, the growing of battery energy is not enough to supplying power of chips in the future. The running time of the portable devices, such as the lap tap, mobile phones and digital cameras, is a very important requirement for the consumers. Therefore, how to save the battery energy and use it more efficiently is the most important topic for power management system.

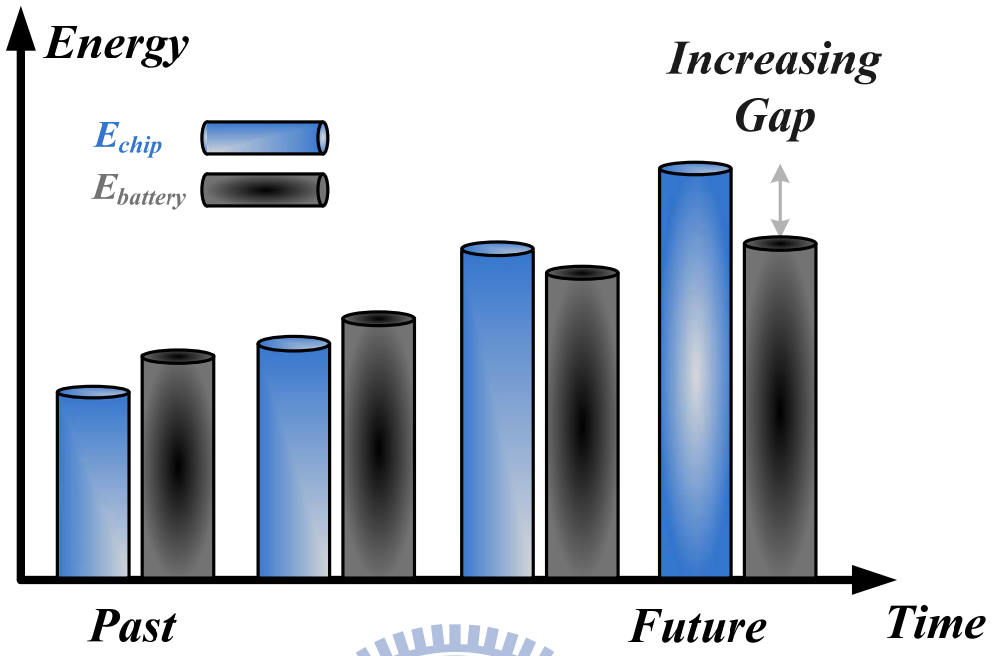



Fig. 1. Energy constrained operation.

As mentioned above, the increasing battery content doesn't satisfy device requirement. Therefore, we construct the power management system managing battery energy efficiently. As shown in Fig. 2, it may have many power devices for a mobile phone, which needs four regulated voltages, one buck converter for core micro processor, one boost converter for LCD panel, one charge pump for white LED driver and one Low-dropout (LDO) regulator for RF power amplifier [1]. The system of cell phone will operate in different modes, such as sleeping mode, communication mode and so on. And these blocks are only needed powered when the function are active. The control unit is used to control these block enable or disable, respectively. As a result, we can enhance system efficiency by using the control unit cell that decides the operational mode of power supply module.

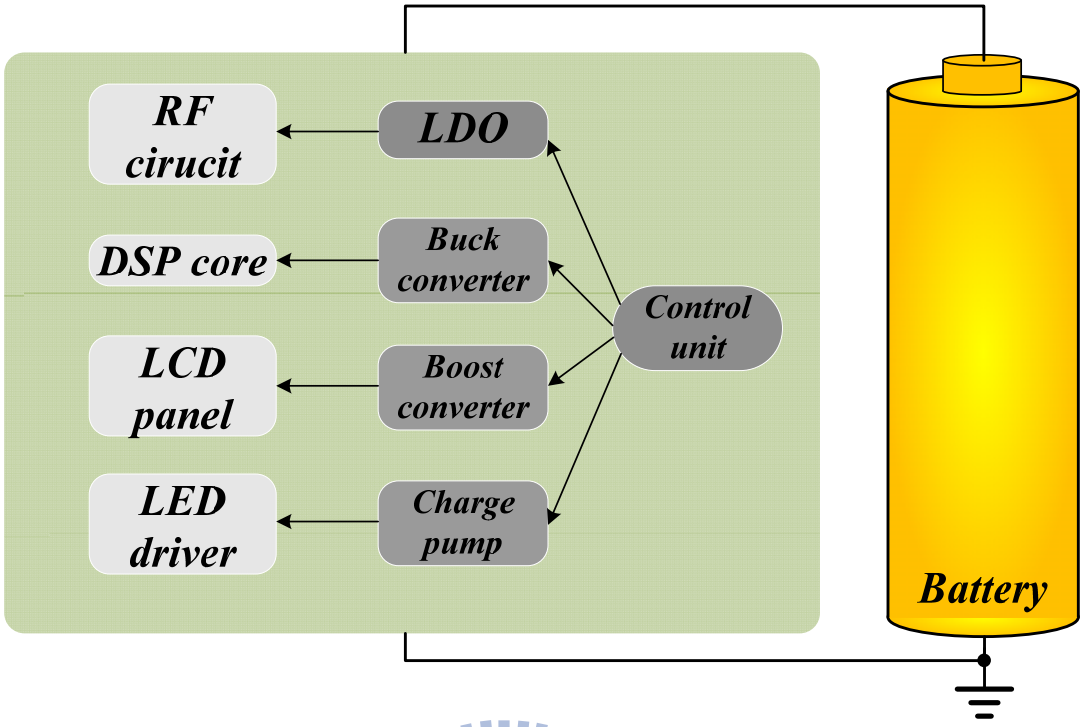



Fig. 2. Power management system.

## 1.2 Classification of Voltage Regulators

In this section, three types of voltage regulators will be introduced briefly, including linear regulators, switched capacitor circuits and switching regulators. Finally, a brief comparison will be given about three types of voltage regulators. The comparisons included circuit complexity, cost, efficiency, load ability and so on.

### 1.2.1 Linear Regulator

Linear regulator is also called LDO voltage regulator because there is a low drop-out voltage between input and output pin about 100~500mV [2]. LDO regulators are widely used as power management ICs in portable communication systems since they occupy a small chip area and can convert Li-Ion battery voltage to a low-noise and high-precision voltage to noise-sensitive analog blocks for ensuring high performance. The characteristic

of LDO is compact without complex control unit, results in smaller chip size and cost. As shown in Fig. 3, the construction of LDO regulators usually utilizes a pass device, an error amplifier and a resistive feedback network. The pass device typically uses a p-type MOSFET for low dropout voltage. The error amplifier is used to regulate output voltage by controlling the pass device to supply load current. That is, LDO regulator utilizes the feedback network to construct shunt negative feedback effect to regulate output voltage. Therefore, LDO regulator does not need oscillation clock, then the output noise can be minimized and the output voltage does not have ripple. However, the disadvantage of this type regulator is the conversion efficiency, which is about the output voltage dividing input voltage. The highest efficiency occurs when output voltage is near input voltage. Besides, the supply load current ability is dependent on the pass device's size.

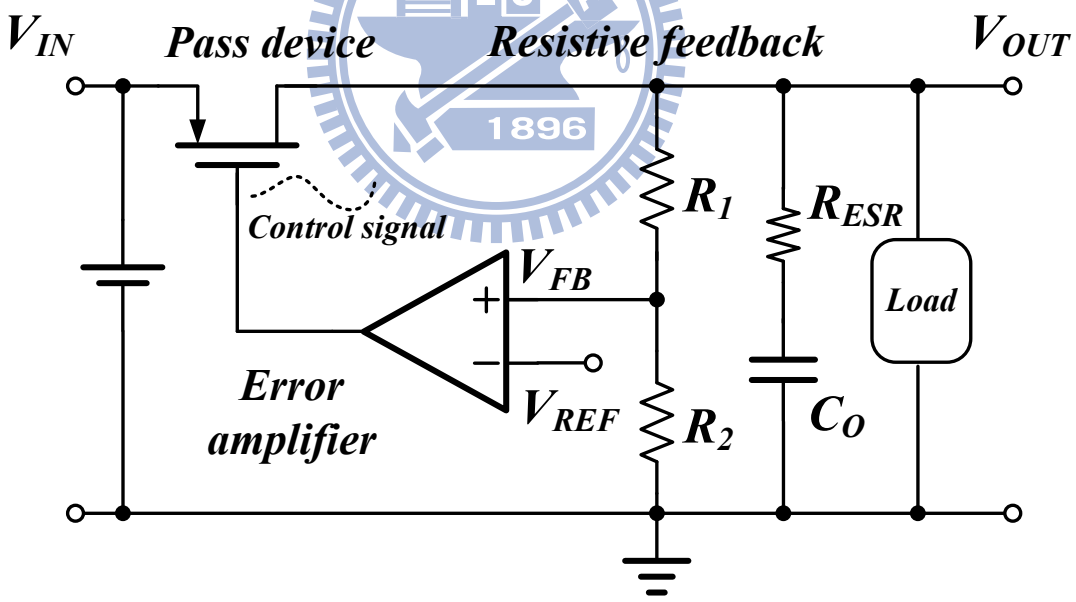



Fig. 3. The basic structure of linear regulator.

## 1.2.2 Charge Pump

The features of charge pump are described as follows [3] [4]. Firstly, the charge pump can be operated in both buck and boost mode, it depends on the reference voltage of the hysteric feedback control, but it is more efficiently in boost mode operation. Secondly, the circuit complexity of charge pump is between linear regulator and switching regulator. Thirdly, the electromagnetic interference (EMI) and switching noise problem are not heavier than switching regulator because of lower switching frequency. Finally, the load ability is weak because of output capacitor and switching frequency.

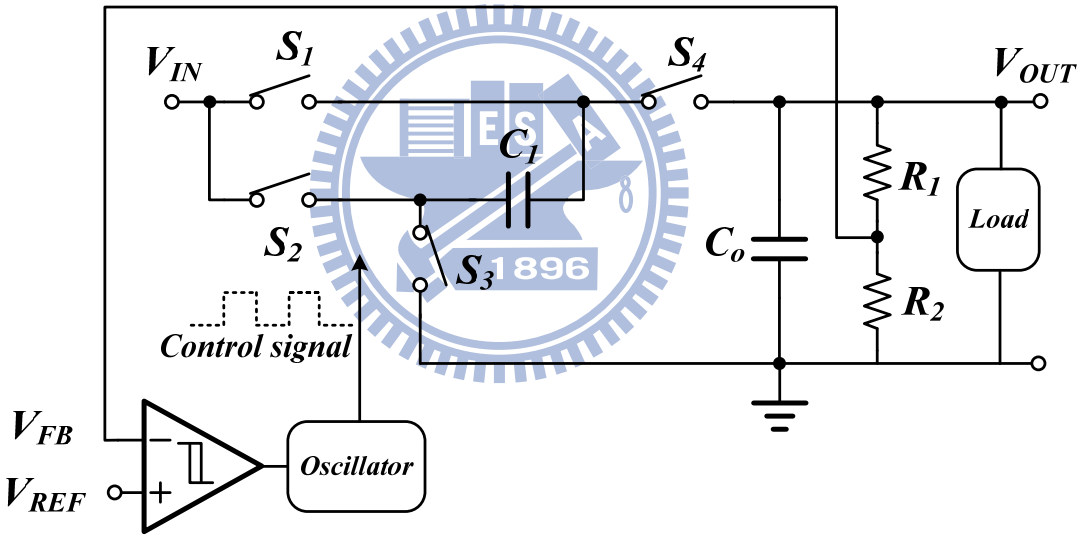



Fig. 4. The basic structure of charge pump.

Fig. 4 shows the basic structure of two phase charge pump regulator. It consists of four switches, two capacitors, one hysteric comparator, one oscillator and resistive feedback. The operation concept is charging and discharging the capacitor $C_1$ in complementary phases. Firstly, during phase $\Phi_1$, switches $S_1$ and $S_3$ are closed and switches $S_2$ and $S_4$ are opened, the capacitor $C_1$ is charged by input to $V_{in}$ approximately. Secondly, during phase $\Phi_2$,

switches $S_1$ and $S_3$ are opened and switches $S_2$ and $S_4$ are closed. $V_{in}$ added the voltage on capacitor $C_1$ to charge output capacitor $C_o$, so $C_o$ maintains an output voltage close to $2V_{in}$. With the hysteric feedback control, the output voltage level can be regulated at a desired value.

### 1.2.3 Switching Regulator

Switching regulators are mixed-signal circuits which have both analog and digital block in feedback loop. An analog signal which is error signal feeds back to produce a digital signal at a certain frequency rate which calls duty cycle. Output capacitor and inductors use duty cycle to regulate output voltage. The basic structure of buck type voltage mode switching regulator is shown in Fig. 5 [5]. The power stage of switching regulator consists of a couple of complementary power MOSFET ($M_P$ $M_N$), passive storage elements inductor ($L$) and capacitor ($C$) and resistive feedback network ($R_1$ $R_2$). Detailed operation is described as follows; the resistors $R_1$ and $R_2$ sensing the variation of output voltage and error amplifier receives the voltage variation information then brings the error signal ($V_C$). The comparator's inputs receive the error signal from error amplifier and the ramp signal ($V_{RAMP}$) from ramp generator, then compares the quantity between the error signal and the ramp signal to decide the duty cycle. After generating the control signal, the PWM generator control the detail timing to avoid short through current. At last, the purposes of gate drivers are driving huge complementary power MOSFET.

Generally speaking, the conversion efficiency of switching regulator can achieve above 90% under heavy load condition. Meanwhile, with higher switching frequency in the range from hundreds of Kilo-Hertz to several Mega-Hertz, the storage components can be designed smaller to save the cost. But the EMI and noise problems become critical. The supply load

ability is the largest always in the range about hundreds of milliamps to several amps.

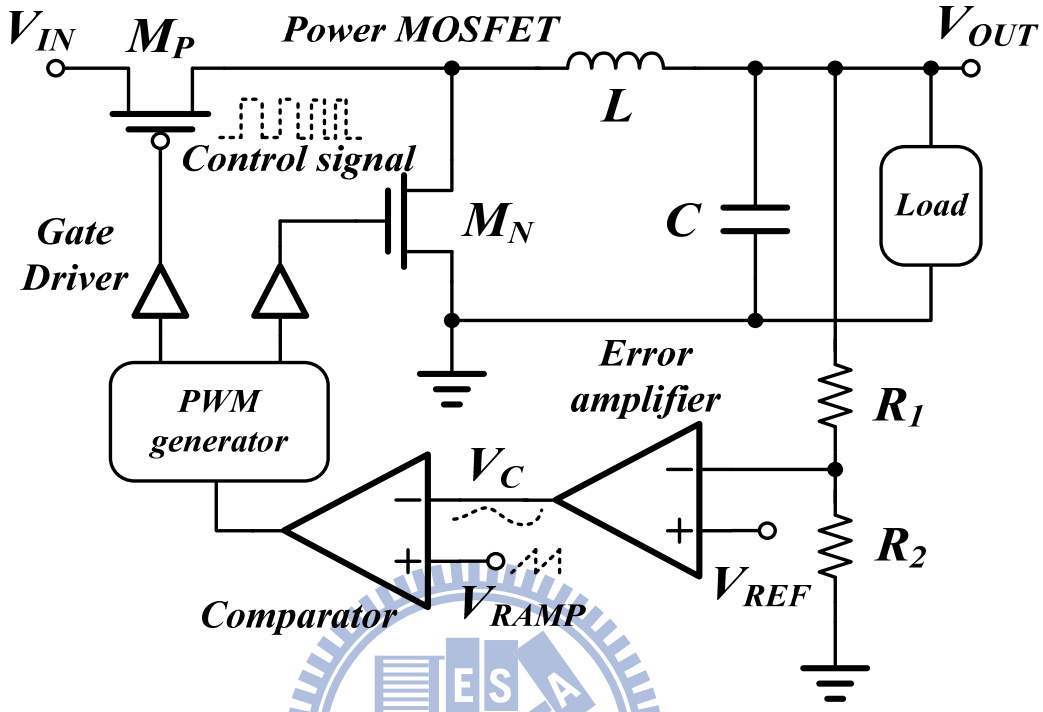



Fig. 5. The basic structure of buck type voltage mode switching regulator.

The characteristics of switching regulator are described as the following. Firstly, due to the storage components such as inductor and capacitor, the switching regulator can operate in three kinds of type including buck, boost and buck-boost mode. But the more external components cause the bigger PCB size and cost. Secondly, it suffers from EMI and switching noise problem due to switching based circuits.

## 1.2.4 Comparison

As the above description, three types of voltage regulator have its own advantages and disadvantages. How to choose the best voltage regulator as power supply depend on the electronic applications characteristics and specifications. The comparison of different type

voltage regulator is listed in TABLE I.

TABLE I. COMPARISONS OF DIFFERENT TYPE REGULATORS.

| *Characteristics* | *Linear Regulator* | *Switching Regulator* | *Charge Pump* |
|---|---|---|---|
| *Regulation Type* | ***Buck*** | ***Buck/boost/buck-boost*** | ***Buck/boost*** |
| *Chip Area* | ***Compact*** | ***Large*** | ***Moderate*** |
| *Efficiency* | ***Minimum*** | ***Maximum*** | ***Medium*** |
| *EMI/Noise* | ***Minimum*** | ***Maximum*** | ***Medium*** |
| *Load ability* | ***Medium*** | ***Maximum*** | ***Minimum*** |
| *Complexity* | ***Simplest*** | ***Complicated*** | ***Medium*** |
| *Cost* | ***Low*** | ***High*** | ***Medium*** |

## 1.3 Motivation

The buck converters are widely used in portable devices to provide power from battery. In these applications, the DC-DC converter has to regulate the output voltage to lower voltage and must quickly respond to load current variation to keep the output voltage within a limited range. Conventional control methods for switching converter such as voltage-mode and current-mode control include the error amplifier, which is connected with frequency compensation network, to compensate for step changes in the load current. However, it leads to relatively slow response time and thus makes the switching converter hard to meet the load transient response requirement.

Switching converters using the output voltage ripple as the PWM ramp signal have been widely used to extend the battery life due to the simple control mechanism [6] [7].

Besides, the response time of line and load transient is fast due to large control loop bandwidth. Its control method is usually called ripple-based control [8] [9]. Ripple-based control methods include hysteretic control, constant on-time control, and constant off-time control. The hysteretic control is widely used for buck converter to achieve a fast transient response, and the circuitry of the hysteretic control method is compact without complexity. But the major disadvantage of the hysteretic control is the noise effect on the output voltage ripple. This noise can prematurely terminate or initiate a switching period. Another drawback is the switching frequency is affected by parasitic parameters and can change a lot with different input and output voltage.

Constant on-time control operates at a relatively constant frequency without a oscillator due to the on-time period is set by input supply voltage and output voltage, and it does not require error amplifier and loop compensation network, leads to a fast line and load transient response due to its wide control bandwidth. For practical implementation, the equivalent series resistance (ESR) of the output capacitor can be used as the sensing resistor, which means the output voltage ripple including the current information. Moreover, the larger ESR value can reduce the noise effect on the output voltage ripple because of large output voltage ripple induced by ESR, but the unfavorably large overshoot/undershoot voltage in transient period comes from the use of large ESR. Therefore, in this thesis, a constant on-time control DC-DC converter without ESR compensation allows to use low ESR output capacitors, eliminating the need for ESR induced output ripple.

## 1.4 Thesis Organization

The thesis introduces the basic knowledge of switching regulator in the Chapter 2. In the Chapter 3, the design and architecture of constant on-time control DC-DC converter without ESR compensation are presented. The internal overall circuit implementation and simulation results are shown in Chapter 4. Finally, the whole system chip simulation, system specification, conclusions and future work are presented in Chapter 5.

# Chapter 2

# Basic Knowledge of Switching Regulator

In this chapter, the basic knowledge of switching regulator is presented. The characteristics and performance specification of switching regulator are shown in section 2.1. In section 2.2, the controlling modulator including pulse width modulation (PWM) and pulse frequency modulation (PFM) are introduced. Three kinds of ripple-based control method including hysteretic control, constant on-time control and constant off-time control are described in section 2.3.

## 2.1 Performance Specification of Switching Regulator

Due to more and more electronics application need to be supplied by switching converter, the performances of switching converter have to be considered. The following are significant specifications of switching regulators. Firstly, the conversion efficiency of switching regulator is an important topic, how to keep high efficiency over wide loading range and loss analysis will be discussed in the section 2.1.1. The second part is excellent load and line regulation, the lower steady-state error of switching regulator will be discussed in the section 2.1.2. The final part is transient response, how to immediately response when the sudden large current changing will shown in the section 2.1.3.

### 2.1.1 Losses and Efficiency

#### 2.1.1.1 Conduction Loss

Power loss of regulators is the combination of the switching loss and the MOSFET's conduction loss in Eq. (1). The conduction loss also can classify into high-side transistor loss and low-side transistor loss.

$$P_{MOSFET} = P_{SW} + P_{COND} \quad (1)$$

Calculating the high-side conduction loss is straightforward that the conduction loss is just the $\boldsymbol{I^2R}$ loss timing the MOSFET's duty cycle as below:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot \frac{V_{OUT}}{V_{IN}} \quad (2)$$

Where $\boldsymbol{R_{DS(ON)}}$ is at the maximum operation MOSFET junction temperature ($\boldsymbol{T_{J(MAX)}}$) Low-side loss are also comprised of conduction loss and switching loss. Conduction loss for low-side is given by:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

#### 2.1.1.2 Switching Loss

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current power MOSFET's gate to charge its input capacitance. There is no switching loss until $\boldsymbol{V_{GS}}$ reaches the MOSFET's $\boldsymbol{V_{TH}}$ therefore power loss equal zero.

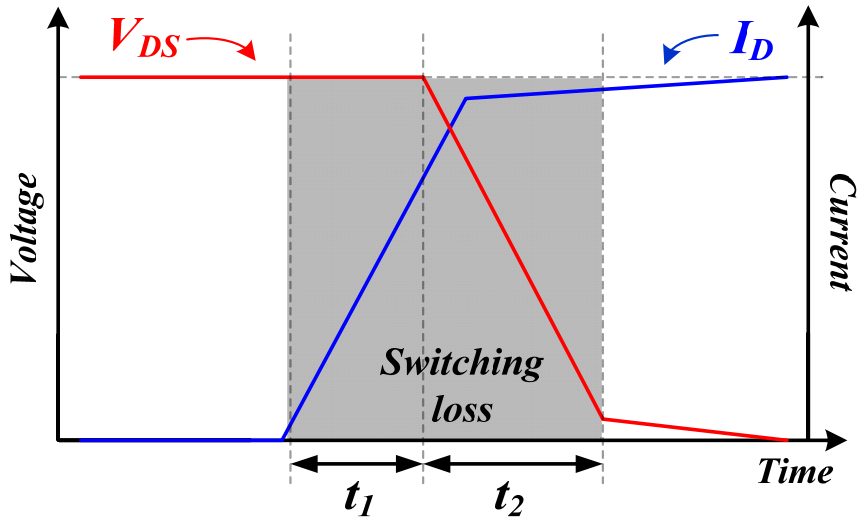



Fig. 6. Transient waveform of $V_{DS}$ and $I_D$ curve in switching losses.

When $V_{GS}$ reaches $V_{TH}$, the input capacitance ($C_{ISS}$) is being charged and $I_D$ (the MOSFET's drain current) is rising linearly until it reaches the current $I_L$ which is presumed to be $I_{out}$. During this period ($t_1$) the MOSFET is sustaining the entire input voltage across it, the energy in MOSFET during $t_1$ is:

$$P_{t_1} = t_1 \cdot (\frac{V_{in} \cdot I_{out}}{2}) \quad (4)$$

Now, we enter $t_2$. At this point, $I_{out}$ is flowing through high-side MOSFET, and the $V_{DS}$ begin to fall. All of the gate current will be going to recharge $C_{GD}$. $C_{GD}$ is similar to the "Miller" capacitance of transistor, so $t_2$ could be thought of as "Miller time". During this time the current is constant (at $I_{out}$) and the voltage is falling fairly linearly from $V_{IN}$ to $0$, therefore:

$$P_{t_2} = t_2 \cdot (\frac{V_{in} \cdot I_{out}}{2}) \quad (5)$$

The switching loss for any given edge is just the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval:

$$P_{SW} = (\frac{V_{in} \cdot I_{out}}{2}) \cdot (t_1 + t_2) \cdot F_S \quad (6)$$

### 2.1.1.3 Static Loss

The static loss also called as quiescent loss that was consumed by controllers of switching regulators. The smaller quiescent loss had higher efficiency.

$$P_Q = V_{in} \cdot I_Q \tag{7}$$

The other power losses that don't be mentioned above obeyed the rules of $\boldsymbol{I^2R}$.

### 2.1.1.4 Efficiency

The efficiency of switching regulator is defined as the ratio of the output power consumption and input power supplies, formed as below:

$$E_{ff} = \frac{P_O}{P_{in}} = \frac{P_O}{P_O + P_Q + P_{SW} + P_{COND} + P_{Else}} \times 100\% \tag{8}$$

The input power supplies consist of the output consumption ($\boldsymbol{P_O}$), quiescent loss ($\boldsymbol{P_Q}$), switching loss ($\boldsymbol{P_{SW}}$), conduction loss ($\boldsymbol{P_{COND}}$) and other losses ($\boldsymbol{P_{Else}}$) in parasitic elements. A high efficiency results in a high performance extending the battery life.

## 2.1.2 Load and Line Regulation

Switching regulators are powerful system of stepping up or down the desires voltage. Therefore, to keep the regulated voltage and decrease the steady state error when increasing the supply voltage and load condition of DC-DC converter is most important.

The load regulation is defined as the percentage of steady state error of output voltage when the load condition changes and can be calculated as follows.

$$Load\ Regulation = \frac{\Delta V_{out}}{V_{out\_norm}} . \frac{100}{\Delta I_{load}} \left( \frac{\%}{mA} \right) \quad (9)$$

The line regulation is defined as the percentage of steady state error of output voltage when the input voltage changes and can be calculated as follows.

$$Line\ Regulation = \frac{\Delta V_{out}}{V_{out\_norm}} . \frac{100}{\Delta V_{IN}} \left( \frac{\%}{mV} \right) \quad (10)$$

### 2.1.3 Transient Response

The transient response is an important specification of DC-DC converter for the system applications [10]. The large load current changes suddenly will cause a voltage fluctuation at output of DC-DC converter. The voltage fluctuation may trigger the logic circuit or affect the analog circuit. Therefore, it's important to reduce the large voltage changing and the time during voltage variation. The transient response of output voltage relates to load current is shown in Fig. 7. During the first period $\Delta t_1$, the large current flow into the output load from DC-DC converter, due to the DC-DC converter cannot provide enough energy to maintain the output voltage, the output voltage will drop in this period because the output capacitor discharges the energy to support the load current. The drop voltage is shown in Eq. (11). According to the parameters of Eq. (11), selecting the output capacitor well can reduce the drop in this period.

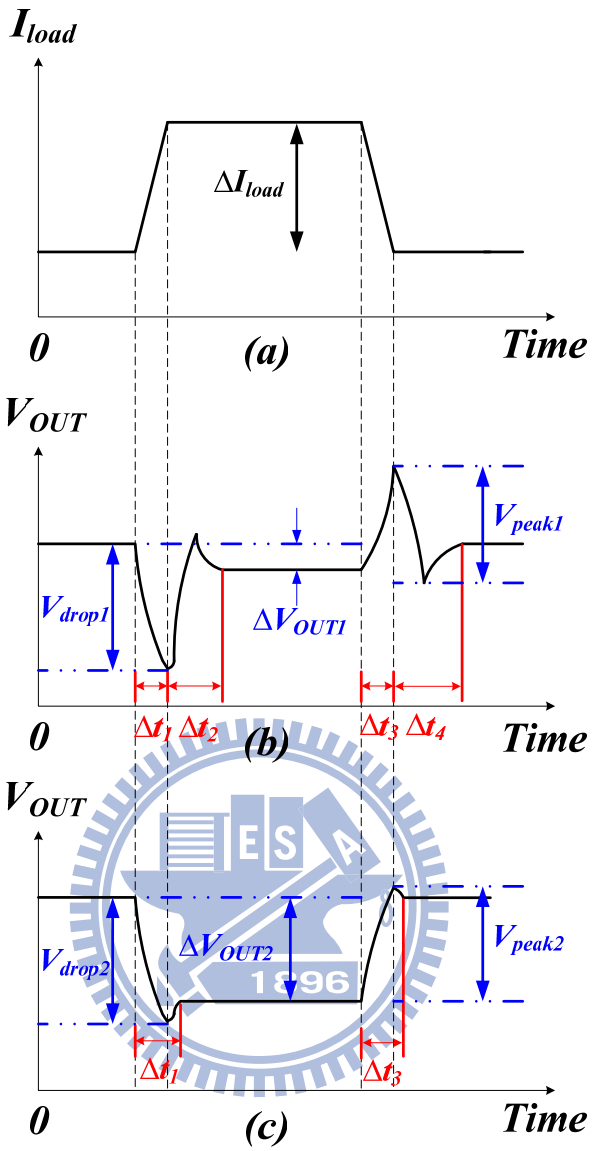



Fig. 7. The transient response of output voltage relates to load current.

$$V_{drop1} = V_{drop2} = \Delta I_{out} \times \left( \frac{\Delta t_1}{C_{out}} + R_{ESR} \right) \tag{11}$$

During the second period $\Delta t_2$, the system senses the output variation by feedback loop then turn on the power P-type MOSFET to recover the regulated output voltage. The sum of $\Delta t_1$ and $\Delta t_2$ is called the recovery time and the second period $\Delta t_2$ depends on the system bandwidth of the DC-DC converter

The static error $\Delta V_{OUT}$ between light load and heavy load is relates to the voltage regulator DC gain, the higher DC gain bringing the better load regulation [11]. Comparing

to the Fig. 7(b) and Fig. 6(c), the performance of Fig. 7(b) due to the large DC gain and causes the better load regulation, but the second period $\Delta t_2$ extend the recovery time. However, it reduces the time of transient response. The performances of Fig. 7(c) due to the poor DC gain and cause huge static error but reduce the time of second period $\Delta t_2$ and improve the dynamic performance.

When the load current is decreasing to light load suddenly, the output voltage will jump until the DC-DC converter start to recovery the regulated voltage. The redundant current charges the output capacitor resulting to a peak voltage as shown in shown in Eq. (12) before the feedback loop of DC-DC converter react.

$$V_{peak1} = V_{peak2} = \Delta I_{out} \times \left( \frac{\Delta t_3}{C_{out}} + R_{ESR} \right) \tag{12}$$

During the final period $\Delta t_4$ the output capacitor discharged the redundant current to feedback resistors. As mention described, the transient response is relates to the bandwidth of DC-DC converter, output capacitor, equivalent series resistance ($R_{ESR}$) of output voltage and the load current.

## 2.2 Modulation Technologies

There are two mainly kind of modulation technologies in switching regulators. Firstly, PWM modulates the switching signal by a fixed switching frequency. Secondly, PFM uses a hysteresis window to generate a switching signal. Both of the technologies modulate the on and off time of switches to control the energy transfer to output.

### 2.2.1 Pulse Width Modulation (PWM)

Operating with PWM control, the power MOSFET are controlled by a constant clock cycle, the PWM control waveform is shown in Fig. 8 [12] [13]. While the ramp signal is lower than the control signal, the PWM signal at high level; the ramp signal is higher than the control signal, the PWM signal changes to low level. The main modulation is change the width of every clock cycle by the control signal and the output voltage is determined by the duty ratio of the PWM signal.

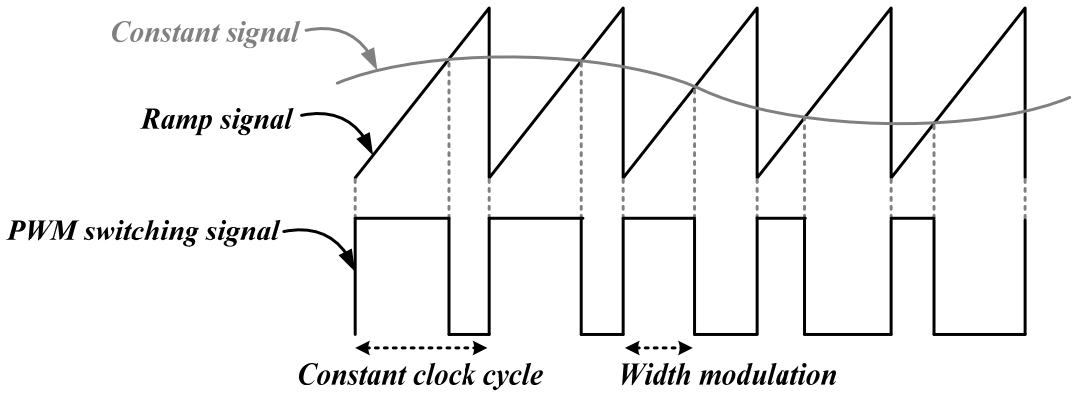



Fig. 8. Pulse width modulation waveform.

About the power consumption of PWM focus on the conduction and switching loss,

total power loss is expressed as follows.

$$P_{SW} + P_{CON} = I_{OUT}{}^2 R_{Duty} + (C_{GP} + C_{GN}) V_{IN}{}^2 F_{SW} \quad (13)$$

As shown in Eq. 13, operating at PWM control the switching frequency is constant but output current varies with loading. That is to say, the switching loss is invariable with load but conduction loss will increase with the output loading, as shown in Fig. 9.

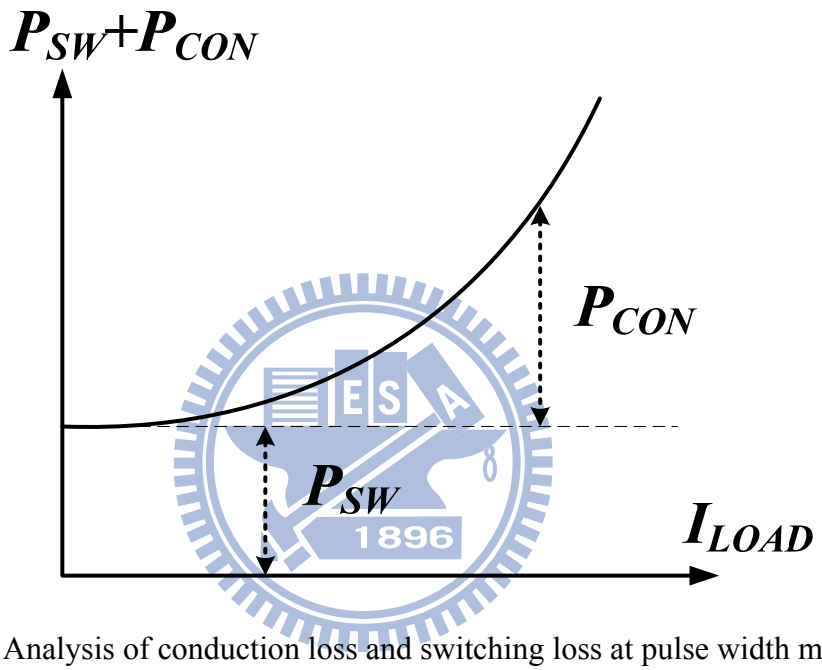



Fig. 9. Analysis of conduction loss and switching loss at pulse width modulation.

## 2.2.2 Pulse Frequency Modulation (PFM)

Operating with PWM control, the power MOSFET are controlled by a vary frequency, the PFM control waveform is shown in Fig. 10 [14] [15]. The on-time of PFM controller is constant width and off-time is variable with loading. By controlling the off-time of every switching cycle can obtain different switching signal to achieve desirable output voltage. Therefore, the smaller output loading can reduce the switching frequency.

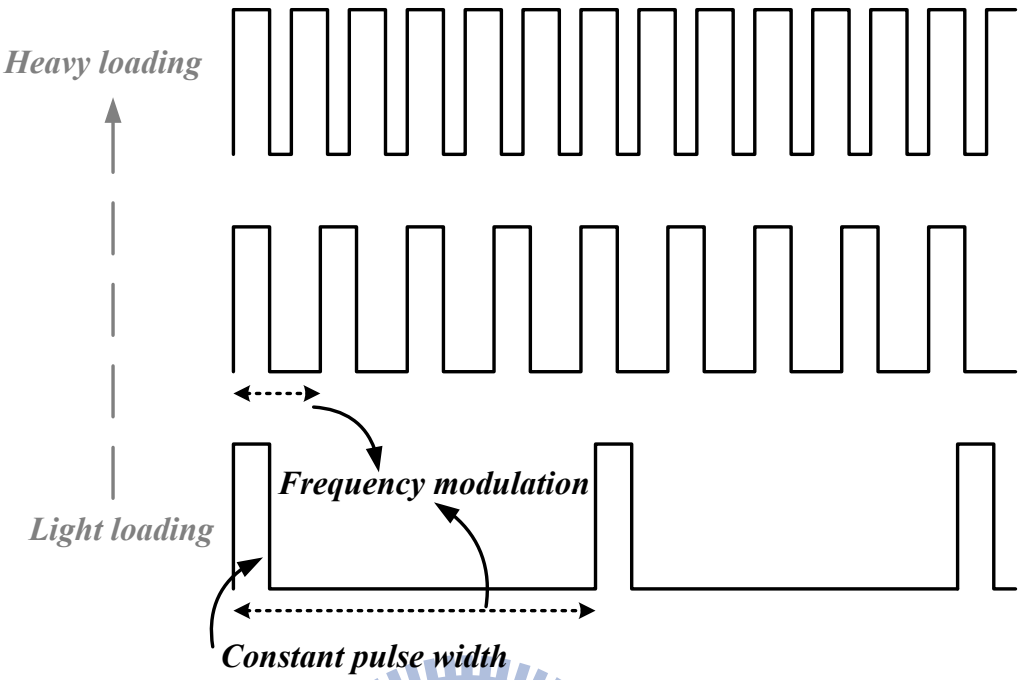



Fig. 10. Pulse frequency modulation waveform.

About the power consumption of Pulse Frequency Modulation also focus on the conduction and switching loss, total power loss is expressed as Eq. (13). Operating at PFM control both the switching frequency and output current varies with loading. That is to say, the switching loss and conduction loss will increase with the output loading, as shown in Fig. 11.

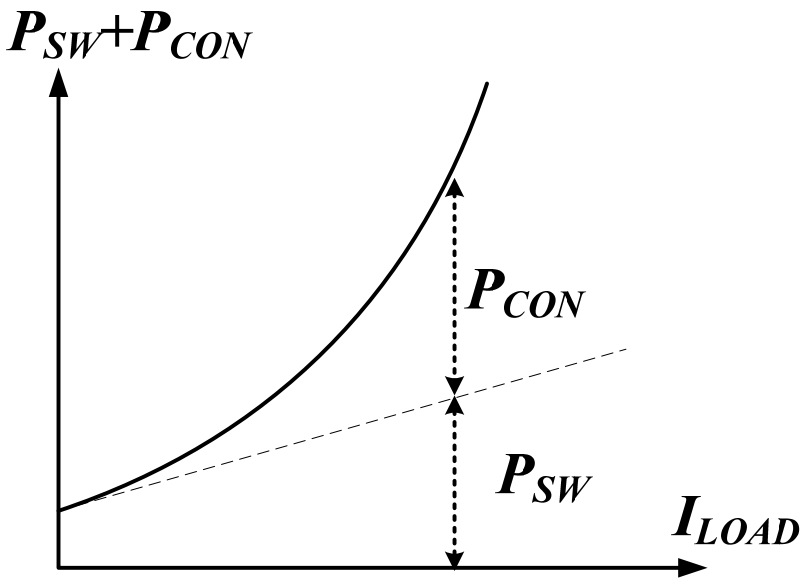



Fig. 11. Analysis of conduction loss and switching loss at pulse frequency modulation.

# 2.3 Descriptions of Ripple-Based Control Methods

Three kinds of ripple-based control method of buck converter including hysteretic control, constant on-time control and constant off-time control are introduced in this section.

## 2.3.1 Hysteretic Control Method

The hysteretic controller is shown in Fig. 12 [16], the main control method is generating a hysteresis window. By controlling the upper and lower boundary to regulate the output voltage, when the feedback voltage touch to the hysteretic upper boundary, the power N-type MOSFET will turn on and power P-type MOSFET will turn off to discharge the inductor current and feedback voltage will decrease. At the same time, the hysteretic

window will change to the lower boundary. While the feedback voltage touch to the hysteretic lower boundary, the power P-type MOSFET will turn on and the power N-type MOSFET will turn off to charge the inductor current and feedback voltage will increase. The hysteretic window which is calculating by superposition theorem can be expressed as follows.

$$V_H = V_{uppper} - V_{lower} = (V_{REF}\frac{R_2}{R_1+R_2} + V_{IN}\frac{R_1}{R_1+R_2}) - (V_{REF}\frac{R_2}{R_1+R_2}) = V_{IN}\frac{R_1}{R_1+R_2} \quad (14)$$

The features of hysteretic controller are described as follows; firstly, the main control circuit is comparator and the error amplifier does not be used, so it is no problem about system compensation. Secondly, without using any clock generator, the switching frequency of hysteretic controller is generated by system itself. The following is the calculation of feedback voltage variation, as expressed as follows.

$$I = C\frac{dV}{dt} \Rightarrow \frac{V_{FBAVG}-0}{R} = C\frac{\Delta V_{FB}}{t_{OFF}} \Rightarrow \Delta V_{FB} = \frac{t_{OFF}V_{FBAVG}}{RC} = \frac{DV_{IN}(1-D)T_0}{RC} \quad (15)$$

The voltage $V_{FBAVG}$ is the average voltage of feedback voltage, ideally is $DV_{IN}$, the parameter $D$ is the duty ratio of buck converter. And the hysteresis window variation ($V_H$) equals to feedback voltage variation ($\Delta V_{FB}$). Combining the Eq. (14) and Eq. (15), the switching frequency can as expressed as follows.

$$V_H = \Delta V_{FB} \Rightarrow V_{IN}\frac{R_1}{R_1+R_2} = \frac{DV_{IN}(1-D)T_0}{RC} \Rightarrow f_0 = \frac{1}{T_0} = \frac{1}{RC}D(1-D)(1+\frac{R_2}{R_1}) \quad (16)$$

By controlling the resistor $R$, capacitor $C$ and the ratio of resistors $R_1$ and $R_2$ can define the switching frequency. However, as line and load conditions change, the hysteretic regulator operates over a wide frequency range that depends on the input and output voltages, the output filter inductance, the hysteresis window and ESR of output capacitor. Finally, because the output ripple has been defined, it can't choose the low ESR capacitor to

reduce output ripple.

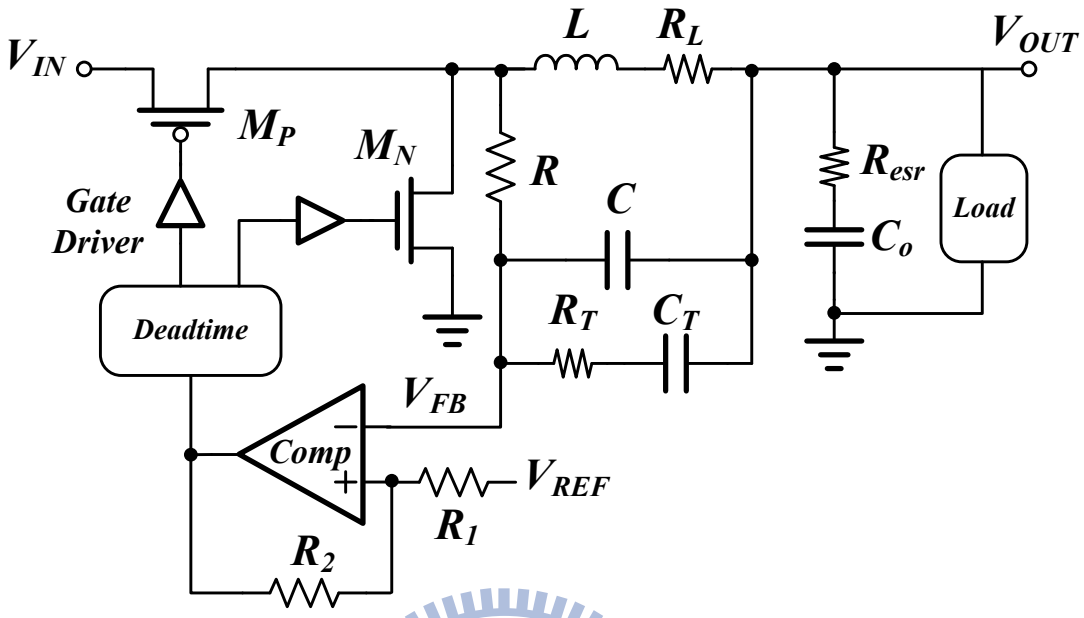



Fig. 12. The block diagram of hysteretic control method.

## 2.3.2 Constant On-time Control Method

As shown in Fig. 13, the basic constant on-time control structure consists of a comparator and one-shot on-time timer, with the output voltage feedback compared with an internal reference. The constant on-time control method is a modification of hysteretic control that operates at a relative constant frequency without an oscillator. It controls the high side power MOSFET switch whose on-time varies inversely with the input supply voltage.

In normal operation, the system initiates an on-time period when the feedback voltage $V_{FB}$ falls below the reference voltage $V_{REF}$, which can be viewed as a valley voltage. The high side power P-type MOSFET stays on for the programmed on-time, causing the feedback voltage to rise above the reference voltage. After the on-time period, the power

P-type MOSFET remains off until the feedback voltage falls below the reference voltage. Besides, the one-shot on-time timer provides a period that is inversely proportional to input supply voltage for constant frequency operation over input supply voltage variation.

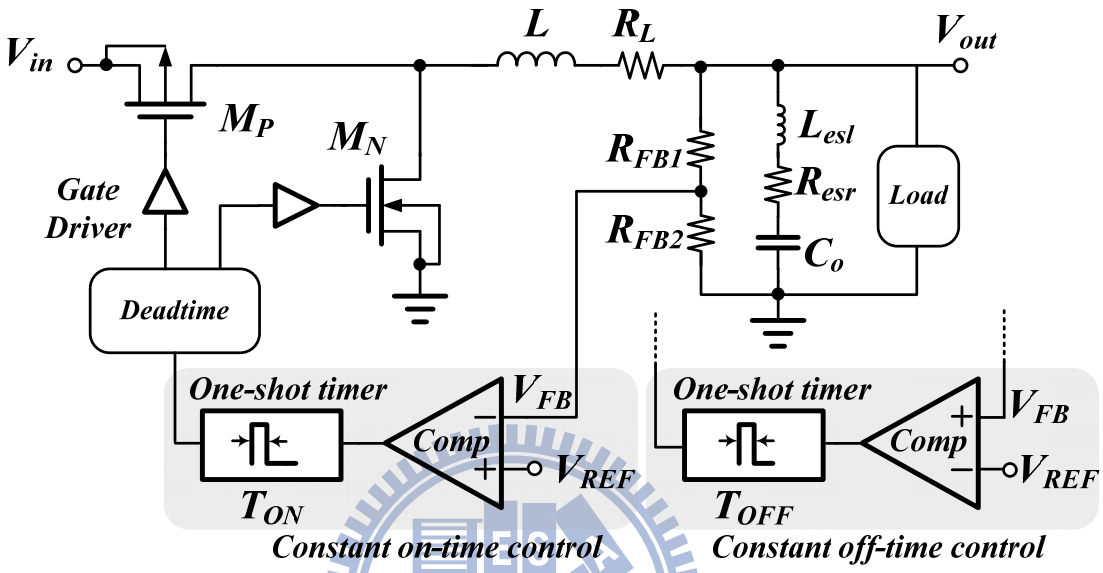



Fig. 13. The block diagram of constant on-time control method.

In continuous conduction mode (CCM) the frequency depends only on duty cycle and on-time period. This is in contrast to hysteretic regulators where the switching frequency is determined by the output inductor and capacitor. In discontinuous conduction mode (DCM), experienced at light loads, the frequency will vary according to the load condition, similar to the operation in PFM mode [17]. This leads to high efficiency and good transient response.

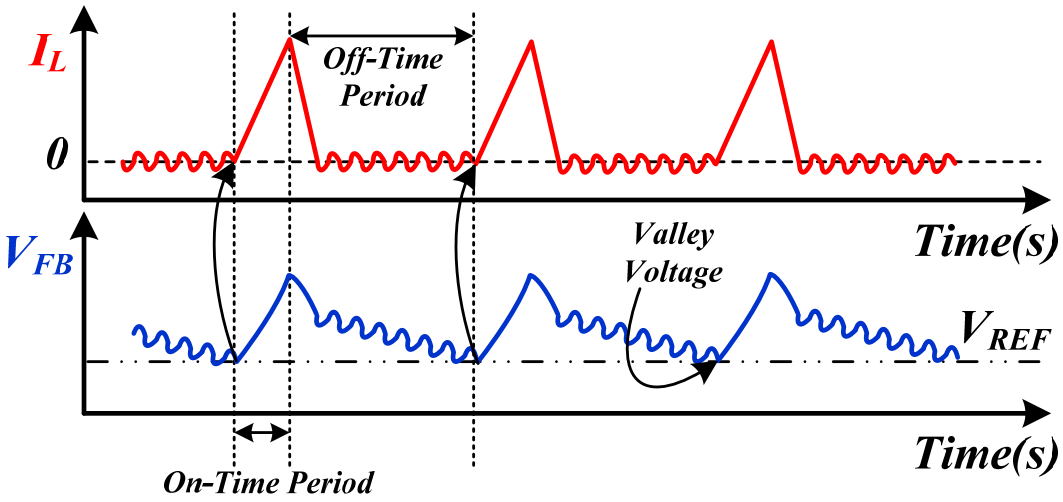



Fig. 14. Inductor current and feedback voltage waveforms in DCM operation of constant on-time control.

Fig. 14 shows the waveforms of constant on-time control in DCM operation, inductor current $I_L$ raises to peak value during the fixed on-time period, and it falls back to zero before feedback voltage $V_{FB}$ reaches valley voltage $V_{REF}$ for constant on-time control. When $V_{FB}$ reaches $V_{REF}$, the next on-time period is introduced. Therefore, the off-time period of constant on-time control is dependent on load current condition in DCM operation.

### 2.3.3 Constant Off-time Control Method

The approach of constant off-time control is similar to constant on-time control. In normal operation, the system initiates an off-time period when the feedback voltage $V_{FB}$ rises above the reference voltage $V_{REF}$, which can be viewed as a peak voltage. However, constant on-time control is more popular than constant off-time control in application of

power management system. The reason is that the switching frequency in DCM operation of constant off-time control is inversely proportional to the load current.

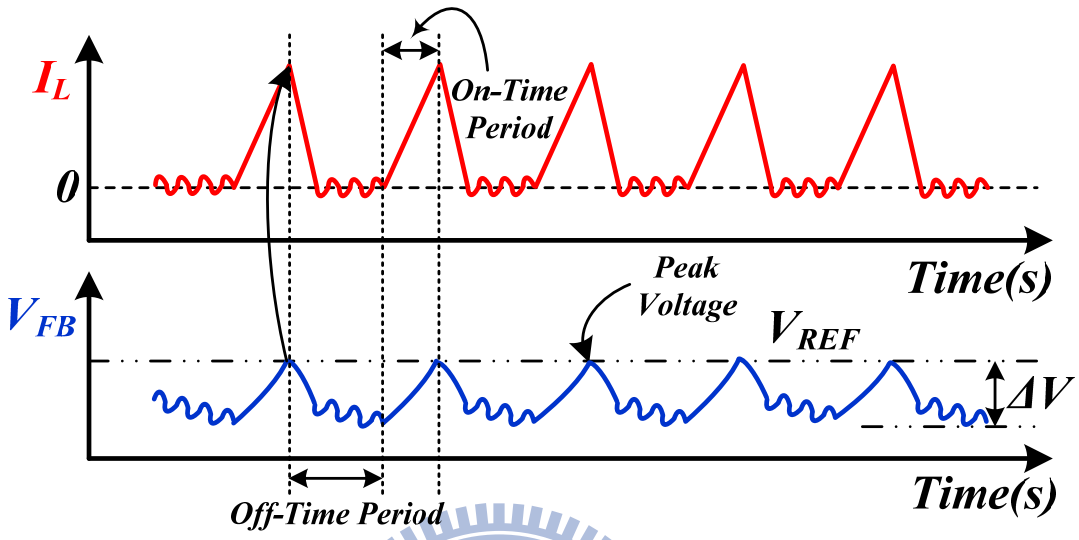



Fig. 15. Inductor current and feedback voltage waveforms in DCM operation of constant off-time control.

As shown in Fig. 15, the off-time period of constant off-time control is fixed, which is independent of load current condition. However, the voltage difference $\Delta V$ is proportional to output current. As the $\Delta V$ becomes larger, the $V_{FB}$ needs to extend on-time period to reach $V_{REF}$ to cause the decrease of the switching frequency. The switching frequency increases as output current decreases in the DCM. It deteriorates the system efficiency. Thus, constant on-time control is widely used in practice [18].

# Chapter 3

# Topology of Constant On-time Control DC-DC Buck Converter without ESR Compensation

In this chapter, the system stability analysis and operation of proposed constant on-time control DC-DC buck converter are presented. The system stability analysis of conventional constant on-time control converter is shown in section 3.1. In section 3.2, the system operation is introduced.

## 3.1 System Stability Analysis of Conventional Constant On-time Control

The basic concept of constant on-time control is introduced in chapter 2. Besides, constant on-time control is more popular than constant off-time control owing to the conversion efficiency at light loads. In this section, we will analyze the system stability of constant on-time control in time-domain and frequency-domain, respectively.

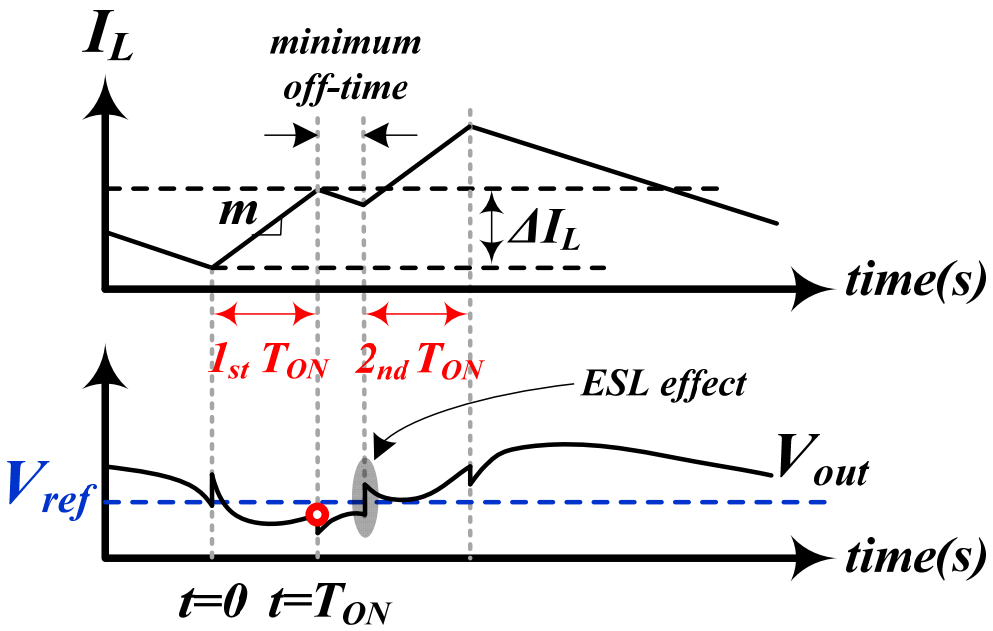



Fig. 16. Small ESR caused double-pulse problem.

In conventional constant on-time control with small ESR value on the output capacitor, the converter is easily affected by the noise due to small output ripple, which is dominated by the ripple on the output capacitor. Besides, the loop phase delay may further decrease the system stability owing to the double-pulse problem. As illustrated in Fig. 16, the delayed output voltage, $V_{out}$, is unable to reach the reference voltage, $V_{ref}$, even after the first constant on-time period. Consequently, the second constant on-time is inserted after the minimum off-time period to raise $V_{out}$ higher than $V_{ref}$. The constant on-time control can't regulate the output voltage within one switching cycle and thus induces the double-pulse problem. That is, the system needs two or more switching periods to regulate the output voltage. The output voltage ripple is increased to ensure the system stability due to the decreased switching frequency.

In Fig. 16, the slope of the inductor current is $m$, which is expressed in Eq. (17), during the on-time period.

$$m = \frac{dI_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{17}$$

The value of $V_{out}$ for time=$t$ can be calculated as shown in Eq. (18). $R_{esr}$ is the ESR on output capacitor, $C_O$. $L_{esl}$ is the ESL on the output capacitor. $\Delta I_L$ is the inductor current variation during one on-time period.

$$V_{out}(t) = V_{ref} + R_{esr} mt + \frac{1}{C_O}\int(-\Delta I_L + mt)dt + L_{esl}\frac{dI_L}{dt} \tag{18}$$

The output ripple is composed of three components including ESR part, capacitor part and ESL part. In Eq. (18), the second term indicates the contribution of the ESR while the third term represents the ripple on the output capacitor. The last term indicates the contribution of the ESL. To ensure the system can be regulated for each switching cycle. At $t=T_{ON}$, the value of $V_{out}(T_{ON})$ needs to be larger than $V_{ref}$ as shown in Eq. (19).

$$V_{out}(T_{ON}) - V_{ref} = R_{esr} mT_{ON} - \frac{mT_{ON}^2}{C_O} + \frac{mT_{ON}^2}{2C_O} + L_{esl} m > 0 \tag{19}$$

The arrangement of Eq. (19) can be expressed in Eq. (20).

$$R_{esr} C_O + \frac{L_{esl} C_O}{T_{ON}} > \frac{T_{ON}}{2} \tag{20}$$

Generally speaking, as the ESL of output capacitor is not sufficient large, the criterion of system stability is decided by the time constant, $R_{esr}C_O$, and it can be derived in Eq. (21).

$$R_{esr} C_O > \frac{T_{ON}}{2} \tag{21}$$

That is, the time constant, $R_{esr}C_O$, must be larger than half of on-time period to ensure

the system stability. Consequently, the ripple contributed by the ESR dominates the whole output ripple to guarantee the system stability. Therefore, a large ESR is utilized in the conventional constant on-time control at the sacrifice of large output ripple. However, for certain applications of output capacitor combination, as the total ESL of the output capacitor becomes larger, the double-pulse problem will appear as shown in Fig. 17. At the beginning of the minimum off-time, the voltage across ESL will step down since the negative slope of inductor current. If the voltage spike on the ESL is larger enough to let the output voltage smaller than $V_{ref}$, the second constant on-time period will appear. Large ESL will cause the system unstable due to large step voltage on ESL.

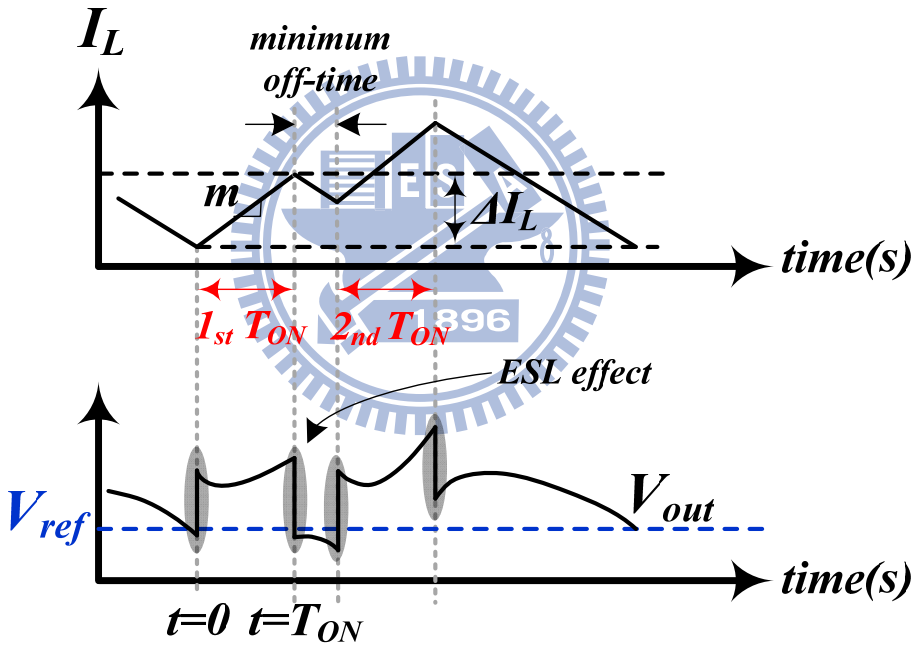



Fig. 17. Large ESL caused double-pulse problem.

Considering the noise causes the variation of reference voltage as shown in Fig. 18, the rising edge of the power MOSFET switching signal is perturbed to induce a large jitter. The time deviation of $t_n$ indicates the jitter caused by the noise. Unfortunately, the switching frequency can't be kept constant and thus the system suffers from the electromagnetic interference (EMI) problem. The performance of system is seriously deteriorated. Thus,

small jitter and constant switching frequency are also demanded in the constant on-time control.

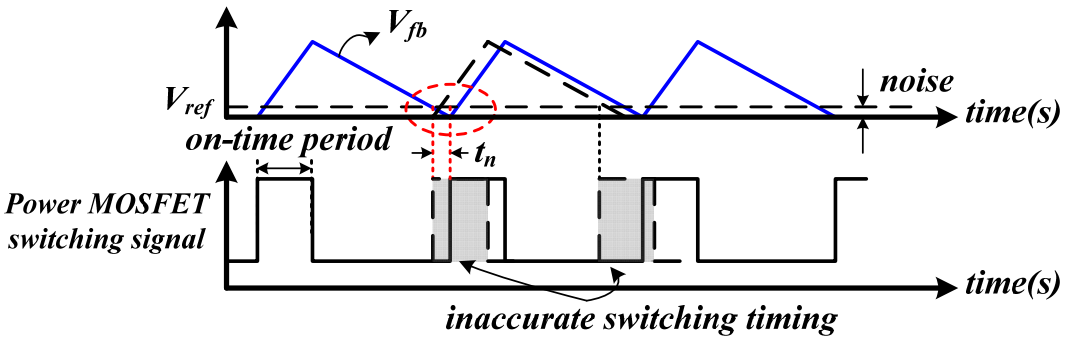



Fig. 18. The noise effect on feedback voltage and power MOSFET switching signal.

Fig. 19 shows the enlarged waveform of $V_{fb}$ with a negative slope of $a$ when the inductor current decreases. If the slope becomes more sharp and has a value of $a'$, the new waveform of $V_{fb}'$ decides another switching period. Once the noise perturbs the reference voltage from $V_{ref}$ to $V_{ref}'$, the variation of switching period can be decreased from $t_1$ to $t_0$ due to the sharp slope. Basically, the slope can be expressed as Eq. (22), which is proportional to the value ESR. Eq. (22) is under the assumption of neglecting the voltage across ESL and capacitor. In other words, the ESR value can determine the system stability in the constant on-time control. Thus, the conventional design uses a large ESR value to suppress the jitter problem. A lower jitter effect can be derived by a larger ESR value. But, a large ESR value will cause the increase of output ripple and transient dip voltage.

$$slope = \frac{-R_{esr} \times V_{out}}{L} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \propto \frac{R_{esr}}{L} \tag{22}$$

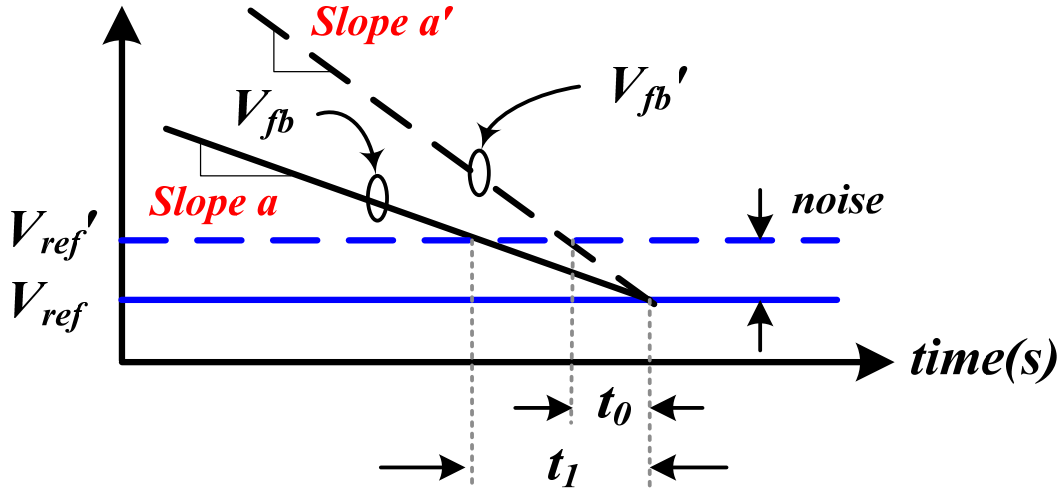



Fig. 19. Enlarged waveform of feedback voltage and reference voltage that affected by noise.

A large ESR is usually selected to avoid the double-pulse problem. In other words, the ripple content at the output voltage should have a minimum value to maintain the system noise margin. The larger ESR value causes the larger output voltage ripple. For the purpose of solving the dependence of ESR value, the proposed constant on-time control DC-DC converter provides sufficient noise margin without using large ESR capacitor so that the low jittery behavior can be attained to eliminate the double-pulse problem.

## 3.2 Topology of the Proposed System

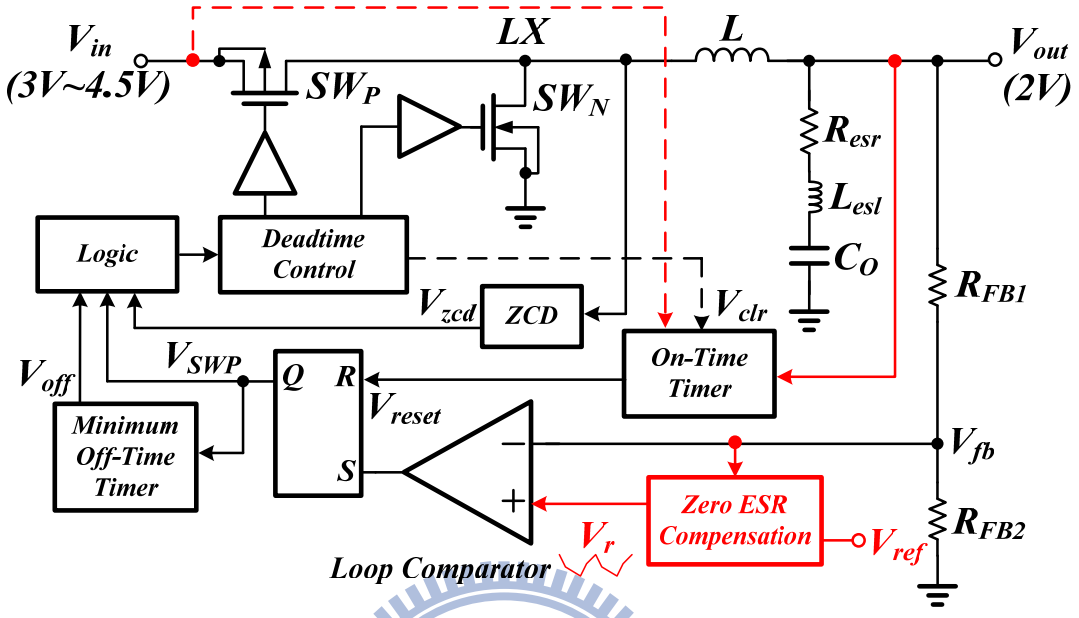



Fig. 20. Topology of proposed constant on-time control DC-DC buck converter.

Fig. 20 shows the proposed constant on-time control DC-DC converter without ESR compensation. The $V_{out}$ is regulated by the loop comparator through the voltage divider, $R_{FB1}$ and $R_{FB2}$. The $V_r$ from the zero ESR compensation circuit and the feedback voltage $V_{fb}$ are compared by the loop comparator. The output of loop comparator is used to decide the timing to store energy in the inductor. The minimum off-time signal $V_{off}$ is used to provide a minimum off-time period to ensure a minimum off-time during startup interval and extreme duty condition. Besides, the zero current detector signal, $V_{zcd}$, is used to avoid the reverse inductor current. The deadtime control circuit is used to avoid the short-through current.

The output stage of converter can be viewed as an integrator. As a result, the output voltage ripple can be recognized as an integration of the inductor current ripple. Therefore, the inductor current information can be derived by differentiating the output voltage. As shown in Fig. 21, the proposed zero ESR compensation technique generates a differential

signal $V_s$ to get the inductor current information. $V_s$ can be viewed as a ramp signal, providing good noise immunity for system operation [19]. However, the ESL, $L_{esl}$, on output capacitor $C_O$ will distort the differential signal of the conventional differentiator. The output voltage $V_{out}$ contains high frequency component caused by $L_{esl}$. It will deteriorate the system stability due to the double-pulse problem. Afterwards, the $V_s$ goes through the reflector, which produces the reflective signal $V_r$. Once the inductor current rises up, $V_r$ starts to fall. Fortunately, the $V_r$ can generate a sufficient noise margin at the input node of loop comparator.

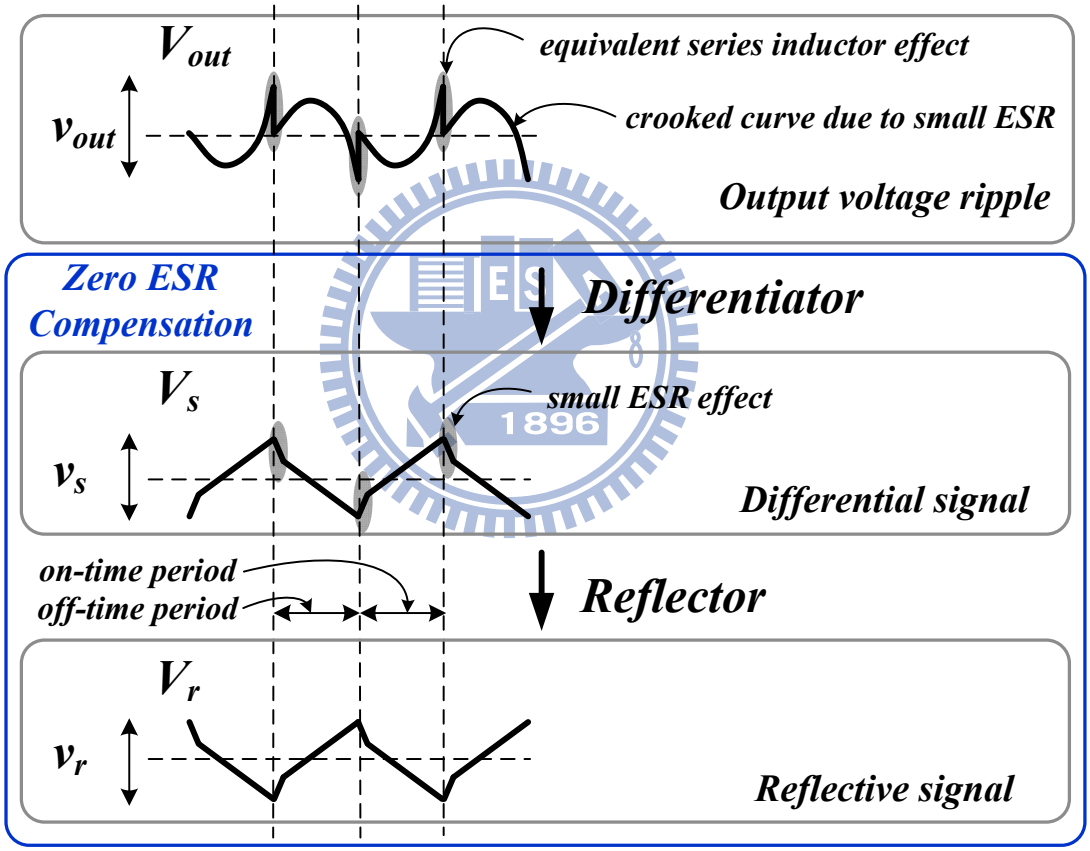



Fig. 21. The concept of the proposed technique.

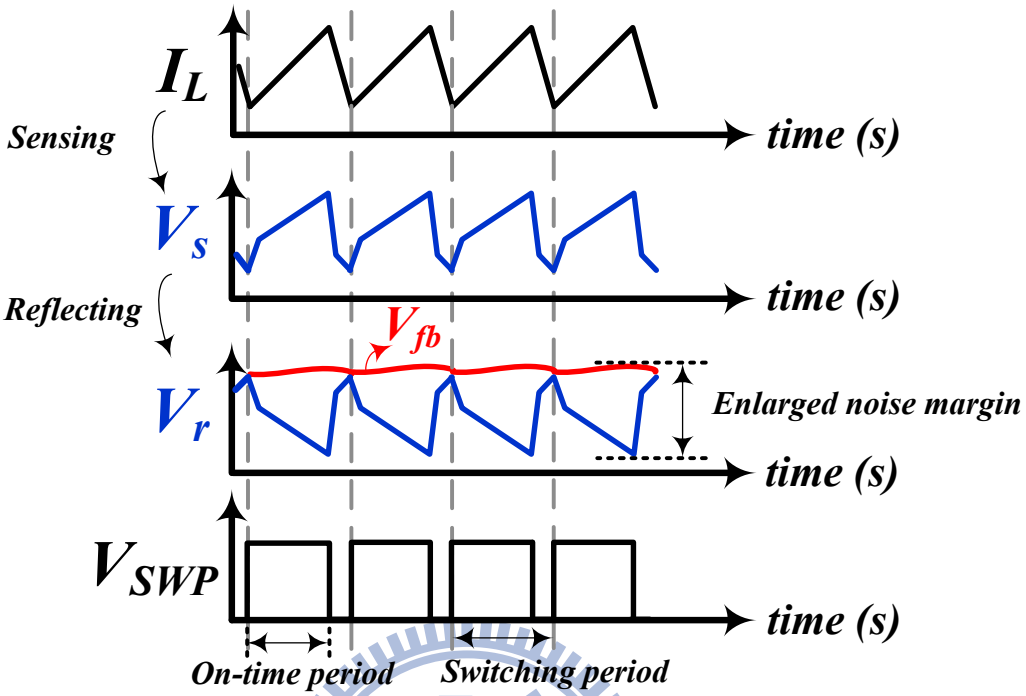



Fig. 22. The operational scheme of the proposed technique.

At the beginning of the inductor charging period, the control signal $V_{clr}$ clears the on-time timer in order to recount on-time period. As on-time period ends up, the signal $V_{reset}$ goes from low to logic high. The high-side power MOSFET $SW_P$ turns off to start the inductor discharging period to release the stored energy. When the $V_r$ rises above the $V_{fb}$, the high-side power MOSFET $SW_P$ turns on and the on-time timer is cleared, again, to restart the inductor charging period as shown in Fig. 22. The $V_{fb}$ is compared with the $V_r$, which represents the opposite shape of the differential signal $V_s$. The ripple of $V_{fb}$ is much smaller than $V_r$. That is, $V_r$ can be regard as the feedback voltage in the original constant on-time control and the $V_{fb}$ can be regard as the reference voltage. In other words, the $V_{fb}$ can be viewed as the peak voltage of the $V_r$. When the $V_r$ starts to decline from the level of $V_{fb}$, the slope of $V_r$ is sufficient steep and thus it can provide good noise immunity. That is, a sufficient noise margin is proposed to avoid the double-pulse problem.

# Chapter 4

# Circuit Implementation

In this chapter, the sub-circuits of the proposed constant on-time control DC-DC buck converter are introduced. In section 4.1, zero ESR compensation circuit is presented. It consists of differential circuit part and reflection circuit part. In section 4.2, the on-time timer is presented. It generates one on-time pulse each switching cycle to control switches.

## 4.1 Zero ESR Compensation Circuit

The proposed zero ESR compensation circuit is depicted in Fig. 23. The differentiator is composed of $M_1$-$M_9$, $C_1$-$C_2$, and $OP_1$. Differentiating feedback voltage $V_{fb}$ through the capacitor $C_1$, the inductor current can be derived. $V_d$ is composed of ESR and inductor current ripple information. However, $V_d$ has unwilling distortion due to equivalent series inductor effect of output capacitor. The expressions of $V_{fb}$ and $V_d$ are shown in Eq. (23) and Eq. (24), respectively.

$$V_{fb} = k\left( R_{esr} i_L + \frac{1}{C_O}\int i_L dt + L_{esl}\frac{di_L}{dt} \right) \tag{23}$$

$$V_d = V_{fb}' = \tau k\left( R_{esr}\frac{V_{in}-V_{out}}{L} + \frac{i_L}{C_O} + L_{esl}\frac{d^2 i_L}{dt^2} \right) \tag{24}$$

$k$ is the feedback ratio and $\tau$ is a constant generated in the procedure of differentiation. The unwilling ESL effect caused by $L_{esl}$ is a high frequency component, which will result in a surge on the differential voltage $V_d$. To avoid this problem, a capacitor $C_2$ is introduced at

the gates of transistors $M_6$ and $M_7$. Therefore, the current $I_L$ flowing into $M_7$ is filtered by $C_2$. That is, the high frequency component of $V_d$ has been eliminated. Then, the equivalent series inductor effect can be reduced. After that, the current $I_H$ flowing into $M_8$ is mirrored to $M_9$, and $I_H$ is the deduction of $I_{HL}$ about $I_L$. That is, $I_H$ contains high frequency component of $V_d$. The low frequency component current $I_L$ can be obtained by deducting $I_H$ from $I_{HL}$. The voltage $V_s$ would therefore contain low frequency component only, eliminating the equivalent series inductor effect of output capacitor. The expression of $V_s$ is shown in Eq. (25).

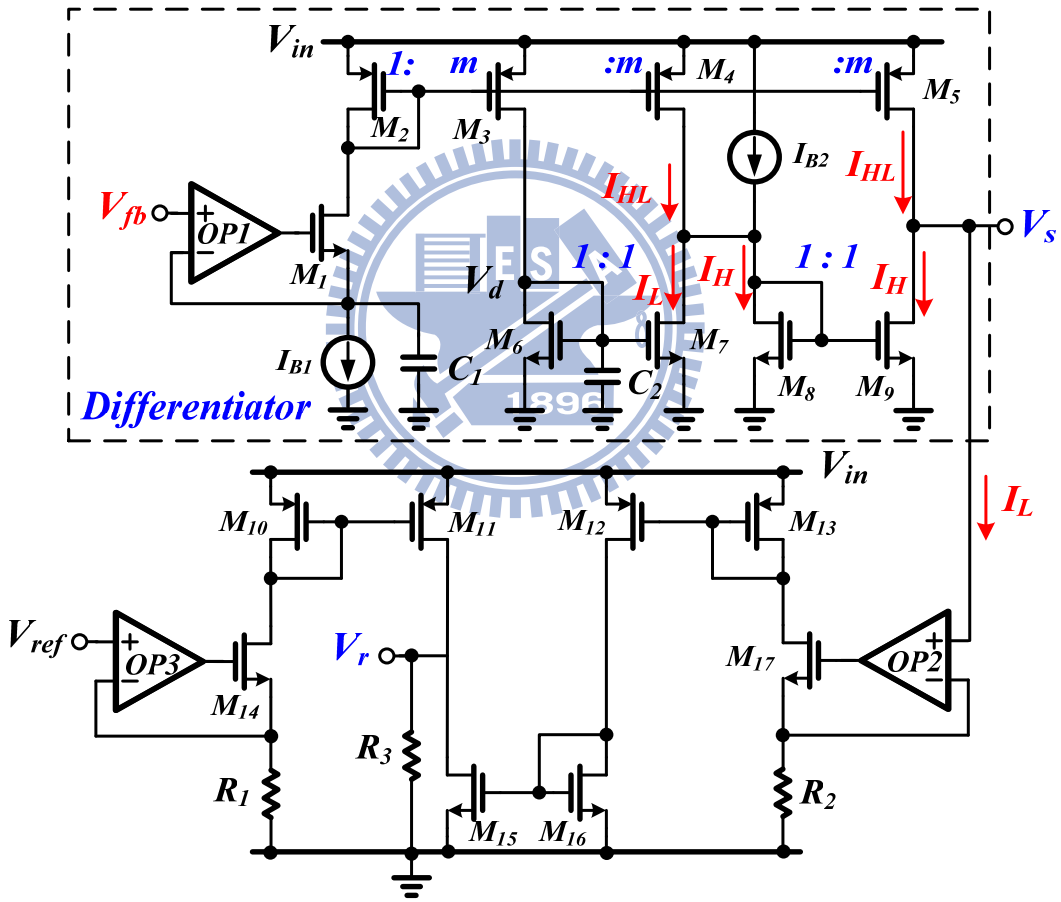



Fig. 23. The proposed zero ESR compensation circuit.

$$V_s = \tau k\left( R_{esr}\frac{V_{in}-V_{out}}{L} + \frac{i_L}{C_O} \right) \tag{25}$$

The shape of the $V_r$ is the reflection of the $V_s$. $M_{14}$, $M_{17}$, the resistors $R_1$ and $R_2$, and the

operational amplifiers $OP_2$ and $OP_3$, constitute the voltage-to-current converter. $R_1$, $R_2$ and $R_3$ are the conversion factors of the voltage-to-current converter. The $V_{ref}$ decides the DC level of the $V_r$, which affects the DC level of the $V_{out}$. The expression of $V_r$ is shown in Eq. (26).

$$V_r = \left(\frac{V_{ref}}{R_1} - \frac{V_s}{R_2}\right)R_3 \tag{26}$$

## 4.2 On-Time Timer

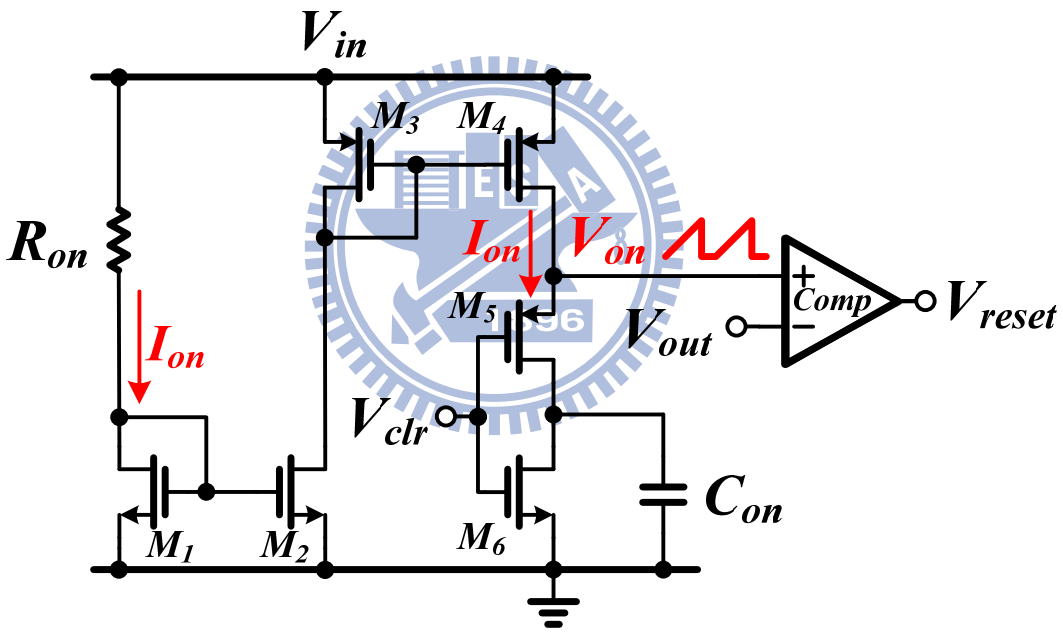



Fig. 24. The on-time timer.

Fig. 24 shows the on-time timer circuit. The transistors $M_1$-$M_4$ and the resistor $R_{on}$ generate a current $I_{on}$ to charge the capacitor $C_{on}$. Variable current $I_{on}$ depends on the $V_{in}$. $I_{on}$ is given by Eq. (27).

$$I_{on} = \frac{V_{in} - V_{GS1}}{R_{on}} \tag{27}$$

The transistors $M_5$-$M_6$ and $V_{clr}$ are used to decide the on-time capacitor, $C_{on}$, to be charged or discharged. At the beginning of first switching period, $V_{clr}$ is high and $C_{on}$ is charged by $I_{on}$. Then, $V_{on}$ is raised. As the $V_{on}$ reaches the $V_{out}$, the $V_{reset}$ becomes high to decide the on time period. As a result, the time $T_{on}$ required to reach $V_{out}$ is inversely proportional to the $V_{in}$ and proportional to the $V_{out}$. $T_{on}$ is expressed in Eq. (28).

$$T_{on} = \frac{C_{on}V_{out}}{I_{on}} = \frac{C_{on}V_{out}R_{on}}{V_{in} - V_{GS1}} \tag{28}$$

The switching frequency is relatively constant as the duty ratio $D$ as expressed in Eq. (29).

$$D = \frac{V_{out}}{V_{in}} \tag{29}$$

# 4.3 Control Logic Circuit and Flow Chart

Fig. 25 shows the detailed control logic circuit of the proposed constant on-time control DC-DC converter. The circuit consists of one inverter, two AND gates, two OR gates and two SR-latch. The purpose of the control logic circuit is producing the pulse width modulation (PWM) switching signal $V_{SWP}$ and $V_{SWN}$ to control power MOSFET $SW_P$ and $SW_N$. $V_{off}$ and $V_{zcd}$ are the minimum off-time timer signal and zero current detector signal, respectively. $V_{off}$, when the minimum off-time period gets through, it will go from logic low to logic high. $V_{zcd}$, goes from logic low to logic high as the reverse inductor current appears, and is used to turn off the power MOSFET $SW_N$. $V_{fb}$ and $V_r$, as mentioned before, are

feedback voltage and reflective voltage of differential signal $V_s$. $V_{reset}$, produced by on-time timer, resets the SR-latch in order to turn off the power MOSFET $SW_P$.

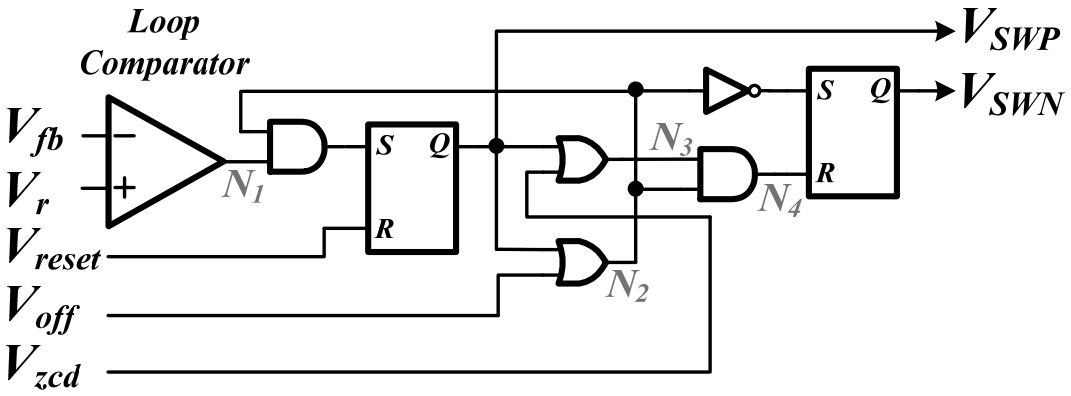



Fig. 25. The control logic circuit.

Fig. 26 shows the flow chart of control logic circuit, it can be divided into two parts, on-time period and off-time period. The logic level of inner nodes in the control logic circuit is shown in the flow chart, which interprets the operational procedure of proposed converter.

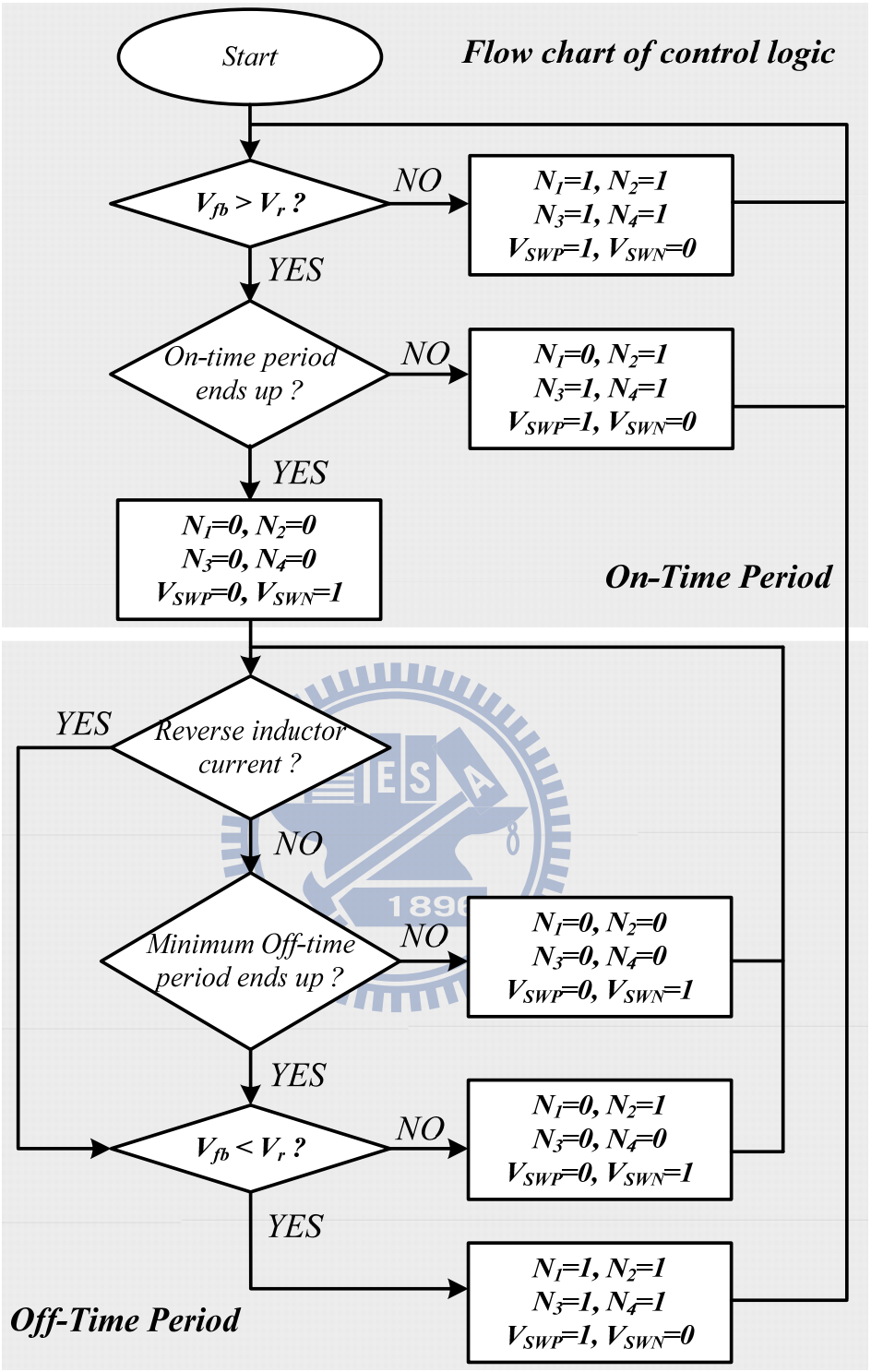



Fig. 26. Flow chart of control logic circuit.

# Chapter 5

# System of Reduction of Equivalent Series Inductor Effect in Constant On-Time Control DC-DC Converter without ESR Compensation Simulation Results, Conclusions and Future Work

In this chapter, the simulation results are shown in section 5.1. The conclusions are made in section 5.2. Finally, the future work is shown in section 5.3.

## 5.1 Simulation Results

The circuit was fabricated in TSMC 0.25μm CMOS process. The chip layout is shown in Fig. 27 The filter components contain $L$=4.7μH, $C_O$=4.7μF, $R_{esr}$=0mΩ and $L_{esl}$=2nH. The input voltage ranges from 3V to 4.5V and output voltage is 2V. The switching frequency is designed as 1MHz.

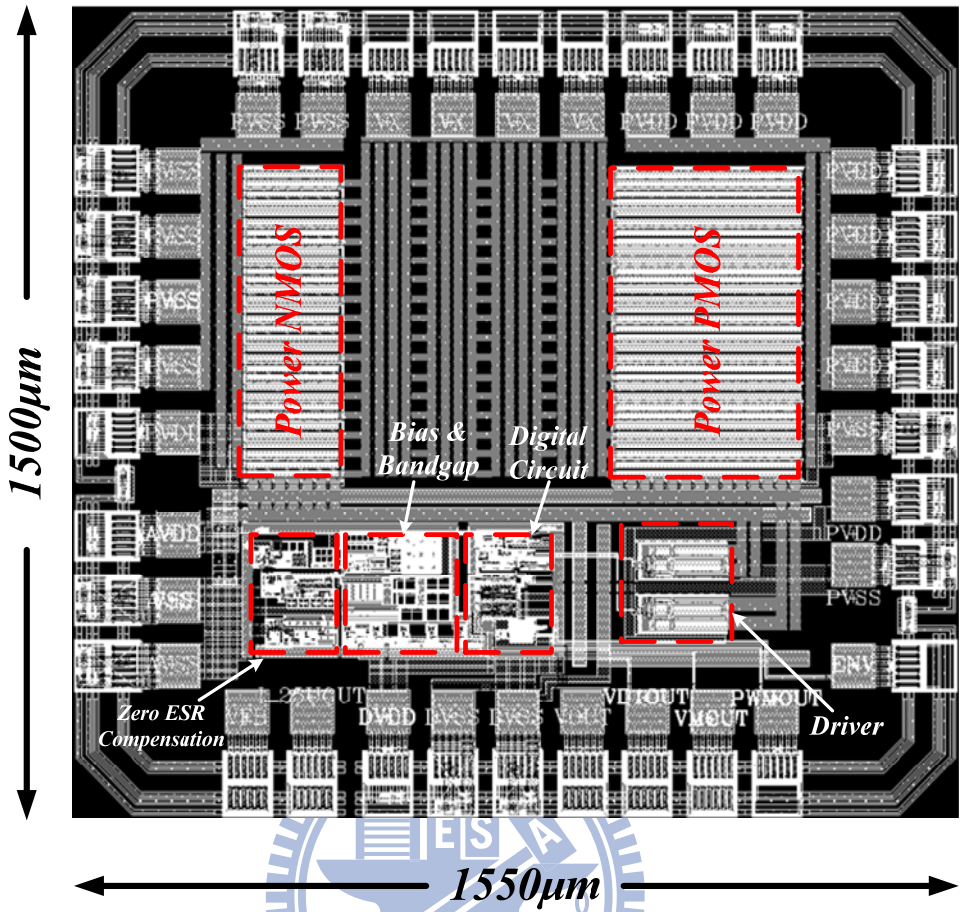
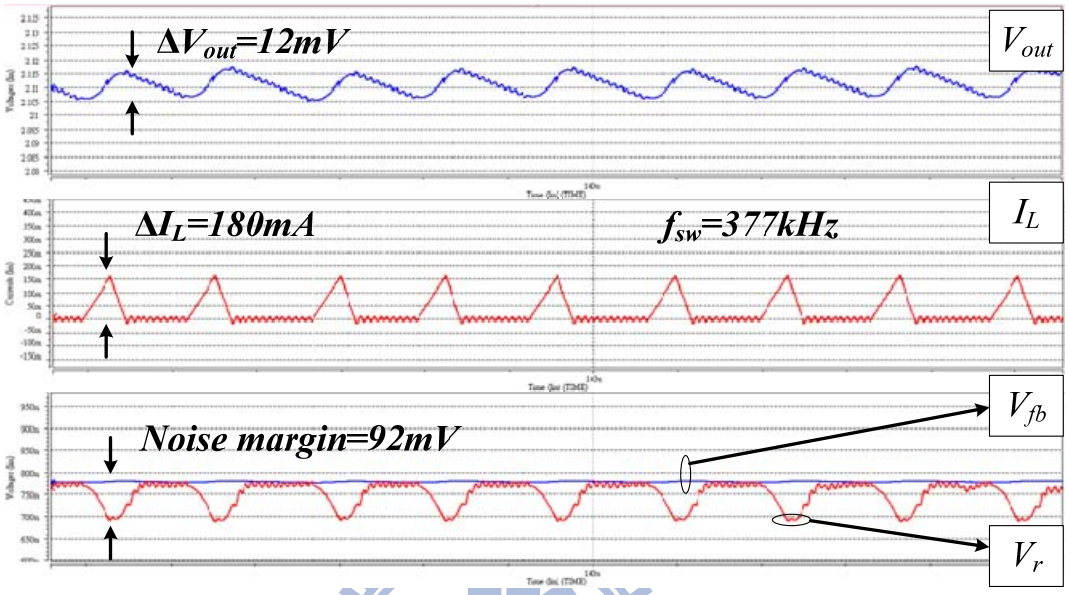


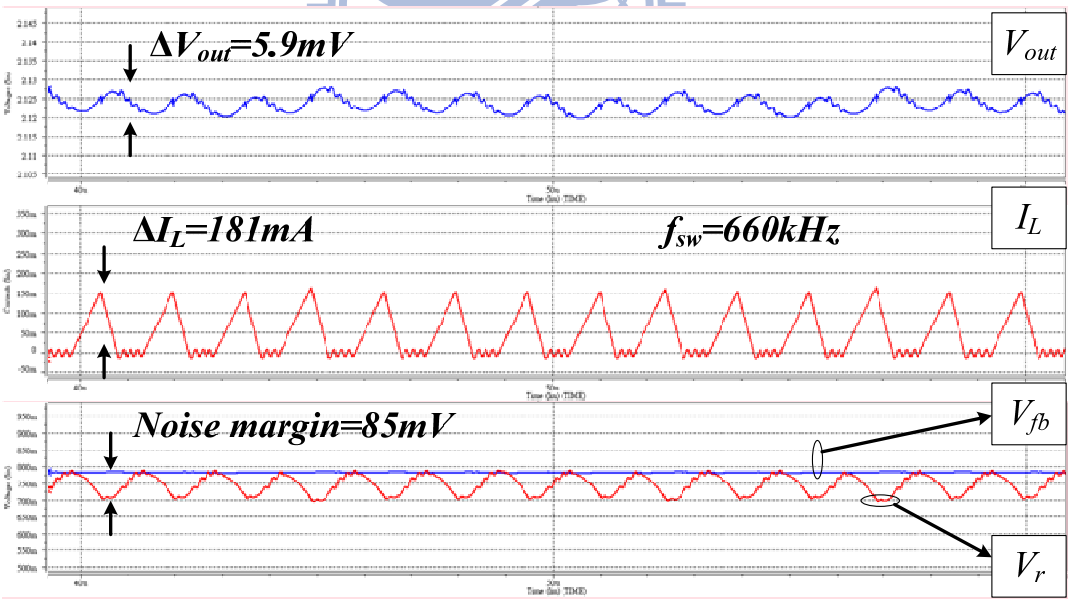

Fig. 27. Chip layout.

Fig. 28 shows the output waveforms at different load current condition when the converter operates in the CCM and DCM. Fig. 28(a) and (b) show that the proposed zero ESR compensation technique adjusts the switching frequency of the buck converter dynamically according to the load current condition. When the load current is about 30mA, the switching frequency is about 377kHz. As the load current increases to 50mA, the switching frequency increases to 660kHz. On the other words, when the converter operates in the DCM, the switching frequency is proportional to the load current condition. Besides, the noise margin between $V_{fb}$ and $V_r$ is not less than 80mV. Fig. 28(c) shows the converter correctly operates in the CCM without the double-pulse problem when 2nH of ESL and no ESR exist at output capacitor. The output voltage ripple is about 2.6mV due to small ESR.

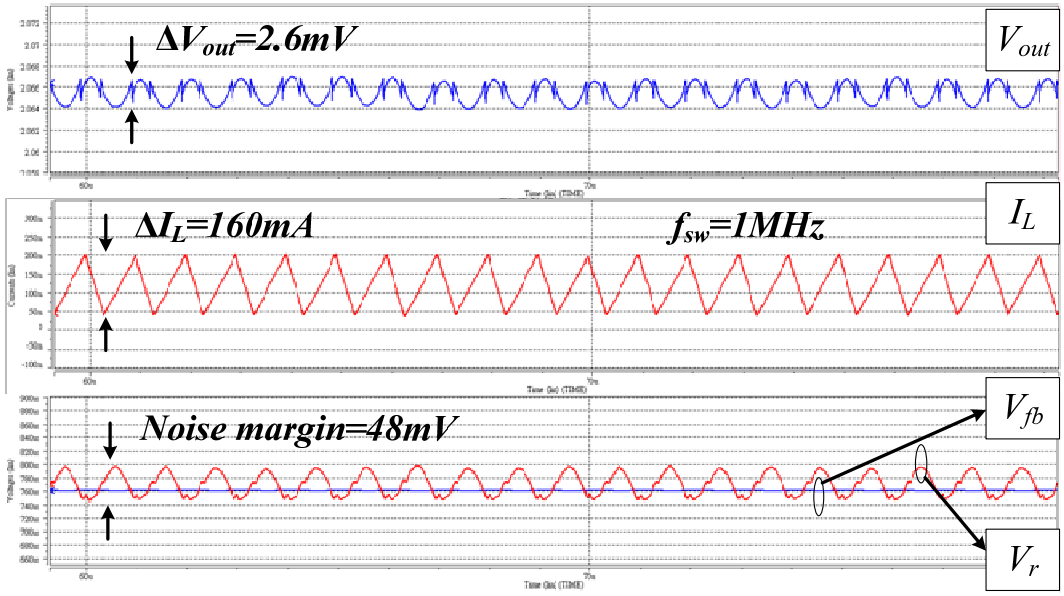
Furthermore, the switching frequency reduces for power saving when the load current decrease in the DCM.




(a)



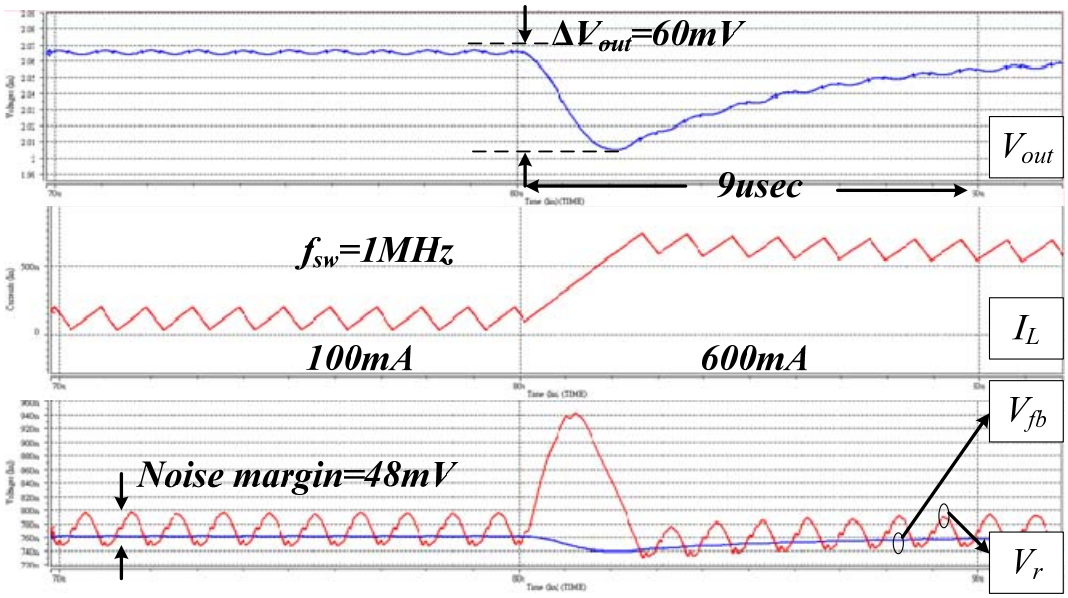

(b)



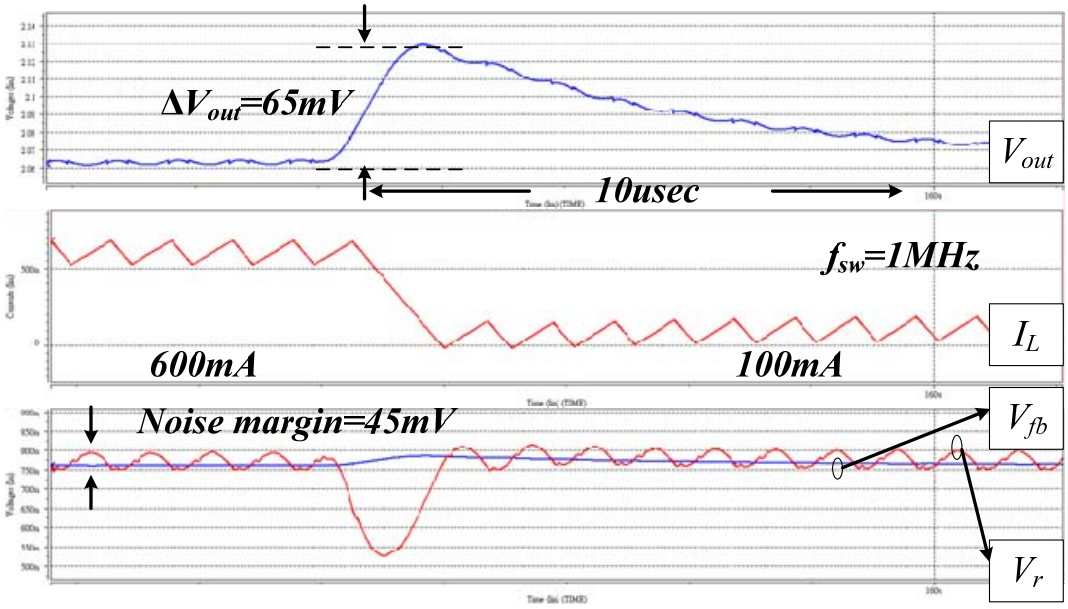

(c)

Fig. 28. Waveforms of the output voltage and inductor current at different load current condition. (a) $I_{load}$ =30mA (b) $I_{load}$ =50mA (c) $I_{load}$ =100mA.

As shown in Fig. 29, simulation results of the output voltage and the inductor current demonstrate the CCM operation during load transient response. The recovery times are about 9μs and 10μs when the load current changes from 100mA to 600mA and vice versa, respectively, if $V_{in}$ = 3.3V. The zero compensation circuit provides good noise margin for constant on-time control system to operate correctly with no ESR exist at output capacitor. Besides, constant on-time control can achieve fast transient response since the system is not need frequency compensation. The specifications are listed in Table II.




(a)




(b)

Fig. 29. Transient response (a) when load current changes from 100mA to 600mA and (b) from 600mA to 100mA.

TABLE II. DESIGN SPECIFICATIONS.

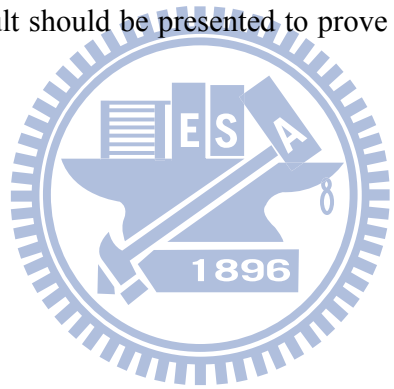
| PARAMETER | VALUE | UNIT |
|---|---|---|
| Supply variation ($V_{in}$) | 3 - 4.5 | V |
| Output voltage ($V_{out}$) | 2 | V |
| Switching frequency | 1 | MHz |
| Undershoot voltage recovery time @ $I_{OUT}$ changes from 100mA to 600mA | 9 | μs |
| Overshoot voltage recovery time @ $I_{OUT}$ changes from 600mA to 100mA | 10 | μs |
| Maximum load current | 800mA | mA |
| Inductor ($L$) | 4.7 | μH |
| Output capacitor ($C_o$) | 4.7 | μF |
| ESR on output capacitor ($R_{esr}$) | 0 | Ω |
| ESL on output capacitor ($L_{esl}$) | 2 | nH |

## 5.2 Conclusions

A reduction of equivalent series inductor effect in constant on-time control DC-DC converter without using ESR compensation is proposed to eliminate equivalent series inductor effect of output capacitor and remove the dependency of output ripple induced by ESR. Besides, the noise margin at the comparator input node has been increased. Furthermore, although the ramp compensation is applied at feedback point, the system still presents a good transient response. The system can operate correctly even that no ESR exists at output capacitor both in CCM and DCM.

## 5.3 Future Work

The proposed zero ESR compensation technique not only removes the need of conventional ESR compensation but also aims to eliminate ESL effect of the output capacitor. Besides, fast transient response and small dip voltage variation can be achieved. The noise margin at the loop comparator input nodes can also be extended. Therefore, the SNR of the constant on-time control system is increased. However, the phase delay caused by zero ESR compensation circuit will reduce the noise margin and deteriorate the transient response. In addition, the output voltage DC level is not accurately defined. On the other words, the output voltage accuracy will be affected by parasitic component, such as ESR and ESL. Finally, the experimental result should be presented to prove simulation result of whole system is matching.



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