國 立 交 通 大 學

電 控 工 程 研 究 所

碩 士 論 文

具雙調變機制且寬負載範圍之高效率高頻切換

直流-直流降壓式電源轉換器

Dual Modulation Technique for High Efficiency in High-switching

Buck Converters Over a Wide Load Range

研 究 生：黃 琮 瑛

指導教授：陳 科 宏 博士

中 華 民 國 九 十 九 年 十 月

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研 究 生：黃琮瑛　　Student：Tsung-Ying Huang

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摘　　要

在現今可攜式電子產品的應用上，高效能和小型的電壓轉換器在提供系統電源上扮演非常重要的角色。為了減少輸出級濾波器的面積，提出高頻切換的直流轉直流降壓轉換器來達到元件整合的功能。

然而，對傳統的電流控制模式之直流轉直流降壓式電源轉換器來說並不適合在高切換頻率下操作，因為系統的電源轉換效率在輕載時會急遽下降以及控制器電路中所使用到的運算放大器會限制電源轉換器整體系統的頻寬。換言之，轉換器在輕載時系統轉換效率的降低不適合商業上的應用與電路頻寬的限制造成在高切換頻率下的不正確操作。為了解決以上提到的問題，雙調變機制在本論文中被提出。

由於雙調變機制的使用，主調節器中的交流漣波偵測器不僅讓電壓轉換器在高切換頻率下能夠正常操作而且能加速系統的暫態響應，而由次調節器製造的跳頻切換脈波能做到減少功率開關元件的切換次數以達到提高系統在輕載時的轉換效率。

本論文中，實現一個雙調變控制機制用來改善電源轉換效率伴隨著輸出電壓漣波小幅的提高；所提出的交流漣波偵測器可以減輕輸出電容上的寄生電阻與寄生電感在高速切換下所產生的切換雜訊。此外，雙調變機制能夠在系統暫態響應時做到加快系統反應時間；且當系統操作在極輕載時，系統操作頻率能維持在一高於音頻之最小值，避免系統產生噪音。實驗結果顯示電源轉換器使用 1μH 的電感操作在 5MHz 的切換頻率，輸出電壓為 1.8 伏特。負載電流在 150 毫安培與 450 毫安培間瞬間變換時的反應時間小於 3μS；且電源轉換效率在寬負載範圍下可以維持在百分之八十五以上。相較於傳統控制方式，輕載時的轉換效率最高可以改善百分之四十五。

Dual Modulation Technique for High Efficiency in High-switching Buck Converters Over a Wide Load Range

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ABSTRACT

For today's portable electronic device applications, high performance and compact size voltage regulator plays an important role to provide system power. To reduce the size of output filter, a high switching dc-dc buck converter is presented to achieve high integration.

However, the conventional current mode DC-DC buck converter is not suitable for high switching operation, because the system conversion efficiency deceases drastically at light load condition and the operational amplifiers of control circuits restrict system's bandwidth. That is to say, the drop of the efficiency at light load makes the converter not suitable for commercial application and the limitation of circuit bandwidth causes incorrect operation at a high switching frequency. To solve these issues mentioned above, the dual modulation technique is presented in this thesis.

Owing the dual modulation technique, the AC ripple detector in primary modulator not only makes converter operate at a high switching frequency correctly but also speeds up the transient response, and the hopping switching pulse produced by secondary modulator reduces switching times of power switches to raise efficiency at the light load condition.

In this thesis, a dual modulation technique to improve power conversion efficiency with minimal increase in output voltage ripple is presented. The worsening switching noise caused by parasitic resistance and inductance due to high-switching operation can also be alleviated by the proposed AC ripple detector. Furthermore, the dual modulation method can speed up the load transient response since the switching frequency can increase to 10 MHz during the transient period. At very light loads, the switching frequency is always kept higher than the acoustic frequency to avoid noisy sound. Experiment results show that the converter operates at 5MHz using a small inductor of 1μH. The load transient response time is shorter than 3μs when load current changes from 150 to 450mA or vice versa. Power efficiency is kept higher than 85% over a wide load current range. Specifically, light efficiency can be raised to about 45% above that of the conventional design.

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國立交通大學

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Chapter 1
Introduction

Nowadays, portable devices are popularly used such as cell phones, digital cameras and MP3 players, etc. The more functions in one product, the more competitive in marketing. However, the multi-function in portable devices makes the demand on supply energy increase greatly. That is to say, extending the battery life has become an important issue determined by the power management module. Thus, minimizing power loss and effective energy usage on power management ICs are two major topics to achieve the enhancement on power conversion efficiency. In this chapter, we will show the background and basic knowledge of power management system in chapter 1.1 firstly. The classification of power management circuits which including switching converters, linear regulators, and charge pump converters will show in chapter 1.2. The motivation will give in chapter 1.3. Finally, the thesis organization will show in chapter 1.4.

1.1 Background of Power Management System

For portable power applications, the multi-level supply constructed by voltage regulators is an important technology. For example, the block diagram of cell phone system is shown in Fig. 1 [1]. Voltage regulator circuits (VR) regulate the battery voltage to provide different level voltage to suitable blocks: audio, display, interface, DSP core, analog circuits, and digital circuits. The system will operate in different modes, such as sleeping mode, communication mode and so on. The control unit is needed to control the internal power management block enable or disable, respectively. That is to say, by using control unit can enhance system efficiency of power supply circuits, such as linear regulators, switching regulators and charge pumps. When this technology is used, the energy consumption can be

reduced compared to that with the battery supply only [2].

As shown in Fig. 2, due to the increasing functionality and complexity in every single chip, the requirement on energy raises rapidly, make the growing of battery energy is not enough to supplying power of chips in the future. An easy method to solve is enlarging the capacity of batteries, but the increasing volume of portable devices isn't pleased to see because of user's convenience. In order to minimize the cost, the ability of saving power and increasing of power conversion efficiency is an important issue, that's why the power management system playing an irreplaceable role in analog integrated circuit design.

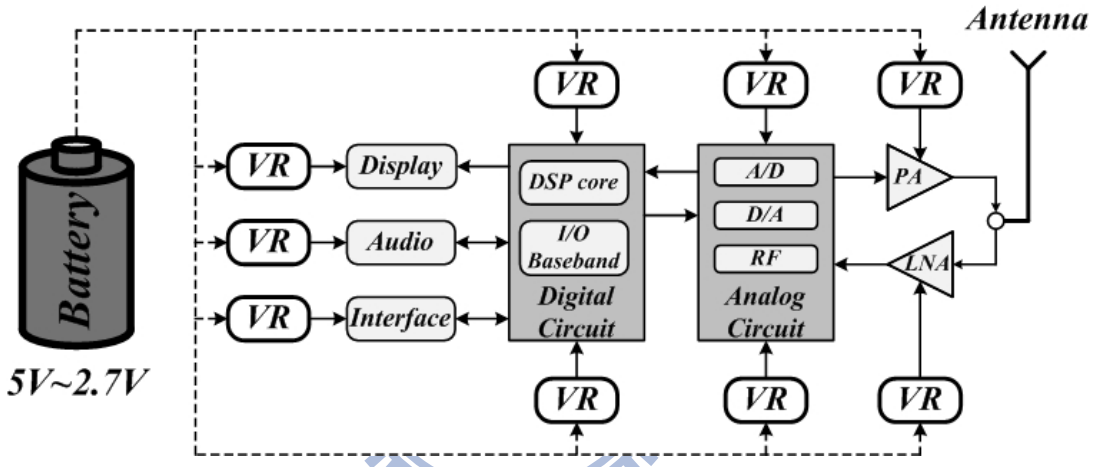


Fig. 1. The block diagram of cell phone system.

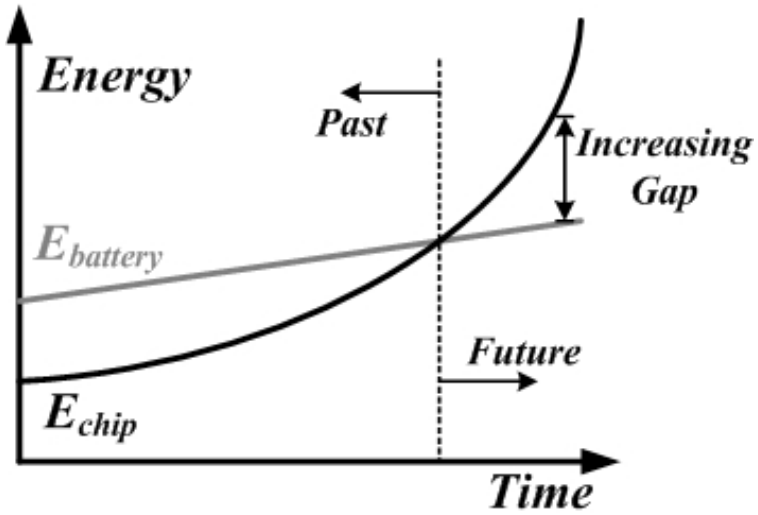


Fig. 2. The energy constrained operation.

1.2 Classifications of Voltage Regulators

General power management circuits used in portable devices can be classified into three technologies: linear regulators, switched capacitor circuits, and switching regulators. These voltage regulators will be introduced in briefly in this section, and comparisons will be given finally, including load ability, efficiency, circuit complexity, efficiency and so on.

1.2.1 Linear Regulator

The basic structure of linear regulator is shown in Fig. 3 [3], it's also called low drop-out (LDO) voltage regulator because of a drop out voltage ($V_{dropout}$) between input and output voltages about 100~500mV. An error amplifier controls the gate voltage of the pass transistor (M_{PWP}) with respect to a reference voltage (V_{REF}). These devices are constructed in a feedback configuration to maintain the output voltage irrespective of the load current variations. The power transistor has equivalent resistor (R_{DS}) from input to output, so the size of power transistor should be well designed to fit the regulated output voltage and load ability.

The advantages of linear regulator are described as follows. One is the circuit structure is simple, make the die size is the smallest in all kind of voltage regulators, another is linear regulator only uses feedback resistors and error amplifier's output analogy signal to control power transistor, it makes a purely analogy operation environment without any digital base circuits. So there is no Electro Magnetic Interference (EMI) issue and no output ripple.

There are two major disadvantages described as follows. Firstly, because of without dual storage components, the linear regulators only can do buck regulation. Secondly, since the output current must pass through the series transistor which consumes the dropout voltage between the output and input voltages, the efficiency is low for large voltage across

input and output voltages. The efficiency that depends on the difference of input and output voltages is given by (1).

$$\eta = \frac{V_{OUT} \cdot I_{LOAD}}{V_{OUT} \cdot I_{LOAD} + (V_{IN} - V_{OUT}) \cdot I_{LOAD}} \cong \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The major applications that use linear regulators can be classified to digital and analog. The digital applications include Digital Signal Processors (DSP), Input/Output (I/O) modules and memory type devices. Analog applications include signal-path applications such as power amplifier (PA) and Phase lock loop (PLL).

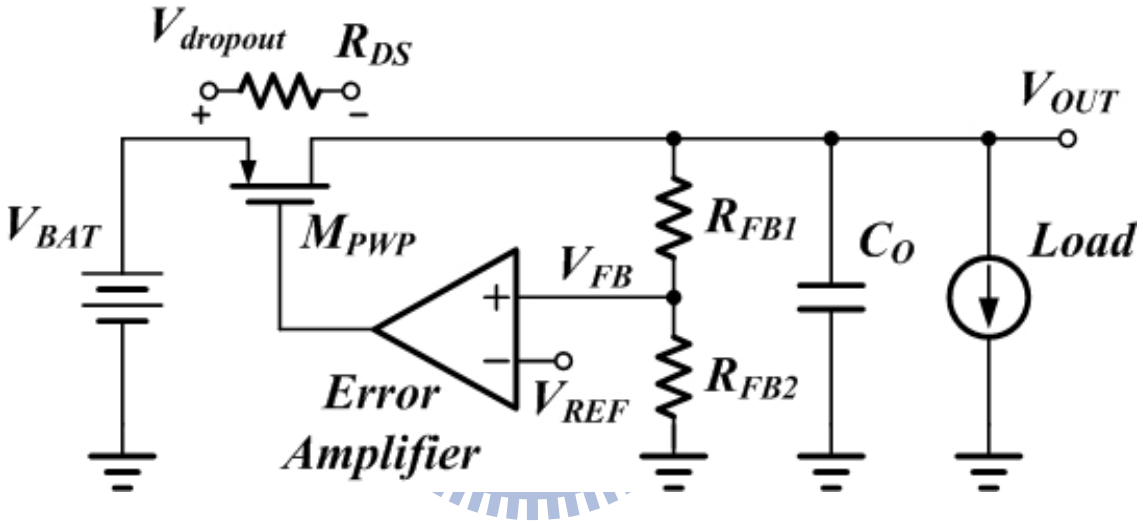


Fig. 3. The basic structure of linear regulator.

1.2.2 Switched Capacitor Circuit

The switched capacitor circuit is also called chare pump, is used to generate a dc voltage higher or lower than the supply voltage or opposite in polarity to the supply voltage in low power applications. Charge pumps use capacitors as energy storage devices. The capacitors are switched to deliver energies to obtain desired output voltage. Fig. 4 illustrates a conventional switched capacitor voltage doubler [4].

The switches S_1 and S_3 are closed during the first interval of the switching period, charging capacitor C_S to supply voltage (V_{BAT}). During the second interval of the switching

period, the switches S_2 and S_4 are turned on and the voltage across capacitor C_S is placed in series with the input to generate an output voltage that is twice the input voltage. In order to maintain the output voltage, there are many ways to modulate the output voltage of a switched capacitor circuit to a desired value. The most straightforward method is to use a control circuit and an error amplifier. The error amplifier senses the output voltage variations via the feedback resistors. The control circuit fed from the error amplifier controls switches S_1~S_4 to regulate output voltage to a stable value through a voltage control oscillator.

Depending on the hysteric feedback control and reference voltage, both buck and boost type can be used in switched capacitor circuits, and the circuit complexity is between linear regulators and switching regulators. But there is major drawback which is the load ability is depend on the size of output capacity (C_O) and switching frequency. That is to say, larger capacitor makes stronger load ability but consumes more chip size.

The charge pumps are useful in many different applications including low-voltage circuits, dynamic random access memory circuits, Electrically Erasable Programmable Read-Only Memory (EEPROM), and transceivers.

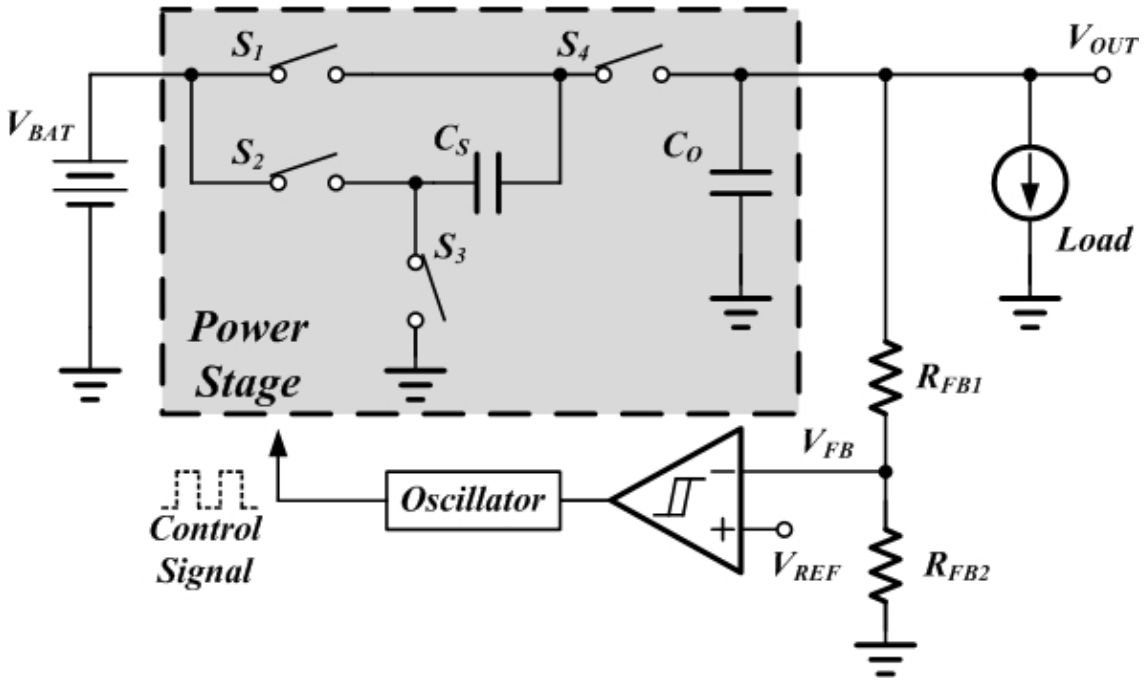


Fig. 4. The conventional structure of voltage doubler.

1.2.3 Switching Regulator

Switching regulators are widely used in power management system, because it has high efficiency and power handing capability. The conventional structure of buck type voltage mode control switching regulator is shown in Fig. 5 [5]. The regulator consists of a couple of complementary power transistors (M_{PWP} M_{PWN}), passive storage inductor (L), output capacitor (C_O), feedback resistors (R_{FB1} R_{FB2}), and control circuits.

The circuit operation is described as follows. The error amplifier receives the output voltage variation and produces the error signal (V_{EA}). The inputs of comparator receive the error signal from error amplifier and the ramp signal (V_{RAMP}) from ramp generator, then compares the quantity between V_{EA} and V_{RAMP} to decide the duty cycle. After generating the control signal, the logic block produce the detail timing to avoid short through current. Finally, control signals are sent to gate drivers to drive huge complementary power transistors. At the first subinterval, power PMOS (M_{PWP}) turns on and power NMOS (M_{PWN})

turns off then supply source charges the inductor and the output capacitor. At the second subinterval, power NMOS (M_{PWN}) turns on and power PMOS (M_{PWP}) turns off then the inductor will discharge to the output capacitor and load. As mentioned above, the switching regulator adjusts the output voltage error and regulates to correct voltage.

The advantages of switching regulators are described as follows. Firstly, the load ability is very large which in the range from no load to several amps. Secondly, the power conversion efficiency is high in medium to heavy load condition, up to 90%. Thirdly, switching regulators can operate in different kinds of type including buck, boost, and buck-boost type.

Nevertheless, there are some drawbacks described as follows. Firstly, the power conversion efficiency is poor at light load condition. Secondly, too many external components enlarging PCB size and cost. Finally, there are EMI and noise issues should be considered due to digital switching.

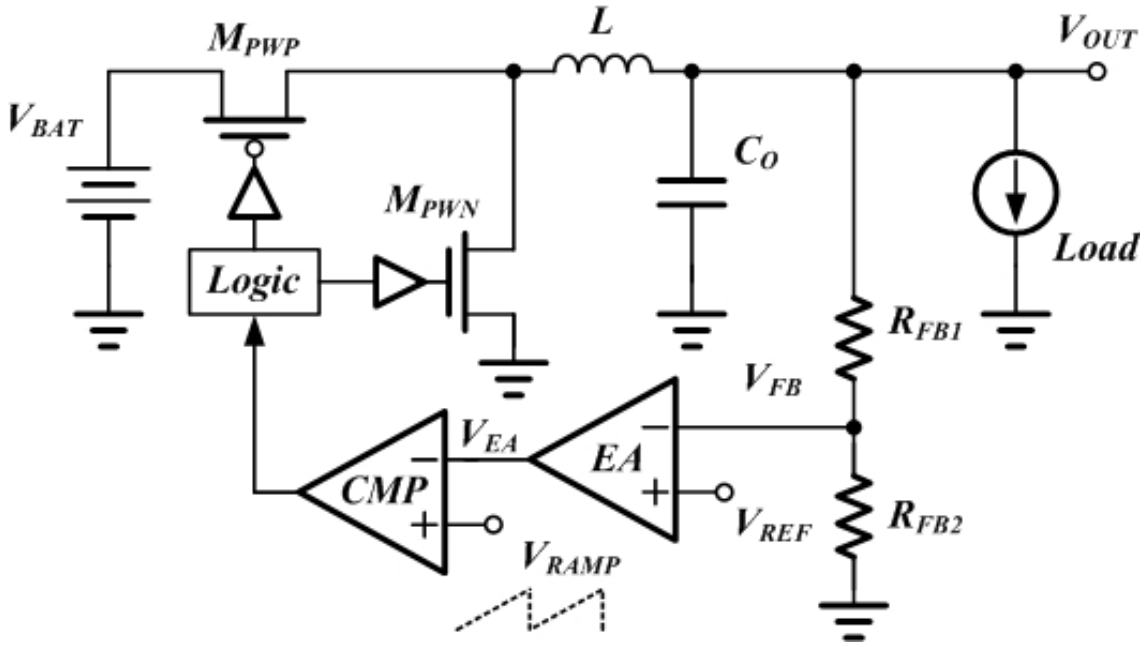


Fig. 5. The structure of buck type voltage mode control switching converter.

1.2.4 Comparison

A comparison table of power management circuits is listed in Table I. From Table I, we can conclude that switching regulators are best choices for power supplies driven portable application because of their high efficiency and large power handling capability.

Table I. Comparative table of power management circuits.

	Linear Regulator	***Charge Pump***	***Sw tching Regulator***
Regulation Type	Buck	Buck/Boost	Buck/Boost/Buck-Boost
Efficiency	Low	Medium	High
Power Capability	Medium	Medium	High
Footprint Area	Compact	Moderate	Large
Cost	Low	Medium	High
Complexity	Low	Medium	High
Noise	Low	Medium	High

1.3 Motivation

Recently, switching power converters use a high-switching controller to reduce the size of the output filter for compact solution in portable devices, such as cellular phones, wireless devices, and Bluetooth applications. However, the design of a high-switching controller needs to consider carefully the power conversion efficiency and high-switching noise caused by parasitic components. In general, the efficiency of a converter is defined as the ratio of output power, P_{out}, to input power, P_{in}, as expressed in (2).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{2}$$

P_{loss} is the sum of power loss in switching converters and can be expressed as (3). P_{con}

and $\boldsymbol{P_{sw}}$ are the conduction and switching losses, respectively. $\boldsymbol{P_{sys}}$ is the power loss in the controller, which is composed of analog and digital circuits [6].

$$P_{loss} = P_{con} + P_{sw} + P_{sys} \tag{3}$$

The conventional pulse width modulation (PWM) of the current mode control (Fig. 6) becomes limited as switching frequency increases. The control system can have high efficiency at heavy loads as the $\boldsymbol{P_{con}}$ is kept low by using low on-resistance of power switches. Incidentally, efficiency decreases drastically when the load gradually decreases to no load condition since the increasing value of $\boldsymbol{P_{sw}}$ dominates it. Specifically, the high-switching operation resulting from the use of a small inductor could deteriorate efficiency. Thus, it is important to keep high efficiency over a wide load range.

The power converter system generally undergoes multiple operation modes in order to extend the battery life of present-day portable devices. Essentially, these include standby mode regulated by the pulse frequency modulation (PFM), burst mode to save on power, and normal PWM operation mode to sustain system operation [7]. However, the circuit complexity, output ripple, and noise issue are not effectively treated [8]. It deteriorates the performance of the power converter and limits the load current range.

Furthermore, in the current-mode control, high-switching frequency decreases system accuracy due to limited response time of the inductor current sensor [9]. In addition, the switching noise drastically increases to deteriorate the accuracy of current sensor to decrease the system stability.

Thus, it is important to improve the estimation accuracy of the inductor current for high-switching operation. In prior arts, the equivalent series resistance (ESR) on the output capacitor can be used to generate the current ripple to achieve fast load transient response through the two voltage feedback loops [10]. However, it suffers from large output voltage ripple [11]. In addition, using large ESR for system stability limits the selection of output

capacitor. Specifically, the large ripple reduces the performance of the sequent stage that needs small transient voltage dip.

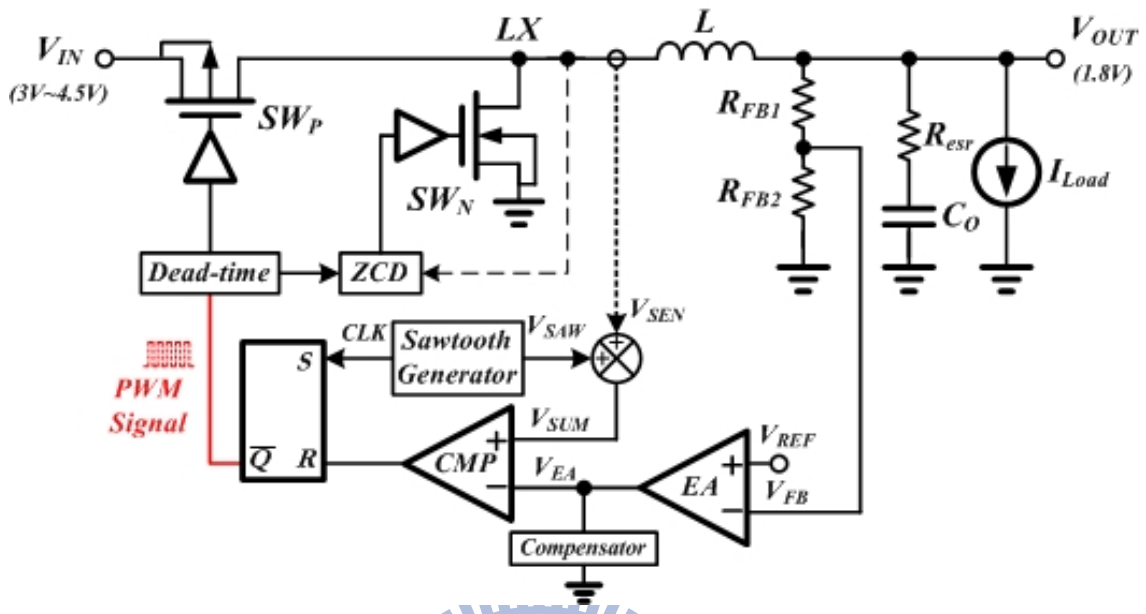


Fig. 6. The Conventional Current Mode Buck Converter.

1.4 Thesis Organization

Therefore, the proposed dual modulation technique with the AC ripple detector needs to improve power conversion and remove high-switching noise to increase system stability simultaneously.

The dual modulation technique can separate the inductor current into the AC ripple signal and the loading potential signal. It can accurately acquire the inductor current information to decide the duty cycle without the need of large ESR. The loading potential signal not only can determine the optimum switching numbers for each power switch at different loads, it also can generate a hopping switching frequency at light loads for high-conversion efficiency. Furthermore, the hopping switching frequency should be higher than the acoustic frequency to avoid noisy sound. Compared with conventional PWM switching converters, the dual modulation technique can achieve faster transient response

and higher power conversion efficiency simultaneously with an acceptable output ripple. In addition, multilayer ceramic capacitors (MLCC) can be selected as the output capacitor for low cost.

Table II compares the converter with different control methods. The dual modulation mode not only has good efficiency but also reduces the output ripple and chip area compared with other methods. Specially, the audio noise, which is important issue for communication applications, can be effectively reduced.

The organization of this thesis is shown as follows. Chapter 2 introduces the design concept of the proposed dual modulation technique and the AC ripple detector. The close-loop analysis is described in chapter 3 to demonstrate the system stability. The circuit implementation is shown in chapter 4. In the chapter 5, experimental results can prove the correction of the dual modulation technique and the conclusion are demonstrated.

Table II Comparative table of power management circuits.

	PFM mode	***Burst mode***	***Dual modulation mode***
Efficiency	Good	Good	Good
Circuit Complexity	Large	Medium	Small
Output Ripple	Large	Medium	Small
Audio Noise	Small	Large	Small
Load Range	Medium	Small	Wide

Chapter 2
Basic Knowledge of Switching Regulators

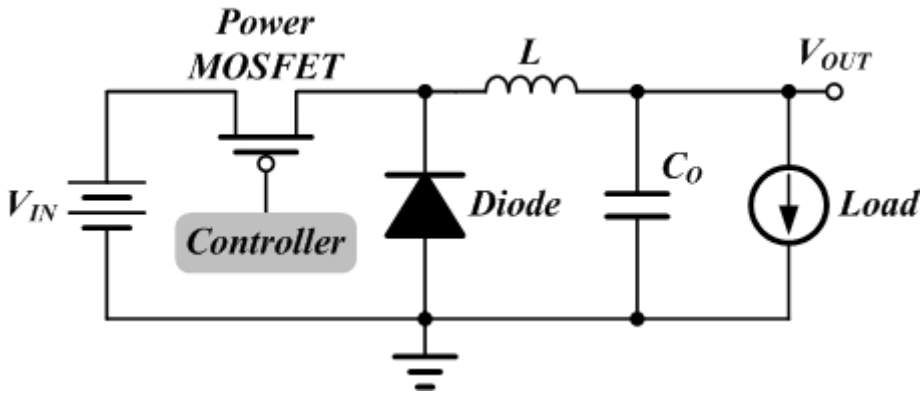
In the chapter 2, the basic knowledge of switching regulators is presented. The three kinds of switching regulators including buck, boost, and buck-boost converters are introduced in section 2.1. The section 2.2 will show three kinds of controlling modulators including pulse width modulation (PWM), pulse frequency modulation (PFM), and hysteretic control technique in buck converters. Finally, the characteristics and performance specifications of buck converters are presented in section 2.3.

2.1 Topologies of DC-DC Converters

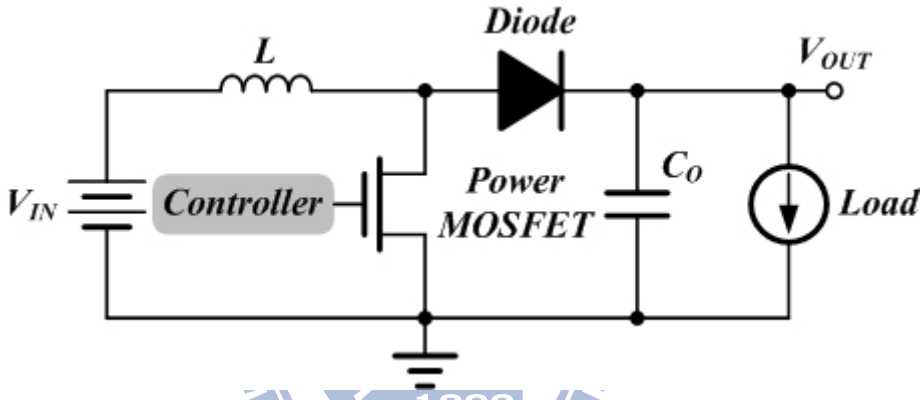
According to different placement of components, DC-DC converters can be classified into three types which are buck, boost, and buck-boost converters. These three types of converters are shown in Fig. 7 [12]-[14] and introduced in this section. All of converters consist of storage elements; power MOSFETs as the switch to control and drive large current by the control signal, and diode as another current passage to charge or discharge output loads. The control signal controls the energy from input to output by passing the power MOSFETs and regulated output to desired voltage.

The buck converter can only regulate a voltage lower than the input voltage. Contrarily, the boost converter only regulates a voltage higher than the input voltage. The buck-boost converter can regulate output voltage no matter higher or lower than the input voltage. A briefly comparison of three converter topologies characteristics are listed in the Table II. The conversion ratio is defined as dividing the input voltage into the output voltage, and

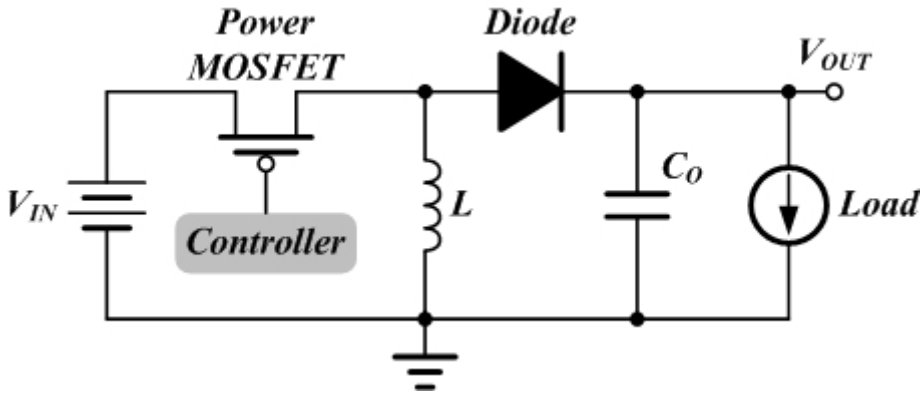
duty ratio (***D***) is defined as the power MOSFETs on time during one switching period.



(a) Buck type DC-DC converter



(b) Boost type DC-DC converter



(c) Buck-boost type DC-DC converter

Fig. 7. The three topologies of DC-DC converters

Table III. Comparisons of three converter topologies.

	Buck Con erter	***Boost Converter***	***Buck-boost Converter***
Conversion Ratio	$\frac{V_{OUT}}{V_{IN}} = D$ ***(CCM)***	$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$ ***(CCM)***	$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D}$ ***(CCM)***
Conversion Type	***Step-down only***	***Step-up only***	***D>0.5:Step-up D<0.5:Step-down***

2.2 Technologies of Controlling Modulator

Although switching converters have high conversion efficiency, but the power loss will increase and result in efficiency reduction at different load conditions. The power consumptions can be classified with three parts. The first is the power losses due to large current pass through the equivalent resistance of the power MOSFET, the equivalent resistance can be expressed as R_{ON}, this power consumption is named conduction loss (P_{CON}) and expressed as follow.

$$P_{CON} = I_{OUT}^2 R_{ON} \tag{4}$$

The second part is the charging and discharging alternately at large gate parasitic capacitor of the power MOSFET when the switching on and off periodically. This is a large loss of converters at light load condition named switching loss (P_{SW}) and expressed as follow.

$$P_{SW} = (C_{GP} + C_{GN}) V_{IN}^{\ 2} f_{SW} \tag{5}$$

The C_{GP} and C_{GN} are represented as gate parasitic capacitors of power PMOSFET and NMOSFET, V_{IN} is represented as input voltage, and f_{SW} is represented as switching

frequency. The third is the quiescent current of converter's internal controller to regulate output voltage at no load, it's also called idle mode. This power consumption is named system power loss ($\boldsymbol{P_{SYS}}$) and defined the multiplication of quiescent current and input voltage. That is to say, the power conversion efficiency of DC-DC converters can be defined the ratio of the output power and the total input power, and is expressed as follow.

$$\begin{aligned} Efficiency(\eta) &= \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \\ &= \frac{P_{OUT}}{P_{OUT} + P_{SW} + P_{CON} + P_{SYS}} \times 100\% \end{aligned} \tag{6}$$

As above mentioned, the conduction loss ($\boldsymbol{P_{CON}}$) is dominated at heavy load because of large output current flowing through the power MOSFETs. Contrarily, switching loss ($\boldsymbol{P_{SW}}$) and system loss ($\boldsymbol{P_{SYS}}$) are dominated at light load condition because of slight output current. So how to maintain high efficiency at wide load range is an important issue.

There are three most basic controlling methods named pulse width modulation (PWM), pulse frequency modulation (PFM), and hysteretic control technique. The following sections will introduce these controlling methods, respectively.

2.2.1 Pulse Width Modulation (PWM)

In PWM control operating, the power MOSFETs are controlled by a constant clock cycle, the PWM control waveforms are shown in Fig. 8 [15] [16]. While the ramp signal is lower than the control signal, the PWM signal at high level; contrarily, when the ramp signal is higher than the control signal, the PWM signal changes to low level. The main modulation is change the width of every clock cycle by the control signal and the output voltage is determined by the duty ratio of the PWM signal.

The conduction loss and switching loss are focused in PWM control operation. The summation of these two power loss is expressed as follows.

$$P_{CON} + P_{SW} = I_{OUT}{}^2 R_{ON} + (C_{GP} + C_{GN}) V_{IN}{}^2 f_{SW} \quad (7)$$

As shown in Eq. (5), the switching frequency is constant but output current varies with different loads. That is to say, the conduction loss maintains fixed but the switching loss is variable with loads. The summation of conduction loss and switching loss at different load can be shown in Fig. 9.

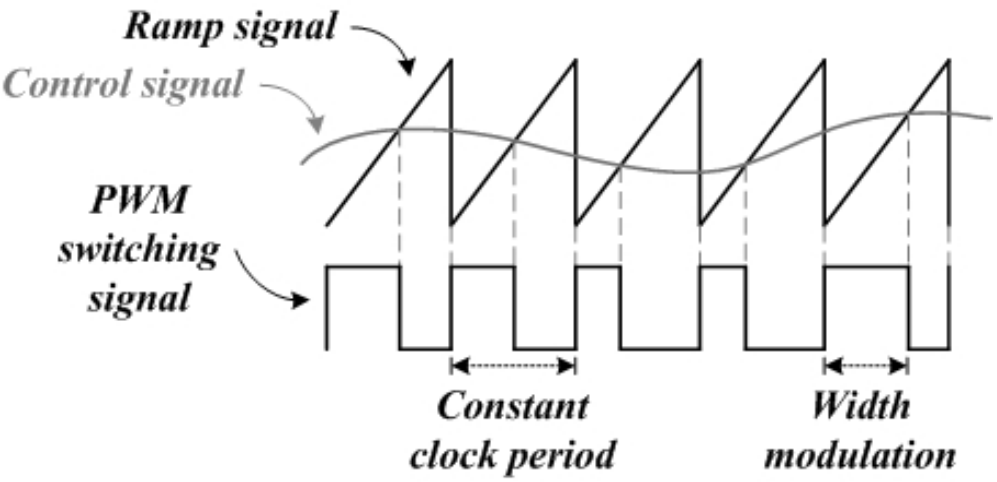


Fig. 8. Waveforms of pulse width modulation.

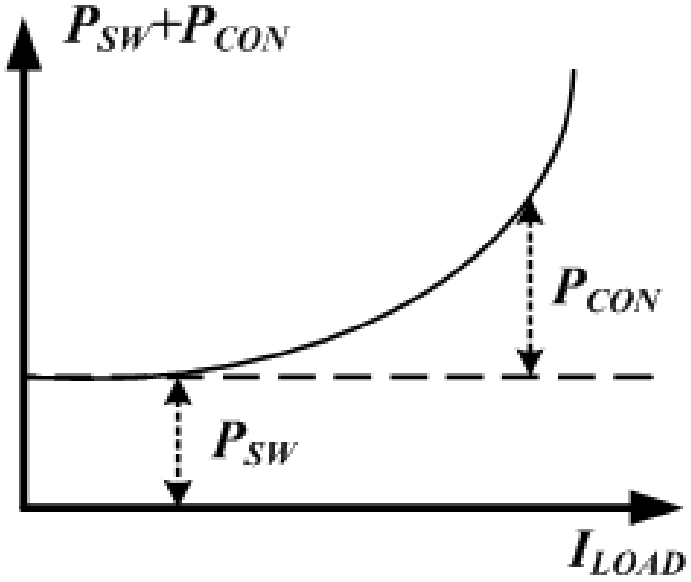


Fig. 9. Combination of conduction loss and switching loss in PWM control.

2.2.2 Pulse Frequency Modulation (PFM)

In PFM control operating, power MOSFETs are controlled by a vary frequency, the control waveforms are shown in Fig. 10 [17]. The on-time is fixed and off-time is variable determined by different loads in PFM control. By controlling the off-time of each switching cycle, the desired output voltage can be obtained. Therefore, the smaller output load could make switching frequency reduced.

The summation of conduction loss and switching loss in PFM control is the same with Eq. (5). In PFM control operating, vary switching frequency with different load conditions makes the switching loss reduced at light load, the diagram is shown in Fig. 11.

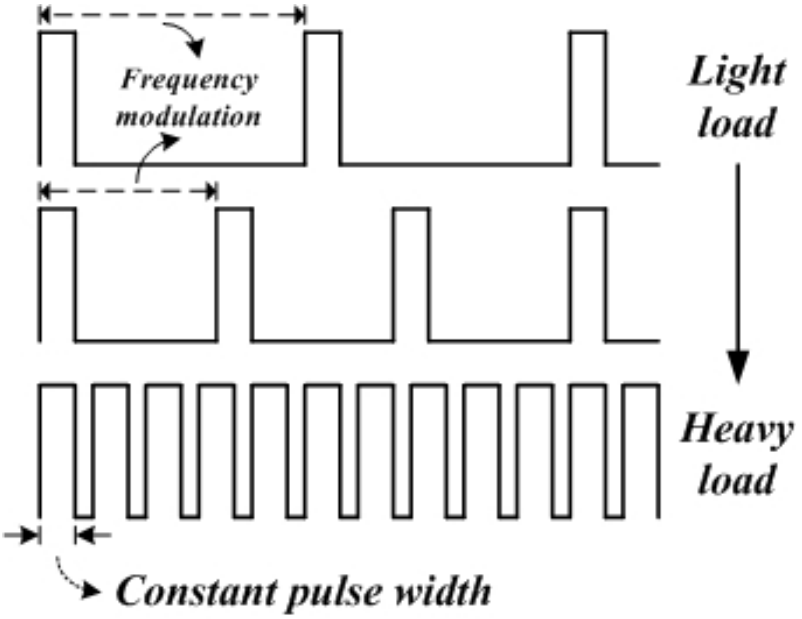


Fig. 10. Control signal waveforms of pulse frequency modulation.

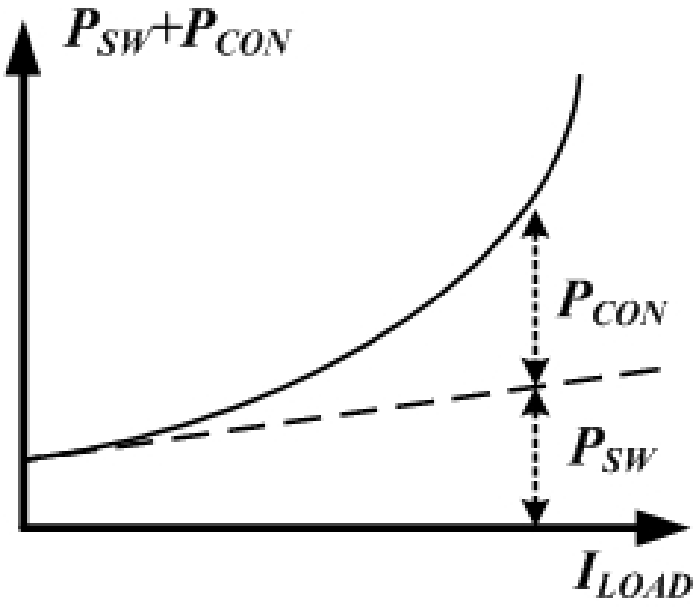


Fig. 11. Combination of conduction loss and switching loss in PFM control.

2.2.3 Hysteretic Control Technique

The hysteretic control structure is shown in Fig. 12 [18], the main control method is generating a hysteresis window. By controlling the upper and lower boundary to regulate the output voltage, when the feedback voltage touch to the hysteretic upper boundary, the power NMOSFET will turn on and PMOSFET will turn off to make the inductor current discharged and feedback voltage will decrease. At the same time, the hysteretic window will change to the lower boundary. While the feedback voltage touch to the hysteretic lower boundary, the power PMOSFET will turn on and the power NMOSFET will turn off to make the inductor current charged and feedback voltage will increase. The hysteretic window which is calculating by superposition theorem can be expressed as follows.

$$\begin{aligned} V_H &= V_{upper} - V_{lower} \\ &= (V_{REF}\frac{R_2}{R_1+R_2} + V_{IN}\frac{R_1}{R_1+R_2}) - (V_{REF}\frac{R_2}{R_1+R_2}) \\ &= V_{IN}\frac{R_1}{R_1+R_2} \end{aligned} \tag{8}$$

The features of hysteretic controller are described as follows; firstly, the main control

circuit is comparator, so there is no compensation issue without error amplifier. Secondly, without using any clock generator, the switching frequency of hysteretic controller is generated by system itself. The following is the calculation of feedback voltage variation, as expressed as follows.

$$I = C\frac{dV}{dt} \Rightarrow \frac{V_{FBAVG} - 0}{R} = C\ \frac{\Delta V_{FB}}{t_{OFF}}$$
$$\Rightarrow \Delta V_{FB} = \frac{t_{OFF} V_{FBAVG}}{RC} = \frac{DV_{IN}(1-D)T_0}{RC} \quad (9)$$

The voltage V_{FBAVG} is the average voltage of feedback, ideally is D_{VIN}, the parameter D, is the duty ratio of the buck converter. Because the hysteresis window variation (V_H) equals to feedback voltage variation ($\triangle V_{FB}$). Combining the Eq. (8) and Eq. (9), the switching frequency can as expressed as follows.

$$V_H = \Delta V_{FB} \Rightarrow V_{IN}\frac{R_1}{R_1 + R_2} = \frac{DV_{IN}(1-D)T_0}{RC}$$
$$\Rightarrow f_0 = \frac{1}{T_0} = \frac{1}{RC}D(1-D)(1+\frac{R_2}{R_1}) \quad (10)$$

By controlling the resistor R, capacitor C and the ratio of resistors R_1 and R_2 can define the switching frequency, which is very suitable for high switching frequency design. Finally, because the output ripple has been defined, it can't choose the low ESR capacitor to reduce output ripple.

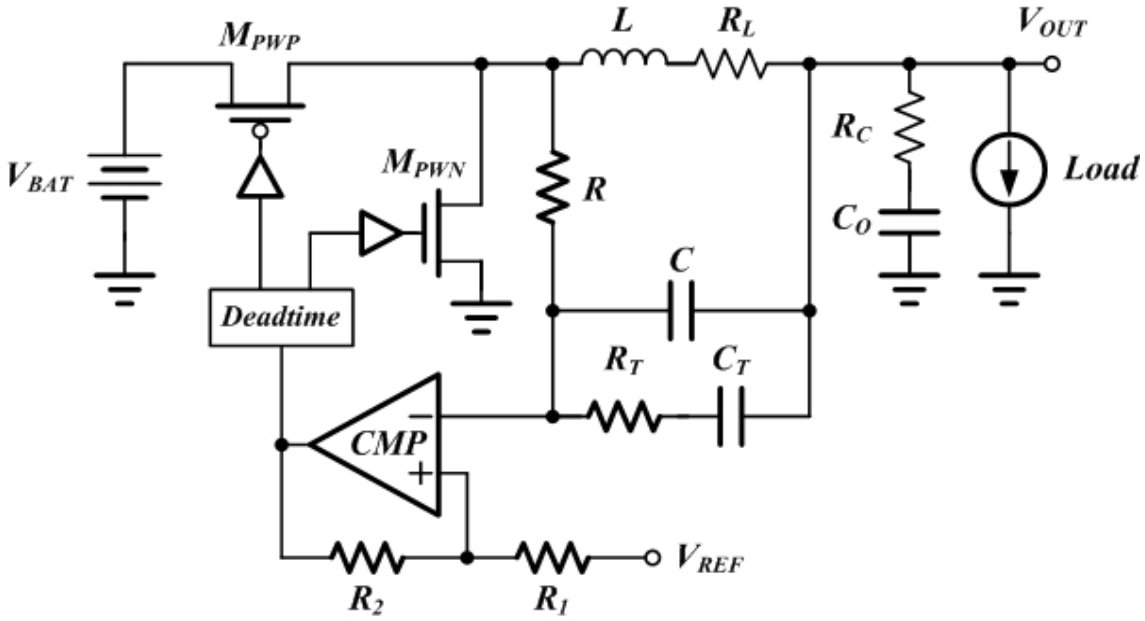


Fig. 12. The structure of hysteretic control technique.

2.3 Specifications of Switching Regulators

Due to more and more electronics application need to be supplied by switching converter, the performances of switching converter have to be considered. The important specifications should be care about are listed as follows. Firstly, the power conversion efficiency of switching regulator is an important topic, how to maintain high efficiency over wide load range will be discussed in the section 2.3.1. The second is excellent load and line regulation, which will be discussed in the section 2.3.2. Final part is the transient response, how to immediately response when the suddenly large output current variation will be shown in the section 2.3.3.

2.3.1 Power Conversion Efficiency

The definition of switching regulator's power conversion efficiency is the ratio of input power and output power and can be wrote as

$$Efficiency(\eta) = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100\% \quad (11)$$

The detail power losses and the operation range of control modulator have been shown in the section 2.2. Overall saying, the pulse width modulation (PWM) mode is suitable for operating in heavy load condition, and the pulse frequency modulation (PFM) is suitable for operating in light load condition. If the switching regulators operating only one module mode, take cell phone for example, the cell phone system operates in standby mode and many blocks of system doesn't work, at light load condition but the converter only have PWM controller, as a result, the battery lifetime will reduce quickly. Hence, the best way to improve the efficiency is including the pulse frequency modulation (PFM) to control at light load condition. By dual mode control can keep high efficiency over wide load range. The comparison of PWM and PFM control technique will be listed in TABLE III.

Table IV. Comparisons between PWM and PFM controls.

	Pulse Width Modulation	***Pulse Frequency Modulation***
Well Efficiency Range	*Moderate to heavy load*	*Light load*
Frequency	*Constant*	*Variable*
Switching Loss of Whole Load	*Constant*	*The heavier load the larger loss*
Output Ripple	*Smaller*	*Larger*
Transient Response	*Faster*	*Slower*
Circuit Complexity	*Complicated*	*Simple*
Quiescent Current	*Larger*	*Lower*

2.3.2 Load and Line Regulation

Switching regulators are powerful system of stepping up or down the desired voltage. Therefore, to keep the regulated voltage and decrease the steady state error when varying the supply voltage and load condition of DC-DC converter is the most important.

The load regulation is defined as the percentage of steady state error of output voltage when the load condition changes and can be calculated as follows.

$$Load\ Regulation = \frac{\Delta V_{OUT}}{V_{OUT\_desired}} \cdot \frac{100}{\Delta I_{load}} \left(\%/mA \right) \tag{12}$$

The line regulation is defined as the percentage of steady state error of output voltage when the input voltage changes and can be calculated as follows.

$$Line\ Regulation = \frac{\Delta V_{OUT}}{V_{OUT\_desired}} \cdot \frac{100}{\Delta V_{IN}} \left(\%/mA \right) \tag{13}$$

2.3.3 Transient Response

The transient response is an important specification of DC-DC converter for the system applications. The large load current changes suddenly will cause a voltage fluctuation at output of DC-DC converter. The voltage fluctuation may trigger the logic circuit or affect the analog circuit. Therefore, it's important to reduce the large voltage changing and the time during voltage variation. The transient response of output voltage relates to load current is shown in Fig. 13. During the first period Δt_1, the large current flows into the output load from DC-DC converter, due to the DC-DC converter cannot provide enough energy to maintain the output voltage, the output voltage will drop in this period because the output capacitor discharge the energy to support the load current. The drop voltage is shown in Eq. (14). According to the parameters of Eq. (11), selecting the output capacitor well can reduce the drop in this period.

$$V_{drop1} = V_{drop2} = \Delta I_{OUT} \times \left(\frac{\Delta t_1}{C_O} + R_{ESR} \right) \tag{14}$$

During the second period Δt_2, the system senses the output variation by feedback loop then turn on the power PMOSFET to recover the regulated output voltage. The summation of Δt_1 and Δt_2 is called the recovery time and the second period Δt_2 depends on the system bandwidth of the DC-DC converter

The static error ΔV_{OUT} between light load and heavy load is relates to the voltage regulator DC gain, the higher DC gain bringing the better load regulation [19]. Comparing to the Fig. 12(b) and Fig. 12(c), the performance of Fig. 12(b) due to the large DC gain and causes the better load regulation, but the second period Δt_2 extends the recovery time. However, it reduces the time of transient response. The performances of Fig. 12(c) due to the poor DC gain and cause huge static error but reduces the time of second period Δt_2 and improve the dynamic performance.

When the load current is decreasing to light load suddenly, the output voltage will jump until the DC-DC converter start to recovery the regulated voltage. The redundant current charges the output capacitor resulting to a peak voltage as shown in shown in Eq. (15) before the feedback loop of DC-DC converter reacts.

$$V_{peak1} = V_{peak2} = \Delta I_{OUT} \times \left(\frac{\Delta t_3}{C_O} + R_{ESR} \right) \tag{15}$$

During the final period Δt_4 the output capacitor discharged the redundant current to feedback resistors. As mention described, the transient response is relates to the bandwidth of DC-DC converter, output capacitor, equivalent series resistance (R_{ESR}) of output voltage and the load current.

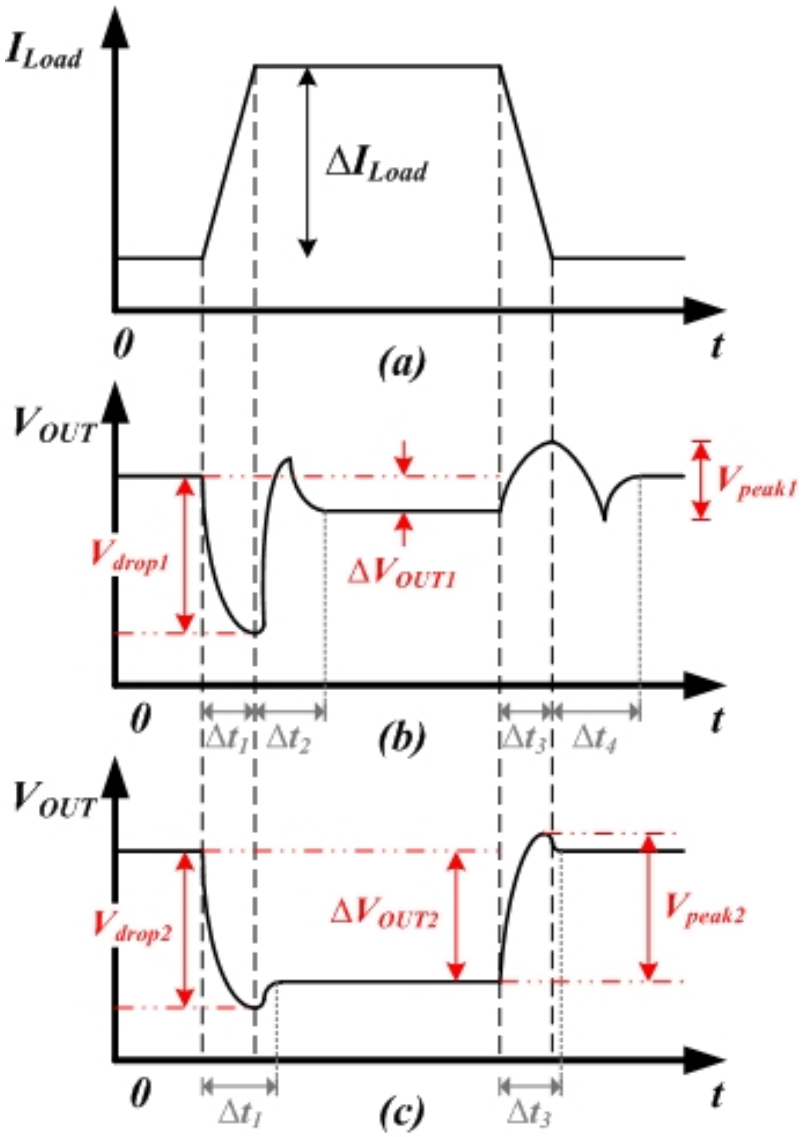


Fig. 13. The transient response of output voltage relates to load current.

Chapter 3

The Theory of the Dual Modulation Technique in High Switching Buck Converters

In the chapter 3, we present the concept description of the proposed technique in high-switching converters. In the section 3.1, we discuss the drawbacks of the conventional switching converter operating at a high switching frequency. And the section 3.2 describes the analysis of the proposed dual modulation technique. Finally, the loop analysis of conventional V^2 control and the proposed system are presented in section 3.3.

3.1 High Switching Operation Issues

The conventional switching power converters are suitable for normal operation frequency such as the range from 0.1MHz to 1MHz. The bandwidth and the operational phase delay of sub-circuits can be neglected because of the longer switching period. But lower switching frequency makes the output passive components including inductor and capacitor must be chosen larger values and need to be placed off-chip. That is to say, the cost increases due to the off-chip components and the larger PCB size.

In DC-DC buck converters, the inductor current ripple is inversely proportional to the switching frequency, so the size of output LC filter can be reduced due to the smaller inductor current ripple. Hence, in order to integrate the passive components into chip, increasing switching frequency is the most straightforward way.

When buck converter operates in high switching frequency, the internal controller of the converter may suffer from some problems. Firstly, the quiescent current of comparators

must be increased to have enough slew rate, it results more power consumption. Secondly, the inductor current signal is hard to be sensed due to the current sensing circuit doesn't have enough bandwidth in conventional current mode control. Finally, the main power consumption is determined by the sum of the conduction loss and the switching loss. Arising switching frequency makes the switching loss increased, so the power conversion efficiency is deteriorated when load current decreases gradually. Thus, high switching converters are rare to be used in common commercial applications.

To solve the drawbacks mentioned above, the frequency hopping modulation technique with AC ripple detection is presented, and the design concept description of the proposed method is introduced in the next section.

3.2 Design Concept Description

3.2.1 Dual Modulation Technique

For high-switching operation, power conversion efficiency decreases drastically when load current changes from heavy to light. The dual modulation technique needs to hop switching frequency to find a trade-off between power conversion efficiency and output voltage ripple when load current decreases [20].

The timing diagram of the dual modulation technique is illustrated in Fig. 15. The original PWM control uses a high- switching signal V_{PRI} to regulate the output voltage to achieve a reduced ripple. Since the conduction loss dominates the whole power consumption at heavy loads, the high-switching signal would not result in a great decrease in efficiency. However, the switching loss drastically deteriorates efficiency from medium- to light-load condition due to the high-switching operation. Therefore, the secondary modulator becomes necessary to reduce the switching numbers as shown by the modulated signal V_{GATE} used to control the power switches. At this time, dual modulation operates to

raise efficiency within an allowable output ripple.

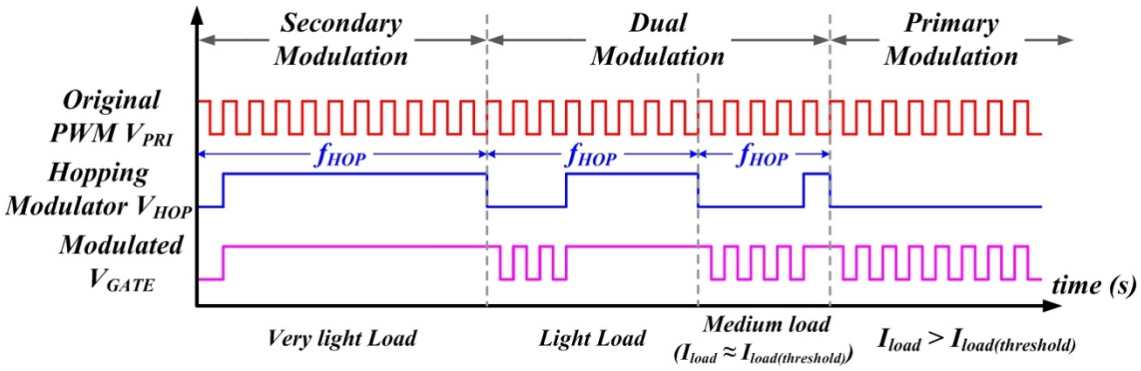


Fig. 14. Waveforms of the buck converter with the dual modulation technique.

The secondary modulator contributes to the decrease in the switching frequency and the increase in the hopping period. Light-load conditions require reduced switching frequency in order to save power. The hopping frequency modulator (HFM) circuit can determine a suitable switching frequency to reduce substantially the switching power loss at the power switches. Meanwhile, dual modulation starts to decrease the switching frequency from the constant $f_{SW(constant)}$ to $f_{SW(dynamic)}$ through the hopping frequency, f_{HOP}, in the secondary modulator. As depicted in Fig. 16, the value of f_{HOP} varies with load current. In addition, the hopping frequency not only reduces switching loss but also always keeps the output ripple within the allowable range.

The decrease in the switching frequency is accompanied with an increase in the hopping period as load current declines continuously. The decrease in switching frequency results in increased efficiency from a medium- to light-load condition. Much power is retrenched due to the switching loss reduction at the power MOSFETs. To further raise efficiency at very light loads, the primary modulator is shut down automatically and only the secondary modulator is employed to regulate the output voltage and to save much power in the quiescent operation loss. Furthermore, to avoid operation in the acoustic region, the hopping frequency is always kept higher than the acoustic frequency, $f_{acoustic}$, even at no load condition.

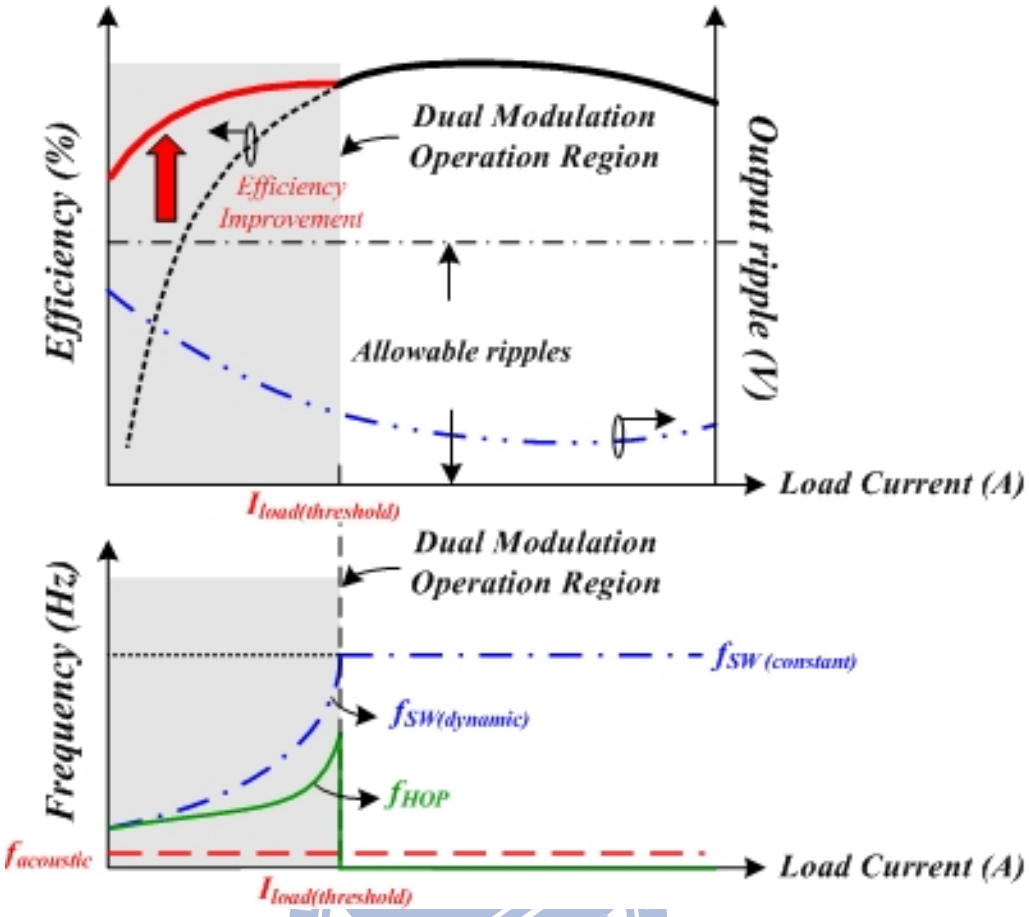


Fig. 15. Efficiency and hopping frequency versus load current for the proposed converter system.

3.2.2 AC Ripple Detection Technique

The architecture of the proposed dual modulation technique is shown in Fig. 16. The controller is separated into two parts. The primary modulator makes the system operate normally under high-switching frequency, and the secondary modulator can raise power conversion efficiency at light loads. Thus, high power conversion efficiency and a fast transient response under high-switching operations can be achieved.

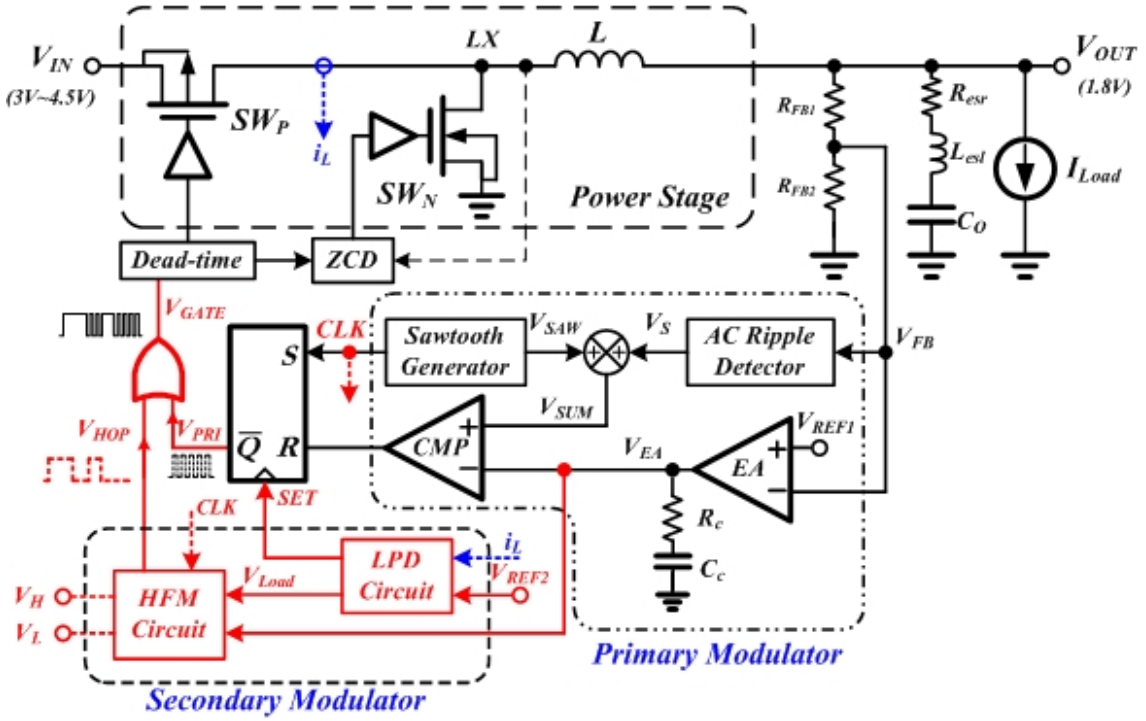


Fig. 16. The proposed buck converter with the dual modulation technique.

The dual modulation technique should detect the load condition using the proposed loading potential detector (LPD) circuit. In addition, the combination of the LPD circuit and the error signal received by the error amplifier can be viewed as the control signal in the HFM circuit. As a result, the hopping signal generated by the secondary modulator can regulate the original PWM signal to find the trade-off between efficiency and output voltage ripple.

For high-switching converters, the conventional current sensing method may fail to provide accurate sensing load current due to limited bandwidth. Thus, it is better to find a

suitable current sensing method for the high-switching converter. Fig. 17 shows the concept of the proposed AC ripple control. In time domain, the output LC stage of the converter can be considered as a low-pass filter and work as an integrator.

However, the existence of ESR and ESL may deteriorate the accuracy of current sensing signal and the steady state duty cycle. Considering the ESR, Resr, and the equivalent series inductor (ESL), Lesl, on the output capacitor, CO, the output voltage ripple can be evaluated as the summation expressed in (16).

$$v_{out} = v_{out|esr} + v_{out|esl} + v_{out|Co} = R_{esr} i_L + L_{esl} \frac{di_L}{dt} + \frac{1}{C_O} \int i_L dt \tag{16}$$

Briefly, (16) is composed of overshoot voltage, $\boldsymbol{v_{out|esr}}$, across the ESR; induced voltage, $\boldsymbol{v_{out|esl}}$, which is the differentiation of the inductor current with ESL; and voltage ripple, $\boldsymbol{v_{out|Co}}$, which is the integration of the inductor current on the $\boldsymbol{C_O}$. Thus, it is convenient to differentiate $\boldsymbol{v_{out}(t)}$ in order to obtain the AC signal of the inductor current. This can be expressed as

$$v_s = \frac{dv_{out}}{dt} = R_{esr} \frac{di_L}{dt} + L_{esl} \frac{d^2 i_L}{dt^2} + \frac{i_L}{C_O} \tag{17}$$

At the right side of (17), the first and second terms represent the effect of the ESR and ESL, respectively. Owing to high-switching operation, the ESR and ESL seriously affect system stability and result in a large output ripple. The inductor current information can be accurately derived through the operation of the proposed AC ripple detector. The AC ripple detector behaves as a differentiator and inserts one low-frequency zero to increase system stability. One low-pass filter is utilized to filter out the high-frequency components contributed by the ESR and ESL. Consequently, the accurate inductor current can be derived as the PWM ramp since the effect of the ESR and ESL can be efficiently removed. In other words, the cheap MLCC can be selected as the output for low cost.

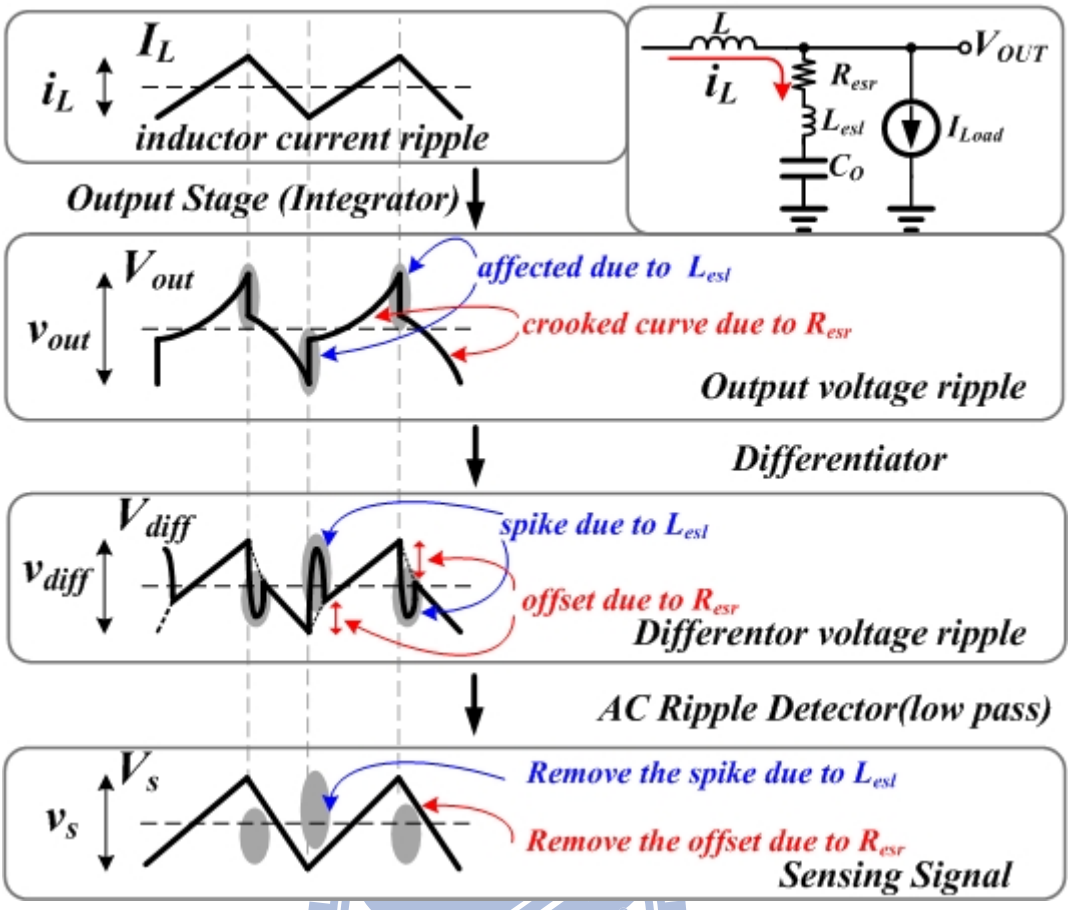


Fig. 17. The concept of current sensing flow as it utilizes the AC ripple detector.

3.2.3 Summary

To sum up the concept described above, the proposed dual modulation technique can solve the converter's large switching loss in high switching frequency operating. Hence, the size of the output LC filter is reduced without consuming too much power consumption in the light load condition, it makes high switching converters are more suitable for common commercial applications. And the modified V^2 control method can regulate output voltage even in zero-ESR condition, and the reduced output voltage ripple can make the converter more suitable for portable device applications. The V^2 control topology contains two voltage feedback paths; the path from output voltage can rapidly react to the output voltage variation to speed up the transient response.

We present a new control technique can operate in high switching frequency, which not

only can speed up the transient response, but also can maintain high power conversion efficiency over a wide load range.

3.3 Loop Analysis

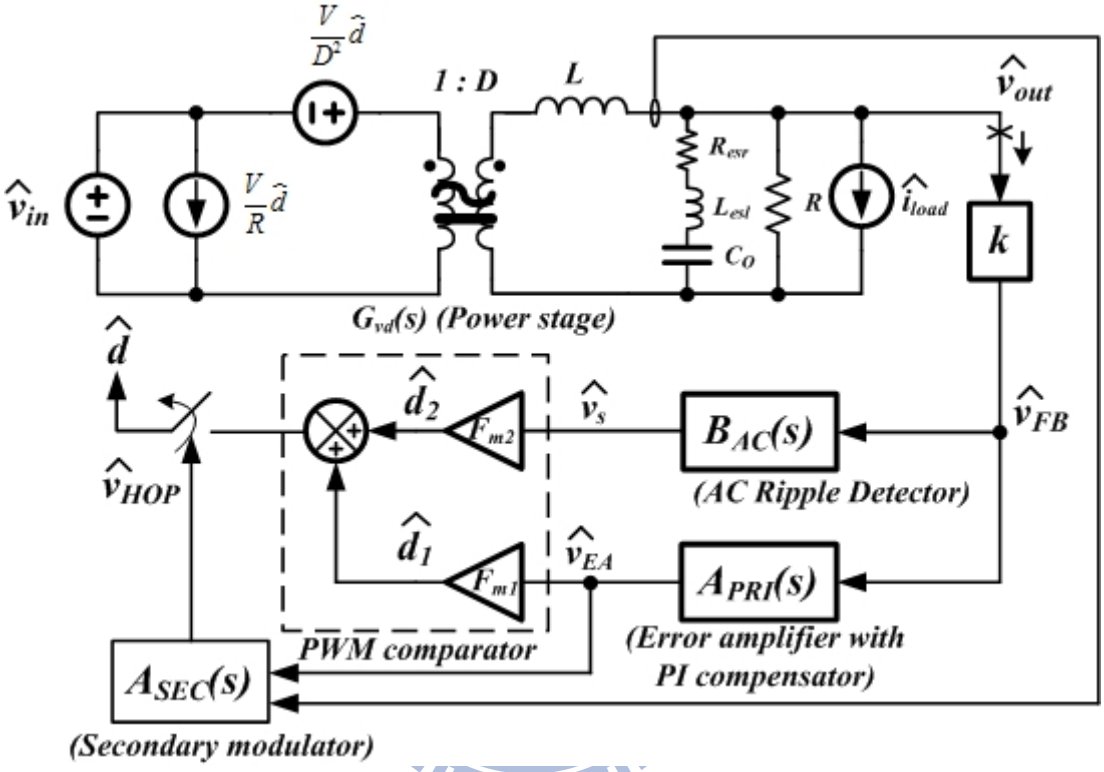


Fig. 18. Small-signal model of the AC ripple control buck converter.

Fig. 18 shows the small-signal model of the dual modulation buck converter with the AC ripple detector [23]. The loop gain can be divided into two parts. The first part, which is the power stage, contributes duty-to-output transfer function and contains dual poles due to the output LC filter as expressed in (18) with a DC gain of G_{vd0}.

$$G_{vd}(s)=\frac{\hat{v}_{out}}{\hat{d}}=G_{vd0}\cdot\frac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{2\zeta}{\omega_O}s+\left(\dfrac{s}{\omega_O}\right)^2} \tag{18}$$

$$\text{where } \omega_{esr}=\frac{1}{R_{esr}C_O},\omega_O=\frac{1}{\sqrt{LC_O}}, \text{ and } \zeta=\frac{1}{2}\left(\sqrt{\frac{C_O}{L}}R_s+\frac{\sqrt{\dfrac{C_O}{L}}}{R_L}\right)$$

The zero, ω_{esr}, generated by R_{esr} is pushed to high frequencies by using small ESR. R_L is the loading resistor and R_s is the series resistor of the LC resonant loop, which is the sum of MOSFET on resistance, inductor resistance, and R_{esr}.

The second part, composed of the controller, contributes the output-to-duty transfer function. In dual modulation, the control path contains two feedback loops, namely, the primary loop and the secondary feedback loops. The primary feedback loop is determined by the AC ripple detector and the error amplifier. Thus, the primary duty cycle can be decided through the signals, v_s and v_{EA}, by the PWM comparator. On the other hand, the secondary feedback loop is determined by the error amplifier and the secondary modulator.

The loop selection is determined by the LPD circuit. At very light loads, only the secondary modulator loop is selected as the feedback path. The feedback signal directly passes through the secondary modulator loop, $A_{SEC}(s)$, to generate the duty cycle. As load current increases continuously, the feedback signal passes through both primary and secondary loops. Thus, dual modulation combines the primary and the secondary modulators at medium to light loads. At heavy loads, the feedback path is decided by the primary modulator when load current is larger than $I_{load(threshold)}$. The feedback signal only passes through the primary loop since the secondary loop $A_{SEC}(s)$ is disabled and the switch is always connected to the primary path.

The transfer function, $A_{PRI}(s)$, of the error amplifier with the PI compensator can be

derived as (19).

$$A_{PRI}(s) = G_m R_o \frac{1+\frac{s}{\omega_{PI\_z}}}{1+\frac{s}{\omega_{PI\_p}}} \tag{19}$$

The DC gain is constituted by the error amplifier's transconductance, $\boldsymbol{G_m}$, and the output resistance, $\boldsymbol{R_o}$. The PI compensator introduces one pole, $\boldsymbol{\omega_{PI\_p}}$ composed of $\boldsymbol{R_o}$ and compensation capacitor $\boldsymbol{C_c}$, and one zero, $\boldsymbol{\omega_{PI\_z}}$ composed of the compensation network, $\boldsymbol{R_c}$ and $\boldsymbol{C_c}$.

Similarly, the transfer function, $\boldsymbol{A_{SEC}(s)}$ as shown in (20) contributed by the secondary modulator, is used to provide a low-bandwidth response to filter out the high-switching PWM signal according to the load current. Thus, the DC gain of the $\boldsymbol{A_{SEC}(s)}$ is inversely proportional to the load current and controlled by $\boldsymbol{I_{load(threshold)}}$.

$$A_{SEC}(s) = A_{SEC0} \cdot \left(\frac{I_{load(threshold)} - I_{load}}{I_{load(threshold)}} \right) \cdot \frac{1}{\left(1+\frac{s}{\omega_{SEC\_p1}}\right)\left(1+\frac{s}{\omega_{SEC\_p2}}\right)} \tag{20}$$

where $\omega_{SEC\_p1} = \frac{1}{R_{L1}C_{L1}}$, $\omega_{SEC\_p2} = \frac{1}{R_{L2}C_{L2}}$,

and A_{SEC0} is the low-frequency gain

The close-loop transfer function in the secondary modulator can be expressed as (21).

$$T_{SEC}(s) = k \cdot G_{vd}(s) \cdot A_{PRI}(s) \cdot A_{SEC}(s) \tag{21}$$

Therefore, the close-loop transfer function in dual modulation can be expressed as (22).

$$T_{(dual)}(s) = \left(\frac{I_{load}}{I_{load(threshold)}} \right) T_{PRI}(s) + T_{SEC}(s) \tag{22}$$

As the load decreases continuously, the contribution of the primary modulation becomes smaller than that of the secondary modulation. At very light loads, the secondary

modulator can take over the control authority.

In this study, the primary modulation is demonstrated as follows: The control duty can be expressed as (23) to include the results from the AC ripple detector and the error amplifier.

$$\hat{d} = \hat{d}_1 + \hat{d}_2 = \left(F_{m1}A_{PI} + F_{m2}B_{AC}\right)\cdot k \cdot \hat{v}_{out} \quad \text{where } k \text{ is the sensor gain} \tag{23}$$

Owing to the LC double poles, the AC ripple detector as a differentiator can introduce a low-frequency zero, ω_{AC}, with a time constant, C_dR_d, to increase the system stability. Thus, the transfer function, $B_{AC}(s)$, is shown in (24).

$$B_{AC}(s) \approx \frac{s}{\omega_{AC}} = sC_dR_d \tag{24}$$

In a steady state, the PWM comparator transfer functions F_{m1} and F_{m2} have the same value of Fm as defined in (25).

$$F_m = F_{m1} = F_{m2} \tag{25}$$

Thus, the output-to-duty transfer function can be derived as shown in (26). As expressed in (27), the system contains one single, low-frequency dominant pole, ω_{PI_p}, and two compensated zeros, $\omega_{zcomp1,2}$.

$$\frac{\hat{d}}{\hat{v}_{out}} = k \cdot F_m\left[A_{PRI}(s) + B_{AC}(s)\right] = kF_mG_mR_o\frac{\left(1+\frac{s}{\omega_{zcom1}}\right)\left(1+\frac{s}{\omega_{zcom2}}\right)}{\left(1+\frac{s}{\omega_{PI\_p}}\right)} \tag{26}$$

$$\text{where } \omega_{PI\_p} = \frac{1}{R_oC_c} \text{ and } \omega_{zcom1,2} = \frac{G_mR_c}{2C_dR_d}\left(1 \pm \sqrt{1-\frac{4C_dR_d}{G_mC_cR_c^2}}\right) \tag{27}$$

As a result, the close-loop transfer function can be expressed in (28), which contains two zeros and three poles. According to design parameters shown in Table V, the position of the three poles and the two zeros can guarantee system stability during the primary PWM

operation.

$$T_{PRI}(s) = kF_m G_{vd}(s)\left[A_{PRI}(s) + B_{AC}(s)\right]$$
$$\approx kF_m G_{vd0} G_m R_o \frac{\left(1+\frac{s}{\omega_{zcom1}}\right)\left(1+\frac{s}{\omega_{zcom2}}\right)}{\left[1+\frac{2\zeta}{\omega_O}s+\left(\frac{s}{\omega_O}\right)^2\right]\left(1+\frac{s}{\omega_{PI\_p}}\right)} \quad (28)$$

Table V: Design parameters of the proposed converter.

EA's G_m	*62.5 μA/V*		
Resistor	R_o=*90 MΩ*	R_c=*150 kΩ*	R_d=*5 MΩ*
Capacitor	C_c=*30 pF*	C_d=*2 pF*	
Three Poles	f_{PI_p}=*59 Hz*	f_{O1}=f_{O2}=*73 kHz*	
Two Zeros	f_{zcom1}=*57.7 kHz*	f_{zcom1}=*91.5 kHz*	

Fig. 19 depicts the analytic Bode plot of the primary modulator with the AC ripple detector. Expectedly, the phase margin is larger than 45 degrees since the pole-zero cancellation of the proposed AC ripple detection technique is achieved without using a large ESR.

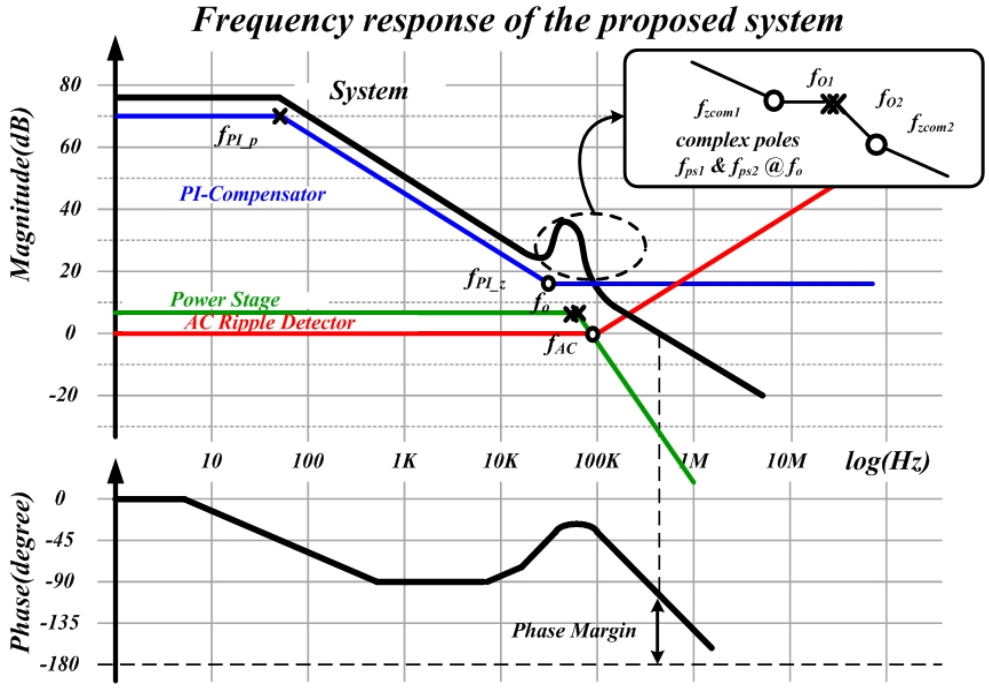


Fig. 19. Bode plot of the proposed converter system.

Chapter 4
Circuit Implementation

The architecture of the proposed buck converter has illustrated in Fig. 16. The converter is composed of a power stage, a feedback network, and the control stage including primary modulator and secondary modulator. The power stage contains a pair of power switches SW_P and SW_N, and an inductor L. Owing to high switching frequency, compact off chip inductor and filtering capacitor C_O can be used. Output voltage V_{OUT} is scaled down to V_{FB} by the voltage divider, composed of resistors R_{FB1} and R_{FB2}. The controller stage is utilized to turn on/off power switches SW_P and SW_N.

In normal operation, the primary modulator produces the original PWM pulse to regulate output voltage. The comparator CMP compares the output signal V_{EA} generated from the error amplifier EA, with the summation of the sensing signal V_S and the slope compensation signal V_{SAW} to decide system duty.

In light load condition, the secondary modulator generates the HFM pulse to combine with original PWM pulse. The LPD circuit generates V_{Load}, which stands for the load condition, V_{Load} is combined with the error signal V_{EA} to generate input control signal of HFM circuit, V_{Ctrl}, and HFM circuit produces the optimal HFM pulse (V_{HOP}) to modulate with original PWM pulse (V_{PRI}), the modulated control signal (V_{GATE}) can reduce the switching times of power switches to reduce the switching loss.

Furthermore, the primary modulator will shut down automatically in very light load or no load condition, and the secondary modulator can regulate the output voltage by itself to save much more efficiency.

The operation of the whole system is mentioned above. The operations of key sub-circuits in the control stage are explained in the following sections.

4.1 Hopping Frequency Modulator (HFM) Circuit

The HFM circuit, as shown in Fig. 20, can generate a load-dependent pulse, V_{HOP}, to modulate the primary PWM signal in order to reduce further the switching loss [24]. The signal V_{Ctrl}, is controlled by two variables, which are the error signal, V_{EA}, from the error amplifier and the DC load current signal, V_{Load}, from the LPD circuit. It can decide an adequate duty cycle in the HFM circuit once the dual modulation technique is triggered. The output voltage may have a large drop voltage caused by the small value of V_{Load}, which induces a large number of switches skipped. The drop voltage at the output raises the value of V_{EA} to constitute a negative feedback loop for increased system stability.

The charging current for the capacitor, C_1, is determined by the current signal I_C decided by the values of I_{IN} and I_{OUT} and expressed as (29).

$$I_C = I_{IN} - I_{OUT} = I_{IN} - \frac{V_{Ctrl}}{R_1} = \frac{C_1 \cdot \Delta V}{\Delta T} \tag{29}$$

I_{IN} defines the threshold current that switches the operation from the primary PWM to dual modulation. As load current decreases continuously, the system switches automatically to dual modulation; that is, load current is smaller than $I_{load(threshold)}$. The current I_{OUT} is converted from the signal V_{Ctrl} by the voltage-to-current (V-to-I) converter. The minimum value of V_{Ctrl} corresponds to the largest charging current for the C_1 that result in the shortest charging time. As a result, the duty of the HFM pulse can contain the longest duration at very light loads to reduce the switching frequency at the power switches.

The charge on the capacitor C_1 is reset by a hopping frequency signal, RST_{HOP}, generated by the frequency hopper in order to vary the hopping frequency, f_{HOP}, based on load current. Consequently, the f_{HOP} decreases and the duty cycle increases to reduce the switching numbers at the power MOSFETs when load current becomes light. Thus, efficiency can be improved. On the other hand, the HFM pulse is greatly decreased, and

small enough to have no effect on the high-switching PWM pulse during the primary PWM operation. Only the primary PWM operates to suppress output ripple.

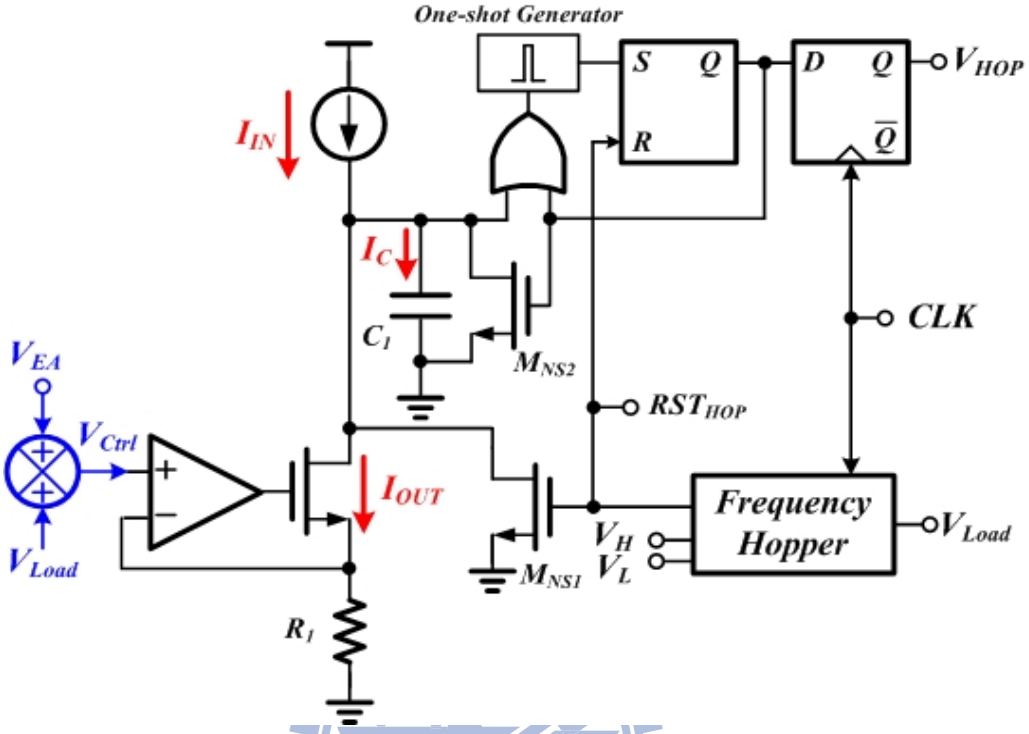


Fig. 20. The schematic of HFM circuit.

4.2 Frequency Hopper

The frequency hopper is used to generate a load-dependent hopping switching frequency for the HFM circuit. The load-dependent hopping switching frequency varies over a wide load range if the secondary starts to work from medium to very light-load condition.

As shown in Fig. 21, the V_{Load} is generated by the LPD circuit to determine the DC load current condition. The current signal I_L converted from the V_{Load} by the V-to-I converter is nearly equal to the charging current I_C, which is expressed as (30) and can determine the hopping frequency as shown in (31) due to the small current I_T. The frequency hopper can let the user design the desired frequency by adjusting of R_T and I_T.

$$I_C = I_L - I_T = \frac{V_{Load}}{R_T} - I_T \tag{30}$$

$$f_{HOP} = \frac{\frac{V_{Load}}{R_T} - I_T}{C_T \cdot (V_H - V_L)} \approx \frac{I_C}{C_T \cdot (V_H - V_L)} \tag{31}$$

Since the system has a primary high-switching frequency, f_{SW}, the clock synchronizer is used to synchronize the output signal RST_{HOP} with high-switching clock, CLK. It also can fix the pulse width of the signal RST_{HOP} for regular operation in the dual modulation technique compared with using the signal RST.

When load current changes from 1mA to 150 mA, the f_{HOP} varies from 70 kHz to 1 MHz. Meanwhile, the $f_{SW(dynamic)}$ can range from 70 kHz to 3 MHz. As a result, a lot of switching loss can be reduced to improve power conversion efficiency. In this design, the switching frequency reverts to high-switching operation of 5 MHz when load current is larger than $I_{load(threshold)}$, which is designed as 150 mA.

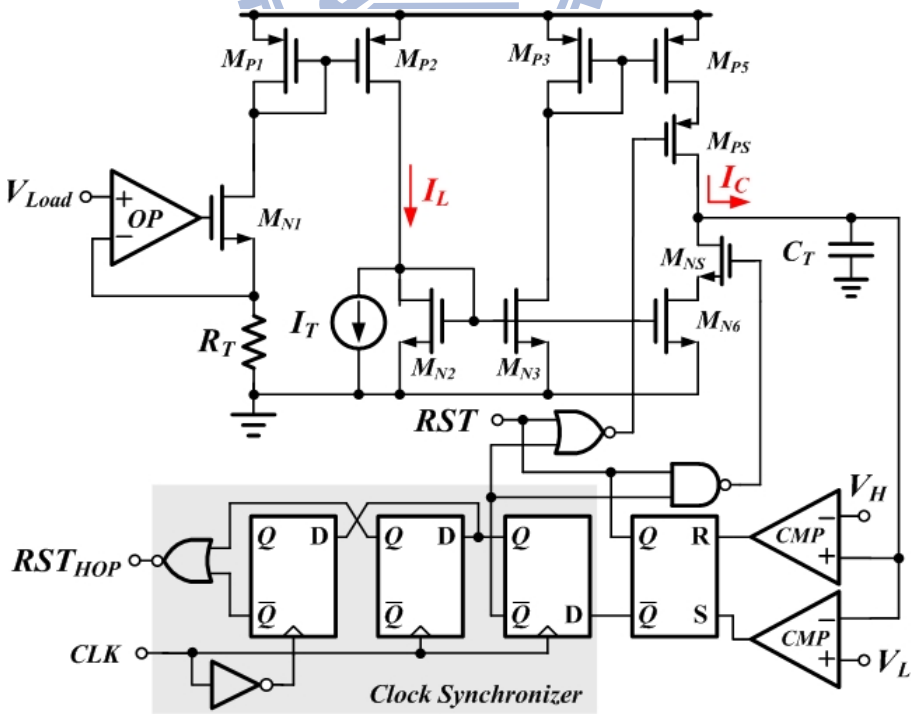


Fig. 21. The schematic of frequency hopper.

4.3 Loading Potential Detector (LPD) Circuit

The LPD circuit (Fig. 22) is used to generate the loading potential signal, V_{Load}, which is proportional to the DC load current [25]-[27].

The sensing transistor, M_{SEN}, with the aspect ratio much smaller than the power PMOSFET, SW_P, at the power stage, the virtual short-circuit characteristic of the operational amplifier can mirror the inductor current in the power P-type MOSFET to the sensing transistor. The sensing current can be scaled down to the transistor M_{P3} during the rising period. The sensing current I_{SEN} flows through the internal resistor R_{SEN} and is filtered by the low-pass filter to suppress the switching ripple in generating the loading potential signal V_{Load}.

The hysteretic comparator compares the output signal V_{Load} with the predefined threshold voltage V_{REF2}. When V_{Load} is smaller than V_{REF2} (i.e., the system is at very light loads), the hysteretic comparator triggers the signal, SET, from high to low. Specifically, to promote additional power saving, the primary modulator shuts down and the output voltage of the system is regulated only by the secondary modulator at very light loads.

Since the LPD circuit extracts the DC value of the load current, the bandwidth of the operational amplifier should not be too large to save power; that is, the selection of the operational amplifier can only be a simple one-stage structure with low quiescent current in order to save chip area and power consumption. Furthermore, the biasing current induces a minimum output sensing current even at no load condition, indicating a minimum value at the signal V_{Load}. As a result, the hopping frequency can be always kept higher than the acoustic frequency to address the noise issue.

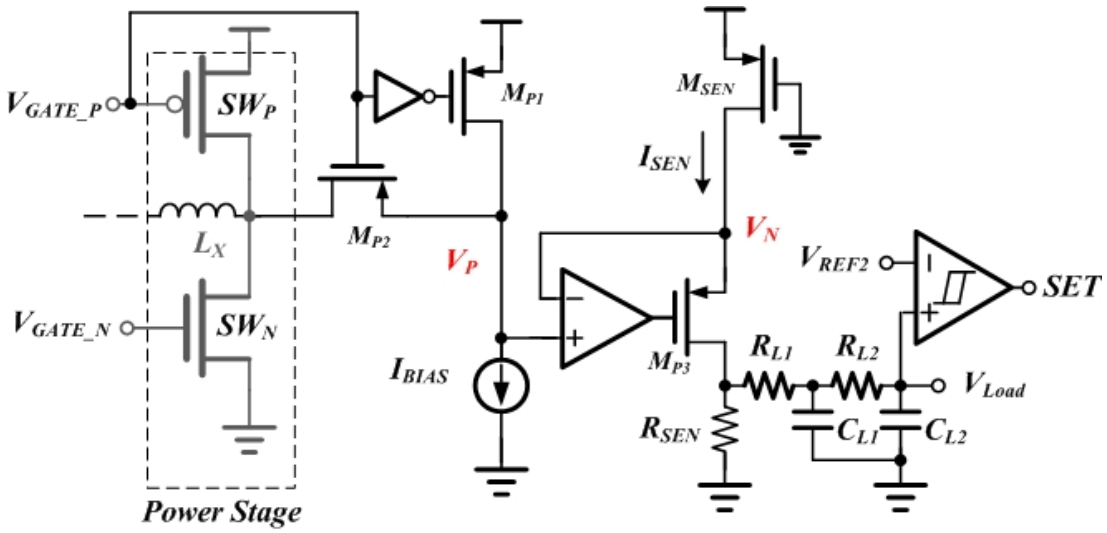


Fig. 22. The schematic of loading potential detector.

4.4 Voltage Adder

For detecting the optimal HFM pulse to modulate with original PWM signal, there should be a control signal contains the load condition information and error information of the error amplifier. The voltage adder is used to combine the error signal from error amplifier, V_{EA}, and loading signal from LPD circuit, V_{Load}, to produce the control signal, V_{Ctrl}, for the HFM circuit.

The schematic of the voltage adder is shown in Fig. 23 [28], it's composed of two *V-to-I converters* and a summing resistor, R_{SUM}. The *V-to-I converters* convert the input voltages V_{Ctrl} and V_{EA} into current information which are expressed as (32), and the currents are mirrored to the resistor R_{SUM} to produce output voltage V_{SUM}, which is expressed as (33).

$$I_{S1} = \frac{V_{Ctrl}}{R_{S1}} \quad , \quad I_{S2} = \frac{V_{EA}}{R_{S2}} \tag{32}$$

$$V_{SUM} = R_{SUM}\left(I_{S1} + I_{S1}\right) = R_{SUM}\left(\frac{V_{Ctrl}}{R_{S1}} + \frac{V_{EA}}{R_{S2}}\right)$$
$$= \frac{R_{SUM}}{R_S}\left(V_{Ctrl} + V_{\mathrm{EA}}\right) \quad \text{when} \quad R_{S1} = R_{S2} = R_S \tag{33}$$

Furthermore, the operational amplifier's bandwidth of the *V-to-I converters* can work as a low pass filter to filter high frequency noise.

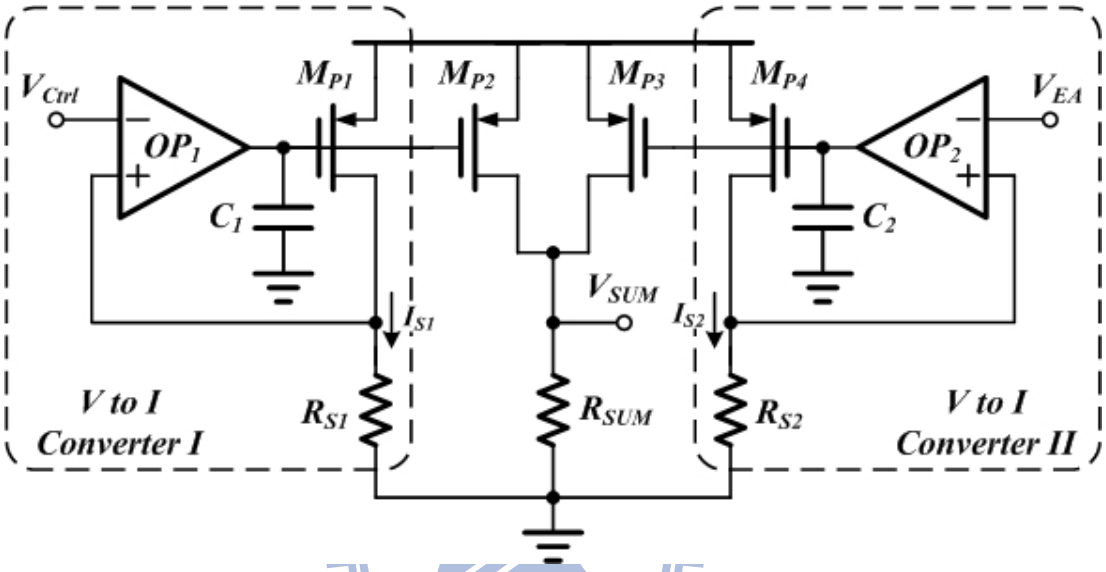


Fig. 23. The schematic of voltage adder.

4.5 AC Ripple Detector Circuit

The schematic of the AC ripple detector is shown in Fig. 24. Apart from its ability to determine the AC value of the inductor current, the AC ripple detector can also eliminate high-frequency noise due to ESL [29].

In time-domain, the high-speed voltage-controlled current-source (VCCS) circuit is used to differentiate the output feedback signal, $\boldsymbol{V_{FB}}$, to generate a low-frequency zero without the need of large compensation capacitor for reducing silicon area. Owing to the simple circuit structure, the bandwidth can be extended beyond that of conventional current sensing circuit using an operational amplifier. Thus, the $\boldsymbol{v_{FB}}$ is converted to a small-signal current $\boldsymbol{sC_d v_{FB}}$ to charge and discharge the capacitor. Before generating the sensing signal

V_s, the small-signal current is delivered to the ESL cancellation circuit to eliminate the ESL effect using a low-pass filter.

The signal of sC_dv_{FB} contains the AC inductor current, i_{AC}, and the high-switching noise generated by the ESL, in. After the operation of ESL cancellation circuit, the pure AC inductor current can be derived to modulate the primary modulator. Thus, the value of i_{AC} approximately equals to (34). $v_{FB(low\text{-}pass)}$ represents the value of v_{FB} after the low-pass filter.

$$i_{AC}(s) \approx skC_d v_{FB(low-pass)} \tag{34}$$

The sensing AC signal, V_s, can be received as shown in (35) by the sensing resistor R_d.

$$V_s(s) = skC_d R_d v_{FB(low-pass)} \tag{35}$$

Thus, the sensing signal can be produced correctly and rapidly under high-switching operation.

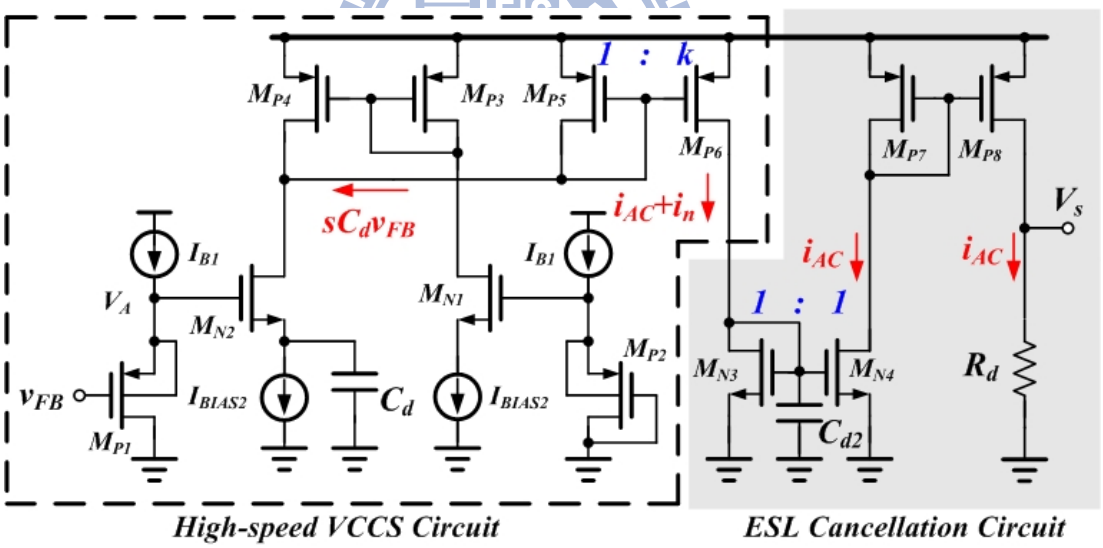


Fig. 24. The schematic of AC ripple detector.

Chapter 5
Experimental Results and Conclusion

In this Chapter, the test chip has been measured and the function works correctly. The experimental results are discussed and shown in section 5.1. Finally, the conclusion and future work are made in section 5.2 and section 5.3.

5.1 Experimental Results

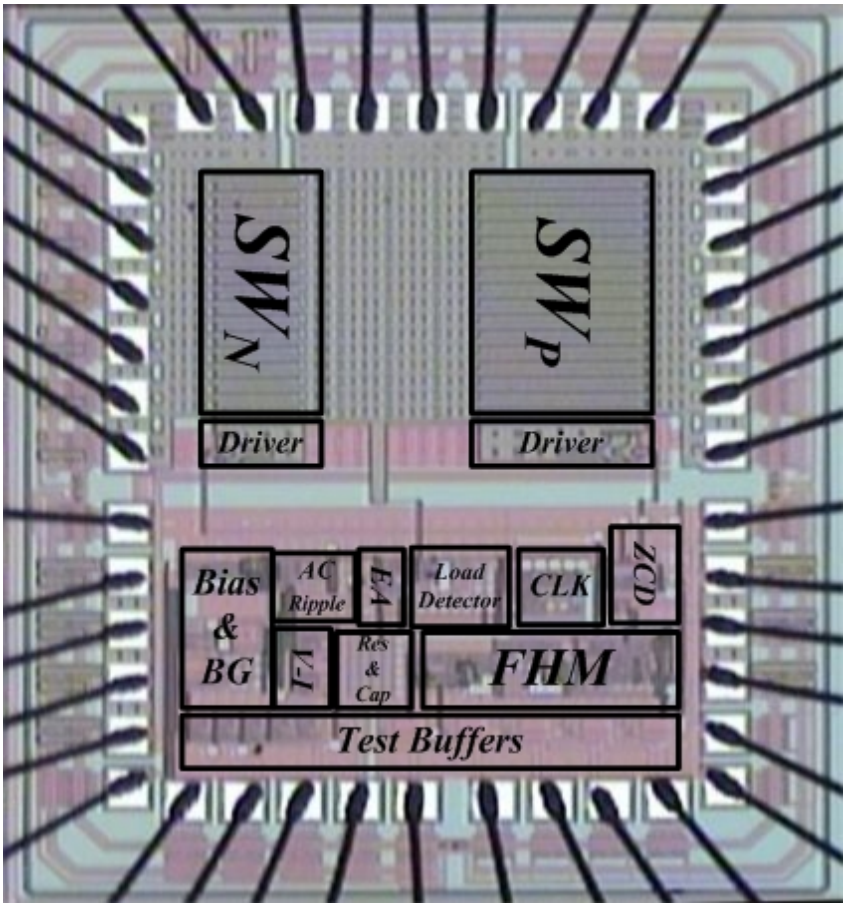


Fig. 25. The chip micrograph.

The proposed dual modulation technique high-switching buck converter is fabricated by TSMC 0.25μm CMOS process. The off-chip inductor and output capacitor are 1μH and 4.7μF, respectively. The switching frequency is 5MHz in primary modulation and the

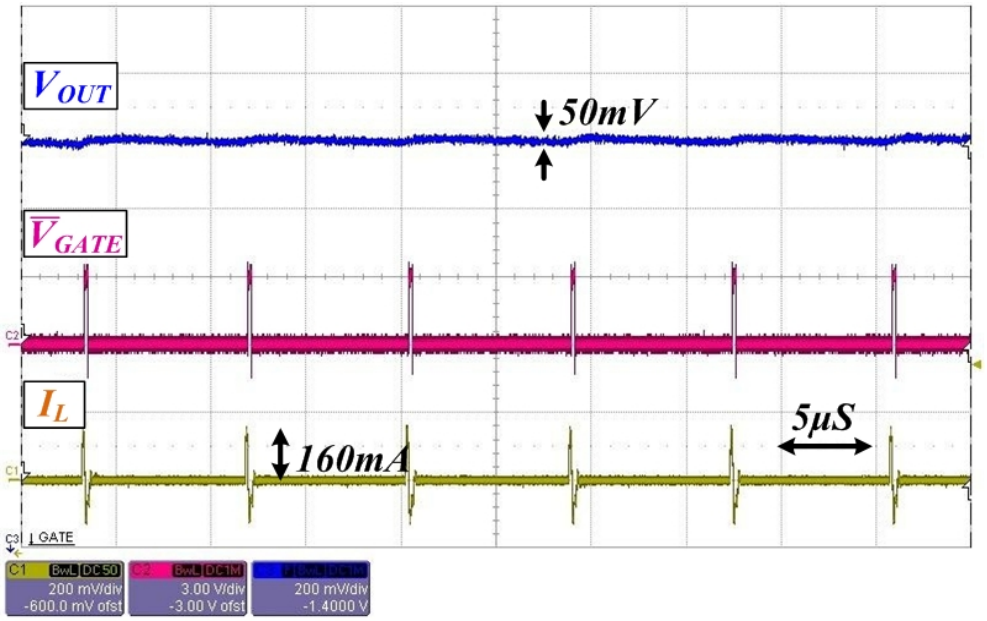
output voltage V_{OUT} is 1.8V. The chip micrograph is shown in Fig. 25 and the chip area is about 1200μm × 1150μm including the test pads. And the specification of the converter is listed in Table VI.

Table VI: Design parameters.

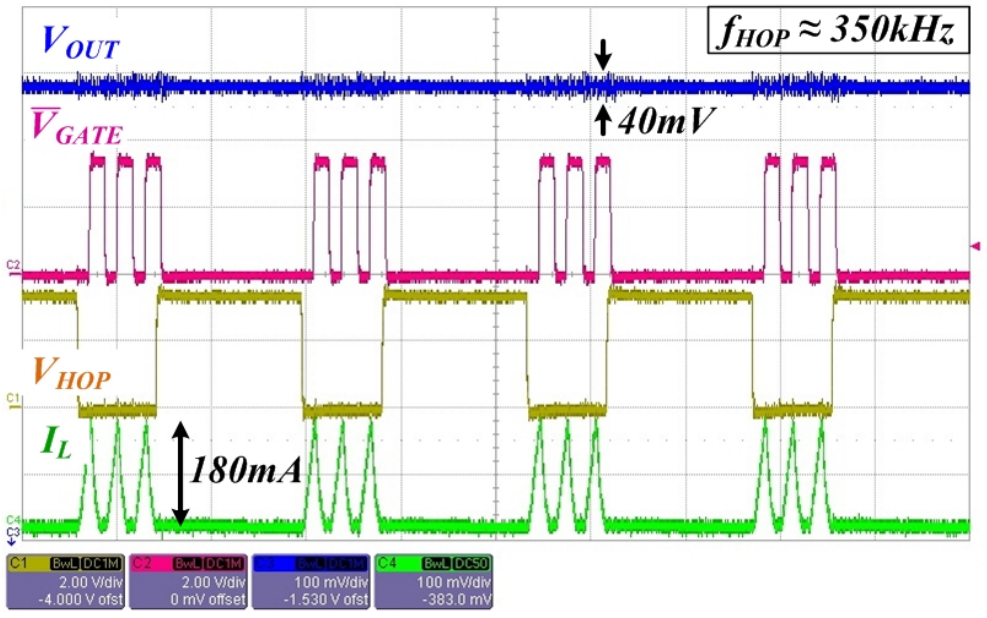
Technology	TSMC 0.25μm CMOS
Proposed die area (with test pads)	1700μm × 2000μm
Supply variation (V_{IN})	3–4 5V
Output voltage (V_{OUT})	1.8V
Switching frequency (f_{SW})	5MHz
Maximum output voltage ripple	50mV
Undershoot / Overshoot (150mA to 450mA)/(450mA to 150mA)	20mV / 15mV
Undershoot / Overshoot (1mA to 500mA)/(500mA to 1mA)	60mV / 60mV
Recovery time 150mA to 450mA/450mA to 150mA	2.5μs / 3μs
Recovery time 1mA to 500mA / 500mA to 1mA	14μs / 15μs
Inductor (L)	1μH
Output capacitor (C_O)	4.7μF
Secondary modulation range	1–10mA
Dual modulation range	10–150mA
Primary modulation range	150–600mA

5.1.1 Performance of Steady State

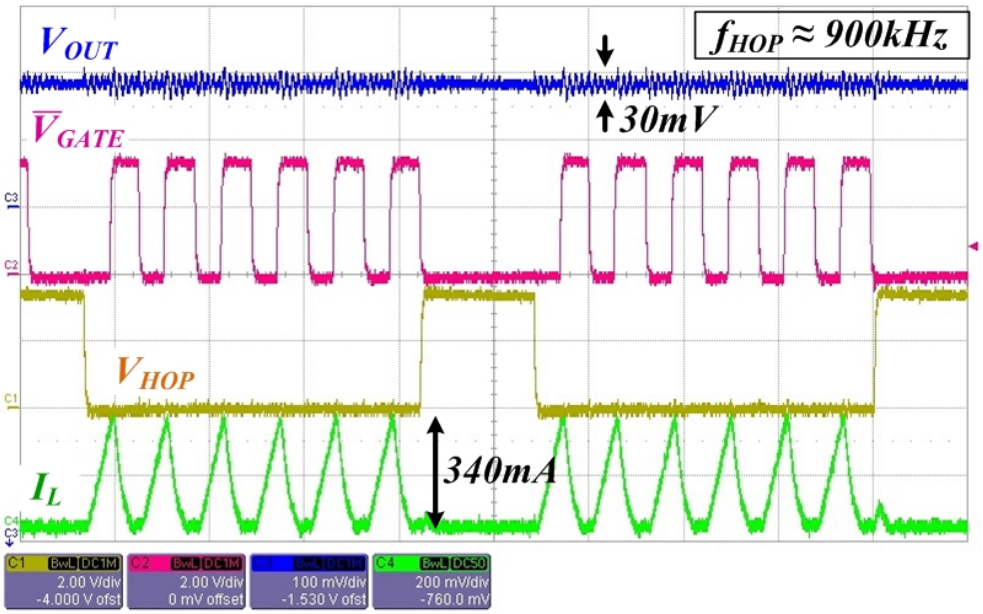
Fig. 26 shows the output waveforms at different load current conditions when the converter enables the dual modulation technique. Figs. 26(a)–(c) reveal how the HFM circuit can adjust the switching frequency dynamically according to load current. Fig. 26(d) shows the system correctly reverts to the PWM mode when load current is raised higher than $I_{load(threshold)}$.



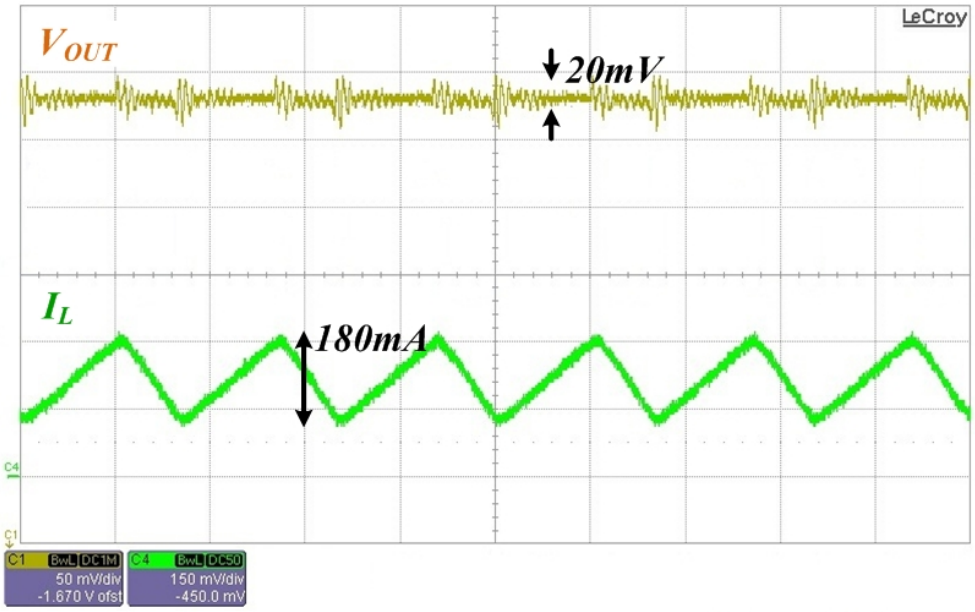
(a)



(b)



(c)

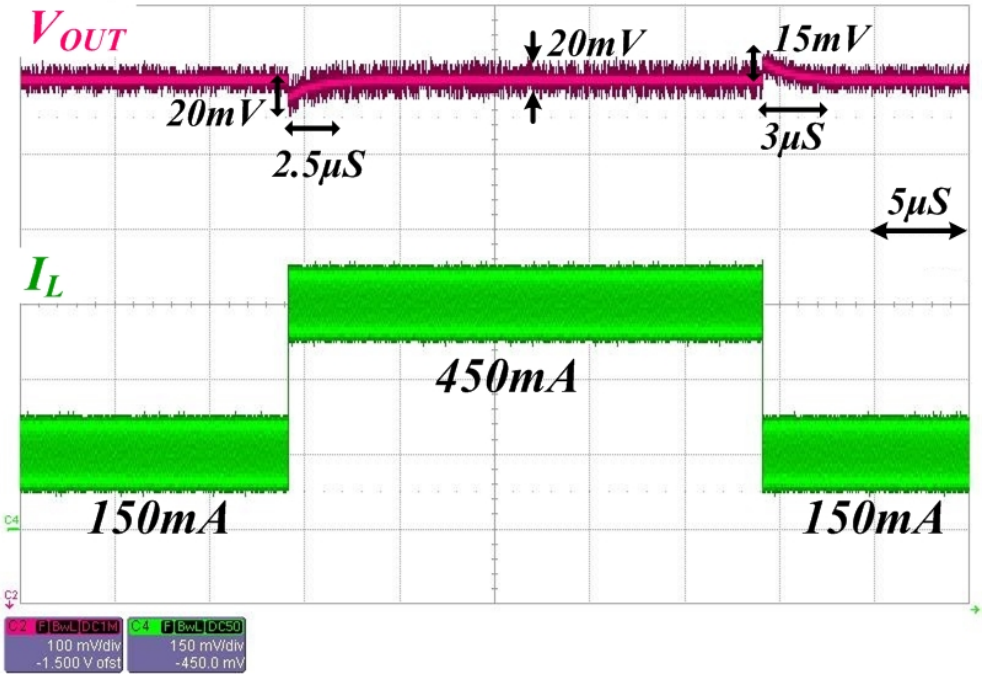


(d)

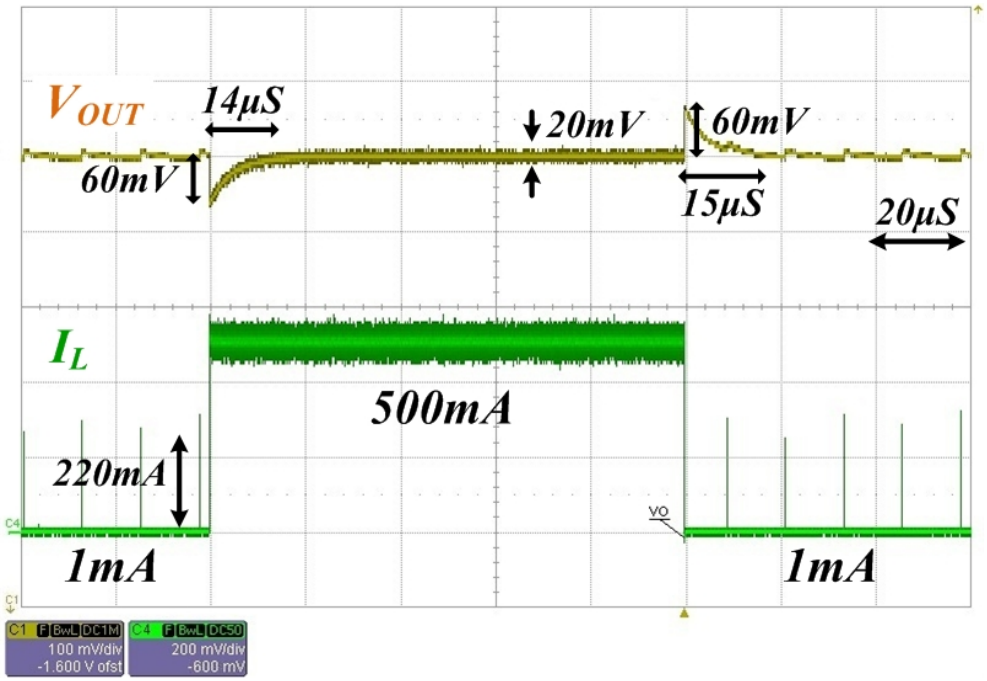
Fig. 26. Waveforms of the output voltage and inductor current at different load current conditions. (a) I_{Load} =5 mA. (b) I_{Load} =20 mA. (c) I_{Load} =110 mA (d) I_{Load} =220 mA.

5.1.2 Performance of Transient Response

The waveforms of the output voltage and the inductor current during load transient response are shown in Fig. 27. Fig 27(a) shows the recovery times are about 2.5μs and 3μs when load current changes from 150mA to 450 mA and vice versa, respectively. And the load current changes from 1mA to 500mA and vice versa as shown in Fig. 27(b). This demonstrates the system stability is controlled by the dual modulation system with the AC ripple detector.



(a)

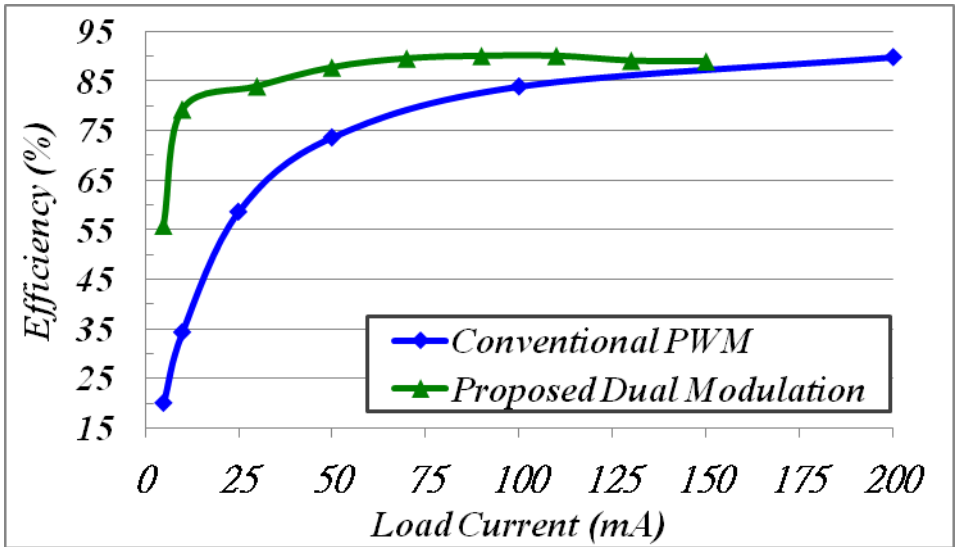


(b)

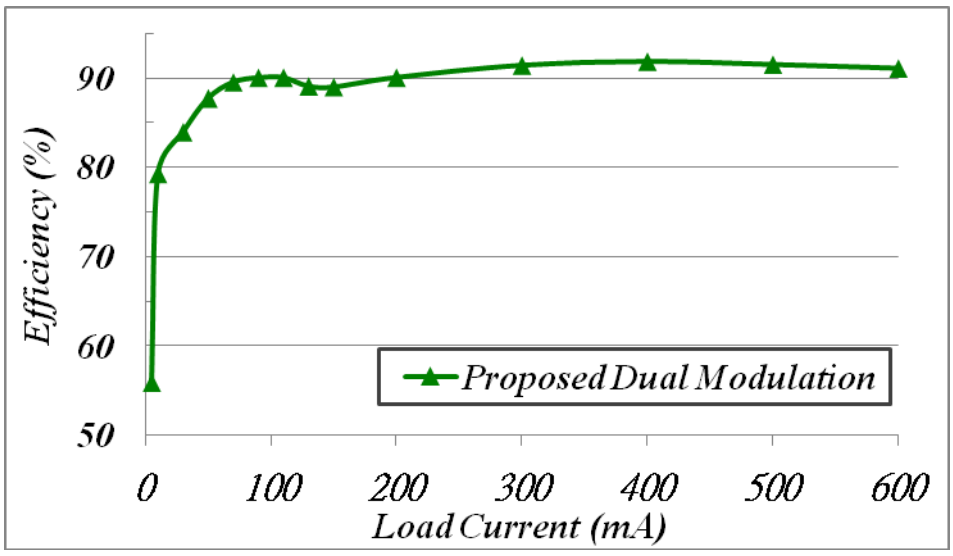
Fig. 27. Load transient response. (a) Load current steps from 150mA to 450mA or vice versa. (b) Load current steps from 1mA to 500mA or vice versa. The modulation rapidly switches between the secondary and the primary modulation techniques.

5.1.3 System Efficiency Comparison

Fig. 28(a) shows the comparison in efficiency between the conventional PWM operation and the proposed dual modulation technique. The number of switching signal at the gate of the power MOSFETs can be effectively reduced. As a result, the maximum efficiency improvement is about 45% at load current=10mA. The efficiency of the proposed converter over a wide load range is shown in Fig. 28(b). The level of efficiency dropped slightly at the mode transition within allowable specification. However, this demonstrates that efficiency can be always kept high by using the dual modulation technique.



(a)



(b)

Fig. 28. (a) Efficiency comparison between the original PWM operation and the proposed dual modulation technique. (b) Efficiency of the proposed converter over a wide range of load current.

5.2 Conclusion

The proposed dual modulation technique can enhance power conversion efficiency within the allowable output voltage ripple for the supply of system-on-a-chip applications. The proposed AC ripple detector can alleviate the worsening switching noise caused by parasitic resistance and inductance due to high-switching operation. In addition, the switching frequency can be kept higher than the acoustic frequency to avoid noisy sound in the LPD circuit. Experiment results show that the inductor size can be reduced to about 1μH with the switching of 5MHz. The load transient response time is smaller than 3μs when load current changes from 150 to 450mA or vice versa. Furthermore, the power efficiency can be always kept higher than 85% over a wide load current range. It ensures light efficiency can be raised about 45% above that of the conventional design.

5.3 Future Work

In this theory, we present a high-switching converter operating at 5MHz switching frequency, the inductor size is reduced to 1μH that can be integrated into chip successfully. In our design, the 5MHz switching frequency is hard to increase because the bandwidths of the sub-circuits in the controller have reached the limits. That's to say, how to speed up the sub-circuits' operating time, to raise the switching frequency much more could be the next topic. The higher switching frequency also makes the size of output capacitor reduced, once the output capacitor can be integrated into chip, we can present a fully-integrated DC-DC converter.

References

[1] D. Maksimovic, “Power management model and implementation of power management ICs for next generation wireless applications,” *Tutorial presented at the International Conference on Circuits and System (ISCAS)*, 2002.

[2] Pedram, M.; Qing Wu, “Design considerations for battery-powered electronics,” *Design Automation Conference*, 1999. Proceedings. 36th, 21-25, pp. 861-866, June 1999.

[3] “Technical Review of Low Dropout Voltage Regulator Operation and Performance,” Texas Instruments Incorporated, Dallas, TX, Aug. 1999.

[4] P. Favrat, P. Deval and M. J. Declercq, ”A high-efficiency CMOS voltage doubler” *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.

[5] Abraham I. Pressman, “SWITCHING POWER SUPPLY DESIGN,” McGraw-Hill, 1991.

[6] Robert W. Erickson and Dragan Maksimovic, *Fundamentals of Power Electronics, 2nd ed.*, pp. 92-101, Norwell, MA: Kluwer Academic Publishers, 2001.

[7] Hong-Wei Huang, Ke-Horng Chen, and Sy-Yen Kuo, “Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-on-chip Applications,” *IEEE Journal of Solid-State Circuits*, pp. 2451-2465, Nov. 2007.

[8] Chi-Lin Chen, Wei-Lun Hsieh, Wei-Jen Lai, Ke-Horng Chen and Ching-Sung Wang, "A new PWM/PFM control technique for improving efficiency over wide load range," *IEEE International Conference on Electronics, Circuits and Systems*, pp. 962-965, Sept. 2008

[9] Ke-Horng Chen, Chia-Jung Chang, and Ter-Hsing Liu, “Bidirectional Current-Mode Capacitor Multipliers for On-Chip Compensation,” *IEEE Transaction on Power Electronics*, pp. 180-188, Jan. 2008.

[10] Song Qu, “Modeling and Design Considerations of V^2 Controlled Buck Regulator,”

IEEE Apply Power Electron. Conf. Exp., pp. 507-513, Mar. 2001.

[11] Jian Sun, "Characterization and Performance Comparison of Ripple-based Control for Voltage Regulator Modules," *IEEE Trans. Power Electronics*, vol. 21, no. 2, pp. 346-353, Mar. 2006.

[12] Cheung Fai Lee, Philip K. T. "A Monolithic Current-Mode CMOS DC-DC Converter with On-Chip Current-Sensing Technique," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 3-13, Jan. 2004.

[13] Chi Yat Leung, Philip K.T. Mok, "A 1-V Integrated Current-Mode Boost Converter in Standard 3.3/5-V CMOS Technologies," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 11, pp. 2265-2274, Nov. 2005.

[14] Robert W. Erickson and Dragan Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Norwell, MA: Kluwer Academic Publishers, 2001.

[15] Cheung Fai Lee, Philip K. T. "A Monolithic Current-Mode CMOS DC-DC Converter with On-Chip Current-Sensing Technique," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 3-13, Jan. 2004.

[16] Ding Ge, Zhiliang Chen, "On-chip boost DC-DC converter in color OLED driver & controller ICs for mobile application," *IEEE ASICON*, vol. 1, pp. 459–463, Oct. 2005.

[17] Chi-Lin Chen, Wei-Lun Hsieh, Han-Hsiang Huang, Ke-Horng Chen, "Fast Mode-Switching Technique in Hybrid-Mode Operation," *The 51st Midwest Symposium on Circuits and Systems,* pp. 9-12, Aug. 2008.

[18] Peter Hazucha, Gerhard Schrom, Jaehong Hahn, Bradley A. Bloechel, Paul Hack, Gregory E. Dermer, Siva Narendra, Donald Gardner, Tanay Karnik, Vivek De, Shekhar Borkar," A 233-MHz 80%–87% Efficient Four-Phase DC–DC Converter Utilizing Air-Core Inductors on Package," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 838-845, April. 2005.

[19] Hollinger, W. and Punzenberger, M., "An Asynchronous 1.8MHz DC/DC Boost

Converter Implemented in the Current Domain for Cellular Phone Lighting Management," *IEEE ESSCIRC*, pp. 528-531, Sep. 2006.

[20] Jen-Chieh Tsai, Tsung-Ying Huang, Wang-Wei Lai, and Ke-Horng Chen, "Dual Modulation Technique for High Efficiency in High Switching Buck Converters Over a Wide Load Range," *IEEE International Symposium on Circuits and Systems*, pp. 3709-3712, May 2010.

[21] Jian Li and Fred C. Lee, "Modeling of V^2 Current-Mode Control," *IEEE Applied Power Electronics Conference and Exposition*, pp. 298-304, Feb. 2009.

[22] Yu-Huei Lee, Shih-Jung Wang, and Ke-Horng Chen, "Quadratic Differential and Integration Technique in V^2 Control Buck Converter with Small ESR Capacitor," *IEEE Transaction on Power Electronics*, pp. 829-838, Apr. 2010.

[23] Behzad Razavi, *Design of Analog CMOS Integrated Circuits, 1st ed.*, pp. 345–373, 2000.

[24] Albert M. Wu, Steven M. Piekiewiez, "Switched converter with variable peak current and variable off-time control," *United States Patent*, Pat. No. 7528587, May, 2009.

[25] Hylas Y.H Lam, Wing-Hung Ki and Dongsheng Ma, "Loop gain analysis and development of high-speed high-accuracy current sensors for switching converters," *IEEE International Symposium on Circuits and Systems*, pp. 828-831, May. 2004.

[26] Chi Yat Leung, Philip K. T. Mok, Ka Nang Leung, Mansun Chan "An Integrated CMOS Current-Sensing Circuit for Low-Voltage Current-Mode Buck Regulator," *IEEE Trans. Circuits and System*. vol. 52, no. 7, July 2005.

[27] Chi-Lin Chen, Wei-Jen Lai, Wei-Lun Hsieh, and Ke-Horng Chen, "A High-Speed and Precise Current Sensing Circuit with Bulk Control (CCB) Technique," *IEEE International Conference on Electronics, Circuits and Systems*, pp. 283-287, Sep. 2008.

[28] Hong-Wei Huang, Wei-Lun Hsieh, and Ke-Horng Chen, "Programmable Voltage-to-Current Converter with Linear Voltage Control Resistor," *IEEE International Symposium on Circuits and Systems*, pp. 2310-2313, May. 2008.

[29] Cheung Fai Lee and Philip K.T.Mok, ”A Monolithic Current-Mode CMOS Converter With On-Chip Current-Sensing Technique,” *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, Jan. 2004.