國立交通大學

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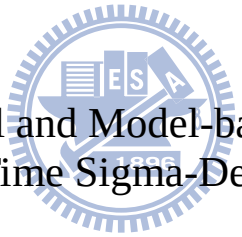
碩士論文

雜訊相依模型與模組設計最佳化運用在

離散時間積分三角類比數位轉換器



Noise Correlation Model and Model-based Design Optimization for Discrete-Time Sigma-Delta Modulators

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中 華 民 國 九 十 九 年 九 月

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摘要

傳統高階積分三角調變器的設計上，主要是依賴行為模擬的方法。然而此方法相當耗時。本論文是第一個提出使用模組化設計的方法去設計積分三角調變器。在速度上，使用模組化設計的方法將會比使用行為模擬的方法快上萬倍。由於先前非理想雜訊以及失真模型的不完備，模組化設計的方法一直無法真正的去實現。如今，由於積分器充放電雜訊模型以及放大器非線性直流增益諧波失真模型的推出，使得模組化設計方法得以實現。然而，使用模組化設計方法將會遭遇到雜訊相依的問題；本論文將會提出雜訊相依模型以便解決這個問題。除此之外，本論文也同時提出了積分三角調變器最佳化設計流程。對照於一篇積分三角調變器設計實例，模組化積分三角調變器最佳化設計將可以使用更短的時間去達到更高的訊號對雜訊以及失真比，同時降低積分三角調變器的功率消耗。

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ABSTRACT

The conventional high-level SDM synthesis is mainly based on behavior simulation which is very time-consuming. This thesis is the first one in the literature to propose model-based SDM synthesis. Model-based method can be at the order of 10^4 times faster than simulation-based method, but it is never realized before due to the incompleteness of non-ideality models. The recent establishment of settling noise model [18] and OTA distortion model [17] facilitates model-based SDM designs. Nonetheless, new problem associated with model-based method arises, notably correlation between noises. Noise correlation models here are derived. In addition, a SDM design optimization scheme is proposed, which incorporates a comprehensive power consumption model. This model-based optimization is tested against a published SDM design, achieving higher SNDR and lower power results in a much shorter design time.

誌謝 Acknowledgment

我要將此論文獻給

我親愛的母親-許錦碧 女士

最疼我的父親-盛景徽 先生

若沒有他們，我不可能有機會完成此篇論文，並且從交通大學碩士班畢業。除此之外, 必須感謝指導教授陳福川博士兩年來嚴格的督促與指導，讓我學會做研究的方法與心態。另外，也要感謝口試委員廖德誠教授、趙昌博教授與洪浩喬教授對本篇論文所給予的建議與指導。

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List of Symbols

Symbols

Physical

K	Boltzmann's constant
T	Absolute temperature

Definitions

σ_{cap}	Standard deviation of unit capacitance
σ_{jit}	Standard deviation of clock jitter
a_i	Gain coefficient of i th integrator
A_0	OTA finite DC-gain
A_{in}	Amplitude of input signal
B	Number of bits in the quantizer
C_C	Compensation capacitor
$C_{D,eq}$	DWA equivalent capacitor
C_I	Integrating capacitor
C_L	OTA Load capacitor
C_S	Sampling capacitor
C_{Switch}	Switch parasitic capacitor
C_u	Unit feedback capacitor
Erf	Error function
f	Feedback factor
f_B	Signal bandwidth
f_{in}	Input signal frequency
f_S	Sampling Frequency
g_m	OTA transconductance
n	Order of the sigma-delta modulator
N	Quantizer levels
R_{Switch}	Switch on-resistance
V_{LSB}	Quantizer step size
V_{OS}	OTA maximum output swing
V_{ref}	Reference voltage of the quantizer
V_S	Input signal plus feedback DAC signal

Abbreviations

ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor

DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DR	Dynamic Range
DWA	Data Weighted Averaging
FFT	Fast Fourier Transform
FOM	Figures of Merit
GBW	OTA Gain Bandwidth
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
SC	Switched Capacitor
SNDR	Signal to Noise plus Distortion Ratio
SNR	Signal to Noise Ratio
SR	OTA Slew Rate

1
Introduction

1.1 Current Status and Background

Sigma-Delta ADCs have become popular for high-resolution medium-to-low-speed applications such as digital audio [1-2], voice codec, and DSP chip. Recently, Sigma-Delta ADCs have been applied to higher bandwidth signals, and low power designs are frequently emphasized. For example, in xDSL [3-4] applications, signals up to several MHz must be handled. Since significantly increasing the sampling rate is difficult, designer either seeks to increase the order or the cascade stages [5-6], or employ multi-bit quantization [7-8], or both, in order to achieve the required dynamic range (DR). DAC linearity can be improved due to process technology advances, and it makes the multi-bit architecture more popular. However, Sigma-Delta Modulator (SDM) design is a complex and time consuming process because many coupled design parameters must be determined. Coming up with an acceptable design is very difficult with increasing design specification demands, previously described. Even an acceptable design may not be the best one. For this reason, we propose an optimization approach to increase automation and reduce complexity in the SDM design.

1.2 Motivation and Aims

To propose the design optimization for many SDM structures, we need a complete set of important non-ideality models and a power consumption model. Some issues concerning SDM noises and errors modeling appeared in [1-2] [9]. The SDM performance is usually expressed in terms of signal to noise ratio (SNR) and signal to noise plus distortion ratio (SNDR). Circuit designers must take into consideration of non-idealities, and decide design parameters to meet the desired specifications. A SDM design optimization procedure

proposed in [10] could meet design specifications while minimizing power consumption. However, it didn't consider nonlinear distortions, so that the effectiveness of the proposed design optimization is limited. In this work, we discuss all the important noise and distortion models into the optimization process in order to achieve more reliable designs.

Currently, the major approaches for SDM high-level optimization design was using MATLAB SIMULINK and related power models while simulated with annealing or generic algorithm [11-12] to find an optimal design parameter set. Although they used different algorithm to reduce the searching time, it still spent much time in behavior simulation. Besides, in existing approaches, the optimization result can't indicate the magnitude of each noise and distortion power, hence designer is hard to adjust design parameters. Differing with these approaches which employ behavioral simulators to explore the design space finding out the optimal set of SDM architecture and design parameters, we proposed an optimization design approach for SDM based on analytic all typical architecture noise, distortion, and power consumption with general math models. So that our approach, namely the model-based SDM design, can explicitly generate each noise power and distortion power after optimization is performed. Designer can obtain design parameters they want and know how to correct the result. More importantly, our design method need not behavior simulation, so the simulation time not depends on system clock cycles, but relates to CPU clock. It will be much faster than other optimization design approaches based on behavioral simulators. Nonetheless, a new problem associated with model-based method surface, notably the correlation problem. The correlation issue is due to dependency between non-ideality models. In this thesis, we establish models to compute correlation powers. We also establish a SDM power model which is much more comprehensive and involves more design parameters than the model used in [11].

In the end, we propose an optimization algorithm based on analytical models of noise, distortion, and power consumption. This algorithm searches the SDM design parameter

space to find out a design parameter set which meets design specs in terms of SNR or SNDR while keeping minimum power consumption.

1.3 Organization

This work is organized as follows. In Chapter 2, we discuss all the important noise and distortion models in SDM. In Chapter 3, the correlation issue for each SDM noise would be discussed. In Chapter 4, advantages of model-based SDM design are presented. In Chapter 5, the SDM power consumption is derived. In Chapter 6, we would propose a design optimization scheme, and use a published design case [3] to demonstrate its accuracy and practicability. Conclusion and future works are presented in Chapter 7.

2

SDM Noise Power and Distortion Power Models

Model-based high-level SDM design employs only mathematical models. In this chapter, we will first check about the availability of noise and distortion models against all non-idealities in SDM. These models are functions of design parameters. Modification to existing models will be made wherever needed. The models discussed here are for the popular switch-capacitor single-loop 2nd-order SDM structure shown in Fig. 2.1.

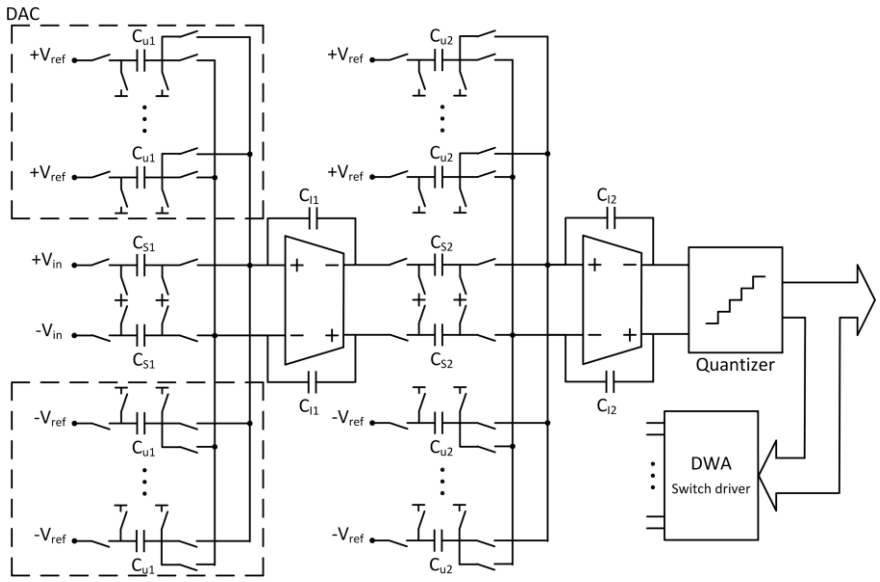


Fig. 2.1: Schematic of SC single-loop 2nd-order SDM

For SC single-loop 2nd-order SDM shown in Fig. 2.1, major circuit non-idealities are listed below:

1) Switches non-idealities;
2) Capacitors non-idealities;
3) Finite and nonlinear DC-gain;

4) Bandwidth and slew rate;

5) OTA noises;

6) Clock jitter effect;

7) Comparators;

8) Multi-bit DAC non-idealities.

The non-idealities of (1) - (5) are related to integrators. The non-idealities of (6) - (8) are from outside of integrators. In the following, noise and distortion power models related to each of eight non-idealities are discussed.

2.1 Switch Non-idealities

2.1.1 Switch Thermal Noise Power Model ($P_{Switch\_thermal}$)

$P_{Switch\_thermal}$ [13] [14] is from switches before C_u and C_S. The PSD of switch thermal noise at SDM output is derived as $(8KT)/C_S$. Therefore, the in-band switch thermal noise power is

$$P_{Switch\_thermal} = \int_{-f_B}^{f_B} \frac{8KT}{C_S} df = \frac{1}{OSR} \frac{8KT}{C_S} \tag{2.1}$$

2.1.2 Nonlinear Switch on-resistance Distortion Power Model ($P_{Switch\_distortion}$)

The switch on-resistance is nonlinear because its value depends on input signal. The SDM output distortion power $P_{Switch\_distortion}$ can be obtained from [15].

2.1.3 Clock-Feedthrough

The clock-feedthrough is caused by the charge of the gate-to-source capacitors of the switch that is injected to the sampling capacitor when switch turns off. This error can be attenuated by fully differential integrator [16].

2.1.4 Charge Injection

Charge injection is due to the charge of mobile channel injected to the sampling

capacitor when the switch turns off. This error can be solved by widely used circuit technology [16].

2.2 Capacitors Non-idealities

2.2.1 Capacitor Mismatch Noise Power Model ($P_{Cap\_mismatch}$)

Capacitor mismatch can alter integrator gain from its nominal value, resulting in SDM output noise power $P_{Cap\_mismatch}$ [14].

2.2.2 Capacitor Nonlinearity Distortion Power Model ($P_{Cap\_distortion}$)

The capacitor C_S introduces harmonic distortion because its capacitance depends on the input signal. The output distortion power $P_{Cap\_distortion}$ is derived in [14] under the assumption that the gain of the second stage equals to one.

2.3 Finite and Nonlinear DC-gain

2.3.1 Finite DC-gain Noise Power Model ($P_{Finite\_DC\text{-}gain}$)

Finite DC-gain affects the noise transfer function, resulting SDM output noise power $P_{Finite\_DC\text{-}gain}$ [14].

2.3.2 Nonlinear DC-gain Distortion Power Model ($P_{DC\text{-}gain\_distortion}$)

OTA DC-gain is nonlinear because it varies with integrator output voltage. The output distortion power $P_{DC\text{-}gain\_distortion}$ can be obtained from [17].

2.4 Bandwidth and Slew-Rate

2.4.1 Settling Noise Power Model ($P_{Settling\_noise}$)

The limited integrator bandwidth and slew-rate make the voltage charge and discharge incomplete at integrator output, which causes SDM output noise power $P_{Settling\_noise}$ [18].

2.4.2 Slew-Rate Distortion Power Model ($P_{Settling\_distortion}$)

If input signal of integrator is so large that it exceeds the integrator slew-rate limitation,

a dependency of the settling error on its input is created, which results slew-rate distortion. The output distortion power $P_{Settling\_distortion}$ can be obtained from [14].

2.5 OTA Noises

2.5.1 OTA Thermal Noise Power Model ($P_{OTA\_thermal}$)

The OTA thermal noise originates from the OTA MOSFET non-idealities. Form the input-referred noise PSD V_{nOTA}^2 [14] [20], the in-band OTA thermal noise power at SDM output can be derived as

$$P_{OTA\_thermal} \cong \frac{1}{a_1^2 OSR}\int_0^{\infty} V_{nOTA}^2 \cdot \left(\left|H_{samp}(f)\right|^2 + \left|H_{int}(f)\right|^2\right) df \qquad (2.2)$$

where a_1 donates the first integrator gain, and $H_{samp}(f)$ and $H_{int}(f)$ are the transfer functions from noise source to integrator output in sampling phase and integration phase, respectively.

2.5.2 Flicker (1/f) Noise Power Model ($P_{OTA\_flicker}$)

The flicker noise also originates from the transistor non-idealities of OTA. The output noise power $P_{OTA\_flicker}$ can be obtained from [20].

2.5.3 Reference Circuit Noise Power Model (P_{Ref_noise})

Reference circuit noise usually contains OTA thermal noise and flicker noise, appearing at reference voltage of DAC circuit in Fig. 2.1. The output noise power can be obtained from [13] [20].

2.6 Clock Jitter Effect (P_{Jitter_noise})

The clock jitter noise originates from the sampling phase, resulting in non-uniform sampling of converter input signal. The noise power P_{Jitter_noise} can be obtained from [1].

2.7 Comparator Hysteresis($P_{Hysteresis}$)

The comparator hysteresis is defined as the minimum overdrive to change the

comparator's output, which leads to a loss of performance of SDM, and the noise power $P_{Hysteresis}$ can be obtained from [1].

2.8 Multi-bit DAC Non-idealities

2.8.1 DAC Noise Power Model (P_{DAC_noise})

The DAC noise originates from the capacitance of C_u mismatch, and can be obtained from [13].

2.8.2 DAC Distortion Power Model ($P_{DAC\_distortion}$)

The DAC is nonlinear because the transfer function of DAC depends on the capacitance of C_u. It causes DAC distortion.

3

SNDR Generation in Model-Based SDM Designs

The SDM design spec is typically given in terms of SNDR. SNDR is defined as

$$SNDR = \frac{P_S}{P_N + P_D} \tag{3.1}$$

where P_S represents the signal power, P_N the total noise power and P_D the total distortion power, respectively. In simulation-based SDM designs, P_N and P_D are generated from behavior simulations. In model-based SDM designs, P_N and P_D are computed by summing up each SDM output noise and distortion power models described in Chapter 2. However, there is one issue associated with the computation of P_N and P_D; i.e., the correlation problem. The direct sum up of noise powers and distortion powers would work only when the SDM output noises and distortions are independent. Indeed, correlations between noises and distortions do exist, and they have to be considered in the computation of P_N and P_D. In this chapter, P_N and P_D are defined as

$$\begin{aligned} P_N = {} & P_{Modified\_quantization\_noise} + P_{Switch\_thermal} + P_{OTA\_thermal} + P_{Jitter\_noise} \\ & + P_{DAC\_noise} + P_{Settling\_noise} \end{aligned} \tag{3.2}$$

and

$$P_D = P_{DC\text{-}gain\_distortion} + P_{DAC\_distortion} \tag{3.3}$$

Since finite DC-gain may produce changes in noise transfer function and increase in-band quantization noise, the quantization noise would be rewritten as

$$P_{Modified\_quantization\_noise} = (\frac{V_{LSB}{}^2}{12})(\frac{\pi^4}{5OSR^5} + \frac{2\mu^2\pi^2}{3OSR^3}) \quad (3.4)$$

where μ represents the finite DC-gain error and V_{LSB} represents the quantizer step size for mid-tread quantizer.

For the six noise powers in equation (3.2), the first five can be correctly summed up, since the five corresponding noises (i.e., modified quantization noise, switch thermal noise, OTA thermal noise, jitter noise and DAC noise) are independent. However, due to the reasons explained later, these five noises are correlated with settling noise. Therefore, there should be additional correlation powers terms in equation (3.2) to account for the correlation between settling noise and the five independent noises. These correlation terms are derived in follows.

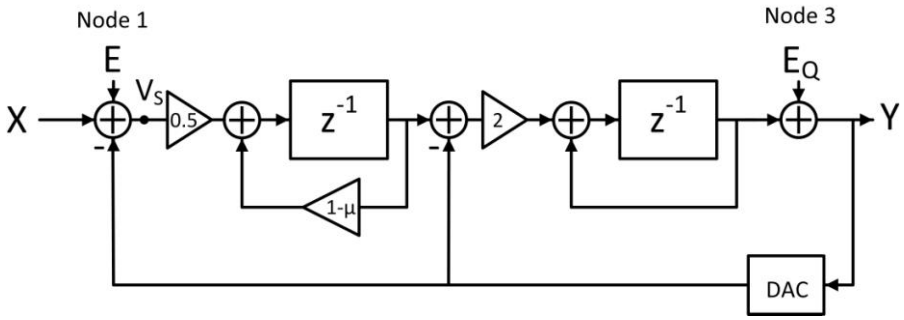


Fig. 3.1: Block diagram of single-loop 2nd-order SDM

Consider the five independent noises. The modified quantization noise (3.4) is expressed in Fig. 3.1 as E_Q applied at nodes 3 and the factor μ at feedback loop of first integrator. The remaining four noises are applied at node 1 of Fig. 3.1, the sum of which is donated as E. These five noises are treated as independent because E_Q and the four noises in E are all assumed to be Gaussian and white. Next, to explain why these five noises are correlated to settling noise, recall that settling error ε is approximated in [18] as

$$\varepsilon = \alpha_1 V_S{}^1 + \alpha_3 V_S{}^3 + \alpha_5 V_S{}^5 \quad (3.5)$$

According to Fig. 3.1, the V_S in equation (3.5) can be expressed as

$$V_S \cong (1 - z^{-2})E - [1 - z^{-1}(1-\mu)]^2 E_Q \quad (3.6)$$

It is clear from equations (3.5) and (3.6) that settling error ε is correlated to E, E_Q and μ.

From discussions above, the noise signal at SDM output can be expressed as

$$v_N(t) = v_{Modified\_quantization\_noise}(t) + v_{Settling\_noise}(t) + v_E(t) \tag{3.7}$$

where

$$v_E(t) = v_{Switch\_thermal}(t) + v_{OTA\_thermal}(t) + v_{DAC\_noise}(t) + v_{Jitter\_noise}(t) \tag{3.8}$$

The autocorrelation function of $v_N(t)$ is

$$\begin{aligned} R_N(\tau) &= E[v_N(t)v_N(t+\tau)] \\ &= R_{Modified\_quantization\_noise}(\tau) + R_E(\tau) + R_{Settling\_noise}(\tau) \\ &\quad + R_{SQ}(\tau) + R_{QS}(\tau) + R_{SE}(\tau) + R_{ES}(\tau) \end{aligned} \tag{3.9}$$

where $R_{SQ}(\tau)$ and $R_{QS}(\tau)$ are cross-collection function of $v_{Settling\_noise}(t)$ and $v_{Modified\_quantization\_noise}(t)$, and $R_{SE}(\tau)$ and $R_{ES}(\tau)$ are cross-collection function of $v_{Settling\_noise}(t)$ and $v_E(t)$. Since $v_{Modified\_quantization\_noise}(t)$ and $v_E(t)$ are uncorrelated, thus, $R_{EQ}(\tau)$ and $R_{QE}(\tau)$ do not exist in equation (3.9). Then, the power spectral density function of $v_N(t)$ is

$$\begin{aligned} S_N(f) &= F\{R_N(\tau)\} \\ &= S_{Modified\_quantization\_noise}(f) + S_E(f) + S_{Settling\_noise}(f) \\ &\quad + S_{SQ}(f) + S_{QS}(f) + S_{SE}(f) + S_{ES}(f) \end{aligned} \tag{3.10}$$

where $S_{Settling\_noise}(f)$, $S_{Quantization\_noise}(f)$, and $S_E(f)$ represent PSD of $v_{Settling\_noise}(t)$, $v_{Modified\_quantization\_noise}(t)$, and $v_E(t)$. The $S_{SQ}(f)$ and $S_{QS}(f)$ are the cross spectral density between $v_{Modified\_quantization\_noise}(t)$ and $v_{Settling\_noise}(t)$. The $S_{SE}(f)$ and $S_{ES}(f)$ are the cross spectral density between $v_E(t)$ and $v_{Settling\_noise}(t)$. Thus, the in-band noise power P_N of equation (3.1) can be obtained by

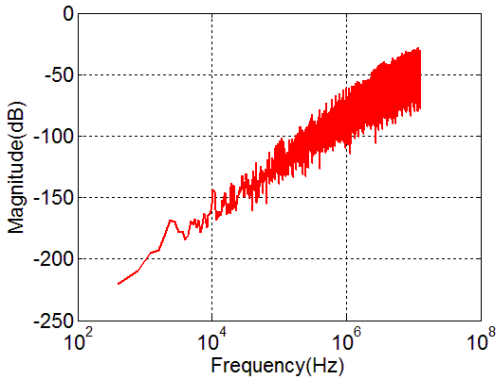
$$\begin{aligned} P_N &= \int_{-f_B}^{+f_B} S_N(f)df \\ &= P_{Modified\_quantization\_noise} + P_{Switch\_thermal} + P_{OTA\_thermal} + P_{DAC\_noise} + P_{Jitter\_noise} \\ &\quad + P_{Settling\_noise} + \int_{-f_B}^{+f_B} S_{SQ}(f) + S_{QS}(f) + S_{SE}(f) + S_{ES}(f)df \end{aligned} \tag{3.11}$$

The first six terms at equation (3.11) are identical to those in equation (3.2). The remaining

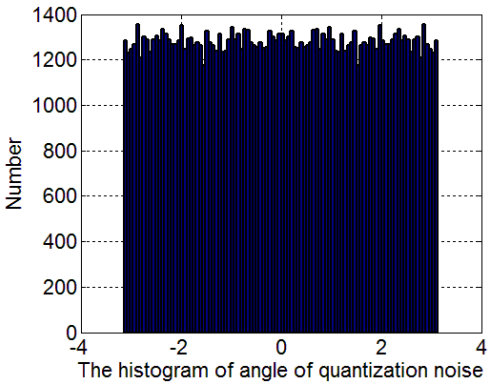
terms at equation (3.11) are the correlation power models to be derived. The $S_{QS}(f)$, $S_{SQ}(f)$, $S_{SE}(f)$ and $S_{ES}(f)$ can be approximated as [21]

$$\begin{aligned} S_{SQ}(f) &= S_{QS}^{*}(f) \\ &\cong \frac{1}{2T} V_{Settling\_noise}(f) V_{Modified\_quantization\_noise}^{*}(f) \\ S_{SE}(f) &= S_{ES}^{*}(f) \\ &\cong \frac{1}{2T} V_{Settling\_noise}(f) V_{E}^{*}(f) \end{aligned} \tag{3.12}$$

where $V_{Settling\_noise}(f)$, $V_{Modified\_quantization\_noise}(f)$, and $V_E(f)$ are the Fourier transforms of $v_{Settling\_noise}(t)$, $v_{Modified\_quantization\_noise}(t)$, and $v_E(t)$, respectively, over a finite time interval [-T, T].



(a)



(b)

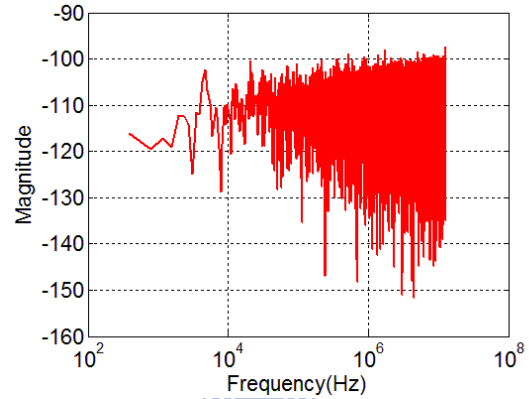
Fig. 3.2: The magnitude and angle of $V_{Modified\_quantizaition\_noise}(f)$

Fig. 3.2 (a) shows the FFT of a typical $v_{Modified\_quantization\_noise}(t)$ obtained from behavior simulation. Fig. 3.2 (b) shows that the angle of $V_{Modified\_quantization\_noise}(f)$ is random and is

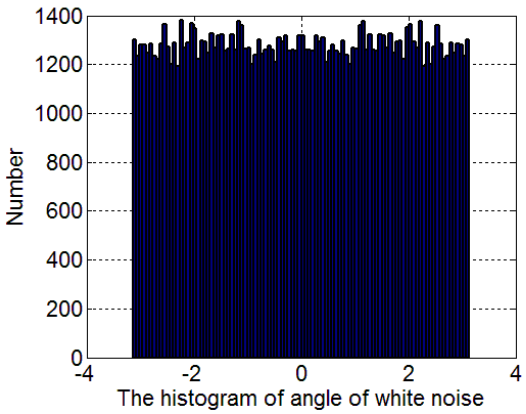
close to uniform distribution. Therefore, $\theta_Q(f)$ is assumed to be an arbitrary value in $-\pi\sim\pi$, and $V_{Modified\_quantization\_noise}(f)$ is modeled as

$$V_{Modified\_quantization\_noise}(f) \cong \left[\left(2\sin\left(\frac{\pi f}{f_S}\right)\right)^2 + 4\mu\sin\left(\frac{\pi f}{f_S}\right)\right]\frac{V_{LSB}}{\sqrt{12 f_S}}e^{i\theta_Q(f)} \tag{3.13}$$

Fig. 3.3 shows the FFT of $v_E(t)$ obtained from behavior simulation.



(a)



(b)

Fig. 3.3: The magnitude and angle of $V_E(f)$

The angle of $V_E(f)$ is also close to a uniform distribution. Therefore, $\theta_E(f)$ is assumed to be an arbitrary value in $-\pi\sim\pi$, and $V_E(f)$ is modeled as

$$V_E(f) = \frac{1}{\sqrt{f_S}}\left(\begin{array}{l}\left(P_{Switch\_thermal}\right)^{1/2} + \left(P_{OTA\_thermal}\right)^{1/2} \\ + \left(P_{Jitter\_noise}\right)^{1/2} + \left(P_{DAC\_noise}\right)^{1/2}\end{array}\right)\cdot e^{i\theta_E(f)} \tag{3.14}$$

For the settling noise, $V_{Settling\_noise}(t)$ and $v_{Settling\_noise}(f)$ are expressed in [18] as

$$v_{Settling\_noise}(t) = \alpha_1 v_S{}^1(t) + \alpha_3 v_S{}^3(t) + \alpha_5 v_S{}^5(t) \tag{3.15}$$

$$V_{Settling\_noise}(f) = \alpha_1 V_{S1}(f) + \alpha_3 V_{S3}(f) + \alpha_5 V_{S5}(f) \tag{3.16}$$

where $v_S(t)$ is the first integrator input signal, and by equation (3.6)

$$\begin{aligned} V_{S1}(f) &= V_S(f) \\ &= (1 - e^{-j4\pi f/f_S}) V_E(f) - V_{Modified\_quantization\_noise}(f) \end{aligned} \tag{3.17}$$

Then, the Fourier transform of $v_S{}^2(t)$ can be obtained by convoluting $V_S(f)$ and $V_S(f)$, i.e.

$$V_{S2}(f) = V_S(f) \otimes V_S(f) \tag{3.18}$$

Subsequently, $V_{S3}(f)$ and $V_{S5}(f)$ can be obtained by

$$V_{S3}(f) = V_{S1}(f) \otimes V_{S2}(f) \tag{3.19}$$

$$V_{S5}(f) = V_{S2}(f) \otimes V_{S3}(f) \tag{3.20}$$

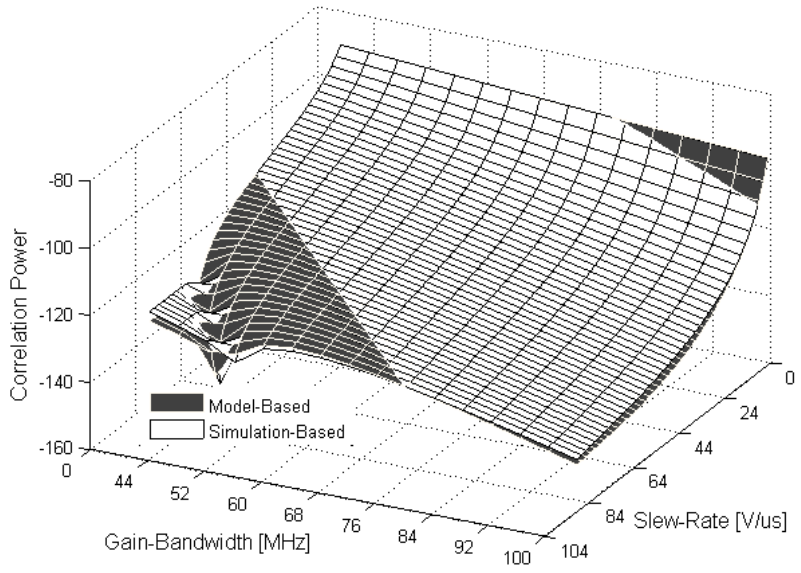
With $V_{Quantization\_noise}(f)$, $V_E(f)$, and $V_{Settling\_noise}(f)$ described in equations (3.13), (3.14) and (3.16), the cross-spectral densities, $S_{QS}(f)$, $S_{SQ}(f)$, $S_{SE}(f)$ and $S_{ES}(f)$, can be computed, and then the correlation power can be evaluated as

$$P_{Correlation} = \int_{-f_B}^{+f_B} S_{SQ}(f) + S_{QS}(f) + S_{ES}(f) + S_{SE}(f) df \tag{3.21}$$

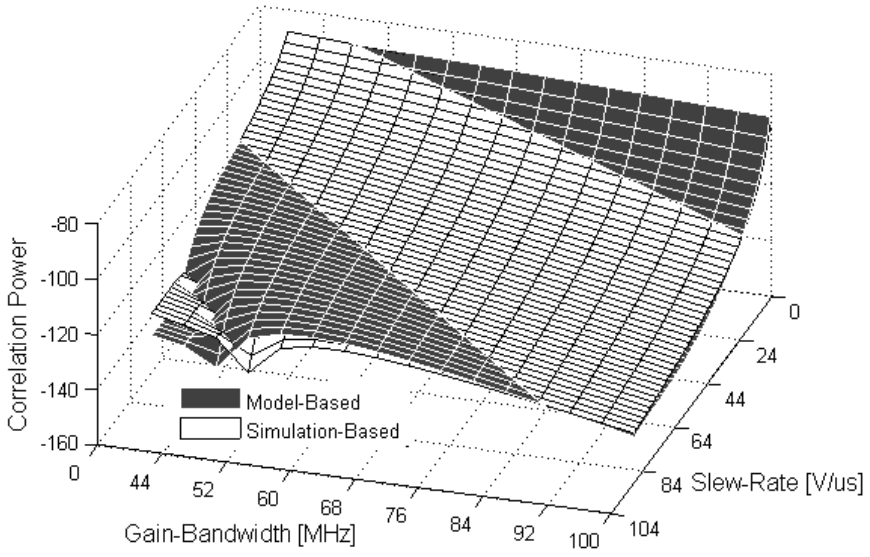
With $P_{Correlation}$ added, P_N in equation (3.1) is then rewritten as

$$\begin{aligned} P_N &= P_{Modified\_quantization\_noise} + P_{Switch\_thermal} + P_{OTA\_thermal} + P_{Jitter\_noise} + P_{DAC\_noise} \\ &\quad + P_{Settling\_noise} + P_{Correlation} \end{aligned} \tag{3.22}$$

To verify the correctness of correlation model (3.21), Fig. 3.4 (a) (b) shows the correlation power calculated by equation (3.21) and by behavior simulation for various SR and GBW combinations, with other parameters set at F_{in}=100kHz, B=1, OSR=100, A_{in}=0.2V and V_{ref} =1V. The two surfaces in Fig. 3.4 (a) (b) are very close.



(a)



(b)

Fig. 3.4: Correlation powers (a) assumption that V_E in negligible (b) assumption that V_E exists

Next, an example is provided to investigate the relations between $P_{Settling\_noise}$, $P_{Quantization\_noise}$ and $P_{Correlation}$ under the assumption that $V_E(f)$ in negligible, which is the typical case. The relevant parameters are: F_{in}=100kHz, B=1, OSR=256, A_{in}=0.2V, V_{ref}=1V and GBW=51.2MHz, Fig. 3.5 shows the three noise powers w.r.t different SR values.

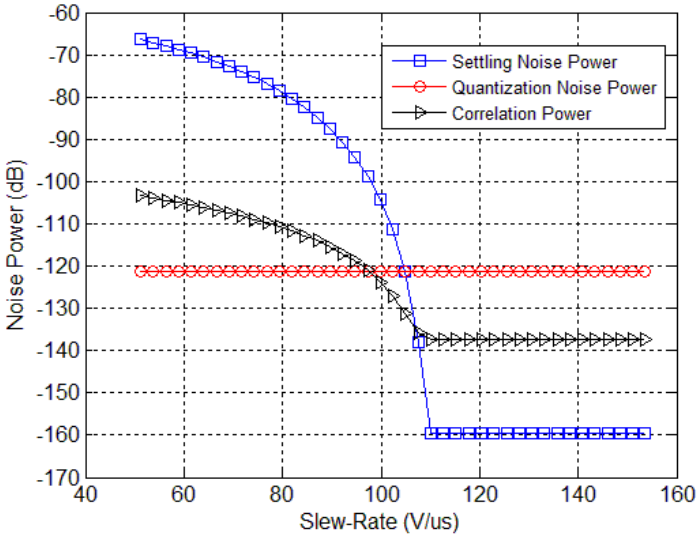


Fig. 3.5: Each noise power for different SR values.

Discussion 1: As Fig. 3.5 shows, settling noise is in linear region [18] when slew-rate is large than 110V/μs. In this case, the α_3 and α_5 in equation (3.16) can be neglected, such that

$$V_{Settling\_noise}(f) = \alpha_1 V_{S1}(f) \tag{3.23}$$

Then, it can be shown that

$$P_{Correlation} = \int_{-f_B}^{+f_B} S_{SQ}(f) + S_{QS}(f) df = 2\left(P_{Quantization\_noise} \cdot P_{Settling\_noise}\right)^{1/2} \tag{3.24}$$

Since $P_{Quantization\_noise}$=-120dB and $P_{Settling\_noise}$=-159dB, the correlation power is -137dB, as is shown in Fig. 3.5.

Discussion 2: When slew-rate is less than 110 V/μs, the α_3 and α_5 in equation (3.16) would increase dramatically. Therefore, the normalized correlation between settling noise and quantization noise reduces when slew-rate decreases. However, as is shown in Fig. 3.5, $P_{Correlation}$ increases steadily as SR decreases, and $P_{Correlation}$ becomes larger than $P_{Quantization\_noise}$ when SR<100 V/μs. This is because $P_{Correlation}$ represents an absolute correlation power, not a relative one.

4
Advantages of Model-Based SDM Design

The first advantage of model-based design over simulation-based design is obviously its speed; the former can be at the order 10^4 times faster. The second advantage is that the model-based approach provides more insights to guide the design, since this design method explicitly computes all noise powers and distortion powers. These issues are quantitatively analyzed in this chapter.

4.1 SNDR Speed Comparison

For model-based SDM design, the SNDR is computed by equation (3.1). In simulation-based SDM design (in MATLAB SIMULINK environment), generating SNDR is a more complex process. First, behavior simulation is conducted and output data points are collected. Then, FFT is performed on collected data points to generate power spectral density (PSD). The total noise power P_N is obtained from integrating in-band PSD floor, and total distortion power is obtained by summing up distortional powers in PSD. The accuracy of SNDR computed heavily depends on the number of data points involved, since sufficient number of data points in needed to generate relatively accurate PSD [22]. However, more data points require almost proportionally more simulation time because FFT accounts for only 0.3% of the total simulation time for generating SNDR. Table 4.1 lists the simulation times for obtaining 16384, 32768 and 65536 data points.

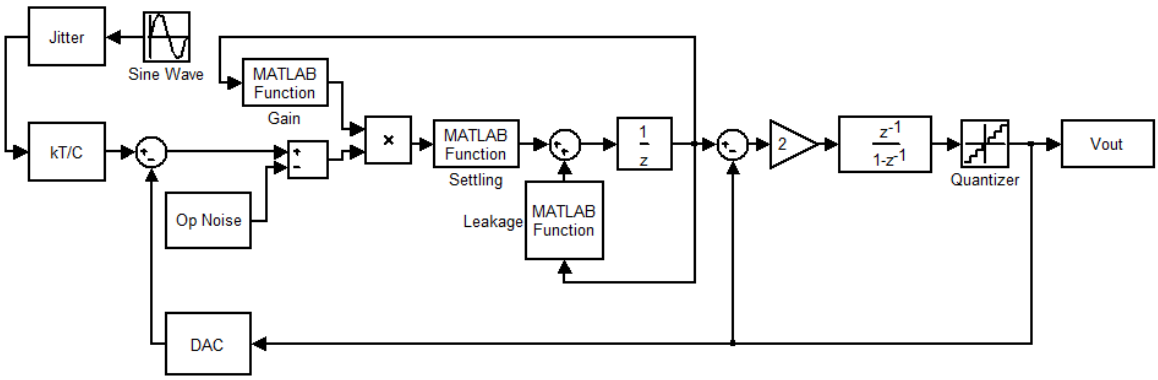


Fig. 4.1: Single-loop 2nd-order SDM model with relevant non-ideality blocks.

TABLE 4.1: Running time of each non-ideality for both design approaches

Non-idealities	Data Points	16384	32768	65536
Quantization Noise	Simulation-Based	56.515ms	114.125ms	285.375ms
	Model-Based	0.016ms	0.016ms	0.016ms
Switch thermal Noise	Simulation-Based	108.203ms	182.969ms	423.25ms
	Model-Based	0.016ms	0.016ms	0.016ms
Jitter Noise	Simulation-Based	67.985ms	123.703ms	254.562ms
	Model-Based	0.016ms	0.016ms	0.016ms
DAC Noise	Simulation-Based	83.86ms	165.157ms	370.297ms
	Model-Based	0.016ms	0.016ms	0.016ms
OTA thermal Noise	Simulation-Based	65.438ms	119.219ms	256.844ms
	Model-Based	0.422ms	0.422ms	0.422ms
Settling Noise	Simulation-Based	2171.72ms	4865.94ms	8578.59ms
	Model-Based	23.469ms	23.469ms	23.469ms
DC-Gain Distortion	Simulation-Based	1967.063ms	3941.09ms	7828.078ms
	Model-Based	0.031ms	0.031ms	0.031ms
Total Non-idealities	Simulation-Based	3847.03ms	7631.25ms	15382.03ms
	Model-Based	24.125ms	24.125ms	24.125ms

In MATLAB 7.0.1, simulations were carried on AMD Athlon (tm) 64 X2 Dual Core Processor 6000+ PC with 4GB memory running at 3.11GHz.

In contrast, as is shown in Table 4.1, in model-based approach the SNDR computation time is a least 10^2 times loss than that in simulation-based approach. The model-based SNDR computation time can be reduced much further, since little research has been done on

the computational issue which would be discussed in follows.

As Fig. 4.2 shows, computing settling noise power accounts for 97% of the total time for generating SNDR. To reduce the computation time of settling noise power, we modify the settling noise analytic model [18].

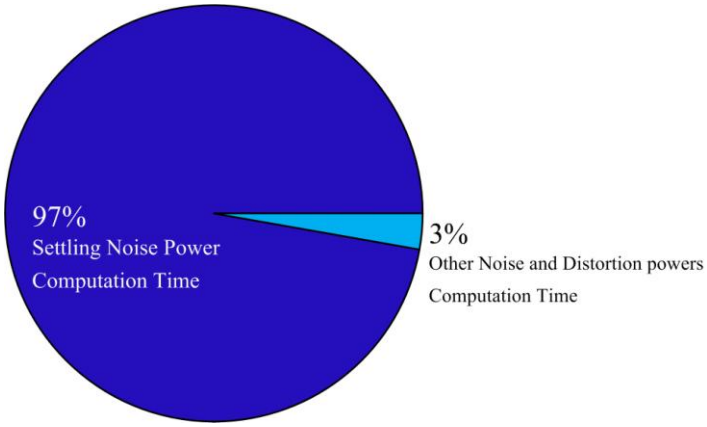


Fig. 4.2: The pie chart of SNDR computation time in model-based SDM design method

The settling noise is approximated by following polynomial

$$v_{Settling\_noise} = \alpha_1 v_S^{\,1} + \alpha_3 v_S^{\,3} + \alpha_5 v_S^{\,5} \tag{4.1}$$

First, coefficients α_1, α_3 and α_5 are computed by

$$\begin{bmatrix} \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} \int_0^{V_H} W(V_S)\cdot V_S^{\,2} dV_S & \int_0^{V_H} W(V_S)\cdot V_S^{\,4} dV_S & \int_0^{V_H} W(V_S)\cdot V_S^{\,6} dV_S \\ \int_0^{V_H} W(V_S)\cdot V_S^{\,4} dV_S & \int_0^{V_H} W(V_S)\cdot V_S^{\,6} dV_S & \int_0^{V_H} W(V_S)\cdot V_S^{\,8} dV_S \\ \int_0^{V_H} W(V_S)\cdot V_S^{\,6} dV_S & \int_0^{V_H} W(V_S)\cdot V_S^{\,8} dV_S & \int_0^{V_H} W(V_S)\cdot V_S^{\,10} dV_S \end{bmatrix}^{-1}$$
$$\times \begin{bmatrix} \int_0^{V_L} W(V_S)\cdot \beta \cdot V_S^{\,2} dV_S + \int_{V_L}^{V_H} W(V_S)\cdot V_L \cdot \beta \cdot e^{-1} \cdot e^{|V_S|/V_L} \cdot V_S^{\,1} dV_S \\ \int_0^{V_L} W(V_S)\cdot \beta \cdot V_S^{\,4} dV_S + \int_{V_L}^{V_H} W(V_S)\cdot V_L \cdot \beta \cdot e^{-1} \cdot e^{|V_S|/V_L} \cdot V_S^{\,3} dV_S \\ \int_0^{V_L} W(V_S)\cdot \beta \cdot V_S^{\,6} dV_S + \int_{V_L}^{V_H} W(V_S)\cdot V_L \cdot \beta \cdot e^{-1} \cdot e^{|V_S|/V_L} \cdot V_S^{\,5} dV_S \end{bmatrix} \tag{4.2}$$

where $W(V_S)$ is the weight function,

$$W(V_S) = \frac{V_H}{\int_0^{V_H} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{V_s}{2\sigma^2}\right) dV_s} \frac{1}{\sqrt{2\pi}\sigma_{V_S}} \exp\left(-\frac{V_s}{2\sigma_{V_S}^{\,2}}\right) \tag{4.3}$$

Second, $V_S^{\,1}(f)$, $V_S^{\,3}(f)$, and $V_S^{\,5}(f)$ are needed to computed settling noise.

$$V_S^{\,3}(f) = V_S(f) \otimes V_S(f) \otimes V_S(f) \tag{4.4}$$

$$V_S^{\,5}(f) = V_S(f) \otimes V_S(f) \otimes V_S(f) \otimes V_S(f) \otimes V_S(f) \tag{4.5}$$

Finally, the settling noise power is obtained by

$$P_{Settling\_noise} = \int_{-f_B}^{+f_B} \alpha_1 V_S^{\,1}(f) + \alpha_3 V_S^{\,3}(f) + \alpha_5 V_S^{\,5}(f) df \tag{4.6}$$

In computing settling noise power, simulation result indicates that the first step, i.e., the coefficient computation, is the most time-consuming because using MATLAB to evaluate integrals in equation (4.2) costs much time. In MATLAB environment, dealing with algebra problem is much faster than evaluating integral problem. Hence, find the antiderivative of integrand in equation (4.2) and substitute the upper and lower limits of integration would make computation time for coefficients α_1, α_3, and α_5 much faster. In this way the computation time for coefficients α_1, α_3 and α_5 become much faster, and it only takes 0.219ms to generate settling noise power.

In addition, computing OTA thermal noise power also needs to evaluate the integrals in equation (4.7). Hence, we find the antiderivative of integrand in equation (4.7) and substitute the upper and lower limits of the integration to reduce the running time of computing OTA thermal noise power. In this way it takes 0.016m second for generating OTA thermal noise power.

$$P_{OTA\_thermal} \cong \frac{1}{a_1^{\,2} OSR} \int_0^{\infty} V_{nOTA}^{\,2} \cdot \left(\left| H_{Samp}(f) \right|^2 + \left| H_{Int}(f) \right|^2 \right) df$$

$$\cong \frac{1}{a_1^{\,2} OSR} \left(\frac{10\alpha kT}{4C_L} + \int_0^{\infty} \frac{\left(2a_1 + 1\right)^2 + \left(\omega RC_S \left(a_1 + 1\right)\right)^2}{\left(\frac{A\omega^2 RC_S \left(1 + a_1\right)}{GBW} + 1 \right)^2 + \left(\omega RC_S + \frac{A\omega \left(2a_1 + 1\right)}{GBW} \right)} d\omega \right) \tag{4.7}$$

Eventually, it takes only 0.312m second for generating SNDR in model-based SDM design after modifying noise analytic models. It is hundred times faster than before. But computing

settling noise power still accounts for 63% of the total time in generating SNDR as is shown in Fig. 4.3.

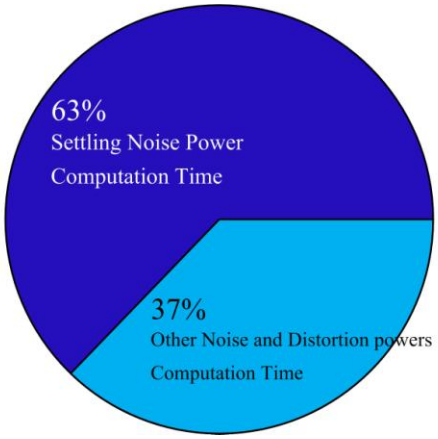


Fig. 4.3: The pie chart of SNDR computation time in modified model-based SDM design method

Despite the detail of two design approaches, in model-based SDM design the SNDR computation time is a least 10^4 times faster than that in simulation-based SDM design. Consequently, model-based method is a time-efficient and practical solution in SDM design cycle.

4.2 SDM Design Guide

Simulation-based SDM design generates sum of noise P_N and sum of distortion P_D from SDM output PSD. In this process, it is not easy to find out the magnitude of individual noise or distortion. In contrast, model-based SDM design can explicitly compute all noise and distortion powers. This advantage may be exploited by designers. We now consider two possible cases.

In the case that design specification cannot be met, the knowledge about dominating noise or distortion would indicate where design can be improved. For example, in a design problem for the sensor applications, SNDR is required to be better than 96dB (i.e., a resolution of 16 bits), but SNDR at 87dB is the highest that is achieved by traditional design method. After computing noise and distortion powers using their models, it revealed that all noises and distortions are very small except that the DAC noise at -86dB is the dominating

factor for previous design result. This gives a guide about how the design can be improved. After employing the DWA algorithm or making use of better CMOS device technology, the designer is able to reduce DAC noise to -123dB. New computations reveal that SNDR at 97dB is achieved, with dominating non-ideality power being switch noise power at -99dB.

In the case that design specification is met, the knowledge about magnitude of each noise or distortion would suggest where design parameters can be relaxed. For example, SNDR for an audio application is required to be better than 84dB (i.e. a resolution of 14 bits), and SNDR at 87dB is achieved by traditional design method. Since our model can compute all noise and distortion powers, we immediately find that -121dB for the settling noise power is by far smaller than the dominating non-ideality power which here is switch thermal noise at -94dB. Our models suggest that adjusting SR and GBW would significantly affect settling noise power and SDM power consumption, but otherwise has little effect on other noises and distortions. After relaxing design parameters SR (from 160V/μs to 91V/μs) and GBW (from 120MHz to 80MHz), designer raised settling noise to -98dB. Although SNDR is consequently lowered to 86dB, it still meets the 84dB requirement. But the benefits received are obvious: OTA power consumption is reduced from 11.23mW to 7.04mW, and OTA design complexity is much decreased.

5
Models of SDM Power Consumption

In this chapter, we propose an effective SDM power consumption model, which bases on single-loop 2nd-order SDM architecture shown in Fig. 2.1. Our power consumption model is split up in two parts: the analog power consumption of OTA and quantizer, and the digital power consumption of switch, DAC and data weighted averaging (DWA).

5.1 Analog Power Consumption:

5.1.1 OTA Power Consumption:

Given design parameters GBW, SR, and C_{eq}, OTA power consumption is derived partly based on study [23] [24]. Here, OTA model is depicted in Fig. 5.1. This model includes:

A single-pole dynamic

A non-linear characteristic with maximum output current I_O

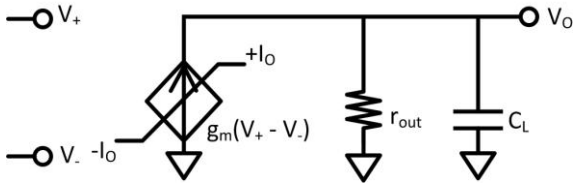


Fig. 5.1: OTA model

The OTA open-loop transfer function can be expressed as

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} \tag{5.1}$$

A_0 is the OTA open-loop dc gain

$$A_0 = g_m \cdot r_{out} \tag{5.2}$$

where g_m is the OTA transconductance and r_{out} is the OTA open-loop output resistance.

p_1 is the OTA open-loop pole

$$p_1 = \frac{1}{r_{out} \cdot C_L} \tag{5.3}$$

where C_L donates the open-loop effective load capacitance.

Using OTA model shown in Fig. 5.1 with infinite r_{out}, the model of the SC integrator is shown in Fig. 5.2. Meanwhile, it also takes the parasitic capacitors associated to its input and output nodes into account.

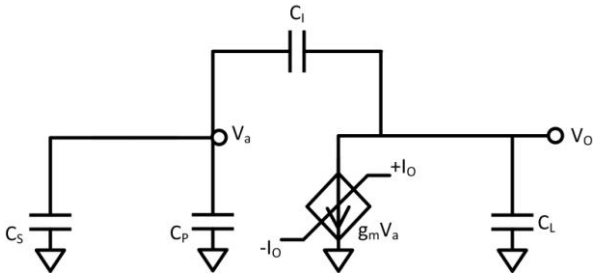


Fig. 5.2: Integrator model with the parasitic capacitor

Here, C_S and C_I are the sampling and integrating capacitors of integrator; C_P is the parasitic input capacitance and C_L is the output load capacitance, which includes the OTA output node parasitic and the bottom plate parasitic of C_I. For the SC integrator, the close-loop transfer function is

$$A_{CL}(s) = \frac{1}{f} \cdot \frac{1}{1 + \frac{s}{f \cdot \omega_u}} \tag{5.4}$$

where f is the feedback factor of integrator, and ω_u is the OTA unity-gain frequency. The feedback factor for the integrator is

$$f = \frac{C_I}{C_S + C_I + C_P} \tag{5.5}$$

The unit-gain frequency for integrator is

$$\omega_u = A_0 \cdot p_1 = \frac{g_m}{C_O} \tag{5.6}$$

where C_O is the open-loop effective load capacitance of the integrator shown in Fig. 5.2.

$$C_O = C_L + C_I \,//\, (C_S + C_P) \tag{5.7}$$

The close-loop gain -3dB bandwidth is defined as

$$\omega_{-3dB} = \omega_u \cdot f = \frac{g_m}{C_{eq}} \tag{5.8}$$

where C_{eq} is the equivalent load capacitance for the integrator, and is estimated as

$$C_{eq} = C_P + C_S + C_L\left(1 + \frac{C_P + C_S}{C_I}\right) \tag{5.9}$$

For the step response calculation, the time constant τ_a of the integrator is defined as

$$\omega_{-3dB} = \frac{1}{\tau_a} = 2\pi \cdot GBW = \frac{g_m}{C_{eq}} \tag{5.10}$$

Then, OTA transconductance for the integrator is obtained by

$$g_m = 2\pi \cdot GBW \cdot C_{eq} \tag{5.11}$$

Besides, SR for the integrator is defined as

$$SR = \frac{I_O}{C_{eq}} \tag{5.12}$$

Hence, OTA maximum output current I_O is obtained by

$$I_O = SR \cdot C_{eq} \tag{5.13}$$

Given specific values of GBW, SR and C_{eq}, equation (5.11) and equation (5.13) indicate the corresponding value of g_m and I_O of the OTA. However, estimating OTA power consumption is not only determined by these three design parameters, but also decided by chosen OTA topology. The merits of three OTA topologies here are examined: telescopic OTA, folded-cascode OTA, and two-stage Miller-compensated OTA. Their simplified circuit schematics would be presented in Fig. 5.3 (a), (b) and (c), respectively.

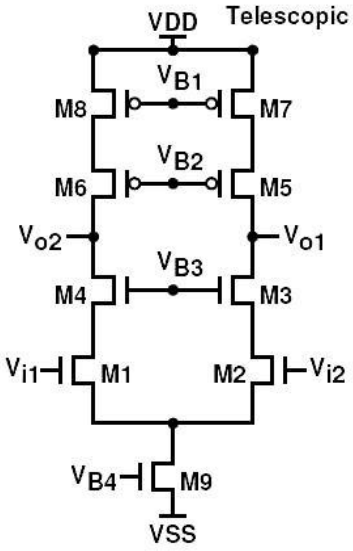


Fig. 5.3 (a) Telescopic OTA

For telescopic OTA, the slew-rate is

$$SR = \frac{I_{D9}}{C_{eq}} \tag{5.14}$$

Then, the bias current I_{D9} corresponded to SR is defined as

$$I_{D9(SR)} = SR \cdot C_{eq} \tag{5.15}$$

The close-loop -3dB bandwidth for the integrator is

$$\omega_{-3dB} = \frac{g_{m1}}{C_{eq}} \tag{5.16}$$

Combing (5.17) with the transcoductance equation in strong region inversion region,

$$g_{m1} = \frac{2I_{D1}}{V_{OV1}} = \frac{I_{D9}}{V_{OV1}} \tag{5.17}$$

The bias current I_{D9} corresponded to ω_{-3dB} is defined as

$$I_{D9(GBW)} = \omega_{-3dB} \cdot C_{eq} \cdot V_{OV1} = 2\pi \cdot GBW \cdot C_{eq} \cdot V_{OV1} \tag{5.18}$$

where V_{OV1} is the transistor overdrive voltage of the differential pair.

Equation (5.15) and equation (5.18) indicate that the telescopic OTA bias current I_{D9} depends on V_{OV1}. The designer could assume that V_{OV1} has a range (such as 0.1v~0.3v) when calculating I_{D9}. If V_{OV1} is in the range, it would be self adjusted to make following

equation hold.

$$I_B = I_{D9(SR)} = I_{D9(GBW)} \tag{5.19}$$

If V_{OV1} is out of range, it would be stuck at the extreme value of the range and the following equation would be hold.

$$I_B = Max\left(I_{D9(SR)}, I_{D9(GBW)}\right) \tag{5.20}$$

Finally, the telescopic OTA power consumption is

$$PC = V_{DD} \cdot I_B \tag{5.21}$$

where V_{DD} donates the supply voltage.

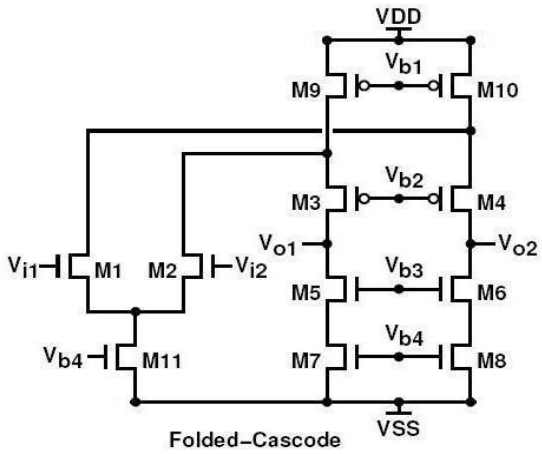


Fig. 5.3 (b): Folded-Cascode OTA

For folded-cascode OTA, the slew-rate is

$$SR = \frac{I_{D11}}{C_{eq}} \tag{5.22}$$

Then, the bias current I_{D11} corresponded to SR is defined as

$$I_{D11(SR)} = SR \cdot C_{eq} \tag{5.23}$$

Notice that the value of I_{D9} and I_{D10} is set to $1.2 \cdot I_{D11}$ to avoid zero current in cascades when OTA is slewing [25], and slew limiting occurs only in the input stage of the circuit.

The close-loop -3dB bandwidth for the SC integrator is

$$\omega_{-3dB} = \frac{g_{m1}}{C_{eq}} \tag{5.24}$$

Combing (5.24) with the transcoductance equation in strong region inversion region, the bias current I_{D11} corresponded to ω_{-3dB} is defined as

$$I_{D11(GBW)} = \omega_{-3dB} \cdot C_{eq} \cdot V_{OV1} = 2\pi \cdot GBW \cdot C_{eq} \cdot V_{OV1} \tag{5.25}$$

Equation (5.23) and equation (5.25) indicate that the folded-cascode OTA bias current I_{D11} depends on V_{OV1}. The designer could assume that V_{OV1} has a range when calculating I_{D11}. If V_{OV1} is in the range, it would be self adjusted to make following equation be hold.

$$I_B = I_{D11(SR)} = I_{D11(GBW)} \tag{5.26}$$

If V_{OV1} is out of range, it would be stuck at the extreme value of the range and the following equation would be hold.

$$I_B = Max\left(I_{D11(SR)}, I_{D11(GBW)}\right) \tag{5.27}$$

Finally, the folded-cascode OTA power consumption is

$$PC = 2.4 \cdot V_{DD} \cdot I_B \tag{5.28}$$

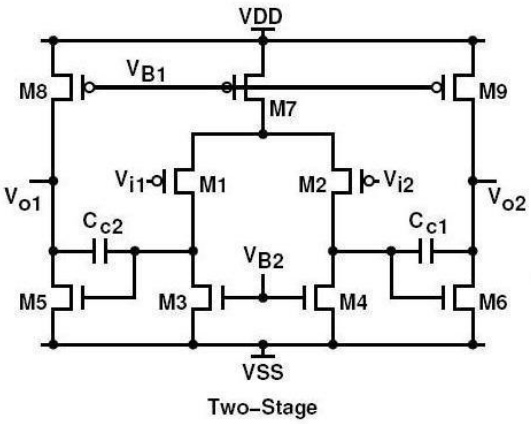


Fig. 5.3 (c): Two-stage Miller-compensated OTA

For the two-stage Miller-compensated OTA, the slew-rate is

$$SR = \min\left(\frac{I_{D7}}{C_C}, \frac{2I_{D9}}{C_O + C_C}\right) = \min(SR_{int}, SR_{ext}) \tag{5.29}$$

The non-dominant pole is

$$p_2 \cong \frac{g_{m6}}{C_O} \tag{5.30}$$

The zero is

$$z_0 = \frac{g_{m6}}{C_C} \tag{5.31}$$

And the unit-gain bandwidth is

$$\omega_u = \frac{g_{m1}}{C_C} \tag{5.32}$$

Assuming that phase margin is greater than 70°, and z_0 is twenty times higher than ω_u, p_2 must be placed at least 3.2 times higher than ω_u. From the assumption above, we get $C_C > 0.16C_O$, and the internal slew-rate SR_{int} is the limiting factor.

Then, the close-loop gain -3dB bandwidth is

$$\omega_{-3dB} = \omega_u \cdot f = \frac{g_{m1}}{C_{eq}} \tag{5.33}$$

where C_{eq} for two-stage Miller-compensated OTA is expressed as

$$C_{eq} = C_C\left(1+\frac{C_S + C_P}{C_I}\right) \tag{5.34}$$

Combing (5.33) with the transcoductance equation in strong region inversion region, the bias current I_{D7} corresponded to ω_{-3dB} is defined as

$$I_{D7(GBW)} = \omega_{-3dB} \cdot C_{eq} \cdot V_{OV1} = 2\pi \cdot GBW \cdot C_{eq} \cdot V_{OV1} \tag{5.35}$$

Besides, the bias current I_{D7} corresponded to SR is defined as

$$I_{D7(SR)} = SR \cdot C_C \tag{5.36}$$

Equation (5.35) and equation (5.36) indicates that the two-stage Miller-compensated OTA bias current I_{D7} depends on V_{OV1}. The designer could assume that V_{OV1} has a range when calculating I_{D7}. If V_{OV1} is in the range, it would be self adjusted to make following equation be hold.

$$I_B = I_{D7(SR)} = I_{D7(GBW)} \tag{5.37}$$

If V_{OV1} is out of range, it would be stuck at the extreme value of the range and the following equation would be hold.

$$I_B = Max\left(I_{D7(SR)}, I_{D7(GBW)}\right) \tag{5.38}$$

For $I_{D9} = 20I_{D1}$ form assumption above, and $I_B = 2I_{D1}$, the power consumption of two-stage Miller-compensated OTA is

$$PC = V_{DD} \cdot (I_B + 2I_{D9}) = 21V_{DD} \cdot I_B \tag{5.39}$$

As OTA topology is selected, the total OTA power consumption for SDM is approximated as

$$PC_{OTA} = K_{SDM} \cdot PC \tag{5.40}$$

where K_{SDM} represent the ratio between the total power consumption of all the OTAs and OTA in first stage.

5.1.2 Quantizer Power Consumption:

Quantizer in SDM is usually implemented by a flash ADC, and its power consumption is

$$PC_{Quantizer} = 2^B \cdot I_{comp} \cdot V_{Supply} \tag{5.41}$$

where I_{comp} donates the total current of each comparator and must be determined before computing the quantizer power; V_{Supply} is the comparator supply voltage.

5.2 Digital Power Consumption:

5.2.1 DAC Power Consumption:

For the SC stage structure shown in Fig. 2.1, DAC power consumption is approximated by

$$PC_{DAC} = N_{DAC} \cdot k_{C_s} \cdot C_u \cdot {V_{ref}}^2 \cdot f_S = 2 \cdot k_{C_s} \cdot C_s \cdot {V_{ref}}^2 \cdot 2 \cdot f_B \cdot OSR \tag{5.42}$$

where first factor 2 comes from the differential implementation; C_u is the unit feedback capacitor used in the first stage, with $C_u = C_S/2^B$; k_{Cs} is the ratio between C_S in all stages and

C_S in first stage; N_{DAC} is the total number of the unit capacitor in first stage and can be written as $N_{DAC} = 2^B$.

5.2.2 Switch Power Consumption:

The switch power consumption is approximated by

$$PC_{Switch} = N_{Switch} \cdot C_{Switch} \cdot V_{Supply}{}^2 \cdot 2 \cdot f_B \cdot OSR \tag{5.43}$$

where N_{Switch} is the number of total switches in SDM; V_{Supply} is the switch supply voltage; C_{Switch} is the switch parasitic capacitance corresponding to the switch structure.

For transmission gate switch circuit, the relation of C_{Switch} and R_{on} is estimated as

$$C_{Switch} = \frac{\left(\mu_n^{-1} + \mu_p^{-1}\right) \cdot L^2}{R_{on} \cdot \left(V_{Supply} - V_{tn} - \left|V_{tp}\right|\right)} \tag{5.44}$$

where L is the channel length of transistors. Given R_{on}, L and the specific process technology, C_{Switch} could be obtained.

5.2.3 DWA Power Consumption:

DWA algorithm used to solve the nonlinearity problem of the feedback DAC can be implemented with an accumulator and a logarithmic shifter [27], as is depicted in Fig. 5.4.

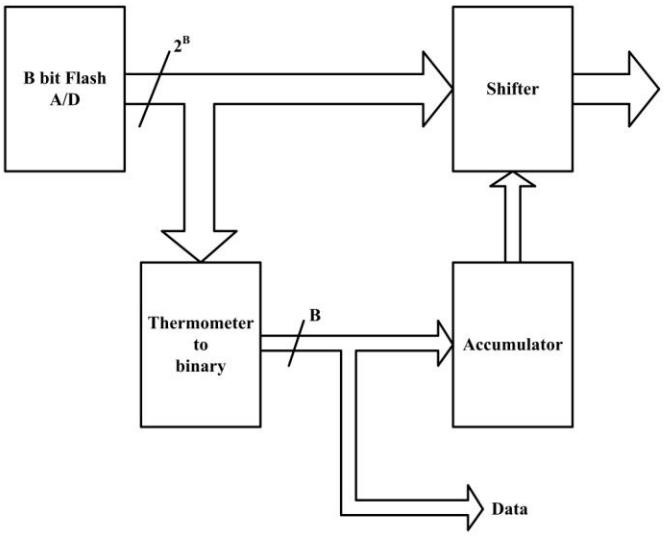


Fig. 5.4: Block diagram of DWA implementation

As Fig. 5.4 is shown, the DWA circuit would be separate in: ROM encoder, accumulator,

and logarithmic shifter. A 2-bit ROM encoder is shown in Fig. 5.5.

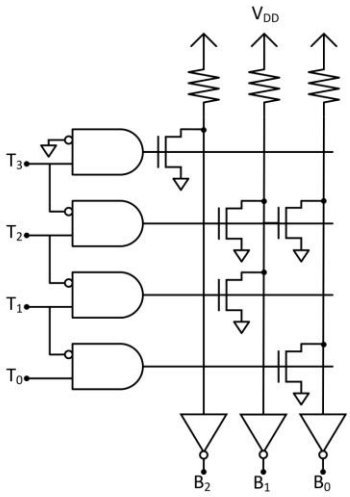


Fig. 5.5: 2-bit thermometer-to-binary ROM encoder

When NMOS turns on, the current flows through the resistor and can be calculated as equation (5.44).

$$I_D = \frac{(V_{DD} - V_{DS})}{R} = \mu_n C_{ox} \left(\frac{W}{L}\right)\left(V_{GS} - V_t - \frac{V_{DS}}{2}\right)V_{DS} \tag{5.45}$$

When the NMOS turns off, there is no current on the resistor and no power consumption. For example, as input thermometer code is 0000, the output binary code is 000, and then the ROM encoder consumes no power. As the input thermometer code is 0001, the output binary code is 001, and the power of the ROM encoder is $V_{DD} \cdot I_D$ (Because one NMOS turns on). For the input thermometer code is given over some time interval, ROM encoder power consumption can be estimated.

For the accumulator and the logarithmic shifter, their power consumption are approximated as

$$PC_{DWA} = C_{D,eq} \cdot V_{Supply}{}^2 \cdot 2 \cdot f_B \cdot OSR \tag{5.46}$$

where V_{Supply} is the circuit supply voltage; $C_{D,eq}$ is the equivalent capacitance corresponding to the complexity of the accumulator and the logarithmic shifter, and its derivation is based on study [26]. Here, accumulator builds up with register and adder, and logarithmic shifter builds up with multiplexer. Therefore, a good approximation of $C_{D,eq}$ is the number of one

bit accumulator and logarithmic shifter that are operating at frequency f_S, and is expressed as

$$C_{D,eq} = B \cdot (C_{Add} + C_{Reg}) + B \cdot 2^B \cdot C_{MUX} \tag{5.47}$$

where C_{Add}, C_{Reg}, and C_{MUX} are the one bit equivalent capacitance of adder, register and multiplexer, respectively.

For example, when we give $C_{D,eq}$ a specific value shown in Table 5.1, Fig. 5.6 (a)-(c) show the DWA power in equation (5.45) with the corresponding simulation result.

TABLE 5.1: The specific value of $C_{D,eq}$ for different bit number

	2 Bit	**3 Bit**	**4 Bit**
$C_{D,eq}$	0.2935 pF	0.4846 pF	0.8295 pF

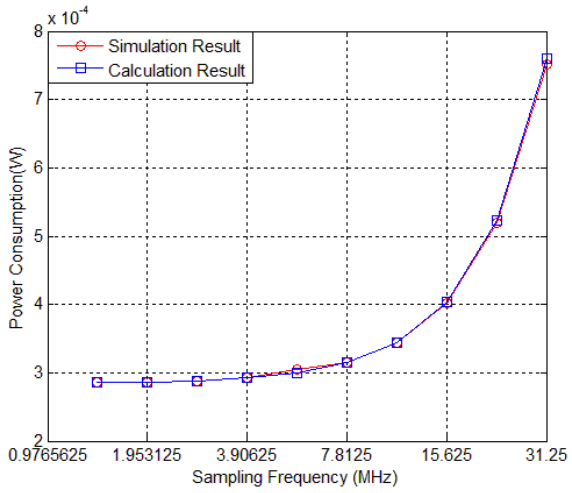


Fig. 5.6 (a): 2-bit DWA Power

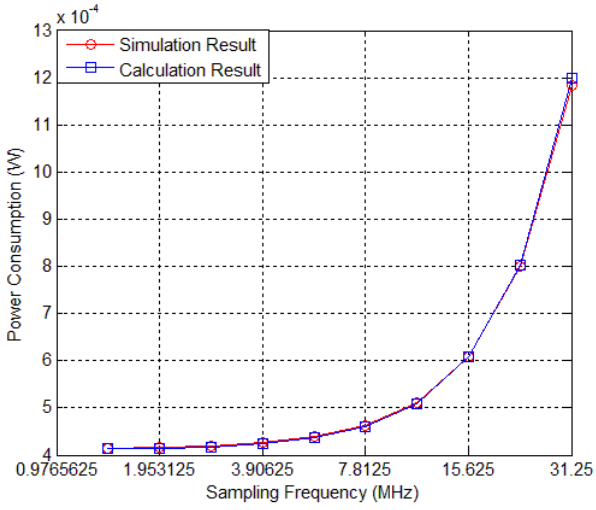


Fig. 5.6 (b): 3-bit DWA Power

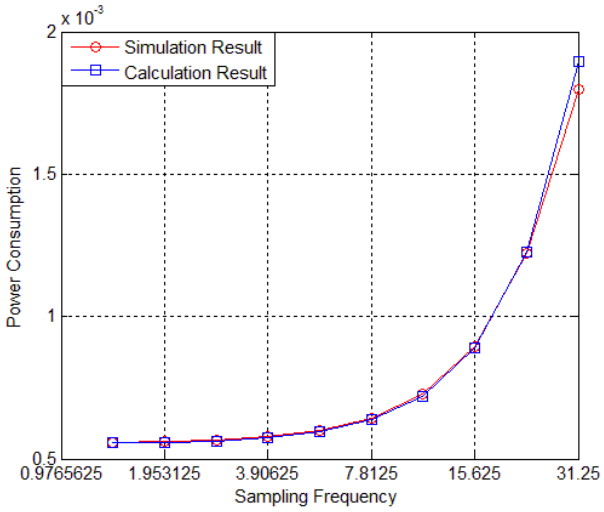


Fig. 5.6 (c): 4-bit DWA Power

By summing up all the contributions in equations (5.40) - (5.43) and (5.46), the SDM power consumption can be estimated as

$$POWER = PC_{OTA} + PC_{Quantizer} + PC_{DAC} + PC_{Switch} + PC_{DWA} \tag{5.48}$$

The SDM power consumption is related to f_B, OSR, C_S, R_{on}, B, GBW and SR.

6
Model-Based SDM Design Optimization

In this chapter, we propose a methodology for model-based SDM design optimization. This design method is applied to a published design task [3]. Compared with the single-loop SDM reported in [3], the SDMs designed by our method achieves much higher SNDR and significantly lowers power consumption. This shows that our method can effectively achieve more balanced designs for piratical application.

6.1 Design Optimization Schemes

A typical SDM design optimization algorithm is shown in Fig. 6.1. This algorithm searches the SDM design parameter space to find out one design parameter set which meet in terms of SNR or SNDR while keeping the power consumption as low as possible. The blocks or signals in Fig. 6.1 are explained in the following.

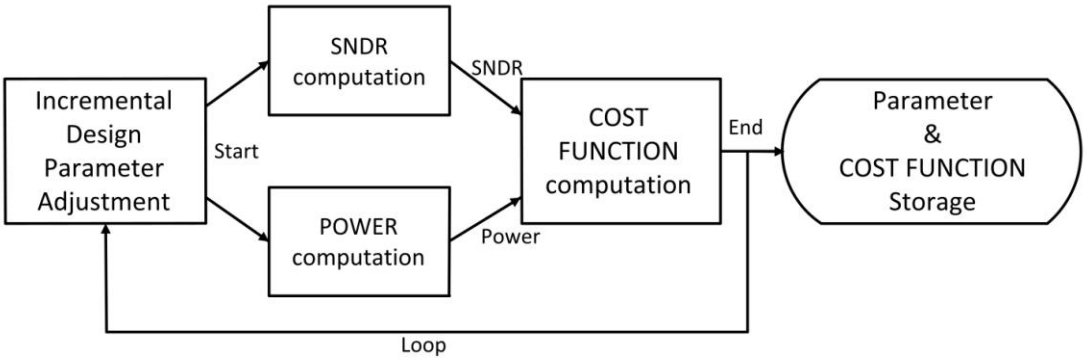


Fig. 6.1: Design optimization schemes

6.1.1 Design Parameters

Designers need to determine which design parameters are fixed to a specific value and which design parameters are adjusted during the optimization process run.

6.1.2 SNDR and POWER Computation

SNDR computation has been described in equation (3.1), and the POWER computation has been described in equation (5.48).

6.1.3 Cost Function Generation

After the *SNDR* and *POWER* are computed, they are used to generate

$$COST\ FUNCTION = -K \cdot SNDR + 10\log(\frac{POWER}{f_B}) \tag{6.1}$$

which is a modified figure of merit (FOM) [22]. The factor K served as the relative weighting. If high resolution design is required, the value of K can be set bigger, and increasing SNDR would play a more important role than reducing POWER. In contrast, if low power design is needed, the value of K would be set smaller.

At the end of the optimization process, the design parameter set corresponding to the minimum cost function value is treated as the design.

6.2 ΣΔ ADC for ADSL-CO Applications

The ADSL design specs reported in [3] to be achieved are

- Peak SNDR : 78 dB
- Signal bandwidth : 276 kHz

According to [3], V_{ref} and V_{DD} are set at 0.9V and 1.8V for the 0.18-μm CMOS technology. The σ_{dac} is set at 0.04% for the MIM capacitance. Design parameter space searched by our model-based optimization scheme is

- B: 1 ~ 4
- OSR: 8~96
- C_S: 0.1 ~1.7 pF
- A_0: 45 ~ 55 dB
- GBW: 80 ~ 400 MHz
- SR: 50 ~ 500 V/μs

- R: 100 ~ 300 Ω
- A_{in}: 0.1 ~ 0.9 V

The design published in [3] and that achieved from our methodology are listed in Table 6.1. The noise powers and distortion powers for both designs are listed in Table 6.2.

TABLE 6.1: Comparisons of our design results with those in [3]

Design parameters	**Reference [3]**	**K = 0.2**	**Unit**
B	3	2	-
OSR	96	96	-
C_S	1.7	1.12	pF
A_0	55	50	dB
GBW	**400**	**160**	MHz
SR	**500**	**201**	V/μs
A_{in}	300	300	V
SNDR reported in [33]	0.638	0.45	dB
SNDR(Our model)	78	-	dB
SNDR(SIMULINK)	**75.51**	**89.91**	dB
POWER(Our model)	75.17	87.08	mW

TABLE 6.2: The corresponding noise and distortion power for both designs

Non-ideality Power	**Reference [3]**	**K = 0.2**	**Unit**
$P_{Modified\_Quantization\_noise}$	-109.69	-103.95	dB
$P_{Switch\_thermal}$	-96.92	-95.11	dB
$P_{OTA\_thermal}$	-116.28	-111.97	dB
$P_{Settling\_noise}$	**-216.63**	**-115.63**	dB
P_{DAC_noise}	**-85.68**	**-123.17**	dB
P_{Jitter_noise}	-122.87	-125.90	dB
$P_{Correlation}$	-145.61	-123.36	dB
$P_{DC\text{-}gain\_distortion}$	-95.58	-102.58	dB
$P_{DAC\_distortion}$	**-77.05**	-	dB

Discussion 1: The design from model-based optimization is better than that of [3], achieving 89.91dB SNDR at 13.22mW compared with 75.51dB SNDR at 34.19mW in [3].

Discussion 2: Ref. [3] chose to use a 3-bit DAC without DWA, resulting in a dominating DAC distortion at -77.05dB and a large DAC noise at -85.68dB which brought

down SNDR. In contrast, our method by nature tries to evenly distribute noise power and distortion power among all noise and distortion categories, while minimizing POWER at the same time. This is the main reason our design can achieve a higher SNDR with lower POWER. Our algorithm selected a 2-bit DAC with DWA, eliminating DAC distortion and lowering DAC noise to -123.17dB.

Discussion 3: The power consumption by SDM of [3] is more than two times that of our SDM. This large power consumption is due to high values of GBW and SR used. Although large GBW and SR values indeed reduce Settling noise to -216dB in [3], this offered no help to boost SNDR.

Discussion 4: The SNDR computed by our model are verified by SIMULINK behavior simuation.

TABLE 6.3: Model-based optimization design results for different K values

Design parameters	**K = 1**	**K = 0.2**	**K = 0.04**	**Unit**
B	3	2	2	-
OSR	96	96	64	-
C_S	1.7	1.1	0.75	*pF*
A_0	50	50	50	*dB*
GBW	180	160	80	*MHz*
SR	201	201	100.5	*V/μs*
A_{in}	0.47	0.45	0.45	*V*
SNDR(Our model)	**91.69**	**89.83**	**85.47**	*dB*
POWER(Our model)	**23.11**	**18.78**	**8.98**	*mW*

Discussion 5: Table 6.3 shows model-based optimization design results for different K values. It can be observed form Table 6.3 that when K increases, more emphasis is on rising SNDR; when K decreases, more emphasis is on reducing POWER.

7
Conclusions and Future Works

In order to increase the speed of circuit design for sigma-delta ADCs, this thesis offers an efficient optimization method to achieve the most suitable circuit specifications. All the noise and distortion powers also can be obtained after optimization process is performed, and the dominant noise or distortion power can be attenuated by adjusting the design parameters. Our proposed method has acceptable accuracy and fantastic speed, and the flexibility can be enhanced by building more noise or distortion models for different circuit structures.

Further, in order to reduce the time-cost for optimization, the algorithm efficiently search the entire design parameters space to find the design parameter set which satisfies the specifications must to be established.

Appendix

The antiderivative of integrand in first matrix in equation (4.2) shows in equations (A.1) - (A.5).

$$\int_0^{V_H} av^2 e^{-\frac{v^2}{b}} dv = a\left(\frac{1}{4}b^{3/2}\sqrt{\pi}erf\left(\frac{v}{\sqrt{b}}\right) - \frac{1}{2}bve^{-\frac{v^2}{b}}\right)\Bigg|_0^{V_H} \tag{A.1}$$

$$\int_0^{V_H} av^4 e^{-\frac{v^2}{b}} dv = a\left(\frac{3}{8}b^{5/2}\sqrt{\pi}erf\left(\frac{v}{\sqrt{b}}\right) - \frac{1}{4}bv\left(3b+2v^2\right)e^{-\frac{v^2}{b}}\right)\Bigg|_0^{V_H} \tag{A.2}$$

$$\int_0^{V_H} av^6 e^{-\frac{v^2}{b}} dv = a\left(\frac{15}{16}b^{7/2}\sqrt{\pi}erf\left(\frac{v}{\sqrt{b}}\right) - \frac{1}{8}bv\left(15b^2+10bv^2+4v^4\right)e^{-\frac{v^2}{b}}\right)\Bigg|_0^{V_H} \tag{A.3}$$

$$\int_0^{V_H} av^8 e^{-\frac{v^2}{b}} dv = a\left(\begin{array}{l}\frac{105}{32}b^{9/2}\sqrt{\pi}erf\left(\frac{v}{\sqrt{b}}\right) \\ -\frac{1}{16}bv\left(105b^3+70b^2v^2+28bv^4+8v^6\right)e^{-\frac{v^2}{b}}\end{array}\right)\Bigg|_0^{V_H} \tag{A.4}$$

$$\int_0^{V_H} av^{10} e^{-\frac{v^2}{b}} dv = a\left(\begin{array}{l}\frac{945}{64}b^{11/2}\sqrt{\pi}erf\left(\frac{v}{\sqrt{b}}\right) \\ -\frac{1}{32}bv\left(945b^4+630b^3v^2+252b^2v^4+72b^1v^6+16v^8\right)e^{-\frac{v^2}{b}}\end{array}\right)\Bigg|_0^{V_H} \tag{A.5}$$

where

$$a = \frac{V_H}{\int_0^{V_H}\frac{1}{\sqrt{2\pi}}\exp\left(-\frac{V_s}{2\sigma^2}\right)dV_s}\frac{1}{\sqrt{2\pi}\sigma_{V_S}}$$

$$b = 2\sigma_{V_S}{}^2$$

The antiderivative of integrand in second matrix in equation (4.2) shows in equations (A.6) - (A.8).

$$\int_{V_L}^{V_H} av^1 e^{-\frac{v^2}{b}} e^{\frac{v}{c}} dv = -a\left(\frac{1}{4c}b^{3/2}\sqrt{\pi}e^{\frac{b}{4c^2}}erf\left(\frac{b-2cv}{2\sqrt{bc}}\right) + \frac{1}{2}be^{\frac{v}{c}-\frac{v^2}{b}}\right)\Bigg|_{V_L}^{V_H} \tag{A.6}$$

$$\int_{V_L}^{V_H} av^3 e^{-\frac{v^2}{b}} e^{\frac{v}{c}} dv = -a \left(\begin{array}{l} \frac{1}{16c^3} b^{5/2} \left(b+6c^2\right) \sqrt{\pi} e^{\frac{b}{4c^2}} erf\left(\frac{b-2cv}{2\sqrt{bc}}\right) \\ +\frac{1}{8c^2} be^{\frac{v}{c}-\frac{v^2}{b}} \left(b^2+2bc\left(2c+v\right)+4c^2v^2\right) \end{array} \right) \Bigg|_{V_L}^{V_H} \tag{A.7}$$

$$\int_{V_L}^{V_H} ax^5 e^{-\frac{v^2}{b}} e^{\frac{v}{c}} dv = -a \left(\begin{array}{l} \frac{1}{64c^5} b^{7/2} \left(b^2+20bc^2+60c^4\right) \sqrt{\pi} e^{\frac{b}{4c^2}} erf\left(\frac{b-2cv}{2\sqrt{bc}}\right) \\ +\frac{1}{32c^4} e^{\frac{v}{c}-\frac{v^2}{b}} \left(\begin{array}{l} b^4+2b^3c\left(9c+v\right)+4b^2c^2\left(8c^2+7cv+v^2\right) \\ +8bc^3\left(4cv^2+v^3\right)+16c^4v^4 \end{array} \right) \end{array} \right) \Bigg|_{V_L}^{V_H} \tag{A.8}$$

where

$$a = \frac{V_H}{\int_0^{V_H} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{V_s}{2\sigma^2}\right) dV_s} \frac{1}{\sqrt{2\pi}\sigma_{V_S}} V_L \cdot \beta \cdot e^{-1}$$

$$b = 2\sigma_{V_S}{}^2$$

$$c = V_L$$

Besides, Erf donates the error function in equations (A.1) - (A.8), and is defined as

$$erf\left(x\right) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \tag{A.9}$$

Erf has Taylor expansion and is expressed as

$$\frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt = \frac{2}{\sqrt{\pi}} \sum_{n=0}^{\infty} \frac{\left(-1\right)^n x^{2n+1}}{n!\left(2n+1\right)} \tag{A.10}$$

The antiderivative of integrand in equation (4.7) shows in equation (A.11).

$$\int_0^{\infty} \frac{a+bx^2}{\left(cx^2+1\right)^2+dx^2} dx = \frac{1}{\sqrt{2}c\sqrt{d}\sqrt{4c+d}} \cdot \left\{ \begin{array}{l} \frac{\left(2ac^2-b\left(-\sqrt{d\left(4c+d\right)}+2c+d\right)\right)}{\sqrt{-\sqrt{d\left(4c+d\right)}+2c+d}} \cdot \tan^{-1}\left(\frac{\sqrt{2}cx}{\sqrt{-\sqrt{d\left(4c+d\right)}+2c+d}}\right) \\ +\frac{\left(-2ac^2+b\left(\sqrt{d\left(4c+d\right)}+2c+d\right)\right)}{\sqrt{\sqrt{d\left(4c+d\right)}+2c+d}} \cdot \tan^{-1}\left(\frac{\sqrt{2}cx}{\sqrt{\sqrt{d\left(4c+d\right)}+2c+d}}\right) \end{array} \right\} \Bigg|_0^{\infty} \tag{A.11}$$

where

$$a = \left(2a_1 + 1\right)^2$$

$$b = R^2 C_S{}^2 \left(a_1 + 1\right)^2$$

$$c = \frac{A\omega^2 R C_S \left(a_1 + 1\right)}{GBW}$$

$$d = RC_S + \frac{A\left(2a_1 + 1\right)}{GBW}$$

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