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博 士 論 文

應用於超寬頻通訊系統之互補式金氧半毫米波積體電路設計與分析

The Design and Analysis of CMOS Millimeter-Wave Integrated Circuits for Ultra-Wideband Communication Systems

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摘要

可預期的，未來利用無線傳輸的資料量與其所需頻寬將與日俱增，因此毫米波頻段的超寬頻系統在個人通訊上的使用亦將無可避免。針對此應用，本論文提出了數種互補式金氧半製程關鍵積體電路元件的架構、設計方式與分析，其中包含了 (1) 直接注入式鎖定除頻器的模組、分析與設計，(2) 應用於降頻的三階諧波主動式混波器，(3) 直接降頻接收機前置電路的設計與分析，(4)一個適用於毫米波頻段的多頻段寬頻壓控震盪器。而另一個射頻頻段的低電壓多頻段寬頻壓控震盪器也在此提出。

首先，本論文將分析適用於毫米波頻段的直接注入式鎖定除頻器，並且將建立其等效模組，利用此模組將可歸納出數個設計規則用以最佳化除頻器的效能，如頻率鎖定範圍。為了驗證所提出的等效模組與設計規則，一個不使用可變電容的直接注入式鎖定除頻器採用了 0.13 微米的互補式金氧半製程來製作。在此除頻器中，P 型電晶體電流源將用以限制其輸出電壓振幅與增加輸入電晶體的直流驅動跨壓以加大頻率鎖定範圍。此除頻器的輸入電晶體長寬分別僅為 0.12 與 3.6 微米，而所量測到的中心頻率與頻率鎖定範圍分別為 70GHz 與 13.6%。在 1V 的工作電壓下，其功率消耗為 4.4mW。

其次，本論文提出了一個應用於降頻的三階諧波主動式混波器與其設計考量。此混波器所需的本地振盪頻率僅為傳統基頻混波器的三分之一。因此，與此混波器整合的壓控震盪器之頻率操作範圍將可被大幅的增進。再者，由於所提出之混波器利用本地振盪訊號的三階諧波降頻，而三階諧波的極性特徵與基頻完全相同，因此此混波器將可基頻混波器一樣輕易的擁有平衡架構。此混波器與一整合的壓控震盪器採用了 0.13 微米的互補式金氧半製程製作。量測結果顯示整合壓控震盪器的中心頻率為 19.48GHz 而頻率操作範圍可達 13.35%，其相對應的射頻頻率可由 54.54GHz 至 62.34GHz。在此射頻頻率範圍中，混波器的平均增益為 7.8dB，且增益變化不超過 2.2dB。其 1dB 增益下降點約為-10.2dBm，而在 1.2V 的工作電壓下，其與壓控震盪器平均功率消耗分別為 6.6 與 0.36mW。

再其次，利用所提出之三階諧波主動式混波器，本論文提出了一個適用於毫米波頻段超寬頻系統的直接降頻接收機，並且使用 0.13 微米互補式金氧半製程設計。此接收機包含了一個低雜訊放大器、一對三階諧波主動式混波器、基頻放大器、輸出級與一個正交壓控震盪器。由於使用三階諧波混波器而降低了所需的本地震盪頻率，正交壓控震盪器的頻率操作範圍將可被大幅的增進。模擬結果顯示，當中心頻率為 20.35GHz 時，正交壓控震盪器的頻率操作範圍可達 19.87%，其相對應的射頻頻率已足以涵蓋整個毫米波於美國之開放頻段，57 – 64GHz。而在此頻段中，接收機的增益在 25 至 29.25dB 間，且其雜訊指數在 11.1 至 13.4dB 間。接收機的 1dB 增益下降點約為-28dBm，而正交壓控震盪器在操作頻段中 1MHz 偏移頻率的平均相位雜訊為-96dBc/Hz。接收機的工作電壓為 1.2V，平均功率消耗為 35.6mW。

最後，本論文提出了兩個不同的多頻段寬頻壓控震盪器。其中之一適用於毫米波頻段。其使用可變電感調整振盪頻率。使用此可變電感調整振盪頻率，壓控振盪器將可擁有寬頻且多頻段的特性，且其振盪頻率亦不會因此而有所犧牲。利用 90 奈米互補式金氧半製程設計與製作，量測結果顯示，所提出之壓控振盪器

的振盪頻率可由 52.2 調整至 61.3GHz。相對應的中心頻率與調整範圍則分別為為 56.75GHz 與 16%。當振盪頻率為 61.3GHz 時，10MHz 偏移頻率的相位雜訊為-118dBc/Hz，而振幅約為-4.55dBV。在 0.7V 的工作電壓下，其功率消耗為 8.7mW，晶片面積為 0.28×0.36 平方公釐。

另一個所提出的多頻段寬頻壓控震盪器則適用於數 GHz 的射頻頻段與低電壓操作。除了射頻頻段的應用外，此壓控震盪器亦可做為毫米波外差式接收機的中頻本地振盪訊號源。其使用了反轉型電晶體可變電容且利用一個大電阻隔絕基底的寄身效應以增大頻率調整範圍。為了降低壓控震盪器增益以增進相位雜訊效能，此壓控震盪器亦使用了多頻帶切換技術。以 0.18 微米互補式金氧半製程設計，模擬結果顯示，當工作電壓與頻率調整電壓均為 0.8V 時，其頻率調整範圍可由 4.4 至 5.9GHz，調整百分比為 29.12%。當振盪頻率為 5.52GHz 時，在 1-MHz 偏移頻率的相位雜訊為-109.65dBc/Hz，功率消耗為 1.2mW。

經由模擬與量測結果證實，本論文所提出的關鍵積體電路元件將可用於高效能、高整合度、全補式金氧半製程的毫米波頻段超寬頻無線通訊系統中。在未來將針對其他的毫米波頻段積體電路元件整合而成為一個完整的收發器。

The Design and Analysis of CMOS Millimeter-Wave Integrated Circuits for Ultra-Wideband Communication Systems

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ABSTRACT

In this thesis, the design methodologies and implementation techniques of CMOS integrated circuits (ICs) for millimeter-wave (MMW) ultra-wideband (UWB) applications are presented. There are four different kinds of MMW ICs presented in this thesis, including: 1) a direct injection-locked frequency divider; 2) a down-conversion third-order sub-harmonic active mixer; 3) a MMW UWB homodyne receiver front-end; and 4) two multi-band voltage-controlled oscillators (VCOs) with a large frequency tuning range in MMW band and RF band for low-voltage applications.

At first, direct injection-locked frequency dividers operated in the millimeter-wave band are analyzed. An analytically equivalent model of the direct injection-locked frequency dividers is developed and important design guidelines for a large frequency locking range are obtained. A direct injection-locked frequency

divider without varactors is designed and fabricated using 0.13-μm bulk- CMOS process to verify the developed model and design guidelines. The size of the input device is only 3.6μm/0.12μm and the measured frequency locking range is 13.6% at 70GHz with a power consumption of 4.4mW from a supply voltage of 1V.

Secondly, a down-conversion third-order sub-harmonic active mixer is analyzed and fabricated with an on-chip VCO using 0.13-μm CMOS technology. The required LO frequency is one third of that required in a fundamental mixer. Because of the decrease in the LO frequency, the frequency tuning range of the integrated VCO can be extended significantly. Moreover, with the essential differential characteristics of the third harmonic components of LO signals, a balanced structure can be achieved without any extra effort as a fundamental mixer. From the measurement results, it can be observed that the tuning range of the VCO is 13.35% at 19.48 GHz with the corresponding RF frequency range from 54.54 to 62.34 GHz. The average gain of the proposed mixer is 7.8 dB and the variation is smaller than 2.2 dB within the tuning range. The input 1-dB compression point is around –10.2 dBm and the power leakage of the 2LO/LO signal at the RF port is smaller than –35/–42.5 dBm, respectively. The average power consumption of the VCO and the mixer core within the operating frequency range are 6.6 and 0.36 mW, respectively.

Thirdly, a homodyne receiver using third-order sub-harmonic active mixers is analyzed and designed by using 0.13-μm CMOS technology. The receiver consists of a low-noise amplifier (LNA), sub-harmonic active mixers, baseband amplifiers, output buffers, and a qudrature VCO. Due to the reduction in the required LO frequency by using the sub-harmonic mixers, the frequency tuning range of the integrated quadrature VCO can be significantly extended. From ADS and SpectreRF

simulation results, the frequency tuning range of the qudrature VCO is 19.87% at 20.35 GHz and the corresponding RF frequency range is sufficient to cover the entire MMW unlicensed band in the U.S. (i.e. 57 – 64 GHz). The gain of the receiver within the unlicensed band is form 25 to 29.25 dB and the noise figure is from 11.1 to 13.4 dB. The 1-dB compression point occurs around -28 dBm. The phase noise of the quadrature VCO at 1-MHz offset is -96 dBc/Hz. The average power consumption of the receiver is 35.6 mW from a supply voltage of 1.2 V.

Finally, two different multi-band VCOs with wide tuning range are proposed. One of them is operated in the MMW band. It employs a single variable inductor for frequency tuning. By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operations are achieved without sacrificing its operating frequency. Fabricated in a 90-nm CMOS process, the VCO is capable of covering frequency range from 52.2 to 61.3 GHz. The tuning percentage is 16% at 56.75 GHz. The measured average phase noise within the tuning range is about -102.4 dBc/Hz at 10-MHz offset. The maximum oscillation voltage amplitude is around -4.55 dBV. The VCO core dissipates 8.7 mW from a 0.7-V supply. Chip size is 0.28×0.36 mm^2.

The other VCO is operated around 5 GHz which can be chosen as the intermediate frequency in an MMW heterodyne receiver. In this situation, the designed VCO can be used as the LO signal generator in the MMW heterodyne receiver to downconvert the intermediate frequency signals to the baseband. Inversion-mode MOS (I-MOS) varactors are used in the VCO to maintain a wide tuning range in the situation that the supply and tuning voltage is lower than 1V. Moreover, a large resistor is inserted between ground and bulk terminals of each I-MOS varactor to further improve the tuning capability. Through this resistor, the

tuning range is increased by 500 MHz (50%). A bandswitching topology is used to ameliorate the adverse effects of highly sensitive I-MOS varactors. The VCO is designed using 0.18-μm CMOS technology. With a 0.8-V supply, it is shown from simulation results that the VCO has a tuning range of 29.12% from 4.4 to 5.9 GHz when tuned from 0 to 0.8 V. The simulated phase noise is -109.65 dBc/Hz at 1-MHz offset from the 5.52-GHz carrier. The power consumption is 1.2 mW.

It is believed that the proposed IC components can be applied to the design of high-performance high-integration all-CMOS wireless communication systems for MMW UWB applications. Further research on the integration of other transceiver components to form all-CMOS MMW UWB systems will be conducted in the future.

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虞　繼　堯

誌於　風城交大

九十七年　初夏

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

In the last few years, 7 GHz of contiguous bandwidth have been opened for unlicensed use at millimeter-wave (MMW) frequencies in the U.S. (57-64 GHz) and Japan (59-66 GHz). This allows for various application systems in ultra-wideband (UWB) communication including wireless local area networks (WLANs) with extraordinary capacity, point-to-point ultra-high speed communications (e.g. local multipoint distribution system), short-range high-data-rate Wireless Personal Area Networks (WPANs), local rebroadcasting of high throughput data source (e.g. high definition television within a home), and vehicular radar. With continuing advance of CMOS technologies into nanometer regime, the unit-gain frequency f_T of a CMOS device is beyond 100 GHz. Thus using CMOS technologies to implement integrated circuits operated at MMW frequencies becomes realizable [1]-[3]. With advantages of lower cost and a higher integrated level, CMOS MMW IC components for wireless communication systems have attracted increasing interest and research, recently.

In general, a wireless communication system consists of three functional sub-systems, namely, receiver, transmitter, and frequency synthesizer. The receiver usually includes low-noise amplifiers (LNAs) and down-conversion mixers to perform amplification, downconversion, and demodulation on the received signals. The transmitter includes up-conversion mixers and power amplifiers (PAs) to perform modulation, upconversion, and amplification on the transmitted signals. The frequency synthesizer is used to generate local oscillation (LO) signals in the system.

Its main blocks with the highest operating frequency are the voltage-controlled oscillators (VCOs) and the frequency dividers. The performance of a communication system depends heavily on each of the IC components mentioned above. However, when the operating frequency increases to the MMW band, the substrate loss and low-quality passives in CMOS technology significantly impact the performance of these IC components. Therefore, to maintain high performance in the MMW band, the IC components should be carefully designed and optimized with the help of accurate electromagnetic (EM) simulations to model all passive device/parasitics including routing paths.

In this thesis, the main research focus is on CMOS MMW IC components for UWB communication systems. It includes a frequency divider with a wide frequency locking range, a sub-harmonic mixer suitable for UWB systems, a UWB receiver using the sub-harmonic mixer, and a multi-band VCO with a wide frequency tuning range. Several key IC components will be briefly reviewed in the following subsections.

1.2 REVIEW ON CMOS IC COMPONENTS

1.2.1 FREQUENCY DIVIDER

In general, phase-locked loops (PLLs) are extensively used in CMOS RF front-end systems as frequency synthesizers or clock sources to generate local oscillating signals. In an MMW PLL, the main blocks with the highest operating frequency are typically the VCO and the frequency divider. More specifically, the main design issues of an MMW VCO concern the oscillating frequency tuning range, phase noise, power consumption and output power level [4]-[19]. Most of these

degrade as the input capacitance of the next stage which may be a frequency divider, increases. Therefore, the reduction of the input capacitance of the divider becomes very important as the operating frequency to the MMW band increases. In addition, the wide operating frequency range of the divider is also important for MMW UWB applications. A small operating frequency range will become a bottleneck to extend the operating bandwidth of the MMW PLL. Therefore, the main design challenge facing the MMW divider designers is to reduce input capacitance while maintaining a wide operating frequency range. As in other integrated CMOS RF circuits, power consumption and noise performance are also important in divider design.

Frequency dividers generally can be divided into two groups: flip-flop-based static frequency dividers [20]-[24] and injection-locked frequency dividers (ILFDs) [26]-[38]. The block diagram of a 2:1 flip-flop-based static frequency divider is shown in Fig. 1.1. The internal dividing function is based on a master-slave D-type flip flop by connecting the inverted slave outputs to the master inputs. Such divider usually has a large operating frequency range because it can be operated down to a very low frequency. However, its frequency capability is dominated by the maximum operating frequency of the latches which usually is difficult to reach MMW band in bulk-CMOS technologies. Moreover, the operating frequency becomes even lower if lower power consumption is required.

In comparison with flip-flop-based static frequency dividers, ILFDs generally have lower power consumption and higher frequency capability. However, operating at MMW frequency with a small input capacitance is still difficult by using a conventional LC-based ILFD [26]-[28] as shown in Fig. 1.2. The input stage M_{in} is used to provide both an input signal path and a DC bias path. Thus, M_{in} is typically

large, resulting in a large input capacitance. Moreover, the input signal is significantly degraded by the parasitic capacitor C_{tail} in Fig. 1.2. By using a peaking inductor between the drain terminal of M_{in} and the ground, this problem can be reduced [29]; however, this strategy requires a greater chip area. Moreover, the Miller divider proposed in [39] faces the same problems of a large input capacitance and the need for a peaking inductor.

Recently, a direct injection-locked structure [33]-[38] is widely used for MMW frequency division due to its small input capacitance. A typical direct ILFD [34] is shown in Fig. 1.3. At MMW frequency, the input devices M_{inp} and M_{inn} are usually small to satisfy the specifications of the input capacitance. Such small input devices result in a small injection current and limit the frequency locking range. Therefore, it is important to optimize the frequency locking range of an MMW direct ILFD for UWB applications.

The frequency locking range of a conventional ILFD in Fig. 1.2 has been derived in previous work [25]-[28]. All of them indicate that the phase-limited frequency locking range is inversely proportional to the quality factor (Q factor) of the LC resonator. This result was adopted in the design of direct ILFD [34]-[35] without theoretical verification on the correctness of theory and design. So far, the analytical model and design guidelines for a direct ILFD have not been developed to optimize the frequency locking range.

1.2.2 DOWNCONVERSION MIXER

Downconversion mixer is one of key circuit components in a receiver for frequency translation. The mixers have two distinctly different inputs, namely, the RF

port and the LO port. The RF port senses the signal to be downconverted and the LO port senses the signal generated by the local oscillator, usually a VCO. In general, the main design issues of a downconversion mixer are conversion gain, linearity, noise figure, and port-to-port isolation [40]-[59]. However, when the LO frequency is increased to the MMW unlicensed band, a new problem emerges in bulk-CMOS mixer design for UWB applications. It becomes difficult to integrate the conventional fundamental mixer with a VCO whose frequency tuning range covers the entire MMW unlicensed band, because the input capacitance of the LO port usually is too large. Therefore, it can only be used in narrow band applications [65]-[69].

One solution to increase the frequency tuning range of integrated VCO is to use sub-harmonic mixers to decreases the required LO frequency. Most previous work of sub-harmonic mixers in bulk-CMOS technology [53]-[59] employ second harmonic component of LO signals for frequency conversions. However, for a differential LO signal, the second harmonic component is a single-phase harmonic. By directly using this component, a non-balanced structure can be developed [53]-[54]. Such a non-balanced structure is rarely adopted in the receiver for wireless communication because its LO-to-RF port isolation is poor. Thus the receiver usually prefers differential output signals to reject the common-mode noise. In order to obtain a balanced structure, a differential RF signal or a quadrature LO signal [55]-[59] is required. In comparison with a balanced fundamental mixer, this significantly increases the complexity of circuit design when the mixer is integrated into a receiver.

The third harmonic component of the LO signal has the same polarity as the fundamental component. Therefore, a sub-harmonic mixer employing the third component can retain the balanced structure as a fundamental counterpart with a

single-phase RF signal and a differential LO signal. Moreover, the required LO frequency is lower than those of the mixers using the second harmonic components. So far, the third harmonic component of the LO signal has been successfully used for frequency conversion in a passive downconversion mixer [53]. However, the mixer has a large conversion loss and is still a non-balanced structure which is not suitable for receiver applications in wireless communication.

1.2.3 RECEIVER

Receivers for wireless communication can be divided into two types: heterodyne and homodyne receivers [40]. Both structures have been used in bulk-CMOS receivers operated around the 60-GHz unlicensed band [60]-[69].

A general block diagram of MMW heterodyne receivers is shown in Fig. 1.4. The selection of the intermediate frequency (IF) is an important design issue. For a relatively low IF [61]-[63], the required oscillation frequency of VCO_{RF} is high and the image-reject circuit, which usually degrades the LNA performance, is required to improve the image-reject ratio. For higher IF [60], the required oscillation frequency of VCO_{RF} is lower and the image-reject circuit is not required if the image is well out of band and can be strongly rejected by LNA. The expense of higher IF is that it requires a higher-frequency quadrature LO signal (e.g. VCO_{IF} in Fig. 1.4) or a high-frequency broad-band phase shifter at IF signal path, which degrades the RF mixer performance. Moreover, the band-pass filter for channel selection for a higher IF usually is more complicated to maintain the selectivity [40].

The half-IF receiver shown in Fig. 1.5 [64] is a special case of heterodyne receivers. The main advantage of the half-IF receiver in the MMW band is that the

required oscillation frequency of the VCO is only a half of the frequency of input RF signal. This benefits VCO integration. However, as shown in Fig. 1.5, a high-frequency broad-band poly-phase filter in the RF path and two RF mixers are required to reject the image introduced by the third harmonic of the LO in the RF mixing operation. Moreover, if channel selection needs to be performed in the IF paths, two well match and complex band-pass filters should be inserted into the IF paths. These requirements significantly increase the chip area, integration difficulty and design complexity.

In comparison with heterodyne receivers, the structure of homodyne receivers is more compact as shown in Fig. 1.6. Conventional problems in the homodyne receiver are LO leakage, flicker noise, and DC offset [40]. However, when the operating frequency increases around the 60-GHz unlicensed band, homodyne receivers [65]-[69] suffer from a new problem of the quadrature VCO (QVCO) integration for UWB applications. The required oscillating frequency of the QVCO is too high to maintain its frequency tuning range in bulk-CMOS technologies. Therefore, the main design challenge of the MMW homodyne receiver is to extend the operating frequency range without decreasing the operating frequency while maintaining its relatively simple structure.

1.2.4 VOLTAGE-CONTROLLED OSCILLATOR

In the RF transceiver front-end, LC-tank voltage-controlled oscillators (VCOs) are extensively used in frequency synthesizers to provide local carriers for up and down frequency conversion. In general, the specifications of VCOs such as oscillating frequency, phase noise, output power level, and frequency tuning range significantly affect the performance of the RF transceiver. Therefore, a high-performance

bulk-CMOS VCO is usually required for a highly integrated communication system.

Conventionally, MOS varactors are used in LC-tank VCOs for frequency tuning and can be divided into two types: inversion-mode MOS (I-MOS's) and accumulation-mode MOS (A-MOS's) varactors. At several GHz, an I-MOS varactor provides a larger frequency tuning range than an A-MOS varactor [70], especially in the case of a low tuning voltage. By using deep n-well and inserting a large resistor between the I-MOS bulk and ground, the tuning range can be extended further [84]. However, because the electron concentration in the inversion layer cannot change instantaneously, the maximum operation frequency of published VCOs using I-MOS varactor is around 10GHz [85]. Therefore, for MMW applications, such VCO only can be used in a heterodyne receiver to downconvert the IF signal to the baseband (i.e. VCO_{IF} in Fig. 1.4).

LC-tank VCOs operated in the MMW band usually employ A-MOS varactors for frequency tuning [5]-[19]. Fig. 1.7 shows a widely used LC-tank MMW VCO structure. The negative resistance is provided by an NMOS cross-coupled pair to maintain the oscillation. The inductors are implemented by an on-chip center-tapped metal coil. C_{load} represents the capacitance from the next stages, e.g. buffers, frequency dividers, or mixers. Obviously, the sizes of the A-MOS varactors dominates the maximum to minimum capacitance ratio of the LC tank and the frequency tuning range for a given cross-coupled pair and C_{load}. However, when the oscillating frequency is increased to the MMW band, the sizes of the varactors are strictly limited because of two reasons. Firstly, for the same cross-coupled pair and C_{load}, the sizes of varactors should be decreased to decrease the total capacitance of the LC tank for MMW oscillation. Secondly, the quality factor of the LC tank is dominated by the

varactors in the MMW band [17]. Thus small varactors are desired to maintain the quality factor of the LC tank and the oscillation. With these two reasons, the published bulk-CMOS MMW VCOs above 50 GHz [8]-[19] usually suffer form a narrow frequency tuning range which makes the circuits sensitive to process variation and less feasible for UWB applications. To extend the frequency tuning range of the structure shown in Fig. 1.8, the circuit layout should be carefully optimized and some test chips are required for device size trimming [17].

In comparison to the VCO operated at several GHz, the same frequency tuning percentage of an MMW VCO results in a relatively large VCO gain. Therefore, for a wide-tuning-range MMW VCO for UWB applications, multi-band operation is required to degenerate the VCO gain and alleviate phase noise performance when integrated into a broadband frequency synthesizer. However, the conventional capacitor bank for multi-band operation [71]-[74] is no longer applicable at MMW oscillating frequency because its parasitic capacitance is too large. Therefore, a new tuning strategy is required for an MMW VCO to achieve a wide frequency tuning range and multi-band operation without degrading its oscillating frequency.

1.3 ORGANIZATION OF THIS THESIS

It is the aim of this thesis to analysis and design bulk-CMOS ICs for MMW UWB applications. The thesis includes an analytical model and optimization of MMW direct injection-locked frequency divider, the design of third-order sub-harmonic mixer with an on-chip wide-tuning-range VCO, the design of homodyne receiver for MMW UWB applications, and a new frequency tuning strategy for an MMW VCO. Moreover, a wide-tuning-range RF VCO for low-voltage

applications is presented. The VCO can be used as a local signal generator in a MMW heterodyne receiver to downconvert the IF signal to the baseband.

In Chapter 2, an analytical model and design guidelines of a direct ILFD are presented. The proposed model herein reveals that for a direct ILFD, increasing the quality factor of the LC resonator can reduce the power consumption without reducing the frequency locking range. This result differs from the conventional one. Based on the developed model and guidelines, the design methodology for a MMW direct ILFD is given. The phase noise analysis of a direct ILFD is also presented in this chapter. It is shown from simulation results that a direct ILFD has good noise suppression capability in the MMW band. Based on the proposed design methodology, a direct ILFD without a varactor is designed and fabricated by using 0.13-μm bulk-CMOS technology. For comparison purpose, the other direct ILFD using an LC resonator with a lower quality factor is also fabricated on the same chip. Finally, the experimental results are summarized.

In Chapter 3, a new down-conversion third-order active sub-harmonic mixer with on-chip VCO is proposed and designed for MMW UWB applications. The equation of the frequency tuning range of a VCO with A-MOS varators is derived in this chapter. It shows that the frequency tuning range is inversely proportional to the square of the oscillating frequency. Many VCOs are simulated by using HSPICE to verify the theoretical result. The proposed mixer consists of two common-gate amplifiers with differential LO signals from the VCO applied to their gate terminals to modulate the transconductances for frequency conversion. In comparison to a fundamental or second-order sub-harmonic mixer, the tuning range of the integrated VCO can be improved by reducing the oscillating frequency, while retaining the

balanced structure. Moreover, with proper design, the conversion gain of the mixer can be made much larger than that of a passive mixer with only a small increase in the power consumption. With input matching and isolation improving circuit, the proposed mixer with on-chip VCO is fabricated using 0.13-μm bulk-CMOS technology. The experimental results are presented.

In Chapter 4, a homodyne receiver is designed for MMW UWB applications by using the proposed mixer in Chapter 3 and 0.13-μm bulk-CMOS technology. The receiver includes a broadband-matching LNA, active sub-harmonic mixers, a quadrature VCO, IF amplifiers, and output buffers. A single common-source NMOS structure with a source degeneration inductor is used as the first stage of the LNA. From ADS and SpectreRF simulations, the structure has better noise figure and input matching bandwidth in the MMW band in comparison with the conventional cascode structure. Because the required LO frequency is reduced by using the sub-harmonic mixers, the frequency tuning range of the integrated quadrature VCO can be significantly extended. From ADS and SpectreRF simulation results, the tuning range can cover the entire MMW unlicensed band (i.e. 57 – 64 GHz). The IF amplifiers are used to enhance the voltage gain and bandwidth of the receiver. The output buffers are used to drive off-chip 50-Ω load. The ADS post-simulation results of the whole receiver are also given in this chapter. It is shown that the proposed homodyne receiver provides a solution to extend the operating frequency range to the MMW band while maintaining a simple structure.

In Chapter 5, an MMW VCO with a single variable inductor (VID) for frequency tuning is proposed and analyzed. The VID consists of a transformer and a variable resistor. The equivalent inductance of the VID can be varied by adjusting the

resistance of the variable resistor. From the analysis, the lower bound of the frequency tuning range of the VCO with the proposed VID is independent of the oscillating frequency. Therefore, the frequency tuning range is not degraded even when the oscillating frequency is up to MMW band. Moreover, the VID can be modified to achieve multi-band operation by decomposing the variable resistor into several smaller parts. It is shown that the multi-band operation can be achieved without sacrificing the oscillating frequency. The experimental prototype of the VCO is fabricated in 90-nm CMOS technology and the experimental results are presented.

Another RF multi-band VCO for low-voltage applications is also proposed in this chapter. To maintain a fine frequency tuning range in the case of low tuning voltage, I-MOS varactors are used for bandswitching and frequency tuning because of their natural abrupt gradient of the C-V curve (i.e. capacitance relative to tuning voltage curve). A large resistor which connects ground and each I-MOS bulk terminal is used to isolate the I-MOS gate-to-bulk parasitic capacitance and improve the tuning range further. The VCO is designed by using 0.18-μm bulk-CMOS technology and the simulation results are presented.

In Chapter 6, conclusions and future work are given.

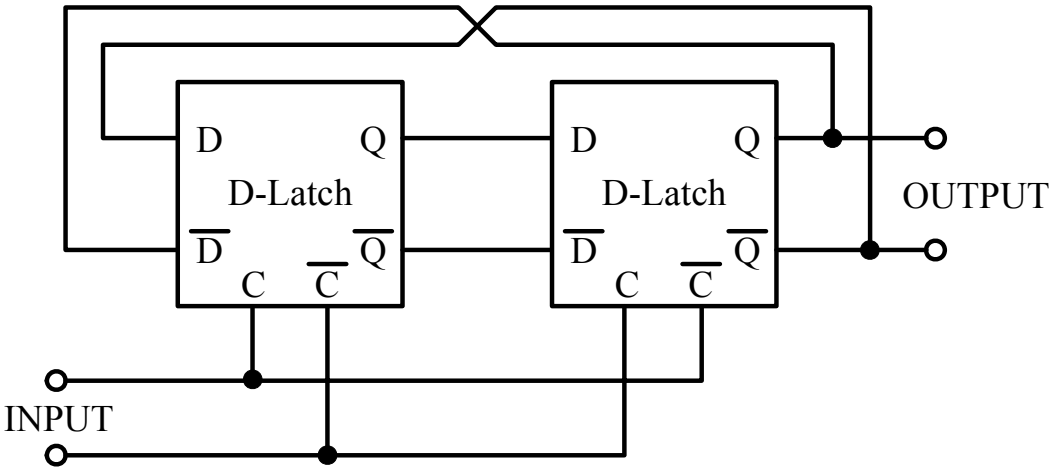


Fig 1.1 2:1 flip-flop-based static frequency divider.

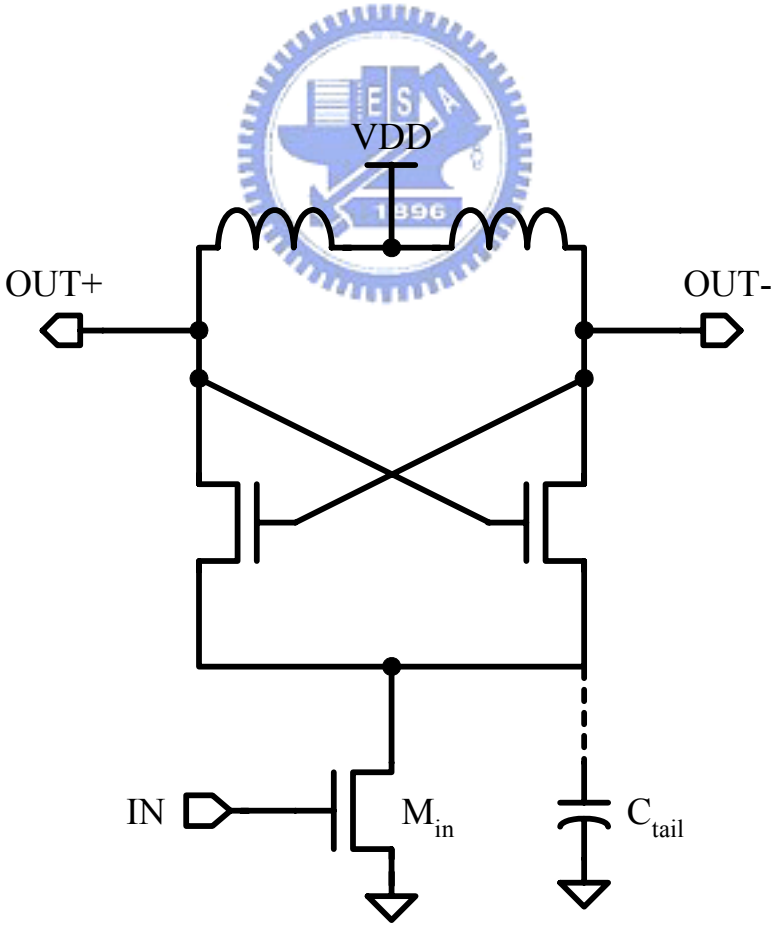


Fig 1.2 Conventional LC-based ILFD.

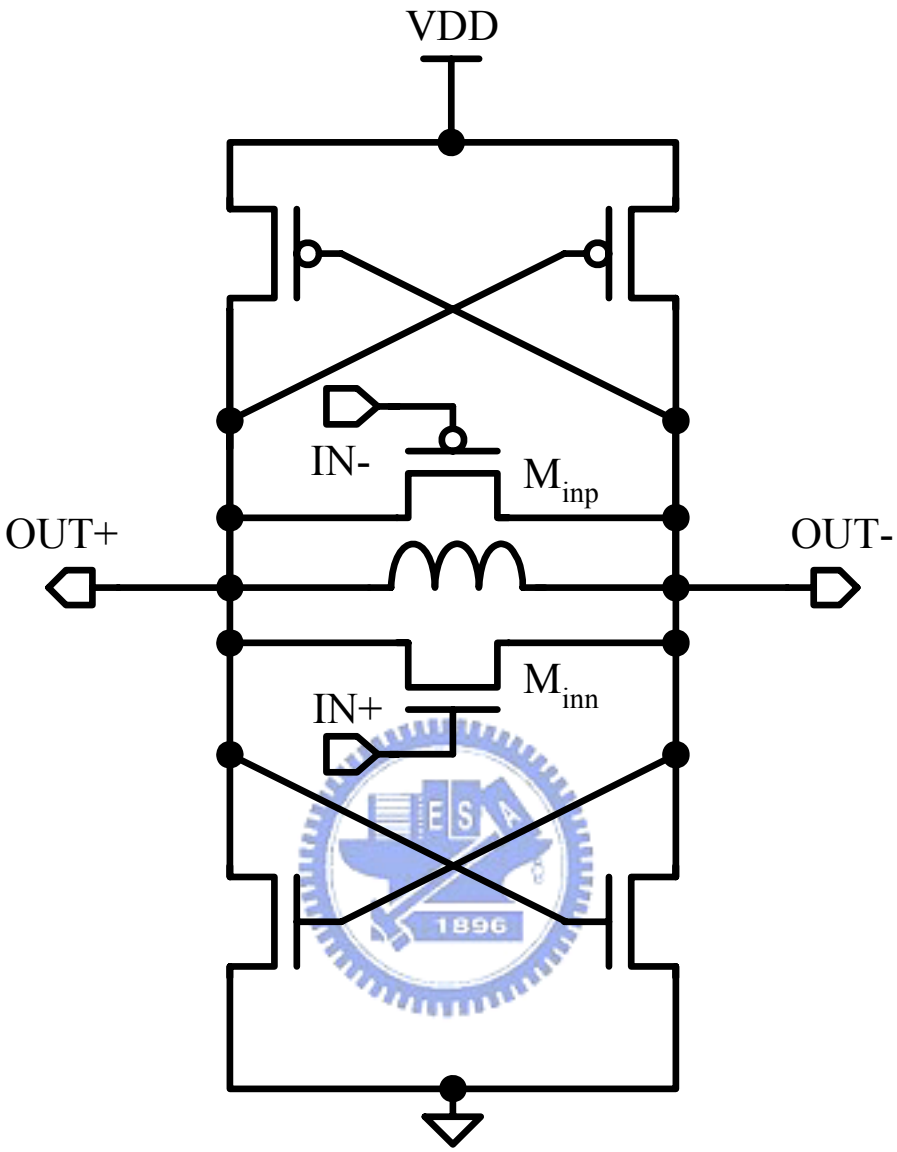


Fig 1.3 Direct ILFD.

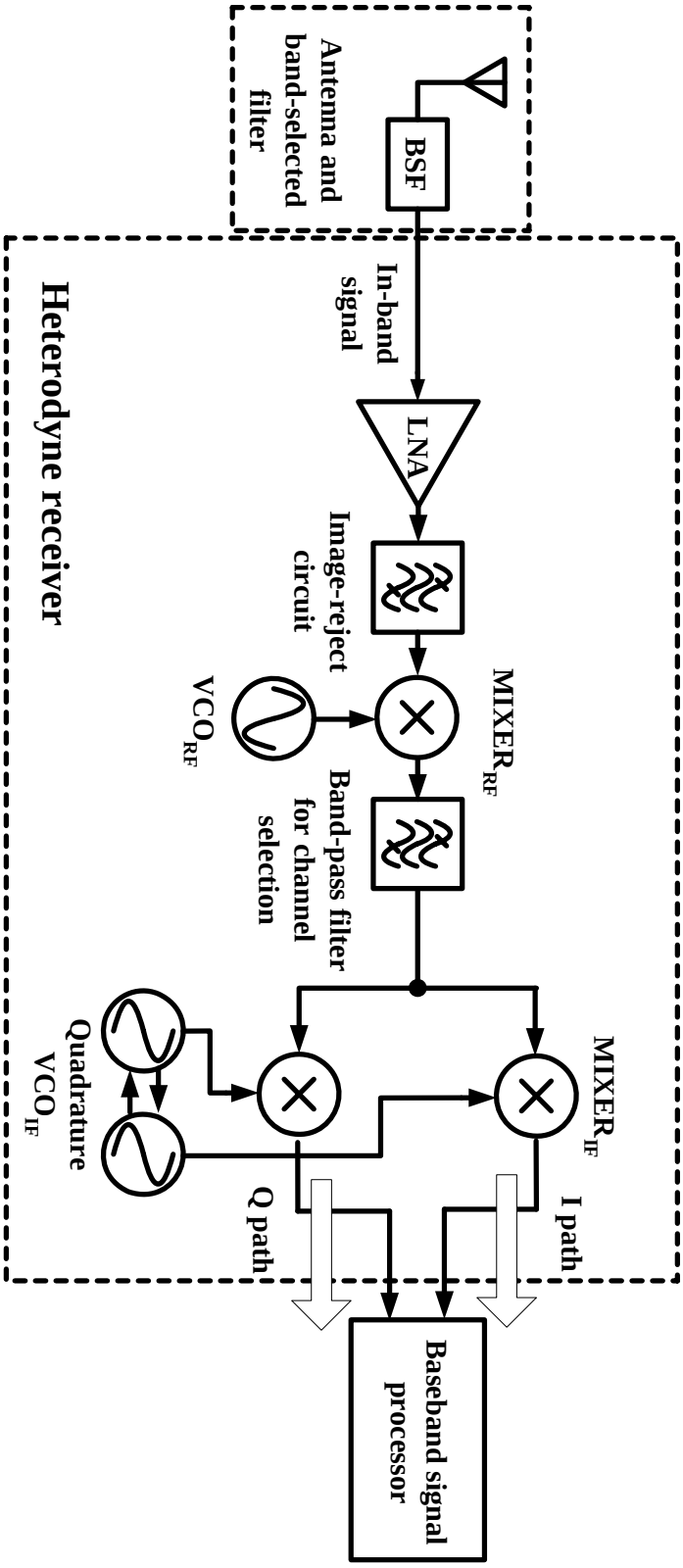


Fig 1.4 Block diagram of the heterodyne receiver.

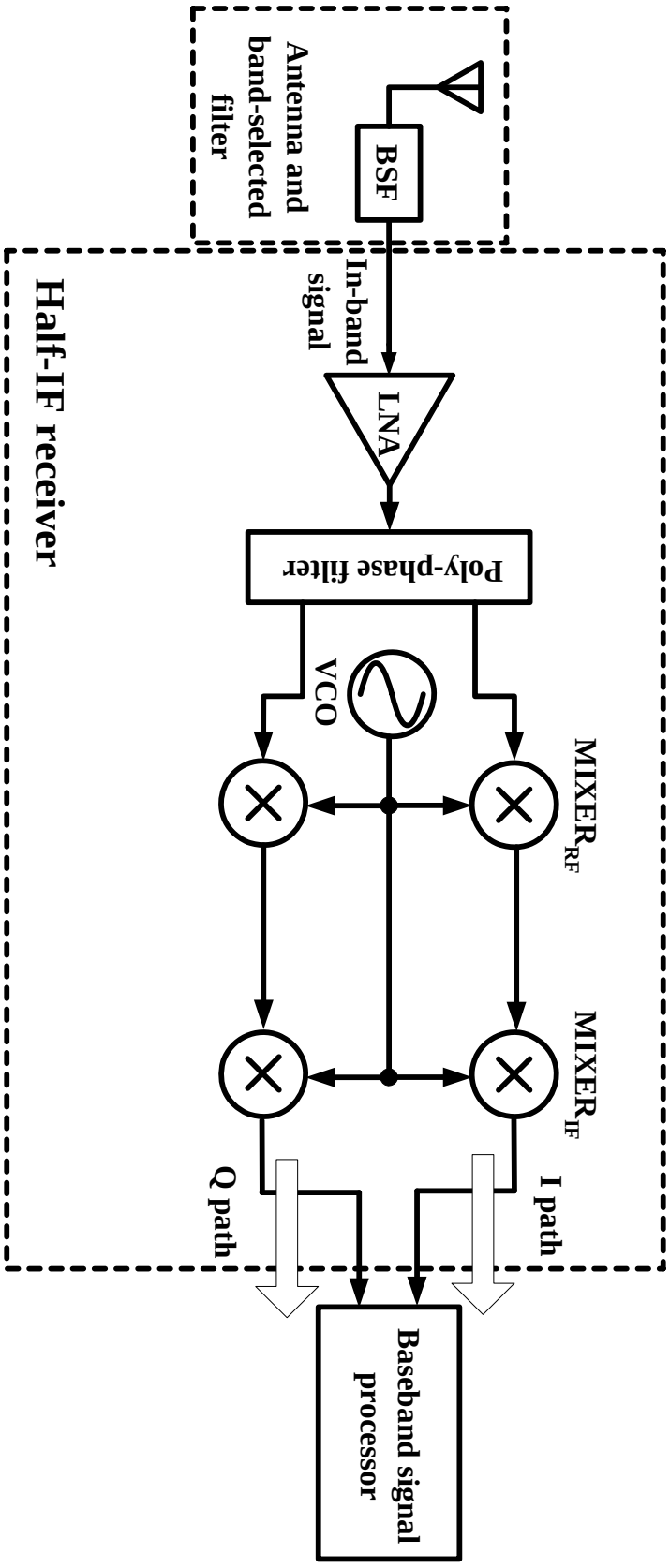


Fig 1.5 Block diagram of the half-IF receiver.

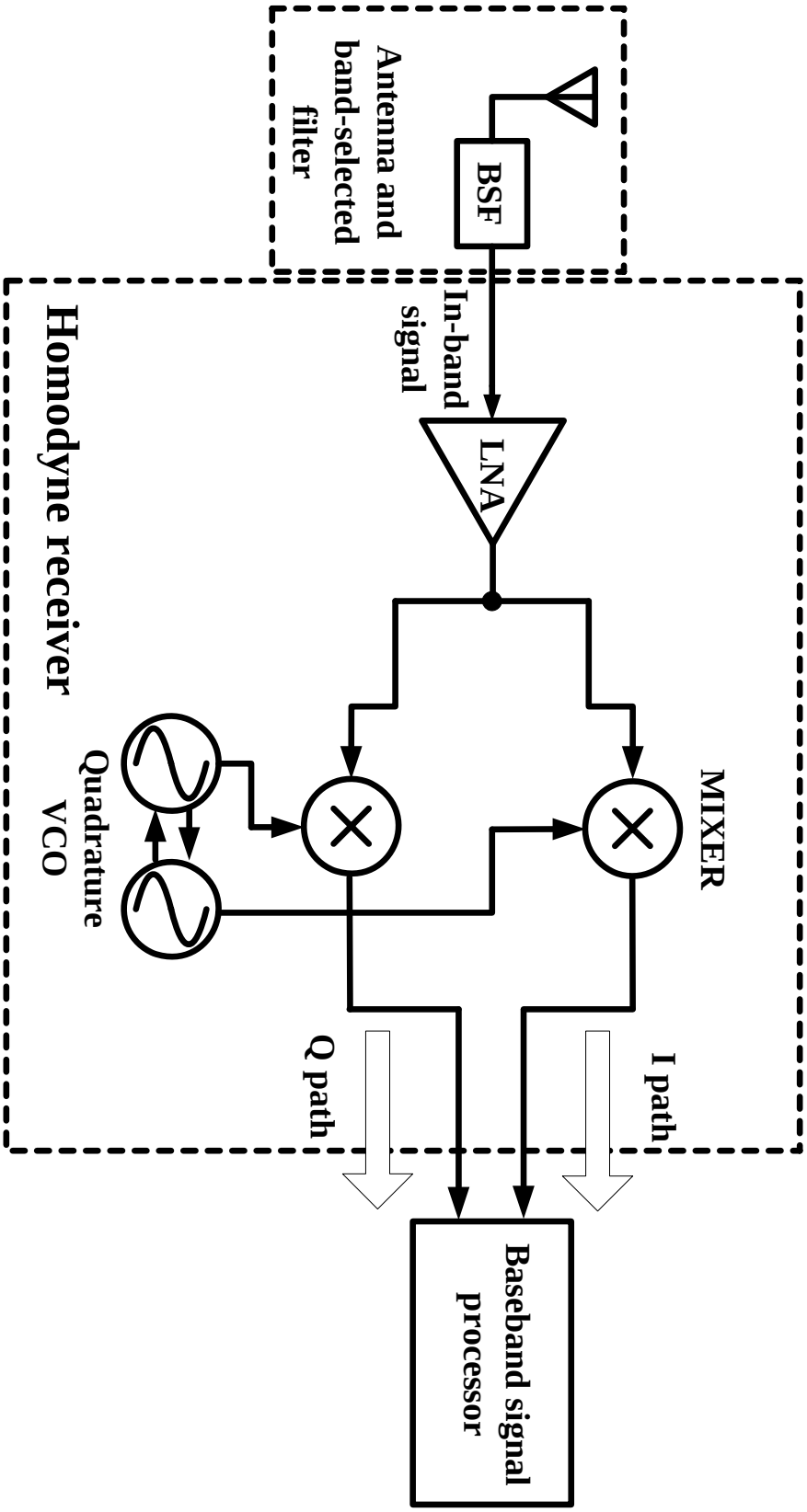


Fig 1.6 Block diagram of the homodyne receiver.

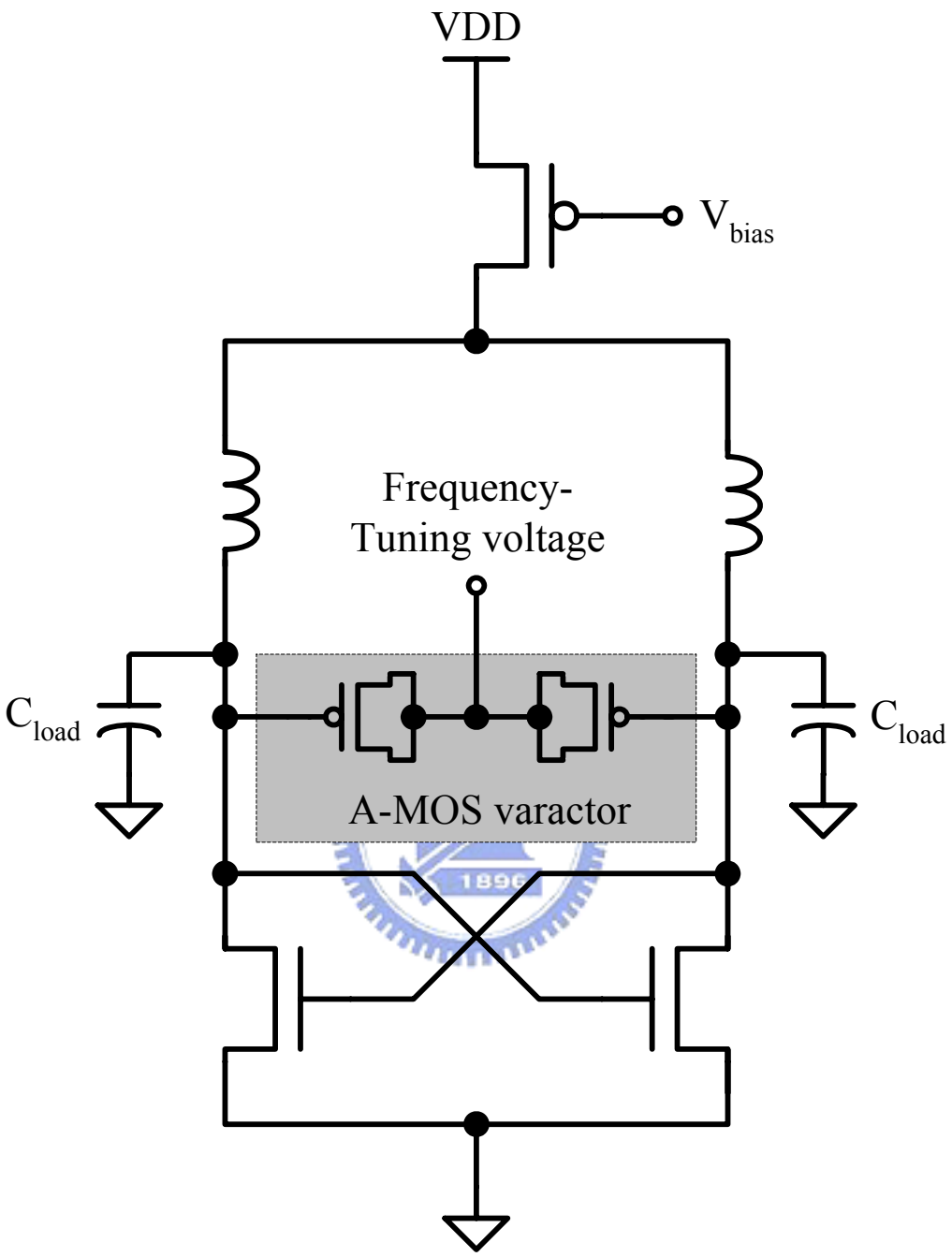


Fig 1.7 Conventional LC-tank MMW VCO structure.

CHAPTER 2

DIRECT INJECTION-LOCKED FREQUENCY DIVIDER

2.1 ANALYTICAL MODEL

The general block diagram of a differential direct ILFD is shown in Fig. 2.1. The active G_m cell with positive feedback is designed to provide a negative resistance to compensate for the power loss from the resistive load per oscillating cycle for the stable output oscillating signals. L, C and R represent the equivalent passive loads of the active G_m cell. To reduce the input capacitance for high-frequency operation, the input stage is implemented by using an NMOS M_{in} only. The input voltage $V_{in} = v_{in}\cos(2\omega t+\varphi_{in})$ is applied to the gate node of M_{in}, where φ_{in} is the input phase. For the sake of convenience it is assumed that $\varphi_{in} = 0$, as shown in Fig. 2.1. If the input frequency 2ω falls into the divided-by-2 locking range, then the differential output voltages, $V_{out\pm}$, at the drain and the source nodes of M_{in} are given by $\pm v_o\cos(\omega t+\varphi_{out})$, where φ_{out} is the output phase. If $\varphi_{in} = 0$, then φ_{out} can be denoted as φ, which represents the phase difference between the input and output signals. In this situation, M_{in} can be regarded as a mixing device and the mixing channel current of M_{in} is denoted by I_{in}.

In most cases, the input voltage is a large signal so M_{in} is operated in the on-off mode. Figs. 2.2(a) and 2.2(b) show the two sample waveforms of V_{in}, $V_{out\pm}$ and I_{in} as φ is equal to $\pi/2$ and $\pi/4$ respectively. As shown in Fig. 2.2, the time interval between the two neighboring turn-on periods of M_{in} is π/ω. Since the frequency of the

differential output voltages at the drain and source nodes of the M_{in} is exactly half of that of the input voltage, the resulting I_{in} in the two neighboring turn-on periods displays the same shapes but opposite polarities as those shown in Figs. 3(a) and 3(b). Therefore, the fundamental frequency of I_{in} is ω and the fundamental component of I_{in} is denoted by $I_{in,\omega}$.

To develop the desired analytical model, $I_{in,\omega}$ is decomposed into in-phase and quadrature components:

$$I_{in,\omega} = I_i(\varphi)\cos(\omega t + \varphi) + I_q(\varphi)\sin(\omega t + \varphi) \tag{2.1}$$

As shown in Figs. 2.2(a) and 2.2(b), the shape of I_{in} strongly depends on φ. Therefore, the amplitudes of both components in (2.1) should also be the functions of φ.

In fact, φ is determined by the input frequency 2ω. Figs. 2.3(a) to 2.3(c) plot the HSPICE simulated waveforms of V_{in}, $V_{out\pm}$ and I_{in} when 2ω is equal to, larger than, or smaller than $2\omega_o$ where ω_o is the resonant frequency of the equivalent passive load in Fig. 2.1. The waveforms of $I_i\cos(\omega t+\varphi)$ and $I_q\cos(\omega t+\varphi)$ calculated from I_{in} are also shown in each figure. Fig. 2.3(a) plots the waveforms in the case of $2\omega = 2\omega_o$. In this case, φ equals $\pi/2$ and $I_q(\pi/2) = 0$, so the phase of $I_{in,\omega}$ is the same as the output voltage signal. Therefore, the M_{in} can be modeled as a single resistor R_{in} with the value of $I_i(\pi/2)/2v_o$. The equivalent model in this case is also shown in Fig. 2.3(a).

When the input frequency 2ω exceeds $2\omega_o$, as the waveforms plotted in Fig. 2.3(b), φ becomes slightly smaller than $\pi/2$ so $I_{in,\omega}$ lags behind the output voltage signal. Therefore, $I_q(\varphi)$ is larger than 0 and M_{in} can be modeled as R_{in} in parallel with an inductor L_{in}. R_{in} and L_{in} are calculated as

$$R_{in} = I_i(\varphi)/2v_o \tag{2.2}$$

and

$$L_{in} = 2v_o/\omega I_q(\varphi) \approx 2v_o/\omega_o I_q(\varphi). \tag{2.3}$$

The equivalent model in this case is also presented in Fig. 2.3(b). The output frequency ω can be easily calculated as

$$\begin{aligned} \omega &= 1/\sqrt{C(L \parallel L_{in})} \\ &\approx \sqrt{\left(1 + 2\omega_o L v_o / I_q(\varphi)\right)/LC} \approx \omega_o + I_q(\varphi)/4Cv_o \,. \end{aligned} \tag{2.4}$$

Therefore, the maximum available value of ω, ω_{max}, is determined by the maximum available value of $I_q(\varphi)/2v_o$ which is denoted by $g_{q,max}$. ω_{max} is given by

$$\omega_{\max} \approx \omega_o + \frac{1}{2C}\left(\frac{I_q(\varphi)}{2v_o}\right)_{\max} \equiv \omega_o + \frac{g_{q,\max}}{2C}. \tag{2.5}$$

The waveforms and the equivalent model of the final case in which the input frequency 2ω is less than $2\omega_o$ are shown in Fig. 2.3(c). In this case, φ becomes slightly larger than $\pi/2$ such that $I_{in,\omega}$ leads to the output voltage signal. Therefore, $I_q(\varphi)$ is smaller than 0 and M_{in} can be modeled as R_{in} in parallel with a capacitor C_{in}, whose capacitance is given by

$$C_{in} = I_q(\varphi)/2v_o\omega \approx I_q(\varphi)/2v_o\omega_o \,. \tag{2.6}$$

The output frequency ω can be easily calculated as

$$\omega = 1/\sqrt{L(C+C_{in})} \approx \sqrt{1/LC\left(1-I_q(\varphi)/2\omega_o C v_o\right)} \approx \omega_o - |\, I_q(\varphi)/4Cv_o \,|. \tag{2.7}$$

Therefore, the minimum available value of ω, ω_{min}, is determined by the minimum available $I_q(\varphi)/2v_o$ which is denoted by $g_{q,min}$. ω_{min} can be expressed as

$$\omega_{\min} \approx \omega_o - \frac{1}{2C}\left|\left(\frac{I_q(\varphi)}{2v_o}\right)_{\min}\right| \equiv \omega_o - \frac{|\, g_{q,\min}\,|}{2C}. \tag{2.8}$$

From (2.5) and (2.8), the input frequency locking range denoted by $\Delta\omega_{in}$ can be calculated as

$$\Delta\omega_{in} = 2(\omega_{\max} - \omega_{\min}) = \left(g_{q,\max} + |\, g_{q,\min}\,|\right)/C. \tag{2.9}$$

Given the symmetric differential structure in Fig. 2.1, for a particular output voltage amplitude v_o, $g_{q,max}$ equals $-g_{q,min}$ and (2.9) can be further simplified as

$$\Delta\omega_{in} = 2\, g_{q,\max}/C = 2\omega_o^2 L g_{q,\max}. \tag{2.10}$$

According to (2.10), $g_{q,max}$ should be designed as large as possible to maximize the locking range $\Delta\omega_{in}$ for fixed values of L and ω_o. However, since all voltage signals that are applied to M_{in} are large signals, no analytical equation exists for $g_{q,max}$. Therefore, HSPICE is adopted to find the values of $g_{q,max}$ in the variously biased cases. Figs. 2.4(a) to 2.4(d) show contour maps of $g_{q,max}$ for various DC overdrive voltages V_{ov} of M_{in} and output voltage amplitudes v_o with different input voltage amplitudes v_{in}. In all these cases, $g_{q,max}$ increases with V_{ov} for a fixed v_o and decreases as v_o increases in the high-V_{ov} region.

According to the proposed model, shown in Fig. 2.3, and the derived locking range equation, (2.10), for a fixed L, the quality factor $Q = R/\omega L$ of the passive load in Fig. 2.3 does not directly influence the locking range. More accurately, the value of Q only indirectly influences the locking range through a change in V_{ov} or v_o which changes $g_{q,max}$, as shown in Fig. 2.4. For example, for a given G_m cell, a low Q of the passive load results in a smaller v_o and thus a larger $g_{q,max}$ and the locking range that is given by (2.10). However, in low and high Q cases, the locking ranges can more fairly be compared with a fixed v_o and V_{ov}. In this situation, $g_{q,max}$ is fixed as shown in Fig. 2.4, such that the locking ranges in low and high Q cases are the same for a fixed L and ω_o, as determined by (2.10). Since a lower-Q passive load has a lower R, the G_m cell needs to consume more power in order to compensate for R to maintain the same output voltage amplitude v_o at resonance. Therefore, for any required v_o, using a higher-Q passive load can reduce the power requirement without any reduction in the locking range.

From the above analysis, some design guidelines for a direct ILFD can be inferred. Firstly, V_{ov} of the input device should be designed as large as possible to maximize the $g_{q,max}$ and frequency locking range. Secondly, a trade-off exists between the output voltage amplitude v_o and the frequency locking range. Therefore, v_o should be set at its minimum tolerant value to maximize the frequency locking range. Finally, the Q factor of the passive load should be as large as possible, to reduce the required DC power consumption without reducing the frequency locking range.

2.2 CIRCUIT DESIGN

2.2.1 Circuit Structure

Based on the design guidelines in Section 2.1, the proposed ILFD circuit for high-speed operation is shown in Fig. 2.5. The circuit structure is simple in that it has no varactor but it still provides a large frequency locking range.

In order to reduce the input capacitance, NMOS M_{in} is used as the only input stage to generate the injected current I_{in}. Furthermore, instead of a complementary cross-coupled pair [35], an NMOS cross-coupled pair is used to implement the G_m cell in Fig. 2. Since the frequency locking range is inversely proportional to the total capacitance value at the output node as in (2.10), the absence of a PMOS cross-coupled pair can significantly increase the frequency locking range. Adding a PMOS current source M_p as shown in Fig. 2.5 provides two advantages over an ILFD presented in an earlier work [37], increasing the locking range. Firstly, since a trade-off exists between the output voltage amplitude and the frequency locking range, the output voltage amplitude can be set to its minimum value by designing an appropriate DC current of M_p to maximize the locking range. Secondly, the gate voltage of M_{in} is connected to VDD and the DC voltage at the output node can be set much lower than the VDD because the DC current is limited by M_p. Therefore, the M_{in} can be biased in the high overdrive voltage region. Additionally, through the resistor R_x, the at the substrate node of M_{in} is connected to the common-mode node of the spiral inductor. The DC voltage at the substrate node can be equal to those at the drain and source nodes such that the threshold voltage of M_{in} can be kept low to increase overdrive voltage. It should be noted that the threshold voltage of M_{in} is modulated by the output voltages and affects $g_{q,max}$. This effect should be considered in the large signal simulations as the $g_{q,max}$ simulations is the Section 2.1.

2.2.2 Input Stage

Based on the design guidelines proposed in Section 2.1, the locking range of the proposed ILFD can be extended even a small device is used. In this design, the width of the input NMOS M_{in} is designed as 3.6μm, with the minimum length which is smaller than that in [35]. From the simulation, the input capacitance of M_{in} is less than 10fF, which is an acceptable load for an on-chip 70-GHz VCO.

2.2.3 PMOS Current Source

The DC current of the PMOS current source denoted by I_{DC} directly influences the output voltage amplitude v_o. According to the model in Fig. 4, v_o can be estimated as $I_{DC}(R||R_{in})$ [75]. Notably, a trade-off exists between v_o and the frequency locking range. Therefore, I_{DC} should be designed appropriately such that v_o just equals the required value at the edges of the frequency locking range.

2.2.4 Integrated Spiral Inductor and Cross-Coupled Pair

Since the small size of M_{in} constrains the value of $g_{q,max}$, careful design of an integrated spiral inductor and cross-coupled pair to achieve a large frequency locking range is important. It can be seen from (2.10), that the frequency locking range is proportional to the inductor value L. Initially the frequency locking range increases with an increase in inductance. However, as L increases over an optimum value, the locking range begins to drop for the following two reasons. Firstly, the output center frequency ω_o can be expressed as

$$\omega_o \approx \sqrt{1/L\left(2W_{1,2}C_{ov} + C_{ox}W_{1,2}L_{1,2}/3 + C_{next}\right)} \tag{2.11}$$

where $W_{1,2}$ ($L_{1,2}$) is the width (length) of M_1 and M_2 in Fig. 2.5, C_{ov} is the overlap capacitance per unit width, C_{ox} is the gate oxide capacitance per unit area, and C_{next} is

capacitance from the next stage. Thus, as L increases, $W_{1,2}$ must be reduced to maintain the required ω_o. At a fixed DC current, this drop increases the DC gate voltages of M_1 and M_2 and thus reduces the overdrive voltage of M_{in} and $g_{q,max}$ and thus the locking range. Secondly, if $W_{1,2}$ is too small to maintain enough G_m, such that the power loss per oscillating cycle form R and R_{in} in Fig. 4 can not be compensated for when the input frequency falls in the range specified in (2.10), then the frequency locking range declines rapidly. Therefore, in this design, iterative simulations are required to find the optimum inductance of the spiral inductor for the maximum frequency locking range.

As mentioned in the Section 2.1, the Q factor of the passive load should be designed as large as possible to reduce the power consumption or I_{DC}. Accordingly, no extra resistor is connected in parallel to the inductor in the proposed circuit.

The results of Ansoft Nexxim simulation involving the frequency locking ranges with various inductances are shown in Fig. 2.6. In the simulation, the center output frequency is around 70GHz, the input amplitude is 0.6V, the input NMOS size is 3.6μm/0.12μm, and the minimum required output voltage amplitude is 250mV. The $g_{q,max}$ value in each case is obtained from Fig. 5, so the locking range can be given by (2.10). Fig. 2.6 also plots the $g_{q,max}$ value and the locking range given by (2.10), which are consistent with the simulation results.

Because the input device is small (i.e. 3.6μm/0.12μm), the size variation of the input device should be considered in the circuit design. Fig. 2.7(a) shows the simulation results when the length of input device varies from 0.12μm to 0.144μm (i.e. 20% variation). When input power is 5dBm, the locking range deceases from 11.6GHz to 9.6GHz and the corresponding percentage is from 16.3% to 13.5%. It can be observed that because the locking range is significantly extended by the proposed

circuit structure, even 20% variation of the input device is considered, the locking range still can be maintained above 10%.

In order to integrate with other 0.13-μm CMOS circuit, Fig. 2.7(b) shows the simulation results when the supply voltage increases to 1.2V. It should be noted that the direct ILFDs in both cases in Fig. 2.7(b) have the same DC current. The simulation results show that, for any input power, the locking ranges increase when VDD increases to 1.2V because the overdrive voltage of the input device increases. This is consistent with the analysis results. When the input power is 5dBm, the locking range increases from 11.6 to 14.1GHz (i.e. from 16.3% to 20.6%).

2.2.5 To Integrate with a differential VCO

There are 2 general methods to integrate single-ended input ILFD with a differential VCO:

1) If a quadrature output signal is required, two independent ILFDs with single-ended input can be directly integrated with a differential VCO [26]
2) If only a differential output signal is required, a dummy input device can be used to balance the differential VCO to reduce the phase and amplitude error [92].

2.3 PHASE NOISE ANALYSIS

In this section, the noise model in an earlier work [26] is modified and used to analysis the phase noise of a direct ILFD. The block diagram of a direct ILFD is redrawn in Fig. 2.8(a) with the active G_m cell replaced by a negative resistor $-R_{act}$. $I_{in,\omega}$ is now given by a single sinusoidal function:

$$\begin{aligned} I_{in,\omega} &= i_{in,amp}\cos(\omega t + \alpha) \\ &= i_{in,amp}\cos(\omega t + \varphi_{out} + \gamma(\varphi_{in}/2 - \varphi_{out})) \end{aligned} \tag{2.12}$$

where $i_{in,amp}$ is the amplitude of $I_{in,\omega}$ and α is the phase of $I_{in,\omega}$ which can be decomposed to φ_{out} and the extra phase γ. Here γ is related to the phase difference between the input and output voltage signal, and so it can be given as a function of $\varphi_{in}/2$-φ_{out}.

Fig. 2.8(b) presents the linear loop for the phase noise analysis, where φ_{n_in} and φ_{n_out} are the random variables that represent the small phase fluctuations of the input and output voltage signals. Here $Z(\omega_m)$ represents the small phase response of the equivalent load in Fig. 2.8(a) and is given by

$$Z(\omega_m) = \frac{1}{1 + 2jQ_{eq}\omega_m/\omega_o} \tag{2.13}$$

where $Q_{eq} \approx (R_{act}\text{-}R)/\omega_o L$ is the quality factor of the equivalent load and $\omega_m = \omega\text{-}\omega_o$ is the offset frequency. The values of the partial differentiations in Fig. 2.8(b) can be easily calculated using

$$\frac{\partial\alpha}{\partial\varphi_{in}} = \frac{1}{2}\gamma'\left(\frac{1}{2}\varphi_{in} - \varphi_{out}\right) \tag{2.14}$$

and

$$\frac{\partial\alpha}{\partial\varphi_{out}} = 1 - \gamma'\left(\frac{1}{2}\varphi_{in} - \varphi_{out}\right) \tag{2.15}$$

where γ' is the derivative of γ. From (2.13) to (2.15), the transfer function of the input and output phase noise spectral densities, $S_{\varphi n\_in}$ and $S_{\varphi n\_out}$ respectively, is given

by

$$\frac{S_{\varphi n\_out}(\omega_m)}{S_{\varphi n\_in}(\omega_m)} = \frac{1/4}{1+(\omega_m/\omega_P)^2} \tag{2.16}$$

where

$$\omega_P = \omega_o\gamma'\left(\frac{1}{2}\varphi_{in} - \varphi_{out}\right)\Big/2Q_{eq} \approx \omega_o^2\gamma'\left(\frac{1}{2}\varphi_{in} - \varphi_{out}\right)L\Big/2(R_{act} - R). \tag{2.17}$$

For a stable oscillating signal, R_{act} is equal to $R+R_{in}$. Therefore, (2.17) can be rewritten as

$$\omega_P \approx \omega_o^2 v_o\gamma'\left(\frac{1}{2}\varphi_{in} - \varphi_{out}\right)L\Big/I_i\left(\varphi_{out} - \frac{1}{2}\varphi_{in}\right). \tag{2.18}$$

The calculation of the transfer function of the free running and output phase noise spectral densities ($S_{\varphi n\_free\text{-}run}$ and $S_{\varphi n\_out}$) is as in an earlier cited work [26]; only the result is shown here:

$$\frac{S_{\varphi n\_out}(\omega_m)}{S_{\varphi n\_free-run}(\omega_m)} = \frac{(\omega_m/\omega_P)^2}{1+(\omega_m/\omega_P)^2}. \tag{2.19}$$

From (2.16), the input phase noise appears at the output with a 6-dB reduction and low-pass shaping, dominating the output phase noise when the offset frequency is less than ω_P. When the offset frequency exceeds ω_P, then from (2.19), the output phase noise is dominated by the phase noise of the divider in free-run. This result is similar to that of a conventional ILFD. The simulated curves of $S_{\varphi n\_out}/S_{\varphi n\_in}$ with various ω_o, V_{ov} and v_{in} at the central frequency are plotted in Fig. 2.9. From Fig. 2.9, $\omega_P/2\pi$ increases with $\omega_o/2\pi$ and generally exceeds 1GHz when $\omega_o/2\pi$ > 35GHz and V_{ov} > 0V.

Therefore, with respect to noise, this structure is also suitable for MMW operations because as ω_o becomes large, its internal noise can be suppressed even at a large offset frequency.

2.4 EXPERIMENTAL RESULTS

The proposed ILFD shown in Fig. 2.5 is designed and fabricated using 0.13μm bulk CMOS technology with a supply voltage of 1V. The size of the M_{in} is only 3.6μm/0.12μm. Based on the proposed design guidelines, Q factor of the passive load should be designed as large as possible. Therefore, any finite resistor in parallel with L degrades the locking range and power consumption. Here, a low-Q ILFD with a resistor around 1kΩ connected in parallel with L to reduce the Q factor is also fabricated on the same chip to observe the relationship between the locking range and the Q factor. The low-Q ILFD circuit schematic is shown in Fig. 2.10 where R_p = 1kΩ. The chip micrographs of both fabricated ILFDs are shown in Fig. 2.11.

The measurement setups for input power and ILFD measurement are shown in Fig. 2.12(a) and (b) respectively. After the losses from the cable and the buffer have been de-embedded, the measured output amplitudes versus the input frequencies for the various values of I_{DC} are presented in Fig. 2.13(a). The locking range can be determined by the difference between the frequencies at the two ends of each curve in Fig. 2.13(a). Fig. 2.13(b) plots the curves of the locking range and the minimum output amplitude in throughout the locking range, versus I_{DC}. The simulated and calculated curves are also shown for comparison. Possible sources of the error between the calculation and simulation are: 1) distributed effect of the passive load is not considered; 2) the output voltage amplitudes are different at lower and higher locking range due to the distributed effect; and 3) harmonic output components are

neglected. Moreover, the difference between the simulated and measured curves mainly results from the inaccurate RF model card provided by the foundry which is only valid up to 18GHz and for small signal simulation and is not accurate at 70GHz and for large signal simulation.

From the measured curve in Fig. 2.13(b), the locking range can be increased significantly by choosing a suitable value for I_{DC} at the cost of a reduced output voltage amplitude. This result is consistent with those of the analysis. Notably, I_{DC} should be kept larger than the specific current to maintain a sufficient G_m to compensate for the power loss form the equivalent resistive load per oscillating cycle. Otherwise, the stable output oscillating signals cannot be maintained. Thus, the locking range declines rapidly as shown in the long-broken-line regions of the measured curves in Fig. 2.13(b). The maximum measured locking range is 13.6% (66.4-76 GHz) with an I_{DC} of 4.4mA from a 1-V supply. Except at the low I_{DC}, the calculated locking ranges from (10) are consistent with the measurement results.

The measured frequency locking ranges as the supply voltage decreases to 0.8V are plotted in Fig. 2.14. The locking ranges are considerably smaller than those in the 1-V case, because the drop in the supply voltage reduces the overdrive voltage of M_{in} and also the $g_{q,max}$. Therefore, the gate voltage of M_{in} should be connected to the maximum available voltage, i.e. usually is VDD, to maximize V_{ov} and the locking range. This result is also consistent with analytic results.

The measured locking ranges versus the output voltage amplitudes of the proposed and low-Q ILFDs are plotted in Fig. 2.15. The value of I_{DC} in each case is marked on the measured curves. For any required output voltage amplitude, reducing the Q factor not only increases the required I_{DC} but also reduces the frequency locking range. The locking range declines because an increase in I_{DC} reduces the overdrive

voltage and thereby $g_{q,max}$ also. The measured input sensitivities of both dividers are plotted in Fig. 2.16. The proposed ILFD also has a greater input sensitivity than the low-Q ILFD.

The measured output phase noise and the phase noise of the input signal from the Agilent mm-wave Source Module E8257DS15 [77] are both plotted in Fig. 2.17(a). The measured curve is not sensitive to the bias condition. Fig. 2.17(a) reveals that the output phase noise is determined by the input phase noise below the 300-kHz offset frequency. Beyond the 300-kHz offset, the output phase noise is corrupted by a flat noise floor of about -120dBc/Hz. The waveform of this extra noise is flat and shapeless, so its source is not within the closed loop that is shown in Fig. 2.8(b). Since only the single-ended output signal is measured, this noise floor may be from the common-mode noise from the PMOS current source, supply voltage and ground, or the instrument itself. The output phase noise and the phase noise in free-run are both plotted in Fig. 2.17(b). Although the output signal in free-run is noisy, the output phase noise after locking is almost independent of the phase noise in free-run below the 10-MHz offset frequency. Beyond the 10-MHz offset frequency, the phase noise in free-run is also corrupted by a flat noise floor at around -120dBc/Hz. Therefore, the internal noise in the loop in Fig. 2.8(b) form the ILFD is observably suppressed before the 10-MHz offset frequency at the very least.

The performances of the proposed divider and other CMOS frequency dividers at above 40GHz are compared in TABLE I. With a smaller input device and without a varactor, the locking range of the proposed divider can be extended to 13.6% at 70GHz. Moreover, it consumes lower power and has higher frequency capability in comparison with Miller divider [38].

2.5 SUMMARY

In this chapter, an analytical model for a direct ILFD is presented. From the proposed model, important design guidelines have been developed. Based on the design guidelines, a 70-GHz direct ILFD has been designed and fabricated using 0.13μm bulk CMOS technology, where a PMOS current source was used to restrict the output voltage amplitude and to increase the overdrive voltage of the input device to improve the frequency locking range. For a direct ILFD, a higher-Q passive load can release the power required without decreasing the frequency locking range. Even if the input device size is small and the varactor is not used, the frequency locking range is large. Simulation results show that the proposed direct ILFD also can be operated in the case of using 1.2-V supply voltage. Therefore, it can be integrated with other circuit using 1.2-V supply voltage. Moreover, if 90-nm CMOS technology is used in the future, 1V can be chosen as the supply voltage of the proposed circuit structure as in this design. Therefore, the proposed direct ILFD can be integrated with an MMW VCO easily and is a favorable choice for use in a CMOS MMW PLL system.

Table 2.1

Performance Comparison between the Proposed CMOS ILFD and Other CMOS Frequency Dividers

	This work		[35]	[36]	[37]	[38]
Technology	0.13μm		0.13μm	90nm	0.2μm	0.18μm
Divided number	2		2	4	2	2
Input frequency	70GHz		50GHz	70GHz	55GHz	40GHz
VDD (V)	1	*1.2	1.5	0.5	1	2.5
Locking Range (%)	13.57	*20.6	0.16	12.4	5.89	5.8
With/without varactors	Without		Without	With	Without	Without
Power consumption (mW)	4.4	*5.3	3	2.75	10.1	16.8
Size of the input device	3.6μm/ 0.12μm		6μm/ 0.12μm	N.A.	N.A.	N.A.

*Simulation data

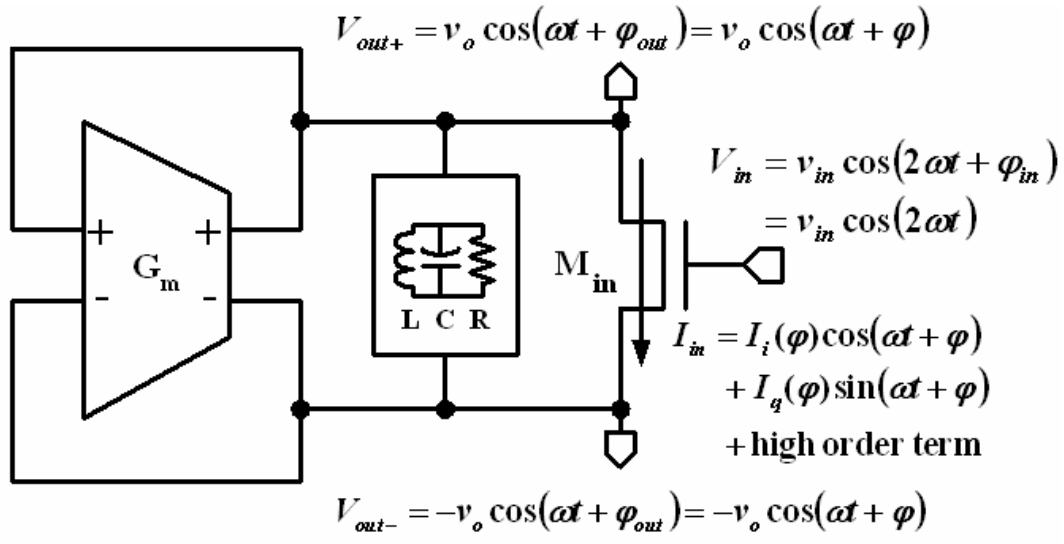
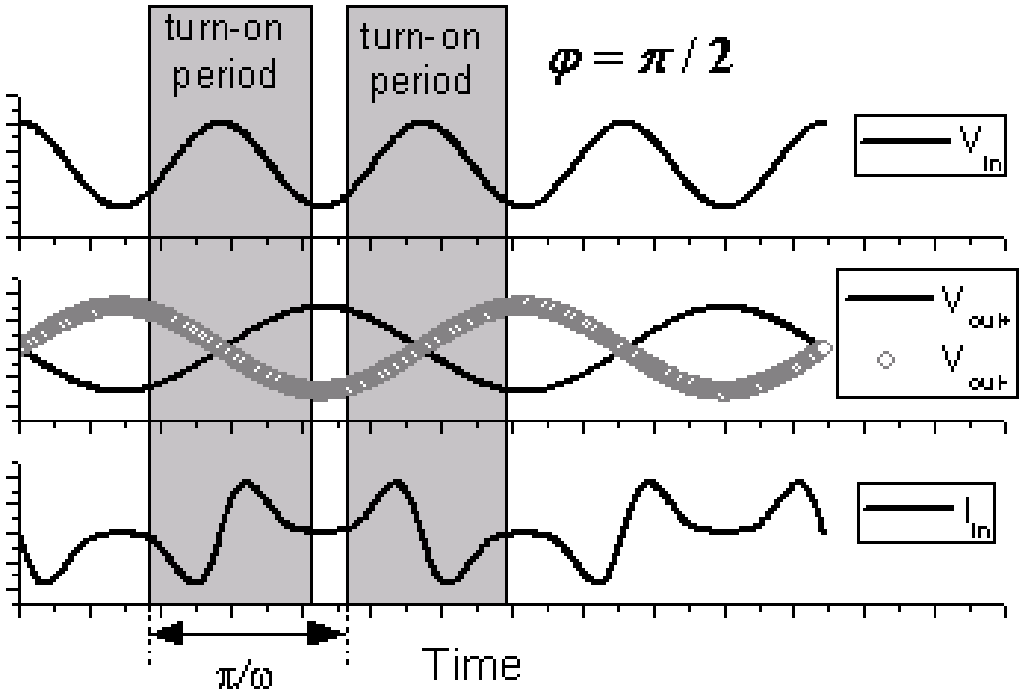
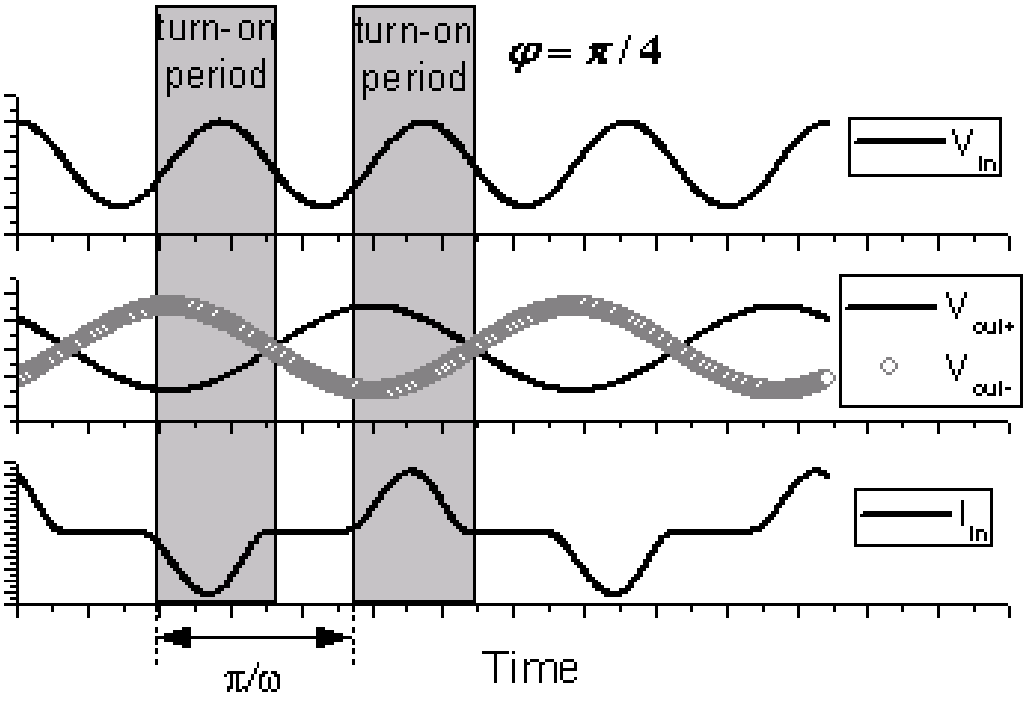


Fig. 2.1 A general block diagram of a differential direct ILFD.

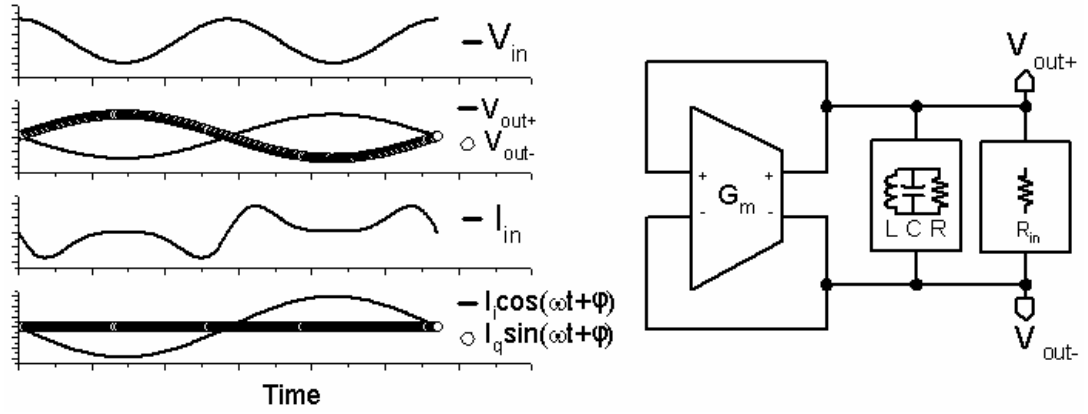


(a)

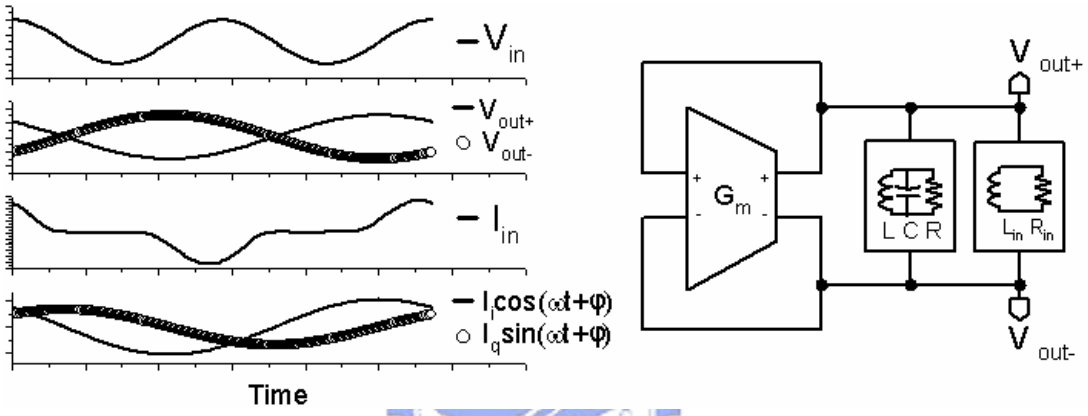


(b)

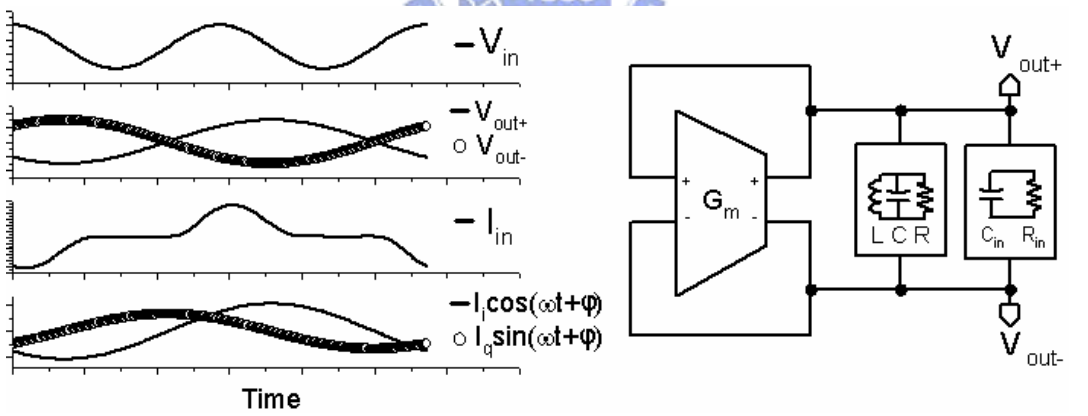
Fig. 2.2 Two waveforms of V_{in}, $V_{out\pm}$, and I_{in} as φ is equal to (a) π/2. (b) π/4.



(a)

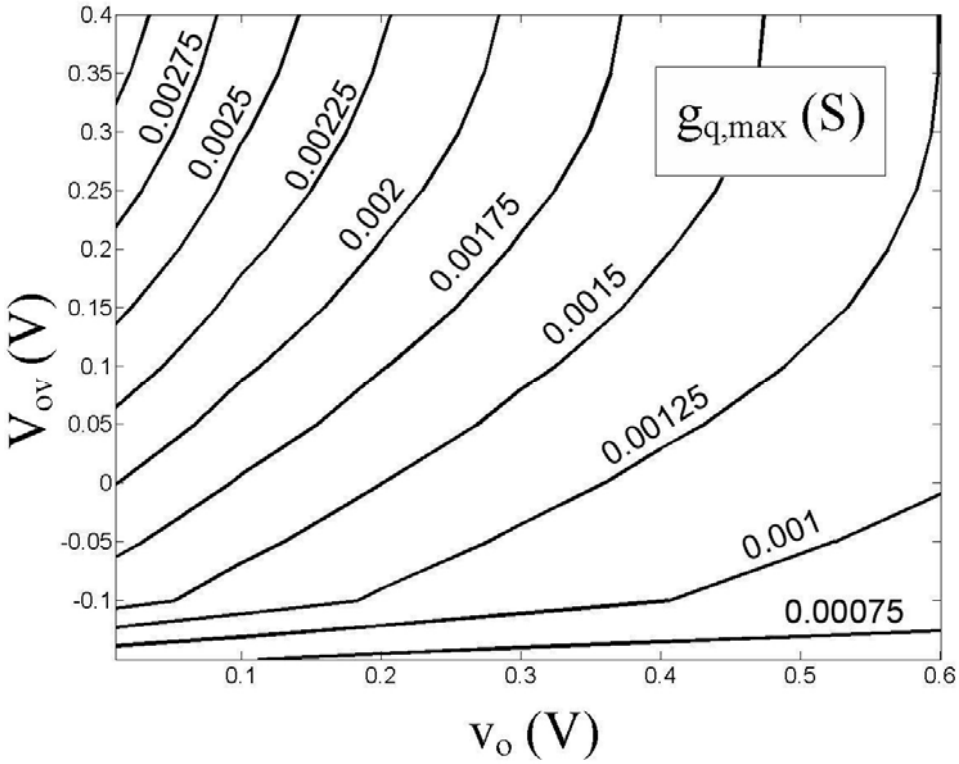


(b)

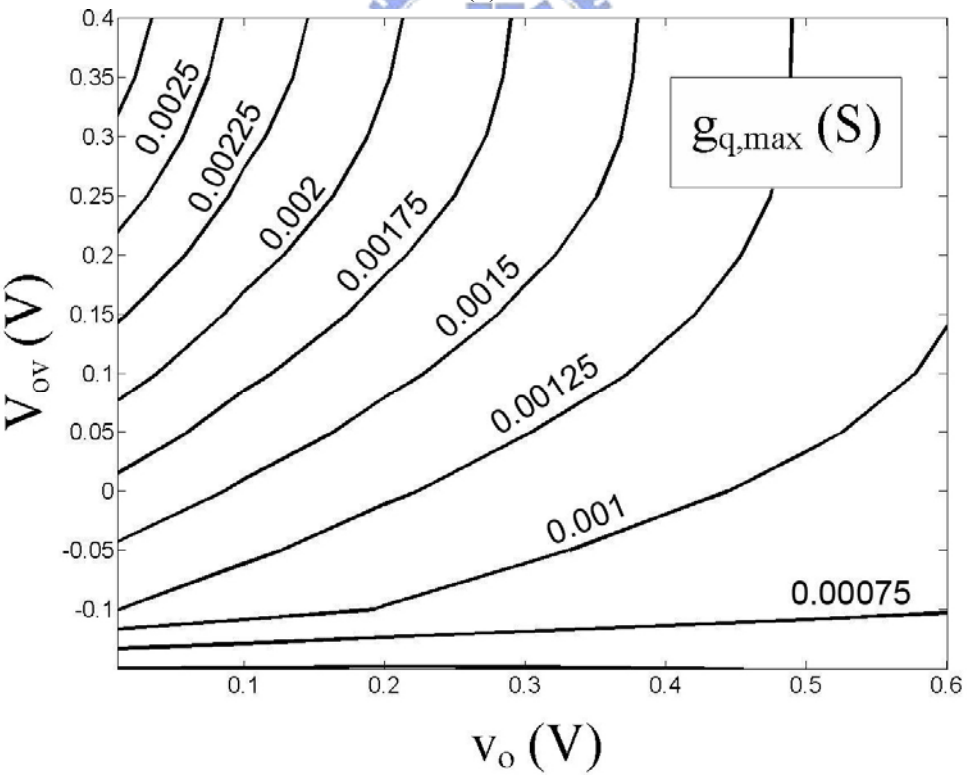


(c)

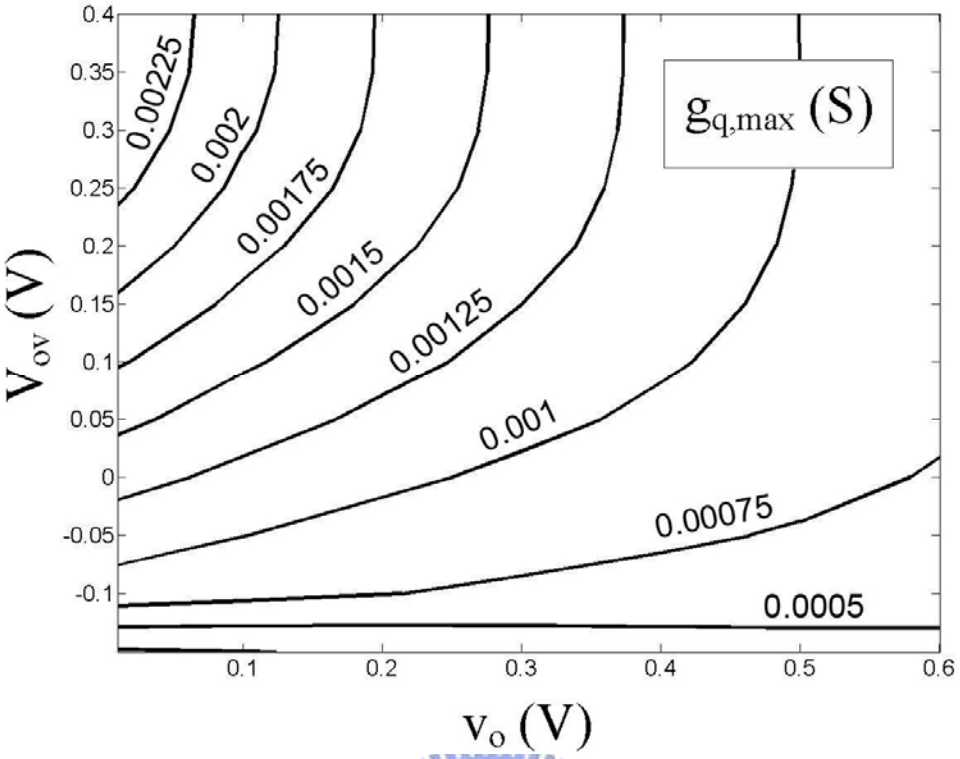
Fig. 2.3 The simulated waveforms of V_{in}, $V_{out\pm}$, I_{in}, $I_i\cos(\omega t+\varphi)$, $I_q\sin(\omega t+\varphi)$ and the equivalent model as (a) $2\omega=2\omega_o$. (b) $2\omega>2\omega_o$. (c) $2\omega<2\omega_o$.


$g_{q,max}$ (S)
0.00275
0.0025
0.00225
0.002
0.00175
0.0015
0.00125
0.001
0.00075
V_{ov} (V)
v_o (V)

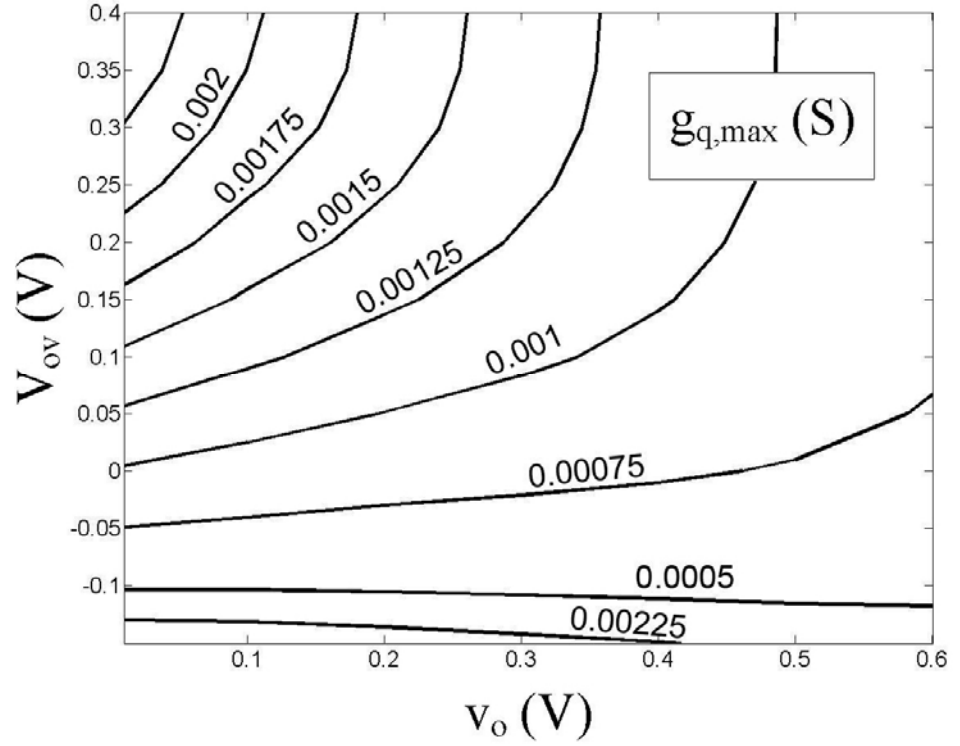
(a)


$g_{q,max}$ (S)
0.0025
0.00225
0.002
0.00175
0.0015
0.00125
0.001
0.00075
V_{ov} (V)
v_o (V)

(b)



(c)



(d)

Fig. 2.4 The contour maps of $g_{q,max}$ as (a) v_{in}=0.6V. (b) v_{in}=0.5V. (c) v_{in}=0.4V. (d) v_{in}=0.3V.

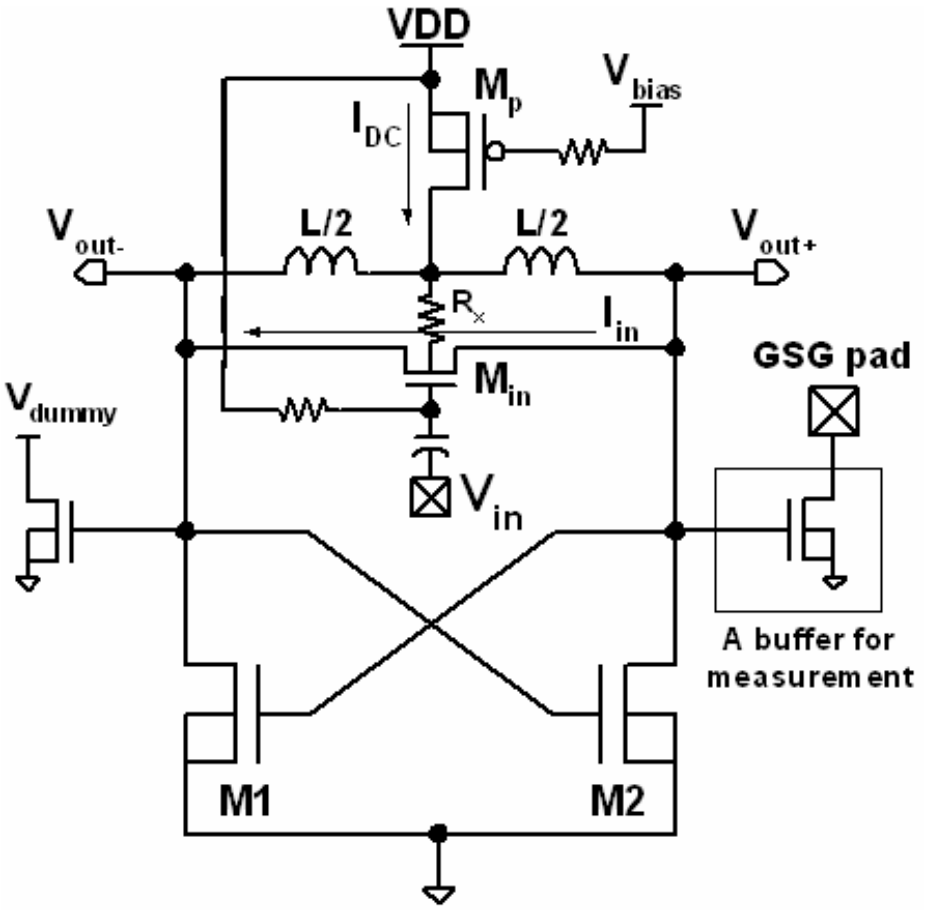


Fig. 2.5 Circuit structure of the proposed direct ILFD.

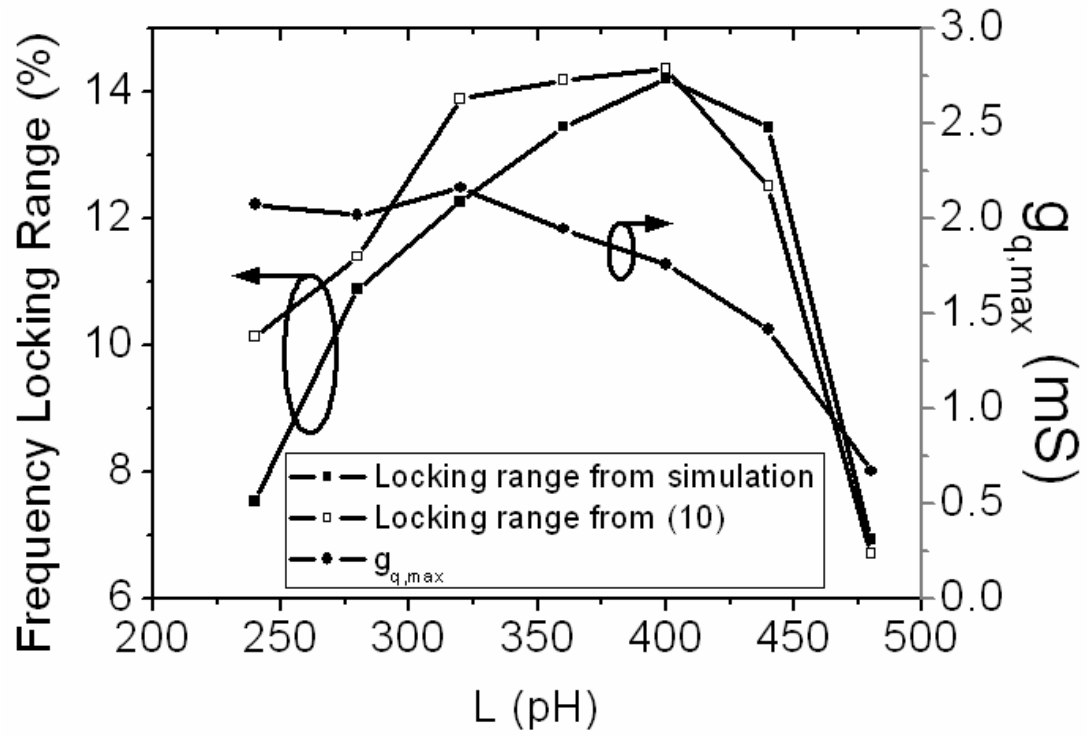
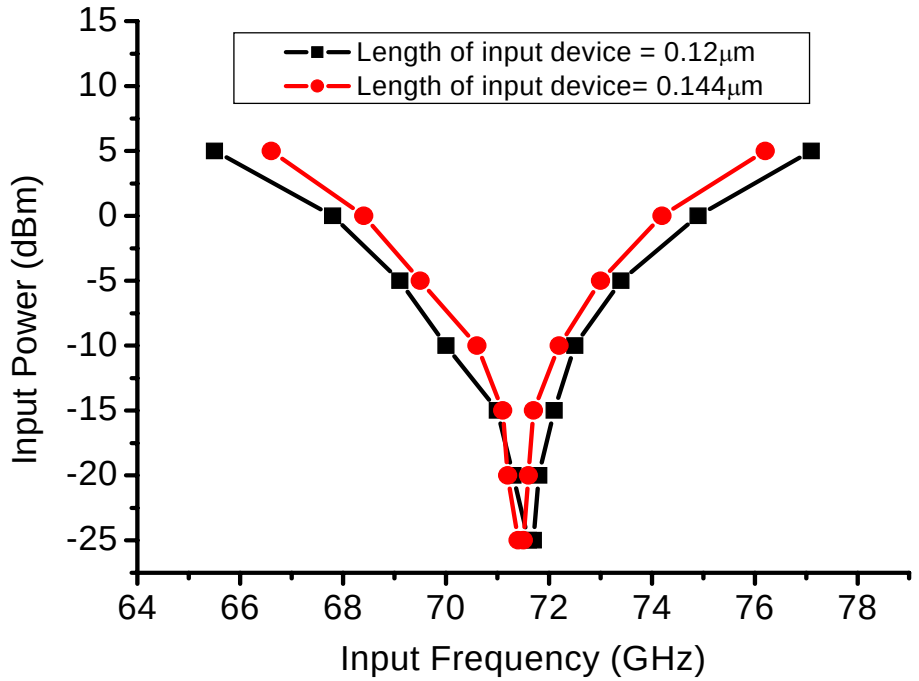
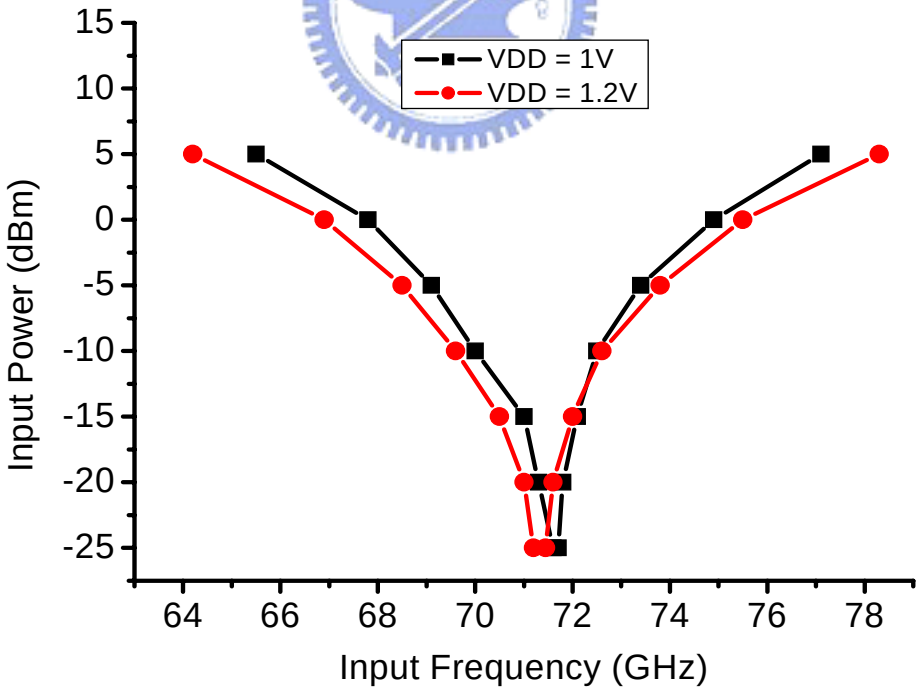


Fig. 2.6 The simulated frequency locking ranges and $g_{q,max}$ with different values of the inductor.

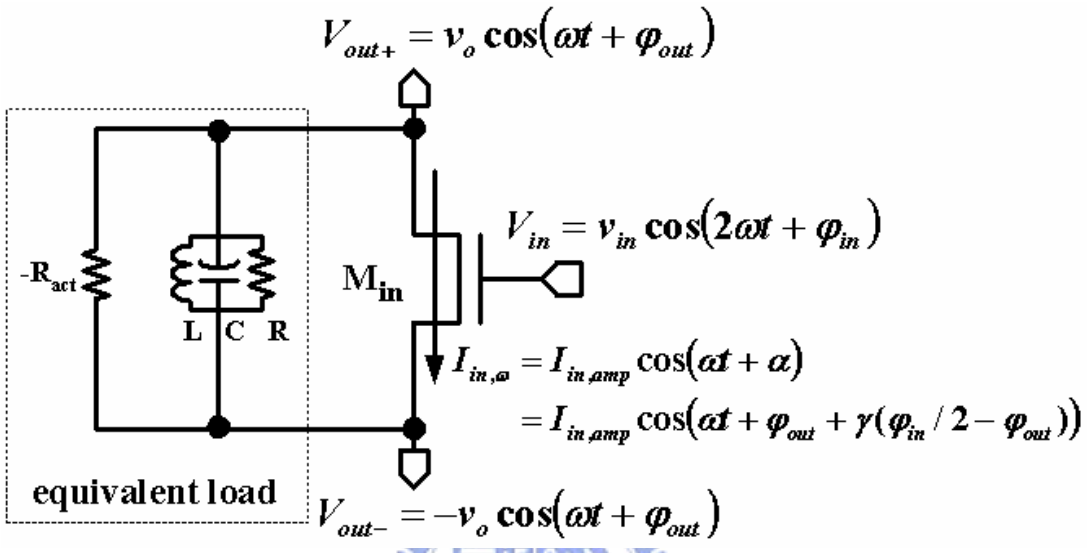


(a)

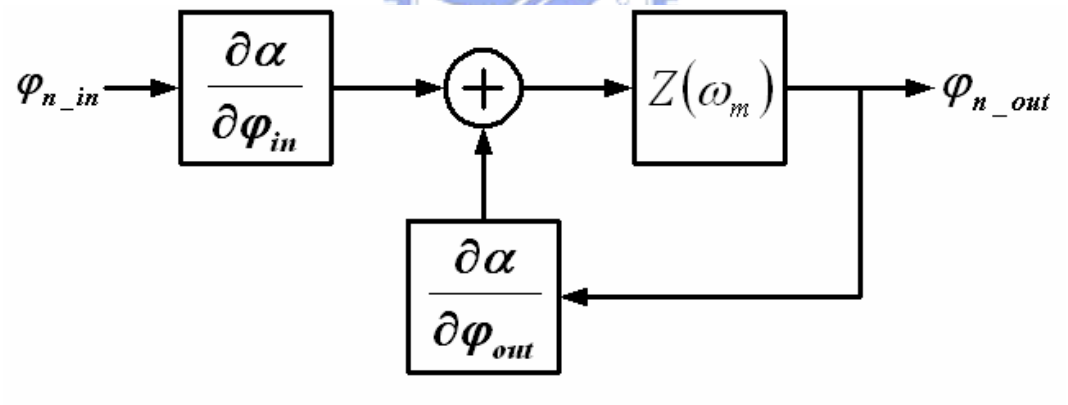


(b)

Fig. 2.7 The simulated input sensitivity curves (a) in cases of different input device length. (b) in the cases of different VDD.

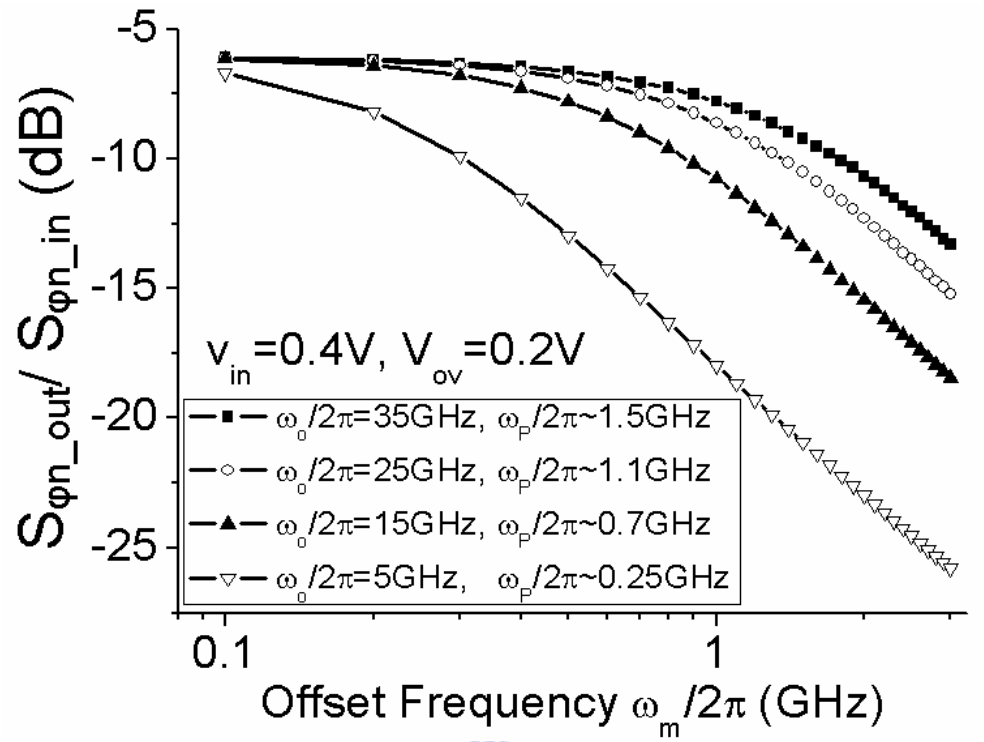


(a)

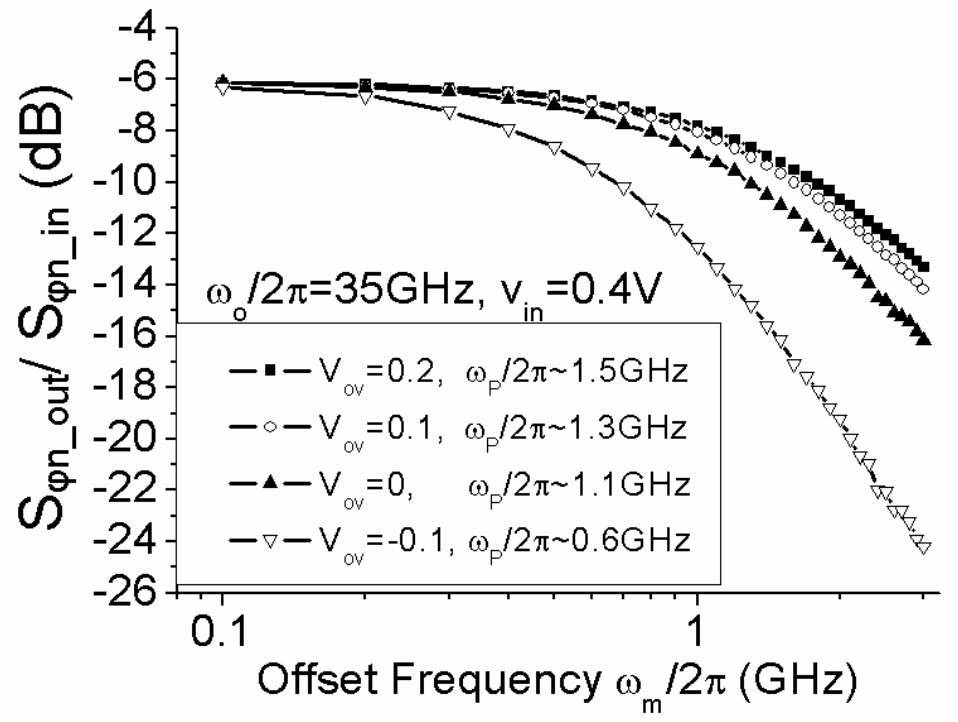


(b)

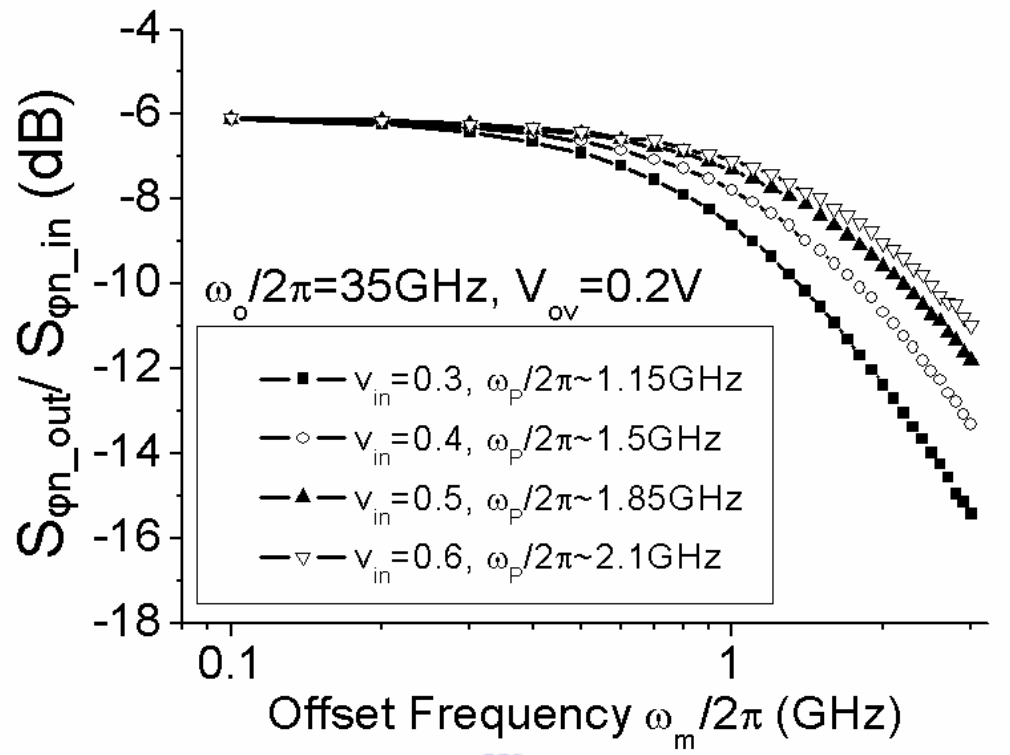
Fig. 2.8 (a) The block diagram of the direct ILFD. (b) the linear loop for the phase noise analysis.


-5
-10
-15
-20
-25
$S_{\varphi n\_out}/S_{\varphi n\_in}$ (dB)
v_{in}=0.4V, V_{ov}=0.2V
$\omega_o/2\pi$=35GHz, $\omega_P/2\pi$~1.5GHz
$\omega_o/2\pi$=25GHz, $\omega_P/2\pi$~1.1GHz
$\omega_o/2\pi$=15GHz, $\omega_P/2\pi$~0.7GHz
$\omega_o/2\pi$=5GHz, $\omega_P/2\pi$~0.25GHz
0.1
1
Offset Frequency $\omega_m/2\pi$ (GHz)

(a)


-4
-6
-8
-10
-12
-14
-16
-18
-20
-22
-24
-26
$S_{\varphi n\_out}/S_{\varphi n\_in}$ (dB)
$\omega_o/2\pi$=35GHz, v_{in}=0.4V
V_{ov}=0.2, $\omega_P/2\pi$~1.5GHz
V_{ov}=0.1, $\omega_P/2\pi$~1.3GHz
V_{ov}=0, $\omega_P/2\pi$~1.1GHz
V_{ov}=-0.1, $\omega_P/2\pi$~0.6GHz
0.1
1
Offset Frequency $\omega_m/2\pi$ (GHz)

(b)



(c)

Fig. 2.9 The simulated curves of $S_{\varphi n\_out}/S_{\varphi n\_in}$ with different (a) ω_o (b) V_{ov} (c) v_{in} at the central frequency

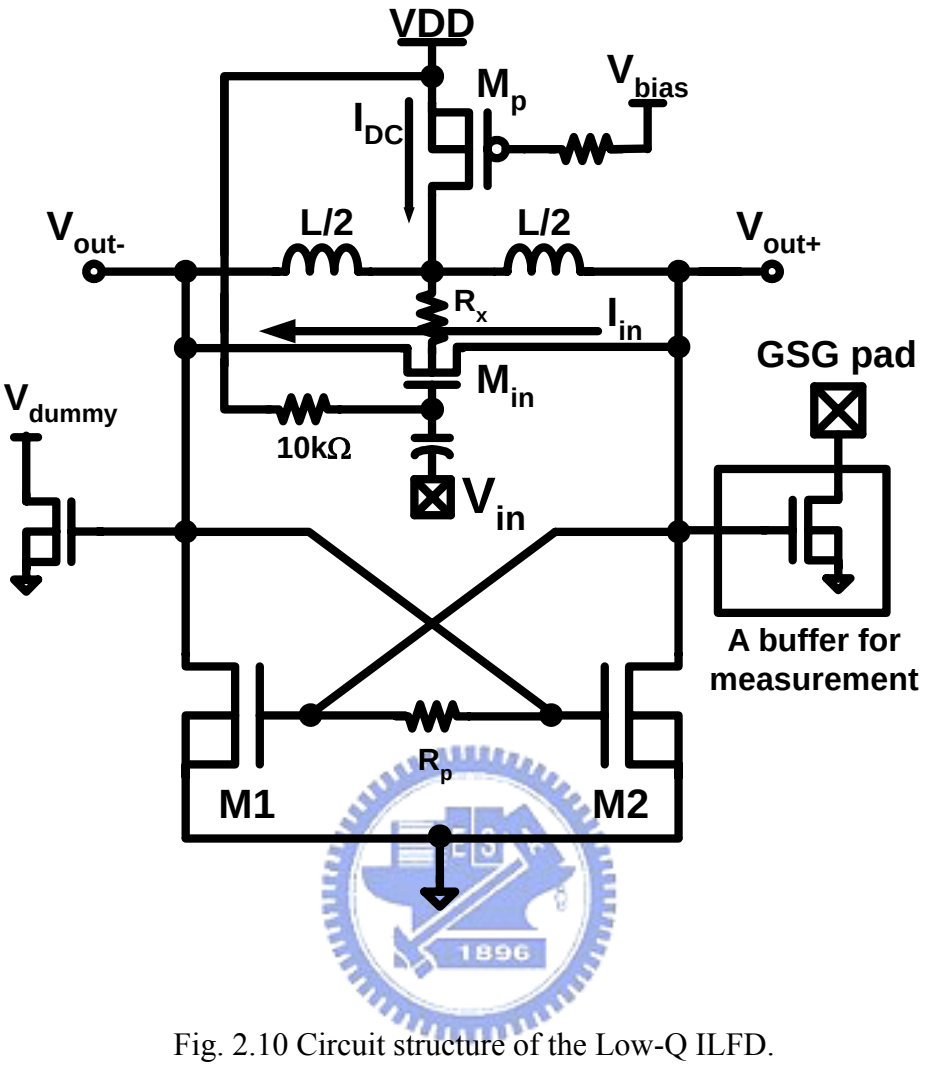


Fig. 2.10 Circuit structure of the Low-Q ILFD.

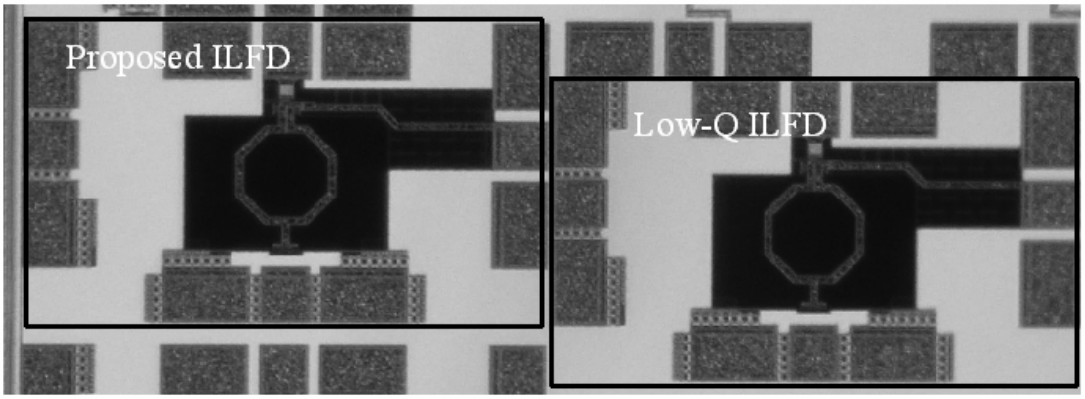
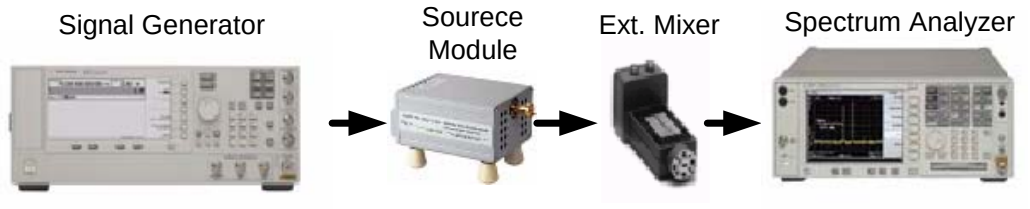
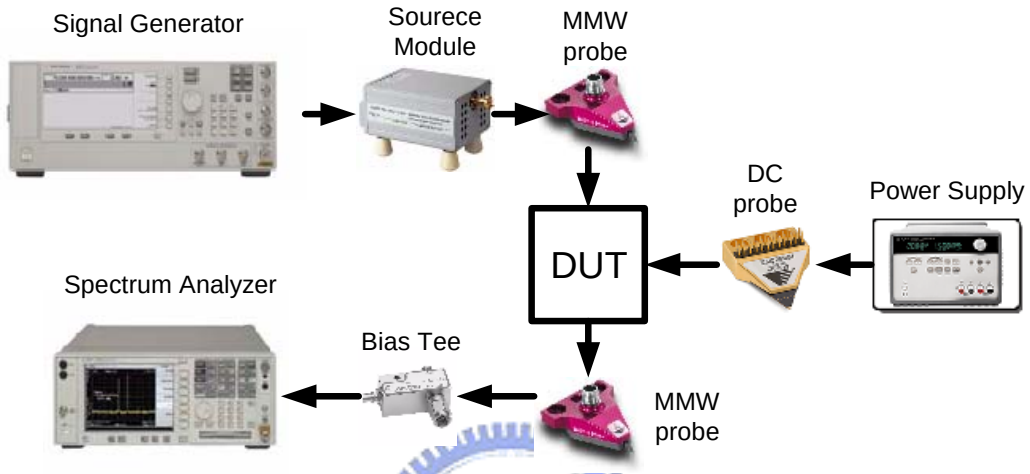


Fig. 2.11 The micrographs of ILFDs.

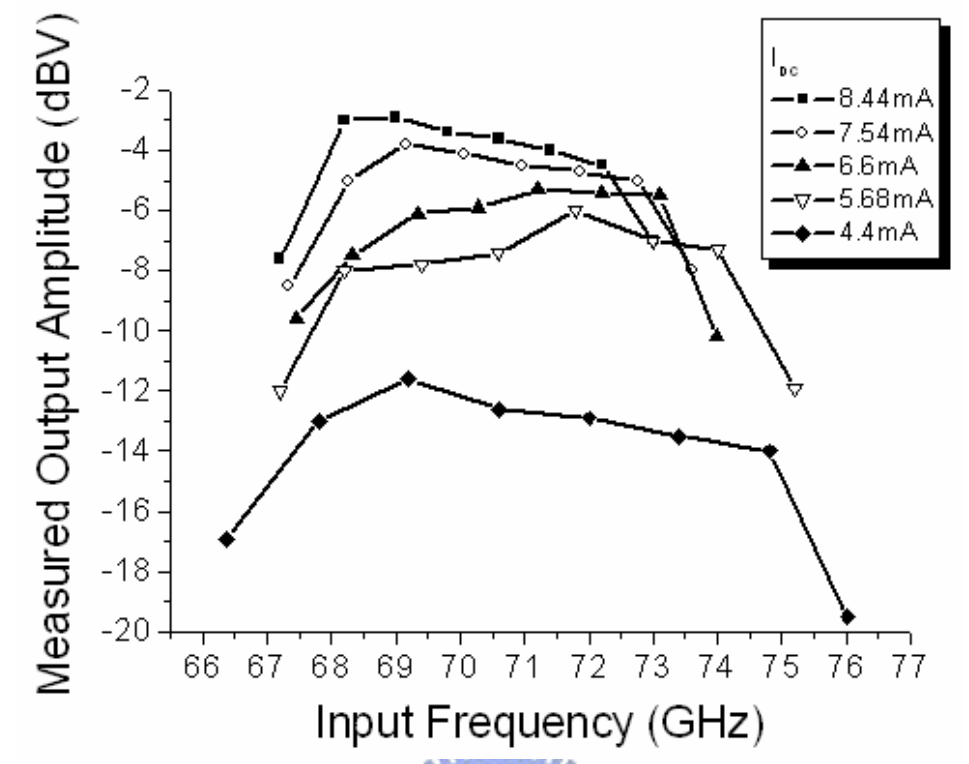


(a)

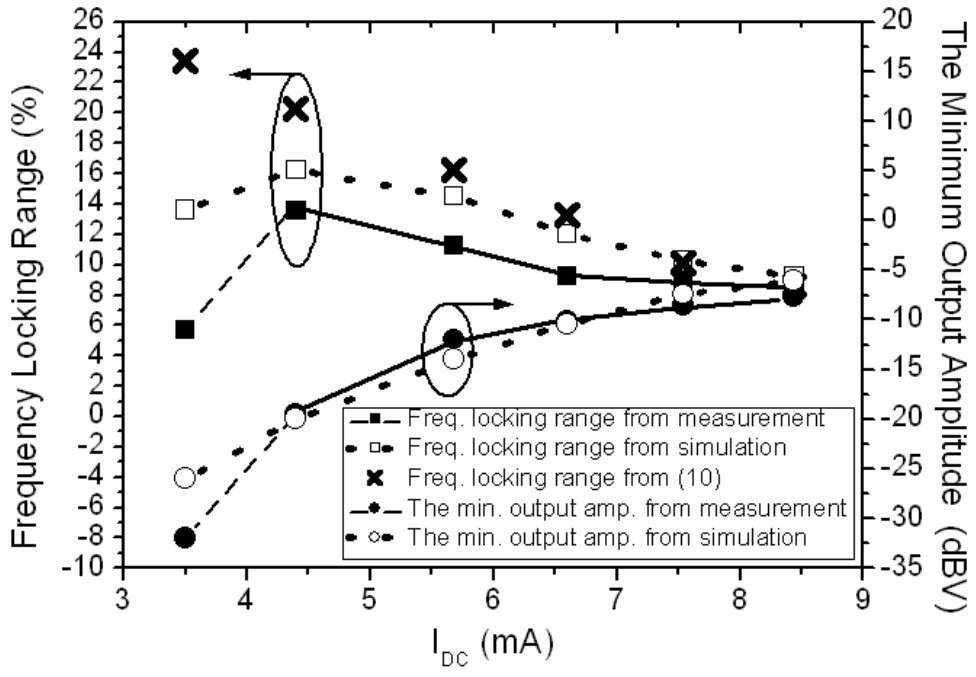


(b)

Fig. 2.12 (a) The measurement setup for input power measurement. (b) the measurement setup for divider measurement.



(a)



(b)

Fig. 2.13 (a) The measured output amplitude versus input frequency. (b) the measured and calculated/simulated locking range and the minimum output amplitude versus I_{DC}.

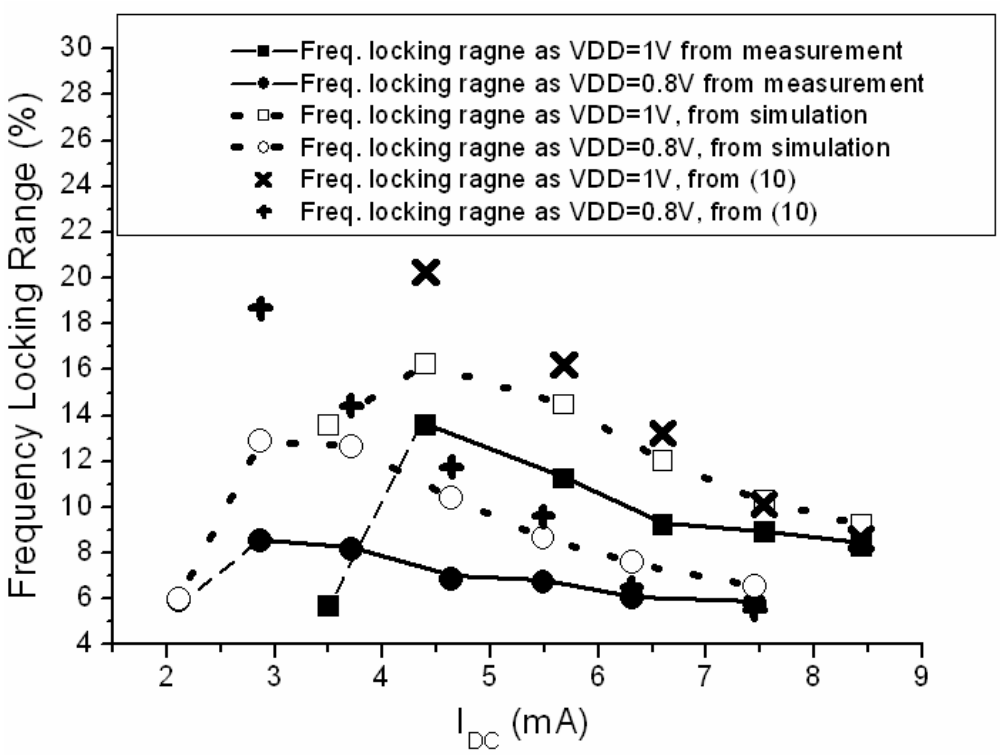


Fig. 2.14 The locking range as the supply voltages are 0.8V and 1V.

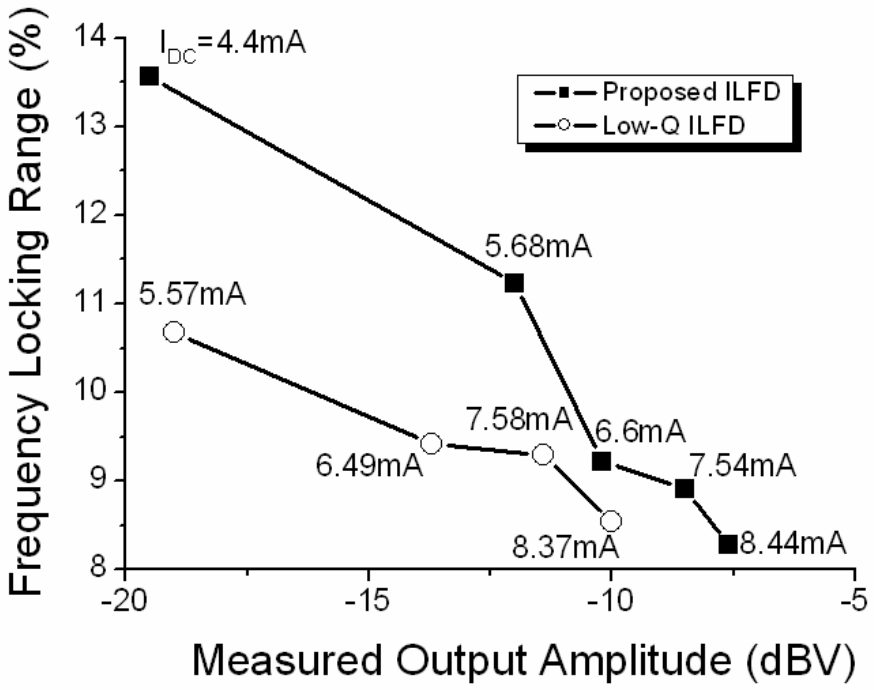


Fig. 2.15 The measured locking ranges versus output voltage amplitudes of both proposed and low-Q ILFDs.

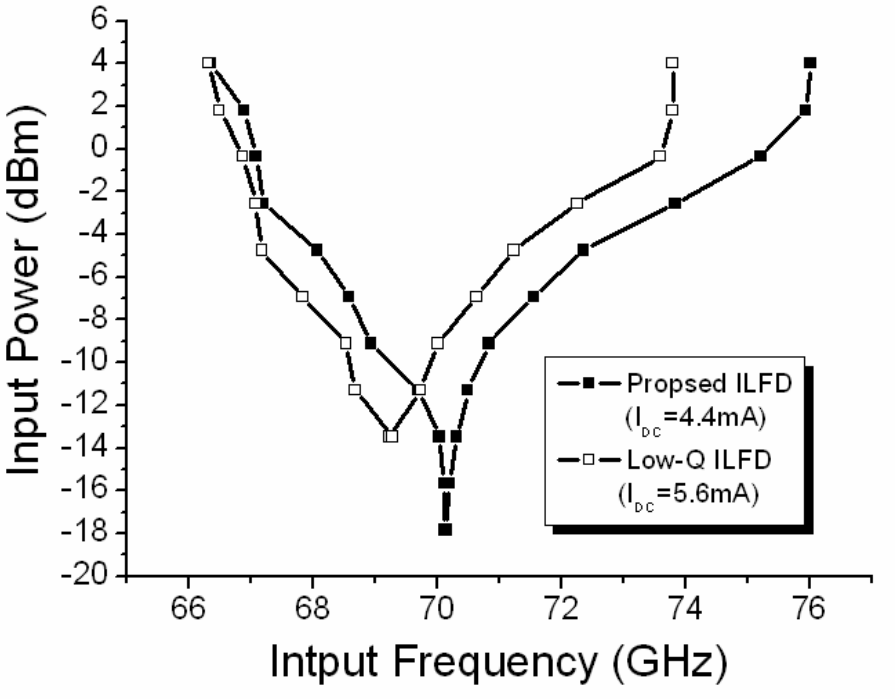
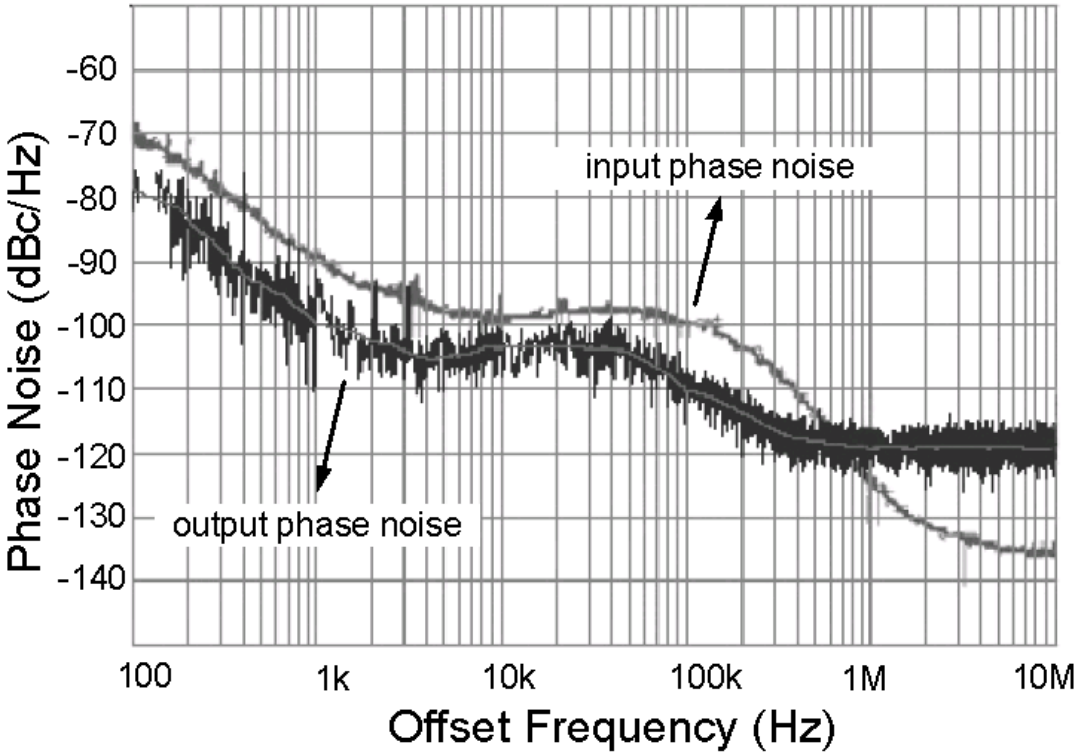
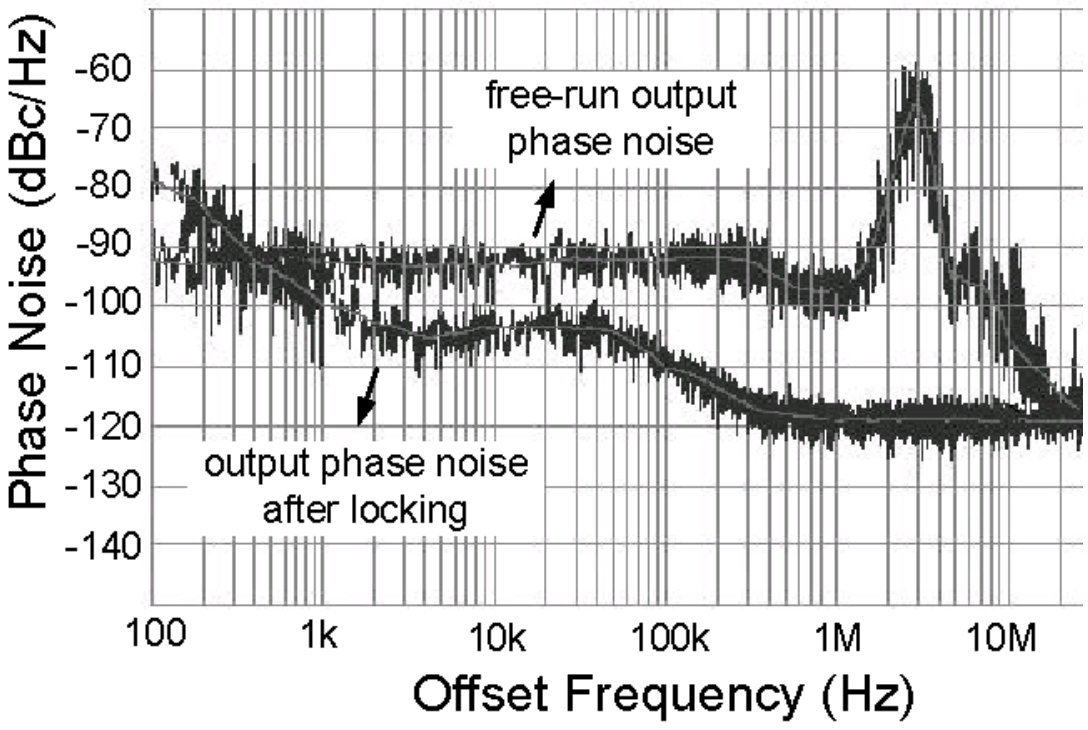


Fig. 2.16 The measured input sensitivities of both ILFDs.



(a)



(b)

Fig. 2.17 (a) The measured output phase noise and the phase noise of input signal from Agilent mm-wave Source Module E8257DS15 [77]. (b) The measured output phase noise and the free-run phase noise.

CHAPTER 3

THIRD-ORDER SUB-HARMONIC MIXER WITH AN ON-CHIP WIDE-TUNING-RANGE VCO

3.1 FREQUENCY TUNING RANGE OF COMVENTIONAL CMOS VCO

In order to analyze the relationship between the frequency tuning range and oscillating frequency, a conventional high-frequency VCO is used, as shown in Fig. 3.1(a), where M_{v1} and M_{v2} are varactors implemented by accumulation-mode MOS's (A-MOS's). The model of the equivalent circuit of the VCO is shown in Fig. 3.1(b), where the broken line in the middle represents either the common mode or ground. The integrated spiral inductor L_{int} is modeled with g_L, L_{ind}, and C_{ind}. Because the impedance of the varactor M_{v1}/M_{v2} is a function of the tuning voltage V_{tune}, it is modeled with a capacitive function $C_{var}(V_{tune})$ and a conductive function $g_{var}(V_{tune})$. The cross-coupled pair formed by M_1 and M_2 is modeled with $-g_{ccp}$ and C_{ccp}. C_{load} represents the load capacitance from the next stage.

From the equivalent model in Fig. 3.1(b), the frequency tuning range α of the VCO can be calculated as

$$\alpha = \frac{2(f_{\max} - f_{\min})}{f_{\max} + f_{\min}} = \frac{2\left(\sqrt{1 + \Delta C / C_{\min}} - 1\right)}{\sqrt{1 + \Delta C / C_{\min}} + 1} \approx \frac{\Delta C}{2C_{\min}}, \tag{3.1}$$

where f_{max} (f_{min}) is the maximum (minimum) oscillating frequency of the VCO, $C_{min} = C_{ind}+C_{var}(VDD)+C_{ccp}+C_{load} \approx C_{var}(VDD)+C_{ccp}+C_{load}$, and $\Delta C = C_{var}(0)-C_{var}(VDD)$.

The startup condition is considered to find the relationship between α and f_{min}. When V_{tune} = 0V, $g_{var}(V_{tune})$ is maximum and the oscillation frequency is minimum (f_{min}). For a large f_{min} (e.g. 60GHz), $g_{var}(0)$ is usually much larger than g_L. Therefore, the startup condition in the worst case (i.e. at f_{min}) with a small-signal loop gain of β can be expressed as

$$g_{ccp} = \beta\left(g_L + g_{\mathrm{var}}(0)\right) \approx \beta g_{\mathrm{var}}(0). \tag{3.2}$$

In order to express g_{ccp} by process parameters, the small-signal model shown in Fig. 3.2 is applied to M_1/M_2 in Fig. 3.1(a), where r_g is the parasitic gate resistor; C_{gs}, the parasitic gate-to-source capacitor; C_{gd}, the parasitic gate-to-drain capacitor; V_{gs}, the voltage on C_{gs}; and g_m the small-signal transconductance. Considering the gate-to-channel and overlap capacitance, C_{gs} and C_{gd} can be written as

$$C_{gs} = \frac{2}{3}C_{ox}WL + C_{ov}W \tag{3.3}$$

and

$$C_{gd} = C_{ov}W = \frac{3C_{ov}}{2C_{ox}L + 3C_{ov}}C_{gs}, \tag{3.4}$$

respectively, where C_{ox} is the gate-oxide capacitance per unit area; $C_{ov,}$ the overlap capacitance per unit width; and W (L), the MOS width (length). If the quality factor $Q_g = (2\pi f r_g C_{gs})^{-1}$ looking into the gate terminal at frequency f is much larger than 1, $g_m r_g << 1$, and the minimum length L_{min} is chosen for M_1/M_2, from (3.3) and (3.4), g_{ccp} can be calculated as

$$g_{ccp} \approx g_m - (2\pi f)^2 \gamma_1, \tag{3.5}$$

where

$$\gamma_1 = \frac{r_g\left(2C_{ox}L_{\min} + 9C_{ov}\right)^2}{\left(2C_{ox}L_{\min} + 15C_{ov}\right)^2} C_{ccp}^2 . \tag{3.6}$$

Moreover, to express $g_{var}(0)$, the equivalent model of a single-finger A-MOS varactor is shown in Fig. 3.3(a), where $C_{var,s}$ is a function of V_{tune} and $R_{s,s}$ represents the parasitic resistors of the poly gate and channel. When $V_{tune} = 0$, for a frequency f, the equivalent parallel model using impedance transformation is as shown in Fig. 3.3(b), where

$$R_{p,s} \approx \frac{1}{2\pi f\left(C_{\mathrm{var},s}(VDD) + \Delta C_s\right)^2 R_{s,s}} \tag{3.7}$$

with the definition that

$$\Delta C_s = C_{\mathrm{var},s}(0) - C_{\mathrm{var},s}(VDD) . \tag{3.8}$$

If M_{v1}/M_{v2} in Fig. 3.1(a) has F_{var} fingers, from (3.7), $g_{var}(0)$ can be calculated as

$$g_{\mathrm{var}}(0) \approx (2\pi f)^2 \left(1 + \frac{C_{\mathrm{var},s}(VDD)}{\Delta C_s}\right)^2 R_{s,s}\Delta C_s^2 F_{\mathrm{var}} = (2\pi f)^2 \gamma_2 \Delta C , \tag{3.9}$$

where

$$\gamma_2 = \left(1 + \frac{C_{\mathrm{var},s}(VDD)}{\Delta C_s}\right)^2 R_{s,s}\Delta C_s . \tag{3.10}$$

.

ΔC in (3.1) can be calculated at f_{min} from (3.2), (3.5), and (3.9). By replacing the result into (3.1), α can be re-expressed as

$$\alpha \approx \frac{\Delta C}{2C_{\min}} \approx \frac{1}{\beta\gamma_2\left(2C_{\text{var}}(VDD)+C_{ccp}+C_{load}\right)}\left[\frac{g_m}{(2\pi f_{\min})^2}-\gamma_1\right], \qquad (3.11)$$

where the parameters γ_1 and γ_2 are independent of frequency. From the above equation, it can be observed that α exhibits a drastic decrease for an increase in the oscillating frequency f_{min}.

In order to observe the relationship between α and f_{min} in (3.11), simulations of the circuit shown in Fig. 3.1(a) are performed using 0.13μm CMOS technology. All simulations are performed by assuming C_{load} = 30fF and the gate voltage of M_1/M_2 is designed as VDD/2 = 0.6V in order to achieve the maximum tuning range as V_{tune} ranges from 0 to VDD = 1.2V. For simplification, the finger sizes of M_1/M_2 and M_{v1}/M_{v2} are fixed, and their sizes are changed by their finger numbers F_M and F_v, respectively. The single-turn spiral inductor shown in Fig. 3.4 is used and all inductor models are obtained by using an EM simulator. For different values of F_M, the corresponding inductor radii R_{ind} and F_v are decided by the required f_{min} and the startup condition in (3.2) with β = 3 [78]. The simulation results of α for different size of M_1/M_2 and f_{min} are shown in Fig. 3.5(a). The corresponding values of R_{ind} for all simulations are shown in Fig. 3.5(b). From Fig. 3.5(a), it can be observed that the maximum frequency tuning ranges are 22.9%, 8.47%, and 2.16% when f_{min} is 20, 40, and 60GHz, respectively. The results agree with (3.11), where a drastic decrease is observed in α for an increase in f_{min}.

From the above results, it can be seen that a 60-GHz conventional VCO is

difficult to cover the entire unlicensed band from 57 to 64GHz (i.e. 11.57% at 60.5 GHz). Therefore, a 60-GHz third-order sub-harmonic mixer with a 20-GHz VCO is proposed in this chapter for wideband applications.

3.2 OPERATIONAL PRINCIPLE

Consider a common-gate amplifier, as shown in Fig. 3.6. The LO signal $V_{LO}(t)$ at the gate terminal results in a time-varying transconductance $G_m(t)$, which is the dominant contributor to frequency conversion. Fig. 3.7(a) shows the simulation results of the relationship between $G_m(t)$ and $V_{LO}(t)$. Moreover, for a sinusoidal $V_{LO}(t)$,

$$V_{LO}(t) = V_G + v_{LO}\cos(\omega_{LO}t), \tag{3.12}$$

where V_G is the DC gate voltage, and v_{LO} and ω_{LO} are the LO amplitude and radian frequency, respectively, the corresponding $G_m(t)$, as shown in Fig. 3.7(b), can be generally expressed as

$$G_m(t) = G_{m0} + G_{m1}\cos(\omega_{LO}t) + G_{m2}\cos(2\omega_{LO}t) + G_{m3}\cos(3\omega_{LO}t) + \cdots. \tag{3.13}$$

If an RF signal with an amplitude (radian frequency) of v_{RF} (ω_{RF}) is applied to the source terminal, as shown in Fig. 3.6, the desired IF current I_{IF} for the third-order sub-harmonic mixer can be calculated as

$$I_{IF} = v_{RF}G_{m3}\cos[(3\omega_{LO} - \omega_{RF})t]/2. \tag{3.14}$$

From the above equation, it is apparent that G_{m3} should be maximized for higher conversion gain. As shown in Fig. 3.7(a), in an LO period, M_{mix} operates in three different regions—cut-off, weak-inversion, and strong-inversion. Therefore, it is

difficult to frame a general equation for G_{m3} based on the process parameters of M_{mix}. Hence, in this section, HSPICE simulations are used to observe the relationship between G_{m3}, G_{m0}, V_G, v_{LO}, and the DC current I_{DC} of M_{mix} and also to find a proper bias voltage V_G.

For a given MOS size, the value of G_{m3} is dependent on V_G and v_{LO}. Fig. 3.8(a) shows a simulation contour map of G_{m3} for various V_G and v_{LO}. In the simulation, M_{mix} has 15 fingers and the width (length) of each finger is 2.6μm (0.13μm). From Fig. 3.8(a), the maximum value of G_{m3} is obtained when V_G = 0.45V irrespective of the value of v_{LO}. Therefore, without considering I_{DC} and G_{m0}, for a given G_{m3}, V_G should be set as 0.45V in order to use the smallest M_{mix}.

However, if I_{DC} is considered, G_{m3}/I_{DC} should be used as a criterion to compare the efficiency for different conditions of V_G and v_{LO}. The simulation results of G_{m3}/I_{DC} are plotted against V_G for different v_{LO}, as shown in Fig. 3.8(b). In general, v_{LO} is determined by the VCO for other more important specifications in a receiver, e.g. phase noise. From Fig. 3.8(b), it can be observed that for all values of v_{LO}, the efficiency can be improved significantly by decreasing V_G, which results in a larger M_{mix} for a given G_{m3}. However, because the LO frequency is only 1/3 of the RF input frequency, the limitation on the size of M_{mix}, which loads the integrated VCO, is extended significantly.

When the previous stage of the mixer is an LNA, G_{m0} of M_{mix} also acts as an important parameter. In general, the performance of an LNA degrades with the increase in G_{m0}. Fig. 3.8(c) shows the simulation contour map of G_{m0} for various V_G and v_{LO}. In order to make an unbiased comparison between the different conditions, the simulation contour map of G_{m3}/G_{m0} is shown in Fig. 3.8(d). For a fixed v_{LO} and

required G_{m3}, lower V_G results in lower G_{m0} and this results in an improved LNA design.

In summary, for a given G_{m3}, lower V_G provides two advantages—lower power consumption and lower G_{m0}, with the cost that a larger size of M_{mix} is required.

3.3 CIRCUIT DESIGN

A 60-GHz single-balanced third-order sub-harmonic active mixer with a 20-GHz integrated VCO is designed and fabricated using 0.13μm CMOS technology. The circuit schematic is shown in Fig. 3.9(a). A conventional VCO structure is used for high-frequency operations. In order to reduce the capacitance at the oscillating nodes to obtain a wider tuning range, an NMOS cross-coupled pair formed by M_{ccp1} and M_{ccp2} is used in the VCO. The varactors are implemented using two n-type A-MOS's (i.e. M_{var1} and M_{var2} in Fig. 3.9(a)). Each A-MOS has 26 fingers and the finger width (length) is 2μm (0.4μm). From the simulation, it is observed that the maximum to minimum capacitance ratio of the varactor is approximately 3.57 with a quality factor of 9.7 at 20GHz. A PMOS current source M_p is used in the VCO to limit the amplitude of the output voltage. Moreover, by using M_p, the DC voltage at the oscillating nodes can be easily designed to 0.6V in order to achieve the maximum tuning range as V_{tune} ranges from 0 to 1.2V.

The differential LO signals from the VCO are applied to the gate terminals of M_{mix1} and M_{mix2}, which are the core mixing devices and V_G is set to 0V for higher efficiency, as mentioned in Section 3.2. The RF signal is applied to the common

source terminal through a transmission line *T1*, which is used to match the RF port to a 50-Ω system for measurement. Due to the balanced structure of the mixer, the fundamental and odd harmonic components of the LO signal are cancelled at the RF port. Therefore, the power leakage from the LO to the RF port mainly results from the even harmonic components. The transmission lines *T2* and *T3* are used to filter out the second LO harmonic component, denoted by 2LO and whose frequency is 40 GHz in this case, to improve the 2LO to RF isolation of the mixer. An on-chip unit-gain buffer is used to drive 50-Ω load from the measuring equipment. It should be noted that the third-order transconductances (G_{m3}) of the M_{mix1} and M_{mix2} are sensitive to the threshold voltage variation in this situation. Therefore, a bias circuit which compensates such variation can be used to bias V_G for a robust design.

It should be noted that when the RF input port does not need to be matched to the 50-Ω system or is directly connected to the LNA output port, *T1*, *T2*, and *T3* can be replaced by a notch filter, as shown in Fig. 3.9(b). The rejection frequency of the notch can be designed to be equal to the 2LO frequency to improve the 2LO to RF isolation. Moreover, if the LNA provides enough reverse isolation, such notch filter also can be replaced by a simple current source for DC bias.

M_{load1} and M_{load2} are used as active loads to improve the conversion gain to prove the proposed mixer can be used in high-gain applications. However, if the specification of the conversion gain is low (e.g. the required gain is provided by following IF stages), the passive resistive loads can be used (or in parallel with the active loads) for wider bandwidth. Moreover, the proposed mixer can also be applied to a heterodyne receiver [86] if the active loads are replaced by LC tanks that resonate

at the required IF frequency.

3.4 EXPERIMENTAL RESULTS

The die micrograph of the proposed mixer with an integrated VCO is shown in Fig. 3.10. The chip is measured on-wafer on a high-frequency probe station. The measurement setup and environment are shown in Fig. 3.11. The LO frequency is measured by the LO power leakage at the IF port. The measured and simulation frequency tuning ranges of the integrated VCO are shown in Fig. 3.12. The measured LO frequency range is from 18.18 to 20.78GHz and the corresponding RF frequency range is from 54.54 to 62.34GHz. Using either set of information, it can be determined that the tuning percentage is 13.35%. The simulation phase noise within the tuning range is also shown in Fig. 3.12. The average phase noise at 1-MHz offset is around –100dBc/Hz. The power consumption of the VCO is 6.6mW from a 1.2-V supply.

The measured and simulation conversion gains of the mixer within the tuning range when V_G = 0 and the IF frequency is fixed at 100MHz are shown in Fig. 3.13. The measured results indicate that the average conversion gain is 7.8dB and the gain variation is smaller than 2.2dB within the tuning range. Moreover, the average power consumption of the mixer core (i.e. M_{mix1} and M_{mix2}) is 0.36mW from a 1.2-V supply. The measured and simulation IF frequency response is shown in Fig. 3.14 for V_G = 0 and 0.1V. In both cases, the VCO frequency is fixed at 20GHz, while the RF frequency varies between 60.05 and 61GHz, corresponding to an IF frequency varying between 50MHz and 1GHz. When V_G = 0 V, the measured conversion gain is 8.5dB, the 3-dB bandwidth is around 300MHz, and the DC current of the mixer core

is 0.27mA. However, when V_G = 0.1V, the measured conversion gain, 3-dB bandwidth, and the DC current become 3.45dB, 500MHz, and 0.72mA, respectively. The changes in the 3-dB bandwidth and conversion gain mainly result from the variant output resistances of the active loads due to different DC currents. It should be noted that if the load resistance of the output buffer increases from 50 Ω to a few kΩ when the mixer is used in practice, the bandwidth of the mixer can be extended because the required output buffer size becomes much smaller. The measured IF power versus RF power when V_G = 0 is shown in Fig. 3.15. The input 1-dB compression point is around –10.2dBm.

Fig. 3.16 presents the measured power leakages of the 2LO and LO signals at the RF port. The 2LO and LO leakages in power are less than –35dBm and –42.5dBm, respectively, within the operating frequency range. Fig. 3.17 and Fig. 3.18 are the measured spectrums of IF power, LO-to-IF leakage, and LO/2LO-to-RF leakages. The output SNR for 1Hz is measured using a spectrum analyzer for an input frequency (intermediate frequency) of 60.1GHz (100MHz). The input power level is measured by a power meter. Based on this data, the noise figure is determined to be 27.6dB.

The fundamental conversion gain of the mixer is also measured and the measured results within the tuning range are shown in Fig. 3.19. When the input frequency around 20 GHz, the fundamental gain is 7 dB larger than the third-order gain. This implies that in the fundamental operation, the noise figure of the mixer is also 7-dB better than that in the third-order operation.

Table 3.1 presents a comparison of the performances of the integrated LO generators. As there is no doubler or buffer, the VCO can be directly connected to the proposed mixer and has a relatively larger operating frequency range and lower power

consumption. A comparison of mixer performances is shown in Table 3.2. The proposed active third-order sub-harmonic mixer has a performance comparable to that of the fundamental mixer when used in a homodyne receiver [65]. Additionally, in comparison with other sub-harmonic mixers [43], [53], the proposed mixer provides a much larger conversion gain and better isolation. Moreover, it consumes the least amount of power among all the other active mixers. The main expense of using the sub-harmonic mixer is a higher noise figure. To suppress the noise from the mixer, a high-gain LNA can be used in front of the mixer in a receiver system.

3.5 SUMMARY

In this chapter, a CMOS third-order sub-harmonic active mixer is proposed and analyzed. The required oscillating frequency of the integrated VCO is 3 times less than that required by a conventional fundamental mixer. Therefore, for a 60-GHz system, the problems in the integration of the LO due to the increase in the LO frequency can be significantly reduced. Based on the experimental results, it is apparent that in percentage, the tuning range of the integrated VCO is sufficient to cover the unlicensed band from 57 to 64GHz. In addition, the performance of the proposed mixer is comparable to that of the fundamental mixer. Moreover, due to the balanced structure and proper bias strategy, the mixer also has the advantages of good isolation and low power consumption. Therefore, this mixer has potential to be used in a CMOS 60-GHz receiver for wideband applications.

TABLE 3.1

Performance Comparison between the Integrated LO Generators in this and Other Works

	This work	[63]	[66]	[67]
Technology	0.13 μm	0.13 μm	90 nm	0.13 μm
Corresponding LO generators	VCO only	VCO and doubler	VCO only	VCO and buffer
VDD	1.2 V	1.2 V	1.2 V	N.A.
VCO tuning range (GHz)	18.18~20.78 (13.35%)	28.4~29.4 (3.46%)	61.2~64.4 (5.1%)	61.5~62.3 (1.3%)
Corresponding RF freq. (GHz)	54.54~62.34 (13.35%)	56.8~58.8 (3.46%)	61.2~64.4 (5.1%)	61.5~62.3 (1.3%)
Phase noise at 1-MHz offset (dBc/Hz)	*–100	–93	–88	–92.2
Power consumption	6.6 mW	**12 mW	N.A.	30 mW

*Simulation data (internal node cannot be measured)

** Only the power consumption of the input and core stage of the stand-alone doubler

TABLE 3.2

Performance Comparison Between the Mixers in this and Other Works

	This work	[43]	[53]	[65]
Technology	0.13 μm	SiGe	90 nm	0.13 μm
Type	Active	Active	Passive	Active
RF frequency (GHz)	60	77	33	60
IF frequency (GHz)	0.1	1	1	0.1
LO harm. no.	3^{rd}	2^{nd}	3^{rd}	1^{st}
Conversion gain (dB)	7.8	-10.3	-14	***12
P_{1dB} (dBm)	–10.2	2.4	**–2.6	N.A.
LO/2LO-to-RF iso. (dB)	*42.5/35	30/25	21.7/29.4	N.A.
Noise figure (dB)	27.6	***23	N.A.	***18.5
Power consumption	0.36 mW	22 mW	0	***1.08 mW

*Measured power leakage at RF port in –dBm ** Measured IIP3 – 9.6 dB

*** Simulation data

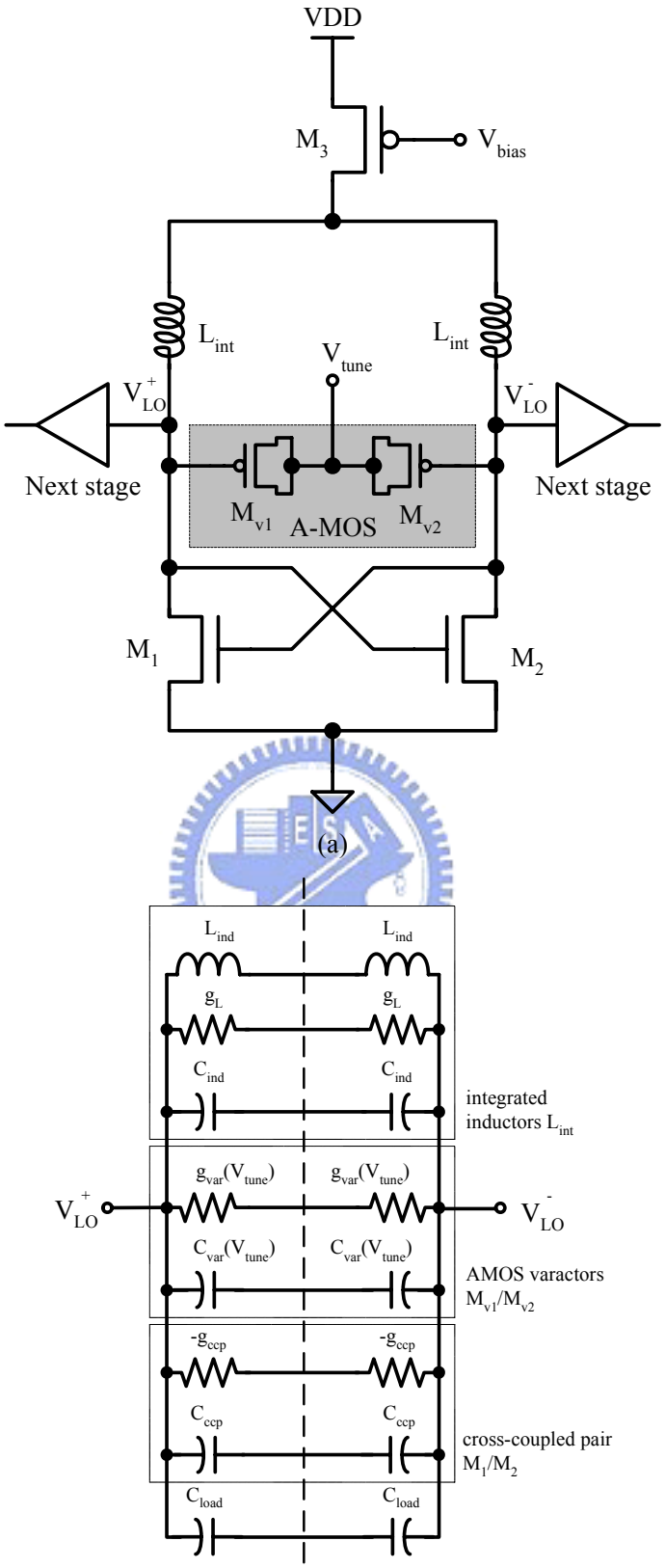


Fig. 3.1 (a) Conventional high-speed VCO (b) equivalent model of the VCO.

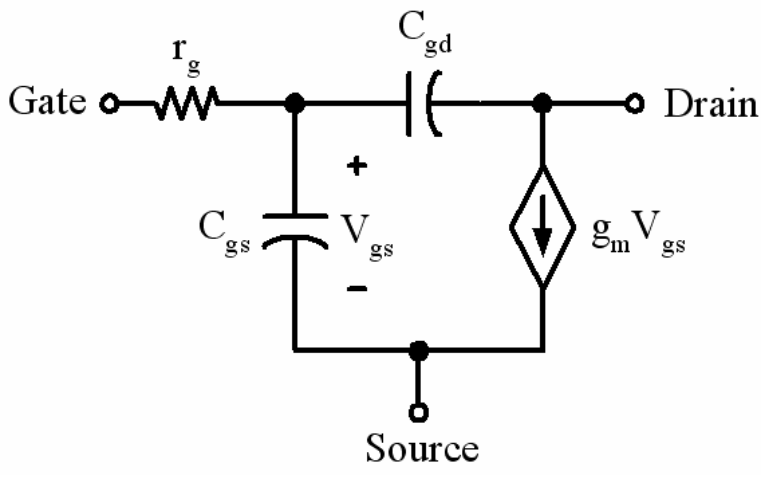


Fig. 3.2 Small signal model for M_1/M_2.

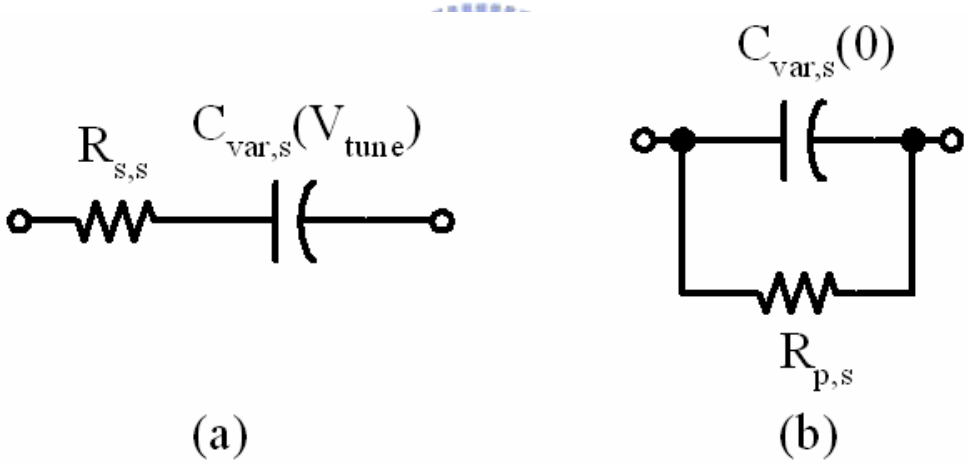


Fig. 3.3 (a) Equivalent model of a single-finger varactor and (b) equivalent parallel model when $V_{tune} = 0$.

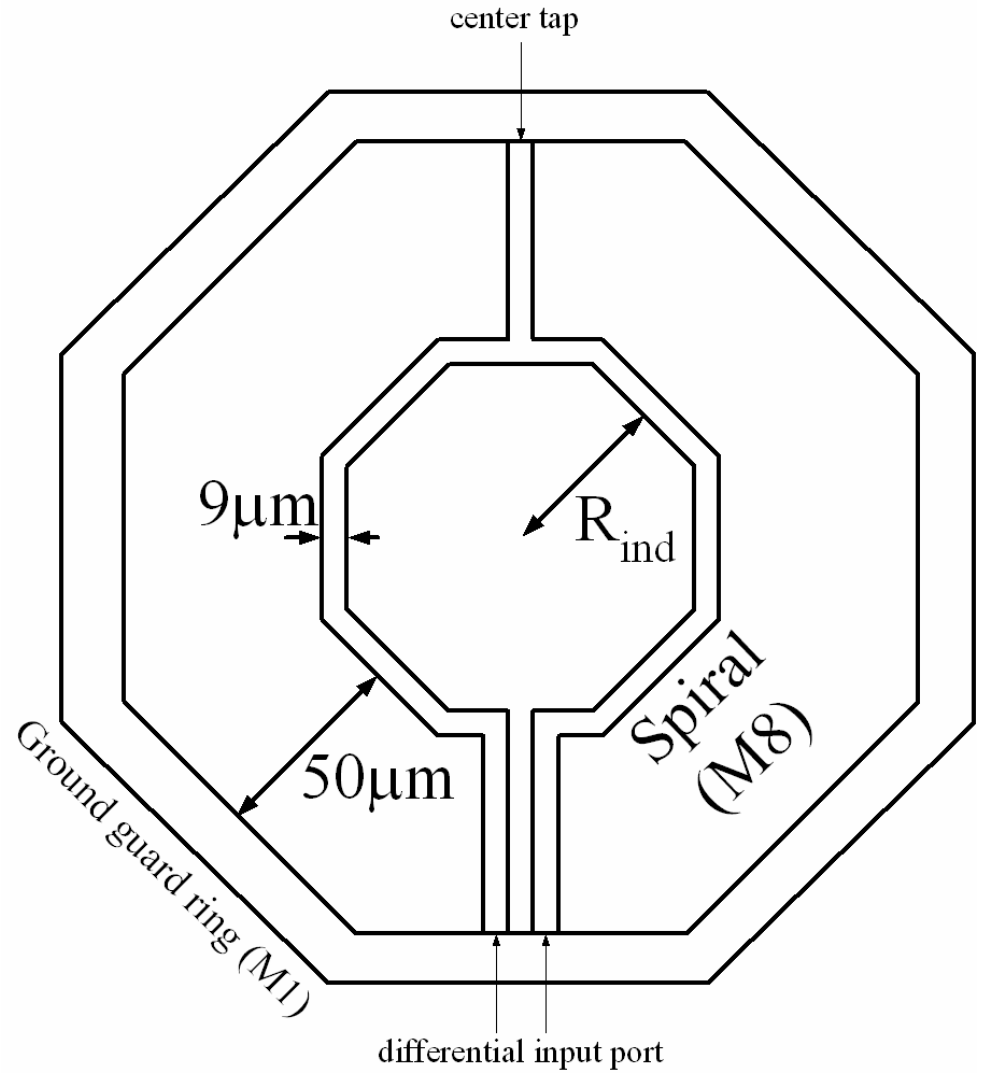


Fig. 3.4 Single-turn spiral inductor.

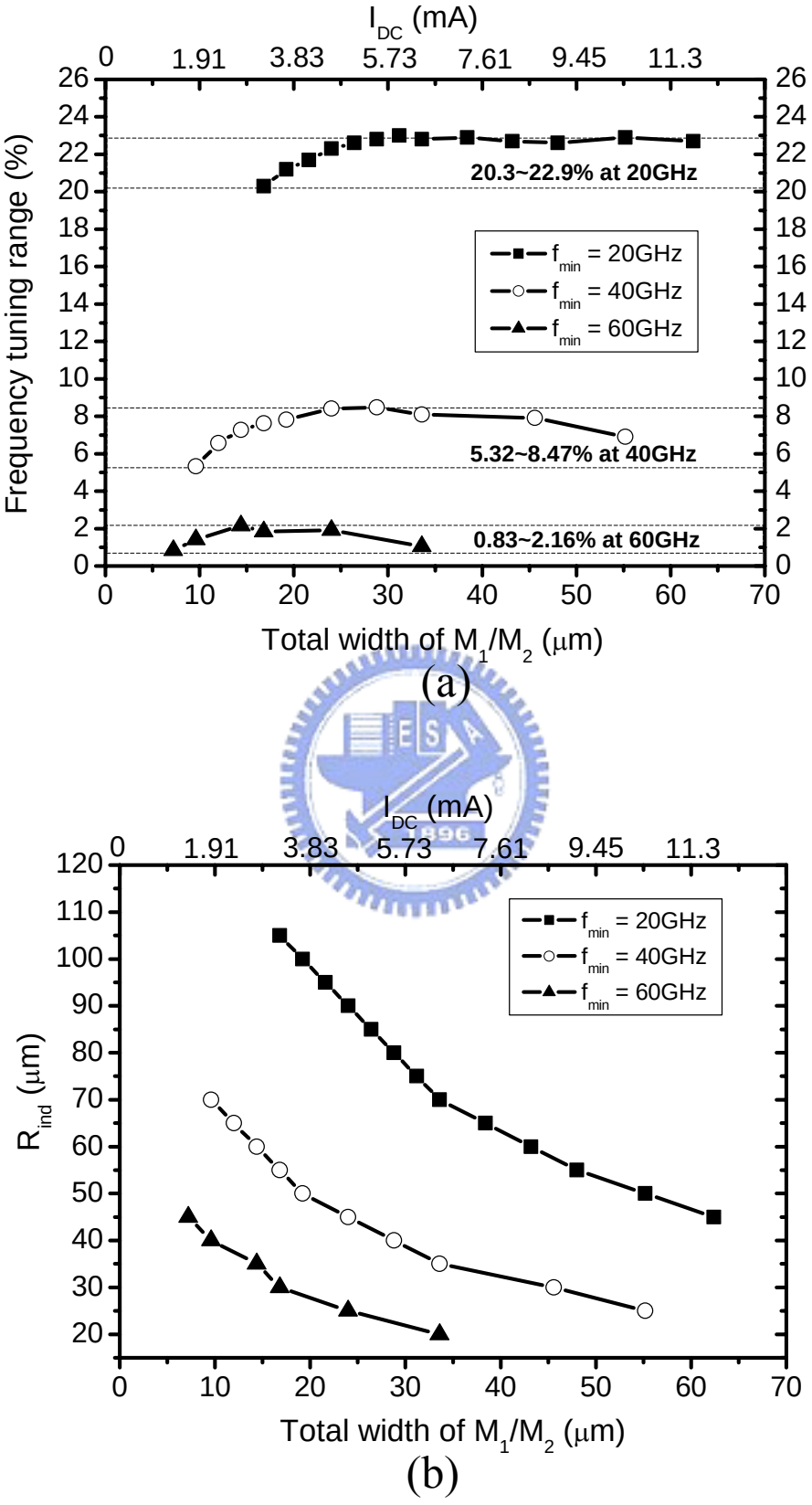


Fig. 3.5 Simulation results of: (a) frequency tuning range and (b) R_{ind}.

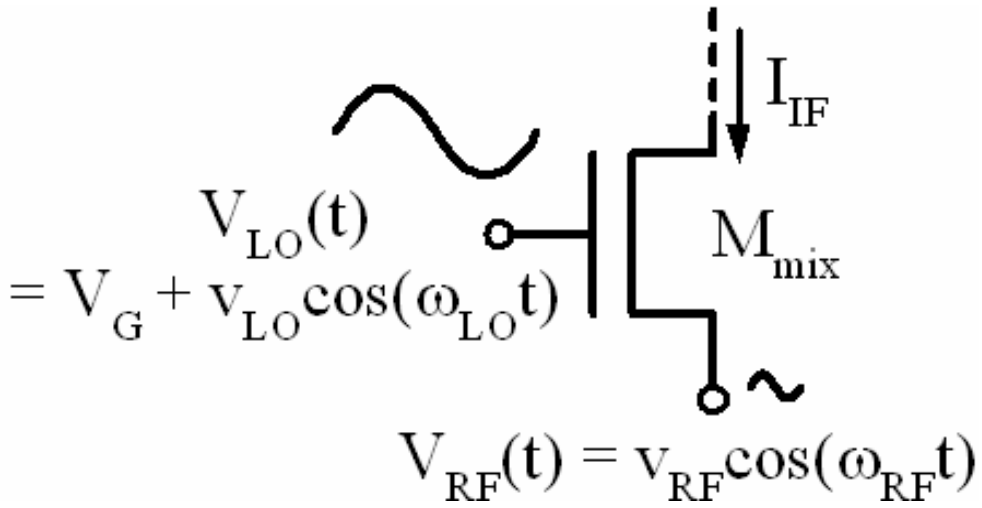


Fig. 3.6 Common-gate amplifier with time-varying transconductance.

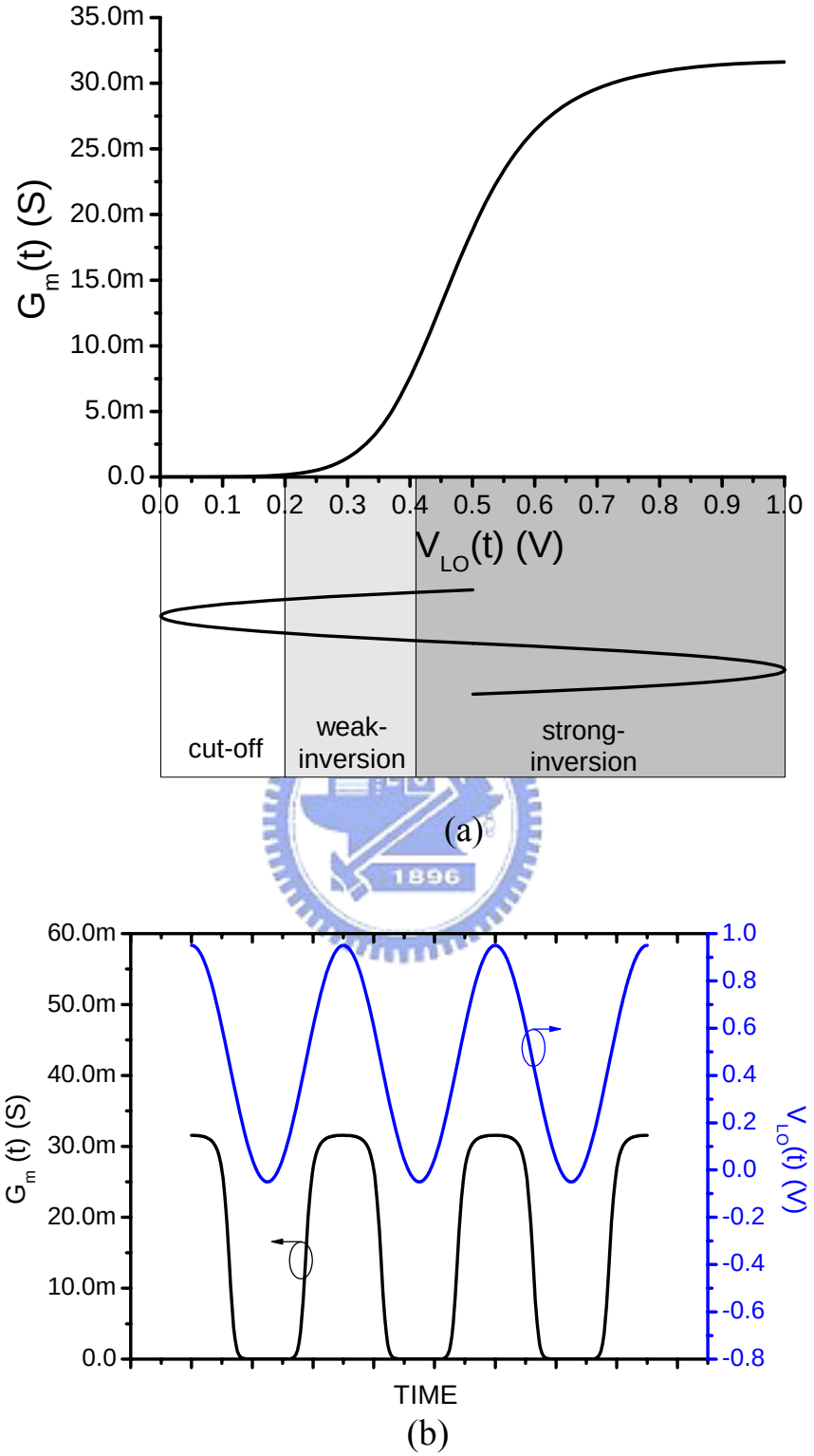
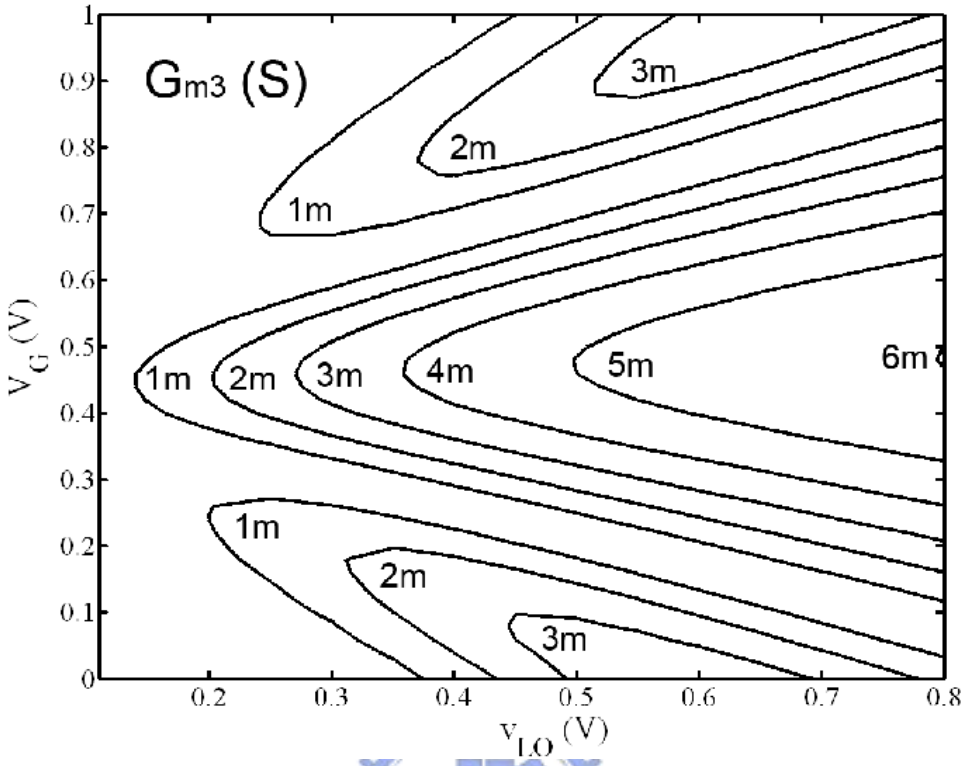
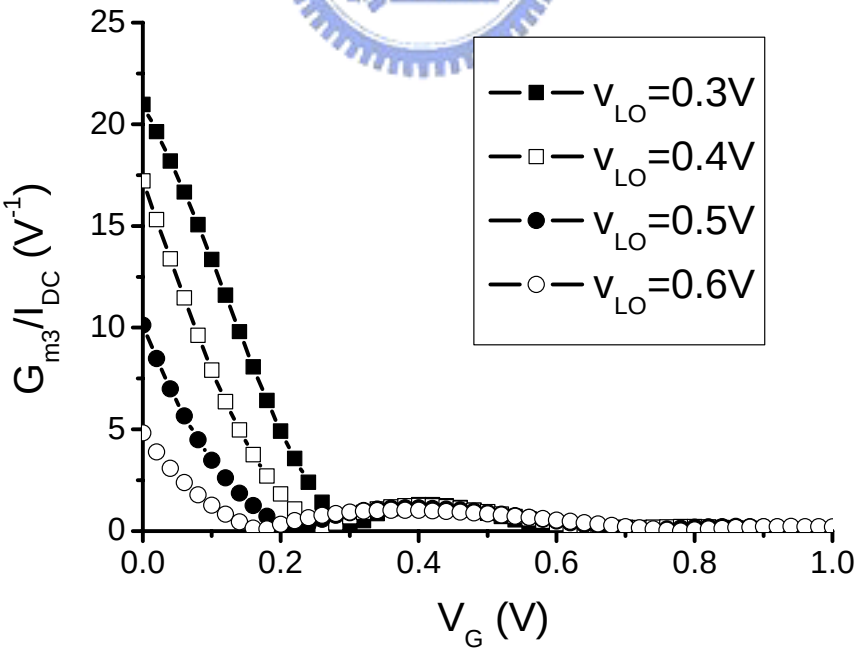


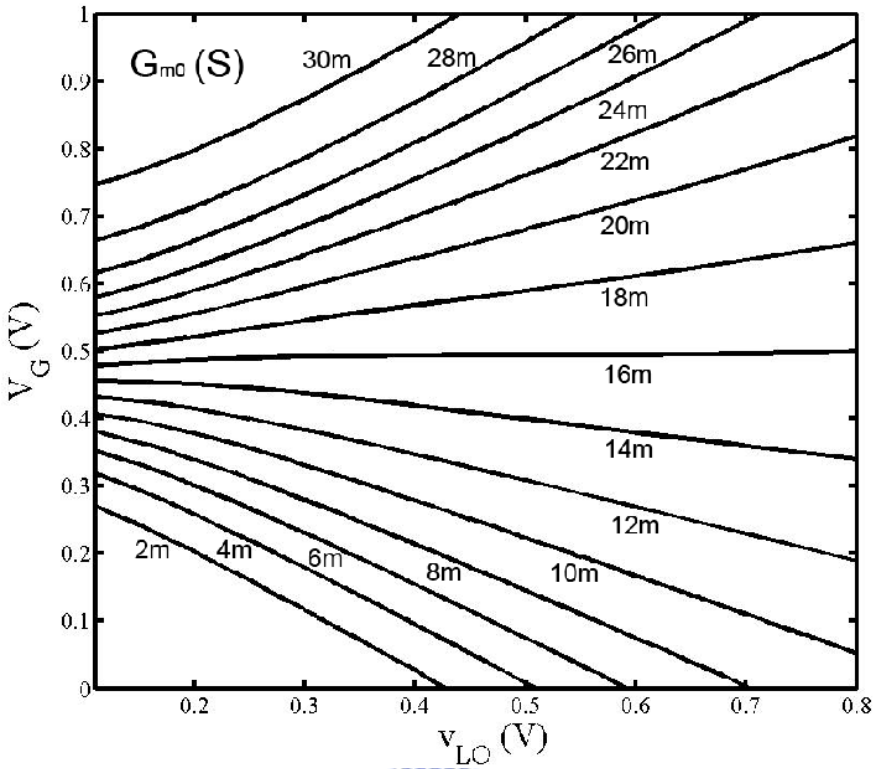
Fig. 3.7 Simulation results of (a) $G_m(t)$ versus $V_{LO}(t)$ and (b) $G_m(t)$ and $V_{LO}(t)$ versus t.


Gm3 (S)
3m
2m
1m
1m
2m
3m
4m
5m
6m
1m
2m
3m
VG (V)
VLO (V)

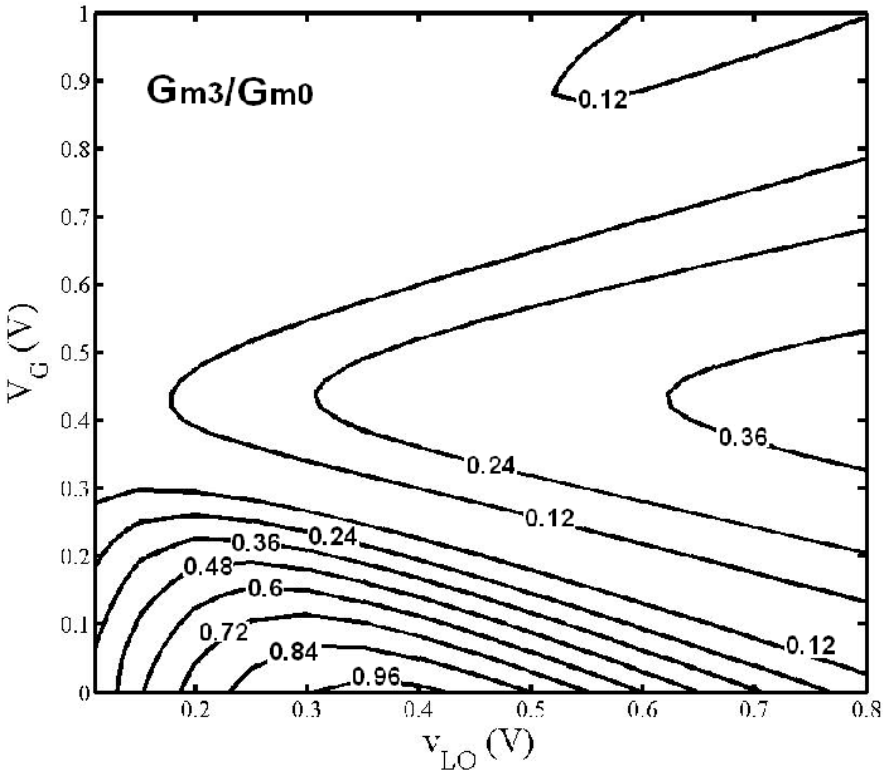
(a)


vLO=0.3V
vLO=0.4V
vLO=0.5V
vLO=0.6V
Gm3/IDC (V-1)
VG (V)

(b)



(c)



(d)

Fig. 3.8 Simulation results of (a) G_{m3}, (b) G_{m3}/I_{DC}, (c) G_{m3}, and (d) G_{m3}/G_{m0}.

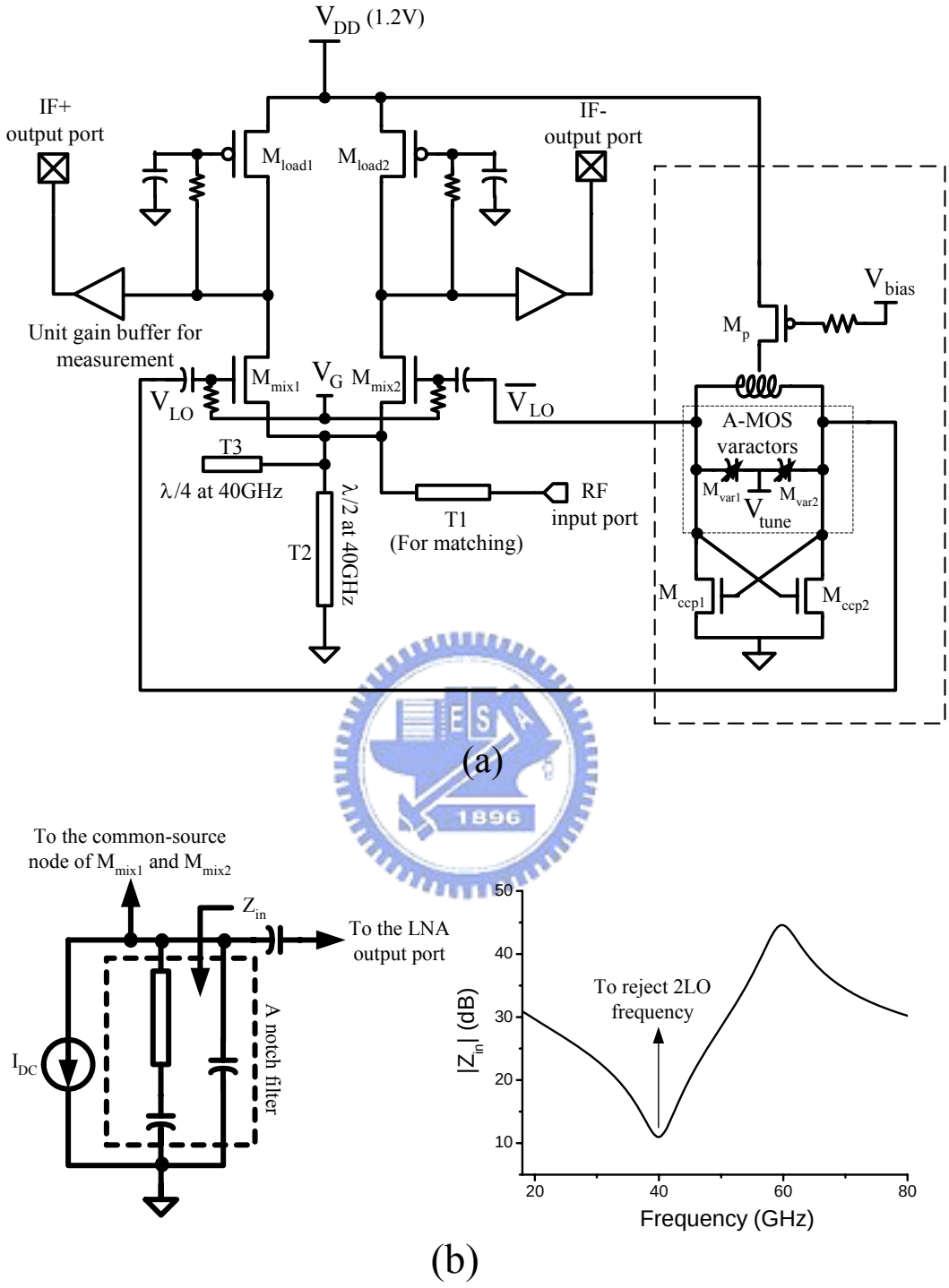


Fig. 3.9 (a) Circuit schematic and (b) notch filter and its frequency response.

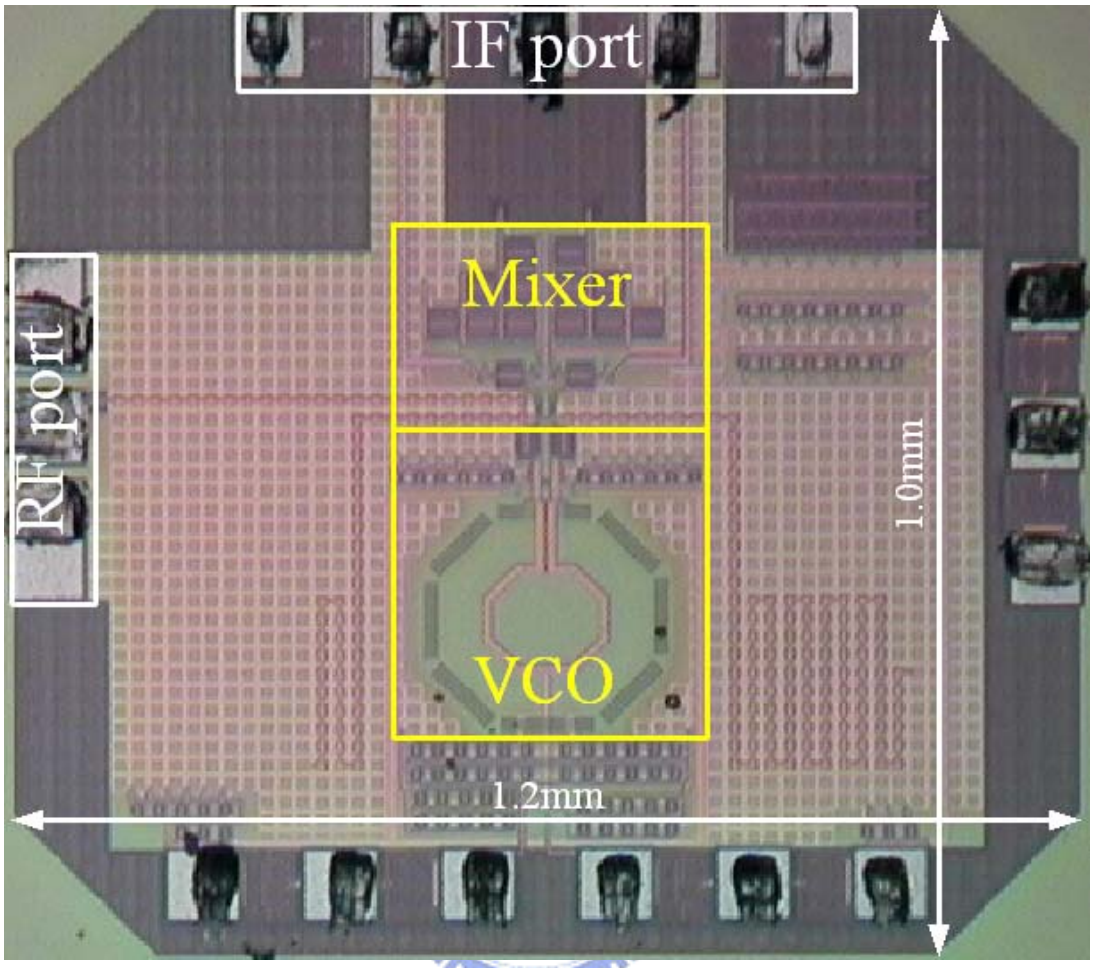


Fig. 3.10 Die micrograph.

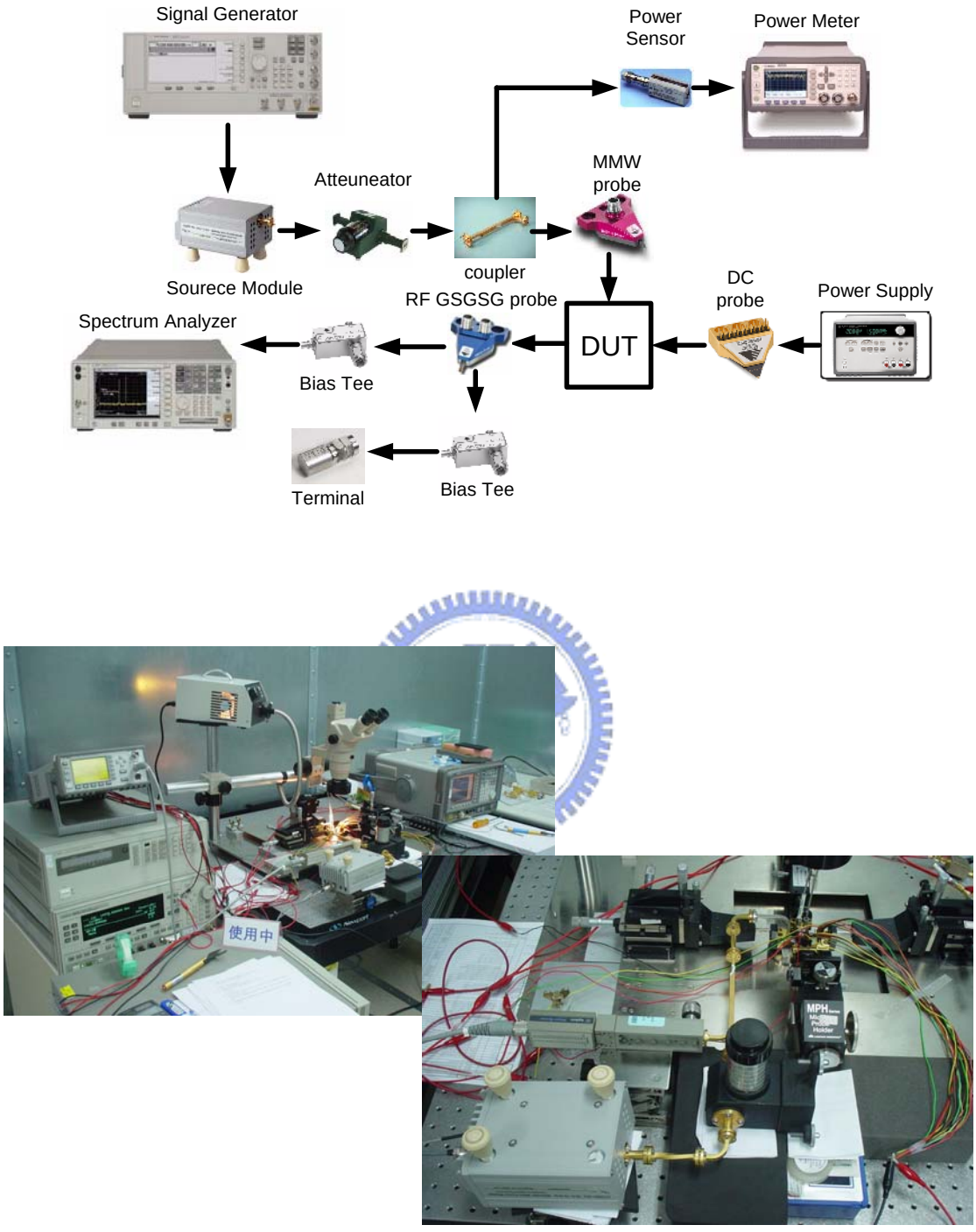


Fig. 3.11 Sub-harmonic mixer measurement setup and environment.

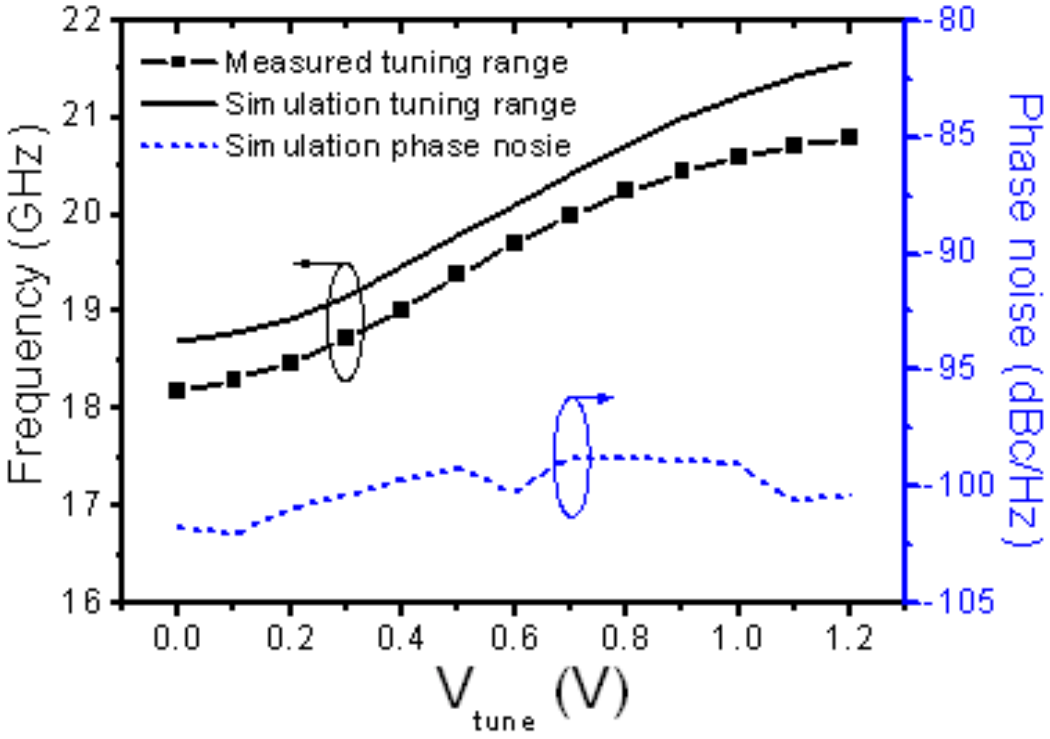


Fig. 3.12 Frequency tuning range and phase noise.

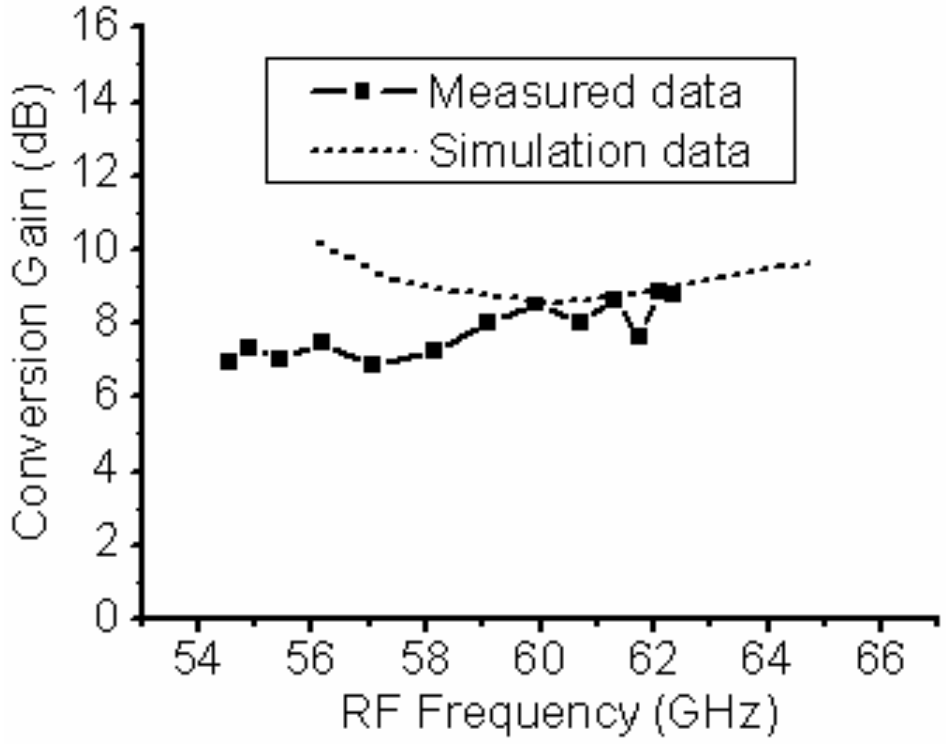


Fig. 3.13 Conversion gain within tuning range.

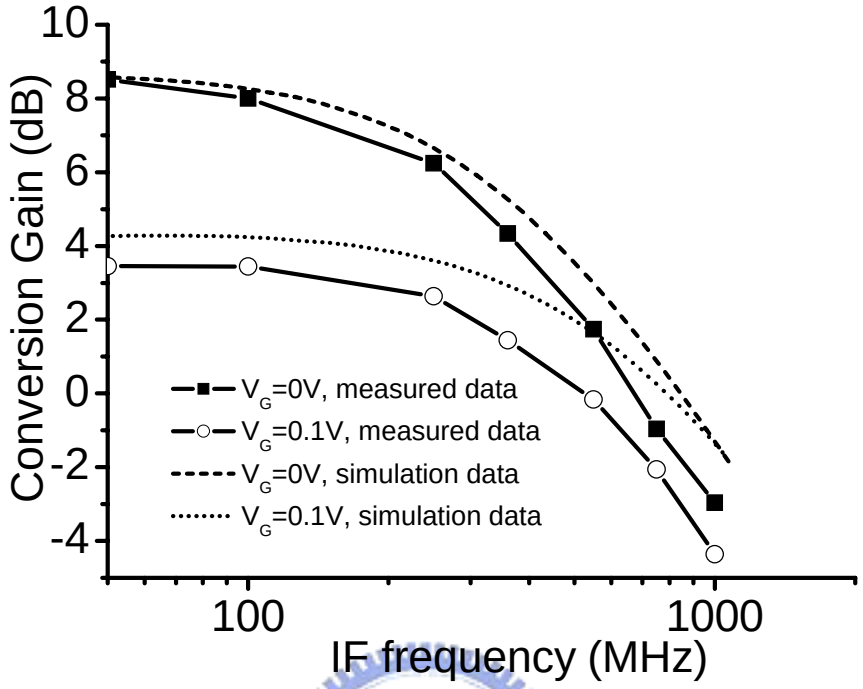


Fig. 3.14 Conversion gain versus IF frequency for different V_G.

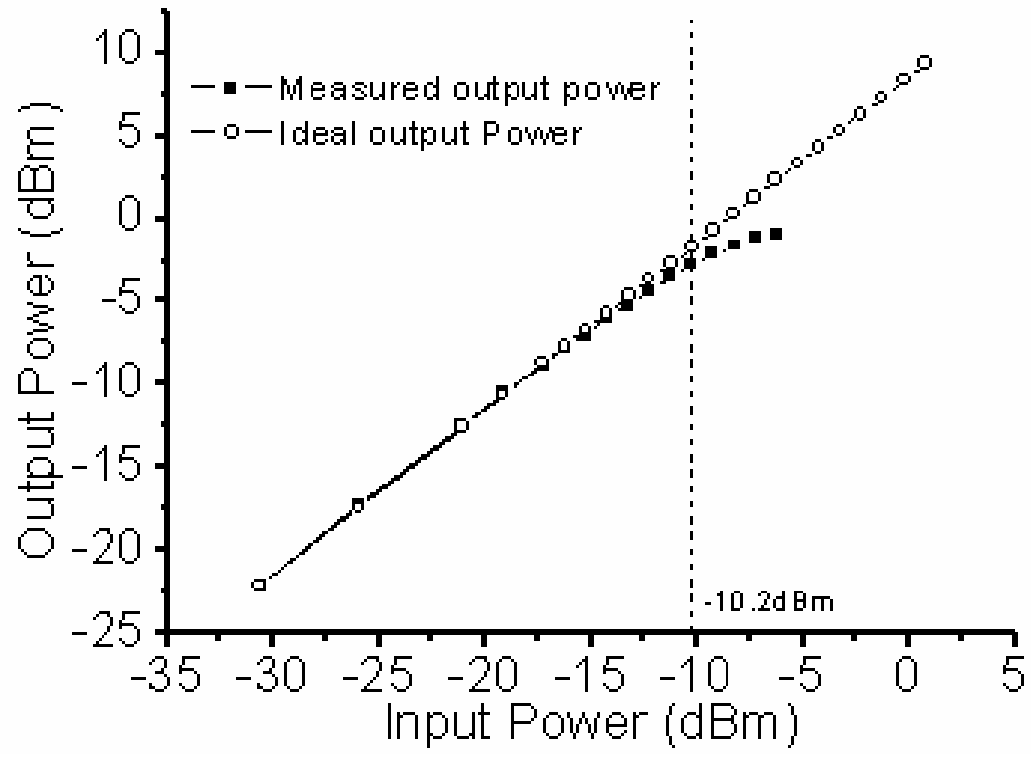


Fig. 3.15 IF power versus RF power.

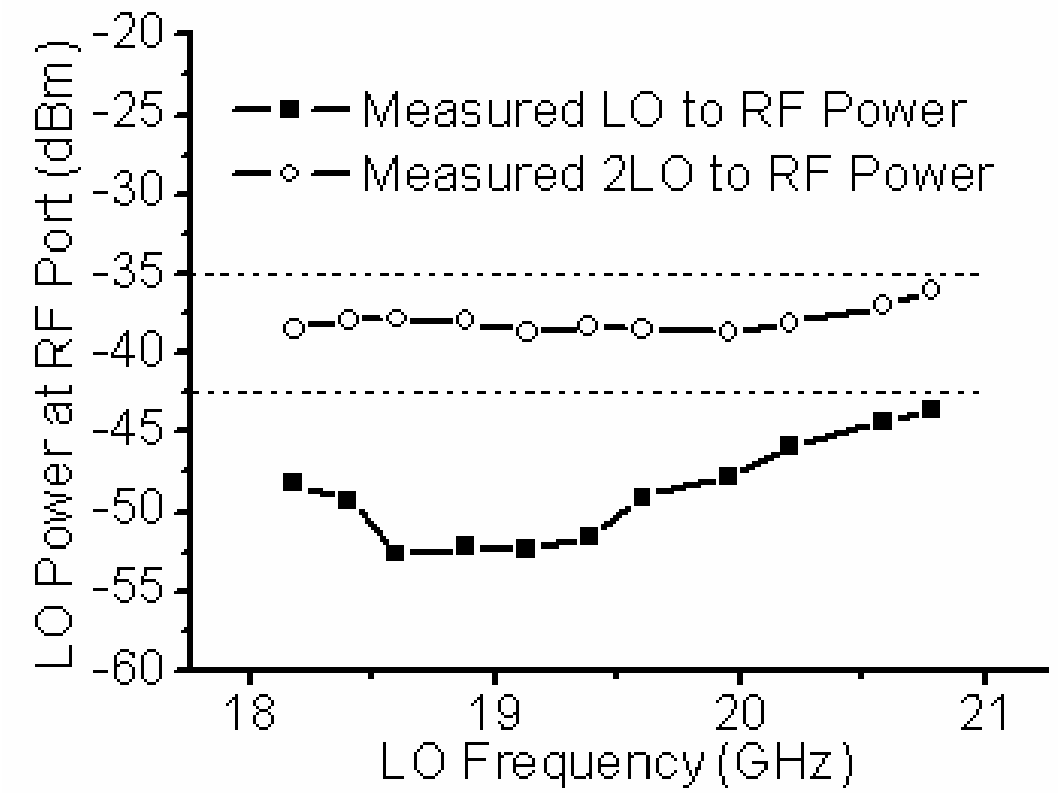


Fig. 3.16 Power leakages of the 2LO and LO signals at RF port.

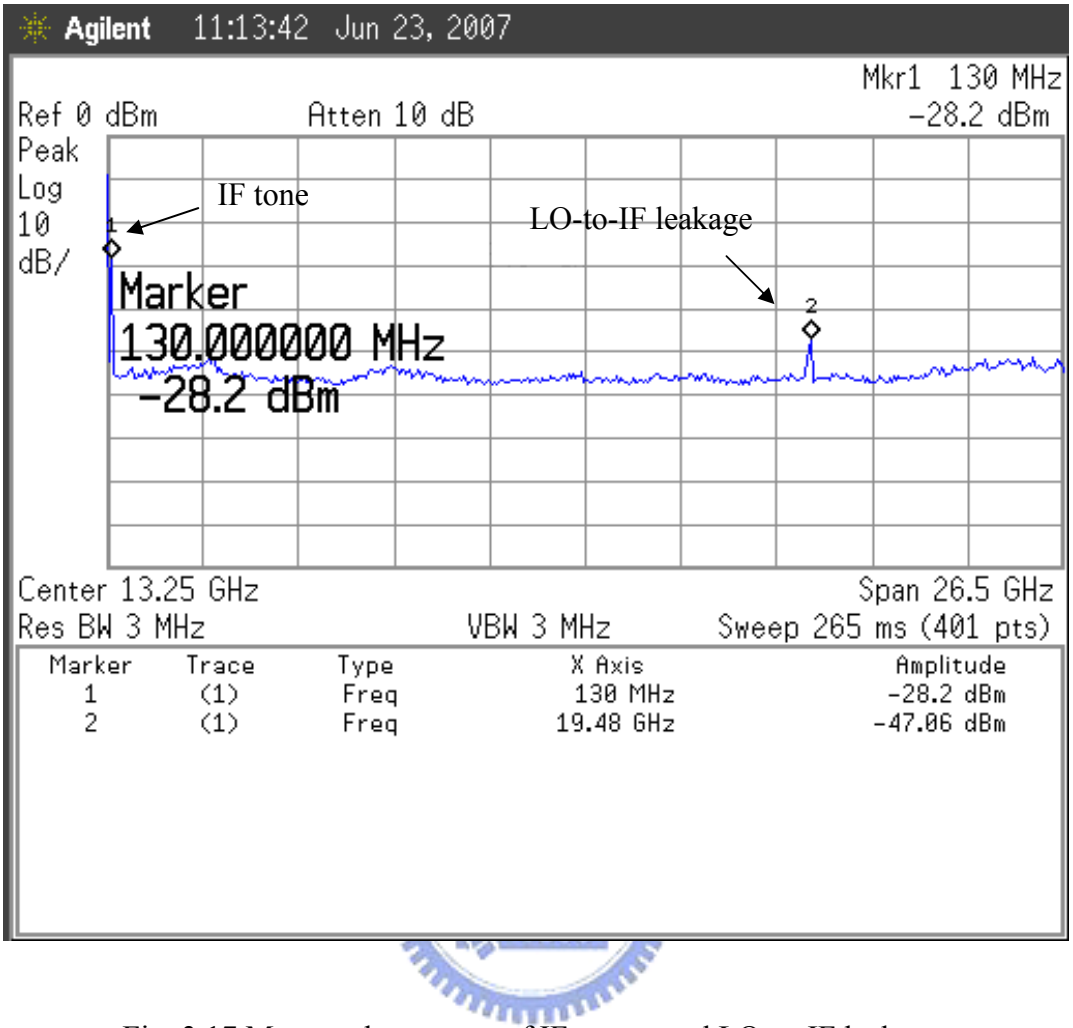


Fig. 3.17 Measured spectrum of IF power and LO-to-IF leakage.

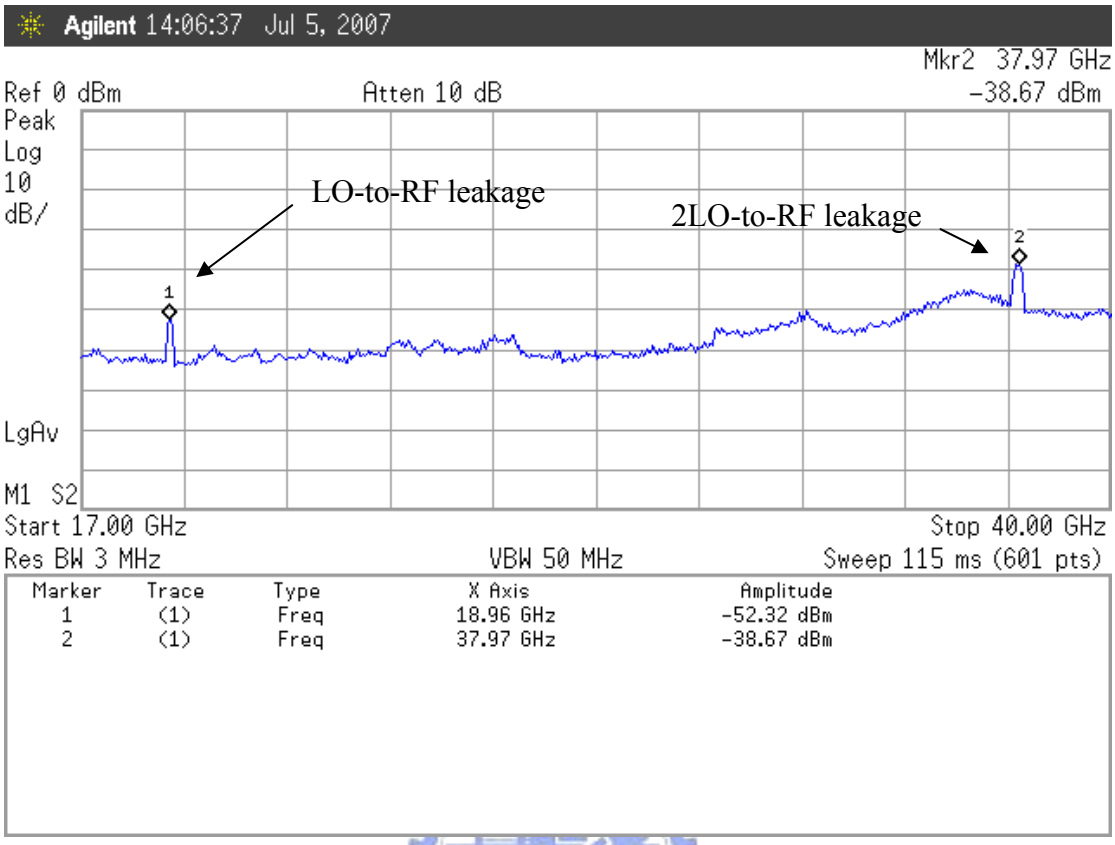


Fig. 3.18 Measured spectrum of LO/2LO-to-IF leakages.

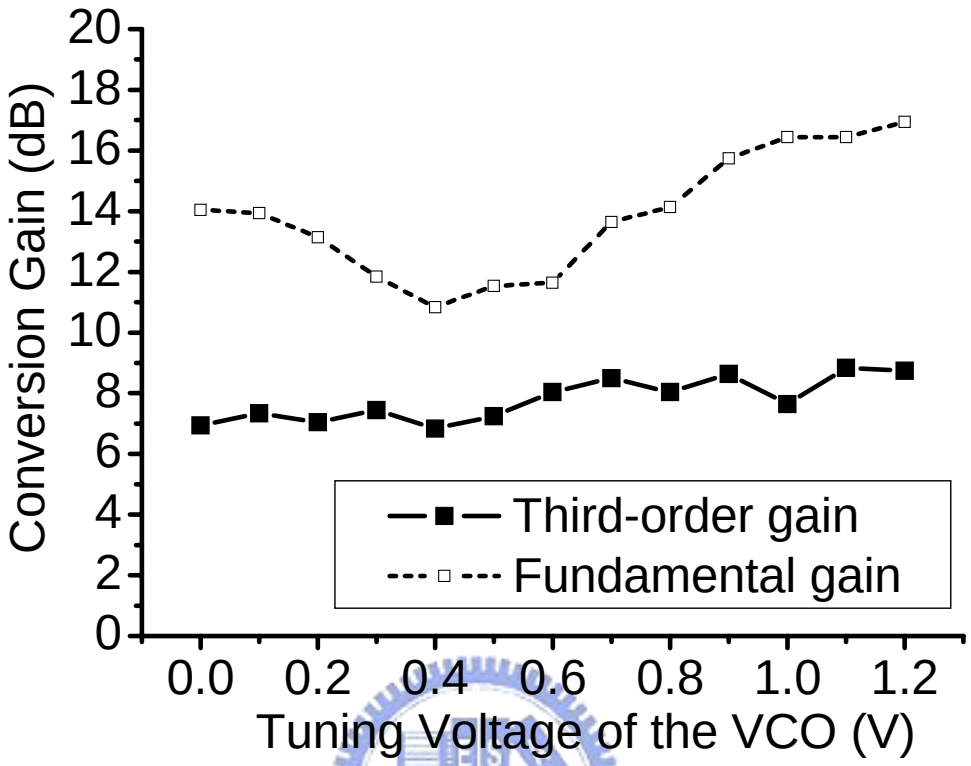


Fig. 3.19 Measured fundamental and third-order conversion gain.

CHAPTER 4

MILLIMETER-WAVE UWB HOMODYNE RECEIVER

4.1 STRUCTURE

For future UWB applications in the unlicensed band from 57 to 64 GHz, a homodyne receiver is proposed in this chapter. Fig. 4.1 shows the architecture of the proposed receiver. Through the antenna and the band-selected filter, all in-band signals are fed to the LNA input port. Therefore, within the unlicensed band, the LNA input impedance need match to the output impedance of the previous stage, which usually is 50 Ω. After the LNA, two third-order sub-harmonic mixers proposed in Chapter 3 are used in in-phase (I) and quadrature (Q) paths respectively to directly convert the RF signals to baseband signals. A quadrature VCO (QVCO) is used to generate quadrature local oscillating (LO) signals for frequency conversion. By using the sub-harmonic mixer, the required LO frequency is three times less the input frequency. Thus, corresponding to the unlicensed band from 57 to 64 GHz, the required LO frequency range is from 19 to 21.33 GHz, i.e. 11.55% at 20.165GHz. The baseband amplifier in each path has two stages and is used to enhance the voltage gain and extend the baseband bandwidth of the receiver while driving the output buffer. Finally, unit-gain output buffers are used to drive 50-Ω system for measurement in both paths.

The architecture shown in Fig. 4.1 offers several advantages over other published 60-GHz homodyne and heterodyne counterparts [60]-[69].

1) The system requires a single frequency synthesizer operating around 20GHz which is lowest among all published works, relaxing the requirement of the QVCO and prescaler.

2) Due to lower LO frequency, the frequency tuning range of the integrated LO signal generator can be extended. Therefore, the architecture is suitable for UWB applications.

3) The LO emission produced by the receiver is well out of the band and heavily suppressed by the selectivity of the antenna and LNA.

4) The architecture does not need a RF-to-IF mixer which is required in a heterodyne receiver [60]-[64]. The mixer consumes extra power. Moreover, its inductive load occupies a large area and results in a long routing path from LNA to the mixer whose parasitic effect needs to be predicted accurately.

5) In comparison with low-IF heterodyne receivers [61]-[63], the proposed receiver is immune to the image problem. Any phase-shift circuit in the RF signal path (e.g. poly phase filter) is not required. So, its area can be saved and RF routing path in layout is simplified. Moreover, the LNA performances can be improved because it need not drive a 50-Ω load.

6) The architecture is simple.

Critical design issues of a homodyne receiver are LO leakage, DC offsets, and flicker noise [40]. In a conventional homodyne receiver, the finite reverse isolation allows the LO leakage to couple to the antenna and the radiated LO power can affect nearby receivers. However, in the proposed architecture, the LO signal is well out of

the band so the LO-leakage problem can be significantly reduced.

One conventional method to remove the DC offsets is employing ac coupling [79]-[81], i.e. high-pass filtering. For the signal degradation to be negligible, the corner frequency of the high-pass filter should be less than 0.1% of the symbol rate [79]. For example, in IS-54, a data rate of 48.6 kb/s mandates a corner frequency less than 50 Hz. Such a low value requires a prohibitively large capacitors and resistors. However, the reasonable symbol rate of 60-GHz UWB applications should be larger than 1 GHz. Therefore, the corner frequency of the high-pass filter becomes around 1 MHz which is large enough to be integrated on-chip. Moreover, because the typical *1/f* noise corner frequency of a submicron MOS is in the vicinity of 1 MHz, flicker noise also can be filtered out by the high-pass filter.

From above discussions, the homodyne receiver with sub-harmonic mixer as shown in Fig. 4.1 is suitable to be used in 60-GHz UWB applications.

4.2 CIRCUIT DESIGN

4.2.1 LNA

The proposed LNA circuit schematic is shown in Fig. 4.2. A three-stage LNA is used to provide sufficient gain to suppress the noise from the following circuit blocks. The second and third stages of the LNA are implemented by conventional cascode structures where L_{LNA4} and L_{LNA6} are used to resonate with the parasitic capacitances at sources of M_{LNA3} and M_{LNA5} for higher gain and better noise performance. However, design of the first stage of the LNA is most critical because it dominates noise figure and input matching performances of the LNA. As shown in Fig. 4.2, a single

common-source transistor M_{LNA1} with source degeneration inductor L_{LNA2} and gate inductor L_{LNA1} are adopted as the first stage in the proposed LNA instead of the conventional cascade structure as shown in Fig. 4.3. This is because the noise performance of the cascade structure is degraded rapidly when the operating frequency is on the same order of the unit-gain frequency (f_T) of the transistor. The degradation of the noise performance mainly results from two reasons. Firstly, the pole at drain of M_{LNA1} due to the parasitic capacitance C_p is typically on the order of f_T /2 [65]. When the operating frequency is well below f_T, C_p can be neglected so most noise current of M_{CC}, i_n in Fig. 4.3, is trapped in the loop p_1 and does not affect the output voltage of this stage (i.e. drain of M_{CC}). However, when the operating frequency is close to f_T, a considerable portion of i_n flows from output node to ground along the path p_2 as shown in Fig. 4.3. Thus, it produces noise voltage at output node, thereby degrading the noise performance. Secondly, C_p also lowers the LNA gain because it shunts a considerable portion of the RF signal current to ground. This raises the noise contributed by i_n and degrades the noise performance further.

Some ADS simulations using 0.13μm CMOS technology are performed to observe the noise performances in both structures. Fig. 4.4 shows the simulated minimum noise figures (NF_{min}) of the LNAs in Fig. 4.2 and 4.3. In the simulations, all devices in Fig. 4.3 have the same sizes as the counterparts in Fig. 4.2 and the additional NMOS M_{cc} in Fig. 4.3 has the same size as M_{LNA1}. It can be observed that the NF_{min} increases 3.3 dB if M_{cc} is used. To find actual noise contribution from non-ideal effect of M_{cc} as mentioned before, M_{cc} in Fig. 4.3 is replaced by a noiseless current buffer with infinite f_T in another simulation and the result is also shown in Fig. 4.4. It can be found that M_{cc} contributes NF_{min} of 4.6 dB and the NF_{min} of the proposed LNA in Fig. 4.2 is much closer to this ideal case with increase in NF_{min} of only 1.3

dB.

Another important design issue of an LNA is the input matching performance. The Miller capacitor provided by the gate-to-drain parasitic capacitor of M_{LNA1} decreases after the resonance at drain node of M_{LNA1}. This characteristic significantly extends the input bandwidth to cover the frequency after the resonance. Fig. 4.5 shows simulated S11 of the LNAs in Fig. 4.2 and Fig. 4.3. For a fair comparison, in the simulations, L_{LNA1} in Fig. 4.2 and Fig. 4.3 both are optimized for the input matching bandwidth, defined as the frequency range when S11 < -12dB, to cover the unlicensed band. From Fig. 4.5, by using the proposed LNA, the input matching bandwidth can be extended from 13 GHz to 23 GHz and the improvement is 76.9%.

In summary, when the operating frequency is on the same order of transistor f_T, using a simple common-source structure as the first stage of an LNA has not only better noise performance but also a wider input matching bandwidth than using the conventional cascode structure. Therefore, it is a better choice to be adopted in a receiver for 60-GHz UWB applications.

4.2.2 Sub-Harmonic Mixer

Third-order sub-harmonic mixers are used in the proposed receiver to reduce the required LO frequency (e.g. 20-GHz LO signal for 60-GHz RF signal). Fig. 4.6 shows the circuit schematic of the proposed third-order sub-harmonic mixer. M_{Mixer1} can be seen as a voltage buffer provided a capacitive load to the previous stage, i.e. LNA. M_{Mixer2} and M_{Mixer3} are the differential common-gate amplifier whose transconductances are modulated by LO signals. As mentioned in Chapter 3, they dominate the frequency conversion. Because a high-gain stage follows the mixer and

provides enough gain, passive resistor are chosen as output load in this situation for wider baseband bandwidth. Moreover, it is very important to reduce LO-to-output leakage to prevent the saturation of the high-gain stage. Therefore, M_{Mixer3} and M_{Mixer4} whose sizes are equal to M_{Mixer2} and M_{Mixer3} are used to improve the LO-to-output isolation even their extra load effect slightly degrades gain and bandwidth. At the output node o_{mixer}^{+} (o_{mixer}^{-}), the LO leakage from M_{Mixer2} (M_{Mixer3}) can be cancelled by the opposite-phase leakage from M_{Mixer4} (M_{Mixer5}). On the other hand, because the previous stage is a 3-stage LNA with good reverse isolation, the matching network reported in Chapter 3 is replaced NMOS current sources, M_{Mixer6} and M_{Mixer7}. The current sources fix the output DC voltages which bias the following gain stages in the non-saturation operation region.

As mentioned in Chapter 3, the transconductance $G_m(t)$ of M_{Mixer2} or M_{Mixer3} can be represented as

$$G_m(t) = G_{m0} + G_{m1}\cos(\omega_{LO}t) + G_{m2}\cos(2\omega_{LO}t) + G_{m3}\cos(3\omega_{LO}t) + \cdots, \quad (4.1)$$

where ω_{LO} is the radian LO frequency. If the input voltage is $v_{RF}\cos(\omega_{RF}t)$ where v_{RF} (ω_{RF}) is the input RF voltage amplitude (radian frequency), the desired differential output mixing term V_{IF} can be calculated as

$$V_{IF} \approx v_{RF}\, g_{m1} G_{m3} R_{mixer} \cos[(3\omega_{LO} - \omega_{RF})t]/2G_{m0}\,, \quad (4.2)$$

where g_{m1} is the small signal transconductance of M_{Mixer1} and R_{mixer} is the load resistance as shown in Fig. 4.6. From (4.2), the differential conversion gain A_{mixer} of the third-order sub-harmonic mixer can be calculated as

$$A_{mixer} = g_{m1} G_{m3} R_{mixer} / G_{m0}\,, \quad (4.3)$$

which is proportional to G_{m3}/G_{m0}. The simulated contour map of G_{m3}/G_{m0} is shown in Fig. 3.8(d) in Chapter 3. In this case, a current source M_{mixer6} (M_{mixer7}) is used to control bias current of M_{Mixer2} and M_{Mixer3} (M_{Mixer4} and M_{Mixer5}), which determines the gate-to-source DC voltages of M_{Mixer2} and M_{Mixer3} (M_{Mixer4} and M_{Mixer5}). Therefore, as the analysis in Chapter 3, for a given G_{m3}/G_{m0}, the bias current should be designed as low as possible until the total size of M_{Mixer2} to M_{Mixer5} reaches the maximum which can be accepted by the previous stage, i.e. the integrated QVCO.

4.2.3 Quadrature VCO

Due to the reduction of the required LO frequency, for a 60-GHz direct-conversion receiver, the conventional QVCO [81] can be integrated in the system easily while covering entire unlicensed band from 57 to 64 GHz (the corresponding LO frequency is from 19 to 21.33 GHz). Fig. 4.7 shows the circuit schematic of the QVCO.

In order to reduce the capacitance at the oscillating nodes to obtain a wider frequency tuning range, NMOS cross-coupled pairs formed by M_{QVCO1} to M_{QVCO4} are used in the QVCO. M_{QVCO5} to M_{QVCO8} provide coupling between the output ports for quadrature outputs. The varactors are implemented using n-type A-MOS's. Each A-MOS has 29 fingers and the finger width (length) is 2μm (0.5μm). The simulated maximum to minimum capacitance ratio of the varactor is approximately 3 with a quality factor of 8.49 at 20GHz. M_{QVCO9} and M_{QVCO10} are biased in the triode region and the DC voltages at the output nodes are designed as *VDD/2* (0.6 V in this case) in order to achieve the maximum tuning range as V_{tune} ranges from 0 to *VDD* (1.2 V in this case).

4.2.4 Baseband Amplifier and output buffer

Fig. 4.8 shows the circuit schematic of the baseband amplifier and the output buffer. The baseband amplifier consists of two cascaded differential pairs and is used to enhance the receiver gain and extend the bandwidth while driving the output buffer. The output buffer provides unit voltage gain when the off-chip 50-Ω loads is connected to its output ports.

4.2.5 Layout consideration

Layout is an important step in designing the receiver when the operating frequency is up to 60 GHz, because a different shape or length of each interconnecting metal line may significantly affect the performances of the receiver. Therefore, all parasitic effects from the interconnections on the MMW signal path are considered in the circuit design by using an EM simulator (Ansoft HFSS). Using 0.13-μm CMOS technology, the circuit layout of the receiver is shown in Fig. 4.9. The interconnections between the LNA and mixers are extracted with the inductors as a 17-ports component for EM simulation as shown in Fig. 4.10 (a). Moreover, the parasitic inductances of the interconnections between QVCO and mixers significantly reduce the down-conversion gain, so the interconnections should be designed as short as possible. In this design, they are extracted as a 12-ports component for EM simulation as shown in Fig. 4.10 (b).

Except the interconnections on the RF and LO paths, the layout of the cascode devices, i.e. M_{LNA3} and M_{LNA5} in Fig. 4.2, should be designed carefully as well. Considering the parasitic inductor L_{pg} at gate node to VDD as shown in Fig. 4.11, M_{LNA3} or M_{LNA5} provides negative resistance looking into its source like in a Colpitts

oscillator. Therefore, the parasitic inductor L_{pg} significantly degrades the stability of the LNA. To reduce the effect from L_{pg}, space near the gate node should be reserved to put a bypass capacitor to ground. In this design, two sandwich capacitors, marked by C_{LNA3} and C_{LNA5} as shown in Fig. 4.9, are put close to the gate nodes of M_{LNA3} and M_{LNA5} as bypass capacitors to ground to improve the LNA stability.

4.3 SIMULATION RESULTS

4.3.1 Quadrature VCO

The simulation frequency tuning ranges of the integrated QVCO are shown in Fig. 4.12. The LO frequency range is from 18.31 to 22.35 GHz (i.e. 19.87% at 20.33 GHz) and the corresponding MMW frequency range is from 54.93 to 67.05 GHz which covers the entire unlicensed band. The simulation phase noise within the tuning range is also shown in Fig. 4.12. The average phase noise at 1-MHz offset is around -96 dBc/Hz. Using the mismatching models provided by the foundry, 60-times Monte-Carlo simulations are performed to observe the phase and amplitude mismatch of the integrated QVCO. Fig. 4.13 (a) and (b) show the simulation results. The phase error varies form -1.6° and 1.34°. The average differential peak-to-peak voltage amplitude is 2.09 V and the maximum amplitude error is 5 mW. The power consumption of the QVCO is 23.65 mW from a 1.2-V supply.

4.3.2 LNA

Simulation results of S11 of the LNA are shown Fig. 4.14. The frequency range when S11 < -12 dB is from 57 to 79 GHz and covers the entire unlicensed band. The voltage gain of the LNA is shown in Fig. 4.15. Within the unlicensed band of 57 to 64

GHz, the voltage gain varies from 15.4 to 17.2 dB. The noise figures of the LNA are shown in Fig. 4.16. The noise figure varies from 5.89 to 6.83 dB from 57 to 64 GHz. The power consumption of the LNA is 7.3 mW from a 1.2-V supply.

The stability factor [83]

$$\mu \equiv \frac{1-|S11|^2}{|S22-S11^{*}\Delta|+|S21S12|}, \tag{4.4}$$

where

$$\Delta \equiv S11S22 - S12S21 \tag{4.5}$$

is used here for the stability simulation. Fig. 4.17 shows the simulation results of μ. From 1k to 100 GHz, μ is larger than 1 which necessarily and sufficiently proves that the LNA is unconditional stable within the frequency range.

4.3.3 Receiver

The simulation voltage gains of the receiver within the entire QVCO frequency tuning range when the IF frequency is fixed at 500MHz are drawn in Fig. 4.18. Considering the unlicensed band of 57 to 64 GHz, the voltage gain varies from 25 to 29.25 dB and the input frequencies for the extreme cases are 57.5 and 61.88 GHz, respectively. The simulation baseband frequency responses with different LO frequencies are shown in Fig. 4.19. In all simulations, when the QVCO frequency is fixed at f_{LO}, the input frequency varies between $3 \times f_{LO}$ + 50 MHz and $3 \times f_{LO}$ + 3 GHz, corresponding to an IF frequency varying between 50 MHz and 3 GHz. Among all cases, the minimum and maximum 3-dB bandwidths are 2.7 and 1.1 GHz and the

corresponding 3 × f_{LO} are 57 and 63.57 GHz, respectively.

The simulation noise figures as 3 × f_{LO} ranges from 57 to 64 GHz are shown in Fig. 4.20, where the noise figure varies from 11.11 to 13.4 dB and f_{LO} for the extreme cases are 20.25 and 19 GHz (i.e. 3 × f_{LO} = 60.75 and 57 GHz), respectively. By the way, the noise figure of the sub-harmonic mixer is around 24dB. It should be noted that different corner cases results in different device unity gain frequencies which vary the receiver performance in the most simulations.

The simulated baseband output power versus RF input power is shown in Fig. 4.21. The input 1-dB compression point is around -28 dBm. A two-tone simulation is used to find the input IIP_3 and the results are shown in Fig. 4.22. The input IIP_3 is around -18.2 dBm. The transient waveforms of quadrature LO signals and the I/Q baseband output signals are shown in Fig. 4.23 (a) and (b), respectively. The whole receiver consumes 35.6 mW from a 1.2-V supply.

The performances of the proposed and other 3-stage LNAs operated around 60 GHz are compared in Table 4.1. The power consumption of the proposed LNA is smallest among them because the LNA can directly connect to the mixers which can be seen as capacitive load instead of resistive load. Moreover, the LNA has the widest input matching bandwidth due to the single common-source structure of the first stage. The performances of the proposed receiver and other CMOS receivers operated around 60 GHz are compared in Table 4.2. Even though the homodyne strategy is adopted, a QVCO can be integrated into the receiver successfully while its frequency tuning range can cover the unlicensed band of 57 to 64 GHz. Due to the simple structure, the power consumption of the proposed receiver is lower than other heterodyne and low-IF receivers, although some of them are implemented using more

advanced technology. The 1-dB compression point of the proposed receiver is lower because a high gain LNA is required to suppress the noise from sub-harmonic mixers and maintain the noise figure. Therefore, the main expense of using sub-harmonic mixers for broadband operation is a stricter trade-off between the noise and linearity.

4.4 SUMMARY

In this chapter, a 60-GHz homodyne receiver is proposed and analyzed. The receiver consists of: 1) an integrated QVCO for qudrature down conversion; 2) an LNA with low noise figure and wide input matching bandwidth; 3) third-order sub-harmonic mixers in I/Q paths; and 4) baseband amplifiers and output buffers in I/Q paths.

The proposed receiver is highly integrated and its operating frequency range is sufficiently to cover the unlicensed band of 57 to 64 GHz. Moreover, the power consumption of the receiver is lower than heterodyne or low-IF receivers because its structure is much simpler. Therefore, the proposed homodyne receiver is a favorable choice for use in future 60-GHz UWB applications.

Table 4.1

Performance Benchmark of 3-stage LNAs

References	*This work	[61]	[63]	***[66]
Technology	0.13μm	0.13μm	0.13μm	90nm
VDD	1.2	1.2	1.5	1.2
Load type	Capacitive	Resistive	Resistive	Resistive
Frequency (GHz)	60	50	60	60
Gain (dB)	**17.2	18	12	16.3
NF (dB)	5.89	*5.8	8.8	7.8
Matching bandwidth	S11<-12dB 57-80GHz	S11<-8dB 49-51GHz	S11<-12dB 51-65GHz	S11<-10dB 60-66GHz
Power consumption	7.3mW	17.8mW	36mW	42.84mW

* Simulation data ** Voltage gain *** Differential LNA

Table 4.2

Performance Comparison between the Proposed Receiver and Other Receivers Operated around 60GHz

References	*This work	[63]	[64]	[65]	[66]
Technology	0.13μm	0.13μm	90nm	0.13μm	90nm
Structure	homodyne	heterodyne	half-IF	homodyne	homodyne
LO integration	with	with	with	without	with
Quadrature down conversion	with	without	with	without	without
Operating freq. range (GHz)	57-64	56.8-58.8	57-61	57-64	61.4-63
LO freq. tuning range (GHz)	18.3-22.4 (19.87%)	28.4-29.4 (3.46%)	28.5-30.5 (6.78%)	off-chip LO signal	61.2-64.4 (5.1%)
Gain (dB)	25-29.25	11.8	18.3-22	24-28	21.8-22.5
S11 (dB)	< -12	N.A.	N.A.	N.A.	N.A.
NF (dB)	11.1-13.4	10.4	5.7-8.8	12.5-15.4	8.4
P_{1dB} (dBm)	-28	-15.8	-27.5	-22.5	N.A.
P.N. (dBc/Hz) at 1-MHz offset	-96	-86	-87	off-chip LO signal	-88
Power consumption	35.6mW	64mW	36mW	9mW (without VCO)	**60mW
VDD	1.2V	1.2V	1.2V	1.2V	1.2V

* Simulation data

** Exclusive of the frequency synthesizer for a fair comparison

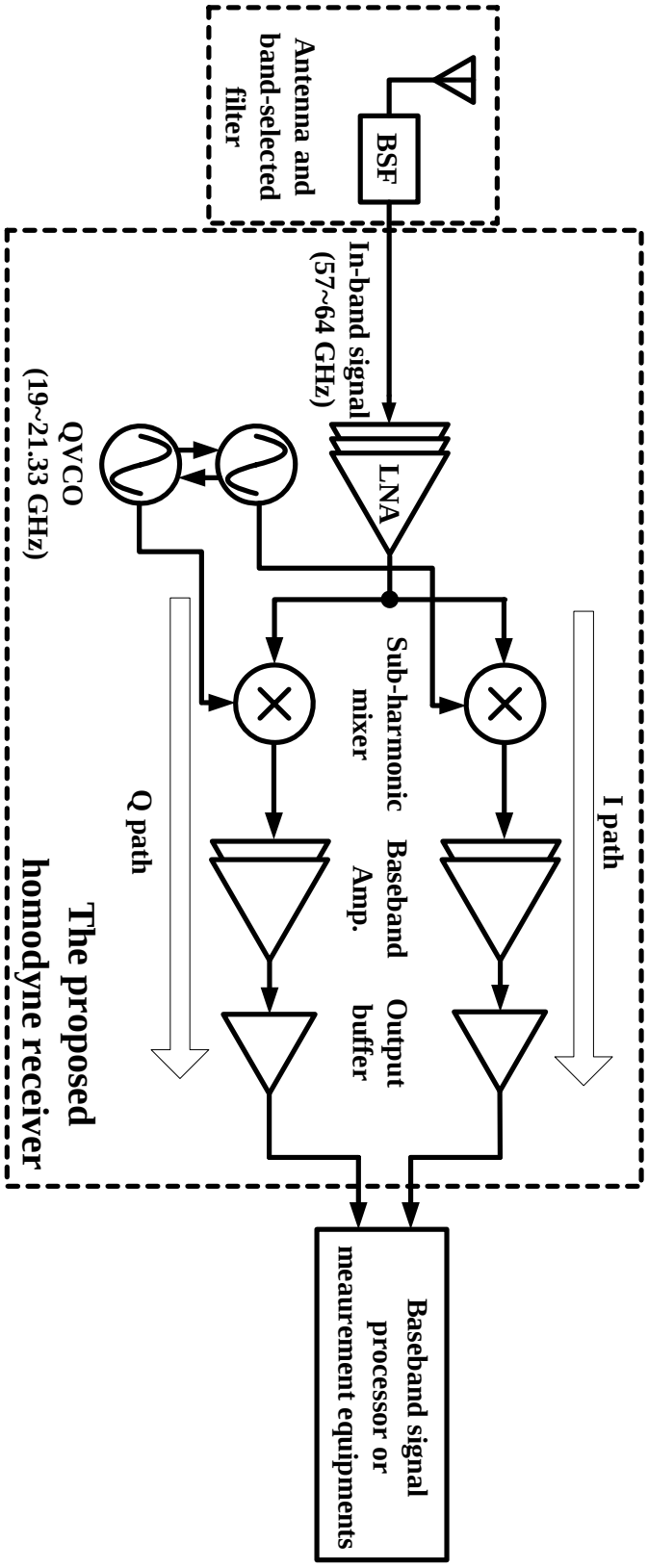


Fig. 4.1 Architecture of the proposed receiver.

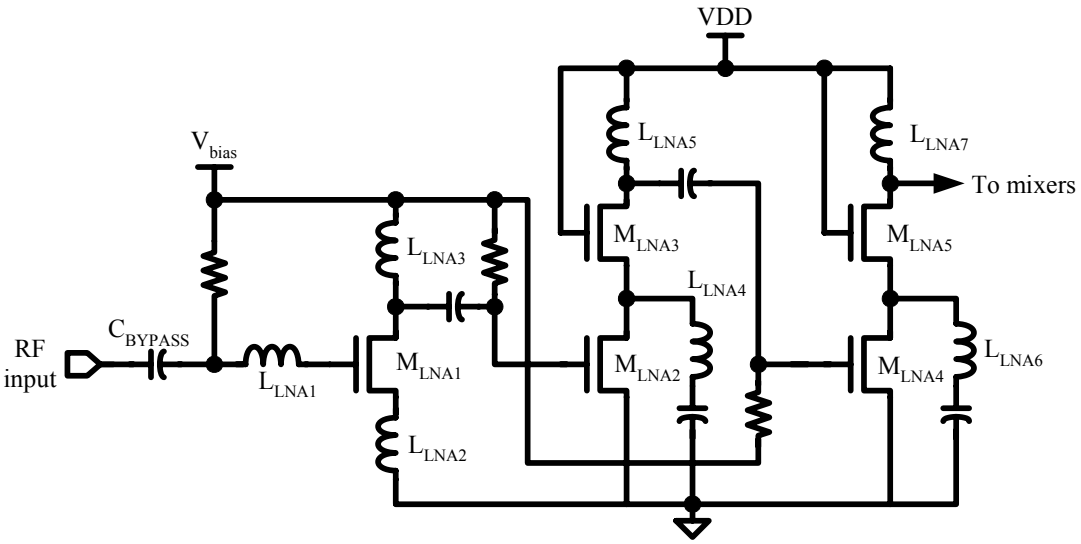


Fig. 4.2 Proposed LNA circuit schematic.

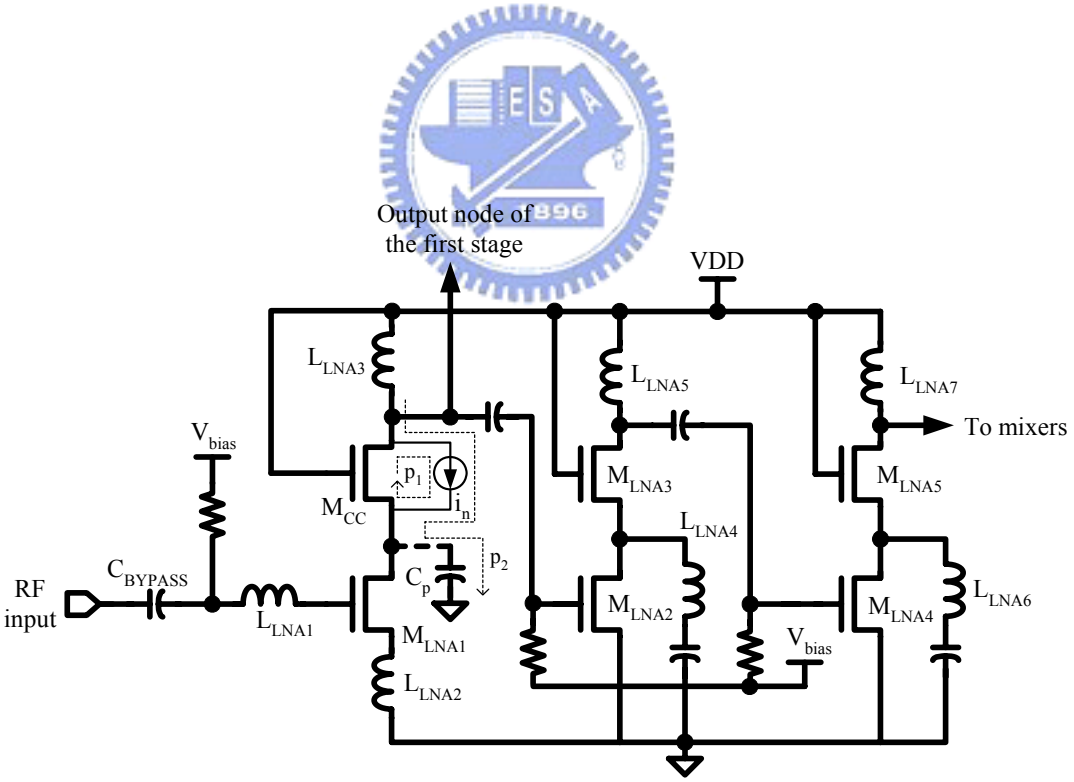


Fig. 4.3 LNA using conventional cascode structure as the first stage.

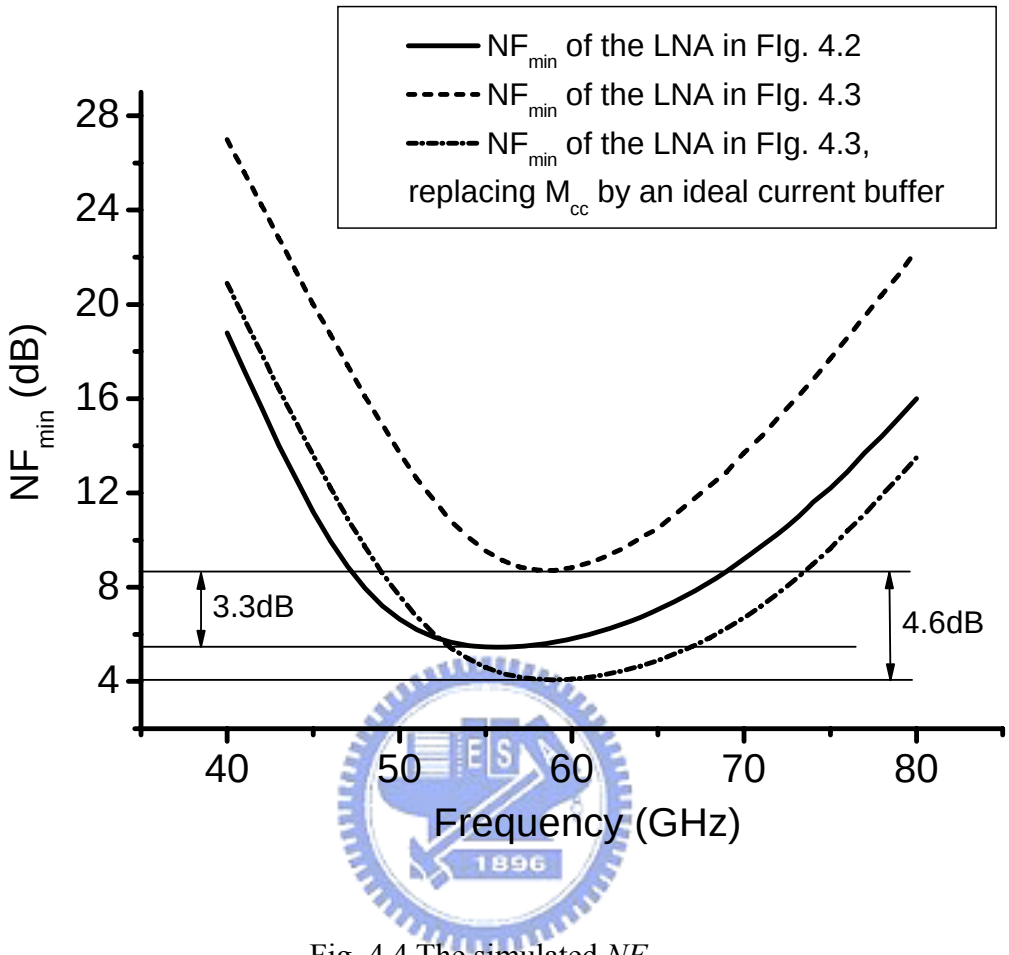


Fig. 4.4 The simulated NF_{min}.

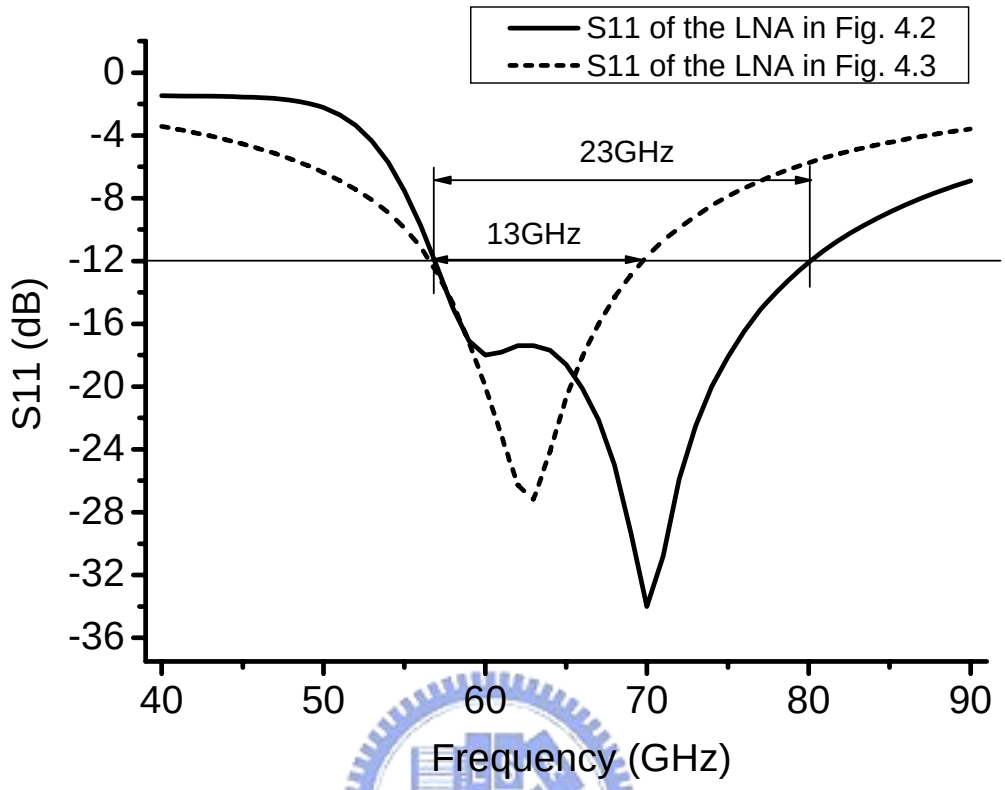


Fig. 4.5 The simulated *S11*.

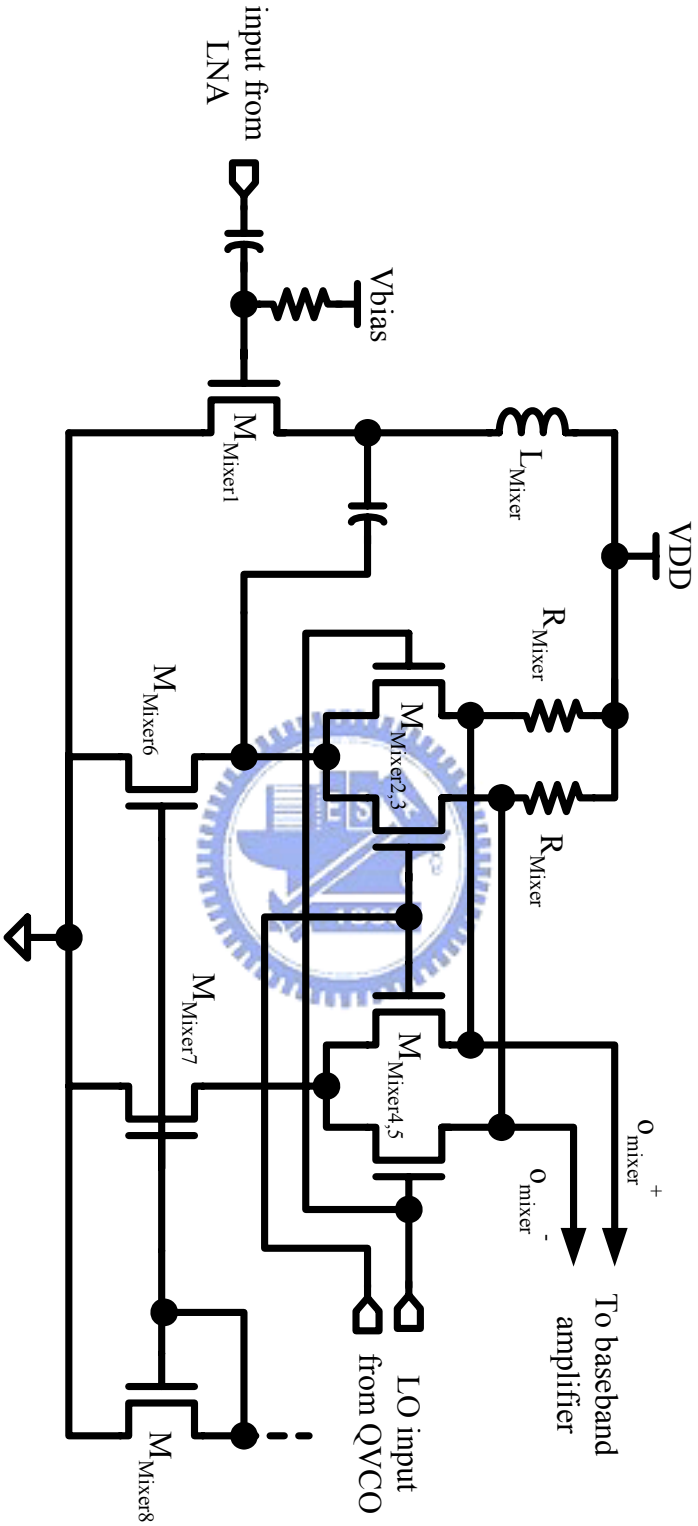


Fig. 4.6 Circuit schematic of the proposed third-order sub-harmonic mixer.

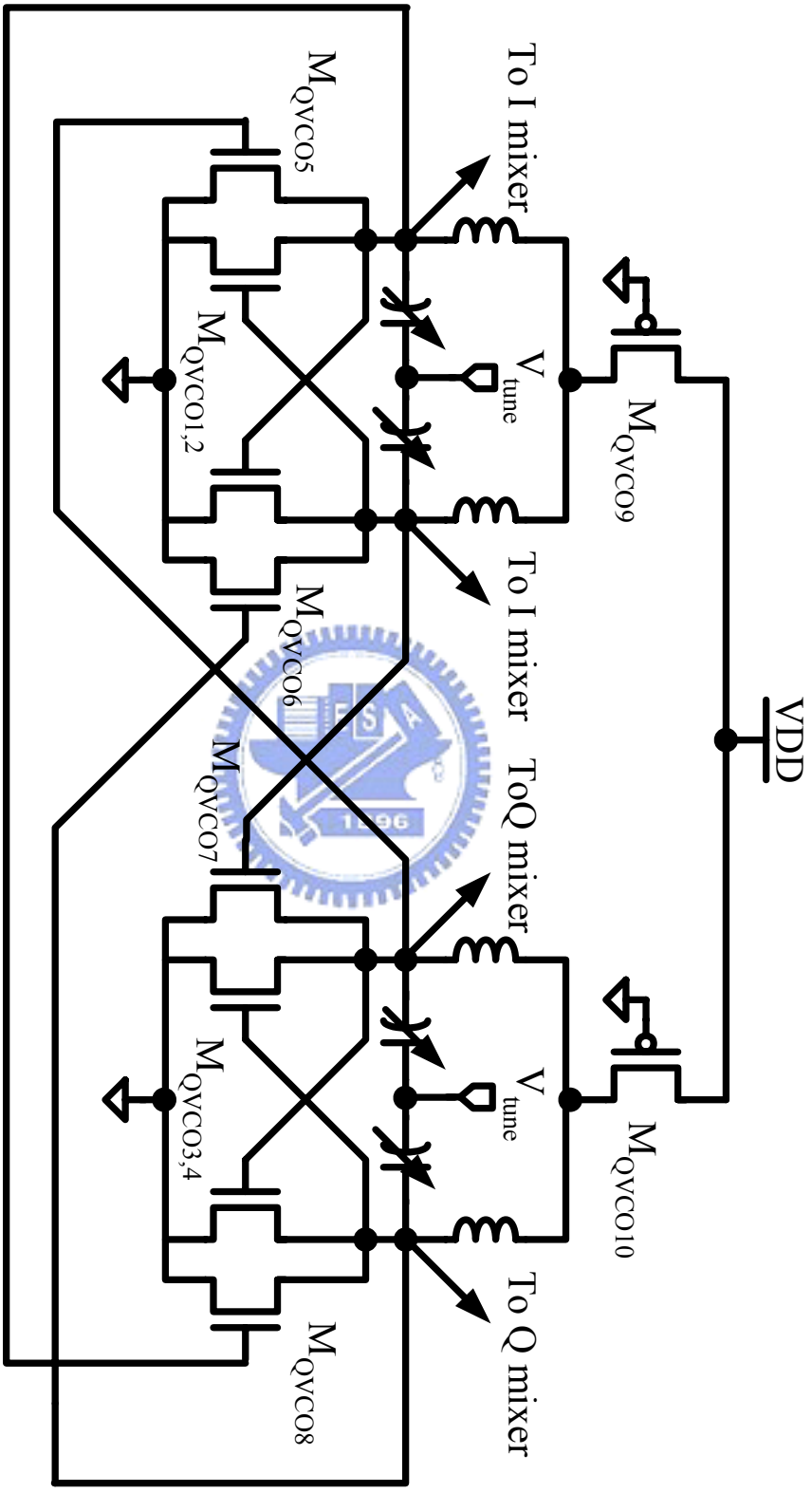


Fig. 4.7 Circuit schematic of the QVCO.

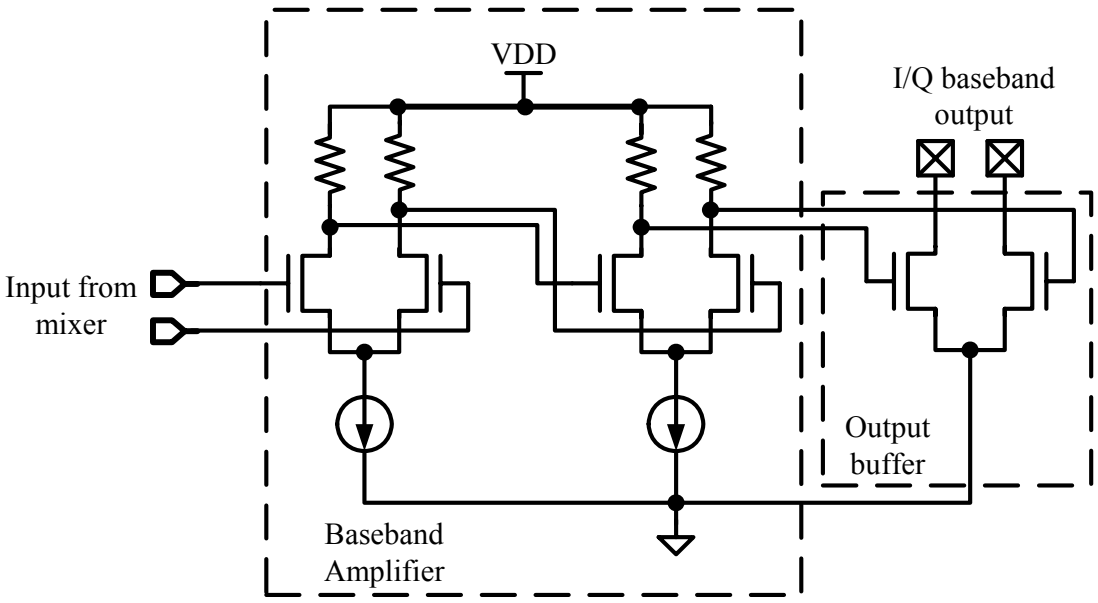


Fig. 4.8 Circuit schematic of the baseband amplifier and output buffer.

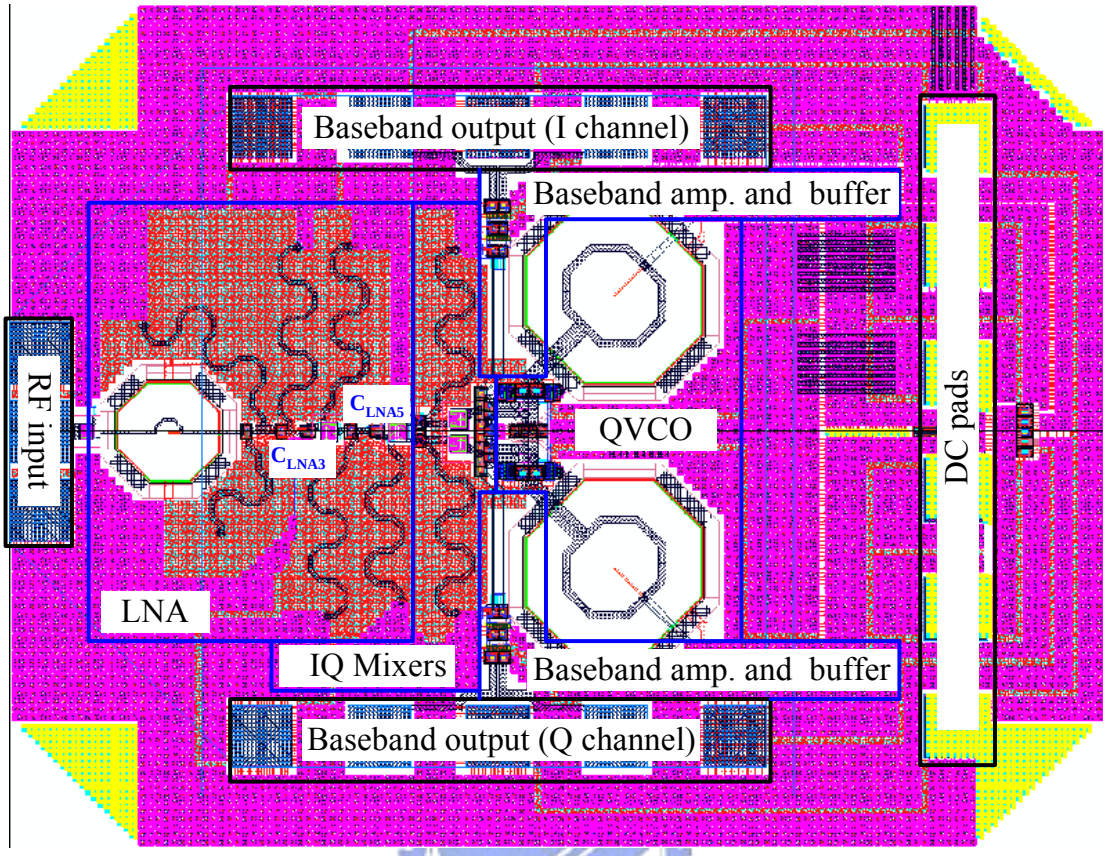
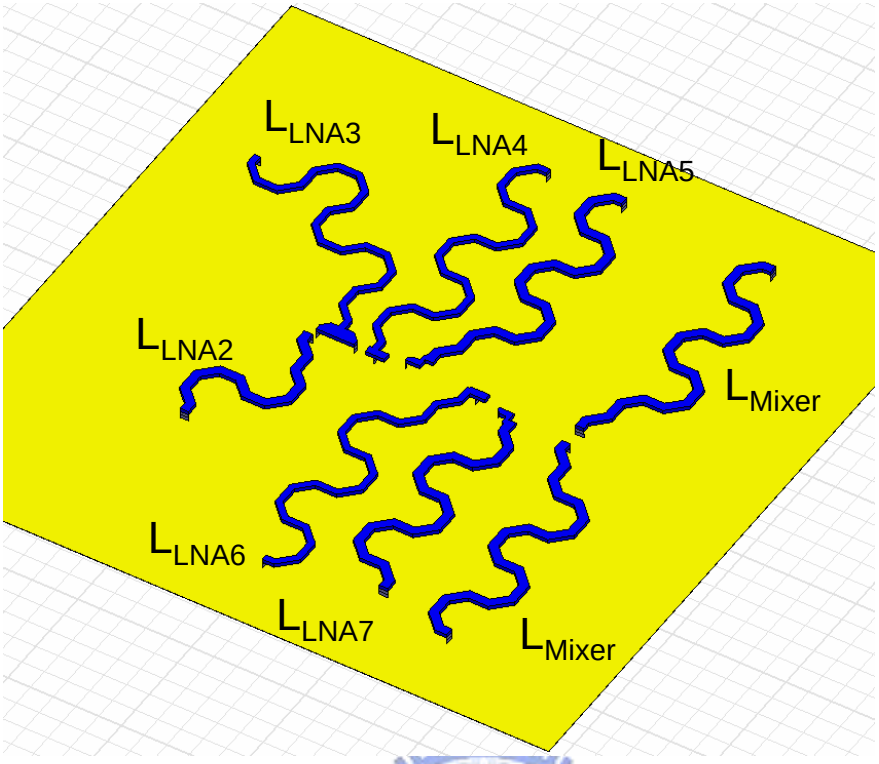
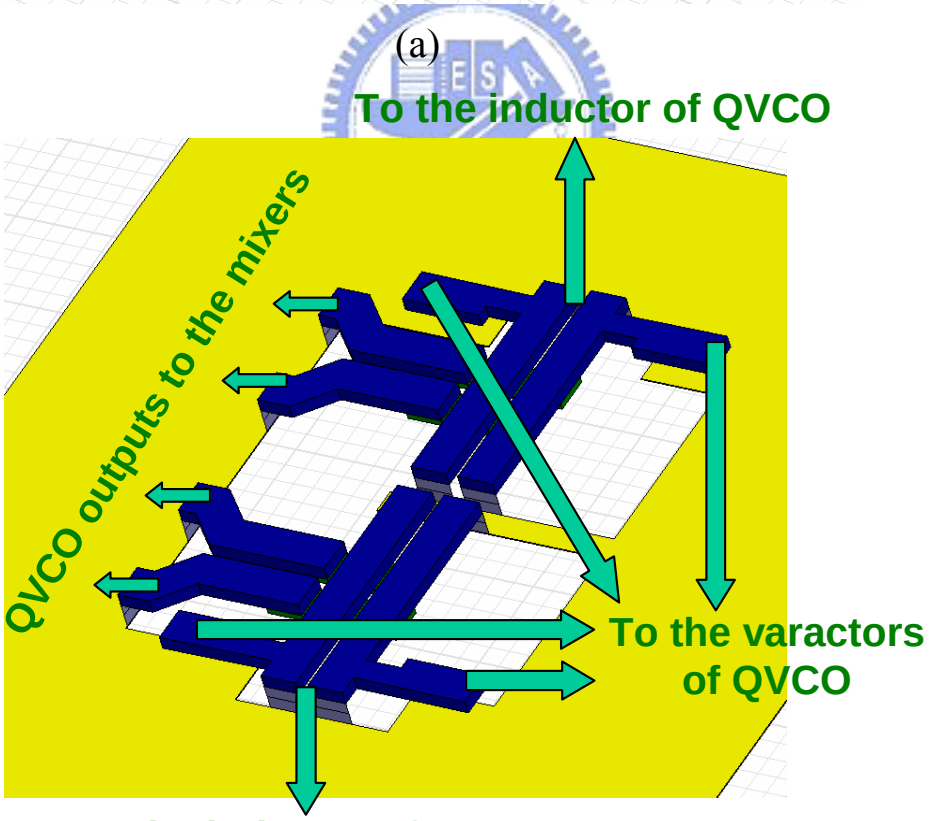


Fig. 4.9 Circuit layout of the receiver.



(a)



(b)

Fig. 4.10 Interconnections on the (a) RF (b) LO signal path for EM simulation.

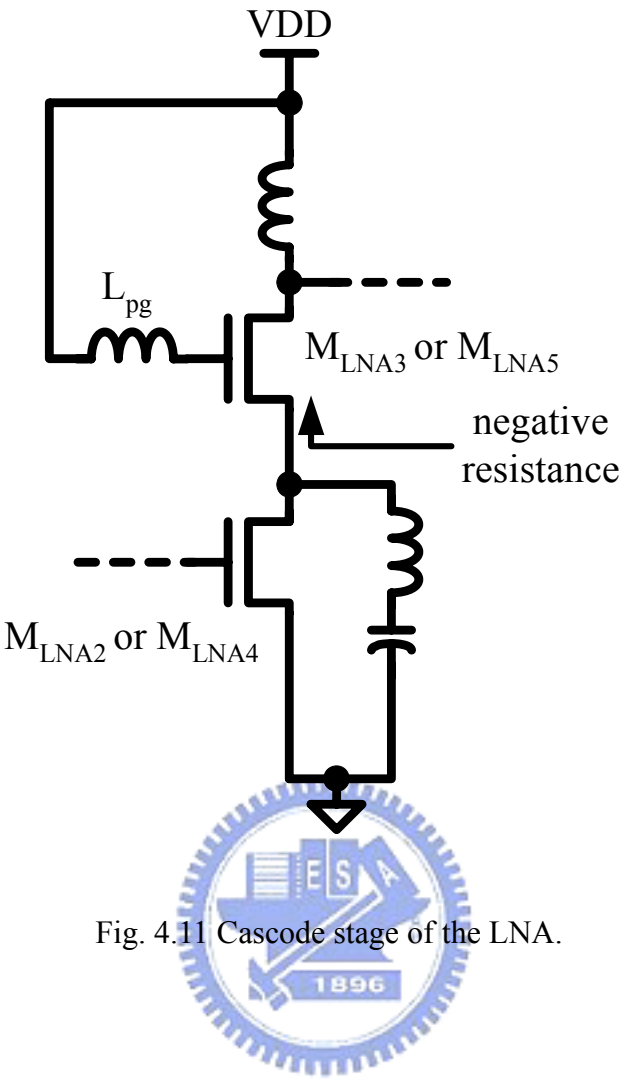


Fig. 4.11 Cascode stage of the LNA.

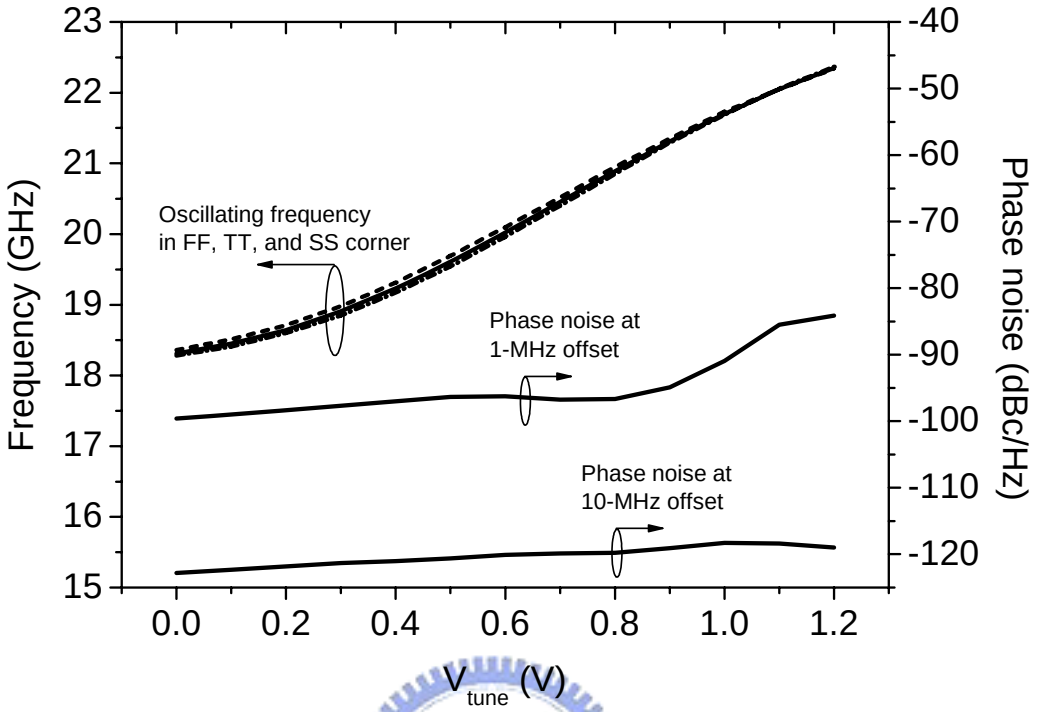


Fig. 4.12 Simulation frequency tuning ranges and phase noises of the integrated QVCO.

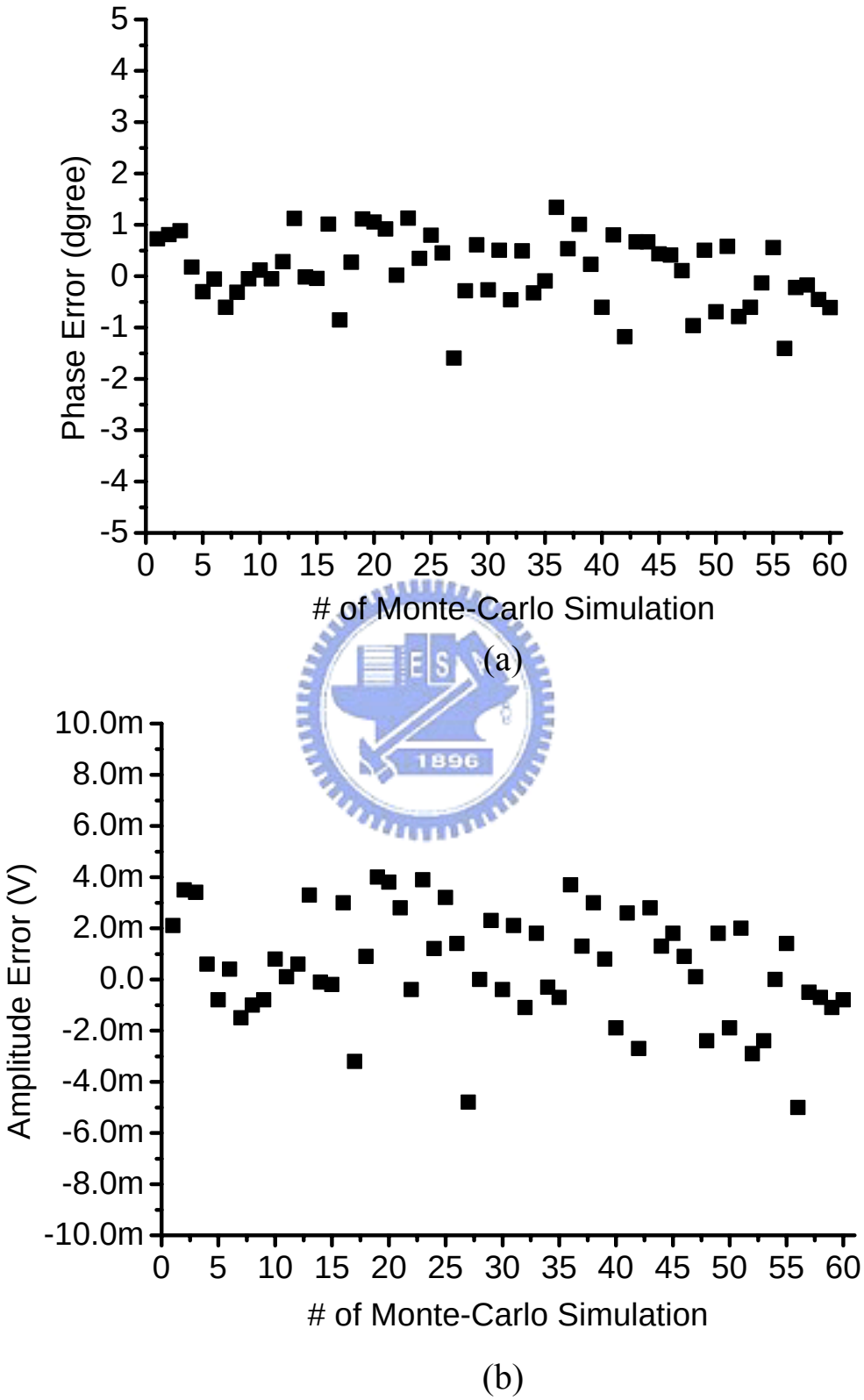


Fig. 4.13 Monte-Carlo simulation results of (a) phase (b) amplitude errors.

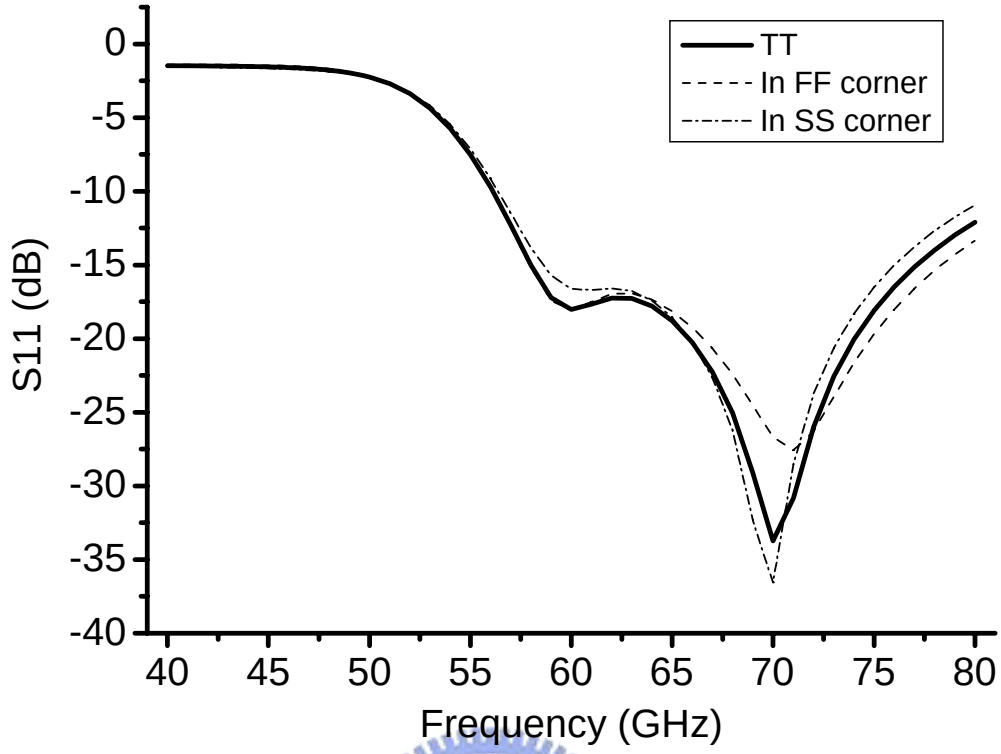


Fig. 4.14 Simulation results of S11.

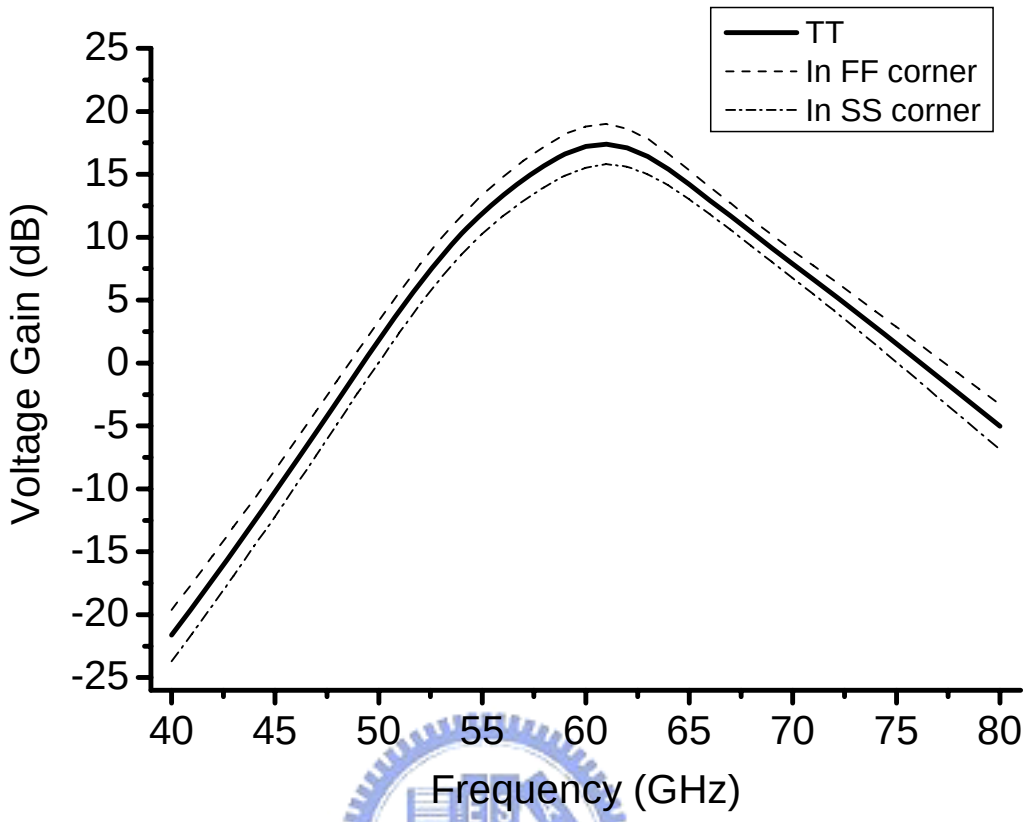


Fig. 4.15 Simulation results of LNA voltage gains.

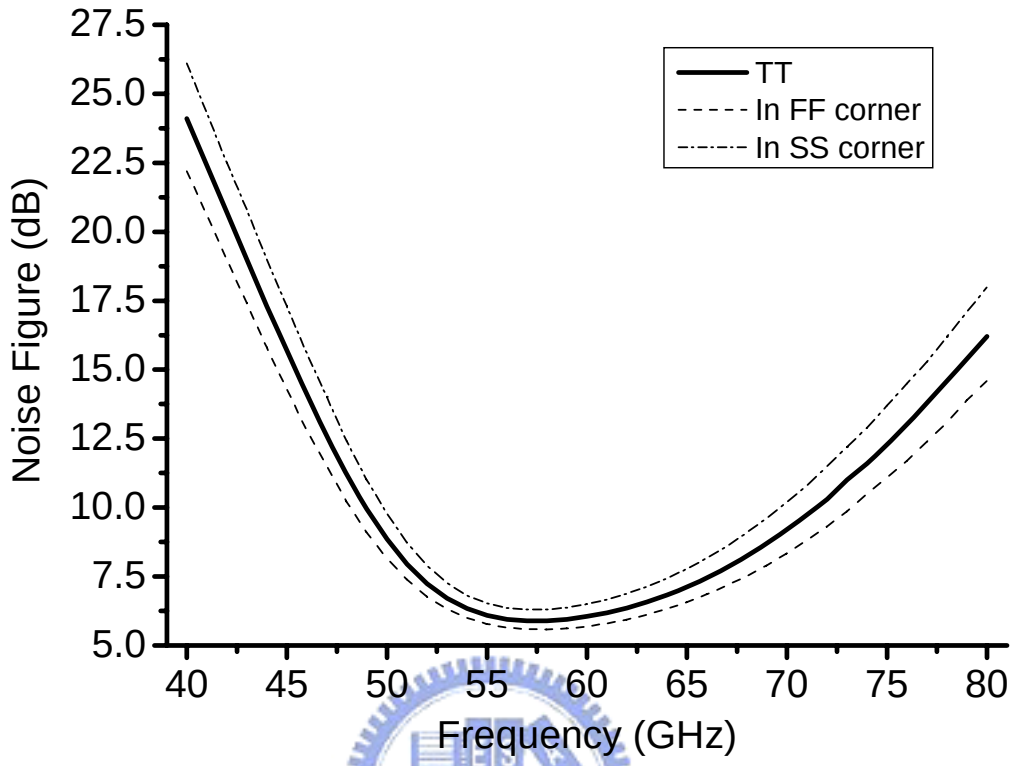


Fig. 4.16 Simulation results of LNA noise figures.

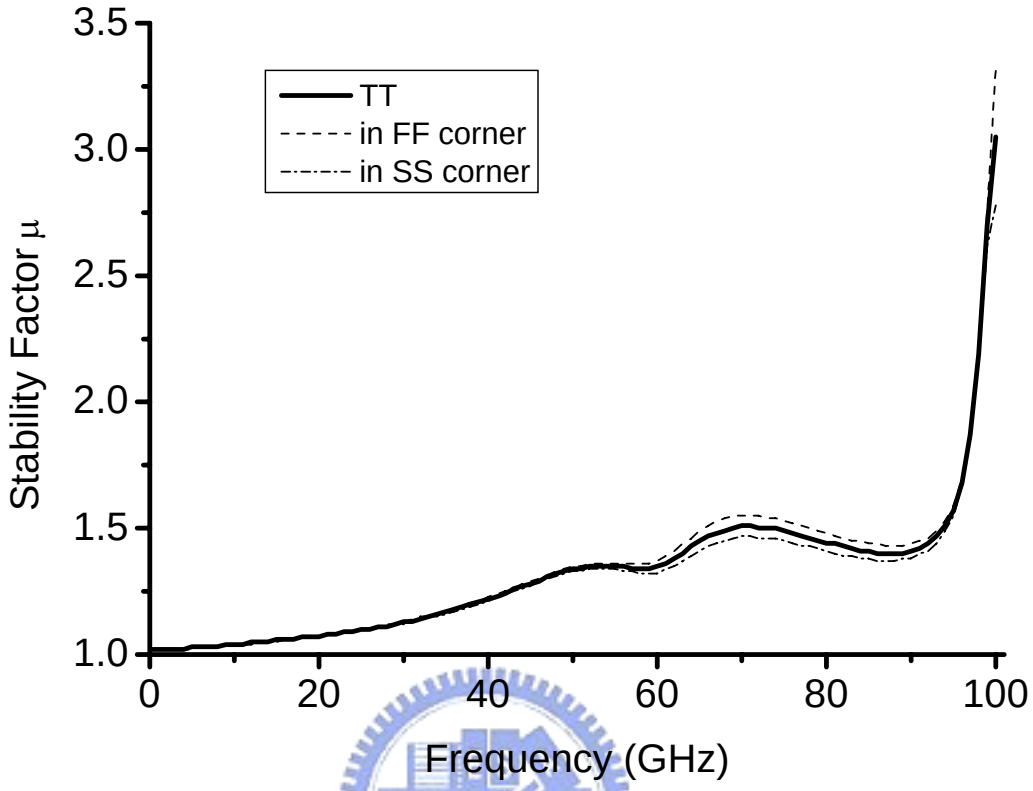


Fig. 4.17 Simulation results of stability factor μ.

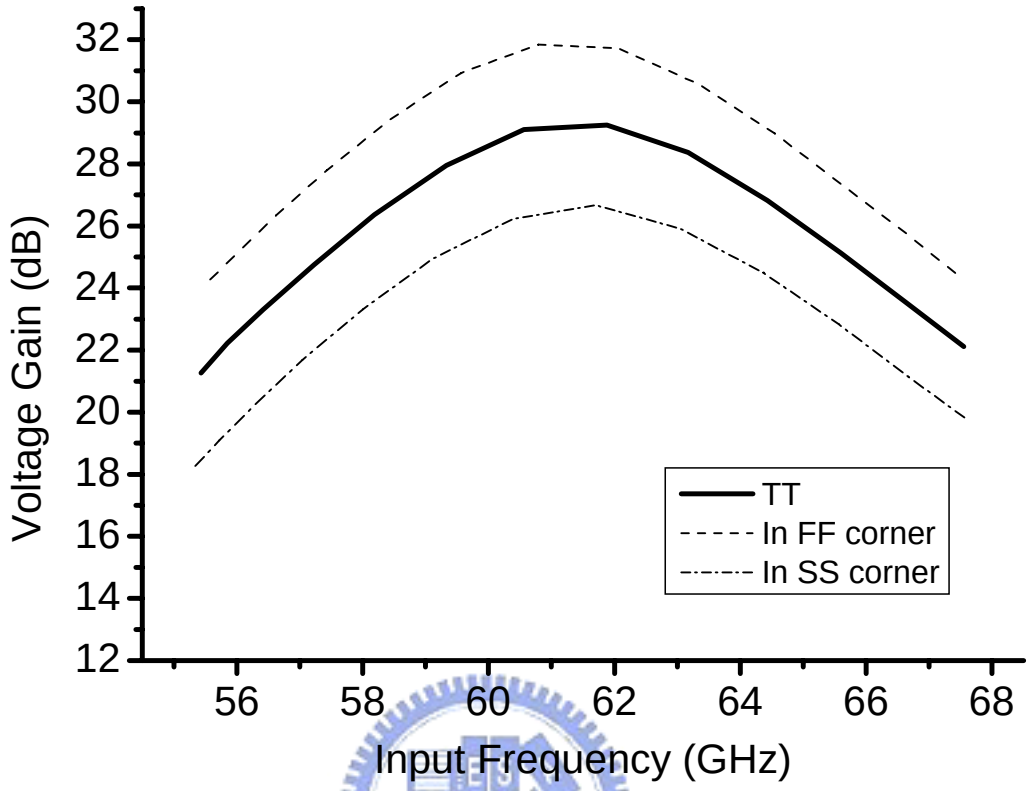


Fig. 4.18 Simulation results of receiver voltage gains.

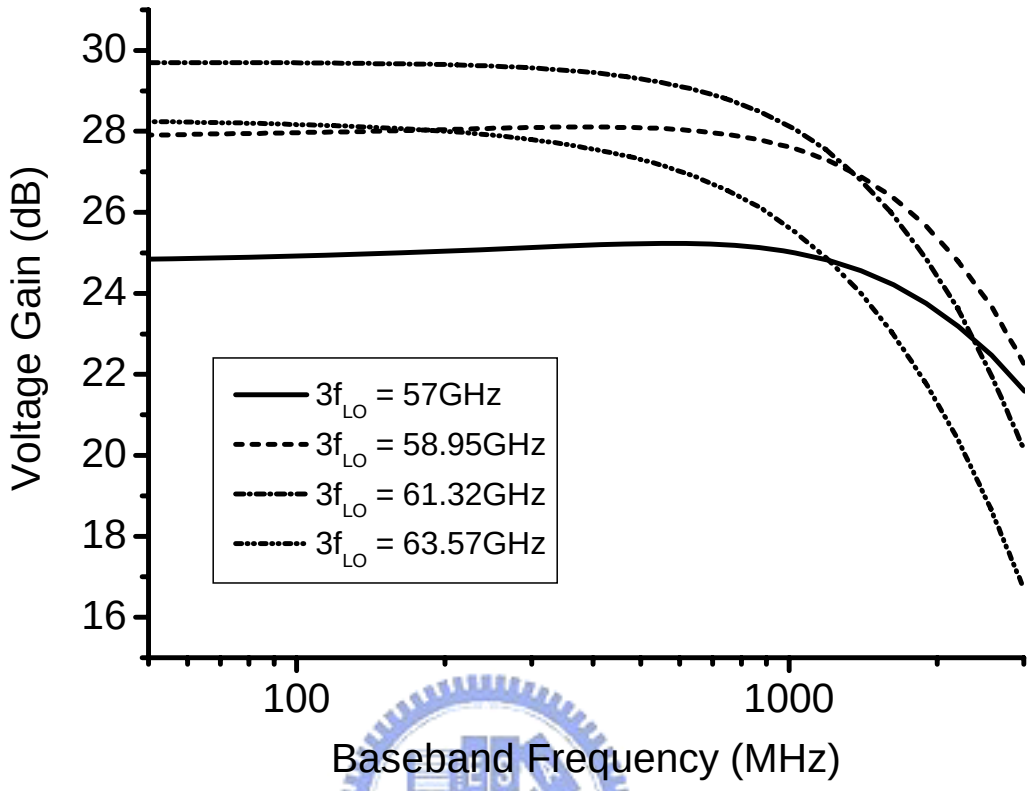


Fig. 4.19 Simulation baseband frequency responses with different LO frequencies.

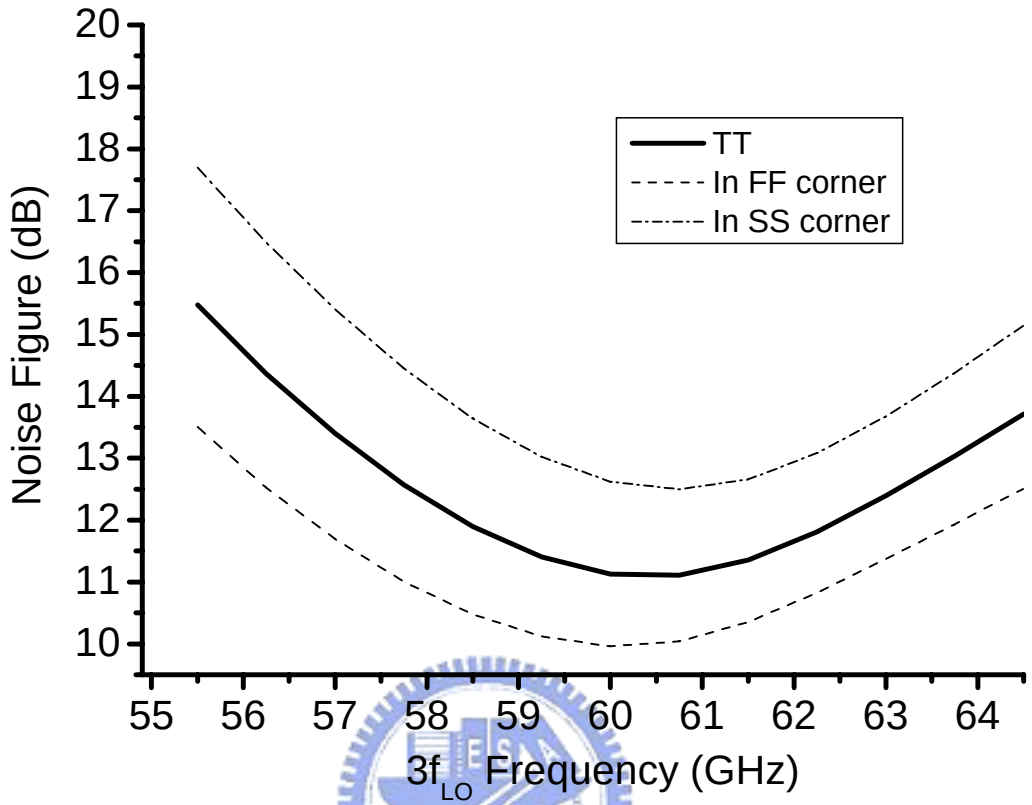


Fig. 4.20 Simulation receiver noise figures.

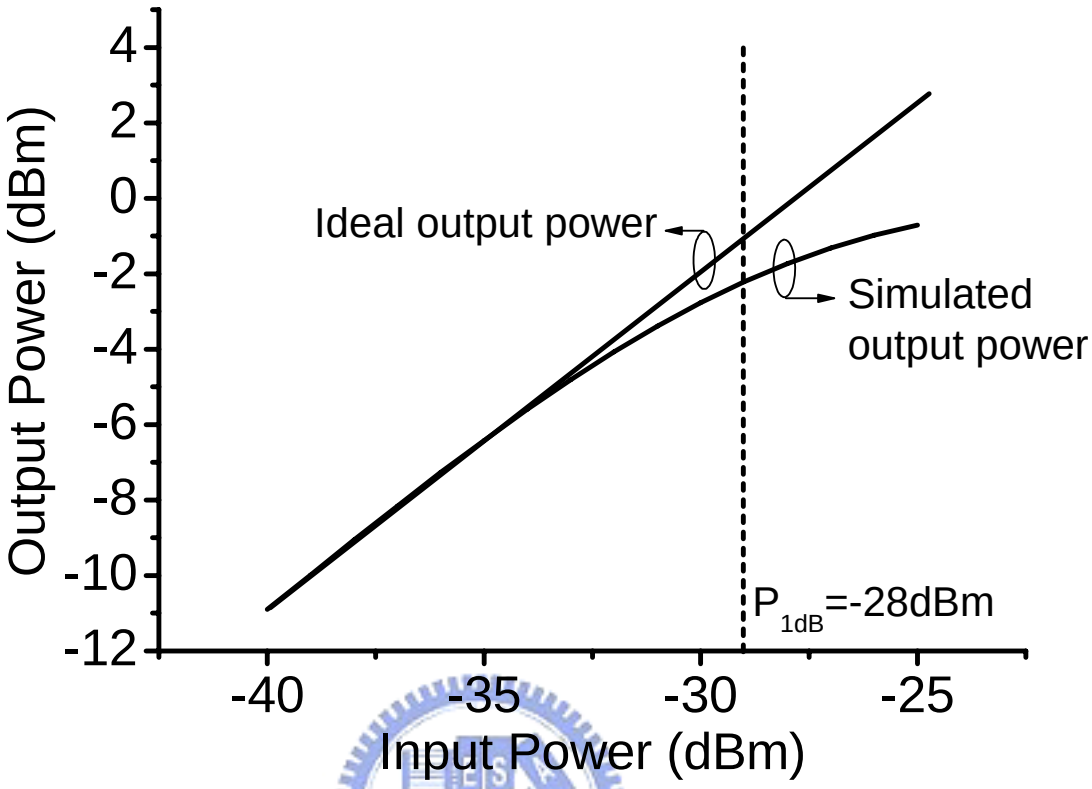


Fig. 4.21 Simulation input P_{1dB}.

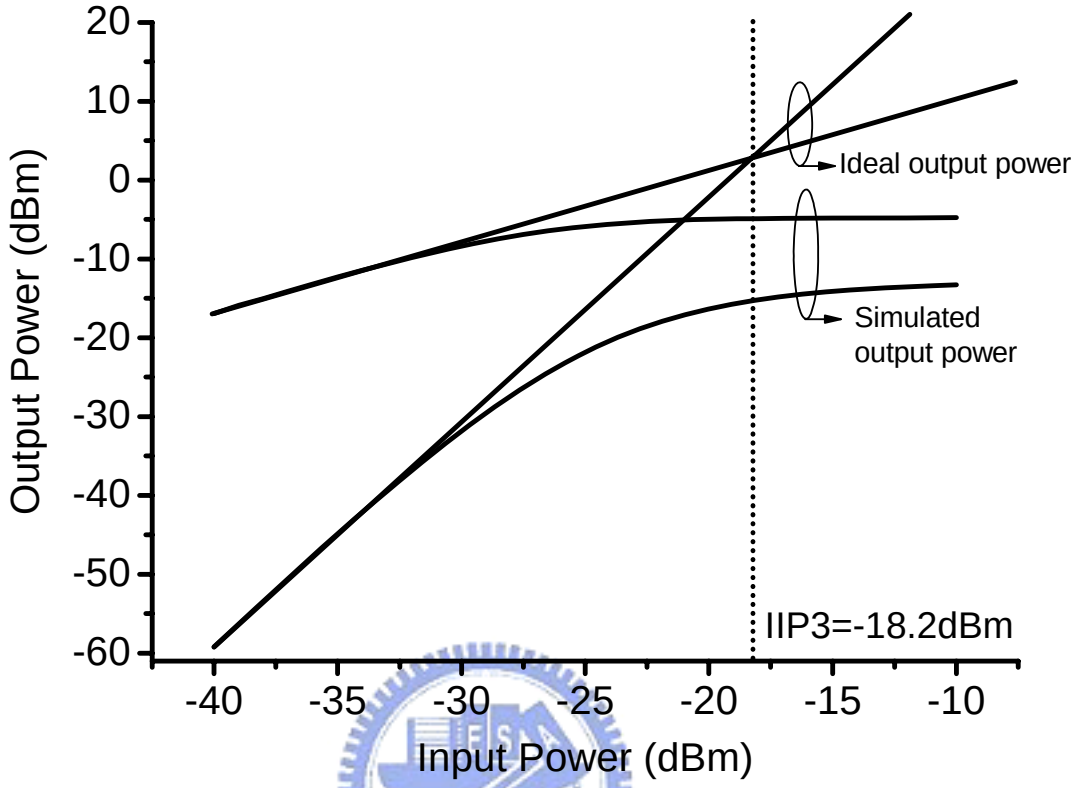


Fig. 4.22 Simulation IIP3.

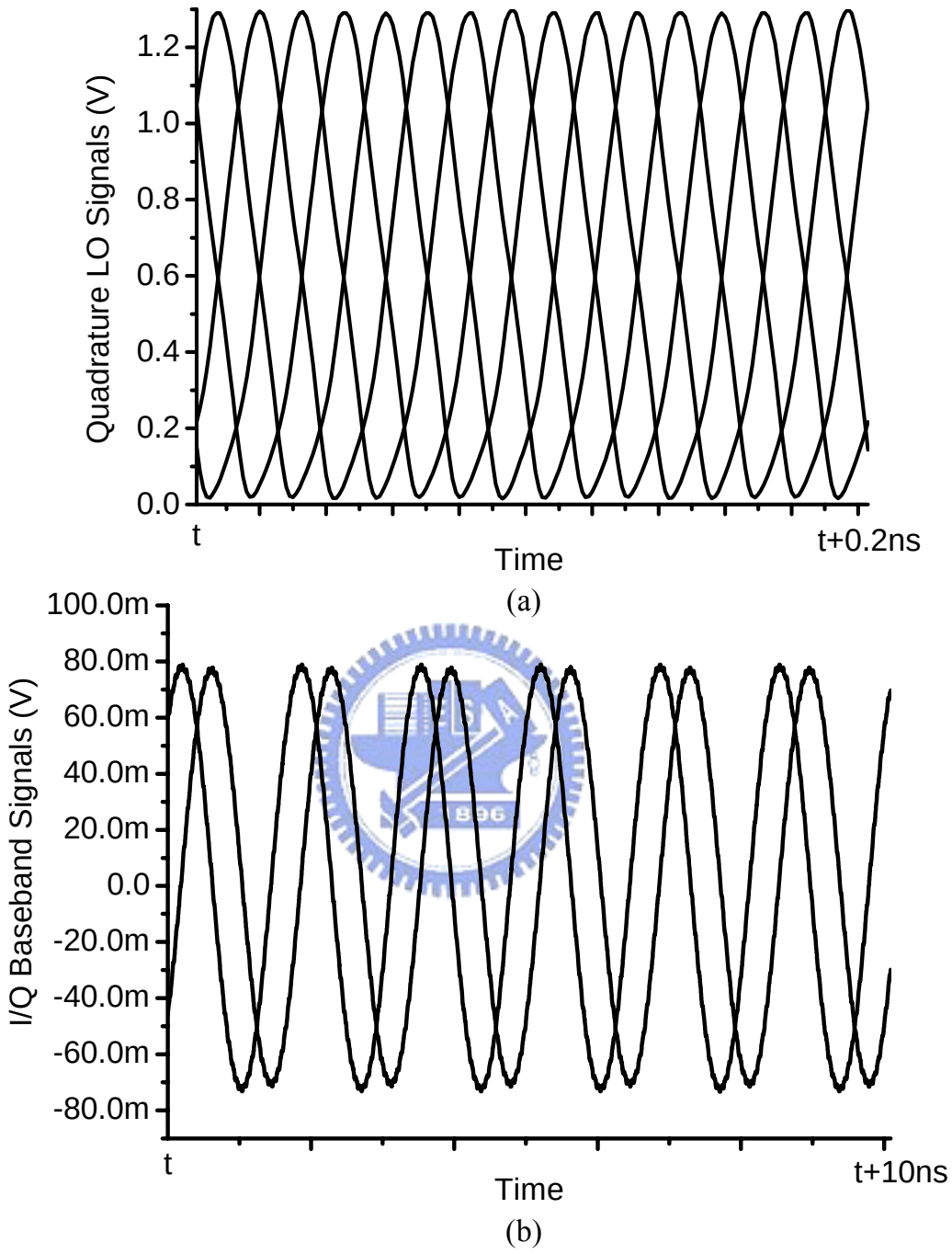


Fig. 4.23 Waveforms of (a) LO (b) baseband output signals.

CHAPTER 5

MILLIMETER-WAVE AND RF VOLTAGE-CONTROLLED OSCILLATORS USING VARIABLE INDUCTORS

5.1 MMW VCO

5.1.1 VARIABLE INDUCTOR

Fig. 5.1(a) illustrates the schematic of the proposed variable inductor (VID), which consists of a transformer T_1 and a variable resistor R_v. L_1 and L_2 represent the self inductance of the primary and secondary coils of T_1, respectively. k is the coupling factor of the primary and secondary coils and C_v is the parasitic capacitor at the secondary coil. The VID can be modeled by a variable inductor L_{eq} in parallel with a variable resistor R_{eq} as shown in Fig. 5.1(b). Both L_{eq} and R_{eq} are functions of R_v and the radian frequency ω. It can be derived that

$$L_{eq}(R_v,\omega)=\frac{R_v^2L_1\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]^2+\omega^2L_1L_2^2\left(1-k^2\right)^2}{R_v^2\left(1-\omega^2C_vL_2\right)\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]+\omega^2L_2^2\left(1-k^2\right)} \tag{5.1}$$

and

$$R_{eq}(R_v,\omega)=\frac{R_v^2L_1\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]^2+\omega^2L_1L_2^2\left(1-k^2\right)^2}{R_vk^2L_2}. \tag{5.2}$$

If the resonant frequency of C_v and L_2 is larger than the operating frequency ω, i.e.

$\omega^2 C_v L_2 < 1$, L_{eq} is minimum when R_v is equal to 0 (i.e. $L_{eq}(0,\omega)$) and maximum when R_v is infinite (i.e. $L_{eq}(\infty,\omega)$). In this saturation, the L_{eq} monotonically increases with the increases in R_v and the inductance tuning ratio α, defined as $[L_{eq}(\infty,\omega)-L_{eq}(0,\omega)]/L_{eq}(\infty,\omega)$, can be calculated as

$$\alpha = \frac{k^2}{1-\omega^2 C_v L_2\left(1-k^2\right)}. \tag{5.3}$$

The realization of the VID is shown in Fig. 5.2(a). Here R_v is implemented by an NMOS M_v operated in triode region. Thus R_v and L_{eq} are tunable by adjusting V_{tune}. The second coil is center tapped to ground, so as to diminish DC power dissipation. In the experimental prototype, using 90-nm CMOS technology, a single-turn 1:1 transformer is adopted in the VID. Fig 5.2 (b) shows the detailed layout of the transformer. The inner radius of the primary (secondary) coil is 25 μm (37 μm); the metal width is 9 μm; and the space between the first and second coils is 3 μm. By EM simulation (using Ansoft HFSS), the self-resonant frequency of the transformer is about 194 GHz. The self inductance of the primary (secondary) coil is about 123 pH (175 pH) and the coupling factor is about 0.45. The width of M_v is 25.8 μm with the minimum length and its turn-on resistance is about 40 Ω with the parasitic capacitance of 20 fF.

The simulated L_{eq} around 60 GHz are illustrated in Fig. 5.3. When V_{tune} changes from -0.3 to 1.2 V, the L_{eq} is tunable from 142 to 103 pH, and the quality factor is changed from 11.35 to 3.6. The frequency response curve of the quality factor has a U shape, which reveals that the VID has a better quality factor in the extreme cases when M_v is nearly fully turned on or off. In either case the magnetic energy dissipated in the passive R_{eq} can be minimized.

5.1.2 MULTI-BAND OPERATION

The proposed VID can be modified to achieve multi-band operation. Here M_v in Fig. 5.2(a) is decomposed into several smaller devices M_{v1} … M_{vn} in parallel, as is shown in Fig. 5.4. Each smaller device is separately controlled by voltages V_{b1} … V_{bn}. As the device size of M_v is equal to those of M_{v1} … M_{vn} in total, the parasitic capacitance at node X in Fig. 4 is almost the same as that in Fig. 5.2(a). Thus multi-band operation can be achieved without severely decreasing the oscillating frequency. This is a significant advantage in contrast to conventional capacitor-bank structure, where the parasitic capacitance in general limited the oscillating frequency and tuning range. Moreover, due to the absence of capacitors in the proposed multi-band tuning strategy, the area occupation of the tuning circuit is also much smaller than that of the conventional capacitor bank.

5.1.3 CIRCUIT DESIGN

By using the proposed VID, a 60-GHz multi-band varactorless VCO is designed and fabricated in a 90-nm CMOS technology. The circuit schematic is shown in Fig. 5.5, where the transformer T_1 is implemented by the single-turn 1:1 transformer as shown in Fig. 5.2(b). The primary coil is center tapped by metal 8 to VDD as a DC current path while secondary coil is center tapped to ground by metal 9. In this experimental prototype, the variable resistor consists of six binary-weighted NMOSFETs (M_{c1}-M_{c6}) controlled by digital codes (V_{b1}-V_{b6}) for band switching, and an NMOS M_f controlled by V_{fine} for fine frequency tuning. It should be noted that more digitally controlled NMOSFETs results in smaller maximum VCO gain. In order to reduce the capacitance at the oscillating nodes, an NMOS cross-coupled pair formed by M_1 and M_2 is used in the VCO. M_3 is an output buffer to drive the 50-Ω

load form the measurement equipment. M_4 is a dummy buffer to balance the parasitic capacitance from M_3 at the oscillating node.

Incorporating with the VID model shown in Fig. 5.1(b), the equivalent small-signal model of the VCO is shown in Fig. 5.6. C_t in Fig. 5.6 represents the total capacitance at the resonator, including the parasitic capacitances of the cross-coupled pair M_1/M_2, the output buffer M_3/M_4, and the parasitic capacitance of the transformer T_1. R_{eq} is the equivalent resistance looking into the primary coil of the VID as derived in (5.2). The negative resistance provided by the cross-coupled pair M_1 and M_2 is denoted as $-R_{neg}$ which is approximately equal to $-2/g_m$, where g_m is the small-signal transconductance of M_1/M_2. R_{neg} must be smaller than R_{eq} to guarantee oscillation start-up. In this design, R_{neg} is chosen to be smaller than $R_{eq}/2.5$ within the entire frequency range. From Fig. 5.6 and (5.1), the radian oscillating frequency is the solution of ω of the following equation,

$$\omega = \frac{1}{\sqrt{C_t L_{eq}(R_v, \omega)}} = \sqrt{\frac{R_v^2\left(1-\omega^2 C_v L_2\right)\left[1-\omega^2 C_v L_2\left(1-k^2\right)\right]+\omega^2 L_2^2\left(1-k^2\right)}{C_t R_v^2 L_1\left[1-\omega^2 C_v L_2\left(1-k^2\right)\right]^2+\omega^2 C_t L_1 L_2^2\left(1-k^2\right)^2}}. \quad (5.4)$$

However, the boundary of the VCO frequency tuning range can be found easily without solving such complex equation. As mentioned in sub-Section 5.1.1, when the radian resonant frequency of C_v and L_2, denoted by ω_2, is larger than the radian oscillation frequency (i.e. $\omega_2 > \omega$), the minimum L_{eq} is $L_{eq}(0,\omega)$ which can be written as

$$L_{eq}(0,\omega) = L_1\left(1-k^2\right), \quad (5.5)$$

and the maximum L_{eq} is $L_{eq}(\infty,\omega)$ which can be written as

$$L_{eq}(\infty,\omega)=L_1\left(1+\frac{\omega^2/\omega_2^2}{1-\omega^2/\omega_2^2}k^2\right)>L_1\,. \tag{5.6}$$

Using (5.5) and (5.6), the maximum and minimum radian oscillation frequencies, ω_{max} and ω_{min}, can be calculated as

$$\omega_{\max}=\frac{1}{\sqrt{C_t L_{eq}(0,\omega_{\max})}}=\frac{1}{\sqrt{C_t L_1(1-k^2)}}, \tag{5.7}$$

and

$$\omega_{\min}=\frac{1}{\sqrt{C_t L_{eq}(\infty,\omega_{\min})}}<\frac{1}{\sqrt{C_t L_1}}, \tag{5.8}$$

respectively. Based on (5.7) and (5.8), the lower bound of the frequency tuning range β of the VCO can be derived as

$$\beta\equiv\frac{2(\omega_{\max}-\omega_{\min})}{\omega_{\max}+\omega_{\min}}>\frac{2\left(1-\sqrt{1-k^2}\right)}{1+\sqrt{1-k^2}}\approx\frac{k^2}{2}, \tag{5.9}$$

which is determined by only one parameter, the coupling factor k of the transformer. Therefore, for a given transformer to implement the VID, the minimum frequency tuning range of the VCO using the VID can be quickly estimated even before the VCO circuit design. In this design, the simulated resonant frequency of C_v and L_2 is over 85 GHz which is larger than the target oscillation frequency, i.e. 60 GHz. With the coupling factor around 0.45, the minimum frequency tuning range of the VCO is

about 10.125%. Therefore, such VCO can be integrated in fundamental front-end system for low-noise and high-linearity MMW broadband applications. Moreover, if the VCO is used in a sub-harmonic front-end system for broadband applications, the operating frequency can be boosted higher than using a conventional VCO.

To integrate with other circuit using 1-V supply voltage, a PMOS current source M_p can be used to raise VDD to 1V with the same DC current as shown in Fig. 5.7(a). Fig. 5.7(b) shows the simulation results in this situation. It can be observed that such current source can be used without degrading the frequency tuning range and the phase noise.

5.2 RF VCO

5.2.1 INVERSION-MODE VARACTOR

Fig. 5.8 shows circuit schematic of the I-MOS varactor using in the RF VCO for frequency tuning. A large poly resistor R_{bulk} connects the NMOS bulk and ac ground V_{bulk}. When the terminal *DS* in Fig. 5.8 is biased at the positive end voltage, the I-MOS is operated in the depletion mode and Fig. 5.9 (a) shows the equivalent model. The parasitic capacitance $C_{parasitic}$ is dominated by the gate-to-source and gate-to-drain overlap capacitance; C_{ox} is the gate-oxide capacitance; and C_d is the depletion capacitance. The conductance looking into terminal *G* in Fig. 5.8, G_{dep}, can be calculated as

$$G_{dep} = \frac{j\omega(C_{ox} \parallel C_d)G_{bulk}}{j\omega(C_{ox} \parallel C_d) + G_{bulk}} + j\omega C_{parasitic}, \quad (5.10)$$

where ω is the radian frequency and G_{bulk} is the inverse of the resistance of R_{bulk}. If

G_{bulk} is much smaller than $\omega(C_{ox}||C_d)$ and $\omega C_{parasitic}$ within the entire frequency tuning range, G_{dep} is approximately equal to $j\omega C_{parasitic}$ and the minimum capacitance C_{min} can be estimated by $C_{parasitic}$. However, if the NMOS bulk is connected directly to the ac ground (i.e. case of infinite G_s), C_{min} will become $C_{parasitic}+C_{ox}||C_d$. Thus, C_{min} can be decreased by $C_{ox}||C_d$ by using a large resistance R_{bulk} in Fig. 5.8. When *DS* is biased at the negative end, a sheet of electrons accumulates at the surface of the channel and the IMOS is operated in the inversion mode. Fig. 5.9 (b) shows the equivalent model. R_{ch} is the channel resistance, which can be estimated by following equation [86],

$$R_{ch} \approx \frac{L}{k_n W V_{ov}}, \tag{5.11}$$

where W (L) are the width (length) of the NMOS in Fig. 5.8, k_n (V_{ov}) is its gain factor (overdrive voltage). To simplify, assuming R_{bulk} goes to infinite, the conductance looking into terminal G, G_{inv}, in Fig. 5.9(b) is

$$G_{inv} = \frac{12 j\omega C_{ox} G_{ch}}{j\omega C_{ox} + 12 G_{ch}} + j\omega C_{parasitic}, \tag{5.12}$$

where G_{ch} is the inverse of the resistance of R_{ch}. Calculating from (2), $12G_{ch}/\omega C_{ox}$ is larger than 20 at the carrier frequency from 4 to 6 GHz when L is 0.36 μm. Thus, the imaginary part of G_{inv} is approximately equal to $\omega(C_{ox}+C_{parasitic})$ and the maximum capacitance C_{max} can be estimated by $C_{ox}+C_{parasitic}$.

Using 0.18-μm CMOS technology, the HSPICE simulated C-V characteristics of an I-MOS varactor are shown in Fig. 5.10. The resistance of R_{bulk} is 10k in this simulation. The voltage of terminal G in Fig. 5.8 is set to a fixed voltage, 0.8 V, and the voltage of *DS* is swept from 0 to 0.8 V. The improvement of the C_{max}/C_{min} ratio

using the modified I-MOS varactor of Fig. 5.8(a) is close to 25%. It should be noted that the center voltage V_c in Fig. 5.10 can be right-shifted by increasing the bulk biased voltage, V_{bulk} in Fig. 5.8. In the simulation, V_{bulk} is 0.4V.

5.2.2 MULTI-BAND OPERATION

A large varactor sensitivity k_v [87] degrades of phase noise performance. The effect of k_v on phase noise can be shown by the following equation [87],

$$L(\Delta f, k_v) = 10\log\left\{\left(\frac{f_o}{2Q\Delta f}\right)^2\left[\frac{FkT}{2P_o}\left(1+\frac{f_c}{\Delta f}\right)+\left(\frac{k_v v_n}{2k_{CL}\Delta f}\right)^2\right]\right\}, \qquad (5.13)$$

where f_o is the oscillating frequency, Q is the quality factor of the LC tank, Δf is the offset frequency from the carrier, F is the noise factor of the gain element, k is Boltzmann's constant, T is the flicker noise corner frequency, and k_{CL} is a function of C and L in the resonator. If the required tuning range is large, a bandswitching topology is suggested to reduce varactor sensitivity k_v [87]. However, Fig. 5.11 shows the C-V characteristics of an A-MOS varactor with the same size and bias condition as the I-MOS varactor simulated in Fig. 5.10.The A-MOS varactor cannot be fully switched when tuned from 0 to 0.8V. Thus, there is no benefit to implement bandswitching topology with A-MOS varactors to reduce k_v in the case of a low tuning voltage. On the other hand, from Fig. 5.10, the gradients of the I-MOS C-V curve are relatively small when the voltages at terminal DS is 0 and 0.8V. Therefore, it makes sense using I-MOS as on/off only varactors in a bandswitching topology to reduce k_v and improve phase noise performance with low tuning voltages.

5.2.3 CIRCUIT DESIGN

The VCO is designed using 0.18-μm CMOS technology. Fig. 5.12 shows the circuit schematic for the VCO. It is an LC-tank VCO with an NMOS cross-coupled pair to generate the negative resistance for oscillation. The current source I_{dc} draws 1.5mA. The bandswitching I-MOS varactor array consists of one continuous tuning varactor controlled by tuning voltage V_{c1} and two on/off only digital switching varactors controlled by V_{c2} and V_{c3}. Gate terminal (*G* in Fig. 5.8) of each IMOS connects to the oscillation ports and the drain and source terminal (*DS* in Fig. 5.8) connects to the tuning ports (V_{c1} to V_{c3} in Fig. 5.12). The equivalent C-V curve of the three varactors on each side is shown in Fig. 5.10.

Fig. 5.13 shows the detail layout and equivalent model of the spiral inductor. The spiral inductor is implanted using the thick top metal and the inner radius is 80 μm. A symmetrical architecture with center tapping is used to save chip area. ADS Momentum is used for EM simulation. The two-turn inductor provides 1.55nH of inductance, and the quality factor is from 9.5 to 11 across the entire tuning range.

5.3 EXPERIMENTAL AND SIMULATION RESULTS

5.3.1 MMW VCO

Fig. 5.14(a) shows the circuit schematic of the fabricated MMW VCO in 90-nm bulk-CMOS technology. The chip micrograph is shown in Fig. 5.14(b). However, all PMOS's and MIM capacitors are failed in the shuttle. Therefore, the debug pad which connects node Y and VDD is used in the measurement. Moreover, FIB is used to connect the output node to the output GSG pad.

The measurement setup and environment is shown in Fig. 5.15. The core size is

0.28 × 0.36 mm^2. The chip is measured on-wafer on a high-frequency probe station. With VDD = 0.7 V, the measured and simulated frequency tuning characteristics are shown in Fig. 5.16. The tuning voltages of V_{b1}-V_{b6} and V_{fine} are tied together and varied from -0.3 to 1.2 V, and the VCO frequency is changed from 52.2 to 61.32 GHz. The corresponding tuning percentage is 16.07%. If the tuning voltage range reduces to 0 to 0.7 V, the tuning percentage becomes 13.98%. The difference of the central frequency between measurement and simulation is about 1.14 GHz. After the loss from the output buffer, probes, cables, adapters, and external mixer have been deembedded, the measured single-end oscillating voltage amplitudes are also shown in Fig. 5.16, where the simulation results also are shown for comparison. From the measurement results, the oscillating voltage amplitude varies from -10.55 to -4.55 dBV within the entire frequency tuning range.

The oscillation of the VCO is started as VDD is larger than 0.37 V. The measured frequency tuning ranges for VDD from 0.4 to 0.9 V are shown in Fig. 5.17. When VDD = 0.5 V, the VCO has the maximum frequency tuning range from 53.21 to 62.78 GHz (i.e. 16.5% at 58 GHz).

Multi-band operation is achieved by digitally controlling V_{b1}-V_{b6} and fine-tuning V_{fine}. By the mixed-mode frequency tuning scheme, the VCO manifests 64 frequency bands. The measured frequency tuning ranges of these 64 bands are shown in Fig. 5.18, where the bands are numbered from 1 to 64 according to the digitally controlling voltages of the binary-weight MOS's. The K_{VCO} of each band can be calculated using the measured data and is drawn in Fig. 5.19. The maximum K_{VCO} is 720 MHz/V at band 8 which is more than 10 times less than that in single-band operation. If more digitally controlled NMOSFETs are used, the maximum K_{VCO} can be reduced further.

In the case of multi-band operation, the measured phase noises at 10-MHz offset frequency within the entire frequency tuning range are plotted in Fig. 5.20. The phase noise ranges from -94 to -118.75 dBc/Hz within the frequency tuning range and the average phase noise is -102.44 dBc/Hz. The measured VCO output spectrums at different frequencies are also shown in Fig. 5.20. For comparison, when V_{b1}-V_{b6} and V_{fine} are tied together (i.e. single-band operation) for frequency tuning, the measured phase noises are also shown in Fig. 5.20. It can be observed that phase noise performance can be significantly improved by the multi-band operation at high-K_{VCO} region.

When VDD = 0.7 V, the measured average power consumptions of the VCO core within the frequency tuning range is 8.7 mW. The buffer stage dissipates 5.6 mW.

The performance benchmark of the proposed VCO and the prior works [15]-[19] are summarized in Table 5.1. Three different figures of merits are illustrated to investigate their advantages. They are

$$FOM = PN - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{cons}}{1mW}\right), \tag{5.14}$$

$$FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\frac{TP}{10\%}\right) + 10\log\left(\frac{P_{cons}}{1mW}\right), \tag{5.15}$$

and

$$FOM_{T/V} = PN - 20\log\left(\frac{f_o}{\Delta f}\frac{TP}{10\%}\frac{1V}{\Delta V_t}\right) + 10\log\left(\frac{P_{cons}}{1mW}\right), \tag{5.16}$$

where PN is the phase noise at the offset frequency Δf, f_o is the oscillating frequency, P_{cons} is the power consumption, TP is the frequency tuning percentage, and ΔV_t is tuning voltage range. At over 50-GHz operating frequency, the proposed VCO has the widest frequency tuning range, and is the only one with the feature of

multi-band frequency tuning. Thus, the proposed VCO can be integrated in fundamental front-end system for low noise and high linearity broadband applications. Moreover, when the VCO is used in a sub-harmonic front-end system, the operating frequency can be boosted even higher while a wide operating frequency range can be maintained.

5.3.2 RF VCO

With a 0.8-V supply voltage, Fig. 5.21 shows the tuning characteristics of the VCO when V_{c1}, V_{c2} and V_{c3} are connected together and tuned from 0 to 0.8 V. From the simulation results shown in Fig. 5.21, the frequency tuning range can be improved by 500MHz (i.e. 50%) through the large resistance R_{bulk} connected to the NMOS bulk. Multi-band operation is achieved by digitally controlling V_{c2}-V_{c3} and continuously controlling V_{c1}. As shown in Fig. 5.22, the oscillating frequency can be tuned from 4.4 to 5.9 GHz, achieving 29.12% tuning range with the center frequency at 5.15 GHz. Fig. 5.23 shows the simulated phase noise when the VCO operates at a carrier frequency 5.52GHz. It has -88.01 dBc/Hz at 100-kHz offset and -109.65 dBc/Hz at 1-MHz offset. The phase noise is simulated when V_{c1} is 0.3V and V_{c2} and V_{c3} are 0.8 V. When the supply and tuning voltage is reduced to 0.6 V, the tuning range becomes 22.64% from 4.7 to 5.9 GHz. The phase noise is 81.52 dBc/Hz at 100KHz offset and -105.24dBc/Hz at 1 MHz offset from the carrier at 5.65GHz.

Figures of merits in (5.13)-(5.16) are used in Table 5.2 for comparison with some published RF VCOs. It can be seen that the proposed VCO has good tuning capability even if the tuning voltage is lower than 1V.

5.4 SUMMARY

In this chapter, a novel variable inductor and a modified I-MOS varactor are proposed and analyzed. By using the proposed variable inductor, a VCO is designed in the MMW frequency band. Because the minimum frequency tuning range of the VCO is independent of the oscillating frequency, it has a wider tuning range than the conventional VCO using A-MOS varactors. Moreover, in comparison with conventional capacitor bank, multi-band operation can be achieved without severely decreasing the oscillating frequency and increasing the area occupation. Simulation results show that a PMOS current source can be used to raise the VDD to 1V without degrading the frequency tuning range. Moreover, if 0.13-μm CMOS technology is used, the same method can be used to raise the VDD to 1.2V to integrate with other circuit. Therefore, the VCO using the proposed tuning strategy manifests strong potential to be applied in the MMW UWB system.

On the other hand, by using the proposed I-MOS varactor, a VCO is designed around 5 GHz for low-voltage applictions. The VCO has a fine frequency tuning capability even the supply voltage is lower than 1 V. Besides conventional RF applications, it also can be used as an LO signal generator in a heterodyne receiver for MMW applications to downconvert the IF signals to the baseband.

Table 5.1 Performance Benchmark

References	[15]	[16]	[17]	[18]	[19]	This Work
CMOS process	.25μm	.12μm	.13μm	90nm	90nm	90nm
Multi-band operation	without	without	without	without	without	with
VDD/ΔV_t (V)	1.3/2.5	1/1.6	1.5/1.5	1/N.A.	0.7/1.1	0.7/1.5 *(1/1.5)
Freq. Range (GHz)	49-50.1	50.9-51.6	53.6-59.4	59.9-60	73.8-79.3	52.2-61.3 *(50.67-60.59)
Tuning Percentage	2.22%	1.37%	10.3%	0.2%	7.2%	16.07% *(17.83)
PN at Δf (dBc/Hz)	-100 at 1MHz	-85 at 1MHz	-108 at 10MHz	-100 at 1MHz	-110 at 10MHz	-102.4 *(-106.8) at 10MHz
Power (mW)	13	1	9.8	1.9	13.58	8.7 *(13.5)
FOM (dBc/Hz)	-182.8	-179.2	-173.1	-192.8	-176.3	-168.14
FOM_T (dBc/Hz)	-169.7	-161.9	-173.4	-158.8	-173.5	-172.34
$FOM_{T/V}$ (dBc/Hz)	-161.7	-157.8	-169.9	N.A.	-172.7	-168.74

* Simulation data (PMOS current source is used to raise the VDD to 1V with the same DC current)

Table 5.2 Performance Benchmark

References	[87]	[88]	*[89]	[90]	[91]	*This Work
CMOS process	.13μm SOI	.25μm	.25μm	.35μm	.35μm	.18μm
Var. type	A-MOS	A-MOS	N.A.	A-MOS	No var.	I-MOS
VDD/ΔV_t (V)	1/1.4	2.5/2.5	2/4	2/4	1.5/1.5	0.8/0.8
Freq. Range (GHz)	3.1-5.6	4.2-5.05	4.73-5.87	1.8-2.45	5.51-6.53	4.4-5.9
Tuning Percentage	58.7%	18%	21.5%	26.5%	16.8%	29.12%
PN at 1-MHz offset (dBc/Hz)	-120.8	-114	-106	-125	-98.4	-109.65
Power (mW)	2	13.8	4	2	18	1.2
FOM (dBc/Hz)	-186.6	-176.6	-174	-187.6	-161.8	-183.7
FOM_T (dBc/Hz)	-202	-181.7	-180.6	-196.1	-166.3	-193
$FOM_{T/V}$ (dBc/Hz)	-199.1	-173.7	-168.6	-184.1	-162.8	-194.9

* Simulation data

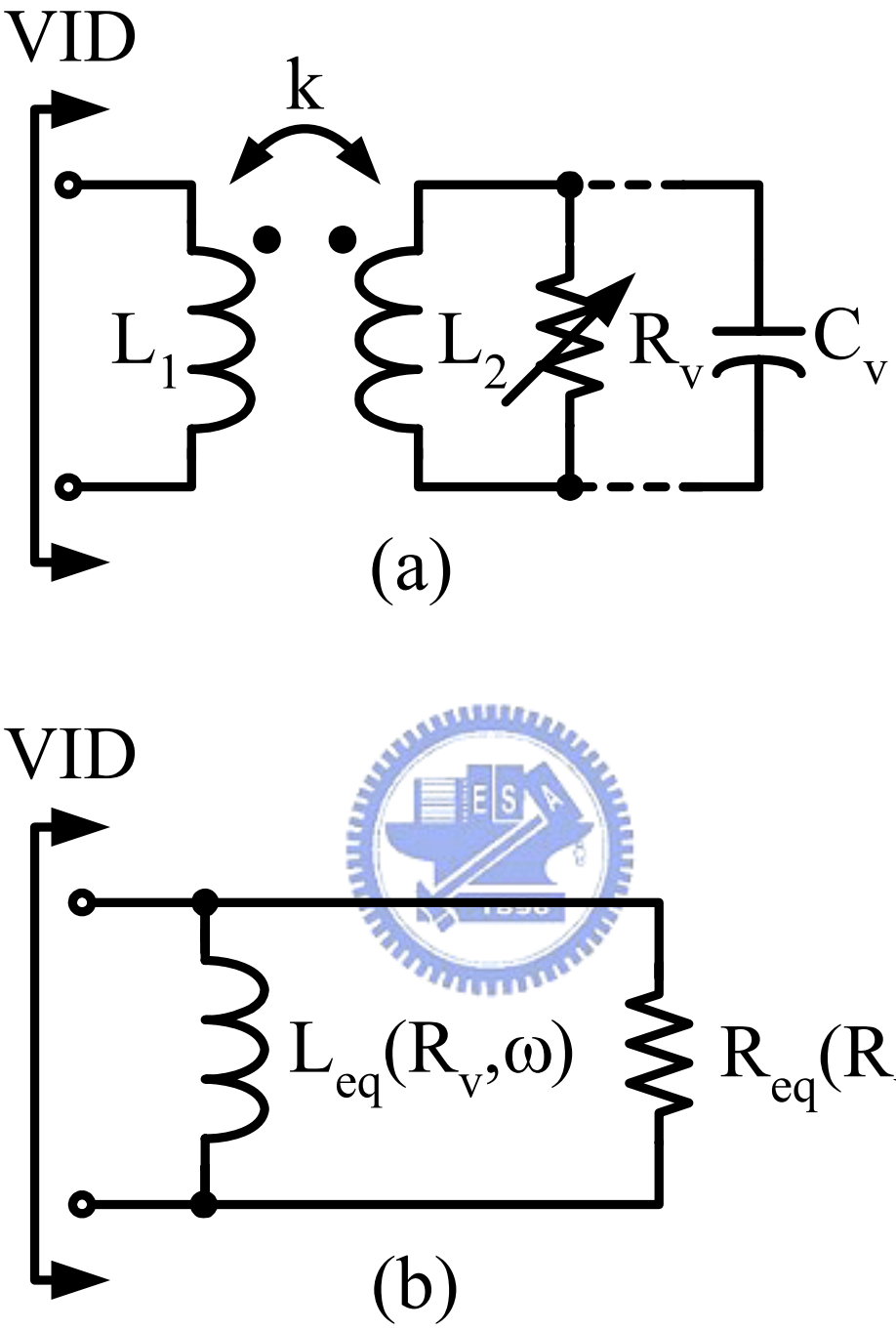


Fig. 5.1 (a) The proposed variable inductor (b) equivalent circuit model.

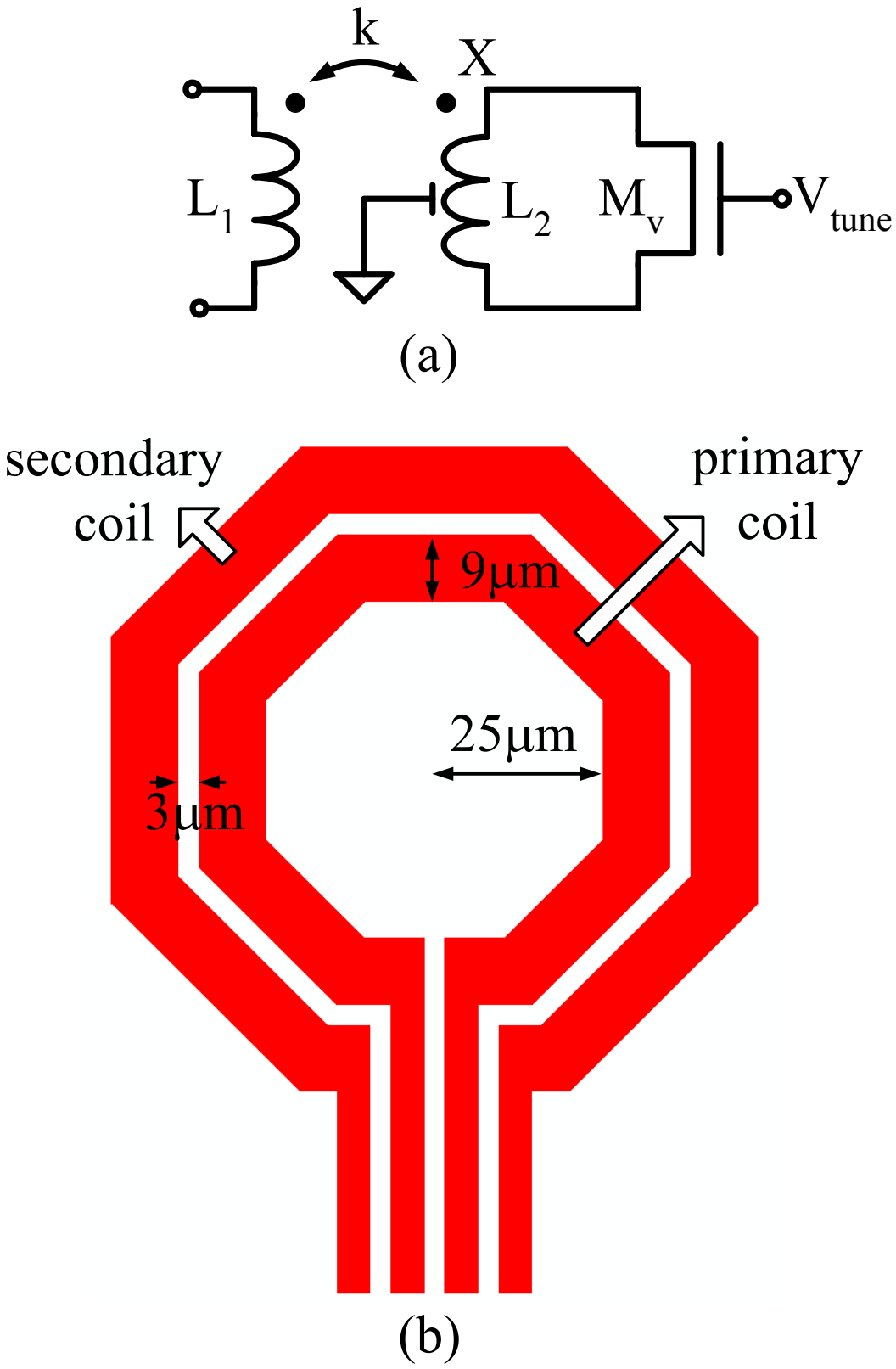


Fig. 5.2 (a) Variable inductor circuit schematic (b) 1:1 transformer layout view.

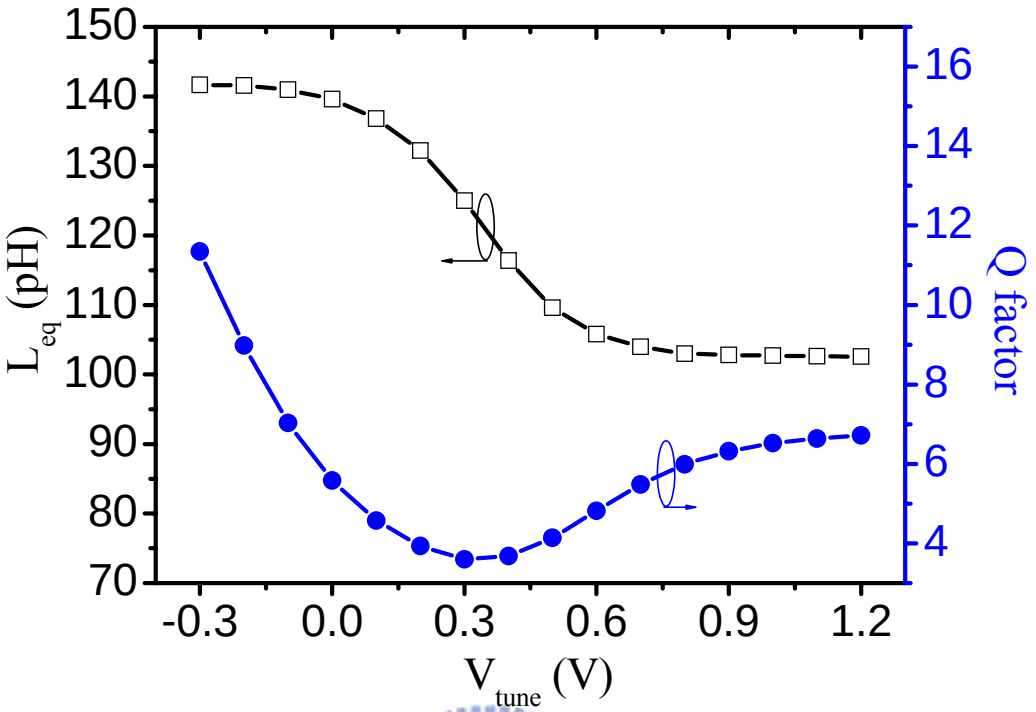


Fig. 5.3 Simulated L_{eq} and quality factor of VID.

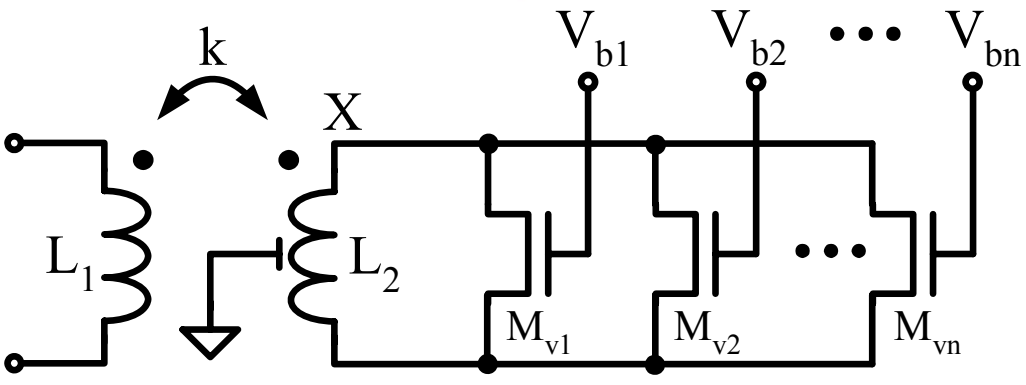


Fig. 5.4 Multi-band variable inductor.

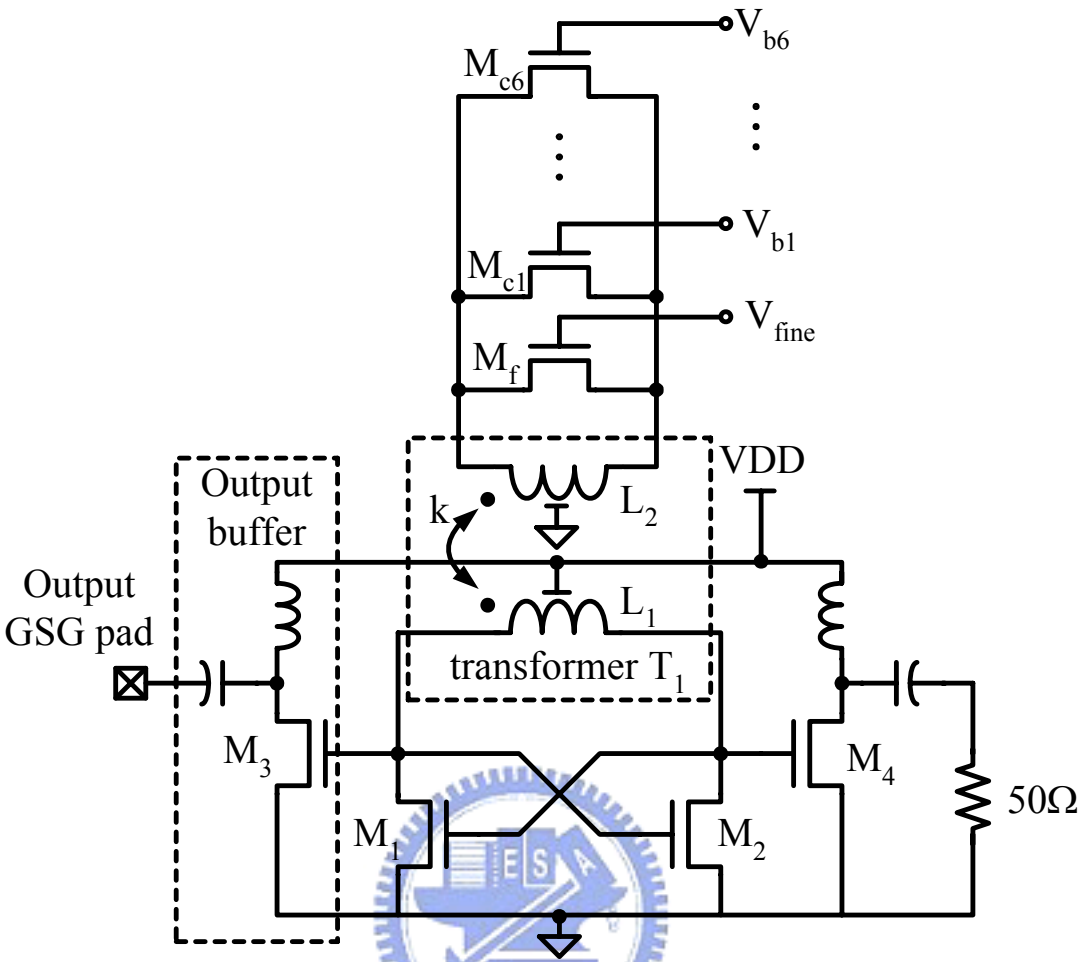


Fig. 5.5 VCO circuit schematic.

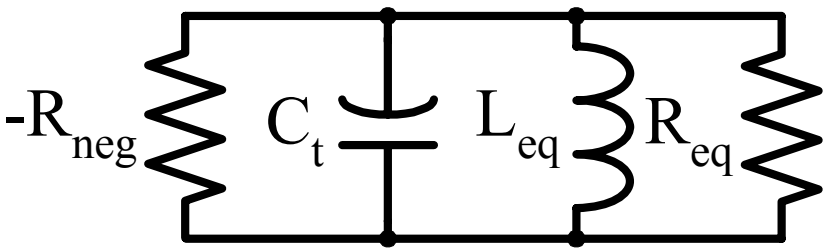
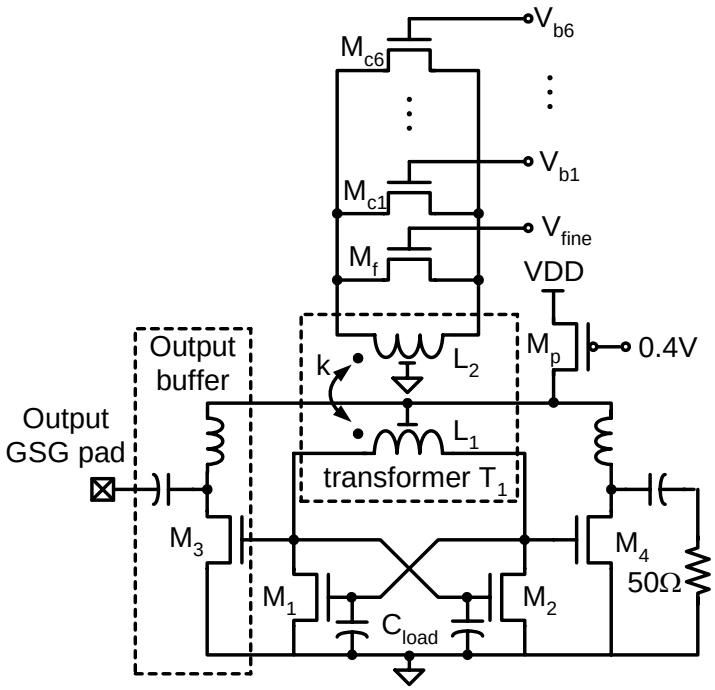
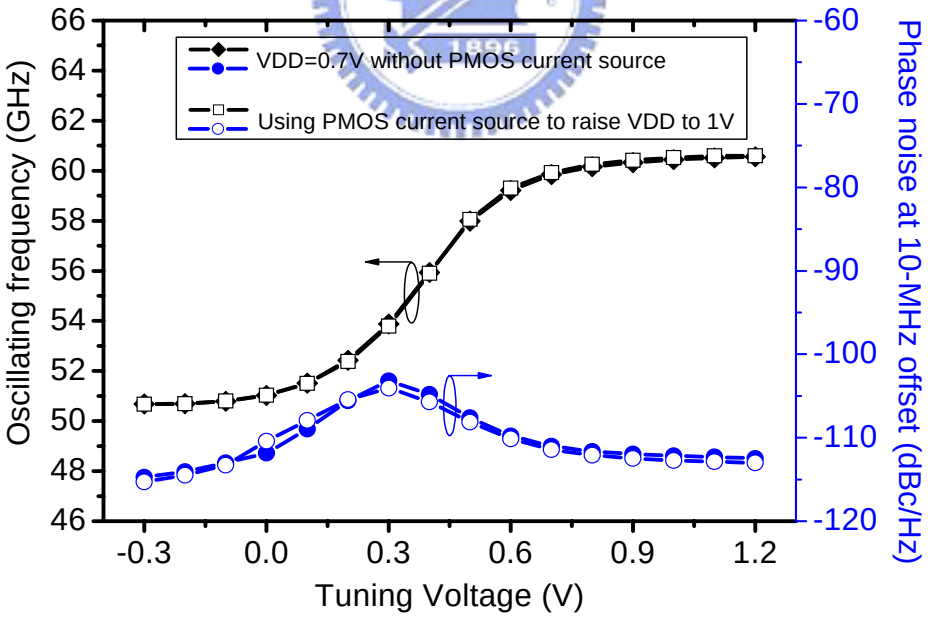


Fig. 5.6 VCO small-signal model.



(a)



(b)

Fig. 5.7 (a) Circuit schematic using PMOS current source. (b) simulation results.

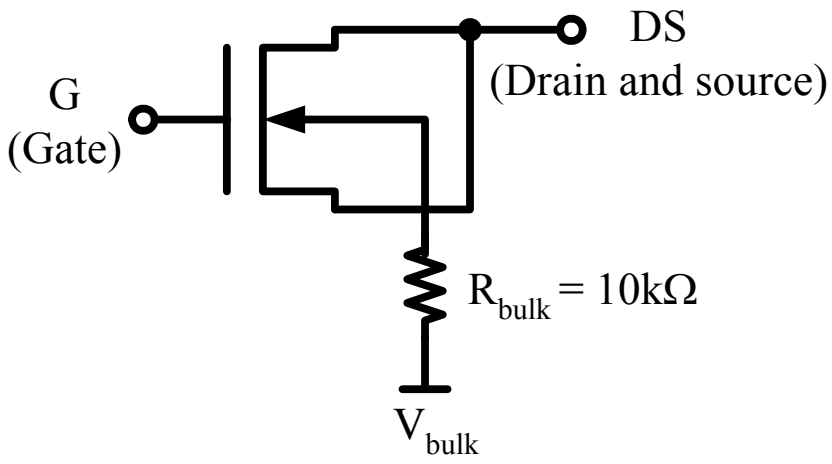


Fig. 5.8 Circuit schematic of the I-MOS varactor.

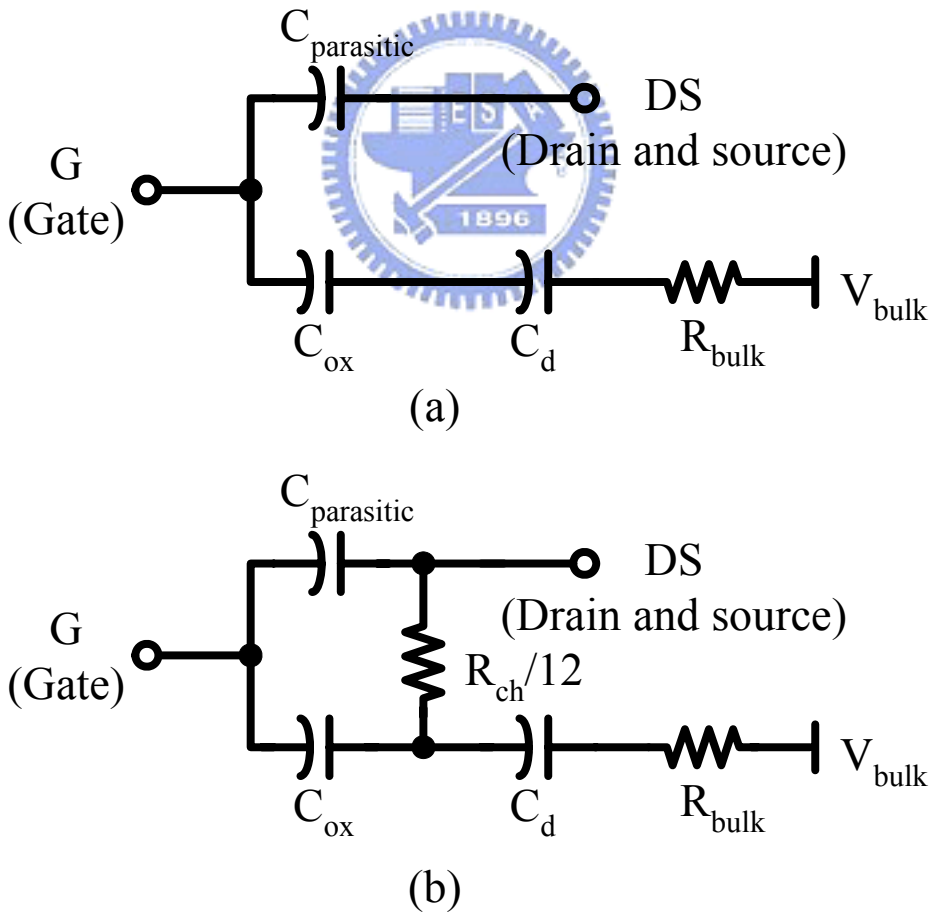


Fig. 5.9 Equivalent model of the I-MOS varactor in (a) depletion (b) inversion mode.

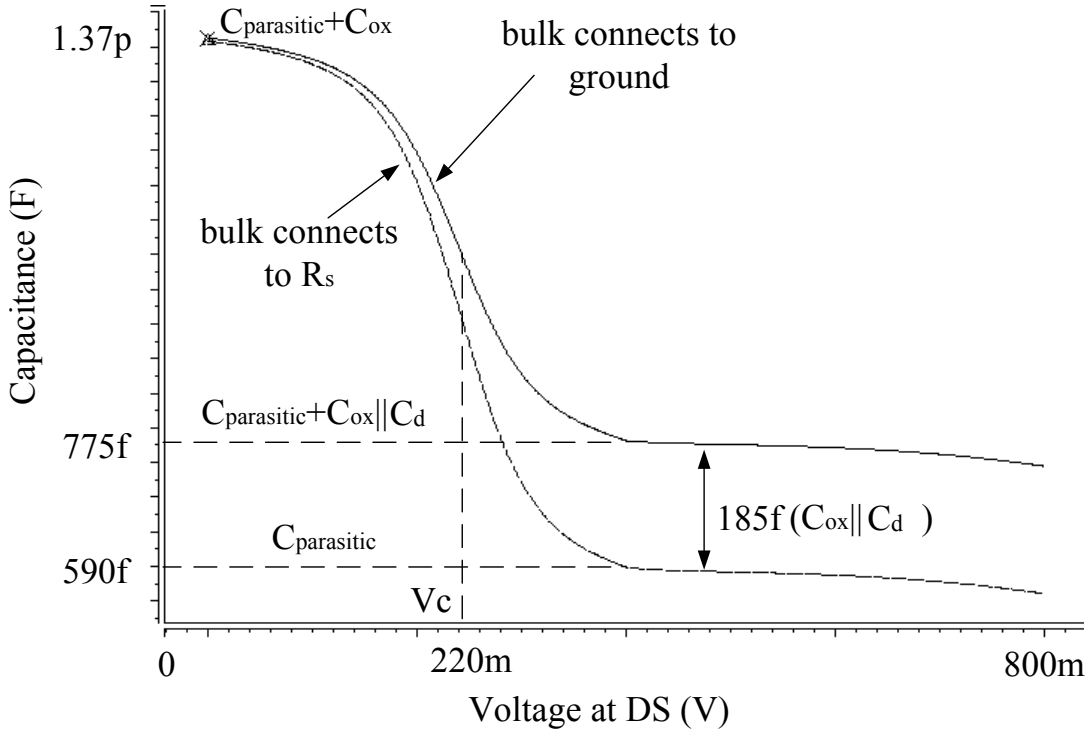


Fig. 5.10 C-V curves of theI-MOS varactor.

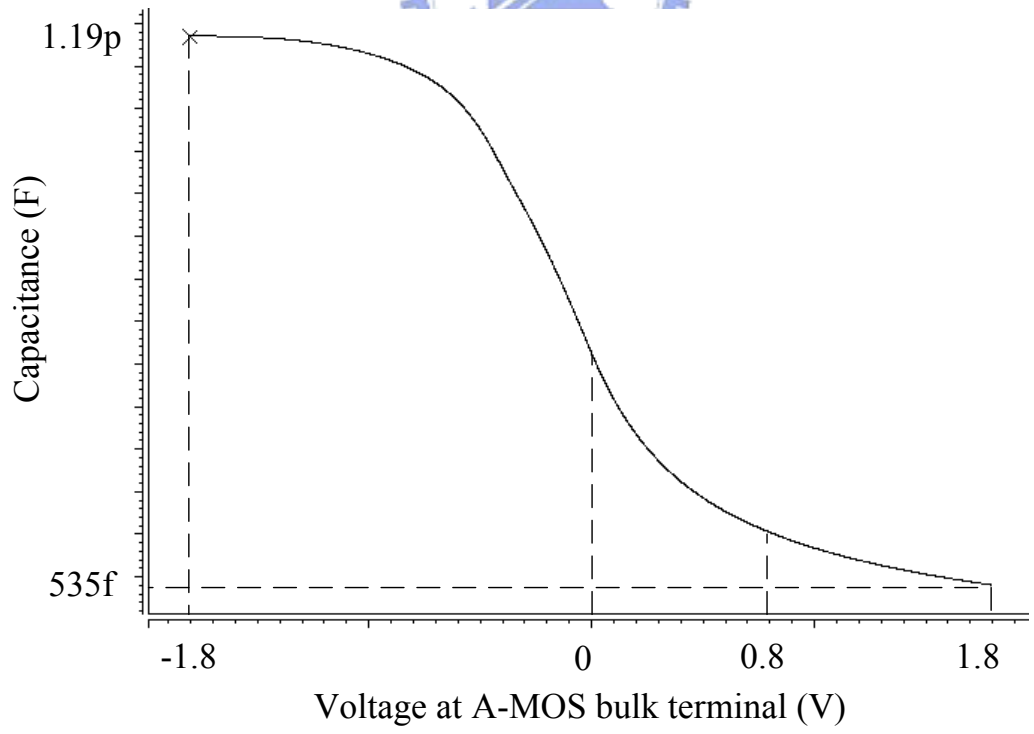


Fig. 5.11 C-V curves of the corresponding A-MOS varactor.

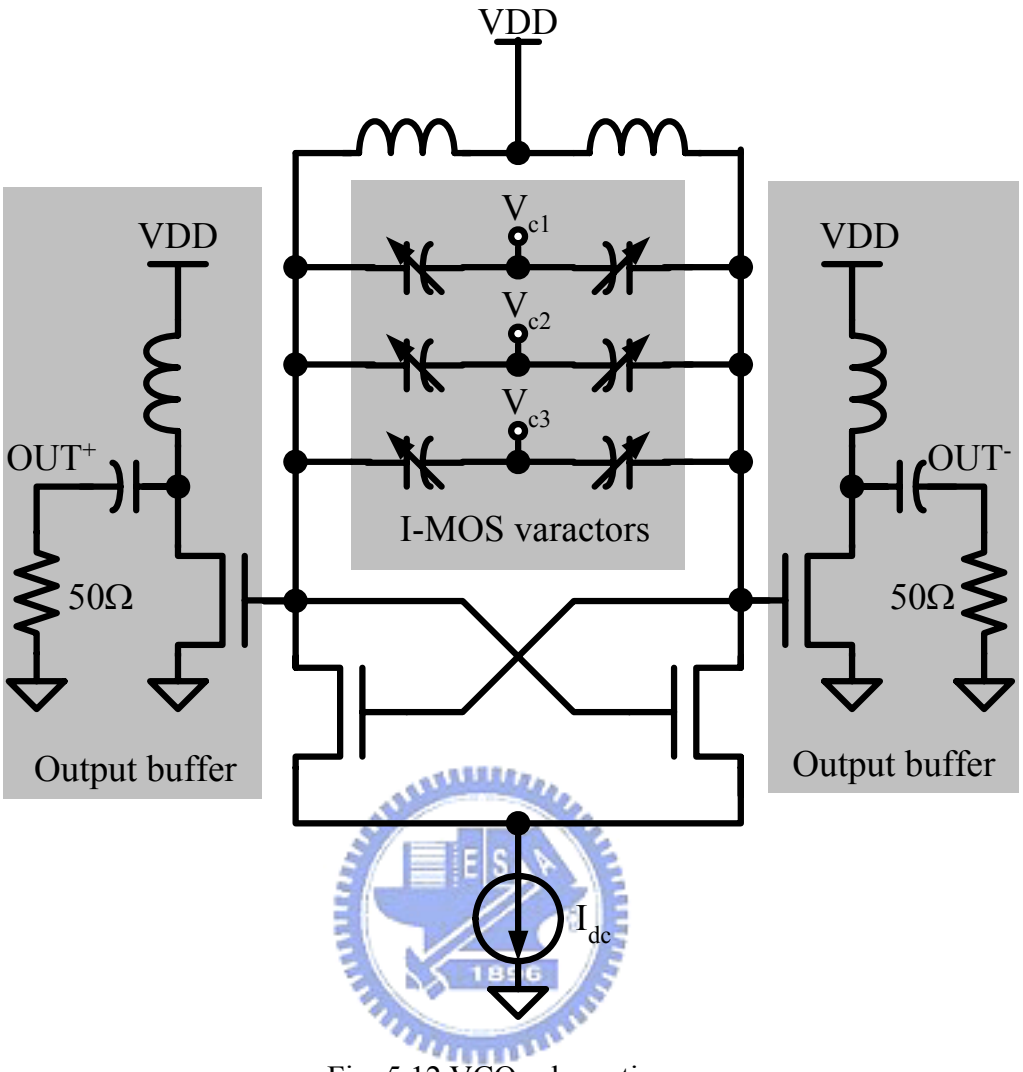


Fig. 5.12 VCO schematic.

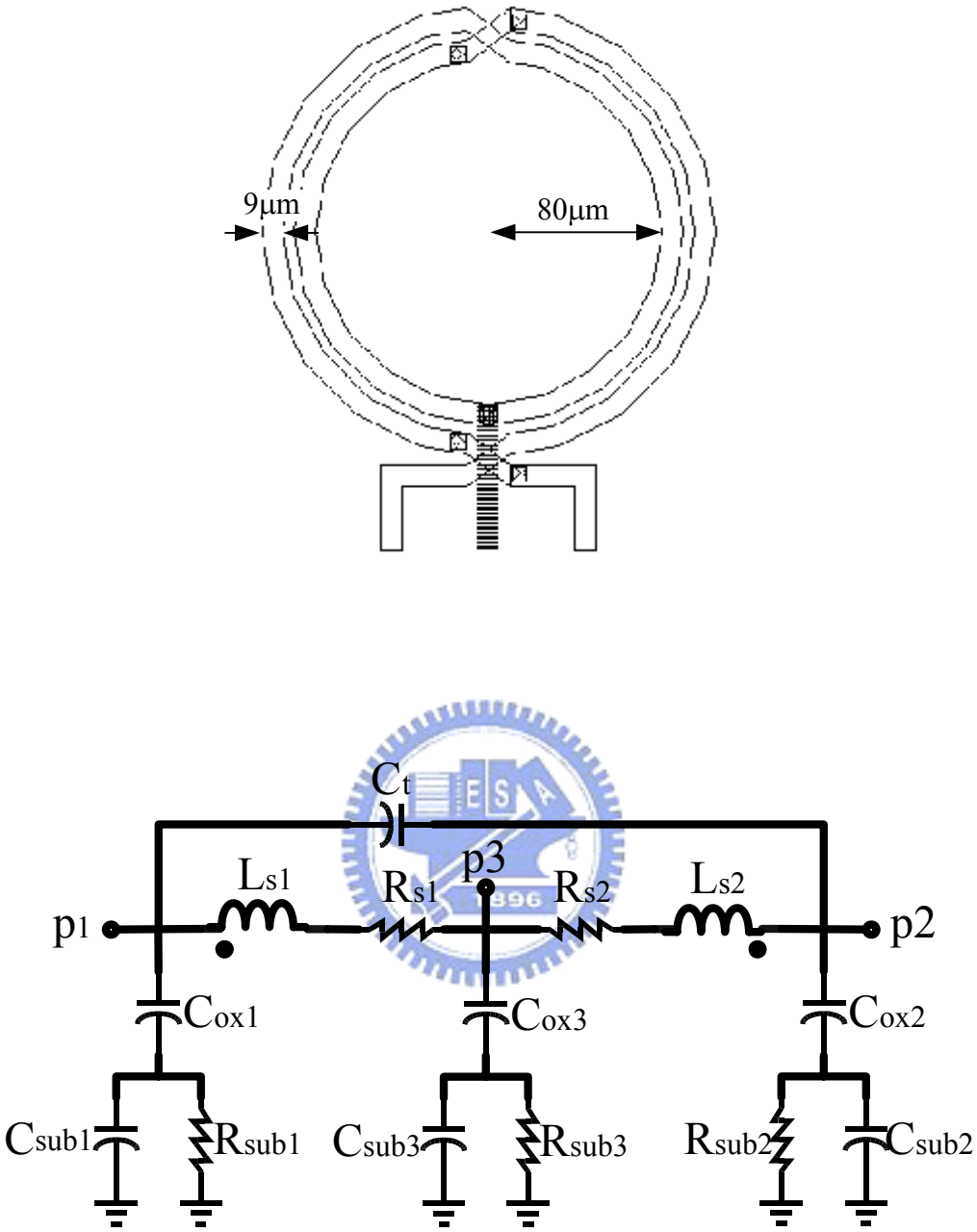
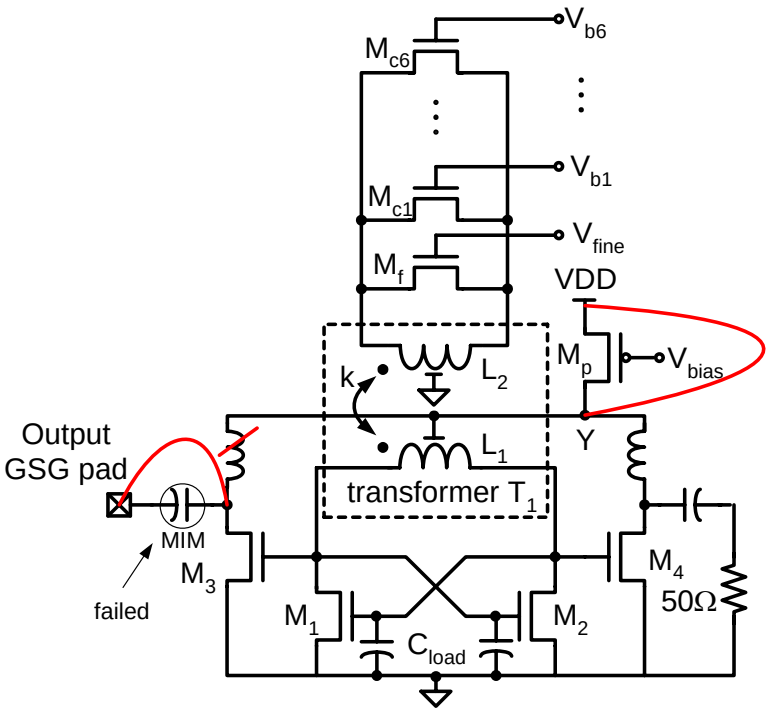
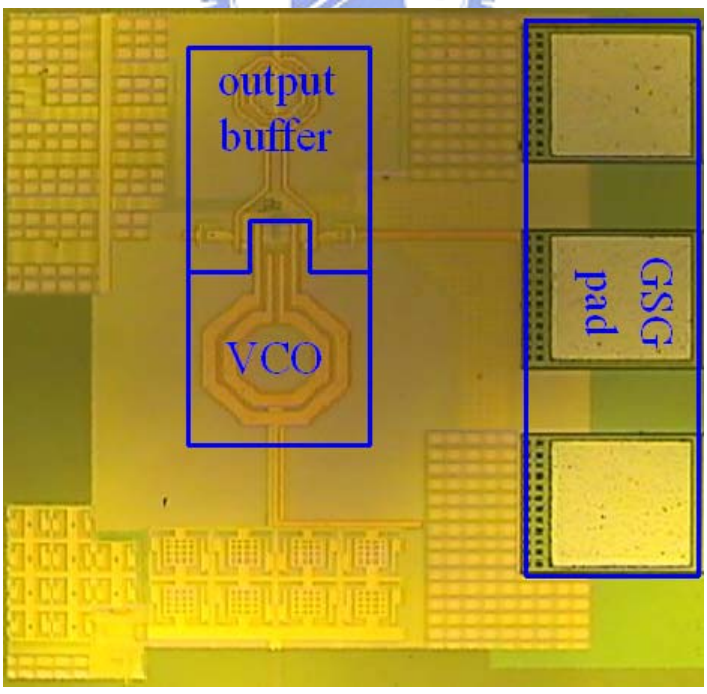


Fig. 5.13 Layout and equivalent model of the spiral inductor.



(a)



(b)

Fig. 5.14 (a) Fabricated VCO circuit schematic. (b) chip micrograph.

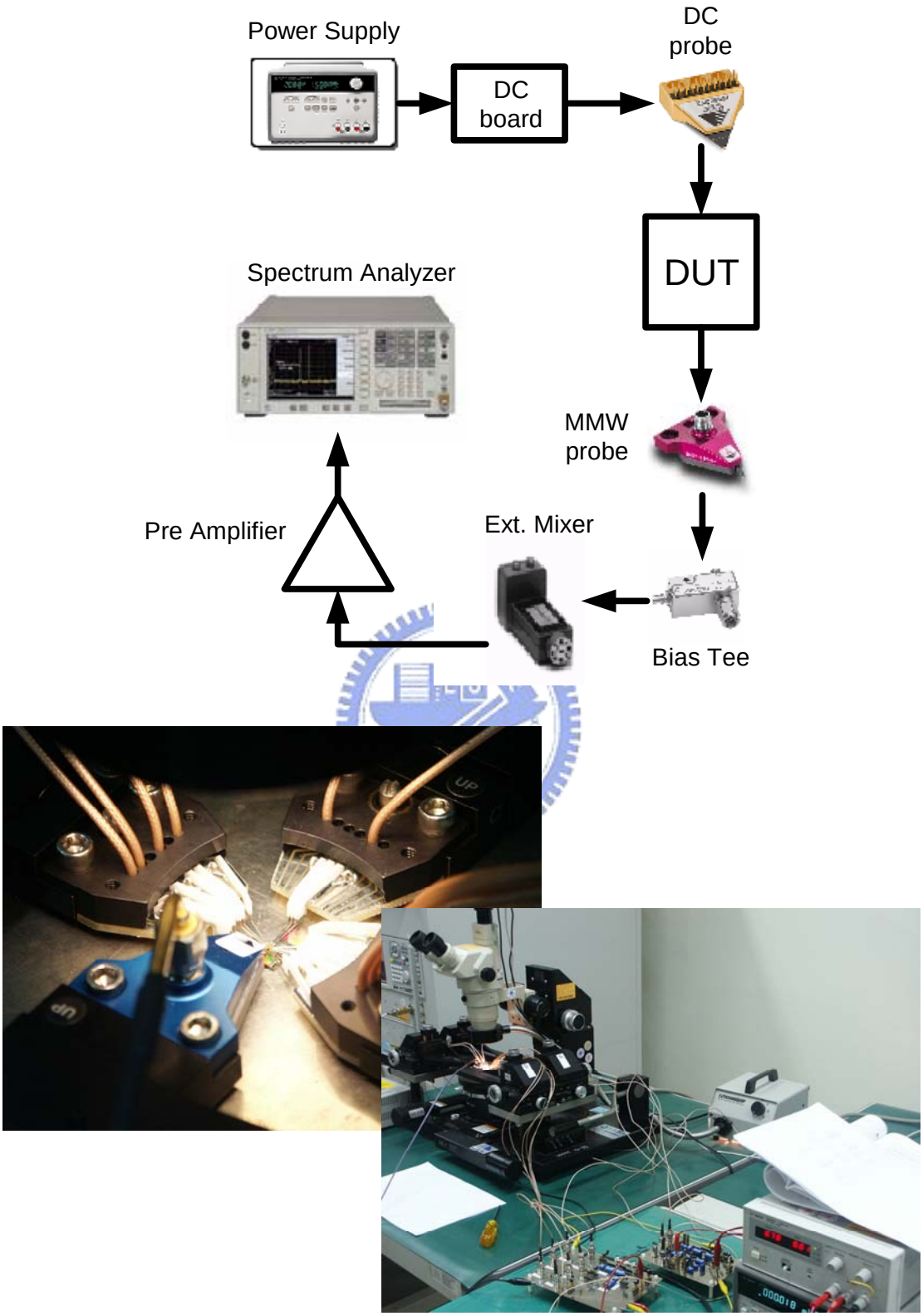


Fig. 5.15 Measurement setup and environment.

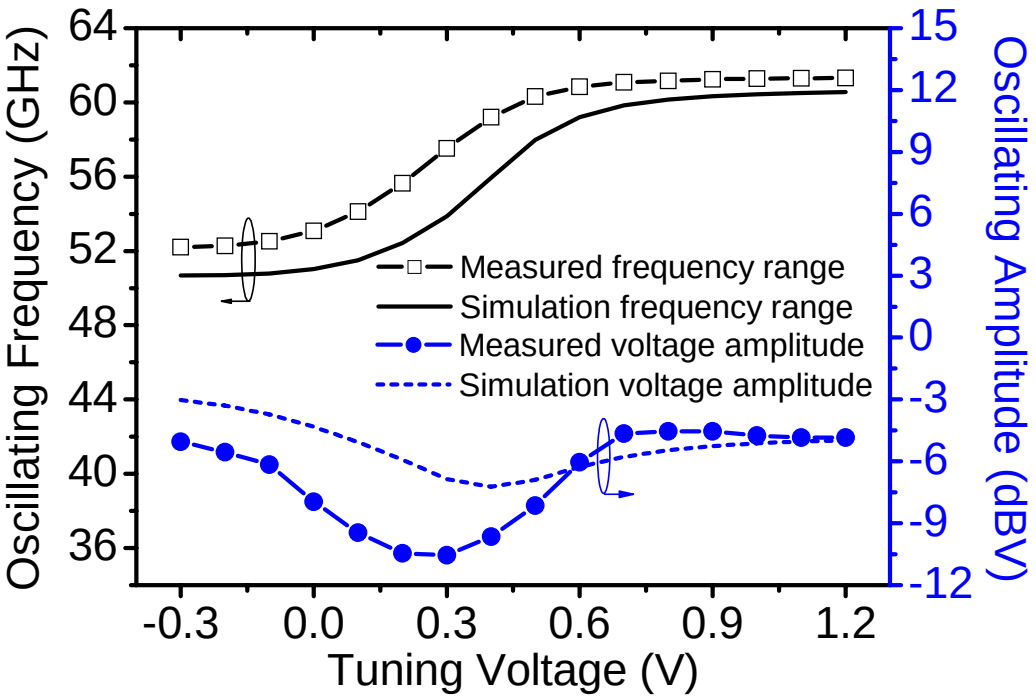


Fig. 5.16 Measured and simulated frequency tuning ranges and oscillating amplitudes.

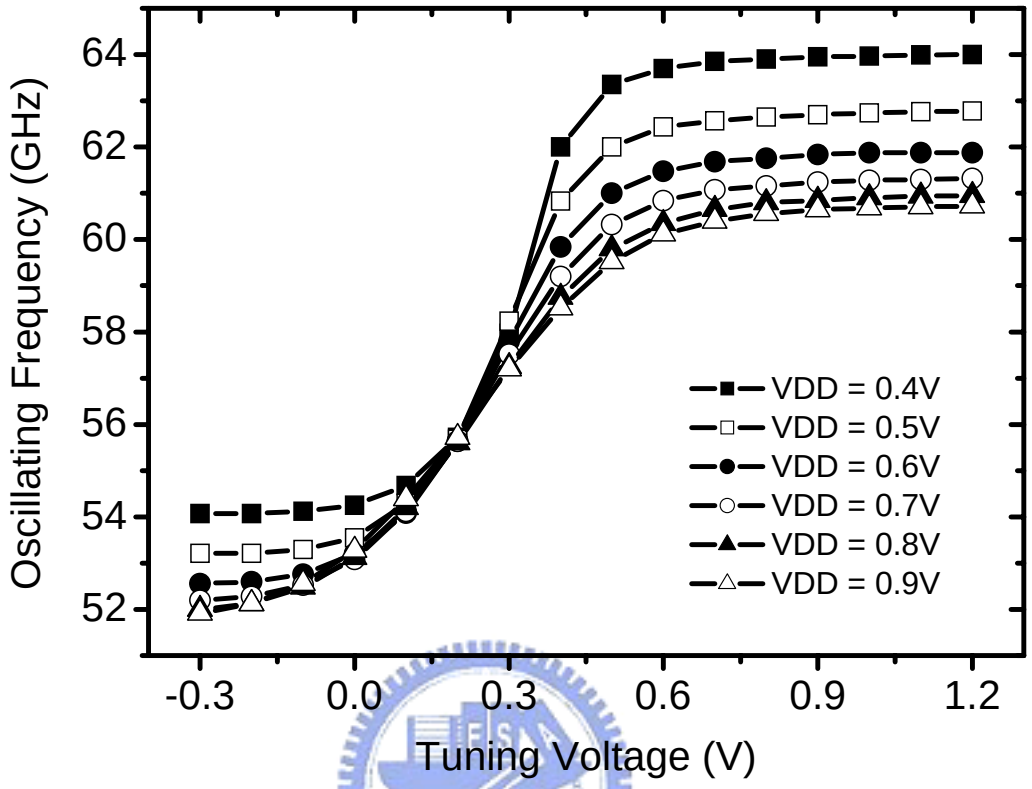


Fig. 5.17 Measured frequency tuning ranges with different supply voltages.

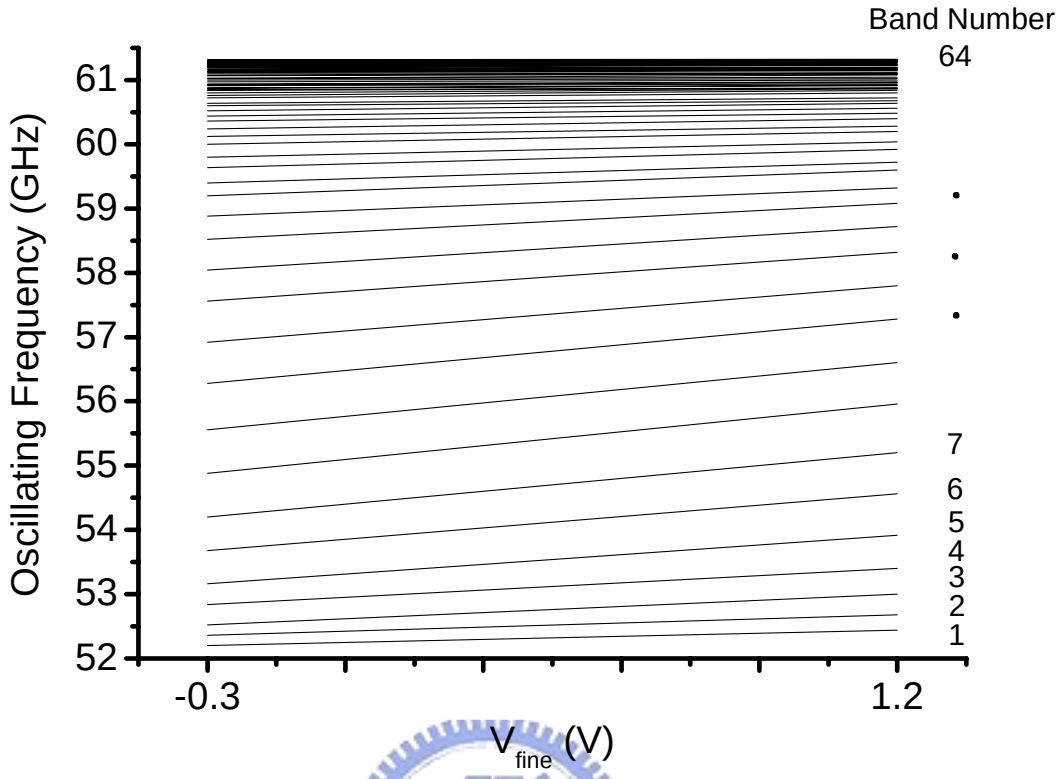


Fig. 5.18 Measured frequency tuning ranges of all bands.

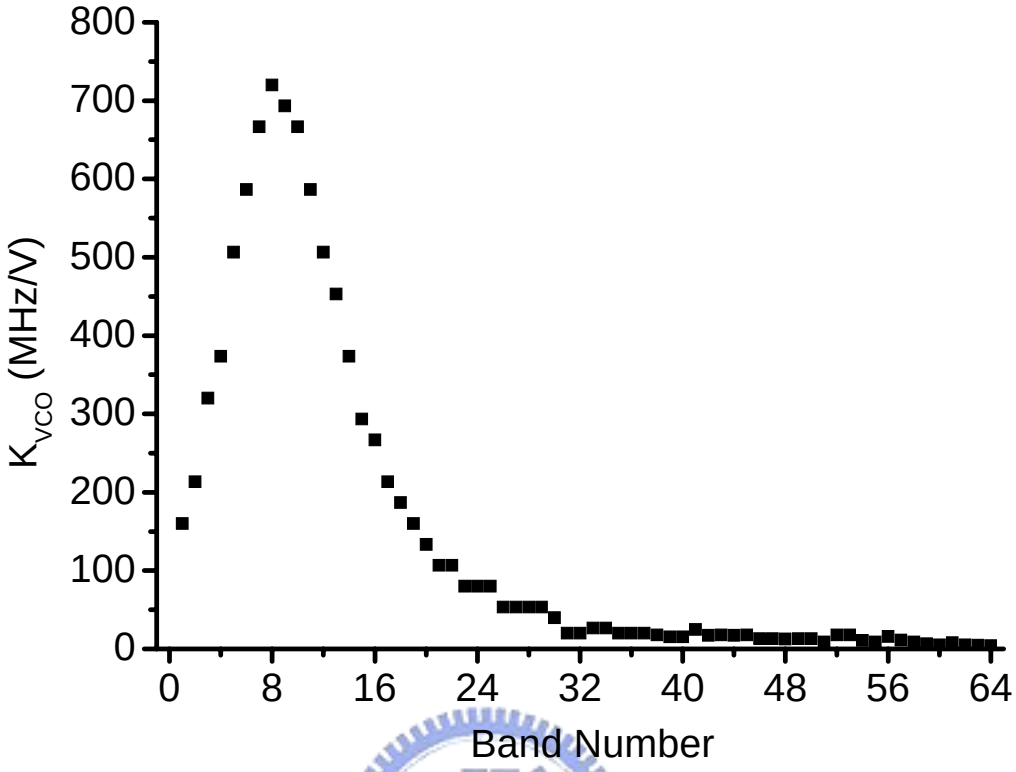
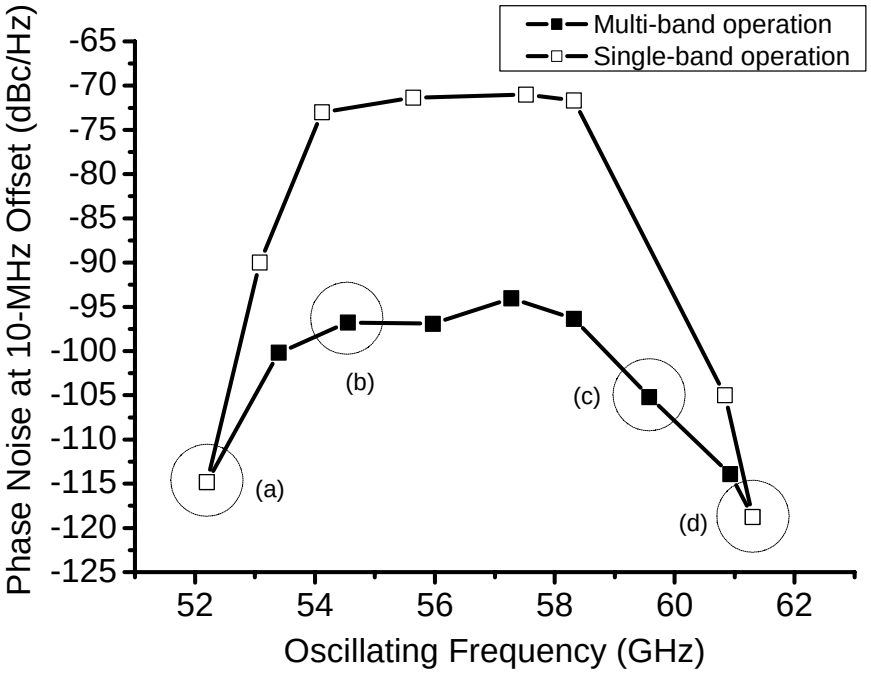


Fig. 5.19 K_{VCO} of all bands.



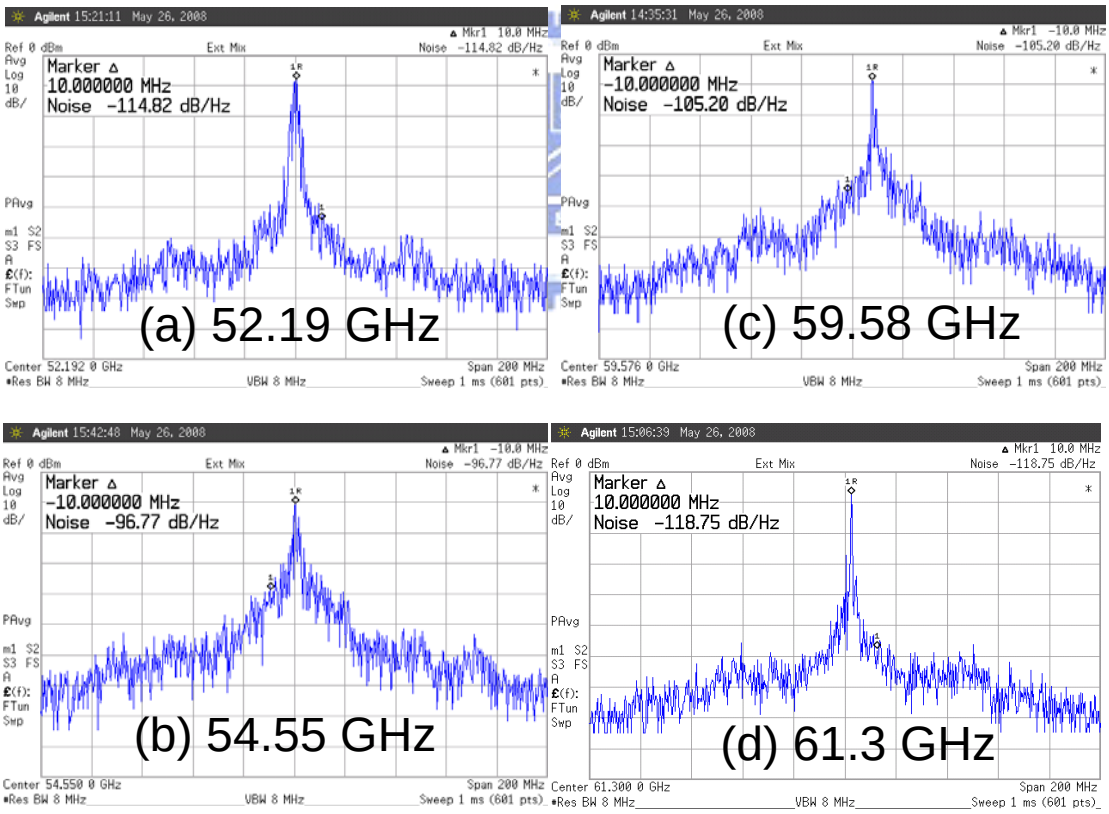


Fig. 5.20 Measured phase noises and spectrums within the frequency tuning range.

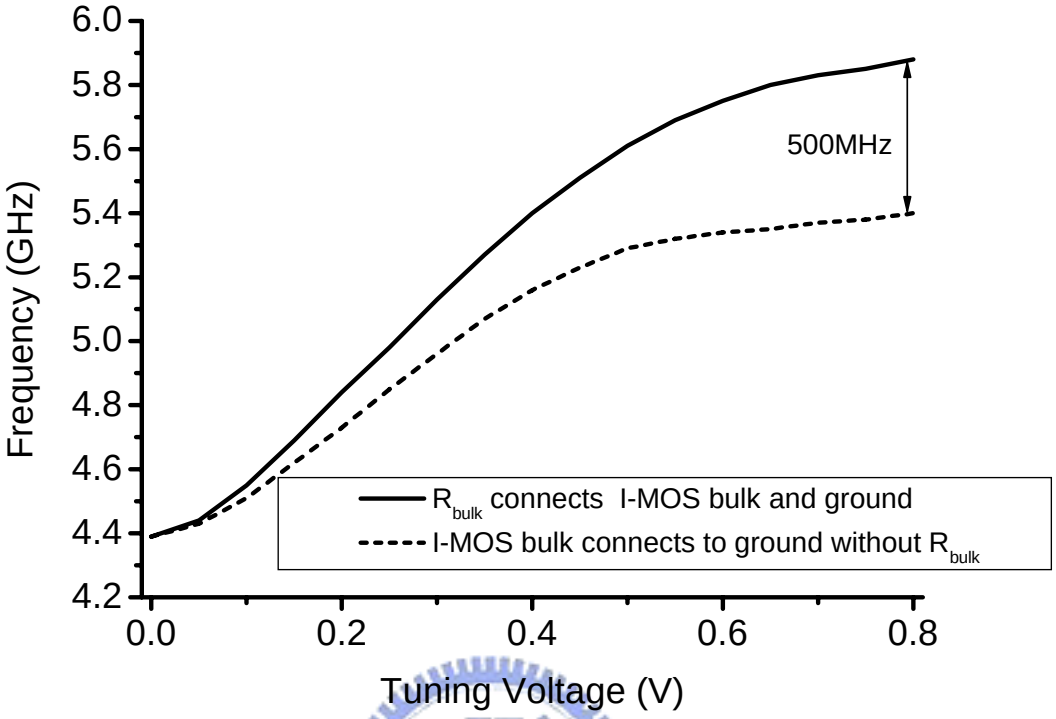


Fig. 5.21 Simulated frequency tuning ranges of the VCO.

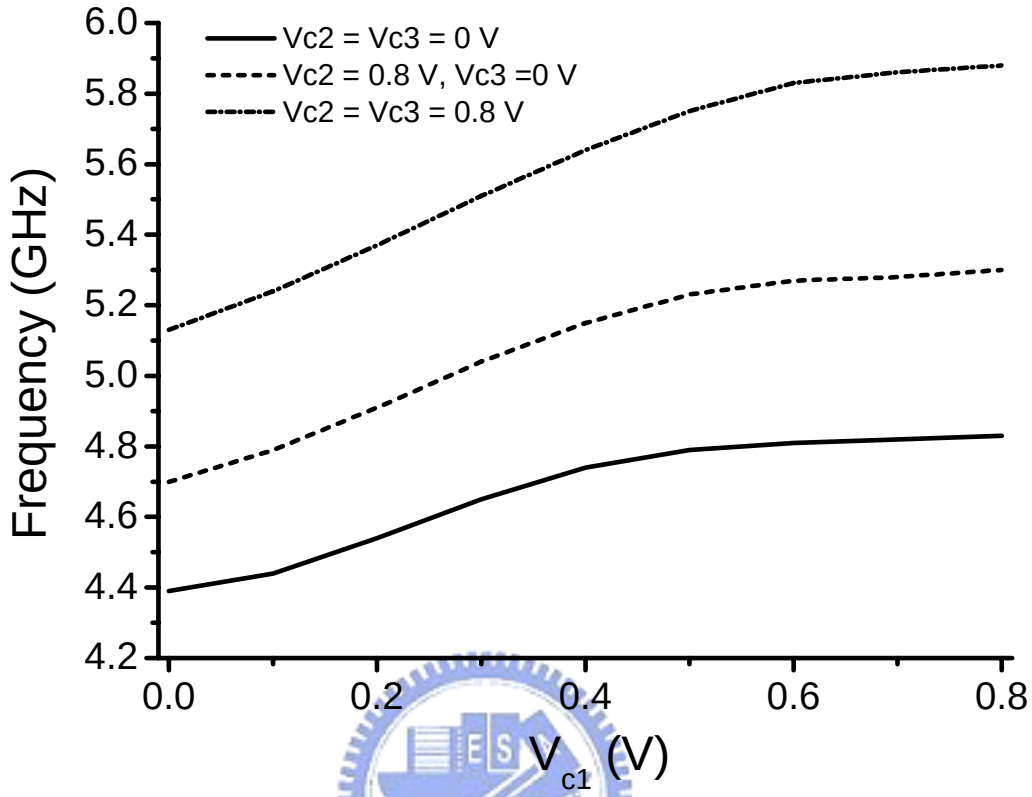


Fig. 5.22 Simulated frequency tuning range of each band.

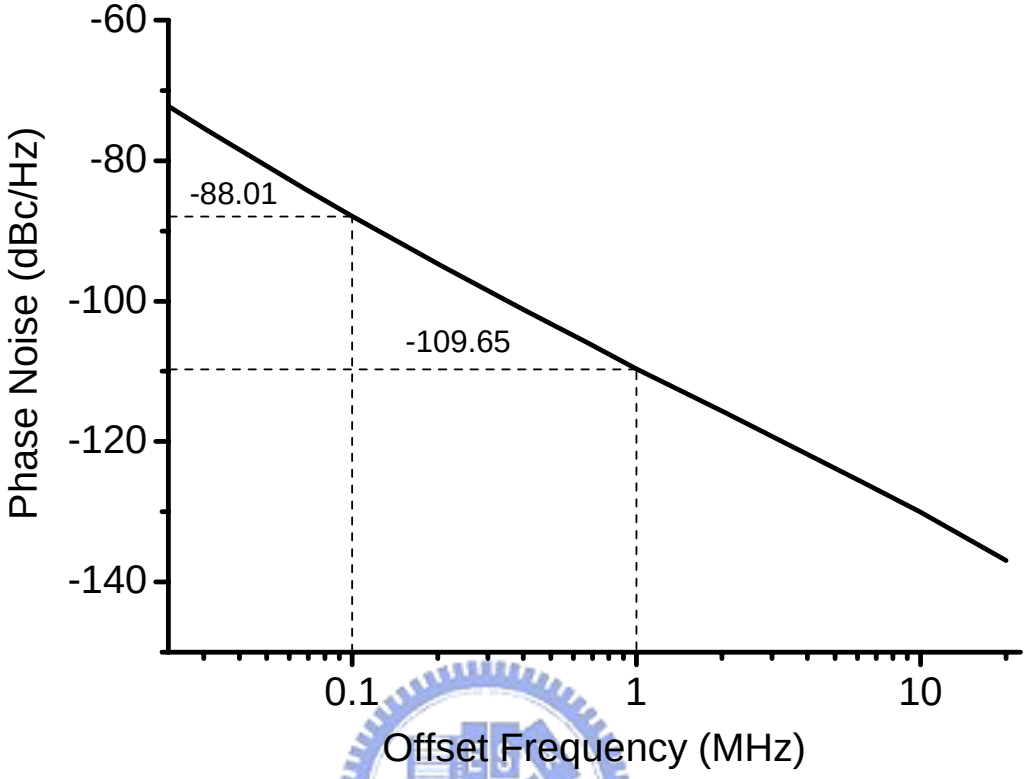


Fig. 5.23 Simulated phase noise curve.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 MAIN RESULTS OF THIS THESIS

In this thesis, design methodologies and implementation techniques of several CMOS MMW RF ICs including a direct injection-locked frequency divider, a sub-harmonic mixer, a homodyne receiver, and a multi-band VCO for MMW UWB applications are presented.

Firstly, an analytical model of a direct ILFD is presented to optimize the frequency locking range. From the proposed model, it is shown that maximizing the quality factor of the passive LC resonator in a direct ILFD can reduce the power consumption without degrading the frequency locking range. Moreover, both maintaining low output voltage amplitude and increasing the DC overdrive voltage of the input device can increase the frequency locking range. Based on these design guidelines, a direct ILFD is proposed and fabricated by using 0.13-μm bulk-CMOS technology. In the proposed structure, a PMOS current source is used to restrict the output voltage amplitude and increase the DC overdrive voltage of the input device to improve the frequency locking range. Additionally, through a resistor which connects the input device substrate and the center tapped node of the inductor, the threshold voltage of the input device can be kept low for a higher overdrive voltage such that the locking range can be improved further. For comparison purpose, the other direct ILFD designed by using an LC resonator with a lower quality factor is also fabricated and comparisons on measurement results are made. It has been shown from measurement results that the proposed ILFD has a wider frequency locking range than

the low-Q ILFD when their output amplitudes are the same. The proposed ILFD has frequency locking range of 13.6%, power consumption of 4.4 mW and its input device size is 3.6μm/0.12μm. Therefore, it is suitable for the integration with a phase-locked loop system for MMW UWB applications.

Secondly, a third-order sub-harmonic mixer is designed and analyzed. The mixer consists of two common-gate amplifiers whose gate terminals are connected to the VCO oscillation signals to modulate the transconductances for frequency conversion. The required LO frequency of the proposed mixer is 3 times less than that of the fundamental mixer. From the derived frequency tuning range of a VCO with A-MOS varators, it is shown that the frequency tuning range is inversely proportional to the square of the oscillating frequency. Therefore, by using the proposed mixer, the frequency tuning range of the integrated VCO for LO-signal generation can be significantly extended. Moreover, because the third harmonic component of the LO signal has the same polarity as the fundamental component, the third-order sub-harmonic mixer can retain the balanced structure as a fundamental counterpart with a single-phase RF signal and differential LO signals. Therefore, it has better LO-to-RF isolation in comparison with second-order sub-harmonic mixers. The proposed mixer with an on-chip VCO is fabricated by using 0.13-μm bulk-CMOS technology. The measurement results show that the frequency tuning range of the on-chip VCO is 13.35% and the corresponding RF frequency is from 54.54 to 62.34 GHz. The LO-to-RF (2LO-to-RF) power leakage is -42.5 dBm (-35 dBm). Moreover, the mixer has conversion gain of 7.8 dB and power consumption of 0.36 mW.

Thirdly, a homodyne receiver using the proposed third-order sub-harmonic mixer is proposed and designed for MMW UWB applications. The receiver includes a

broadband-matching LNA, active sub-harmonic mixers, a quadrature VCO, IF amplifiers, and output buffers. A 3-stage LNA is used to amplify the input signal and suppress the noise for the following stages. The first stage of the LNA consists of a single common-source NMOS structure with a source degeneration inductor. In comparison with the conventional cascode structure, it provides better noise figure and input matching bandwidth in the MMW band. Two double-balanced active sub-harmonic mixers are used for quadrature down conversion. Because the required LO frequency is reduced, the frequency tuning range of the integrated quadrature VCO can be significantly extended. Two-stage IF amplifiers following the mixers are used to enhance the voltage gain and bandwidth of the receiver. The final stage of the receiver is output buffers to drive off-chip 50-Ω load. It is shawn from the ADS post-simulation results that the frequency tuning range of the integrated quadrature VCO is 19.87% at 20.35 GHz and is sufficient to cover the entire MMW unlicensed band (i.e. 57-64 GHz). The voltage gain of the receiver within the unlicensed band is from 25 dB to 29.25 dB and the noise figure is from 11.1 to 13.4 dB. The receiver totally consumes 35.6 mW. In conclusion, the proposed homodyne receiver provides a solution to extend the operating frequency range for MMW UWB applications while maintaining a compact structure.

Fourthly, a new frequency tuning strategy using a single variable inductor is proposed for an MMW VCO. The variable inductor consists of a transformer and a variable resistor. The lower bound of the tuning ratio of the variable inductor is determined by the coupling factor of the transformer when the operating frequency is lower than the resonant frequency at the second coil. Therefore, the frequency tuning range of the VCO using the variable inductor is not degraded even when the oscillating frequency is increased to MMW band. Moreover, the proposed variable

inductor can be modified for multi-band operation without sacrificing the oscillating frequency. The experimental prototype of the VCO is fabricated in 90-nm CMOS technology. The measurement results show that the VCO has a frequency tuning range of 16.07% at 56.75 GHz while achieving multi-band operation. The average phase noise at 10-MHz offset is 102.4 dBc/Hz. Therefore, the VCO is suitable for MMW UWB applications.

Finally, the modified I-MOS varactors are proposed. Because of the natural abrupt gradient C-V characteristic of the I-MOS varactor, it is an attractive choice in the design of an RF multi-band VCO for a wide frequency tuning range in the case of a low tuning voltage. With a large resistor connecting ground node and I-MOS bulk node, the tuning range can be improved further. The experimental prototype of the RF multi-band VCO is designed in 0.18-μm CMOS technology. The simulation results show that the VCO has a frequency tuning range of 29.12% at 5.15 GHz when the supply and tuning voltage is 0.8 V. Such RF VCO can be used in an MMW heterodyne receiver to downconvert the IF signals to baseband.

In summary, as the bulk-CMOS technology rapidly advances toward the nanometer nodes, the CMOS ICs can be operated in the MMW band with good performance. By using the proposed CMOS MMW ICs, the operating frequency ranges can be extended and excellent performance can still be maintained. With higher levels of integration and lower cost, CMOS MMW transceivers become feasible for future MMW UWB system applications.

6.2 FUTURE WORK

The proposed analytical model of a direct ILFD is simple and useful in the direct

ILFD design. In the future, the analysis methodology which is to decompose the injection current into in-phase and quadrature terms, can be used to develop a simple analytical model for a conventional ILFD. As in the case of direct ILFD, some design guidelines can be obtained from the model to help designers to optimize the frequency locking range of a conventional ILFD.

A down-conversion third-order sub-harmonic mixer in receiving path for MMW UWB applications is proposed and analyzed. The conversion gain of the mixer is sensitive to the threshold voltage variation. A bias circuit which compensates such variation can be used to bias the mixer for a robust design. Moreover, the on-chip LO signals are usually shared between receiving and transmitting paths in an integrated transceiver. Therefore, if a third-order sub-harmonic mixer is used in the receiving path for down conversion, an up-conversion third-order sub-harmonic mixer is necessary in the transmitting path. Because the design issues of an up-conversion mixer are quite different from a down-conversion mixer, a different design methodology and circuit topology of an up-conversion third-order sub-harmonic mixer should be developed for an MMW UWB integrated transceiver.

In the implementation of the homodyne receiver for MMW UWB applications, current or gain control technique can be incorporated to improve the linearity. Because the currents of the sub-harmonic mixers are relatively low in the receiver for higher efficiency, the linearity of the receiver is limited by the mixer. However, to handle the large signals, sufficient linearity is necessary. To improve the linearity, the currents or gains of the mixers can be adjusted. One possible gain control technique is to switch the supply voltage of the mixers to ground such that the mixer becomes a passive mixer and the linearity can be improved significantly. Therefore, the receiver

can be operated in high-gain low-linearity mode for a weak input signal, but operated in low-gain high-linearity mode for a strong signal. Such technique can be implemented in the future. Furthermore, the proposed structure is beneficial for integration. Thus, more than a VCO, a frequency synthesizer also can be integrated with the proposed homodyne receiver as shown in Fig. 6.1 in the future.

An MMW VCO using a variable inductor to achieve wide-frequency-tuning range and multi-band operations is proposed. However, the oscillating voltage amplitude of the VCO is not fixed within the frequency tuning range because of the variable quality factor of the variable inductor. Therefore, an amplitude control technique can be incorporated to maintain a fixed oscillating voltage amplitude. Moreover, the VCO gains are not fixed in all bands. If a constant VCO gain is required, a more complex resistor network or g_m-controlled circuit should replace the variable resistor in the variable inductor. Moreover, based on the proposed MMW frequency divider and VCO, which are the main blocks with the highest operating frequency in a PLL system, a frequency synthesizer can be implemented for MMW UWB applications in the future. Such frequency synthesizer can be integrated with a conventional fundamental UWB front-end system as shown in Fig. 6.2 for the applications simultaneously require low noise and high linearity (i.e. sub-harmonic technique is not suitable). The fundamental receiver and the direct ILFD can be implemented using 90-nm CMOS technology to integration with the MMW VCO proposed in Chapter 5. In this situation, 1V can be chosen as the supply voltage of the whole system in Fig. 6.2. However, if the proposed MMW VCO is implemented in 0.13μm to integrate with the sub-harmonic UWB receiver and the direct ILFD proposed in Chapter 4 and Chapter 2 as shown in Fig. 6.3, the operating frequency can be boosted even higher while the operating frequency range still can be kept wide.

In this situation, 1.2V can be chosen as the supply voltage of the whole system in Fig. 6.3. Finally, when 90-nm or more advanced technologies are used in the future, gate leakage current should be modeled and considered in the MMW circuit or system (e.g. LNA and receiver) design.

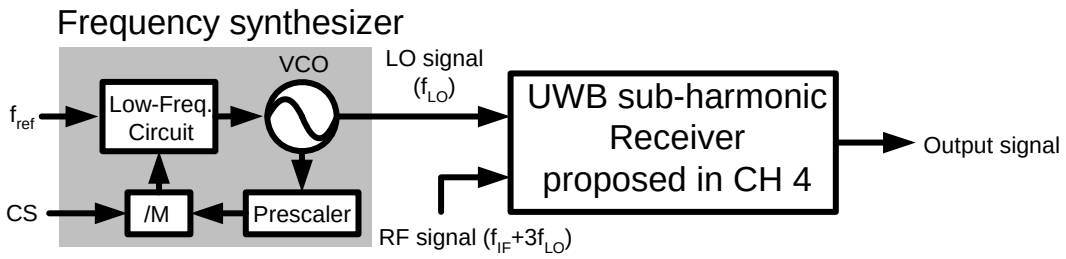


Fig. 6.1 The sub-harmonic receiver with a frequency synthesizer.

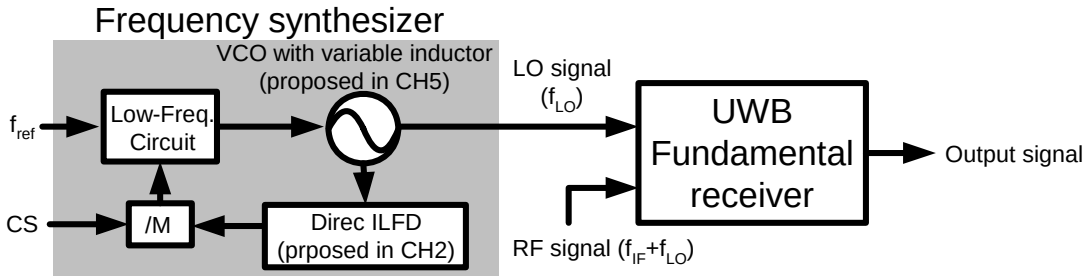


Fig. 6.2 The fundamental receiver and a frequency synthesizer using the proposed direct ILFD in Chapter 2 and MMW VCO in Chapter 5.

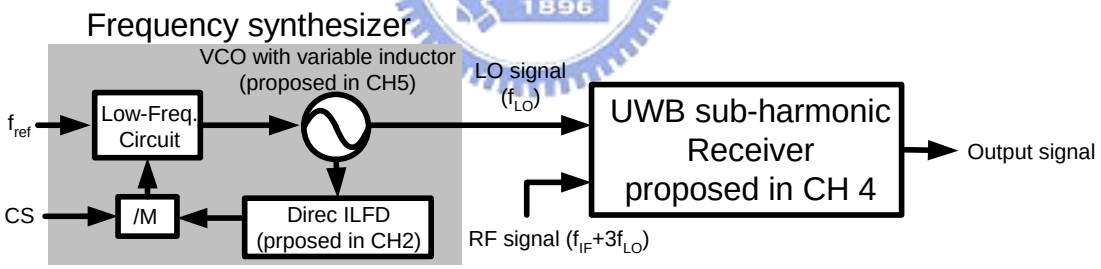


Fig. 6.3 The sub-harmonic receiver and a frequency synthesizer using the proposed direct ILFD in Chapter 2 and MMW VCO in Chapter 5.

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The Design and Analysis of CMOS Millimeter-Wave Integrated Circuits for Ultra-Wideband Communication Systems

著作　　：(見附件)

PUBLICATION LIST

(A) JOURNAL PAPERS

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(B) CONFERENCE PAPERS

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