國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

低電壓互補式金氧半製程下的類比電路設計與可靠度

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中華民國 九十六年九月

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摘要

隨著電子科技的快速發展，電子產品不斷地要求輕、薄、短、小，使得積體電路(Integrated Circuit)可靠度(Reliability)的重要性與日俱增，許多應用更需透過奈米級先進製程來實現才能帶來性能上的突破。半導體製程的微縮化造成電晶體(Transistor)元件尺寸越來越小、閘極氧化層(Gate Oxide)也越來越薄、和操作電壓也越來越低，所帶來一些元件非理想特性也對類比電路產生了重大的影響，大大提高了類比積體電路設計難度，其中在低電壓的操作設計和越來越薄閘極氧化層問題最為嚴重，所以新型低電壓類比電路設計技術與閘極氧化層的可靠度對類比積體電路之影響是十分重要的研究主題。本論文提出了一個新型之低操作電壓能隙參考電壓源(Bandgap Reference)電路與適用於低操作電壓能隙參考電壓源電路之溫度曲率補償(Curvature Compensation)技術，並針對閘極氧化層可靠度對類比電路影響進行研究與分析，另外探討了在奈米互補式金氧半製程中閘極漏電流(Gate Tunneling Current)對鎖相迴路(PLL)之影響，最後針對低溫多晶矽製程(LTPS)中提出適用於玻璃基板上類比電路設計且具有臨界電壓(Threshold Voltage)補償功能之偏壓電路設計技術。

在第二章中，本論文提出了一個低操作電壓之能隙參考電壓源電路與一個適於低操作電壓隙參考電壓源電路之溫度曲率補償技術。該新型低操作電壓能隙參考電壓源電路，最低操作電壓為 0.85 伏特，在此操作電壓之下，溫度範圍從-10°C 到 120°C 的條件下，能隙參考電壓源電路的輸出電壓之溫度係數(Temperature Coefficient)為 58.1 ppm/°C，此外，也將提出適於低操作電壓能隙參考電壓源電路之新型溫度曲率補償技術，經由實際晶片實現與驗證，此新型溫度曲率補償技術可以在能隙參考電源電路在最低操作電壓為 0.9 伏特，在溫度範圍從 0°C 到 100°C 的條件下，能隙參考電壓源電路的輸出電壓之溫度係數可以達到 19.5 ppm/°C。本論文所提出的一個新型低操作電壓能隙參考電壓源電路與一個適於低操作電壓能隙參考電壓源電路之新型溫度曲率補償之技術，已經在 0.25 微米互補式金氧半製程中實現並驗證。

半導體製程的微縮化造成電晶體元件尺寸越來越小、閘極氧化層也越來越薄，電晶體的閘極氧化層變得更為脆弱更容易遭受破壞，目前已有文獻針對閘極氧化層可靠度對數位與射頻積體電路影響進行分析與探討，可是在類比積體電路上仍未有深入的研究與分析。因此，在第三章中，針對閘極氧化層可靠度對類比電路影響進行研究與分析，針對有無堆疊結構之主動式負載共源級放大器(Common-Source Amplifier)和雙級式(Two Stage)與折疊式(Folded Cascade)運算放大器(Operational Amplifier)進行探討，分析閘極氧化層可靠度對類比電路的影響，並針對閘極氧化層軟式崩潰(Soft Breakdown)與閘極氧化層硬式崩潰(Hard Breakdown)對類比電路的影響作了詳細的分析。本論文所探討之測試電路已經在 1 伏 130 奈米互補式金氧半製程裡實現，並已在 2.5 伏的操作電壓環境下進行分析。

在低電壓互補式金氧半製程中為了使交換式電容電路(Switched-Capacitor Circuit)具有較大的輸入信號範圍與操作速度，因而在交換式電容

電路中電晶體開關均會利用閘極升壓技術(Gate Bootstrapped Technique)來設計，可是此設計方式會使得電晶體開關之閘極氧化層跨壓超過正常操作電壓，長時間操作下會對電晶體開關之閘極氧化層產生破壞。在第四章中，本論文探討電晶體開關之閘極氧化層可靠度對交換式電容電路的影響。利用所提出的交換式電容測試電路來進行分析，包括在時域與頻域的波形變化，並針對閘極氧化層軟式崩潰與閘極氧化層硬式崩潰對交換式電容電路的影響作了詳細的分析。此測試電路已經在 1.2 伏 130 奈米互補式金氧半製程中驗證。

鎖相迴路是用來於晶片系統中產生一個精準時脈的電路，為了使鎖相迴路能夠穩定的操作，在鎖相迴路之迴路濾波電路(Loop Filter)中均需要一個很大之電容器，通常在晶片上，此電容主要是利用電晶體來實現。當使用奈米互補式金氧半製程來設計鎖相迴路時，因為越來越薄的閘極氧化層將會發生嚴重的閘極漏電流問題。因此，在第五章中，本論文探討電晶體電容之閘極漏電流問題對鎖相迴路的影響，分析鎖相迴路之時基抖動(Jitter)在時域上受電晶體閘極漏電流的影響。本論文所探討之二階鎖相迴路使用 1 伏 90 奈米互補式金氧半製程之元件模型進行模擬與分析。

顯示系統面板技術的發展，已可在面板基板上加入電子電路，擴張顯示器產業的應用領域。由於複晶矽薄膜電晶體較傳統用於薄膜電晶體顯示器面板之非晶矽薄膜電晶體有更大的載子遷移率(Mobility)、較大的驅動電流、較小的臨界電壓，所以可實現顯示器驅動電路的潛力。然而，目前在系統面板內建電路設計中，最難克服的一個重點，即為“元件的變動率(Variation)”，相同元件在不同面版上的元件特性可能會有高達~30%的變動。因此，在第六章中，本論文提出具有臨界電壓補償功能之偏壓電路設計技術，此技術可以大幅降低元件的變動對偏壓電路的影響，提高類比電路在玻璃基板上之可行性。本論文所提出之適用於玻璃基板上類比電路設

計且具有臨界電壓補償功能之偏壓電路設計已經在 8 微米低溫複晶矽薄膜電晶體製程中實現並驗證。

本博士論文提出了一個新型之低操作電壓能隙參考電壓源電路與適用於低操作電壓能隙參考電壓源電路之溫度曲率補償技術，並針對閘極氧化層可靠度對類比電路影響進行研究與分析，另外探討了在奈米互補式金氧半製程中閘極漏電流對鎖相迴路之影響，最後針對低溫多晶矽製程中提出適用於玻璃基板上類比電路設計且具有臨界電壓補償功能之偏壓電路設計技術。所提出的電路已在實際晶片上成功驗証，並有相對應的國際會議論文、國際期刊論文發表。

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ABSTRACT

Due to the growing popularity of electronic technology, the electronic products are continuously asked to reduce its weight, thickness, and volume. So, the reliability of analog integrated circuit is more and more important. Moreover, with the device dimensions of the integrated circuits scaling down, the operation voltage and gate-oxide thickness of device had also been reduced. However, the extra non-ideal effects of devices have great impact on analog integrated circuit to increase design difficulty, such as the lower operation voltage and thin gate oxide. So the new design technique in low-voltage analog integrated circuit and the impact of gate-oxide reliability on performances of analog circuits can be developed. The thinner gate oxide of device will cause the reliability problem in nanoscale analog integrated circuit. In this dissertation, a new sub-1-V CMOS bandgap reference and curvature-compensation technique for CMOS bandgap reference circuit with sub-1-V operation, the impact of gate-oxide reliability on CMOS analog amplifier, the impact of gate tunneling current on performances of phase locked loop, and the new gate bias voltage generating technique with threshold-voltage compensation for on-glass analog circuits in LTPS process are presented. There are seven chapters included in this dissertation.

The new sub-1-V CMOS bandgap reference and curvature-compensation technique for CMOS bandgap reference circuit with sub-1-V operation are presented in Chapter 2. The new proposed CMOS bandgap reference without using low-threshold-voltage device can be

operated with minimum supply voltage of 0.85 V and the temperature coefficient is 58.1 ppm/°C from -10 °C to 120 °C without laser trimming. The new sub-1-V curvature-compensated CMOS bandgap reference, which utilizes the temperature-dependent currents generated from the parasitic NPN and PNP BJT devices in CMOS process, is presented. The new proposed curvature-compensation technique for CMOS bandgap reference circuit with sub-1-V operation has with has been temperature coefficient of 19.5 ppm/°C from 0 °C to 100 °C under minimum supply voltage of 0.9 V without laser trimming.

In general, the VLSI productions have lifetime of 10 years, but the thin gate-oxide thickness of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current, and hot carrier effect that will degrade the lifetime of the MOS transistor. Therefore, to improve the gate-oxide reliability of MOS transistor and to investigate the effect of gate-oxide breakdown on CMOS circuit performances will become more important in the nanometer CMOS technology. In Chapter 3, the influences of gate-oxide reliability on CMOS analog amplifier are investigated with CMOS common-source amplifiers with diode-connected active load, two-stage and folded-cascade operational amplifiers in a 130-nm low-voltage CMOS process. The test conditions of this work include the dc stress, ac stress with dc offset, and large-signal transition stress under different frequencies and signals. After overstresses, the small-signal parameters, such as small-signal gain, unity-gain frequency, phase margin, and output dc voltage levels, are measured. The impact of soft and hard gate-oxide breakdowns on CMOS analog amplifiers has been analyzed and discussed. The hard breakdown has more serious impact to the CMOS analog amplifiers.

The MOS switch with bootstrapped technique is widely used in low-voltage switched-capacitor circuit. The switched-capacitor circuit with the bootstrapped technique could be a dangerous design approach in the nano-scale CMOS process due to the gate-oxide transient overstress. In Chapter 4, the impact of gate-oxide transient overstress on MOS switch in switched-capacitor circuit is investigated with the sample-and-hold amplifier in a 130-nm CMOS process. After overstress on the MOS switch of SHA with open-loop configuration, the circuit performances in time domain and frequency domain are measured to verify the impact of gate-oxide reliability on circuit performances. The oxide breakdown on switch device will degrade the performance of bootstrapped switch technique.

In nanoscale CMOS technology, the thin gate oxide causes the large gate tunneling leakage. In Chapter 5, the influence of MOS capacitor, as loop filter, with gate tunneling leakage on the circuit performances of phase locked loop (PLL) in nanoscale CMOS

technology has been investigated and analyzed. The basic PLL with second-order loop filter is used to simulate the impact of gate tunneling leakage on performance degradation of PLL in a standard 90-nm CMOS process. The MOS capacitors with different oxide thicknesses are used to investigate this impact to PLL. The locked time, static phase error, and jitter of second-order PLL are degraded by the gate tunneling leakage of MOS capacitor in loop filter. Overview on the prior designs of gate tunneling leakage compensation technique to reduce the gate tunneling leakage on MOS capacitor as loop filter in PLL is provided in this work.

Low-temperature poly-Si LTPS thin-film transistors (TFTs) have attracted a lot of attentions in the applications with the integrated on-panel peripheral circuits for active-matrix liquid crystal display (AMLCD) and active-matrix light emitting diodes (AMOLEDs). Recently, LTPS AMLCDs integrated with driving and control circuits on glass substrate have been realized in some portable systems, such as mobile phone, digital camera, notebook, etc. In the near future, the AMLCD fabricated in LTPS process is promising toward System-on-Panel (SoP) or System-on-Glass (SoG) applications, especially for achieving a compact, low-cost, and low-power display system. However, the poly-Si TFT device suffers from significant variation in its threshold voltage, owing to the nature of poly silicon crystal growth in LTPS process. In Chapter 6, a new proposed gate bias voltage generating technique with threshold-voltage compensation for analog circuits in the low-temperature polycrystalline silicon LTPS thin-film transistors (TFTs) is proposed. The new proposed gate bias voltage generating circuit with threshold-voltage compensation has been successfully verified in a 8-μm LTPS process. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under biasing voltage of 3 V. The new proposed gate bias voltage generating technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented by LTPS process on glass substrate for active matrix LCD (AMLCD) panel.

In summary, several design and reliability of analog circuits in low-voltage CMOS processes are presented in this dissertation. The proposed circuits have been implemented and verified in silicon chips. The proposed CMOS bandgap reference circuits, the impact of gate-oxide reliability on CMOS analog amplifiers, and the proposed gate bias voltage generating technique are very useful for the advanced nanoscale CMOS technology and SoP application, respectively.

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陳 榮 昇
誌於竹塹交大
96 年 夏

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TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER 1

Introduction

In this chapter, the background of this dissertation is discussed. First, the scaling trend of the CMOS technology is introduced. The device dielectric reliability issue about the gate-oxide breakdown, hot-carrier injection, and negative bias temperature instability in the advanced technology are also discussed. Then, the design and reliability issues of the analog circuits realized in low-voltage CMOS processes are discussed. Finally, the rest of this dissertation is organized.

1.1. CMOS Scaling

The goals of CMOS scaling are to increase the speed and density of the transistors in integrated circuits. Table 1.1 summarizes the key features of the semiconductor scaling trend, which are predicted by the Semiconductor Industry Association (SIA) [1]. The increase of speed requires the higher current density of the transistor due to the load capacitance per unit transistor width has historically remained constant. The drain current (I_D) of the NMOS transistor in the saturation region can be expressed as

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 - \lambda \cdot V_{DS}), \tag{1.1}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{1.2}$$

where μ_n is the mobility of the NMOS transistor, C_{ox} is the gate capacitance per unit area of the NMOS transistor, W and L are the channel width and channel length of the NMOS transistor, V_{TH} is the threshold voltage of the NMOS transistor, λ is the channel-length modulation parameter, ε_{ox} is a dielectric constant of gate oxide, and t_{ox} is the oxide thickness. As shown in Table 1.1, the reduction in channel length (L) and the gate oxide thickness (t_{ox}) of MOS transistor increase the current density, and more functional MOS transistors can be

fabricated on the same silicon area in advanced CMOS technology. In order to decrease the leakage current and second-order effect of MOS transistor, the operation voltage must be scaled. There three major current leakage phenomenons in short channel MOS device: drain-induced barrier lowering (DIBL), punch-through, and gate-induced drain leakage (GIDL) in advanced CMOS technology. Furthermore, the operation voltage and threshold voltage of MOS transistor are decreased simultaneously for keeping the characteristic and reliability of MOS transistor. In order to decrease the leakage current of MOS transistor, the operation voltage must be scaled. These advances in CMOS circuit performance have been enabled by the miniaturization of MOS device in advanced CMOS technology.

Although the CMOS scaling is toward to increase the speed and the density of MOS transistor, the reliability issue becomes more responsible in the future technologies. The gate oxide thickness and the channel length of MOS transistor are become thinner and shorter, respectively, in future technologies. These result in the gate-oxide breakdown (BD) [2]-[5], hot-carrier injection (HCI) [6], [7], and negative bias temperature instability (NBTI) [8]-[11] issues become more important. Besides, the thinner gate-oxide thickness of MOS transistor also causes extra gate tunneling leakage current. It provides motivation for why design and reliability of integrated circuit is an important issue for future.

1.1.1. Device Dielectric Reliability

The dielectric reliability of MOS transistor includes the ate-oxide breakdown (BD) [2]-[5], hot-carrier injection (HCI) [6], [7], and negative bias temperature instability (NBTI) [8]-[11] issues in advanced CMOS technology. The predominant failure modes of HCI and NBTI are a shift of threshold voltage, device current, and transconductance of MOS transistor over time. The gate-oxide breakdown of MOS transistor causes the dielectric leakage current increases with time under constant voltage stress.

1.1.1.1. Gate-Oxide Breakdown

The gate oxide thickness (t_{ox}) of CMOS transistor can be became thinner in order to scale CMOS technology. Since electric fields in the gate oxide are expected to rise with scaling, the long-term reliability of thin gate oxides becomes an important issue in advance

CMOS processes. Gate-oxide breakdown is defined as the time when a cluster of connected bonds, beginning from a "seed" at one interface of the gate-oxide reaches the opposite interface [12]. The gate-oxide breakdown mechanism of MOS transistor in CMOS technology includes the soft gate oxide breakdown and hard gate oxide breakdown.

Gate-oxide breakdown begins when traps form in the gate oxide of MOS transistor. At first the traps are non-overlapping and thus do not conduct as shown in Fig. 1.1, but as more and more traps are created in the gate oxide, traps start to overlap creating a conduction path [13]. Once these traps form a conduction path from the gate to the channel, oxide breakdown occurs [13], as shown in Fig. 1.2. This breakdown mode is called soft gate oxide breakdown (SBD). Once there is conduction, new traps are created by thermal damage, which in turn allows for increased conductance as shown in Fig. 1.3 [13]. The cycle of conduction leading to increased heat to increased conduction leads to thermal runaway [14] and finally to a lateral propagation of the breakdown spot [15], as shown in Fig. 1.4. The silicon within the breakdown spot starts to melt, and oxygen is released, and a silicon filament is formed in the breakdown spot [14]. This breakdown mode is called hard gate oxide breakdown (HBD).The lift time of MOS transistor under voltage stress can be expressed as [16]

$$\frac{1}{\tau_0}\int_0^{t_{BD}} \exp\left(-\frac{G \cdot X_{eff}}{V_{ox}(t)}\right) \cdot dt = 1, \tag{1.3}$$

where τ_0 and G are two constants, X_{eff} is the effective thickness of the gate oxide due to the defeats, and $V_{ox}(t)$ is the time-dependent voltage across the gate oxide, t_{BD} is the time-to-breakdown, and t_{ox} is the oxide thickness. The equation 1.3 can be re-written by

$$t_{BD} = \tau_0 \cdot \exp\left(\frac{G \cdot t_{ox}}{V_{ox}}\right) \tag{1.4}$$

under the DC stress and the defeat-free gate oxide. In equations 1.3 and 1.4, the t_{ox} and V_{ox} are two key factors under oxide breakdown. Therefore, the gate-oxide reliability is as very important issue in advanced CMOS technology.

1.1.1.2. Hot-Carrier Injection

When the CMOS technology is scaled, the channel length of MOS transistor becomes

thinner and thinner. The short-channel MOS transistor may experience high lateral electric field to cause the hot-carrier injection, if drain-to-source voltage is large. The hot-carrier injection of NMOS transistor is illustrated in Fig. 1.5 [17]. When the channel of NMOS transistor is formed ($V_G>V_{TH}$) and a large drain-to-source voltage (V_{DS}) is applied, 1. electrons are accelerated by the large lateral electric field. 2. These electrons arrive to the drain depletion region and create electron-hole pairs through impact ionization. 3. If the generated electron has more than approximately 1.5 eV, they can tunnel into the oxide region. The trapped charge in oxide region of MOS transistor will decrease the saturation current I_{DS}, cause the threshold voltage drift, decrease the linear region transconductance, and degrade the sub-threshold slop. 4. The generated holed will be collected by source and substrate. This will result in that the snapback breakdown or latch-up occurs in MOS transistor to cause the large current into the substrate. Lightly doped drain (LDD) structure can be used in the advanced processes to allow the higher drain-source voltage without the hot-carrier degradation [17]-[20]. However, the LDD structure increases the series drain resistance, which degrades the speed performance.

1.1.1.3. Negative Bias Temperature Instability

Negative bias temperature instability (NBTI) occurs in PMOS transistor stressed with negative gate bias at elevated temperatures. NBTI degradation in MOSFETs is explained by the reaction-diffusion (RD) model mentioned in [21]–[24]. The hydrogen gas diffuses into the gate-oxide and yields passivated Si bonds, as shown in Fig. 1.6 [24]. The hydrogen-annealing technique has provided a viable solution to the interface-trap instabilities for decades; however, recent scaling trends and processing modifications have brought NBTI into attention. According to the standard reaction–diffusion model for NBTI, for a negatively biased PMOS transistor, the holes in the inversion layer react with the Si-H bonds at the Si/SiO_2 interface. This leads to the dissociation of the Si-H bonds and results in Si- dangling bonds at the interface. The generated hydrogen species diffuse away from the interface toward the polysilicon gate. In the absence of holes near the interface, a reverse reaction takes place in which hydrogen species diffuse back to the Si/SiO_2 interface and react with Si-bonds to anneal the generated interface states [21]–[24]. Specifically, negative bias temperature instability causes systematic reduction in transistor parameters, such as drain current, transconductance, threshold voltage, capacitance, when a PMOSFET is biased in inversion ($V_S=V_D=V_B=V_{DD}$ and $V_G=0$).

Advances in technology have raised many new issues related to both circuit performance and reliability. Since electric fields in the gate oxide are expected to rise with scaling, the long-term reliability of thin oxides becomes an important concern in advanced CMOS processes. As described in sections 1.1.1, 1.1.2, and 1.1.3, the CMOS scaling causes many reliability issues in advanced CMOS technology, such as gate-oxide breakdown, hot carrier injection, and negative bias temperature instability.

1.1.2. Gate Tunneling Leakage Current

According to the SIA roadmap [1], CMOS with gate length below 70 nm will need an oxide thickness of less than 1.5 nm, which corresponds to two to three layers of silicon dioxide atoms.With such a thin gate oxide, direct tunneling occurs resulting in an exponential increase of gate leakage current [25]-[31]. The resulting gate leakage current will increase the power dissipation and will deteriorate the device performance and circuit stability for VLSI circuits. Control of off-state drain leakage (I_{off}) and on-state gate leakage (I_G) is one of the most important issues for scaling MOSFETs toward the 0.10 μm regime [25]-[31]. For deep submicron technology, as effective gate length decreases, the leakage increases because of the following scaling trends: 1) subthreshold leakage (I_{sub})increases exponentially due to threshold voltage reduction [29]; 2) gate edge-direct-tunneling leakage (I_{EDT}) and gate-induced drain-leakage (I_{GIDL}) increase exponentially due to reduced gate oxide thickness [30], [31]; 3) bulk band-to-band-tunneling leakage ($I_{B\text{-}BTBT}$) increases exponentially due to increased lightly doped-drain (LDD) or pocket-doping concentrations [29]. The cross section of the NMOSFET structure and drain leakage components are schematically shown in Fig. 1.7 [28]. The off-state drain leakage (I_{off}) and on-state gate leakage (I_G) of MOSFET will increase the power consumption and degrade the performances of integrated circuit in advanced CMOS technology. The high-K gate dielectrics of MOSFET can be used to avoid the gate leakage effect in advanced CMOS technology [32]-[34].

1.2. Issues of Analog Circuit Design and Reliability in Low-Voltage CMOS Technology

The desire for portability of electronic equipment generated a need for low power

systems in battery-operated products, such as cell phones, PDAs and notebooks. The device dimension of transistor has been scaled toward the nanometer region and the power supply voltage of chips in the nanoscale CMOS technology has been also decreased due to the reliability and power consumption issues [1]. Voltage reductions guarantee the reliability devices to low the electrical fields inside oxide layers of MOSFET. As shown in Table. 1.1, the power supply voltage is decreased and the oxide thickness is thinner when the process is scaled down. Because of noise and offset voltage constraints, the minimum size transistors cannot be used in analog circuit. However, scaling results in better performance in digital circuit. When analog circuit operates in low voltage, the main constraints are the device noise level and the threshold voltage (V_{TH}). The reduction of threshold voltage is dependent on the device technology. High threshold voltage gives better noise immunity and lower threshold voltage reduces the noise margin to result in poor signal-to-noise ratio (SNR) [35]. In order to get the better performance of analog circuit in low-voltage CMOS technology, a possible solution to get higher DC voltage on-chip is multiplication. However, this technique is noisy and not compatible with sensitive analog circuit. Another problem of this technique is gate-oxide reliability. Many design technique of analog circuit in low-voltage CMOS technology have been proposed, such as MOSFET operated in sub-threshold region [35]-[37], bulk driven transistors [35], [36], [38], [39], self-cascode structures [35], floating gate approach [35], [40]-[44], and level shifter techniques [35], [45]-[47].

In general, the VLSI productions have lifetime of 10 years, but the thin gate-oxide thickness of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current, and hot carrier effect that will degrade the lifetime of the MOS transistor. Another important problem in low-voltage CMOS technology is the gate-oxide reliability. In modern CMOS very large scale integrated circuits (VLSIs) including digital signal processor and embedded analog circuitry, the digital logic or digital logic circuits are generally implemented using thin-oxide devices. However, analog circuitry needs to be operated at a higher supply voltage than the nominal supply voltage of thin-oxide devices to achieve a wide dynamic range performance or meet the compatibility requirement with standardized protocols or with ICs from previous generations [48]. High-voltage tolerance of analog circuit design technique in nanoscale CMOS technology has been proposed [48]. Therefore, to improve the gate-oxide reliability of MOS transistor and to investigate the effect of gate-oxide breakdown on CMOS circuit performances will become more important in the nanometer CMOS technology. The impact of gate-oxide reliability on CMOS digital and RF

circuit has been investigated [49]-[52]. Reference [49] has reported that the oxide breakdown do not affect the digital circuit operation. Only the power consumption of digital circuit will be increased due to the gate-oxide breakdown. Reference [50] has reported the performances of dynamic digital circuit are degraded by gate-oxide breakdown. In [51], [52], the performances of RF and SRAM circuits are also degraded by gate-oxide breakdown. However, the impact of gate-oxide breakdown on CMOS analog circuits did not have particular report.

Therefore, in this dissertation, several sub-1-V bandgap reference circuits and the impact of gate-oxide reliability on analog circuits in low-voltage CMOS technology are investigated and presented.

1.3. Organization of This Dissertation

In Chapter 2, a new sub-1-V CMOS bandgap voltage reference without using low-threshold-voltage device is presented in this paper. The new proposed sub-1-V bandgap reference with startup circuit has been successfully verified in a standard 0.25-μm CMOS process, where the occupied silicon area is only 177 μm × 106 μm. The experimental results have shown that, with the minimum supply voltage of 0.85 V, the output reference voltage is 238.2 mV at room temperature, and the temperature coefficient is 58.1 ppm/°C from -10 °C to 120 °C without laser trimming. Under the supply voltage of 0.85 V, the average power supply rejection ratio (PSRR) is -33.2 dB at 10 kHz. The new sub-1-V curvature-compensated CMOS bandgap reference, which utilizes the temperature-dependent currents generated from the parasitic NPN and PNP BJT devices in CMOS process, is presented. The new proposed sub-1-V curvature-compensated CMOS bandgap reference has been successfully verified in a standard 0.25-μm CMOS process. The experimental results have confirmed that, with the minimum supply voltage of 0.9 V, the output reference voltage at 536 mV has a temperature coefficient of 19.5 ppm/°C from 0 °C to 100 °C. With 0.9-V supply voltage, the measured power noise rejection ratio is -25.5 dB at 10 kHz.

In Chapter 3, the influence of gate-oxide reliability on common-source amplifiers with diode-connected active load is investigated with the non-stacked and stacked structures under analog application in a 130-nm low-voltage CMOS process. The test conditions of this work

include the DC stress, AC stress with DC offset, and large-signal transition stress under different frequencies and signals. After overstresses, the small-signal parameters, such as small-signal gain, unity-gain frequency, phase margin, and output DC voltage levels, are measured to verify the impact of gate-oxide reliability on circuit performances of the common-source amplifiers with diode-connected active load. The small-signal parameters of the common-source amplifier with the non-stacked diode-connected active load structure are stronger degraded than that with non-stacked diode-connected active load structure due to gate-oxide breakdown under analog and digital applications. The common-source amplifiers with diode-connected active load are not functional operation under digital application due to gate-oxide breakdown. The impact of soft and hard gate-oxide breakdowns on common-source amplifiers with non-stacked and stacked diode-connected active load structures has been analyzed and discussed. The hard breakdown has more serious impact to the common-source amplifiers with diode-connected active load. The effect of the MOSFET gate-oxide reliability on operational amplifier is investigated with the two-stage and folded-cascode structures in a 130-nm low-voltage CMOS process. The test operation conditions include unity-gain buffer (close-loop) and comparator (open-loop) configurations under the DC stress, AC stress with DC offset, and large-signal transition stress. After overstress, the small-signal parameters, such as small-signal gain, unity-gain frequency, and phase margin, are measured to verify the impact of gate-oxide reliability on circuit performances of the operational amplifier. The gate-oxide reliability in the operational amplifier can be improved by the stacked configuration under small-signal input and output application. A simple equivalent device model of gate-oxide reliability for CMOS devices in analog circuits is investigated and simulated.

In Chapter 4, the MOS switch with bootstrapped technique is widely used in low-voltage switched-capacitor circuit. The switched-capacitor circuit with the bootstrapped technique could be a dangerous design approach in the nano-scale CMOS process due to the gate-oxide transient overstress. The impact of gate-oxide transient overstress on MOS switch in switched-capacitor circuit is investigated with the sample-and-hold amplifier in a 130-nm CMOS process. After overstress on the MOS switch of SHA with open-loop configuration, the circuit performances in time domain and frequency domain are measured to verify the impact of gate-oxide reliability on circuit performances. The oxide breakdown on switch device will degrade the performance of bootstrapped switch technique.

In Chapter 5, the thin gate oxide causes the large gate tunneling leakage in nanoscale CMOS technology. In this work, the influence of MOS capacitor, as loop filter, with gate tunneling leakage on the circuit performances of phase locked loop (PLL) in nanoscale CMOS technology has been investigated and analyzed. The basic PLL with second-order loop filter is used to simulate the impact of gate tunneling leakage on performance degradation of PLL in a standard 90-nm CMOS process. The MOS capacitors with different oxide thicknesses are used to investigate this impact to PLL. The locked time, static phase error, and jitter of second-order PLL are degraded by the gate tunneling leakage of MOS capacitor in loop filter. Overview on the prior designs of gate tunneling leakage compensation technique to reduce the gate tunneling leakage on MOS capacitor as loop filter in PLL is provided in this work.

Chapter 6 presents a new proposed gate bias voltage generating technique with threshold-voltage compensation for analog circuits in the low-temperature polycrystalline silicon LTPS thin-film transistors (TFTs). The new proposed gate bias voltage generating circuit with threshold-voltage compensation has been successfully verified in a 8-μm LTPS process. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under biasing voltage of 3 V. The new proposed gate bias voltage generating technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented by LTPS process on glass substrate for active matrix LCD (AMLCD) panel.

Chapter 7 summarizes the main results of this dissertation. Then, some suggestions for the future works are also addressed in this chapter.

Table 1.1

Key Features of the Semiconductor Scaling Trend

(High-Performance Logic Technology) [1]

Year/Process	2007	2008	2009	2010	2011	2012	2013	90 nm	65 nm
Gate Length, L (nm)	25	22	20	18	16	14	13	100	60
Oxide Thickness, t_{ox} (Å)	11	10	9	6.5	5	5		23.3	20
Power Supply Voltage, V_{DD} (V)	1.1	1	1	1	1	0.9	0.9	1	1
Threshold Voltage, V_{TH} (mV)	165	164	237	151	146	148		228	300
NMOS Drain Current (μA/μm)	1200	1210	1180	2050	2490	2300			

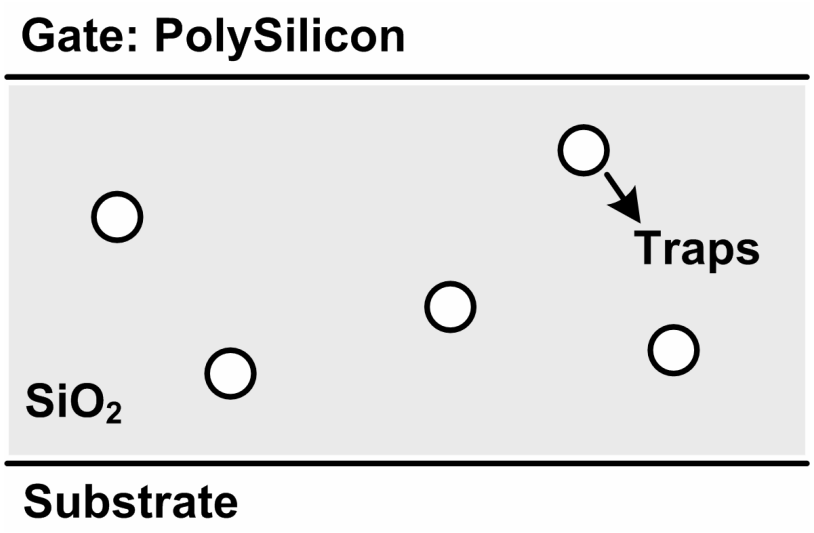


Fig. 1.1. Formation of traps in the gate oxide of MOS transistor.

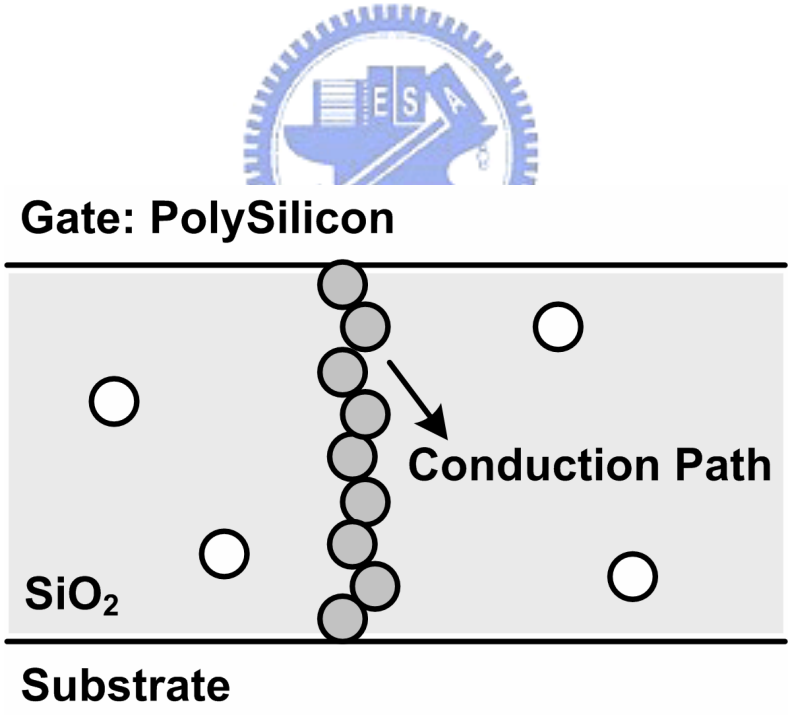


Fig. 1.2. Creation of conduction path through traps in the gate oxide of MOS transistor.

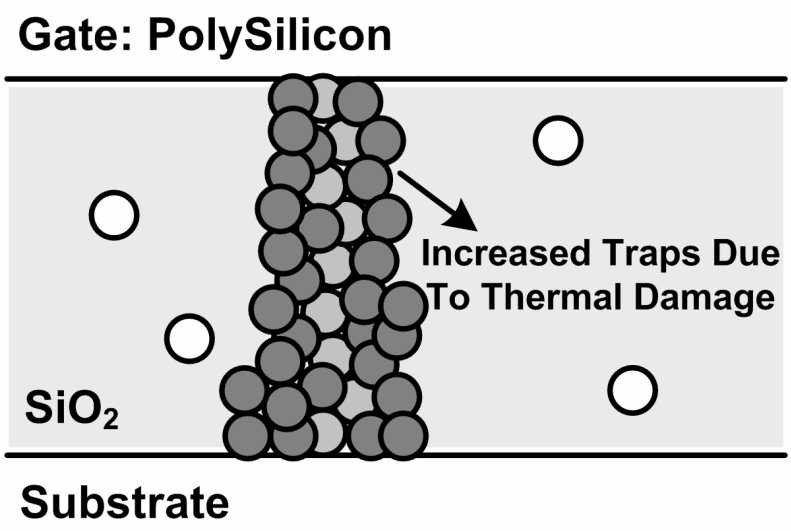


Fig. 1.3. Increased traps in gate oxide of MOS transistor after Conduction.

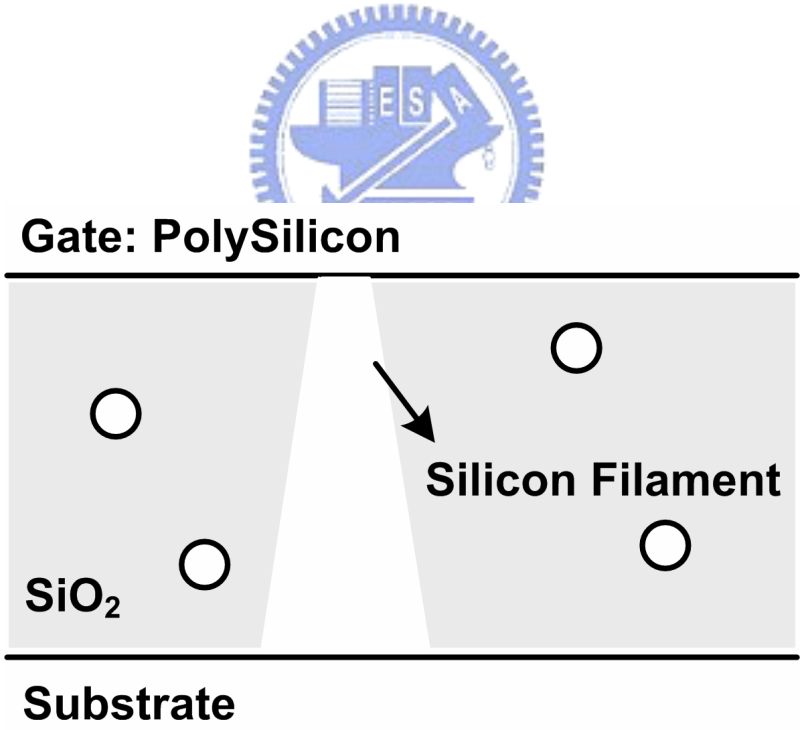


Fig. 1.4. Cross section of the gate oxide of MOS transistor after hard gate oxide breakdown.

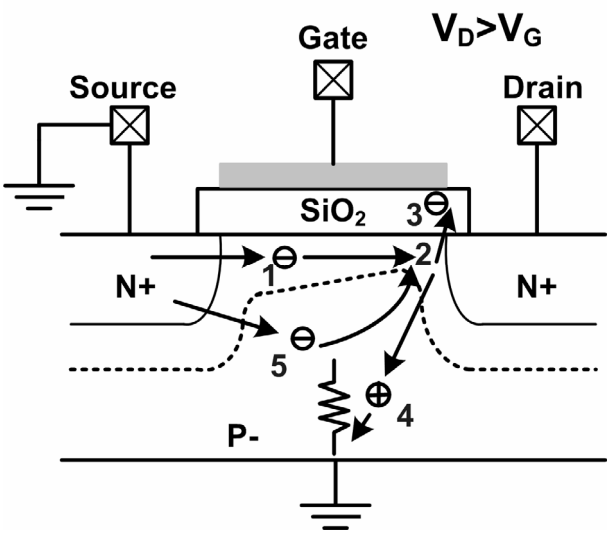


Fig. 1.5. Hot carrier injection in CMOS technology [17].

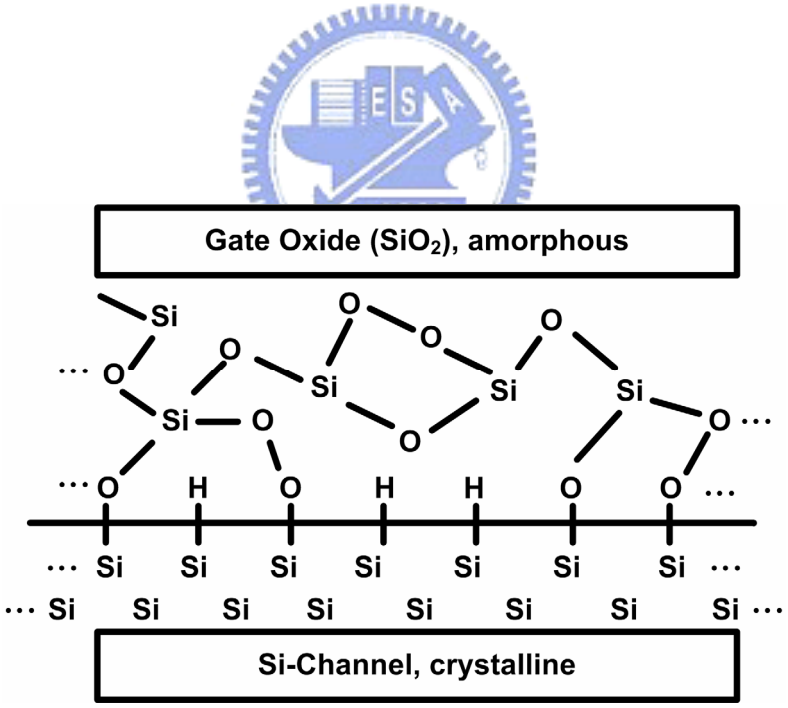


Fig. 1.6. Schematic of the Si/oxide interface of a MOSFET. The dangling Si bonds are present due to the mismatch between the ordered channel and amorphous oxide. These act as interface traps unless they are passivated by hydrogen annealing. NBTI induces the dissociation of the Si–H bonds causing hydrogen to diffuse away from the interface [24].

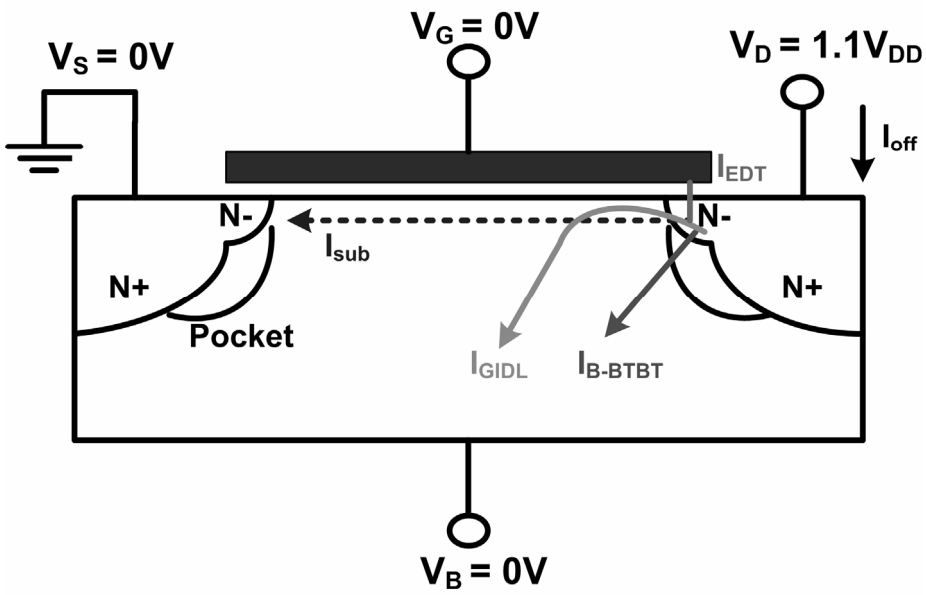


Fig. 1.7. The cross section of the NMOSFET structure and drain leakage components [28].

CHAPTER 2

CMOS Bandgap Reference Circuit With Sub-1-V Operation

In this chapter, two sub-1-V CMOS bandgap voltage references without using low-threshold-voltage device are presented. First, the new proposed sub-1-V bandgap reference with startup circuit has been successfully verified in a standard 0.25-μm CMOS process, where the occupied silicon area is only 177 μm × 106 μm. The experimental results have shown that, with the minimum supply voltage of 0.85 V, the output reference voltage is 238.2 mV at room temperature, and the temperature coefficient is 58.1 ppm/°C from -10 °C to 120 °C without laser trimming. Under the supply voltage of 0.85 V, the average power supply rejection ratio (PSRR) is -33.2 dB at 10 kHz. Second, a new sub-1-V curvature-compensated CMOS bandgap reference, which utilizes the temperature-dependent currents generated from the parasitic NPN and PNP BJT devices in CMOS process, is presented. The new proposed sub-1-V curvature-compensated CMOS bandgap reference has been successfully verified in a standard 0.25-μm CMOS process. The experimental results have confirmed that, with the minimum supply voltage of 0.9 V, the output reference voltage at 536 mV has a temperature coefficient of 19.5 ppm/°C from 0 °C to 100 °C. With 0.9-V supply voltage, the measured power noise rejection ratio is -25.5 dB at 10 kHz.

2.1. CMOS Bandgap Reference Circuit for Sub-1-V Operation Without Extra Low-Threshold-Voltage Device

2.1.1. Background

Low voltage and low power are two important design criteria in both analog and digital systems. It has been expected that the whole electronic system will be operated down to a single 1-V supply in near future. The bandgap reference (BGR) generators which can be operated under 1-V supply have been widely used in DRAM, flash memories, and analog-to-digital converter (ADC). So far, many techniques have been proposed to develop voltage or current references, which can be almost independent to temperature and power-supply voltage. The bandgap reference is the major design to provide a precision voltage reference with low sensitivity to the temperature and the supply voltage.

When CMOS technologies enter the nano-scale eras, the demand for battery-operated portable equipments will increase. The supply voltage has been scaled down from 1.8 V (in 0.18-μm technology) to 1.2 V (in 0.13-μm technology), and will drop to only 0.9 V in the next generation technology [53]. In CMOS technology, the parasitic vertical bipolar junction transistor (BJT) had been commonly used to implement P-N junction of the bandgap reference. But, the traditional CMOS bandgap reference circuits did not work in sub-1-V supply voltage. The reason, that the minimum supply voltage can not be lower than 1 V, is constrained by two factors. One is the bandgap voltage of around 1.25 V in silicon [54]-[63], which exceeds 1 V supply. The other factor is that the low-voltage design of the proportional to absolute temperature current generation loop is limited by the input common-mode voltage of the amplifier [54], [57]. These two limitations can be solved by using the resistive subdivision methods [55], [59], low-threshold voltage (or native) device [58]-[60], BiCMOS process [57], or DTMOST device [61]. However, those approaches often require specialized processes and characterization, which increase fabrication cost and process steps.

In this work, a new bandgap reference is proposed, which can be successfully operated with sub-1-V supply in a standard 0.25-μm CMOS process without special process technology [64]. Without laser trimming, the new proposed bandgap voltage reference has been proven in the silicon chip with a stable output voltage V_{REF} of 238.2 mV at room temperature and a temperature coefficient of 58.1 ppm/°C under VDD power supply of 0.85 V.

2.1.2. Traditional Bandgap Reference Circuit

A typical implementation of bandgap reference in CMOS technology is shown in Fig. 2.1. In this circuit, the output is the sum of a base-emitter voltage (V_{EB}) of BJT and the voltage drop across the upper resistor. The BJTs (Q_1 and Q_2) are typically implemented by the diode-connected vertical PNP bipolar junction transistors. The output voltage of the traditional bandgap reference circuit can be written as

$$V_{REF\text{-}TRAD} = V_{EB2} + \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right), \tag{2.1}$$

where A_1 and A_2 is the emitter areas of Q_1 and Q_2, and V_T is the thermal voltage. The second item in (2.1) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of V_{EB}. Usually, the V_{PTAT} voltage comes from the thermal voltage V_T with a temperature coefficient about + 0.085 mV/°C, which is quite smaller than that of V_{EB}. After multiplying V_{PTAT} with an appropriate factor and summing with V_{EB}, the bandgap reference will have a very low sensitivity to temperature. Hence, if a proper ratio of resistors is kept, an output voltage with very low sensitivity to temperature can be obtained. In general, the V_{REF} is about 1.25 V in CMOS process, so that the traditional bandgap reference circuit can not be operated in low voltage application, such as 1 V or below.

2.1.3. New Proposed Bandgap Reference Circuit

The design concept of the new proposed bandgap reference is that the two voltages (which are proportional to V_{EB} and $V_{T,}$ respectively) are generated from the same feedback loop. The two-stage operational amplifier with p-channel input is used in this new proposed bandgap reference. The p-channel input has a lower input common-mode voltage than that of the n-channel input to keep the transistors working in the saturation region.

The new proposed bandgap reference is shown in Fig. 2.2, which uses the resistive subdivision R_{1a}, R_{1b}, R_{2a}, and R_{2b} to reduce the input common-mode voltage of the amplifier. The voltages V_1 and V_2 in Fig. 2.2 have a negative temperature

coefficient as that of V_{EB}. In the traditional bandgap reference, the negative input of the operational amplifier is connected to V_{EB2}, whose value is varying from 0.65 V to 0.45 V when the temperature is changed from 0 °C to 100 °C. The minimum supply voltage (V_{DD}) of the traditional bandgap reference circuit needs $V_{EB2}+2|V_{DSsat}|+|V_{THp}|$. The V_{THp} is the threshold voltage of PMOS. The supply voltage of the traditional bandgap reference is more than 1 V. In Fig. 2.2, the dimensions of PMOS devices M_1 and M_2 are kept the same. The resistance of R_{1a} and R_{2a} is the same, and the resistance of R_{1b} and R_{2b} is also the same. Following the KCL at the nodes of V_1 and V_2 in Fig. 2.2, the node equation can be written as

$$\frac{\Delta V}{R_3} = \frac{V_{REF} - V_2}{R_4}, \tag{2.2}$$

$$\frac{\Delta V_{EB} - \Delta V}{R_{1a}} = \frac{\Delta V}{R_{1b}}, \tag{2.3}$$

where $\Delta V_{EB} = V_{EB2} - V_{EB1}$ and $\Delta V = V_2 - V_1$. According to the equations (2.2) and (2.3) reference voltage V_{REF} can be expressed as

$$V_{REF} = \frac{R_{1b}}{R_{1a}+R_{1b}}\left[\frac{\left(R_4 + \frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)}{R_3}\Delta V_{EB} + V_{EB2}\right]$$

$$= \frac{R_{1b}}{R_{1a}+R_{1b}}\left[V_{REF\text{-}TRAD} + \left(\frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)\frac{\Delta V_{EB}}{R_3}\right]. \tag{2.4}$$

The item of $V_{REF\text{-}TRAD}$ in (2.4) is identical to the traditional reference voltage in (2.1). In order to achieve sub-1-V operation, the ratio of R_{1b} / (R_{1a}+R_{1b}) is used to scale down the reference voltage level. Therefore, the minimum supply voltage of the new proposed bandgap reference can be effectively reduced to only

$$V_{DD(Min)} = V_2 + |V_{THp}| + 2|V_{DSsat}|. \tag{2.5}$$

The new proposed bandgap reference can be operated under sub-1-V supply voltage.

The whole complete circuit to realize the proposed sub-1-V bandgap reference is shown in Fig. 2.3. The circuit is composed of a bias circuit, a bandgap core, two

startup circuits, and a two-stage operational amplifier. The bandgap reference circuit has two stable points. To ensure that it ends up to the correct state, a startup circuit must be added. The startup circuit for the bias circuit is used to avoid the bias circuit working in the zero-current state, which is realized by M_{S1a}~M_{S3a} in Fig. 2.3 [55]. Similarly, another startup circuit is used to ensure that the input voltage of the amplifier is not kept at zero in the initial state. The M_{S1a} and M_{S2a} form a function of inverter in the startup circuit. The device dimensions (W/L) of M_{S2a} and M_{S2b} are chosen to be much less than one. When the circuit operates in zero-current state, the gate voltages of M_{S1a} and M_{S1b} are pulled high and close to V_{DD}. The drain voltages of M_{S2a} and M_{S2b} are pulled low to turn on the M_{S3a} and M_{S3b}, which inject current to the bandgap core circuitry (by M_{S3b}) and the bias circuit (by M_{S3a}). The drain voltages of M_{B3} and M_4 are decreased, therefore the bandgap core circuitry and bias circuit start to operate. Once the drain voltage of M_{B4} and the gate voltages of M_1, M_2, M_{A1}, and M_{A6} are decreased, the drain voltages of M_{S1a} and M_{S1b} are pulled high to cut off M_{S3a} and M_{S3b}. The device dimensions (W/L) of M_{S2a} and M_{S2b} are critical since the loop of the bandgap reference could be destroyed, if M_{S3a} or M_{S3b} were not completely cut off after startup. To ensure a complete cutoff operation of M_{S3a} and M_{S3b}, the device dimensions (W/L) of M_{S3a} and M_{S3b} should be designed with the considerations of both maximum supply voltage and operating temperature [55]. The capacitors C_1 and C_2 are used to stabilize the circuit. The bulk and the source of the input pair transistors M_{A2} and M_{A3} in the amplifier should be connected together to avoid the body effect.

In real-world applications, the power supply voltage is never perfect. It consists of a DC level plus AC noise caused by transient currents from circuit operations. Another important factor of the bandgap reference circuit operated in sub-1-V supply voltage is the power supply rejection ratio (PSRR) [65], which represents the resistance against the noise from the supply voltage in the unit of decibel (dB). The small-signal model of the proposed bandgap reference circuit with the operational amplifier of p-channel input is shown in Fig. 2.4, where only considers the noise from the supply voltage. The resistances of R_3' and R_4' in Fig. 2.4 are $R_3 + (R_{1a} // R_{1b})$ and $R_4 + (R_{2a} // R_{2b})$, respectively. The capacitor C is the parasitic drain-to-bulk junction capacitance of M_2. Since the turn-on resistance of the PNP transistors is small, both Q_1 and Q_2 can be simplified as short-circuit path to the ground. The

amplifier is modeled with an output resistor R_{out} and two voltage-controlled current sources i_d and i_{dd}, which are driven by the differential input voltage v_d and power supply voltage v_{dd}, respectively. The power supply rejection ratio (PSRR) of this new proposed bandgap reference circuit, which is the ratio of the output reference voltage and the noise from the supply voltage, can be expressed as

$$\frac{V_{REF}(s)}{V_{DD(Noise)}(s)} = \frac{1}{sCr_{o2} + \frac{r_{o2}}{R_4'} + 1}. \tag{2.6}$$

From (2.6), the PSRR of the proposed bandgap reference will become worse at high frequency. It is apparent that the pole location can be shifted by changing the capacitance at V_{REF} node. Moving the pole to the left in the s-plane will result in an improvement in high-frequency noise rejection. This can be achieved by inserting a capacitance C_p to ground at V_{REF} node. Thus, the PSRR in (2.6) is modified to

$$\frac{V_{REF}(s)}{V_{DD(Noise)}(s)} = \frac{1}{s(C+C_p)r_{o2} + \frac{r_{o2}}{R_4'} + 1}. \tag{2.7}$$

A larger C_p provides better stability, but the startup time will become longer. The pre-regulated circuit [73] also used to improve the PSRR of the bandgap circuit. However, minimum supply voltage is the tradeoff.

The operational amplifier in Fig. 2.3 under sub-1-V operation has a limited gain. Thus, there will be a nonzero input-referred offset voltage V_{OS}. Considering the offset voltage of V_{OS}, the V_{REF} in (2.4) including the offset voltage can be written as

$$V_{REF} = \frac{R_{1b}}{R_{1a}+R_{1b}}\left[\frac{\left(R_4 + \frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)}{R_3}\Delta V_{EB} + V_{BE2}\right] - \frac{R_4}{R_3}V_{OS}. \tag{2.8}$$

The offset voltage, V_{OS}, is a temperature dependent voltage. To reduce the impact of V_{OS} on V_{REF}, the ratio of R_4 / R_3 should be designed as small as possible. The resistor ratio can be fabricated by CMOS technology with a very good percent.

2.1.4. Simulation and Experimental Results

2.1.4.1. Simulation Results

The proposed bandgap reference circuit has been simulated by varying its operating temperature from 0 to 100 °C. The dependence of V_{REF} (output reference voltage) on the operating temperature is shown in Fig. 2.5 under difference power supply voltage (from 0.8 to 1.1 V). The temperature coefficient is around 75 ppm/°C with the supply voltage of 0.85 V. With supply voltage of 0.8 V, the temperature coefficient grows sharply to be above 200 ppm/°C. The dependence of V_{REF} on the supply voltage is shown in Fig. 2.6 under the temperatures of 0, 25, and 100 °C. The curves of output reference voltages under the temperatures of 0, 25, and 100 °C grow together while the supply voltage of the proposed bandgap reference is above 0.85 V. This means that the minimum supply voltage for the new proposed bandgap reference can be as low as 0.85 V. The PSRR at low frequency of the proposed bandgap reference, which works in the low supply voltage of 0.85 V, is - 30.2 dB.

2.1.4.2. Silicon Verification

The proposed bandgap reference circuit has been fabricated in a 0.25-μm single-ploy-five-metal (1P5M) CMOS process. Fig. 2.7 shows the overall die photo of the new sub-1-V bandgap reference circuit. The occupied silicon area of the new proposed bandgap reference circuit is only 177 μm × 106 μm. The active devices (MOSFETs) have been drawn in a common centroid layout to reduce process mismatch effect. The bipolar transistors in this chip are the parasitic vertical PNP BJTs in CMOS process. The ratio between the emitter areas of Q_1 and Q_2 is 8. The total emitter area of Q_1 is 200 μm^2 and that of Q2 is 25 μm^2 in the layout. The resistors in this chip are formed by salicided ploy resistors, which have minimum process variation to improve the accuracy of resistance ratio. The bandgap reference circuit has been measured by varying its operating temperature from -10 to 120 °C. The power supply voltage was set from 0.8 to 1.2 V. The measured data is measured by Agilent 4156. The measured results are shown in Fig. 2.8. The measured

temperature coefficient of the new proposed bandgap reference circuit is around 58.1 ppm/°C under the supply voltage of 0.85 V. The dependence of output reference voltage on the V_{DD} supply voltage under different temperatures is shown in Fig. 2.9. The experimental results in Fig. 2.9 have confirmed that the minimum supply voltage for this sub-1-V bandgap reference is 0.85 V.

About the measurement setup for power supply rejection ratio (PSRR), a sinusoidal ripple is added on power supply to measure the small-signal gain between the supply voltage and output reference voltage. The AC input signal at the power supply pin must include a DC offset that corresponds to the normal power supply voltage so that the bandgap reference circuit remains powered up [67]. The dependence of measured PSRR on the frequency under different input sinusoidal amplitudes is shown in Fig. 2.10. The averaged power supply rejection ratio (PSRR) is - 33.8 dB at 10 kHz, whereas the reference output voltage is 238.2 mV at 25 °C under the V_{DD} power supply of 0.85 V. The comparison among the proposed sub-1-V bandgap reference of this work with other prior-art low voltage bandgap references is summarized in Table 1. The new proposed bandgap reference has the advantages of low operating voltage and low temperature coefficient in the general standard CMOS technology without special low-threshold-voltage device.

2.1.5. Summary

A CMOS bandgap voltage reference with V_{REF} of 238.2 mV and temperature coefficient of 58.1 ppm/°C, which consumes a maximum current of 28 μA at 0.85 V supply, has been presented. The sub-1-V operation of the bandgap reference has been successfully achieved in this work without using the low-threshold-voltage devices. Moreover, other techniques to achieve sub-1-V operation have been described, such as low voltage startup circuit and the lower common-mode input range of the amplifier by using the resistive subdivision method. Without using low-threshold-voltage device, the proposed bandgap reference circuit can be implemented in general CMOS technology. In order to improve the impact of process variation on performances of new proposed sub-1-V bandgap voltage reference, the resistor with trimming network should be added into the proposed bandgap reference circuit.

2.2. Curvature-Compensation Technique for CMOS Bandgap Reference Circuit With Sub-1-VOperation

2.2.1. Background

Reference circuits are the basic building blocks in many applications from pure analog, mixed-mode, to memory circuits. The demand for low-voltage operation is especially apparent in the battery-operated mobile products, such as cellular phones, PDA, camera recorders, and laptops [54].

In CMOS technology, the parasitic vertical bipolar junction transistors (BJT) have been used in high-precision bandgap voltage references. The conventional CMOS bandgap references did not work with sub-1-V supply voltage. The reason, why the minimum supply voltage can not be lower than 1 V, is constrained by two factors. One is due to the bandgap voltage of silicon around 1.25 V [55], [57], which exceeds 1-V supply. The other is that the low-voltage design of the proportional to absolute temperature current generation loop is limited by the input common-mode voltage of the amplifier [55], [57]. These two limitations can be solved by using the resistive subdivision methods [55], [59], low-threshold voltage (or native) device [58]-[60], BiCMOS process [57], or DTMOST device [61]. However, the bandgap reference working with low supply voltage often has a higher temperature coefficient than that of traditional bandgap reference. This has resulted in the development of new temperature compensated techniques, such as quadratic temperature compensation [68], exponential temperature compensation [69], piecewise-linear curvature correction [62], [70], and resistor temperature compensation [71], [72]. To implement those advanced mathematical functions with high accuracy, the development of the low-voltage bandgap structure requires precision matching of current mirrors or a pre-regulated supply voltage. Cascode current mirror [62], [68] and pre-regulated circuit [73] are good methods to solve this problem, but the minimum supply voltage is the tradeoff to use such methods.

In this work, a new sub-1-V curvature-compensated CMOS bandgap reference is proposed to be successfully operated with sub-1-V supply in a standard 0.25- m

CMOS process. The new proposed sub-1-V curvature-compensated bandgap voltage reference with a stable output voltage V_{REF} of 536 mV and temperature coefficient of 19.5 ppm/°C under supply voltage of 0.9 V has been verified in the silicon chip [74].

2.2.2. Non-Linearity Term of Traditional Bandgap Reference Circuit

The typical implementation of traditional bandgap voltage reference in CMOS technology is shown in Fig. 2.1. In this circuit, the output reference voltage is the sum of a base-emitter voltage (V_{BE}) of BJT and the voltage drop across the upper resistance (R_2). The BJTs (Q_1 and Q_2) are typically implemented by the diode-connected vertical PNP bipolar junction transistors. The output reference voltage of the traditional bandgap voltage reference circuit can be written as

$$V_{REF\text{-}TRAD} = \left|V_{BE2}\right| + \frac{R_2}{R_1}\frac{kT}{q}\ln\left(N\right), \tag{2.9}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), q is electronic charge (1.6×10^{-19} C), and N is the emitter area ratio of BJTs. The second item in equation (2.9) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of V_{BE}. Usually, the proportional to the absolute temperature voltage (V_{PTAT}) comes from the thermal voltage (kT/q) with a temperature coefficient about + 0.085 mV/°C which is quite smaller than that of V_{EB}. After multiplying V_{PTAT} with an appropriate factor and summing with V_{BE}, the bandgap voltage reference will have a low sensitivity to temperature variation. However, the relationship between V_{BE} of BJT and temperature is a non-linear property. That can be expressed by [75]

$$V_{BE} = V_G(T_0) + \frac{T}{T_0}\left[V_{BE}(T_0) - V_G(T_0)\right] - (\eta - m)\frac{kT}{q}\ln(\frac{T}{T_0}), \tag{2.10}$$

where V_G is the bandgap voltage of silicon extrapolated at 0 K, T is the absolute temperature in degrees Kelvin (^oK), η is a temperature constant depending on technology, m is the order of the temperature dependence of the collector current, and T_0 is the reference temperature. In equation (2), the term of $Tln(T/T_0)$ is the nonlinear temperature-dependence factor to V_{BE}. When equation (2.10) is expanded by Taylor

series, it can be represented by [75]

$$V_{BE} = a_0 + a_1 T + a_2 T^2 + ... + a_n T^n , \tag{2.11}$$

where a_0, a_1, ..., and a_n are the corresponding coefficients. The relationship between nonlinear temperature-dependence V_{BE} and linear temperature-dependence V_{PTAT} on the output reference voltage of bnadgap reference is shown in Fig. 2.11. The first-order temperature compensation involves the cancellation of the T term by using the V_{PTAT}, but the high-order temperature-dependence factor can not be compensated with V_{PTAT} in the traditional bandgap voltage reference. Therefore, the traditional bandgap voltage reference working in low supply voltage has a higher temperature coefficient.

2.2.3. Sub-1-V Bandgap Reference Circuit With Curvature-Compensated Technique

2.2.3.1. Design Concept

The proposed bandgap voltage reference with new curvature- compensation technique is illustrated in Fig. 2.12. There are two types of bandgap voltage reference circuits in standard CMOS process. The first type uses the parasitic vertical PNP BJTs to realize the badgap voltage reference circuit, which has been widely used in many integrated circuits. The second type is realized with parasitic vertical NPN BJTs. The parasitic vertical NPN BJT in standard CMOS process is implemented with deep N-well structure. Thus, there is no extra cost to have NPN parasitic transistor. The cross-sectional view of parasitic vertical NPN BJT in CMOS process is shown in Fig. 2.13. The emitter, base, and collector of parasitic vertical NPN BJT are realized by the N+ diffusion, P-well, and deep N-well layers, respectively.

The new proposed curvature-compensation technique has two output reference currents, I_{REF1} and I_{REF2}, which are formed by two bandgap voltage references. The current I_{REF1} comes from a bandgap voltage reference with PNP BJTs, whereas the I_{REF2} is produced by another bandgap voltage reference with NPN BJTs. The output reference currents act with concave-up shapes in the temperature range from 0 to 100

°C, which are designed with the same center temperature (T_0) where the temperature coefficient of I_{REF1} and I_{REF2} is zero. Through the current mirrors, a temperature-independence current generated from the difference between I_{REF1} and I_{REF2} can be produced to compensate the high-order temperature-dependence factor of V_{BE}.

In Fig. 2.12, an output reference voltage V_{REF} with very low sensitivity to temperature can be obtained across the resistance R_{REF}. Thus, the new proposed curvature-compensated bandgap voltage reference has the excellent curvature-compensated result with low-voltage operation.

2.2.3.2. Circuit Implementation

The whole complete circuit to realize the new proposed sub-1-V curvature-compensated CMOS bandgap voltage reference is shown in Fig. 2.14. The new proposed sub-1-V curvature-compensated bandgap voltage reference is composed by two sub-1-V bandgap cores [55] with two operational amplifiers, which are designed with the two-stage structure. The startup circuit for the self-bias circuit is used to avoid the circuit working in the zero-current state, which is realized by M_{SN1}~M_{SN3} (M_{SP1}~M_{SP3}) for bandgap reference with NPN (PNP) BJTs. The M_{SN1}~M_{SN2} and M_{SP1}~M_{SP2} form the functions of inverter in the startup circuits. The device dimensions (W/L) of M_{SN1} and M_{SP2} are chosen to be much less than one, respectively. To ensure a complete cutoff operation of M_{SN3} and M_{SP3}, the device dimensions (W/L) of M_{SN3} and M_{SP3} should be designed with the considerations of both maximum supply voltage and operating temperature [55]. The low-voltage operational amplifiers also need the startup circuit to avoid the zero-current state. The same startup circuits in Fig. 2.14 also use in the low-voltage operational amplifiers with two-stage structure. The current I_{REF1} in Fig. 2.14 is produced by a sub-1-V bandgap voltage reference with PNP BJTs and a p-channel input pair of operational amplifier. The I_{REF1} can be expressed as

$$I_{REF1} = \frac{\left|V_{BE\_PNP}\right|}{R_{1\_PNP}} + \frac{1}{R_{3\_PNP}} \frac{kT}{q} \ln N_{PNP}, \tag{2.12}$$

where R_{1_PNP} is set to $R_{1a\_PNP} + R_{1b\_PNP}$ (or $R_{2a\_PNP} + R_{2b\_PNP}$), $R_{1a\_PNP} = R_{2a\_PNP}$, and $R_{1b\_PNP} = R_{2b\_PNP}$. The current I_{REF2} is produced by another sub-1-V bandgap voltage reference with NPN BJTs and an n-channel input pair of operational amplifier. Similarly, I_{REF2} can be expressed as

$$I_{REF2} = \frac{V_{BE\_NPN}}{R_{1\_NPN}} + \frac{1}{R_{3\_NPN}} \frac{kT}{q} \ln N_{NPN}, \tag{2.13}$$

where R_{1_NPN} is set to $R_{1a\_NPN} + R_{1b\_NPN}$ (or $R_{2a\_NPN} + R_{2b\_NPN}$), $R_{1a\_NPN} = R_{2a\_NPN}$, and $R_{1b\_NPN} = R_{2b\_NPN}$. Through the current mirrors, the difference current, I_{REF}, between the I_{REF1} and I_{REF2} can be written as

$$\begin{aligned} I_{REF} &= K_2 I_{REF2} - K_1 I_{REF1} \\ &= \left(\frac{K_2 V_{BE\_NPN}}{R_{1\_NPN}} - \frac{K_1 \left|V_{BE\_PNP}\right|}{R_{1\_PNP}}\right) + \frac{kT}{q}\left(\frac{K_2 \ln N_{NPN}}{R_{3\_NPN}} - \frac{K_1 \ln N_{PNP}}{R_{3\_PNP}}\right), \end{aligned} \tag{2.14}$$

where K_1 is the device ratio of M_{4_PNP} and M_{5_PNP}, and K_2 is the device ratio of M_{4_NPN} and M_{5_NPN}. If the lnN_{NPN} and lnN_{PNP} have the same value and proper pairs of R_{1_NPN}, R_{1_PNP}, R_{3_NPN}, R_{3_PNP}, K_1, and K_2 are chosen, the difference current (I_{REF}) will ideally become a temperature-independence current. Therefore, a temperature-independence voltage can be achieved across R_{REF}, which has the lower temperature coefficient. The output reference voltage can be expressed as

$$\begin{aligned} V_{REF} &= R_{REF}(K_2 I_{REF2} - K_1 I_{REF1}) \\ &= R_{REF}\left[\begin{array}{l} \left(\dfrac{K_2 V_{BE\_NPN}}{R_{1\_NPN}} - \dfrac{K_1 \left|V_{BE\_PNP}\right|}{R_{1\_PNP}}\right) \\ + \dfrac{kT}{q}\left(\dfrac{K_2 \ln N_{NPN}}{R_{3\_NPN}} - \dfrac{K_1 \ln N_{PNP}}{R_{3\_PNP}}\right) \end{array}\right]. \end{aligned} \tag{2.15}$$

Thus, the new proposed sub-1-V bandgap voltage reference with new curvature-compensated technique has the excellent curvature-compensated result.

The minimum supply voltage of the new proposed sub-1-V curvature-compensated bandgap voltage reference can be expressed by

$$V_{DD(Min.)} = Max\left[\begin{array}{l}\left(\dfrac{R_{1b\_PNP}}{R_{1a\_PNP}+R_{1b\_PNP}}\left|V_{BE\_PNP}\right|+\left|V_{THP}\right|+2\left|V_{DSsat}\right|\right),\\ \left(\dfrac{R_{2b\_NPN}}{R_{1a\_NPN}+R_{1b\_NPN}}V_{BE\_NPN}-V_{THN}+2V_{DSsat}\right)\end{array}\right], \qquad (2.16)$$

where V_{THP} and V_{THN} are threshold voltages of the PMOS and NMOS transistors, respectively. Since the base-emitter voltages (V_{BE_NPN} and V_{BE_PNP}) of the bipolar transistors in equation (2.16) are multiplied by the resistance subdivision, this circuit can be operated with sub-1-V supply voltage.

Because the operational amplifier of the bandgap voltage reference is not ideal, the offset voltage (V_{OS}) of operational amplifier will increase error on output reference voltage of bandgap voltage reference. The bnadgap voltage reference in CMOS technology suffers from the effect of MOS transistor due to the mismatch of transistor dimensions and threshold voltage. In new proposed sub-1-V curvature-compensated CMOS bandgap voltage reference, the relationship between output reference voltage and offset voltage (V_{OS}) of the operational amplifier can be rewritten by

$$\begin{aligned} V_{REF} &= R_{REF}(K_2 I_{REF2} - K_1 I_{REF1}) \\ &= R_{REF}\left[\begin{array}{l}\left(\dfrac{K_2}{R_{1\_NPN}}V_{BE\_NPN}-\dfrac{K_1}{R_{1\_PNP}}\left|V_{BE\_PNP}\right|\right)\\ +\dfrac{kT}{q}\left(\dfrac{K_2\ln N_{NPN}}{R_{3\_NPN}}-\dfrac{K_1\ln N_{PNP}}{R_{3\_PNP}}\right)+\\ \dfrac{K_2R_{1\_NPN}}{R_{1b\_NPN}}V_{OSN}-\dfrac{K_1R_{1\_PNP}}{R_{1b\_PNP}}V_{OSP})\end{array}\right], \end{aligned} \qquad (2.17)$$

where V_{OSN} and V_{OSP} are the offset voltage of the operational amplifiers with n-channel and p-channel input pairs, respectively. The effect of the V_{OSN} and V_{OSP} is amplified by the resistance ratio of $K_2R_{1\_NPN} / R_{1b\_NPN}$ and $K_1R_{1\_PNP} / R_{1b\_PNP}$, respectively. However, this can be reduced by increasing the emitter areas ratio of the BJTs (N_{NPN} and N_{PNP}), and the required resistance ratio of $K_2R_{1\_NPN} / R_{1b\_NPN}$ and $K_1R_{1\_PNP} / R_{1b\_PNP}$ is reduced to minimize the negative impact from V_{OS} [72]. In operational amplifier, the systematic offset can be minimized by adjusting transistor dimensions and bias current in ratio, while the random offset can be reduced by symmetrical and compact layout.

2.2.4. Simulation and Experimental Results

2.2.4.1. Simulation Results

The bandgap voltage reference with new proposed curvature-compensated technique has been simulated during the operating temperature from 0 to 100 °C. The temperature coefficient of the bandgap voltage reference with new curvature-compensated technique is around 7.5 ppm/°C under the supply voltage of 1 V. The dependence of I_{REF} (output reference current) on the operating temperature from 0 to 100 °C is shown in Fig. 2.15 under the supply voltage of 1 V.

2.2.4.2. Silicon Measurement

The new proposed sub-1-V curvature-compensated bandgap voltage reference has been fabricated in a 0.25-μm CMOS technology. The proposed sub-1-V curvature-compensated bandgap voltage reference consists of the bandgap cores, bipolar transistors, and resistors. Fig. 2.16 shows the overall die photo of the new proposed sub-1-V curvature-compensated bandgap voltage reference. The occupied silicon area of the new proposed curvature-compensated bandgap voltage reference is only 480 μm × 226 μm. The active devices (MOSFETs) have been drawn in a common centroid layout to reduce process mismatch effect. The bipolar transistors in this chip are the parasitic vertical PNP BJTs and NPN BJTs. The ratio between the emitter areas of Q_{1_PNP} and Q_{2_PNP} (Q_{1_NPN} and Q_{2_NPN}) is 8. The total emitter area of Q_{1_PNP} (Q_{1_NPN}) is 200 μm^2 and that of Q_{2_PNP} (Q_{2_NPN}) is 25 μm^2 in the layout. The resistors in this chip are formed by un-salicided P+ ploy resistances, which have minimum process variation and temperature coefficient in the given foundry's CMOS process, to improve the accuracy of resistance ratio. The bandgap voltage reference has been measured with the operating temperature varying from 0 to 100 °C. The power supply voltage was set from 0.85 to 1.2 V. The measured results are shown in Fig. 2.17. The measured data is measured by Agilent 4156. The temperature coefficient is around 13.4 ppm/°C with the supply voltage at 1 V. The experimental results in Fig. 2.18 have confirmed that the minimum supply voltage for the new proposed sub-1-V curvature-compensated bandgap voltage reference is 0.9 V with

temperature coefficient of 19.5 ppm/°C.

About the measurement setup for power supply rejection ratio (*PSRR*), a signal with sinusoidal ripple is added on power supply to measure the small-signal gain between the supply voltage and output reference voltage. The AC input signal at the power supply pin must include a DC offset of the normal power supply voltage, so that the bandgap voltage reference circuit remains powered up [67]. The averaged measured power supply rejection ratio (*PSRR*) is - 25.5 dB at 10 kHz, whereas the reference output voltage is 536 mV at 25 °C under the supply voltage of 0.9 V. The comparison among the proposed sub-1-V curvature-compensation bandgap voltage reference of this work with other prior-art curvature- compensation bandgap voltage references is summarized in Table 2.2. From this table, the exponential temperature compensation [69] and piecewise-linear curvature correction [62], [70] are realized by BiCMOS and BJT processes, respectively. The resistor temperature compensation [72] in CMOS process requires a higher supply voltage to realize it. Those prior arts [62], [69], [70], [72] shown with very low temperature coefficients were achieved by trimming after silicon fabrication. In this work, the new proposed sub-1-V curvature-compensated bandgap voltage reference can achieve a low enough temperature coefficient without trimming in the general CMOS technology.

2.2.5. Summary

A new proposed sub-1-V curvature-compensated bandgap voltage reference with V_{REF} of 536 mV and temperature coefficient of 19.5 ppm/°C under supply voltage of 0.9 V was presented, which consumes a maximum current of 50 μA at 0.9 V. The sub-1-V operation of the curvature-compensated bandgap voltage reference has been successfully verified in silicon. The new proposed curvature-compensated technique used to improve the temperature coefficient of sub-1-V bandgap voltage reference can be implemented in general CMOS technology. In order to improve the impact of process variation on performances of new proposed sub-1-V curvature-compensated bandgap voltage reference, the resistor with trimming network should be added into the proposed bandgap reference circuit.

2.3. Conclusion

Chapter 2 has presented a new sub-1-V and a new sub-1-V curvature-compensated CMOS bandgap references. The new sub-1-V CMOS bandgap voltage reference with V_{REF} of 238.2 mV and temperature coefficient of 58.1 ppm/°C, which consumes a maximum current of 28 μA at 0.85 V supply, has been presented. The sub-1-V operation of the bandgap reference has been successfully achieved in this work without using the low-threshold-voltage devices. Moreover, other techniques to achieve sub-1-V operation have been described, such as low voltage startup circuit and the lower common-mode input range of the amplifier by using the resistive subdivision method. Without using low-threshold-voltage device, the proposed bandgap reference circuit can be implemented in general CMOS technology. The new proposed sub-1-V curvature-compensated bandgap voltage reference with V_{REF} of 536 mV and temperature coefficient of 19.5 ppm/°C under supply voltage of 0.9 V was presented, which consumes a maximum current of 50 μA at 0.9 V. The sub-1-V operation of the curvature-compensated bandgap voltage reference has been successfully verified in silicon. The new proposed curvature-compensated technique used to improve the temperature coefficient of sub-1-V bandgap voltage reference can be implemented in general CMOS technology.

Table 2.1

Comparison among the Low Voltage Bandgap References

	This work	Ref. [54]	Ref. [55]	Ref. [59]
Technology (CMOS)	0.25 μm	1.2 μm	0.6 μm	0.4 μm
Minimum Supply Voltage	0.85 V	1.2 V	0.98 V	0.84 V
Temperature Coefficient	58.1 ppm/°C	100 ppm /°C	15 ppm /°C	59 ppm /°C
Die Size	0.018 mm^2	1 mm^2	NA	0.1 mm^2
Power Consumption	23.8 μW	0.6 mW	17.64 μW	NA
Extra Modification / Process	No	No	Laser Trimming	Native NMOS

Table 2.2

Comparison among the Curvature-Compensated Bandgap Voltage References

	This work	Ref. [62]	Ref. [69]	Ref. [70]	Ref. [72]
Technology	0.25-μm CMOS	2-μm BiCMOS	1.5-μm BiCMOS	BJT	0.6-μm CMOS
$VDD_{(min)}$	0.9 V (1 V)	1.1 V	5 V	1 V	2 V
Temperature Range	0 ~ 100 ˚C	-15 ~ 90 ˚C	-55 ~ 125 ˚C	0 ~ 125 ˚C	0 ~ 100 ˚C
Temperature Coefficient	Without Trimming 19.5 ppm/˚C (13.4 ppm/˚C)	After Trimming ≅ 20 ppm/˚C	After Trimming 8.9 ppm/˚C	After Trimming 4 ppm/˚C	After Trimming 5.3 ppm/˚C

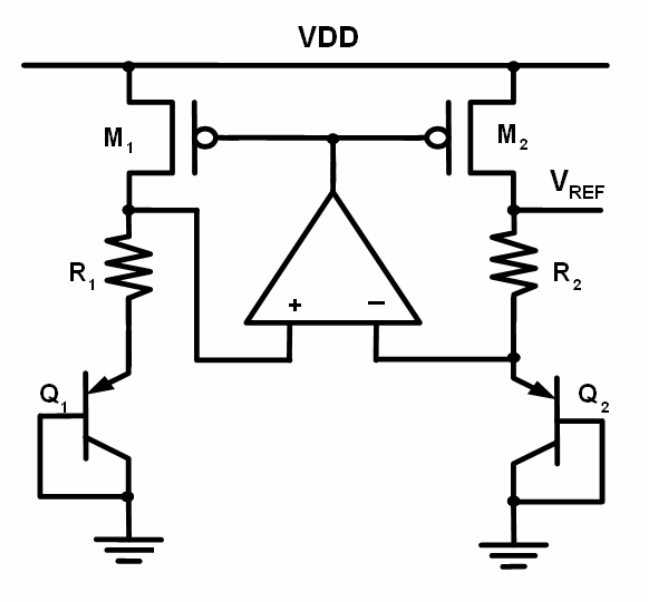


Fig. 2.1. The traditional bandgap reference circuit in CMOS technology.

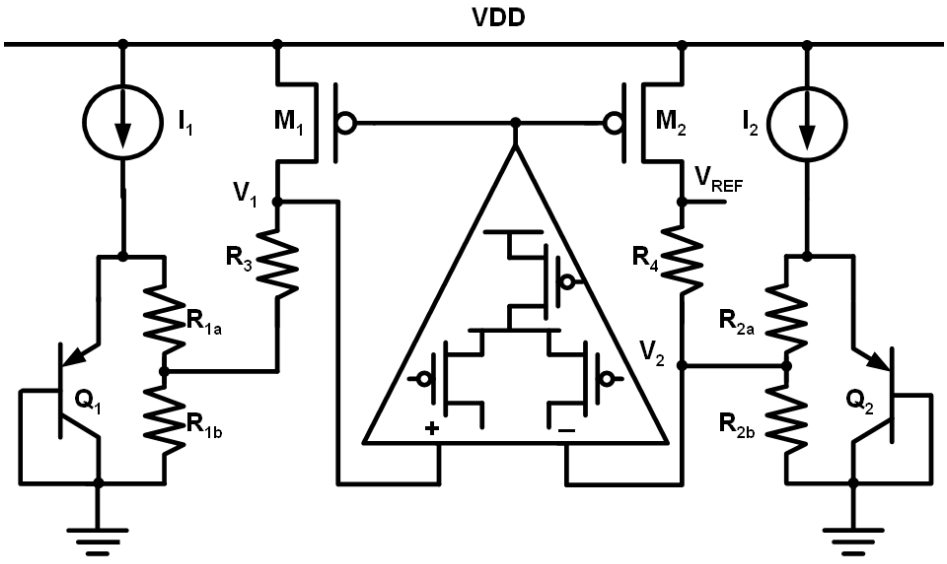


Fig. 2.2. The new proposed bandgap reference circuit for sub-1-V operation.

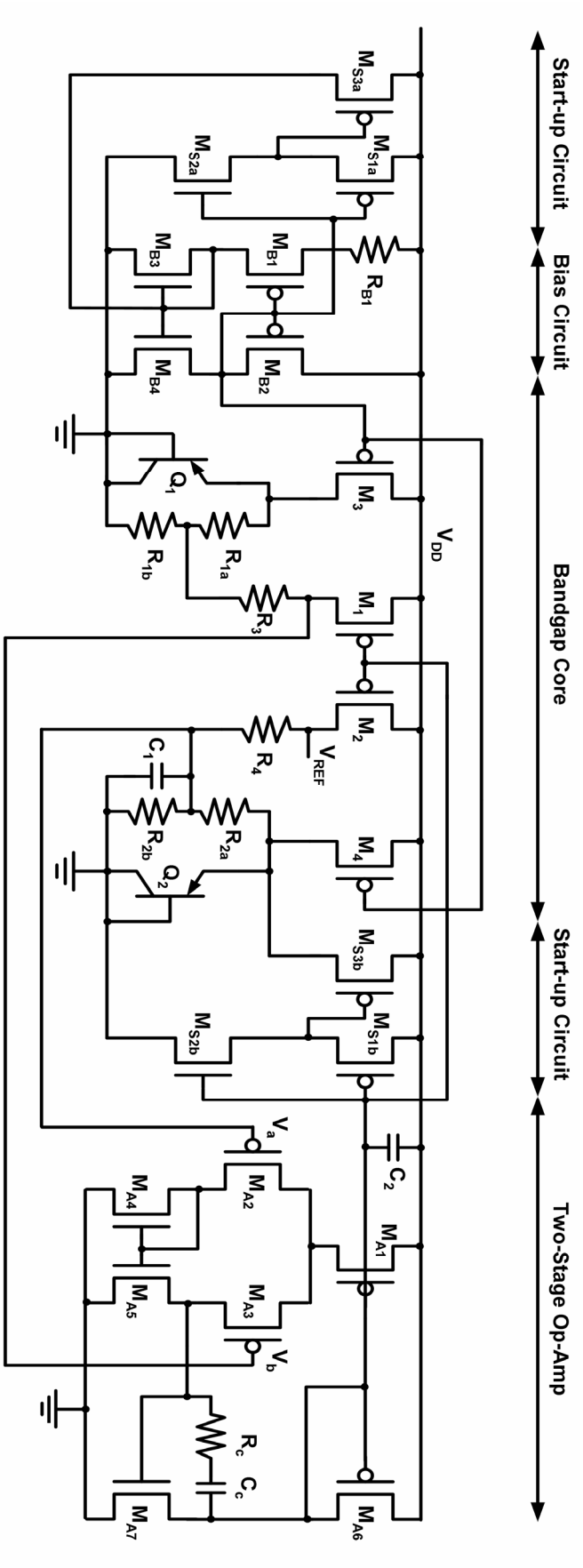


Fig. 2.3. Complete schematic of the new proposed bandgap reference.

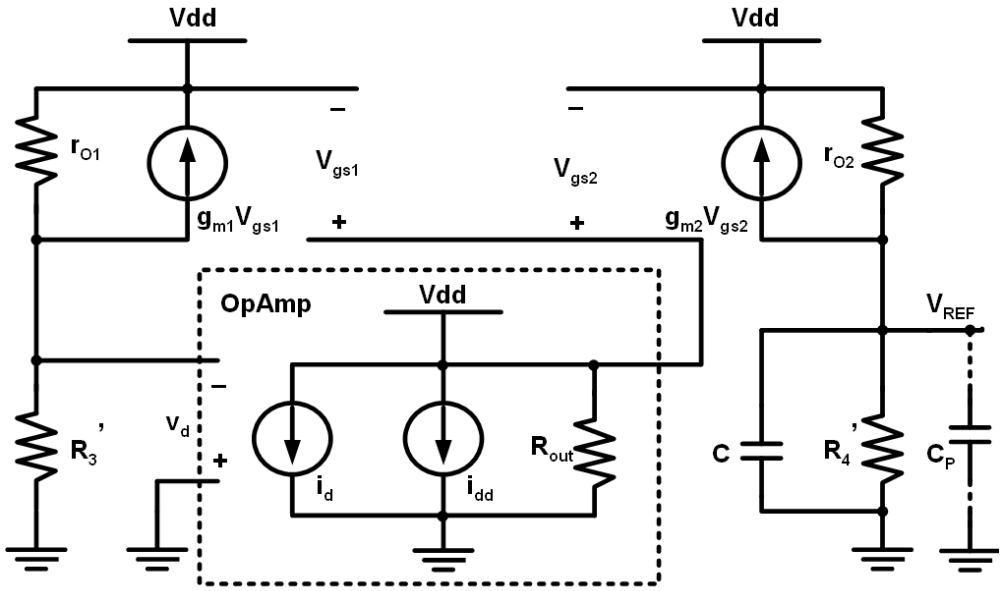


Fig. 2.4. Small signal model of the proposed bandgap reference.

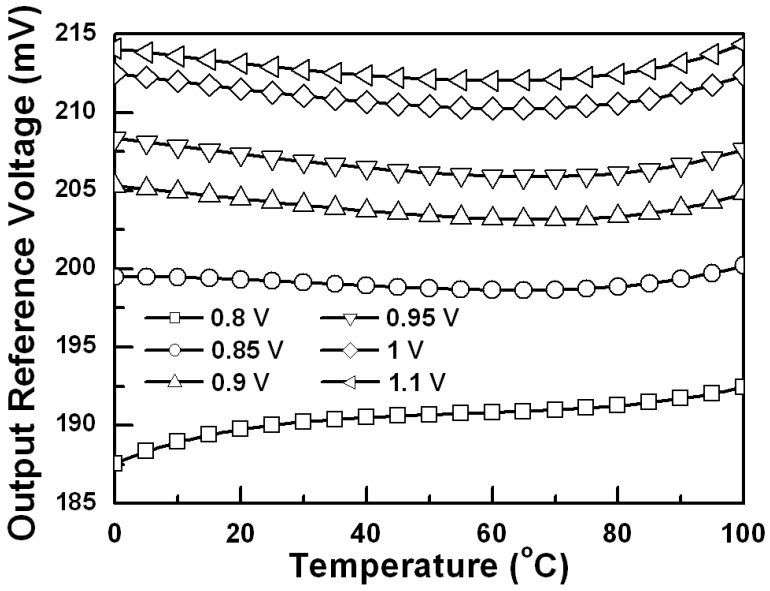


Fig. 2.5. Simulated reference voltage of the proposed bandgap reference with different supply voltages.

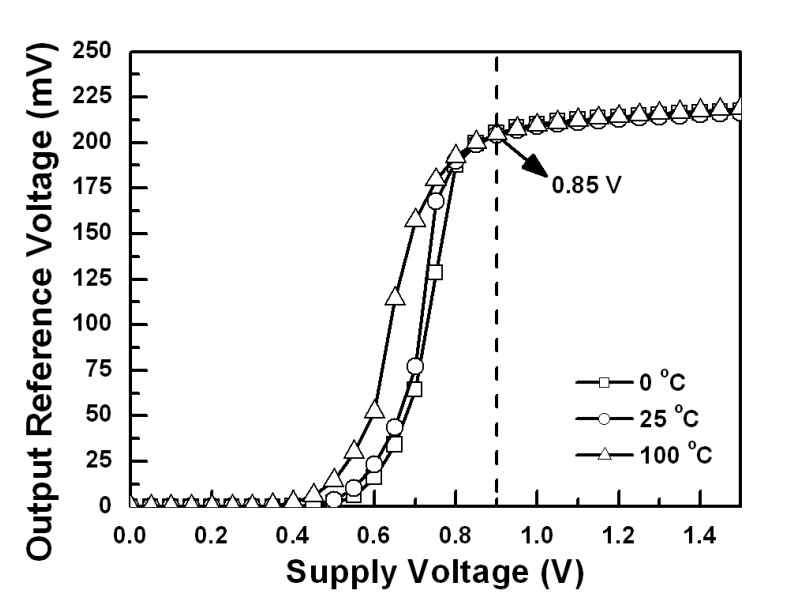


Fig. 2.6. Simulated minimum supply voltage of the proposed bandgap reference.

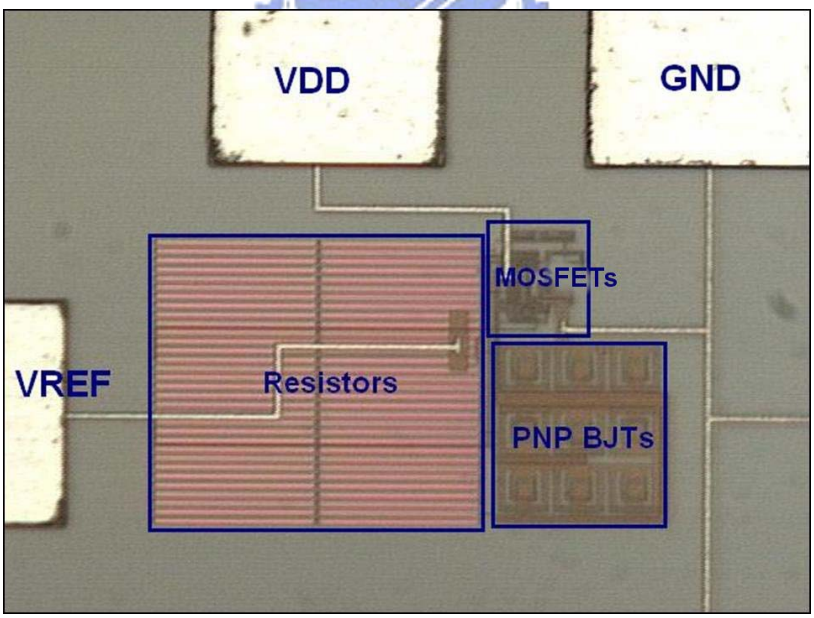


Fig. 2.7. Die photo of the new proposed bandgap reference circuit fabricated in a 0.25-μm CMOS process.

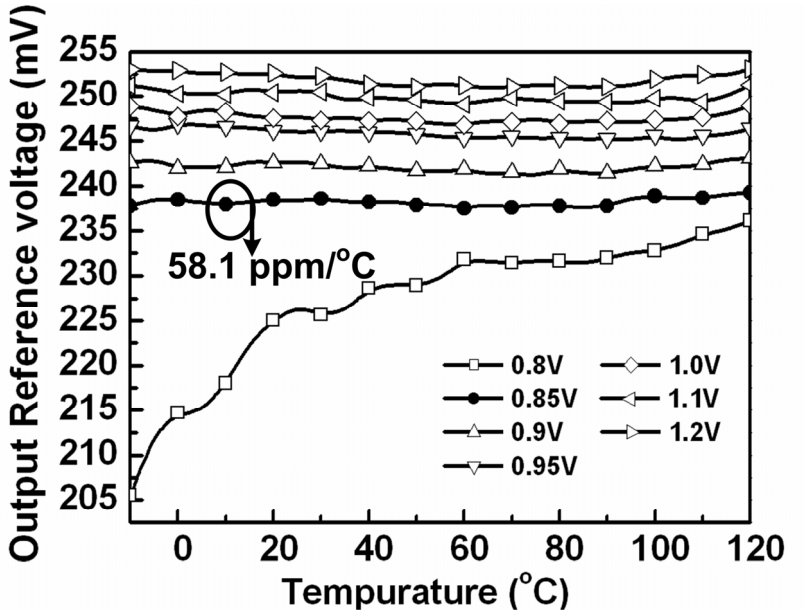


Fig. 2.8. Dependence of output reference voltage on the temperature under different VDD voltage levels.

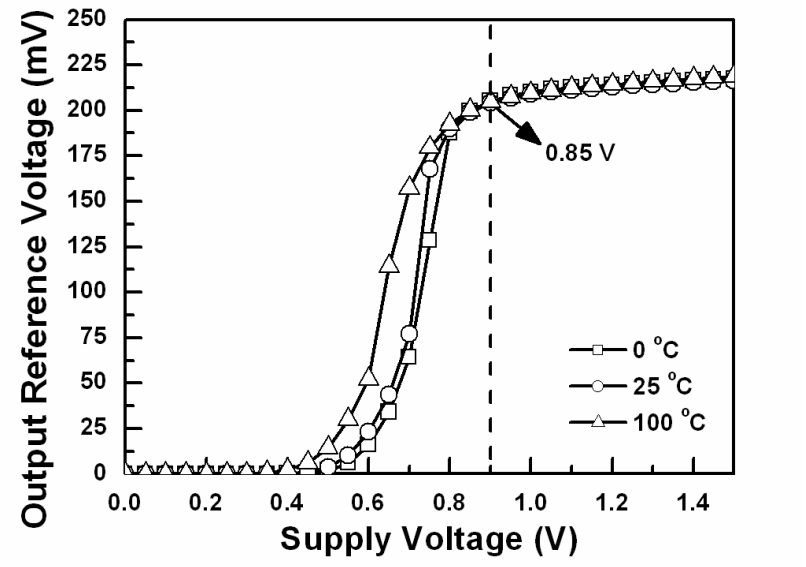


Fig. 2.9. Dependence of output reference voltage on the VDD supply voltage under different temperatures.

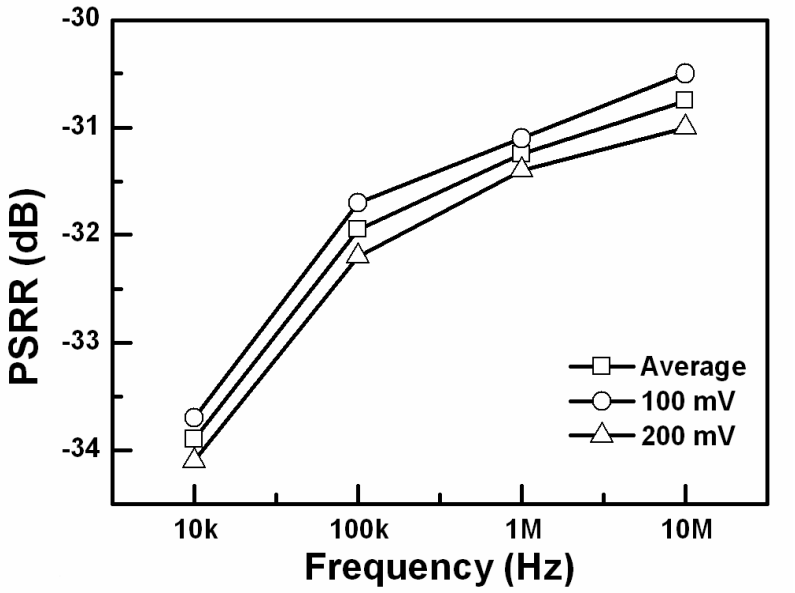


Fig. 2.10. Dependence of PSRR on the frequency under different input sinusoidal amplitudes.

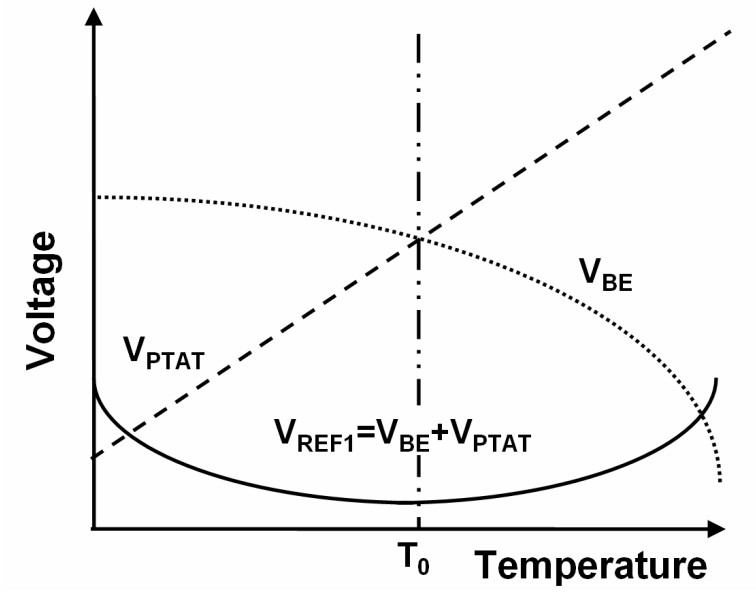


Fig. 2.11. The relationship between nonlinear temperature-dependence V_{BE} and linear temperaturedependence V_{PTAT} on the output reference voltage of bnadgap voltage reference circuit. The multiplying V_{PTAT} with K_{factor} is used to compensate the V_{BE}.

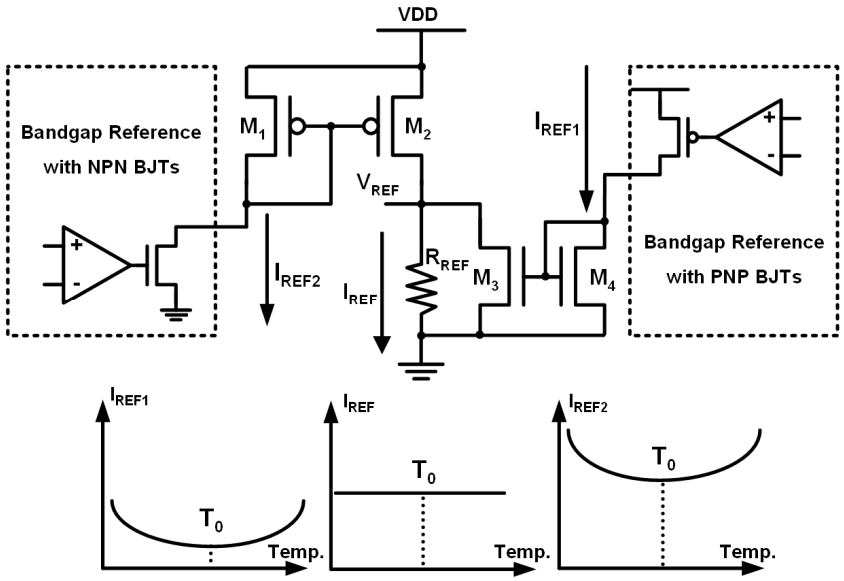


Fig. 2.12. The new proposed sub-1-V curvature-compensated bandgap voltage reference circuit.

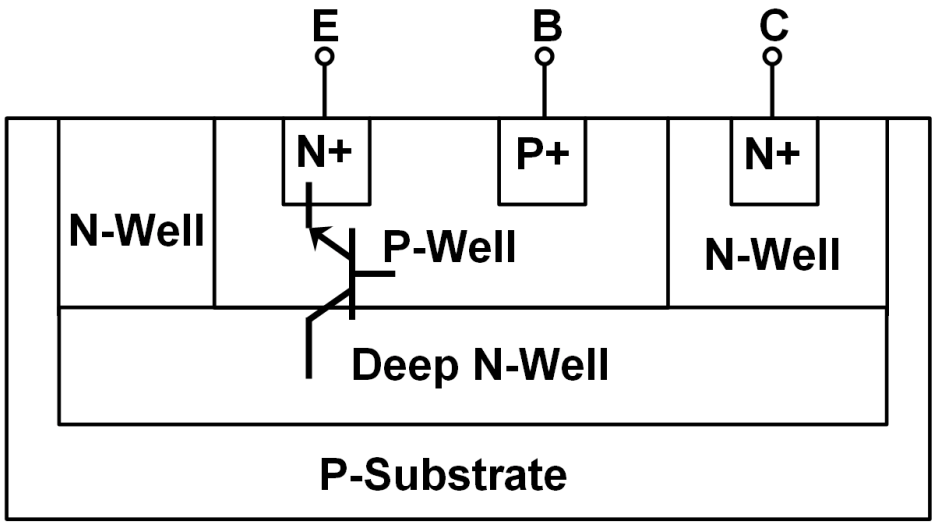


Fig. 2.13. The cross-sectional view of parasitic vertical NPN BJT in CMOS technology.

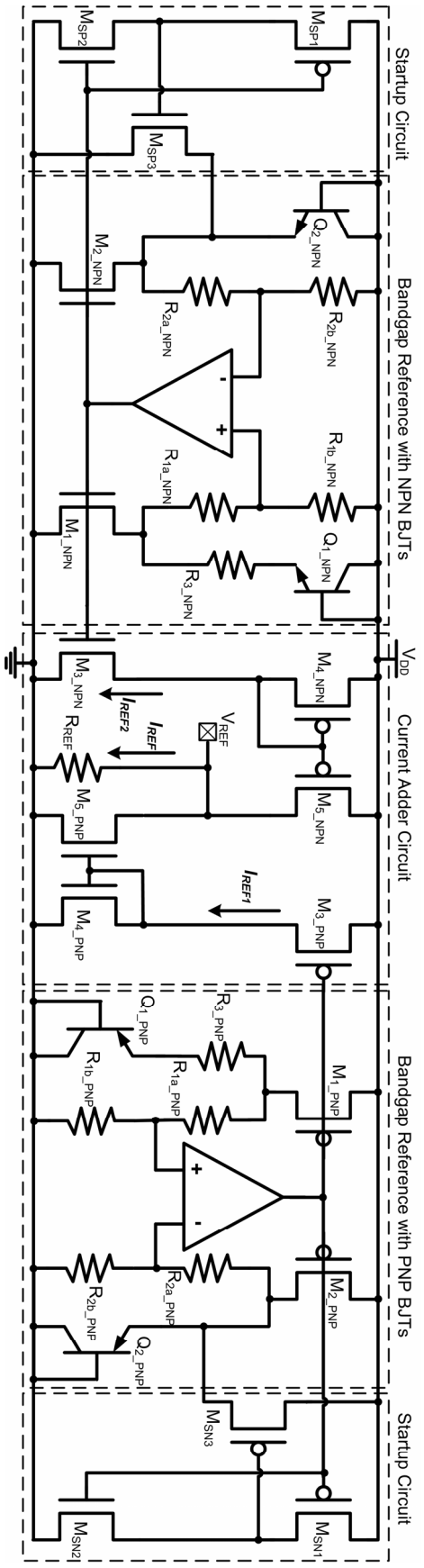


Fig. 2.14. Complete circuit of the new proposed curvature-compensated bandgap voltage reference for sub-1-V operation.

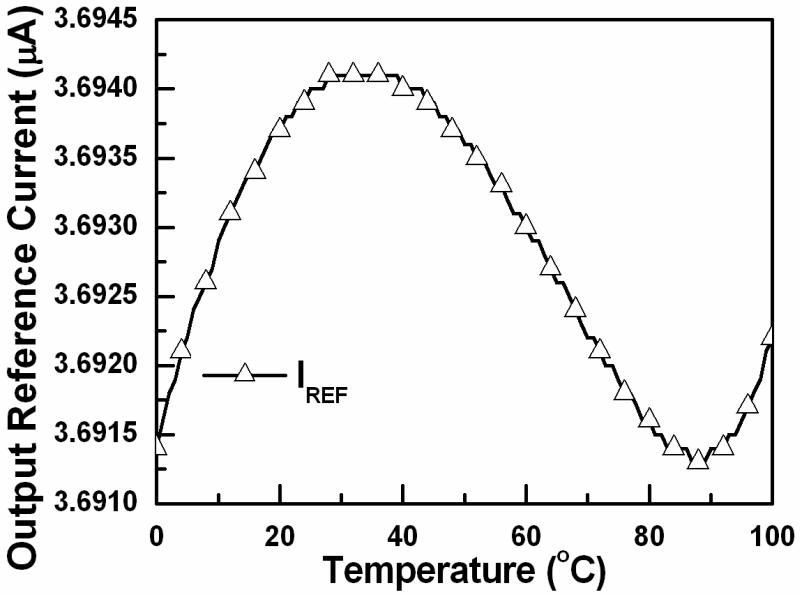


Fig. 2.15. Simulated output reference current (I_{REF}) of the new proposed bandgap voltage reference under different temperatures from 0 to 100 ˚C with supply voltage of 1 V.

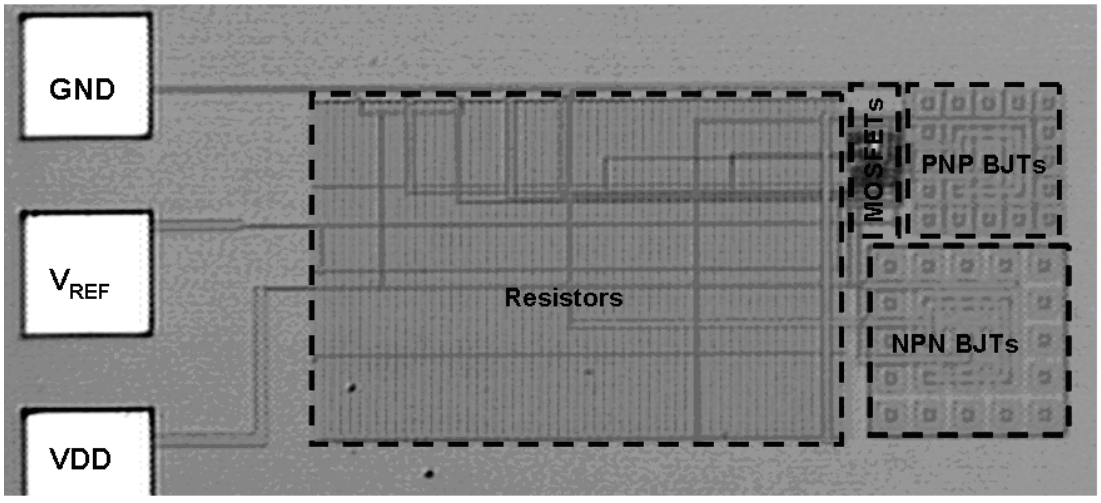


Fig. 2.16. Die microphotography of the new proposed curvature-compensated bandgap voltage reference fabricated in a 0.25-μm CMOS process.

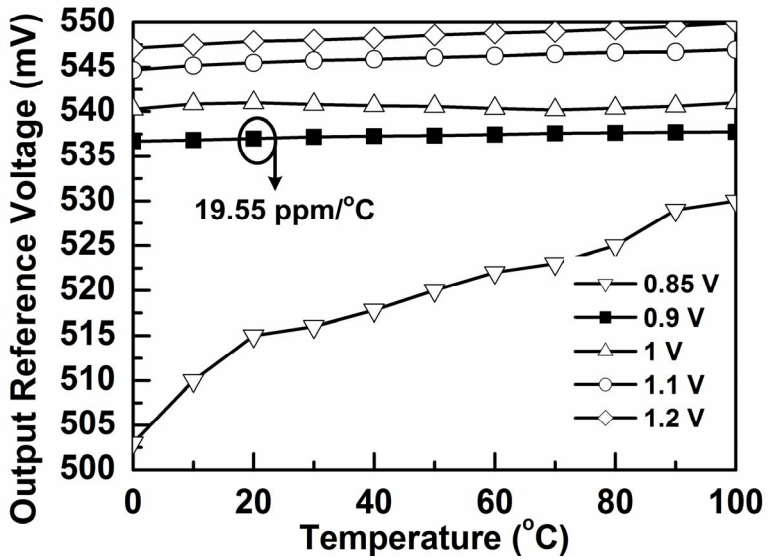


Fig. 2.17. The measured dependence of output reference voltage on the operating temperature under different supply voltage levels.

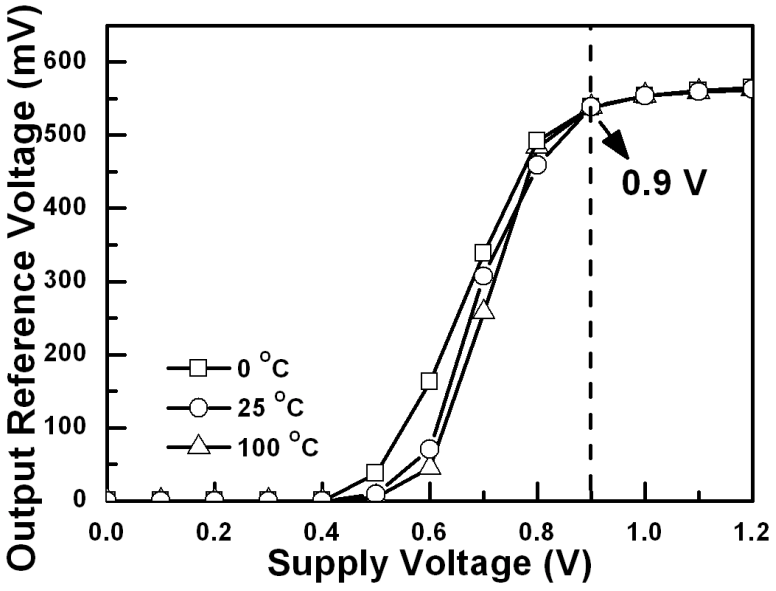


Fig. 2.18. The measured dependence of output reference voltage on the supply voltage under different operating temperatures.

CHAPTER 3

Impact of Gate-Oxide Reliability on CMOS Analog Amplifiers in Nanoscale CMOS Technology

The influences of gate-oxide reliability on analog amplifiers are investigated with common-source amplifier and operational amplifier in a 130-nm low-voltage CMOS process. The test conditions of this work include the DC stress, AC stress with DC offset, and large-signal transition stress under different frequencies and signals. After overstresses, the small-signal parameters, such as small-signal gain, unity-gain frequency, phase margin, and output DC voltage levels, are measured to verify the impact of gate-oxide reliability on circuit performances of the analog amplifiers. The impact of soft and hard gate-oxide breakdowns on common-source amplifiers with non-stacked and stacked diode-connected active load structures has been analyzed and discussed. The hard breakdown has more serious impact to the analog amplifiers.

3.1. Single Amplifier

3.1.1. Background

The reduction of power consumption has become increasingly important to portable products, such as mobile phone, notebook, and flash memory. In general, the most common and efficient way to reduce the power consumption in CMOS very large scale integrated circuits (VLSI) is to reduce the power-supply voltage. To reduce the power consumption in CMOS VLSI systems, the standard supply voltage trends to scale down from 2.5 to 1 V. Thus the gate-oxide thickness of the MOS transistor will be become thin to reduce nominal operation voltage (power-supply voltage). In general, the VLSI productions have lifetime of 10 years, but the thin gate-oxide

thickness of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current, and hot carrier effect that will degrade the lifetime of the MOS transistor. Therefore, to improve the gate-oxide reliability of MOS transistor and to investigate the effect of gate-oxide breakdown on CMOS circuit performances will become more important in the nanometer CMOS technology.

The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time-to-breakdown at operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem for the old CMOS technologies, which had thick gate oxide. However, because the probability of gate-oxide breakdown strongly increases with the decreasing oxide thickness [76], [77], the CMOS circuit in nano-scale technologies could be insufficiently reliable. The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown has been investigated [49]-[52], [76]-[83], which point out that the gate-oxide breakdown will degraded the small-signal parameters of the MOS transistor, such as transconductance, g_m, and threshold voltage, V_{TH}. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits have been reported [49]-[52], [78], [79]. In [49], it was demonstrated that the digital circuits would remain functional beyond the first gate-oxide hard breakdown. A soft gate-oxide breakdown event in dynamic CMOS digital circuit relying on the uncorrected soft nodes may result in some failure of the circuit [50]. The gate-oxide breakdown on RF circuit has been studied [51]. The impact of gate-oxide breakdown on SRAM stability was also investigated [52], [78]. Some designs of analog circuits [84], [85] and the mixed-voltage I/O interface [86], [87] indicate that gate-oxide reliability is a very important design consideration in CMOS integrated circuits. The impact of MOSFET gate-oxide reliability on the CMOS operational amplifiers had been investigated and simulated [88]. The performances of analog circuits strongly depend on the I-V characteristics of MOSFET devices, because the small-signal parameters of MOSFET device are determined by the biasing voltage and current of MOSFET devices. The small-signal gain and frequency response of analog circuits in CMOS processes are determined by the transconductance g_m and output resistance r_o of MOSFET devices. The transconductance g_m and output resistance r_o of MOSFET device can be expressed by

$$g_m = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right) = \frac{2I_D}{\left(V_{GS} - V_{TH}\right)}, \tag{3.1}$$

$$r_o = \frac{V_A}{I_D}, \tag{3.2}$$

where μ is the mobility of carrier, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage of MOSFET device, V_{GS} is the gate-to-source voltage of MOSFET device, V_A is the Early voltage, and the current I_D is the drain current of MOSFET device. Comparing the equations (3.1) and (3.2), the drain current I_D is the key factor for analog circuits in CMOS process. Therefore, the performances of analog circuits in CMOS processes are dominated by the drain currents of MOSFET devices. The drain current I_D of MOSFET device operated in saturation region can be expressed by

$$I_D = \frac{1}{2}\mu C_{OX} \frac{W}{L}(V_{GS} - V_{TH})^2. \tag{3.3}$$

The channel-length modulation and body effect of MOSFET devices are not included in equation (3.3). The threshold voltage and gate-to-source voltage of MOSFET device are the important design parameters in equation (3.3). However, the gate-oxide overstress of MOSFET will cause degrade the device characteristics of MOSFET. Therefore, gate-oxide breakdown can be expected to have serious impact on the performances of analog circuits in nanoscale CMOS technology.

In this work, the influence of gate-oxide reliability on common-source amplifiers with diode-connected active load is investigated with the non-stacked and stacked structures in a 130-nm low-voltage CMOS process under the DC stress, AC stress with DC offset, and large-signal transition stress. The small-signal gain, phase margin, unity-gain frequency, and output DC voltage level of the two common-source amplifiers are measured and compared under the different stresses in analog and digital applications. The impact of soft and hard breakdowns on these two amplifiers has been discussed and analyzed.

3.1.2. Analog Amplifiers

The common-source amplifier is a basic unit in many typical analog circuitry cells, such as level converter and output stage. The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are used to verify the impact of MOSFET gate-oxide reliability on CMOS analog amplifier. The complete circuits of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are shown in Figs. 3.1(a) and 3.1(b). The common-source amplifiers have been fabricated in a 130-nm low-voltage CMOS process. The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in these two common-source amplifiers are 1-V and 2.5-nm, respectively, in a 130-nm low-voltage CMOS process. The device dimensions of two amplifiers are shown in Table 3.1. The body terminals of the all NMOS and PMOS transistors are connected to ground and power supply voltage, respectively. The small-signal gain, $A_{V\_Non\text{-}Stacked}$, of the common-source amplifier with the non-stacked diode-connected active load structure is given by

$$A_{V\_Non-Stacked} = -\frac{g_{m1} - SC_{GD1}}{g_{o1} + g_{o2} + g_{m2} + S\left(C_{GD1} + C_{GS2} + C_L\right)}, \tag{3.4}$$

where the g_o and g_m are the output conductance and transconductance of MOS transistor, respectively. In the MOSFET device, the C_{GS} is the parasitic capacitance between the gate and source nodes, and the C_{GD} is the parasitic capacitance between the gate and drain nodes. The C_L is the output capacitive load. The small-signal gain, $A_{V\_Stacked}$, of the common-source amplifier with the stacked diode-connected active load structure can be written as

$$A_{V\_Stacked} = -\frac{g_{o3}\left(g_{m3} - SC_{GD3}\right)}{\left(SC_{GD3} + g_{o3} + g_{oz}\right)\left[\left(SC_L + g_{ox} \,//\, g_{oy}\right) - g_{oz}g_{o3}\right]}, \tag{3.5}$$

where the g_{ox}, g_{oy}, and g_{oz} equal to $g_{m5}+g_{o5}+SC_{GS5}$, $g_{m6}+g_{o6}+SC_{GS6}$, and $g_{m4}+g_{o4}+SC_{GS4}$, respectively. Before overstress, the small-signal gains of the common-source amplifiers with the non-stacked and stacked diode-connect active load structures are 17.5-dB and 13.2-dB, respectively. The body effect of the NMOS and PMOS transistors in the common-source amplifiers with the non-stacked and stacked diode-connect active load structures is not included in equations (3.4) and (3.5). The phase margin of the two common-source amplifiers is more than 60 degree under output capacitive load of 10 pF. Comparing the common-source amplifiers with

the non-stacked and stacked diode-connected active load structures, the impact of gate-oxide reliability on the CMOS common-source amplifier has been investigated under analog and digital applications.

3.1.3. Overstress Test

The impact of gate-oxide reliability on common-source amplifier needs long-term operation, which may need many years, to measure the performance degradation under the gate-oxide degradation of MOSFET device. In order to accelerate the gate-oxide degradation and understand the impact of gate-oxide reliability on common-source amplifiers with the non-stacked and stacked diode-connected active load structures, the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are statically stressed at supply voltage V_{DD} of 2.5 V. Because the MOS transistors in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur in conventional time-dependent dielectric breakdown (TDDB). High V_{GS}, V_{GD}, and V_{DS} of the MOSFET are set to get a fast and easy-to-observe breakdown occurrence for investigating the impact of gate-oxide reliability on the common-source amplifier with diode-connected active load. The advantages of using static stress are the known and well-defined distributions of the voltages in the common-source amplifiers with diode-connected active load and better understanding of the consequences of this stress. After the overstresses, the small-signal parameters of the common-source amplifiers with non-stacked and stacked diode-connected active load structures are re-evaluated on the same operation condition under the DC stress, AC stress with DC offset, and large-signal transition stress.

3.1.3.1. DC Stress

The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are continuously operated in this DC overstress, as shown in Fig. 3.2. The power supply voltage, V_{DD}, and output capacitive load, C_L, of the common-source amplifiers with non-stacked and stacked diode-connected active load structures are set to 2.5 V and 10 pF, respectively. The input nodes, V_{IN_1}

and V_{IN_2}, are biased to 0.5 V in order to set the output DC voltage level at 1.25 V under the power supply voltage of 2.5 V. During this DC overstress, the small-signal gain and unity-gain frequency of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are measured. When those parameters are measured, the input signal of DC 0.5 V at input nodes, V_{IN_1} and V_{IN_2}, is replaced by the AC small-signal of 200 mV sinusoidal signal (peak-to-peak amplitude) with DC voltage of 0.5 V. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress is shown in Fig. 3.3. The small-signal gain of the common-source amplifier with the non-stacked diode-connected active load structure is degraded by gate-oxide breakdown. Moreover, the common-source amplifier with the non-stacked diode-connected active load structure does not maintain its amplified function with continuous stress condition under the DC stress, when the stress time is increased. The small-signal gain of the common-source amplifier with the stacked diode-connected active load structure is not changed under the same stress condition even through the stress time up to 2000 minutes. The measured waveforms of the input and output signals in the common-source amplifier with the non-stacked diode-connected active load structure on the different stress times are shown in Figs. 3.4(a), 3.4(b), and 3.4(c). Fig. 3.5 shows the dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress. The bandwidth of the common-source amplifier with non-stacked diode-connected active load structure on the stress time is decreased, but that of the common-source amplifier with the stacked diode-connected active load structure is almost not changed after the stress. The phase margin of the common-source amplifier with the non-stacked diode-connected active load structure on the stress time is varied with gate-oxide breakdown, but that is still stable (phase margin > 45 degree). The dependence of the output DC voltage level on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress is shown in Fig. 3.6. The output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure on the stress time will be closed to the power supply voltage of 2.5 V, but that of the common-source amplifier with the stacked diode-connected active load structure is not changed after the stress.

The reason, why the circuit performances of the common-source amplifier with the non-stacked diode-connected active load structure, such as small-signal gain, unity-gain frequency, and output DC voltage level, is degraded with the overstress, is summed up that the gate-oxide breakdown will degrade the transconductance (g_m), threshold voltage (V_{TH}), and output conductance (g_o) of the MOS transistor. In equation (3.4), if the small-signal parameters g_m, V_{TH}, and g_o of the MOS transistor are degraded with gate-oxide breakdown, the small-signal gain will be changed. From the equation (3.4), the dominant pole of the common-source amplifier with the non-stacked diode-connected active load structure can be written as

$$\omega_{p\_Non-Stacked} = \frac{g_{m2} + g_{o1} + g_{o2}}{C_{GS2} + C_{GD1} + C_L}, \tag{3.6}$$

which is dominated by transconductance, g_{m2}, and output capacitive load, C_L. Therefore, the unity-gain frequency of the common-source amplifier with the non-stacked diode-connected active load structure will be degraded by gate-oxide breakdown. In this test condition, if the transistors M_1 and M_2 of the common-source amplifier with the non-stacked diode-connected active load structure are designed to operate in saturation region, the output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure can be expressed as

$$V_{OUT\_1(DC)} = V_{DD} - V_{TH(M2)} - \sqrt{\frac{\left(\frac{W}{L}\right)_{M1}}{\left(\frac{W}{L}\right)_{M2}}}\left(V_{IN\_1} - V_{TH(M1)}\right). \tag{3.7}$$

In the equation (3.7), the output DC voltage level, $V_{OUT\_1(DC)}$, is function of the $V_{TH(M1)}$ and $V_{TH(M2)}$. Therefore, the output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure will be changed with gate-oxide breakdown after the stress.

3.1.3.2. AC Stress with DC Offset

The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are continuously tested in this stress of AC

small-signal input and DC offset, as shown in Fig. 3.7. The input nodes, V_{IN_1} and V_{IN_2}, of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are biased to the AC small-signal input of 200-mV sinusoidal signal (peak-to-peak amplitude) with DC offset voltage of 0.5 V under the different frequencies of 100 Hz, 500 kHz, and 1 MHz. The power supply voltage, V_{DD}, and output capacitive load, C_L, of the common-source amplifiers with non-stacked and stacked structures are set to 2.5 V and 10 pF, respectively. The measurement setup is used to investigate the relationship between gate-oxide breakdown and different frequencies of input signals in the CMOS analog circuit applications.

The dependence of the small-signal gain in the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on the stress time under the stress of the AC small-signal input with DC offset is shown in Fig. 3.8. The circuit performances of the common-source amplifier with the stacked diode-connected active load structure are not degraded by the stress of the AC small-signal input with DC offset. In the common-source amplifier with the non-stacked diode-connected active load structure, the high-frequency input signal causes a slow degradation on the small-signal gain, but the low-frequency input signal causes a fast degradation on the small-signal gain under the stress of the AC small-signal input with DC offset. The other small-signal performances in the common-source amplifier with the non-stacked diode-connected active load structure under the stress of the AC small-signal input with DC offset have the same change trend as that under the DC stress, but the different frequencies of the input signal will cause the different degradation times. These measured results are consistent to that reported in [90]. The frequency dependence of t_{BD} (time to breakdown) is reasonably understood in terms of the re-distribution of the breakdown species from the anodic interface toward the oxide bulk. These two different frequency regimes correspond to two extreme distributions. When the frequency is very high, the concentration of "breakdown species" is expected to be low. The distribution strongly peaked at both interfaces. This presumably explains the reduction of degradation. On the contrary, in the low frequency, concentration is expected to be high and to have a uniform distribution throughout the oxide film. This causes the lead to faster degradation process [90]. Therefore, the small-signal performance of the non-stacked

common-source amplifier with different frequencies of the input signals will cause different degradation times under the stress of the AC small-signal input with DC offset.

3.1.3.3. Large-Signal Transition Stress

This research results [49], [89] indicated that the high and low output voltage levels of the CMOS digital complementary logic circuits under large-signal transition stress were not be degraded with gate-oxide breakdown. Only the maximum operation frequency of the CMOS digital complementary logic circuits was decreased with gate-oxide breakdown, but the impact of gate-oxide breakdown on the inverter with active load (common-source amplifier) is still not studied. Therefore, the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are used to investigate the impact of gate-oxide reliability on CMOS inverter with active load under the large-signal transition stress. The common-source amplifiers with the non-stacked and stacked diode-connected active load structures are continuously tested in this stress of large-signal transition, as shown in Fig. 3.9. The input nodes, V_{IN_1} and V_{IN_2}, of the amplifiers with the non-stacked and stacked diode-connected active load structures are biased at DC 0.5 V, the output capacitive load, C_L, is set to 10 pF, and the power supply voltage, V_{DD}, is set to 2.5 V. The input square voltage from 0 V to 1 V with frequency of 100 Hz is applied to the input node of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the large-signal transition stress. The square voltage of input signal from 0 V to 1 V will not induce the damage on the input devices, M_1 and M_3, of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures, because the voltage across the input devices (V_{GS}) of the common-source amplifiers is lower than the 1 V in this measurement.

The dependences of the high and low voltage levels at the output node on the stress time are show in Fig. 3.10, where the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are stressed by the large-signal transition. The high and low output voltage levels of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the stress of large-signal transition are increased, when the stress time is increased. The

measured waveforms of the input and output signals of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on the different stress times under the large-signal transition stress are shown in Figs. 3.11(a), 3.11(b), and 3.11(c). The impact of gate-oxide breakdown on the common-source amplifier with the non-stacked diode-connected active load structure is more serious than that of common-source amplifier with the stacked diode-connected active load structure under the large-signal transition stress. The maximum operation frequency of the common-source amplifiers with the non-stacked and stacked structures has the same change trend as that of the CMOS digital complementary logic circuits under the large-signal transition stress. The measured results of the large-signal transition stress have some difference with the results of the prior researches [49], [89], because the high and low output voltage levels of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures are controlled by diode-connected transistors M_2, M_4, M_5, and M_6, respectively. For example, the high output level of the common-source amplifier with the non-stacked diode-connected active load structure can be expressed as

$$VH_{\_Non-Stacked} = V_{DD} - \left|V_{TH(M2)}\right|. \tag{3.8}$$

The low output level of the common-source amplifier with the non-stacked diode-connected active load structure can be written as

$$VL_{\_non-stacked} = 2\left(V_{IN\_1} - V_{TH(M1)}\right) - \sqrt{\left[4(V_{IN\_1} - V_{TH(M1)})^2 - 4\frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}}\left(V_{DD} - \left|V_{TH(M2)}\right|\right)\right]}. \tag{3.9}$$

The threshold voltage (V_{TH}) of the MOS transistor will be degraded by gate-oxide breakdown, so that the $VH_{\_non\text{-}stacked}$ and $VL_{\_stacked}$ of the common-source amplifier with the non-stacked diode-connected active load structure will be changed under the stress of large-signal transition. In the CMOS digital complementary logic circuits, either pull-up or pull-down MOS transistors will be turn-on under the logic high or low steady state, respectively. The logic high and low steady states of the CMOS digital complementary logic circuits are independent on dimension and threshold voltage of the MOS transistors. Therefore, the voltage levels of the logic high and low steady states in the CMOS digital complementary logic circuits will not be degraded

with gate-oxide breakdown.

3.1.4. Discussions

The summary of overstress results under three overstress conditions (DC, AC, and large-signal transition stresses) is listed in Table 3.2. The gate-oxide breakdown will degrade the transconductance (g_m), output conductance (g_o), and threshold voltage (V_{TH}) of MOSFET devices. After the overstress, the performances of the common-source amplifier with the non-stacked diode-connected active load structure under the DC, AC with DC offset, and large-signal transition stresses are seriously degraded with gate-oxide breakdown, and those of the common-source amplifier with stacked diode-connected active load structure are only slightly degraded under the large-signal transition stress. As a result, the performance degradation of the common-source amplifier with the non-stacked diode-connected active load structure is more seriously than that of the common-source amplifier with the stacked diode-connected active load structure. The small-signal performance of the common-source amplifier is very sensitivity to the DC operation point, so the gate-oxide breakdown will cause the g_m, V_{TH}, and g_o degradations and extra gate-leakage current of the MOS transistor to induce the change of the DC operation point in the common-source amplifier. Considering the common-source amplifier with the non-stacked diode-connected active load structure, if the parameters, g_{m1} and g_{m2}, are variable factor in the equation (3.1), the sensitivities of the equation (3.1) to the parameters, g_{m1} and g_{m2}, are expressed as

$$S_{g_{m1}}^{A_{V\_Non-Stacked}} = \frac{g_{m1}}{g_{m1} - SC_{GD1}}, \tag{3.10}$$

$$S_{g_{m2}}^{A_{V\_Non-Stacked}} = \frac{g_{m2}}{g_{o1} + g_{o2} + g_{m2} + S\left(C_{GD1} + C_{GS2} + C_L\right)}. \tag{3.11}$$

In the equations (3.10) and (3.11), the parameters g_{o1} and g_{o2} can be ignored, because they are small than 1. The parasitic capacitances C_{GD1} and C_{GS2} of the MOS transistors are not considered. The sensitivities of the equations (3.10) and (3.11) to the parameters g_{m1} and g_{m2}, respectively, are approximate 1. Therefore, the gate-oxide breakdown of the MOS transistors has serious impact to the circuit performances of

analog circuits. As a result, the gate-oxide reliability is very important design issue in the nano-meter CMOS process. The gate-oxide reliability can be improved by the stacked structure in the common-source amplifier under small-signal input and output applications. The common-source amplifier with the stacked diode-connected active load structure can be worked in high supply voltage depended on the stacked number of transistor used to control the voltages (V_{GS}, V_{GD}, and V_{DS}) across the transistor and to avoid the gate-oxide breakdown.

3.1.5. *Effect of Hard and Soft Breakdowns on Performances of Common-Source Amplifiers*

3.1.5.1. DC Stress

The measured dependence of power supply current I_{VDD} in two amplifiers on stress time have been measured and recorded, as shown in Fig. 3.12, under the DC stress. Because the power supply current I_{VDD} of the common-source amplifier with the stacked diode-connected active load structure is not degraded after the DC stress, the gate-oxide degradation of MOSFET is not occurred in this measurement. However, the power supply current I_{VDD} of the common-source amplifier with the non-stacked diode-connected active load structure is degraded during the DC stress. Based on the prior proposed method [82], [91], the gate-oxide breakdown of MOSFET device can be modeled as resistance. Only the gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst-case situation. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard breakdown leakage has close-to-linear I-V behavior and an equivalent resistance of ~ 10^3-10^4 Ω, while typical soft breakdown paths have high non-linear, power law I-V behavior and equivalent resistance above 10^5-10^6 Ω [82]. The oxide breakdown is not occurred on gate-to-source side of M_1 device in the common-source amplifier with the non-stacked diode-connected active load structure, because the voltage across gate-to-source side of M_1 device is smaller than 1 V in the amplifier. The complete circuit of the common-source amplifier with the non-stacked diode-connected active load structure including gate-oxide breakdown model is shown in Fig. 3.13. The breakdown resistances of R_{BD1} and R_{BD2} can be used to simulate the impact of hard

and soft breakdowns on performances of the common-source amplifier with the non-stacked diode-connected active load structure. Comparing the measured results among Figs. 3.3, 3.5, 3.6, and 3.12, the dependence of power supply current I_{VDD} (non-stacked) on stress time in Fig. 3.12 can be separated by three regions (I, II, and III regions) due to the gate-oxide breakdown. This result has some differences between the impact of gate-oxide breakdown on performances of analog and digital circuits. When the performances of the common-source amplifier with the non-stacked diode-connected active load structure are degraded due to the gate-oxide breakdown, the power supply current I_{VDD} is not increased immediately. The relationship between power supply current I_{VDD} and gate-oxide breakdown occurred on M_1 and M_2 devices under three regions in the common-source amplifier with the non-stacked diode-connected active load structure can be modeled by

Region I: no gate-oxide breakdown occurred on M_1 and M_2 devices,
Region II: hard breakdown occurred on M_2 device, and
Region III: hard breakdown occurred on M_1 and M_2 devices.

In Region I, the gate-oxide breakdown of MOSFET device is more likely to occur as the time-dependent dielectric breakdown (TDDB). In this region, the small-signal performance and power supply current I_{VDD} of the common-source amplifier with the non-stacked diode-connected active load structure have very small variations on the stress time under DC stress. The gate-oxide breakdown is not occurred on M_1 and M_2 devices.

In Region II, the power supply current I_{VDD} was not changed, but the small-signal performances of the common-source amplifier with the non-stacked diode-connected active load structure was seriously degraded. The reason, why the power supply current I_{VDD} of the common-source amplifier is not changed, is due to the gate-oxide breakdown on M_2 device. The simulated dependence of power supply current I_{VDD} under different breakdown resistances R_{BD1} and R_{BD2} is shown in Fig. 3.14. The power supply current I_{VDD} of the common-source amplifier with the non-stacked diode-connected active load structure is dominated by M_1 device. Because the gate-oxide breakdown on M_1 device is not occurred, the power supply current I_{VDD} of the common-source amplifier is limited under the DC stress. The simulated dependence of small-signal gain and output DC voltage level of the

common-source amplifier with the non-stacked diode-connected active load structure under different resistances R_{BD2} is shown in Fig. 3.15. Based on the prior proposed method [81], the impact of soft breakdown occurred on M_2 device has less influence on circuit performances. The hard breakdown occurred on M_2 device causes the serious degradations on performances of the common-source amplifier with the non-stacked diode-connected active load structure, but the power supply current I_{VDD} is not changed under the DC stress. These simulated results can be used to confirm and understand that the hard breakdown is only occurred on M_2 device of the common-source amplifier with the non-stacked diode-connected active load structure during the DC stress in Region II.

In the Region III, the power supply current I_{VDD} and small-signal performances of the common-source amplifier with the non-stacked diode-connected active load structure are seriously degraded under DC stress. The hard breakdown is occurred on both M_1 and M_2 devices under the DC stress in Region III.

Comparing the Regions I, II, and III under DC stress, the degradation on power supply current I_{VDD} is dominated by gate-oxide breakdown on M_1 device. The gate-oxide breakdown occurred on M_2 device is a dominated factor to degrade the performances of the common-source amplifier with the non-stacked diode-connected active load structure. As a result, the hard breakdown has more serious impact on performances of the common-source amplifier.

3.1.5.2. Large-Signal Transition Stress

In order to investigate and understand the impact of hard and soft breakdowns on performances of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under large-signal transition stress, the complete circuits including the gate-oxide breakdown model are shown in Figs. 3.13 (non-stacked) and 3.16 (stacked), respectively. In these two amplifiers, the gate-oxide breakdown does not occur on gate-to-source sides of M_1 (in Fig. 3.13) and M_3 (in Fig. 3.16) devices under large-signal transition stress, because the voltages across gate-to-source sides of M_1 and M_3 devices are smaller than 1 V, respectively. The static and the dynamic currents in two amplifiers under digital operation are increased

after the gate-oxide breakdown [49]. The hard gate-oxide breakdown has been occurred on the common-source amplifier with non-stacked diode-connected active load structure after overstress. The soft gate-oxide breakdown has been occurred on common-source amplifier with stacked diode-connected active load structure after overstress. The simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifiers with the non-stacked diode-connected active load structures under the different resistances R_{BD1} and R_{BD2} is shown in Fig. 3.17. The high output voltage level VH and low output voltage level VL of common-source amplifier with non-stacked diode-connected active load structure are degraded by oxide breakdown occurred on M_1 and M_2 devices, respectively. Comparing Figs. 3.10 and 3.17, the breakdown location in the common-source amplifier with the non-stacked diode-connected active load structure is occurred on M_2 device after large-signal transition stress.

The impact of gate-oxide breakdown on performance of the common-source amplifier with the stacked diode-connected active load structure can be simulated and investigated by the same method to find breakdown location. Fig. 3.18 shows the simulated dependence of the high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active load structure under the different resistances of R_{BD3}, R_{BD4}, R_{BD5}, and R_{BD6}, respectively. The different breakdown locations cause different performance degradations of the common-source amplifier with the stacked diode-connected active load structure under large-signal transition stress. Comparing Figs. 3.10 and 3.18, the breakdown location in the common-source amplifier with the stacked diode-connected active load structure is occurred on M_5 or M_6 device under large-signal transition stress. The high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active load structure are increased, when the stress time is increased. The common-source amplifier with the stacked diode-connected active load structure has slow degradation rate, because the voltage across MOSFET device is smaller than that of common-source amplifier with the non-stacked diode-connected active load structure. The hard breakdown has more serious impact on performances of common-source amplifier with non-stacked diode-connected active load structure. The stacked structure can be used to improve the reliability of analog circuits in nanoscale CMOS technology.

3.1.5. Summary

The impact of gate-oxide reliability on CMOS common-source amplifiers with the non-stacked and stacked diode-connected active load structures has been investigated and analyzed under the DC stress, AC stress with DC offset, and large-signal transition stress. The small-signal parameters of the common-source amplifier with the non-stacked diode-connected active load structure are seriously degraded than that with stacked diode-connected active load structure by gate-oxide breakdown under DC, AC, and large-signal transition stresses. The stacked structure can be used to improve the reliability of analog circuit in nanoscale CMOS process. The impact of soft breakdown, hard breakdown, and breakdown location on circuit performances of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures has been investigated and analyzed. The hard gate-oxide breakdown has more serious impact on performances of the common-source amplifier with the diode-connected active load.

3.2. Operational Amplifier

3.2.1. Background

The reduction of power consumption has become increasingly important to portable products, such as mobile phone, notebook, and flash memory. In general, the most common and efficient way to reduce the power consumption in CMOS very large scale integrated circuits (VLSI) is to reduce the power-supply voltage. To reduce the power consumption in CMOS VLSI systems, the standard supply voltage trends to scale down from 5 to 1 V. Thus the gate-oxide thickness of the MOS transistor will be become thin to reduce nominal operation voltage (power-supply voltage). In general, the VLSI productions have lifetime more than 10 years, but the thin gate oxide of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current and hot carrier effect, that will degrade the lifetime of the MOS transistor. Therefore, to improve the gate-oxide reliability of MOS transistor and to investigate the effect of gate-oxide breakdown on CMOS circuit performances will become more important in the nanometer CMOS technology.

The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time-to-breakdown at circuit operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem for old CMOS technologies, which have the thick gate oxide. However, because the probability of gate-oxide reliability strongly increases with the decrease of gate-oxide thickness [1], the CMOS circuits in nano-scale technologies could be insufficiently reliable.

The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown has been investigated [49]-[52], [79]-[82], [80], [92], [93], which point out that the gate-oxide breakdown will degraded the small-signal parameters of the MOS transistor, such as tranconductance g_m and threshold voltage V_{TH}. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits have been reported [49]-[52], [78], [79]. In [49], it was demonstrated that the digital complementary logic circuits would remain functional beyond the first gate-oxide hard breakdown. A soft gate-oxide breakdown event in the CMOS digital dynamic logic circuits relying on the uncorrected soft nodes may result in the failure of the circuit [50]. The gate-oxide breakdown on RF circuits was also studied [51]. The impact of gate-oxide breakdown on CMOS differential amplifier and digital complementary logic circuits had been simulated [89]. Some designs of analog circuits [84], [85] and the mixed-voltage I/O interface [86], [87] indicate that gate-oxide reliability is a very import design consideration in CMOS circuits. However, the impact of MOSFET gate-oxide breakdown on the CMOS operational amplifier circuits is still not well studied and really verified in a silicon chip. The CMOS analog circuits are very sensitive to the small-signal parameters of MOSFET, such as tranconductance g_m and threshold voltage V_{TH}. Therefore, the gate-oxide breakdown is expected to have severe impact on the circuit performances of analog circuits.

In this work, the effect of MOSFET gate-oxide reliability on the operational amplifiers with the two-stage (non-stacked) and folded-cascode (stacked) structures is investigated in a 130-nm low-voltage CMOS process [88]. The small-signal gain, phase margin, unity-gain frequency, and power supply rejection ratio (PSRR) of these

operational amplifiers with different configurations are measured and compared after different stresses.

3.2.2. Operational Amplifiers

The operational amplifier is a basic unit in many analog circuits and systems, such as output buffer, sample-and-hold circuit, and analog-to-digital converter. The operational amplifiers with the two-stage and folded-cascode structures are selected to verify the impact of MOSFET gate-oxide reliability on analog circuits. The complete circuits of the operational amplifiers are shown in Figs. 3.19(a) and 3.19(b). The operational amplifier with the two-stage structure comprises the differential amplifier (M_1-M_5), common-source amplifier (M_6-M_7), and source follower (M_8-M_9). The operational amplifiers with the two-stage and folded-cascode structures have been fabricated in a 130-nm low-voltage CMOS process. The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in these operational amplifiers are 1 V and 2.5 nm, respectively, in a 130-nm low-voltage CMOS process. The channel length of NMOS and PMOS transistor in the two operational amplifiers is set to 0.5 μm or 1 μm to avoid the short channel effect, such as threshold variation, drain-induced barrier lowering (DIBL) effect, hot-carrier effect, velocity saturation, and mobility degradation effect. The body terminals of the all NMOS and PMOS transistors are connected to ground and power supply voltage, respectively. The device dimensions of two amplifiers are shown in Table 3.3. This design approach is usually used to design the operational amplifier in analog integrated circuit applications.

In signal MOSFET device, if the critical terminal voltage of the device, such as gate-to-source voltage (V_{GS}), gate-to-drain voltage (V_{GD}), and drain-to-source voltage (V_{DS}), is kept within the normal operating voltage V_{DD} of the technology, the electric fields across the MOS device will not cause the damage on the gate oxide. Therefore, the bias circuit of the operational amplifiers is designed with stacked structure to avoid the gate-oxide breakdown. The Miller compensated capacitance C_C of the two-stage operational amplifier in Fig. 3.19(a) is realized by the metal-insulator-metal (MIM) structure, which has no gate-oxide reliability problem. The impact of

MOSFET gate-oxide reliability on the operational amplifiers with the two-stage and folded-cascode structures is verified by using continuous stress with supply voltage of 2.5 V. The input common-mode voltage of the operational amplifiers is set to 1.25 V, respectively. Simulated by HSPICE, the open-loop gain and phase margin of the operational amplifier with the two-stage structure are 64.7 dB and 47.8 degree, respectively, under output capacitive load of 10 pF. The open-loop gain and phase margin of another operational amplifier with the folded-cascode structure are 61.9 dB and 89 degree, respectively, under output capacitive load of 10 pF. The open-loop small-signal gain ($A_{V\_two\text{-}stage}$) of the operational amplifier with the two-stage structure is given by

$$A_{V\_two-stage}(S) \cong \frac{g_{m1}g_{m6}g_{m8}}{g_{ox}g_{oy}g_{oz}} \frac{1-SC_c/g_{m6}}{(1-SC_L/g_{oz})(g_{oy}+g_{m6}SC_L)}, \tag{3.12}$$

where the g_o and g_m are the output conductance and transconductance of the corresponding MOSFET in the operational amplifiers. The g_{ox}, g_{oy}, and g_{oz} equal to $g_{o5}+g_{o2}$, $g_{o6}+g_{o7}$, and $g_{o8}+g_{o9}$, respectively. The open-loop small-signal gain ($A_{V\_folded\text{-}cascode}$) of the operational amplifier with the folded-cascode structure is also written as

$$A_{V\_folded-cascode}(S) \cong \frac{g_{m11}R_o}{1+SC_LR_o}, \tag{3.13}$$

$$R_o = \frac{1}{\frac{g_{o11}+g_{o20}}{g_{m18}r_{o18}} + \frac{g_{o14}}{g_{m16}r_{o16}}}, \tag{3.14}$$

where the r_o is the output resistance of the corresponding MOSFET in the operational amplifiers. The short-channel effect, body effect, and parasitic capacitance of MOS transistors in the two operational amplifiers are ignored in the equations (3.12), (3.13), and (3.14). The capacitances C_L and C_C are the output capacitive load and Miller compensated capacitance, respectively, in the two operational amplifiers.

3.2.3. Overstress Test

The operational amplifiers with the close-loop (unity-gain buffer) and open-loop (comparator) configurations are selected to verify the impact of MOSFET gate-oxide

reliability on the circuit performances of the operational amplifiers with the two-stage and folded-cascode structures in a 130-nm low-voltage CMOS process. The small-signal gain, phase margin, output-signal swing, PSRR, and rise and fall times of the operational amplifiers varied with gate-oxide breakdown will be measured and analyzed. Because the MOSFET devices in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur as the conventional time-dependent dielectric breakdown (TDDB). High gate-to-source voltage (V_{GS}), gate-to-drain voltage (V_{GD}), and drain-to-source voltage (V_{DS}) of the MOSFET are used to get a fast and easy-to-observe breakdown occurrence for investigating the impact of the gate-oxide reliability on the operational amplifiers. The advantages of using static stress are the well-defined distributions of the voltages on the devices in the operational amplifiers and the better understanding of the consequences of this overstress. After overstress, the small-signal parameters of the operational amplifiers with the two-stage and folded-cascode structures are re-evaluated under the same operation condition. The test operation conditions include unity-gain buffer (close-loop) and comparator (open-loop) configurations under the DC stress, AC stress with DC offset, and large-signal transition stress.

3.2.3.1. DC Stress

The operational amplifiers with the two-stage and folded-cascode structures under the configuration of the unity-gain buffer are continuously tested in this DC stress, as shown in Fig. 3.20. The output node of the operational amplifiers is connected to the inverting input node to form the configuration of a unity-gain buffer. According to the basic negative-feedback theory, the close-loop small-signal gain of the operational amplifiers with the two-stage and folded-cascode structures under the unity-gain buffer configuration can be expressed as

$$A_{fV\_two-stage}(S) = \frac{A_{V\_two-stage}(S)}{1 + A_{V\_two-stage}(S)}, \tag{3.15}$$

$$A_{fV\_folded-cascode}(S) = \frac{A_{V\_folded-cascode}(S)}{1 + A_{V\_folded-cascode}(S)}, \tag{3.16}$$

where the $A_{V\_two\text{-}stage}(S)$ and $A_{V\_folded\text{-}cascode}(S)$ equal to the equations (3.12) and (3.13).

The small-signal gain, unity-gain frequency, and phase margin of the operational amplifier with the two-stage structure operating in a unity-gain buffer are 0.48 dB, 2.3 MHz, and 168 degree, respectively, under output capacitive load of 10 pF. Those of the operational amplifier with the folded-cascode structure operating in a unity-gain buffer are -0.4 dB, 1 MHz, and 163 degree, respectively, under output capacitive load of 10 pF. The non-inverting node of the operational amplifiers is biased at 1.25 V, the output capacitive load is set to 10 pF, and the supply voltage V_{DD} is set to 2.5 V. The measured results of the fresh frequency responses before any stress are shown in Figs. 3.21(a) and 3.21(b), where the operational amplifiers operate in the unity-gain buffer.

During this DC overstress, the small-signal gain, unity-gain frequency, phase margin, offset voltage, PSRR, and rise and fall times of the operational amplifiers will be measured under the unity-gain buffer configuration. When those parameters are measured, the input signal of 1.25 V at the non-inverting node (V_{IN}) is replaced by the AC small-signal of 200 mV sinusoid signal (peak-to-peak amplitude) with DC common-mode voltage of 1.25 V. The dependence of the small-signal gain on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 3.22. The close-loop small-signal gain of the operational amplifiers with the two-stage and folded-cascode structures under the DC stress is not changed; even through the stress time is up to 4000 minutes. The dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 3.23. The unity-gain frequency of the operational amplifier with the two-stage structure under the DC stress is decreased, but that of the operational amplifier with folded-cascode structure is not obviously changed under the same stress condition. The dependence of the phase margin on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 3.24. The phase margin of the operational amplifier with the two-stage structure under the DC stress is decreased, but that of the operational amplifier with folded-cascode structure is not obviously changed. The degradation on the small-signal performances in the operational amplifier with the two-stage structure under the DC stress can be explained that the gate-oxide breakdown will degrade the tranconductance g_m and threshold voltage V_{TH} of MOS transistor. In the equations

(3.12), the g_m and V_{TH} parameters are the principal factors, which dominate the small-signal gain, pole, and zero of the operational amplifier with the two-stage structure. Therefore, if the g_m and V_{TH} parameters are degraded with the stress, the small-signal performances of the operational amplifier with the two-stage structure will be changed under the unity-gain buffer configuration.

The dependence of the output-voltage swing on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 3.25. The output-voltage swing of the operational amplifier with the two-stage structure under the DC stress is decreased, but that of the operational amplifier with folded- cascode structure is not changed. The maximum output-signal swing of the operational amplifier with the two-stage structure under the unity-gain buffer configuration can be written as

$$V_{DS\_sat(M8)} \le V_{out} \le V_{DD} - V_{DS\_sat(M9)}, \tag{3.17}$$

where the V_{DS_sat} is the over-drive voltage (V_{GS}-V_{TH}). The gate-oxide degradation will degraded the threshold voltage V_{TH}, so the output-signal swing of the operational amplifier with the two-stage structure operating in unity-gain buffer will be degraded with the overstress under the DC stress.

The input DC offset voltage of operational amplifiers operating in the unity-gain buffer can be measured from the voltage difference between the inverting and non-inverting nodes of the operational amplifiers, when the input pin (V_{IN}) is set to common-mode voltage of 1.25 V. The dependence of the input DC offset voltage on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 3.26. The offset voltage of the operational amplifier with the two-stage structure under the DC stress is increased, but that of the operational amplifier with the folded-cascode structure is not changed. The input DC offset voltage V_{OS} of the operational amplifier is caused by the MOS device mismatch and finite-gain error, which corresponding to the V_{OS1} and V_{OS2}, respectively, under the unity-gain buffer configuration. The input DC offset voltage of the operational amplifier under the unity-gain buffer configuration can be expressed as

$$V_{OS} = V_{OS1} + V_{OS2}, \tag{3.18}$$

$$V_{OS1} = \frac{V_{GS(M1)} - V_{TH(M1)}}{2}\left[\frac{\Delta(\frac{W}{L})_{(M1,M2)}}{(\frac{W}{L})_{(M1,M2)}} + \frac{\Delta(\frac{W}{L})_{(M4,M5)}}{(\frac{W}{L})_{(M4,M5)}}\right] - \Delta V_{TH(M1,M2)}, \tag{3.19}$$

$$V_{OS2} = \frac{V_{out}}{A_{V\_two-stage}(0)}. \tag{3.20}$$

The DC offset voltage V_{OS1} is caused by MOS transistor mismatch of differential amplifier. The finite small-signal gain of the operational amplifier will procure the DC offset voltage V_{OS2}. The DC offset voltage V_{OS1} plus V_{OS2} equals the total input DC offset voltage V_{OS}. In the case, only the impact of MOSFET gate-oxide degradation on the offset voltage V_{OS2} will be considered in the operational amplifier with the two-stage structure, because the differential pair of the two-stage operational amplifier is not degraded with the overstress. The DC offset voltage V_{OS2} is inverse proportion to $A_{V\_two-stage}(0)$ in equation (3.12). However, the $A_{V\_two-stage}(0)$ of the operational amplifier with the two-stage structure will be degraded by gate-oxide degradation, so the input DC offset voltage will be degraded with gate-oxide degradation under the DC stress.

About the measurement setup for output-signal rise and fall times of the operational amplifiers operating in the unity-gain buffer, the square voltage signal from 1 to 1.5 V is applied to the input pin to measure the rise and fall times of the signal at output pin. The rise and fall times are defined as the times of the output-signal rise and fall edges from 10 % to 90 %, when the square waveform of input signal has the rise and fall times of 1 ns. The dependence of the rise and fall times on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Figs. 3.27(a), 3.27(b), and 3.27(c). The rise and fall times of the operational amplifier with the two-stage structure under the DC stress is obviously changed, but that of the operational amplifier with folded-cascode structure is not changed. The rise and fall times of the operational amplifier with the two-stage structure can be expressed as

$$T_{rise} \cong \frac{C_L}{I_{DM8}}, \tag{3.21}$$

$$T_{fall} \cong \frac{C_L}{I_{DM9}}, \tag{3.22}$$

where the I_{DM9} and I_{DM8} correspond to across the MOS transistors M8 and M9 drain currents, respectively. The drain current of MOS transistor in the saturation region can be written as

$$I_D = K_n(\frac{W}{L})(V_{GS} - V_{TH})^2, \tag{3.23}$$

where the K_n is the tranconductance of MOS transistor, and the W/L is the MOS transistor dimension ratio. In the equations (3.21) and (3.22), the rise and fall times of the operational amplifier with the two-stage structure is dominated by drain current of MOS transistor, which is depended on threshold voltage V_{TH} in equation (3.23). The gate-oxide degradation will degrade the threshold voltage V_{TH} of the MOS transistor, so the rise and fall times of the operational amplifier with the two-stage structure will be changed under the DC stress.

The measurement setup for power supply rejection ratio (PSRR), a sinusoidal ripple of 100 mV is added to the power supply to measure the small-signal gain between the supply voltage and output pin voltage (V_{OUT}). The AC input signal at the power supply pin must include a DC bias that corresponds to the normal power supply voltage (2.5 V), so that the operational amplifiers operating in the unity-gain buffer remains powered up. The dependence of the PSRR on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 3.28. The PSRR of the operational amplifier with the two-stage structure under the DC stress is obviously changed, but that of the operational amplifier with folded-cascode structure is not changed. The PSRR of the operational amplifier with the two-stage structure under the unity-gain buffer configuration can be simple expressed as

$$PSRR = \frac{V_{out}}{V_{DD}} \cong \frac{r_{oM8}}{r_{oM8} + r_{oM9}}, \tag{3.24}$$

$$r_o = \frac{V_A}{I_D}, \tag{3.25}$$

where the V_A is the early voltage of the MOS transistor. The small-signal output resistance depends on the drain current in the MOS transistor. Therefore, the gate-oxide degradation will degrade the PSRR of the operational amplifier with the two-stage structure under the unity-gain buffer configuration during the DC stress.

3.2.3.2. AC Stress With DC Offset

The operational amplifiers under the configuration of the unity-gain buffer are continuously tested in the stress of the AC small-signal input with DC offset, as shown in Fig. 3.29. The non-inverting node of the operational amplifiers with the two-stage and folded-cascode structures is biased by the AC sinusoid signal of 500-mV (peak-to-peak amplitude) plus DC offset voltage of 1.25 V with different frequencies of 100 Hz, 500 kHz, and 1 MHz. The output capacitive load is set to 10 pF, and the supply voltage V_{DD} was set to 2.5 V. The measurement setup is used to investigate the relationship between gate-oxide reliability and different frequencies of input signals in the CMOS analog circuit applications.

The dependence of the unity-gain frequency in the unity-gain buffers on the stress time under the stress of the AC small-signal input with DC offset is shown in Fig. 3.30. The performances of the operational amplifier with folded-cascode structure are not degraded by the stress of the AC small-signal input with DC offset. In the operational amplifier with the two-stage structure, the high- frequency input signal causes a slow degradation on the unity-gain frequency, but the low-frequency input signal causes a fast degradation on the unity-gain frequency under the stress of the AC small-signal input with DC offset. The dependences of the small-signal gain and phase margin in the unity-gain buffers on the stress time under the stress of the AC small-signal input with DC offset are almost the same as the change under the DC stress. Because the different frequencies of the input signal have different periods, the period of the high-frequency input signal has shorter time than that of the low-frequency input signal. The MOS transistors in analog circuits usually work in the saturation region, so that the gate-oxide breakdown is more likely to occur in

conventional time-dependent dielectric breakdown (TDDB). Therefore, the small-signal performance of the non-stacked common-source amplifier with different frequencies of the input signal will cause different degradation time under the stress of the AC small-signal input with DC offset. As a result, the gate-oxide breakdown degrades the performances of the operational amplifier with the two-stage structure under the AC stress with DC offset. The operational amplifier with the folded-cascode structure under the AC stress can be still functioned correctly in high supply voltage (2.5 V) to overcome the gate-oxide reliability.

3.2.3.3. Large-Signal Transition

The operational amplifiers under the comparator (open-loop) configuration are used to investigate the impact of gate-oxide reliability on CMOS analog circuits under the large-signal transition. The inverting input node of the operational amplifiers is biased at 1.25 V, the output capacitance load is set to 10 pF, and the supply voltage V_{DD} is set to 2.5 V. The operational amplifiers under the comparator configuration are continuously tested in this stress of large-signal transition, as shown in Fig. 3.31. The input square voltage waveform from 1 V to 1.5 V with frequency of 100 Hz is applied to the non-inverting input node of the operational amplifiers under the comparator configuration. The square waveform of input signal from 1 V to 1.5 V will not induce the damage on the input devices of the operational amplifiers, because the voltages across the input devices (V_{GS}, V_{GD}, and V_{DS}) of the operational amplifiers are lower than the 1 V in this measurement.

The dependences of the high- and low-voltage levels at the output node on the stress time are show in Fig. 3.32, where the operational amplifiers with the two-stage or folded-cascode structures in the comparator configuration are stressed by the large-signal transition. The low output voltage level of the operational amplifier with the two-stage structure under the stress of large-signal transition is increased when the stress time is increased. But the high output voltage level of the operational amplifier with two-stage structure is not changed after the same stress condition. The high and low voltage levels at the output node of the operational amplifier with the folded-cascode structure after the 7-day stress of large-signal transition are not changed. The dependence of the unity-gain frequency on the stress time under the

stress of large-signal transition is shown in Fig. 3.33, where the operational amplifiers with the two-stage or folded-cascode structures are connected in the comparator configuration. The unity-gain frequency of the operational amplifiers with the two-stage and folded-cascode structure connected as unity-gain buffer is degraded after the stress of large-signal transition. The reason, why the circuit performances of the operational amplifiers with the two-stage and folded-cascode structures, such as small-signal gain and unity-gain frequency, is degraded with the overstress, is summed up to that the gate-oxide breakdown will degrade the transconductance (g_m), threshold voltage (V_{TH}), and output conductance (g_o) of the MOS transistor. The approximate high and low output voltage levels of the operational amplifier with the two-stage and folded-cascode structures are near the V_{DD} and ground levels, respectively, under the comparator configuration. In this case, the V_{DD} level is set to 2.5 V, and ground level is set to 0 V. The output-stage devices of the operational amplifiers with the two-stage and folded-cascode structures will be degraded with gate-oxide degradation, so the performances of the operational amplifiers with the two-stage and folded-cascode structures will be degraded under the large-signal transition stress.

3.2.4. Discussion

The summary of overstress results under three overstress conditions (DC, AC, and large-signal transition stresses) is listed in Table 3.4. The gate-oxide breakdown will degrade the transconductance (g_m), output resistance (r_o), and threshold voltage (V_{th}) of MOSFET devices. After the overstress, the performances of the two-stage operational amplifiers under close-loop and open-loop configurations are degraded. Because the differential amplifier of the operational amplifier with the two-stage structure consists of three cascode MOSFET devices, the voltages across the devices in the differential amplifier of the operational amplifier with the two-stage structure do not exceed 1 V under the stress with the input common-mode voltage of 1.25 V and supply voltage of 2.5 V. The differential amplifier of the operational amplifier with the two-stage structure is not degraded under the stresses with the supply voltage of 2.5 V. However, the output stage in the operational amplifier with the two-stage structure will be degraded under the stress with the input common-mode voltage of

1.25 V and supply voltage of 2.5 V. Therefore, the open-loop gain of the operational amplifier with the two-stage structure is decreased after the stresses. The offset voltage due to the finite gain error of the operational amplifier with the two-stage structure is increased after the stress.

The rise time, fall time, output voltage swing, and phase margin of the operational amplifier with the two-stage structure are also decreased after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure. The DC operating point is very important in the analog circuit design, because all small-signal parameters of the devices and circuits are determined by the DC operating point. If the DC operating point is changed after gate-oxide degradation, the analog circuits will not work correctly. However, the large-signal transition at input and output nodes of the operational amplifier with stacked structure still causes some degradations on circuit performances of analog circuits. As a result, the analog circuits with stacked structure are only effective to improve the gate-oxide reliability under small-signal applications at input and output nodes.

Under the same stress condition, the two-stage operational amplifier under close-loop (negative-feedback) configuration can be more easily stressed than that under open-loop configuration. The close-loop configuration in the operational amplifiers is used to make the circuits stable and keep the virtual short between inverting and non-inverting nodes of the operational amplifiers. Therefore, the inverting, non-inverting, and output nodes of the operational amplifiers have the same DC voltage level under the configuration of negative feedback. The transconductance (g_m), output resistance (r_o), and threshold voltage (V_{TH}) of MOSFET devices will be changed after the stress. In order to make the circuits stable and to keep the virtual short between the two input nodes of the operational amplifier with the two-stage structure, the DC operating point of the output stage in the two-stage operational amplifier will be changed after the stress. Therefore, the power consumption (circuit performances) of the operational amplifier with the two-stage structure under the negative-feedback configuration will be increased (degraded) after the stress.

3.2.5. Effect of Hard and Soft Gate-Oxide Breakdown on Performances of Operational Amplifier

3.2.5.1. DC Stress

After oxide breakdown, the measured output voltage swing waveform of operational amplifier with the two-stage structure after DC stress, as shown in Fig. 3.20, is shown in Fig. 3.34. Based on the prior proposed method [81], [90], the gate-oxide breakdown of MOSFET device can be modeled as resistance. Only the gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst-case situation. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard breakdown leakage has close-to-linear I-V behavior and an equivalent resistance of ~ 10^3-10^4 Ω, while typical soft breakdown paths have high non-linear, power law I-V behavior and equivalent resistance above 10^5-10^6 Ω [82]. The complete circuit of the operational amplifier with the two-stage structure including gate-oxide breakdown model is shown in Fig. 3.35. The breakdown resistances of R_{BD6}, R_{BD7} and R_{BD8} can be used to simulate the impact of hard and soft breakdowns on performances of the operational amplifier with the two-stage structure. The non-inverting node of the operational amplifiers with the two-stage structure is biased by the AC sinusoid signal of 500-mV (peak-to-peak amplitude) plus DC offset voltage of 1.25 V with frequency of 5 kHz. The output capacitive load is set to 10 pF, and the supply voltage V_{DD} was set to 2.5 V. The simulated output voltage swing waveform of operational amplifier with the two-stage structure under different breakdown resistances R_{BD6}, R_{BD7}, and R_{BD8} is shown in Fig. 3.36. Comparing with Fig. 3.34, the hard breakdowns have been occurred on M_6, M_7, and M_8 devices in two-stage operational amplifier after DC stress.

3.1.5.2. Large-Signal Transition Stress

In order to investigate and understand the impact of hard and soft breakdowns on performances of the operational amplifier with the two-stage structure under large-signal transition stress, the complete circuits including the gate-oxide breakdown model are shown in Fig. 3.37. The simulated dependence of high and low

output voltage levels of the operational amplifier with the two-stage structure under the different resistances R_{BD8} and R_{BD9} is shown in Fig. 3.38. The high output voltage level and low output voltage level of operational amplifier with the two-stage structure are degraded by oxide breakdown occurred on M_8 and M_9 devices, respectively. Comparing Figs. 3.32 and 3.38, the breakdown location in the operational amplifier with the two-stage structure is occurred on M_8 and M_9 devices after large-signal transition stress.

3.2.6. Summary

The impact of MOSFET gate-oxide reliability on CMOS operational amplifiers with the two-stage (non-stacked) and folded-cascode (stacked) structures has been investigated and analyzed. The tested structures of the operational amplifiers including both the unity-gain buffer (close-loop) and comparator (open-loop) configurations are stressed under different input frequencies and signals. Because the DC operating point of the analog circuits is changed due to the gate-oxide degradation, the small-signal performances of the operational amplifier with the two-stage structure are seriously degraded after the stress. The performances of the operational amplifier with the two-stage structure under the close-loop configuration are damaged more easily than that under the open-loop configuration after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure under small-signal input and output applications. But, the large-signal transition still causes some degradation on the circuit performances of the operational amplifier with the folded-cascode (stacked) structure.

3.3. Conclusion

Chapter 3 has investigated and analyzed the impact of gate-oxide breakdown on CMOS analog amplifiers. The impact of gate-oxide reliability on CMOS common-source amplifiers with the non-stacked and stacked diode-connected active load structures has been investigated and analyzed under the DC stress, AC stress with DC offset, and large-signal transition stress. The small-signal parameters of the common-source amplifier with the non-stacked diode-connected active load structure

are seriously degraded than that with non-stacked diode-connected active load structure by gate-oxide breakdown under DC, AC, and large-signal transition stresses. The stacked structure can be used to improve the reliability of analog circuit in nanoscale CMOS process. The impact of soft breakdown, hard breakdown, and breakdown location on circuit performances of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures has been investigated and analyzed. The hard gate-oxide breakdown has more serious impact on performances of the common-source amplifier with the diode-connected active load. The impact of MOSFET gate-oxide reliability on CMOS operational amplifiers with the two-stage (non-stacked) and folded-cascode (stacked) structures has been investigated and analyzed. The tested structures of the operational amplifiers including both the unity-gain buffer (close-loop) and comparator (open-loop) configurations are stressed under different input frequencies and signals. Because the DC operating point of the analog circuits is changed due to the gate-oxide degradation, the small-signal performances of the operational amplifier with the two-stage structure are seriously degraded after the stress. The performances of the operational amplifier with the two-stage structure under the close-loop configuration are damaged more easily than that under the open-loop configuration after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure under small-signal input and output applications. But, the large-signal transition still causes some degradation on the circuit performances of the operational amplifier with the folded-cascode (stacked) structure. The optimized design solution to further overcome such degradation from the stress of large-signal transition on the operational amplifiers should be an important challenge to analog circuits in the nanoscale CMOS technology.

Table 3.1

Device Dimensions of Common-Source Amplifiers With the Non-Stacked and Stacked Diode-Connected Active Load Structures

Device	Dimension	Device	Dimension
M_1	8μ/1μ	M_4	2μ/1μ
M_2	1μ/1.5μ	M_5	1μ/1μ
M_3	1.8μ/1μ	M_6	1μ/1μ

Table 3.2

Comparisons of Common-Source Amplifiers With the Non-Stacked and Stacked Diode-Connected Active Load Structures among Three Overstress Conditions

Stress Conditions	Performances	Non-Stacked	Stacked
DC Stress	Small-Signal Gain	Seriously Degraded	No Change
	Unity-Gain Frequency	Seriously Degraded	No Change
	Output DC Voltage Level	Seriously Degraded	No Change
AC Stress with DC Offset	Small-Signal Gain	• High Frequency → Slow Degraded Rate • Low Frequency → High Degraded Rate	No Change
Large-Signal Transition Stress	High and Low Output Voltage Levels	Seriously Degraded	Degraded

Table 3.3

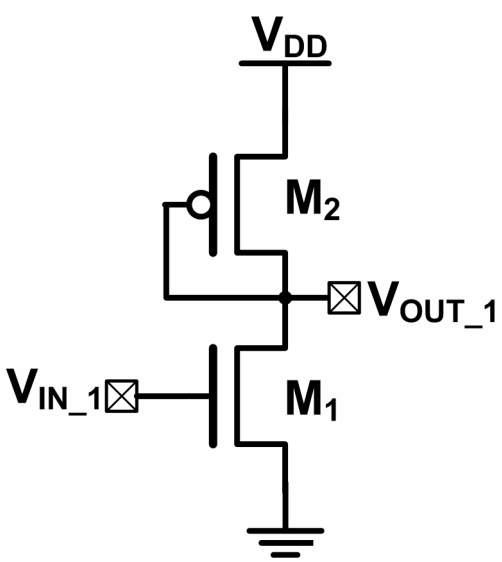
Device Dimensions of Operational Amplifiers With the Two-Stage or Folded-Cascode Structures

Device	Dimension	Device	Dimension
M_1	12.5μ/0.5μ	M_{11}	25μ/0.5μ
M_2	12.5μ/0.5μ	M_{12}	8μ/0.5μ
M_3	1μ/0.5μ	M_{13}	2μ/0.5μ
M_4	2μ/0.5μ	M_{14}	2μ/0.5μ
M_5	2μ/0.5μ	M_{15}	1μ/0.5μ
M_6	4μ/1μ	M_{16}	1μ/0.5μ
M_7	1μ/1μ	M_{17}	4μ/0.5μ
M_8	15μ/0.5μ	M_{18}	4μ/0.5μ
M_9	1.8μ/1μ	M_{19}	4μ/0.5μ
M_{10}	25μ/0.5μ	M_{20}	4μ/0.5μ

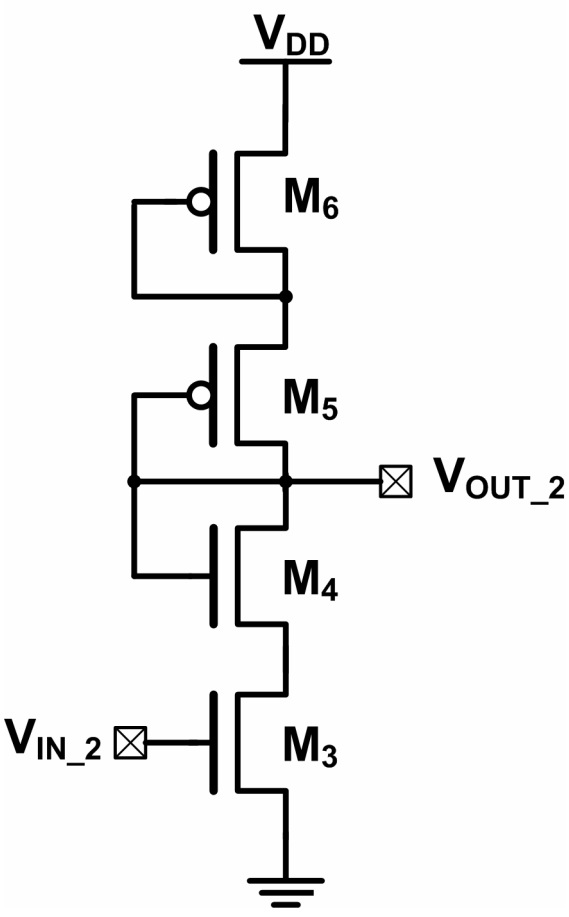
Table 3.4

Comparisons of Operational Amplifiers With the Two-Stage or Folded-Cascode Structures among Three Overstress Conditions

Stress Conditions	Performances	Two-Stage	Folded-Cascode
DC Stress	Small-Signal Gain	Seriously Degraded	No Change
	Unity-Gain Frequency	Seriously Degraded	No Change
	Output Voltage Swing	Seriously Degraded	No Change
AC Stress With DC Offset	Small-Signal Gain	• High Frequency → Slow Degraded Rate • Low Frequency → High Degraded Rate	No Change
Large-Signal Transition Stress	High and Low Output Voltage Levels	Seriously Degraded	No Change
	Unity-Gain Frequency	Seriously Degraded	Degraded



(a)



(b)

Fig. 3.1. Complete circuits of the common-source amplifiers with the (a) non-stacked and (b) stacked diode-connected active load structures.

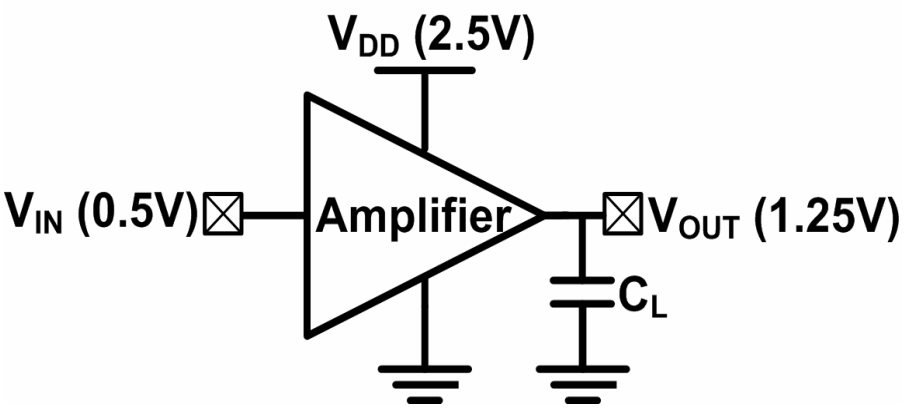


Fig. 3.2. The measured setup for common-source amplifiers with the non-stacked and stacked diode-connected active load structures under DC stress to investigate the impact of gate-oxide reliability to circuit performances.

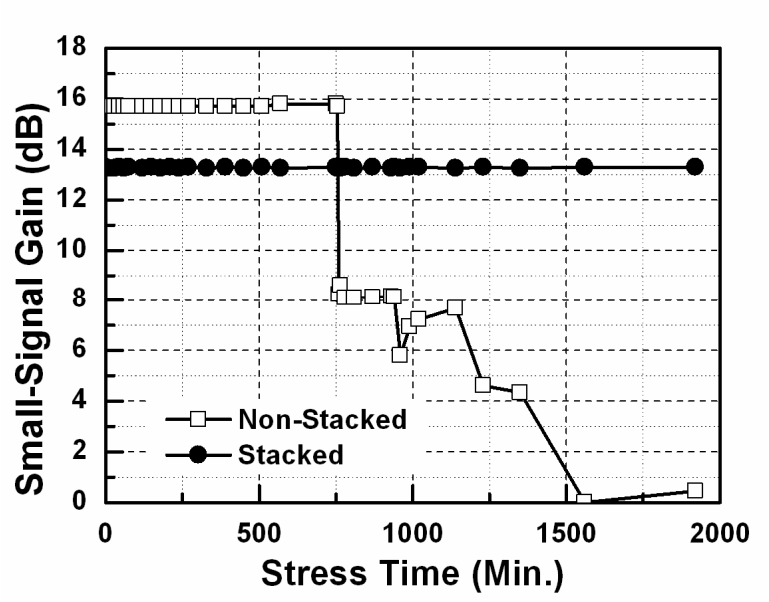
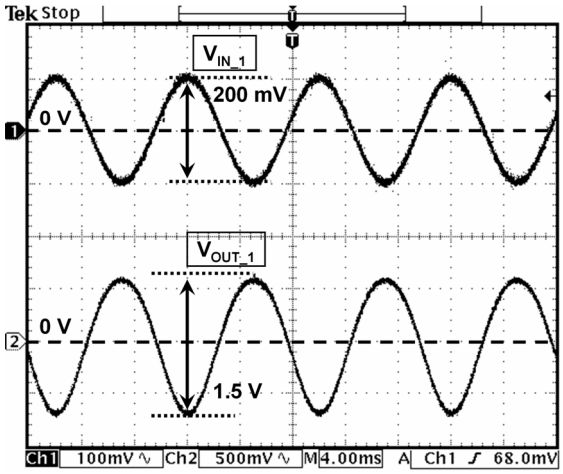
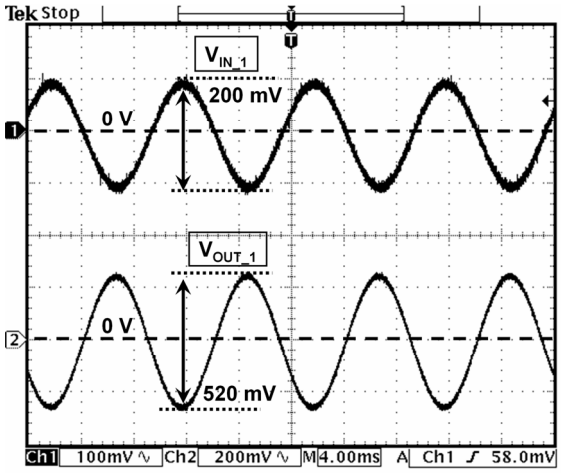


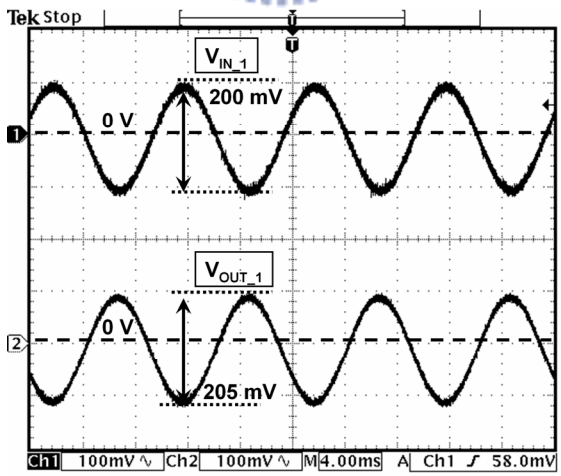
Fig. 3.3. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress.



(a)



(b)



(c)

Fig. 3.4. The input and output signal waveforms on the different stress times of the common-source amplifier with the non-stacked diode-connected active load structure under the DC stress. (a) Stress time = 0 min., (b) Stress time = 980 min., and (c) Stress time = 2000 min.

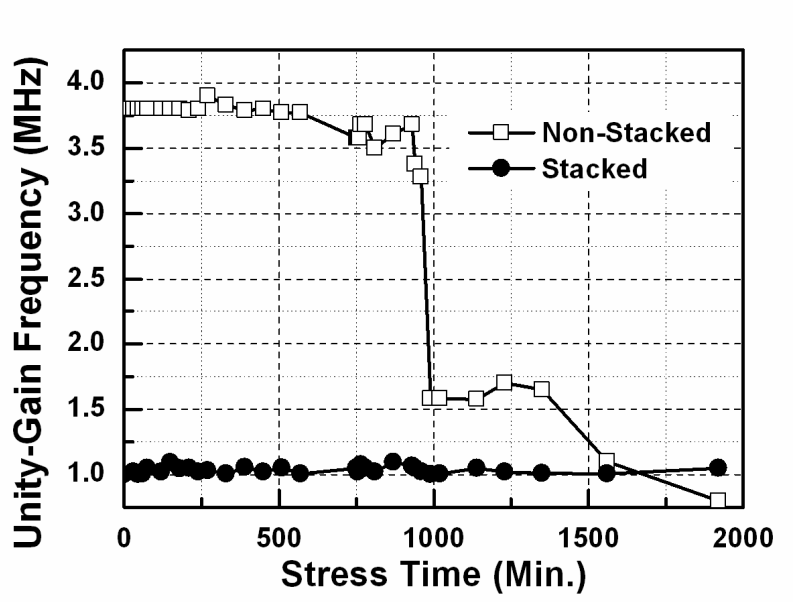


Fig. 3.5. The dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress.

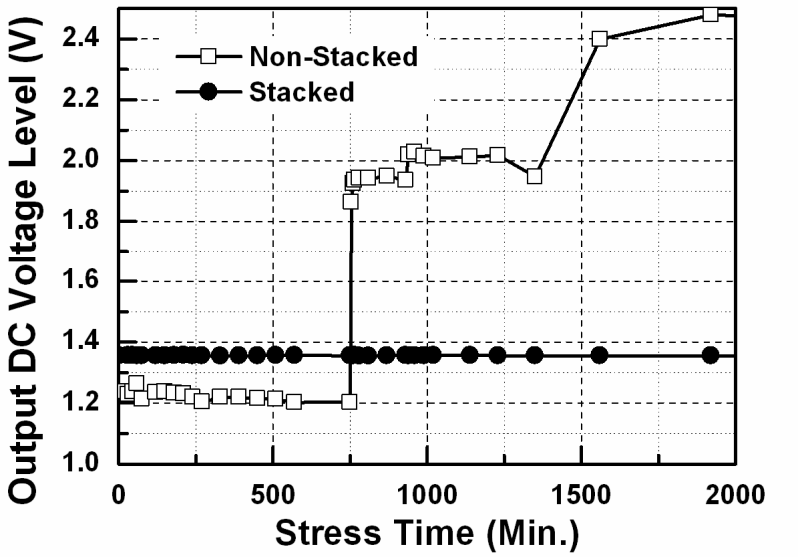


Fig. 3.6. The dependence of the output DC voltage level on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the DC stress.

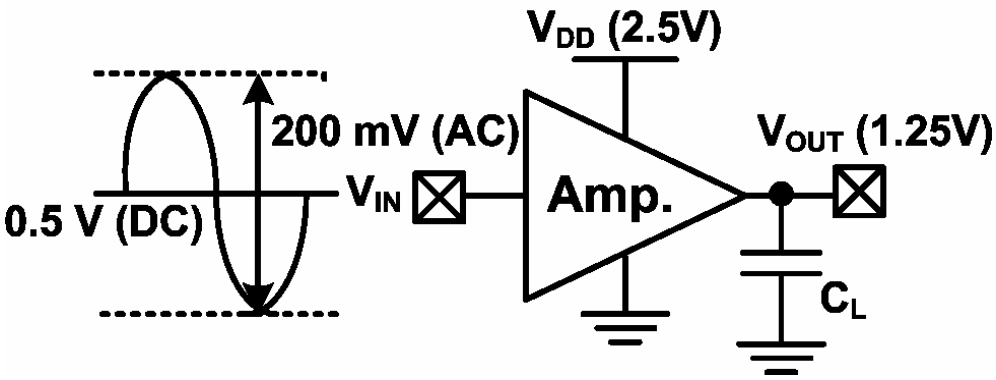


Fig. 3.7. The measured setup for common-source amplifiers with the non-stacked and stacked diode-connected active load structures under AC stress with DC offset to investigate the impact of gate-oxide reliability to circuit performances.

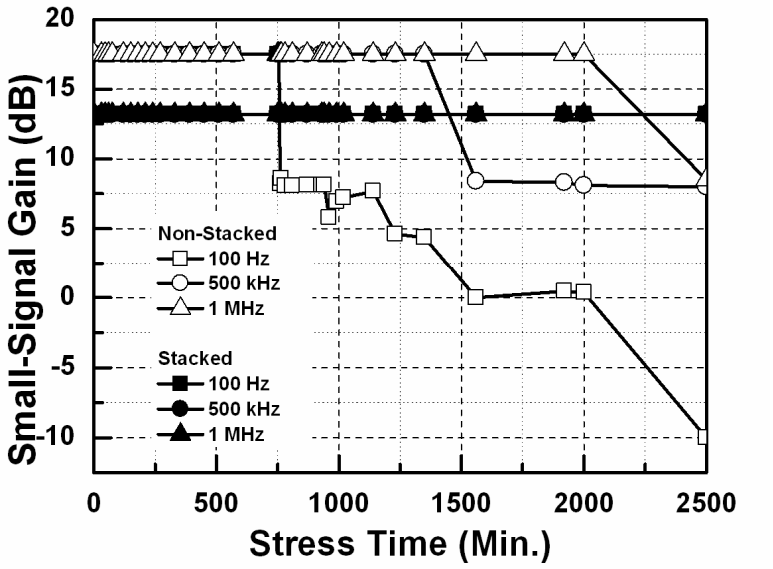


Fig. 3.8. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures under the stress of the AC small-signal input with DC offset.

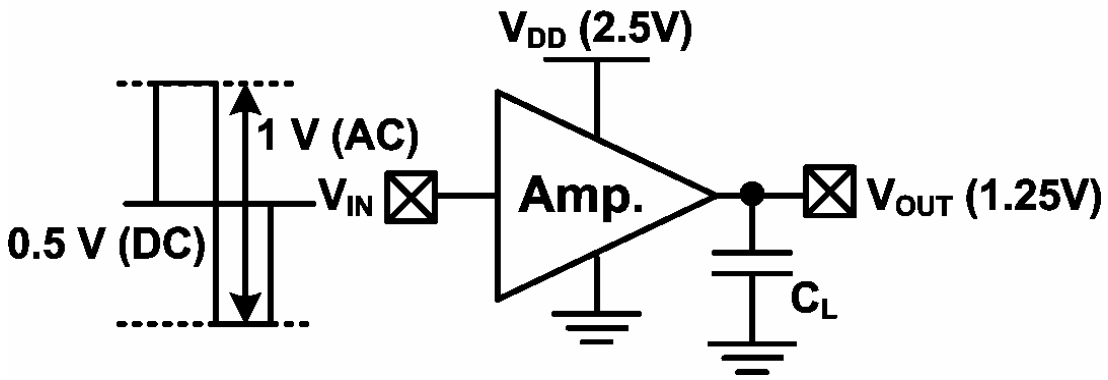


Fig. 3.9. The measured setup for common-source amplifiers with the non-stacked and stacked diode-connected active load structures under large-signal transition stress to investigate the impact of gate-oxide reliability to circuit performances.

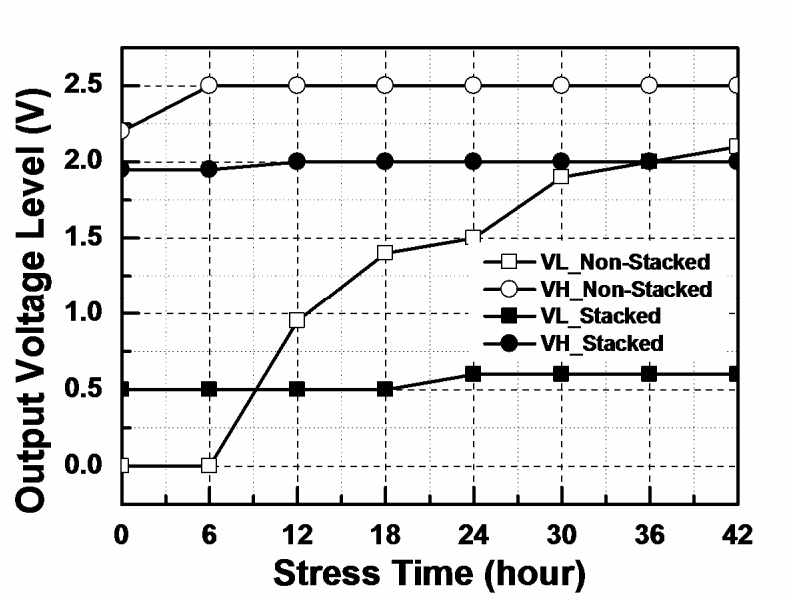
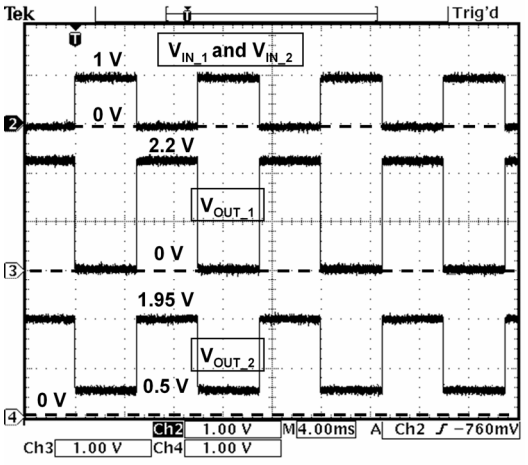
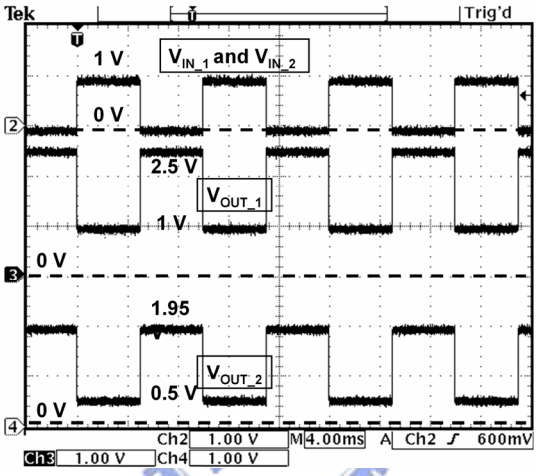


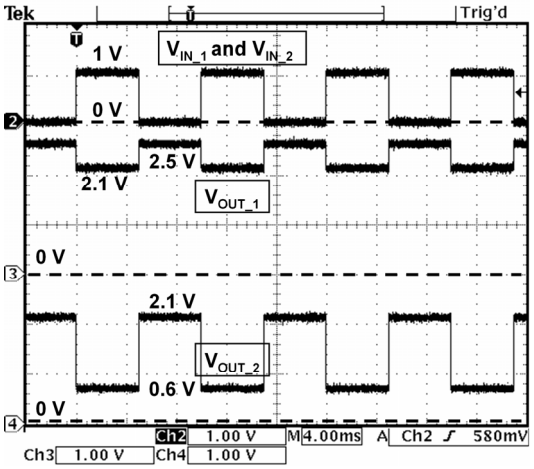
Fig. 3.10. The dependences of the high and low output voltage levels (VH and VL) at the output nodes of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on the stress time under stress of large-signal transition.



(a)



(b)



(c)

Fig. 3.11. The input and output signal waveforms on the different stress times of the common-source amplifier with the non-stacked and stacked diode-connected active load structures under the large-signal transition stress. (a) Stress time = 0 hour, (b) Stress time = 12 hours, and (c) Stress time = 42 hours.

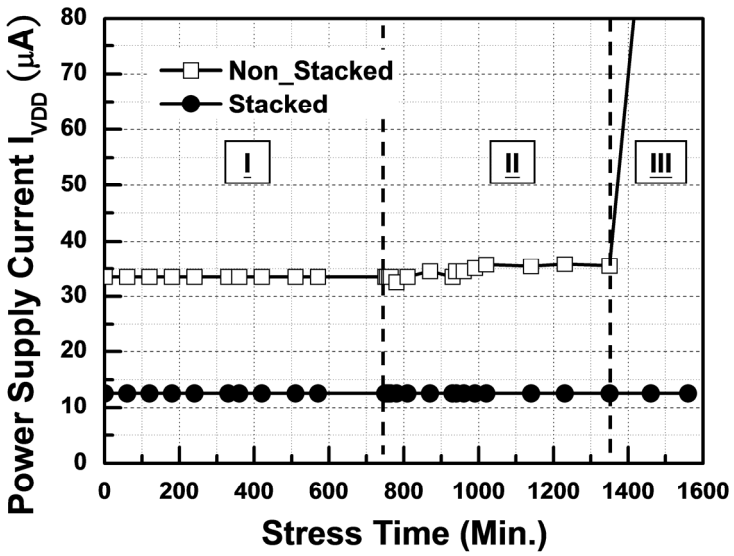


Fig. 3.12. The measured dependence of power supply current I_{VDD} of the common-source amplifiers with the non-stacked and stacked diode-connected active load structures on stress time under DC stress.

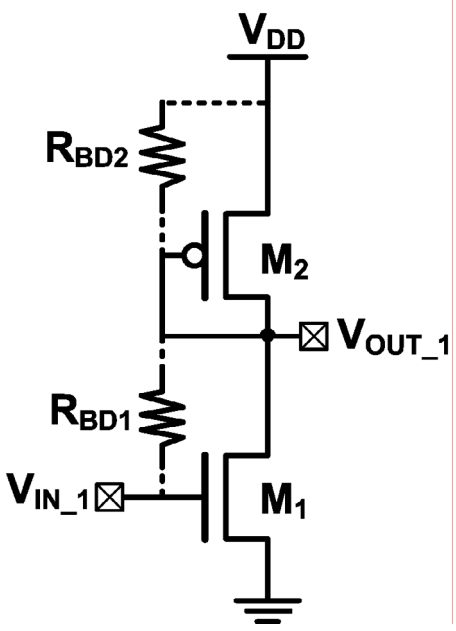


Fig. 3.13. The complete circuit of the common-source amplifier with the non-stacked diode-connected active load structure including the gate-oxide breakdown model.

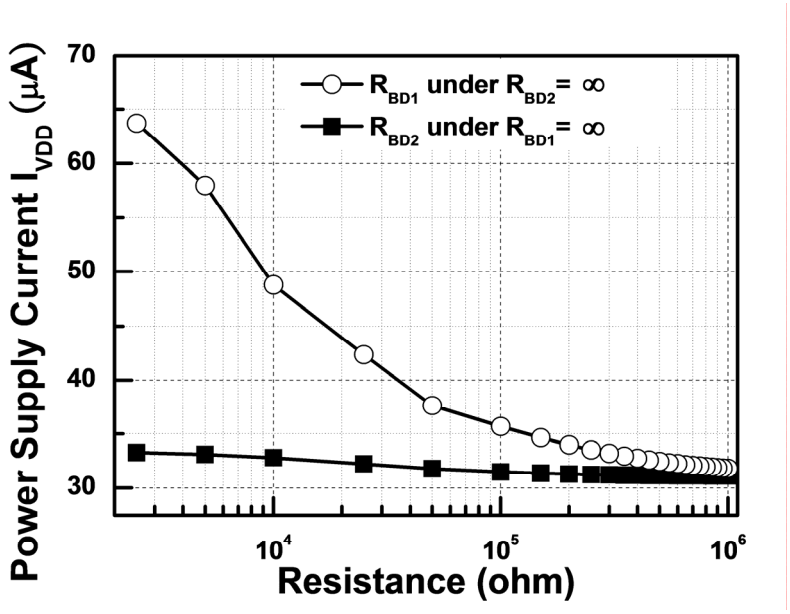


Fig. 3.14. The simulated dependence of power supply current I_{VDD} of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances of R_{BD1} and R_{BD2}.

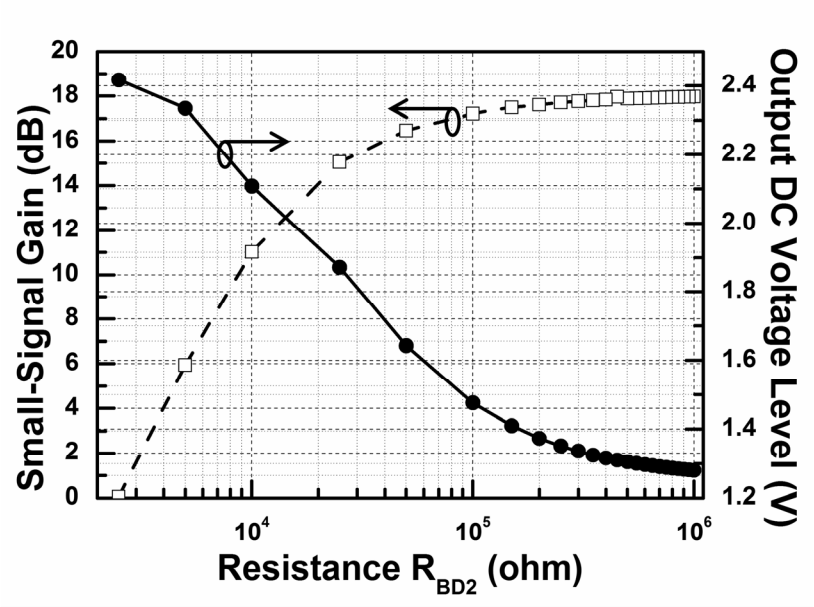


Fig. 3.15. The simulated dependence of small-signal gain and output DC voltage level of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances R_{BD2}.

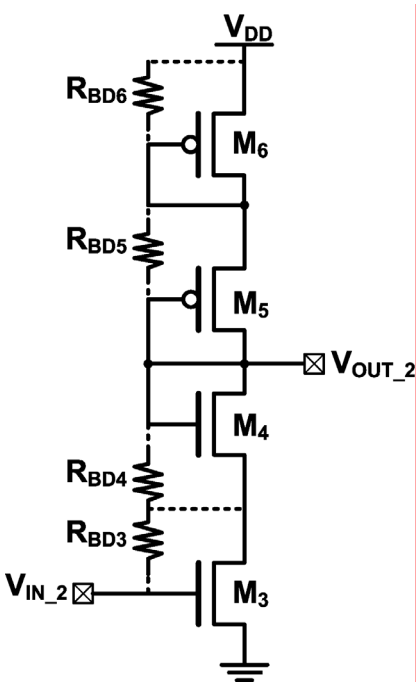


Fig. 3.16. The complete circuit of the common-source amplifier with the stacked diode-connected active load structure including the gate-oxide breakdown model after large-signal transition stress.

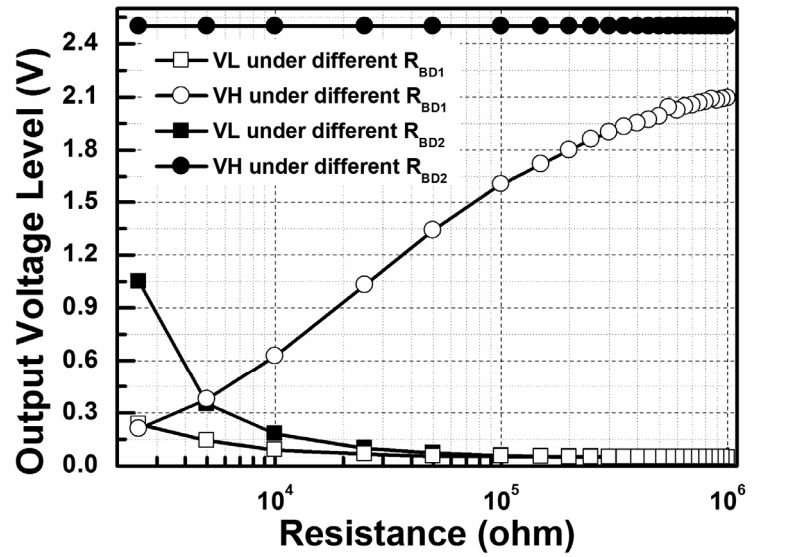


Fig. 3.17. The simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifier with the non-stacked diode-connected active load structure under different resistances of R_{BD1} and R_{BD2} after large-signal transition stress.

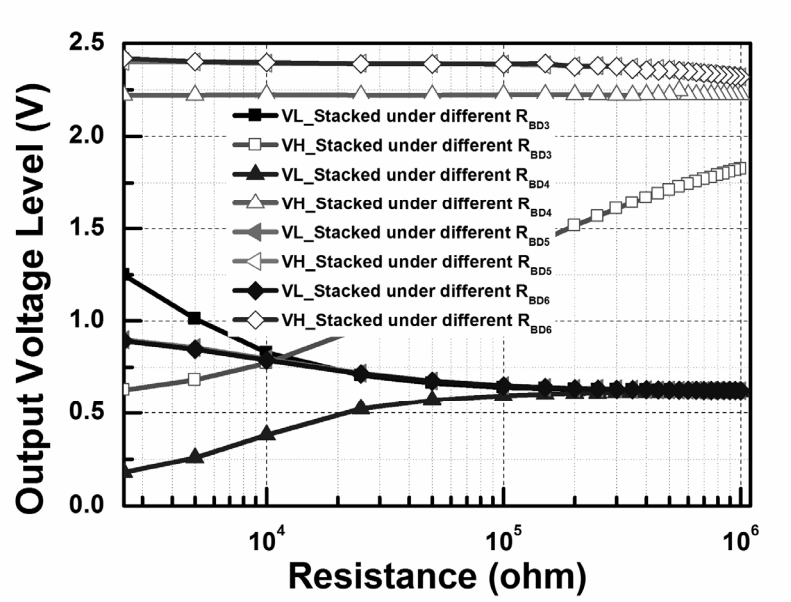
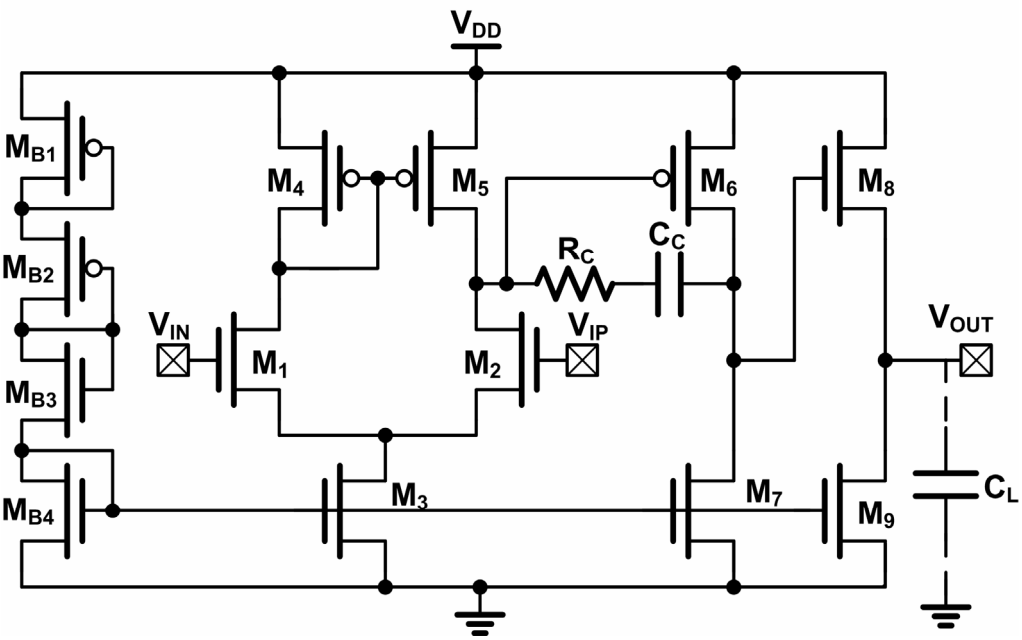
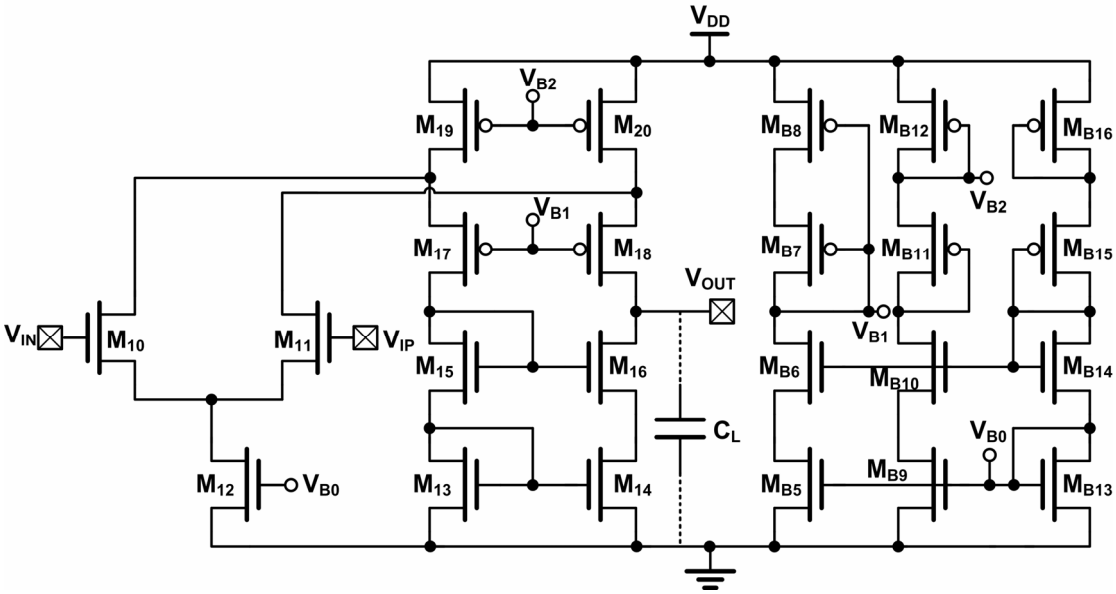


Fig. 3.18. The simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active load structure under different resistances of R_{BD3}, R_{BD4}, R_{BD5}, and R_{BD6} after large-signal transition stress.



(a)



(b)

Fig. 3.19. The complete circuits of the operational amplifiers with the (a) two-stage and (b) folded-cascode circuit structures.

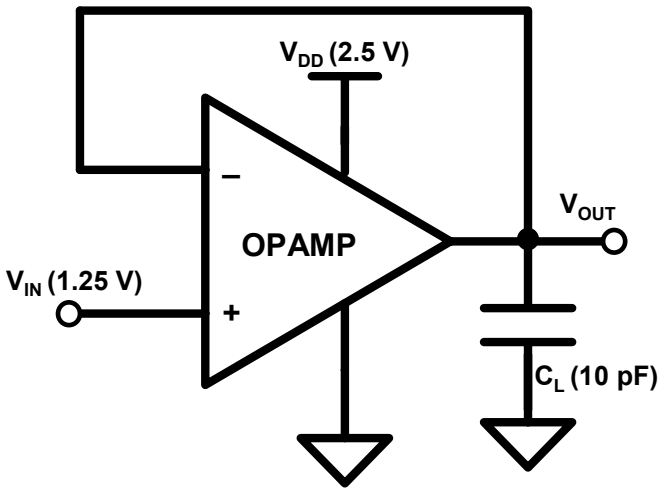
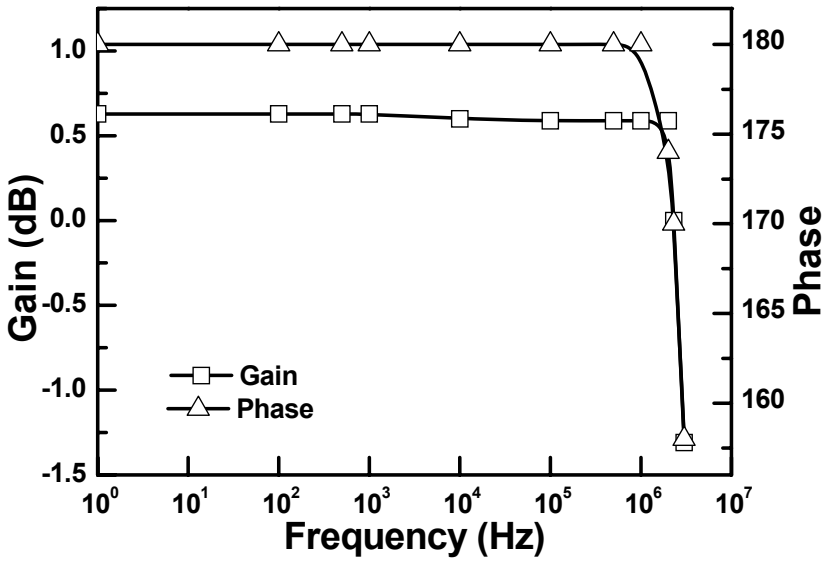
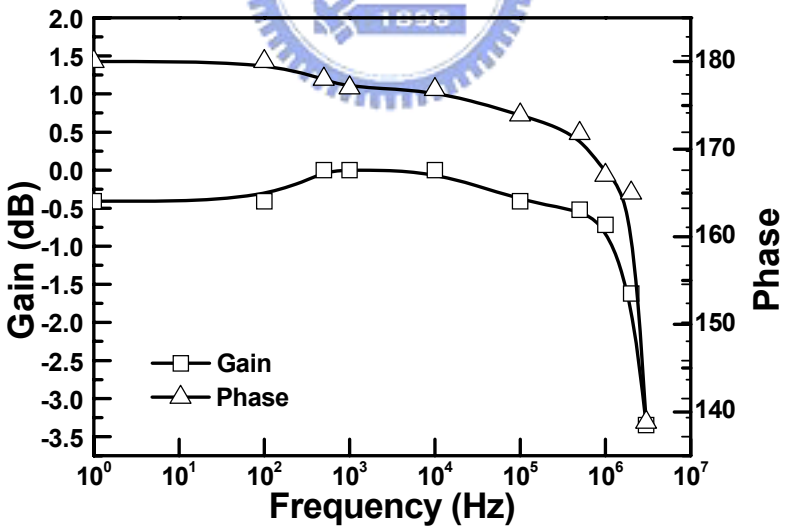


Fig. 3.20. The unity-gain buffer configuration for operational amplifiers under DC stress to investigate the impact of gate-oxide reliability to circuit performances.



(a)



(b)

Fig. 3.21. The fresh frequency responses of the operational amplifiers with the (a) two-stage, and (b) folded-cascode, structures operating in the unity-gain buffer.

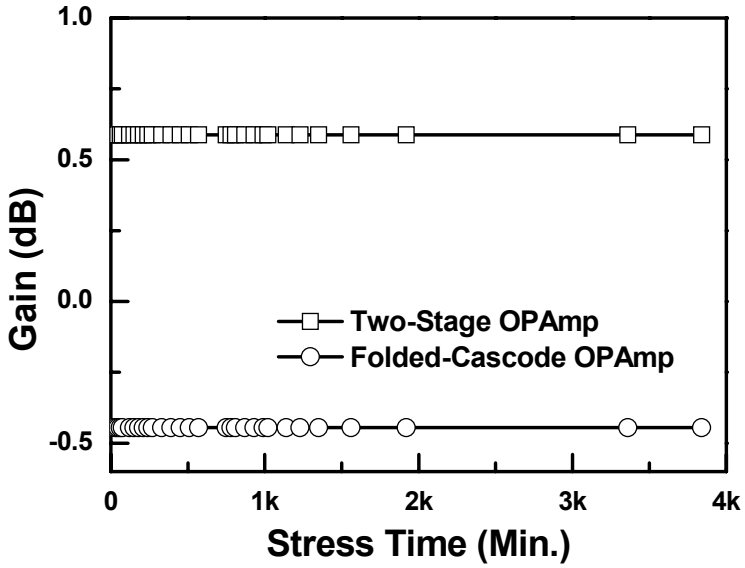


Fig. 3.22. The dependence of the small-signal gain on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress.

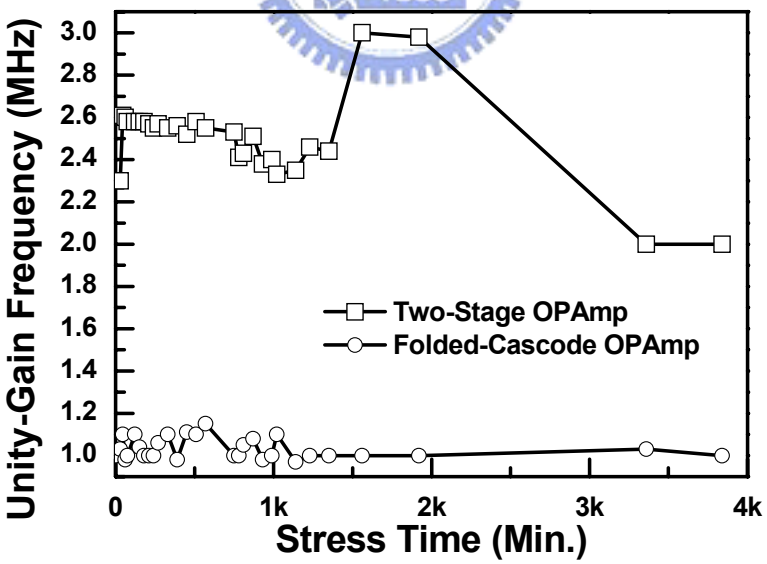


Fig. 3.23. The dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress.

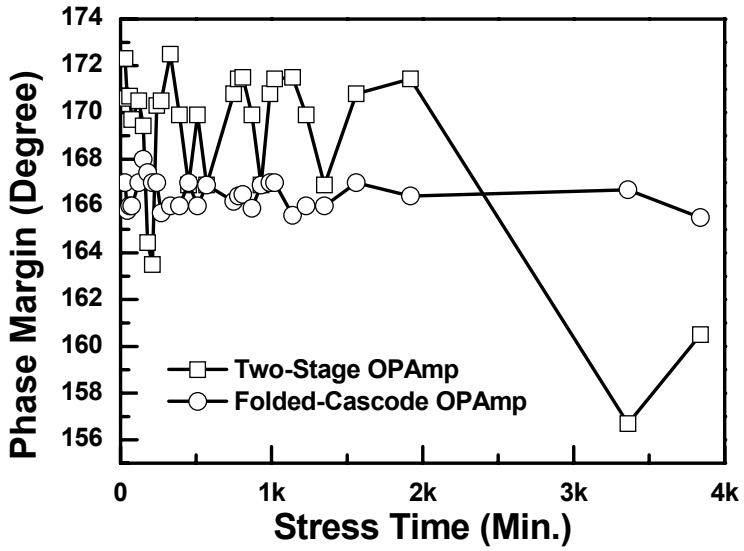


Fig. 3.24. The dependence of the phase margin on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress.

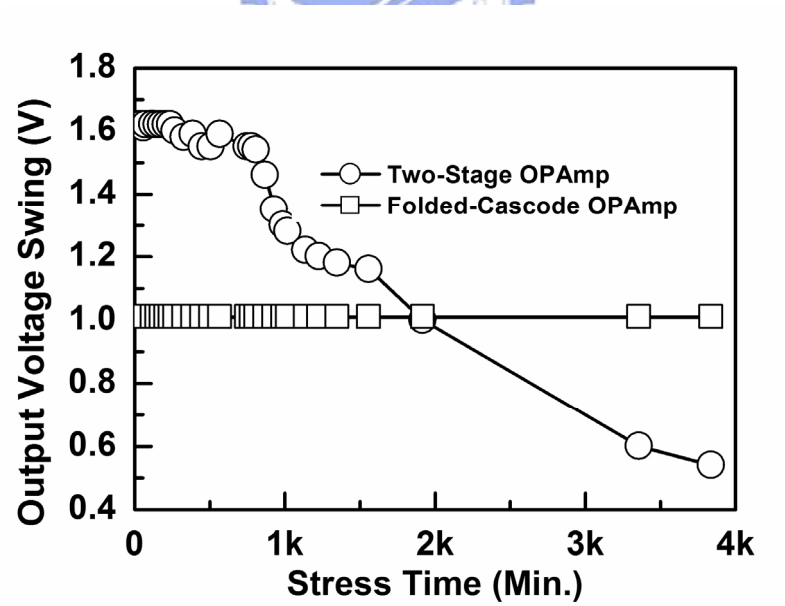


Fig. 3.25. The dependence of the output-voltage swing on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress.

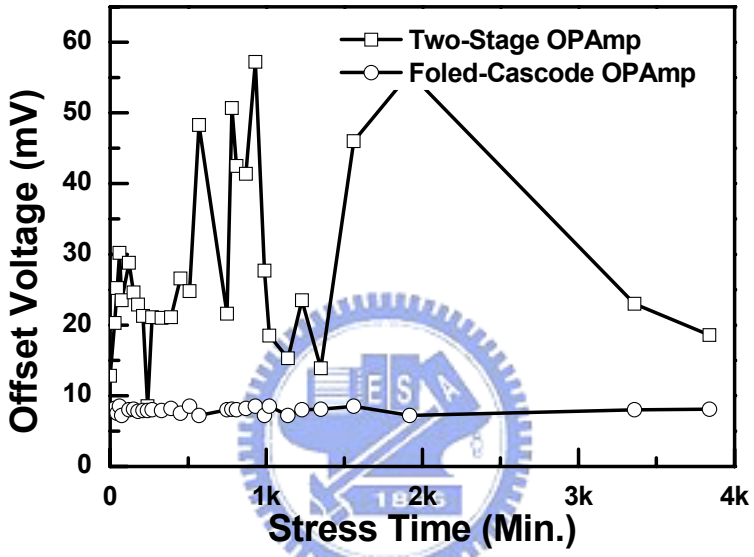
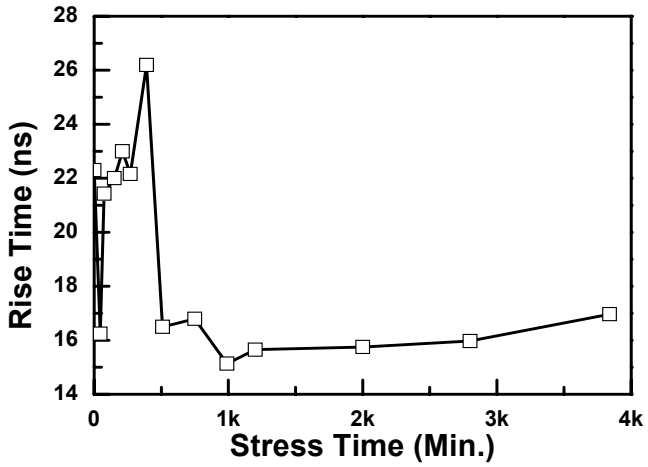
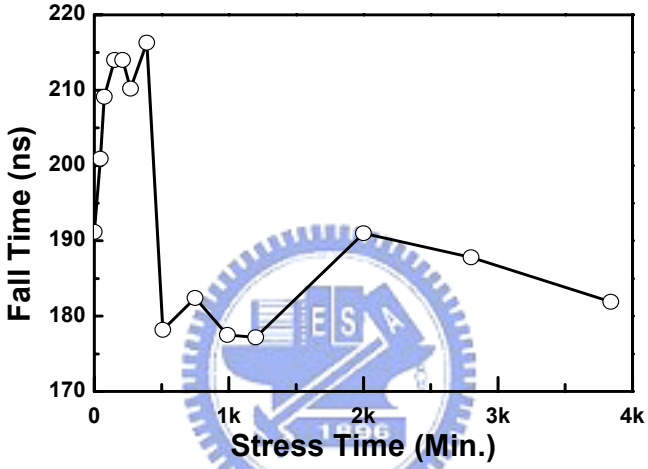


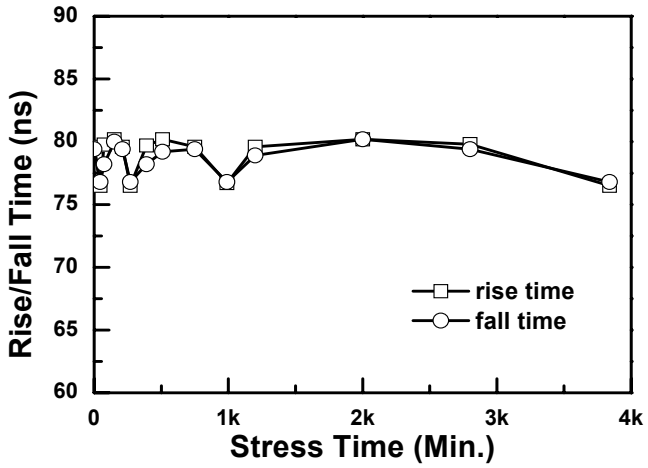
Fig. 3.26. The dependence of the offset voltage on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress.



(a)



(b)



(c)

Fig. 3.27. The dependence of the rise and fall times on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress. (a) and (b) two-stage operational amplifier. (c) folded-cascode operational amplifier.

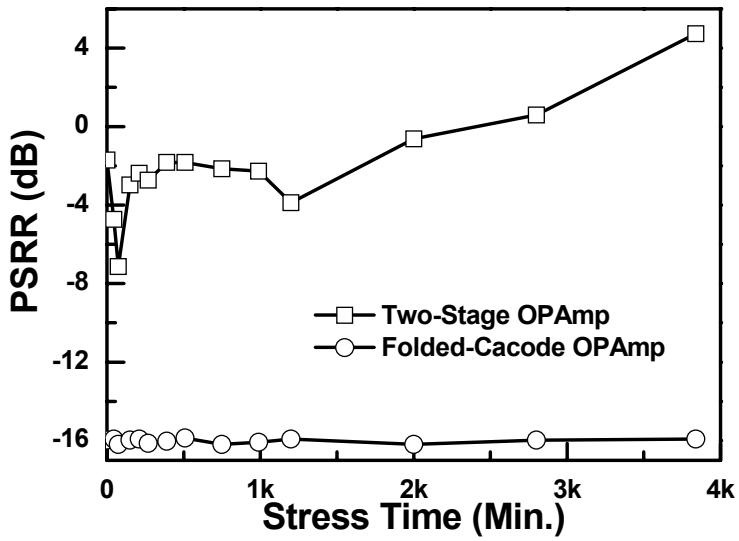


Fig. 3.28. The dependence of the PSRR on the stress time of the operational amplifiers with the two-stage or folded- cascode structures operating in the unity-gain buffer under the DC stress.

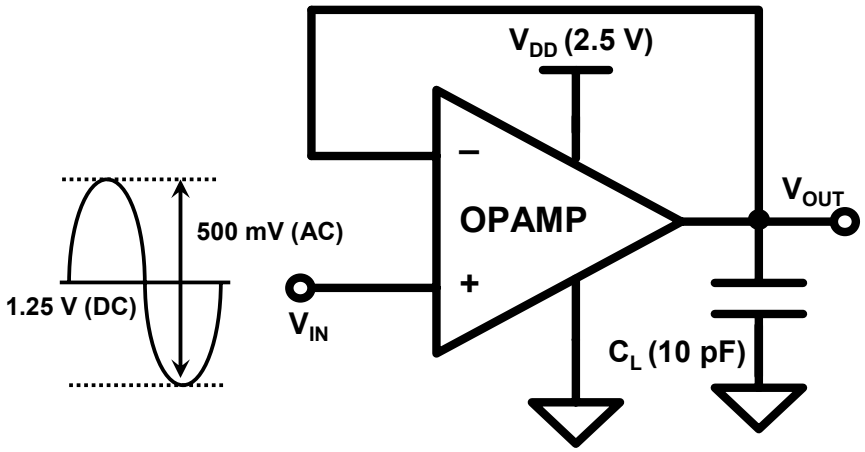


Fig. 3.29. The unity-gain buffer configuration for operational amplifiers under the stress of AC small-signal input with DC offset to investigate the impact of gate-oxide reliability to circuit performances.

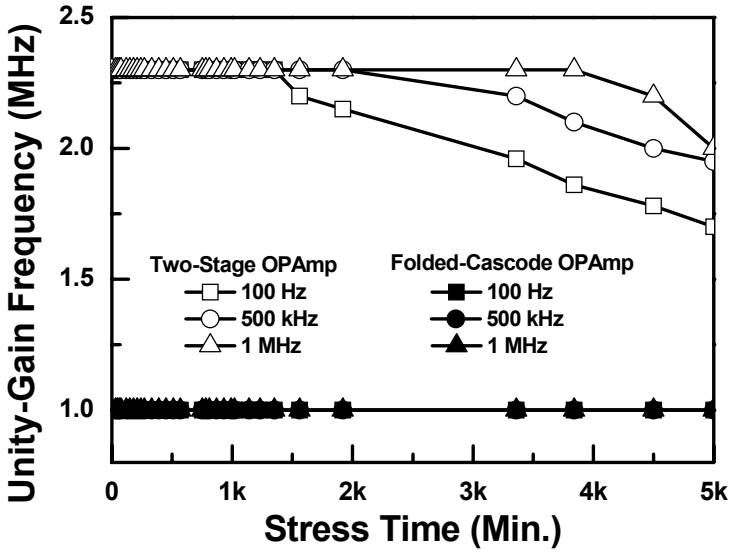


Fig. 3.30. The dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage structure under the stress of the AC small-signal input with DC offset.

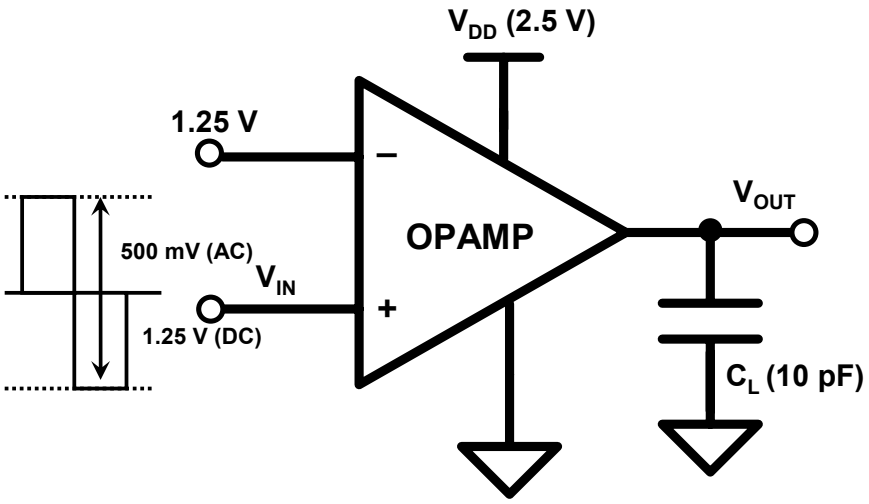


Fig. 3.31. The comparator configuration for operational amplifiers under the stress of large-signal transition to investigate the impact of gate-oxide reliability to circuit performances.

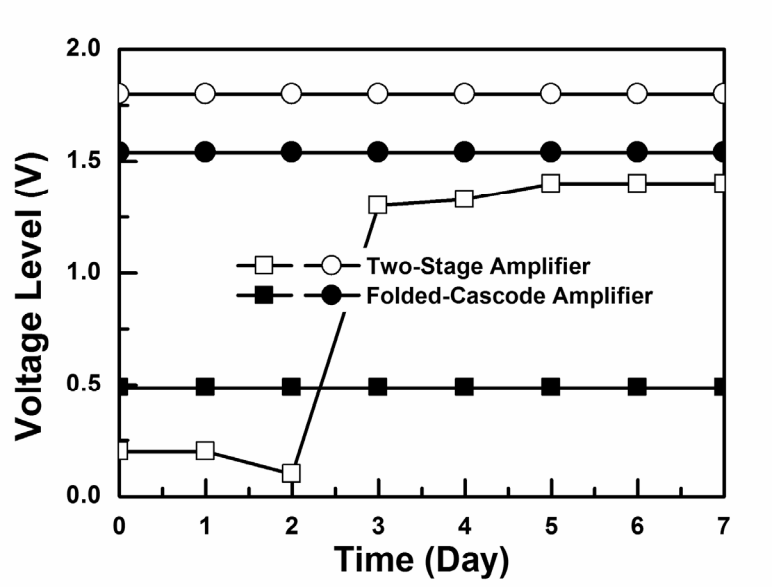


Fig. 3.32. The dependences of the high and low voltage levels at the output node on the stress time under stress of large-signal transition. The operational amplifiers with the two-stage or folded-cascode structures are stressed under the comparator configuration.

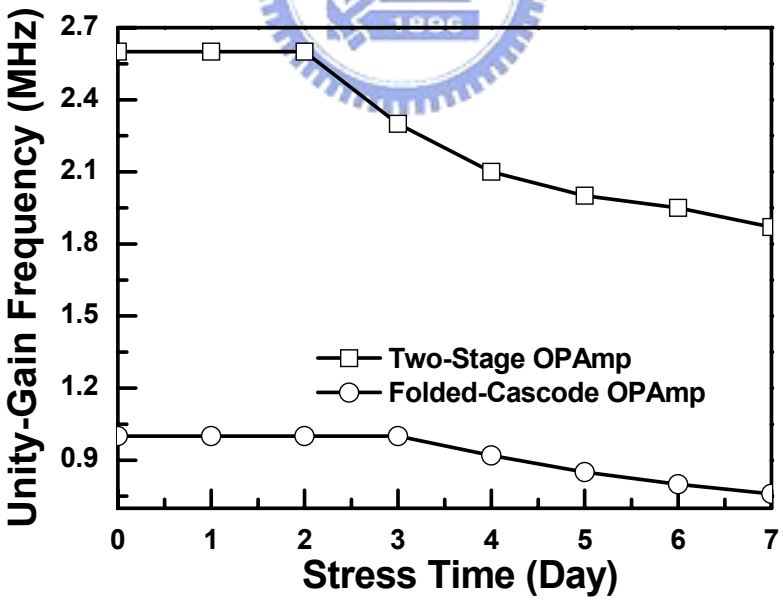


Fig. 3.33. The dependence of the unity-gain frequency on the stress time under the stress of large-signal transition. The operational amplifiers with the two-stage or folded-cascode structures are stressed under the comparator configuration.

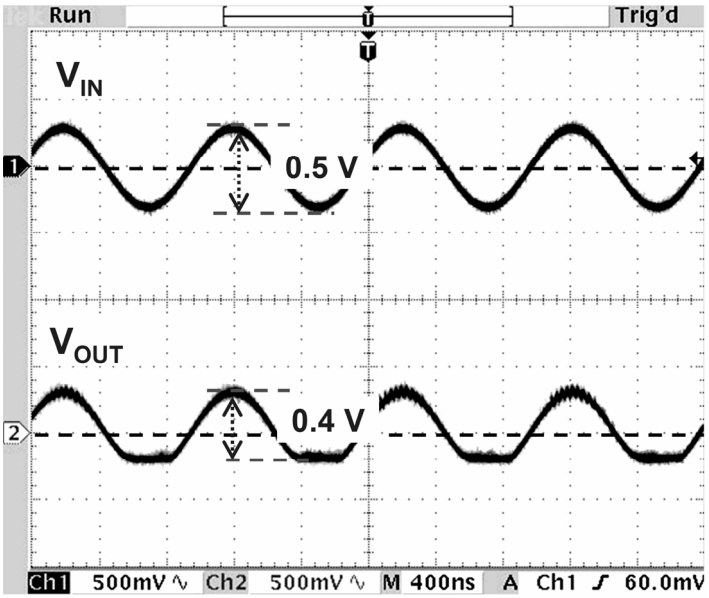


Fig. 3.34. The measured output voltage swing waveform of operational amplifier with the two-stage structure after DC stress.

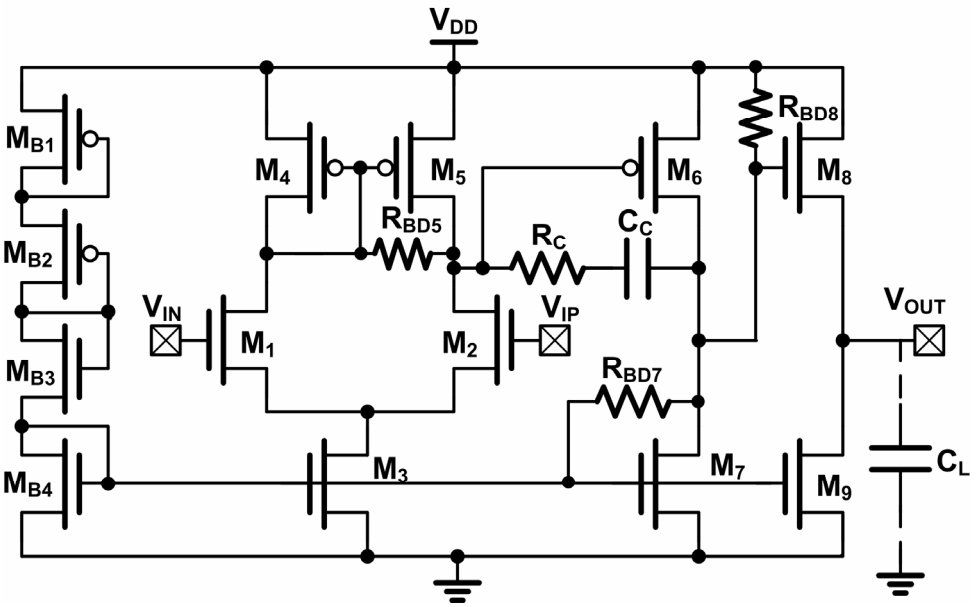


Fig. 3.35. The complete circuit of the operational amplifier with the two-stage structure including gate-oxide breakdown model under DC stress.

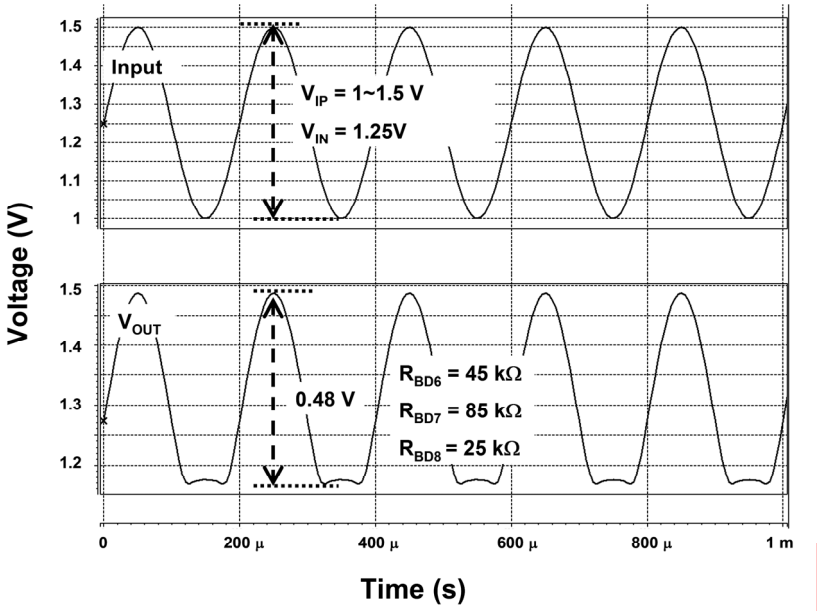


Fig. 3.36. The simulated output voltage swing waveform of operational amplifier with the two-stage structure under different breakdown resistances R_{BD6}, R_{BD7}, and R_{BD8}.

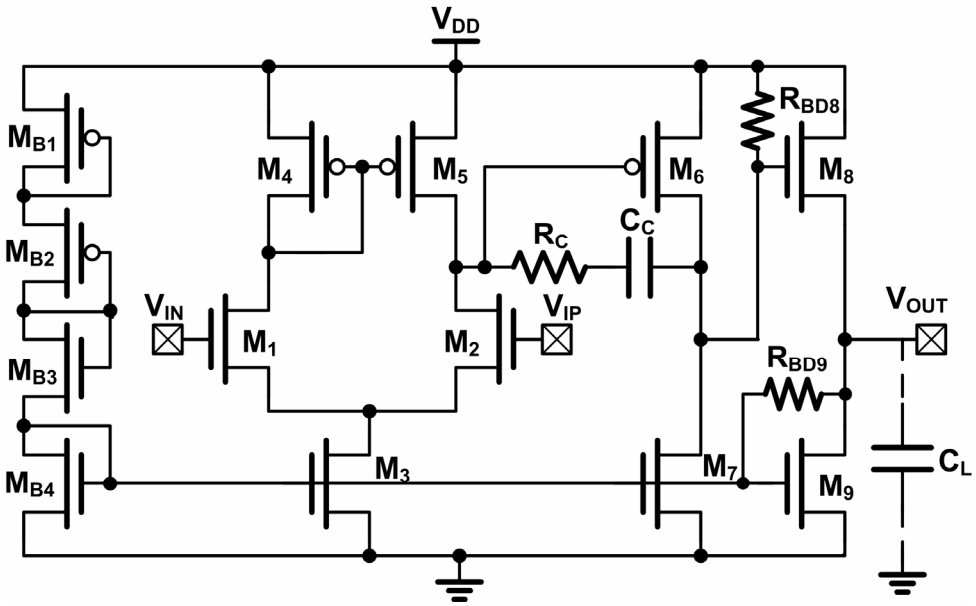


Fig. 3.37. The complete circuit of the operational amplifier with the two-stage structure including gate-oxide breakdown model under large-signal transient stress.

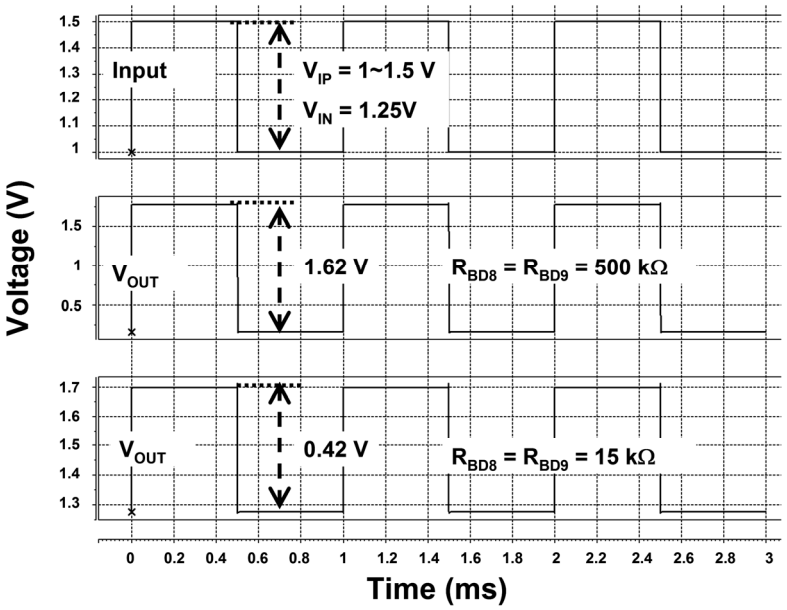


Fig. 3.38. The simulated high and low output voltage levels of operational amplifier with the two-stage structure under different breakdown resistances R_{BD8} and R_{BD9}.

CHAPTER 4

Circuit Performance Degradation of Switched-Capacitor Circuit With Bootstrapped Technique due to Gate-Oxide Overstress

The MOS switch with bootstrapped technique is widely used in low-voltage switched-capacitor circuit. The switched-capacitor circuit with the bootstrapped technique could be a dangerous design approach in the nano-scale CMOS process due to the gate-oxide transient overstress. The impact of gate-oxide transient overstress on the MOS switch in switched-capacitor circuit is investigated in this work with the sample-and-hold amplifier (SHA) in a 130-nm CMOS process. After overstress on the MOS switch of the SHA with unity-gain buffer, the circuit performances in time domain and frequency domain are measured to verify the impact of gate-oxide reliability on circuit performances. The oxide breakdown on the switch device degrades the circuit performance of bootstrapped switch technique.

4.1. Background

The switched-capacitor circuit is an important building block in analog integrated circuits, such as analog-to-digital data converter (ADC). The high-speed and high-resolution analog-to-digital data converter needs a high performance switched-capacitor circuit. The low-supply voltage will degrade the performance of the switched-capacitor circuit due to the nonlinear effects of the MOSFET switch such as body effect, turn-on resistance variation, charge injection, and clock feedthrough [84], [85], [94]-[100].

The bootstrapped switch [84], [85], [94], [95] and switched-opamp (switched operational amplifier) techniques [96]-[100] have been widely used in low-voltage

switched-capacitor circuit. The switched-opamp technique is not suitable for high-speed switched-capacitor circuit, because it needs much more time to turn opamp on/off than to turn switch on/off [97]. The bootstrapped technique provided a constant voltage between the gate and drain nodes of the MOS switch is used to improve the performances of low-voltage and high-speed switched-capacitor circuit. However, the bootstrapped technique causes the gate-oxide overstress on MOS switch to degrade the lifetime of switch device [84]. The gate-oxide reliability of MOS switch in the low-voltage and high-speed switched-capacitor circuit with the bootstrapped technique is a very important reliability issue. The suitable device size design for the bootstrapped switch circuit [84], the thick-oxide MOSFET device [85], and the drain extended MOSFET device [94] can be used to avoid the gate-oxide overstress on the switch devices. Some design techniques of limit gate voltage in bootstrapped switch circuit had been proposed [95]. The impact of gate-oxide reliability on circuit performance of switched-capacitor circuit with bootstrapped technique wasn't investigated in the previous works [84], [85], [94], [95].

In this work, the impact of gate-oxide reliability on MOS switch in the switched-capacitor circuit with the bootstrapped technique is investigated with the sample-and-hold amplifier (SHA) in a 130-nm CMOS process [101]. The time-domain and frequency-domain circuit performances of the SHA with the unity-gain buffer are measured after the gate-oxide overstress on the MOS switch.

4.2. Bootstrapped Technique with Gate-Oxide Reliability

The conceptual schematic of the bootstrapped technique for switched-capacitor circuit is shown in Fig. 4.1(a). The basic schematic includes the signal MOS switch M_S, five ideal switches S_1-S_5, and a capacitor C_b. The CLK_1 and CLK_2 clock signals are the out-of-phase signals. When CLK_1 is low and CLK_2 is high (under sampling mode), the S_3 and S_4 switches charge the capacitor C_b to the supply voltage V_{DD}, and the S_5 switch is used to turn off the switch device M_S. When CLK_1 is high and CLK_2 is low (under hold mode), the S_1 and S_2 switches change the capacitance C_b in series with the input signal V_{IN} and connect to the gate of switch device M_S, such that the gate-to-source voltage across the switch device M_S is equal to the supply voltage V_{DD}.

The gate voltage of switch device M_S will be charged to $V_{IN}+V_{DD}$, which is larger than the supply voltage. The detailed circuit implementation is shown in Fig. 4.1(b) [102]. The M_1, M_2, M_3, M_4 and M_5 correspond to the five ideal switches S_1-S_5 of Fig. 4.1(a). The M_6 transistor is added to reduce the maximum drain-to-source voltage (V_{DS}) of M_5 transistor to avoid the gate-oxide overstress. The capacitor C_b must be large enough to supply charge to the gate of switch device in addition to all parasitic capacitors in the charge path. Moreover, charge sharing will significantly reduce the boosted voltage [84].

The sampling capacitor C_S in the switched-capacitor circuit with the bootstrapped technique is usually designed with several pF to improve the circuit performance. If the rise time of the voltage at gate node of switch device is too fast, a large voltage could exist across the gate oxide of switch device to degrade the lifetime of switch device, before a channel is formed to equalize the potential between the source and drain. In order to explain the gate-oxide transient overstress event in switched-capacitor circuit with bootstrapped technique, the simulated waveforms of the bootstrapped switch circuit are shown in Fig. 4.2. The drain node of switch device is driven by an input signal V_{IN}, and the source node of switch device is connected to a large sampling capacitor. As the switch device turns on, an approximate voltage of V_{IN} + V_{DD} will be generated on the gate node to keep the constant voltage V_{DD} between the gate and drain nodes of switch device. Before a channel is formed and before the sampling capacitor is charged to supply voltage V_{DD}, an excessive voltage greater than V_{DD} may exist across the gate-to-source side of switch device. This effect could create an oxide reliability problem. In Fig. 4.2, the simulated result is a worse case of switched capacitor circuit with bootstrapped technique under the gate-oxide transient overstress.

4.3. Dependences of Design Parameters on Transient Gate-Oxide Reliability

4.3.1. Difference Time Delay between Sampling and Bootstrapped Networks

The input signal frequency, sampling frequency, and delay times of bootstrapped and sampling networks are the major design factors in the switched-capacitor circuit with the bootstrapped technique. Fig. 4.3 shows the dependence of the different sampling capacitors on output voltage waveform in the switched-capacitor circuit with the bootstrapped technique. The V_G is the gate voltage of switch device M_S. The input signal V_{IN} is set to 2-MHz sinusoidal signal with peak-to-peak amplitude of 1.2 V, and sampling frequency is set to 10 MHz. The different sampling capacitors in the switched-capacitor circuit with bootstrapped technique can be used to simulate the different delay times of sampling network. The difference RC delay time between the sampling network (M_S and C_S) and the bootstrapped network (M_1-M_8 and C_b) will induce the gate-oxide transient overstress across the gate-to-source side of the switch M_S to cause the long-term reliability issue in the switched-capacitor circuit with the bootstrapped technique.

4.3.2. Input/Sampling Frequency Ratio

The dependences of the input/sampling frequency (f_I/f_S) ratio on maximum transient voltage in the switched-capacitor circuit with the bootstrapped technique are shown in Fig. 4.4. The maximum transient voltage is defined as the maximum voltage difference between the source node and the gate node of switch M_S during the sampling mode. The sampling capacitance of switched-capacitor circuit with bootstrapped technique is set to 8 pF. The high input/sampling frequency ratio has a larger transient voltage than the low input/sampling frequency ratio in the switched-capacitor circuit with the bootstrapped technique.

The overstress time is related to the RC time constant ratio of the sampling and bootstrapping networks in bootstrapped switch technique. Based on the Figs. 4.3 and 4.4, the RC delay time of bootstrapped network should be designed slower than that of sampling network in the switched-capacitor circuit with the bootstrapped technique to avoid the transient gate-oxide reliability. The best solution is that the bootstrapped and sampling networks have same RC delay times to avoid the transient gate-oxide overstress and to achieve the best performance.

4.4. Switched-Capacitor Circuit With Gate-Oxide Reliability Test Circuit

The switched-capacitor circuit with the bootstrapped technique has a long-term reliability problem, which causes the circuit performance degradation. The overstress voltage on the gate oxide of the switch device depends on the voltages of input and clock signals. The obvious degradation on circuit performance in the switched-capacitor circuit with the bootstrapped technique needs a long-term operation, which may need many years, to observe the change due to the gate-oxide degradation of switch device. The gate-oxide degradation of switch M_S in switched-capacitor circuit with bootstrapped technique is more likely to occur as the conventional time-dependent dielectric breakdown (TDDB). The TDDB accelerated lifetime-model equation for the nMOSFET can be expressed as [103]

$$t_f = A_{TDDB}\left(\frac{1}{A}\right)^{\frac{1}{\beta}} F^{\frac{1}{\beta}} V_{gs}^{a+bT} \exp\left(\frac{c}{T}+\frac{d}{T^2}\right), \tag{4.1}$$

where $A = W \times L$ is the device gate-oxide area, β is Weibull slope parameter, F is the cumulative failure percentage at use condition, V_{gs} is the gate-to-source voltage, T is the temperature, and a, b, c, and d are the model-fitting parameters determined from the experimental work, A_{TDDB} is the model factor. Note that $a + bT$ is always negative. The model of TDDB breakdown related with frequency is still a challenge. The equation (4.1) is not suitable to calculate the lifetime of the switch device in the switched-capacitor circuit with bootstrapped technique. Therefore, to investigate the impact of gate-oxide reliability on circuit performance of the switched-capacitor circuit with bootstrapped technique is very important in advanced CMOS technology.

In order to accelerate the degradation of circuit performance and to understand the impact of gate-oxide transient overstress event on switched-capacitor circuit with bootstrapped technique, the SHA with the gate-oxide reliability test circuit is proposed in Fig. 4.5. The SHA with unity-gain buffer is used to verify the gate-oxide reliability of the bootstrapped switch. The two-stage operational amplifier is used to realize the output buffer. The folded-cascode operational amplifier and common-source amplifier are used to form the two-stage operational amplifier to achieve high output swing and

high small-signal gain. Simulated by HSPICE, the two-stage operational amplifier has the open-loop gain of 75 dB, the unity-gain frequency of 160 MHz, and the phase margin of 87.3 degree, respectively, under output capacitive load of 2.5 pF. The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in the SHA with the gate-oxide reliability test circuit are 1.2 V and 2.63 nm, respectively, in a 130-nm CMOS process.

The control device M_C is used to control the drain voltage of the switch device M_S. Therefore, the device dimension of the control device M_C should be designed larger than that of the switch device. The device dimensions of switch device (M_S) and control device (M_C) are selected as 40μm/0.12μm and 500μm/0.12μm, respectively, in a 130-nm CMOS process. If the device dimension of the control device is smaller than that of the switch device, the drain voltage of switch device M_S will not be kept at near ground. In normal operation, the control voltage V_C is biased to ground, such that the control device M_C will be turned off. The SHA with the open-loop configuration can be successfully operated. In the gate-oxide overstress test, the control voltage V_C is biased to supply voltage V_{DD}, and input signal V_{IN} is biased to the supply voltage V_{DD}. The voltage at V_{CLK} node can be applied with any higher voltage level than the supply voltage to overstress the gate oxide of switch device. The voltage across the gate-to-drain nodes of switch device M_S can be controlled by the V_{CLK} voltage.

However, the switch device suffers the dynamic (AC) stress in the real operation. The dynamic stress is less harmful than DC stress on switch device, but the dynamic stress on switch device still causes damage on gate oxide of switch device after long-term operation. The DC stress on switch device can be used to accurate the damage occurrence on switch device to investigate the impact of gate-oxide reliability on MOS switch with bootstrapped technique. The difference between the AC stress in real case and DC stress in this test has the different degraded times of circuit performance, but they will have the same degradation trend on circuit performance after long-term operation [104]. Therefore, the proposed test circuit can be used to verify the impact of gate-oxide breakdown on circuit performance of bootstrapped switch technique.

The test chip has been fabricated in a 130-nm CMOS process, and the normal operating voltage of all MOSFET devices is 1.2 V. The chip micrograph and layout view of the SHA with the gate-oxide reliability test circuit are shown in Figs. 4.6(a) and 4.6(b), respectively. The occupied silicon area including two testing circuits and ESD (electrostatic discharge) protection devices is 390 μm × 390 μm. The top layer of test chip is covered and protected by polyimide layer. Fig. 4.7 shows the simulated frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms of the sample-and-hold amplifier with the gate-oxide reliability test circuit under normal operation. The signal at V_{CLK} node is applied with clock signal between 0 V to 1.2 V. Simulated by HSPICE, the spurious free dynamic range (SFDR) of the SHA with the gate-oxide reliability test circuit is 38.6 dB under the 10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node.

4.5. Experimental Results

When the SHA with the gate-oxide reliability test circuit is operating in the overstress mode, the input signal V_{IN} is biased to supply voltage, and the control voltage V_C is set to supply voltage. In order to observe the circuit performance degradation of the SHA due to the gate-oxide degradation of switch device, the voltage at V_{CLK} node is kept to 2.4 V for accelerating the gate-oxide degradation of switch device. Only the gate-to-drain nodes of the switch M_S is overstressed to simulate the switched-capacitor circuit with the bootstrapped technique. The measured results of test circuit are measured with die under test on the printed circuit board (PCB). The time-domain and frequency-domain waveforms are re-evaluated after the gate-oxide overstress on MOS switch. When the time-domain and frequency-domain waveforms are re-evaluated after the gate-oxide overstress on the MOS switch, the signal at V_{CLK} node is applied with clock signal between 0 V to 1.2 V. After overstress time of 5.2 hours, the gate-oxide breakdown has been occurred on switch device. The gate-leakage current ($I_{G\_leakage}$) of switch device is jumped from 330 nA to 80.6 μA under V_{CLK} of 2.4 V due to the gate-oxide breakdown.

Figs. 4.8(a) and 4.8(b) show the frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms at V_{OUT} node under different stress times. A frequency axis is shown till 5MHz because of aliasing by Nyquist criterion. The SFDR of the test circuit is degraded by the gate-oxide breakdown on switch device from 35.62 dB to 30.86 dB, because the gate-oxide breakdown causes extra gate-leakage current across gate oxide of switch device to degrade the circuit performances of SHA with the gate-oxide reliability test circuit. However, the amount of gate-leakage current depends on the gate-oxide breakdown location on switch device. The gate-oxide breakdown location near channel region of switch device (soft breakdown) has a smaller gate-leakage current than that near the drain or source side of switch device (hard breakdown) [82].

4.6. Discussion

In order to investigate the impact of gate-oxide breakdown location (switch device) on performances of switched-capacitor circuit with bootstrapped technique, the prior proposed method [81] can be used to simulate this impact with HSPICE. The gate-oxide breakdown of MOSFET device can be modeled as resistance. Only the gate-to-diffusion (source or drain) breakdown was considered, since it represents the worst-case situation [82], [103]. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard breakdown leakage has a close-to-linear I-V curve and an equivalent resistance of ~ 10^3-10^4 Ω. However, typical soft breakdown paths have high non-linear, power law I-V curve and equivalent resistance above 10^5-10^6 Ω [82]. The equivalent breakdown resistance ($V_{CLK}/I_{G\_leakage}$) of switch device after overstress is approximate 30 kΩ (hard gate-oxide breakdown) under V_{CLK} of 2.4 V.

The SHA including equivalent breakdown resistors R_{GD} and R_{GS} is shown in Fig. 4.9(a). The simulated frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms of the SHA with equivalent breakdown resistor (R_{GS} and R_{GD}) of 30 kΩ are shown in Figs.

4.9(b) and 4.9(c), respectively. Comparing the simulated (Fig. 4.9(c)) with measured (Fig. 4.8(b)) results, the gate-oxide breakdown on switch device in SHA with the gate-oxide reliability test circuit is near the source side of switch device. The difference between Fig. 4.8(b) and Fig. 4.9(c) is due to the gate-to-channel and gate-to-drain breakdowns on switch device caused the extra gate leakage current in SHA. Only the gate-to-source oxide breakdown on switch device will degrade the performances of SHA. In the sampling mode of SHA, the gate leakage current of switch device is smaller than the charge current (I_D) of witch device current. In hold mode of SHA, the extra gate leakage current of will discharge the stored charge in sampling capacitor to degrade the circuit performance of SHA. The relationship between extra gate leakage current and stored charge of sampling capacitor under SHA operated in holding mode can be simple expressed as

$$\Delta V = \frac{\Delta Q_{holding}}{C_S} = \frac{C_S V_{holding} - I_{G\_leakage} T_{holding}}{C_S}, \tag{4.2}$$

where $T_{holding}$ is the holding time ($2/f_S$, f_S sampling frequency), C_S is the sampling capacitor, $Q_{holding}$ is a stored charge in sampling capacitor, $V_{holding}$ is the ideal potential stored in sampling capacitor without oxide breakdown on switch device under hold mode, and $I_{G\_leakage}$ is the extra gate leakage current of switch device due to gate-oxide breakdown. When the SHA operated in high sampling frequency, the gate-oxide breakdown on switch device has small impact on circuit performance. Therefore, the proposed SHA with the gate-oxide reliability test circuit can be used to verify the impact of gate-oxide breakdown on switched-capacitor circuit with bootstrapped switch technique.

In order to investigate the impact of soft gate-oxide breakdown on circuit performances of the switched-capacitor circuit with bootstrapped technique, the test circuit with equivalent breakdown resistor R_{GS} of 500 kΩ can be used to model the soft gate-oxide breakdowns on the switch device [82]. The simulated frequency-domain (10-MHz sampling frequency at V_{CLK} node and 2-MHz sinusoidal signal at V_{IN} node) and time-domain (10-MHz sampling frequency at V_{CLK} node and 1-MHz sinusoidal signal at V_{IN} node) waveforms of the SHA with equivalent breakdown resistor R_{GS} of 500 kΩ is shown in Fig. 10. The soft gate-oxide breakdown

on the switch device also degrades the circuit performance of SHA. The soft and hard gate-oxide breakdowns on a CMOS transistor will cause different extra gate leakage currents. The soft gat-oxide breakdown on a transistor causes a smaller extra gate leakage current than that of the hard gate-oxide breakdown in CMOS process [82]. Therefore, the soft and hard gate-oxide breakdowns will have different impact on circuit performances of the SHA. The hard gate-oxide breakdown has more serious impact on circuit performances than soft gate-oxide breakdown on switch device of switched-capacitor circuit with bootstrapped switch technique.

4.7. Summary

The impact of gate-oxide transient overstress on MOS switch with bootstrapped technique has been investigated and analyzed with the sample-and-hold amplifier. The time-domain and frequency-domain waveforms of the SHA after different stress times have been measured. After the gate-oxide overstress, only the gate-to-source oxide breakdown on switch device will degrade the performances of SHA. The overstress time is related to the RC time constant ratio of the sampling and bootstrapping networks in bootstrapped switch technique. The best solution of bootstrapped switch design is that the bootstrapped and sampling networks have same RC delay times to avoid the transient gate-oxide overstress and to achieve the best performance. The hard gate-oxide breakdown has more serious impact on switched-capacitor circuit with bootstrapped technique.

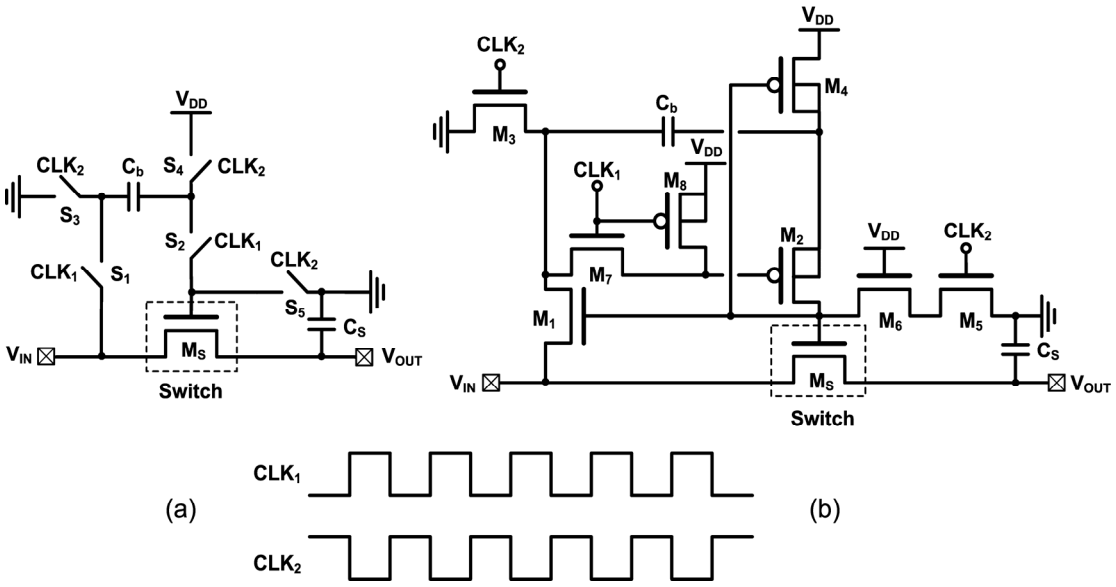


Fig. 4.1. (a) Conceptual schematic and (b) detail circuit implementation of bootstrapped technique for switched-capacitor circuit.

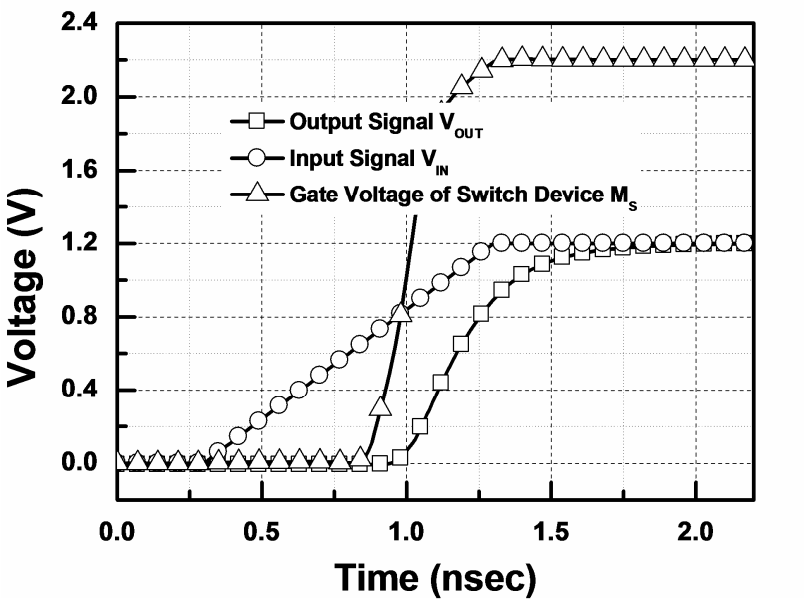


Fig. 4.2. Simulated waveforms of gate-oxide transient overstress event in switched-capacitor circuit with bootstrapped technique.

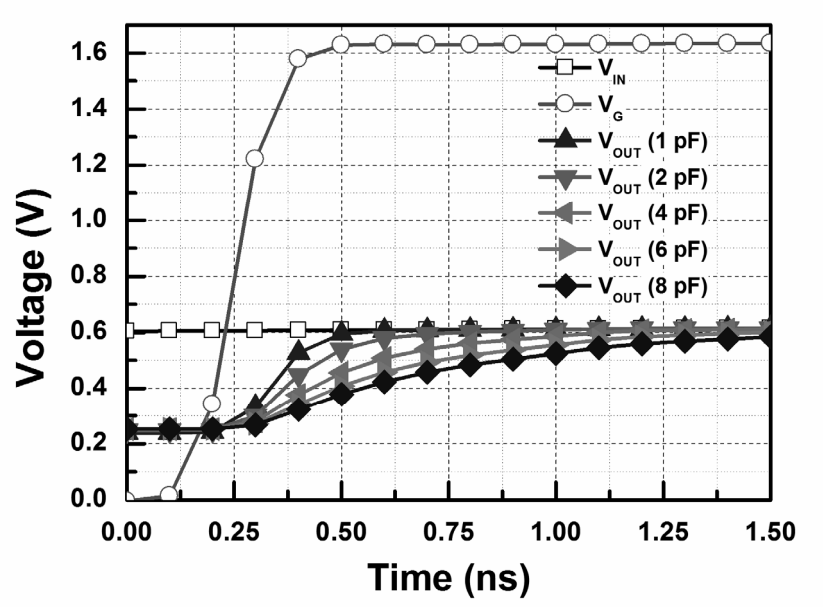


Fig. 4.3. The dependence of the different sampling capacitors on output voltage waveform in the switched-capacitor circuit with the bootstrapped technique.

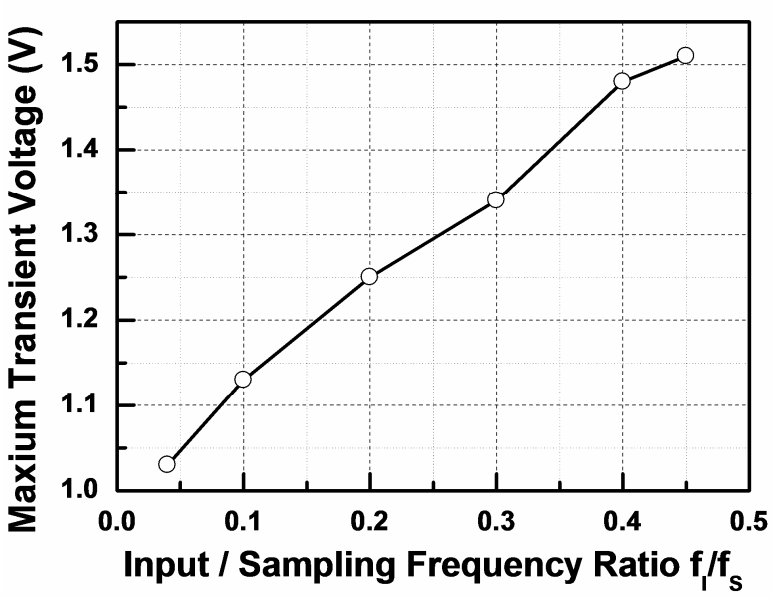


Fig. 4.4. The dependence of the input/sampling frequency ratio on maximum transient voltage in the switched-capacitor circuit with the bootstrapped technique.

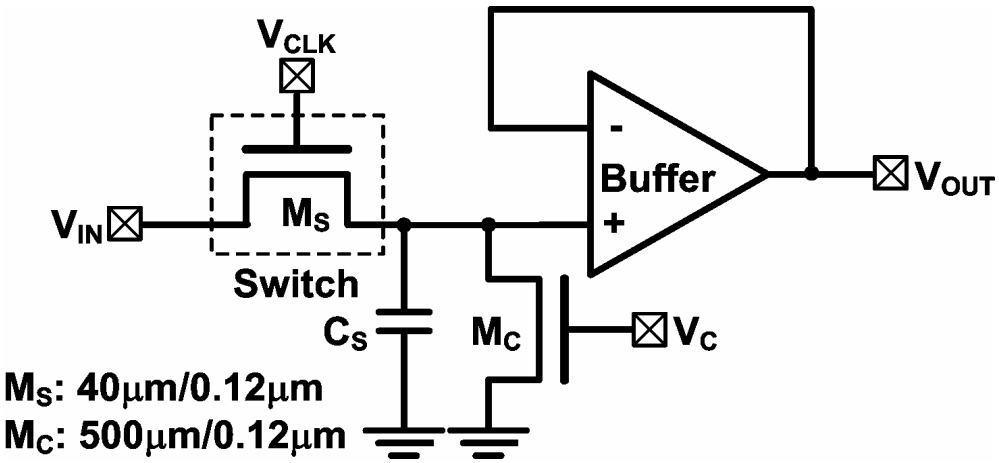
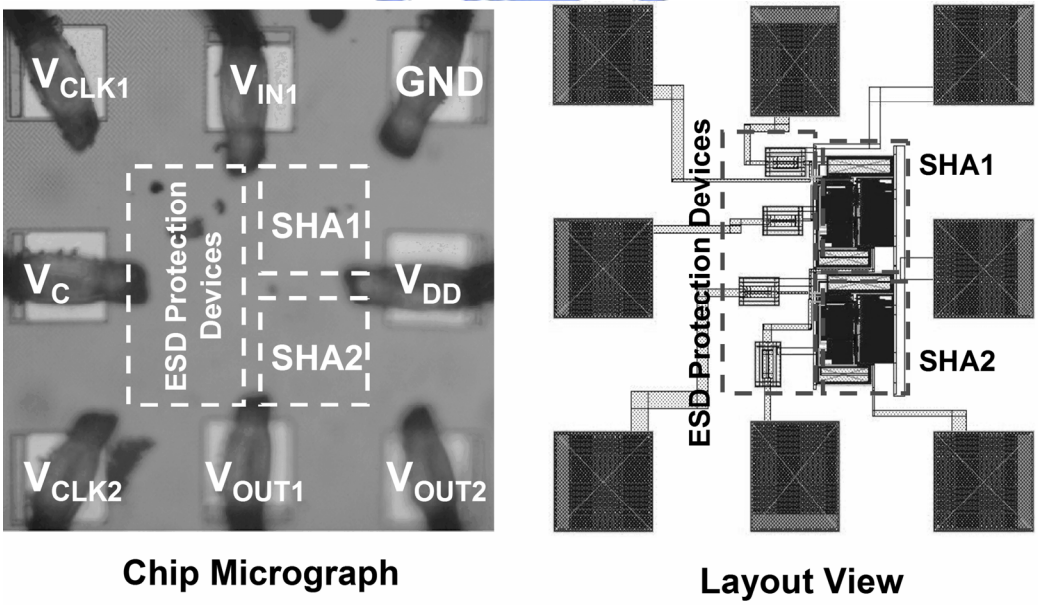


Fig. 4.5. The complete circuit of sample-and-hold amplifier with the gate-oxide reliability test circuit, where the control device M_C is used to control the drain voltage of the switch device M_S for reliability test.



(a) (b)

Fig. 4.6. (a) Chip micrograph and (b) layout view of the sample-and-hold amplifier with the gate-oxide reliability test circuit realized in a 130-nm CMOS process.

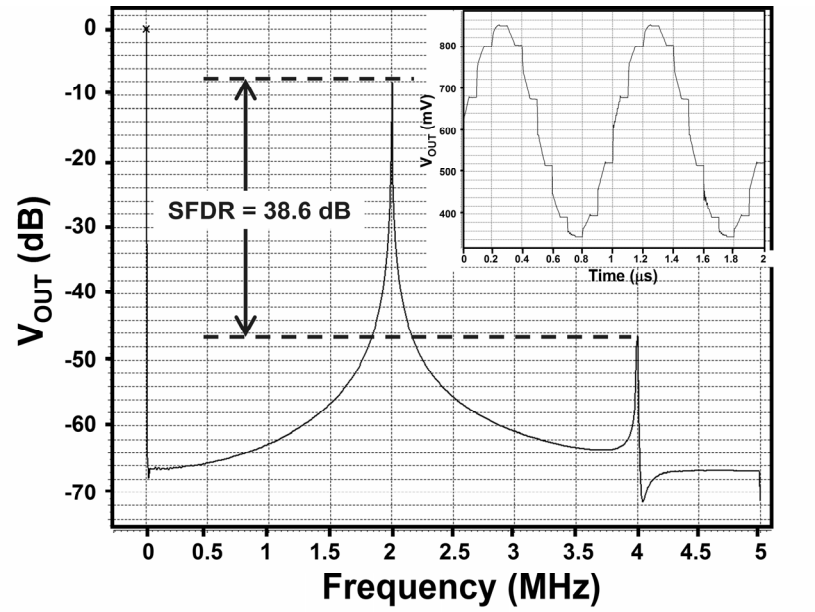
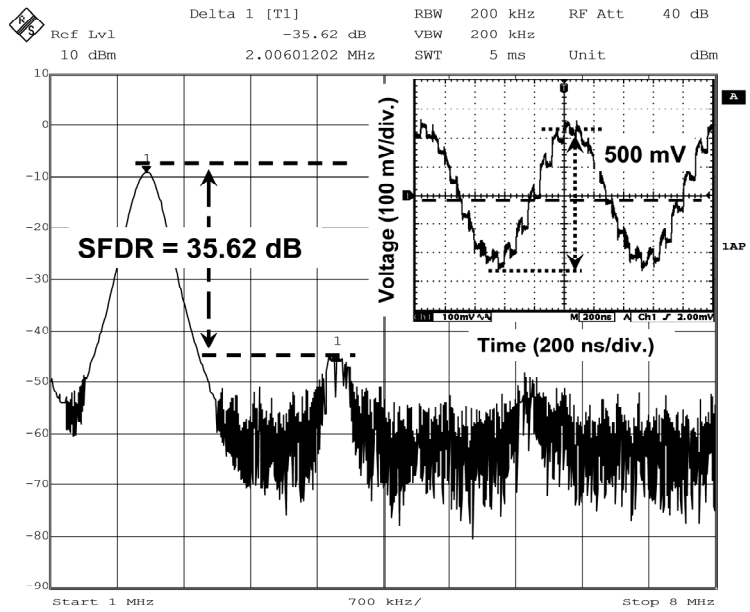
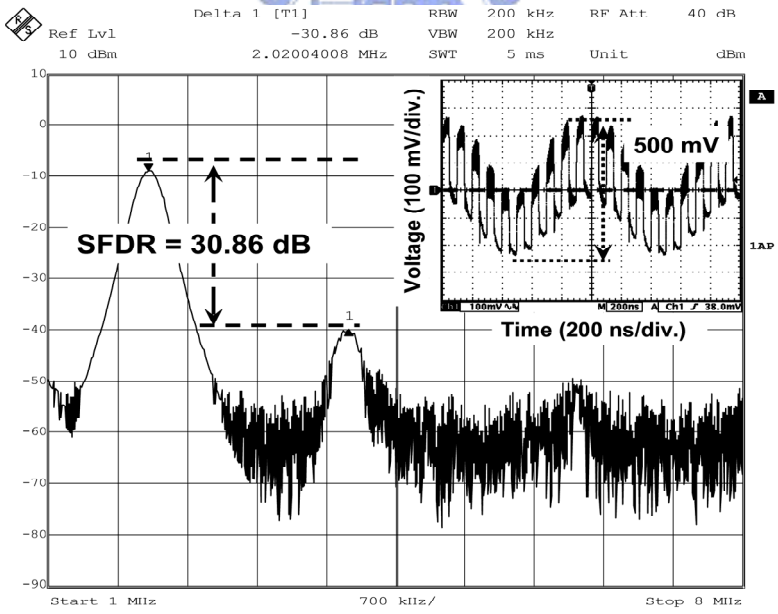


Fig. 4.7. The simulated frequency-domain and time-domain waveforms of the sample-and-hold amplifier with the gate-oxide reliability test circuit under normal operation.

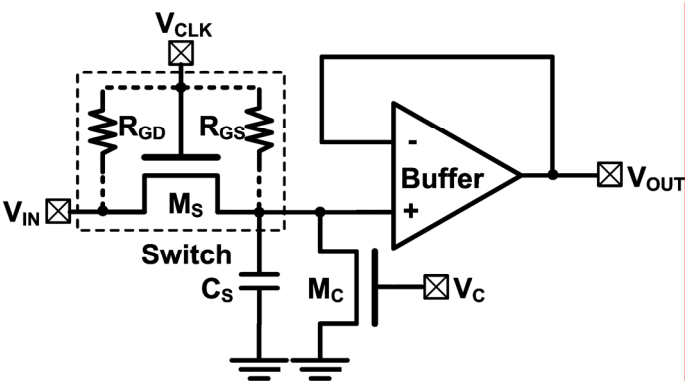


(a)

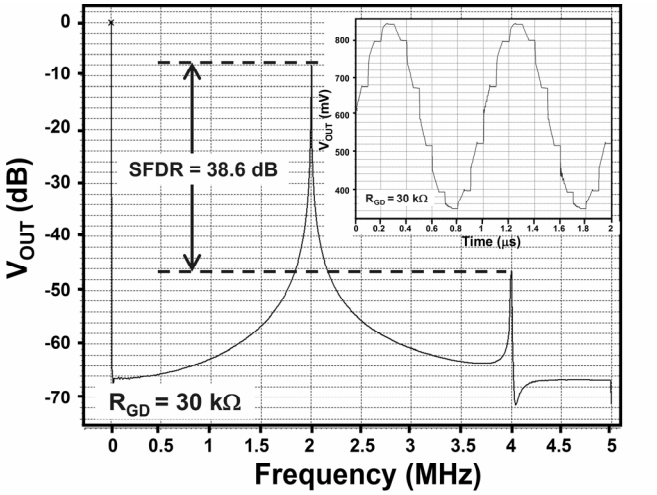


(b)

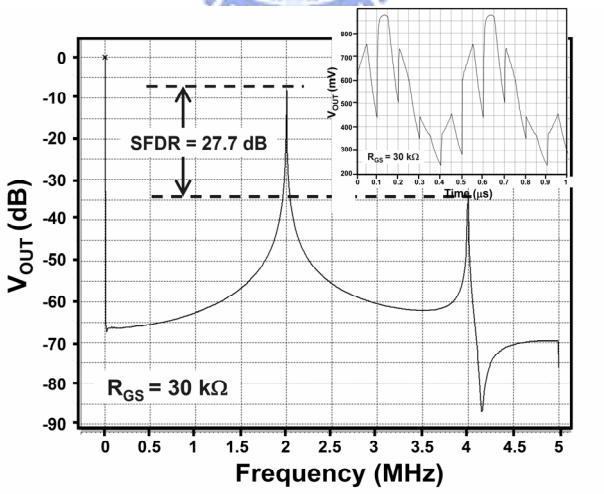
Fig. 4.8. The measured frequency-domain and time-domain waveforms of the sample-and-hold amplifier with the gate-oxide reliability test circuit. (a) Overstress time = 0 hour, and (b) overstress time = 5.2 hours.



(a)



(b)



(c)

Fig. 4.9. (a) The sample-and-hold amplifier with the gate-oxide reliability test circuit including equivalent breakdown resistors R_{GD} and R_{GS}. The simulated frequency-domain and time-domain waveforms of the test circuit with equivalent breakdown resistance (b) R_{GD} and (c) R_{GS} of 30 kΩ , respectively.

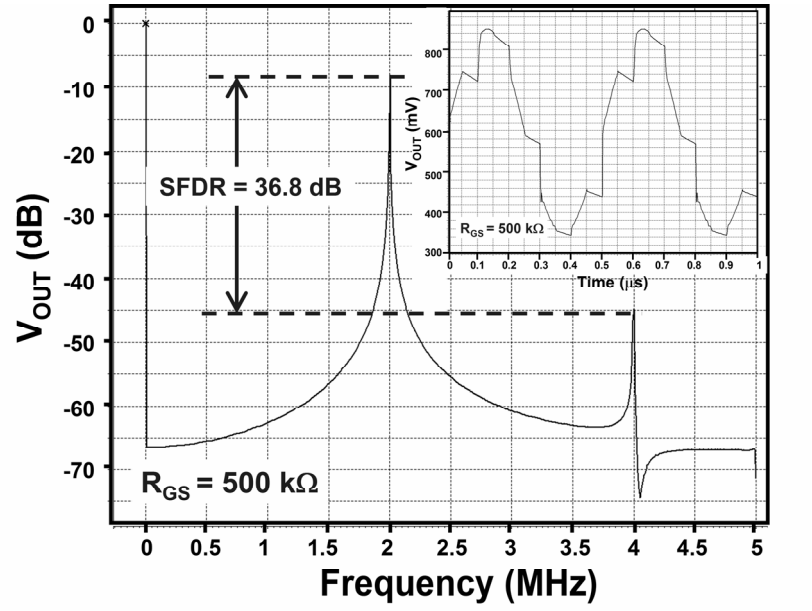


Fig. 4.10. The sample-and-hold amplifier with the gate-oxide reliability test circuit including equivalent breakdown resistors R_{GS}. The simulated frequency-domain and time-domain waveforms of the test circuit with equivalent breakdown resistors R_{GS} of 500 kΩ.

CHAPTER 5

Impact of Gate Tunneling Leakage on Performances of Phase Locked Loop Circuit in Nanoscale CMOS Technology

In nanoscale CMOS technology, the thin gate oxide causes the large gate tunneling leakage. In this work, the influence of gate tunneling leakage in MOS capacitor, as loop filter, on the circuit performances of phase locked loop (PLL) in nanoscale CMOS technology has been investigated and analyzed. The basic PLL with second-order loop filter is used to observe the impact of gate tunneling leakage on performance degradation of PLL in a 90-nm CMOS process. The MOS capacitors with different oxide thicknesses are used to observe this impact to PLL. The locked time, static phase error, and jitter of second-order PLL are degraded by the gate tunneling leakage of MOS capacitor in loop filter. Overview on the prior designs of compensation techniques to reduce the gate tunneling leakage on MOS capacitor in loop filter of PLL is also provided in this work.

5.1. Background

The reduction of power consumption has become increasingly important to portable products, such as mobile phone, notebook, and flash memory. In general, the most common and efficient way to reduce the power consumption in CMOS very large scale integrated circuits (VLSI) is to reduce the power-supply voltage. To reduce the power consumption in CMOS VLSI systems, the standard supply voltage has been scaled down from 2.5 V to 1 V. The gate-oxide thickness of the MOS transistor becomes thinner to reduce normal operation voltage (power-supply voltage). This result causes large gate tunneling leakage (gate leakage current), which relates to

gate-oxide thickness. For the digital circuits, the gate tunneling leakage results in the high stand-by power consumption. For analog circuits, it degrades the circuit accuracy [105]. Therefore, to suppress gate tunneling leakage effect is a very important design issue in analog circuit design in naoscale CMOS process [26], [106].

In PLL, the capacitor of loop filter needs a large capacitance to make PLL stable. The MOS capacitor has a larger capacitance than other structure under the same chip area to reduce the fabrication cost, but it has a large gate tunneling leakage on MOS capacitor of loop filter to degrade the PLL performances in advanced CMOS technology. Recently, some researches of circuit design technique to compensate the gate tunneling leakage of MOS capacitor in PLL have been reported in nanoscale CMOS process [107]-[112]. The MOS capacitor with thick-oxide device has a less gate tunneling leakage [107]. The capacitor with multi-metal structure was used to replace MOS capacitor to avoid the gate tunneling leakage [108]. The thin oxide MOS capacitor with opamp compensated technique is developed to reduce the gate tunneling leakage effect [109]-[111]. The loop filter with gate tunneling leakage compensator was also developed [112]. However, the impact of gate tunneling leakage on PLL performance was not detailed investigation and analysis in advanced CMOS technology.

In this work, the influence of gate tunneling leakage on performances of the phase locked loop (PLL) in nanoscale CMOS technology is investigated and analyzed in a 90-nm 1-V CMOS process [113]. The normal operating voltage of MOSFET device is only 1 V in such a 90-nm CMOS process. The gate tunneling leakage of MOS capacitance is simulated by SPICE with BSIM4 model. The BSIM4 model has been included with the gate tunneling leakage effect [27], [114], [115]. The MOS capacitors with different oxide thicknesses are used to investigate this impact to PLL. Overview on the prior designs of compensation techniques to reduce the gate tunneling leakage on MOS capacitor in loop filter of PLL is also provided in this work.

5.2. Phase Locked Loop

PLL is a necessary building block in many very large scale integrated circuits (VLSI). The demand for low-jitter PLLs has become especially strong in advance nanoscale CMOS process. A PLL is basically an oscillator whose frequency is locked onto some frequency component of an input signal. Fig. 5.1 shows the basic PLL with second-order low-pass loop filter structure [116]. A PLL consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled oscillator (VCO), and a frequency divider (divided by N). The negative feedback system synchronizes the internal signal (F_{BACK}) which is from the frequency divider to the external reference signal (F_{REF}) by comparing their phases. The PFD develops two output control signals, which are proportional to the phase errors. The purpose of the charge pump is to convert the logic states of PFD into analog signals suitable for controlling VCO which varies the frequency of the output signal by charging or discharging the loop filter. In the loop filter, extra poles and zeros should be introduced to filter out high frequency signals from the PFD and the charge pump. The PLL is "locked" when the phase difference between F_{REF} and F_{BACK} is constant. Therefore, the phase of F_{REF} and F_{BACK} are aligned and the frequency of the output signals is N-times of the input reference signal (F_{REF}). The loop filter developed with second-order low-pass filter is widely used in PLL design to improve the stability and to suppress the high-frequency noise. The on-chip capacitor is usually designed with MOS capacitor to reduce the fabrication cost in second-order PLL. The second-order loop filter structure can be realized with PMOS and NMOS devices, respectively, as shown in Fig. 5.2.

5.3. MOS Capacitor With Gate Tunneling Leakage Model

In PLL, the capacitor of loop filter needs a large capacitance to make PLL stable. The MOS capacitor has a larger capacitance than other structure under the same chip area to reduce the fabrication cost, but it has a large gate tunneling leakage on MOS capacitor of loop filter to degrade the PLL performances in advanced CMOS technology. The MOSFET device with gate tunneling leakage model is proposed by Hu [27], [114]. The gate tunneling leakage of MOSFET device is composed of several components, as shown in Fig. 5.3(a): 1. gate-to-substrate (bulk) tunneling leakage I_{gb}, 2. tunneling leakage between gate and source-drain extension (SDE) overlap I_{gso} and

I_{gdo}, and 3. gate-to-channel tunneling leakage I_{gc}, which in turn is partition between the source and drain nodes (I_{gcs} and I_{gcd}). The significance of each component varies with the operation mode of the MOSFET device. They are determined by carrier conduction processes: electron conduction-band tunneling (ECB), electron valence-band tunneling (EVB), and hole valance-band tunneling (HVB), as shown Fig. 5.3(b). Each mechanism is dominant or important in different regions of operation for NMOS and PMOS devices, as shown in Table 5.1. For each mechanism, the gate tunneling leakage density can be modeled as [27], [114],

$$J_g = A\left[\frac{T_{oxref}}{t_{ox}}\right]^{ntox} \frac{V_g V_{aux}}{T_{ox}^2} e^{-B(\alpha-\beta|V_{ox}|)(1+\gamma|V_{ox}|)t_{ox}}, \tag{5.1}$$

where $A = q^2/8\pi h\phi_B$, $B = 8\pi\sqrt{2qm_{ox}}\phi_B^{3/2}/3h$, m_{ox} is the effective carrier mass in oxide, ϕ_B is the tunneling barrier height, t_{ox} is the oxide thickness, T_{oxref} is the reference oxide thickness at which all the parameter that defaults to 1, and V_{aux} is an auxiliary function which approximates the density of tunneling carriers. α, β, and γ are the physical parameters defined by device technology. The V_g is the gate voltage of MOSFET device, ntox is a fitting parameter that defaults to 1, and V_{ox} is the voltage across the oxide of MOSFET device.

The MOS capacitor is usually operated in strong inversion region for CMOS circuit design. In equation (5.1), the gate tunneling leakage density strongly depends on the oxide thickness, device dimension, and voltage across the oxide of MOSFET. Fig. 5.4 shows the dependence of gate tunneling leakage on the gate voltage of different threshold-voltage NMOS and PMOS capacitors in a 90-nm CMOS technology. The capacitance of different MOS capacitors is designed with 85.172 pf under the gate voltage of 0.492 V. The normal operating voltage of MOSFET device is only 1 V, and the typical oxide thickness of MOSFET device is only 2.33 nm in a 90-nm CMOS process. The NMOS capacitor has larger gate tunneling leakage than PMOS capacitor. The reason is that electron tunneling ECB is the dominant component of gate tunneling leakage in NMOS device, whereas it is the HVB in PMOS device. As the barrier height for HVB (4.5 eV) is significantly larger than that for ECB (3.1 eV), the results in the much lower gate tunneling leakage for PMOS device [115]. The

summary of gate tunneling leakage per unit area under different threshold-voltage NMOS and PMOS capacitors in a 90-nm CMOS process is shown Table 5.2. The thin-oxide NMOS device with the low threshold voltage has larger gate tunneling leakage than other devices in a 90-nm CMOS process.

5.4. Effect of Gate Tunneling Leakage in MOS Capacitor on Performances of PLL Circuit

In this work, the PLL with second-order low-pass loop filter is used to investigate the impact of gate tunneling leakage of MOS capacitor on PLL performances. The design parameters and simulated results of second-order PLL in a 90-nm CMOS process are shown in Table 5.3. The results of second-order PLL are simulated by HSPICE with a 90-nm CMOS SPICE model. In order to compare the impact of gate tunneling leakage of MOS capacitor on PLL performances, the loop filter (C_1, C_2, and R_1) in second-order PLL is developed and simulated with ideal capacitor and resistor in Table 5.3. In this work, the different types and oxide thicknesses of MOS devices are used to realize the MOS capacitor and to investigate the impact of gate tunneling leakage on PLL performances. The C_1 and C_2 capacitors of low-pass loop filter in PLL, as shown in Fig. 5.4, are replaced by different oxide thickness MOS capacitors to investigate the impact of gate tunneling leakage on PLL performances. The capacitances of different MOS capacitors C_1 and C_2 are 85.172 pf and 8.782 pf under gate voltage of 0.492 V, respectively, for second-order PLL design. Fig. 5.5 shows the simulated control voltage (V_{CTRL}) transition waveform to find the locked time under different oxide thickness MOS capacitors in second-order PLL. The thin-oxide MOS capacitors (1-V NMOS and PMOS) have longer locked time and cause larger ripple voltage V_r than thick-oxide MOS capacitor (1.8-V NMOS), when the phase difference between F_{REF} and F_{BACK} is constant. The simulated dependence of static phase error Δt on the time under different oxide thickness MOS capacitors in second-order PLL is shown in Fig. 5.6. The thin-oxide MOS capacitors (1-V NMOS and PMOS) cause larger static phase error Δt than thick-oxide MOS capacitor (1.8-V NMOS) in second-order PLL. The simulated jitter under different oxide thickness MOS capacitors in second-order PLL is shown in Fig. 5.7. The thin-oxide MOS

capacitors (1-V NMOS and PMOS) cause larger jitter than thick-oxide MOS capacitor (1.8-V NMOS) in second-order PLL, due to the large ripple voltage at V_{CTRL} node. The dependence of jitter and ripple voltage on different input signal frequencies under different oxide thickness devices is shown in Fig. 5.8. The high input signal frequency F_{REF} has a small jitter, and low input signal frequency has a large jitter in second-order PLL with gate tunneling leakage.

5.5. Discussion

In general, the capacitance of MOS capacitor C_1 is larger than that of MOS capacitor C_2 in second-order PLL design, as shown in Fig. 3. Because the capacitance of MOS capacitor is proportion to device dimension and oxide thickness, the gate tunneling leakage of the MOS capacitor C_2 is larger than the capacitor C_1. The schematic of Fig. 3 can be simplified to that of Fig. 5.9, where the current I_{CP} is the charge pump current, and the current $I_{GTL,\ LF}$ is the total gate tunneling leakage of MOS capacitors C_1 and C_2. The charge pump current I_{CP}, which is controlled by the phase difference between F_{REF} and F_{BACK} signals through PFD, is a constant current source. The effective charge current I_C of MOS capacitors C_1 and C_2 can be expressed as

$$I_C = I_{CP} - I_{GTL,LF}\,. \tag{5.2}$$

In order to reach locked state (phase difference between F_{REF} and F_{BACK} is constant), the second-order PLL needs a setting time for system stability. Therefore, the locked time of second-order PLL is increased due to gate tunneling leakage of MOS capacitor.

In locked state, the dependence of gate tunneling leakage on ripple voltage V_r in second-order PLL can be written by

$$\Delta V_r = \frac{I_{GTL,LF} \times T_{REF}}{C_1}, \tag{5.3}$$

where T_{REF} is the period of input signal F_{REF}. The amount of ripple voltage V_r is proportion to gate tunneling leakage. The large gate tunneling current of MOS

capacitor will cause large ripple voltage at V_{CTRL} node in second-order PLL. In equation (5.3), the ripple voltage V_r is proportion to the period of input signal F_{REF}, so the low input signal frequency causes a large ripple voltage, and the high input signal frequency causes a small ripple voltage in second-order PLL, as shown in Fig. 8. The dependence of gate tunneling leakage on jitter of second-order PLL can be expressed as

$$Jitter = \frac{1}{\Delta V_r \times K_{VCO}}, \tag{5.4}$$

where the K_{VCO} (Hz/V) is the gain of voltage-controlled oscillator VCO. The large ripple voltage ΔV_r cause the large jitter in second-order PLL. The dependence of gate tunneling leakage on static phase error Δt of second-order PLL can be expressed as

$$\Delta t = \frac{I_{GTL,TL}}{I_{CP}} \times T_{REF}. \tag{5.5}$$

In order to reduce the static phase error in second-order PLL, the charge pump current should be designed with large constant current.

As a result, how to design a low-jitter and low-cost second-order PLL in nanoscale CMOS technology is a very important design issue. Comparing the Table 5.2, Figs. 5.5, 5.6, 5.7, and 5.8, the PMOS device with high threshold voltage or thick oxide thickness is a good solution to realize the MOS capacitor of loop filter in low-cost second-order PLL. The new circuit design technique for compensating the gate tunneling leakage of MOS capacitor in low jitter and low-cost PLL is also needed to be developed in nanoscale CMOS technique.

5.6. Overview on the Prior Designs of Loop Filter With Gate Tunneling Leakage Compensation Technique in PLL

5.6.1. Capacitor Structure

The MOS capacitor of loop filter in PLL can be designed with thick gate-oxide

device or metal-insulator-metal capacitor (MIM) to reduce the impact of gate tunneling leakage on performance of PLL [107], [108]. Because the gate tunneling leakage of MOS capacitor is proportion to oxide thickness, the thick gate-oxide device has smaller gate tunneling leakage than thin gate-oxide device in nanoscale CMOS technology. However, the threshold voltage of thick gate-oxide device is higher than that of thin gate-oxide device in nanoscale CMOS process. Thick gate-oxide device needs a high voltage level to reach strong inversion region. This consequently would cause headroom issues and limit the tunneling range of VCO in PLL. These problems can be solved by using thick gate-oxide with multi threshold voltage device in naonoscale CMOS process. The capacitor with MIM structure is no gate tunneling leakage problem. However, MIM capacitor needs more silicon area than MOS capacitor under the same capacitance in nanoscale CMOS technology. Therefore, the capacitor of loop filter in PLL realized with MIM capacitor will increase the fabrication cost.

5.6.2. Opamp Base Compensation Technique

Fig. 5.10 re-draws the PLL with opamp base gate tunneling leakage compensation circuit [109]. The gate tunneling leakage compensation circuit consists with dummy MOS capacitor C_C, M_1, M_2, and opamp to compensate the gate tunneling leakage of MOS capacitors C_1 and C_2. The MOS capacitors of C_1, C_2, and C_C are realized with thin gate-oxide device. The M_1 and M_2 devices form the current mirror. The dimension of MOS capacitor C_C is smaller than that of MOS capacitors C_1 and C_2. Because the gate voltage of MOS capacitor C_1 is not equal to voltage at V_{CTRL} node in track state of PLL, the locked time of PLL should be increased by using the gate tunneling leakage compensation technique. In the locked state of PLL, the voltage at V_{CTRl} node and gate voltage of MOS capacitor C_1 are almost equal. The opamp with negative feedback can be used to keep that the V_+ and V_{ctrl} nodes have the same voltage potential. Because the gate tunneling leakage and capacitance of MOS capacitor are proportion to device dimension and oxide thickness, the relationship between I_1, I_2, and total gate tunneling gate leakage $I_{GTL,LF}$ of MOS capacitors C_1 and C_2 in loop filter can be expressed by

$$I_{GTL,LF} = I_1 = \frac{C_1 + C_2}{C_C} \times I_2 \times \frac{\left(W/L\right)_{M1}}{\left(W/L\right)_{M2}}, \tag{5.6}$$

where the I_2 is the gate tunneling leakage of dummy MOS capacitor C_C. Therefore, the gate tunneling leakage of loop filter with MOS capacitor in PLL can be compensated by this technique.

Fig. 5.11 re-draws another PLL with opamp base gate tunneling leakage compensation circuit [111]. This compensation technique uses a thick gate-oxide device (or MIM capacitor) realized the capacitor C_2 of loop filter and the opamp as gate tunneling compensation circuit. In the locked state of PLL, the voltage at V_{CTRl} node and gate voltage of MOS capacitor C_1 are almost equal. The opamp uses to keep that the voltage at V_{CTRL} node and the gate voltage of MOS capacitor C_1 have the same voltage potential. The gate tunneling leakage of MOS capacitor C_1 can be compensated by opamp. Therefore, the gate tunneling leakage of MOS capacitor C_1 in PLL can be compensated by this technique.

5.6.3. Non-Opamp Base Compensation Technique

Fig. 5.12 re-draws another PLL with non-opamp base gate tunneling leakage base compensation circuit [112]. The gate tunneling leakage compensation circuit consists of a charge pump CPC, MOS capacitors of C_{CP} and C_{CN}, and current source P_{COMP}. When there is a leakage at node V_{CTRL}, the duration of the PFD output "UP" signal is longer than the PFD output "DN" signal. The gate tunneling leakage compensation circuit integrates this error at node V_{CTRL} which controls the compensating current I_{comp} to compensate the gate tunneling leakage $I_{GTL,LF}$ of MOS capacitors C_1 and C_2. To avoid the gate tunneling leakage of MOS capacitors C_{CP} and C_{CN}, the MOS capacitors C_{CP} and C_{CN} are realized with thick gate-oxide devices. The area penalty is insignificant since the capacitance value of MOS capacitors C_{CP} and C_{CN} is far less than that of MOS capacitors C_1 and C_2. Since the capacitance value of MOS capacitors C_{CP} and C_{CN} does not have to be precise, they are built using both PMOS and NMOS thick gate-oxide device to address strong-inversion turn-on voltage issues. In the locked state of PLL, the relationship between compensating current

I_{COMP} and total gate tunneling gate leakage $I_{GTL,LF}$ of MOS capacitors C_1 and C_2 in loop filter can be expressed by

$$I_{COMP} = I_{GTL,LF}, \tag{5.7}$$

$$\frac{\Delta t}{(C_{CP} + C_{CN})} = \sqrt{V_{TH} + \frac{I_{GTL,LF}}{\left(\frac{1}{2}\right)\mu C_{OX}\left(\frac{W}{L}\right)_{PCOMP}}}, \tag{5.8}$$

where Δt is the static phase error of PLL due to the gate tunneling leakage of loop filter, V_{TH} is the threshold voltage of P_{COMP} device, C_{OX} is the gate oxide capacitance per unit area of P_{COMP} device.

5.6.4. Capacitor Multiplier

Fig. 5.13 re-draws loop filter with voltage-mode capacitor multiplier [117]. The capacitor C1 of loop filter is multiplier by miller capacitor theory. A non-inverting CMOS opamp is used as the amplifier input stage, followed by an inverting unity gain buffer for the negative voltage gain, as shown in Fig. 13. The effective input capacitance in Fig. 13 is given by

$$C_1 = \left(1 + \left|A_V\right|\right) C_F = \left(2 + \frac{R_4}{R_3}\right) C_F, \tag{5.9}$$

where A_V=-(1+R_4/R_3) is the amplifier voltage gain, and C_F is the physical feedback capacitance. If we choose R_3=R_4, the C_1 is equal to 3C_F. The silicon area far C_F to implement capacitor C_1 is therefore reduced by 67% [15]. Because the gate tunneling leakage and capacitance of MOS capacitor are proportion to device dimension, the smaller device dimension of MOS capacitor has smaller gate tunneling leakage that larger device dimension of MOS capacitor. Therefore, the impact of gate tunneling leakage on performance of PLL will be reduced by using the voltage-mode capacitor multiplier in advanced CMOS technology.

Fig. 5.14 re-draws current-mode PLL with current-mode capacitor multiplier [118], [119]. Compared with conventional charge-pump PLL, the main difference is it utilizes a current-mode filter that drives the current controlled oscillator (ICO) directly.

The charge pump current I_{CP} is a portion of the control current of the ICO, as referred to self-biased technique [120]. The transfer function can be expressed by

$$\frac{I_{OUT}}{I_{IN}} \cong (1-\alpha)\frac{1-\frac{\alpha}{1-\alpha}SR_GC_1}{SR_GC_1}, \tag{5.10}$$

The transconductance gm is degenerated by the resistor R_G without compromising the tuning range. So the effective loop capacitance is given by

$$C_{eff} = MC_1, \tag{5.11}$$

$$M = \frac{\alpha}{\alpha - 1}, \tag{5.12}$$

The left-hand plane (LHP) zero guarantees the stability of the current-mode loop filter. The $\alpha/(\alpha-1)$ term of current-mode loop filter should be designed larger than zero. So the current-mode loop filter is similar to the conventional loop filter in PLL. The self-biased current-mode filter is biased by PLL loop, then the power and die size could be further saved [118], [119]. Because the gate tunneling leakage and capacitance of MOS capacitor are proportion to device dimension, the smaller device dimension of MOS capacitor has smaller gate tunneling leakage that larger device dimension of MOS capacitor. Therefore, the impact of gate tunneling leakage on performance of PLL will be reduced by using the current-mode capacitor multiplier in advanced CMOS technology.

However, using extra components to realize the loop filter by using the capacitor multiplier technique will increase the extra noise sources to degrade the performances of PLL in advanced CMOS technology.

5.7. Summary

The influence of gate tunneling leakage in MOS capacitor on circuit performances of second-order PLL has been analyzed and investigated in a 90-nm CMOS process. The locked time, static phase error, and jitter of second-order PLL are degraded by gate tunneling leakage of MOS capacitor in loop filter. The high input

signal frequency can be used to reduce the impact of gate tunneling leakage on performance of second-order PLL in nanoscale CMOS technology. The PMOS device with high threshold voltage and thick oxide thickness can be used to realize the MOS capacitor in the loop filter for achieving low-jitter and low-cost second-order PLL. Overview on the prior designs of compensation techniques to reduce the gate tunneling leakage on MOS capacitor in loop filter of PLL is also provided in this work. Considering the chip area, circuit performance and fabrication cost in advanced CMOS technology, the capacitor multiplier technique is a good choice to realize the MOS capacitor in second-order PLL.

Table 5.1

Major Gate Tunneling Leakage Mechanisms of MOSFET Device in Nanoscale CMOS Technology [27]

Current Component	I_{gc}	I_{gb}		I_{gso}/I_{gdo}
Region of Operation	Inversion	Vg>0	Vg<0	All Bias
PMOS	HVB	ECB	HVB	ECB
NMOS	ECB	HVB	ECB	ECB

Table 5.2

The Summary of Gate Tunneling Leakage Per Unit Area under Different Threshold-Voltage NMOS and PMOS Capacitors in a 90-nm CMOS Process

MOS Capacitor			
NMOS		PMOS	
Structure	Gate Tunneling Leakage	Structure	Gate Tunneling Leakage
Standard-V_{TH}	1.11 nA/μm^2	Standard-V_{TH}	0.654 nA/μm^2
High-V_{TH}	0.764 nA/μm^2	High-V_{TH}	0.401 nA/μm^2
Low-V_{TH}	1.161 nA/μm^2	Low-V_{TH}	0.701 nA/μm^2
Native NMOS	1.571 nA/μm^2		
1.8V NMOS	≈ 10^{-26} A/μm^2	1.8V PMOS	≈ 10^{-22} A/μm^2
1.8V Native NMOS	≈ 10^{-25}A/μm^2		

Table 5.3

The Design Parameters and Simulated Results of Second-Order PLL in a 90-nm CMOS Process

Design Parameters of PLL in a Standard 90-nm CMOS Process			
Operating Voltage	1 V	C1	85.172 pF
Input Frequency	25 MHz	C2	8.782 pF
Output Frequency	200 MHz	R1	3.2168 kΩ
Charge Pump Current	50 μA	Phase Margin	57 ^{o}
Divided by N	8	Loop Bandwidth	1.8 MHz
VCO Gain	625 MHz	Damping Factor	≈ 1.1
Simulated Results of PLL in a Standard 90-nm CMOS Process			
Locked Time	1.3 μsec	Output Jitter at 200 MHz	2.7 psec
Static Phase Error	45 psec	Total Power Consumption	4.8647 mW

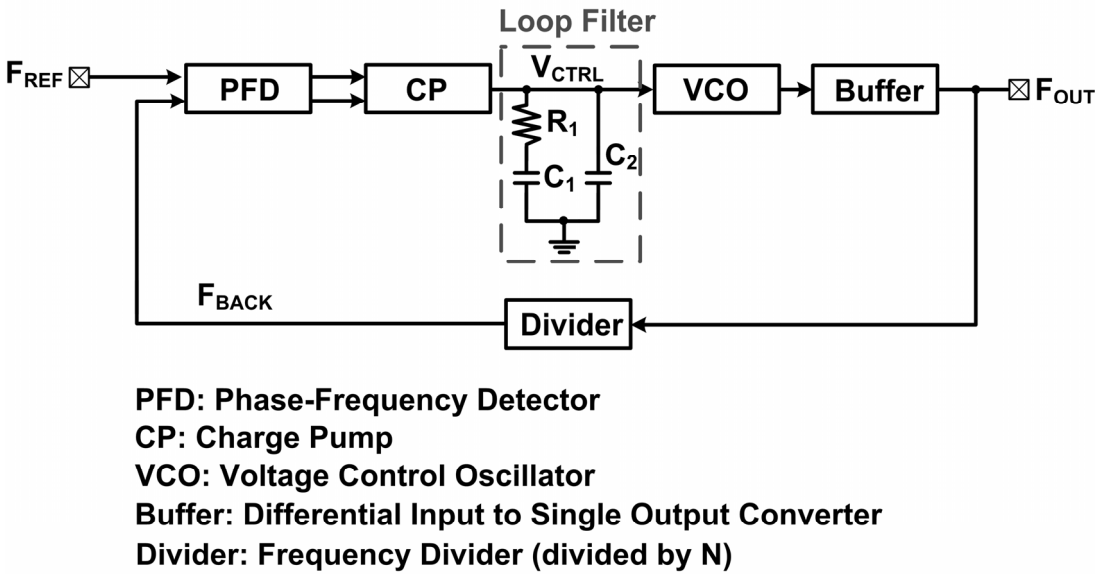
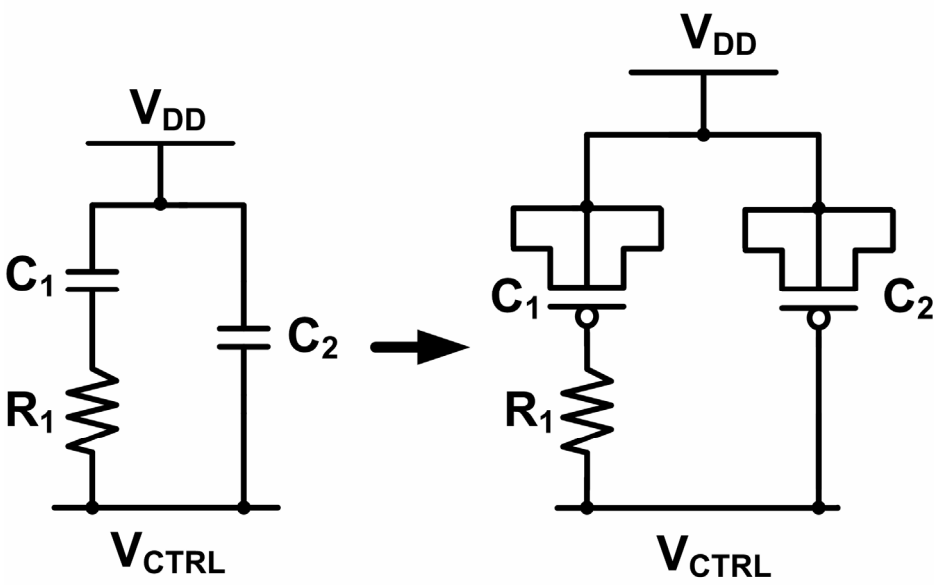
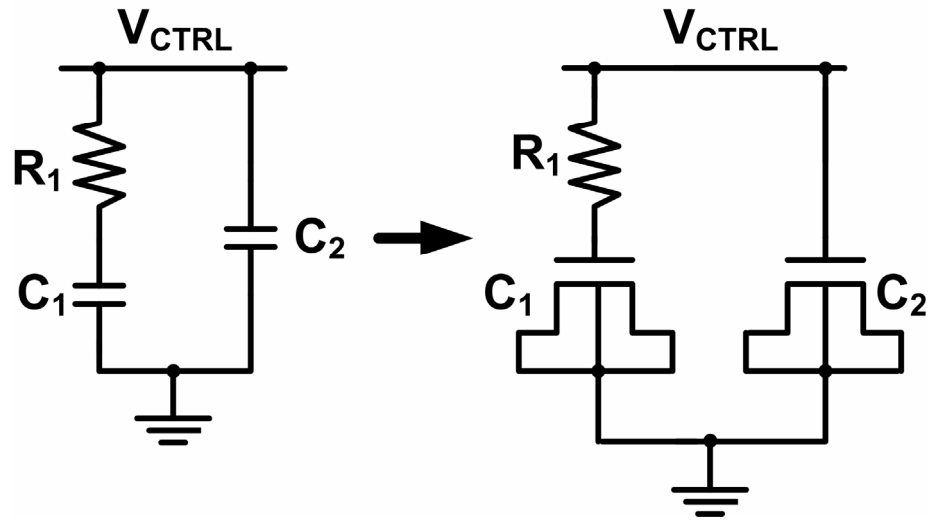


Fig. 5.1. The basic phase locked loop with second-order low-pass loop filter structure.

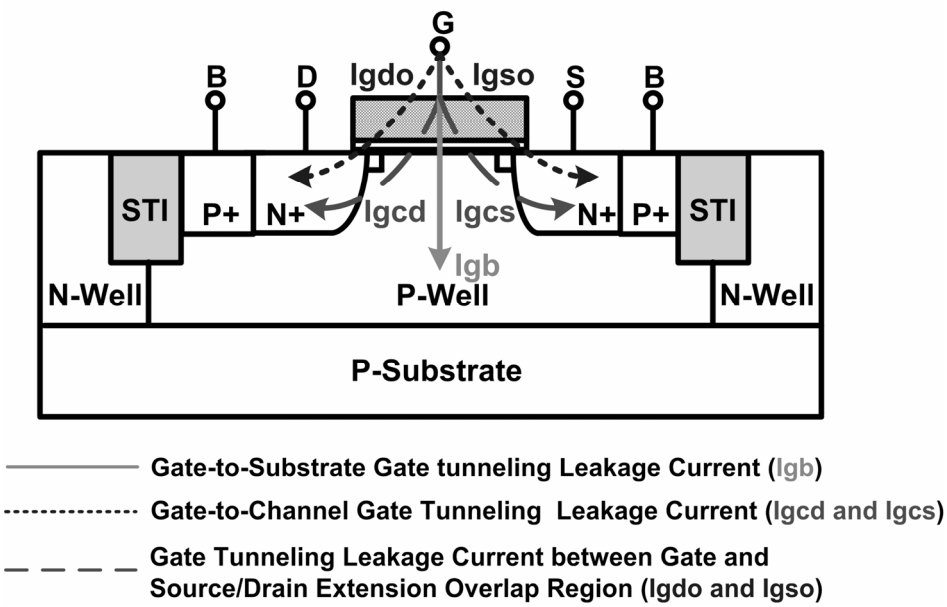


(a)

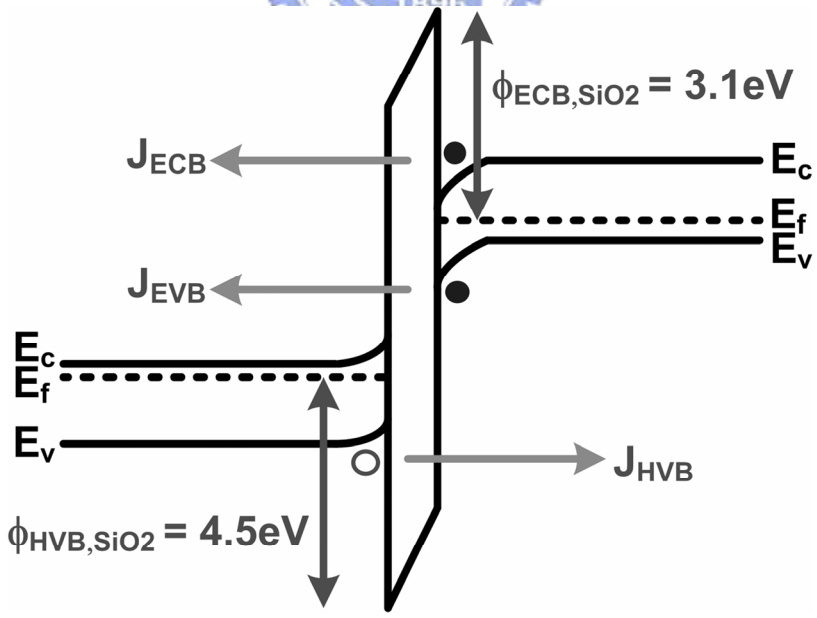


(b)

Fig. 5.2. The second-order loop filter realized with (a) PMOS and (b) NMOS capacitors.



(a)



(b)

Fig. 5.3. (a) Gate tunneling leakage in a thin oxide MOSFET device, and (b) carrier tunneling process with different barrier voltage.

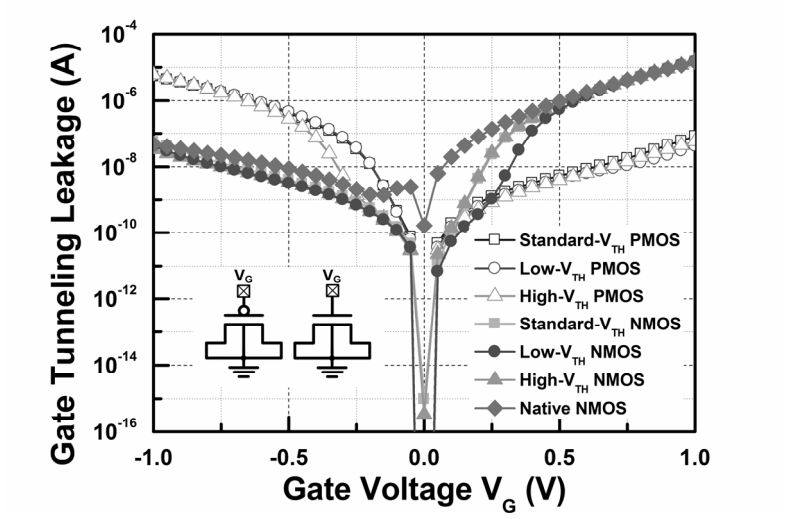


Fig. 5.4. The simulated dependence of gate tunneling leakage on different threshold-voltage NMOS and PMOS capacitors under different gate voltages in a 90-nm CMOS technology.

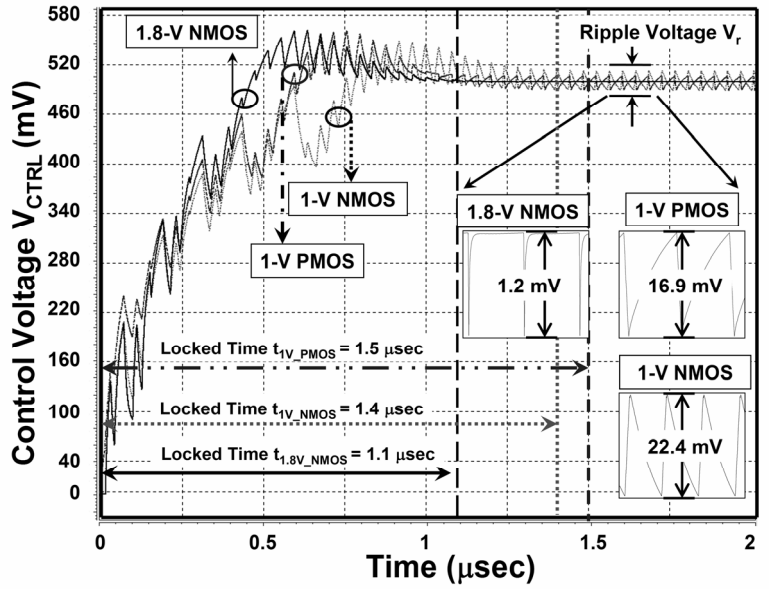


Fig. 5.5. The simulated control voltage waveforms to find the locked time under MOS capacitors with different oxide thicknesses in second-order PLL.

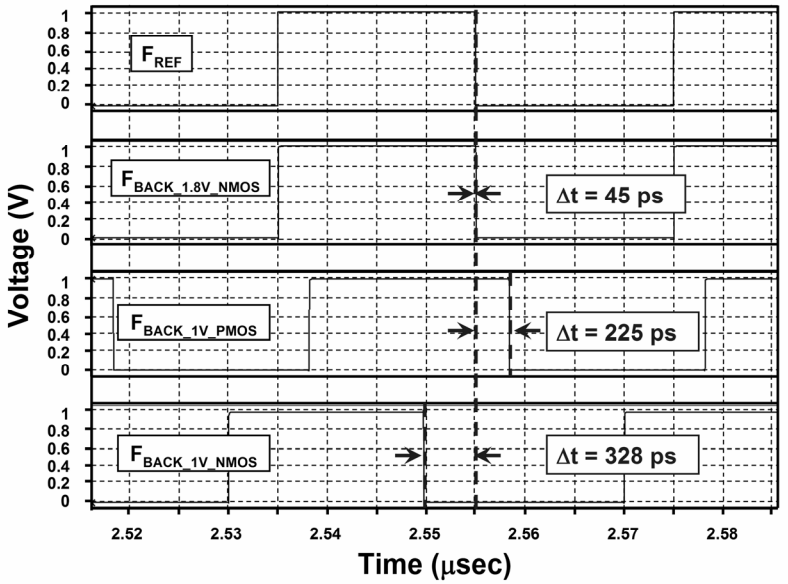


Fig. 5.6. The simulated voltage waveforms to find the static phase error (Δt) under MOS capacitors with different oxide thicknesses in second-order PLL.

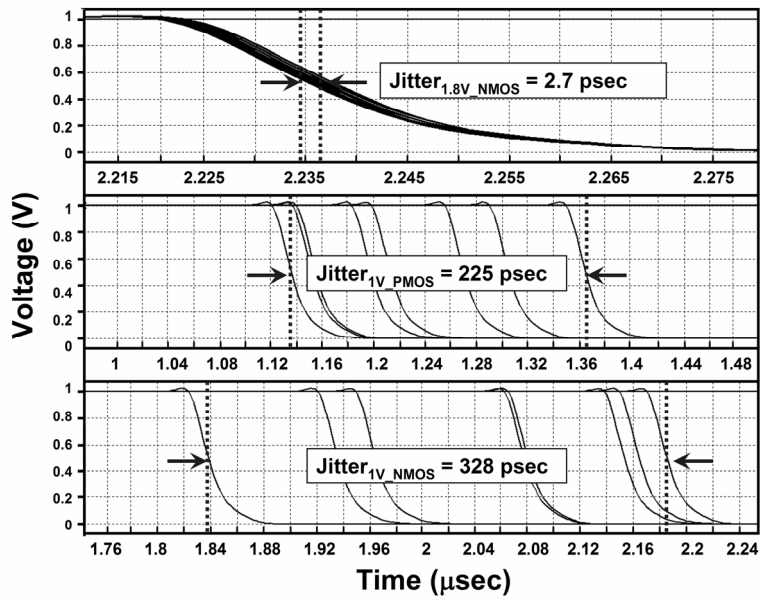


Fig. 5.7. The simulated voltage waveforms to find the jitter under MOS capacitors with different oxide thicknesses in second-order PLL.

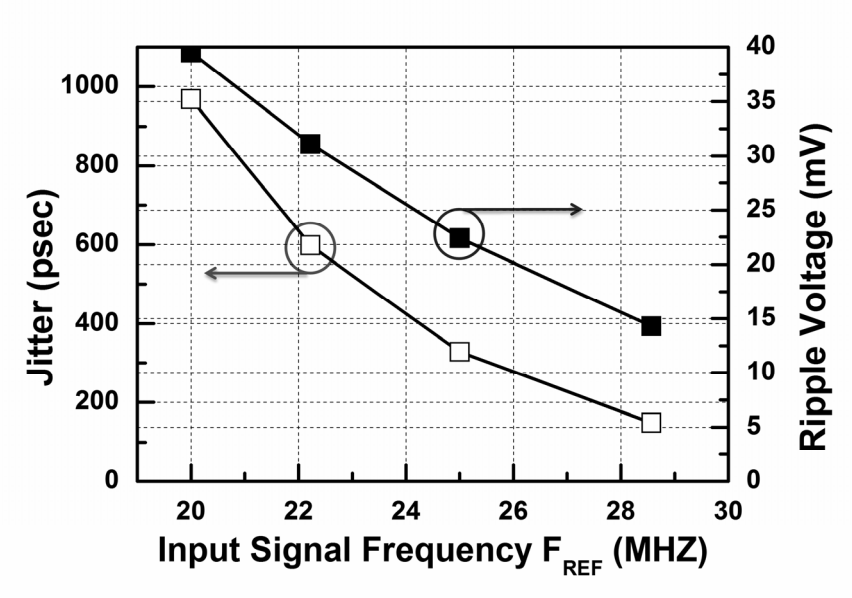


Fig. 5.8. The dependence of different input signal frequencies on jitter and ripple voltage under different oxide thickness devices in the MOS capacitor.

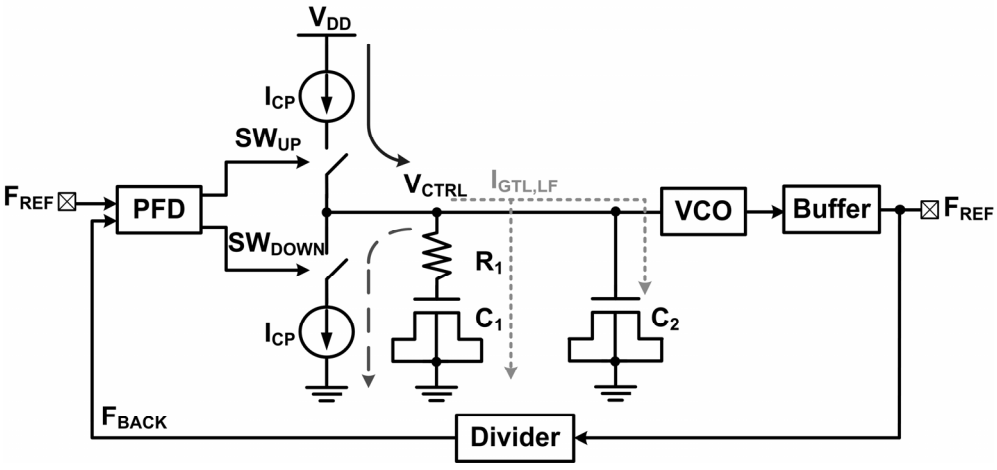


Fig. 5.9. The schematic of second-order PLL including gate tunneling leakage effect.

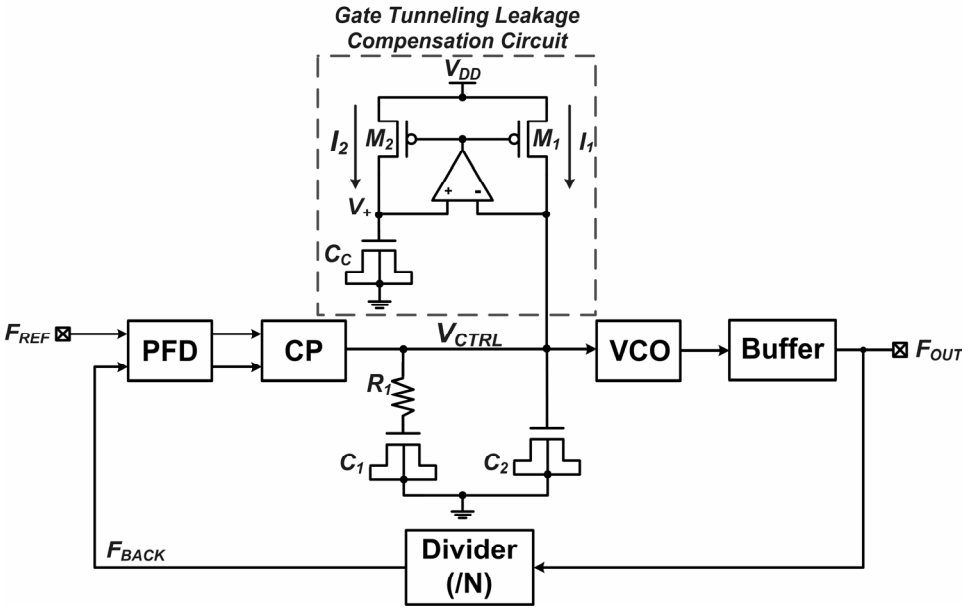


Fig. 5.10. The schematic of PLL with opamp base gate tunneling leakage compensation circuit by only using thin gate-oxide device [109].

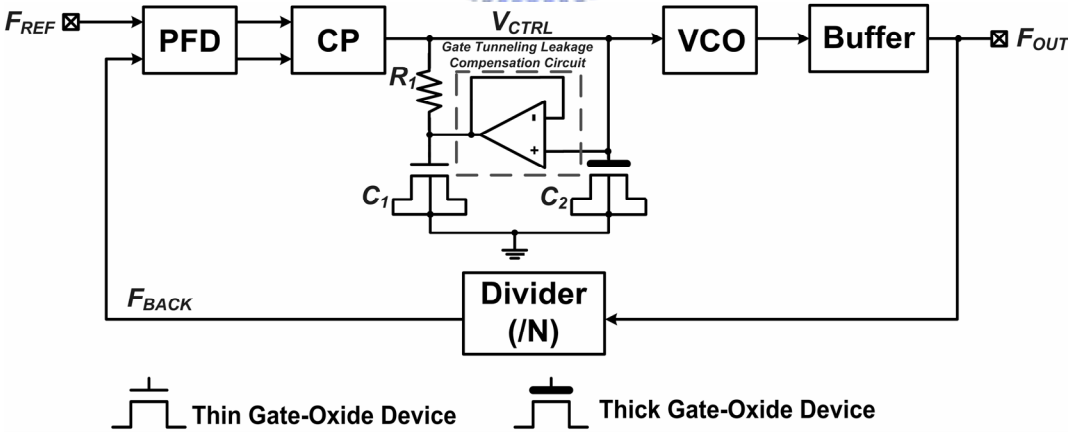


Fig. 5.11. The schematic of PLL with opamp base gate tunneling leakage compensation circuit [111].

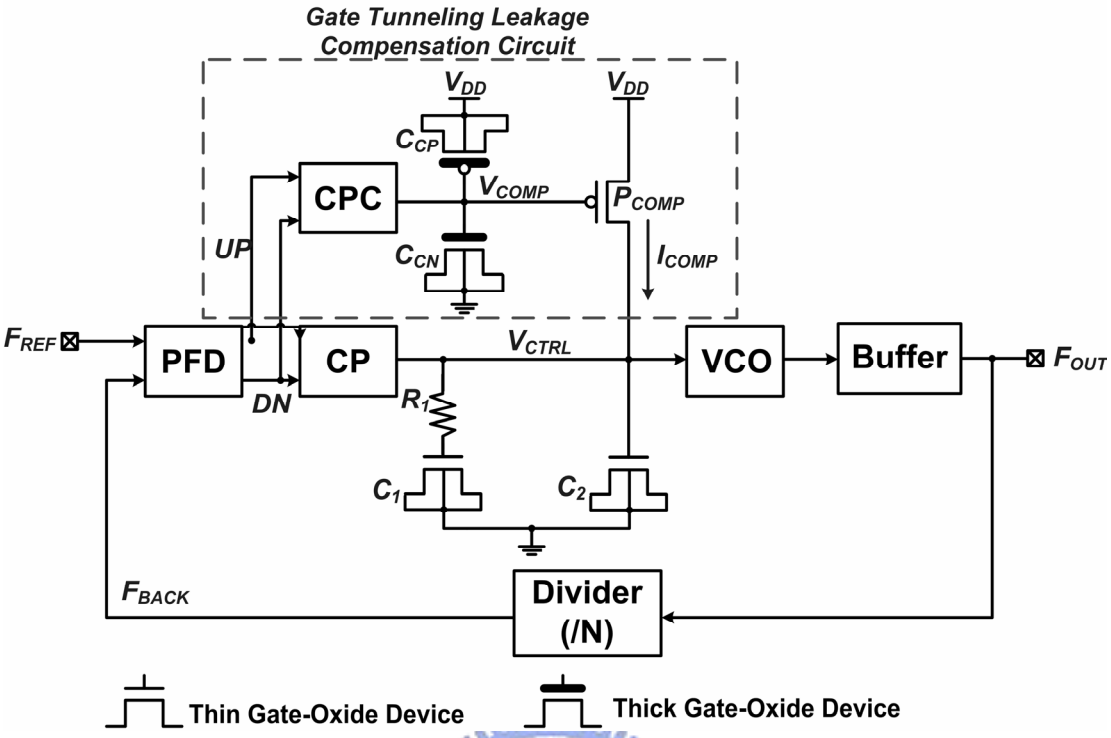


Fig. 5.12. The schematic of PLL with non-opamp base gate tunneling leakage compensation circuit [112].

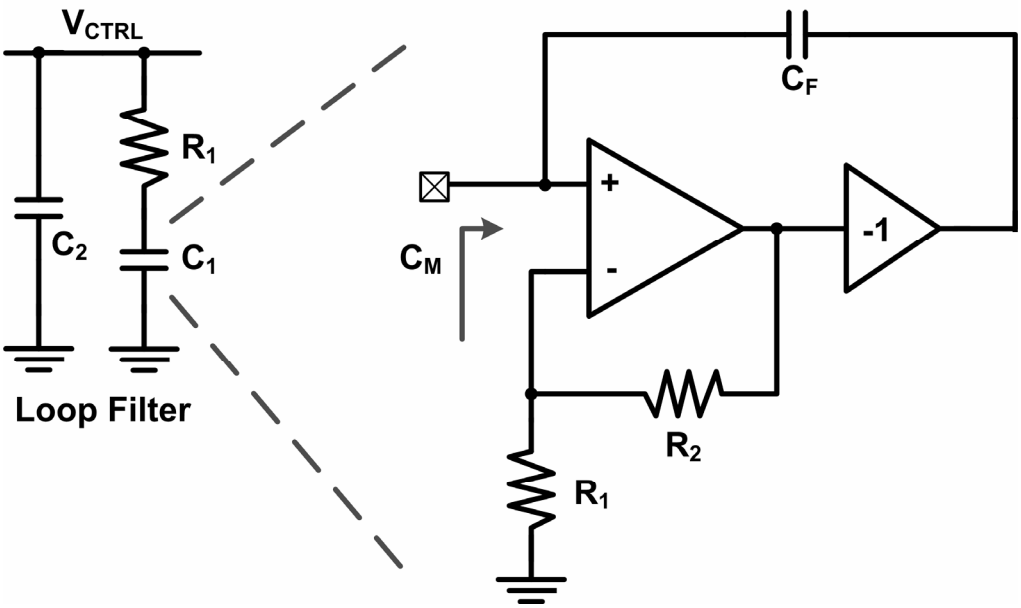


Fig. 5.13. The loop filter with voltage-mode capacitor multiplier [117].

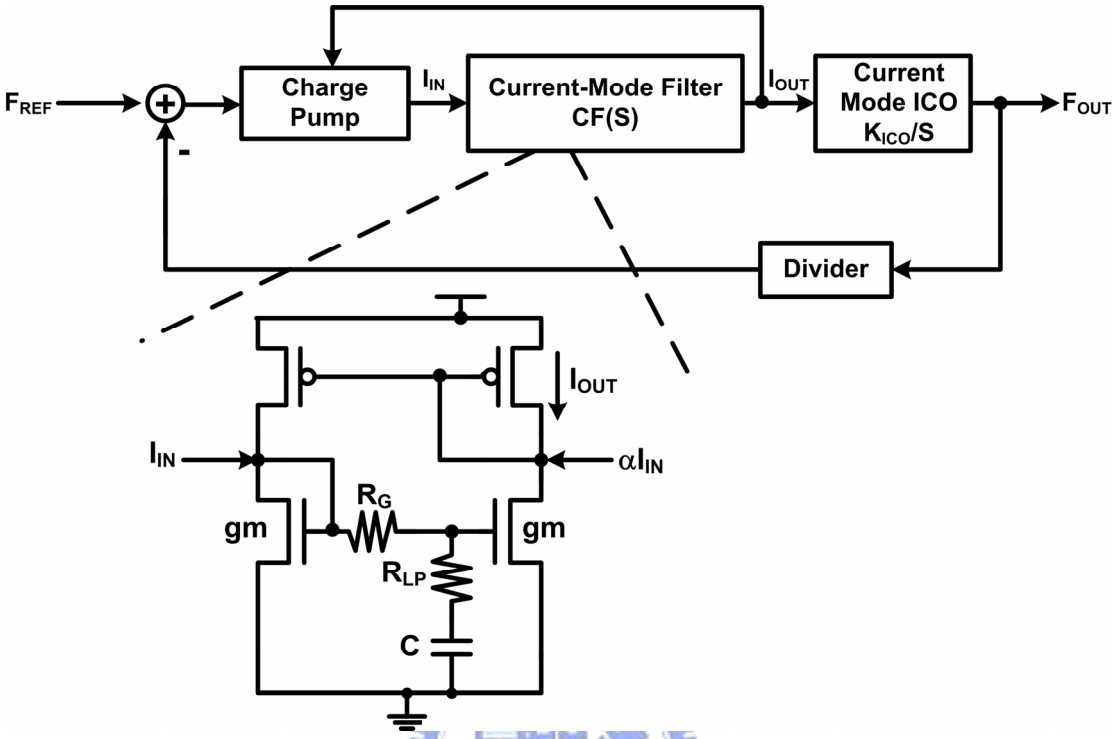


Fig. 5.14. The schematic of current-mode PLL with current-mode capacitor multiplier technique [118], [119].

CHAPTER 6

New Gate Bias Voltage Generating Technique With Threshold-Voltage Compensation for On-Glass Analog Circuits in LTPS Process

A new proposed gate bias voltage generating technique with threshold-voltage compensation for analog circuits in the low-temperature polycrystalline silicon LTPS thin-film transistors (TFTs) is proposed. The new proposed gate bias voltage generating circuit with threshold-voltage compensation has been successfully verified in a 8-μm LTPS process. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under biasing voltage of 3 V. The new proposed gate bias voltage generating technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented by LTPS process on glass substrate for active matrix LCD (AMLCD) panel.

6.1. Background

Low-temperature poly-Si LTPS thin-film transistors (TFTs) have attracted a lot of attentions in the applications with the integrated on-panel peripheral circuits for active-matrix liquid crystal display (AMLCD) and active-matrix light emitting diodes (AMOLEDs) [121]-[123]. Recently, LTPS AMLCDs integrated with driving and control circuits on glass substrate have been realized in some portable systems, such as mobile phone, digital camera, notebook, etc. In the near future, the AMLCD fabricated in LTPS process is promising toward System-on-Panel (SoP) or System-on-Glass (SoG) applications, especially for achieving a compact, low-cost, and low-power display system [124].

The LCD data driver contains shifter registers, level shifters, digital-to-analog converters (DACs), and output buffers. The biasing circuit is a critical circuit block for analog circuits on LCD panel to achieve low power consumption, high speed, and high resolution. However, the poly-Si TFT device suffers from significant variation in its threshold voltage, owing to the nature of poly silicon crystal growth in LTPS process. The threshold-voltage variation across a 2.7-inch panel was about 300 mV [125]. The variation could even be as large as 1 V in some high-performance TFT devices across a large substrate area [126]. The threshold-voltage variations of TFT devices will cause large mismatches on the biasing voltages and currents in analog circuits to result in non-uniformity of performances among analog circuits over the whole panel. The design with threshold-voltage compensation for analog circuits on glass substrate is a very important challenge for SoP applications. The design technique with switches and capacitors under multi-phase clock operation were usually used to compensate the threshold-voltage variation among TFT devices in LTPS AMLCDs [127]-[129]. Some design technique with switch and capacitor under multi-phase clock operation had used to reduce the offset voltage of analog buffer in LTPS process [127]. In LTPS technology, the on-panel output buffers with a pair of n-type and p-type TFT devices immune to the mismatch of threshold voltage were also reported [128], [129]. The mismatch of threshold voltage can be compensated by a holding capacitor or the mathematical product of voltage gain. Besides, the threshold-voltage-shift compensation technique was used to compensate the threshold-voltage variation for differential amplifier in analog circuits [130]. However, those techniques [127]-[130] only emphasize the impact of threshold-voltage variation on offset voltage of analog buffers on glass substrate. The biasing circuit with threshold-voltage compensation for analog circuits in LTPS process is not yet reported in the literature.

In this paper, a method to reduce the influence of threshold-voltage variation on the gate bias voltage generating circuit for analog circuits on glass substrate is proposed. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under biasing voltage of 3 V. The new proposed biasing technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented in LTPS process for active matrix LCD (AMLCD) panel.

6.2. Impact of Threshold-Voltage Variation on TFT I-V Characteristics

In general, the TFT devices on glass substrate are usually designed in saturation region for analog circuit applications. The small-signal gain and frequency response of analog circuits in LTPS process are determined by transconductance (g_m) and output resistance (r_o) of TFT devices. The small-signal parameters of transconductance (g_m) and output resistance (r_o) in TFT devices can be expressed as, respectively,

$$g_m = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right) = \frac{2I_D}{\left(V_{GS} - V_{TH}\right)}, \tag{6.1}$$

$$r_o = \frac{V_A}{I_D}, \tag{6.2}$$

where μ is the mobility of carrier, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage of TFT device, V_{GS} is the gate-to-source voltage of TFT device, V_A is the Early voltage, and I_D is the drain current of TFT device. Comparing equations (6.1) and (6.2), the drain current I_D is the major factor for analog circuits in LTPS process. Therefore, the performances of analog circuits in LTPS process are dominated by drain current of TFT device. The drain current I_D of TFT device operated in saturation region can be expressed as

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2. \tag{6.3}$$

The channel-length modulation of TFT device is not included in equation (6.3). The threshold voltage (V_{TH}) of TFT device is an important parameter in equation (6.3), so the threshold-voltage variation among TFT devices will cause the variation on drain currents of TFT devices to degrade the circuit performances in analog circuits on glass substrate. How to design a stable biasing circuit with threshold-voltage compensation to reduce non-uniformity of performances in analog circuits over the whole panel in LTPS process is an important design challenge.

The HSPICE with Monte Carlo Analysis can be used to simulate and analyze the impact of threshold-voltage variation on drain current of TFT device. The threshold-voltage variation of TFT device on glass substrate can be modeled by Gaussian distribution. The simulated waveforms of N-TFT drain current I_D with 50 % threshold-voltage variation of Gaussian distribution under different gate voltages V_G in a 8-μm LTPS process is shown in Fig. 6.1. The dimension of N-TFT device is 80μm/8μm. The gate voltage is biased from 1.3 V to 4.3 V. In order to confirm that N-TFT device is operated in saturation region, the drain voltage of N-TFT device is also biased from 1.3 V to 4.3 V to keep gate-to-drain voltage of zero volt. The simulated result shows that the N-TFT device with 50 % threshold-voltage variation of Gaussian distribution causes the drain current with a variation as large as 22 μA in LTPS process. Therefore, the large variations on drain currents of TFT devices will cause large mismatches on the biasing voltages and currents in analog circuits to further result in non-uniformity of performances in analog circuits over the whole panel. For the System-on-Plane (SoP) applications, to reduce the impact of threshold-voltage variation on performance among analog circuits in LTPS process is a very important design challenge.

6.3. New Proposed Gate Bias Voltage Generating Technique With Threshold-Voltage Compensation

6.3.1 Design Concept

The new proposed gate bias voltage generating technique with threshold-voltage compensation is illustrated in Fig. 6.2. The biasing current I_{D_MC} is a small current used to bias the M_C device operated in weak inversion region. When the M_C device operated in weak inversion region, the gate control voltage V_{GC} can be written as

$$V_{GC} \cong V_{BIAS} + V_{TH\_MC}, \tag{6.4}$$

where V_{TH_MC} is the threshold-voltage of M_C device, and V_{BIAS} is the applied biasing voltage. The drain current I_{D_MD} of M_D device can be expressed as

$$I_{D\_MD} = \frac{1}{2}\mu C_{OX}(\frac{W}{L})_{MD}(V_{GC} - V_{TH\_MD})^2$$
$$= \frac{1}{2}\mu C_{OX}(\frac{W}{L})_{MD}(V_{BIAS} + V_{TH\_MC} - V_{TH\_MD})^2, \quad (6.5)$$

where V_{TH_MD} is the threshold-voltage of M_D device. The M_C and M_D devices are drawn with the same device dimension. The threshold-voltage difference between M_C and M_D devices can be reduced as small as possible by symmetrical and compact layout in an adjacent location. Therefore, the equation (6.5) can be further rewritten as

$$I_{D\_MD} \cong \frac{1}{2}\mu C_{OX}(\frac{W}{L})_{MD}(V_{BIAS})^2. \quad (6.6)$$

The drain current I_{D_MD} of M_D device can become independent on the threshold voltage and dominated by the V_{BIAS} voltage. The new proposed gate bias voltage generating technique with threshold-voltage compensation does not need any extra clock signal and capacitor to reduce the impact of threshold-voltage variation on the biasing circuit for analog circuits in LTPS processes.

6.3.2. Circuit Implementation

The complete circuit of the proposed gate bias voltage generating technique with threshold-voltage compensation for analog circuit applications in LTPS technology is shown in Fig. 6.3. The new proposed gate bias voltage generating circuit with threshold-voltage compensation is formed with M_1, M_2, M_3, M_4, M_5, and M_6 devices. The M_1, M_2, M_5, and M_6 devices form the current mirror. In order to reduce the power consumption and chip area of the new proposed gate bias voltage generating circuit, the M_3 and M_4 devices are used to realize the referenced current source. The M_3 and M_4 devices are operated in saturation region o generate a biasing current through the current mirror of M_1, M_2, M_5, and M_6 devices to bias M_C device operated in weak inversion region. The voltage V_C can be expressed as

$$V_C = \frac{r(V_B - |V_{TH\_M3}|) + V_{TH\_M4}}{1+r}, \quad (6.7)$$

$$r = \sqrt{\frac{\mu_p \left(W/L \right)_{M3}}{\mu_n \left(W/L \right)_{M4}}} . \tag{6.8}$$

where the V_B is the voltage at source node of M_3 device in proposed gate bias generating circuit. The biasing current I_{D_M4} and I_{D_MC} can be written as, respectively,

$$I_{D\_M4} = \frac{1}{2} \mu C_{OX} \left(\frac{W}{L} \right)_{M4} \left(V_C - V_{TH\_M4} \right)^2 , \tag{6.9}$$

$$I_{D\_MC} = \left(\frac{1}{K} \right) I_{D\_M1} , \tag{6.10}$$

where the K is the dimension ratio of M_5 and M_1 in the current mirror. The K factor is especially designed much larger than one to reduce the impact of biasing current (I_{D_M4}) variation on gate control voltage (V_{GC}) of the new proposed gate bias voltage generating circuit.

The simulated gate control voltage V_{GC} of the new proposed gate bias voltage generating circuit with threshold-voltage compensation under different biasing voltages V_{BIAS} is shown in Fig. 6.4. The typical threshold voltage of N-TFT device in 8-μm LTPS process is approximately 1.3 V. The V_{BIAS} voltage is biased from 0 V to 3V. The gate control voltage V_{GC} is changed from 1.3 V to 4.3 V. The gate control voltage V_{GC} of the new proposed gate bias voltage generating circuit with threshold-voltage compensation is approximately $V_{BIAS}+V_{TH\_MC}$. The HSPICE with Monte Carlo Analysis is used to verify the function of the new proposed gate bias voltage generating circuit with threshold-voltage compensation in LTPS technology. The simulated gate control current V_{GC} of the new proposed gate bias voltage generating circuit with threshold-voltage compensation under the different biasing voltages V_{BIAS} with the 50 % threshold voltage variation (Gaussian distribution) of N-TFT and P-TFT devices is shown in Fig. 6.5. The variation on gate control voltage V_{GC}, which can be used to compensate the threshold-voltage variation of TFT device in LTPS process, is 0.675 V. The simulated drain current I_{D_MD} of the new proposed gate bias voltage generating circuit with threshold-voltage compensation under different biasing voltages V_{BIAS} with the 50 % threshold-voltage variation (Gaussian distribution) of N-TFT and P-TFT devices is shown in Fig. 6.6. The device dimension of M_D device is 80μm/8μm. The gate-to-drain voltage of M_D device is set

to zero voltage to be operated in saturation region. The simulated results show that the 50 % threshold-voltage variation with Gaussian distribution of N-TFT and P-TFT devices causes only a variation of 3.84 μA on the drain current I_{D_MD} in the new proposed gate bias voltage generating circuit with threshold-voltage compensation. Comparing the simulated results of Fig. 6.1 and Fig. 6.6, the new proposed gate bias generating circuit with threshold-voltage compensation can effectively reduce the impact of threshold-voltage variation on the biasing circuit in LTPS process.

6.4. Experimental Results

The new proposed gate bias generating circuit with threshold-voltage compensation has been fabricated in a 8-μm LTPS technology. Fig. 6.7 shows the chip photo of the new proposed gate bias generating technique with threshold-voltage compensation. The test chip size of the new proposed gate bias generating circuit with threshold-voltage compensation circuit is 517 × 389 μm^2 in 8-μm LTPS technology. The averaged power consumption of proposed gate bias generating circuit with threshold-voltage compensation is only 47 μW under the supply voltage of 10 V. In this work, the definitions of mean value and variation (%) of currents in these measured results are adopted as

$$Mean\ Vaule = \frac{I_{D1} + I_{D2} + I_{D3} + I_{D4}}{4}, \tag{6.11}$$

$$Variation\ (\%) = \frac{Mean\ Value - I_{D\_\#}}{Mean\ Value} \times 100\%, \tag{6.12}$$

where the I_{D1}, I_{D2}, I_{D3}, and I_{D4} are drain currents of sample1, sample2, sample3, sample4 of four LPTS N-TFT devices in different panel locations, respectively, and the # is a sample number from 1 to 4. The power supply voltage V_{DD} is set to 10 V. Fig. 6.8 shows the measured dependence of variation (%) on the gate voltage V_G under four LTPS N-TFT devices in different panel locations. The device dimensions of four N-TFT devices are kept at 80μm/8μm in a 8-μm LTPS process. The gate voltages of these samples are biased from 1.3 V to 4.3 V. The gate-to-drain voltage of N-TFT device is set to zero voltage to keep the N-TFT device operated in saturation region. Because the gate-control voltage V_{GC} of the new proposed gate bias

generating circuit is $V_{BIAS}+V_{TH}$, the gate voltage from 1.3 V to 4.3 V is normalized from 0 V to 3 V. The variation (%) among four LPTS N-TFT devices in different panel locations is decreased from 195 % to 30 %, when the gate voltage is increased from 0 V to 3 V. The measured results have confirmed that the variation (%) of four LPTS N-TFT devices in different panel locations under low gate voltage is large, but that under high gate voltage is low.

The measured dependence of variation (%) on the biasing voltage V_{BIAS} among four LTPS test circuits of the new proposed gate bias generating circuit with threshold-voltage compensation in different panel locations is shown in Fig. 6.9. The variation (%) among four LPTS test circuits in different panel locations is decreased from 73 % to 5 %, when the gate voltage is increased from 0 V to 3 V. Comparing the measured results between Fig. 6.8 and Fig. 6.9, the new proposed gate bias generating technique with threshold-voltage compensation can effectively reduce the impact of threshold-voltage variation on the biasing current or biasing voltage for analog circuits in System-on-Panel (SoP) or System-on-Glass (SoG) applications.

6.5. Discussion

When the referenced current source I_{D_M4} is realized with ideal referenced current source, the simulated results show that variation of I_{D_MD} is only 0.27 μA under 50 % threshold-voltage variation (Gaussian distribution) of N-TFT and P-TFT devices. In order to achieve the low power consumption and small chip area, the referenced current source I_{D_M4} in the proposed gate bias voltage generating circuit with threshold-voltage compensation is realized by M_3 and M_4 devices. Because the voltage V_C is dependent on threshold voltages of N-TFT and P-TFT devices, the threshold-voltage variation will cause some variations on the voltage V_C and biasing current (I_{D_M4} and I_{D_MC}) to degrade the performances of the proposed gate bias voltage generating circuit with threshold-voltage compensation. The variation of I_{D_MD} is finally increased from 0.27 μA to 3.84 μA under 50 % threshold voltage variation (Gaussian distribution) of N-TFT and P-TFT devices. In order to reduce the impact of referenced current I_{D_M4} variation on circuit performance, the M_3 and M_4 referenced current source can be further replaced by the modified N-TFT

threshold-voltage referenced current source [131]. The complete circuit of the proposed gate bias voltage generating circuit with N-TFT threshold-voltage referenced current source for analog circuit applications in LTPS technology is shown in Fig. 6.10. When the referenced current source I_{D_M4} is realized with modified N-TFT threshold-voltage referenced current source, the simulated results show that the variation of I_{D_MD} is only 0.36 μA under 50 % threshold-voltage variation (Gaussian distribution) of N-TFT and P-TFT devices, as shown in Fig. 6.11. Because the threshold voltages of N-TFT devices have the same variation trend in the local panel location, the biasing current I_{D_MD} with modified N-TFT threshold-voltage referenced current source can further reduce the variation on performance of the proposed circuit.

6.6. Summary

A new gate bias generating technique with threshold-voltage compensation has been presented to reduce the impact of threshold-voltage variation on analog circuit performance in LTPS technology. The new proposed gate bias generating circuit with threshold-voltage compensation has been successfully verified in a 8-μm LTPS process. The measured results have confirmed that the impact of threshold-voltage variation on drain current of N-TFT device can be reduced from 30 % to 5 % under biasing voltage of 3 V. The new proposed gate bias generating technique with threshold-voltage compensation can be applied to realize analog circuits in LTPS process for System-on-Panel (SoP) or System-on-Glass (SoG) applications.

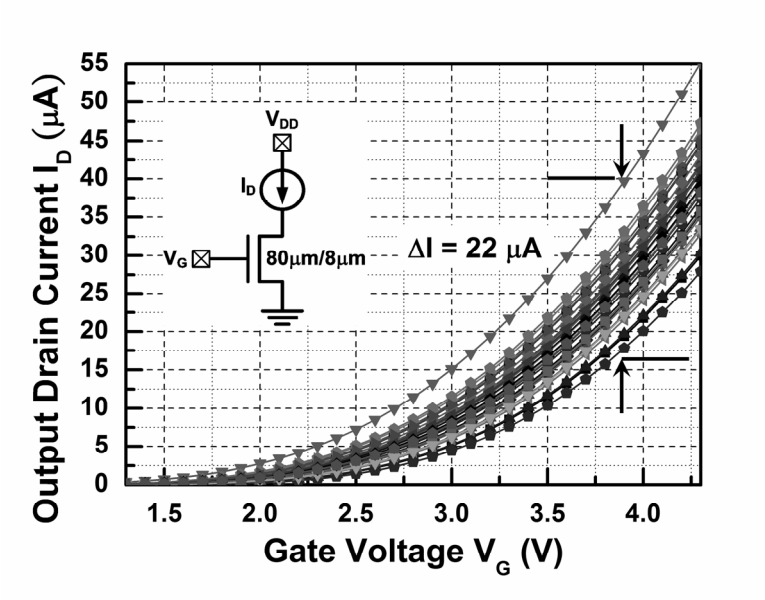


Fig. 6.1. The simulated waveforms of N-TFT drain current I_D with 50 % threshold-voltage variation of Gaussian distribution under different gate voltages V_G in a 8-μm LTPS process.

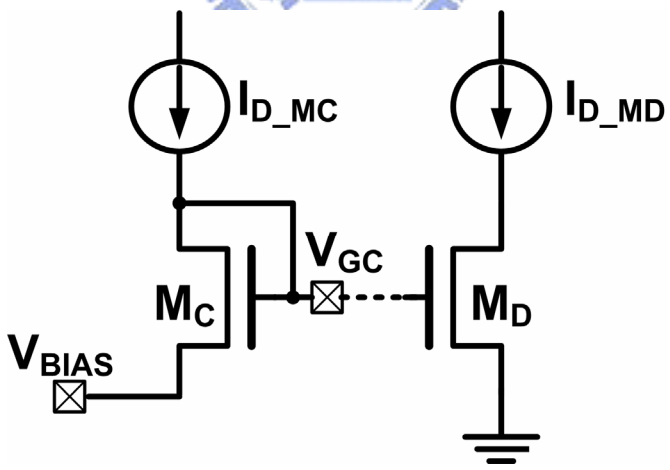


Fig. 6.2. The concept of the new proposed gate bias voltage generating technique with threshold-voltage compensation.

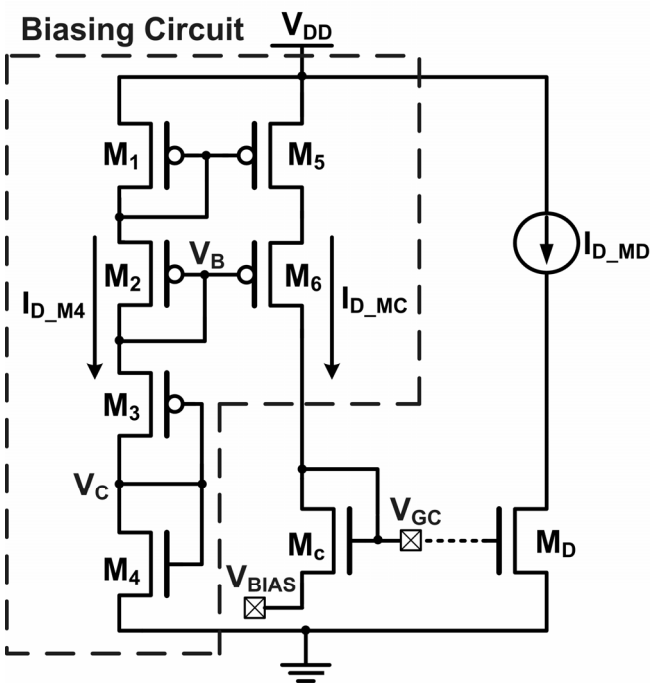


Fig. 6.3. The complete circuit of the proposed gate bias voltage generating circuit with threshold-voltage compensation for analog circuits in LTPS technology.

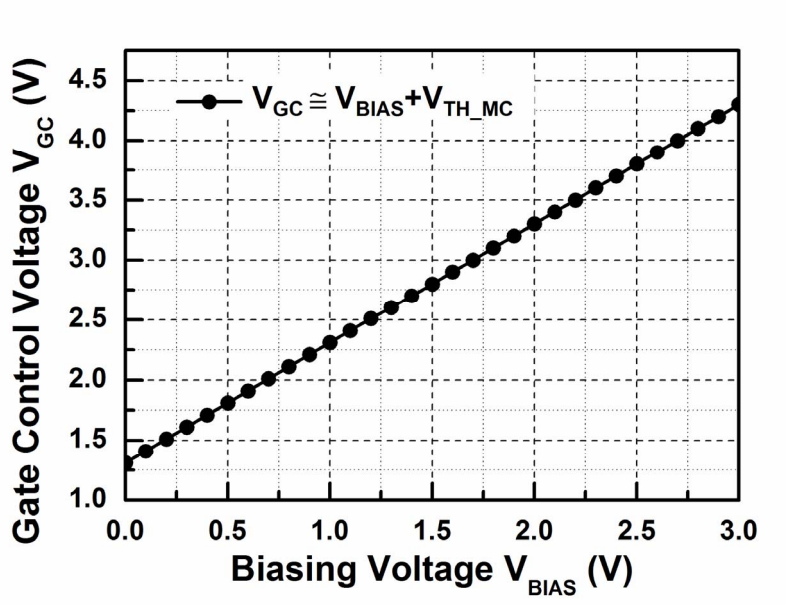


Fig. 6.4. The simulated gate control voltage V_{GC} of the proposed gate bias voltage generating circuit with threshold-voltage compensation under different biasing voltages V_{BIAS}.

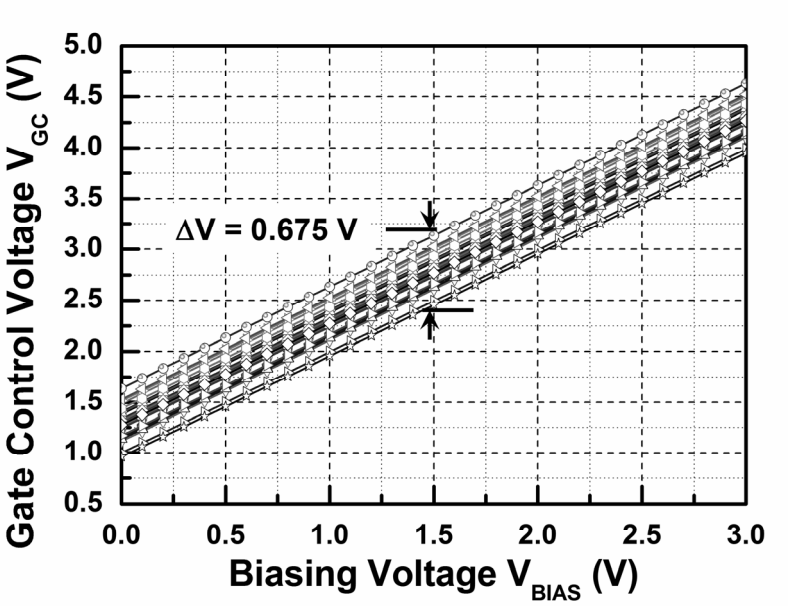


Fig. 6.5. The simulated gate control current V_{GC} of the proposed gate bias voltage generating circuit with threshold-voltage compensation under the different biasing voltages V_{BIAS} with the 50 % threshold voltage variation (Gaussian distribution) on N-TFT and P-TFT devices.

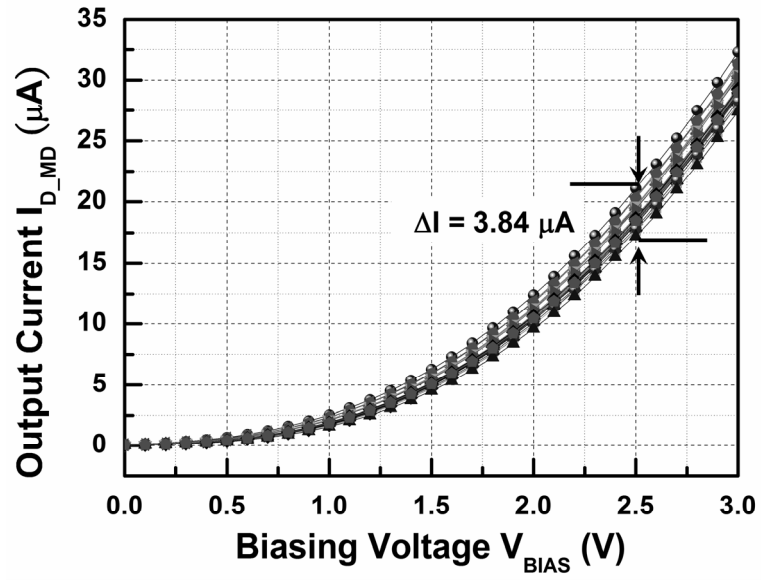


Fig. 6.6. The simulated drain current I_{D_MD} of the proposed gate bias voltage generating circuit with threshold-voltage compensation under different biasing voltages V_{BIAS} with the 50 % threshold voltage variation (Gaussian distribution) of N-TFT and P-TFT devices.

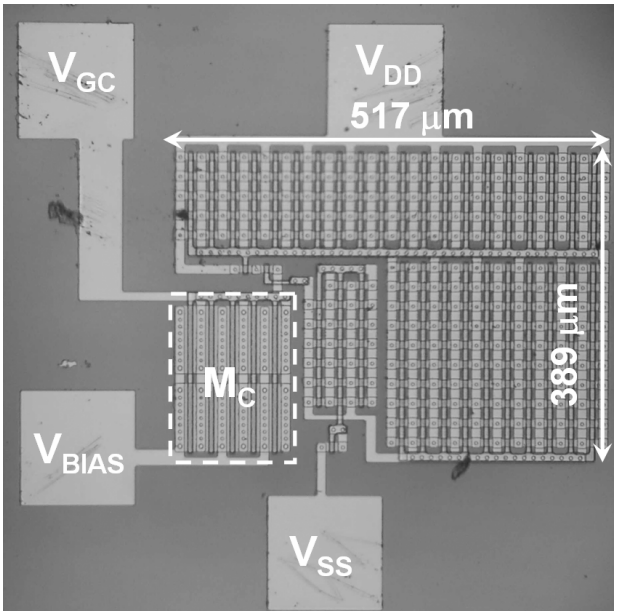


Fig. 6.7. The chip photo of the proposed gate bias generating technique with threshold-voltage compensation fabricated in a 8-μm LTPS process.

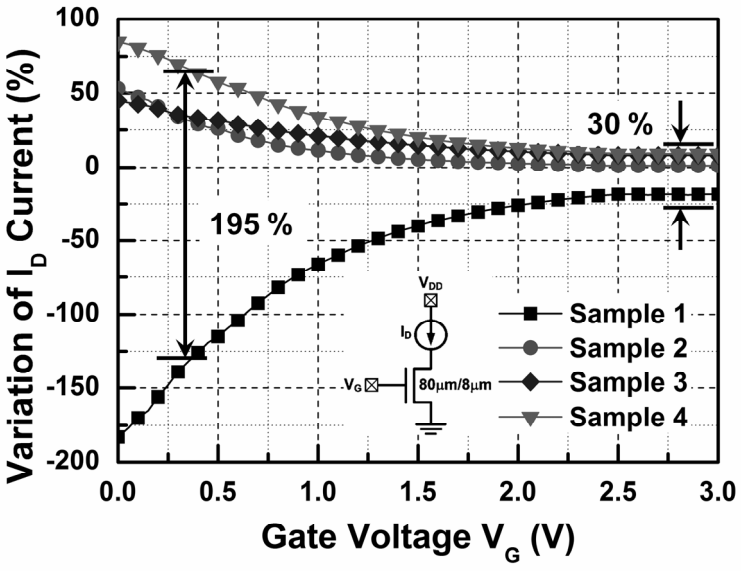


Fig. 6.8. The measured dependence of variation (%) on the gate voltage V_G among four LTPS N-TFT devices in different panel locations.

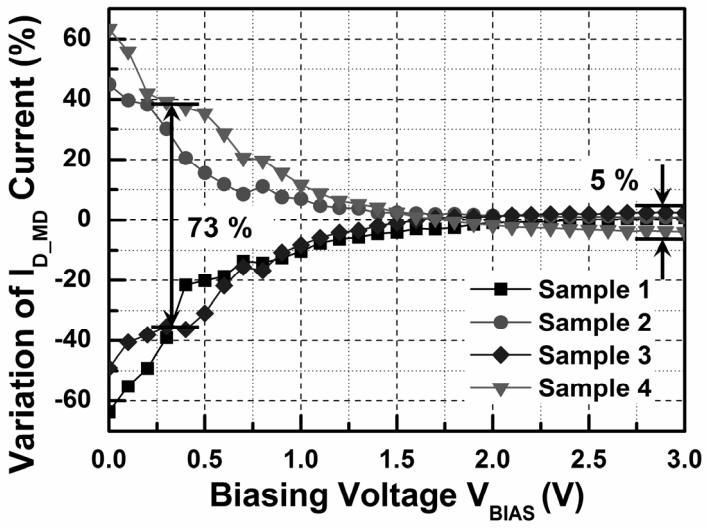


Fig. 6.9. The measured dependence of variation (%) on the biasing voltage V_{BIAS} among four LTPS test circuits of the new proposed gate bias generating technique with threshold-voltage compensation in different panel locations.

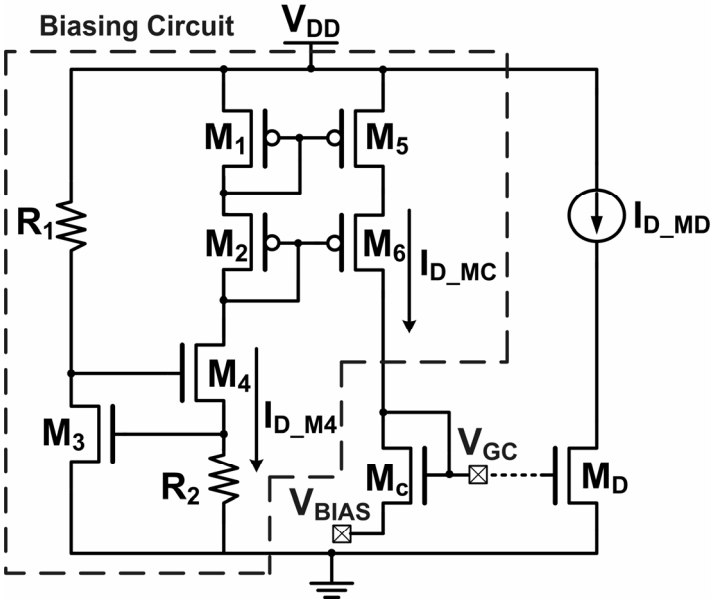


Fig. 6.10. The complete circuit of the proposed gate bias voltage generating circuit with modified N-TFT threshold-voltage referenced current source for analog circuits in LTPS technology.

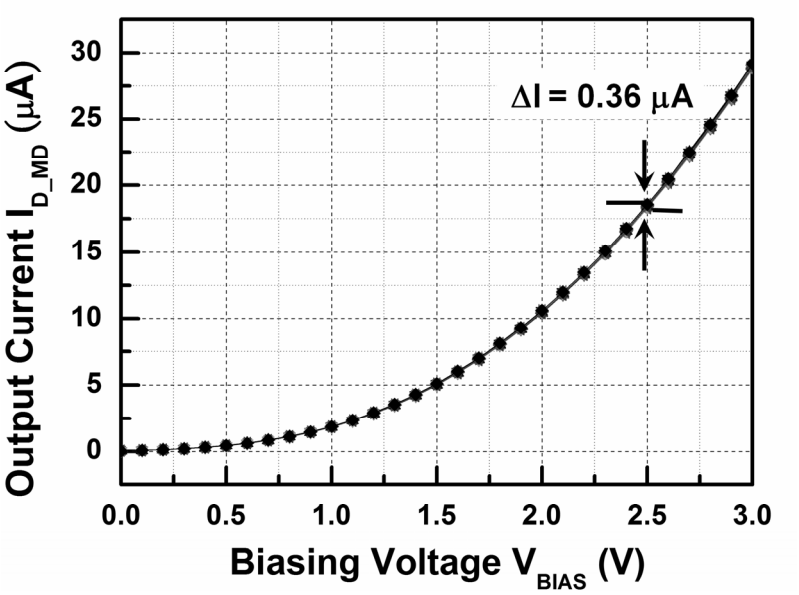


Fig. 6.11. The simulated drain current I_{D_MD} of the proposed gate bias voltage generating circuit with modified N-TFT threshold-voltage referenced current source under different biasing voltages V_{BIAS} with the 50 % threshold voltage variation (Gaussian distribution) of N-TFT and P-TFT devices.

CHAPTER 7

Conclusions and Future Works

This chapter summarizes the main results of this dissertation. Then, some suggestions for the future works about the design and reliability of CMOS analog circuit in low-voltage CMOS processes are also addressed in this chapter.

7.1. Main Results of This Dissertation

Due to the growing popularity of electronic technology, the electronic products are continuously asked to reduce its weight, thickness, and volume. So, the reliability of analog integrated circuit is more and more important. Moreover, with the device dimensions of the integrated circuits scaling down, the operation voltage and gate-oxide thickness of device had also been reduced. However, the extra non-ideal effects of devices have great impact on analog integrated circuit to increase design difficulty, such as the lower operation voltage and thin gate oxide. So the new design technique in low-voltage analog integrated circuit can be developed. The thinner gate oxide of device will cause the reliability problem in nanoscale analog integrated circuit. In this dissertation, a new sub-1-V CMOS bandgap reference and curvature-compensation technique for CMOS bandgap reference circuit with sub-1-V operation, the impact of gate-oxide reliability on CMOS analog amplifier, the impact of gate tunneling current on performances of phase locked loop, and the new gate bias voltage generating technique with threshold-voltage compensation for on-glass analog circuits in LTPS process have been presented.

In Chapter 2, a new sub-1-V CMOS bandgap voltage reference without using low-threshold-voltage device is presented in this paper. The new proposed sub-1-V bandgap reference with startup circuit has been successfully verified in a standard 0.25-μm CMOS process, where the occupied silicon area is only 177 μm × 106 μm. The experimental results have shown that, with the minimum supply voltage of 0.85

V, the output reference voltage is 238.2 mV at room temperature, and the temperature coefficient is 58.1 ppm/°C from -10 °C to 120 °C without laser trimming. Under the supply voltage of 0.85 V, the average power supply rejection ratio (PSRR) is -33.2 dB at 10 kHz. The new sub-1-V curvature-compensated CMOS bandgap reference, which utilizes the temperature-dependent currents generated from the parasitic NPN and PNP BJT devices in CMOS process, is presented. The new proposed sub-1-V curvature-compensated CMOS bandgap reference has been successfully verified in a standard 0.25-μm CMOS process. The experimental results have confirmed that, with the minimum supply voltage of 0.9 V, the output reference voltage at 536 mV has a temperature coefficient of 19.5 ppm/°C from 0 °C to 100 °C. With 0.9-V supply voltage, the measured power noise rejection ratio is -25.5 dB at 10 kHz.

In Chapter 3, the influence of gate-oxide reliability on common-source amplifiers with diode-connected active load is investigated with the non-stacked and stacked structures under analog application in a 130-nm low-voltage CMOS process. The test conditions of this work include the DC stress, AC stress with DC offset, and large-signal transition stress under different frequencies and signals. After overstresses, the small-signal parameters, such as small-signal gain, unity-gain frequency, phase margin, and output DC voltage levels, are measured to verify the impact of gate-oxide reliability on circuit performances of the common-source amplifiers with diode-connected active load. The small-signal parameters of the common-source amplifier with the non-stacked diode-connected active load structure are stronger degraded than that with non-stacked diode-connected active load structure due to gate-oxide breakdown under analog and digital applications. The common-source amplifiers with diode-connected active load are not functional operation under digital application due to gate-oxide breakdown. The impact of soft and hard gate-oxide breakdowns on common-source amplifiers with non-stacked and stacked diode-connected active load structures has been analyzed and discussed. The hard breakdown has more serious impact to the common-source amplifiers with diode-connected active load. The effect of the MOSFET gate-oxide reliability on operational amplifier is investigated with the two-stage and folded-cascode structures in a 130-nm low-voltage CMOS process. The test operation conditions include unity-gain buffer (close-loop) and comparator (open-loop) configurations under the

DC stress, AC stress with DC offset, and large-signal transition stress. After overstress, the small-signal parameters, such as small-signal gain, unity-gain frequency, and phase margin, are measured to verify the impact of gate-oxide reliability on circuit performances of the operational amplifier. The gate-oxide reliability in the operational amplifier can be improved by the stacked configuration under small-signal input and output application. A simple equivalent device model of gate-oxide reliability for CMOS devices in analog circuits is investigated and simulated.

In Chapter 4, the MOS switch with bootstrapped technique is widely used in low-voltage switched-capacitor circuit. The switched-capacitor circuit with the bootstrapped technique could be a dangerous design approach in the nano-scale CMOS process due to the gate-oxide transient overstress. The impact of gate-oxide transient overstress on MOS switch in switched-capacitor circuit is investigated with the sample-and-hold amplifier in a 130-nm CMOS process. After overstress on the MOS switch of SHA with open-loop configuration, the circuit performances in time domain and frequency domain are measured to verify the impact of gate-oxide reliability on circuit performances. The oxide breakdown on switch device will degrade the performance of bootstrapped switch technique.

In Chapter 5, the thin gate oxide causes the large gate tunneling leakage in nanoscale CMOS technology. In this work, the influence of MOS capacitor, as loop filter, with gate tunneling leakage on the circuit performances of phase locked loop (PLL) in nanoscale CMOS technology has been investigated and analyzed. The basic PLL with second-order loop filter is used to simulate the impact of gate tunneling leakage on performance degradation of PLL in a standard 90-nm CMOS process. The MOS capacitors with different oxide thicknesses are used to investigate this impact to PLL. The locked time, static phase error, and jitter of second-order PLL are degraded by the gate tunneling leakage of MOS capacitor in loop filter. Overview on the prior designs of gate tunneling leakage compensation technique to reduce the gate tunneling leakage on MOS capacitor as loop filter in PLL is provided in this work.

Chapter 6 presents a new proposed gate bias voltage generating technique with threshold-voltage compensation for analog circuits in the low-temperature polycrystalline silicon LTPS thin-film transistors (TFTs). The new proposed gate bias

voltage generating circuit with threshold-voltage compensation has been successfully verified in a 8-μm LTPS process. The experimental results have shown that the impact of TFT threshold-voltage variation on the biasing circuit can be reduced from 30% to 5% under biasing voltage of 3 V. The new proposed gate bias voltage generating technique with threshold-voltage compensation enables the analog circuits to be integrated and implemented by LTPS process on glass substrate for active matrix LCD (AMLCD) panel.

7.2. Future Works

In this dissertation, a new sub-1-V CMOS bandgap reference and curvature-compensation technique for CMOS bandgap reference circuit with sub-1-V operation, the impact of gate-oxide reliability on CMOS analog amplifier, the impact of gate tunneling current on performances of phase locked loop, and the new gate bias voltage generating technique with threshold-voltage compensation for on-glass analog circuits in LTPS process have been presented. However, the gate-oxide breakdown of MOSFET device modeled as resistance can be only used to investigate the impact of gate-oxide breakdown on circuit performances. In addition, the more accurate gate-oxide breakdown model of MOSFET devices is required in simulation or Engineering Design Automation (EDA) tool to improve the circuit reliability in advanced CMOS technology. Therefore, the more accurate gate-oxide breakdown model of MOSFET devices must be developed in the future.

Due to the trends of system on chip (SoC) and CMOS technology, the more analog circuits will be designed with low operation voltage in advanced CMOS processes and integrated in a single chip. Thus, not only the bandgap reference circuits but also other circuits, such as OPAMP (operational amplifier), ADC (analog-to-digital converter), and so on, must be designed with low operation voltage in advanced CMOS processes. Such design topic still continues to the future research.

Due to the SoP or SoG applications, more analog and digital circuits will be integrated on glass substrate. However, the threshold-voltage variation of TFT device

will degrade the circuit performance on glass substrate. In order to achieve the high performance and reliability smart plane application, such design topic still continues to the future research.

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Design and Reliability of Analog Circuits in Low-Voltage CMOS Processes

PUBLICATION LIST

(A) Regular Journal Papers

[1] M.-D. Ker, **Jung-Sheng Chen**, and C.-Y. Chu, "A CMOS bandgap reference circuit for sub-1-V operation without using extra low-threshold-voltage device", *IEICE Trans. on Electronics*, pp. 2150-2155, Nov. 2005.

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(B) Brief Journal Papers

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(C) International Conference Papers

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(E) Patents

[1] M.-D. Ker, **Jung-Sheng Chen**, and C.-Y. Hsu, "New gate bias voltage generating technique with threshold-voltage compensation for on-glass analog circuit design in LTPS process," U.S. and R.O.C. Patent pending.