國立交通大學

電子工程學系電子研究所

博士論文

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# Digitally-Calibrated Comparator and Its Application in Flash Analog-to-Digital Converters

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博士論文

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## 摘要

本論文發展一種數位式背景校正技術，用以削減比較器電路的輸入漂移電壓。這種校正技術不需中斷比較器的正常運作，因此特別適合運用在高速，低功率的場合。典型的應用例子是一個快閃型類比數位轉換器。

首先，我們建構出一個隨機切換式比較器。由輸出碼的統計性密度，可以偵測出該隨機切換比較器的漂移電壓極性。再依據漂移電壓的極性，設計一個校正迴路來逐步削減它，直到該比較器的輸入漂移電壓達到一個非常小的值為止。這個校正迴路的所有程序都利用數位電路進行，因此具有優越的可靠度與良率。

校正電路的效能優劣可以從漂移電壓的收斂速度，及其引發之跳動雜訊量的大小看出。對於前述的背景校正式比較器，這兩項效能指標由三個參數決定: 輸入訊號的機率密度，漂移電壓的調整間距，以及應用在校正迴路中，一個雙向峰值偵測器的限制準位。

當應用在快閃型類比數位轉換器時，輸入訊號區域化的技巧可以大幅降低背景校正式比較器的跳動雜訊。這種技巧只要應用快閃型轉換器既有的溫度碼邊緣偵測器，配合校正迴路即可構成。因為溫度碼邊緣偵測器的介入，所可能引發之向上鎖定，進而迫使漂移電壓發散的效應，則可藉由安排相鄰比較器的隨機切換功能在統計上相互獨立來避免。

依據前述的校正技術，我們利用 65 奈米的金屬氧化物半導體製程，實作出一個每秒轉換 20 億次，具有 6 位元解析度的快閃型類比數位轉換器。轉換器所使用的比較器，採用無直流偏壓的類比閂鎖電路，以 3 級串接的方式運作，並在第 1 級加入可微調漂移電壓的機制以配合校正迴路。在校正迴路的參數設定上，漂移電壓的調整間距為 1/4 LSB ，雙向峰值偵測器的限制準位為 16 。

實作出之轉換器有效面積 0.21x0.66 平方釐米，供應電壓 1.5V ，消耗功率 54mW 。在校正迴路啟動前， DNL 與 INL 分別是-1.0/+4.9 LSB 和-4.3/+5.4 LSB 。校正迴路啟動後， DNL 與 INL 分別降為-0.5/+0.6 LSB 和-0.4/+0.7 LSB 。對於一個 32MHz 的輸入訊號，背景校正技術使訊雜失真比從 20.4dB 提昇到 31.0dB 。在每秒轉換 20 億次的速度下，有效解析度頻寬可超過 Nyquist 頻率。該轉換器的效能指標為每階次消耗 0.93 微微焦耳。

# Digitally-Calibrated Comparator and Its Application in Flash Analog-to-Digital Converters

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## Abstract

This thesis presents a digital background calibration technique to trim the input-referred offsets of a comparator circuit. The calibration does not interrupt the normal operation of the comparator, hence is suitable for high speed and power efficient applications such as flash analog-to-digital converters(ADC).

For a random-chopping comparator, the polarity of its offset is detected by observing the code density of its comparison results. A calibration loop is then used to adjust the comparator offset so that the offset is minimized. All procedures in the calibration loop are performed in digital domain. This arrangement ensures excellent reliability and high yields.

The calibration performance is characterized by the converging speed of the calibration loop and the fluctuation noise imposed to the input signal. These two performance indexes of a background-calibrated comparator (BCC) are determined by three parameters:

the probabilistic distribution of input signal, the quantized step size of offset adjustment, and the threshold of an internal bilateral peak detector.

In flash ADCs, the offset fluctuation of a BCC can be drastically reduced by input windowing mechanism, which is accomplished by incorporating the thermometer-code edge detector(TCED) into the calibration loop. When introducing the TCED, uncorrelated random chopping for neighboring BCCs is used to avoid upward locking phenomenon which may lock calibration.

A 2Gsample/s 6-bit ADC with the developed calibration technique is fabricated using 65 nm CMOS technology. A circuit architecture with no DC bias and small transistor sizes is selected for comparators used in the ADC. The comparator includes modifications for variable offset mechanism and high common-mode rejection capability. The parameters for the calibration loop are 1/4 LSB for the quantized offset adjustment step, and 16 for the bilateral peak detector threshold.

The active area of the fabricated ADC is $0.21\times0.66mm^2$. Drawing from 1.5V supply voltage, the ADC consumes 54mW. Before activating the calibration, the DNL is -1.0/+4.9 LSB and the INL is -4.3/+5.4 LSB. After activating the offset calibration, the DNL becomes -0.5/+0.6 LSB and the INL is reduced to -0.4/+0.7 LSB. The calibration improves the SNDR from 20.4dB to 31.0dB with an input frequency of 32MHz. When operating at 2GS/s, the effective resolution of bandwidth extends over the Nyquist frequency. The figure-of-merit of the ADC is 0.93pJ/conversion-step.

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黃鈞正

國立交通大學

中華民國九十九年一月


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# Chapter 1

# Introduction

## 1.1 ADC Enhancement Techniques

Analog-to-digital converter(ADC) is the interface that converts the external physical quantity into a digital value. In modern SOC system such as WLAN, WIFI, HDTV, xDSL, etc; ADC plays an essential role to provide the base band signal streams for the digital signal processing(DSP) core.

As the CMOS technology progresses into nano-scale era, the challenges for ADC design become greater and greater. Due to the channel length shrinkage, the transition frequency of a transistor increases but its $r_{ds}$ is reduced. High transition frequency is beneficial for high speed comparator. While OPAMP with high gain and high linearity becomes more and more difficult to implement due to lower $r_{ds}$. The reduced supply voltage increases the design barrier further. Nevertheless, OPAMP is the key component for pipelined ADCs.

Another issues in nano-scale CMOS technology is the device mismatch. Mismatch becomes significant in tiny devices and limits the circuit speed and accuracy[1]. In comparator based data converter such as flash type ADCs, comparator offset caused from device mismatch corrupts the threshold level accuracy and hence limit the converter resolution.

To overcome these analog design limitation, many enhancement techniques have been developed. For OPAMP based converters such as the pipelined ADCs, correlation based

techniques[2][3][4] and dynamic matching algorithm [5][6] are used to calibrate the mismatch-caused nonlinearity. A comparator based mDAC[7] is used to eliminate the demand on the OPAMP. The off-chip calibration[8], the on-chip calibration using adaptive LMS algorithm[9][10] and the calibration with auxiliary conversion channel[11] are also developed to enhance the performance of the ADC.

For comparator-based converter such as the flash ADCs, various methods are proposed to mitigate the effect of comparator offset voltage. These techniques include spatial averaging[12][13][14][15], offset storage[16][17], calibrated redundancy[18][19] and fault-tolerant encoding[20], and so on. On the other hand, digitally calibrated comparator in which the offset is removed by auxiliary digital circuits[21][22][23] has better reliability and stability but has not been implemented on-line.

In this thesis, we introduce an effective on-line offset calibration technique for the comparator. The calibration is suitable for over-GHz flash ADC and can trim the comparator offset in the background.

### 1.1.1 Flash ADC Design Challenges

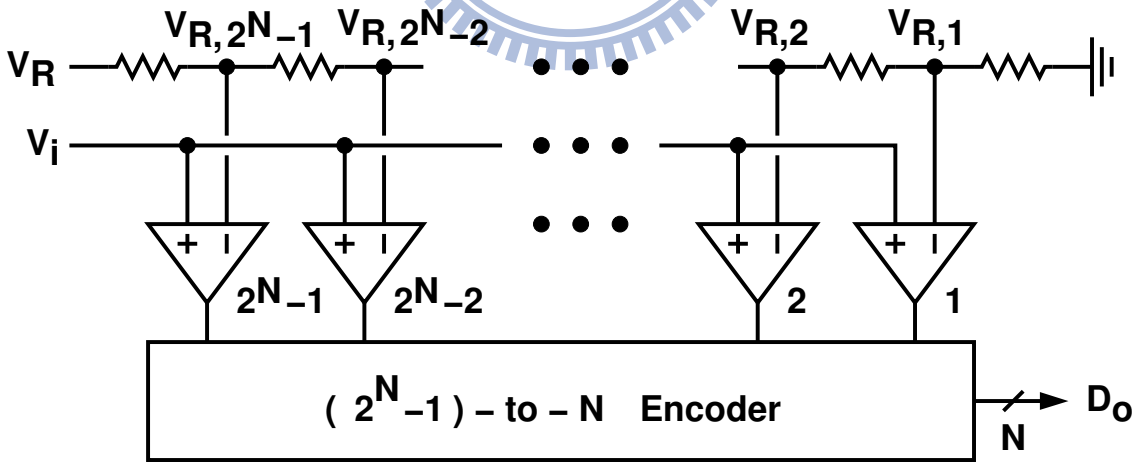



Figure 1.1: A typical flash ADC architecture

Fig. 1.1 shows an $N$-bit flash analog-to-digital converter (ADC) that uses $2^N - 1$ comparators to simultaneously compare input, $V_i$, with $2^N - 1$ references, $V_{R,j}$, where $j = 1, 2, \cdots 2^N - 1$. Outputs of this comparator array appear as a thermometer code.

The output bits have the values of '1' with threshold levels below the input signal, and the values of '0' with threshold level beyond the input signal. The digital output $D_o$ is obtained by encoding this thermometer codes.

For a high-speed CMOS flash ADC, the linearity of its transfer function is predominantly degraded by two characteristics of the comparators: 1. the metastability; 2. the the input offset voltage [24].

Metastability is the incompletely-defined comparator output as input signal falls close to the threshold level. The error probability on output codes, which is equivalent to the ratio of input ranges corresponding to incompletely-defined outputs and well-defined outputs, describe the metastability of a comparator. As comparators suffer metastability, the final value of its output strongly depends on the threshold level of the following digital gates. In addition, it is very sensitive to noise. Faster comparators have less metastable region, but consumes more power.

Input offset voltage is the the input voltage that produces an output value at middle trip-point for a comparator. A systematic input offset voltage is analytical in circuit design phase and can be suppressed using symmetric circuit configuration. While the device mismatch aroused in semiconductor process causes a random input offset voltage that is not predictable. This random offset degrades the comparator resolution and can only be reduced by enlarging device sizes.

Both metastability and input offset voltage produce 'Bubbles' in the thermometer code. Bubbles are the cavities of '0' in a series of '1', or '1' in a series of '0'. Various designs of encoders have been proposed to suppress the effect of the bubbles[25] [26][27]. These techniques are effective but the improvements are limited. Since the bubbles are originated from the imperfection of the comparators, the ADC performance is dominated by the comparators.

Fig. 1.2 is a commonly-used comparator architecture. Theoretically, a latch circuit in the right part of this figure is sufficient to be an comparator. Yet the large input offset voltage of the latch circuit is not tolerant in practical applications. This is why the preamplifier shown in the left part is necessary. The voltage gain of the preamplifier reduces the input-referred offset voltage of the latch.

For the preamplifier, the input offset voltage is related to the device mismatch of the

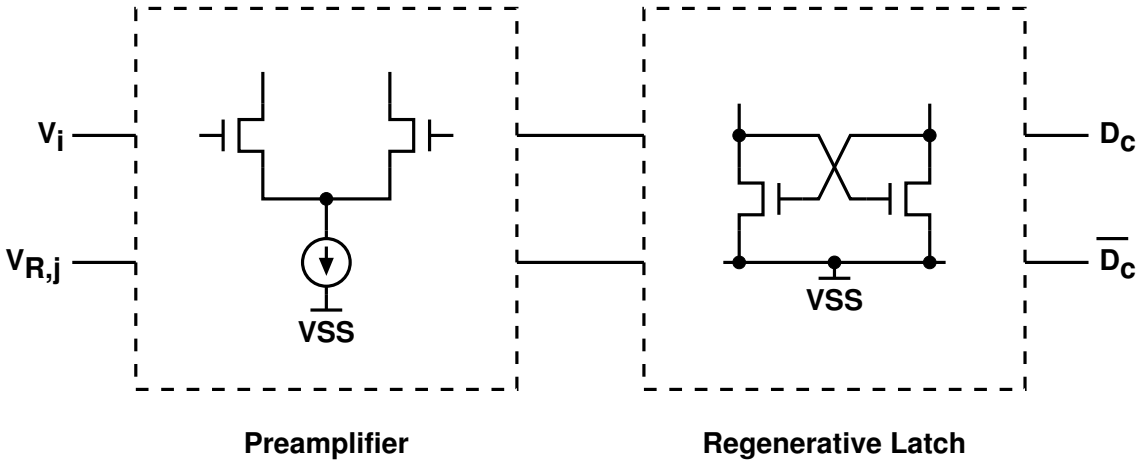



Figure 1.2: The commonly-used comparator architecture

input pair:

$$\sigma(\Delta V_t) = \frac{A_{V_t}}{\sqrt{W L}} \tag{1.1}$$

Circuits with larger device size have better matching properties but less power efficiency. Due to the design consideration on device matching, there exists a fundamental trade-off among the speed, power, and accuracy for a CMOS flash ADC [28]:

$$\frac{\text{Speed} \times \text{Accuracy}^2}{\text{Power}} \approx \frac{1}{C_{ox} \cdot A_{V_t}^2} \tag{1.2}$$

Equation (1.2) figures out a physical limitation in comparator design. As an example, doubled speed and doubled resolution cost a power consumption of eight times. It is hard to exceed or even approach the limit of (1.2) merely by device size optimization.

Several innovative techniques have been proposed to overcome this inherent constraint on devices. Among them, input-offset storage technique and averaging technique are two of the most popular ones. Subsection 1.1.2 and 1.1.3 describe the details of them.

### 1.1.2 Input Offset Storage Technique

The principle of input offset storage(IOS) technique is to sample and store the input offset in the reset phase and then cancel it in the comparison phase[17][29]. As shown in Fig. 1.3, The input signal and the input offset voltage are together sampled to the serial

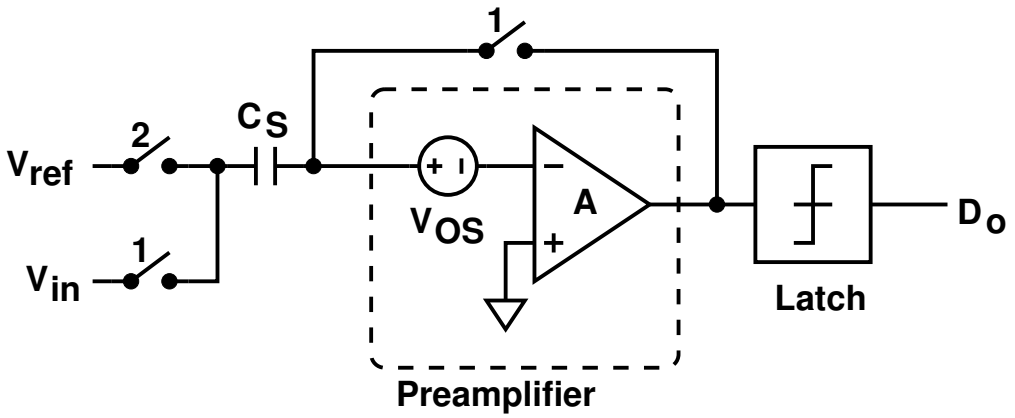



Figure 1.3: Input offset storage(IOS) technique: (a) Comparator with IOS; (b) Offset storage phase($\phi_1$); (c) Comparison phase($\phi_2$).

connected capacitor $C_S$, and then compared with the offseted threshold level. The input offset voltage is thus eliminated in the comparison.

The operation is decomposed into 2 phases: sampling phase in Fig. 1.4a and comparison phase in Fig. 1.4b. In sampling phase, assuming the preamplifier has an infinite voltage gain, its output node is pulled to $V_{OS}$ due to the virtual grounding, thus $C_S$ is charged to $V_{in} - V_{OS}$.

In comparison phase, the feedback loop is broken and $C_S$ is connected to the reference voltage. Since $C_S$ has been charged in the sampling phase, the input node of the preamplifier is pulled to:

$$V_{ref} - (V_{in} - V_{OS}) - V_{OS} = V_{ref} - V_{in} \tag{1.3}$$

This leads to a zero-offset preamplification for the comparator.

Another alternative operation mode for IOS is that the reference level, instead of the input signal, is sampled in reset phase[30]. Then, in the comparison phase, input signal is connected to the comparator input port. Hence the input offset voltage is also stored and eliminated. This operation mode is suitable for higher speed comparison since reference level is a fixed value and the settling time for capacitive charging in sampling phase is shorten. Compared with the input-sampled mode, the reference-sampled mode is lack of the sample-and-hold feature over the input signal. In multiple comparator scenario such as flash ADC application, clock jitter will cause more bubbles in the output code with the

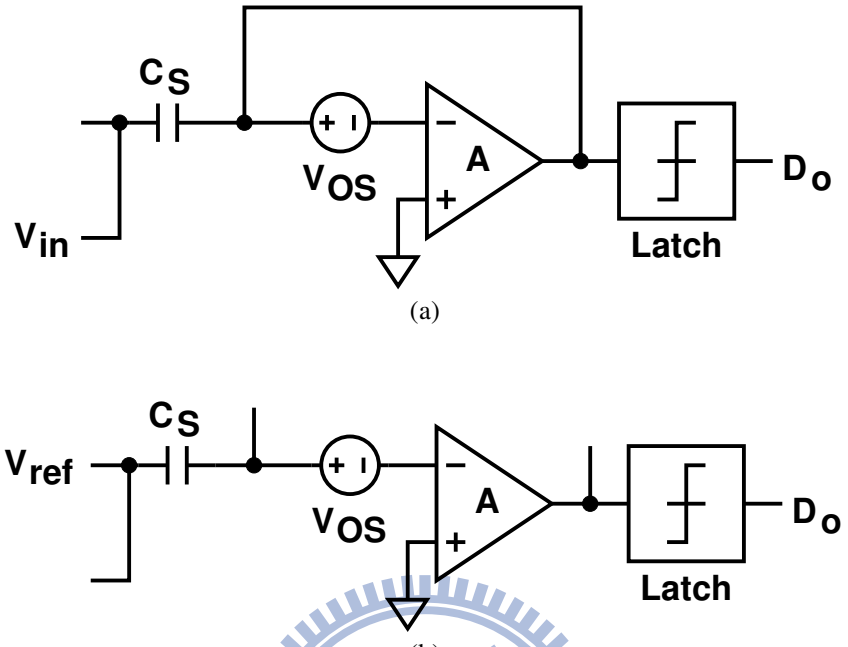



Figure 1.4: Operation phases for IOS:(a) Offset storage phase($\phi_1$); (b) comparison phase($\phi_2$).

reference-sampled mode.

The limitation of IOS technique is the finite gain of the preamplifier. For the preamplifier with infinite gain, feedback guarantees a perfect virtual grounding in input nodes. This is essential to charge $C_S$ correctly. However, due to high speed consideration, typical value for the preamplifier gain is about 5 ~10, resulting in a deviation on offset storage in sampling phase.

Besides, the parasitic capacitance in the comparator input nodes shares the charge of $C_S$ in comparison phase. The charge sharing is equivalent to a voltage divider that degrades the precision of offset cancellation. Large $C_S$ is needed to reduce the effect of charge sharing.

IOS requires extra phase to sample the input offset voltage, thus the clocking is more complex than a simple comparator. The operation speed may also be limited.

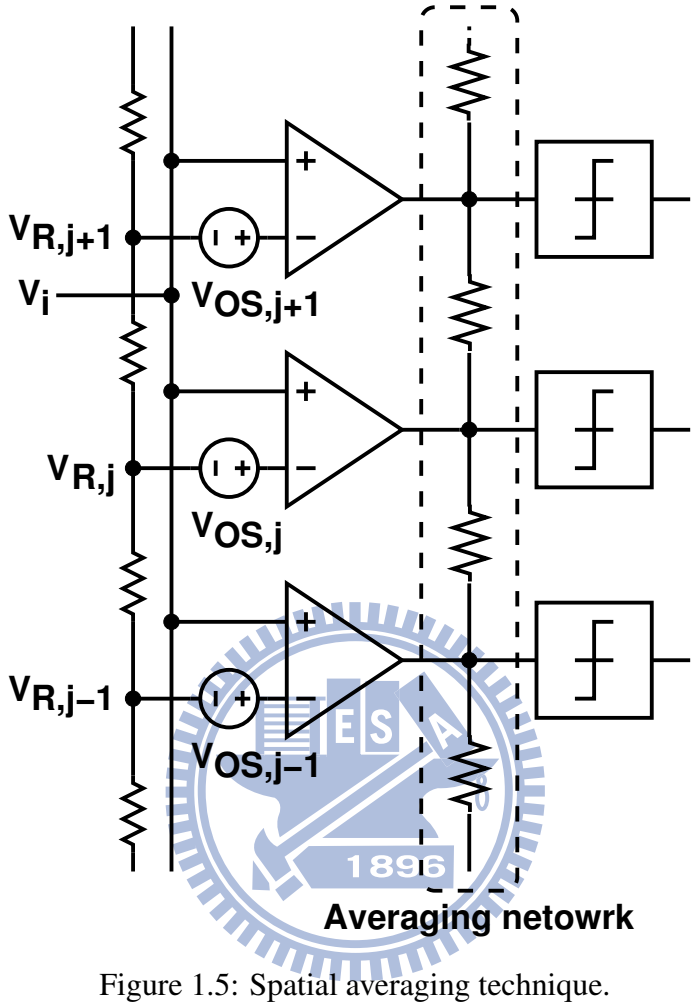



Figure 1.5: Spatial averaging technique.

### 1.1.3 Spatial Averaging Technique

Spatial averaging technique utilizes an averaging network to lower the offset variance of the comparator array[31]. A simplified averaging network is shown in Fig. 1.1.3.

In Fig. 1.1.3, signal on the $j^{th}$ preamplifier output node is composed of not only the part from $j^{th}$ preamplifier, but also parts from $(j\pm1)^{th}$, $(j\pm2)^{th}$... etc., through the resistive summation of the averaging network. Hence, the signal on this output node is effected by the input offset voltage of $j^{th}$, $(j\pm1)^{th}$, $(j\pm2)^{th}$...etc. in total.

The comparator input offset voltage is originated from the random factors on semiconductor process, thus is a random variable itself. The random offset voltage is shown in Fig. 1.6a.

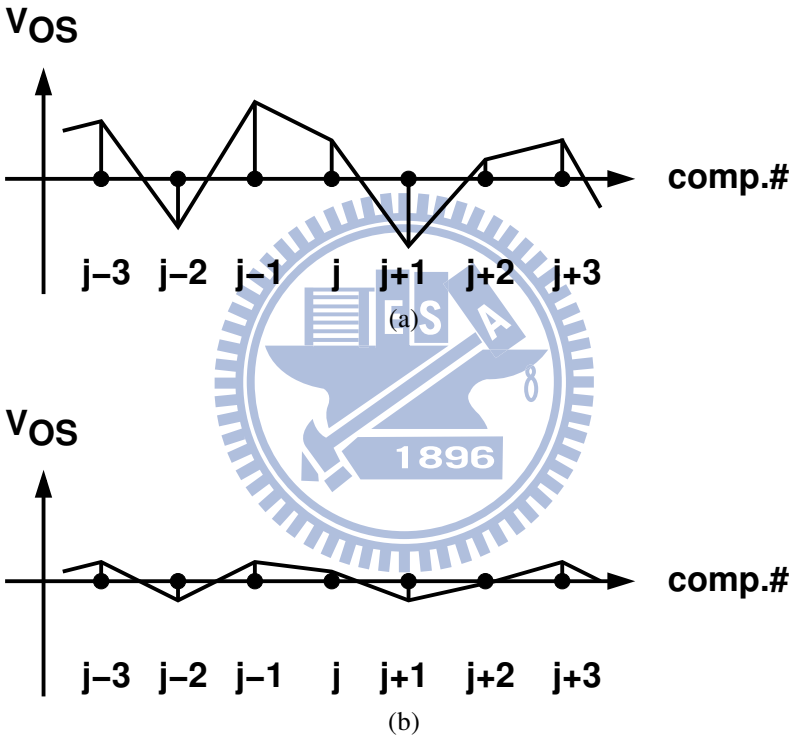
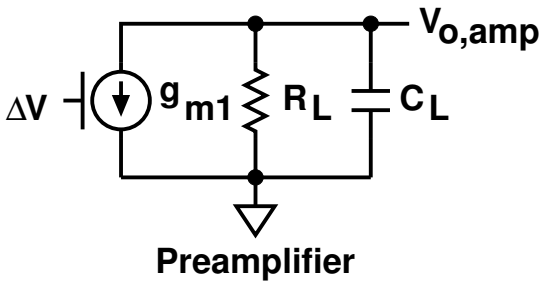
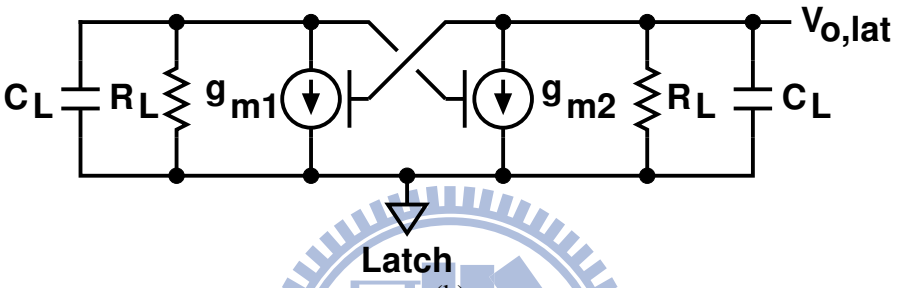



Figure 1.6: Random offset voltages on comparators: (a) without averaging; (b) with averaging.




(a)




(b)

Figure 1.7: Small-signal equivalent circuit: (a) preamplifier; (b) latch

The offset summation is equivalent to performing moving average over the comparator array. The moving average produces a spatial low-pass filtering to the 'peaks' of the random offsets. The output node of each preamplifier thus suffers a smaller equivalent offset voltage, which is shown in Fig. 1.6b.

The limitation of the spatial averaging technique is that it need redundant comparators in both ends of the comparator array[32], since the comparators located near the ends do not have enough neighbors to provide the random offsets for averaging Specialized termination[33] and cyclic connection[14] have been applied to the averaging network to mintage the this overhead, but they still require extra power and area.

### 1.1.4 Background Offset Trimming

The input offset storage and the spatial averaging techniques both require preamplifiers to apply. To verify the cost of the preamplification, small-signal equivalent circuits for a preamplifier and a latch are shown in Fig. 1.7.

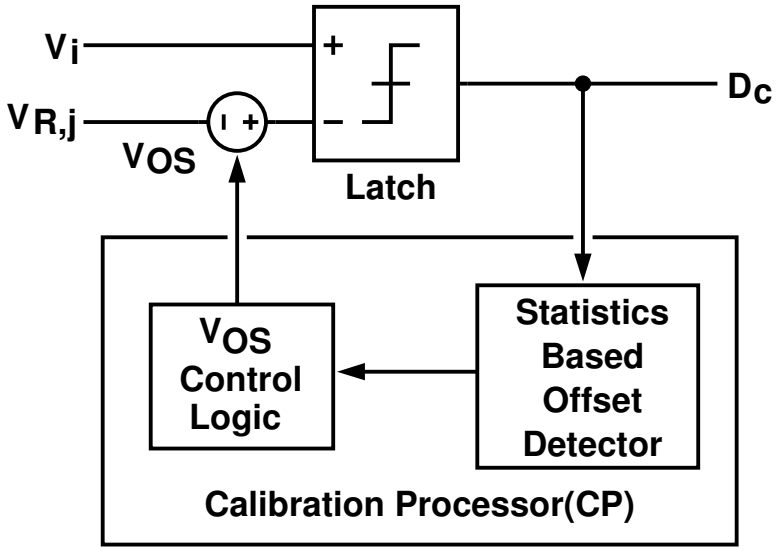



Figure 1.8: Background offset calibration for a comparator

And the transient voltage gains for them are:

$$A_{v,amp} = g_{m1}R_L\left[1-\exp\left(\frac{-t}{R_LC_L}\right)\right], \quad A_{v,lat} = g_{m2}R_L\exp\left(\frac{t}{C_L/g_{m2}}\right) \tag{1.4}$$

As an example, assuming $R_L = 1K\Omega$, $C_L$=1pF, and the settling period is 0.5ns, to obtain a voltage gain of 10 requires $g_{m1}$=25.4 mA/V for the preamplifier and $g_{m2}$=2.65 mA/V for the latch. The preamplifier transconductance is about 9.6 times of the latch transconductance. However, the latch has large offset voltage and kickback noise so that the preamplification is necessary.

In this thesis, we propose a background calibration technique shown in Fig. 1.8 to trim the offset voltage continuously. This background calibration technique adjust the offset voltage according to the code statistics of the latch outputs without interrupting the its operation. As the offset voltage of the latch can be trimmed to zero, and hence the device size is shrunk down, the preamplifier which is used to suppress the offset voltage and to block kickback noise is not necessary. Elimination of the preamplifier will greatly reduce the power consumption of the comparator.

The proposed calibration loop operates in the digital domain and only minor modification is required on the analog path, hence the circuit speed will not degrade. The calibration can be applied concurrently to all latches in the flash ADC to improve its linearity.

Foreground offset trimming techniques have been proposed in [34][35][36][22]. it is executed only once in the beginning or repeatedly in some specific clock periods to detect the offsets and adjust the circuit configuration accordingly. In cases that temperature and supply voltage variate during the ADC operation, trimmed offset voltage may deviate from the zero. On the contrary, background offset calibration is capable to trace back the offset shifts and thus provides better conversion performance.

## 1.2 Analog Latch Circuits

There are various types of analog latch circuits. Fig. 1.9 lists some of them. A simplest regenerative latch is composed of two cross-connected inverters shown in (a). A practical analog latch circuit requires the input coupling path and the clocked mechanism. In (b), (c), (d), (h) and (i), the input signal is parallel coupled. In other circuits, the input is series coupled. Parallel couping of the input signal does not limit the regenerative current, thus is faster then serial coupling. However, serial coupled input device will be turned off as the regenerative operation finished, thus the power consumption is less.

In reset phase, the output nodes of the latch in (h), (i), (j) are equalized, while the output nodes of other latches are pulled high. Equalized output nodes will be separated faster in the regeneration phase, but they consume static power in the reset phase.

The input offset voltage depends on whether the input devices are saturated or not in the regeneration phase. (b), (c), (g), (h), (i), and (k) have smaller input offset voltage than others since the saturated devices contribute more transient gain to pull the positive feedback loop.

Kickback noise is decided by the coupling path between output and input nodes. For (e), (f), and (j), they have smaller kickback noise in nature. Although the output nodes of (h) and (i) do not directly couple back to the input nodes, the clock signal transition may also produce kickback noise.

The input devices in (e) act as a voltage controlled resistor, thus is possible combined with preamplifier interpolation[37]. The circuit is very power efficient since no DC power is consumed. The disadvantage of this circuit is the weak controllability of the input signal over this device, thus its input offset voltage is quite large. Noise can also have

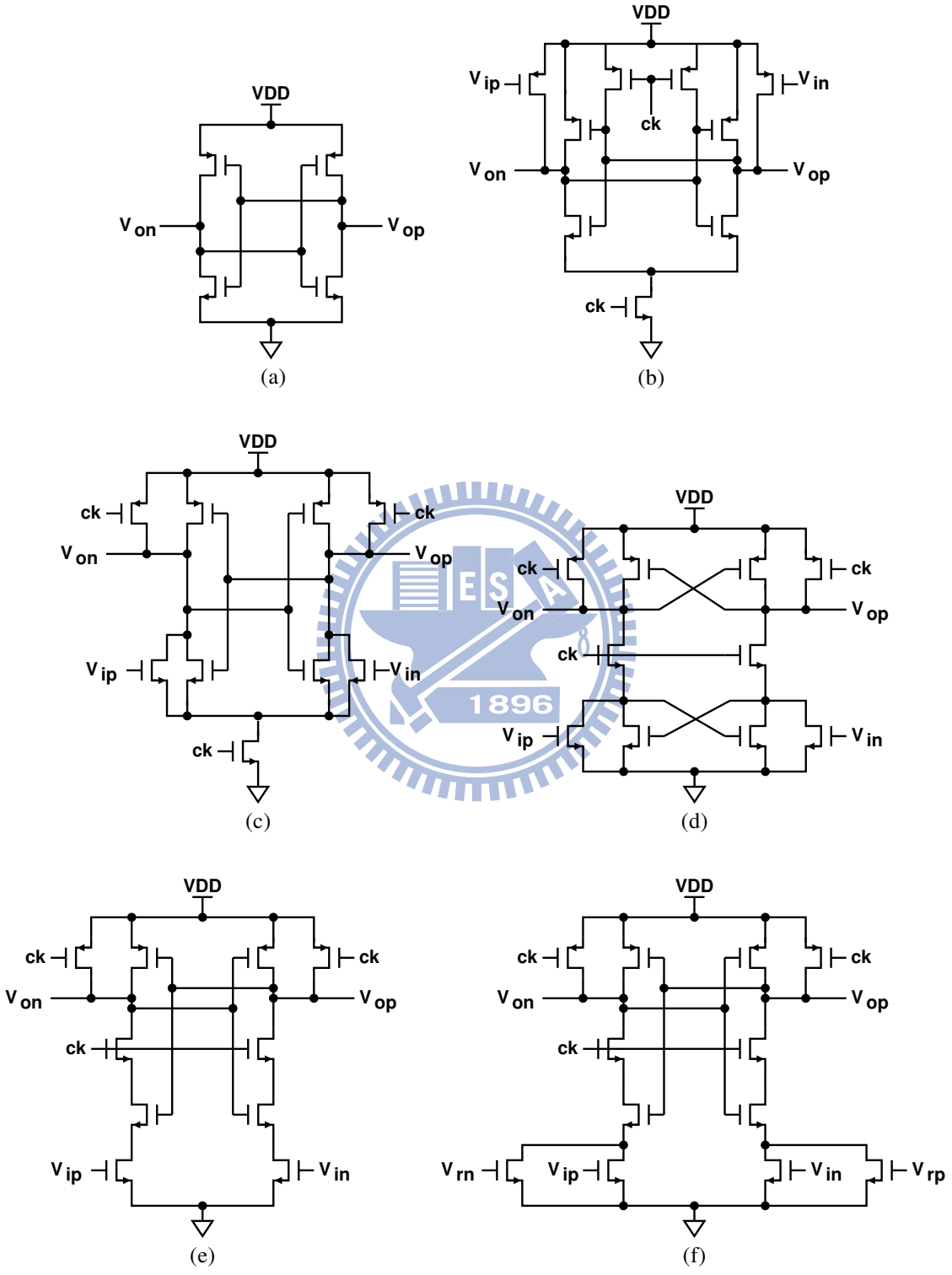



Figure 1.9: Analog latch circuits

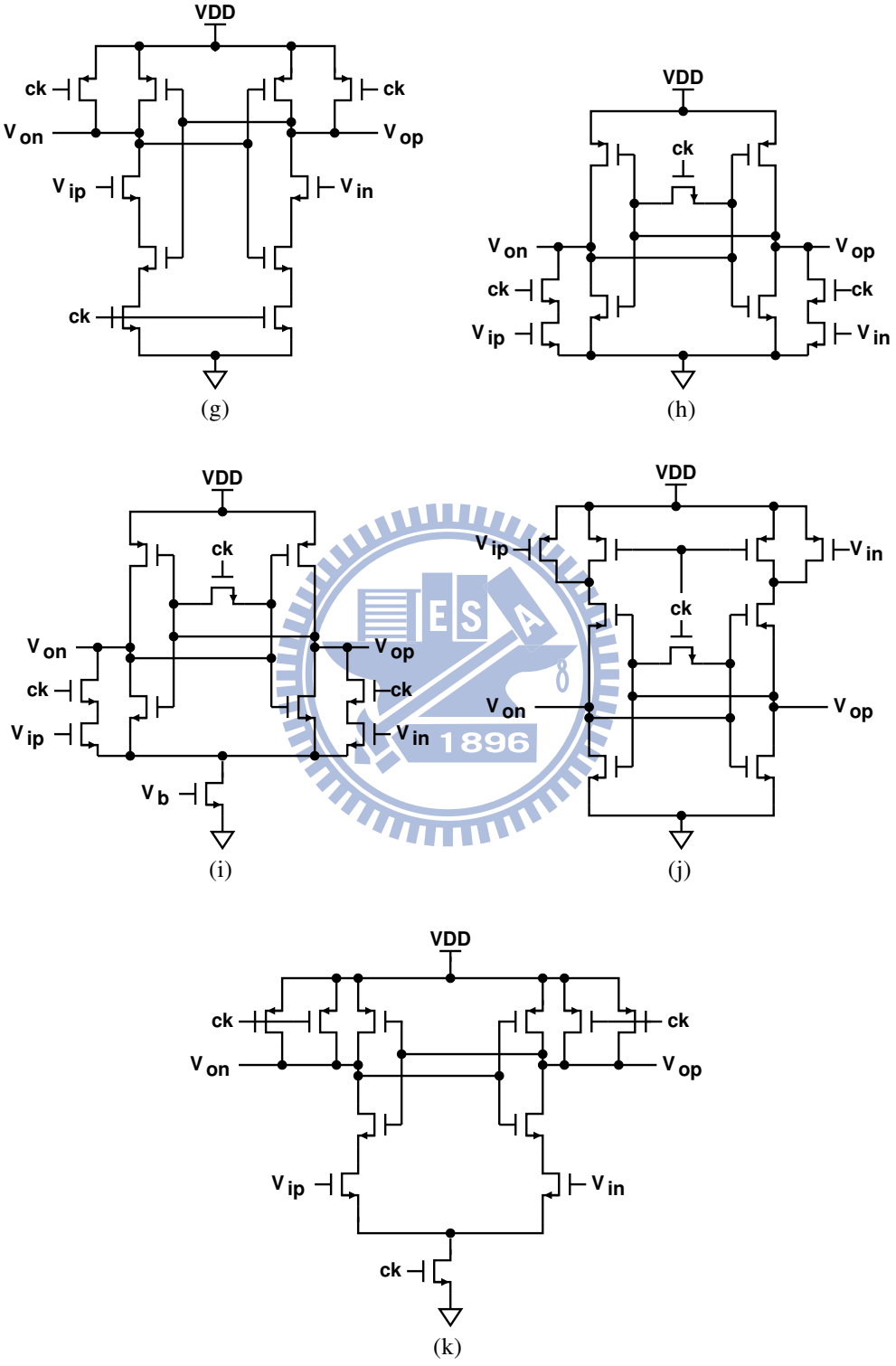



Figure 1.9: Analog latch circuits

strong effect on the comparison results. (f) is similar to (e) except that it operates with differential input. (j) is nearly the same thing but with input signal couple by a P-type MOSFET.

(i) is modified from (h). The added tail transistor may increase both its regeneration speed and the common-mode rejection ability.[13].

Although (c) and (k) have similar structure, the serial coupled input device in the latter will be cut off as the comparison is completed, thus is more power efficient that the former. (k) is usually used as sense amplify for the RAM cell. When applied in ADC circuit, its low power consuming, small input offset and hight comparison speed are very beneficial[38].

## 1.3 Thesis Organization

This thesis is organized as follows. Chap.2 describes the design and analysis of a background-calibrated comparator(BCC). Chap.3 gives the system-level analysis for a flash ADC using the BCCs. Chap.4 illustrates an implementation of a ADC circuit using the proposed background calibration technique. Chap.5 draws conclusions and gives the recommendations for future works. Finally, the Appendix includes a mathematical analysis for the offset fluctuation behavior of the proposed BCC.

# Chapter 2

# Digital Calibration for the Comparators

## 2.1 Random-Chopping Comparator

The proposed comparator calibration scheme is based on a random-chopping comparator(RCC) which is shown in Fig. 2.1.

The RCC is used to replace each comparator in Fig. 1.1. For the $j^{th}$ RCC, input signal $V_i$ is compared with the $j^{th}$ reference voltage $V_{R,j}$, and then generates a corresponding binary output $D_c \in \{1, 0\}$. Due to the clocked operation, $D_c$ can be represented as $D_c[k]$ with the index $k$ indicating the sampling count, or simply the time index. The comparator inside the RCC has an input offset voltage $V_{OS}$. The two choppers, CHP1 and CHP2, are controlled by a binary-state random sequence $q[k] \in \{+1, -1\}$. The probability for $q[k] = +1$ and $q[k] = -1$ is equally 0.5.

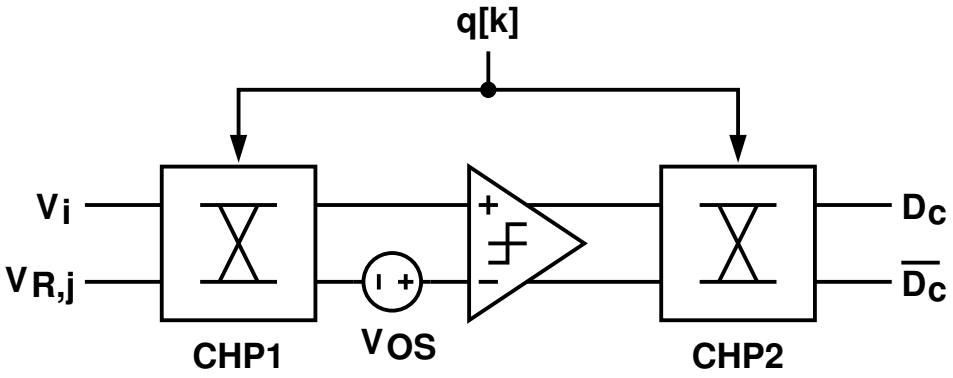



Figure 2.1: The random-chopping comparator(RCC).

CHP1 passes the inputs unchanged when $q = +1$ and interchanges the inputs when $q = -1$. Similarly in the digital domain, CHP2 passes the outputs unchanged when $q = +1$ and invert the outputs when $q = -1$. In CMOS technology, CHP1 can be realized using 4 analog switches. CHP2 is composed of digital gates. The behavior of RCC can be described by:

$$D_c = \frac{1}{2}\Big[1 + q \times \mathrm{SGN}\Big(q(V_i - V_{R,j}) - V_{OS}\Big)\Big] \tag{2.1}$$

Where SGN is the sign function that return +1 if its independent variable is larger than 0 and -1 if its independent variable is smaller than 0. Since $q$ is possibly only +1 or -1, it can be moved to the independent domain of the SGN function. The square of $q$ is 1, thus (2.1) becomes:

$$D_c = \frac{1}{2}\Big[1 + \mathrm{SGN}\Big(V_i - V_{R,j} - qV_{OS}\Big)\Big] \tag{2.2}$$

Equation (2.2) indicates that changing the CHP1/CHP2 states is equivalent to invert the polarity of the input offset voltage on the internal comparator. The SNG function can be represented as adding a quantization error to the normalized independent variable, thus (2.2) can be represented as:

$$D_c = \frac{1}{2}\Big[1 + \frac{2}{A_0}(V_i - V_{R,j} - qV_{OS}) + e\Big] \tag{2.3}$$

Where $A_0$ is the maximum amplitude of $(V_i - V_{R,j})$. The factor of 2 above the denominator $A_0$ implies the swing of $(V_i - V_{R,j})$ is normalized to $\pm 2$. In this case, the quantization error $e$ is assumed to be a zero-mean value and is independent of $q$. If the random sequence $q[k]$ is selected to be uncorrelated with $V_i$ with a zero mean, the averaged value of $(-q \times D_c)$ is described by (2.4):

$$\overline{-q \times D_c} = -\frac{\overline{q}}{2} - \overline{\frac{q}{A_0}(V_i - V_{R,j})} + \frac{\overline{V_{OS}}}{A_0} - \frac{\overline{q \times e}}{2} = \frac{V_{OS}}{A_0} \tag{2.4}$$

Hence it is possible to obtain the value of $V_{OS}$ from the averaging of $(-q \times D_c)$. This is based on the fact that there is no correlation between $q$ and $(V_i - V_{R,j} + e)$. However, the averaging calculation requires data collection over a long period of time and a floating point arithmetic unit. The hardware overhead is too large for a single comparator.

The correlation-based $V_{OS}$ detection can also be understood from the probability density function(PDF) of $V_i - V_{R,j}$ shown in Fig. 2.2. When $q = +1$, the probability for

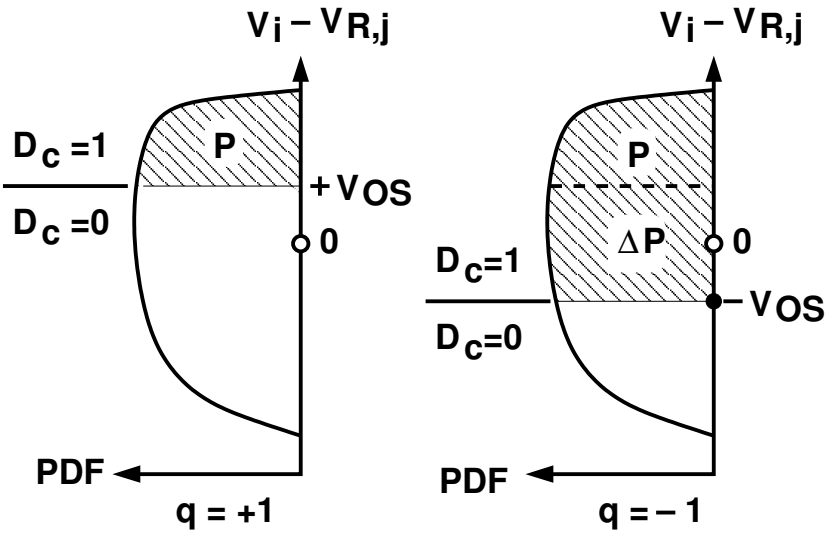



Figure 2.2: Probability of $D_c$=1 for $q = +1$ and $q = -1$.

$D_c = +1$ is $P$. When $q = -1$, the probability for $D_c = +1$ is $(P + \Delta P)$. If the random sequence $q[k]$ is selected to be uncorrelated with $V_i$, the comparator can perceive identical PDF of $(V_i - V_{R,j})$ regardless of $q[k]$. In this case, the averaged value of $(-q \times D_c)$ is proportional to $\Delta P$. Since $\Delta P$ is also proportional to $V_{OS}$, it is possible to trim $V_{OS}$ according to $(-q \times D_c)$. For hardware implementation, to accumulate $(-q \times D_c)$ is much easier that to calculate its averaged value. In mathematical meaning, to trim $V_{OS}$ based on the accumulation within a fixed interval is equivalent to do that based on the averaging. Fig. 2.3 is a calibration example that utilizes the offset detection[39][40].

The calibration loop cuts down the input offset voltage by a fraction of accumulated $(-q \times D_c)$ at each sample. It is equivalent to a linear negative feedback loop. This configuration requires that the proportion parameter $\mu$ be small enough to prevent oscillation and large enough to perform a good tracking behavior.

The main disadvantage for the loop in Fig. 2.3 is that a time-varying input signal distribution will cause a calibration fault. As shown in Fig. 2.4, when the distribution of the input signal changes, $\Delta P$ also changes. In this case, the calibration loop thinks of the changes on $\Delta P$ as the changes on offset and thus misadjust it. For a general-purpose ADC, the signal may have any type of distribution, so this linear feedback calibration scheme is not reliable for general use.

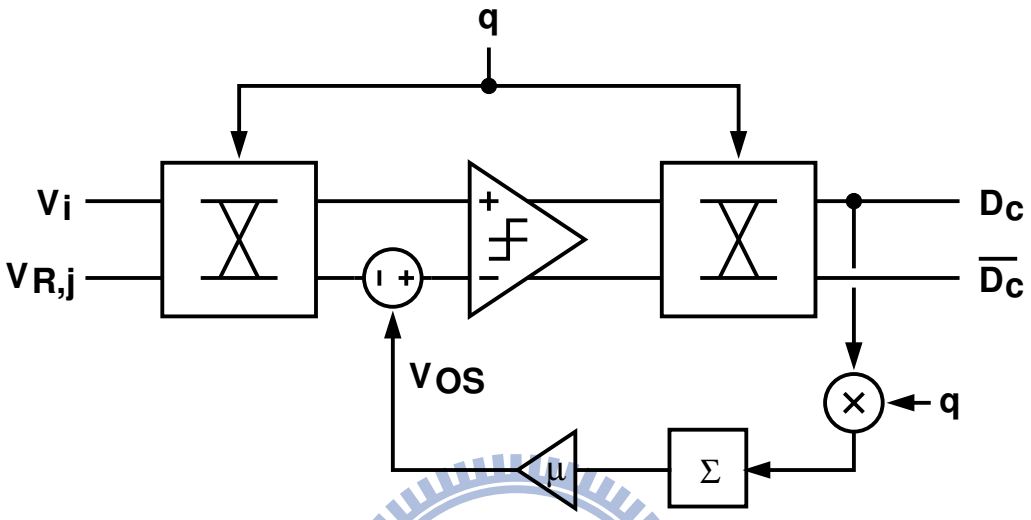



Figure 2.3: Calibration based on $\sum(-q \times D_c)$

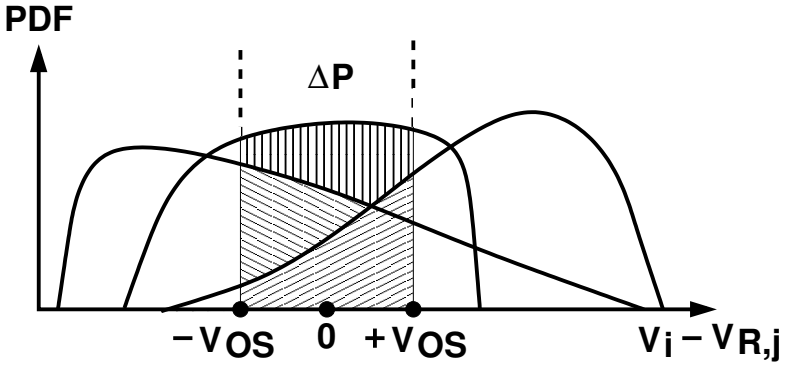



Figure 2.4: Input signal with time-variant PDF

On the contrary, the polarity of accumulated $(-q \times D_c)$ is unchanged even if the input signal variates. Thus it is more reliable to detect the offset polarity according to $(-q \times D_c)$ accumulation. Offset polarity implies the offset direction instead of the offset magnitude. Based on offset polarity detection, the calibration processor is designed to perform a fixed-step adjustment when trimming the offset voltage. A detailed explanation is given in section 2.2.

## 2.2 Calibration Processor Based on Offset Polarity

The calibration processor based on offset polarity detection is shown in Fig. 2.2.

An accumulation-and-reset(AAR) block is used for the detection. In the AAR shown in Fig. 2.2, the accumulated $(q \times D_c)$, which is represented as $R$, is fed to a bilateral peak detector(BPD). BPD has two internal threshold levels $\pm N_C$. As $R > +N_C$, the output of BPD, $S$, will be 1. As $R < -N_C$, $S$ will be -1. In both cases the accumulator itself is also reset and the $(q \times D_c)$ accumulation restarts. Other than the two cases, $S$ keeps in 0.

Another accumulator is used to accumulate $S$. Its output $T$ is used to control the offset voltage.

The behavior of the calibration processor can be understood by Fig. 2.6. The variation of $V_{OS}$ and $R$ is plotted versus the time index. Suppose that the comparator input offset voltage $V_{OS}$ is positive in the beginning, $R$ tends to lean down and cross the lower boundary $-N_C$ of the BPD soon. At this time, the offset voltage is cut down by a fixed step and $R$ is reset immediately, then another accumulation starts.

The crossing and offset trimming repeat again and again until $V_{OS}$ is reduced to a value close to 0. In such a small offset, the leaning of $R$ becomes very indistinctive and the offset trimming rarely happens.

AAR is used to suppress the effect of input signal and extract the polarity information of input offset voltage from the comparator output. Its function resembles a discrete-time integrator in the digital domain [41] [42]. However, for outputs of a 1-bit quantizer such as the comparator, the offset information is accompanied with heavy quantization noise. A linear integrator may not effectively extract the offset information.

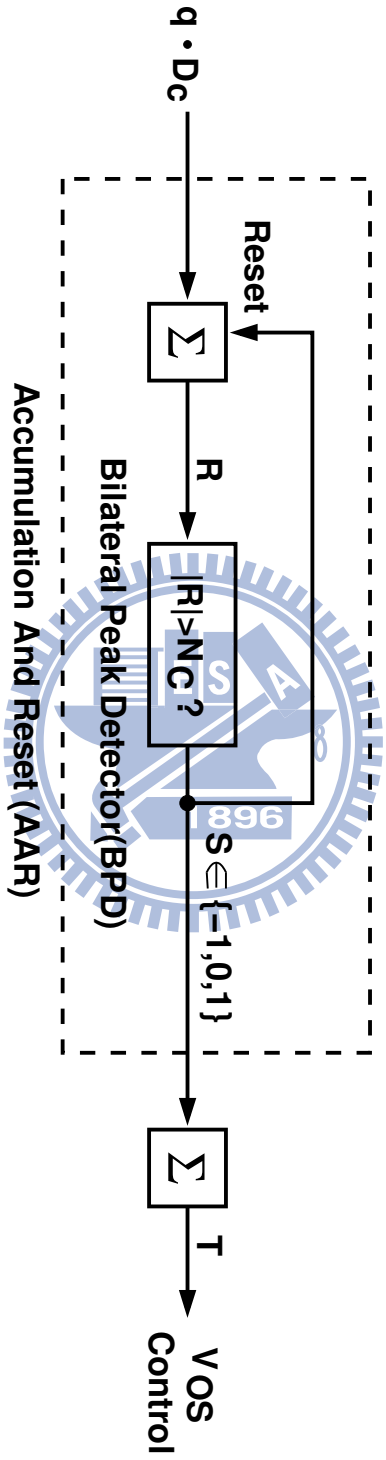



Figure 2.5: Calibration based on accumulation and reset(AAR)

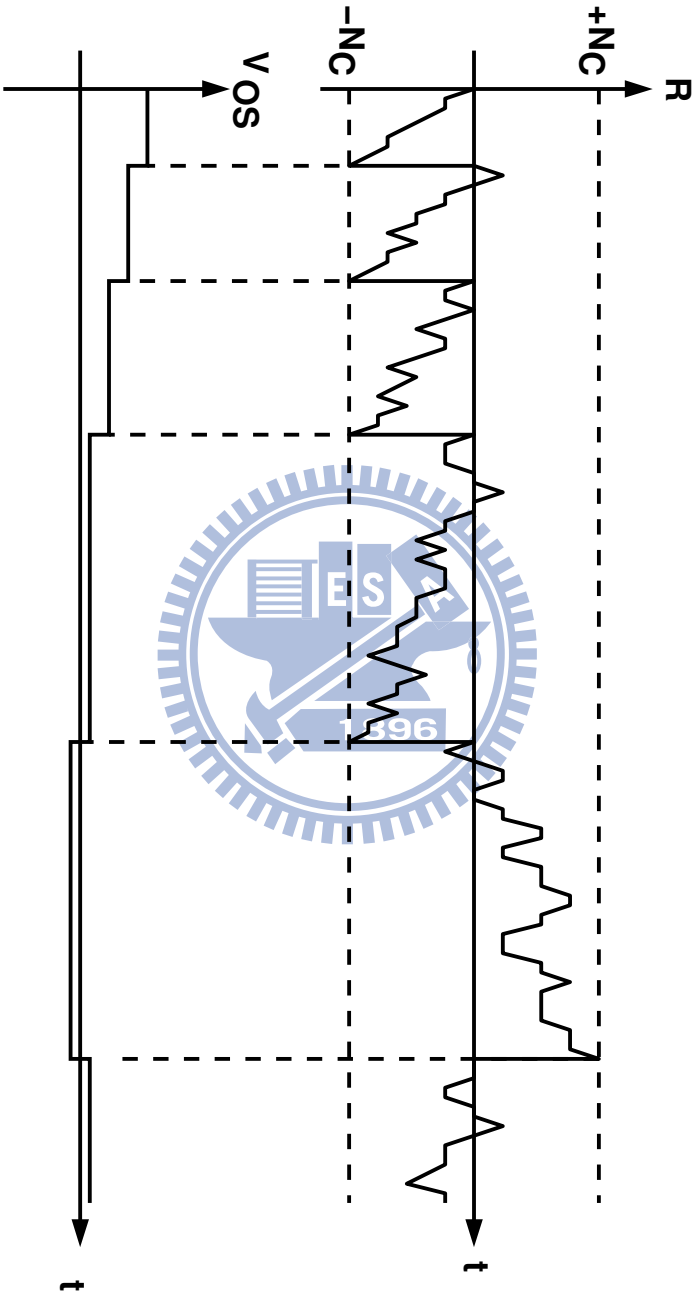



Figure 2.6: $R$ and $V_{OS}$ variations versus time.

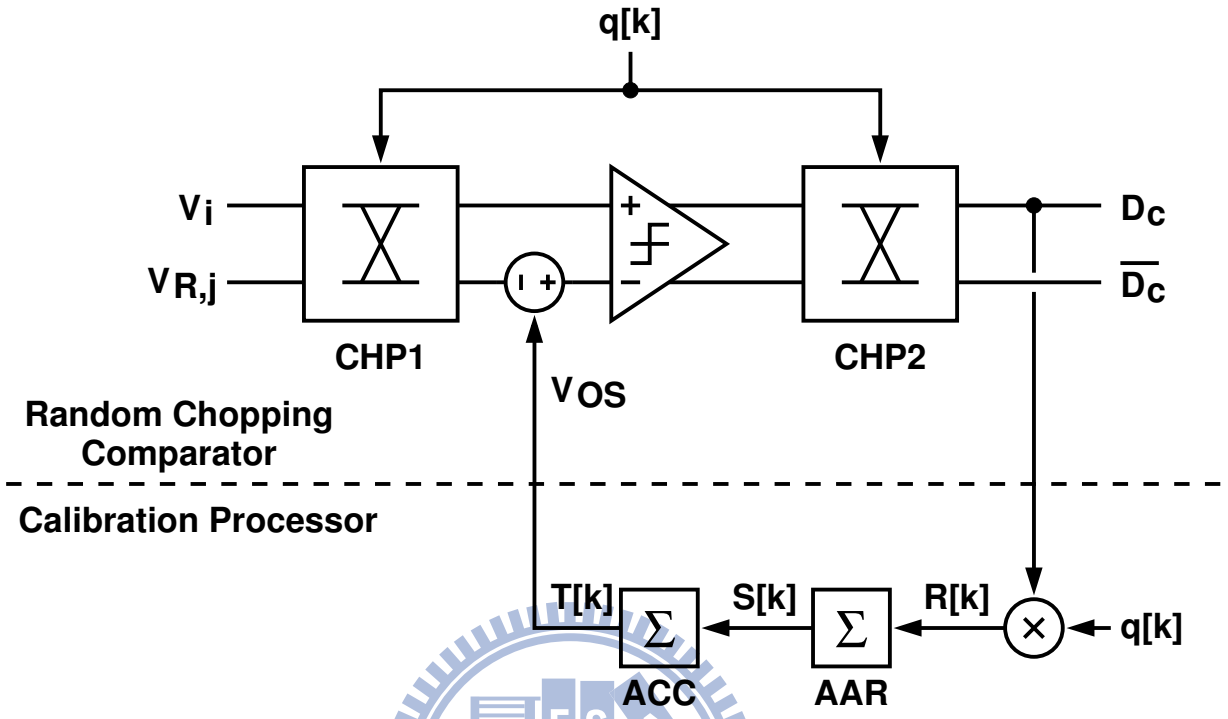



Figure 2.7: A background-calibrated comparator

## 2.3 Background-Calibrated Comparator

The background calibrated comparator(BCC) is composed of a random-chopping comparator and a calibration processor. Fig. 2.7 illustrates its block diagram.

The proposed calibration scheme for BCC is suitable for general purpose application. No extra signals nor the exact information of $V_i$ is needed. The effectiveness of the calibration only depends on the probability difference $\Delta P$ of Fig. 2.2.

The offset of the internal comparator in BCC is adjusted by reconfiguring those low-speed sections, which are separated from the high-speed signal path [34] [36] [35]. Thus the added $V_{OS}$ controllability for the calibration costs relatively low speed and power penalty.

An alternative calibration scheme based on the offset polarity detection is to trim the offset voltage periodically[39]. Compared to the periodically-adjusted scheme, the proposed scheme has faster converging speed and lower offset fluctuation. Based on the AAR algorithm, the the offset trimming gets activated quite often and hence the offset converges very fast with large $V_{OS}$ in the beginning. When $V_{OS}$ has been trimmed close to 0, the $\Delta P$

also becomes small, then the trimming rarely get activated and $V_{OS}$ is more stationary.

The time-varying offset voltage can be expressed as:

$$V_{OS}[k] = V_0 + \Delta V \times T[k] \tag{2.5}$$

where $V_0$ is the inherent comparator offset at $T[k] = 0$, and $\Delta V$ is the step size of the offset control. $\Delta V$, together with the BPD threshold level $N_C$, are two important parameters in BCC. Both parameters affect the converging speed and the offset fluctuation. Large $\Delta V$ and small $N_C$ result in fast converging speed but large offset fluctuation. On the other hand, small $\Delta V$ and large $N_C$ result in small $V_{OS}$ fluctuation but also slow converging speed. The detail analysis for the two parameters is given in subsections 2.3.1 and 2.3.2.

Circuit realization of the BCC is straightforward. As the blocks shown in Fig. 2.1, Fig. 2.2 and Fig. 2.7, there are only choppers, two accumulators and a few digital gates in CP. This digital parts can be easily synthesized using CAD tools. Since no multi-bit multiplier is required, the power and area overhead is quite small. The offset-variable comparator in RCC is the most area-consuming part, since it requires a fine-step offset control unit that covers a wide offset adjustment range. However, this area cost can be minimized by dense layout since there are no power or speed issues here.

### 2.3.1 Transient Behavior

As the calibration starts, BCC suffers a period of transient response before the offset voltage is converged. This period is directly related to the tracking ability of the calibration. To resist the effect of environment parameter variation, such as temperature or supply voltage variation, the time constant of the transient response has to be small.

Fig. 2.8 illustrates the front end of the BCC. In Fig. 2.8a, the input signal is randomly chopped by the chopper and becomes a zero-mean noise. Hence the signal in node $V_c$ is composed of a DC value coming from the offset voltage and a noise coming from the chopped input signal. Chopped input signal is usually quite larger than the offset voltage. This is shown in Fig. 2.8b.

CP suppress the effect of the chopped-input-signal noise and forces $V_{OS}$ moving toward 0 with feedback mechanism. Suppose that the input signal PDF over the range of

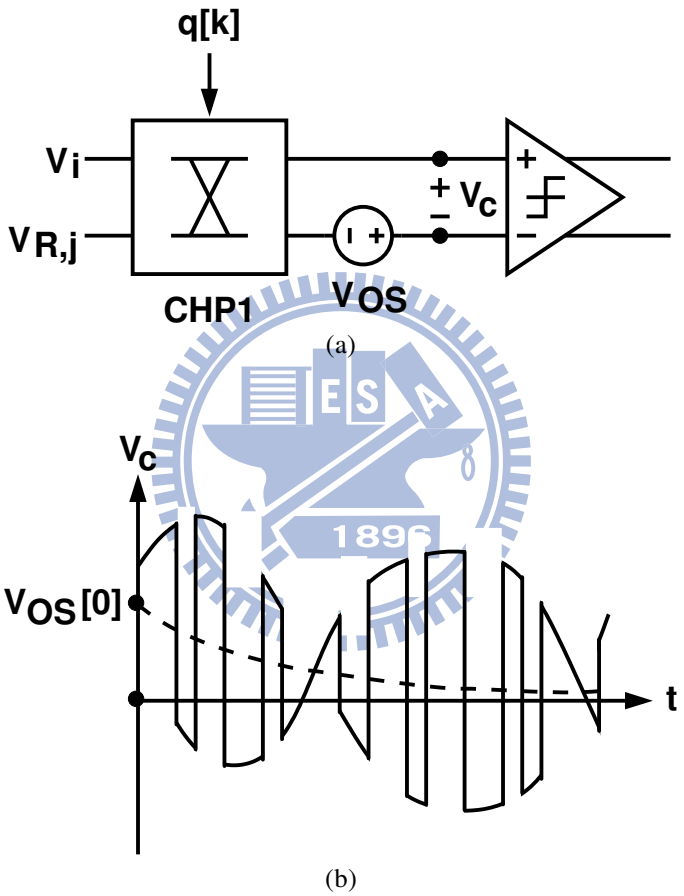



Figure 2.8: Transient behavior of BCC: (a) BCC front end; (b) Waveform on comparator input node.

$V_{R,j} \pm V_{OS}$ is a constant $D(V_{R,j})$, the value of $\Delta P$ in Fig. 2.2 can be expressed as:

$$\Delta P = 2D(V_{R,j})V_{OS} \tag{2.6}$$

Ignoring the disturbance from the input signal, the speed in which CP cuts $V_{OS}$ is proportional to $\Delta P$. As an example, when $\Delta P$ becomes half of its original value, the slope of accumulated $\sum(-q \times D_c)$ becomes half accordingly, and the period of which the BPD outputs non-zero value is doubled. This makes the speed for which CP cutting down $V_{OS}$ reduced by a half. According to (2.6), the above example implies that the decreasing rate of $V_{OS}$ is proportional to its value. Hence the transient behavior of $V_{OS}$ can be described by a single-pole model:

$$\frac{\Delta V_{OS}[k]}{\Delta k} = -\Delta V \times D(V_{R,j})V_{OS}[k] \times \frac{1}{N_C} \tag{2.7}$$

From (2.7), transient response of $V_{OS}[k]$ can be expressed as:

$$V_{OS}[k] = V_{OS}[0] \cdot \exp\left(-k\frac{\Delta P}{N_c}D(V_{R,j})\right) \tag{2.8}$$

where the time constant of this feedback system is:

$$\tau_c = \frac{N_C}{\Delta V \cdot D(V_{R,j)}} \tag{2.9}$$

Shorter $\tau_c$ results in better tracking ability for the calibration loop.

Fig. 2.9 shows an example of the $V_{OS}[k]$ transient response of a BCC. The initial offset, $V_{OS}[0]$, is set to 5.8 LSB. Calibration parameters are $\Delta V = (1/2)$ LSB and $N_C = 64$. The BCC is assumed to be located in the middle of a 6-bit ADC. With a full-range sinusoidal input signal and $V_{R,j} = 0$, we have

$$D(V_{R,j}) = \frac{2}{\pi} \cdot \frac{1}{V_{FS}} \tag{2.10}$$

In Fig. 2.9, the solid line is the discrete-time simulation result, and the smooth dashed line is the approximation using (2.8). The approximation manifests a good agreement with the simulation. The settling time constant is $\tau_c = \pi \cdot 2^6 \cdot 64 \approx 12868$.

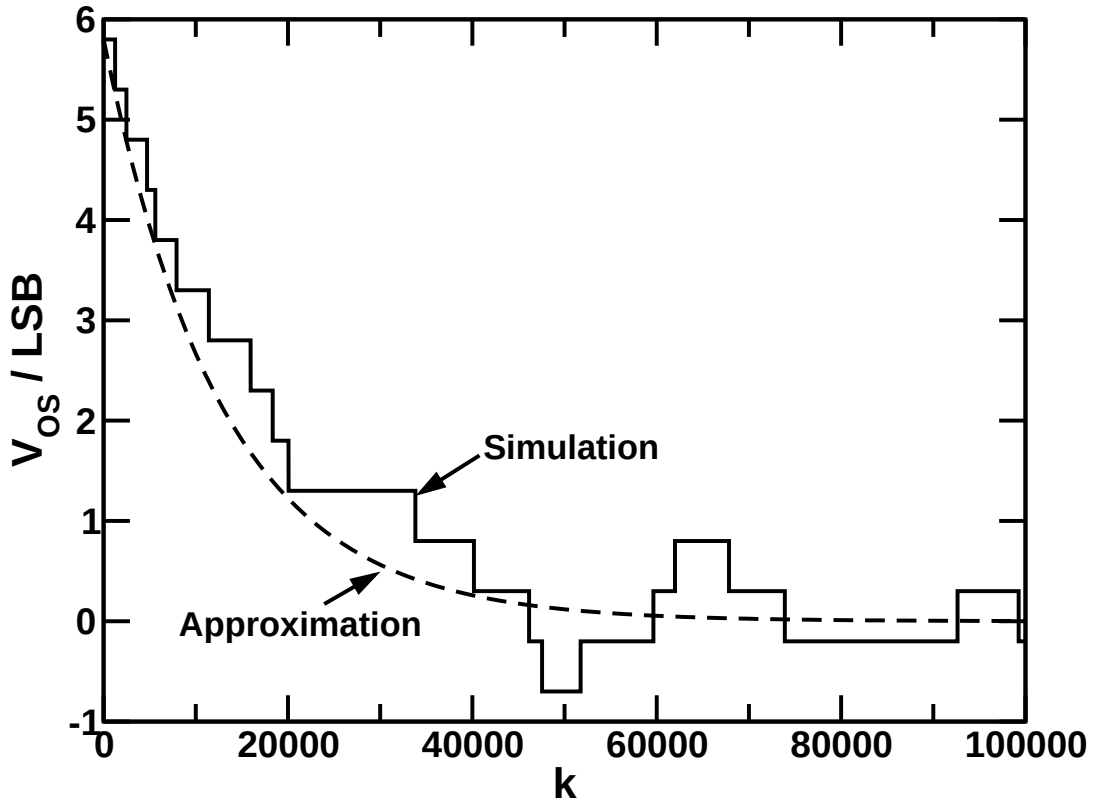



Figure 2.9: Transient response of a BCC example.

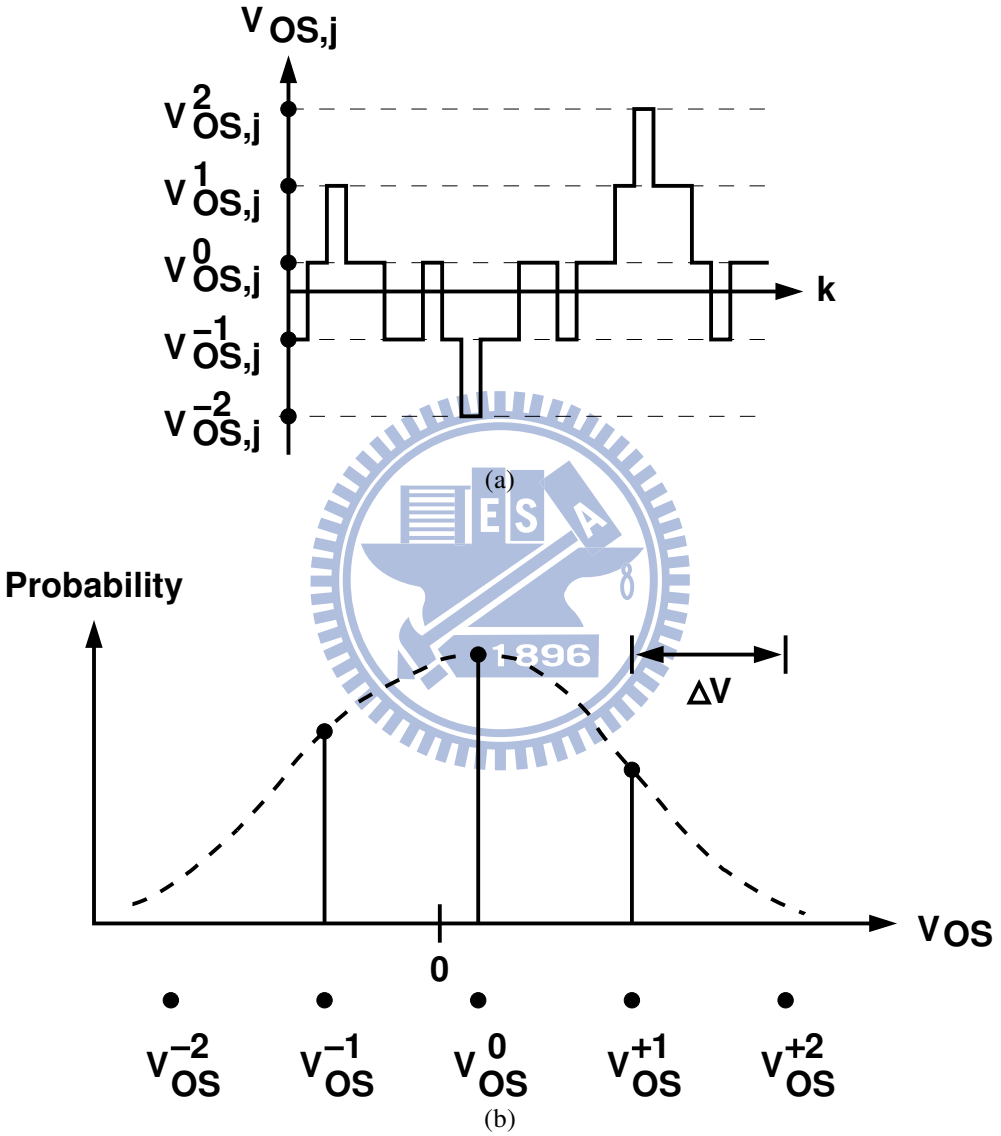



Figure 2.10: Offset fluctuation phenomenon: (a) Offset fluctuation waveform; (b) Probability mass function(PMF) of the offset voltage.

### 2.3.2 Offset Fluctuation

The digital calibration for BCC operates in background. Namely, it is never turned off even the offset voltage has been well trimmed. As the $V_{OS}$ is converged close to 0 due to the calibration process, the behavior of $V_{OS}[k]$ becomes a discrete random fluctuation around zero. This is shown in Fig. 2.10a. The stochastic behavior of $V_{OS}$ is described by a random sequence with discrete values, $\mathbf{V_{OS}}[k]$. Fig. 2.10b illustrates a possible probability mass function (PMF) for $\mathbf{V_{OS}}$ which is represented as $P(V_{OS})$.

The values for $\mathbf{V_{OS}}$ includes $V_{OS}^{0}$, $V_{OS}^{-1}$, $V_{OS}^{+1}$, $V_{OS}^{-2}$, $V_{OS}^{+2}$, ...etc. $V_{OS}^{0}$ is the value point closest to zero. The distance between two adjacent value points is the offset control step $\Delta V$. According to the definition of $V_{OS}^{0}$, possible value for $V_{OS}^{0}$ is between $-\Delta V/2$ and $+\Delta V/2$. The calibration loop forces the maximum value of $P(V_{OS})$ to occur at $V_{OS}^{0}$. A mathematical analysis for $\mathbf{V_{OS}}[k]$ is included in chapter A, which includes the procedures to calculate $P(V_{OS})$ from $\Delta V$, $N_C$, and the PDF of input signal.

Fig. 2.11 shows the $P(V_{OS})$ of a BCC with the condition identical to the Fig. 2.9. Results from both calculation and simulation are presented. The value of $V_{OS}^{0}$ is chosen to be $(1/4)\Delta V$. As expected, the maximum probability for $V_{OS}$ occurs at $V_{OS}^{0}$. The probability of $V_{OS}$ is diminishing when the distance to $V_{OS}^{0}$ is increased.

From $P(V_{OS})$, both the mean $\mu(V_{OS})$, and the standard deviation $\sigma(V_{OS})$ of $V_{OS}$ can be calculated. The value of $\mu(V_{OS})$ is always zero. This is enforced by the calibration feedback mechanism. The value of $\sigma(V_{OS})$ depends on $\Delta V$, $N_C$, and $V_{OS}^{0}$. If $V_{FS}$ is much larger than $\Delta V$ so that $P \gg \Delta P$, the effect of $V_{OS}^{0}$ on $\sigma(V_{OS})$ becomes insignificant.

Fig. 2.12 shows the $\Delta V$ and $N_C$ dependence of $\sigma(V_{OS})$ for a middle BCC in the 6-bit ADC design case. The $V_{OS}^{0}$ dependence of $\sigma(V_{OS})$ is neglected since $P \gg \Delta P$. The $\sigma(V_{OS})$ can be reduced by decreasing $\Delta V$ or increasing $N_C$, but at the expense of increasing the convergence time constant $\tau_c$. To achieve $\sigma(V_{OS}) < (1/3)$ LSB in the 6-bit ADC design case, one can choose $\Delta V = (1/8)$ LSB and $N_C = 2^5$ for short $\tau_c$, or $\Delta V = (1/2)$ LSB and $N_C = 2^8$ for long $\tau_c$. At circuit level, smaller $\Delta V$ is more difficult to implement if the offset adjust range is required to be the same. In this case, more digital bits are required for offset control.

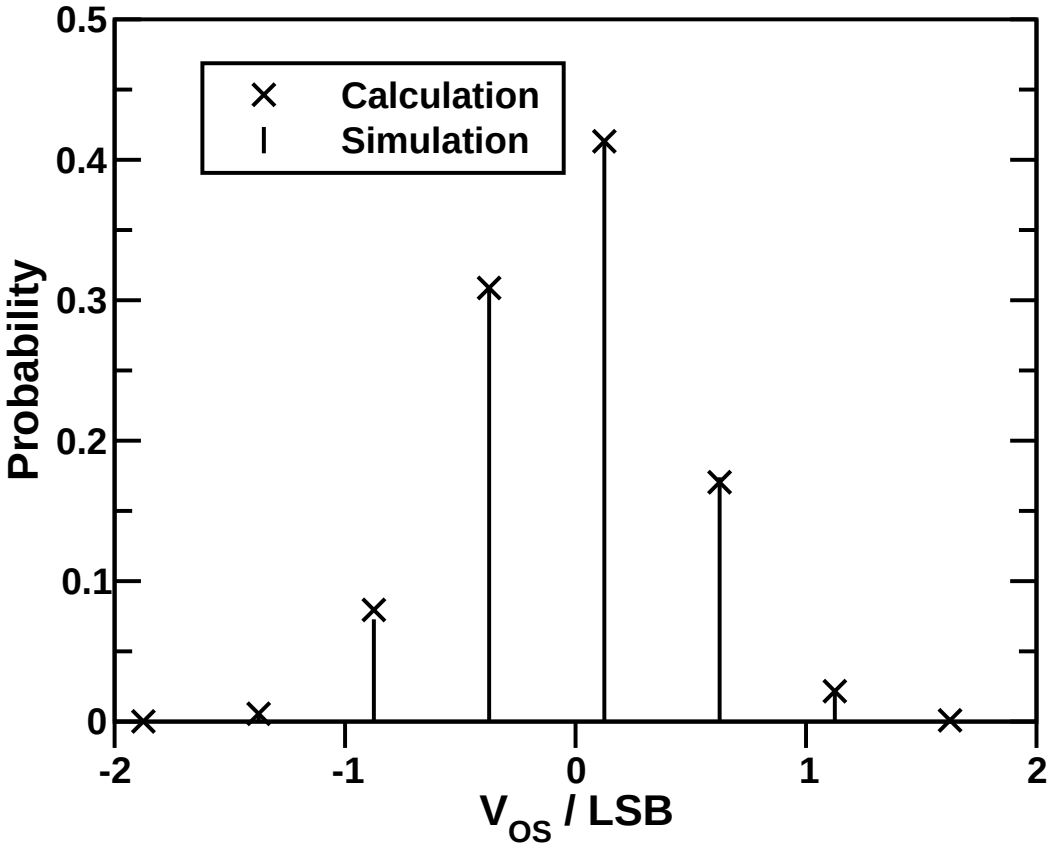



Figure 2.11: $P(V_{OS})$ of a BCC example.

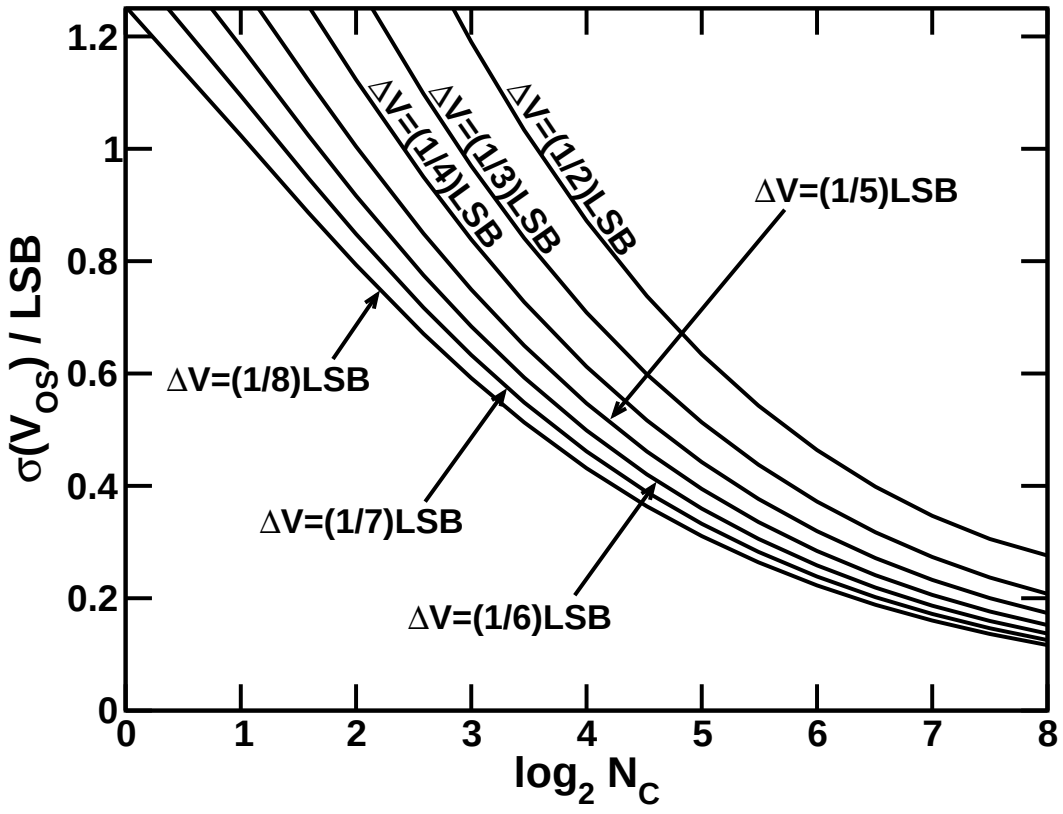



Figure 2.12: $\sigma(V_{OS})$ versus $N_C$

# Chapter 3

# Flash ADC with Digitally Calibrated Comparators

## 3.1 Input Windowing Technique

### 3.1.1 Input Dependent Issues

The background-calibrated comparator(BCC), which is shown in Fig. 2.7, is designed to replace each comparators in a flash ADC. In the BCC, its CP is activated if the corresponding output $D_c = 1$, and the offset formation is available only when $V_i$ falls within $\Delta P$ regions of Fig. 2.2. Since the $V_{R,j}$ for each BCC is different, and the input signal may not be a sine wave in practical applications, several issues need to be addressed while applying BCC into a real ADC design case:

1. Null-information input condition

   When the PDF of $V_i$ has zero value near $V_{R,j}$ for a period of time, the j$^{th}$ BCC experiences a condition with $\Delta P = 0$. This condition is illustrated in Fig. 3.1. The corresponding CP perceives no meaningful information about $V_{OS}$. Since $P \neq 0$, $V_{OS}$ of the j$^{th}$ BCC may wander around the null-information region where $\Delta P = 0$. This wandering phenomenon does not affect the quality of the ADC output as long as $\Delta P$ remains zero. However, as soon as the input condition is changed so that $\Delta P \neq 0$, the ADC may suffer a large $V_{OS}$ at the j$^{th}$ BCC before its CP can make the

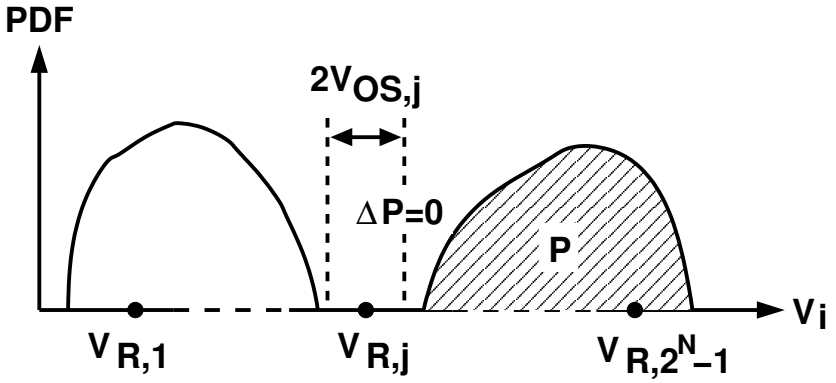



Figure 3.1: Null-information input condition.

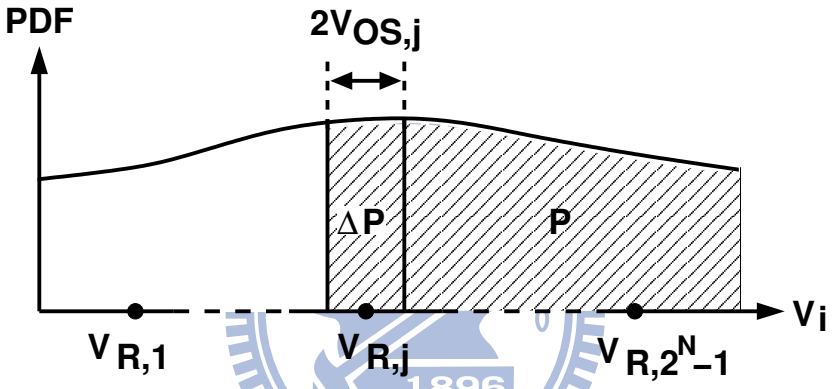



Figure 3.2: Small $\Delta P/P$ ratio in a real ADC case.

necessary correction.

2. Small $\Delta P/P$ ratio

   The calibration is based on the detection of $\Delta P$ and hence the polarity of $V_{OS}$. However, the comparator output contains offset information together with noise corresponding to $V_i$ falling within $P$. This noise causes $V_{OS}$ fluctuation and is suppressed by the AAR loop. When applying BCC into an ADC, $V_{OS}$ of a single BCC is quite small compared with the ADC input swing range. The resultant small $\Delta P/P$ ratio is shown in Fig. 3.2. This condition leads to rare offset information accompanied with large noise, and thus the calibration loop introduces large $V_{OS}$ fluctuation.

3. Location dependent $\Delta P/P$ ratio

   In a flash ADC, different comparators are associated with different $V_{R,j}$ values, thus

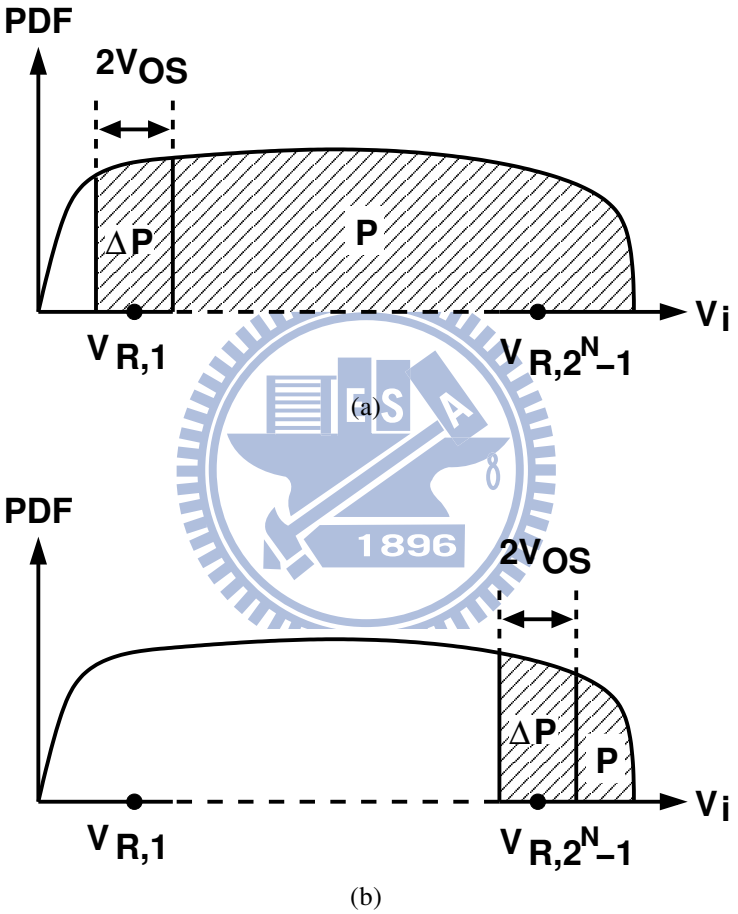



Figure 3.3: Location-dependent $\Delta P/P$ ratio: (a) for the bottom comparator; (b) for the top comparator.

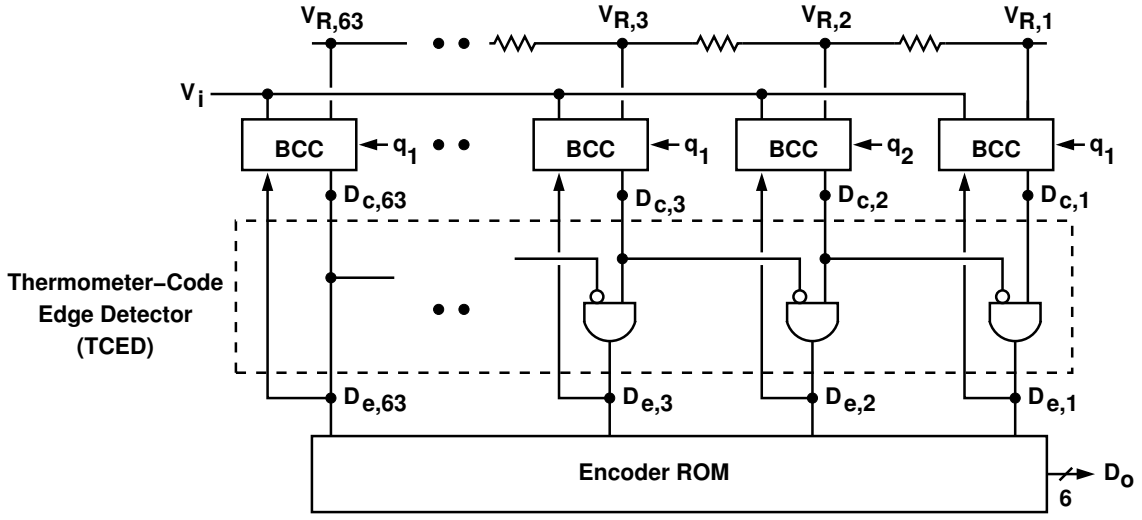



Figure 3.4: Flash ADC incorporating input-windowed BCCs.

perceives drastically different $P$ values even if the input signal has an uniform distribution. This condition is illustrated in Fig. 3.3. It leads to different $\Delta P/P$ ratio for different comparators. For example, the comparator corresponding to the top-end reference level has a much greater $\Delta P/P$ ratio than the comparator corresponding to the bottom-end reference, since the former one has a relatively small $P$ value. This condition complicates the choice of $N_C$ and $\Delta V$ parameters for each BCC if $V_{OS}$ fluctuation is considered.

### 3.1.2 Input Windowing

The issues described in subsection 3.1.1 can be resolved by input windowing technique shown in Fig. 3.4. In this architecture, the BCC output $D_{c,j}$ are fed to a thermometer-code edge detector(TCED), where $1 \leq j \leq (2^N - 1)$. Output of the TCED is a series of 0 except the bit in which the 0-to-1 edge of the thermometer code is located. This edge code is denoted with $D_{e,j}$ for $1 \leq j \leq (2^N - 1)$.

By Fig. 3.4, the TCED simply consists of two-input AND gates, so that $D_{e,j} = 1$ if $D_{c,j} = 1$ and $D_{c,j+1} = 0$. The CP of the j$^{th}$ BCC uses $D_{e,j}$, instead of $D_{c,j}$, as its input. With this arrangement, the j$^{th}$ CP is activated only when $V_i$ appears within $V_{R,j} + q_j V_{OS,j}$ and $V_{R,j+1} + q_{j+1} V_{OS,j+1}$. In most flash ADC designs, the TCED is a building block of the

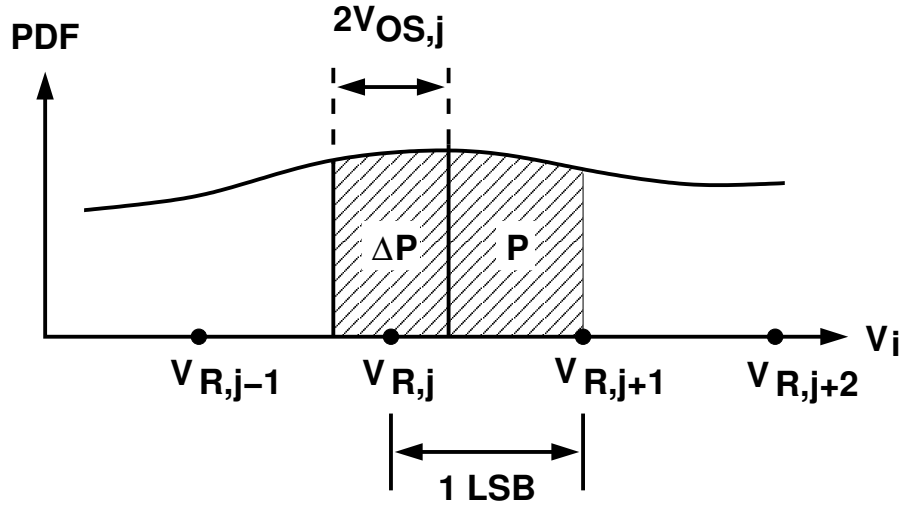



Figure 3.5: Input windowing for the j$^{th}$ BCC.

back-end encoder, thus no extra hardware is required for the proposed architecture.

The arrangement of Fig. 3.4 introduces a windowing effect which can reduce the $P$ value perceived by each BCC. As illustrated in Fig. 3.5, the $P$ region for the j$^{th}$ BCC is now confined between $(V_{R,j} + V_{OS,j})$ and $V_{R,j+1}$.The actual upper bound for the $P$ region is either $(V_{R,j+1} - V_{OS,j+1})$ or $(V_{R,j+1} + V_{OS,j+1})$, depending on the random sequence $q_{j+1}$. The averaged value of $V_{R,j+1}$ is used in Fig. 3.5.

With this windowing mechanism, the $\Delta P/P$ ratio for every BCC is drastically increased, resulting in smaller $V_{OS}$ fluctuation. In addition, the difference in $\Delta P/P$ between different BCCs is also reduced in most input input cases, thus all BCCs in the ADC can employ identical $N_C$ and $\Delta V$ for offset calibration.

The phenomenon of $V_{OS}$ wandering due to null-information input condition can still occur. However, if $\Delta V$ is assumed to be infinitesimal, the maximum distance around which $V_{OS,j}$ can wander is 1 LSB, which is the difference between $V_{R,j}$ and $V_{R,j+1}$. Whenever $V_{OS,j} \geq 1$ LSB, $P$ becomes zero and $V_{OS,j}$ can no longer wander. Thus, for a properly designed ADC of Fig. 3.4, its worst-case differential nonlinearity (DNL) is 1 LSB plus the $\Delta V$ step size.

### 3.1.3 Threshold Level Crossing

The windowing effect introduced by the TCED becomes complicated when the threshold levels of the BCC array are not monotonic. For j$^{th}$ BCC, the actual threshold level may deviate from the nominal level due to input offset voltage, and can be expressed as:

$$V_{t,j} = V_{R,j} + q_j \times V_{OS,j} \tag{3.1}$$

where $q_j \in \{+1, -1\}$ is the random sequence. The difference between two adjacent reference levels is one LSB, i.e., $V_{R,j+1} - V_{R,j} = 1$ LSB. Under normal condition with $V_{OS,j} \ll 1$ LSB, we have $V_{t,j-1} < V_{t,j} < V_{t,j+1}$ for all $j$. However, during the initial phase of calibration, it is possible that $V_{OS,j} > (1/2)$ LSB at some locations. This threshold level crossing is illustrated in Fig. 3.6.

Threshold level crossing does not corrupt the calibration but slow down the converging speed a bit. The effect can be seen from Fig. 3.6b. Here the $V_{OS}$ of the j$^{th}$ BCC is assumed to be a positive value. When $q = +1$, the j$^{th}$ threshold level moves up above the (j+1) $^{th}$ in the left of Fig. 3.6b, hence the output of (j+1) $^{th}$ BCC will certainly be 1 as the output of j$^{th}$ BCC becomes 1. From Fig. 3.6a, it is obvious that $D_{e,j}$ will always be 0 in this case. When $q = -1$, the j$^{th}$ threshold level moves down under the (j-1) $^{th}$, and the probability for $D_{e,j} = 1$ is the shadowed region in the right of Fig. 3.6b.

Comparing Fig. 3.6b with Fig. 2.2, the accumulated $(q \times D_{e,j})$ still tend to the negative direction, although the tendency may be more gradual. The calibration loop thus operates correctly.

As soon as $V_{OS}$ is trimmed less than 1 LSB, the threshold level crossing disappears and the converging speed of the calibration is recovered.

### 3.1.4 Upward Locking

Due to the TCED, the offset perception of j$^{th}$ BCC may be interfered by (j+1) $^{th}$ BCC and thus the calibration locked. This upward locking phenomenon is illustrated in Fig. 3.7.

As an example, it is assumed that $V_{OS,j}$ and $V_{OS,j+1}$ are both positive, $V_{OS,j} < V_{OS,j+1}$, and the j$^{th}$ and (j+1) $^{th}$ BCC are controlled by the same random sequence $q$. The probability for $D_{e,j} = 1$ is shown as the shadowed region in Fig. 3.7b. Compared with Fig. 2.2,

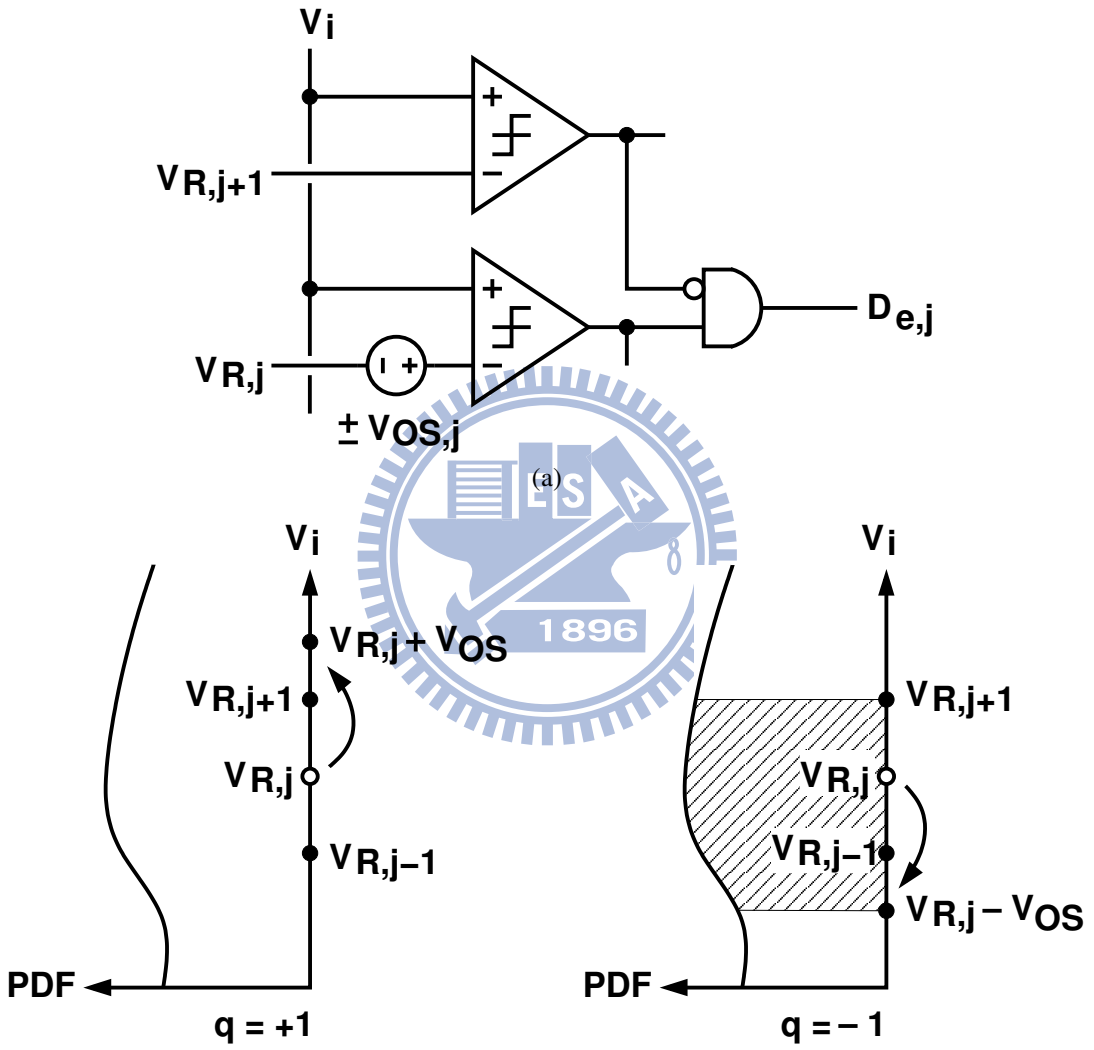



Figure 3.6: Effect of threshold level crossing: (a)j$^{th}$ TCED and the preceded comparators; (b) probability of $D_{e,j}$=1.

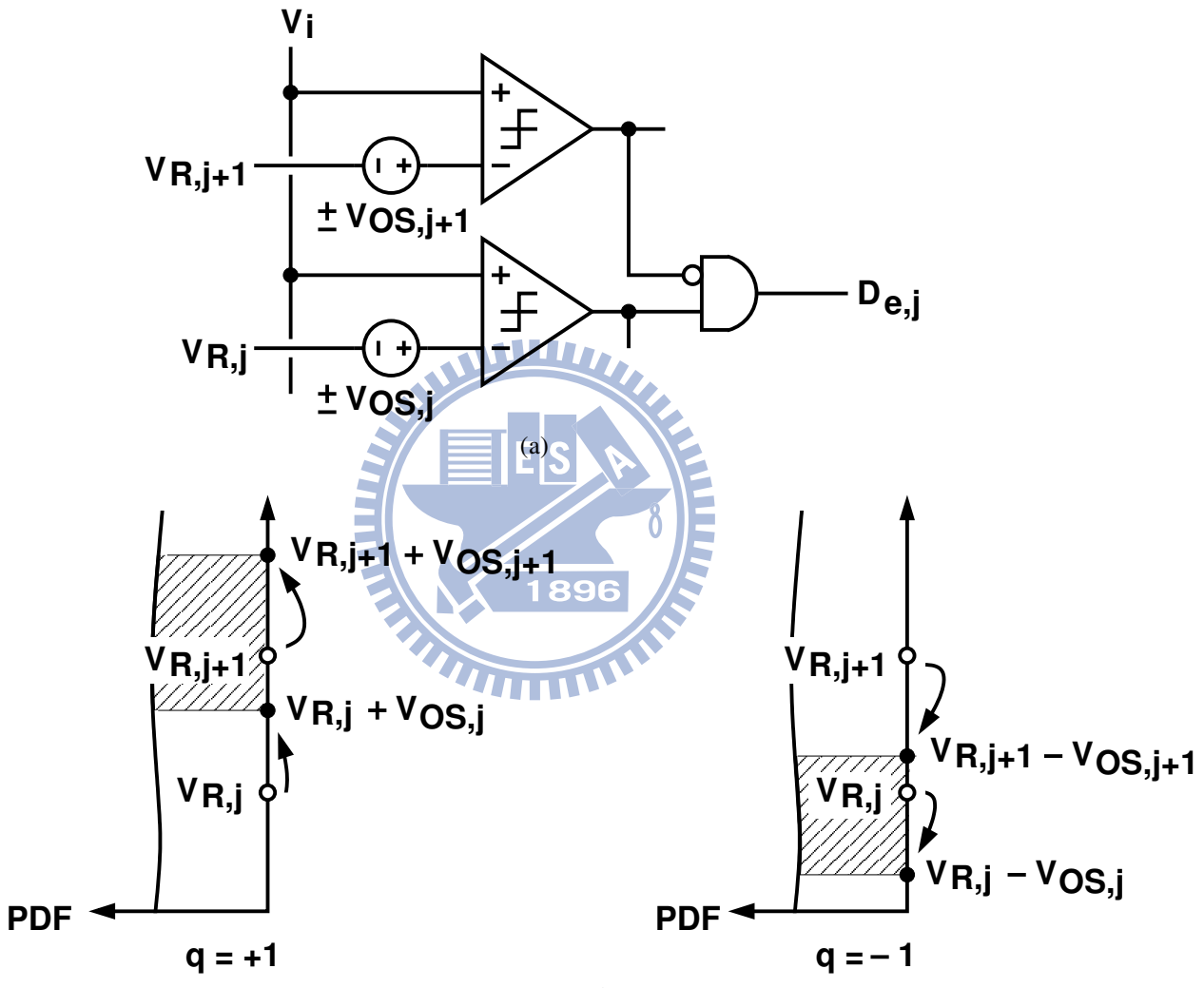



Figure 3.7: Upward locking caused by offseted threshold levels: (a)j$^{th}$ TCED and the preceded comparators; (b) probability of $D_{e,j}$=1.

the integration of $(q \times D_{e,j})$ tends to incline upward because the larger $V_{OS,j+1}$ expand the shadowed region for $q = +1$ and compress the region for $q = -1$. Since the j$^{th}$ calibration processor does not have any information about $V_{OS,j+1}$, the calibration for j$^{th}$ comparator will diverge due to the positive tendency of $q \times D_{e,j}$. The calibration divergence will increase $V_{OS,j}$ until $V_{OS,j} = V_{OS,j+1}$ and then the upward locking is dismissed.

In the case that the input distribution is extended to the upmost comparator, the upward locking forces the offset voltage of the upmost comparator $V_{OS,2^N-1}$ to converge to 0 sooner than other ones. Followed by $V_{OS,2^N-1}$ is the offset voltage next to it, $V_{OS,2^N-2}$. Its convergence depends on $V_{OS,2^N-1}$ and will be slower than $V_{OS,2^N-1}$. Followed by $V_{OS,2^N-2}$ is $V_{OS,2^N-3}$, and so on.

In the case that the input distribution is only extended to some reference level $V_{OS,m}$, all comparator offset voltages corresponding to the lower reference levels will be confined by $V_{OS,m}$ and may never be calibrated to 0, unless there is some inherent comparator offset smaller than $V_{OS,m}$.

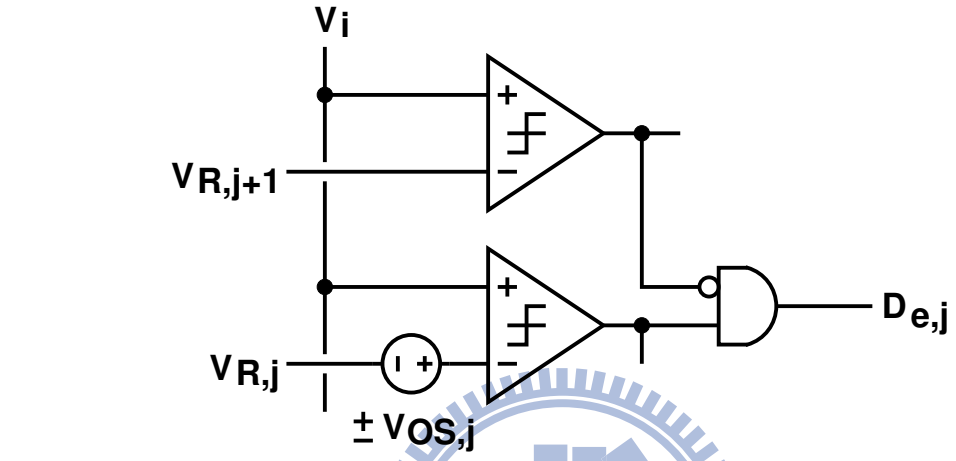
To eliminate the upward locking phenomenon, two independent random sequences are used for even and odd BCCs respectively. This configuration has been illustrated in Fig. 3.4 and the probability for $D_{e,j} = 1$ is shown in Fig. 3.8.

Since $q_j$ is independent of $q_{j+1}$, the j$^{th}$ calibration processor perceives an averaged $V_{OS,j+1}$, which is equal to 0. It is shown in Fig. 3.8a. The shadowed region in Fig. 3.8b becomes exactly the same as in a single random-chopping comparator in Fig. 2.2.

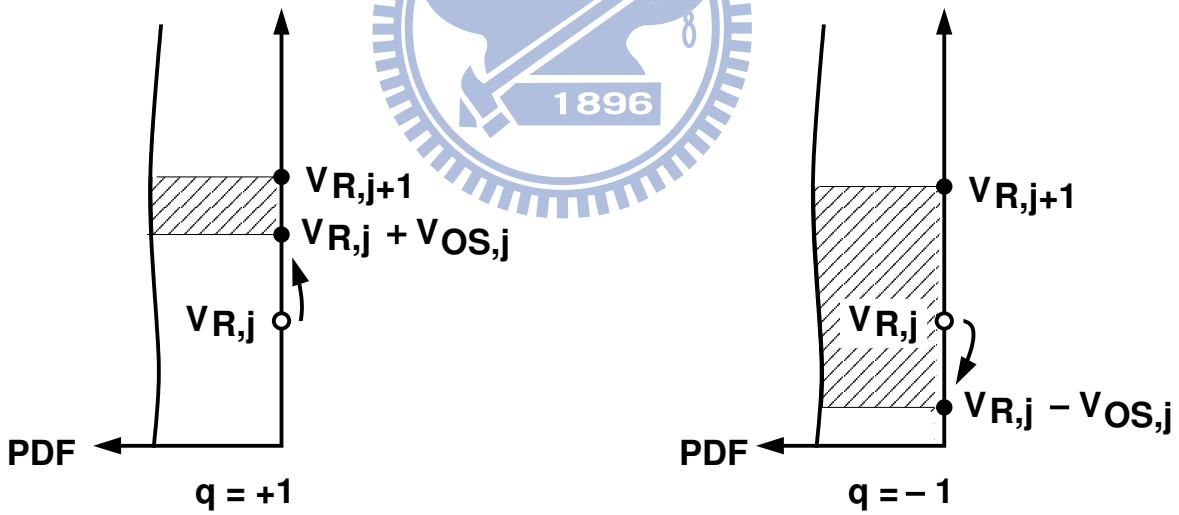
### 3.1.5 Offset Fluctuation

Since $V_{OS,j}$ for all $j$ will be trimmed to less than (1/2) LSB after the calibration process converges, the threshold level crossing effect is eliminated, and the fluctuation analysis for the j$^{th}$ BCC is reduced to the calculation of the probability mass function $P(V_{OS})$ for a simple BCC.

From Fig. 3.5, we have $\Delta P/P = 2V_{OS}/(\text{LSB} - V_{OS})$. It is assumed that the input signal is uniformly distributed within the window. Then we can calculate $P(V_{OS})$ using the procedures described in the Appendix. Notably, the $P(V_{OS})$ depends on $\Delta P/P$, $\Delta V$, and $N_C$ only. The larger probability of $R = 0$ introduced by the windowing effect does




(a) comparators with thermometer-code edge detector.




(b) probability of $D_{e,j}$=1

Figure 3.8: Upward-locking-free operation: (a)j$^{th}$ TCED and the preceded comparators; (b) probability of $D_{e,j}$=1.

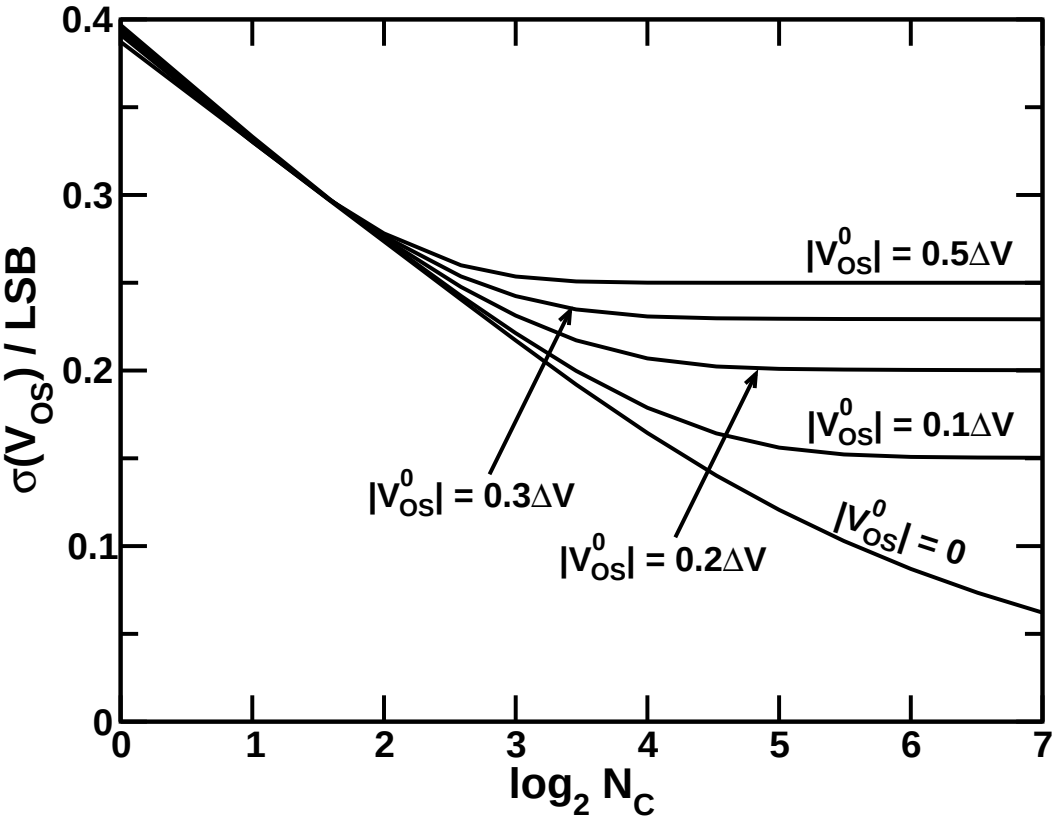



Figure 3.9: $\sigma(V_{OS})$ of a windowed BCC in a 6-bit ADC

not affect $P(V_{OS})$.

Fig. 3.9 shows the calculated standard deviation of $V_{OS}$ for a windowed BCC, which is represented as $\sigma(V_{OS})$. The 6-bit ADC design case with $\Delta V = (1/2)$ LSB are assumed. $V_{OS}^0$ denotes the offset control step closest to the comparator threshold level.

Unlike the calculation results shown in Fig. 2.12, the influence of $V_{OS}^0$ on $P(V_{OS})$ becomes evident due to a much larger value of the $\Delta P/P$ ratio. As $N_C$ increases, the $\sigma(V_{OS})$ decreases and is saturated at different value for different $V_{OS}^0$. The worst-case saturation value for the $\sigma(V_{OS})$ occurs at $|V_{OS}^0| = (1/2)\Delta V$. In this case and with large $N_C$, the $V_{OS}$ stays at either $+(1/2)\Delta V$ or $-(1/2)\Delta V$, resulting in $\sigma(V_{OS}) = (1/2)\Delta V = (1/4)$ LSB.

Fig. 3.10 shows the $\Delta V$ and $N_C$ dependence of the $\sigma(V_{OS})$. The 6-bit ADC case using windowed BCCs and the worst-case $|V_{OS}^0| = (1/2)\Delta V$ are assumed. Comparing with

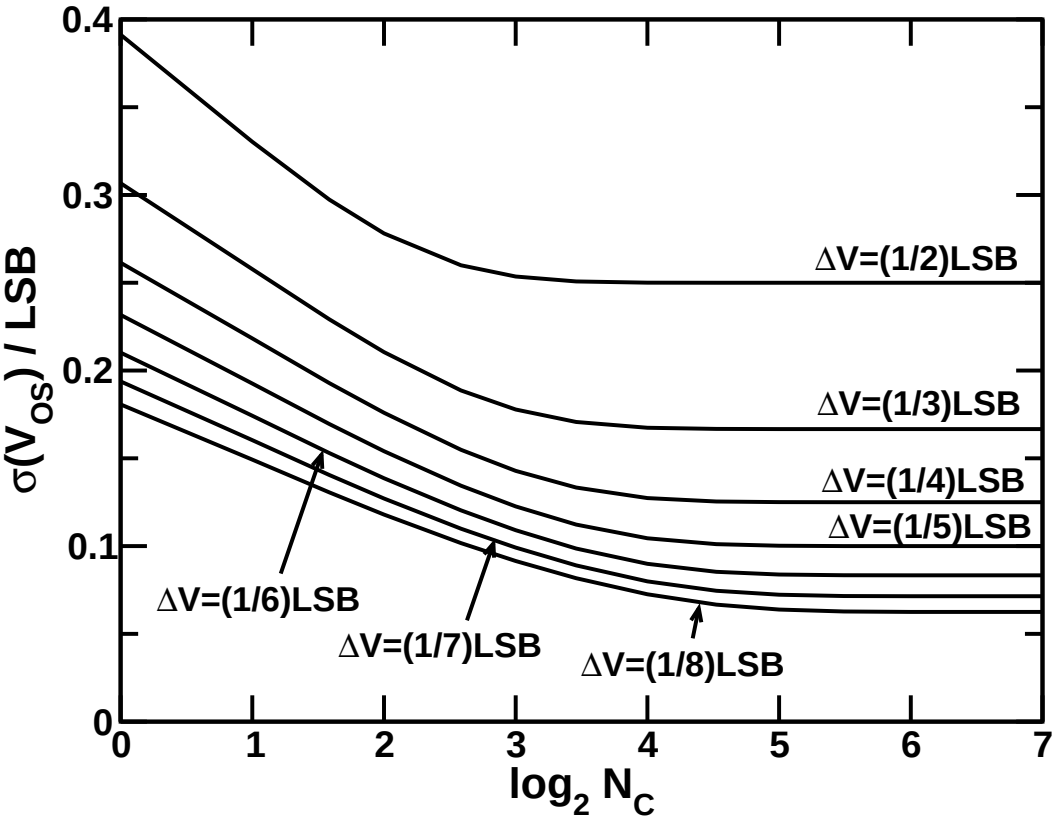



Figure 3.10: Worst-case $\sigma(V_{OS})$ with $V_{OS}^{0} = (1/2)\Delta V$.

Fig. 2.12, the $\sigma(V_{OS})$ corresponding to the same $\Delta V$ and $N_C$ is reduced drastically by using windowed BCCs.

## 3.2 A 6-bit ADC Design Case

In this section, system simulation is performed for an exemplified ADC design case illustrated in Fig. 3.4. All BCCs identically have $\Delta V = (1/4)$ LSB and $N_C = 16$. They are also introduced with random offsets in the initial. The distribution for these random offset is a Gaussian distribution with a standard deviation of 2 LSB. The input signal for the ADC simulation is a full-range sine wave.

The offset fluctuation of each BCC is ergodic, and there are $2^N - 1$ BCCs in this case, thus the ensemble standard deviation of the BCC array, instead of the standard deviation

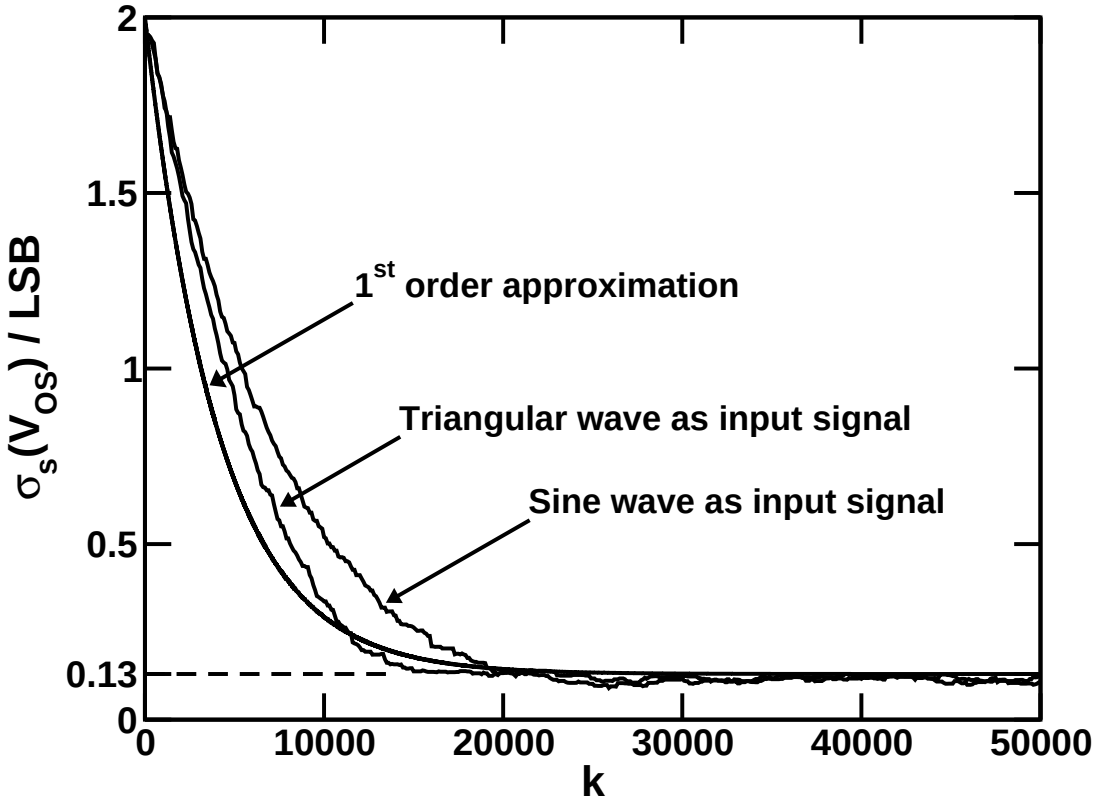



Figure 3.11: Transient behavior of a 6-bit ADC design case.

of individual BCC, is checked here. There is no need to collect the offset data along the time axis for the calculation of the ensemble standard deviation, thus the offset fluctuation can be verified at each time index.

Fig. 3.11 shows the transient behavior of the ensemble standard deviation of $V_{OS}$, which is represented as $\sigma_s(V_{OS})$, from the simulation of the 6-bit ADC example. In Fig. 3.11, $\sigma_s(V_{OS})$ is initially set to 2 LSB. As calibration proceeds, it is forced to settle to a small but non-zero value. This value is closed to 0.13 LSB, which is consistent with the result of Fig. 3.10.

As expected, the input signal affects the calibration transient behavior. Simulation with triangular-wave input, which has an uniform PDF, settles faster than the case with sine-wave input. Also plotted in Fig. 3.11 is the approximation of (3.2) and (2.8). The time constant is $\tau_c = N_C \times 2^6 \times 4 = 4096$. From (2.8), it will take $2.73\tau_c$, which is ap-

proximately 11,000 samples, for the ADC to reduce its $\sigma_s(V_{OS})$ from 2 LSB to 0.13 LSB. On the other hand, the corresponding settling time is approximately 15,000 samples in simulation with triangular-wave input and 20,000 samples in simulation with sine-wave input. The settling time deviation of the triangular-wave case is due to the threshold level crossing effect, which temporarily inhibits some of the BCCs from self-adjusting and thus slows down the entire calibration process.

From (2.7), the derivative of offset variation is a function of $\Delta P$. It is not affected by $P$, thus (2.8) is still applicable to estimate the settling time for input-windowed BCCs in Fig. 3.4. The time constant $\tau_c$ will diverse for different BCC due to non-uniformly distributed $V_i$. Assuming $V_i$ is uniformly distributed over the entire input range and thus $D(V_{R,j}) = 1/V_{FS}$, $\tau_c$ can be expressed as:

$$\tau_c = N_C \times \frac{V_{FS}}{\Delta V} \tag{3.2}$$

The actual transient response can be slower than the one predicted by (3.2) if the threshold level crossing occurs.

All BCCs in Fig. 3.4 can be calibrated independently and simultaneously, thus the settling time is independent of the number of BCCs. To apply BCC to a general-purpose ADC, a power-on calibration is necessary since the input signal distribution is unknown and the large initial offset on comparators may stay for a long time. The power -on calibration can be accomplished by additional circuit hardware or by just feeding for a short period of time an arbitrary waveform which has full-swing distribution. After the power-on calibration, offsets of all comparators are minimized and the ADC is ready to operate well with background calibration.

The effectiveness of the proposed calibration scheme is demonstrated in Fig. 3.12. Shown in the figure are offsets of each BCC before and after calibration. Data are recorded at $k = 0$ and $k = 1,000,000$ respectively. Offsets on all comparators are trimmed to a value below 0.5 LSB.

The spectrum characteristics of the ADC are illustrated in Fig. 3.13a and Fig. 3.13b. Input signal is a full-swing sine wave with frequency 100 MHz. For Fig. 3.13a, the calibration loop is inhibited and an initial $\sigma_s(V_{OS})$ of 2LSB is introduced. Large offset voltages cause considerable distortion tones and severely raise the noise level. The cancellation

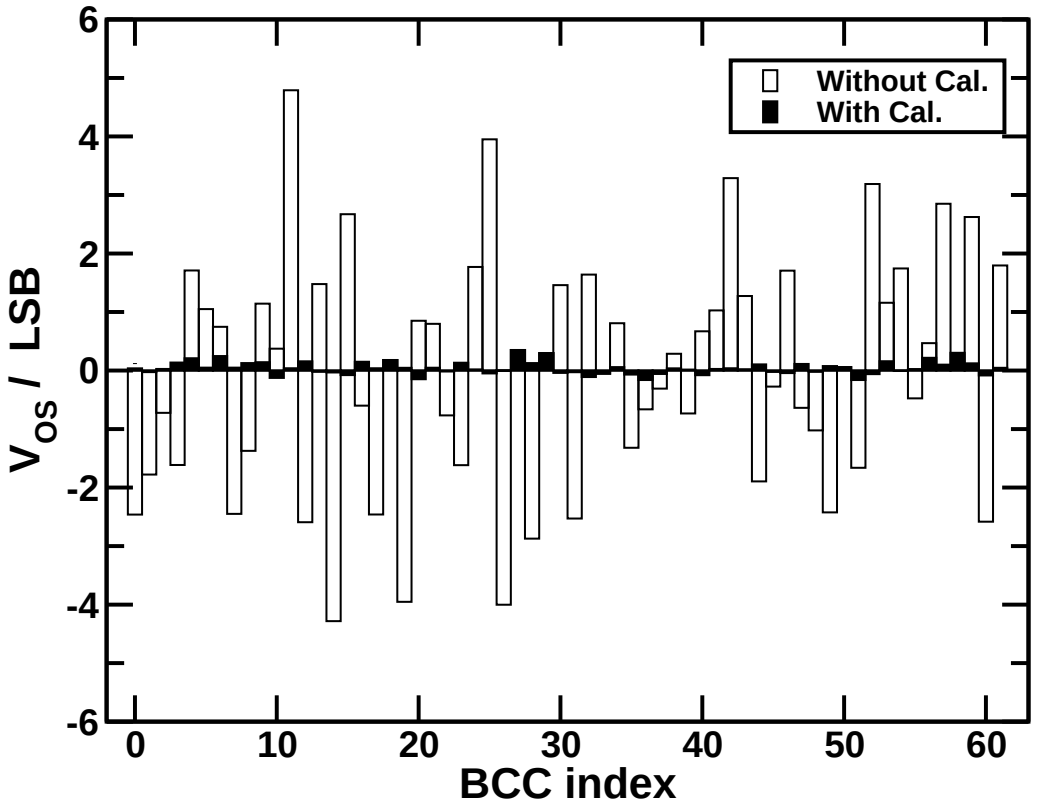
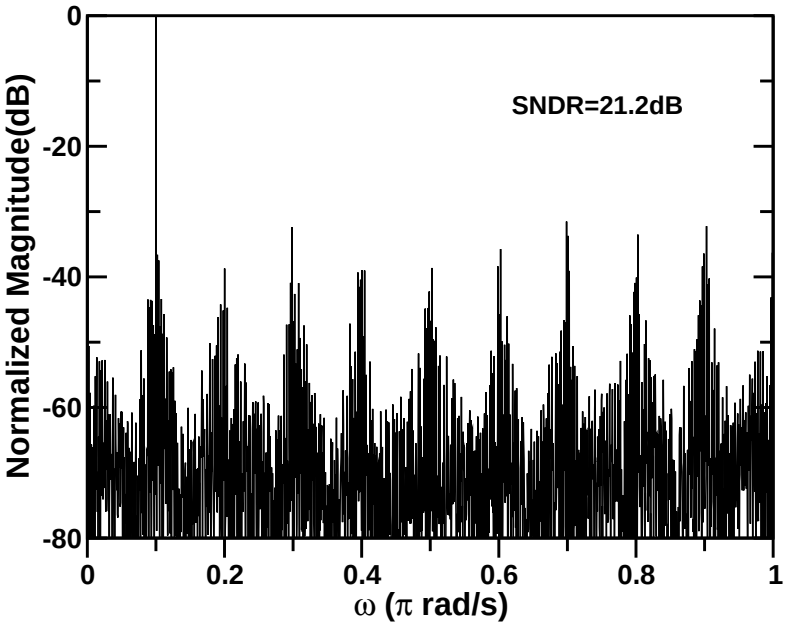


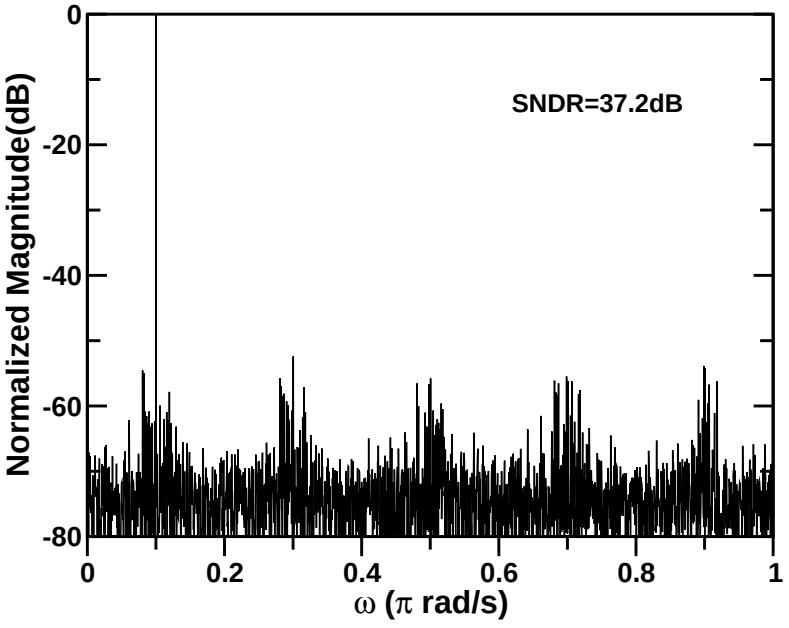

Figure 3.12: BCC Offsets before and after calibration.

of even-order distortion in fully differential architecture is suppressed due to rich bubble errors caused by reference crossing.

With the same input signal, Fig. 3.13b is the output spectrum obtained after the calibration loop has activated for $1,000,000$ of $k$. The selected $\Delta V$ and $N_C$ introduce only insignificant calibration noise in the spectrum and the even order cancellation is recovered. The background calibration technique improves the SNDR from 21.2dB to 37.2dB, which is quite near the limit of quantization noise.




(a)




(b)

Figure 3.13: Spectrum performance for a 6-bit ADC: (a) without calibration; (b) with calibration.

# Chapter 4

# A 6-bit 2GSample/s Flash ADC

## 4.1 Specification and Architecture of the ADC

Based on the proposed calibration technique, an analog-to-digital converter is implemented using 65nm low-power CMOS technology. The circuit architecture is shown in Fig. 4.1. The target specification for this ADC is 6 bits in resolution, 2Gsample/s in sampling rate and minimized power consumption to achieve maximum power efficiency.

Reference levels are generated from a resistor string with which the top and bottom levels are provided. The top and bottom reference levels are set to 1.2V and 0.8V, providing $\pm 0.4V$ for the input swing range. The input common-mode level is 1.0V and is suitable for the N-type differential pair as the comparator amplification. Two P-type MOSFETs, together with the wire parasitic capacitance, act as the sample-and-hold stage.

According to the calculation and the simulation in chapter 3, the parameters for calibration is set to $N_C$=16 and $\Delta V = 1/4$ LSB. Calibration processors for all comparators in this ADC use the same parameters and are activated concurrently. A power-on calibration with a full-filled sine wave as the input signal is applied to zero the offsets of all background-calibrated comparators. The ADC then enter the background calibration mode.

The bubble-insensitive TCEDs, which is made of 3-input AND gates, and an intermediate Gray encoder are included in the ADC to mitigate the bubbles caused by metastable comparison.

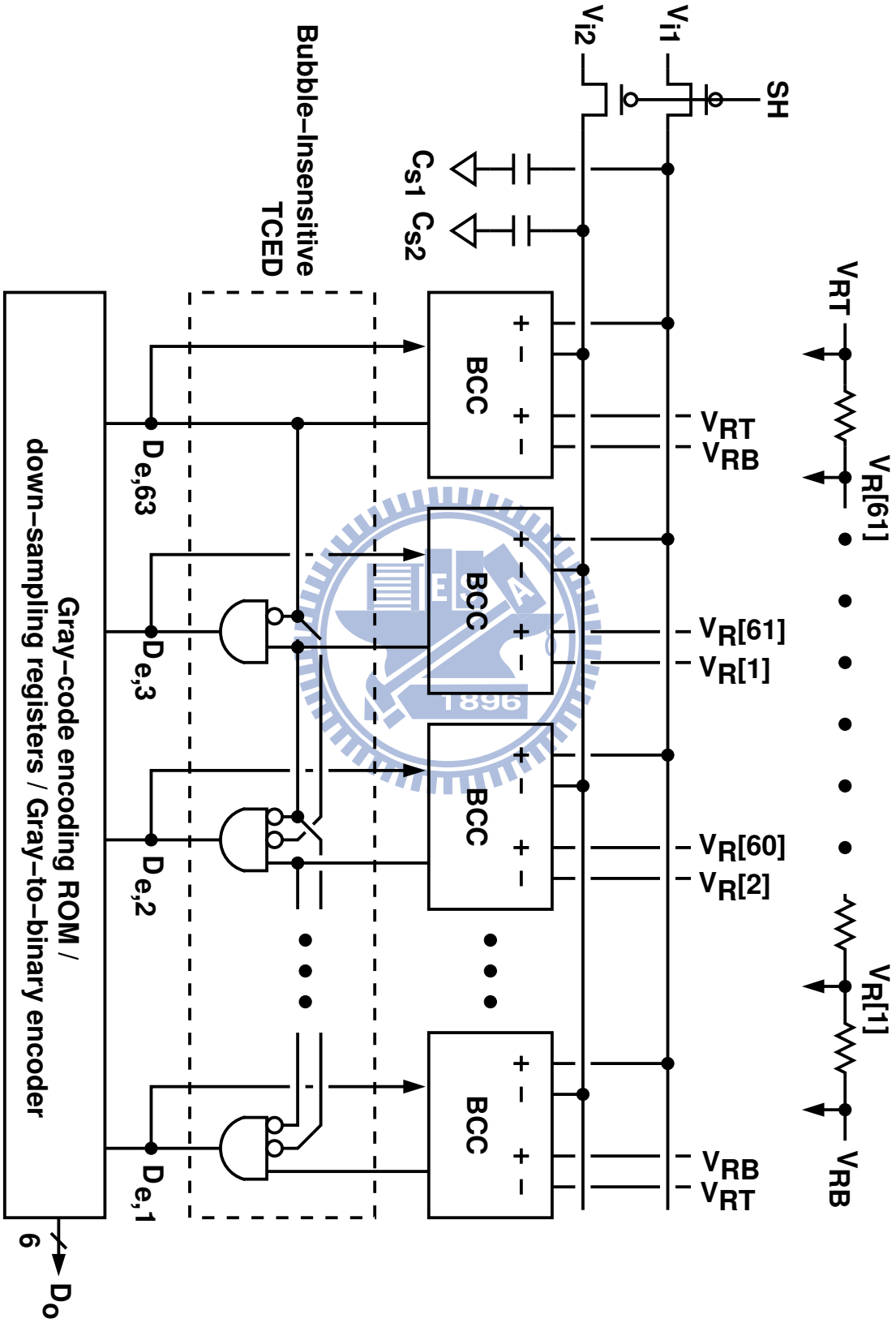



Figure 4.1: ADC architecture for circuit implementation.

The capacitance for the sample-and-hold stage and the layout parasitics in input network are kept as small as possible, hence it is possible to reconfigure this ADC in a time-interleaving application.

The output codes are decimated by 1/64 of the conversion rate for the measurement facilities.

## 4.2 Resistor String

The reference levels required for the BCC array is provided by a resistor string. It is composed of 62 resistors connected in series. Two external reference voltage source $V_{reft}$ and $V_{refb}$ are applied to the top and the bottom ends the resistor string. The resistor string acts as a voltage divider which providing 63 equally spaced reference levels for the comparator array.

Design issues of the resistor string includes the value of the resistance, bypass capacitance, reference level linearity, and the resistor matching. The value of the resistance decides the discharging ability for each reference node. It is important because both the comparator reset and the chopper swapping generate kickback pulses to the reference nodes. Reference levels have to be settled back to its nominal value before the comparison starts. Small resistance gives strong discharging ability but consumes more power. Bypass capacitors connected to reference nodes influence the kickback noise, too. In general, small bypass capacitors make the settling faster but large bypass capacitors reduce the deviation of the reference levels. Since parasitic capacitance on wires are inevitable, they are increased on purpose to provide a larger bypass capacitor in our design.

The resistance of each resistor is set to $5\Omega$. The total resistance of the resistor string is $310\Omega$, consuming a DC power of about 0.5mW. Wire parasitic capacitance in each reference node is 55fF. The resistor type is P-diffusion. The diffusion capacitance of the P-diffusion helps to increase the bypass capacitance. Resistors are put in a N-well entirely surround by guard rings to prevent substrate coupling.

The reference level linearity and the resistor matching issues are related to the layout geometry and the process variation. Layout of the resistor string has to traverse the whole chip to supply the reference levels for all comparators. In such large scale, gradient varia-

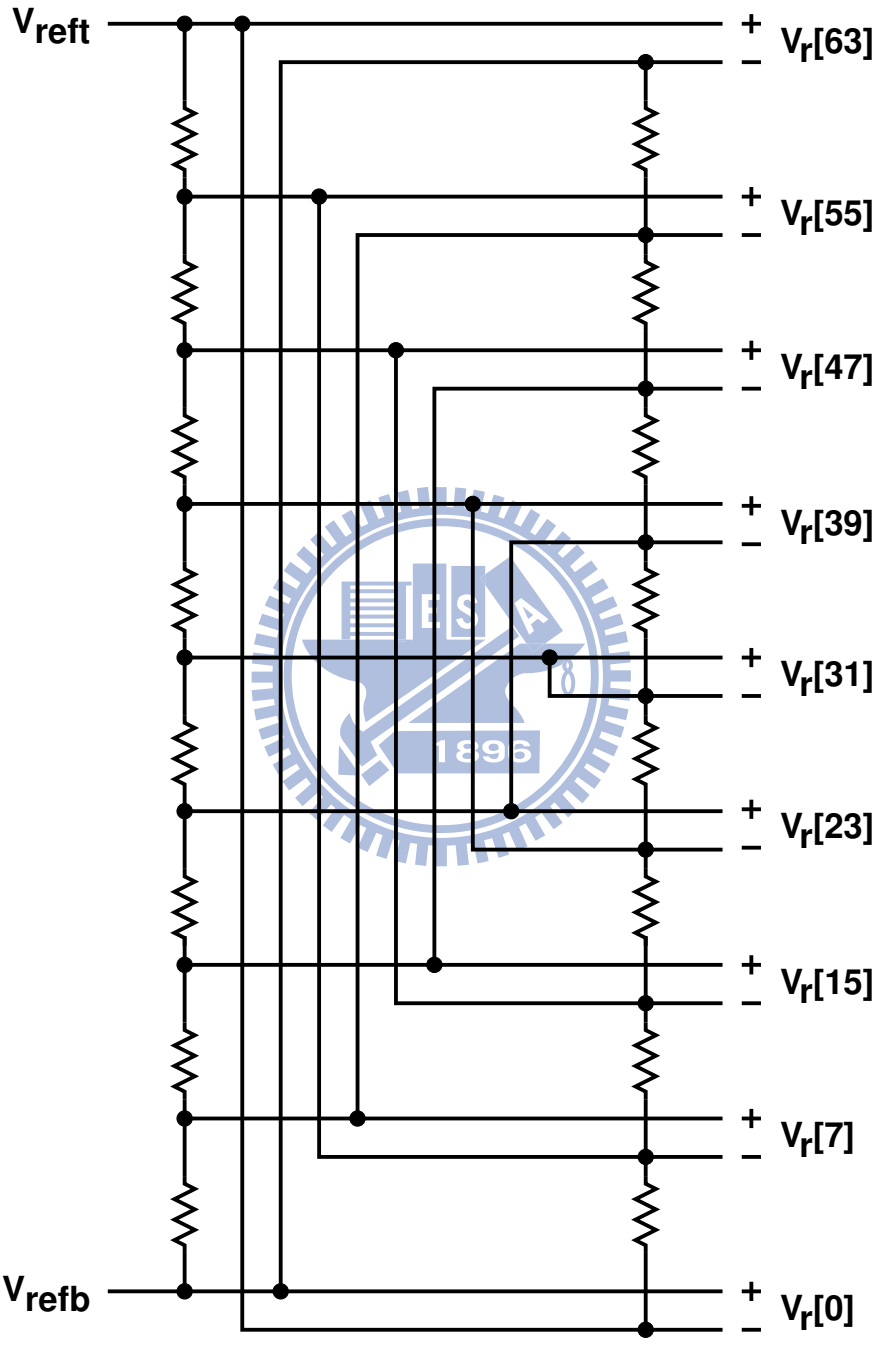



Figure 4.2: Cross connection for resistor string.

tion on process parameters may introduce large deviation on resistance values especially for the resistors in the top and the bottom ends. This deviation forms a distorted reference levels and introduce a non-linear distortion. To mitigate the effect of gradient variation, cross connection is applied to the resistor string, which is shown in Fig. 4.2.

Two resistor strings are put closely in the same layout orientation with the $7^{th}$, $15^{th}$, $23^{th}$, $31^{th}$, $39^{th}$, $47^{th}$, $55^{th}$ node of one string connected to the $55^{th}$, $47^{th}$, $39^{th}$, $31^{th}$, $23^{th}$, $15^{th}$, $7^{th}$ node of the other. $V_{reft}$ is applied to the top end of one string and to the bottom end of the other. Similarly, $V_{refb}$ is applied to the bottom end of the former and to the top end of the latter. Each resistor in the strings has resistance value of $10\Omega$, which is double of the nominal value.

Due to gradient process variation, each resistor on one string has similar resistance deviation to the corresponding resistor on the other string. Cross connection over the strings obtains a harmonic mean of two resistor with opposite resistance deviation. As shown in (4.1), the deviation is transformed into a second-order term. Since the deviation is a small amount, this can minimize the reference level distortion caused by resistance deviation.

$$2(R + \Delta R) \parallel 2(R - \Delta R) = R - \frac{\Delta R^2}{R} \tag{4.1}$$

As an example, connection of the $7^{th}$ node of one string to the $55^{th}$ node of the other string is to connect the first and the last 7 resistors of the two strings in parallel. Suppose the resistance deviation is 0.1%, that is, one 7-resistor section has a resistance value of $70 \times 1.001$ and another section has a value of $70 \times 0.999$, the overall resistance for the parallel connected resistor is $39 \times 0.9999$. The resistance deviation is reduced to 0.01%.

Cross connection is only applied to the section of 7 resistors instead of to each resistor. This is because the wire connection will become too complex and area consuming in the latter case. Since the resistance of a 7-resistor section is as small as $70\Omega$, ultra wide wires are used in the layout for cross connection to ensure a smaller wire resistance. Otherwise the effect of cross connection may be insignificant.

The resistor matching issues are aroused from the local process variation. A Monte-Carlo simulation with 1000 samples are applied to verify the reference level deviation due to resistor mismatch. The simulation is based on the resistor mismatch data supplied by th foundry. The simulation results is shown in Fig. 4.3. The X-axis is the index of the

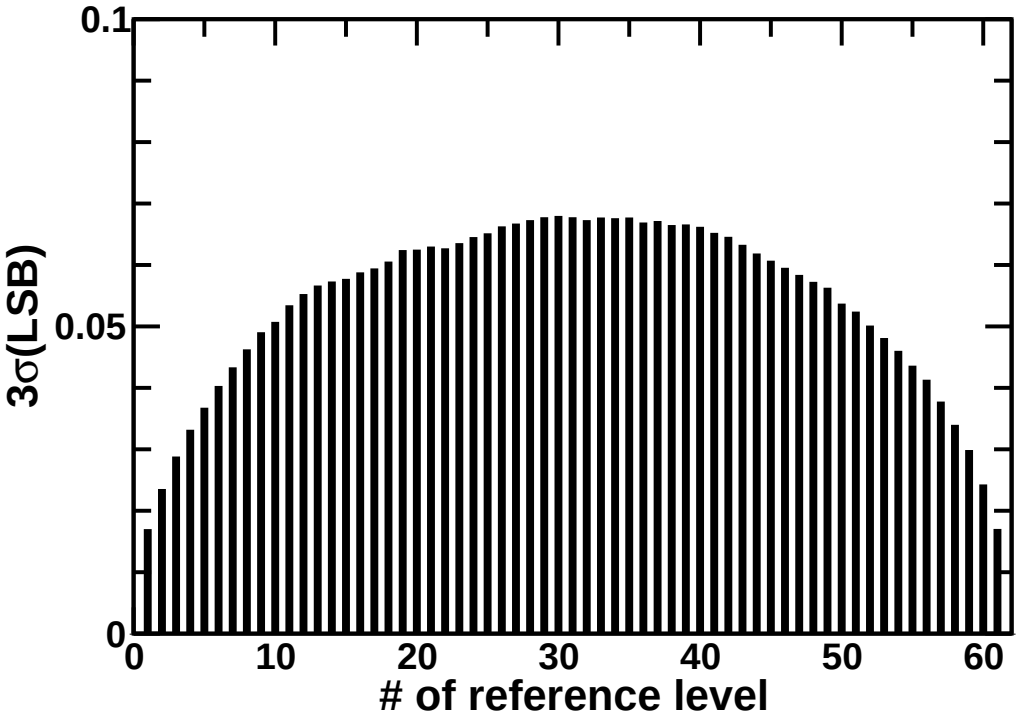



Figure 4.3: Reference level deviation due to resistor mismatch.

reference level, and the Y-axis is the normalized multiplied-by-3 standard deviation of the reference voltage. The maximum value of $3\sigma$ is no more than 0.07 LSB, which can be neglected.

## 4.3 Background Calibrated Comparator

### 4.3.1 Circuit Structure

The circuit structure of the BCC is shown in Fig. 4.4.

The comparator is composed of 3 cascaded latches to enlarge the transient voltage gain and thus reduce metastability. Since the calibration converges fast with the selected parameters $\Delta V$ and $N_C$, the calibration processor operates at 1/64 of the conversion rate.

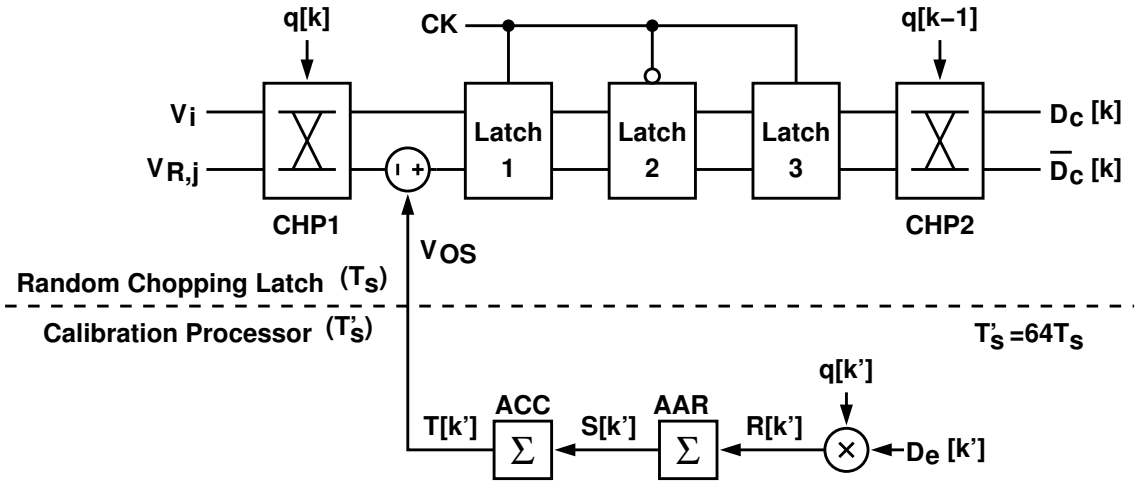



Figure 4.4: Circuit structure of the background calibrated comparator.

This arrangement reduces the power consumption and eliminates conversion latency effect from the calibration loop. The conversion latency is mainly caused by the cascaded latches.

Because of the lower operation speed for calibration processor, there are two two clock domains in the calibration loop. It is important to assure correct timing in the clock domain interfaces. The low-speed clock used by calibration processor is divided from the conversion clock. A delay line is put between the divider and the output buffer to generate 8 clock phases. A 8-to-1 multiplexer controlled by an off-chip controller select a proper phase to latch the output of comparator for the calibration processor. This arrangement provides an off-chip controllability to correct data latching error in the measurement of the test chip. In mass production cases, clocking in different domain can be assured by detailed post-layout simulation. However, the adjustable phases are also common in some commercial applications.

In the output port of the calibration processor, there is another clock domain interface existed. The low-speed signal T[k'] controls the offset of the comparator that operates at full speed. Offset adjust has to be completely settled before next comparison is activated. This requirement becomes more stringent especially when many bits of T[k'] transit at the same time. To avoid complex phase alignment structure, an equally weighted offset adjustment is used to eliminate the spike caused by multi-bit transition. Since the calibra-

tion loop definitely increases or decreases offset by one fixed value $\Delta V$ a time, the phase alignment structure is of no necessary if the equally weighted offset amount is set to $\Delta V$. Even that the adjustment transition happens within the comparison period, its effect will be always less then $\Delta V$, which is 1/4 LSB and can be neglected.

The random sequence q[k] changes it value synchronously with the calibration clock. However, the chopper controlled by q[k] switches in high-speed signal path. Hence the timing of q[k] is set at the resolution of the conversion clock. A register driven in the conversion speed is used to re-latch q[k] and is put distributively in each BCC for this purpose.

### 4.3.2 Chopper Settling Issues

The analog chopper in the input port of the BCC is composed of 4 P-type MOSFET switches. To address the settling issues when chopper is activated, the q[k] timing together with the chopper on-resistance, the resistance of the resistor string and the comparator input capacitance have to be taken into consideration.

The transition of q[k] should be put at the very beginning of the comparator reset phase to provide longest settling time when chopper switched. This is accomplished by give a clock ahead of the conversion clock by one inverter delay to drive the register which is used to re-latch the q[k] in each BCC.

When the chopper is toggled by q[k], the settling error is illustrated in Fig. 4.5. Fig. 4.5 is a simplified single-ended case. As the chopper swaps the signal path, the capacitance in node $V_p$, including the input capacitance of the comparator and the parasitic capacitance of the wires, is discharging from the input level to the reference level by the resistor string. The reference node $V_r$ itself is also discharged. On the other hand the capacitance in node $V_n$ is discharged from the reference level to the input level by the input network.

The discharging for $V_p$ is mostly slower than that for $V_n$, since the equivalent input resistance is two parallel connected termination resistor which is mostly smaller than the equivalent resistance look by the node $V_r$. In addition, the discharging for either $V_p$ or $V_n$ depends on the reference level and the input signals. In general, the discharging is faster for comparators located near the end than for those located in the middle.

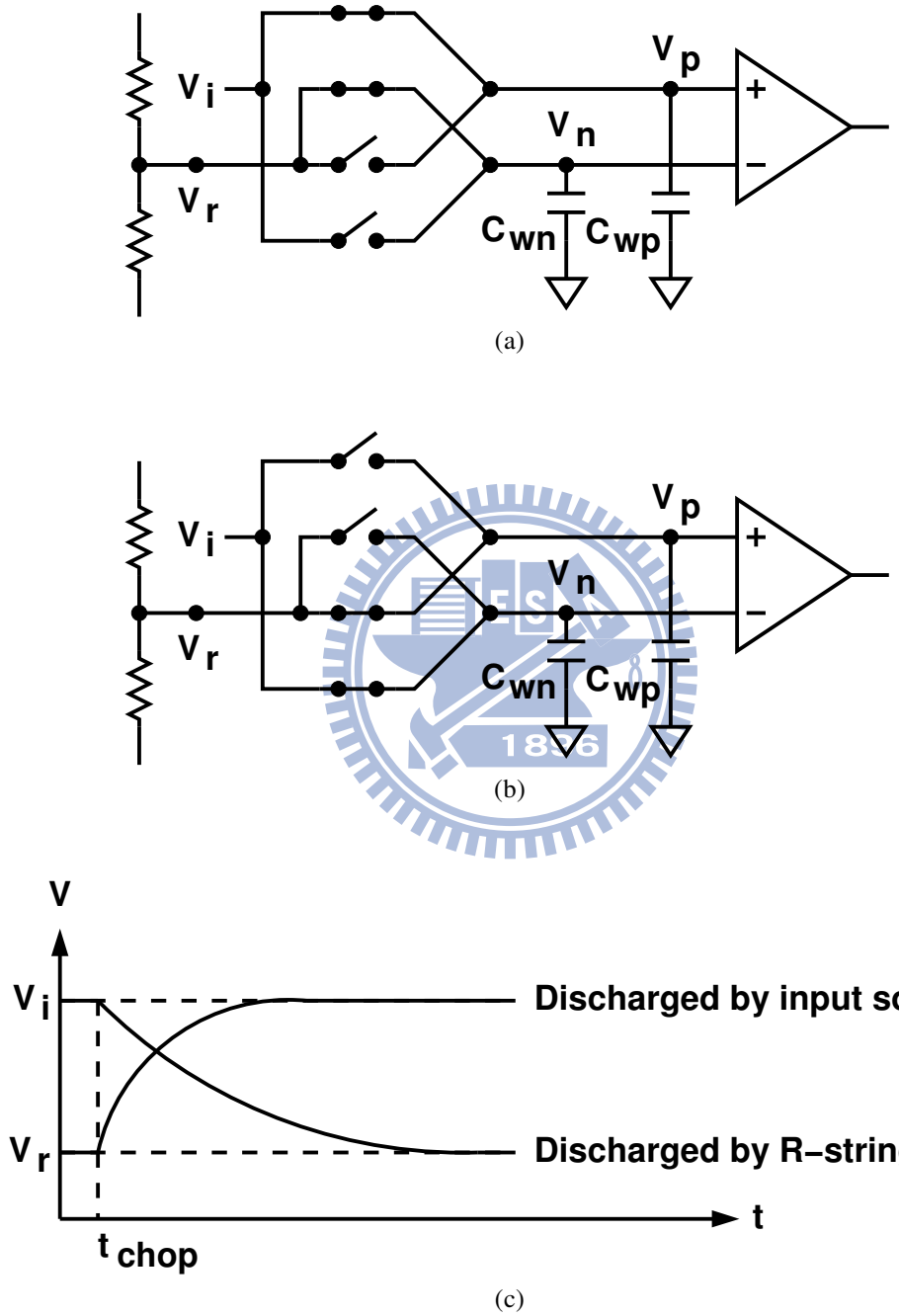



Figure 4.5: Settling issue for chopper switching: (a) before chopper swaps the signal path; (b) after chopper swaps the signal paths; (c) the waveform at nodes $V_p$ and $V_n$.

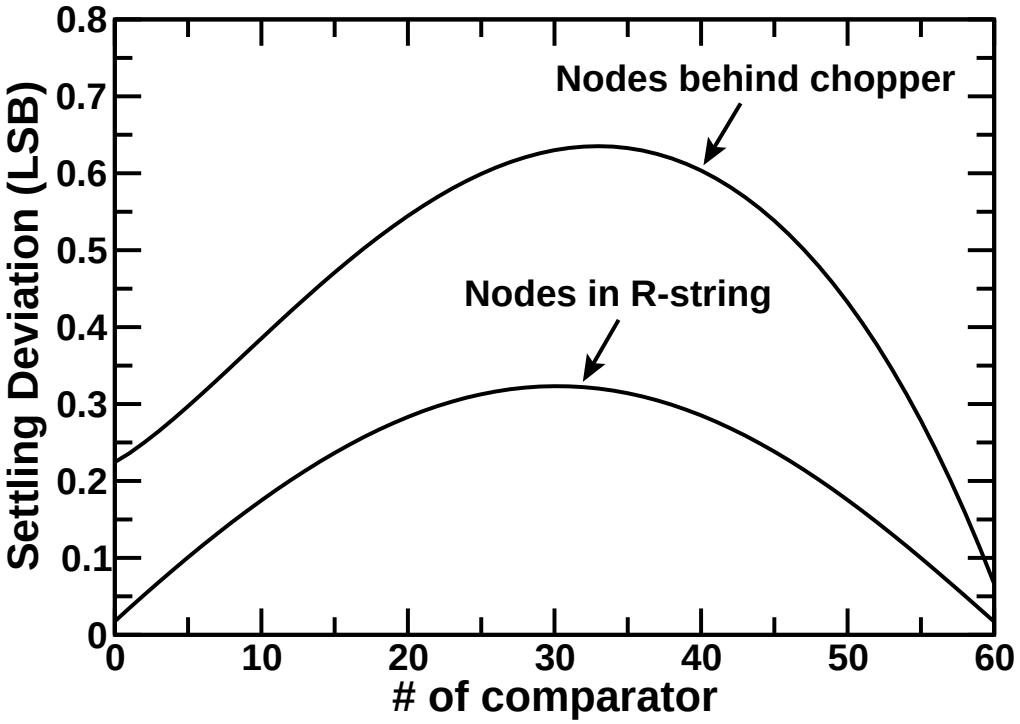



Figure 4.6: Simulation results for settling error.

Notably, in the worst case, all choppers may swap the signal path at the same time, thus the resistor string has to discharge the capacitance at all comparator input nodes. If the discharging is not completed at the end of the reset phase, it will degrade the INL of the ADC.

In the differential operation, $j^{th}$reference node is connected both to the inverting input node of $j^{th}$comparator and to the non-inverting input node of (62-j) $^{th}$ comparator. This complicates the discharging condition. However, in this case, to deduce an analytical form to represent the settling voltage on input nodes is trivial and not necessary. In our design, the settling for the comparator input nodes are verified by post-layout simulation for the worst case. Fig. 4.6 is the simulation result.

The X axis is the comparator index. The Y axis is the deviation from the nominal reference level at the end of comparator reset phase. It is normalized to one LSB. The

parasitic capacitance on wires is also included in the simulation. Fig. 4.6 only shows the case for discharging from input level to reference level. The opposite case for discharging from reference level to input level is much smaller and can be neglected.

There are two curves in Fig. 4.6. For the reference nodes, the slowest settling falls in the middle. This is because the equivalent resistance look into the resistor string has maximum value in the middle node. The settling for the nodes behind the chopper is worse than the reference nodes due to the on-resistance of the chopper. The worst-case deviation for the nodes behind the chopper is 0.65 LSB, which is lower than 1 LSB.

### 4.3.3 Power-Efficient Latch

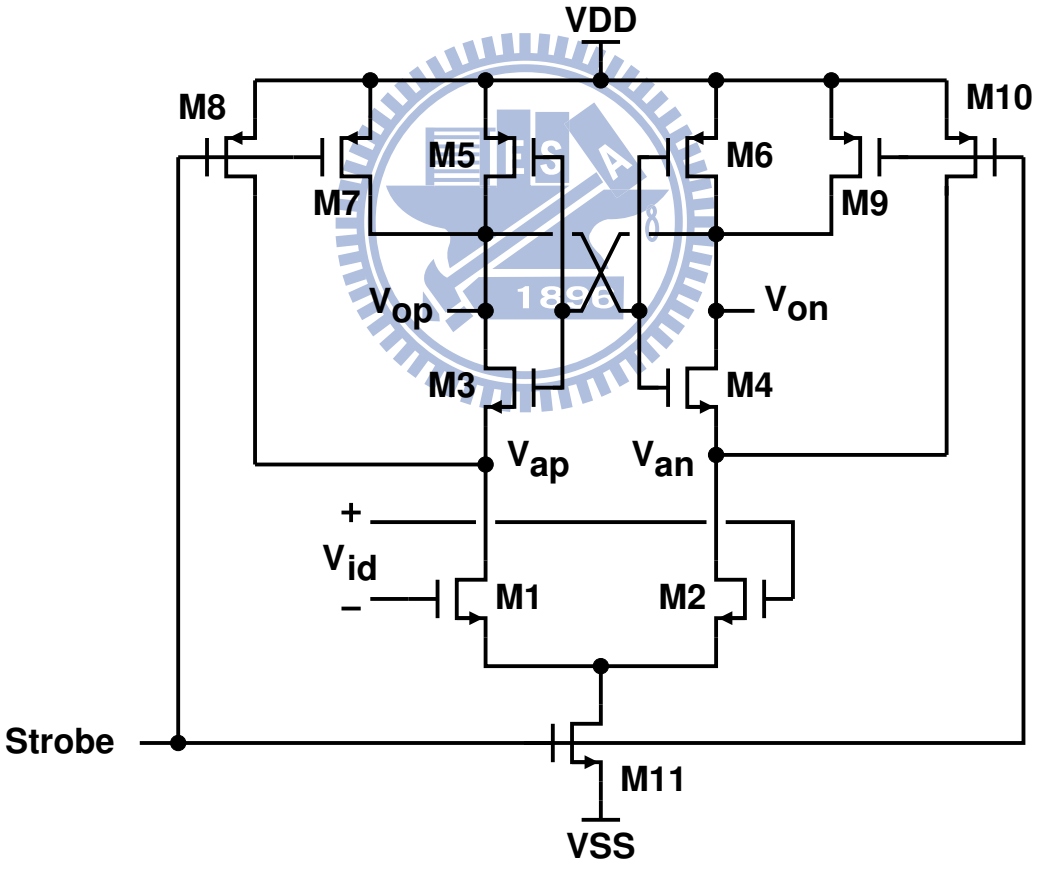



Figure 4.7: Circuit of the power-efficient latch

The selected latch architecture for BCCs is shown in Fig. 4.3.3. The operation of the latch can be divided into 2 phases: reset phase and comparison phase. In reset phase, the

strobe signal stays low, such that the lower source couple pair and the upper regenerative loop are both inactive because M11 is turned off. Output nodes $V_{op}$, $V_{on}$ and intermediate nodes $V_{ap}$, $V_{an}$ are all pulled to $V_{DD}$ by M7-M10. No DC current flows through the latch.

As the strobe signal is pulled high, the latch transfers from reset phase to comparison phase. At the beginning, the source-couple pair formed by M1 and M2 is saturated and pull the nodes $V_{ap}$, $V_{an}$. As $V_{ap}$ and $V_{an}$ fall to $V_{DD}$-$V_{tp}$, $V_{op}$ and $V_{on}$ are also pulled through M3 and M4. At the same time, unidirectional positive feedback loop formed by M3 and M4 starts to enlarge the difference between $V_{op}$ and $V_{on}$.

As $V_{op}$ and $V_{on}$ are also fall to $V_{DD}$-$V_{tp}$, a full positive feedback loop formed by M3-M6 strongly divide $V_{op}$ and $V_{on}$ to a rail-to-rail level. As the rail-to-rail output voltage is settled, either M3/M6 or M4/M5 are turned off, hence the intermediate nodes $V_{ap}$ and $V_{an}$ are also discharged to ground by M1, M2, and M11 and no DC current flow through the latch neither.

The discharging during comparison phase depends on the input signal $V_{id}$. Fig. 4.8 illustrates the output waveform corresponding to various $V_{id}$. Small $V_{id}$ may cause a small difference on output voltage and introduce a metastable condition.

This analog latch circuit requires no DC bias either in reset or in comparison phase. Only small dynamic power is consumed during the probe signal transition, thus the latch is very power efficient.

The comparison speed of the analog latch is analytically described by (4.2)[43]

$$t_d = \frac{2C_L V_{thp}}{I_{d,M11}} + \frac{C_L}{g_{m,eff}} \ln\left[\frac{1}{V_{thp}}\sqrt{\frac{I_{d,M11}}{2\beta}}(\Delta V_o - V_{thp})\right] \tag{4.2}$$

Where $t_d$ is the delay from the beginning of comparison phase to the instant at which one of the output nodes reaches a specific voltage $V_o$. $C_L$ is the capacitive load in one output node. $I_{d,M11}$ is the drain current of M11. $\beta$ and $g_m$ represent the current factor and the effective transconductance of M3-M6, which are assumed in the same size. $V_{thp}$ is the threshold voltage of P-type MOSFET. $V_{id}$ is the input differential voltage.

According to (4.2), the transistor current factor $\beta$ is within the logarithmic function. Hence the transistor sizing only has quite low influences on the latch speed except for the size of M11. $I_{d,M11}$ is decided by both the size of M11 and the input common-mode level. If the current of the tail branch is confined to a fixed value, the effect of M11 sizing and

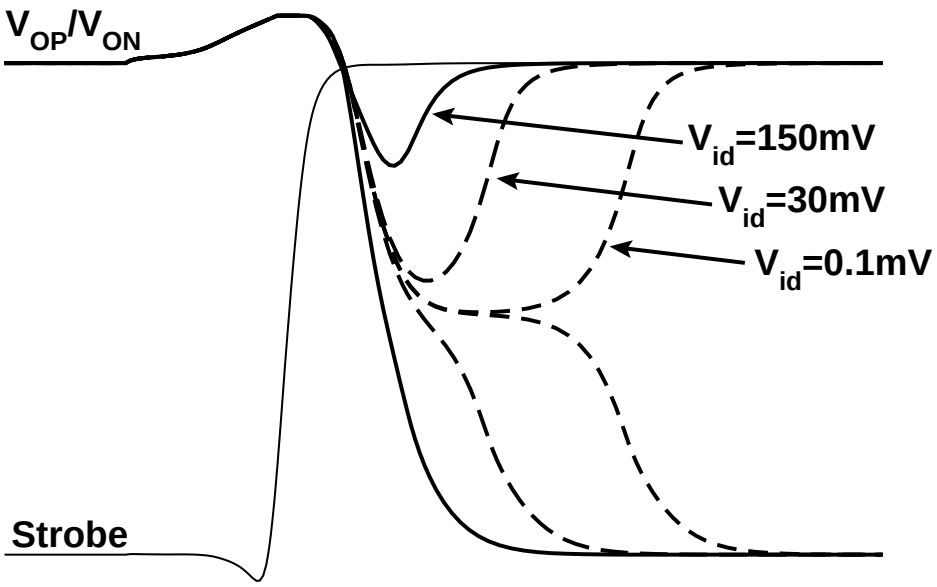



Figure 4.8: Waveforms of the latch

the input common-mode level is eliminated. In our design, all transistors except M11 are set to the same size. M11 is double sized of the others for faster settling.

Two digital latches are put behind this analog latch circuit to retain output values in reset phase. Due to the positive feedback operation, this analog latch circuit is very sensitive to the capacitance in output nodes. Because the gate capacitance of the following digital latches depends on its state, state-dependent input offset voltage on the analog latch will be introduced. This results in hysteresis condition. To avoid the hysteresis condition, two inverters are put between the output port of the analog latch and the input port of the digital latch.

The disadvantage of this analog latch is that it is very sensitive to input common-mode level. Variation on input common-mode level changes the gain of the lower source-couple pair, thus changes its input referred offset voltage and its latching speed. This circuit

architecture is suitable only for the $2^{nd}$ and $3^{rd}$ stages in the BCC circuit.

### 4.3.4 Latch Circuits for $2^{nd}$ and $3^{rd}$ Stages

The complete circuits for $2^{nd}$ and $3^{rd}$ stages are shown in Fig. 4.9. Digital latches for $2^{nd}$ stage are simply transmission gates. The transmission gate passes the signal at the comparison phase of the $2^{nd}$ stage and the reset phase of the $3^{rd}$ stage. At the reset phase of the $2^{nd}$ stage and the comparison phase of $3^{rd}$, the transmission gate breaks the signal path to hold the input voltage at the $3^{rd}$ input stage.

Behind the $3^{rd}$ stage is the bubble-insensitive thermometer-code-edge detector(BITCED), which is composed of 3-input NAND gates to locate the 0-to-1 transition of the output code from the comparator array. The outputs of BITCED is used as the word line of a ROM decoder. When metastability happens, it is possible that none of the 3-input NAND gates has an output of 1. In this case, no word line is selected and the ROM encoder will output an maximum value that corrupts the ADC performance. To avoid the all-zero-output condition for BITCED, both output nodes of the $3^{rd}$ latch has to keep high in metastable interval. After the comparator reaches the definite state, one of the output nodes is pulled low and the final output code is decided[25].

A clock-less SR latches behind the $3^{rd}$ latch stage is used for date latching and to prevent the all-zero-output condition in BITCED. Fig. 4.10 shows the SR latch with its output waveform. In Fig. 4.10, $V_{ip}$ and $V_{in}$ come from the analog latch and are both high in the reset phase. At this time the SR latch keep its output value in previous state. As the analog latch enter the comparison phase, one of $V_{ip}$ and $V_{in}$ will be pulled low and the other still keeps high. If it is different from the previous state, the output node of the SR latch corresponding to the pulled-low input is pulled high at first. After a propagation delay of the NAND gate, the other output node is pulled low. Hence the all-zero-output condition never happens in the output nodes $V_{op}$ and $V_{on}$, and nor does it happen in the BITCED output.

In metastable condition of the analog latch, both $V_{ip}$ and $V_{in}$ voltage may stay in a intermediate value. The transition point of the NAND gate has to keep below this intermediate value by appropriate transistor sizing so that the NAND gate will not turn its state

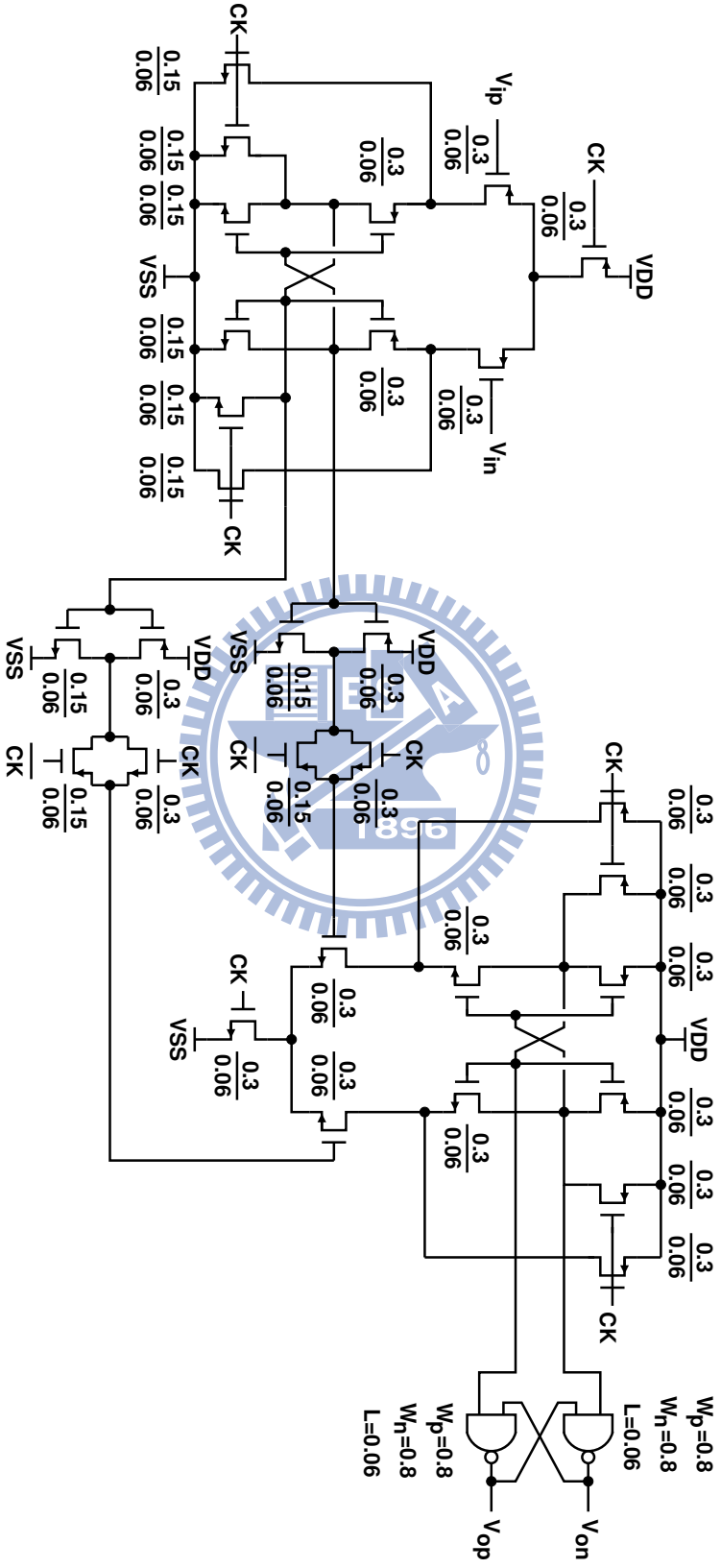



Figure 4.9: The complete $2^{nd}$ and $3^{rd}$ latch circuit.

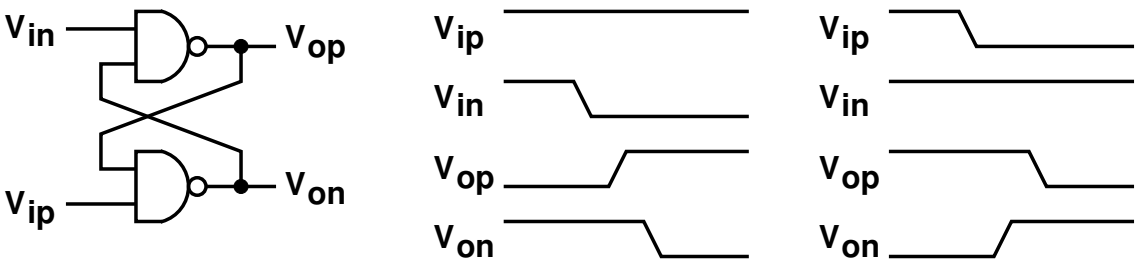



Figure 4.10: SR latch and its waveforms

in the metastable interval. It spends two propagation delay of NAND gate for the SR latch to settle to the final value, thus the comparison speed is slower than the $2^{nd}$ stage. The SR latch is directly connected to the output nodes of the analog latch, thus introduces a hysteresis transition. Both the longer delay and the hysteresis transition can be neglected due to the large over-all gain provided by the preceded cascade latch stages.

### 4.3.5 Latch Circuit for $1^{st}$ Stage

The $1^{st}$ stage of the BCC circuit requires fully-differential operation and offset control mechanism. High common-mode rejection ability is essential for its fully-differential operation to suppress the common-mode noise, which may be severe due to electromagnetic interference and power noise. The offset control mechanism is for offset trimming in the background calibration loop. Hence the latch circuit for the $1^{st}$ stage is configured as Fig. 4.11.

Two source-couple pairs are connected in parallel to drive the positive-feedback loop. This structure facilitates fully-differential operation. A cascade MOSFET in added at the tail branch of each source-couple pair to reduce the sensitivity of input common-node level, since the current flowing through each source-couple pair is limited to roughly the same regardless of their common-mode levels.

The variable input offset voltage is achieved by tuning the loading and pulling strength on nodes $V_{a1}$ and $V_{a2}$[44]. This is done by 16 tiny n-type MOSFET capacitors and 4 weak pulling current sources. Capacitors are responsible for the fine control, and current sources are responsible for the coarse control.

The coarse and fine calibration are managed by the calibration sequence in power-on

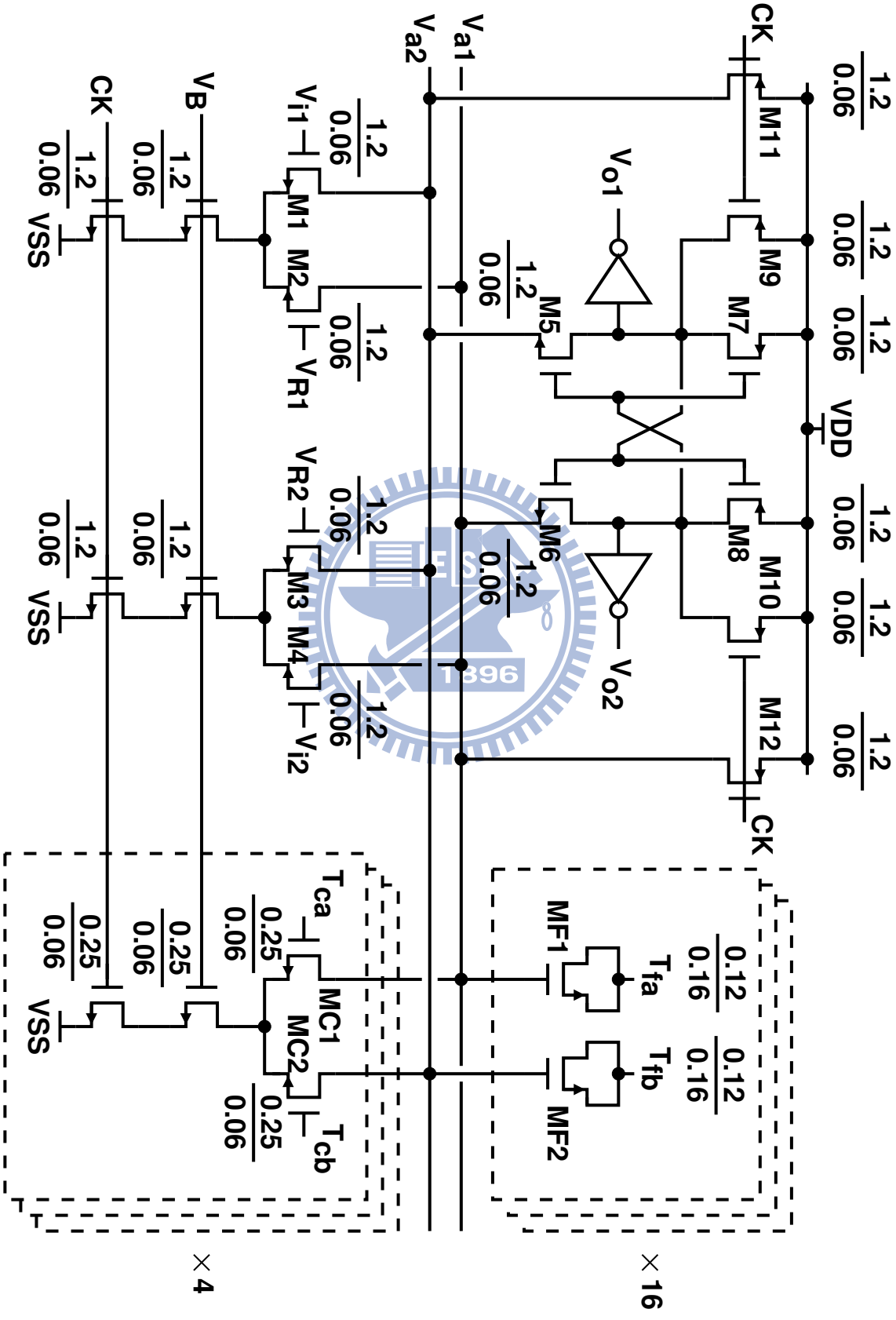



Figure 4.11: The 1$^{st}$ stage latch in the BCC

state and during normal operation. Coarse control is applied only in power-on calibration. After that, the fine control is applied to zero the initial comparator offset. Then the ADC enter background calibration mode with only the fine control.

In fine control, gate nodes of N-type MOSFET capacitors are connected as top plates, and source and drain nodes are controlled by digital gates. When source and drain nodes are pull high, the MOS channel is diminished and thus the $C_{OX}$ steps down. When source and drain nodes are pull low, the MOS channel is established and thus $C_{OX}$ steps up. The variation of $C_{OX}$ gives a fine tuning interval for the BCC offset. The gate node as top plate avoids the addition of large diffusion capacitance on source and drain nodes.

In coarse control, a source-couple pair, which is similar to the input pair but is constructed with smaller transistor sizes, provides a weak pulling strength at the strobe rising instant. This makes a deviation on input offset voltages of BCCs.

It is important to estimate the comparator input offset voltage so that a proper cover range for the offset control can be given. With the voltage gain provided by the $1^{st}$ latch stage, the input-referred offset amount of the $2^{nd}$ and the $3^{rd}$ stages can be neglected. Only the offset amount contributed by the $1^{st}$ stage is considered.

A Monte Carlo simulation with an offset search loop is applied to estimate the offset variance. The offset search loop is composed of the latch net list and a binary search block written by behavioral circuit element. The binary search block is illustrated in Fig. 4.12. The standard deviation of the offset voltage is obtained from 100 runs of the binary search. In each run, the device parameters of the latch circuit is updated according to the mismatch model provided by the foundry.

To eliminate the possible effect of the hysteresis, there are two comparisons in each transient analysis. For the first comparison, the comparator input is given the most(or the least) value of the swing range to set the output to 1-state(or 0-state). For the second comparison, the comparator input is given the calculated value for search process. Double comparison assures the output of each search step is obtained behind the same state and thus no hysteresis factor is involved in the search process. Using the simulation methodology, the standard deviation of the comparator offset voltage is 27.1mV.

The hysteresis itself is also verified by the search process shown in Fig. 4.12. The hysteresis interval, which is the difference between the offsets obtained from a preceded 1-

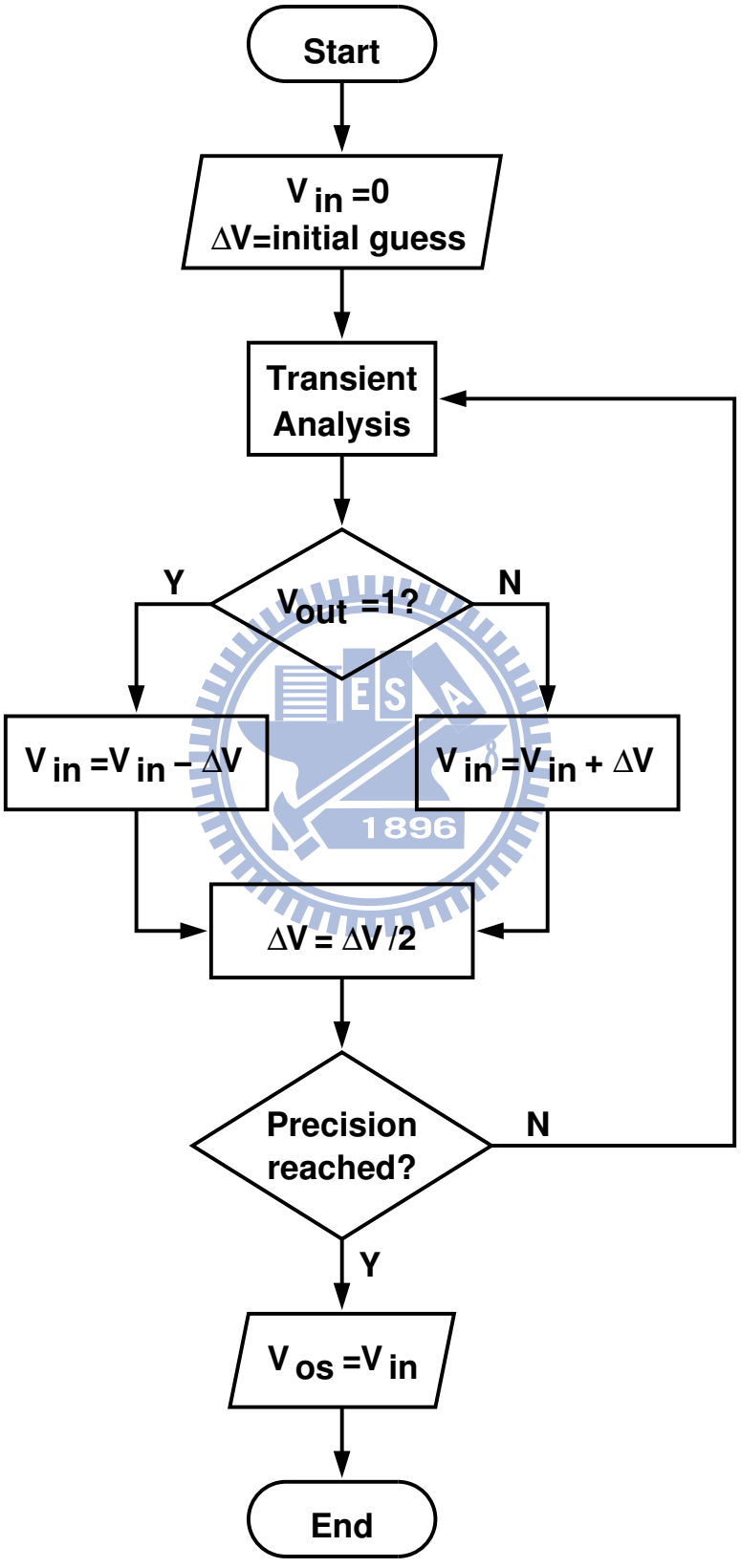



Figure 4.12: Binary search process for offset extraction

Table 4.1: Codes for coarse offset control

| $T_{ca}$ | 0000 | 0000 | 0001 | 0001 | 0011 | 0011 | 0111 | 0111 | 1111 |
|---|---|---|---|---|---|---|---|---|---|
| $T_{cb}$ | 1111 | 1110 | 1110 | 1100 | 1100 | 1000 | 1000 | 0000 | 0000 |
| Offset dev.($\Delta V$) | -4 | -3 | -2 | -1 | 0 | 1 | 2 | 3 | 4 |

state and from a preceded 0-state. By the simulation methodology, the hysteresis interval for the comparator is less than 0.01 LSB, which can be neglected.

To get rid of the offset voltage, the offset adjustment range has to cover 6 times of this standard deviation, which is equal to 81.3mV. However, the comparator offset itself depends on the offset control circuitry, hence a recursive simulation is required to get a well-designed latch comparator.

### 4.3.6 Offset Control

Fig. 4.3.6 is the circuit for the coarse offset control.

In Fig. 4.3.6, each tuning pair provides three possible offset deviations: $-\Delta V$, 0, and $+\Delta V$. To obtain uniform control steps over the whole control range, the control codes are arranged as Table 4.1.

At the middle point of the control range, half of the tuning pairs are switched to the left and the others are switched to the right. This arrangement makes the averaged pulling strength the same value over the whole control range, thus the offset control step in the most positive or negative end is the same as in the middle point.

In a BCC, the input codes to the ACC block(Fig. 4.4) is +1, 0 or -1. As discussed in p.54, with an equally-weight offset adjustment, this accumulation resembles the operation of a bidirectional shift register. A shift register with specialized logics shown in Fig. 4.14 is used as the ACC block to control the offset voltage.

To obtain the finest control step, each ($T_{ca}$, $T_{cb}$) pair changes to (0,1), (0,0), (1,0) in turns during register shifting. To reset the shift register is to set one half of ($T_{ca}$, $T_{cb}$) pair to (0,1) and the other half to (1,0) as the offset control midpoint.

The code arrangement and the shift register for the fine offset control are operated in the same way as the coarse offset control.

Fig. 4.15 illustrates the simulation results of the offset control. For the coarse control,

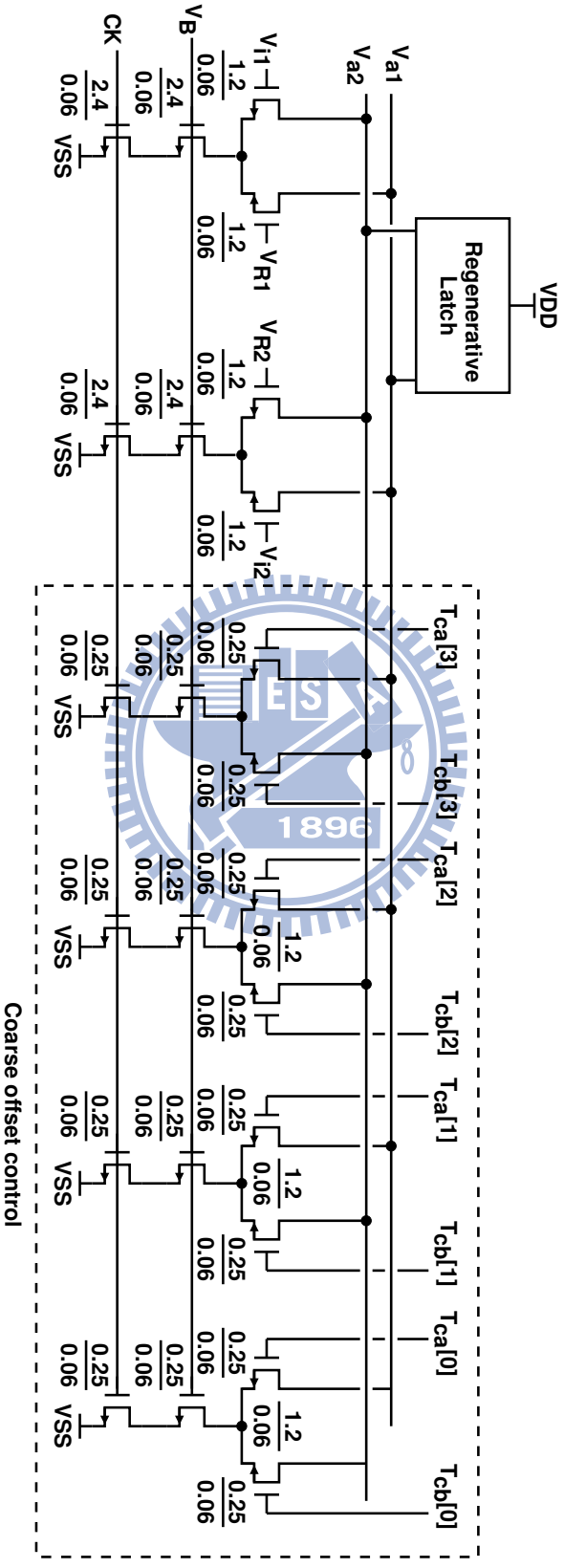



Figure 4.13: Circuits for coarse offset control in the 1$^{st}$-stage latch.

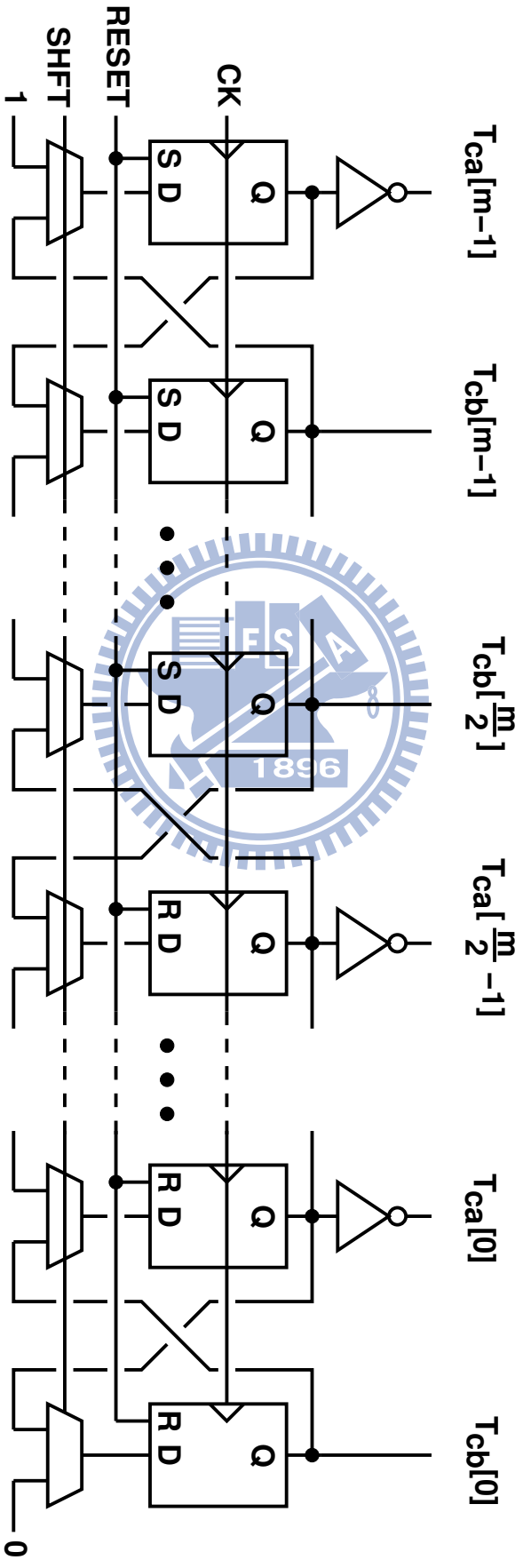
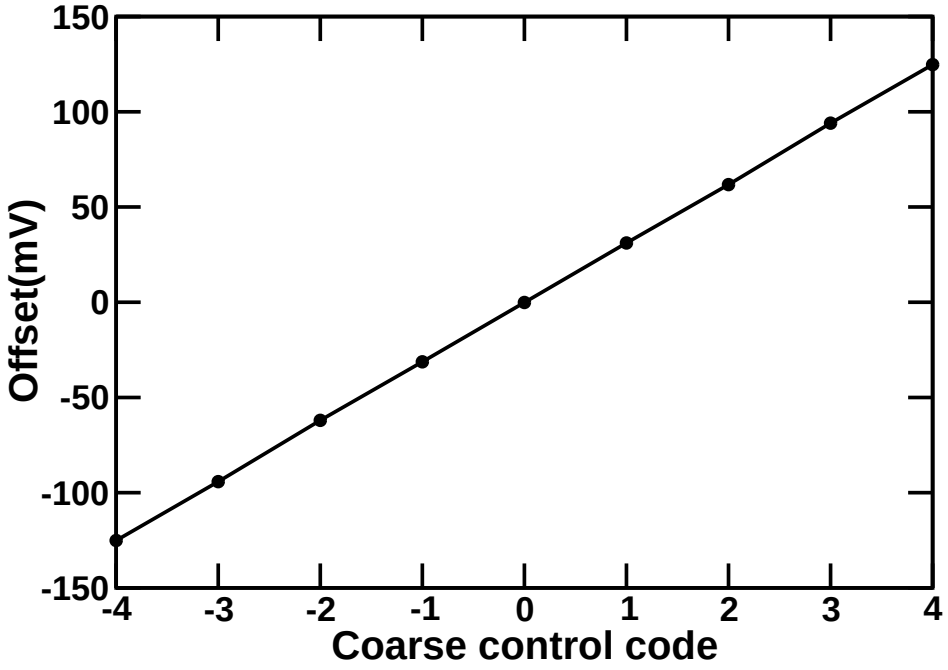
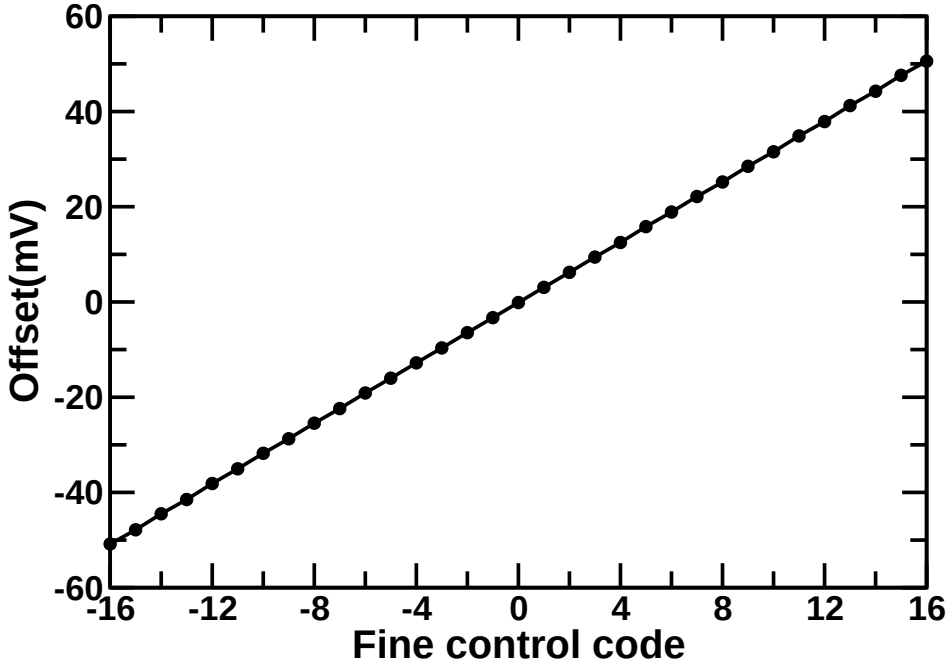



Figure 4.14: Shift register used in ADC calibration

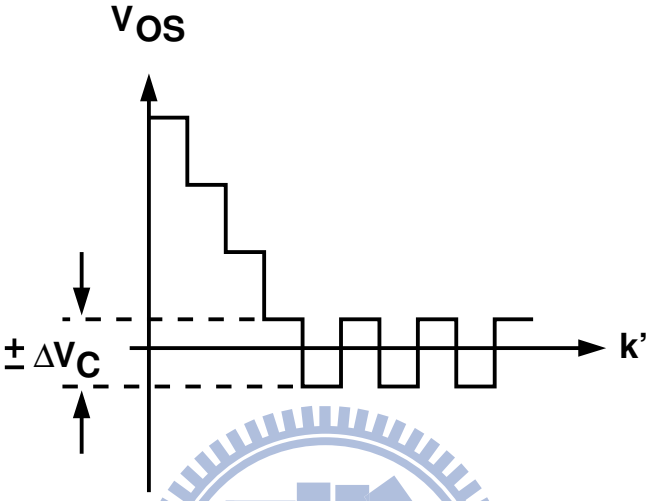



(a)

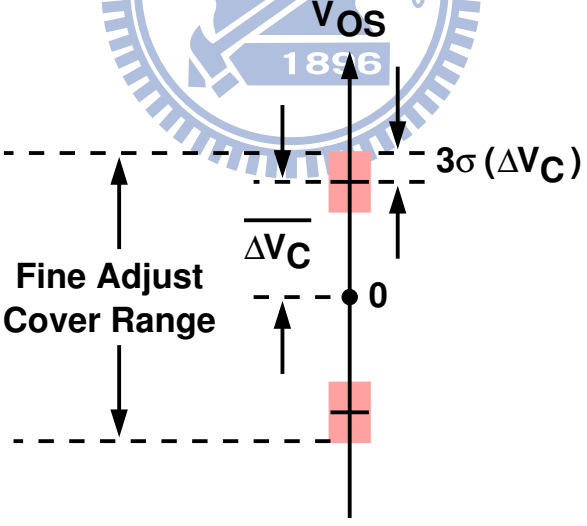



(b)

Figure 4.15: Simulation results for offset Adjustment: (a) coarse control; (b) fine control.




(a)




(b)

Figure 4.16: (a) Offset residue after the coarse calibration complete; (b) required cover range for fine control.

one offset step $\Delta V_c$ is 32 mV. With $\pm 4\Delta V_c$, the coarse control cover an offset deviation of $\pm$128 mV, which is larger than $\pm 3\sigma_s(V_{OS})$= $\pm$81.3mV.

To decide the cover range for the fine offset control, the issue for the coarse control step variation has to be addressed. As the waveform shown in Fig. 4.16a, after the coarse calibration is completed, at worst, a residual $\pm\Delta V_c$ may appear as the input offset voltage. The CMOS process may also cause a variation in $\Delta V_c$. The standard deviation of $\Delta V_c$ is 3mV from Monte Carlo simulation. Thus the fine offset control has to be designed to cover a range larger than $\pm[\Delta V_c + 3\sigma_s(\Delta V_c)]$, which is shown in Fig. 4.16b and is equal to $\pm$41mV. In out design, $\Delta V_f$ is set to 3.154mV for a fine step. With $\pm$16 steps, cover range of the fine control is $\pm$50.5mV, which is larger than $\pm$41mV.

With the ADC input swing range set to $\pm$0.4V, $\Delta V_f \approx$ 1/4 LSB. This is consistent to the selected calibration parameters discussed in p.47.

## 4.4 Back-End Encoder

The back-end encoder is shown in Fig. 4.17. A NOR-type ROM encoder is used to generate Gray codes. Operation of the ROM encoder is divided into two phases which occupy half one clock cycle individually. In first half of the clock cycle, upper P-type MOSFETs are activated by $\overline{CK}$ to pre-charge the output nodes. Meanwhile, all N-type MOSFETs with their drain connected to the output nodes are turned off. In the second half of the clock cycle, upper P-type MOSFETs are turned off and the N-type MOSFETs is activated by the word lines to discharge the corresponding output nodes. The gate nodes of these N-type MOSFETs are the word lines of the ROM encoder. Output codes are obtained from the inversion of the output nodes.

The word line driven signals $D'_e[1:63]$ are the latched and gated $D_e[1:63]$, which are the output of the BITECD. The gating of $D_e[1:62]$ are achieved by a 2-input NOR gate and is controlled by the clock signal connected to $CK$. Gating is to inhibit the effect of $D_e$ on the word line of the ROM encoder at the pre-charging phase.

The pattern of the N-type MOSFET is arranged according to Gray codes, with which only one bit transition is allowed for neighboring code values. Use of Gray code is to

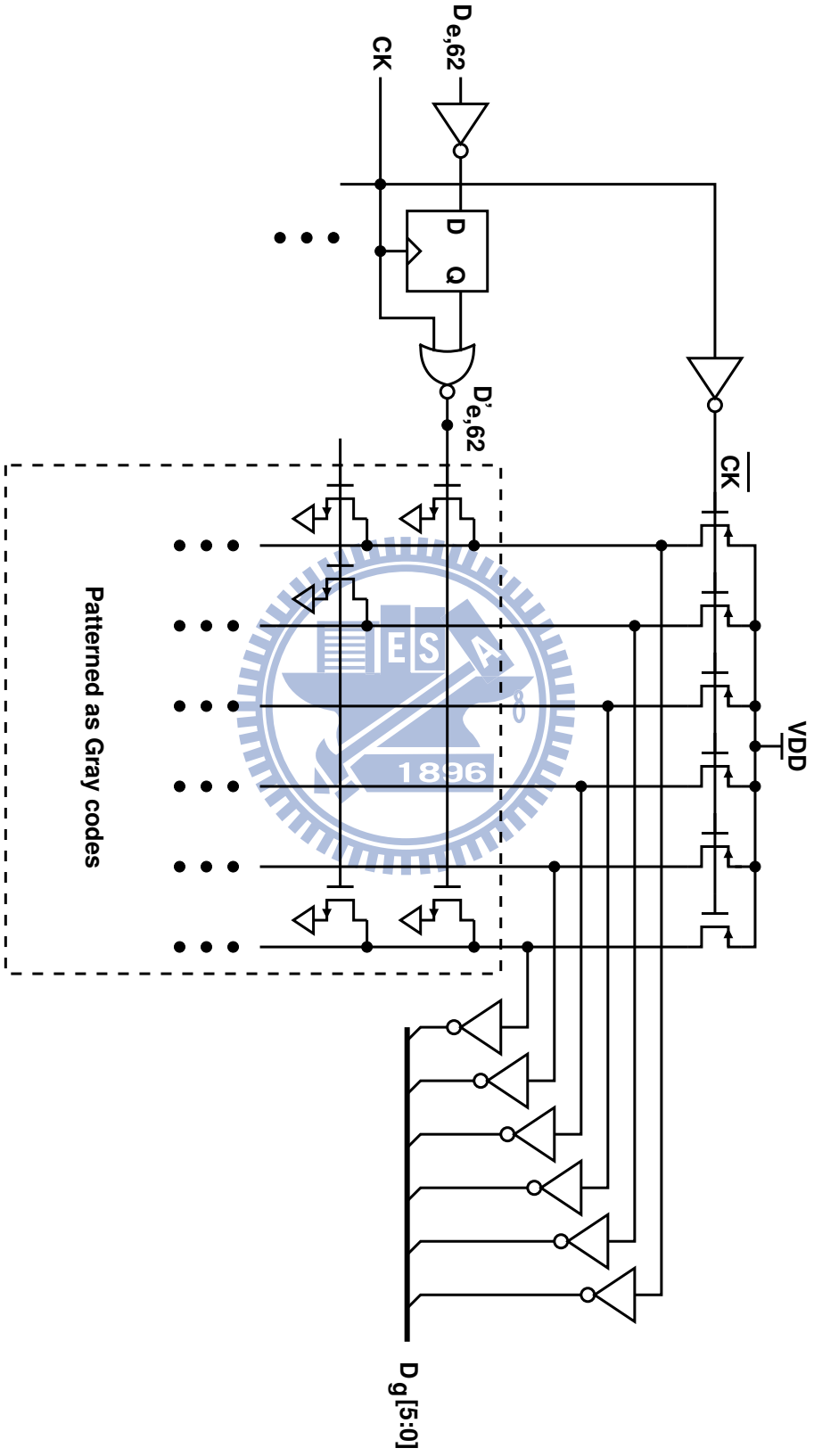



Figure 4.17: Block diagram of the back-end encoder

mitigate the effect of bubble. In case that some bubbles exist in the thermometer codes, there may be more than 1 bit of the edge code $D_e[1:63]$ having the value of 1. This kind of edge code will activate multiple code patterns in the ROM, and the output code becomes the OR operation of these code patterns. The OR-operated code patterns will cause severe error in the output codes if the N-type MOSFETS are patterned in binary fashion. Since bubbles in thermometer code are usually located near the 0-to-1 edge, the corresponding activated code patterns in the ROM is also closed to each other. If the N-type MOSFETs are patterned according to Gray code, the bit value difference of these code patterns are very small, and their OR operation only cause minor errors in the output codes[24].

The output Gray codes are then decimated by 64 and encoded again into binary codes to facilitate the fetching of the logic analyzer.

## 4.5 Other Building Blocks

The random sequence $q[k]$ is generated from a 14-bit pseudo random number generator(PRNG). The $7^{th}$ bit of the generated random number is used to chop even-numbered BCCs, and the $14^{th}$ bit is used to chop the odd-numbered BCCs[45] The PRNG operates in 1/64 of the conversion speed which is synchronous with the calibration processor. Since the BITCED is composed of 3-input NAND gates, it is more proper to use 3 independent random sequences to avoid upward lock. However, the use of 2 random sequences are still applicable if the swing range of input signal covers the reference level of the upmost comparator.

There are two clock frequencies used in the whole chip. These clocks are divided into 5 clock domains. The first domain is for the conversion clock, which is the fastest clock that operates in 2GHz. Buffers for the conversion clock consume about 1/3 to 1/2 of the total power consumption, hence are carefully layout with separated power wires.

The second and the third clock domains are for the calibration processor and the PRNG. Both the two clocks are generated from the conversion clock divided by a 8-bit ripple counter. Output of this ripple counter is re-latch by the conversion clock for phase alignment and then fed to two multiplexed delay line. One of them is for calibration pro-

cessor and the other is for PRNG. Both clocks are the same except that their phased can be adjusted independently.

The fourth clock domain is for output code decimation. The decimation clock frequency is also 1/64 of the conversion clock. In addition to phase adjustment, the decimation clock have conversion clock latency control. The phase difference of the decimation clock and the PRNG clock can be set to 6 or 7 periods of the conversion clock. This option is to verify the settling issue when chopper switching. Because the cascaded lathes in the BCC and the following pipelined register for decoding, output code corresponding to some chopper state will be delay 6 conversion clock cycles. If the decimation clock latches the output data with other than exactly 6 conversion clock latency, the settling problem will never be observed if it exists.

The fifth clock domain is for an internal finite-state machine(FSM). This FSM interprets the control sequences from the serial port mentioned in p.4.6.1. Since this FSM clock should not configure its own phase or latency, this clock is directly divided from the conversion clock. There is not any adjustment option for it.

## 4.6 Chip Measurement

### 4.6.1 Setup

Fig. 4.18 is the micrograph of the fabricated ADC chip. Using the low power 65nm CMOS process technology, the active area is 0.21x0.66 $mm^2$.

The setup for chip measurement is shown in Fig. 4.19. The input signal and the clock signal are both generated from RF signal generators, and then split into differential signals by 180° RF power splitters. The PCB traces for the two signals are carefully drawn to keep them as symmetric as possible for differential operation. Impedance control is also applied when manufacturing the PCB to assures the impedance matching for transmission lines. The chip is directly mounted in the PCB and all pads on the chip are bonded to a predefined copper pattern on the PCB by golden wires.

The required power sources are provided from a separated PCB board. These power sources are made of discrete OPAMPs and power transistors. There is a PCI socket on the

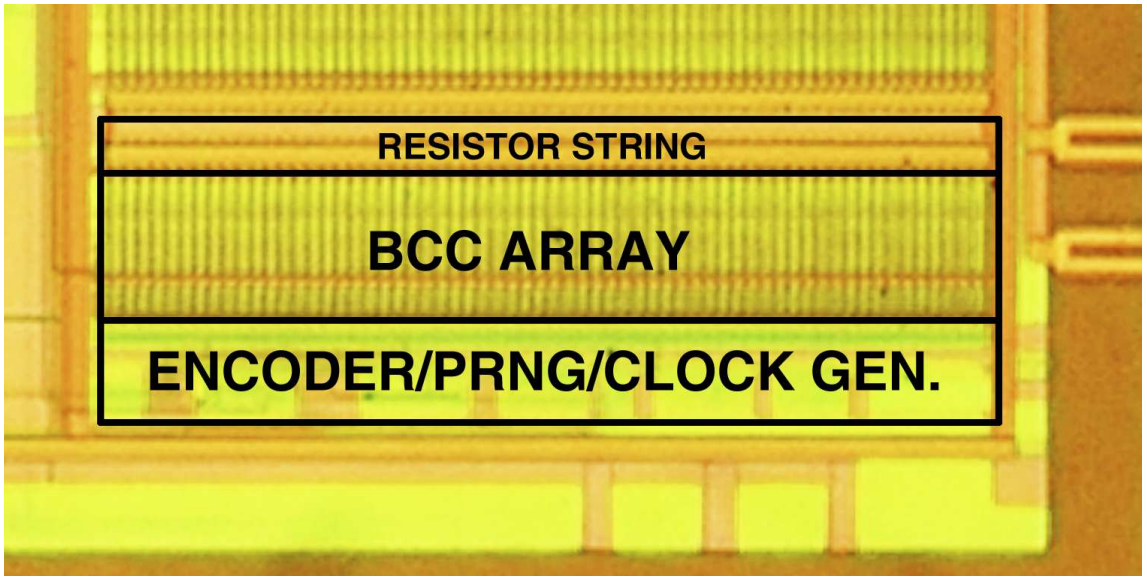



Figure 4.18: Micrograph of the implemented circuit die

edge of the power board. In the corresponding edge of the chip board, a PCI plug with golden fingers are profiled. The power board and the chip board are connected through this PCI interface so that chip under test can be fast set up. The required reference sources and bias sources are also supplied from the power board. All voltage sources are adjustable by a high resolution potential pot. At least 4 decoupling capacitors with different order of capacitance is put as near the chip as possible in the chip board for each power/reference/bias source pins.

Output digital bus together with the low-speed clock signal from the chip are also bridged to the power board. A logic analyzer is used to fetch the output codes for further analysis in PC.

For measurement configuration, a specialized control port that is composed of a 2-bit serial bus is used to send control sequences. The control sequence is sent from the PC printer port. The interface circuit for the printer port is also put in the power board, and the serial bus is bridged to chip board by the same PCI interface.

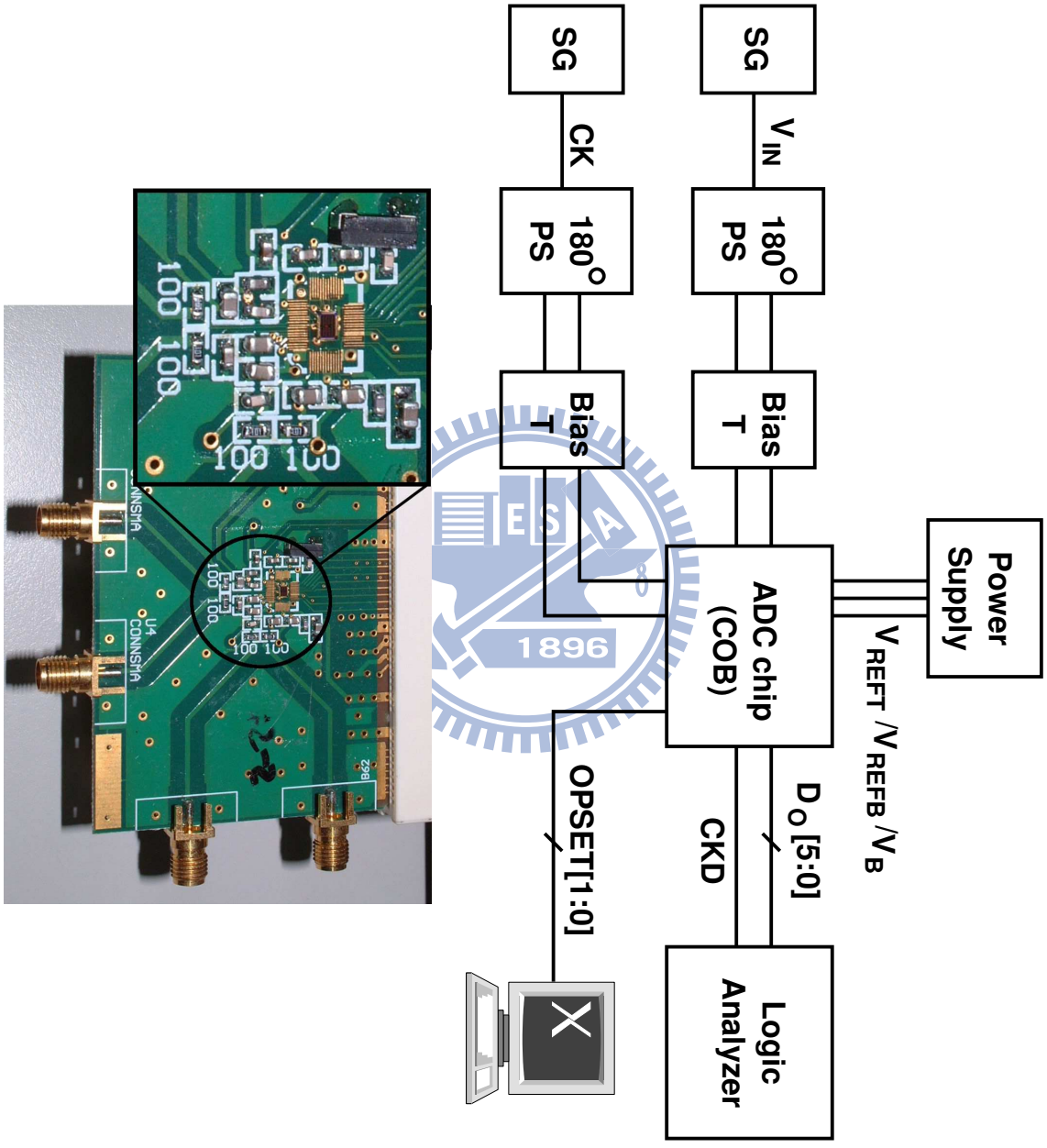
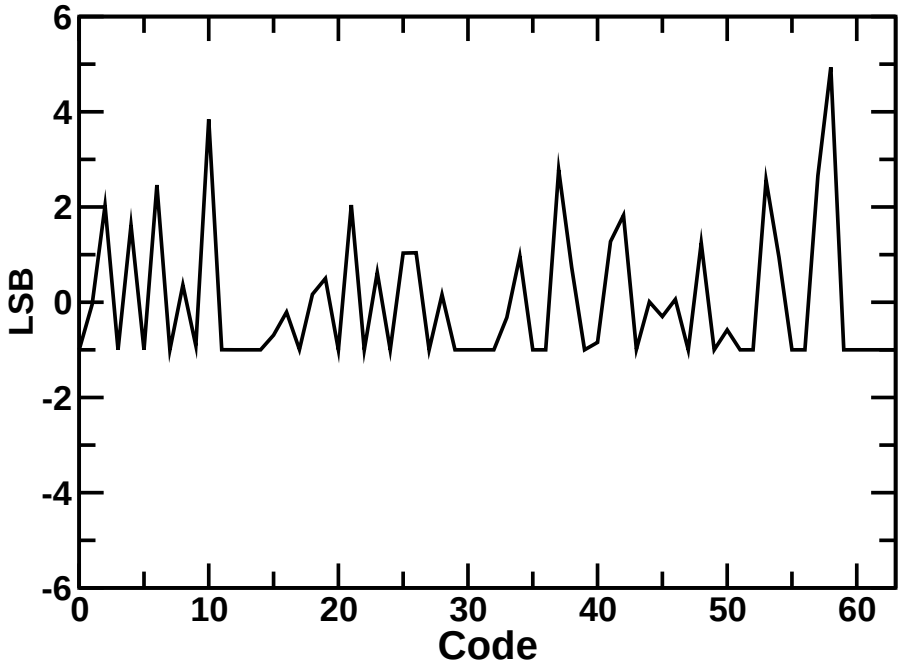
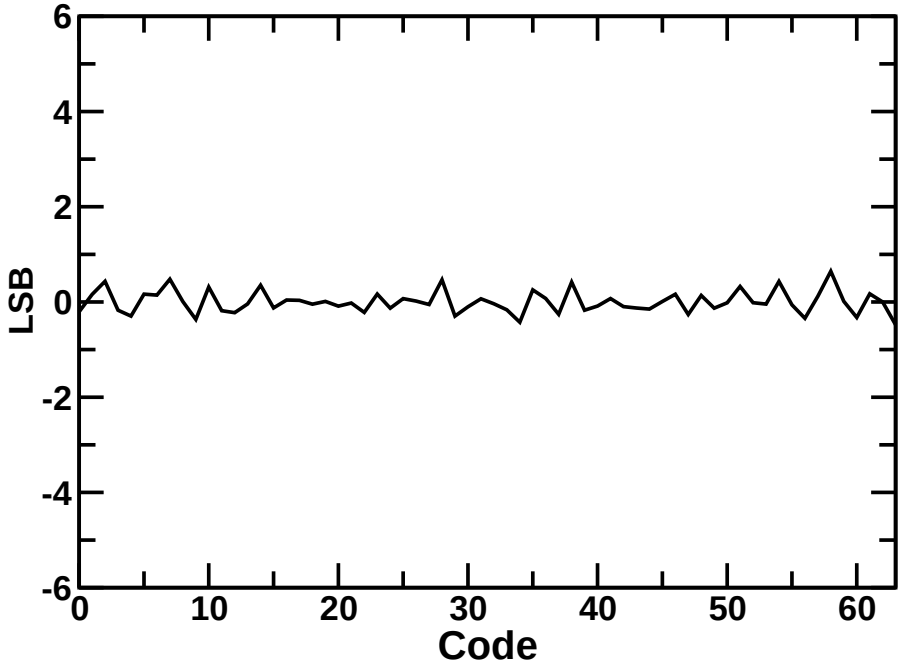



Figure 4.19: Measurement setup

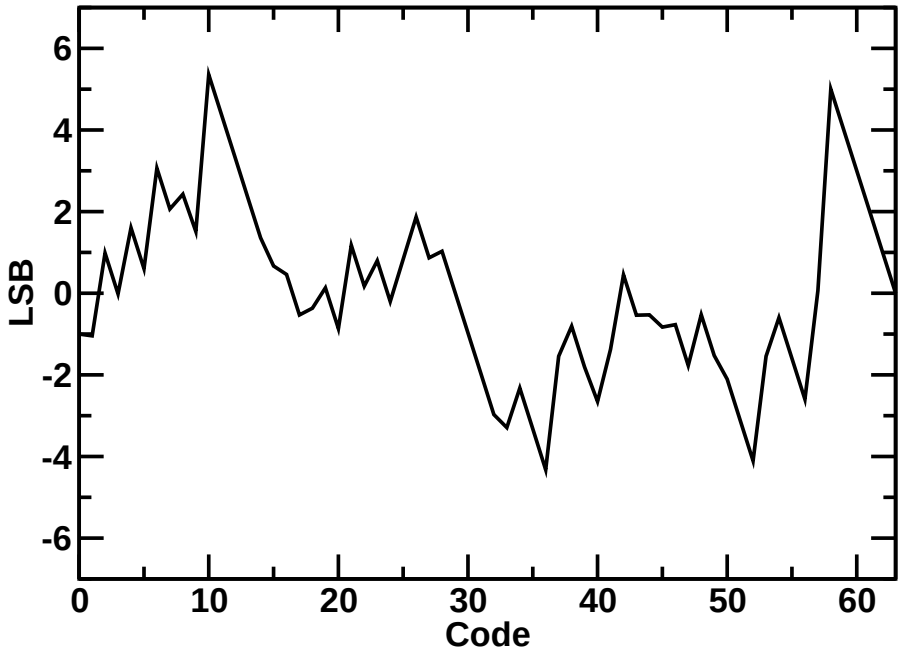



(a)

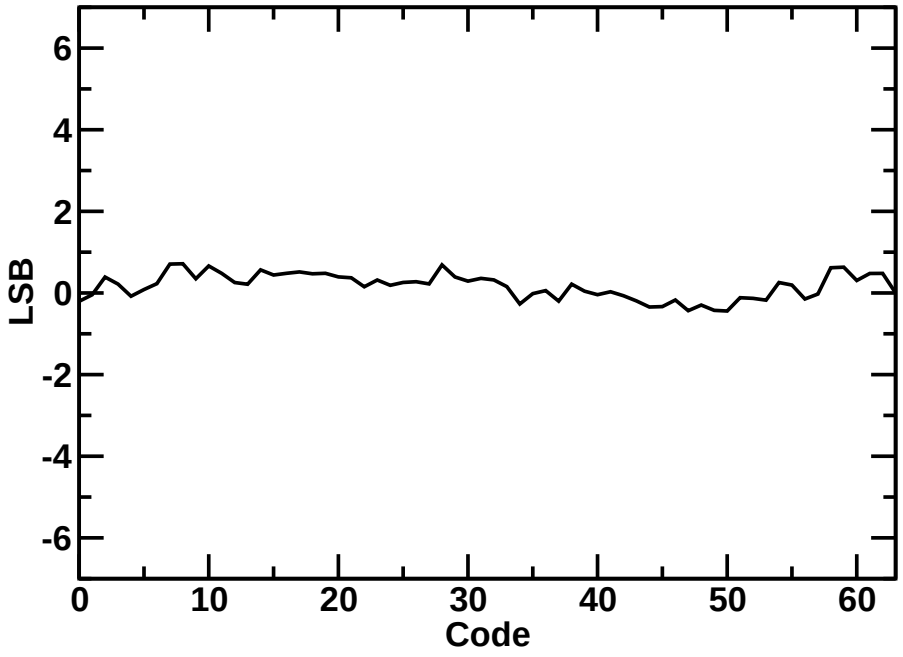



(b)

Figure 4.20: Measured DNL: (a) without calibration; (b) with calibration.




(a)




(b)

Figure 4.21: Measured INL: (a) without calibration; (b) with calibration.

### 4.6.2 Measurement Results

With the nominal supply voltage 1.2V, this ADC consumes 31mW at a maximum conversion rate 1.6GS/s. With supply voltage raised to 1.5V, this ADC consumes 54mW at a maximum conversion rate 2.1GS/s. The performance degrade with the nominal supply voltage is mainly due to the nonlinearity of sample-and-hold stage and the comparator metastability. The following measurements are under 1.5V supply voltage.

The measured DNL is shown in Fig. 4.20. Without calibration, the ADC exhibits DNL as large as +4.9/-1.0 LSB. There are also many missing codes. With calibration, the DNL is improved to -0.5/+0.6 LSB.

The measured INL is shown in Fig. 4.21. Without calibration, the INL is +5.4/-4.3 LSB. With calibration, the INL is improved to -0.4/+0.7 LSB.

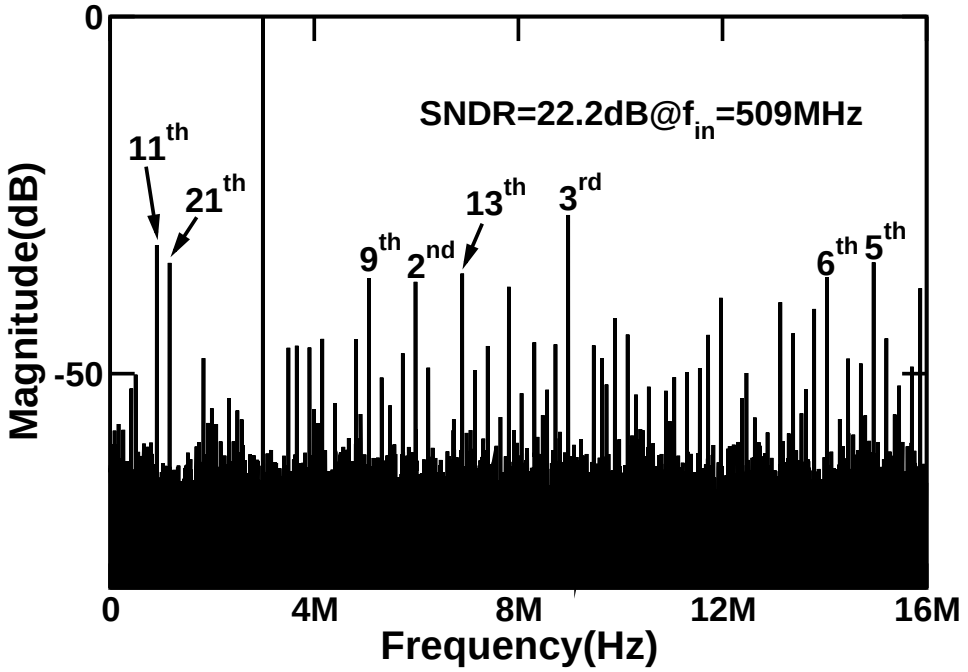
The plots of DNL and INL manifest the effectiveness of the background offset calibration.

Fig. 4.22 is the spectrum performance of the ADC with the input frequency 509MHz. Without calibration, lots of harmonic tones is present in the spectrum. The SNDR is 22.2dB in this case. This inferior performance is mainly caused by large comparator offset voltages.

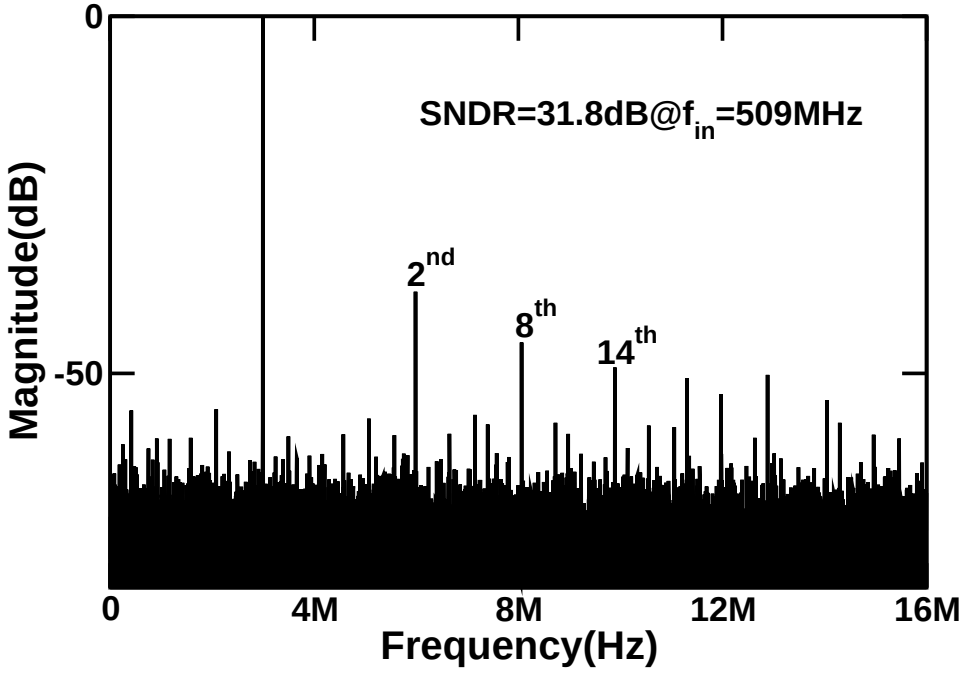
As the calibration is turned on, the SNDR is improved to 31.8dB. Most odd-order harmonic tones are removed due to the improvement on linearity. Some even-order tones are still present. These even-order tones are caused by the mismatch over the two sample-and-hold stages used in the differential signal path. The mismatch includes the layout asymmetry in both the switches and the capacitors that introduce imbalanced impedance matching condition in the differential path. The deviation of the impedance matching may cause both magnitude difference and phase difference on the differential signals, which is equivalent to an additive common-mode signal in the input port that introduce even-order harmonic tones.

Other asymmetry characteristics such as gradient variation over the resistor string, comparator kickback noise, signal source and power splitter nonlinearity may also have minor contribution on the even-order distortion.

Fig. 4.23 is the plot of SNDR versus the input frequency. The SNDR is flat up to




(a)




(b)

Figure 4.22: Spectrum performance of the implemented ADC: (a) without calibration; (b) with calibration.

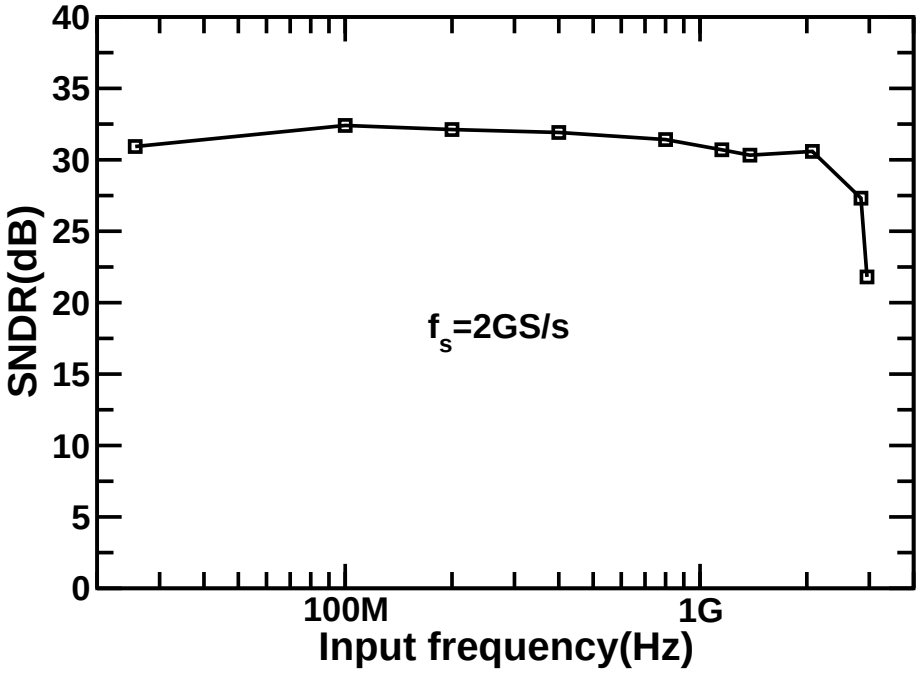



Figure 4.23: SNDR versus input signal frequency.

about 3GHz, which is far beyond Nyquist frequency. The wide bandwidth manifests the possibility of time-interleaving application for this ADC circuit. The drop of the SNDR over 3GHz is due to the bandwidth limit and the nonlinearity on the sample-and-hold stage.

The SNDR versus sampling rate is shown in Fig. 4.24. In this plot, the input signal is 61MHz. The SNDR remains beyond 30dB up to 2.1GS/s.

With the definition

$$\text{Figure-of-Merit} = \frac{\text{Power}}{2^{\text{ENOB}} \times 2 \times \text{ERBW}} \tag{4.3}$$

the FOM of this ADC circuit is 0.93 pJ/conversion-step.

The performance summary is listed in Table 4.2. Selected publications of high-speed ADC are also listed in Table 4.2 for comparison. Of these publications, this work has the best figure-of-merit.

Table 4.2: Performance summary and comparison.

| Publication | JSSC 2005 | ISSCC 2006 | JSSC 2008 | This work | This work |
|---|---|---|---|---|---|
| Author | Sandner et al. | Figueiredo et al. | Ismail et al. | Huang & Wu | Huang & Wu |
| Tech. scale | 130 nm | 90 nm | 130 nm | 65 nm(LP) | 65 nm(LP) |
| $V_{dd}$ | 1.5 V | 1.2 V | 1.5 V | 1.2V | 1.5 V |
| Input Swing | 1 $V_{PP}$ | N.A. | N.A. | 0.8 $V_{PP}$ | 0.8 $V_{PP}$ |
| $f_s$ | 1.2 GS/s | 1.0 GS/s | 1.6 GS/s | 1.6 GS/s | 2.0 GS/s |
| DNL | 0.4 LSB | N.A. | 0.42 LSB | 0.53 LSB | 0.6 LSB |
| INL | 0.6 LSB | N.A. | 0.49 LSB | 0.82 LSB | 0.7 LSB |
| SNDR | 36.1 dB | 33.7 dB | 34.5 dB | 30.7 dB | 31.0 dB |
| ERBW | ≥ Nyquist | ≥ Nyquist | ≥ Nyquist | ≥ Nyquist | ≥ Nyquist |
| Power | 160 mW | 55 mW | 180 mW | 31 mW | 54 mW |
| Area | 0.12 $mm^2$ | 0.13 $mm^2$ | 0.42 $mm^2$ | 0.14 $mm^2$ | 0.14 $mm^2$ |
| FOM(/conv.-step) | 2.2 pJ | 1.4 pJ | 2.6 pJ | 0.70 pJ | 0.93 pJ |

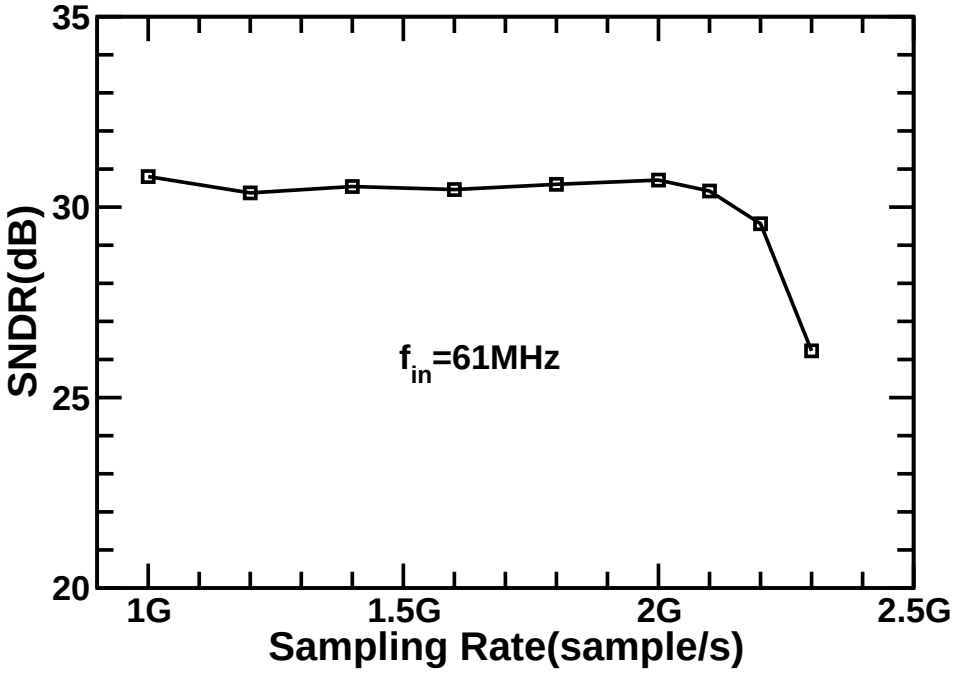



Figure 4.24: SNDR versus sampling rate.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# Chapter 5

# Conclusions

## 5.1 Conclusions

Compared with conventional resolution enhancement techniques such as input-offset storage and spatial averaging, background offset calibration for a comparator is superior in power efficiency. Preamplification-free comparator without any DC bias current is realizable using background offset calibration technique.

In the calibration loop, two design parameters, $\Delta V$ and $N_C$, effect the calibration transient behavior and the offset fluctuation. A first order approximation with the two parameters is developed to predict the calibration convergence speed. Stochastic analysis and system-level simulation ensure the standard deviation of the fluctuation noise keeping below quantization noise at proper selection of the parameters.

To apply the background-calibrated comparator to a flash ADC, input windowing technique can drastically reduce the fluctuation noise. Using input windowing technique, a small amount of fluctuation noise with standard deviation equal to 0.13 LSB is achieved at reasonable parameter values $\Delta V$=1/4 LSB and $N_C$=16.

A 6-bit 2GS/s flash ADC with proposed background comparator calibration is implemented using 65nm low-power CMOS technology. Without calibration, the DNL, INL and SNDR of the ADC are 4.9 LSB, 5.4 LSB and 20.4dB respectively. With calibration, these performance factors are improved to 0.6 LSB, 0.7 LSB and 31.0dB. The effective resolution bandwidth of this ADC extends far beyond the Nyquist frequency, and thus is

suitable for time-interleaving applications. The circuit consumes 54mW from a power supply of 1.5V and occupies 0.21×0.66mm$^2$. The figure of merit is 0.93pJ/conversion-step.

## 5.2 Recommendations for Future Works

The offset control mechanism for offset-variable comparator used in background calibration may be reinvent as a smaller and simpler one. This improvement is worth not only because of the reduction in circuit area, but also because the shrinkage in transistor sizes and wiring parasitics can effectively boost the conversion speed.

The nonlinearity and bandwidth limitation of the implemented ADC is mainly caused by the poor performance of P-type switches in the sample-and-hold stage. Bootstrapped N-type switches can improve the sample-and-hold stage linearity and bandwidth, thus enhance the ADC performance.

Interaction of the parallel connected comparators due to kickback noise is reduced in our design because the background calibration allow the use of a small-size input devices. This is confirmed in the simulation phase with the help of design tools. Nonetheless, a mathematical model for the effect of kickback noise on circuit linearity and speed can further push the performance of the ADC.

A better methodology to estimate the comparator offset voltage, including simulation techniques, mismatch modeling and layout extraction may help to lessen the design margins and improve the DNL of the ADC.

# Appendix A

# Mathematical Model for Offset Fluctuation

## A.1 Formation of $\mathbf{V_{OS}}$

The appendix describes a mathematical analysis for fluctuation noise estimation as the calibration converges. This analysis is based on the stochastic behavior of $V_{OS}$ in a single BCC.

$V_{OS}$ varies over a set of discrete values and forms a random variable $\mathbf{V_{OS}}$, which can be expanded as a discrete random sequence $\mathbf{V_{OS}}[k]$ along time axis. Fig. A.1 shows $\mathbf{V_{OS}}[k]$ versus the time index $k$.

Possible values for $\mathbf{V_{OS}}[k]$ is denoted as $V_{OS}^{m}$ with m=0, ±1, ±2...etc. The subscript j denotes the $j^{th}$BCC. In steady state, the calibration noise can be estimated from the probability mass function(PMF) of $\mathbf{V_{OS}}[k]$ as $k \rightarrow \infty$.

To calculate the PMF of $\mathbf{V_{OS}}[k]$ for each $k$, it is essential to resolve the analytical relation between $\mathbf{V_{OS}}[k]$ and $\mathbf{V_{OS}}[k-1]$. According to the configuration of the calibration loop, $\mathbf{V_{OS}}[k]$ is related to $\mathbf{S}[k]$ and the subsequent accumulated $\mathbf{T}[k]$. $\mathbf{S}[k]$ is decided by $\mathbf{R}[k]$, and $\mathbf{R}[k]$ is decided by $\mathbf{V_{OS}}[k-1]$ and the input signal distribution. $\mathbf{R}[k]$, $\mathbf{S}[k]$ and $\mathbf{T}[k]$ stand for the possible values of $R$, $S$ and $T$ in Fig. 2.7. They are all random sequences.

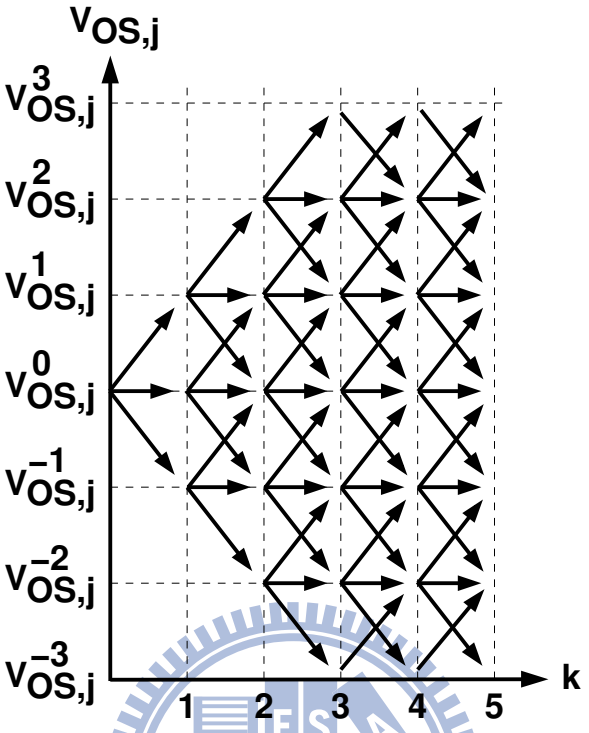


Figure A.1: $V_{OS}$ extended as an irregular random sequence.

## A.2 $\mathbf{V_{OS}}[k]$ Dependence on $\mathbf{T}[k]$ and $\mathbf{S}[k]$

The relation between $\mathbf{V_{OS}}[k]$, $\mathbf{T}[k]$ and $\mathbf{S}[k]$ is straightforwards and can be expressed as:

$$\mathbf{V_{OS}}[k] = \mathbf{V_{OS}}[k-1] + \mathbf{S}[k] \times \Delta V = \mathbf{V_{OS}}[0] + \mathbf{T}[k] \times \Delta V \tag{A.1}$$

where $\mathbf{S}[k] \in \{-1, 0, +1\}$, and $\mathbf{T}[k]$ is the accumulation of $\mathbf{S}[k]$.

## A.3 $\mathbf{R}[k]$ dependence on $\mathbf{V_{OS}}[k-1]$

On the other hand, $R[k] \in \{-1, 0, +1\}$ is the result of a multinomial trial. Its PMF can be calculated from $P$ and $\Delta P$ that describe the input probabilistic distribution as illustrated in Fig. 2.2. $P$ and $\Delta P$ are directly related to the preceding offset value $V_{OS}[k-1]$. Since

the probability for $q = +1$ and $q = -1$ are equally 1/2, we have

$$\begin{aligned} P(\mathbf{R}[k] = +1) &= \frac{1}{2}P \\ P(\mathbf{R}[k] = -1) &= \frac{1}{2}P + \frac{1}{2}\Delta P \\ P(\mathbf{R}[k] = 0) &= 1 - P(\mathbf{R}[k] = +1) - P(\mathbf{R}[k] = -1) = 1 - P - \frac{1}{2}\Delta P \end{aligned} \tag{A.2}$$

where $P(\mathbf{R}[k])$ denotes the PMF of $\mathbf{R}[k]$. $\mathbf{R}[k] = 0$ does not effect the value of $\mathbf{S}$, thus the value of $P(\mathbf{R}[k] = 0)$ has no influence on $P(\mathbf{V_{OS}})$. Only the conditional probability $P_c(\mathbf{R}[k])$, which stands for the condition $\mathbf{R}[k] = \pm 1$, needs to be considered. From (A.2), $P_c(\mathbf{R}[k])$ can be expressed as:

$$\begin{aligned} P_c(\mathbf{R}[k] = -1) &= \frac{P}{2P + \Delta P} = \frac{1}{2 + \Delta P/P} \\ P_c(\mathbf{R}[k] = +1) &= \frac{P + \Delta P}{2P + \Delta P} = \frac{1 + \Delta P/P}{2 + \Delta P/P} \end{aligned} \tag{A.3}$$

Notably, the $P_c(\mathbf{R}[k])$ is a function of the $\Delta P/P$ ratio only.

## A.4 Steady-State Approach for $\mathbf{V_{OS}}[k]$

The left analytical relation is the $\mathbf{S}[k]$ dependence on $\mathbf{R}[k]$. Due to the nonlinear behavior of AAR, a steady-state approach is used to resolve it and hence the relation of $\mathbf{V_{OS}}[k]$ and $\mathbf{V_{OS}}[k-1]$.

Fig. A.2 shows the dynamics of $\mathbf{V_{OS}}[k]$ in steady state. Under the condition in which $\mathbf{V_{OS}}[k] = V_{OS}^m$, the conditional probabilities for $S = -1$, $S = 0$ and $S = +1$ are defined as $P_d^m[k]$, $P_s^m[k]$, and $P_u^m[k]$ respectively. They are named transfer probabilities for convenience. The subscript 'd', 's', and 'u' denote 'downward', 'stationary' and 'upward' respectively. When the calibration converges, $P(\mathbf{V_{OS}}[k])$ becomes time invariant. This leads to the following steady-state properties of the transfer probabilities:

1. *Equality*. The probability for $V_{OS}$ moving upward from $V_{OS}^m$ to $V_{OS}^{m+1}$ is the same as that moving downward from $V_{OS}^{m+1}$ to $V_{OS}^m$.

2. *Conservation*. The probability for $V_{OS}$ moving out of $V_{OS}^m$ is the same as that moving into $V_{OS}^m$.

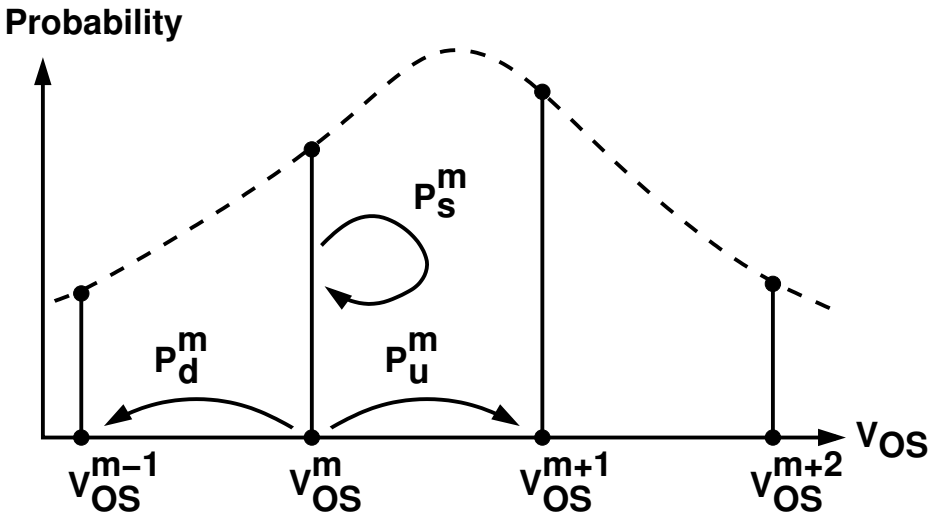


Figure A.2: Steady-state transfer probabilities at $V_{OS}^m$.

3. *Invariance*. Probabilities in the above properties remain constant over $k$.

The third property implies that the conditional transfer probabilities $P_d^m[k]$, $P_s^m[k]$, and $P_u^m[k]$ are also constant over $k$.

Observing that the behavior of $V_{OS}[k]$ depends on the value of $S$, and even the same $S$ value may come from different historically accumulated $R$, we decompose the transfer probabilities into historically-unified fractional terms, $\hat{P}_s^m[i]$, $\hat{P}_u^m[i]$, and $\hat{P}_d^m[i]$, which account for the same move-in-and-stay probability fractions for $V_{OS}$. Fig. A.3 represents the definition of them.

These historically-unified fractional terms are defined as follows: after a time period of $i$ cycles for which $V_{OS}$ remains at $V_{OS}^m$ (i.e., $S$=0), $\hat{P}_d^m[i]$, $\hat{P}_s^m[i]$ and $\hat{P}_u^m[i]$ are defined as the probabilities of $S=-1$, $S=0$ and $S=+1$ at $i+1^{th}$ cycle. Note that this definition excludes the probability of $V_{OS}$ moving into $V_{OS}^m$ from $V_{OS}^{m+1}$ or $V_{OS}^{m-1}$ in this time period. The transfer probabilities illustrated in Fig. A.2 can thus be expressed as:

$$\begin{aligned} P_s^m &= P_0^m \sum_{i=0}^{\infty} \hat{P}_s^m[i] \\ P_u^m &= P_0^m \sum_{i=0}^{\infty} \hat{P}_u^m[i] \\ P_d^m &= P_0^m \sum_{i=0}^{\infty} \hat{P}_d^m[i] \end{aligned} \tag{A.4}$$

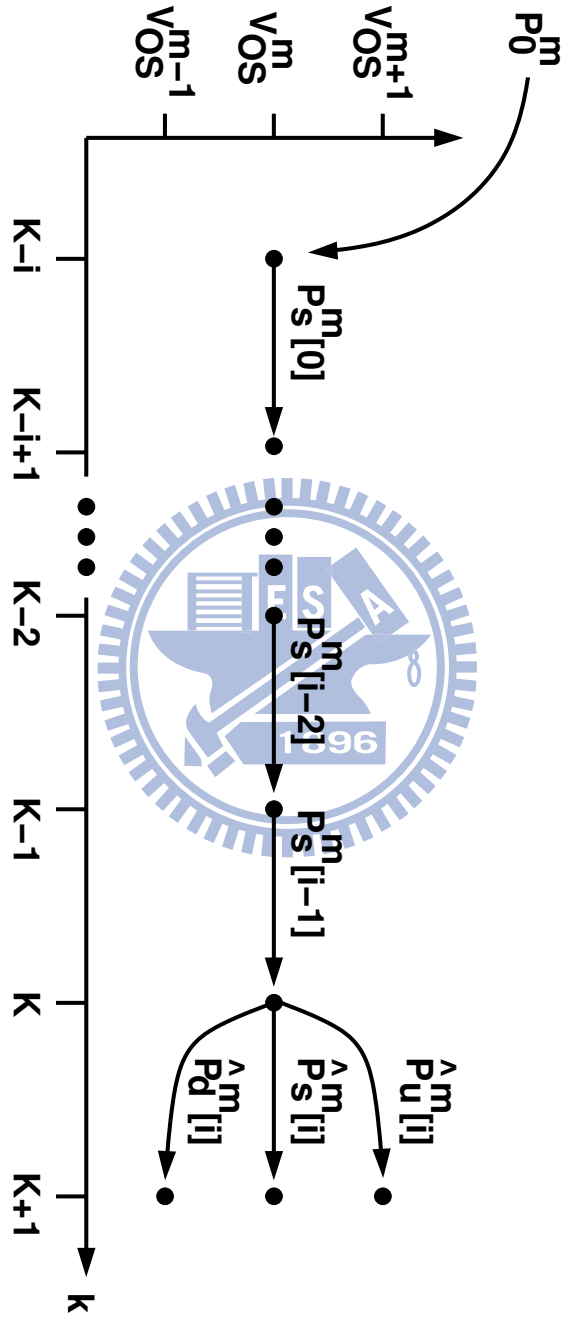


Figure A.3: Historically-unified fractional term for transfer probability.

where $P_0^m$ is a constant probability for $V_{OS}$ moving into $V_{OS}^m$ in the initial.

The $\hat{P}^m[i]$ terms in the right-hand side of (A.4) can be calculated by considering all possible conditions for $S$, and are expressed as:

$$\begin{aligned}
\hat{P}_s^m[i] &= \sum_{-N_C \le S_i^m \le +N_C} P(\mathbf{S}_i^m) \\
\hat{P}_u^m[i] &= P(\mathbf{S}_i^m)\Big|_{S_i^m=+(N_C+1)} \\
\hat{P}_d^m[i] &= P(\mathbf{S}_i^m)\Big|_{S_i^m=-(N_C+1)}
\end{aligned} \tag{A.5}$$

where $\mathbf{S}_i^m$ denotes the random variable corresponding to $S$ after $V_{OS} = V_{OS}^m$ for consecutive $i$ cycles. Its PMF can be calculated by using the following recursive function [46]:

$$P(\mathbf{S}_i^m) = \left[P(\mathbf{S}_{i-1}^m) \times W(\mathbf{S}_{i-1}^m)\right] * P_c(\mathbf{R}^m) \tag{A.6}$$

where $P_c(\mathbf{R}^m)$ is defined in (A.3) with superscript $m$ denoting $\mathbf{V_{OS}} = V_{OS}^m$. Note that $P(\mathbf{S}_0^m) = P_c(\mathbf{R}^m)$ for $i = 0$. The operator "$*$" is the probability convolution over the random variable. $W(S)$ is a window function which has the value 1 if $|S| \le N_c$ and 0 otherwise. Multiplication by $W(S)$ is to exclude the probability of $\mathbf{V_{OS}}$ moving out of $V_{OS}^m$.

From Equation (A.4), (A.5), and (A.6), we can calculate the transfer probabilities $P_s^m$, $P_u^m$, and $P_d^m$. They are all proportional to $P_0^m$. The value of $P_0^m$ can be found by letting the summation of $P_s^m$, $P_u^m$, and $P_d^m$ to be 1. The values of $\hat{P}_s^m[i]$, $\hat{P}_u^m[i]$, and $\hat{P}_d^m[i]$ converge to zero at large $i$, and the convergence of the infinite series in (A.4) is also confirmed by numerical methods. Thus, the transfer probabilities, $P_s^m$, $P_u^m$ and $P_d^m$, can be calculated to any specific precision with the help of computer.

## A.5 A Finite-State Markov Chain Reformation

$P_s^m$, $P_u^m$, and $P_d^m$ depend on $m$ only, thus the $\mathbf{V_{OS}}[k]$ forms a finite-state Markov chain. According to the steady-state property 2, the probability of $V_{OS}$ moving from $V_{OS}^m$ to $V_{OS}^{m+1}$ is the same as it moving in the opposite direction, i.e.,

$$P(\mathbf{V_{OS}} = V_{OS}^m) \times P_u^m = P(\mathbf{V_{OS}} = V_{OS}^{m+1}) \times P_d^{m+1} \tag{A.7}$$

Thus, we have

$$\frac{P(\mathbf{V_{OS}} = V_{OS}^{m})}{P(\mathbf{V_{OS}} = V_{OS}^{m+1})} = \frac{P_d^{m+1}}{P_u^m} \tag{A.8}$$

The above equation can be used to calculate $P(\mathbf{V_{OS}})$, since it states the relative ratio for all probability bins. The absolute values of $P(\mathbf{V_{OS}})$ can be found by the fact that integration of $P(\mathbf{V_{OS}})$ over all $\mathbf{V_{OS}}$ is equal to 1.

An example of calculated $P(\mathbf{V_{OS}})$ is illustrated in Fig. 2.11. Also shown in Fig. 2.11 is the results from simulation using identical design parameters. The simulation result is the normalized histogram of $10^8$ samples. Good agreement is demonstrated between the estimation and simulation.


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# Publication List

- Journal Paper:
  - **Chun-Cheng Huang** and Jieh-Tsorng Wu, "A Background Comparator Calibration Technique for Flash Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 9, pp. 1732–1740, September 2005.
- Conference Paper:
  - **Chun-Cheng Huang** and Jieh-Tsorng Wu, "A Statistical Background Calibration Technique for Flash Analog-to-digital Converters," *Proceedings of the 2004 International Symposium on Circuits and Systems Vol.1*, May 2004, pp.I-125–I-128.
- Patent:
  - **Chun-Cheng Huang** and Jieh-Tsorng Wu, "Background Comparator Calibration Technique for Flash Analog-to-Digital Converters," US patent no. 7,064,693.